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Analysis and design of an 80 Gbit/sec clock and data recovery prototype

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This thesis is dedicated to my friends and family.

A Jean-Baptiste et Olivier,
à l'équipe Conception de Circuits,
à l'équipe Circuits et Systèmes Hyperfréquences.

Contents

Chapter 1 Introduction 19

Chapter 2 Clock and Data Recovery 21

2.1 Serial data communication 21

2.2 Data modulation 24

2.3 CDR overview 30

2.4 Open loop CDR 31

2.5 Phase detector 33

2.6 Charge pump 39

2.7 Jitter 40

2.8 ILO based CDR 42

2.9 High speed PLL and CDR 43

Chapter 3 Critical building blocks 48

3.1 Injection locked oscillator 48

3.2 Proposed phase detector 62

3.3 Stability of the ILO based CDR 65

3.4 SiGe technology: BiCMOS9mW 70

Chapter 4 CDR design and measurements 81

4.1 Cell based design 81

4.2 Data buffer 83

4.3 Injection Locked Oscillator 85

4.4 Pulses generator 92

4.5 D-Flip Flop 93

4.6 Phase comparator 95

4.7 Clock buffer 97

4.8 Multiplexer and demultiplexer chain 98

4.9 Chip measurements 103
4.10 Phase comparator measurement 108
4.11 New chip design 110
4.12 Razrabotka mesurements 113
4.13 Conclusions 118
Chapter 5 Conclusions 119
References: 129

List of Figures:

Figure 1: Photonics Electronics Integration on CMOS: CEA-LETI, MINATEC Campus Grenoble (F) ESSCIRC 2011 22
Figure 2: Communication channel 23
Figure 3: Serial link functional diagram 24
Figure 4: Spectrum for random data with NRZ and bipolar coding 25
Figure 5: Line coding example 26
Figure 6: Insertion losses of a 20 mil, 50 Ohms TL over different substrates [10] 27
Figure 7: Intel light peak cable 28
Figure 8: Bit stream of a 2.5 Gbps signal vs. pre-emphasis 29
Figure 9: Eye diagram with pre-emphasis implementation 29
Figure 10: Optimal sample point 30
Figure 11: PLL based clock and data recovery architecture 31
Figure 12: Open loop CDR architecture 31
Figure 13: Gated oscillator 32
Figure 14: Gated CDR waveforms 32
Figure 15: Gated oscillator-based CDR 33
Figure 16: Linear and binary phase detector behavior 34
Figure 17: XOR transfer function 34
Figure 18: Hogge phase detector schematic (a) and transfer function (b) 35
Figure 19: Hogge detector waveform 35
Figure 20: Delay compensation for the Hogge phase detector 36
Figure 21: CDR with a D-FF as phase detector 37
Figure 22: Alexander phase detector architecture. 37
Figure 23: Operation of the Alexander phase detector 38
Figure 24: Basic architecture of a charge pump 39
Figure 25: Single ended charge pump with NMOS switches 39
Figure 26: Differential charge pump 40
Figure 27: Jitter categories 41
Figure 28: SONET 10Gb eye mask 42
Figure 29: Injection locked CDR architecture 42
Figure 30: CDR architecture based on PLL architecture 43
Figure 31: Optimized latch 46
Figure 32: Half rate phase detector 46

Figure 33: Synchronization of an oscillator during time 48
Figure 34: Huntoon and Weiss model 49
Figure 35: Cross-coupled oscillator 53
Figure 36: LC equivalent small signal model 53
Figure 37: Duty cycle determination 56
Figure 38: ILO schematic 58
Figure 39: Output frequencies of the ILO and the macromodel for 1 mA injection 58
Figure 40: Output frequencies of the ILO and the macromodel for 2 mA injection 59
Figure 41: Phase position: lead, lag or in phase 59
Figure 42: RF line with injection 60
Figure 43: Active injection topologies 61
Figure 44: CDR architecture 62
Figure 45: Pulses generator 62
Figure 46: Windowed phase comparator 63
Figure 47: Proposed phase comparator chronogram 64
Figure 48: Gain of linear, binary and proposed phase detector 65
Figure 49: PLL representation 66
Figure 50: PLL with injection representation 67
Figure 51: Synchronization on 2f0-fi 67
Figure 52: Bode diagram in open loop for $f_{aux}>0$ 69
Figure 53: PLL stability 70
Figure 54: Sum of 1st, 3rd and 5th harmonics approximates square wave. 71
Figure 55: Bipolar transistor operating region 72
Figure 56: HBT SiGe from STMicroelectronics 72
Figure 57: HBT small signal schematic 73
Figure 58: f_t and f_{max} for several transistors 74
Figure 59: ft and fmax variation regardless of the number of emitter, base and collector 74
Figure 60: Three available HBT configuration 75
Figure 61: Temperature effect on ft 75
Figure 62: HBT with its access 76
Figure 63: Metal layer on different technologies 76
Figure 64: BiCMOS9mW microstrip line 77
Figure 65: Electromagnetic field of a microstrip line on HFSS 77
Figure 66: Skin effect for a metal wire 78

Figure 67: S11 and S21 parameters for a 100µ*12µm microstrip line 78
Figure 68: MIM capacitance 79
Figure 69: Quality factor improvement 79
Figure 70: S11 parameter of the RF plot 79
Figure 71: Cell based array 81
Figure 72: Impedance of common circuits 82
Figure 73: Low pass filter effect on data 82
Figure 74: Shielded control line 83
Figure 75: Data buffer schematic 84
Figure 76: Buffer bandwidth without and with interconnection 84
Figure 77: Ideal LC resonator 85
Figure 78: Serial and parallel tank losses 86
Figure 79: (a) NPN junction bipolar transistor. (b) Apply reverse bias to collector base junction 87
Figure 80: Capacitor tank tuning range 88
Figure 81: HBT transistor with 4 emitters and in CBEBC topology and varactor schematic . 88
Figure 82: Capacitor tank quality factor 89
Figure 83: Inductor value 90
Figure 84: Inductor quality factor 90
Figure 85: ILVCO schematic 91
Figure 86: ILVCO frequency range 91
Figure 87: Pulse generator architecture 92
Figure 88: XOR schematic 92
Figure 89: Pulse generator input and output spectrums 93
Figure 90: D latch 94
Figure 91: D-FF transfer function 95
Figure 92: Charge pump 96
Figure 93: Phase comparator output current 96
Figure 94: Clock buffer schematic 97
Figure 95: Nadezhda Chip photography 98
Figure 96: Measurement of 100 Gbit/s MUX and CDR&DEMUX Modules (Micram) 99
Figure 97: Demultiplexing multiplexing chain 99
Figure 98: Demultiplexer 1:2 100
Figure 99: Multiplexer 2:1 100

Figure 100: NAND gate 100
Figure 101: Clock divider 101
Figure 102: Clock tree 101
Figure 103: Demultiplexing 80:2*40GHz 102
Figure 104: Multiplexing 20 GHz to 40 GHz 102
Figure 105: Input and output of the demultiplexing/multiplexing chain 103
Figure 106: Buffer oscillation 104
Figure 107: Oscillator maximum frequency 105
Figure 108: Synchronized ILO spectrum 106
Figure 109: ILO and synchronization signal phase noise (4th harmonic) 107
Figure 110: ILO and synchronization signal phase noise (2nd harmonic) 108
Figure 111: Phase comparator photography 109
Figure 112: Output of the phase comparator 109
Figure 113: Transistor access 110
Figure 114: Clock buffer 111
Figure 115: ILVCO and clock buffer second version layout 112
Figure 116: Nadezhda ILVCO and buffer 112
Figure 117: Loop control voltage 113
Figure 118: VCO tuning range 114
Figure 119: ILVCO phase noise, synchronized on fourth harmonic 115
Figure 120: ILVCO spectrum, (a) with injection, (b) without injection 115
Figure 121: CDR ILVCO output spectrum at 96.8 GHz 116
Figure 122: Jitter RMS with input data at 24.9 GHZ 117
Figure 123: Jitter RMS with input data at 12.2 GHz 117
Figure 124: Second chip layout 120

Abstract:

The increasing bandwidth demand for telecommunication leads to an important rise of serial link operating frequencies. This demand is also present in embedded systems with the growth of devices and peripherals performances. To ensure the data stream is well recovered, a clock and data recovery (CDR) circuit is placed before any logical blocks on the receiver side. The research activities presented in this thesis are related to the design of such a CDR. The phase detector plays a critical role in the CDR circuit and is specially studied. This thesis presents a phase comparator that provides an enhancement by introducing a windowed mode and reducing its operating frequency. The used CDR has a special topology, which is described, and the injection locked oscillator theory is explained. Most of the research of this study has focused on the design and layout of an 80 Gbps CDR. Several prototypes are realized in 130 nm SiGe process from STMicroelectronics.

Keywords: Clock & data recovery, injection locked oscillator, ILO, CDR, PLL

Résumé:

La demande croissante de toujours plus de débit pour les télécommunications entraine une augmentation de la fréquence de fonctionnement des liaisons séries. Cette demande se retrouve aussi dans les systèmes embarqués du fait de l'augmentation des performances des composants et périphériques. Afin de s'assurer que le train de données est bien réceptionné, un circuit de restitution d'horloge et de données est placé avant tout traitement du coté du récepteur. Dans ce contexte, les activités de recherche présentées dans cette thèse se concentrent sur la conception d'une CDR (Clock and Data Recovery). Nous détaillerons le comparateur de phase qui joue un rôle critique dans un tel système. Cette thèse présente un comparateur de phase ayant comme avantage d'avoir une mode de fenêtrage et une fréquence de fonctionnement réduite. La topologie spéciale utilisée pour la CDR est décrite, et la théorie relative aux oscillateurs verrouillés en injection est expliquée. L'essentiel du travail de recherche s'est concentrée sur la conception et le layout d'une restitution d'horloge dans le domaine millimétrique, à 80 Gbps. Pour cela plusieurs prototypes ont été réalisés en technologie BiCMOS 130 nm de STMicroelectronics.

Mots clé: Restitution d'horloge et de données, oscillateur verrouillé en injection, ILO, CDR, PLL

Résumé étendu:

De nos jours, pour le transfert de données, les liaisons numériques rapides (LNR) sont nécessaires dans les charges utiles d'observation, où plusieurs liaisons ont été réalisées/qualifiées pour le CNES. Comme le montre la réalisation de deux ASIC à 200 Mbit/sec pour Spot 5 / Hélios 2 (LNR1 chez SEXTANT Avionique, LHD chez ALCATEL Espace), la qualification d'un composant commercial (COTS) pour Pléiades utilisé à 600 Mbit/sec, l'analyse en cours pour CSO entre la qualification d'un COTS et la réalisation d'un ASIC à plusieurs Gbit/sec.

Les charges utiles de télécommunication nécessitent également ce type de liaisons (plusieurs Gbit/sec se concentrent au cœur de telles charges utiles commutant des réseaux multimédias). La prochaine génération de LNR nécessitera donc un débit au delà de 10 Gbits/sec.

Par ailleurs, la problématique des liaisons rapides est qu'il s'agit du premier composant à être livré en modèle de vol aux équipementiers spatiaux. Par conséquent, l'innovation dans ce domaine doit être anticipée car le temps de développement alloué à ces liaisons dans le cycle réalisation d'un projet spatial est relativement court.

Le spatial a accumulé un vécu sur ces liaisons depuis trois générations. En particulier, l'extraction d'horloge du récepteur – cœur des LNR – a évolué : initialement basée sur un PLL ("Phase-Locked Loop", boucle à verrouillage de phase). Un travail innovant a été entrepris par IMS Bordeaux / Thales Alenia Space / CNES et a permis de breveter un système nouveau basé sur un ILO ("Injection-Locked Oscillator", oscillateur verrouillé en injection). Ces brevets permettent à la communauté spatiale d'envisager la réalisation d'un ASIC en contournant une grande partie de la criticité de développer un PLL à haute fréquence.

Cette thèse se concentre sur l'étude et le développement d'une CDR (Clock and Data Recovery - bloc de restitution d'horloge et de donnée) pour une liaison série à 80 Gb/s.

Une description des liaisons série est abordée dans le Chapter 2 afin de mieux comprendre les contraintes auxquelles nous allons faire face. Les données binaires sont converties en tension électrique dont le niveau DC représente l'information : c'est l'opération de codage.

Le codage retenu pour les données sera de type NRZ (Non Retour à Zéro) afin de diminuer la bande passante tout en maintenant le même débit, contrairement à un codage différent. Dans le cas de notre étude, les données NRZ seront considérées comme déjà encodées. Un

encodage permet d'augmenter la densité de transition en choisissant dans une table d'encodage des mots binaires plus long. Ceci permet d'éviter des problèmes de désynchronisation.
Une fois les données codées et encodées, elles sont émises à travers un médium (un câble de cuivre par exemple). Après un trajet dans un câble, les données peuvent être altérées par les pertes dans le câble. Les pertes sont dépendantes de la longueur du câble et de la fréquence des données. Du coté du récepteur (Figure 3), afin de savoir si les données reçues sont un "zéro" ou un "un", il faut les ré-échantillonner là où le taux d'erreur binaire est le plus petit, i.e. au milieu du diagramme de l'œil (Figure 10).
Il faut donc avoir un signal d'horloge parfaitement en phase avec les données reçues pour toujours échantillonner au bon instant. Un aperçu des différentes topologies de CDR utilisées suivra (2.3), montrant les CDR à boucles fermées et à boucles ouvertes (2.4). Les différents blocs compris dans ces CDR tels que les comparateurs de phase (2.5), les pompes de charges (2.6) permettrons de voir l'intérêt de la solution retenue (2.8), à savoir un oscillateur verrouillé en injection intégré dans une boucle fermée.
La boucle fermée va asservir la fréquence centrale de l'oscillateur qui va pouvoir recopier la phase du signal injecté (les données ici) afin de pouvoir ré-échantillonner les données au milieu du diagramme de l'œil. Un état de l'art des différentes PLL et CDR fonctionnant autour de 100 GHz sera enfin présenté (2.9).
Afin de bien maitriser la structure employée, nous verrons dans le Chapitre 3 le comportement théorique d'un ILO (3.1), en utilisant la théorie d'Huntoon et Weiss. Un oscillateur verrouillé en injection est un vieux phénomène, découvert au 17éme siècle par Huygens. Facilement observable en fixant deux horloges à balanciers sur une poutre et en lançant les balanciers. Petit à petit, grâce aux vibrations qui se propagent dans la poutre, les 2 balanciers vont osciller au même tempo et les 2 horloges seront ainsi verrouillées.
Nous sommes en présence d'un double phénomène: une synchronisation en fréquence (si une des 2 horloges est plus lente elle va accélérer) et en phase (les 2 balanciers vont battre en même temps). Ce même phénomène se retrouve en électronique. En injectant un signal dans un oscillateur, ce dernier va se verrouiller suivant une certaine plage de fréquence, la plage d'accrochage.
Cette plage est définie par le rapport entre la puissance injectée et la puissance de l'oscillateur sans injection (3-17) et de l'harmonique de synchronisation (3-23). Dans cette plage, suivant la fréquence injectée (inférieure, égale ou supérieure à la fréquence naturelle de l'oscillateur), la phase du signal en sortie sera en avance, en phase ou en retard de phase par rapport au signal injecté. Il est donc intéressant dans notre cas d'avoir la fréquence de notre oscillateur

identique à la fréquence injecté. Nous aurons une recopie de la phase injecté, et nous serons sûr de ré-échantillonner au milieu du diagramme de l'œil.

Une modélisation comportementale de l'oscillateur (3.1.3) en VHDL-AMS a été réalisée. Le modèle est comparé avec un ILO réalisé en 65nm CMOS au niveau schématique. Le modèle se montre fidèle à la réalité. Il permet de mieux appréhender le fonctionnement de la CDR et de faciliter les simulations haut niveau.

Les différents comparateurs de phase présentés (2.5) posent des problèmes de phase. En effet, à haute fréquence les portes logiques occupent une surface importante et imposent des contraintes dans le layout. Ces dernières font apparaitre des temps de propagations entre les différents blocs ce qui est problématique. Un nouveau comparateur de phase est proposé (3.2) afin de corriger ces problèmes.

Il compare la phase des données entrantes et des données ré-échantillonnées, ce qui permet de réduire la fréquence de travail des portes logiques le composant. De plus il possède un troisième état, lorsqu'il n'y a pas de données en entrée, aucune information d'erreur n'est envoyée à la pompe de charge. Enfin il dispose d'une fenêtre de comparaison (Figure 48). Lorsque l'erreur de phase est faible, le comparateur ne va pas modifier la fréquence de l'oscillateur. En effet dans cette zone, les données en entrée et les données ré-échantillonnées ont une fréquence très similaire, l'injection est donc dominante et il y a une recopie de la phase des données reçues par l'ILO.

Pour clôturer le chapitre 3, l'étude de stabilité de la CDR est présentée ainsi que la technologie employée (BiCMOS9mW) pour réaliser les circuits. Le transistor présentant les meilleures performances est le transistor bipolaire à hétéro jonction de 5µm de long avec deux collecteurs, deux bases et un seul collecteur.

Le chapitre 4 présente les circuits réalisés et leurs mesures. Les circuits utilisent une structure cellulaire pour simplifier les différentes entrées sorties.

Les tensions d'entrée et de sortie sont entre 1.7 et 2 V, et la logique utilisée est de type ECL. Cela nous permet d'avoir une bonne adaptation tout en travaillant sur une large gamme de fréquence. Les buffers de données (4.2) ont ainsi une bande passante de 0 à 50 GHz.

L'ILO (4.3) est de type LC à paire croisée. Les inductances sont réalisées avec des lignes microstrip (50µm*10µm) déjà optimisées par le fabricant. Le facteur de qualité des lignes est de 34.6 pour une inductance de 15.9 pH. Les varicap (capacité variables) sont quant à elles constituées de transistors bipolaires montés en diode.

La plage de variation est de 61fF à 67fF, soit 10%, et le facteur de qualité autour de 35. L'injection est réalisée par des transistors placés sous ceux de la paire croisée (Figure 85). Une

tension externe (Vilo) permet de gérer la puissance de l'injection en jouant sur la polarisation des transistors M4 et M3. L'oscillateur oscille de 81.1 GHz à 77.5 GHz. Le générateur d'impulsions (4.4) est destiné à améliorer la plage d'accrochage de l'ILO.

En effet les données étant aux mieux à 50 GHz, la plage d'accrochage se trouve réduite, car la synchronisation s'effectue sur l'harmonique 2. Afin d'étendre la plage d'accrochage, le générateur d'impulsions va doubler la fréquence du signal injecté. Il utilise pour cela la différence de temps de propagation entre les 2 entrées d'un ‘‘OU exclusif’’ (Figure 87). Cela permet de générer de la puissance à la fréquence de l'horloge de la CDR. La bascule D (D Flip Flop) (4.5) permet de ré-échantillonner les données. Elle est réalisée de manière classique (Figure 90) avec 2 mémoires D en configuration maitre-esclave.

L'utilisation de lignes microstrip en série avec les résistances de charge permet d'augmenter la fréquence de fonctionnement. Le comparateur de phase (4.6) réutilise la bascule D précitée et incorpore la pompe de charge (Figure 92) et l'interrupteur. Ne disposant pas de transistors PNP performants, des transistors CMOS sont utilisés pour réaliser les miroirs de courant. Enfin les buffers d'horloge (4.7) sont réalisés par une succession de paires différentielles à charge inductive (Figure 94). Enfin une chaine de sérialisation dé-sérialisation (4.8) a été étudiée afin de permettre de générer et mesurer les données. Néanmoins cette chaine n'a pas été intégrée dans la CDR par manque de temps.

Un premier circuit a été réalisé et mesuré au laboratoire. Il comprend la CDR entière et en plus l'ILO avec son système de synchronisation d'une part et le comparateur de phase d'autre part. Nous avons donc 3 circuits sur la puce (Figure 95) permettant de caractériser tous les blocs. Lors des mesures de l'ILO (4.9), nous avons constaté un décalage en fréquence de 12 GHz vers le bas. L'ILO oscille de 66 à 69 GHz. De plus, une oscillation parasite à 43 GHz est présente et masque l'ILO.

Après des analyses et rétro simulations, il s'est avéré que les buffers d'horloge étaient la source de l'oscillation parasite. Cependant l'oscillateur se verrouille correctement sur un signal injecté, et recopie le bruit de phase de la source suivant l'équation (4-54) (Figure 109). De plus, la plage d'accrochage varie de 200MHz à 3 GHz comme en simulation. Même si l'oscillateur fonctionne, la CDR entière ne peut être mesurée car les oscillations parasites empêchent le fonctionnement correct des bascules D. Le circuit du comparateur de phase peut cependant être caractérisé (4.10).

Ne disposant pas de baluns à haute fréquences, les mesures ont été réalisées à 18 GHz. Le comparateur de phase fonctionne exactement comme en simulation (Figure 112) et présente la fenêtre d'échantillonnage attendue.

Un deuxième circuit corrigeant les problèmes rencontrés (4.11) a été réalisé et mesuré au laboratoire.
Nous avons pu corriger le décalage en fréquence provenant d'une piste métallique non modélisée (Figure 113). Incorporer de nouveaux buffers d'horloge permettant de ne pas trop retoucher le layout (Figure 114 & Figure 115).
Le nouveau circuit, nommé Razrabotka, a été caractérisé au laboratoire (4.12). Afin d'avoir une densité de courant optimale la tension d'alimentation a dû être rehaussée à 2.3 V ce qui augmente la fréquence de fonctionnement et la consommation (650mA).
En effet, l'oscillateur couvre la plage de 97 à 102 GHz, résultats que nous retrouvons en simulations pour une telle alimentation. Le système fonctionne parfaitement, avec une bonne recopie du bruit de phase injecté (Figure 119). La CDR est capable de se verrouiller sur un signal allant de 96.4 Gb/s à 101.2 Gb/s. Les données en sortie sont propres, avec une gigue de 1.21 ps à 25 GHz (Figure 122).

Ces travaux de thèse ont permis la réalisation d'une restitution d'horloge et de donnée à 100 GHz en utilisant une combinaison d'ILO et de PLL, avec une étude théorique et la réalisation d'un modèle en VHDL-AMS de l'ILO.
Un comparateur de phase permettant de travailler à haute fréquence a été développé. Le circuit réalisé est une première étape pour la réalisation de liaison série ultra rapide à destination du domaine spatial et se situe dans l'état de l'art avec une consommation de 1.4 W et une gigue de 1.2 ps.

Chapter 1

Introduction

Serial links are used to transmit data since the beginning of telecommunication market. They allow the transfer of large quantity of information over a single link without the parallel links drawbacks such as cross-talk, limited bandwidth and high footprint. Mostly used for medium distance communication at the beginning, they are nowadays used also for longer distance and short range.

In earth observation satellites, high speed serial links allow image data transfer from the Analog to Digital converter (ADC) to the mass memory and data compression units. Recently such links became the telecommunication satellite' system core for high speed data transfer. Very fast serial link cannot be ignored in many domains such as spatial, network, computer (hard disk drive, USB, etc...).

In this thesis, we focus on the receiver circuit of a serial link, and especially the core of this receiver: the CDR (Clock and Data Recovery). The CDR is the hardiest and most critical block to design in serial links.

The PLL (Phase Locked Loop) architecture was mainly used for high frequency CDR [1]. The increasing design and finalization complexity of such architecture lead to the research of other solutions. A solution is to use digital blocks in the CDR, like multi phased CDR. Most of the previous problems were solved but other appears like an increased power consumption and chip size. Those new constraints can only be addressed with new advanced process like 32 nm CMOS or more advanced technologies.

The ILO (Injection Locked Oscillator) design with discrete components was very used in 1950-1960 decade in radio or TV receptor, mainly for its simplicity.

The integrated PLL development eclipses the ILO during the years 1980. ILO interests came back with the advanced semiconductor technologies and some laboratory research activities like the ones done at the IMS laboratory. ILO can be used for frequency synthesizer [2] and for CDR [3].

The goal for this thesis is to reach very high frequency, with an ILO-based CDR, around 80 Gb/s, with a power consumption under 2W. To reach this goal a new ILO-based CDR

generation has been developed. The targeted frequency requires a new architecture for the phase comparator and the ILO as we will see.

This thesis will focus on high speed CDR, in a SiGe process. Chapter 2 provides information on CDR circuits, from an architectural to a circuit level point of view. Different CDR topologies are explained. Figures of merit will be described and used to compare several circuits. In Chapter 3 the Injection Locked Oscillator is described, from theory to circuit design. This introduces the used CDR architecture which is a combination of a PLL based CDR and an open loop CDR. Stability studies are presented to ensure the correct operation of the system. A phase comparator with a windowing mode is proposed to work with the CDR. Chapter 4 depicts the design and measurements of the two designed prototype ASIC circuits. Finally Chapter 5 summarizes this thesis.

Chapter 2

Clock and Data Recovery

This chapter presents a description of a Clock and Data Recovery (CDR) system. The objective is to understand the data transfer background. This will provide useful information for next chapter comprehension. The second objective is to present the particular architecture used in this thesis. Section 2.1 presents the serial data communication, how it is made, and what are the limits we must face on. Data modulation part will describe the CDR, and why are they used. Section 2.3 will explain the open loop CDR. Then the phase detector is presented, why it is so important, how we associate it with a charge pump and its influence on jitter is briefly described in part 2.4 to part 2.6. Then the Injection Locked Oscillator CDR is explained.

2.1 Serial data communication

Serial links are used to transmit data since the beginning of telecommunication market. It allows the transfer of large quantity of information over a single link without the parallel links drawbacks such as cross-talk, limited bandwidth and high footprint. Mostly used for medium distance communication at the beginning, it is nowadays used also for longer distance and short range. The transmission distance increase as do the quantity of data. This is mainly due to the increased Internet traffic. The medium for long distance serial link is optical fiber based. Some protocol like the Synchronous Optical Network (SONET) has become the standard for wide area network (WAN). Fiber-optic serial links used expensive integrated circuits (IC) such as laser diodes, mainly VCSEL (Vertical Cavity Surface Emitting Laser), photodetectors, amplifiers, clock and data recovery (CDR), serializer and deserializer. These circuits are realized on GaAs and SiGe technologies and are expensive. Such substrates are used due to their high gain and operating frequency compared to CMOS process. Continuous development is maintained to increase the link speed and get ready for future needs.

Another wide use of serial link is for backplane telecommunications. As the processor power increases, the bandwidth of the processor link to external devices such as hard disk

drive or memory increases to feed the data fast enough to the processor. Some technology innovations like strained Si significantly improve performances without increasing defaults and allow very fast operating IC with copper link. Classical CMOS components can be used; reducing the cost of such systems but reduce the operating frequency. Strained Si is not available in the laboratory and in order to reach the desired operating frequency bipolar technology will be used. Some researches on optical link on backplane begin, but the high cost limits their implementation.

Serial links are also present inside chips as the designers place more and more circuits in the same die to reduce costs. These circuits communicate through serial links between each others. In this case, CMOS CDRs are used but the CDR integration in CMOS is not trivial. CMOS processes have less gain and the substrate is lossy, allowing noise to interfere with sensitive circuits.

A new market is the silicon photonic technology. An optical link is created inside a silicon chip with silicon oxide, which acts as glass. Electrical components are on another wafer and both wafers are bounded like for SOI technology. The goal is to overcome the copper bandwidth limitation and to have optical link between the processor cores.

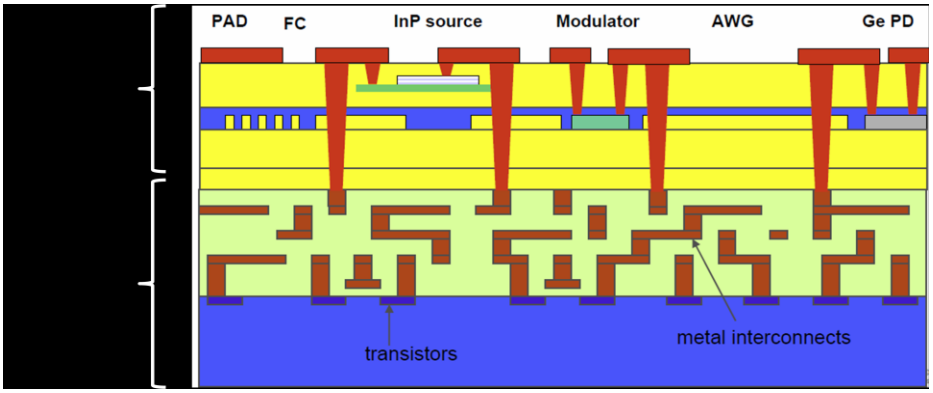


Figure 1: Photonics Electronics Integration on CMOS: CEA-LETI, MINATEC Campus Grenoble (F) ESSCIRC 2011

This technology is still in research as 200 Gbps links are estimated for 2018.

Data communication is the transfer of bits over a channel. The channel can be the air, for wireless communication (cell phone) or a wire, such as copper (USB) or optical fiber. There are three different directions for a channel as we can see in Figure 2. Simple channel is used when there is no need for an acknowledge to confirm that the data are well transmitted, or when transmitter don't need to "hear" the receiver, like a CMOS sensor sending data to the

memory of a camera. Half duplex channel allows the communication in both ways with a simple channel, reducing the cost, but it is like a walkie-talkie, both side can't talk together at the same time. Full duplex channel is like a double simple channel, it requires two channels, and both sides can talk at full speed every time.

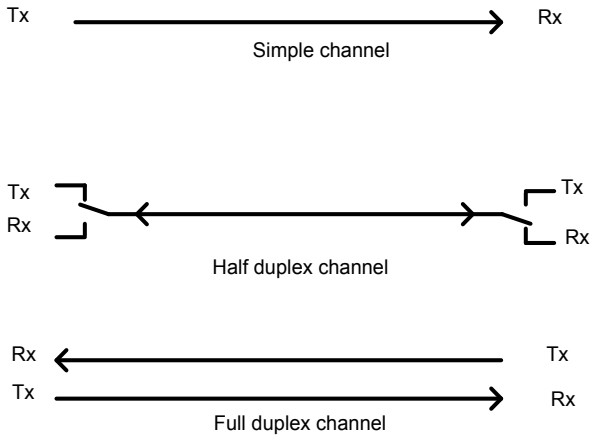


Figure 2: Communication channel

It is called "serial" because bits are sent one by one. By opposition, on parallel data communication, several bits are sent at the same time via different wires. That allows link with less pins on the ASIC and reduces the number of PCB tracks. The data are put into electrical domain, this is the modulation, and can be encoded to optimize the bandwidth occupation or simplify the reception.

A classical link is presented Figure 3. The data arrive in parallel, are encoded, put in serial by the serialization register and transmitted over the link. Once received, they are deserialized and resampled, then decoded, and are able to be computed.

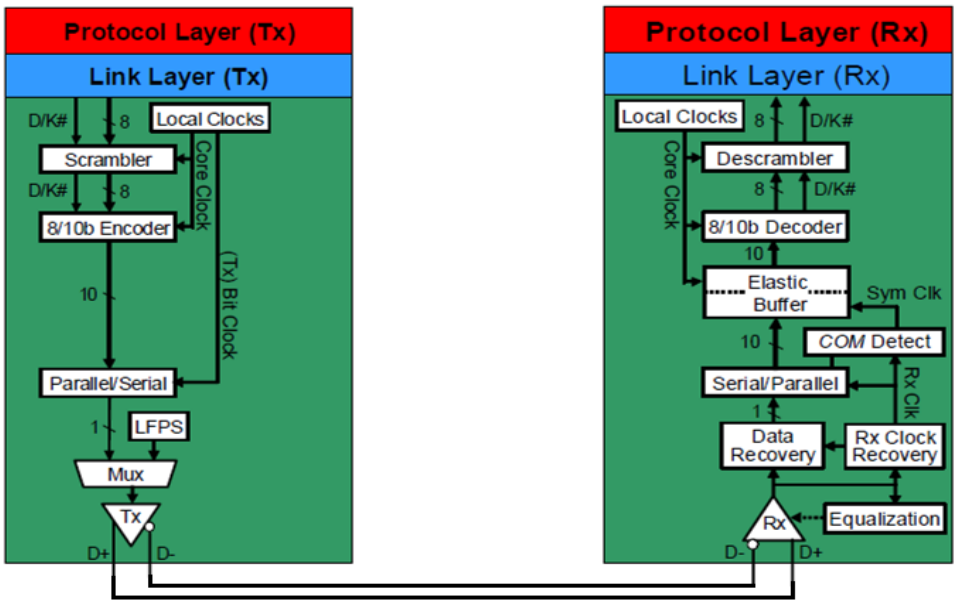


Figure 3: Serial link functional diagram

The drivers (Tx and Rx) are 50 Ω output buffers as most of the links have 50Ω impedance. The buffer can be compliant with LVDS (Low Voltage Differential Signaling) or ECL (Emitter Coupled Logic) standard. The high-speed links are often differential to bring good common-mode noise rejection.

To transmit the data over the link, a modulation must be chosen to ensure a good data transmission.

2.2 Data modulation

Modulation is well known for wireless communication. In wired communication, this is also known as line coding. There is various types of line coding, here are a few examples.

- **Non-Return-to-Zero:**

Also called unipolar encoding, this is the simplest line code. There is only two output, "0" and "1", and their corresponding electrical levels for the entire period clock. For a given data rate, NRZ coding only uses half of the speed of the clock needed to generate it. However there is no frequency power at the data rate (Figure 4), so the clock extraction can be more difficult than with other coding. Another drawback is for long "0" or "1" pattern, the electrical value

will be DC and can be filtered by high-pass filter, and the receiver can lose the clock synchronization.

- **Manchester code**

In Manchester code, each bit will have a transition and occupy the same length of time. This is done by a XOR gate between the data and the clock. This coding is interesting as it doesn't have any DC component. There is data rate frequency information, meaning it can be self-clocking. There is always a transition on the line, so the receiver is able to detect the incoming clock. However it uses all the bandwidth defined by the data rate, i.e. a 10 Gb/s signal needs a 10 GHz bandwidth.

- **Bipolar**

It uses 3 electrical levels. The middle level is the return to zero (and most often 0V) but not the "0" logic state, both others are "1" (+V) and "0" (-V). By using 3 levels, there is no DC value and this coding can be used for long distance communication, as no DC power is sent. It uses the same bandwidth as the Manchester code.

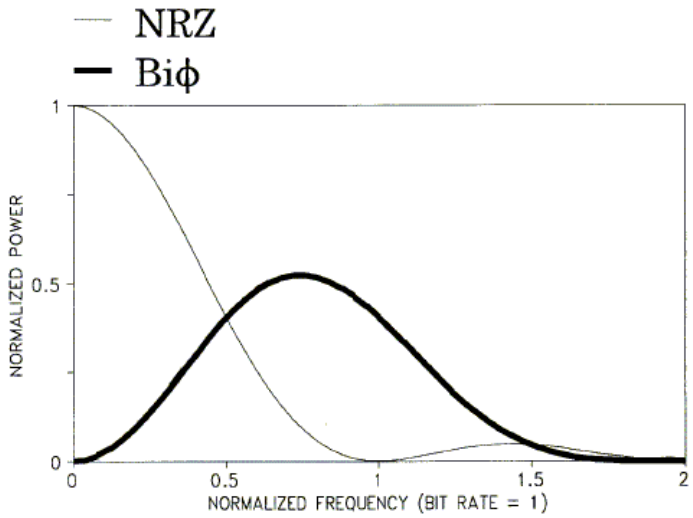


Figure 4: Spectrum for random data with NRZ and bipolar coding

Those 3 different codes can be seen in Figure 5

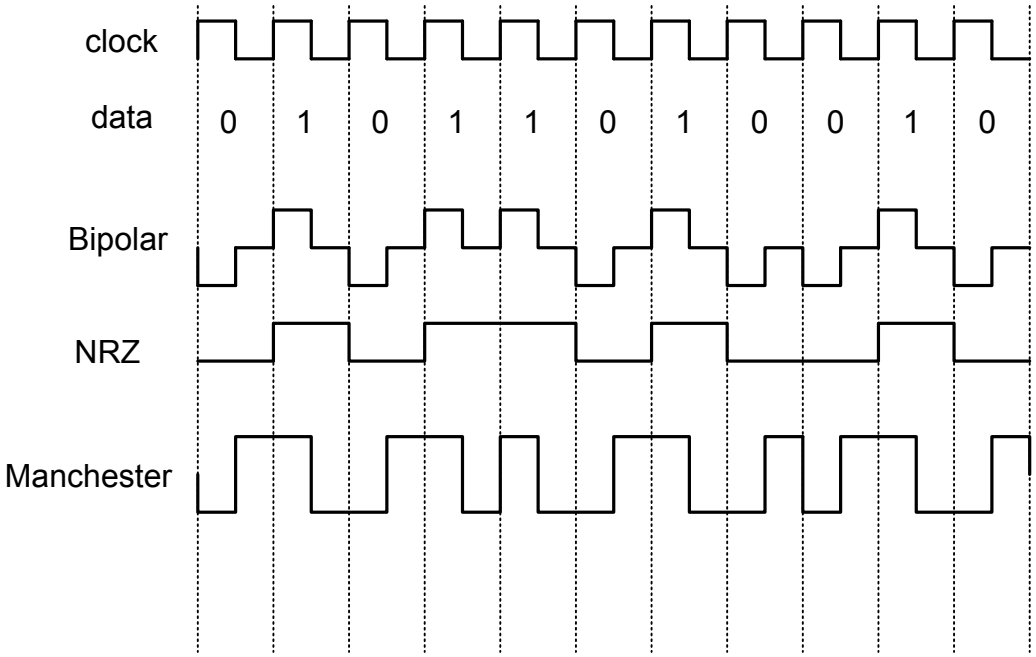


Figure 5: Line coding example

Even with these weaknesses, the reduced bandwidth of the NRZ code allows it to be used in various standards such as the USB which uses a variant, the NRZI [4]. Some other coding are research like multi level [5], [6][7], [8] coding but the increased complexity doesn't seem to outweigh the bandwidth reduction.

A way to compensate the drawback of a code is to encode the data. Encoding is the action of mapping a set of data to another one. For example, after 6 identical bits, a different one is inserted to prevent clock loss. Another advantage is to reduce the DC level. A very common encoding is the 8b/10b. For 8 bits of original data, this scheme uses 10b of transmitted data. These two extra bits reduce the effective bandwidth of the data communication link and are known as overhead. In the 8b/10b encoding, there is 20% overhead. The overhead can be reduced by using other encoding such as the 128b/130b which has 1.6% overhead.

In this thesis we don't focus on the encoding, assuming the encoding is done by the transmitter. The chosen data modulation is the NRZ.

The signal will propagate through the medium, usually copper over a substrate (FR4), or in twisted pair like Ethernet wire. The signal will meet several discontinuities and can be degraded. The discontinuities can come from bonding wires, connectors, lossy transmission lines etc. The bandwidth limitation comes from dielectric loss and skin effect [9]. The more the frequency increases, the more the losses increase. The PCB substrate must be selected

with special care. On Figure 6, we can see the insertion losses for different substrates. Passive and active techniques can be used to improve the transmission speed. Passive techniques use high quality microwaves devices.

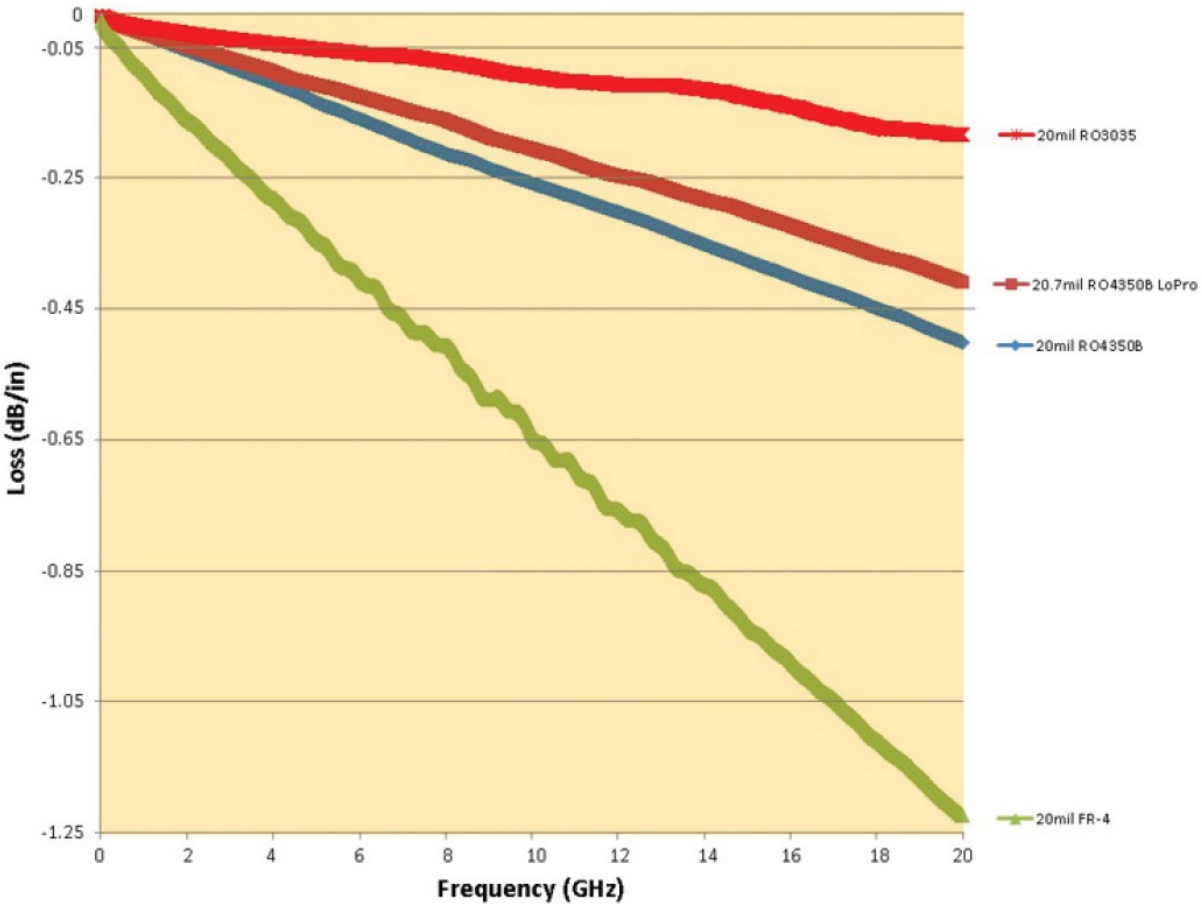


Figure 6: Insertion losses of a 20 mil, 50 Ohms TL over different substrates [10]

For example, the IEEE 802.3bj taskforce defines the appropriate medium for the 100Gbase-KR4. The 100 Gb/s link will be split into 4 lanes to reduce the constraints. The expected speed is 25.7813 Gb/s with NRZ data, so a clock frequency of 12.8913 GHz on an "enhanced FR4". The estimated losses are 10 dB for the backplane version and 30 dB for the cable version [11].

The ITRS estimated the NRZ serial data will reach 100 Gbps in 2018 [12].

For speed higher than 30 Gb/s, the link must have a special package and a dedicated connection, based on K connector or for up to 110 GHz, the 1mm connector. These connectors are nevertheless very expensive. For differential serial link, both wires must be perfectly matched, which is very hard to obtain with high speed data transfer. Serial communication at very high speed uses an optical link to overcome the difficulties previously

presented. The optical fiber is directly connected to the silicon chip with embedded DSP like in Intel light peak cable [13].

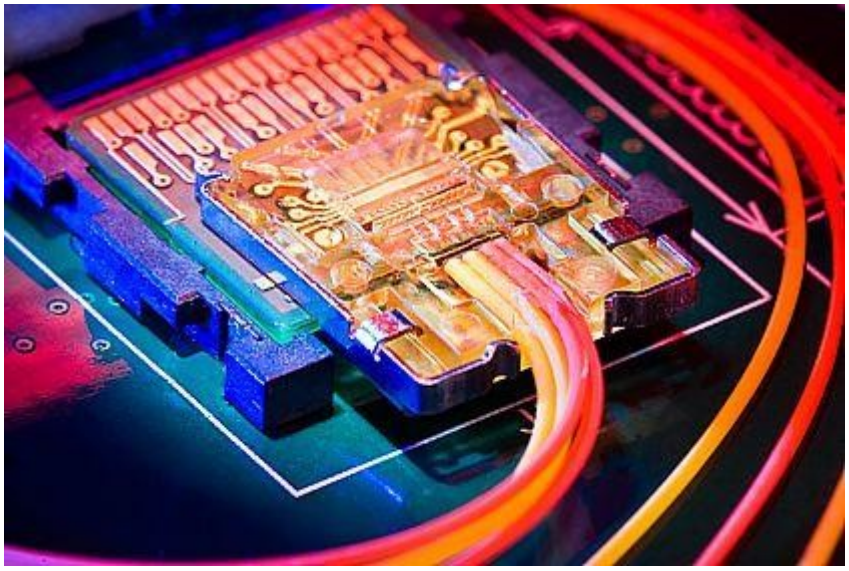


Figure 7: Intel light peak cable

However, photonic components are very expensive, but there is a trend to "siliconize" (integration, high volume and low cost) photonics to reach mass market.

The other technique to improve transmission link includes adaptive decision point [14], pre-emphasis, and multi-level signaling. This solution is cost effective, and is used by industry to increase transmission speed on backplane. Pre-emphasis circuits boost the magnitude of the high frequency data of a serial data transmission without modifying the magnitude of the low frequency contribution. The pre-emphasis influence can be seen in Figure 8. A 2.5 Gbps signal is transmitted over a 30" FR4 stripline [15]. Test point (TP1) 1 is before the stripline and TP2 just after. The pre-emphasis benefits are clearly visible. The eye is open, the BER is maximal.

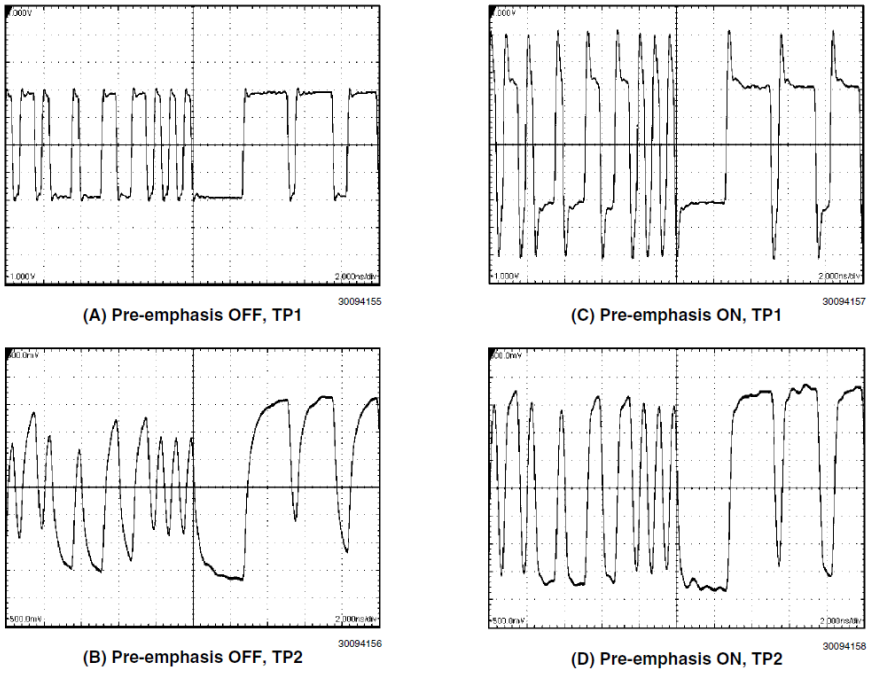


Figure 8: Bit stream of a 2.5 Gbps signal vs. pre-emphasis

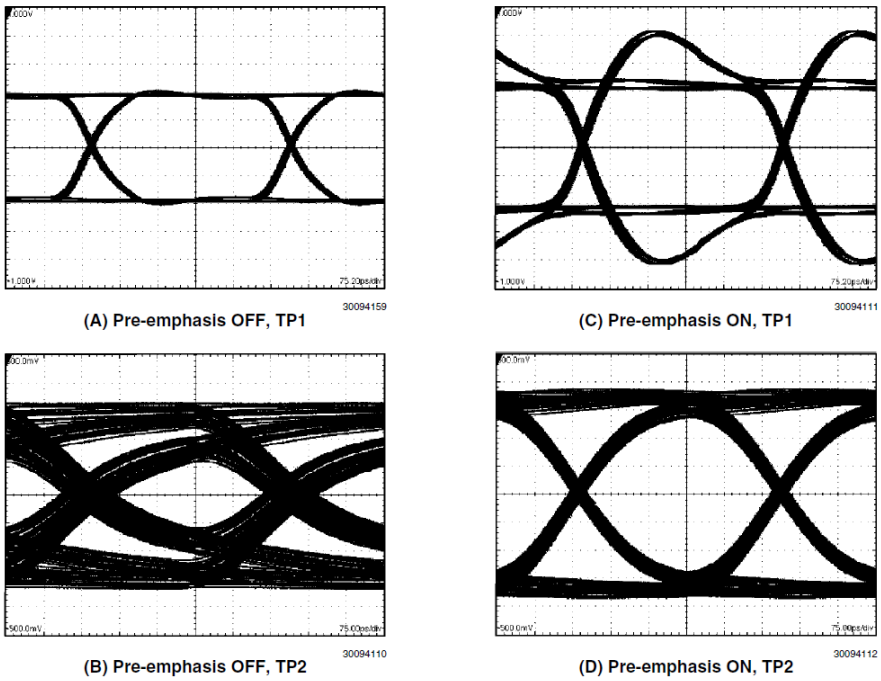


Figure 9: Eye diagram with pre-emphasis implementation

2.3 CDR overview

The CDR function is to receive the serial data, extract the clock from the incoming data and to sample the incoming data with the extracted clock. The purpose of this operation is to increase the signal to noise (SNR) ratio of the data to reduce errors. In other word, the CDR will reduce the Bit Error Rate (BER) of the channel. To minimize the BER, the CDR must sample the incoming data in the middle of the eye diagram (Figure 10). At this point there is the lowest BER. The recovered clock will be used also by the receiver front-end blocks, like the deserializer. The clock is extracted from the data by detecting the edge transitions, and by aligning the clock edges of the internal oscillator with the incoming data edges, so the clock and the data will be in phase.

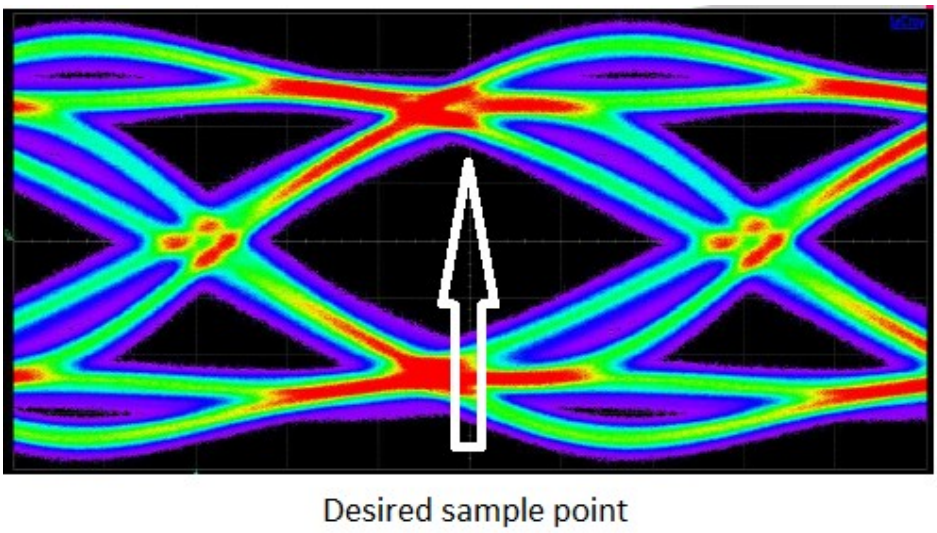


Figure 10: Optimal sample point

Sampling at the same point requires knowing exactly the frequency of the data. This can be done by topologies using feedback phase tracking, such as PLL and DLL; phase interpolator or injection locking. Another solution is to sample multiple (3 or 4) times during a bit period and use majority voting. But for high data rate, the clock speed can be very high and difficult to obtain. There are also topologies with phase alignment [16] but without feedback like high-Q bandpass filter and gated oscillator structures.

The incoming data signal and the Rx clock signal have a phase difference, which is not stable (due for example to thermal differential between Tx and Rx), so the Rx needs to adjust in real time the sampling time. To perform this, the PLL based CDR is composed of three blocks: an oscillator, a phase comparator and a loop filter. A voltage controlled oscillator (VCO) will

generate a clock with a frequency which depends on the voltage applied to one of its gate. The clock signal is sent to the retiming circuit and to the second block. A phase detector or phase comparator will estimate the difference between the clock and the incoming data and gives a signal depending on this error. This signal will be filtered by the last block, the loop filter. The loop filter will remove the high frequency components of the phase detector signal and stabilize the VCO frequency. The phase error voltage will force the VCO to change its frequency and so its phase, and then will move the "effective" sample point to the targeted one. The CDR architecture can be seen in Figure 11. This kind of CDR is very similar to a phase locked loop [17], one difference can be the missing divider on the clock path which is present on some particular CDR. As this topology have slow acquisition, it needs some synchronization frames before sending useful data.

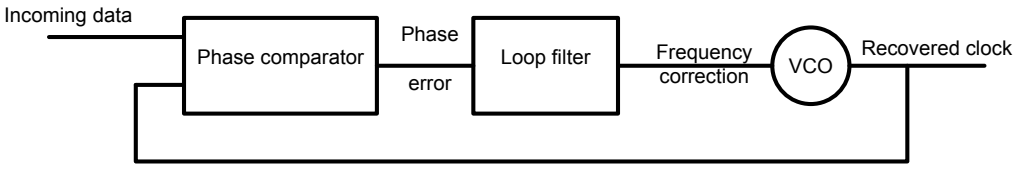


Figure 11: PLL based clock and data recovery architecture

2.4 Open loop CDR

An open loop CDR is mainly based on gated oscillator, high-Q filter and injection locked oscillator architectures [18]. They are used in burst mode communication, due to their very fast response time. The three architectures are very similar:

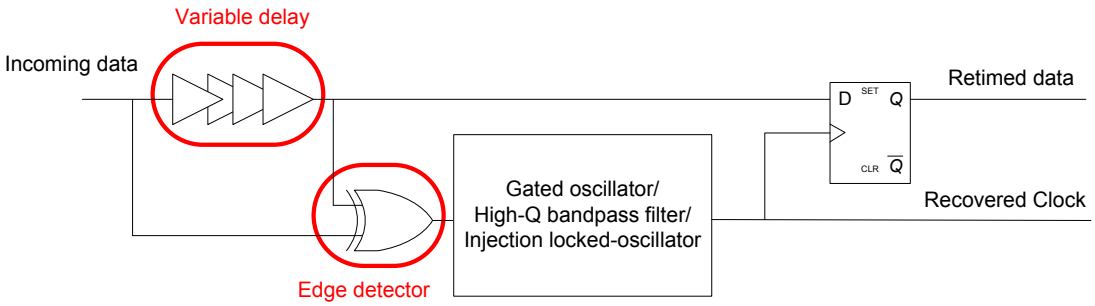


Figure 12: Open loop CDR architecture

Only one block changes, depending of the open loop CDR type.

The variable delay adjusts the phase position of the bit in order to be aligned with the clock edge. The variable delay can be controlled externally to correct the process variation and ensure to sample data at the targeted sample point.

The edge detector (a XOR gate) will generate pulses at the incoming data bit frequency. The pulses command the gated oscillator.

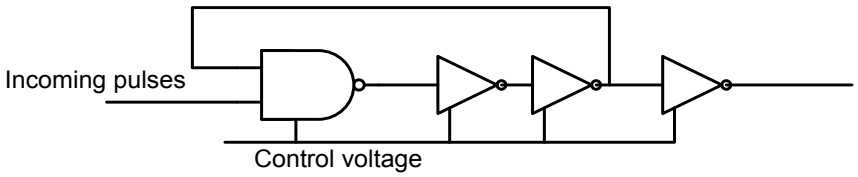


Figure 13: Gated oscillator

A gated oscillator is presented Figure 13. The pulses command the ring oscillator. The two inverters after the NAND gate create a delay of half the bit period and generate the clock. The waveforms of Figure 12 are:

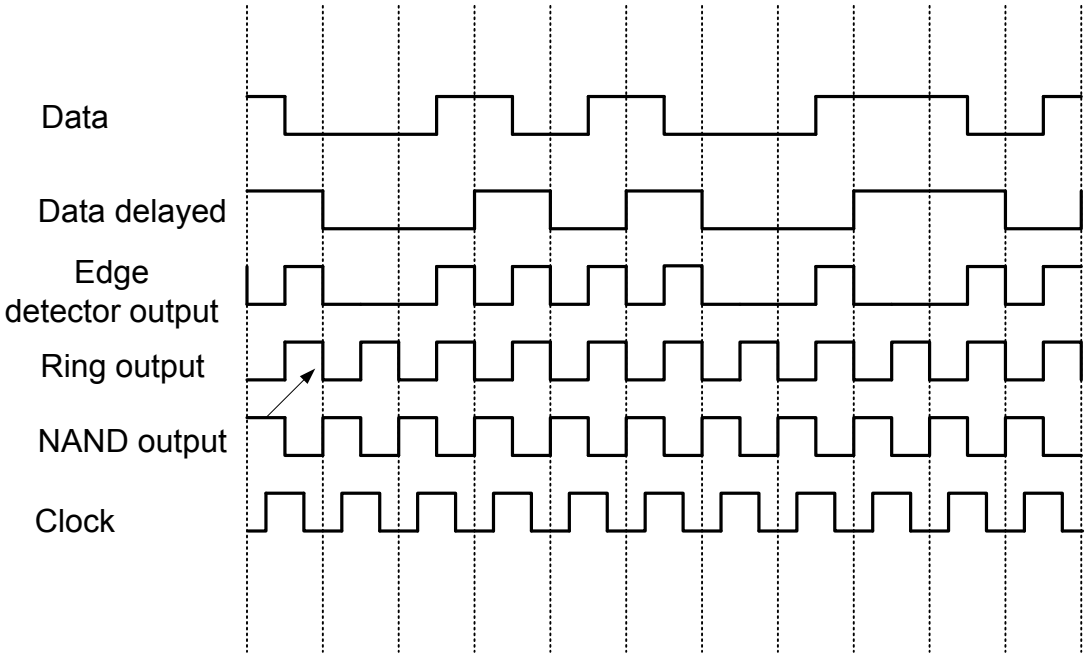


Figure 14: Gated CDR waveforms

Sometimes the gated oscillator is duplicated and inserted in a PLL to have a fine-tuning of the control voltage [19]. The schematic of such a CDR is given on Figure 15:

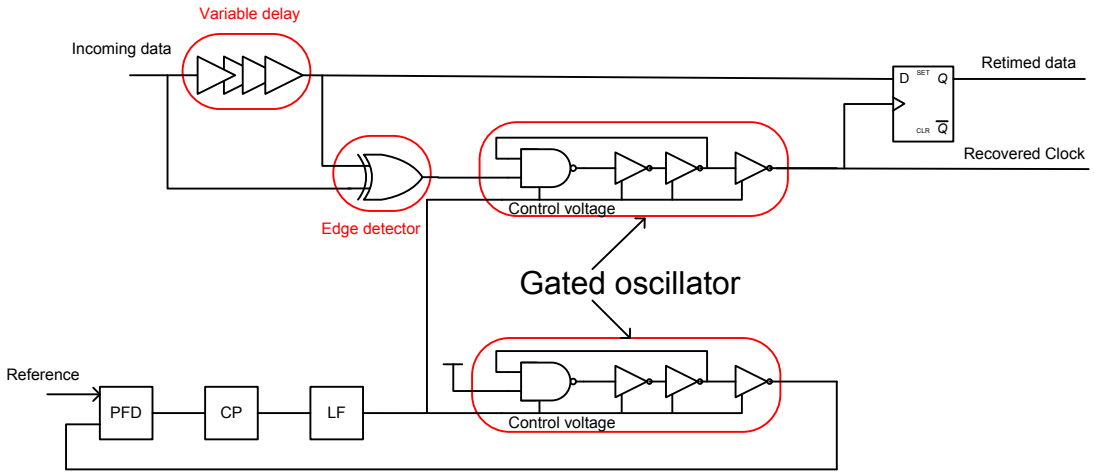


Figure 15: Gated oscillator-based CDR

As we can see, the XOR output has a frequency component at the bit period. The high-Q filter such as a LC filter or a SAW/BAW filter filters this frequency and directly sample the clock on high-Q filter based CDR [20]. However it is difficult to integrate high quality factor filter on chip, and BAW/SAW filters are limited in their maximum frequency (5-10GHz).

For the ILO based open-loop CDR, when the XOR output is injected in an oscillator, it will force it to lock on this frequency allowing a little process variation in the oscillator design.

Open loop CDR is very fast and so is used for burst mode operation, is very simple to design, but suffer from jitter transfer. Another drawback is the phase alignment sensitive to process, temperature, voltage variations and data rate.

2.5 Phase detector

The phase error between the Rx clock and the incoming data is estimated by the phase detector. There are 2 major types of phase detector [21], [22]: the linear phase detector and the binary phase detector. The linear phase detector has an output proportional to the phase error. The binary phase detector output magnitude will be the same if the phase error is small or large. The output will only change regardless of the phase error sign. The ideal behavior of this two phase detectors can be seen in Figure 16. The phase error is represented on the x axis and the output of the phase detector is on the y axis.

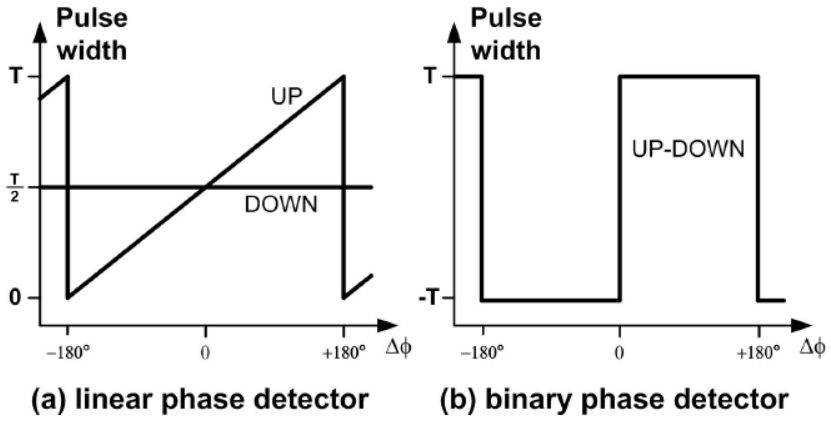


Figure 16: Linear and binary phase detector behavior

- **Linear detector**

Due to its proportional behavior, the linear phase detector will generate low activity on the VCO control voltage when there is a small phase error, like when the CDR is locked. This gives good jitter performance to the CDR.

A very basic linear detector is a XOR gate. It's very simple to implement and can work at high data rate. But it has several drawbacks. Firstly, the output current has always the same sign, so we need to translate the transfer function (red curve in Figure 17), and insert a delay so the signal will be in phase when in fact they are in quadrature. Secondly, when there is no input data, the XOR phase detector interprets this as a phase error and applies a correction and the CDR will not lock correctly.

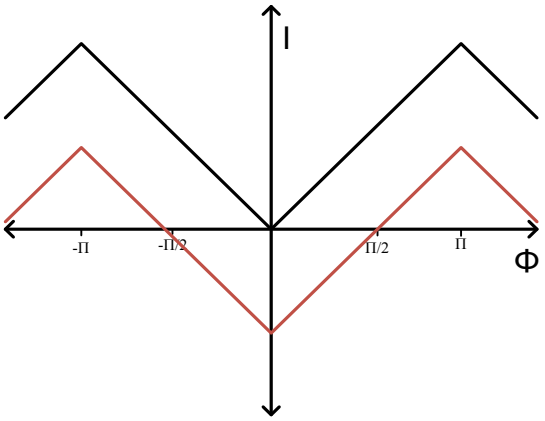


Figure 17: XOR transfer function

The most widely used linear phase detector was created by Hogge [23]. Its schematic and transfer function are shown in Figure 18.

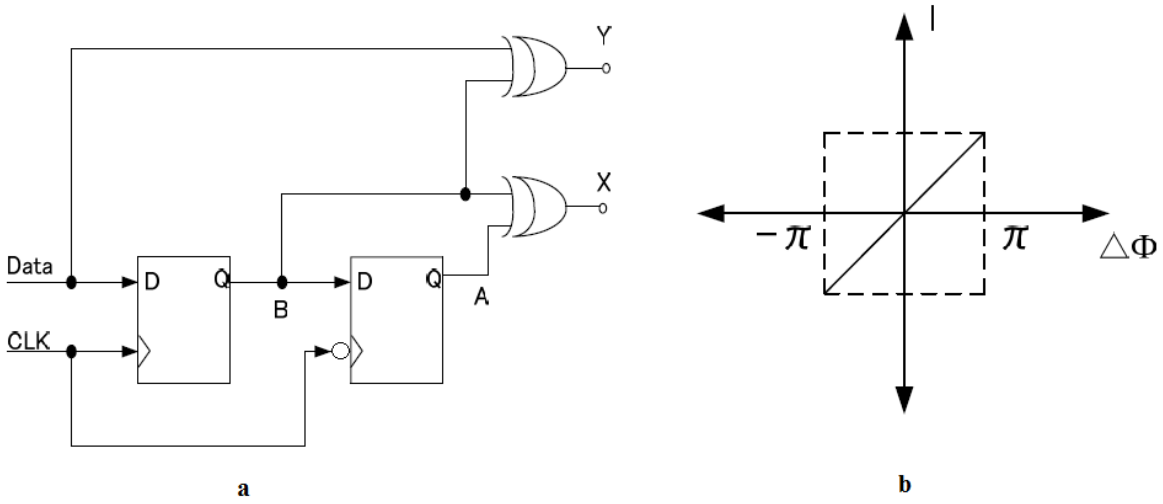


Figure 18: Hogge phase detector schematic (a) and transfer function (b)

The Hogge phase detector generates two pulses to control the charge pump, one to charge the loop filter, called the UP (X) and the other one to discharge the loop filter, called the DOWN (Y).

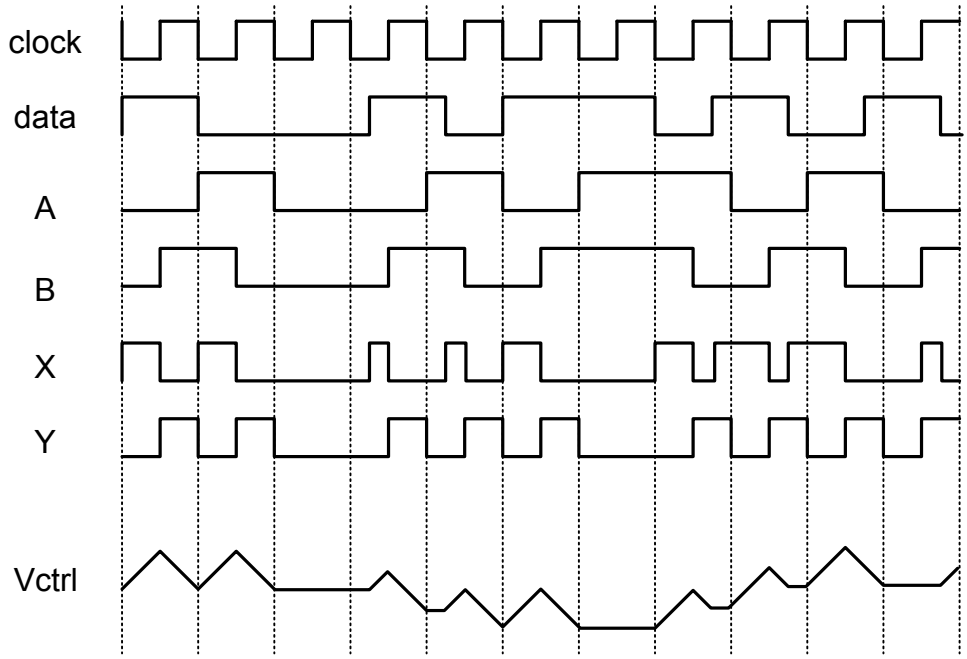


Figure 19: Hogge detector waveform

When the CDR is locked, UP and DOWN pulses have the same width, the same amount of charges is added and subtracted by the charge pump, and the loop control voltage has no change. When the data lags the clock, the UP pulse will be shorter than the DOWN one, and the loop voltage will decrease. The VCO will go slower, and its phase will slowly move toward the data phase. At the opposite, when the data leads the clock, the UP pulse will be

larger than the DOWN one, and the loop voltage will increase. The VCO frequency will increase, and its phase will catch the data. The DOWN pulse is always half a bit time in width. Only the UP pulse time width varies, depending of the phase error between the clock and the data. Despite its improvements compared to a XOR phase detector, the Hogge phase detector still has some drawbacks. Firstly, a delay must be inserted on the data path of the UP XOR to compensate the D-FF (D flip flop) delay, as shown in Figure 20.

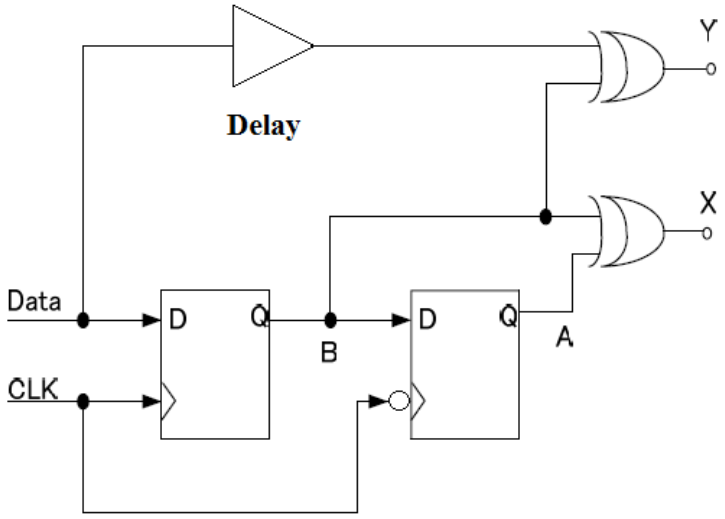


Figure 20: Delay compensation for the Hogge phase detector

Secondly, bandwidth requirements limit the phase detector maximum operating frequency, because it's difficult to generate short pulses at high data rates. Thirdly, a non-ideality in the process will vary the pulses width and generate offset jitter. Some improvements have been done by [24] [25] but the phase detector has become more sensitive to duty cycle distortion on the clock signal.

- **Binary phase detector**

Also known as bang-bang phase detector, the first binary phase detector was published by Alexander [26]. The output has only two states, corresponding to the phase error between the clock and the incoming data. There is no information on the magnitude of the phase error.

As for the linear phase detector, there is a very basic binary phase detector: a D-FF. A CDR with a D-FF as phase detector can be seen in Figure 21.

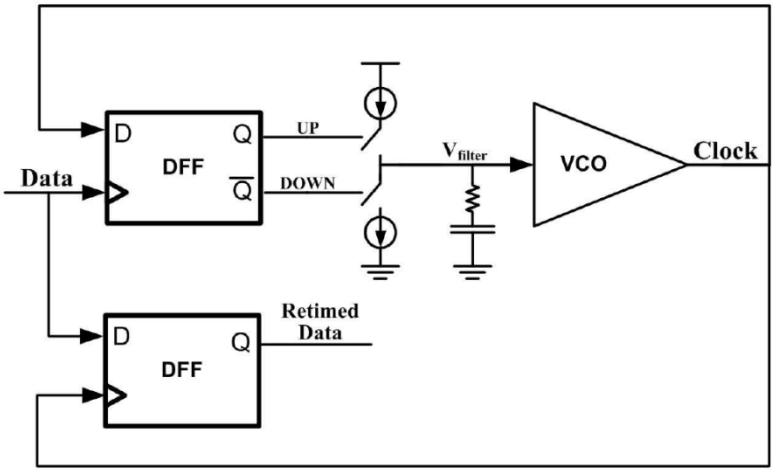


Figure 21: CDR with a D-FF as phase detector

However this phase detector has major drawbacks. A second D-FF is needed for the data retiming, as the clock paths to the phase detector and to the retiming D-FF must be exactly the same. Moreover, when there is no data transition, the phase detector remains in the last know state (charge or discharge), and the CDR can lose lock. A third state can be implemented when no information are sent to the charge pump when there is no data transition. A third state is not necessary when there is a line encoding as seen in 2.2, and the lack of a third state would not break the performances.

Figure 22 shows an implementation of the Alexander phase detector [27], [28] with the third state.

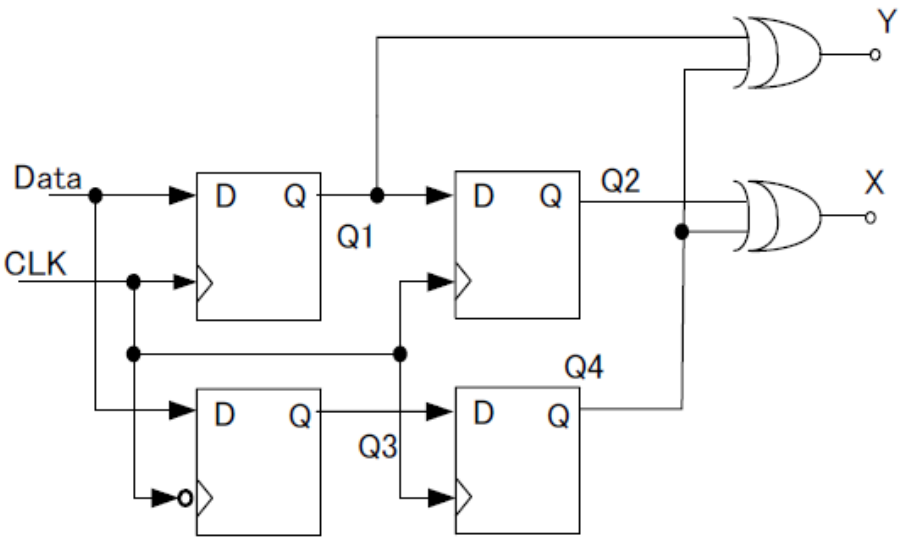


Figure 22: Alexander phase detector architecture.

The corresponding waveforms are given in Figure 23.

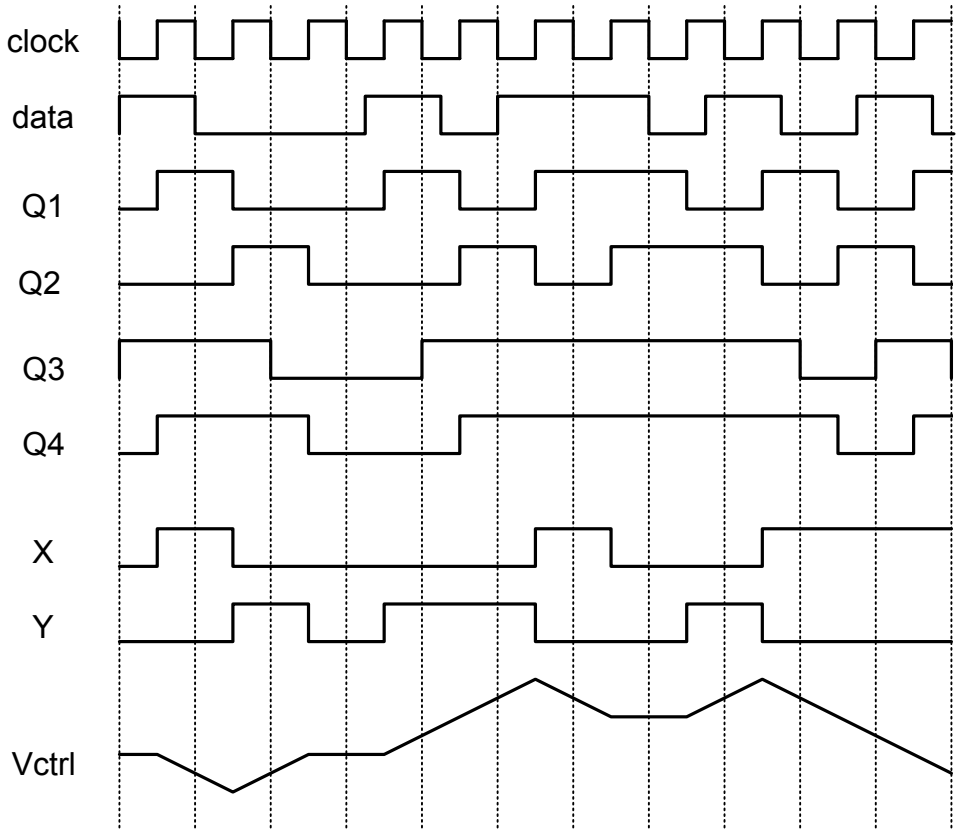


Figure 23: Operation of the Alexander phase detector

The X output is DOWN and Y is UP in the waveforms. When there is no data transition (long "0" or "1" pattern), UP and DOWN remain to low value, and no charge is added or discharged from the control loop. The VCO frequency will not move and the CDR will stay locked. A weakness of the Alexander phase detector comes from the complexity compared to the linear phase detector or a D-FF phase detector. The power consumption and area occupation are higher. Another limitation, the phase detector doesn't provide any information on the magnitude of the phase error, the jitter is worse than the one of a linear phase detector CDR. Binary phase detector can operate at higher frequency than linear phase detector as the UP and DOWN pulses are always wider than a clock period.

The phase detector generates two signals, UP and DOWN, which control the charge pump. The detailed behavior of a charge pump is described in the following section.

2.6 Charge pump

The charge pump with the loop filter translates the phase error signal generated by the phase detector in a control voltage for the VCO. It adds or subtracts charges from the CDR's loop filter. The charge pump is controlled by the phase detector. When the UP signal is active, the UP switch is closed; I_{UP} adds charges in the loop filter and the control voltage increases. When the DOWN signal is active, the charge pump removes charges from the loop filter via I_{DOWN} and the control voltage decreases.

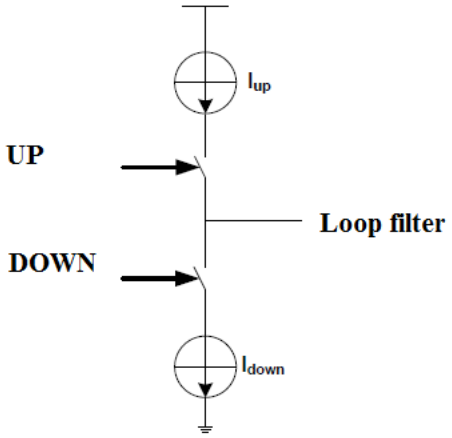


Figure 24: Basic architecture of a charge pump

When UP and DOWN are active, the control voltage must remain constant. I_{UP} and I_{DOWN} must be equal. But if they are made of current mirrors using PMOS and NMOS transistors respectively [29] [30], they are never perfectly matched, leading to a static phase error. This mismatch can be avoided by using NMOS switches only [31] [32].

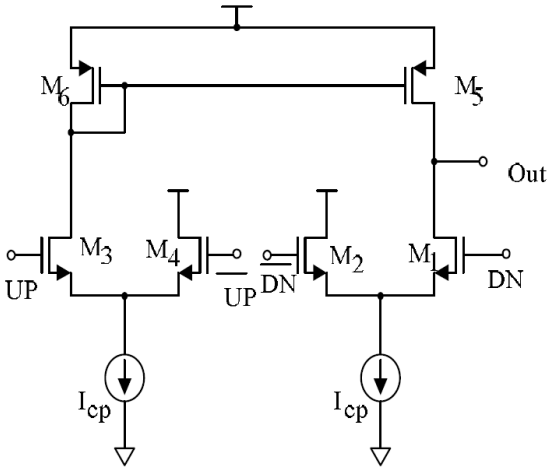


Figure 25: Single ended charge pump with NMOS switches

With NMOS switches only, the diode-connected transistor M6 limits the speed of the charge pump. A differential implementation as [33] can counteract this effect.

However, there is some disadvantage to use differential filters. A common-mode feedback circuit is required to compensate the charge pump non-linearities which generate a DC offset. The loop filter will be duplicated which can be area hungry. Such a charge pump can be seen in Figure 26.

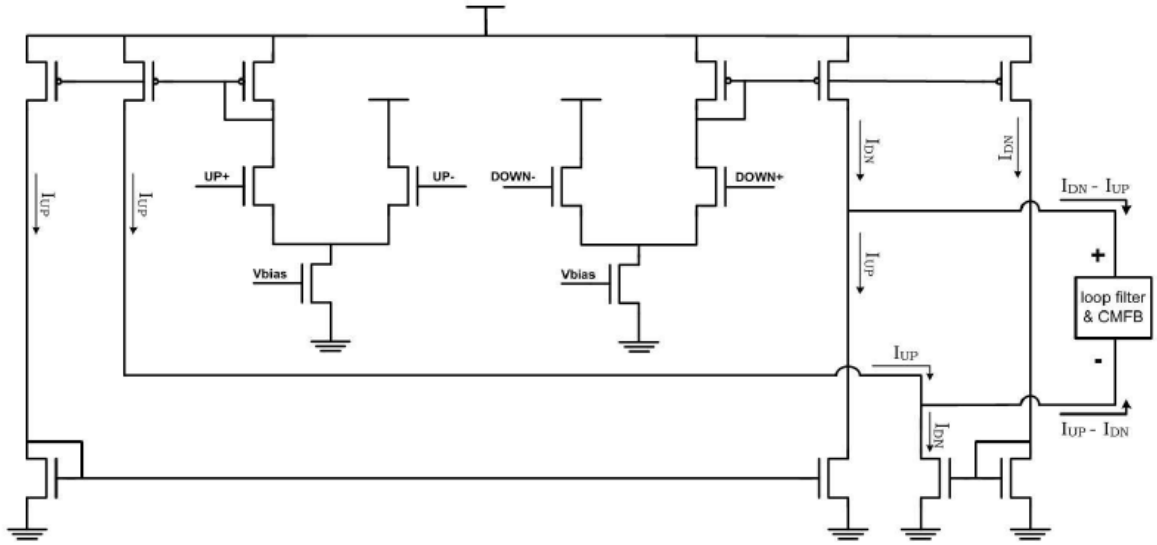


Figure 26: Differential charge pump

2.7 Jitter

Jitter is an undesired variation of the clock phase (and data) edges during time. The clock edge (or crossing for differential clock) may vary around its ideal position of a small percentage. In CDR, clock jitter generates data jitter, as the sampling point varies. Jitter is usually expressed in unit interval (UI). A UI is the theoretical length of a clock period, or for NRZ data, the length of a single bit. The jitter can be deterministic or random.

- **Random jitter**

Random jitter is an unpredictable electric noise. It is characterized by Gaussian distribution. Random jitter is caused by thermal noise of electronic components, flicker noise and shot noise. Random jitter is unbounded.

The random jitter probability density function is:

$$RJ(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\left(x^2/2\sigma^2\right)} \qquad (2\text{-}1)$$

With σ the standard deviation of a Gaussian distribution, and x the time error relative to the ideal position.

- **Deterministic jitter**

Deterministic jitter has specific and reproducible causes. By opposition to random jitter, it is bounded. Deterministic jitter sources are various and include crosstalk (from another serial link), electromagnetic interferences (like power supply variations) etc. Deterministic jitter can also be data dependent, or data uncorrelated.

- **Data dependent jitter**

Total jitter (T) is defined as the combination of random jitter (R) and deterministic jitter (D):

$$T=D_{peak\text{-}to\text{-}peak}+2*n*R_{RMS} \quad (2\text{-}2)$$

n is defined by the wanted BER through $\frac{1}{2}+erfc(\sqrt{2}*n)=BER$

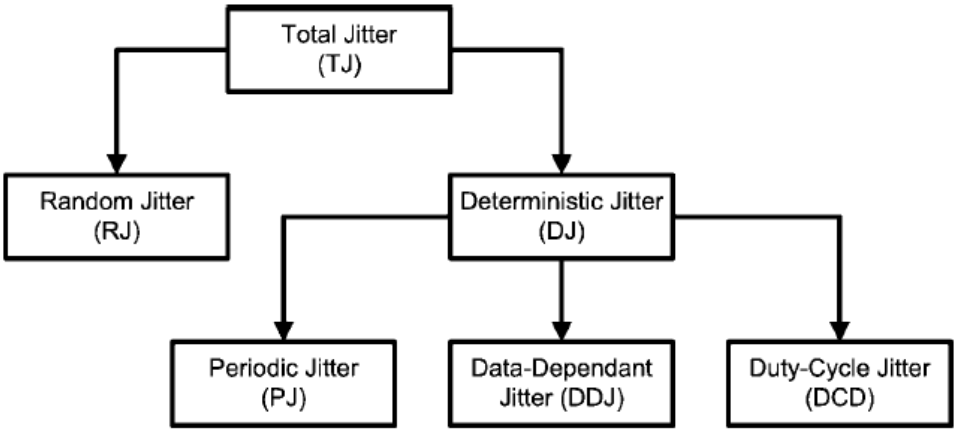


Figure 27: Jitter categories

For a link, jitter tolerance, jitter generation and jitter transfer function are specified by the corresponding standard. It can be an eye opening mask (Figure 28) or a jitter transfer mask.

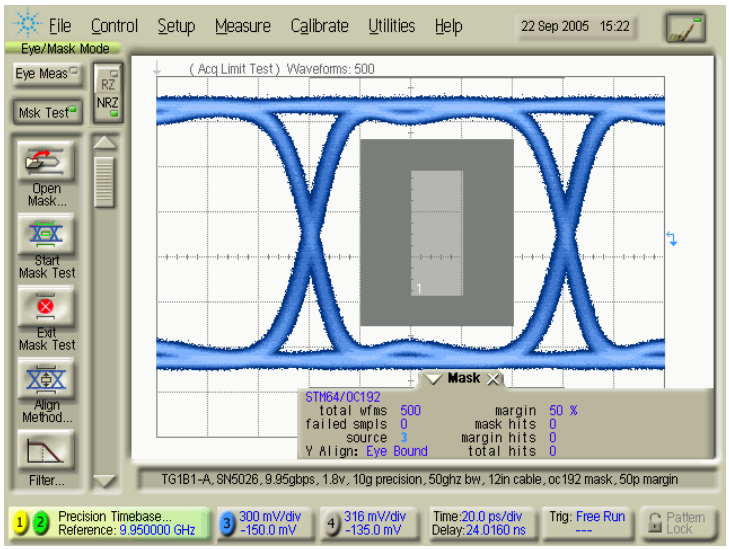


Figure 28: SONET 10Gb eye mask

2.8 ILO based CDR

The Injection Locked CDR architecture uses the locking property of oscillators. When a signal with a frequency close to the oscillator free running frequency is injected in an oscillator, the latter frequency will shift toward the injected frequency. There is no need for phase detector, charge pump and other circuits. The CDR can be very compact, with just the oscillator and the data retiming block. This kind of CDR works up to 10 Gb/s in 47 GHz fT SiGe BiCMOS [34].

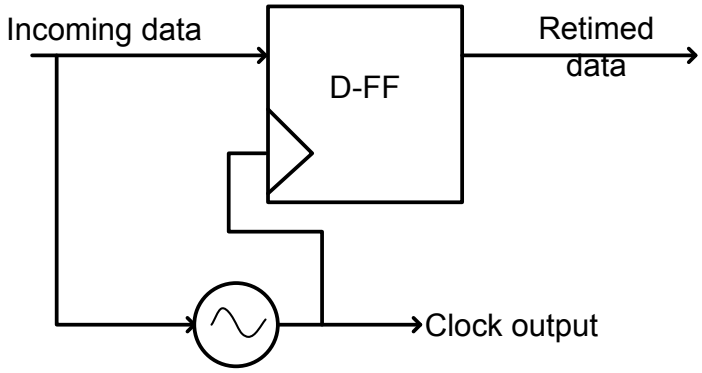


Figure 29: Injection locked CDR architecture

The injection locked CDR has less jitter peaking, is faster, and more stable than PLL based CDR. However, there is quantization phase errors and the jitter is dependent of the oscillator frequency range.

To overcome this problem, a solution is to insert the ILO based CDR in a PLL based CDR [35].

The resulting CDR has the following architecture (Figure 30):

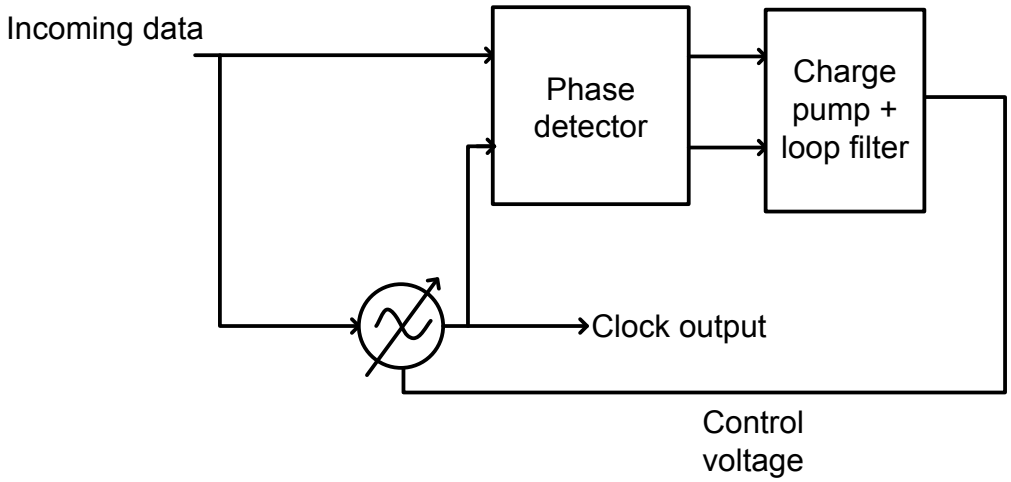


Figure 30: CDR architecture based on PLL architecture

The local oscillator is a voltage controlled oscillator with injection locking (ILVCO). The locking range of the ILVCO is small to reduce the jitter, and this small frequency locking range is compensated by the frequency range of the VCO. The circuit utilizes injection locking to filter out high-frequency reference clock jitter. This architecture has been patented by the CNES and Thales Alenia Space and will be used in this thesis work.

2.9 High speed PLL and CDR

Some millimeter waves PLL and CDR have already been done. Over 100 GHz circuits are mainly built using InP HBT technology. Between 100 GHz and 50 GHz most of the circuits use SiGe HBT. Under 50 GHz, CMOS transistor chips appear more often. Most of the CDR and PLL devices are designed to match a standard, such as the 10 Gb/s SONET or 40 Gb/s optical communication. Over 50 GHz, devices are mainly PLL for automotive radars or dedicated applications. Some chips are just demonstrator to show the abilities of a manufacturing process, such as [36], where a LNA is present conjointly with a 104 GHz oscillator. This paper shows the good performances of the 90 nm CMOS process used.
In Table 1, a comparison between different PLL around 100 GHz is presented.

Table 1: PLL state of the art

Réf.	Technology	Tuning Range (GHz)	Div. Ratio	PN (dB@1MHz)	Spur (dBc)	Output power (dBm)	Dc (mW)	Chip Size (mm²)
[37]	0.13µm BiCMOS	92.7-100.2	64	-102	-60	3	570	1.1x1.1
[38]	0.18µm BiCMOS	90.9-101.4	768	-92	-52	NA	140	1.9
[39]	0.13µm BiCMOS	86-92 162-164	16 to 32	-98.2 -78.9	NA	-3 -25	1150 to 1250	1.7x1.1
[40]	0.18µm BiCMOS	23.8-26.95 75.67-78.5	256 to 768	-114 -103.5	-49.5 -47.8	-9.5 -17.8	50 75	1x0.8
[41]	45nm CMOS	57-66	512 to 8184	-75	-42	NA	78	0.99x0.83
[42]	0.8 µm SiGe HBT	64-81	64	-106	-37	-2.4@64 GHz -6@81 GHz	431	1x1.1

[43]	90 nm CMOS	75-75.320	64	-88@100 kHz	<-72	-28	88	1x0.8
[44]	65 nm CMOS	95.1-96.5	256	-75.86	-51.8	-26.8	43.7	1x0.7
[45]	0.25 µm InP	300.76-301.12	10	-78@100 kHz		-23	301	1.38x0.61
[46]	0.13 µm SiGe BiCMOS	92.7-100.2	64	-102	60	3	570	1.1x1.1

This apercu shows us the possibility to design a high speed PLL-based CDR. The logic blocks such as the phase comparator can be built and operate efficiently. The power consumption is always under 1W, and the chip doesn't need a thermal cooler during operation.

More than 50 Gb/s CDR are very few, such as [47], [48] which are PLL based CDR or [49], an injection-locked CDR. All these CDR integrate a 1:2 DEMUX to reduce the output data frequency. Special design techniques are used, such as optimized DFF [51]. This kind of latches has the clock and data signal in parallel and at the same signal level to reduce the propagation delay present in a classical D latch due to DC offset conversion. If possible, all logic blocks should have this kind of configuration, to prevent any unwanted offset jitter (Figure 31).

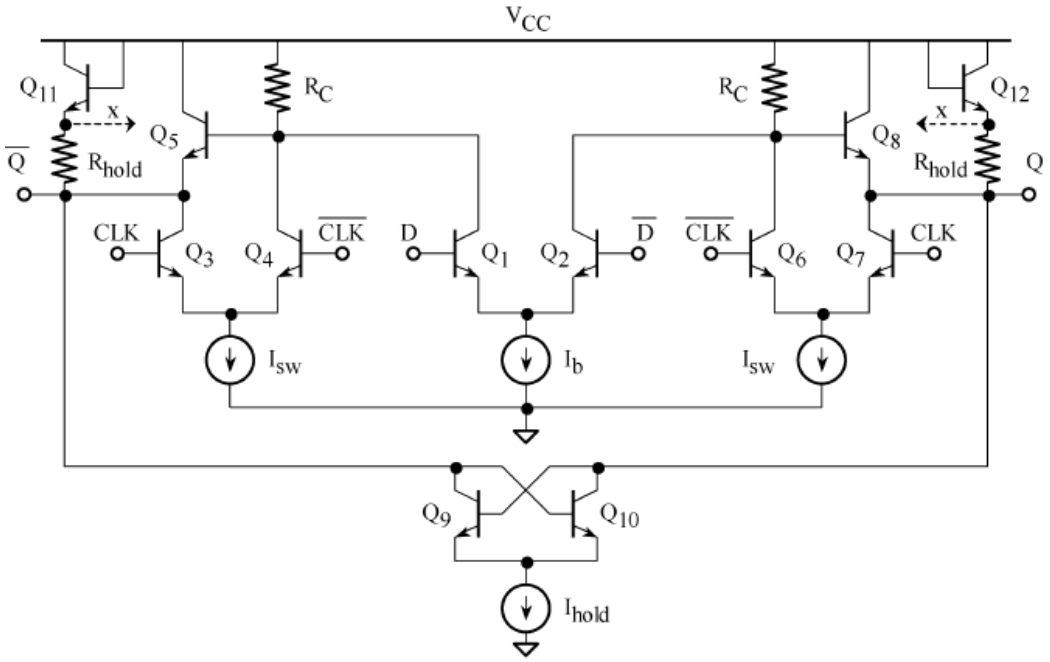


Figure 31: Optimized latch

Another improvement is the use of half rate phase detector (Figure 32) to operate at speed well beyond 100 Gbit/s. The blocks used series-gating concept with the ECL circuit techniques to optimize performances [47].

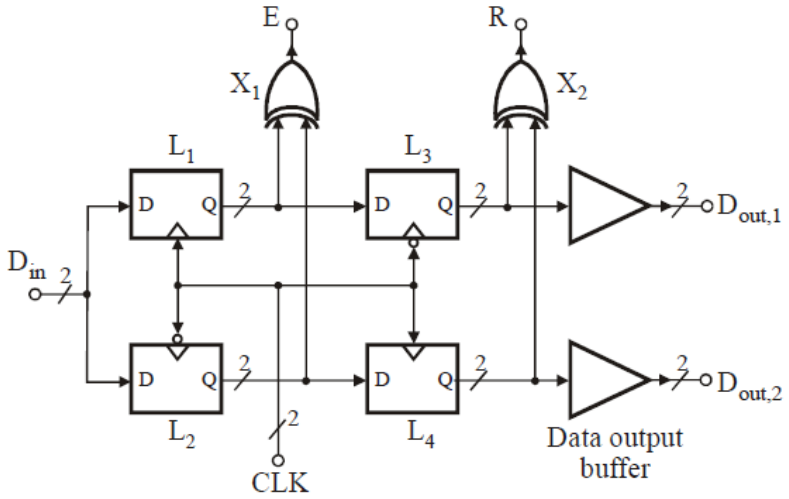


Figure 32: Half rate phase detector

The power supply is very high, from 3.3 V in [49] to 5 V in [48] with 4.5 V in [47]. A high power supply voltage allows transistor stacking to perform some logic functions and higher output voltage swing. All these CDR use microstrip lines as inductor, as even a small piece of metal acts as an inductor at such frequencies.

These characteristics can be seen in Table 2.

Table 2: CDR comparison

Réf.	Technology	Tuning Range (GHz)	DC (W)	Chip Size mm²
[47]	InP 0.7µm	107-112	2.2	2x2
[48]	0.14µm BiCMOS	100-107	5	2.5x1.7
[49]	0.18µm SiGe	71	0.514	1.54
[50]	InP 1µm	100	2.1	2x2

As we can see, all the PLL based CDR have a high power consumption (2 to 5 W) compared to the open loop CDR [49]. However the latter oscillator only operates at 35.5 GHz with a 6.8 GHz tuning range. The other CDR oscillators oscillate at the bit rate frequency. As the parasitic capacitors are more dominant at high frequency, the locking range cannot be so large.

Chapter 3

Critical building blocks

3.1 Injection locked oscillator

As seen in 2.8, our CDR topology uses an Injection Locked Oscillator (ILO). An explanation of the ILO behavior is presented to understand how the CDR works.

3.1.1 Injection locking oscillator theory

"An oscillator can be locked in frequency by an external signal which is injected into the oscillator" [52]. This effect is also known by RF designer as the pulling effect. A VCO will see its self frequency (f_0) shift toward the parasitic signal frequency f_i. This property was used in old TVs to synchronize local oscillator with the TV signal and is used in frequency divider for example.

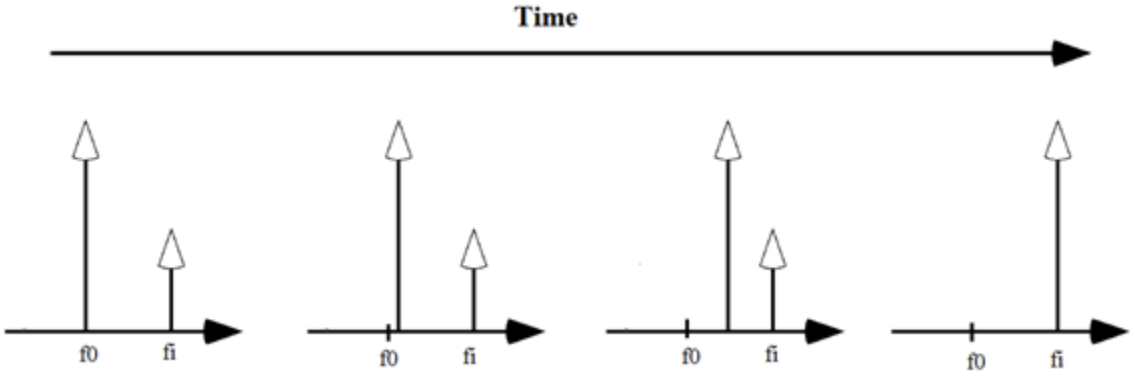


Figure 33: Synchronization of an oscillator during time

Injection Locked Oscillators (ILO) can be used in CDR systems to optimize them [35]. Each time a toggle appears on the incoming data signal, a current is injected in the oscillator. The oscillator frequency will lock with the data frequency. This chapter describes how ILO works. Most of theoretical studies on oscillators modelize the latter as a combination of an inductor and a capacitor for the resonant circuit with a resistor simulating the losses and a negative

resistor for the active part. This theory is quite complex and difficult to scale for different oscillator topologies.

Huntoon and Weiss have developed a theory on how this locking phenomenon appears in [53]. This theory is very simple and generic. Nevertheless this one is only valid for small synchronization signal.

For a synchronization by a voltage source, the model is:

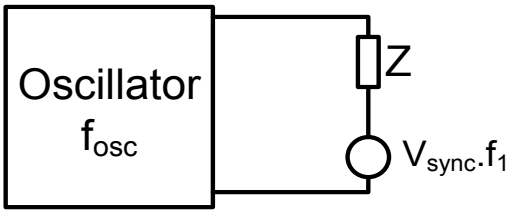


Figure 34: Huntoon and Weiss model

The oscillator is considered as a black box, with its load impedance (Z) and the external synchronization is V_{sync} at frequency f_1. If f_1 is close to f_{osc}, the synchronization source can be replaced by a small variation of the load impedance (Z+dy).

The compliance factors are defined as the amplitude and frequency variations when there is a small variation of the load impedance.

The compliance factor E_A and E_F, expressed as:

$$E_A = |E_A|.\exp(j.\alpha) = A_r + j.A_x = \sqrt{A_r^2 + A_x^2}.\exp(j.\alpha) \tag{3-3}$$

$$E_F = |E_F|.\exp(j.\beta) = F_r + j.F_x = \sqrt{F_r^2 + F_x^2}.\exp(j.\beta) \tag{3-4}$$

Are defined for $dy=g_y+j.b_y$ as

$$\begin{aligned} F_R &= \frac{1}{2\pi}.\left.\frac{\partial\omega}{\partial g_y}\right|_{d_y=0} \quad A_R = \left.\frac{\partial A}{\partial g_y}\right|_{d_y=0} \\ F_X &= \frac{1}{2\pi}.\left.\frac{\partial\omega}{\partial b_y}\right|_{d_y=0} \quad A_X = \left.\frac{\partial A}{\partial b_y}\right|_{d_y=0} \end{aligned} \tag{3-5}$$

A and F terms can be expanded in first order Taylor series for small amplitude and frequency variations, around the free running frequency (f_0) and the amplitude without synchronization A_0.

$$A - A_0 = g_y . A_R - b_y . A_X \quad (3\text{-}6)$$

$$F - F_0 = g_y . F_R - b_y . F_X \quad (3\text{-}7)$$

The synchronization voltage and current are:

$$V_{sync}=|V_{sync}| \exp(j.2\pi.f_{sync}.t) \quad (3\text{-}8)$$

The current through the load and the synchronization source is:

$$I=|I| \exp(j.2\pi.f_{osc}.t) \quad (3\text{-}9)$$

With f_{osc}, the oscillator instantaneous frequency.

For a small voltage variation on the oscillator output, we can assume that the current (I) variation can be neglected and stay at the self oscillating level (I_0). This lead to:
$V_{sync}=I.dy=I_0\ dy$
And so:

$$dy = \frac{V_{sync}}{I_0} = \frac{|V_{sync}|}{|I_0|} . exp(j.\emptyset) = g_y + j.b_y \quad (3\text{-}10)$$

Ø(t) is the phase error between the synchronization signal and the oscillator signal:

$$\phi(t) = \phi_{sync}(t) - \phi_{osc}(t) \quad (3\text{-}11)$$

We can write from (3-4) and (3-5)

$$A - A_0 = \frac{|E_A|.|V_{sync}|}{|I_0|}.cos(\emptyset - \alpha)$$
$$f_{osc} - f_0 = \frac{|E_A|.|V_{sync}|}{|I_0|}.cos(\emptyset - \beta) \quad (3\text{-}12)$$

where

$$\tan(\beta) = \frac{F_x}{F_r}$$
$$\tan(\alpha) = \frac{A_x}{A_r} \quad (3\text{-}13)$$

By derivating (5-9), we obtain:

$$\frac{1}{2.\pi}\frac{d\phi}{dt} = f_{sync} - f_{osc} = (f_{sync} - f_0) - (f_{osc} - f_0) \quad (3\text{-}14)$$

We inject (3-10) in (3-12)

$$\frac{1}{2.\pi}\frac{d\phi}{dt} = (f_{sync} - f_0) - \frac{|E_F|.|V_{sync}|}{|I_0|}.\cos(\phi + \beta) \quad (3\text{-}15)$$

This equation gives us the phase behavior when there is a synchronization signal. The f_{sync}-f_0 term is the beat frequency. The other term defines the locking range. When there is no phase error, we got:

$$(f_{sync} - f_0) = \frac{|E_F|.|V_{sync}|}{|I_0|}.\cos(\beta) \quad (3\text{-}16)$$

As cosines function varies from -1 to 1, the locking range is:

$$\Delta f = 2.\frac{|E_F|.|V_{sync}|}{|I_0|} \quad (3\text{-}17)$$

The synchronization signal can be an harmonic of the injected signal, or can be the result of a mixing between the synchronization signal and an harmonic of the oscillator signal. In the

former case it is called a sub-harmonic synchronization; in the latter case we say it is a super-harmonic synchronization.
Sub-harmonic synchronization can be seen as a PLL with a divider in the feedback. If the synchronization signal is produced by a quartz VCO at 133 MHz and if the oscillator frequency is around 660 MHz, the latter will lock at 665 MHz, on the fifth harmonic of the quartz. A drawback is the low power present on the high frequency harmonic. In this case it will be very difficult to lock on the tenth harmonic.
Super-harmonic injection locked is used in Injection-Locked Frequency Divider (ILFD). It is the opposite of the sub-harmonic synchronization. The injected frequency is a harmonic of the oscillator frequency [54]. For example, the ILFDs are used as prescaler in the PLL divider path.

The Huntoon and Weiss theory describes the phase behavior, the locking range and the amplitude modifications of an oscillator during the synchronization process from the compliance factor. This theory can be applied for voltage or current synchronization. The compliance factor must be calculated for each oscillator topology.

3.1.2 Compliance factor for cross-coupled LC oscillator

The oscillator studied below uses bipolar transistors that have a very high f_t. It is based on a cross coupled topology, which is well known. The LC tank oscillates, and the cross coupled transistors is seen as a negative resistor which compensates the losses. The oscillator architecture is:

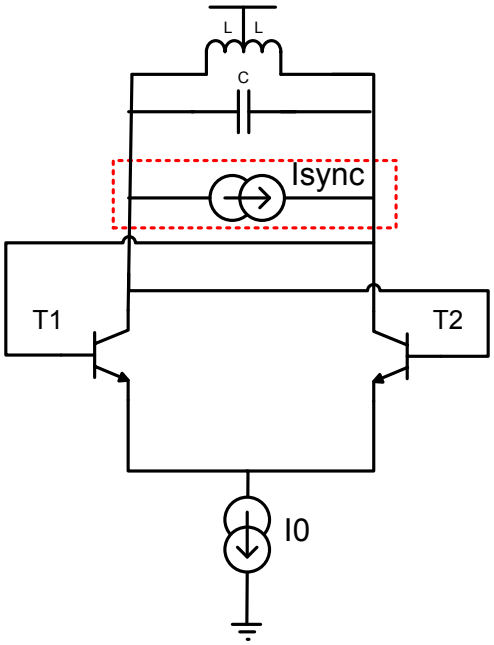


Figure 35: Cross-coupled oscillator

The unknowns of the Huntoon and Weiss theory are the compliance factors in amplitude and frequency. We will solve the frequency equations to find these parameters.

As seen previously, the synchronization block is substituted by a small admittance $d_y=g_y+j.b_y$. To find the compliance factors, we must find the oscillator frequency. The following small signal model helps us to solve it.

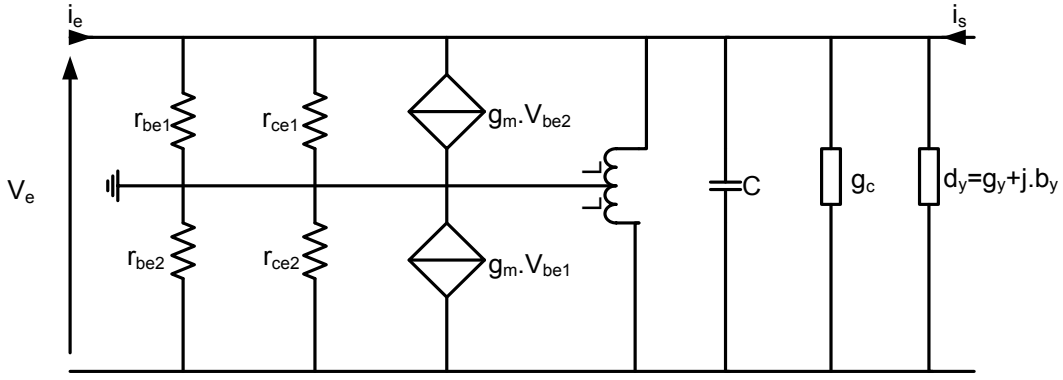


Figure 36: LC equivalent small signal model

Simple small signal model is used for the transistors. gc is the oscillator load admittance. The current equation is:

$$ie = \left[2.\mathrm{d_y} + 2.g_c + 2j.\mathrm{C}\omega + \frac{1}{j.\mathrm{L}\omega} + \left(\frac{1}{\mathrm{r_{be}}} + \frac{1}{\mathrm{r_{ce}}} - \mathrm{g_m}\right)\right].\frac{\mathrm{V_e}}{2} - \mathrm{i_s} \qquad (3\text{-}18)$$

To respect Barkhausen criteria, the input and output current values must be zero. So the Ve term must be null. The real and imaginary part of the V_e argument must be equal to zero:

$$\begin{aligned} 1 - 2\left[b_y L\omega + LC\omega^2\right] &= 0 \\ L\omega.\left[2.g_c + 2.g_y + \left(\frac{1}{r_{be}} + \frac{1}{r_{ce}} - g_m\right)\right] &= 0 \end{aligned} \qquad (3\text{-}19)$$

The solution is:

$$f = \frac{1}{2\pi}.\frac{\sqrt{L(b_y^2.L + 2C)} - b_y.L}{2.C.L} \qquad (3\text{-}20)$$

Without synchronization signal, d_y=0, the oscillator self frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{L.2.C}} \qquad (3\text{-}21)$$

The frequency compliance factors are obtained by derivating (5-18) by g_y or b_y, and then by canceling the g_y or b_y terms.

$$\begin{aligned} F_R &= \frac{1}{2\pi}.\left.\frac{\partial\omega}{\partial g_y}\right|_{d_y=0} = 0 \\ F_X &= \frac{1}{2\pi}.\left.\frac{\partial\omega}{\partial b_y}\right|_{d_y=0} = -\frac{1}{2\pi}.\frac{1}{C_1 + 2.C_2} \end{aligned} \qquad (3\text{-}22)$$

With these compliance factors, we can estimate the locking frequency:

$$\Delta F = 2.\frac{I_{sync}}{V_0}.\sqrt{(F_{by}^2 + F_{gy}^2)} = \frac{I_{sync}.\sqrt{2}}{n.\pi}.\sqrt{1 - \cos(\xi.2.\pi.n)}\,\frac{1}{V_0.\pi.C} \qquad (3\text{-}23)$$

with I_{sync} the synchronization signal amplitude, n the synchronization harmonic and ξ its duty cycle. V_0 is the oscillator output amplitude with no synchronization. We can see the importance to lock on the fundamental to have a great locking range.

The ideal synchronization signal is a square wave signal with its frequency close to the oscillator one.

The Huntoon and Weiss theory has been used to realize a VHDL-AMS model of an injection locked voltage controlled oscillator.

3.1.3 VHDL-AMS model of a injection locked oscillator

In order to help the comprehension of the ILO and to improve the time efficiency of the simulations, we have developed a high level model based on Huntoon and Weiss theory.
This theory is valid only for small amplitude value injected signals. Strong injection modifies the output signal amplitude, and has not been yet solved to our knowledge. As seen before, the phase relation is:

$$\frac{1}{2.\pi}\frac{d\phi}{dt} = (f_{sync} - f_0) - \frac{\Delta F}{2}\cos(\phi(t) + \beta) \qquad (3\text{-}24)$$

Where f_{sync} is the injected signal frequency and f_0 the ILVCO free running frequency (unlocked). β is defined through the compliance coefficients F_R and F_X as:

$$\tan(\beta) = \frac{F_x}{F_r} \qquad (3\text{-}25)$$

The instantaneous ILVCO synchronized frequency is:

$$f_{ILO} = \frac{-1}{2\pi}.\frac{d\phi}{dt} + f_{sync} \qquad (3\text{-}26)$$

And the corresponding phase is

$$\phi_{ILO} = 2\pi.\int f_{ILO} \qquad (3\text{-}27)$$

The output signal is defined as:

$$V_{out} = V_0.\sin(\phi_{ILO}) \qquad (3\text{-}28)$$

ΔF is the ILVCO locking range, defined by (3-23). Several parameters of the synchronization signal must be known to calculate the locking range. Different processes extract these values from the signal. The designer can define the ILO free running frequency, the inductor value and variable capacitor parameters.

The first process P1 determines the synchronization signal duty cycle and its frequency. The process waits for a voltage crossing between the signal and a threshold. The difference between three different crossings gives the duty cycle and the frequency. The crossing value is a global variable and can be defined by the designer. This process requires a very high resolution to calculate the exact input frequency and so imposes the minimal time step of the simulator. T1, t2 and t3 are initialized at the beginning of the program.

```
t <= now ;
P1 : process
        begin
        wait until vin'above(threshold);
        t3 <=t1;
        t1 <= t;
        wait until not vin'above(threshold);
```

Synchronization signal frequency detection

The second process P2 determines the amplitude of the input signal. It waits (duty_cycle)*period/2 after the threshold crossing to take the maximum voltage value. It waits (1-duty_cycle)*period/2 after the threshold crossing to take the minimum voltage value. In the optimal case, the synchronization signal is a square wave signal, so even if it is distorted, the maximum and minimum values are exact.

This is represented on Figure 37. The duty cycle is 0.25. The first value is taken 0.25xT/2 after the first crossing with the threshold value. The second value is taken (1-0.25)*T/2 after the second crossing with the threshold value.

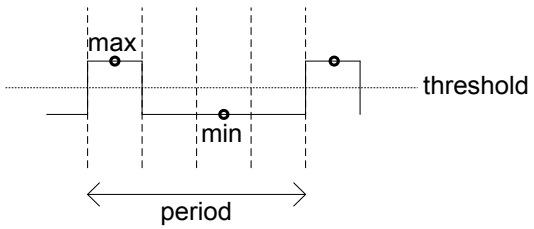


Figure 37: Duty cycle determination

```
P2 : process
        begin
        wait until vin'above(threshold);
        wait for (duty_cycle/(2.0*fsync));
                imax <= iin;
        wait until not vin'above(threshold);
```

Maximum and minimum value

The third process P3 evaluates the synchronizing harmonic. If the synchronizing frequency is between f_0 and $f_0/2$ then it will be synchronized on the fundamental tone. Else it will be on the closest harmonic of f_0. It is calculated by rounding the value f_0/f_{sync}.

```
P3 : process
variable m : real := 0.5;
        begin
        wait until fsync'event;
        m := f0/fsync;
                if m <=0.5 then n<=1.0 ;
```

Synchronization harmonic determination

A fourth process P4 calculates the free running frequency f_0 of the ILVCO. It is determined by the control voltage and K_{vco}.

```
P4 : process
        begin
        f0<=fini+vctrl*Kvco
end process P4 ;
```

ILO frequency determination

With these four processes, all variables of equations (1) to (6) are determined.

The developed model has been compared with an ILVCO at schematic level. The ILVCO is realized using a 65 nm CMOS technology from STMicroelectronics. The DC current is fixed at 5 mA so we can have a large locking range without any amplitude deviation. The schematic is described in Figure 38.

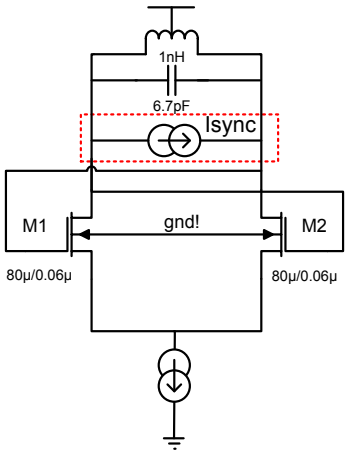


Figure 38: ILO schematic

We apply a pure sinusoidal input signal of 1 mA of amplitude as synchronization signal (doted curve). Its frequency varies during time. We observe the output frequency of the oscillator macromodel (dashed) and of the LC schematic oscillator (solid). In Figure 39 we can see the locking range.

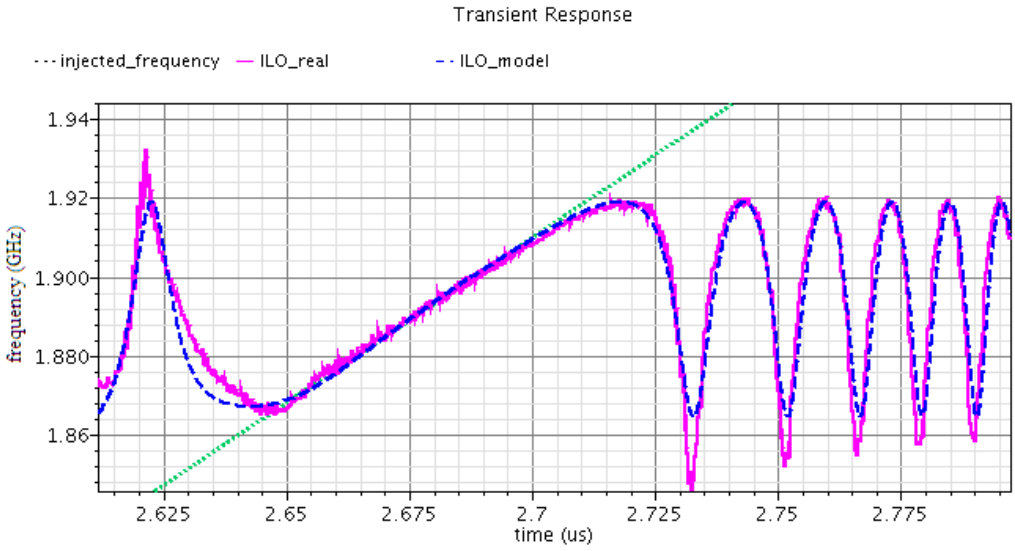


Figure 39: Output frequencies of the ILO and the macromodel for 1 mA injection

The output frequencies of the model and of the LC oscillator are very similar. The locking range and the cycle slipping are nearly the same.

For a higher (2 mA) synchronization signal, we can observe some differences (Figure 40). The output amplitude is modified and the model does not consider those. We are in the case where non-linear effects became dominant.

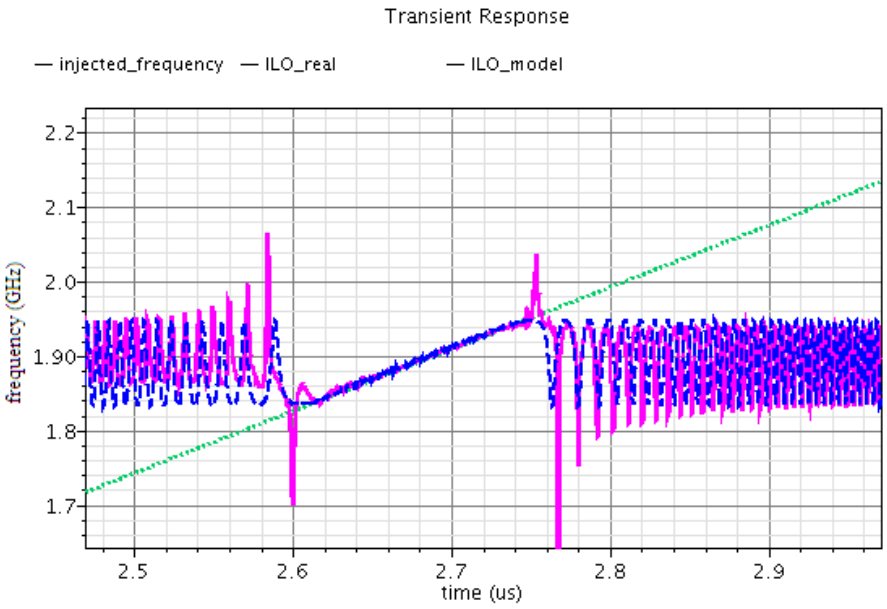


Figure 40: Output frequencies of the ILO and the macromodel for 2 mA injection

The macro model also represents the phase lead or lag. When the injected signal frequency is lower than the ILVCO free running frequency, the ILVCO phase is leading the injected signal. When the injected signal and the ILVCO have the same frequency, the phases are exactly the same. And when the injected signal frequency is higher, the ILVCO phase is lagging.

This can be seen on the Figure 41. Three different synchronization signals are injected: the first is at 1.882 GHz, the second at 1.892 GHz (same as non locked frequency) and the third at 1.902 GHz. The synchronizing signal is a 1 mA peak current. For the same frequency deviation (10 MHz), we can see the same phase offset (30 ps).

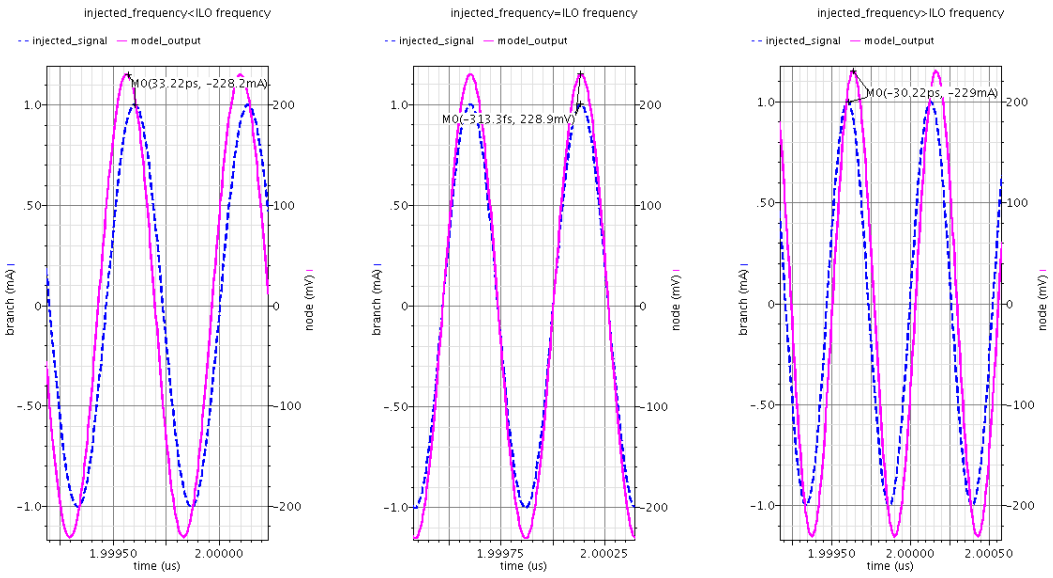


Figure 41: Phase position: lead, lag or in phase

This VHDL-AMS model has been used in high level simulation to validate the CDR architecture faster than with transistor level simulations.

3.1.4 Injection locking techniques

There are several ways to inject a signal in an oscillator. The main goal is to excite one or more components of the oscillator without degrading too much the latter behavior. The injection can be single ended or differential. For a differential oscillator, differential injection is recommended, as it equilibrates the outputs. The injection can be done via an electromagnetic coupling or with an active source which inject current in the oscillator directly. The electromagnetic coupling can be inductive or capacitive. This is generally done by putting a self under or side by side with the oscillator inductance to create a transformer. In millimeter wave design, the inductors are often made with a transmission line [55].

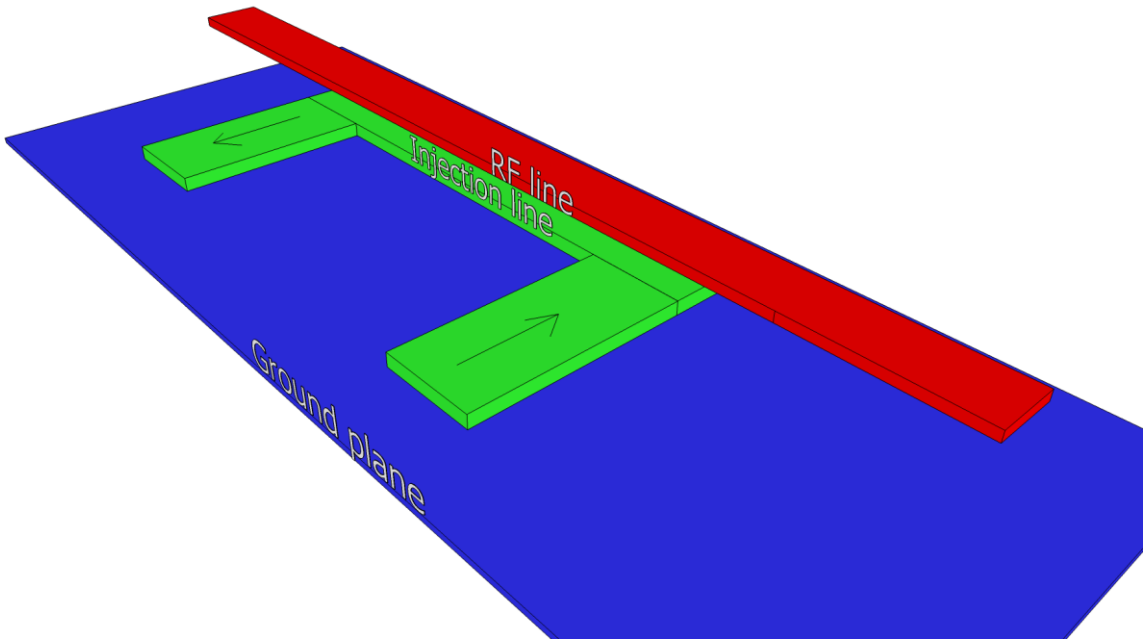


Figure 42: RF line with injection

In Figure 42 the electromagnetic coupling injection method applied to millimeter wave is shown. The oscillator inductor is the upper metal path (red); and under it, there is the injection line (green). A ground plane is present to form a shield (blue). This injection topology needs very accurate electromagnetic simulations to be precisely characterized. Another drawback of this method is the limited use of injected signal harmonics. The injection line is generally optimized for only one frequency. But in serial communication there are several fundamentals, depending of the bit pattern. To improve the injection and the locking range, a

pulse generator is used to generate some pulses at the bit frequency from the data whatever is the bit pattern. The injection line will be most efficient for the clock frequency, where the coupling between the RF line (used as a self), operating at clock frequency and the injection line will be maximal. The voltage amplitude in the injection line controls the synchronization locking range (voltage synchronization).

Another injection method is to inject some current to the oscillator via a current source.

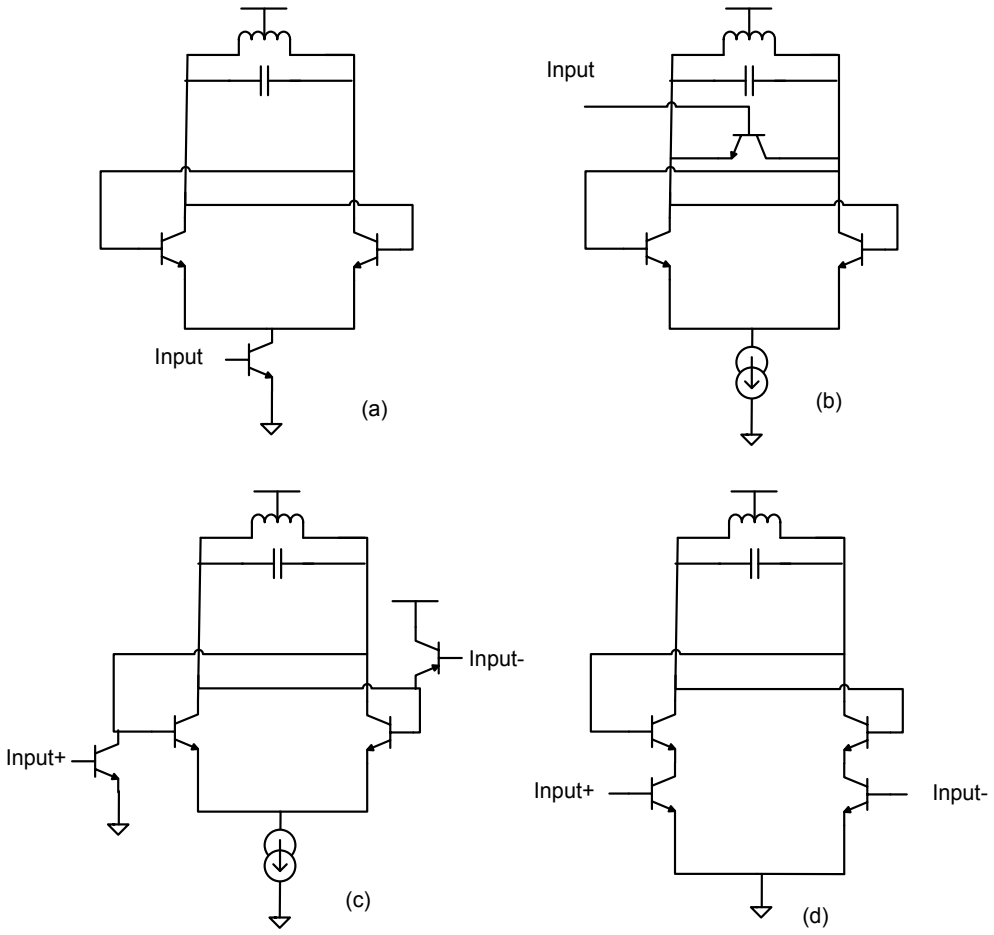


Figure 43: Active injection topologies

Several injection architectures are presented in Figure 43. The first solution is widely used [57] but has the drawback of being single ended. The architecture (b) has the same default and is not symmetrical, in bipolar technology. The biasing of the base of the injection transistor must be higher than the power supply and need another voltage source. The architecture (c) corrects the asymmetry but PNP transistors have low performances. The (d) solution is the differential version of the first and is the injection used in this thesis.

The input transistors increase or decrease the current in the cross coupled transistors and thus inject the synchronization signal. By controlling the biasing of the input transistors, we can

choose the ILO current amplitude and thus the ratio of injected current over oscillator current. This releases the constraint on the voltage swing of the synchronization signal.

3.2 Proposed phase detector

A new phase comparator with a windowed ability is proposed here. The main goal is to lower the number of gates in order to prevent any delay skews between the different phase detector blocks, without compromising the CDR stability, and to decrease the phase comparator operating frequency. Another goal is to longer the zero bit patterns tracking ability. The CDR architecture is the following:

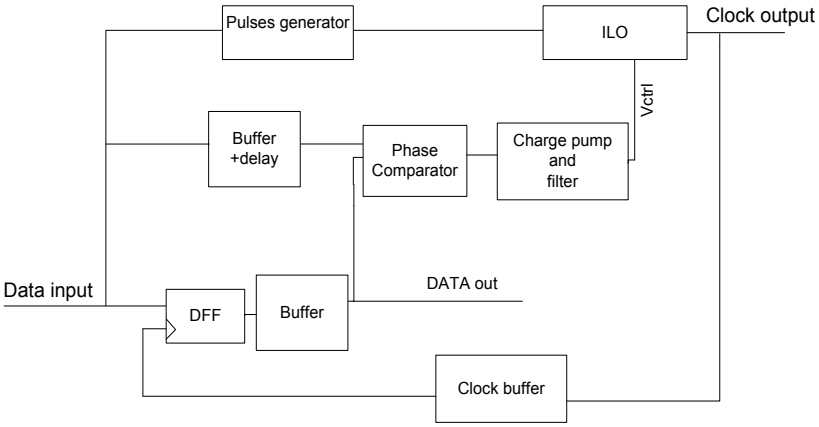


Figure 44: CDR architecture

When data come, they are injected to the ILO through the pulses generator and also compared with the resampled data through the phase comparator. The latter will supply correct information to the charge pump. The charge pump will add or subtract charges to the loop filter. This will increase or decrease the ILO control voltage, and so its instantaneous frequency. When the operating frequency of the ILO is close to the input data one, the clock will be in-phase with the data.

As NRZ data do not have any spectral power at their defined frequency, a frequency doubler or pulse generator is needed. It generates pulses from the difference of time propagation between two paths (Figure 45).

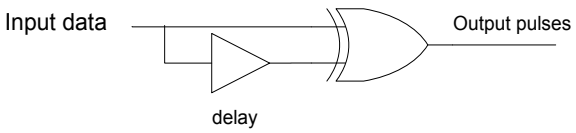


Figure 45: Pulses generator

Ideally the delay is ½ T_{bit} (T_{bit} = bit period). As the data frequency can vary during transmission, the delay is fixed at 1/(2x80e9) seconds, the nominal operating frequency defined by the application. A variable delay can be used, but it adds an order to the loop, and increases the instability of the CDR, so we prefer a fixed one.

Classical CDR systems compare the incoming data with the clock [23][26]. When there is no data transition, the phase comparator interprets this as a phase error and then charges or discharges the loop filter. A solution is to have a data transition detector such as in [26] to compare only when there is data. This solution however still has a problem, as the D-FF must operate at the clock frequency.

At millimeter-wave frequency, there could be some phase errors between the different D-FF (4 in an Alexander phase detector) due to the propagation delay, leading to a sampling error. The proposed solution is to compare the input data with the resampled data. When there is no input data, there will be no output data and then no phase comparison. This also relaxes the frequency constraint on the phase comparator, as the maximum operating frequency is half the clock frequency.

The phase comparator can be linear or binary. In our case, we use a linear one, with a windowed mode. When the phase error between the input data and the sampled data is small, we can assume that their frequencies are very close. Though as we can see in [56], when an ILO frequency is very close to its injected frequency, its phase will lock with it. So the feedback loop can be open. The proposed phase comparator is shown in Figure 46.

The main block of the phase comparator is the D-FF, which gives the phase error signal, like a basic binary phase detector. When both signals are in phase, the XOR opens the switch, and the loop filter output remains constant.

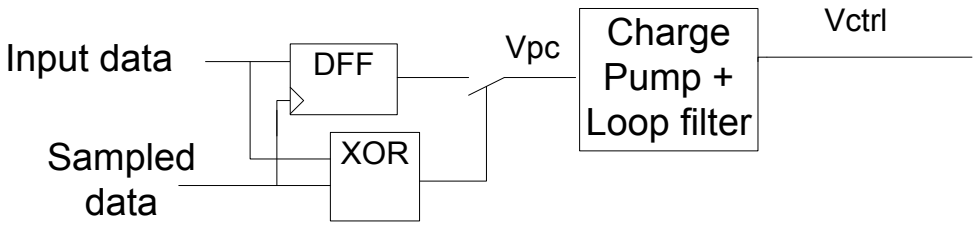


Figure 46: Windowed phase comparator

The phase comparator chronograms are detailed in Figure 47.

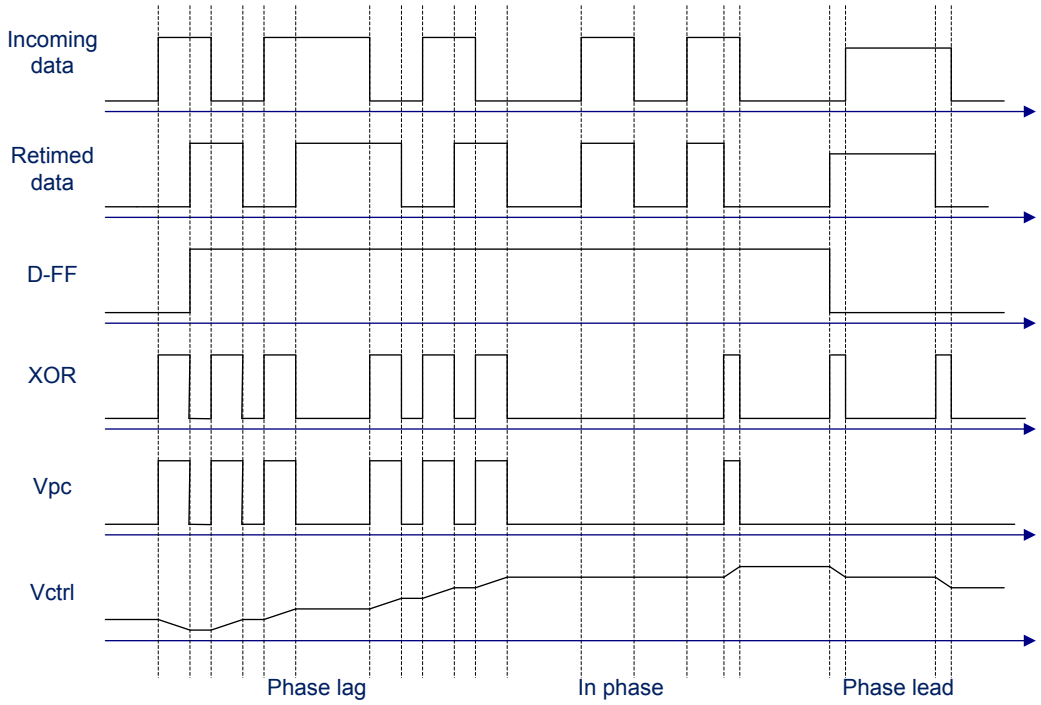


Figure 47: Proposed phase comparator chronogram

The D-FF output will act as an UP or a DOWN signal for the charge pump. The pulses width is proportional to the phase error, which is the definition of a linear phase detector.

The loop filter voltage variations follow the phase error. As the ILO control voltage (V_{ctrl}) only varies when there is a phase error, this voltage remains stable when there is no data transition.

The theoretical transfer functions of a linear, a binary and our proposed solution are shown in Figure 48.

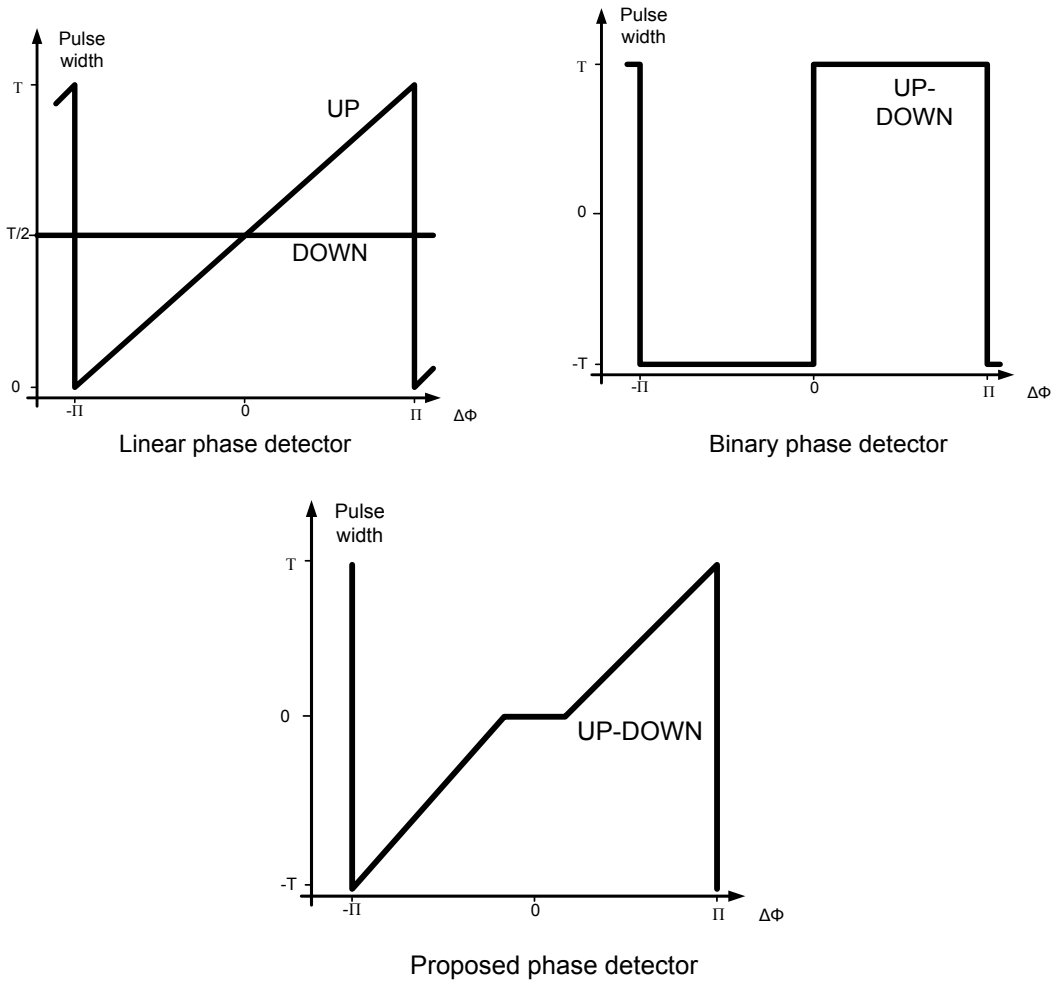


Figure 48: Gain of linear, binary and proposed phase detector

In our proposed topology, the UP and DOWN outputs are a combination between the linear and the binary phase detector. The proposed phase detector generates some pulses with a transfer function similar to a linear one. The widths of the pulses are similar to the ones of a binary phase detector.

3.3 Stability of the ILO based CDR

The stability of the CDR loop is very important, and must be studied. The CDR can be considered in frequency domain, like a PLL. To simplify the analysis, the CDR is considered as a PLL without the sampling block which does not interfere in the feedback loop.

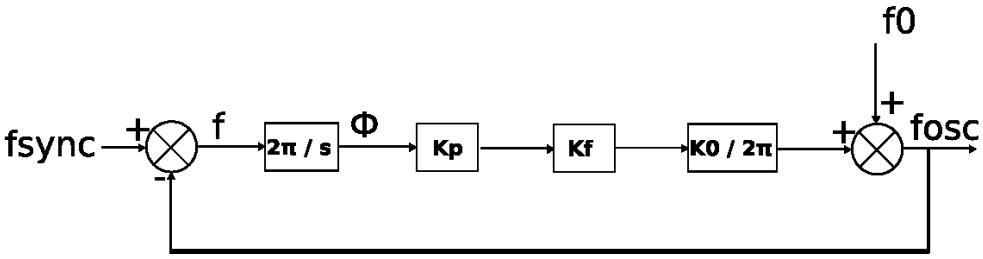


Figure 49: PLL representation

The considered phase comparator is a XOR to simplify its transfer function, with an output from 0 to Vdd. The transfer function is:

$$K_p = \frac{V_{DD}}{\pi} = \frac{2}{\pi}\, V.rad^{-1} \tag{3-29}$$

The maximal output voltage is the power supply, fixed at 2 V.

The loop filter is a basic RC one. Its transfer function is:

$$K_f = \frac{1}{1+RCs} with\ R = 50\ \Omega, C = 5\ pF, \tau = RC = 250\ ps, f_{-3\,dB} = 0.64\ GHz \tag{3-30}$$

These numerical values are the one selected for the designed chip.

This transfer function presupposes that the impedance of the circuit after the loop filter is very important compare to the capacitor one.

The VCO is defined by the natural frequency, and the tuning range calculated by the VCO gain and the loop voltage.

$$f = f_0 + K_{VCO} V_{ctrl} \tag{3-31}$$

From Figure 49, we can extract the transfer function in the open and closed loop of a PLL:

$$OLTF = \frac{K_{VCO} K_f K_p}{s}$$
$$CLTF = \frac{F_{osc}(s)}{F_{sync}(s)} = \frac{K_{VCO} K_f K_p}{s + K_{VCO} K_f K_p} \tag{3-32}$$

With an ILO, the PLL becomes:

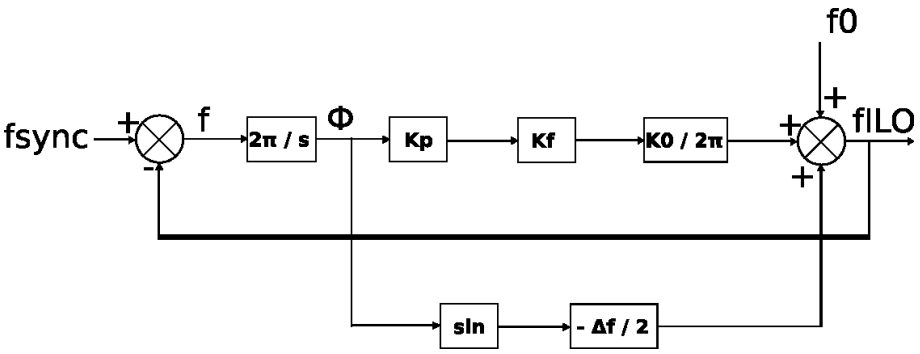


Figure 50: PLL with injection representation

Figure 50 is based on Huntoon and Weiss theory described previously. The output signal frequency (f_{ILO}) is:

$$f_{ILO}(t) = f_{vco}(t) + f_0 - \frac{\Delta f}{2}\cos(\Phi(t) + \beta) = f_{vco}(t) + f_0 - \frac{\Delta f}{2}\sin(\Phi(t)) \qquad (3\text{-}33)$$

By inserting (3-22) in (3-25) we get β=-π/2. Δf is the locking range and Φ the phase error ($\Phi = \Phi_{sync} - \Phi_{ILO}$).

The proposed CDR use a ILO in a PLL to solve some problems on the ILO based CDR. In ILO based CDR, sometimes the ILO will not lock on the injected signal but will try to synchronize on recombination harmonic and will fail:

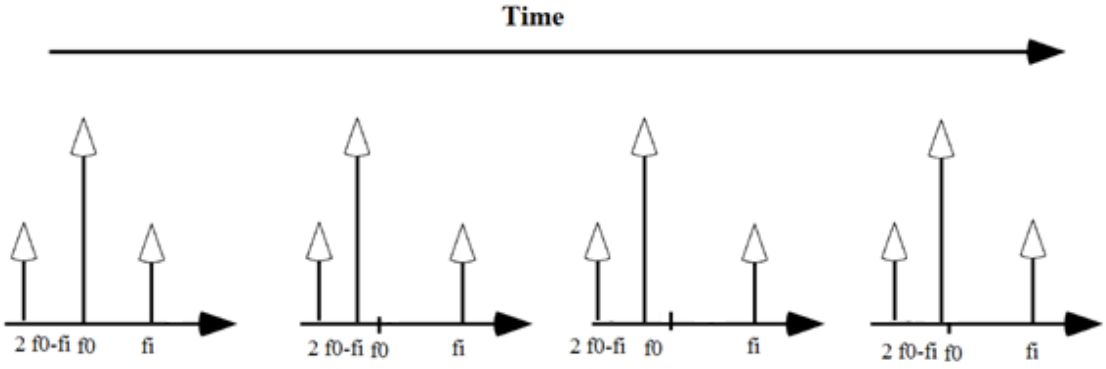


Figure 51: Synchronization on 2f0-fi

In this case, the ILO can't lock correctly and thus generate a lot of jitter. Another problem occur when the injected signal is at the limit of the ILO locking range, the phase cycle slip as we can see on Figure 39. In our case the ILO locking range is extended because we use an ILVCO (Injection Locked Voltage Controlled Oscillator). The proposed CDR solves these two issues because the free running oscillation frequency matches always the synchronized frequency.

We can define:

$$f_{aux}(t) = \frac{\Delta f}{2}\sin\left(\Phi_{sync}(t) - \Phi_{ILO}(t)\right)\ [Hz] \tag{3-34}$$

Due to the sinus function, we can apply a Taylor development on order 1 when $\Phi_{sync} \approx \Phi_{ILO}$. Another approximation is to consider the sinus function as a variation from [-1;1], which will be used later.

The Fourier transformation gives:

$$\begin{aligned} F_{ILO}(s) &= F_{VCO}(s) + \frac{f_0}{s} - \frac{\Delta_f}{2}\Phi(s) \\ &= F_{VCO}(s) + \frac{f_0}{s} - \frac{\Delta_f}{s}\pi F_{sync}(s) + \frac{\Delta_f}{s}\pi F_{ILO}(s) \end{aligned} \tag{3-35}$$

with:

$$F_{VCO}(s) = K_{VCO}K_fK_p(F_{sync}(s) - F_{ILO}(s)) \tag{3-36}$$

We obtain:

$$F_{ILO}(s)\left[1 - \frac{\Delta_f}{s}\pi\right] = K_{VCO}K_fK_p\left(F_{sync}(s) - F_{ILO}(s)\right) + \frac{f_0}{s} - \frac{\Delta_f}{s}\pi F_{sync}(s) \tag{3-37}$$

and so the CLTF of the injection locked PLL:

$$\frac{F_{ILO}(s)}{F_{sync}(s)} = \frac{K_{VCO}K_fK_p - \Delta_f\pi}{s + K_{VCO}K_fK_p - \Delta_f\pi} = \frac{K_{VCO}K_p - \Delta_f\pi(1+RCs)}{s(1+RCs) + K_{VCO}K_p - \Delta_f\pi(1+RCs)} \tag{3-38}$$

f_0 does not influence the result as due to the feedback.

From the Harold-Black formula, we extract the OLTF:

$$OLTF = K_{VCO}K_fK_p - \frac{\Delta_f}{s}\pi$$

The injection locked PLL is an order 2. The poles are:

$$\begin{aligned} s_0 &= \frac{K_{VCO}K_p - \Delta_f\pi}{\Delta_f\pi RC} \\ s_{1/2} &= \frac{(\Delta_f\pi RC - 1) \pm j\sqrt{|\Delta|}}{2RC} \end{aligned} \tag{3-39}$$

where:

$$\Delta = \left(1 - \Delta_f\pi RC\right)^2 - 4RC\left(K_{VCO}K_p - \Delta_f\pi\right) \tag{3-40}$$

This is only valid when $\Phi_{sync} \approx \Phi_{ILO}$. When $\Phi_{sync} = \Phi_{ILO}$, the injection locked PLL is similar as a PLL without injection. For the other case, we estimate the sinus variation as a modulation of the Δ_f term in the transfer function. The extreme of f_{aux} are $\Delta_f/2$ and $-\Delta_f/2$.

The Bode plots in Figure 30 and 31 have been done with the following values:

$$K_{VCO} = 3\ GHz.V^{-1}$$

$$K_f = \frac{1}{1 + RCs} \qquad with\ R = 50\ \Omega, C = 5\ pF \Rightarrow f_{-3\ dB} = 0.64\ GHz$$

$$K_p = \frac{2}{\pi} V.rad^{-1}$$

$$\Delta_f \approx 100\ MHz$$

Δ_f varies from its maximal value (100 MHz) on the red curve and is divided by 10 at each curves.

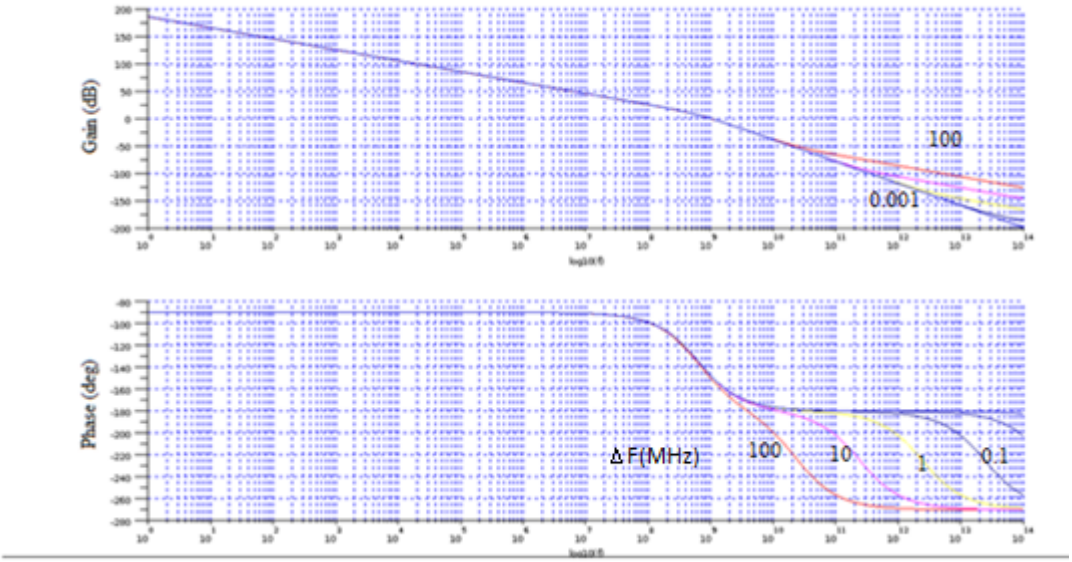


Figure 52: Bode diagram in open loop for $f_{aux}>0$

As expected, the gain curves are similar, only the phase curves vary. When Δ_f is small (1 kHz), the injection locked PLL is close to a classical PLL.

The phase margins are 30°-35°. The gain margins vary a lot, and the phase delay is clearly visible in Figure 52.

A similar experiment is done for the loop filter. The RC filter must be carefully selected to allow a fast and stable PLL.

The study is done with and without injection. The red curve is for a small filter and the green one for a large one.

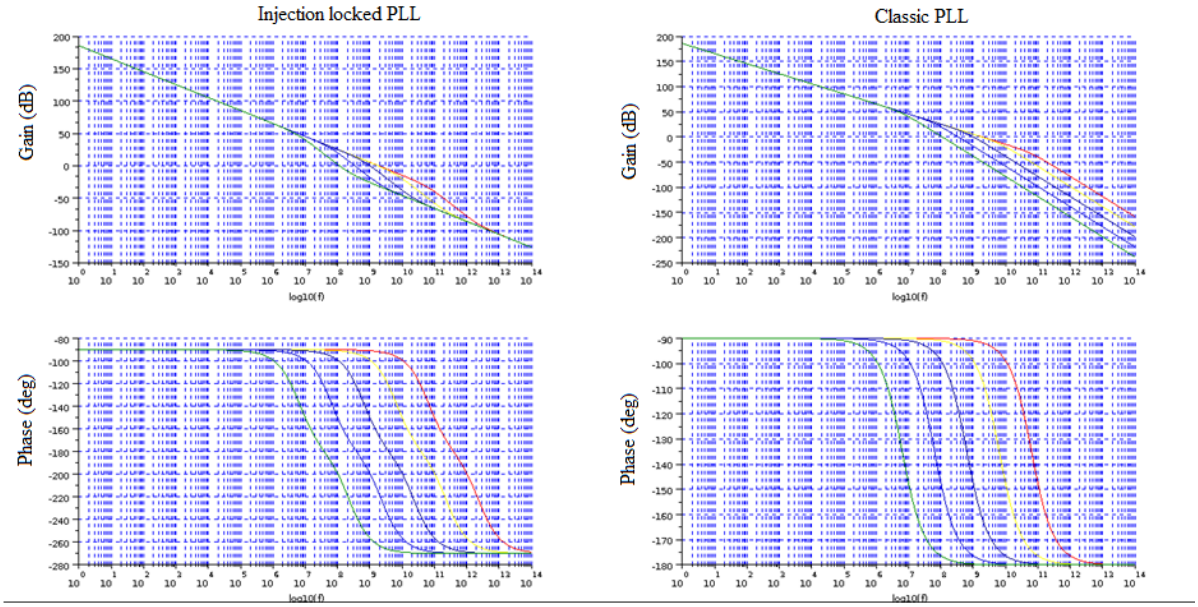


Figure 53: PLL stability

For the PLL without injection, with the previously selected RC filter, the natural frequency is ω_N=2.7e9 rad/s, the cut of frequency is ω_c=4e9 rad/s, and the damping factor equals 0.72, which provides an optimal flat response. However the damping factor, the cut-off frequency and the conversion gain are linked and we cannot improve the static phase offset without degrading the settling time.

The injection locking acts as a 2nd order filter, by injecting a zero pole. The injection shifts the phase curve with a rebound, and delays the -180° crossing at higher frequency.

3.4 SiGe technology: BiCMOS9mW

To meet the requirements in speed, cost and available technology at the laboratory, we use hetero junction bipolar transistor built in SiGe, BiCMOS process from STMicroelectronics. A high f_{max} is needed when operating at high frequency, up to 6-8 times higher than the operating frequency if possible. The goal is to have as much harmonics as possible in order for a square wave signal to appear as square as possible. This is clearly identifiable in the following figure:

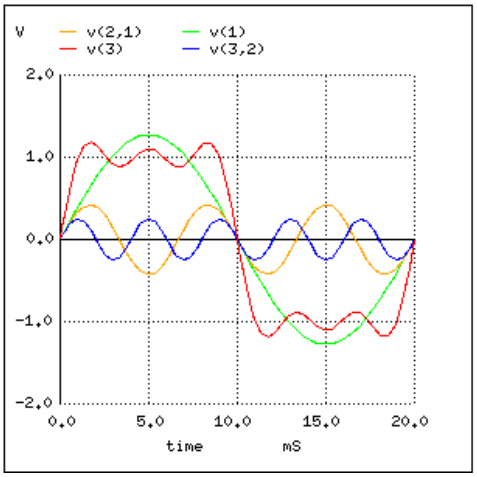


Figure 54: Sum of 1st, 3rd and 5th harmonics approximates square wave.

The BiCMOS technology is a good trade-off between the f_{max}, the power consumption, and the Gm between CMOS, BiCMOS and GaAs process.

3.4.1 Bipolar transistor

The bipolar transistor is formed by two PN junctions with a very thin P region to obtain the transistor effect. The P region is the base; the two N regions are the collector and the emitter. The collector current is controlled by the base voltage variation. The operating regions of the bipolar transistor can be seen:

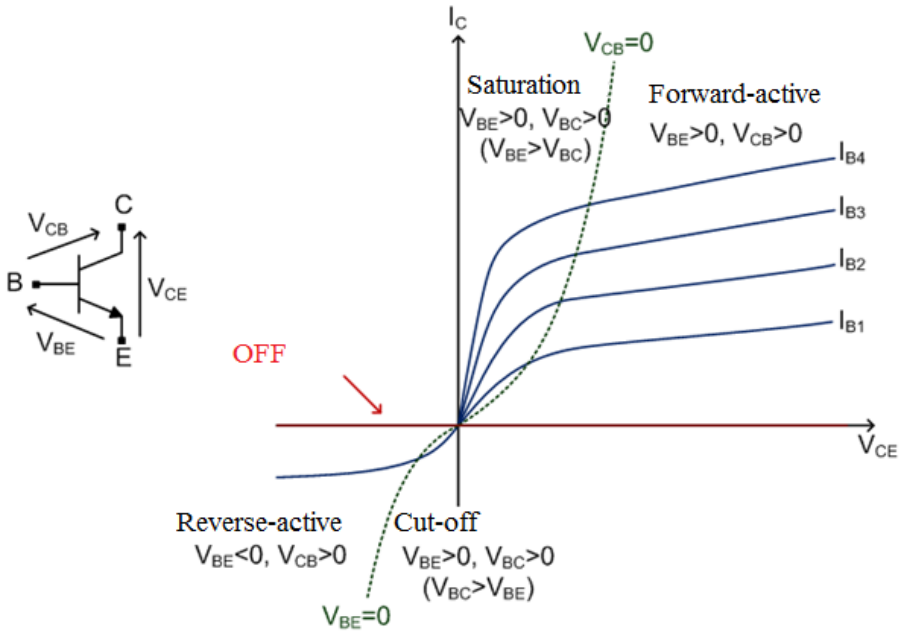


Figure 55: Bipolar transistor operating region

There are 5 operating regions, the four visible one in Figure 55, and the avalanche breakdown region. Forward-active region is used in amplifier and saturation region in TTL logic.

The base and emitter doping determine the transistor performances. To improve the latter, hetero junction transistor is used. The base and emitter materials are different to lower the number of holes injection from the base to the emitter. This can be seen in Figure 56.

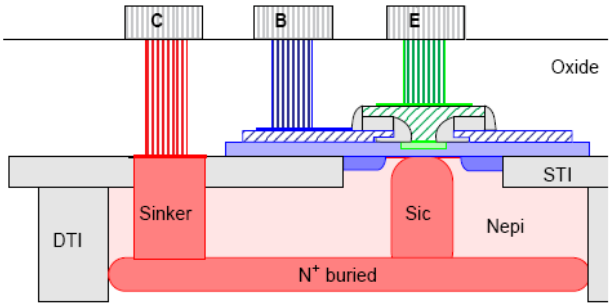


Figure 56: HBT SiGe from STMicroelectronics

3.4.2 Unit gain frequency f_T

The transit frequency or unit current gain frequency is related to the transition time of a charge from the collector to the emitter under forward-active operating. It is calculated from the hybrid pi model which represents the parasitic capacitors. It depends on the transit time.

$$f_T = \frac{1}{2\pi.\tau} \tag{5-41}$$

The transit time is the average time the carriers need to cross a region and it equals:

$$\tau = \frac{C_{BE}.nV_T}{I_E} + \frac{W_B^2}{2.D_{nB}} + \frac{x_{d,BC}}{2.V_{sat}} \tag{5-42}$$

With C_{BE} the base-emitter parasitic capacitor, n the ideality factor, $x_{d,BC}$ the base-collector depletion region width. As we can see, the smallest is the transit time, the parasitic capacitors and resistors, the higher the f_T is. This leads to very small transistors. Another way to improve the speed is to have a high collector current to have a high current density. The corresponding schematic is:

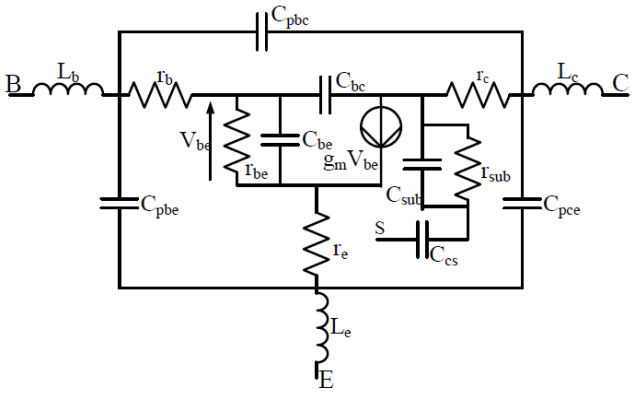


Figure 57: HBT small signal schematic

The f_{max} and ft of the available transistors are given in the DK (Design Kit). For different configurations and current we can choose the appropriate transistor for the desired use.

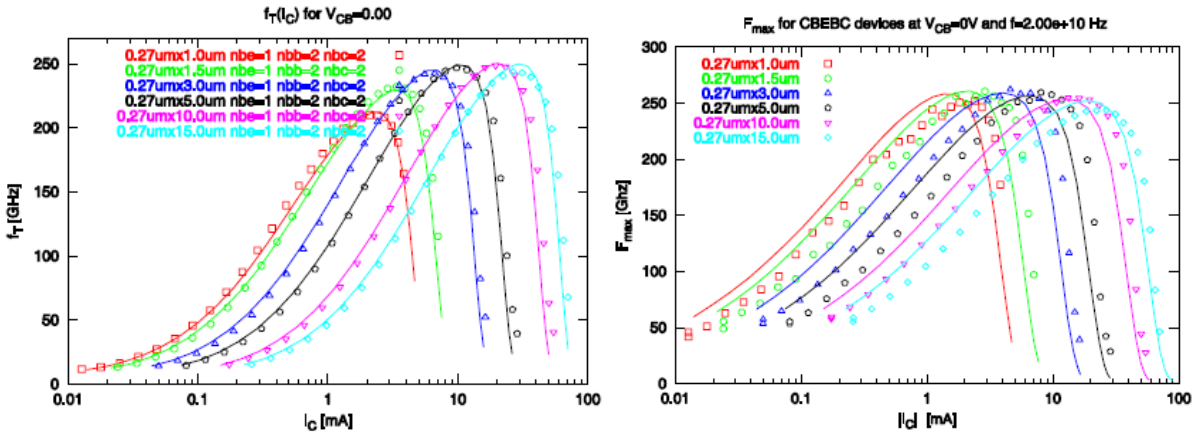


Figure 58: f_t and f_{max} for several transistors

As we can see in Figure 58, the maximal ft is obtained for large transistors (15 µm) but at the cost of high power consumption (30 mA). The number of base, collector and emitter contacts also contributes to the ft, and are given on Figure 59:

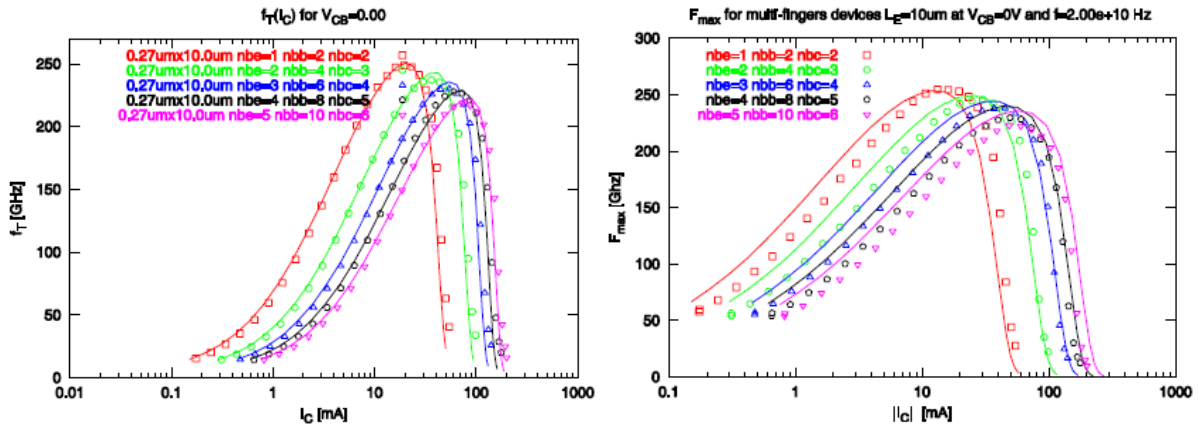


Figure 59: ft and fmax variation regardless of the number of emitter, base and collector

STMicroelectronics propose several transistor layouts. The number of base, collector and emitter contacts can be selected: the transistor can have one emitter, one base and one collector (CBE), or two bases and one emitter, one collector (CBEB). The last option is two bases, two collectors and one emitter (CBEBC). The number of emitters can be selected, thus affecting the number of base and collector.

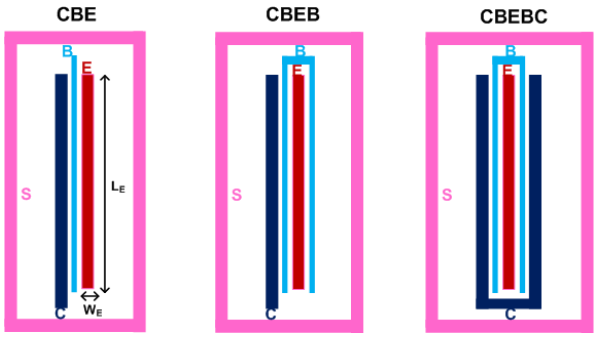


Figure 60: Three available HBT configuration

From the process documentation curves, the best trade-off between ft and power consumption is the 5 µm CBEBC transistor with 7.5 mA collector current biasing. This transistor will be the unit block for all the system design. The thermal effect is taken into account and the temperature influence can be seen Figure 61:

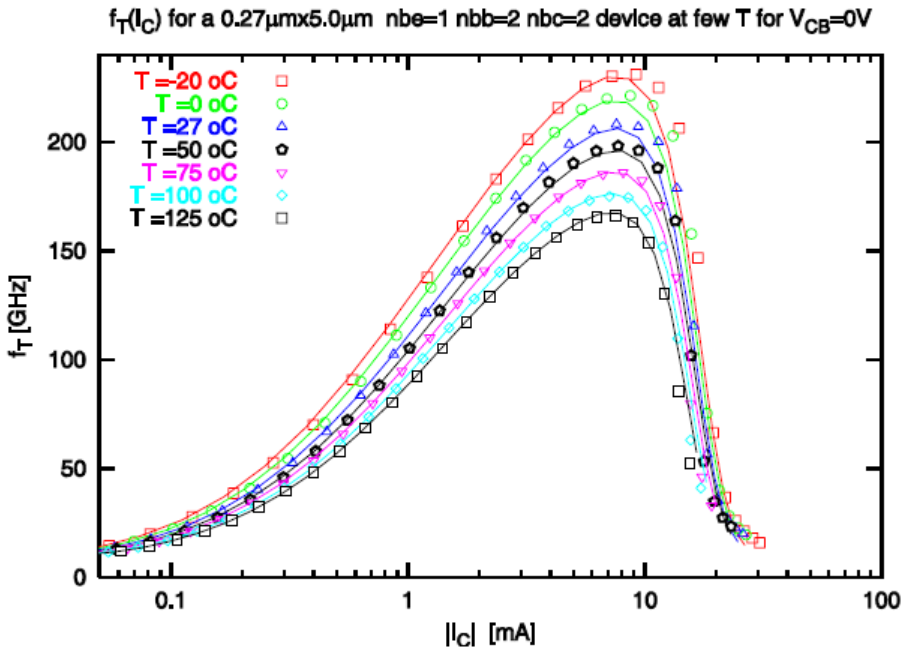


Figure 61: Temperature effect on ft

It is important to keep the chip as cold as possible to maximize the ft. The simulations were done at 70°C to approximate the thermal heating.

Another source of parasitic capacitances is the metallization layer (Figure 62). The HBT transistor (view in cut) has some metallic's access (3D view).

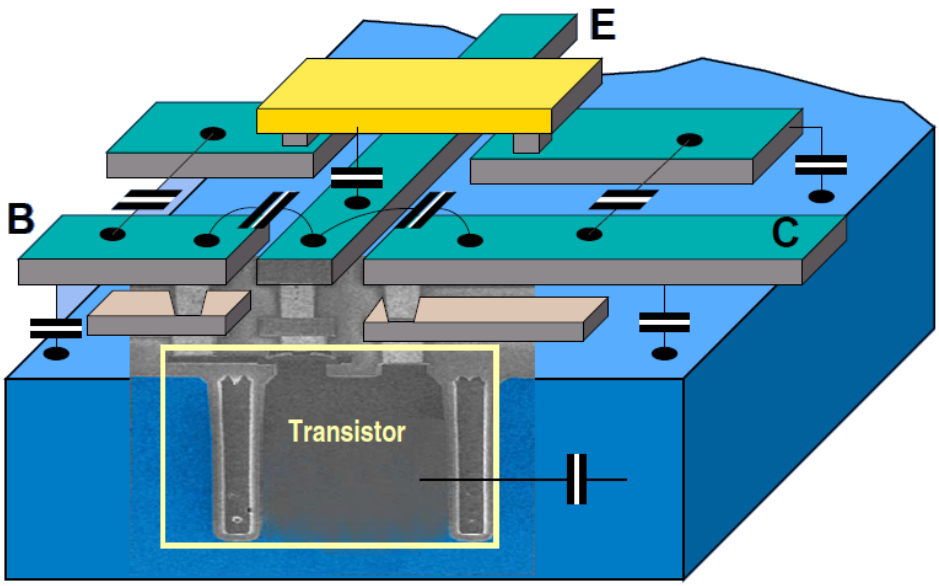


Figure 62: HBT with its access

The capacitances values depend of the width of each metal path, and of the space between two paths. The width is determined by the electromigration, which impose a minimum metal cross-section area to prevent any failure during the circuit life. The fabrication process fixes the minimum space between two metal paths. As the capacitance is inversely proportional as the distance between the two paths, the temptation to increase it is big but must be avoided as it increases the transmission line length.

To decrease parasitic capacitances from metal to substrate, the BiCMOS9mW have a special back-end optimize for RF. The metal layers are thicker and higher than in CMOS technology.

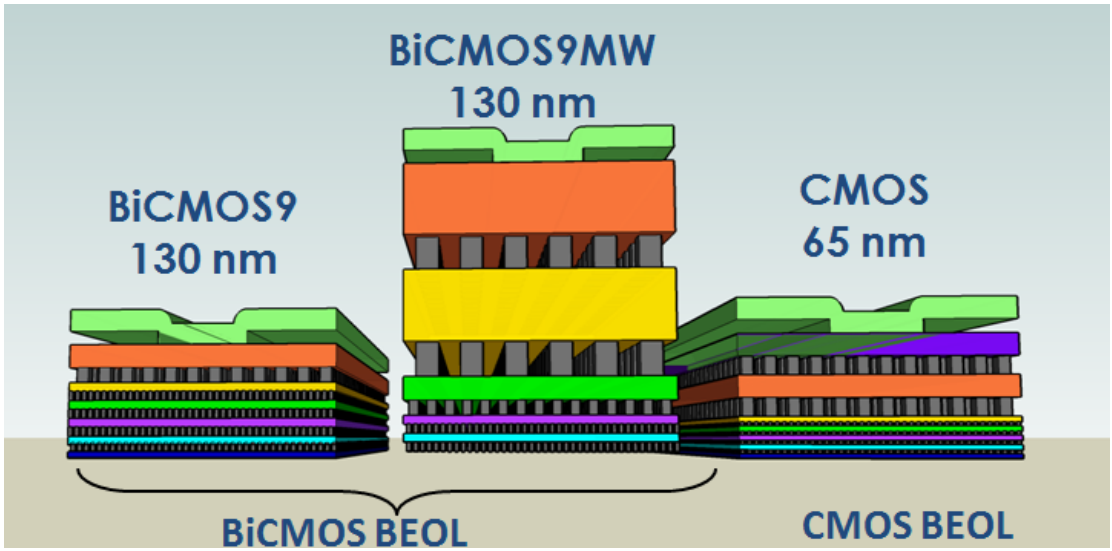


Figure 63: Metal layer on different technologies

Thick metal layer help to reduce the resistivity of a line. As the frequency increase, the skin effect becomes dominant and all the current is present on the skin of the path. By having a thick metal, there are no needs to increase its width.

3.4.3 Microstrip line

In millimeter wave, any interconnection generates a phase shift due to the propagation delay, and some losses or coupling. This effect must be simulated to have a schematic as close to the final circuit as possible. In the design kit, microstrip lines are proposed to do interconnection, and a model is associated.

Microstrip lines are built in metal 6 and alucap to reduce the losses. A ground pattern is done in metal 1 and 2, and is connected to some lateral wall done by stacking metal 1 to 6. This creates a shield to prevent coupling with any other interconnection (Figure 64).

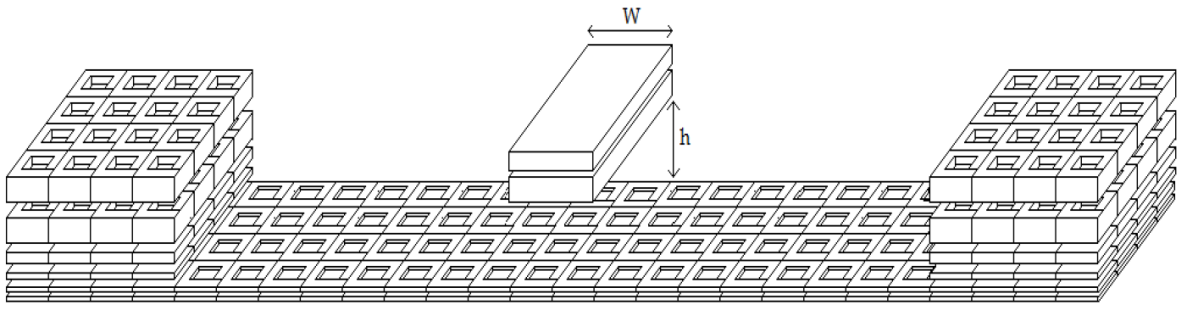


Figure 64: BiCMOS9mW microstrip line

The following figure shows the magnetic and electric field on the microstrip line.

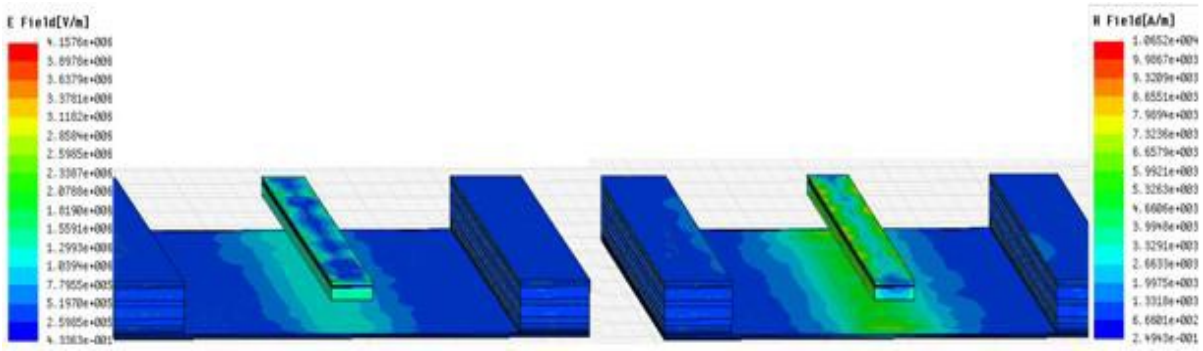


Figure 65: Electromagnetic field of a microstrip line on HFSS

The electric and magnetic field are well confined in the microstrip line walls. The current is present on the skin as expected. The skin depth can be seen Figure 66.

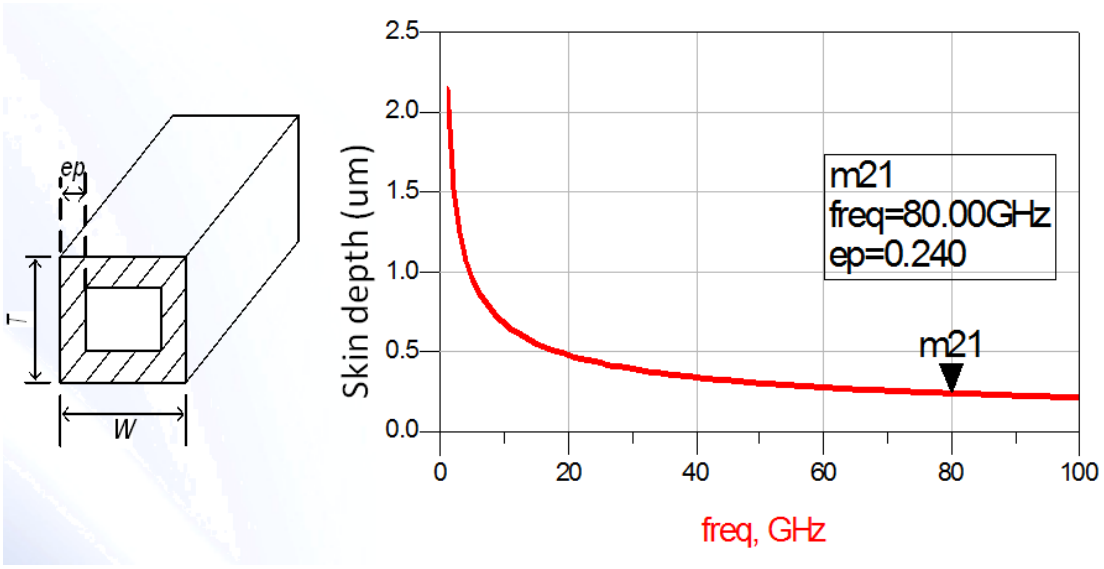


Figure 66: Skin effect for a metal wire

STMicroelectronics give a model in the design kit. This model has been compared with an electromagnetic simulator (HFFS).

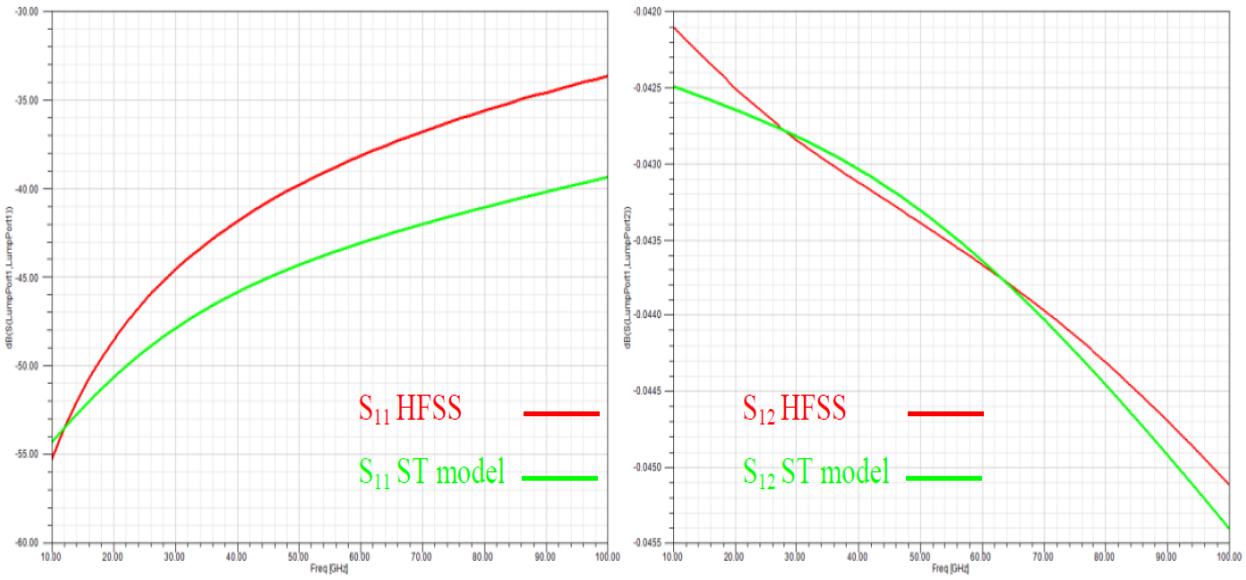


Figure 67: S11 and S21 parameters for a 100µ*12µm microstrip line

The STMicroelectronics model is quite accurate and has been used during the design as the convergence during transient simulation is far better than with the HFSS extracted S parameters.

In order to be called a microstrip line, the walls are at 42 µm of the line, creating a big structure not very convenient for the layout.

The design kit also gives some high performances capacitances. They are metal insulator metal (MIM) type with access on the highest metal, ie the alucap.

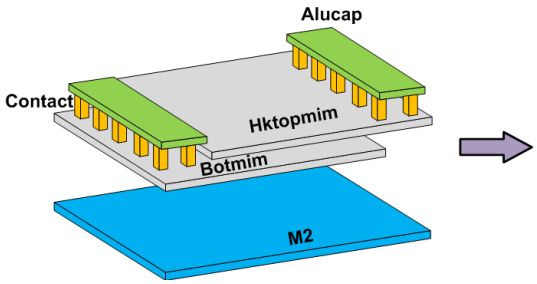


Figure 68: MIM capacitance

The quality factor depends of the geometry and can be improved as we can see on Figure 69:

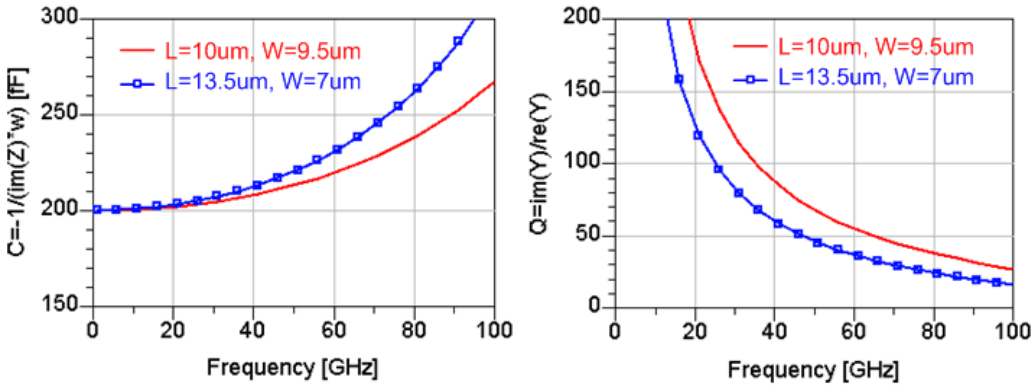


Figure 69: Quality factor improvement

To have the highest quality factor, the capacitance must be as square as possible.

The pad size is fixed by the design rules. An open pad has been measured to see its performances:

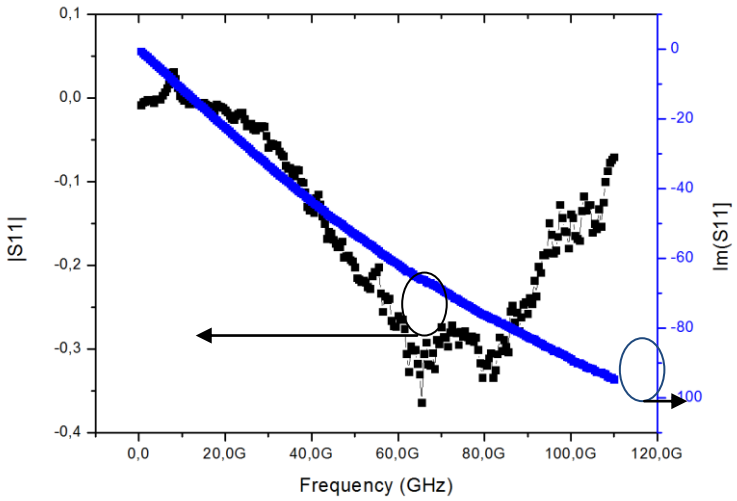


Figure 70: S11 parameter of the RF plot

At 80 GHz the capacitance value is 26.14 fF. This pad is not very well suited for millimeter wave application. However, the parasitic extractor gives us a capacitor of 29 fF, so the Post Layout Simulations (PLS) should be accurate.

Chapter 4

CDR design and measurements

4.1 Cell based design

In digital designs, blocks are built to fit together easily, in a layout point of view. This is the cell based concept. The FPGA (field programmable gate array) is a typical example of this concept [58]. A standard block is duplicated without design or layout modification and repeated in the chip (Figure 71). The input and output metal accesses are the same for all the different blocks in order to simplify the layout. When the basic cell is done or supplied by a founder, the high level description is automatically converted into a layout with the appropriate tools.

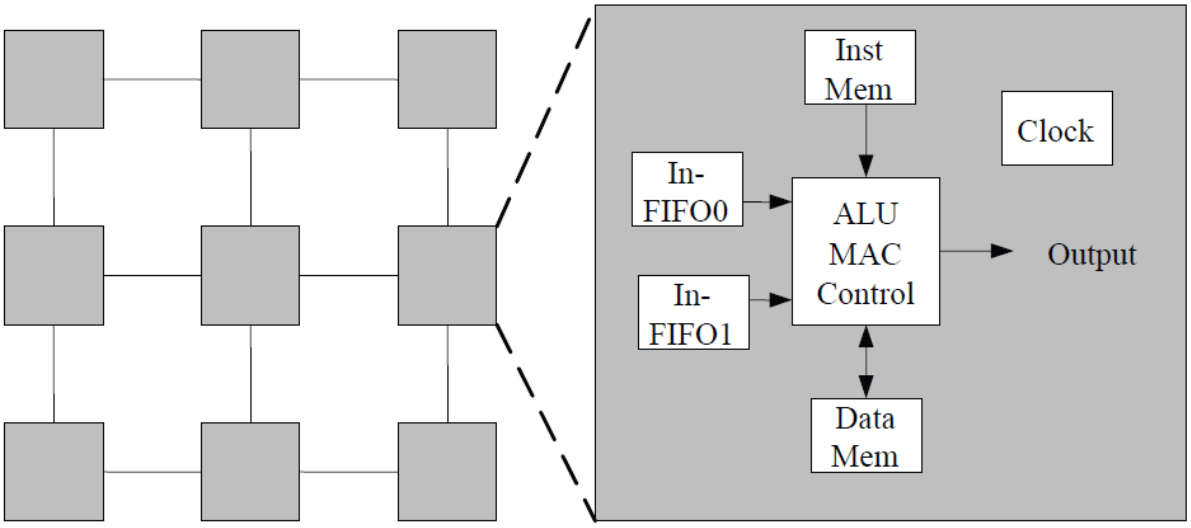


Figure 71: Cell based array

The cell-based approach is very powerful but in our case, the cell needs to be fully designed to match the performances. At the beginning of the design, several choices have to be done, like how to do interconnections, which electrical levels to use… Some design advices are given in [48], and have been used to design the CDR such as the power supply network and the signal routing which greatly impact the overall design performances. Another concern is to transmit all the received bits, even if there is a long zero pattern. This eliminates all

capacitances on the data path to allow a DC level. All blocks must work from DC to clock frequency.

In our design, one big concern is the impedance mismatch. Any signal path is a succession of transistor with strongly mismatched input and output. A wrong impedance matching results in high losses and the signal we want to resample can be seriously degraded at the CDR output.

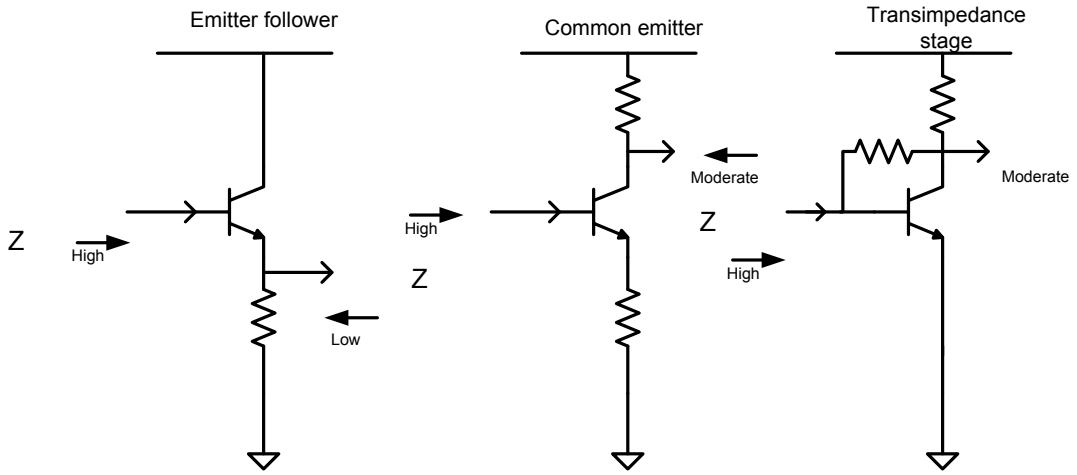


Figure 72: Impedance of common circuits

The selected topology (Figure 72) for each stage in the CDR was an emitter follower as input and a common emitter as output. Thus the impedance matching is correct on a wide band on one side and the signal DC level can be adjusted to select the correct biasing. This is an ECL topology. It makes possible to drive large capacitive loads with small delay and the output structure supports a large fan-out.

Another concern is the path between two blocks. If the metal wire is too wide, it will be highly capacitive and will act as a low-pass filter. A low-pass filter is problematic in data communication as the signal is not periodic, thus an offset can appear.

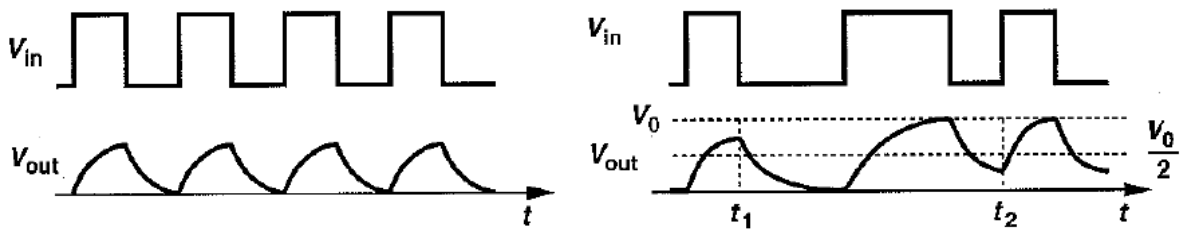


Figure 73: Low pass filter effect on data

To cancel the capacitance that limits the bandwidth, an inductor is used to resonate with the capacitance, thus improving the speed. The overshoot and peaking must be well controlled to be compliant with random data. In millimeter wave the inductor is done with microstrip line.

Another critical point is the noise propagating on bias line. To reduce it, when it is due to fast commutations, all blocks are fully differential. As even differential circuits generate noise, a power supply plan with integrated small capacitor fills every unused place in the layout. The supply plane is done with small metal square stacked. Metal 1 & 2 are used for the ground path and metal 3 to 6 are dedicated to the supply voltage. On long and sensitive path, such as the loop control wire, the signal is on metal 3 and a shield is made with other metal levels which are connected to the ground (Figure 74). This is similar to the supply plane.

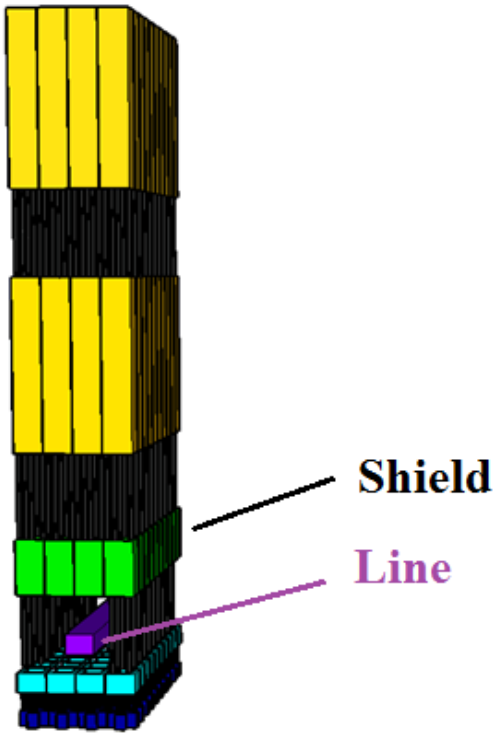


Figure 74: Shielded control line

4.2 Data buffer

Data buffer are present to cancel the losses of metal paths. As they generate some jitter, they must be used with parsimony. It is a very simple block: two common collector blocks

followed by a differential pair (Figure 75). The output voltage is 2 V-1.73 V. This voltage level is used as a standard for the interconnection in all our blocks. The current in the differential buffer collector is 7.5 mA as stated in previous chapter. The power supply is fixed at 2 V.

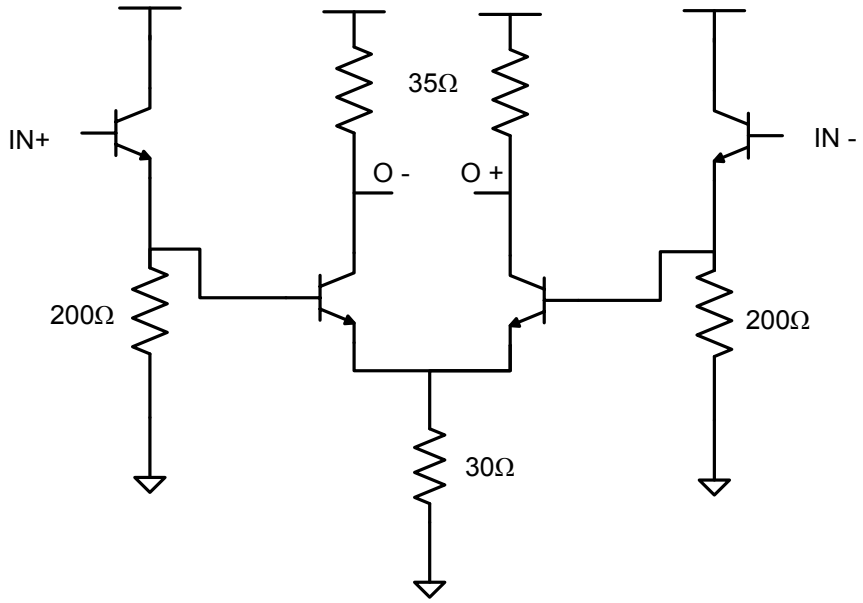


Figure 75: Data buffer schematic

The emitter follower has a little voltage swing drop; the output is only 225 mV peak to peak. The buffer cut-off frequency is over 40 GHz to ensure that no data are lost.

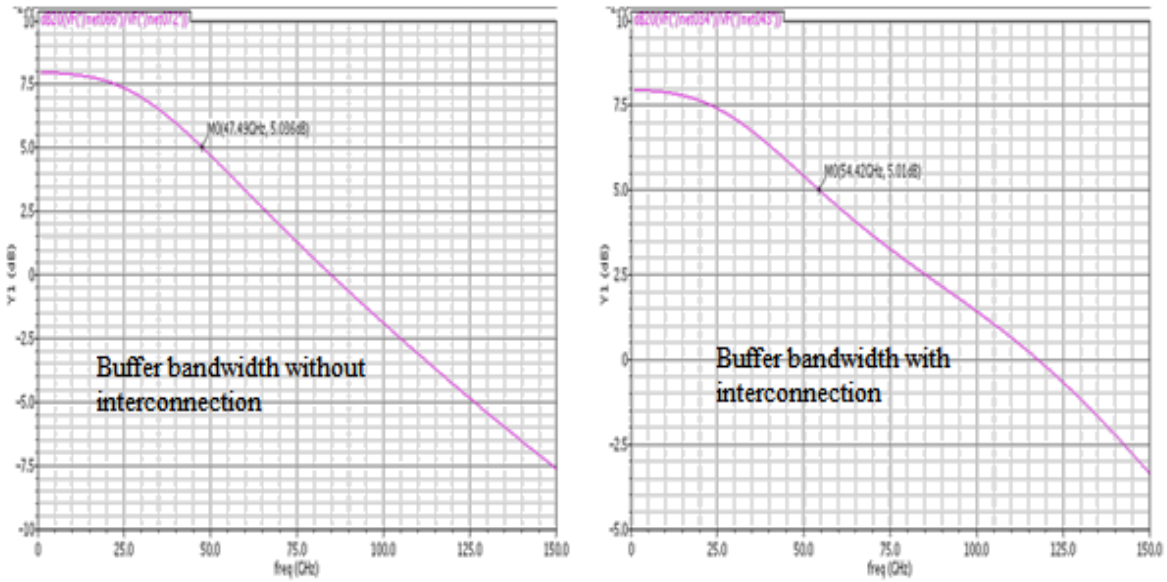


Figure 76: Buffer bandwidth without and with interconnection

The buffer has been studied with and without interconnection to see their influence. As we can see on Figure 76, the interconnections are favorable (7 GHz improvement) and act as

shunt peaking. The bandwidth can be improved with a true shunt peaking on the differential pair load, but the total area of a buffer is too big for a good integration, as each inductive load is done with a microstrip line (200 µm long and 10 µm width). The total inductive load size is 200 µm*80 µm and is too big to be integrated.

4.3 Injection Locked Oscillator

The ILVCO is the main block of the CDR. It will generate the clock and so must be able to oscillate at the right frequency and to have enough output voltage swing. An ideal oscillator is presented Figure 77. The LC tank is lossless. If the capacitor is charged, when the switch is closed a sinusoidal voltage across the resonator appears, depending of the initial conditions and the L and C values.

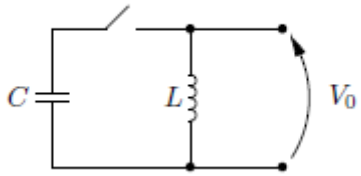


Figure 77: Ideal LC resonator

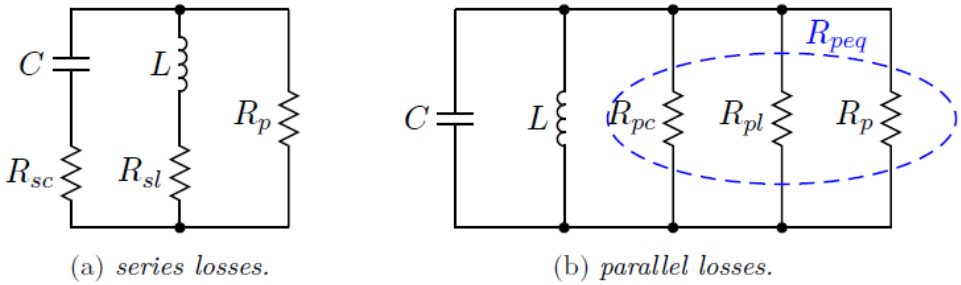
The frequency of the output voltage is defined by the following equation:

$$f_0 = \frac{1}{2\pi\sqrt{L.C}} \quad (4\text{-}43)$$

The ideal tank with lossless component will oscillate indefinitely but it is not realist. The capacitor and the inductor will have some losses represented as resistors in serial (R_{sc}, R_{sl}) and parallel (R_p)

$$Q_L = \frac{\omega.L}{R_{sl}} \quad (4\text{-}44)$$

$$Q_C = \frac{1}{\omega.C.R_{sc}} \quad (4\text{-}45)$$



(a) *series losses.* (b) *parallel losses.*

Figure 78: Serial and parallel tank losses

Q_L and Q_C are the inductor and capacitor quality factors. The quality factor (Q_T) and characteristic impedance (Z_0) of the total tank are:

$$Z_0 = \sqrt{\frac{L}{C}} = \omega_0 . L \tag{4-46}$$

$$R_{peq} = R_p // R_{pl} // R_{pc} \tag{4-47}$$

$$Q_T = \omega_0 . C . R_{peq} \tag{4-48}$$

$$\frac{1}{Q_T} = \frac{Z_0}{R_p} + \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4-49}$$

As we can see the resonator quality factor is dominated by the lowest quality factor component. To cancel the losses introduced by the resistor R_{peq}, a negative resistor can be inserted. The negative resistor must be at minimum equal to R_{peq}. It can be done by using active devices. The resonator can be single ended or differential. The differential output voltage from Figure 85 can be calculated:

$$V_{out,diff} = \frac{4}{\pi} . I_{bias} . Z_0 Q_T \tag{4-50}$$

To be able to vary f_0, we must vary L or C values as seen in eq. 4-43. To vary an integrated inductor is complicated so LC oscillators use variable capacitors. The tuning range of a VCO is:

$$TR = \frac{\Delta f}{f_0} \tag{4-51}$$

The varactors are made with diode mounted NPN transistors. The parasitic capacitance deteriorates the tuning range by adding a fixed capacitance. To reduce the parasitic capacitor influence, we can use large varactor value. In order to keep an identical f_0 the inductor must be reduced according to eq. 4-1. The varactor tuning range is from 0 to V_{dd}. The variable capacitance is made with the reverse biased collector-base junction; this increases the width of the depletion region. The parasitic emitter-base capacitance is isolated from the collector-base capacitance by maintaining the base-emitter junction in a reverse biased condition. When V_{tune} is high, it increases the depletion region and decreases the capacitance.

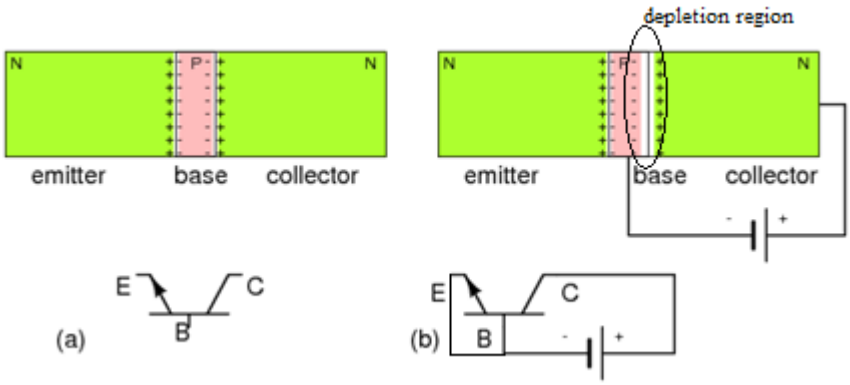


Figure 79: (a) NPN junction bipolar transistor. (b) Apply reverse bias to collector base junction

The capacitor tank has been studied in Z parameters with the following equations:

$$C = \frac{-1}{Im(Z).2\pi.f} \tag{4-52}$$

$$Q = \frac{|Im(Z)|}{Re(Z)} = \frac{1}{\omega.C.Rc} \tag{4-53}$$

The capacitance and the quality factor vary with V_{tune}. In our case, the capacitor tank value varies from 61.75 fF to 67.43 fF.

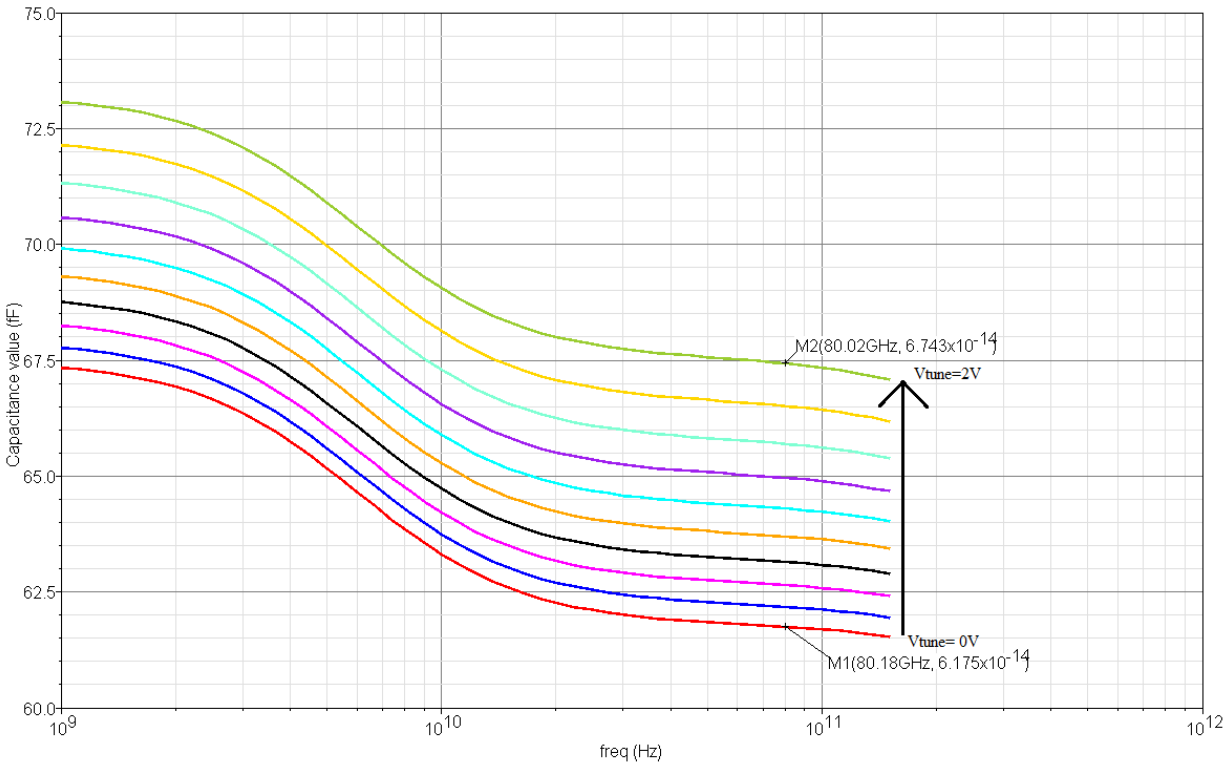


Figure 80: Capacitor tank tuning range

To improve the quality factor, transistors with a lot of finger and small width have been preferred as it reduces the base collector access resistors. On the other hand, increasing the number of fingers rises the fixed parasitic capacitance of interconnects, reducing the tuning capability of the varactor. The selected transistor is 10 µm width and has the maximal number of fingers allowed by the DK (Figure 81).

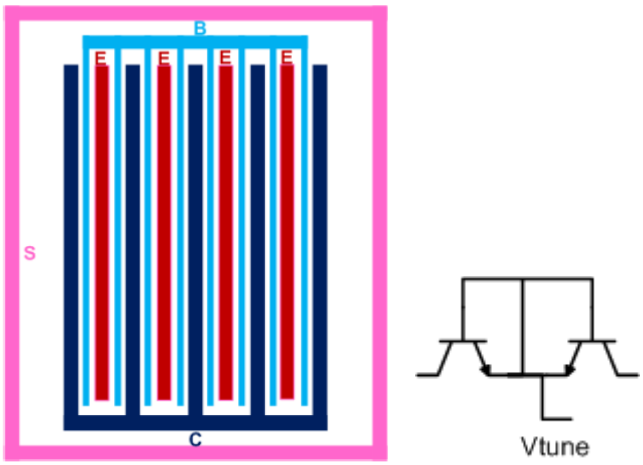


Figure 81: HBT transistor with 4 emitters and in CBEBC topology and varactor schematic

The resulting quality factor for the capacitor tank is:

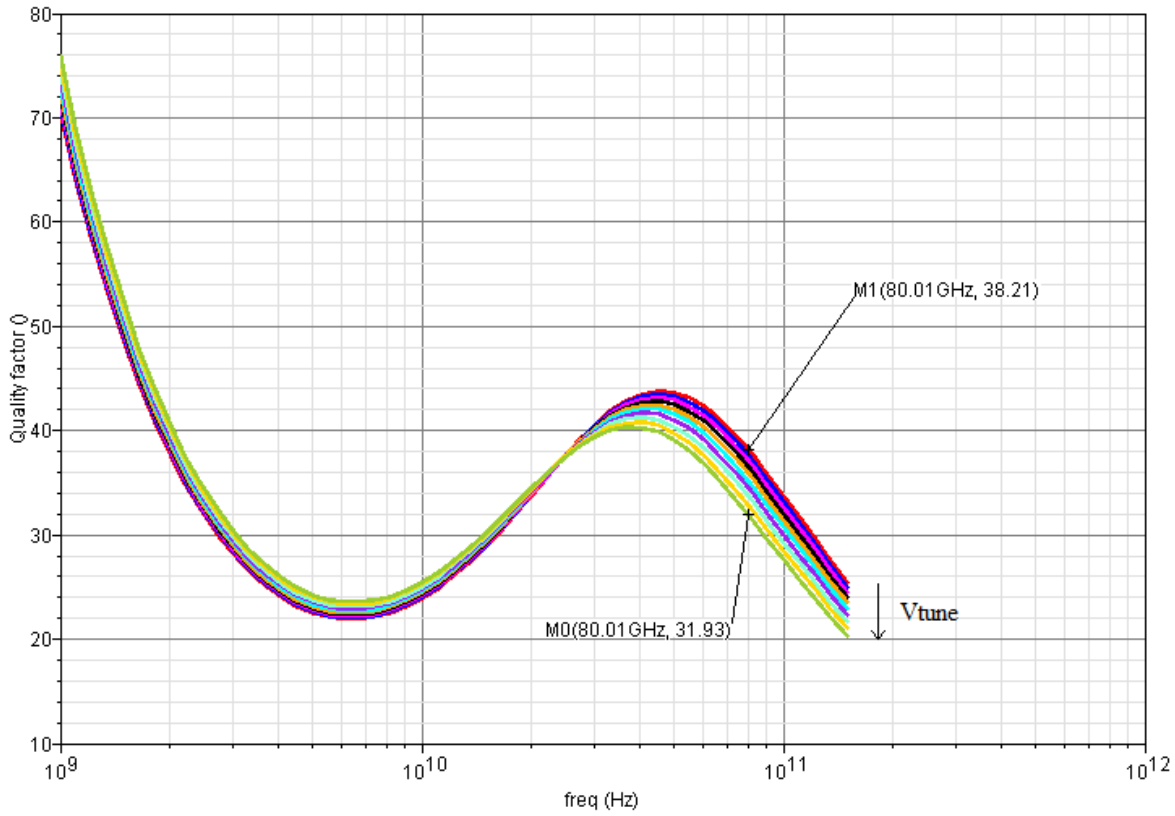


Figure 82: Capacitor tank quality factor

The quality factor is inverted at 15 GHz and the maximal is obtain for 45 GHz, but is still good at 80 GHz. It is better for high V_{tune}, so the oscillator will oscillate more easily at high frequency.

The microstrip line acting as inductor has been studied alone. It is 51 µm long and 10 µm width to reduce the parasitic resistor. The resonance frequency is far from the operating frequency (150 GHz); the inductor value at 80 GHz is 15.95 pH, and its quality factor is 34.

$$L = \frac{Im(Z)}{2\pi . f} \qquad (4\text{-}54)$$

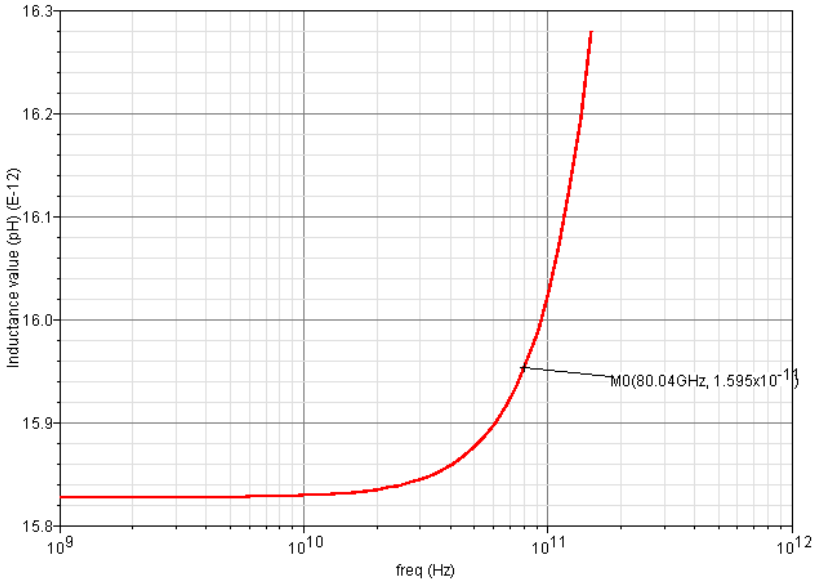


Figure 83: Inductor value

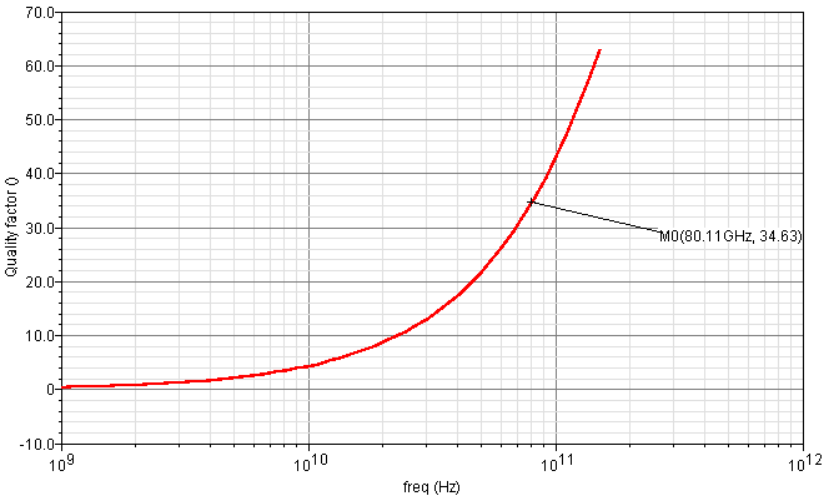


Figure 84: Inductor quality factor

The LC tank resonance frequency is 90.26 GHz; its quality factor is around 17 (depending of V_{tune}). The parasitic capacitance from the other components and the layout shift the resonance to 80 GHz.

The negative resistor is done by using a cross coupled pair. The negative conductance is thus $-g_m/2$

The injection is done by both transistors (M3 & M4) under the cross coupled pair. The M3 and M4 transistors are similar to the M1 and M2 transistors of the cross-coupled pair as the same amount of current passes through them. To ensure the injection is not too powerful and becomes a high current injection, degenerative resistors have been added. The injection

current can also be controlled externally by adjusting the biasing voltage V_{ILO}. The ILVCO schematic is presented Figure 85.

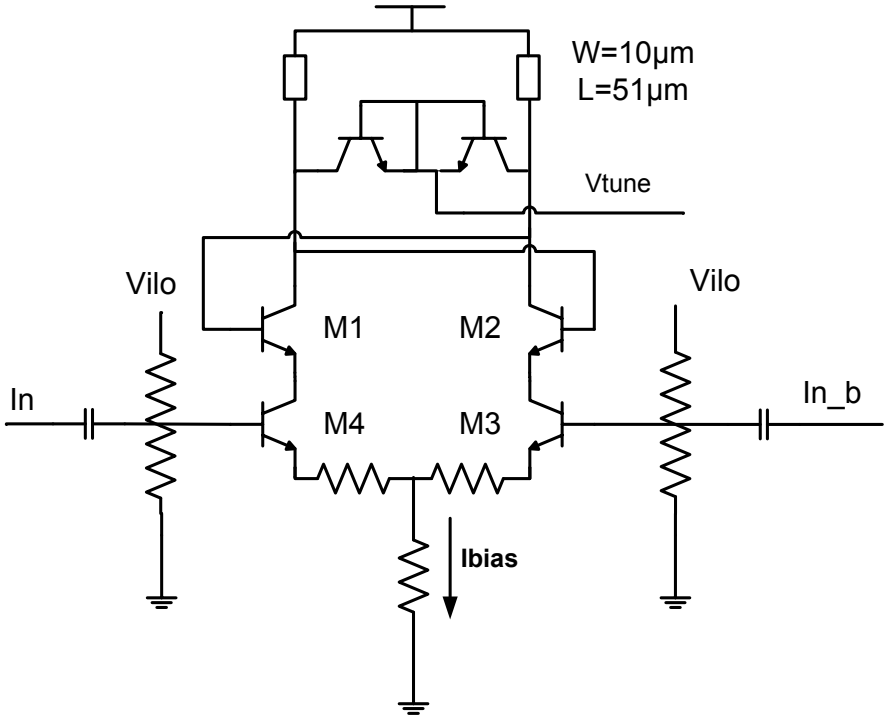


Figure 85: ILVCO schematic

The post layout simulation frequency range of the ILVCO is presented Figure 86. The ILVCO is connected to the pulse generator and the clock buffer to be accurate as the clock buffer presents a capacitive input. The frequency range is 77.5 GHz to 81.1 GHz.

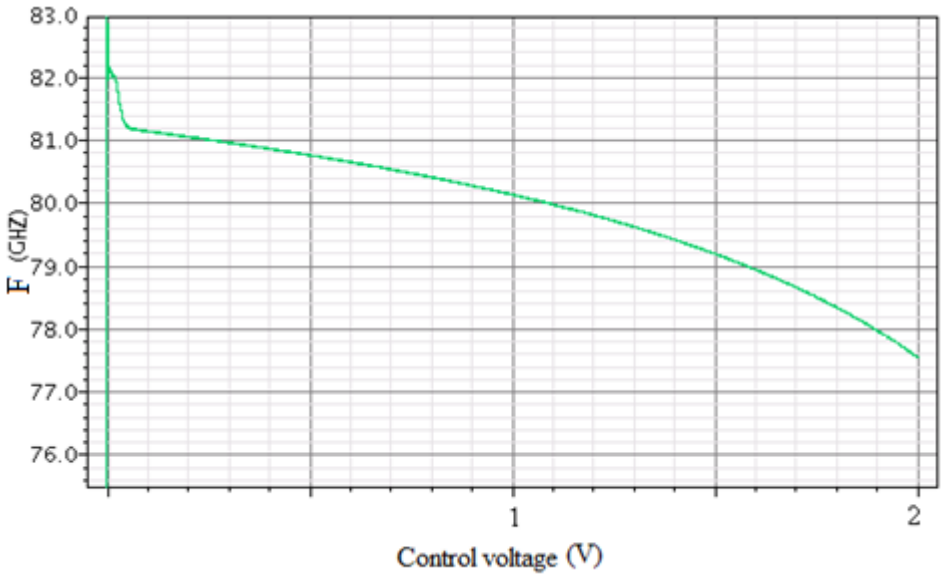


Figure 86: ILVCO frequency range

4.4 Pulse generator

The pulse generator produces some pulses at the bit frequency. The pulses are generated by a XOR gate from which the inputs are the data and the data with a 6.25 ps delay. This delay is made by adding a data buffer on the XOR input path.

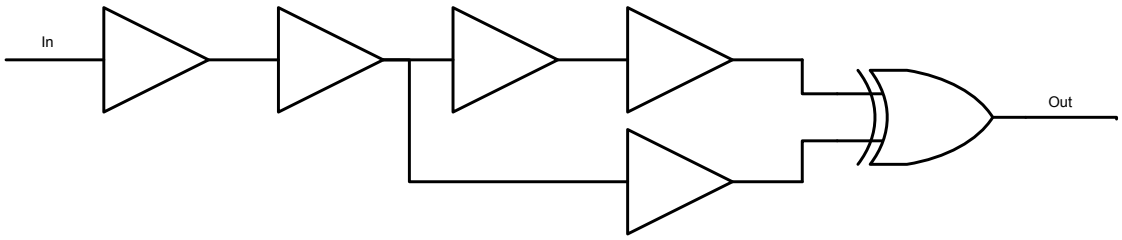


Figure 87: Pulse generator architecture

To prevent any delay mismatch between the different XOR inputs, they all have the same signal level. Some shunt peaking is done to generate signals up to100 GHz.

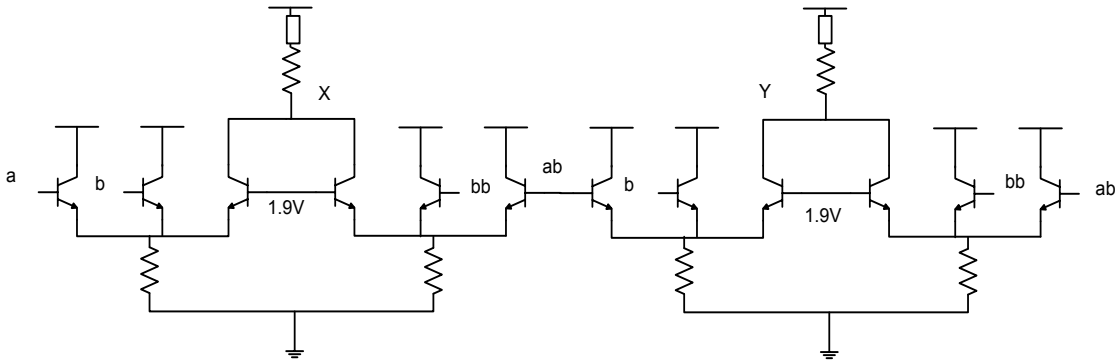


Figure 88: XOR schematic

The pulse generator generates a spectrum line at 80 GHz as expected. The line is absent from the 80 GHz NRZ PRBS input data as we can see on Figure 89 done with post layout simulations.

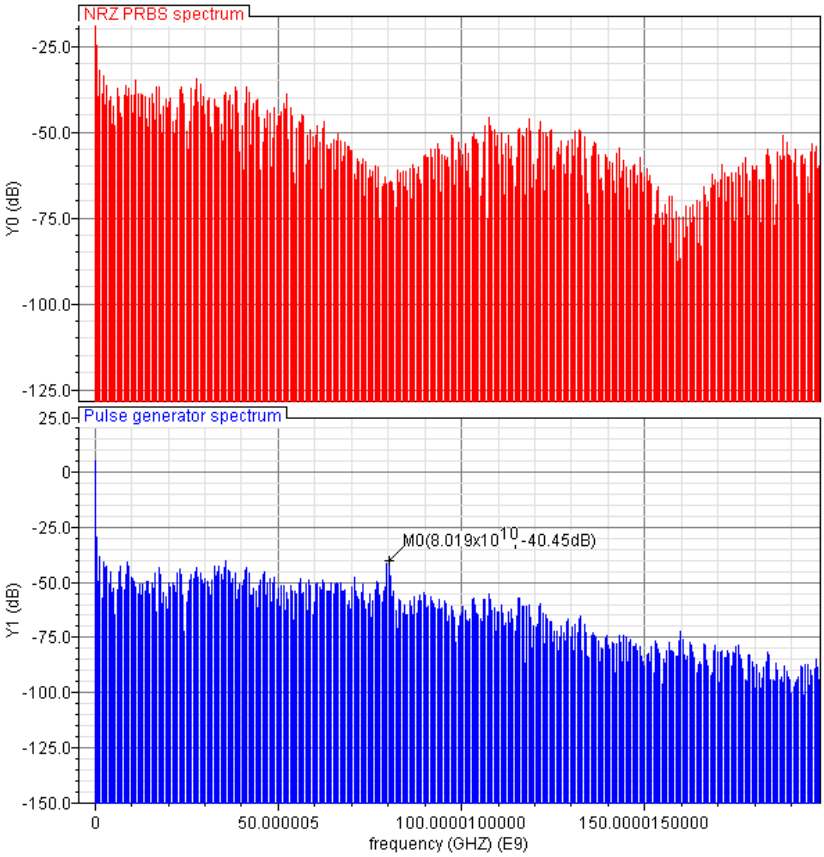


Figure 89: Pulse generator input and output spectrums

4.5 D-Flip Flop

The D-FF is made of two D gates, a master and a slave one. It also has a shunt peaking to boost its operating frequency. A resistor is inserted between both differential pairs in order to allow a small current passing through them. This reduces the resistance seen by each differential pair current source and reduces the overall delay associated with the circuit.

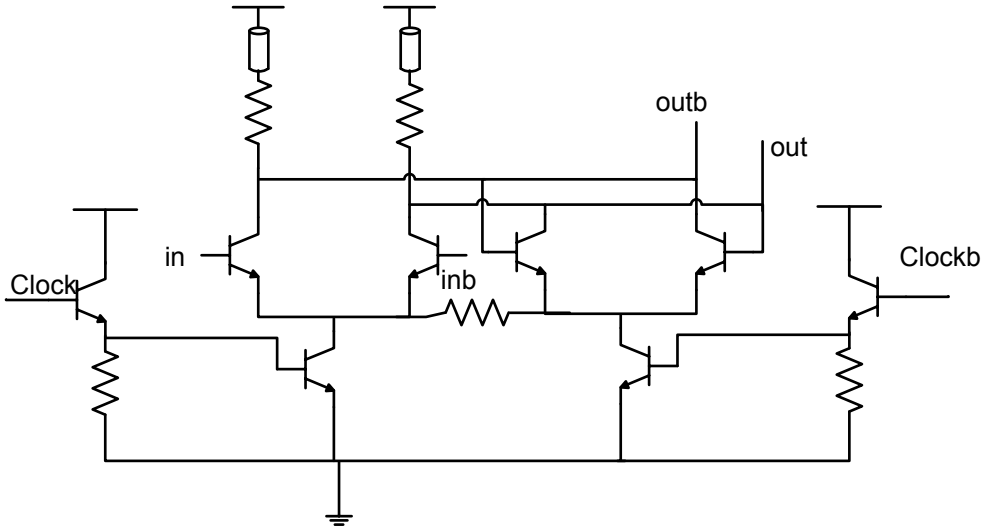


Figure 90: D latch

The emitter follower on the clock path generates a small delay and is taken into account in simulations. This emitter follower is necessary to bias correctly the D gate differential pair.
The D-FF has been simulated with a 40 GHz data signal and an 80 GHz clock and when the clock phase varies. As a result, we can see the D-FF sampling phase behavior.

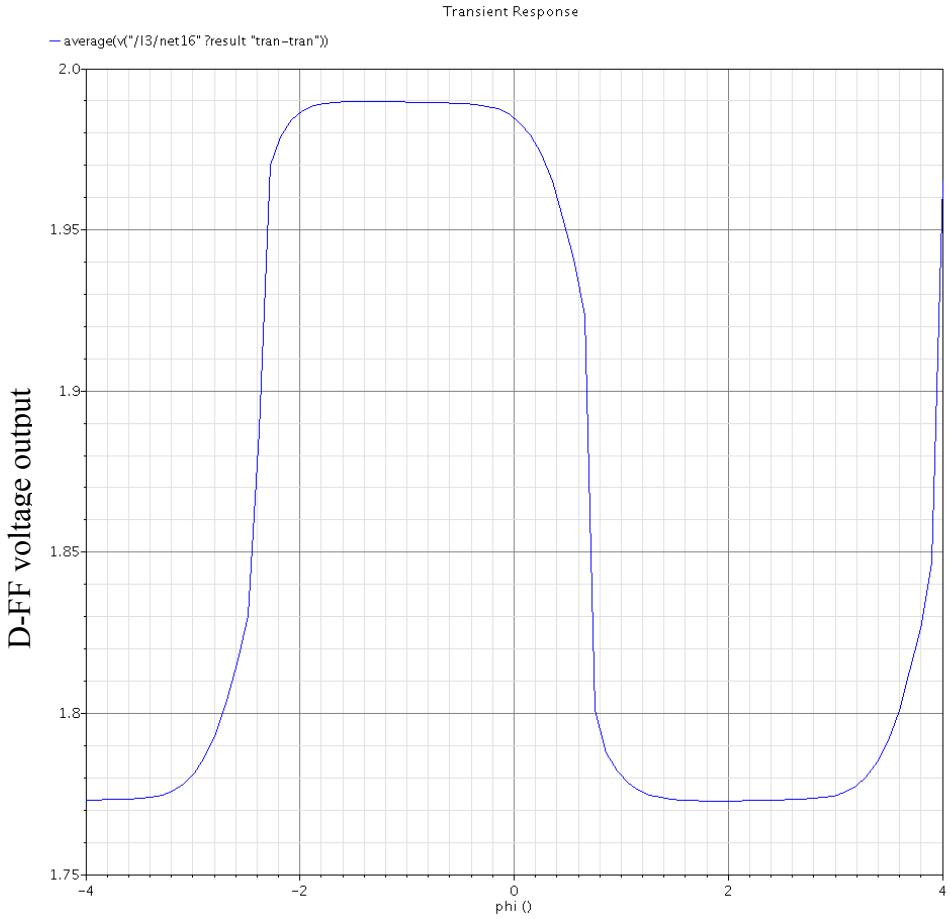


Figure 91: D-FF transfer function

As we can see, there is a phase error: this is the delay introduced by the emitter follower and it must be taking into account during the design of the CDR.

4.6 Phase comparator

The proposed charge pump can be seen on Figure 92. It associates the charge pump and the switch. It is responsible for changing the ILO frequency by changing its control voltage. Current mirrors are made of CMOS transistor, as there is no fast operating PNP transistors in the used technology. Inputs are differential but can be used also in a single ended mode. The output is single ended, as the ILO used is a LC with cross-coupled pair and has only one control voltage.

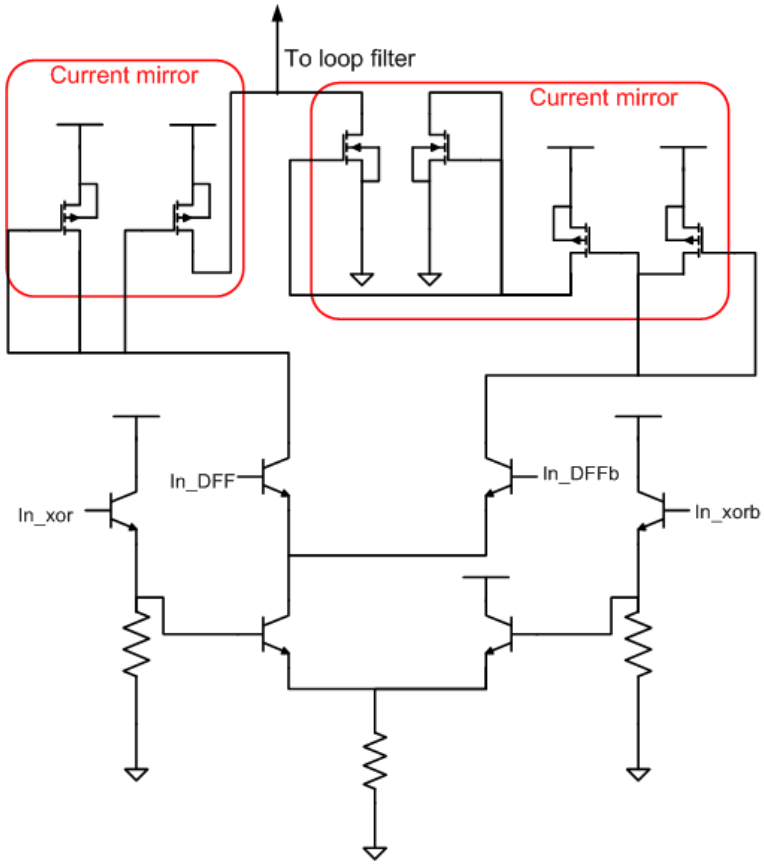


Figure 92: Charge pump

The simulated corresponding output current for 40 GHz input signals is presented in Figure 93.

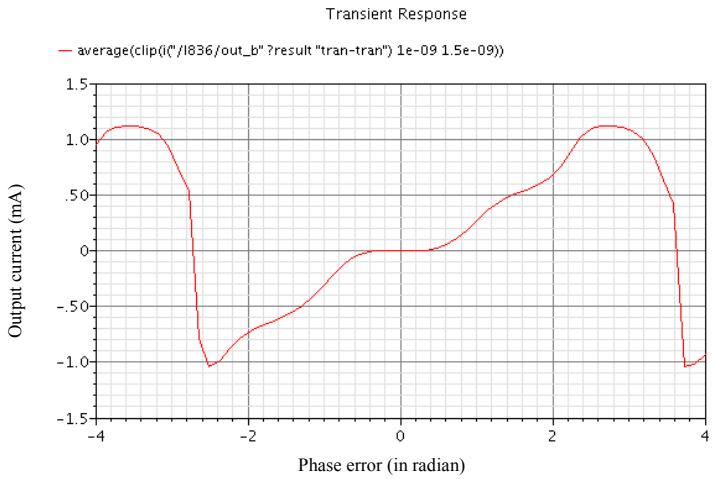


Figure 93: Phase comparator output current

The window is clearly visible when the signals are in phase. The curve is classic for a linear phase comparator.

4.7 Clock buffer

The last block is the clock buffer. Its role is to supply large clock signal to the sampling D-FF and to the output pads. It got one emitter follower and three differential pairs with inductive load in serial. There is two clock buffers, one for the D-FF and the other one for the output. We use the 5µm transistor already optimized.

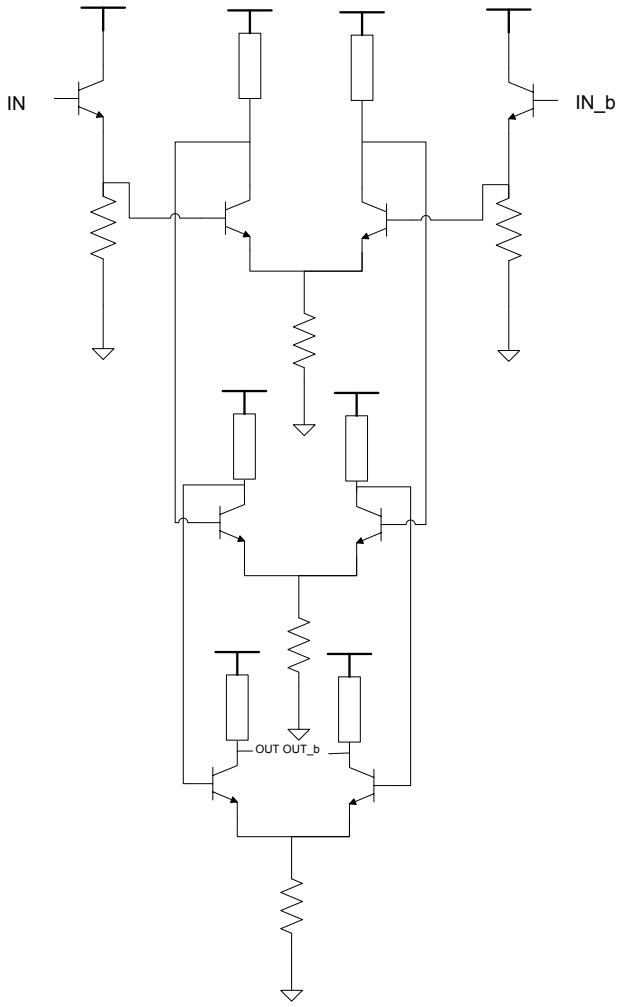


Figure 94: Clock buffer schematic

The whole CDR has been designed and sent in foundry. We also put the ILO and its synchronization blocks on a standalone part and the phase comparator on another standalone part for testing purpose. The die is 2200 µm*2800 µm. The chip photography is presented in Figure 95:

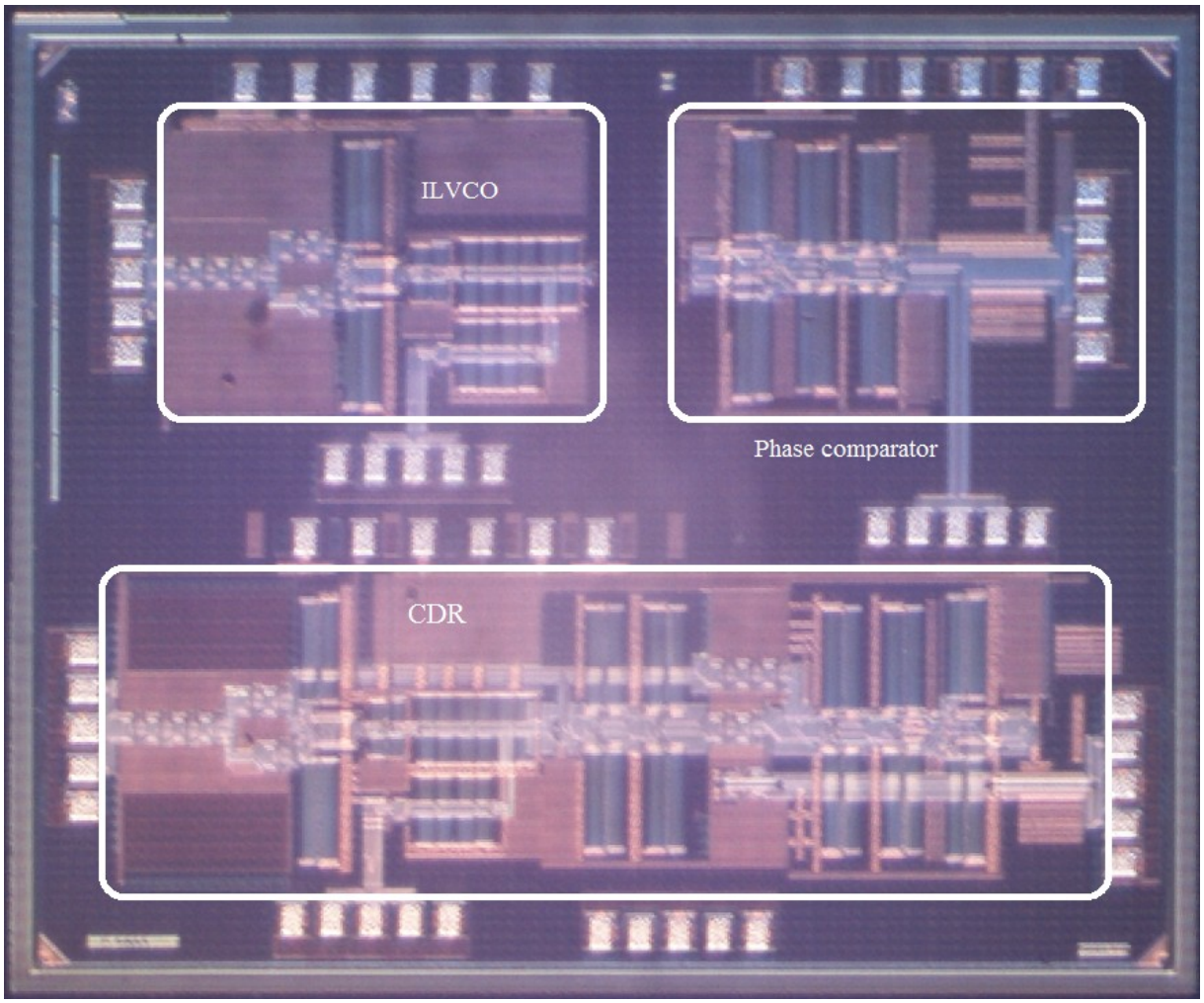


Figure 95: Nadezhda Chip photography

4.8 Multiplexer and demultiplexer chain

As the data bitrate is very high, and not all the necessary material is available in the laboratory, a first measurement method was created. We inject a single sinusoidal signal at 40 GHz, which is set differential by the input buffers. At the output we observe the clock and the data frequency. This method is only enough to demonstrate the basic operation of the CDR, as no BER or eye diagram is measured. To measure a BER we must use a "low" frequency data output as the higher BER tester operating frequency is 28 Gb/s. A solution to test the CDR is to multiplex and demultiplex several inputs and observe only one output.

An internal multiplexer and demultiplexer chain appears to be the simplest solution, as such an off-chip chain is very difficult to implement because of the phasing problem. Such a testing using external multiplexer/demultiplexer is visible Figure 96. It has been done by [59].

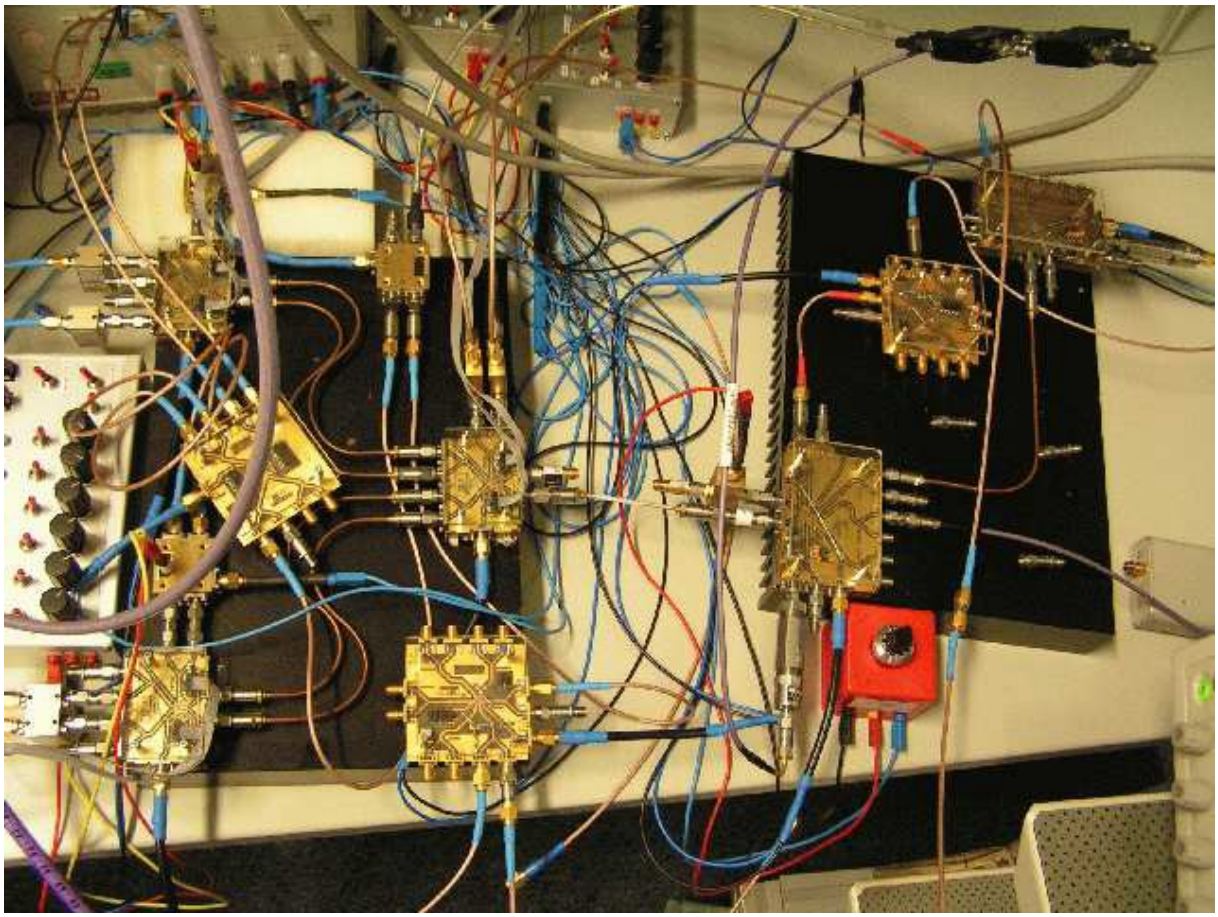


Figure 96: Measurement of 100 Gbit/s MUX and CDR&DEMUX Modules (Micram)

To simplify our demultiplexer / multiplexer chain, we only use 1:2 and 2:1 blocks to perform an 1:8 or 8:1 operation. The chain can be seen Figure 97:

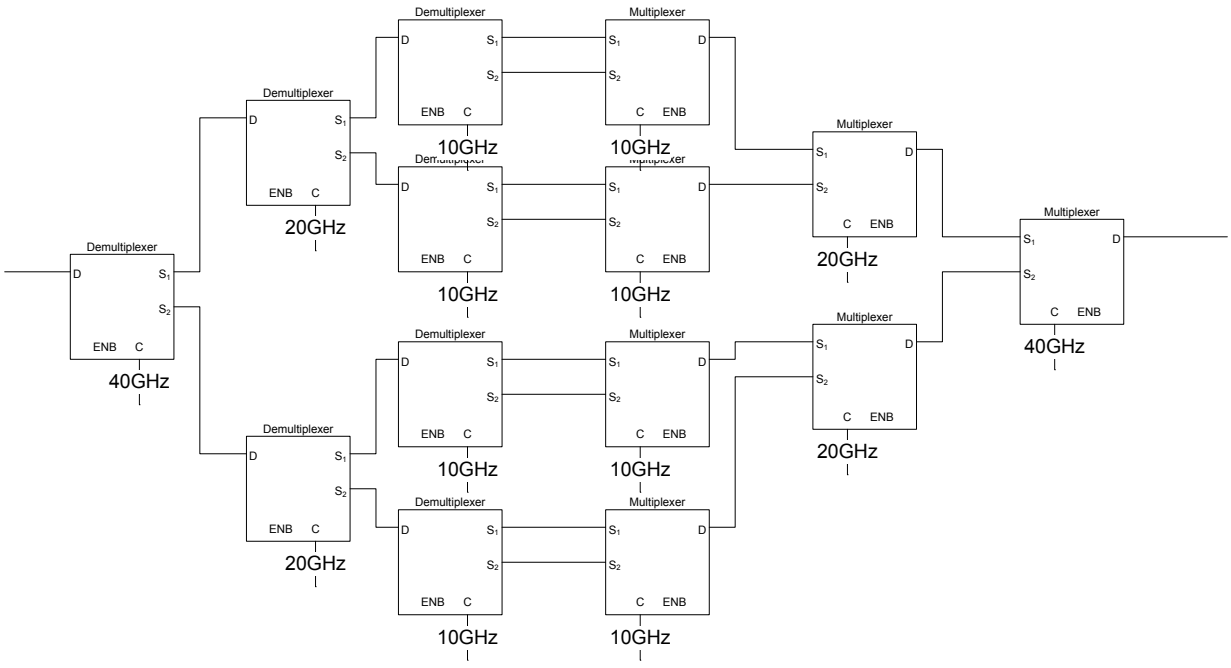


Figure 97: Demultiplexing multiplexing chain

The clock phase error between the different blocks appears to be the major problem and a special care is needed to have the rising clock edge at the middle of each bit. Each demultiplexer is done as follow:

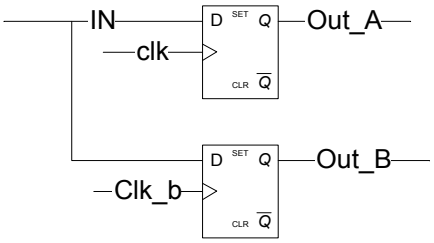


Figure 98: Demultiplexer 1:2

One D-FF samples on the clock rising edge and the second D-FF samples on the falling edge (i.e. the clock complementary rising edge). The D-FF are the ones used in the CDR. It could be interesting to redesign the D-FF operating at low frequency to remove the shunt peaking.

The multiplexer is the following:

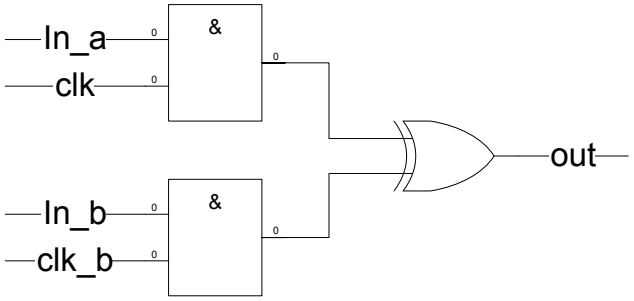


Figure 99: Multiplexer 2:1

The XOR is the same as used in the CDR. The AND gate is:

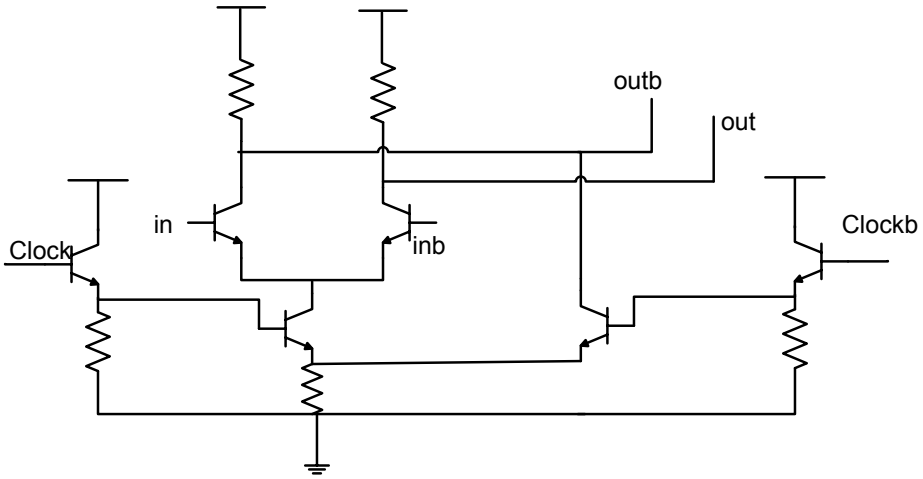


Figure 100: NAND gate

To generate all the clocks, we use some divide by two blocks. They are done with a single D-FF.

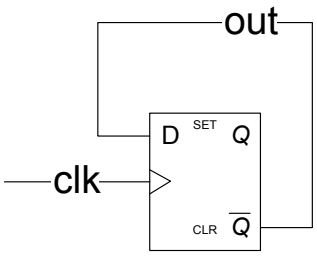


Figure 101: Clock divider

With several dividers in series, we can generate the clocks: 40 GHz, 20 GHz and 10 GHz. The main clock is fixed at 80 GHz and comes from the CDR:

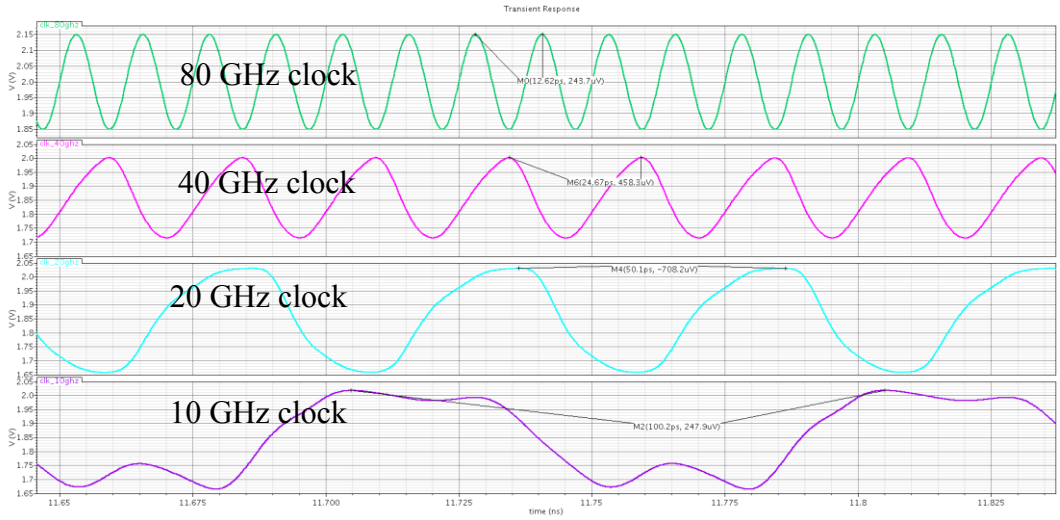


Figure 102: Clock tree

The demultiplexing and multiplexing operation works fine as we can see in the following pictures:

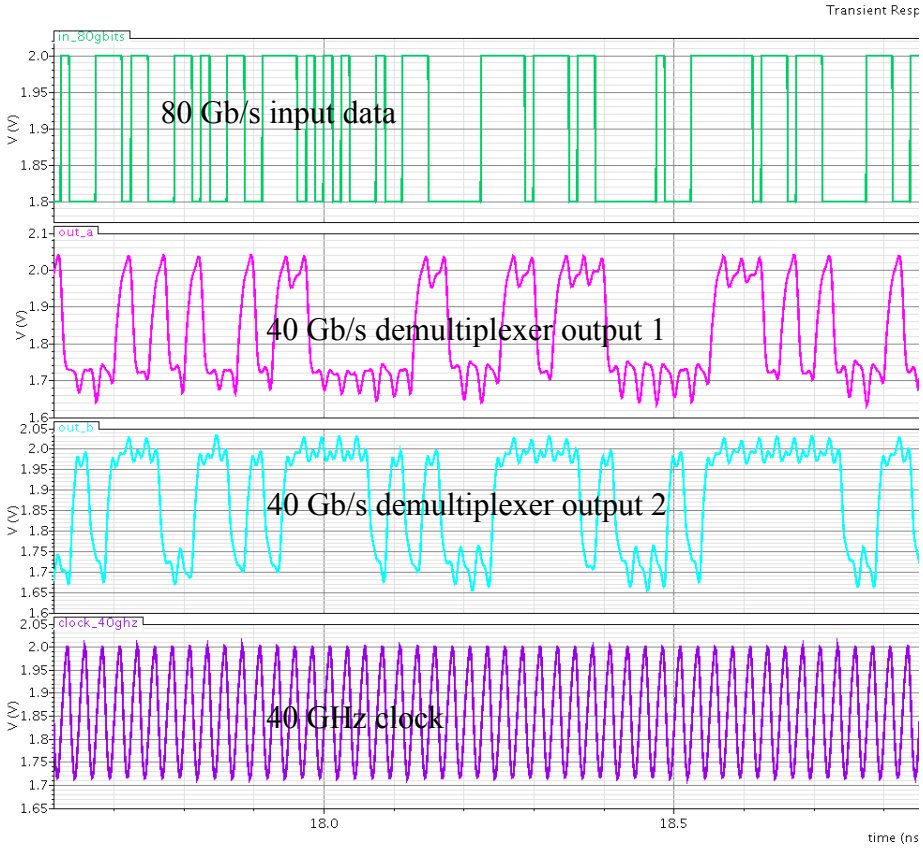


Figure 103: Demultiplexing 80:2*40GHz

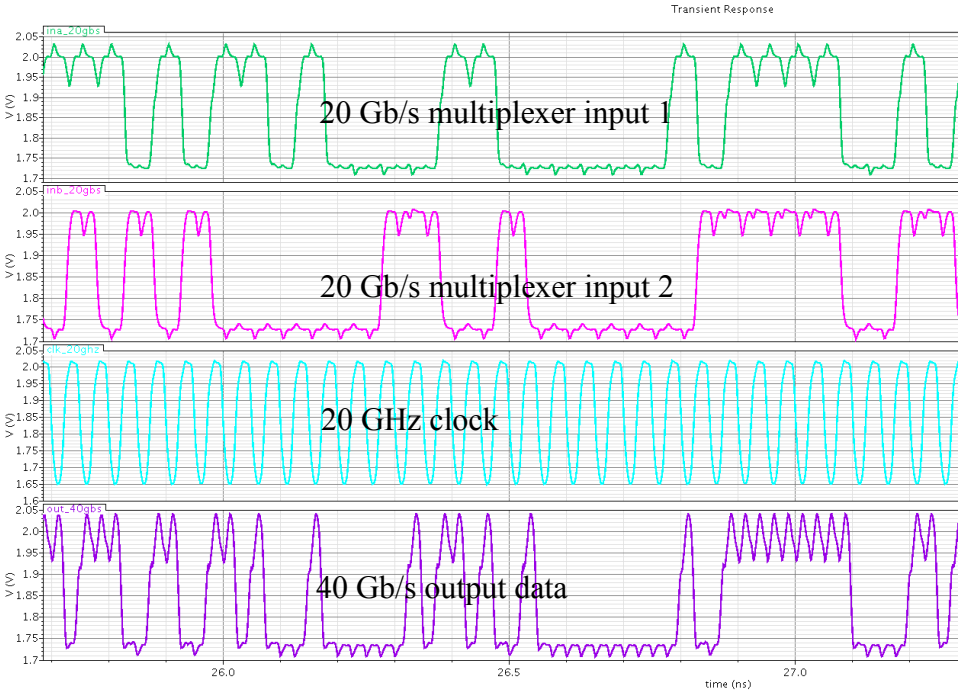


Figure 104: Multiplexing 20 GHz to 40 GHz

The following figure shows the input and the output of the demultiplexing and multiplexing chain. The delay introduced by all the operations is 160 ps.

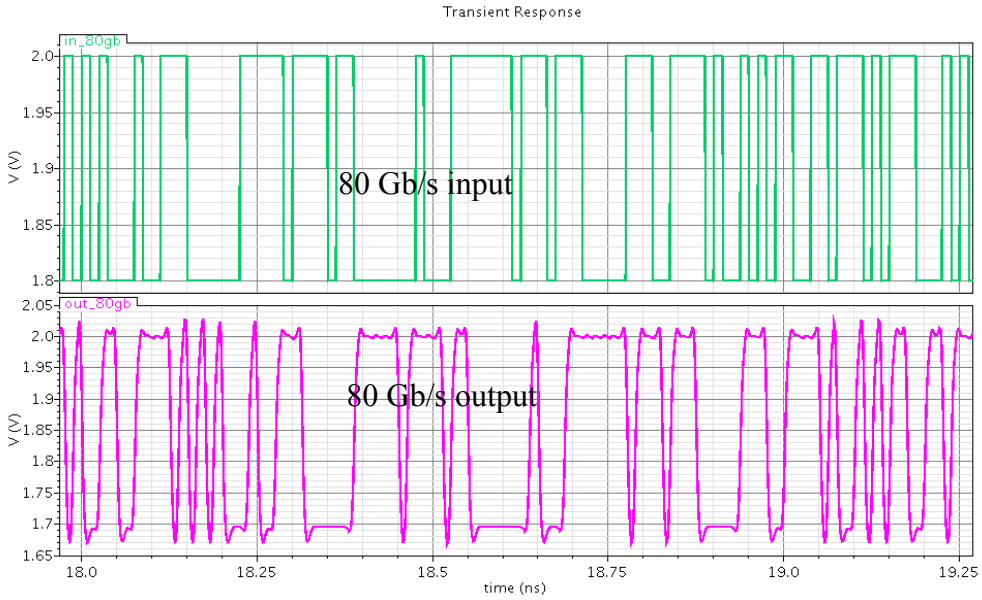


Figure 105: Input and output of the demultiplexing/multiplexing chain

4.9 Chip measurements

The chip has been measured after fabrication with a sinusoidal generator as data source and we observe the output clock spectrum. The clock signal is shown in Figure 106. The clock output presents a parasitic oscillation at 43 GHz and the ILO frequency has shifted to 66 GHz. The parasitic oscillation source has been identified after the measurements during retro simulations, and comes from the ILVCO buffer.

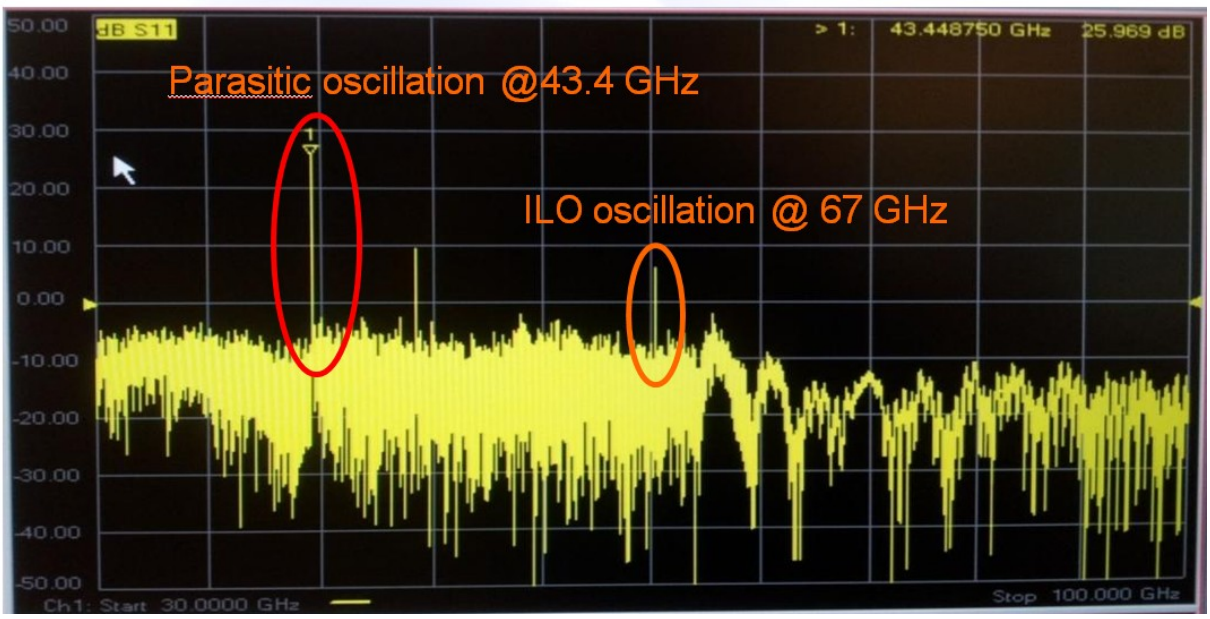


Figure 106: Buffer oscillation

The buffer oscillation is strong and alters (reduce power) the oscillator. However, the oscillator can still be measured and its frequency range is 66.1-69.4 GHz. The frequency range 9% shorter than expected and there is a 12 GHz shift.

The ILVCO in free running mode can be seen Figure 107:

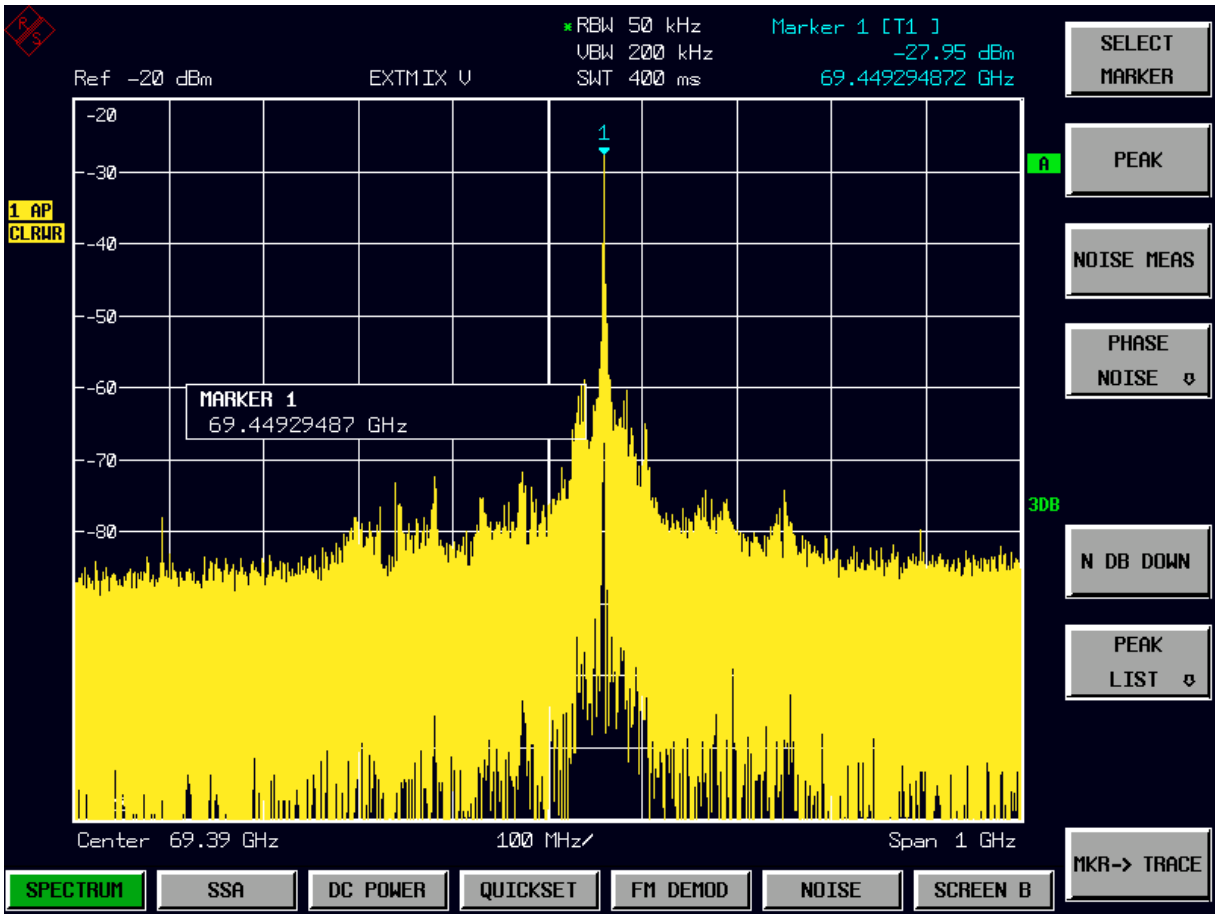


Figure 107: Oscillator maximum frequency

The ILO can still be synchronized with an external signal; we can synchronize it with a 4th order differential signal or a single 34 GHz signal (the available baluns are limited to 18 GHz). The spectrum becomes cleaner. However, the pulse generator can only generate pulses with a width of half a clock period (80GHz), so the ILVCO synchronization signal contains 68 GHz harmonics but the duty cycle is not 0.5. As the duty cycle is not 0.5 the locking range is not maximal.

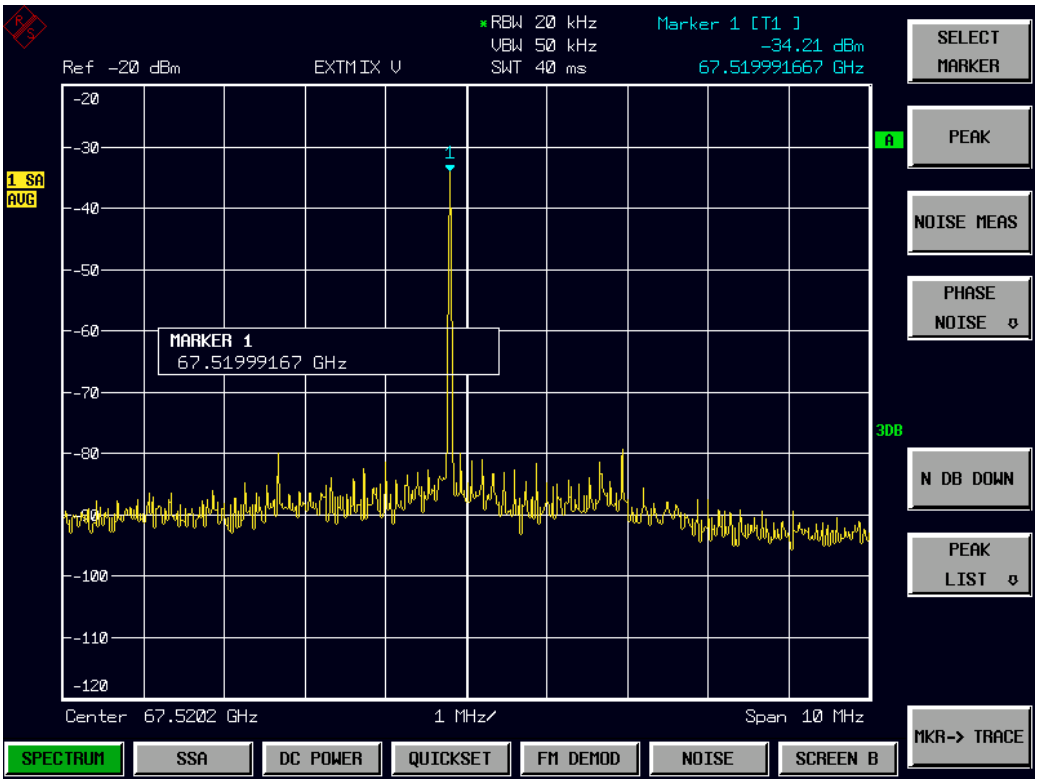


Figure 108: Synchronized ILO spectrum

When synchronized (Figure 108), the ILVCO tracks the injected frequency. The ILVCO can track over 2.09 GHz the input signal. The locking range is not dependent of the input signal amplitude as it is recreated in the pulse generator. Nevertheless, it is dependent of the V_{ILO} voltage as expected. It varies from 200 MHz at 1.8 V to 3 GHz at 2.6 V as in simulation.

The ILO phase noise follows the relation:

$$PN=PN(ref)+20\log(N) \tag{4-55}$$

With N the harmonic rank of synchronization. In the fourth order synchronization, there is 12dB difference between both curves as depicted in Figure 109

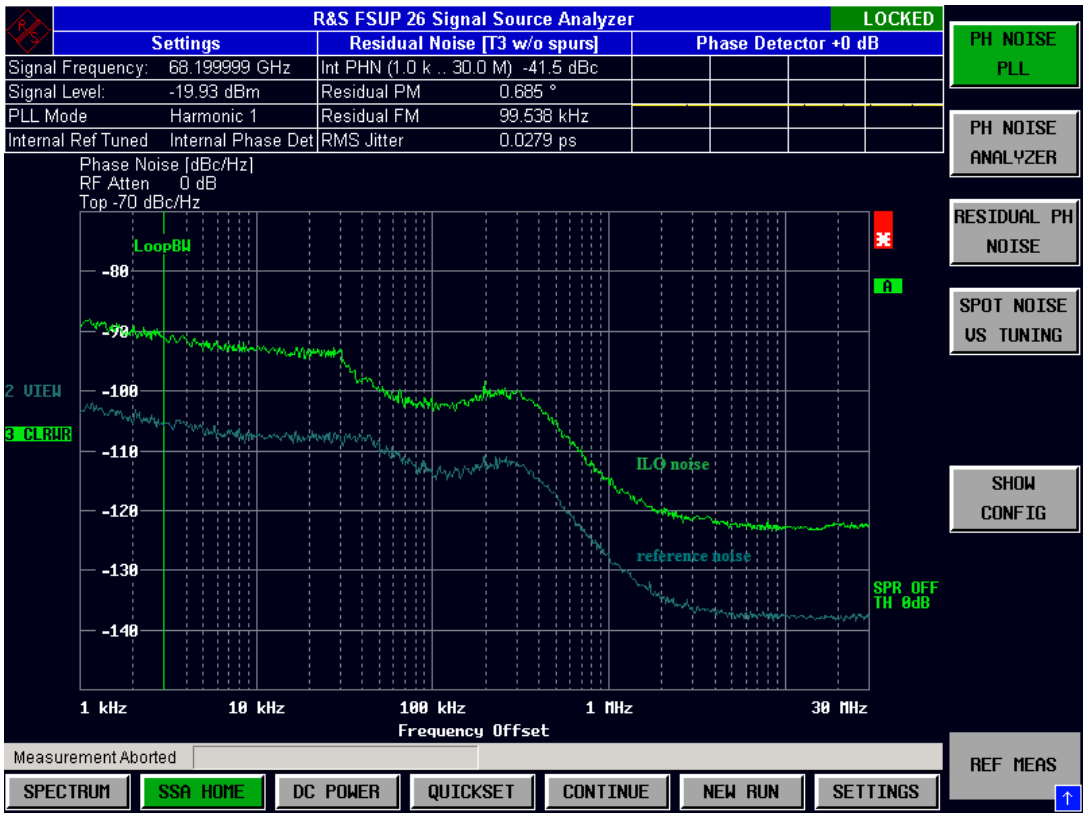


Figure 109: ILO and synchronization signal phase noise (4th harmonic)

The pulse generator works correctly and is able to regenerate differential signal from a single-ended input synchronization signal at 34 GHz. There is 6 dB between the two curves, as we can see on Figure 110.

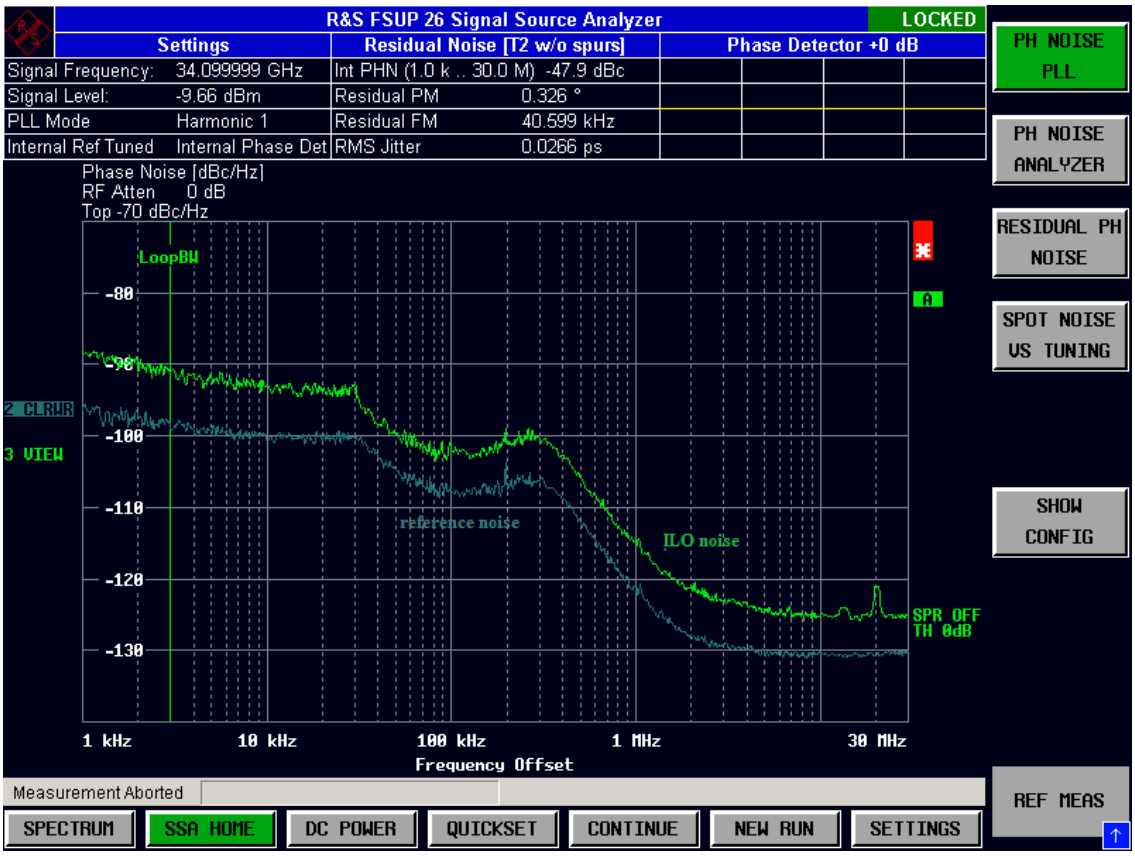


Figure 110: ILO and synchronization signal phase noise (2nd harmonic)

Nevertheless, as the output buffer oscillates with a higher power than the oscillator, the whole CDR is not measurable. Measurements show that the D-FF is working, as a 10.75 GHz input signal is sampled by the D-FF with the unwanted oscillation at 43 GHz and can be observed at the data outputs. However, there is no phase alignment and some bits are missing. The phase comparator can still be measured.

4.10 Phase comparator measurement

The phase comparator photograph is shown in Figure 111. The chip core occupies 600 µm*600 µm without the pads. RF probes impose a minimal distance between both differential inputs, leading to a chip size of 1200 µm*1300 µm (including pads). The chip power consumption is 80 mA from a 2 V power supply exactly as in simulations.

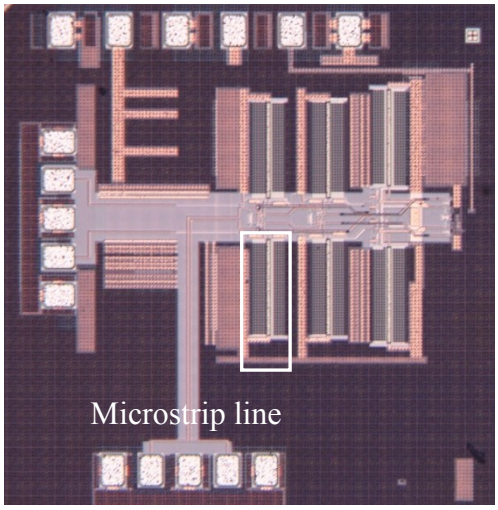


Figure 111: Phase comparator photography

The six microstrip lines used for the shunt peaking are clearly visible. Due to measurement setup limitation (high frequency balun), the phase comparator can only be tested up to 18 GHz. The output of the charge pump is at low frequency because of the implemented loop filter. Two differential sinusoidal 18 GHz signals, one with a 3 kHz phase modulation, are injected to the phase comparator, and we monitor the output of the loop filter. The modulation frequency is set very low to clearly identify the windows characteristic. The results are shown in Figure 112.

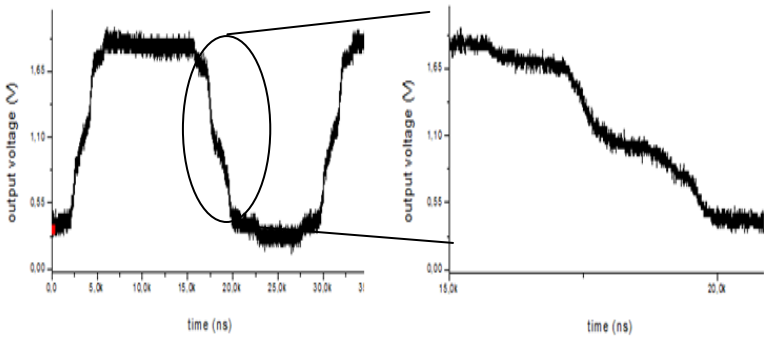


Figure 112: Output of the phase comparator

We can clearly identify the window, and the shape of the obtained curve is identical as the simulated one presented in Figure 93. The measurement results are as expected, even if the phase comparator is designed for square wave signals and measured with sinusoidal ones.

4.11 New chip design

A second chip with corrections has been designed. At first a debugging work has been done to clearly identify the origins of the problems. Both problems (frequency shift and oscillations) have been studied complementary. After retro simulations, it appears that the clock buffer was oscillating, but only with a load, in the design it is the resampling D-FF. The problem did not appear when a perturbation is applied on power supply but only when a perturbation was applied to the input. Moreover, the buffer oscillation was masked by the ILVCO oscillation, as it was very low. With the frequency shift, the buffer oscillation became predominant. The oscillation comes from the base-collector capacitor coupling of the emitter follower in the clock buffer. The frequency oscillation shift surprisingly is not due to an incorrect parasitic capacitor extraction. Hand calculated parasitic and computer parasitic are similar. The extracted capacitance of the pad is similar within 2 fF to the measured value. The shift is due to small metal path not taken into account, which acts as an inductor. This line is the one that connects the microstrip line to the transistor access on the ILVCO:

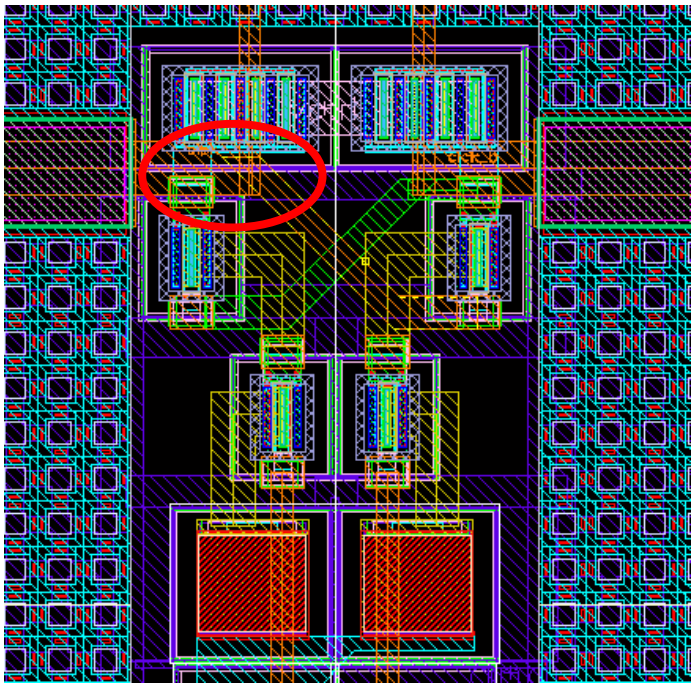


Figure 113: Transistor access

This metal path is 6 µm*4 µm. It is present in any shunt peaking access and in the transistor/resistor access. Retro simulations with this line show an ILVCO central frequency of 69 GHz. It also shifts the clock buffer operating frequency as the D-FF and XOR maximum frequency as the shunt peaking inductance value is higher than expected.

The small metal path error is easy to correct and to fix: the microstrip lines acting as inductors have to be shortened.

The clock buffer needs to be totally redesigned to be corrected and more efficient. We opted for a combination of small differential pairs with resistive load and some differential pairs with inductive load. This design occupies the same area as the previous one and simplifies the layout of the whole CDR.

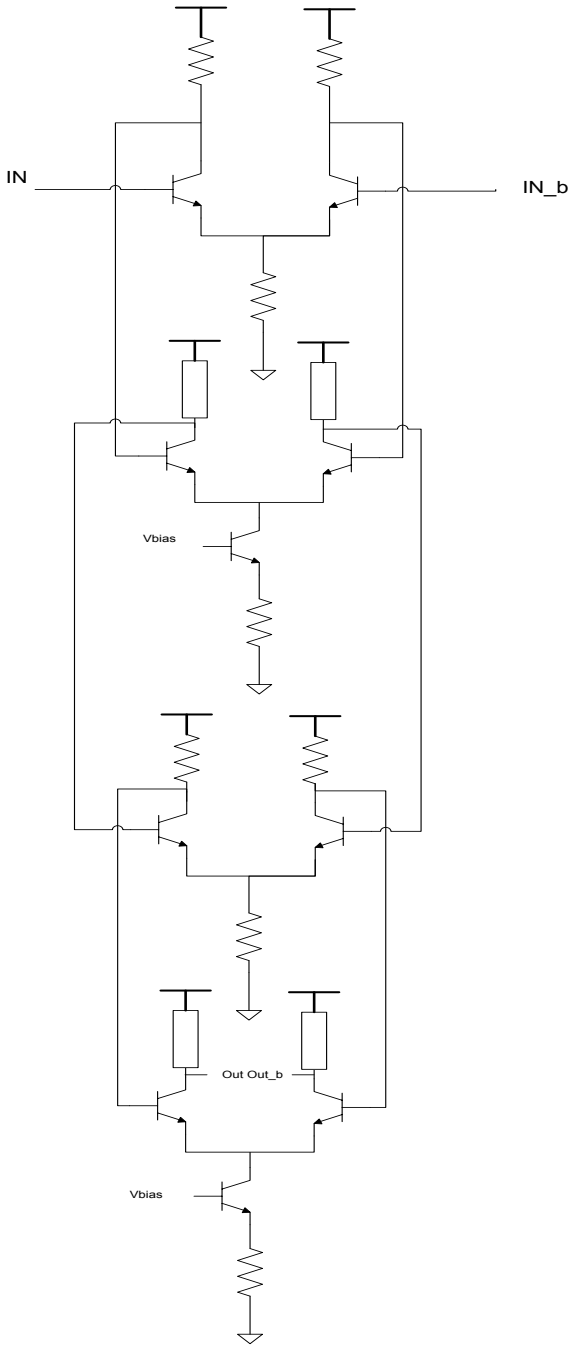


Figure 114: Clock buffer

The ILVCO architecture is the same. The inductors are a bit smaller, the new microstrip line is 48 µm*10 µm. The new range is 79 GHz-82.8 GHz.

Interconnections between the ILVCO and the buffer have also been reduced as the resistive differential pair can fill the empty space:

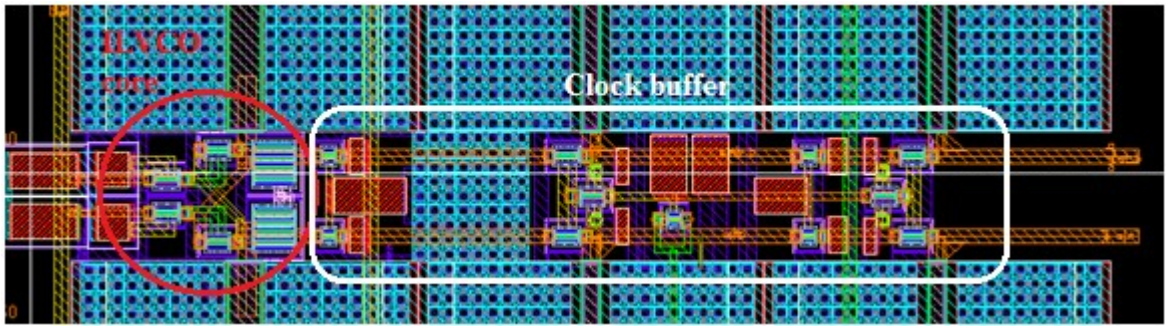


Figure 115: ILVCO and clock buffer second version layout

The blue squares are the microstrip line ground shield exclusion zone. On previous clock buffer the differential pairs were far away from each other due to this exclusion zone (Figure 116).

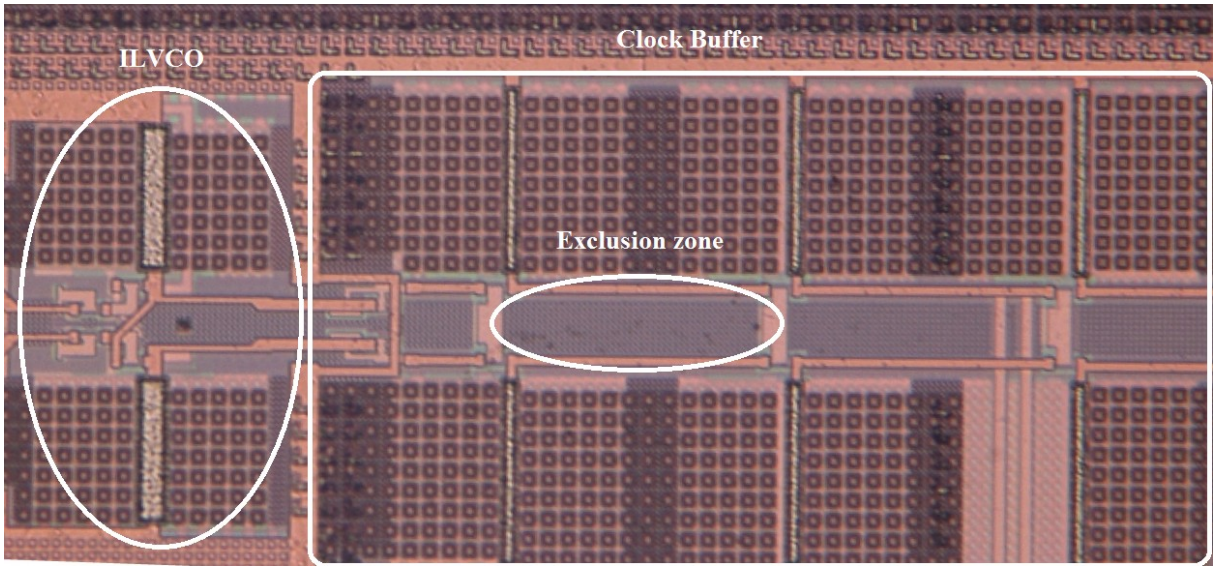


Figure 116: Nadezhda ILVCO and buffer

As for the first chip, some Post Layout Simulations were done to validate the design of the new chip, named razrabotka.

The CDR is simulated with PRBS data. We observe the loop control voltage.

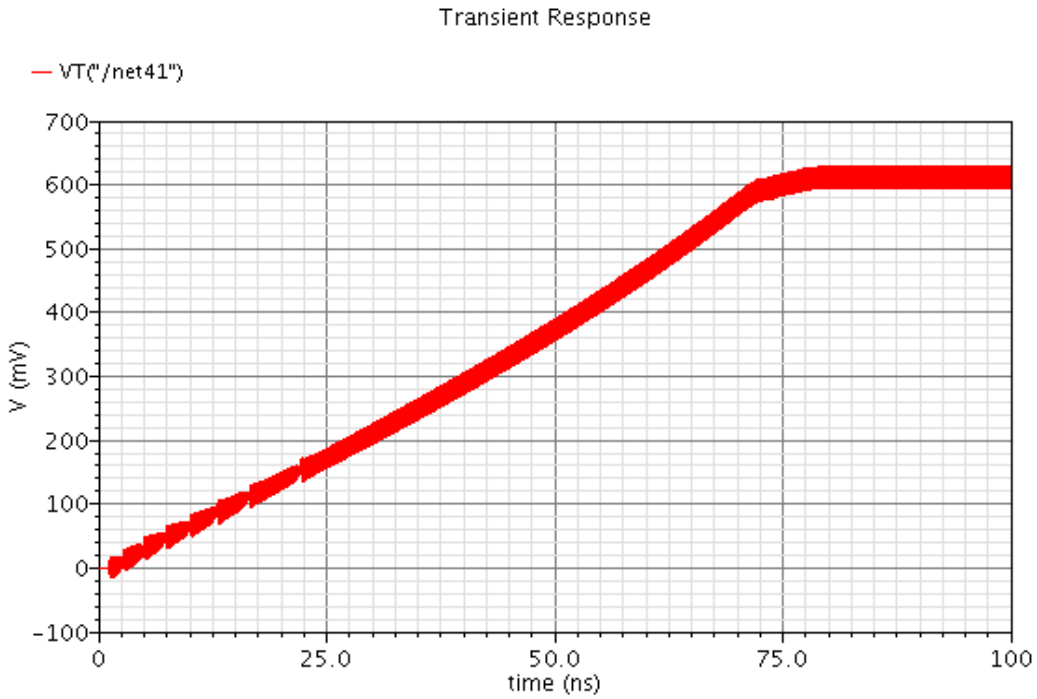


Figure 117: Loop control voltage

As expected, the voltage stabilizes correctly, without oscillations, the chip consumption is 500 mA under 2 V power supply. This chip operates as the first one, but the ILVCO and the phase comparator are not sent alone again as they have been characterize already.

4.12 Razrabotka measurements

The corrected chip only includes the CDR, no other blocks have been integrated. The measurements are done in two steps. Firstly, the loop control voltage is fixed externally to characterize the ILVCO performances. Secondly, the charge pump controls the control voltage. The feedback loop filter parameters (capacitor and resistor) are fixed at a special value and the stability is satisfied for it. When an external device (oscilloscope, multimeter etc...) is connected to the control voltage, it brings a capacitor and a resistor in parallel and changes the feedback loop stability, so unfortunately no measurements of the control voltage when the CDR operates can be done. The injected signal is a pure sinus, which simulates the data signal as no square source is available in the laboratory at 50 GHz.

It appears the best trade-off between performances, consumption and simulations results is obtain for a power supply of 2.3 V and the power consumption is measured at 675 mA, a bit more than expected.

The frequency range without synchronization is 96.71 GHz to 102.14 GHz, it means ΔF=5.43 GHz versus 3.8 GHz in simulation. The frequency shift may be due to the overestimated parasitic components, the high simulation temperature and the increased power supply. At 27°C and 2.3 V power supply, the simulated central frequency is 96 GHz.

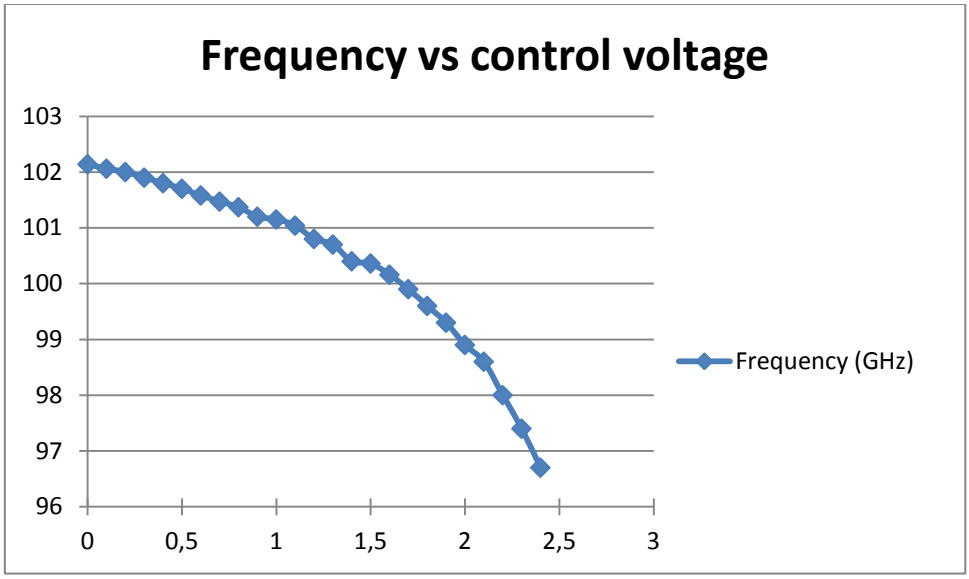


Figure 118: VCO tuning range

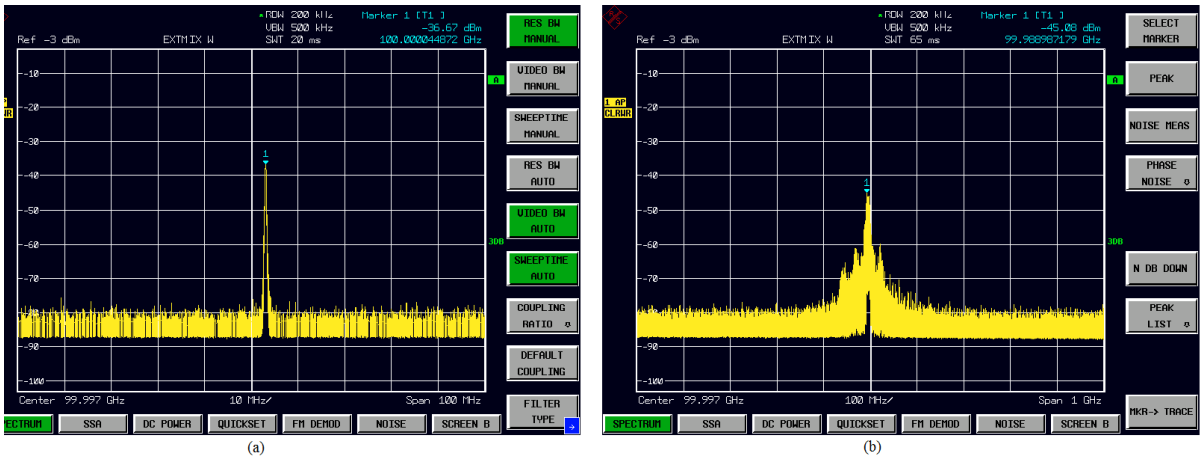
The ILO locking range is dependent of the injected signal frequency and its power level as seen before. It varies from 50 MHz on the tenth harmonic (Pin=0 dBm) to 2 GHz on the second harmonic (Pin=-8 dBm). The ILVCO can lock itself very well on even harmonics, and on odd harmonics the locking range is smaller. For example, the fourth harmonic locking range is 2.1 GHz and only 1.8 GHz on the third one.

On Figure 119 we can see the phase noise of the synchronized VCO.

Figure 119: ILVCO phase noise, synchronized on fourth harmonic

The ILVCO copies the source noise with a 12 dB offset, respecting the equation 4-54.

The corresponding spectrum without and with the injection are presented on Figure 120:



(a) (b)

Figure 120: ILVCO spectrum, (a) with injection, (b) without injection

The ILVCO shows good performances and the whole CDR can be measured.

On the second part of the measurements, the charge pump fixes the loop control voltage and we observe the locking range and the output data.

The CDR can track a data signal from 24.1 GHz to 25.3 GHz, so the corresponding ILVCO frequency is from 96.4 to 101.2 GHz. If we disconnect the Data, the ILVCO frequency shifts toward 102 GHz, but with the injection, it cannot reach such high value. Maybe there is a little phase error at the input of the phase comparator.

The output spectrum with a 24.2 GHz injected signal is:

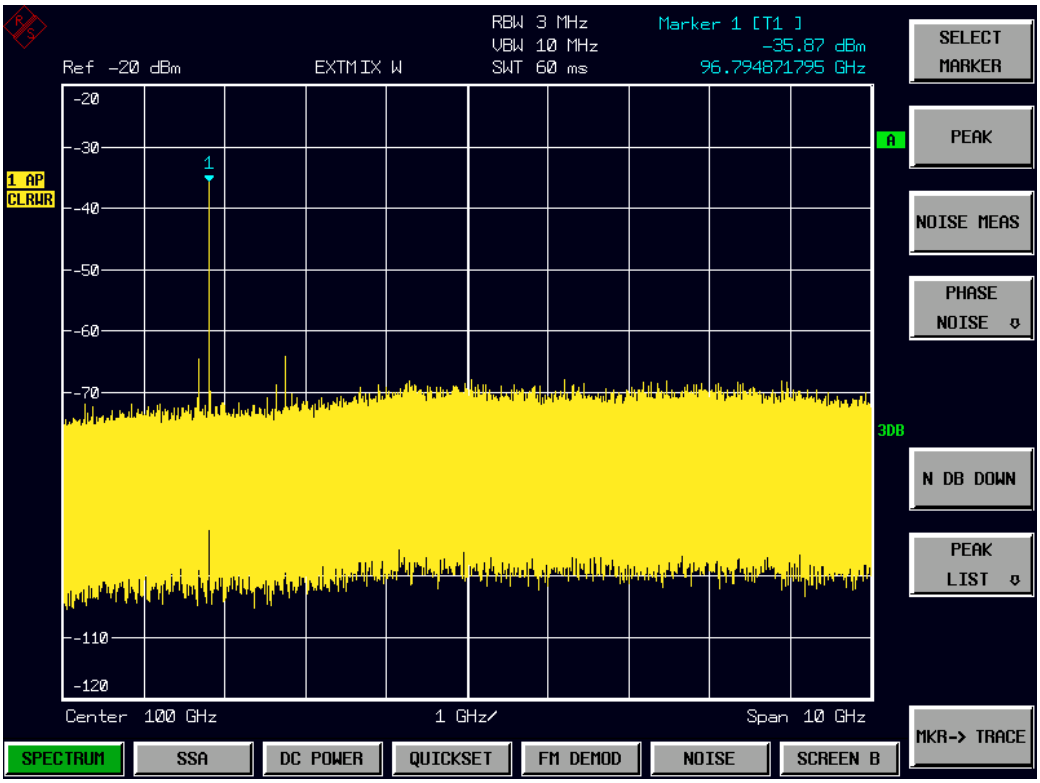


Figure 121: CDR ILVCO output spectrum at 96.8 GHz

A 50 GHz signal, from a network analyzer, has been injected into the CDR. The network analyzer is used as it is the only source in the 50 GHz range available in the laboratory. In this case the locking range is from 100.1 to 103 GHz, confirming the phase-offset error at the input of the phase comparator. Indeed the circuit should operate at 80 GHz and not 100 GHz. The phase comparator was designed to operate at 80 GHz and a corresponding delay was inserted between the resampled data and the injected data. The little phase offset difference may explain this behavior.

Some eye diagrams can be done with a 20 GHz oscilloscope, the highest available in the lab. We have done some RMS jitter measurements with injected data at 12.2 GHz (Figure 123) and 24.9 GHz (Figure 122). We observe the differential data output. As the input is a sinus, we only have half of the eye.

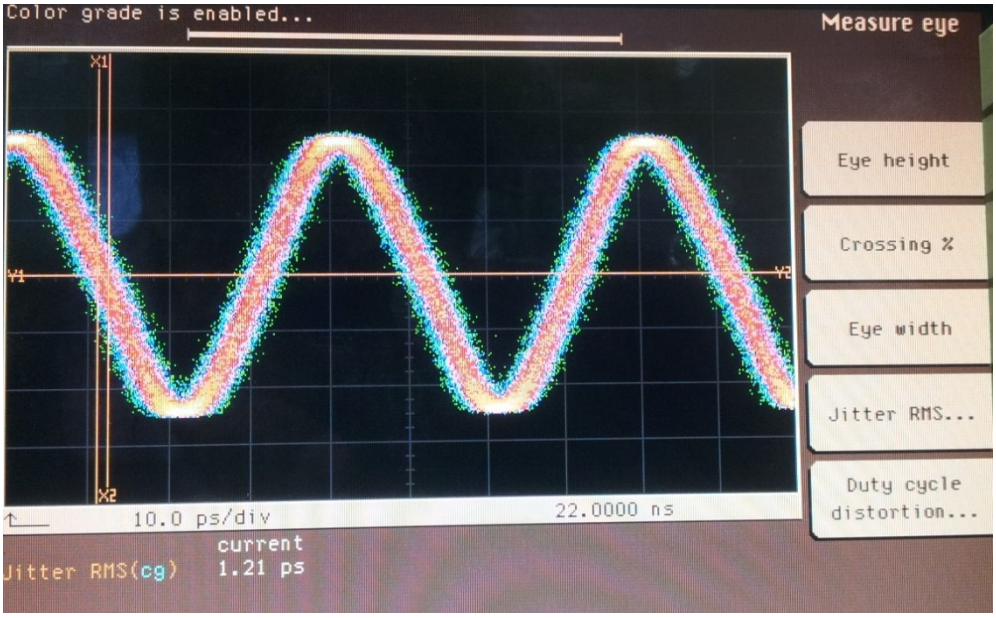


Figure 122: Jitter RMS with input data at 24.9 GHZ

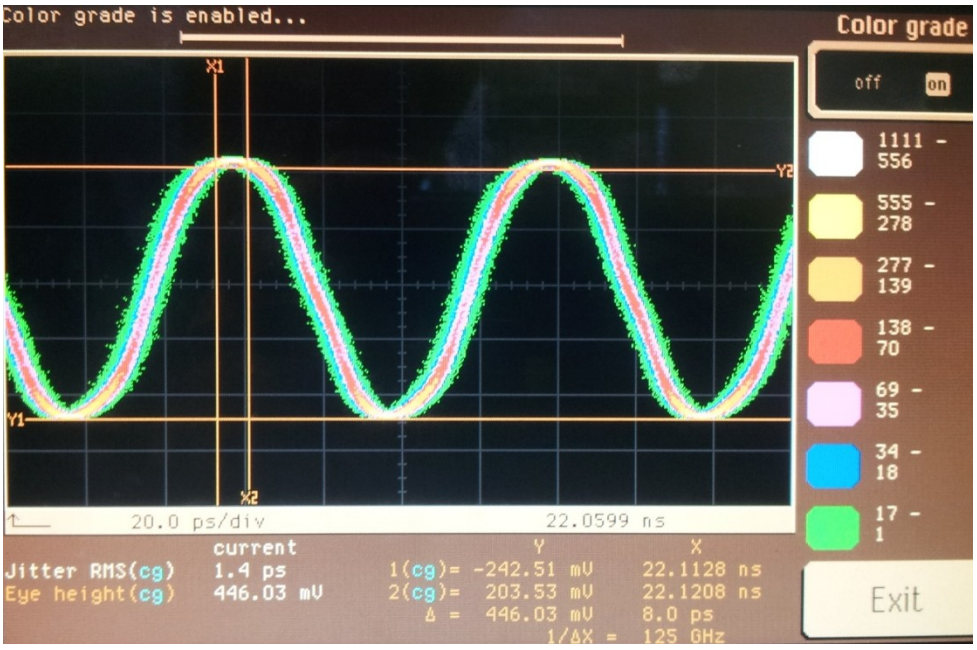


Figure 123: Jitter RMS with input data at 12.2 GHz

The jitter RMS is 1.21 ps and 1.4 ps respectively. It represents 30.25 mUI at 25 GHz and if we extrapolate at 50 GHz (assuming the jitter is the same), it represents 60.5 mUI.

All the blocks were designed to operate up to 100 GHz, excepted the data buffer and the output buffer which can be problematic for a 100 Gb/s signal.

4.13 Conclusions

In this chapter, we have presented the integration of a Clock and Data Recovery using an injection locked voltage controlled oscillator. The first measurements show a frequency shift and an unwanted oscillation on the clock buffer. Despites these problems the ILVCO can lock properly on a reference and shows low phase noise. The injection scheme works correctly. The phase comparator works as expected. The second chip operates at 100 GHz. The CDR can track and lock a signal from 96.4 to 101.2 Gb/s. The jitter RMS is 1.21 ps at 24.9 GHz.

Chapter 5

Conclusions

In this dissertation, millimeter wave clock and data recovery systems have been discussed. The increasing bandwidth of serial links allows high speed interconnects. These interconnects can be integrated in silicon, with all its benefits (low cost, mass market). The CDR circuit is the first block to receive the high-speed data and so have several constraints seen in Chapter 2. The operation of the CDR was described as well as figures of merit used to characterize a CDR performances.

The injection locked oscillator is explained in Chapter 3. A VHDL-AMS model has been developed to help design and simulations. This model is based on Huntoon and Weiss theory, using the calculated compliance. An improvement in this model could be the amplitude variation estimation. Thanks to this model study, a new phase comparator has been developed and it has shown a great interest in high speed CDR as it reduces the phase comparator operating frequency and has a window to reduce the jitter. The CDR can have various topologies, each with its own advantages and limits. The used topology allows a fast respond time and frequency hold when no data are transmitted. This architecture stability has been studied in frequency domain. The used process dedicated to millimetric design presents some high performances components and a dedicated back-end as described.

Chapter 3 introduces the CDR topology, and Chapter 4 presents the designed CDR. The CDR oscillator phase noise copies the phase noise of the injected signal. The phase noise at 1 MHz of the carrier is inferior to -110 dBc/Hz. Unfortunately, the first CDR circuit has a parasitic oscillation, which avoids any CDR measurements. However, the phase comparator works exactly as expected. A second chip with corrected problems has been sent to foundry and has been measured. The power consumption is 675 mA under 2.3 V. It operates around 100 GHz

and can track and lock a signal from 96.4 to 101.2 Gb/s. The jitter RMS is 1.21 ps at 24.9 GHz.

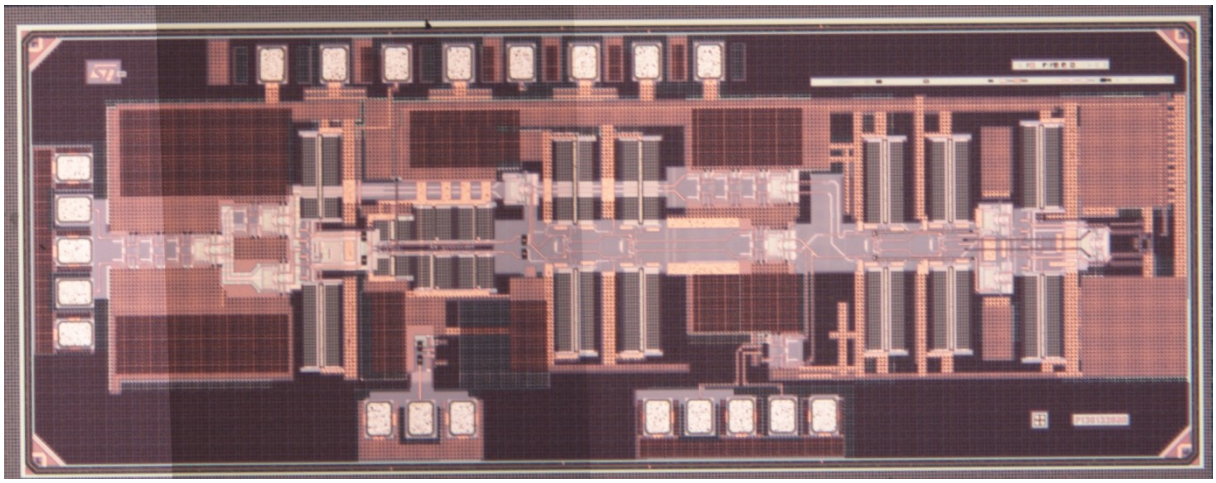


Figure 124: Second chip layout

Publication:

Q. Beraud-Sudreau, O. Mazouffre, M. Pignol, L. Baguena, C. Neveu, J-B. Begueret, T. Taris, "VHDL-AMS model of an injection locked VCO," *IEEE Newcas 2012*, pp25-28.

Q. Beraud-Sudreau, A. Mariano, D. Dallet, Y. Deval, J-B. Begueret, "A fully integrated 4GHz continuous-time bandpass Delta-Sigma converter," *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, vol., no.17, pp.778-781, 12-15 Dec. 2010

Q. Beraud-sudreau, O. Mazouffre, M. Pignol, L. Baguena, C. Neveu, J-B. Begueret, T. Taris, " Windowed phase comparator for an 80 Gbit/s CDR" *IEEE ICECS 2012*, pp185-188.

Appendix:

ILO VHDL-AMS Code:

```
--
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.MATH_REAL.all;
library DISCIPLINES;
use DISCIPLINES.ELECTROMAGNETIC_SYSTEM.all;
library MGC_AMS;
use MGC_AMS.CONVERSION.all;

entity os_test is

  generic (
    vcc : real;                    -- tension d'alim
    fc  : real;                    -- frequence centrale de l'OS
    K   : real;                    -- coeff de variation en Hz/V
    v0   : real;                   -- amplitude des oscillations
    L   : real);                   -- inductance de l'oscillateur

  port (
    terminal synchro    : in  electrical;      -- entree analogique
    terminal retour     : in  electrical;      -- entree analogique
    terminal sortie     : out electrical);     -- sortie analogique

end os_test;

architecture behavioral of os_test is


  signal t0          : real    := 0.01e-12;   -- derniere impulsion synchro
  signal fn          : real    := fc;     -- freq des impulsions synchro
  signal fin               : real := fc;              --freq moyennee sur 5 dernieres valeurs
  signal n           : real    := 1.0;        -- rang d'harmonique
```

```
  signal t1          : real    := 0.1e-12;    --
  signal os_synchro    : boolean := false;      -- etat de  OS
  signal t2          : real    := 0.2e-12;    -- derniere impulsion synchro
  signal iam : real := -10.0e-6;                    --amplitude du crt en entree
  signal rap          : real    := 0.6;    -- rapport cyclique
  signal f1          : real    := fc;     -- freq inter
  signal f2          : real    := fc;     -- freq inter
  signal f3          : real    := fc;     -- freq inter
  signal f4          : real    := fc;     -- freq inter
  signal f5          : real    := fc;     -- freq inter
  signal t3          : real    := 0.1e-12;    --
  signal frc                :real := fc;                --frequence imposé par la tension de controle
  signal comp : std_ulogic;

  quantity iin through synchro to electrical_ground;
  quantity vr across retour;
  quantity vout across iout through sortie;
--  quantity vout across sortie;
  quantity t         : real    := 0.0;         -- temps
  quantity C         : real    := 1.0/(MATH_2_PI*MATH_2_PI*fc*fc*L);-- capacite equivalente
  quantity absolu     : real    := 1.0;         -- valeur absolue d'un terme
  quantity deltaf     : real    := fc*0.2;      -- plage de synchro
  quantity finm        : real    := fc;          -- frequence de synchro
  quantity dphi   : real    := 0.0;         -- dérivée de phi
  quantity phi        : real    := 0.0;         -- phase dynamique de l'OS
  quantity phif       : real    := 0.0;         -- phase inst. signal sortie
  quantity ff          : real    := fc;     -- freq des impulsions synchro
  quantity fout : real := fc;
  signal tm : real := -0.1e-12;
--  quantity fbat : real := fc;
--  quantity vt: real := 0.6;

--  constant v0        : real    := 0.1;         -- amplitude des oscillations
  constant fj        : real    := 653.0e+06;   -- frequence jitter 653 MHz
```

```
begin

 t == now;


        comp <= '1' when iin'above(0.0)
        else '0';


-- Le process detection mesure l'ecart t0 entre deux impulsions de
-- synchronisation et permet ainsi d'en deduire fn
 detection : process
   variable first_pulse : boolean := false;     -- detection 1ere impulsion


 begin

        wait until comp'event;
   if first_pulse then


                        if (comp = '1') then
                        t0 <= t;
                        elsif (comp = '0') then
                        t3 <=t;
                        fn <= abs(1.0/(2.0*(t3-t0)));
                        end if;


   else
     fn <= fc;
     first_pulse := true;
   end if;
 end process detection;
```

```
  --le process ampli mesure l'amplitude du courant de synchro
  ampli : process
          begin
                  wait until not iin'above(-1.0e-6);
                  wait for 5.0e-12;
                  iam <= abs(iin);
          end process ampli;

-- le process mesure le rapport cyclique du signal de synchro
rap_cycl: process
          begin
                  wait until iin'above(0.0);
                  t1 <=t;
                  wait for (3.0/(4.0*fin));
                  wait until not iin'above(0.0);
                  t2 <=t;
                  rap <= abs(t2-t1)*fin;
          end process rap_cycl;


  absolu == abs(2.0*(ff - frc)/deltaf);
  os_synchro <= not(absolu'above(1.0));

  resynchro:process
  begin
--  wait until os_synchro'event;
    wait until os_synchro;
    wait until iin'above(0.0);
      tm <= t;
  end process resynchro;

--le process calcule la freq de l oscillateur libre
```

```
-- Calcul de la frequence propre de l'oscillateur, fonction de la tension de
-- retour vr, comprise entre fc-k*vcc/2 et fc+k*vcc/2
        frequence: process
                begin
                wait for 10.0e-15;
                        frc <= fc + ((vcc/2.0) - vr)*K;
                end process frequence;

  break on fn;

  ff == 1.0e+6*round(fn/1.0e+6);              --lissage de la frequence detectée




-- Cette equation classique d'un oscillateur LC permet d'obtenir la valeur de
-- la capacite equivalente C a partir de f0 et de L
break on frc;
  C == 1.0/(MATH_2_PI*MATH_2_PI*frc*frc*L);
  finm == n*ff;




-- Le process sub_harmonic calcule n, l'harmonique qui synchronise l'OS,
-- en arrondissant la valeur m = f0/fn
  sub_harmonic : process
    variable m : real := 0.5;
  begin
    wait until fn'event;
    m := frc/ff;
    if m<=0.5 then
      n <= 1.0;
```

```
    else
      n <= round(m);
    end if;
  end process sub_harmonic;

-- L'equation suivante determine la plage de synchronisation de l'OS
  break on n, iam, rap;
  deltaf == ((sqrt(2.0)*abs(iam)*sqrt(1.0-
cos(rap*n*2.0*MATH_PI)))/(v0*n*MATH_PI*MATH_PI*C))+10.0;

  dphi == phi'dot;



 (dphi / MATH_2_PI) == (finm-frc)-(deltaf/2.0)*sin(phi);


-- 1% pour simuler le jitter sur l'horloge
break on frc;
  fout == frc*(1.0 + 0.0001*sin(MATH_2_PI*fj*t));

-- L'equation suivante permet d'obtenir une phase comprise entre 0 et 2*Pi et
-- continue (par integration) et une frequence d'oscillation fout

--  t-t0 permet d'avoir l'information de phase du signal de synchro.
  phif == ((MATH_2_PI*fout*(t))+phi);-- mod math_2_pi;


-- L'equation suivante permet simplement d'exprimer la tension de sortie de l'
-- OS en fonction de sa phase



  vout == v0*(1.0+sin(phif))/2.0;
```

```
  iout ==0.0;                --pour le simulateur
end behavioral;
```

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