Optimisation Studies on Strain-Engineered Germanium Heterostructures

by

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ABSTRACT

The physical gate lengths of state-of-the-art CMOS devices are 45 nm and are anticipated to reach just 20 nm by 2007. Due to the prohibitive capital expenditure required for next-generation CMOS technologies, leading device manufacturers are now exploring exotic device architectures and novel substrates in which significant device performance enhancements may by obtained using the existing device fabrication infrastructure.

This thesis reports studies made on an initial evaluation of hole transport properties in strained Ge channels and comprises physical and electrical characterisation of these heterostructures as well as the analysis of SiGe layers using secondary ion mass spectrometry. The initial work of thesis describes the growth, characterisation and optimisation of a novel strained Ge substrate. The substrate technology was developed using a hybrid-epitaxy technique in which a SiGe strain-relaxed buffer layer, so called "virtual substrate", was grown using a ultra-high vacuum chemical-vapour deposition growth technique and the active strained Ge layer was grown using a solid-source molecular-beam epitaxy growth technology. An advanced chemical cleaning procedure has been developed which includes a modified Piranha etch. The novel cleaning procedure enables the successful integration of the two growth techniques.

Significant hole carrier transport enhancements were observed for holes contained within the strained Ge channel. Optimisation of the hole mobility was achieved by the reduction of carrier scattering such as interface roughness scattering and point defect scattering. The optimisation methods employed included growth temperature iterations to reduce Ge channel roughening via elastic relaxation and, channel thickness iterations were also employed in order to minimize channel roughening and defect nucleation. Post-growth annealing procedures were used to combat defects arising from low temperature growth.

The Ge heterostructures were grown on strain relaxed buffer layers, terminating with a Ge content of 60%. The optimised strained Ge channel thickness was found to be 20 nm and the growth temperature of the active layers was reduced to 350°C so as to minimise surface roughening. As grown point defects were eliminated at an optimised post-growth anneal temperature of 650°C for 30 minutes under dry N_2.

Hall mobilities reached 1910 cm^2/Vs at room temperature rising to 26,900 cm^2/Vs at 10 K. A magneto-conductivity transformation measurement and maximum entropy mobility spectrum analysis revealed a room temperature drift mobility of 2700 cm^2/Vs at a carrier density of 1.0×10^{12} cm^{-2}. This result represents a 15-fold increase in hole mobility compared to conventional Si substrates at comparable effective fields.

The second and important part of this thesis addresses charging effects observed when profiling undoped SiGe layers and the quantification of Ge fraction within SiGe layers using secondary ion mass spectrometry.

Due to the highly resistive spreading resistance found for undoped SiGe layers when profiled using an O_2^+ incident beam, charging effects were found to mask the true layer profile. In order to overcome this problem a new approach is discussed for the first time. By illuminating the sample with a red laser light (wavelength 635mn) electron-hole pairs were created via photon absorption. The excess charge carriers were sufficient to overcome localised charging effects induced by the primary ion beam during SIMS analysis. In this manner, total charge suppression was achieved, thereby enabling a true determination of the SiGe sample profile to be obtained via SIMS.

Finally, an analytical method enabling the accurate determination of Ge content of SiGe layers is discussed. The method employs a comparative ion yield methodology and enables both the spatial distribution and Ge concentration of SiGe layers to be accurately determined from a single SIMS measurement.

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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. Except where specifically stated all of the work described in this thesis was carried out by the author or under his direction.

Work discussed within this thesis has been published and presented at conference. The relevant conference and publication details are given below:

- **Conference proceedings**

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- **Journal publications**

Dowsett. M.G, **Morris. R**. Pei-Fen Chou, Corcoran. S.F, Kheyrandish. H, Cooke. G.A, Maul. J.L. and Patel. S.B, Applied Surface Science, (2003), **203-204**, 500.

List of abbreviations

1D	1-dimensional
2D	2-dimensional
2DEG	2-dimensional electron gas
2DHG	2-dimensional hole gas
3D	3-dimensional
AFM	Atomic force microscope
ASF	Absolute sensitivity factor
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapour deposition
DI	De-ionised
FET	Field effect transistor
FLIG™	Floating low energy ion gun
GS-MBE	Gas source- molecular beam epitaxy
HH	Heavy Hole
HRXRD	High resolution X-ray diffraction
HV	High vacuum
IC	Integrated circuit
LEPE-CVD	Low energy plasma enhanced-chemical vapour deposition
LPCVD	Low pressure chemical vapour deposition
MBE	Molecular beam epitaxy
MDQW	Modulation doped quantum well
MFR	Modified Frank Read
MOS	Metal oxide semiconductor

MOSFET	Metal oxide semiconductor field effect transistor
pMOS	Positive-channel metal oxide semiconductor
QHL	Quartz halogen lamp
RBS	Rutherford backscattering
rms	Root mean square
SIMS	Secondary ion mass spectrometry
SS-MBE	Solid source-molecular beam epitaxy
TEM	Transmission electron microscope
UHV	Ultra high vacuum
UHV-CVD	Ultra high vacuum-chemical vapour deposition
ULSI	Ultra large scale integration
VLSI	Very large scale integration
VS	Virtual substrate
XRD	X-ray diffraction
XTEM	Cross sectional transmission electron microscopy

1. Introduction

1.1 Semiconductors and their role in modern day technology

Si is the most widely used semiconductor material for semiconductor device manufacture since it took over from the earlier invention of the Ge transistor back in the 1947, and it is very difficult to see any other rivalling it in the medium term. The major advantages of Si over other semiconductor materials are:

- It is naturally abundant given that it comes from silica which is estimated to be ~25% of the earths crust,

- It is non toxic

- Very high purities can be achieved

- A stable, high quality insulating layer such as SiO_2 can be readily formed.

One negative aspect however is that, compared with other semiconductor materials, especially the III-V materials, Si has an inferior electron mobility, which is now becoming a limiting factor in determining the speed of sub-micron Si devices.

Even so, Si remains the number one choice for Integrated Circuit (IC) manufactures due primarily to economic conditions. Current Si wafers are at 300 mm in diameter and have high purity and low defect densities. By comparison, III-V wafers such as GaAs, and InP, are produced at only 150 mm diameter and contain higher defect densities which results in lower device yields. As a consequence, ICs using III-V compounds are more expensive to manufacture.

In the early years of the IC market, bipolar transistors were the main building blocks, but with the development of Metal Oxide Semiconductors (MOS), such as Field Effect Transistors (FETs), digital MOS devices now prevail. Figure 1.1 shows how the market share between Si HBT's and FET's has changed over the years since Si devices became commercially available. Also shown in figure 1.1 is the small fraction of the market which GaAs devices holds.
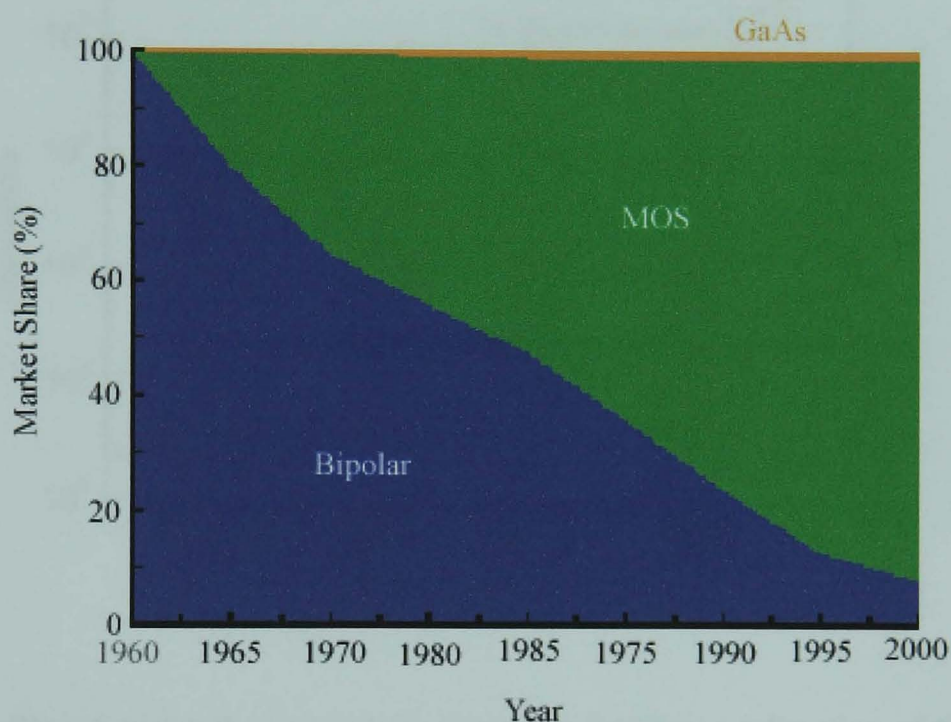
Figure 1.1. Plot showing the market share trend for Si HBT and FET devices since they became commercially available (taken from www.icknowledge.com).

One reason for the continued growth of the IC market has been device miniaturisation. By making devices smaller device speeds have been increased, allowing manufacturers to make faster ICs. However, continued device scaling cannot go on indefinitely, and there is already a trend appearing in the current market where device miniaturisation in slowing down. Researchers across the globe have been pursuing other avenues for many years for an alternative to speed up Si devices in order to supplement the decrease in device miniaturisation with time.

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Since the invention of the planar integrated circuit, the increase in the number of devices with time has followed an exponential trend which was first observed by Gordon Moore, the founder of Intel. The press named the trend "Moore's law" and this title has prevailed ever since. Figure 1.2 shows a plot of Moore's law.
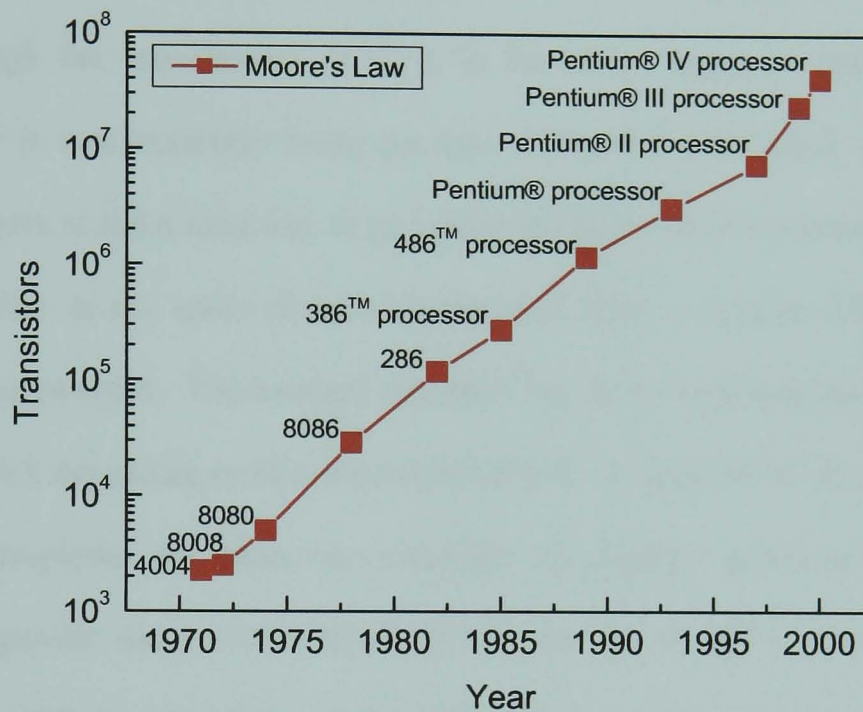
Figure 1.2. Plot showing the increase in transistor density as a function of time, better known as Moore's Law (taken from www.intel.com).

As technology has continued to advance, the doubling of transistors every couple of years for the same area of circuit has been maintained. Scaling cannot continue indefinitely due to physical limitations eg. gate oxide which is now only 5 atoms thick and also economic conditions are coming into play. The capital investment required for a new 300 mm, 90 nm technology node fabrication facility is approximately $4 Billion. The depreciation of this facility must be reflected in the selling price per chip. Due to the large capital investments required for next generation fabrication facilities, semiconductor device manufacturers are now exploring ways by which chip speeds may be increased using existing fabrication facilities.

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1.2 SiGe and its potential

One solution to enhancing the carrier mobility in Si is via bandstructure-engineering. This is where the introduction of a miscible material with Si can lead to superior band structure properties. The most successful material to date is Ge, although the introduction of C is in the early stages of development. SiGe technology is now currently being put into production after many years of research, although there is still a long way to go before this technology is exhausted. Both Si and Ge crystallise in the same diamond lattice and form a random SiGe alloy layer of arbitrary composition. The bandgap variation can be tailored between Si (1.12 eV), and Ge (0.66 eV), depending on the alloy composition. In addition to this, the structural and chemical properties for these two materials are similar, allowing epitaxial growth. Epitaxial growth enables thin layers (a few nm up to 100's of nm) to be readily achieved, which in turn allows layers of Si, SiGe or Ge to be grown under tensile or compressively strained conditions, depending on whether the layer is grown on a substrate with a smaller or larger lattice constant. Structures based on strained layers have enabled devices to make use of the inherent advantages obtained from lower charge carrier effective masses induced by the strain.

In standard Si devices, the carriers are confined to a very thin region adjacent to the SiO_2 interface, where the carrier mobility is found to be low, typically 50-200 cm^2/Vs [Parker and Whall, 1999]. The mobility of holes in this region is lower than electrons, leading to reduced device speeds and ultimately levels of integration. This lower mobility of holes means that p-channel MOS devices have to be bigger than the n-channel MOS devices in order to pass the same current. Due to the larger dimensions there is an increase in power consumption as well as a loss in packing

density across the wafer. By introducing Ge into Si technology, one of the main effects observed has been the pronounced increases in the hole mobility, which had previously been a stumbling block for complementary metal oxide semiconductors (CMOS). Enhanced hole mobilities in strained SiGe and Ge layers have been observed in both modulation doped quantum well structures (MDQW) and MOS devices. For pure Ge MDQW structures, Hall measurements have demonstrated low temperature (4 K) hole mobilites of up to 87,000 cm^2/Vs [Känel et al, 2002] with a carrier density of 6×10^{11} cm^{-2}, whilst room temperature hole mobilites of up to 2,100 cm^2/Vs with a carrier density of 7×10^{11} cm^{-2} have been found [Irisawa et al, 2001]. For Ge MOS devices room temperature mobilities of 2,700 cm^2/Vs have recently been reported [Irisawa et al, 2001], an order of magnitude improvement over hole mobility observed in standard Si pMOS devices.

With the rapidly expanding new markets of mobile communication and other wireless applications operating in the GHz regimes, low noise, high speed and low power consumption devices are required. The enhanced mobility and low noise values now being obtained for SiGe devices should ensure that the future for SiGe technology is healthy. These improvements in the hole mobility has brought a closer parity between holes and electrons which is most important if low power CMOS IC's are going to keep pace with the demands of today's modern equipment.

1.3 <u>Rationale for PhD work</u>

The implementation of Ge into mainstream Si CMOS has demonstrated significant advantages in pMOS devices due to the increase in hole mobility. As a general trend it has been observed that the higher the Ge fraction within the strained

SiGe alloy, the higher the mobility [Hinkley et al, 1989]. It is predicted that the largest hole mobility enhancements will be obtained in pure strained Ge [Fischetti and Laux, 1996] given its naturally occurring higher hole mobility and its lower effect mass. Little previous work had been carried out on the strained Ge channel heterostructure prior to this work, with the optimum hole transport properties showing a mobility of $\sim$1300 cm^2/Vs with a carrier density of $\sim$2$\times$10^{12} cm^{-2} at room temperature and 55,000 cm^2/Vs with a carrier density of 5.5$\times$10^{11} cm^{-2} at 4.2 K [Xie et al, 1993]. The first part of this thesis describes an in-depth study into the structural and electrical optimisation of pure Ge channel heterostructures for advanced CMOS device applications.

The second part of this thesis involves the quantification of Si$_{1-x}$Ge$_x$ layers (x$\leq$0.3) using secondary ion mass spectrometry (SIMS). SIMS has been widely adopted within the Si manufacturing industry to characterise dopant concentrations and their spatial distribution. The current growth in SiGe based devices within the industry also requires similar characterisation via SIMS in order to determine the spatial distribution and atomic fraction of the Ge profile. However, due to the highly intrinsic nature of undoped SiGe epilayers grown using state-of-the-art manufacturing techniques, accurate SIMS analysis has been limited due to sample charging effects. In this work we describe a novel method of charge compensation using optical stimulation. In this manner, sample charging effects are eliminated and accurate SIMS profiles are obtained.

The current chapter has discussed the Si device market, the reasons for the introduction of Ge into Si technology and a brief insight into the rationale for this PhD. The thesis is divided into five further chapters which are outlined below:

Chapter 2 gives the theoretical background behind this work. The chapter itself is divided into three main sections, with the first two explaining the epitaxial growth and formation of strained and relaxed SiGe layers. The final part of this chapter discusses the advantages of such layers from the material's electrical properties perspective.

Chapter 3 provides information regarding the measurement techniques and equipment used for this work. This includes Molecular Beam Epitaxy (MBE) for growth of thin films, X-ray Diffraction (XRD), Secondary Ion Mass Spectrometry (SIMS), Transmission Electron Microscopy (TEM) and Atomic Force Microscopy (AFM) for structural analysis and finally electrical characterisation methods of semiconductor materials.

Chapter 4 presents the results and analysis of the work carried out on pure Ge modulation doped heterostructures grown by Solid-Source Molecular Beam Epitaxy (SS-MBE) on strain tuned virtual substrates (VS) grown by SS-MBE or chemical vapour deposition (CVD). Chapter 4 includes the structural characterisation of such heterostructures using TEM and AFM to investigate dislocation formation processes and the structural integrity of the epilayers. X-ray analysis was used to determine Ge fraction and percentage relaxation, whist doping profiles and Si-Ge inter-diffusion effects were investigated via SIMS analysis. Finally, the electrical transport properties were determined using Hall and mobility spectrum techniques.

Chapter 5 describes an advanced technique developed throughout the course of this work which enables an accurate determination of the structural profiles for SiGe heterostructures grown using CVD techniques. Due to the highly intrinsic nature of such epilayers, conventional SIMS analysis has been shown to be severely hindered due to charging effects during ion bombardment. In this chapter we demonstrate, for the

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first time, a method of overcoming such charging effects using a novel process involving optical laser stimulation. Furthermore, two analytical methods are described enabling the accurate quantification of Ge fraction using conventional SIMS techniques.

Chapter 6 provides a brief summary of the main results from the work carried out throughout this thesis.

2. Theoretical Background

In this chapter a brief review of the theoretical concepts and limitations governing the SiGe semiconductor material are presented. The chapter is divided into three sections. Firstly, the growth of SiGe will be addressed along with the two most common growth techniques, namely Molecular-Beam Epitaxy (MBE) and Chemical-Vapour Deposition (CVD). This will then be followed by a section discussing the use of SiGe as a means of forming a Virtual Substrate (VS) for growing higher composition SiGe/Ge structures. Finally, the fundamental properties of Si, Ge and the combination of these two semiconductors to form heterostructures for device applications will be discussed.

2.1 Growth of strained layer semiconductor heterostructures

2.1.1 Growth of SiGe

Epitaxy is the growth of single-crystal layers upon a single-crystal semiconductor substrate. Thin layer growth of semiconductor material's using a technique such as MBE revert to three main growth regimes:

1. Frank-van der Merwe (FvdM)

2. Volmer-Weber (VW)

3. Stranski-Krastanow (SK)

In the case of FvdM growth, the deposited film will grow on the surface layer by layer forming a smooth continuous 2D layer. During VW growth, the deposited material forms islands, resulting in a 3D layer. Finally Stranski-Krastanow (SK) growth is a combination of the two previously mentioned growth modes, where the initial few monolayers of the deposited film grows in a 2D form until the build up of strain energy becomes too much, triggering a 3D growth transition and allowing local strain relaxation. Figure 2.1 shows a schematic diagram of all three growth modes.

F-vdM Growth mode   V-W Growth mode   S-K Growth mode
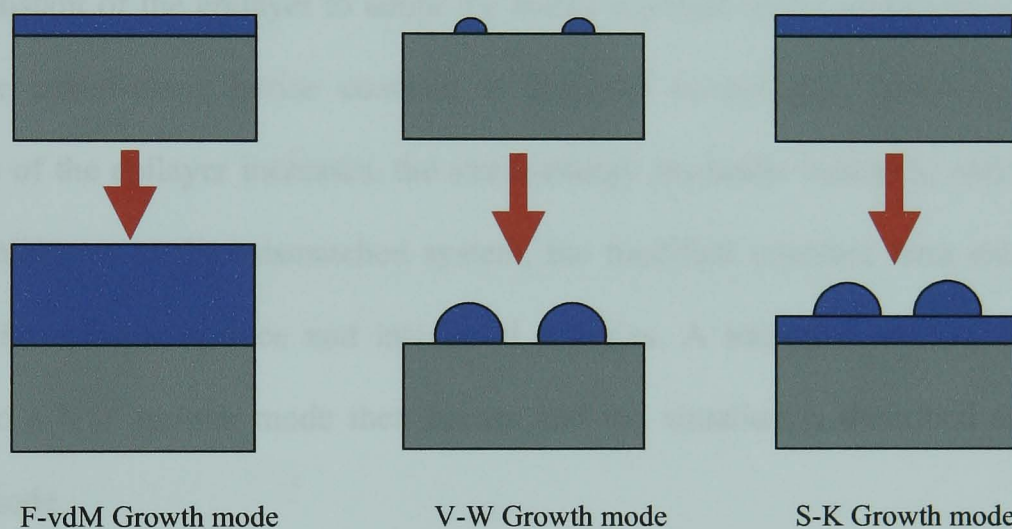
Figure 2.1. Schematic representation of three growth modes possible for MBE.

The particular growth mode that will prevail is dependent on the relative magnitudes of the interfacial free-energy terms and the lattice mismatch of the deposited material to the substrate. Such a process of growth kinetics was first postulated by Burton *et al* [Burton *et al*, 1951], and is known as the Burton-Cabrera-Frank (BCF) model. In the case of lattice-matched systems, Eaglesham and Cerullo [Eaglesham and Cerullo, 1990] suggest that island formation is driven predominantly by high interfacial energies and large epilayer surface energies. According to Eaglesham, 3D growth occurs when the substrate free energy exceeds the sum of the epilayer surface energy

and interfacial energy. In this case, island formation is observed and the growth mode is described as VW. If the sum of the epilayer surface energy and interfacial energy exceed that of the substrate free energy, then a 2D FvdM growth mode is obtained. For the case of the lattice mismatched heteroepitaxial system, the strain energy increases with mismatched layer thickness. If the condition for FdMV growth is met then the film will wet the substrate and 2D growth will uniformly and commensurately form, as in the lattice matched system. In this case, the strain induced within the growing epilayers causes a tetragonal distortion of the epilayer unit cell, forcing the in-plane lattice constant of the epilayer to adopt the lattice constant of the underlying substrate, while the out-of-plane lattice constant is distorted accordingly. However, as the thickness of the epilayer increases, the strain energy gradually increases, until at some critical thickness in the mismatched system, the modified interface term exceeds the sum of the epilayer surface and interfacial energies. A transition from a 2D FvdM growth to a VW growth mode then occurs and the situation is described as the SK growth mode.

Bean *et al* [Bean *et al*, 1984] has shown that by controlling the temperature at which the SiGe material is grown, the onset of island formation can be delayed, or at least controlled. Bean found that 2D growth of $Si_{0.9}Ge_{0.1}$ could be achieved for temperatures up to $\sim750^{\circ}C$ while if the growth temperature was reduced to $550^{\circ}C$, the 2D growth of a pure Ge film was possible as shown in Fig 2.2.
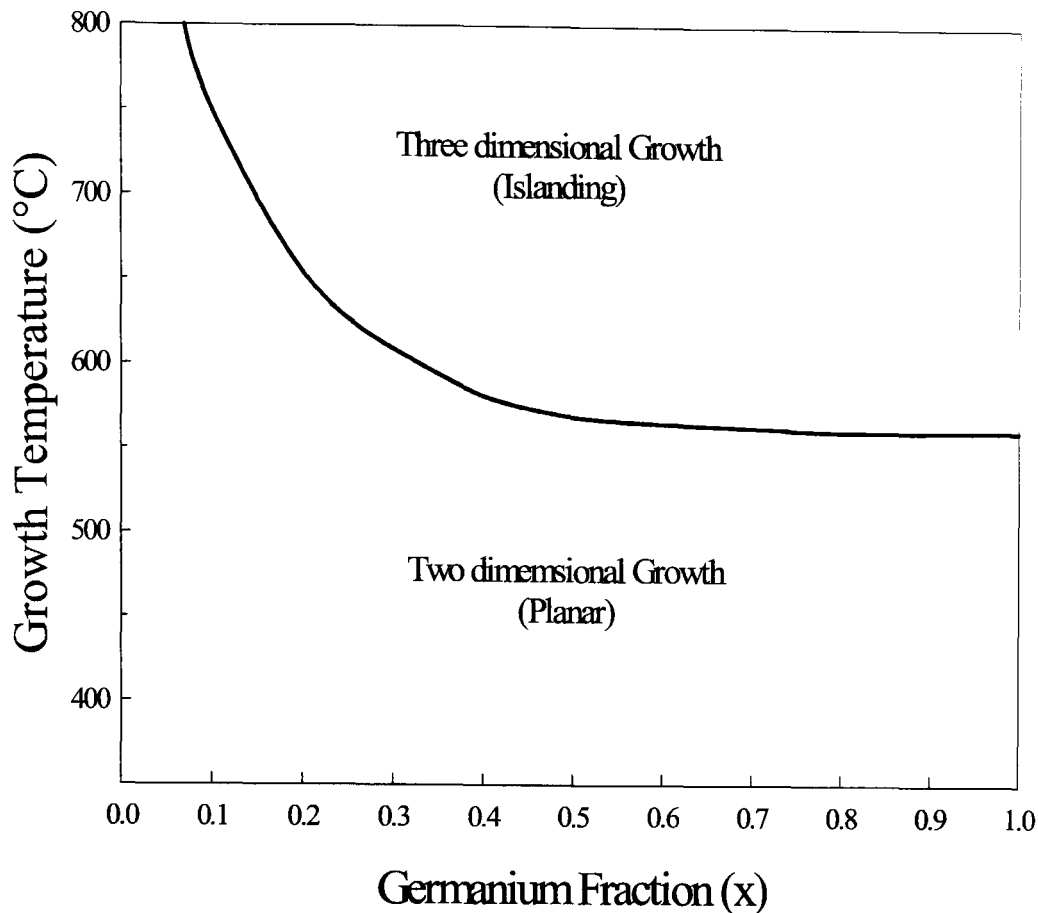
Figure 2.2. Plot of growth temperature dependence on growth mode for a $Si_{1-x}Ge_x$ alloy on Si (001) (taken from Bean *et al*, 1983).

2.1.2 SS-MBE and CVD

There are two main types of growth techniques used today in order to grow high quality SiGe heterostructure material, namely MBE and CVD growth. It is not the author's intention to provide a detailed overview of each individual growth technique and so the reader is referred to papers and review articles by Ashu and Matthai [Ashu and Matthai, 1991], Eaglesham and Cerullo [Eaglesham and Cerullo, 1990], Hartmann *et al* [Hartmann *et al*, 2000] and references within for a more comprehensive understanding of Solid-Source Molecular Beam Epitaxy (SS-MBE) and Gas-Source Molecular Beam Epitaxy (GS-MBE) growth.

Similarly the reader is referred to an excellent review article by Greve [Greve, 1993] who provides a useful introduction to CVD growth.

In the case of SS-MBE, the heterostructure layer is grown by evaporating the semiconductors (Si, Ge) from a solid source. The evaporated atoms impinge onto the cleaned substrate surface. The impinging atoms normally have a higher thermal energy than the substrate and so the substrate is held at a raised temperature in order to supply enough surface energy to maintain adatom mobility and increase crystallinity. This work must be performed under Ultra-High Vacuum (UHV) conditions such that there is no interaction between the molecular beam and residual background contaminants. The main characteristics that the MBE growth technique offers are independent control of growth parameters, low controllable growth temperatures enabling minimisation of solid state out diffusion and auto doping, and low growth rates and shutter control which permits thin, highly uniform layers to be grown.

Whilst SS-MBE has demonstrated high wafer uniformity and ultra-sharp doping profiles, the method does have some inherent limitations. A major limitation is the low wafer through-put and in certain cases a lack of accurate in-line calibration diagnostics during growth. The lack of in-line calibration is particularly missed during the growth of thick (several micron) epilayers and arises from the depletion of the solid-sources material. Typically, for the growth of SiGe epilayers, the solid atomic sources are evaporated via electron beam impingement. However, since the sources are finite, during growth of thick epilayers, the sources are gradually depleted and the initial calibration may fluctuate. In order to overcome this problem, material flux calibrations are required on a rather frequent basis which is time consuming. SS-MBE is therefore quite a slow growth process and is mainly reserved for research rather than industry. Production line scale growth of SiGe epilayers is routinely reserved for CVD.

For CVD, a gas containing the material wished to be deposited, known as a "pre-cursor", is passed over a heated substrate. Under the correct conditions the gas will chemically react with the substrate and produce an epilayer deposition. The standard chemical gases used for the SiGe system are Silane (SiH$_4$) and Germane (GeH$_4$) which are passed down a furnace tube using a carrier gas, typically Hydrogen. This technique offers high growth rates, simultaneous growth of wafers and the technique is more stable and reproducible for thick structures. In addition, the growth of thick layers is possible since the gas sources are effectively infinite and the gas ratios can be constantly maintained and monitored throughout the growth via the use of mass flow control units. It is therefore the technique favoured by industry. CVD grown material is heavily used for VS growth (see section §2.2) due to their large thicknesses and high yield demands which is something that has been studied and used in this work and is discussed in detail at a later stage of this thesis

2.1.3 The equilibrium critical thickness (h$_c$)

In today's modern device technology both strained and relaxed SiGe structures are required. They have now even been integrated on one chip in order to yield better device properties. Relaxed SiGe layers are discussed in detail in section §2.2 of this chapter. The present discussion will be limited to strained layer heteroepitaxy.

When considering using a highly strained layer for device purposes it is important to know the limits with regard to the amount of strain the layer will accommodate and thickness to which the layer can be grown before plastic relaxation occurs. The point at which the thickness leads to the onset of relaxation is known as the *'equilibrium critical thickness'* (h$_c$). The equilibrium critical thickness is the point at

which misfit dislocations become energetically favourable to form within the semiconductor layer. This was first calculated by van der Merve [van der Merve, 1963] using the principle of energy balance for misfit dislocation formation. However the classical model used for predicting this equilibrium critical layer thickness, is the Matthews and Blakeslee (MB) 'mechanical equilibrium' model [Matthews and Blakeslee, 1975]. The MB model equates the net force exerted by the strain of the misfit dislocation on a pre-existing threading-dislocation to the tension within the total dislocation line-length.

The metastable critical thickness (see §2.1.4) of a SiGe epilayer grown on a Si substrate is dependent upon two critical parameters. Firstly, the temperature at which the layer is grown as discussed previously in section §2.1 1. The metastable critical thickness of a SiGe epilayer can be increased by reducing the growth temperature. However, with the reduction of growth temperature a transition from high quality, low defect single crystal growth to high defect density material occurs, while lowering the growth temperature further will lead to poly-crystalline growth due to the reduced adatom mobility. The second influencing factor is the fraction of Ge grown within the SiGe alloy layer. The higher the amount of Ge, the larger the lattice mismatch, hence the greater the strain energy induced. Since the total strain energy of the epilayer is dependent upon its thickness, an increased Ge content leads to a reduction in the thickness of the epilayer prior to the onset of plastic relaxation i.e. as the Ge content of the film is increased, the critical thickness of the film (at a given growth temperature) decreases accordingly. Figure 2.3 shows the MB criterion for a SiGe epilayer grown on a Si(100) substrate by MBE at a growth temperature of 550°C. For a layer below the equilibrium critical thickness, relaxation cannot occur because the elastic energy stored in such a homogeneously strained layer is lower than the elastic energy associated with

the local distortion around the misfit dislocation. However, for epilayer growths which exceed the equilibrium critical thickness, plastic relaxation occurs due to the formation of misfit dislocations.
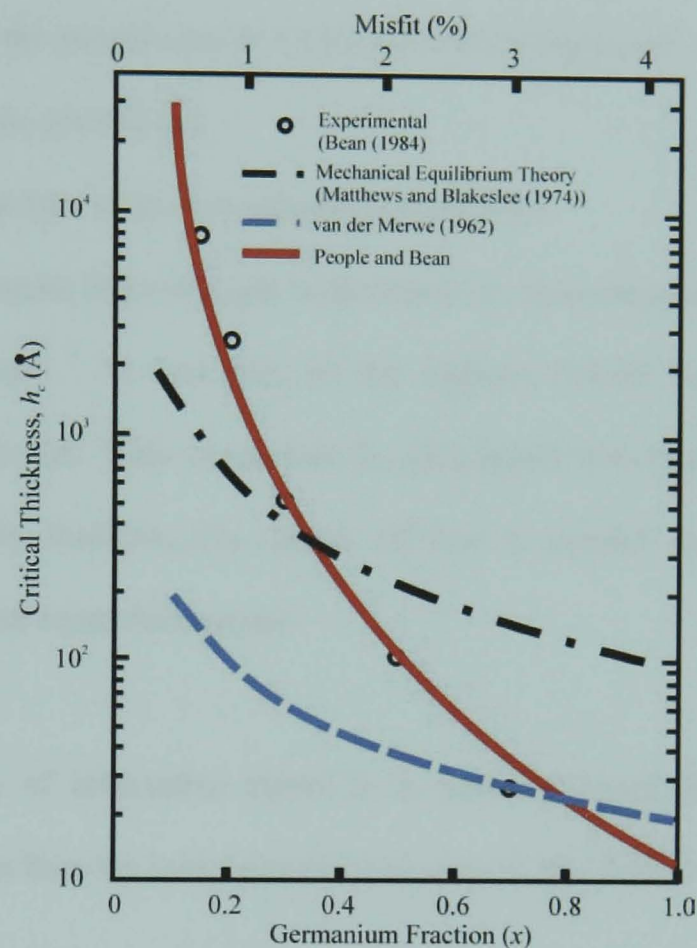
Figure 2.3. Plot showing the experimental and calculated critical thickness (h_c) as a function of Ge fraction and misfit percentage (Taken from People and Bean, 1985).

2.1.4 The metastable critical thickness

The equilibrium critical thickness can be calculated from the parameters of the material under investigation and this value is the one usually cited. However, strained SiGe layers exceeding the equilibrium critical thickness have been grown [Bean *et al*, 1984]. Such layers fall into a region referred to as the *"metastable"* critical thickness. This region appears between the equilibrium critical thickness and the experimental

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measurement of critical thickness (h_c). The thickness of the metastable layer depends on numerous factors with the main ones listed below.

1. Decreasing the temperature at which the layer is deposited,

2. Increasing the growth rate

3. Selecting the type of growth interface orientation.

4. The inter-atomic barrier height with respect to dislocation motion, known as the Peierls barrier. Si has one of the highest Peierls barriers while Ge is significantly less. This means that $Si_{1-x}Ge_x$ layers with high x values will relax more readily than $Si_{1-x}Ge_x$ layers of low x content for equivalent lattice mismatch and layer thicknesses.

In the case of metastable layers it is typically found that when heated to temperatures greater than the initial growth temperature, the layer will begin to relax.

2.2 Tuning of strain - The Virtual Substrate (VS)

2.2.1 Requirement of the VS

Historically, Si CMOS performance enhancements have been achieved by conventional lithographic scaling techniques in which the active device gate lengths have shrunk. In this manner, improved saturated drain currents have been achieved along with increased device operating frequencies. However, due to the prohibitive costs required for continued device scaling, alternative approaches are being employed to improve device performance. One such approach employs the inclusion of strained

layers within the active regions of the device. In this manner the mobility of the active charge carriers may be enhanced, thereby improving device performance.

In the case of SiGe, the thickness to which a strained SiGe/Ge layer can be grown on a Si substrate is limited by an equilibrium critical thickness, which may vary slightly depending upon certain conditions and the way relaxation occurs. The Mathews and Blakeslee model (MB criterion) discussed in section 2.1.3 provides a fundamental energy balance approach to understanding epilayer critical thickness. The critical thickness is of paramount importance to obtaining high mobility carrier gases within the strained Si/SiGe/Ge heterosystem, since the inclusion of misfit dislocations act as scattering centres for electronic charge carriers and thereby reduce carrier mobilities. In order to achieve good carrier confinement for a two dimensional carrier gas (2DCG), the best results have been reported for a strained layer of the order of several nanometers. Due to the lattice mismatch, it is very difficult to achieve thick strained layers of SiGe with a Ge fraction of $\geq 60\%$ directly on a Si substrate without misfit dislocations forming and relaxing the material. Cyca *et al* [Cyca *et al*, 1997] has demonstrated a working buried channel device structure which had a 1 nm strained Ge layer on Si. For such a structure, the stringent constraints that have to be applied in order to obtain a working device leave very little scope for variation in the structure for optimisation.

A way to overcome this problem is to form a relaxed buffer layer also referred to as a virtual substrate (VS). A VS is achieved by growing a layer of SiGe at the required Ge fraction and relaxing it by allowing dislocations to form. This may sound exactly like what you would want to avoid from a device material point of view. However, much work has been carried out on these substrates and using the correct method and under the right conditions, the material can be forced to relax with limited threading

dislocations and minimal surface roughness. By utilising a lattice tuning VS, the mismatch strain energy of an overlaying strained Ge layer may be reduced, allowing for a thicker strained Ge layer to be realised. It also enables strained SiGe layers of lower Ge fraction than the SiGe VS or even a strained Si channel to be grown. This paves the way for both 2D hole gas (2DHG) and 2D electron gas (2DEG) structures to be developed on the same wafer. The ultimate goal of enhancing the performance of 2DHG structures and integrating them on one wafer alongside 2DEG devices (CMOS) therefore looks a much more realistic prospect by using SiGe.

The growth of a thick SiGe film of uniform Ge composition on a Si substrate results in a threading dislocation density of the order of 10^9-10^{12} cm^{-2} [LeGoues et al, 1992]. This level of threading dislocation density is not suitable for FET device structures. However, several methods have been developed whereby the density of threading dislocations may be reduced by several orders of magnitude. By utilising such methods, VS's with a terminating Ge content ranging from 20% to 100% have now been developed with threading dislocations of ~10^6 cm^{-2} or less.

The following sections introduce the mechanisms employed in the relaxation and optimisation of relaxed SiGe VS's.

2.2.2 Strain relaxation processes and their consequences applied to SiGe VS's

In recent years, there has been a significant amount of work performed to understand the relaxation mechanisms of a SiGe film which is grown in excess of its critical thickness. Emphasis has been placed on the optimisation of the relaxation process in order to apply it to modern device structures. As has been discussed, once

the mismatched material exceeds its critical thickness, misfit dislocations are formed at the interface between the epilayer and substrate. Associated with the formation of misfit dislocations are threading dislocations. Threading dislocations are one of the most detrimental problems with the relaxation of SiGe for VS's. It is imperative that the number of threading dislocations is kept to a minimum in order for the VS to be of any use in Ultra Large Scale Integration (ULSI) processing. As previously mentioned, misfit dislocations form due to the excess strain build up in the layer once it exceeds the critical thickness. Upon such an event, misfit dislocation segments form along the [110] directions with the resulting threading dislocation gliding on the 60° {111} planes [Matthews and Blakeslee, 1972]. Problems occur when the threading dislocation of the elongating misfit segment becomes pinned by the strain fields associated with pre-existing orthogonal misfit dislocations present on the same atomic plane or other defects within the material. If the excess stress in the misfit is not large enough to overcome the stress field associated with the impurity, defect or misfit dislocation, the threading dislocation becomes pinned at this location. In order for the strain relaxation process to continue, further misfit dislocations with subsequent threading arms must be formed. This pinning process is a major factor that dictates the eventual threading dislocation density of the relaxed film.

LeGoues *et al* [LeGoues *et al*, 1991] proposed a model for the relaxation of a linearly graded SiGe layers which has now been universally accepted. From its understanding, the threading dislocation density of relaxed SiGe films can be controlled. The mechanism enables the strain relieving defects to be buried within in a compositionally graded layer as well as deep into the Si substrate. LeGoues showed that when a layer of SiGe is deposited upon a Si substrate with the layer thickness taken past the equilibrium critical thickness, a few dislocations are formed. These

dislocations may be in the form of half loops from the surface or as loops nucleated from defects present in the epilayer. Once a network of defects is produced, the intersecting dislocations form nodes which then begin to act as Frank-Read sources [LeGoues *et al*, 1992]. The Frank-read process is schematically depicted in figure 2.4.

Interfacial
dislocation

(a) Ge A ▼ B   (b) Ge A B

Si   Si

(c) Ge A B   (d) Ge A B

Si   Si

(e) Ge A B   (f) Ge A B

Si   Si

(g) Ge A B

Si
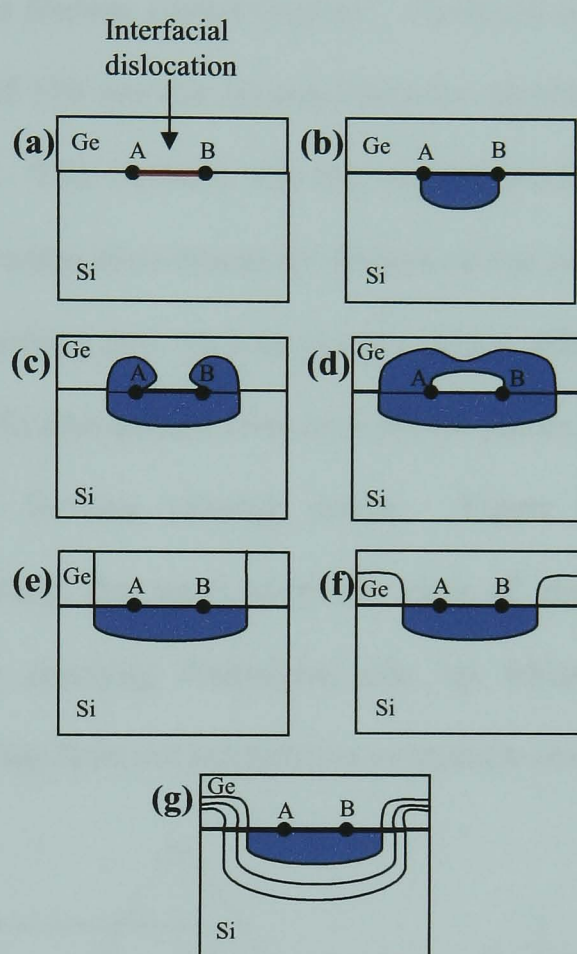
Figure 2.4. Schematic representation of the stages leading up to the nucleation of Frank-Read type dislocations to relive strain. (a) Interfacial dislocation pinned between two points, (b) shows the dislocation bowing into the substrate causing slip as indicated by the blue shaded region, (c) dislocation loops into epilayer, (d) loops combine, (e) loop reaches surface and forms two threading components leading to a half loop, (f) threading components glide to form two more misfits, (g) further loops form pushing the previous loop further down into the substrate.

LeGoues extended his model of Frank-Read generation for epilayer relaxation with a model where dislocation multiplication by a modified Frank-Read mechanism (MFR) [LeGoues, 1994] occurs. This method of relaxation was observed for both graded SiGe structures and uniform composition SiGe layers where the Ge fraction was

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<0.2. The MFR mechanism is simply an extension of the Frank-Read process. The difference between the two processes is that in the case of the MFR process, two pre-existing misfit dislocations gliding in two perpendicular <110> directions combine to act as Frank-Read sources. For this process to yield good results there is a minimum distance between the pinning points required. LeGoues determined that in general a minimum distance of 130 nm was required between pinning points for these to act as Frank-Read sources. This explains why this process works better for graded SiGe/Si layers because if too many dislocations are formed on one single plane, the likelihood of these dislocations meeting and forming pinning points will be higher than for graded layers where the misfit dislocations form on different planes, lowering the probability of them meeting and forming pinning points. Figure 2.5a shows a schematic representation depicting the cross sectional view of the initial orthogonal misfit interaction and the resulting dislocation pile up whilst 2.5b shows the planar microstructure resulting from the annihilation of multiple interactions.
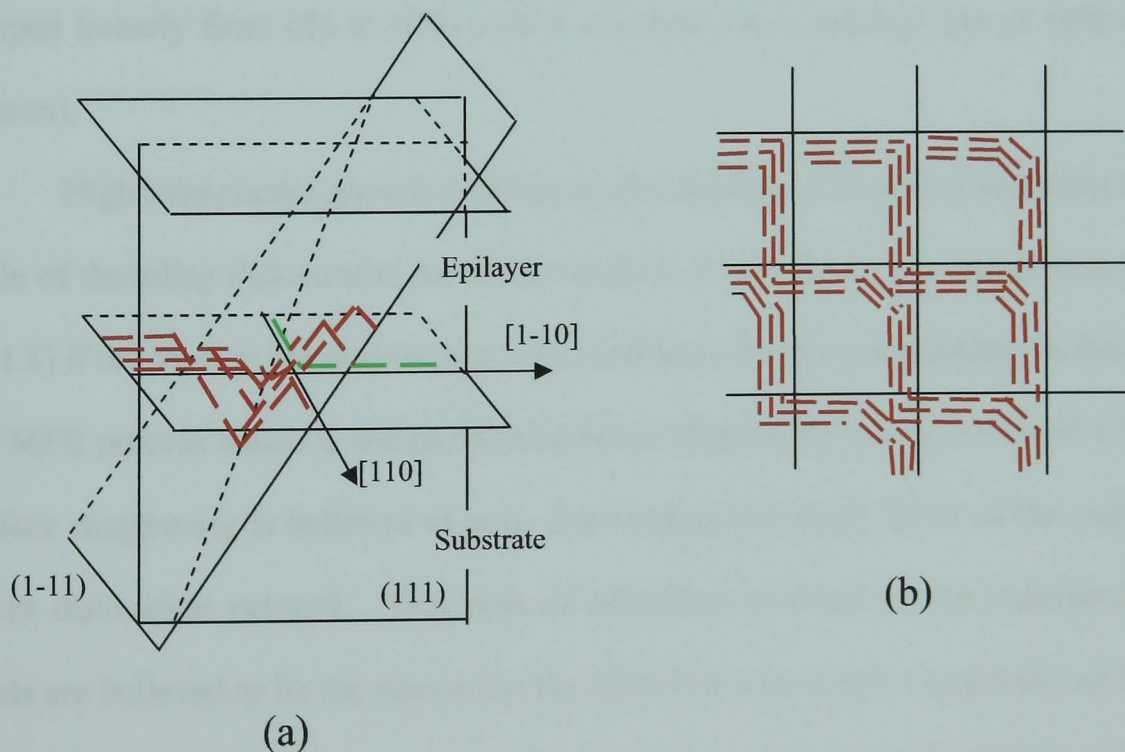
Figure 2.5. (a) represents a cross-sectional view of the MFR dislocation pile up while (b) the plan view microstructure resulting from multiple interactions and annihilation.

In addition to the pile up of corner dislocations, certain threading dislocations will have opposite Burgers vectors and will annihilate. Given the amount of pile ups and threading dislocations created across a wafer, a network of pre-existing dislocations acting as self aligned sources are generated, leading to large scale annihilation of threading components. This reduces the number of pinned dislocations that in turn leads to a greatly reduced threading dislocation density. This MFR process has been shown to yield threading dislocation densities of several orders of magnitude less than other relaxation processes demonstrated.

2.2.3 Linearly graded VS's

The most popular and successful way to date for producing high quality SiGe VS's employs a linearly graded layer followed by a constant compositional layer. Typically, for a VS with a terminating Ge content of 60%, the Ge fraction of the VS is ramped linearly from 0% to 60% over 6 microns (i.e. a grading rate of 10% Ge per micron).

High temperature growth is favoured for enhanced dislocation formation and the glide of threading dislocations but it also leads to strain-driven 3D growth (see section §2.1.1) if the layer is not relaxed, and will yield large surface roughening. In the case of the MFR process which is the preferred method adopted for growing relaxed VS's, the surface roughening is believed to arise from associated strain fields of the underlying misfit dislocation network. This type of relaxation mechanism and associated strain fields are believed to be the reason for the observed cross-hatch roughening of linearly graded VS's. Hsu *et al* [Hsu *et al*, 1992] studied the cross-hatch formation of linearly graded SiGe VS's and found that this cross-hatch pattern does arise from

inhomogeneous strain fields associated with the misfit dislocations combined with the long surface atom diffusion length for high growth temperatures. They also observed that the surface roughness of the cross-hatch increases with the final Ge content or increased grading rate. Strain fields arising from the termination of threading dislocations resulted in shallow depressions at the surface. Any kind of surface roughening will have an effect on any subsequent processing of the material and is therefore required to be minimised. By choosing the correct Ge grading rate and temperature it is possible to minimise threading dislocation formation by allowing the misfit segments to form on different planes, reducing the likelihood of orthogonal pinning events. Once the required relaxed Ge fraction has been obtained within the graded region, a constant composition layer is grown. This constant compositional layer is lattice matched to the terminated Ge content of the linearly graded buffer and remains free from misfit dislocations yielding a low threading dislocation density of $10^6 \, \text{cm}^{-2}$ or less at the VS's surface. Typical grading rates that have been found to work best for such structures are 10% Ge per micron, Fitzgerald *et al* [Fitzgerald *et al*, 1992] and Hohnisch *et al* [Hohnisch *et al*, 1995].

There are numerous papers and reviews of such buffer layers and the author suggests the papers and reviews by Fitzgerald *et al* [Fitzgerald *et al*, 1999], LeGoues *et al* [LeGoues *et al*, 1992] and Mooney [Mooney, 1996] for a more detailed explanation of such VS and dislocation interactions.

2.3 Properties of Si, Ge and SiGe

2.3.1 The energy band structure of Si and Ge

The electronic properties of semiconductor materials are determined by the number of electrons excited into the conduction band and the holes in the valence band. Taking the origin of k-space to be at the band maxima and minima, charge carriers occupy their respective minimum energy configurations ie. in the case of holes the valence band maxima, and in the case of electrons the conduction band minima. The energy (E) versus wave vector (k) relationship for the carriers may be approximated by the quadratic form they take near such extremes and can be expressed as:

$$E_n(\mathbf{k}) = \varepsilon_n + \frac{\hbar^2 \mathbf{k}^2}{2m^*}$$

(2. 1)

Where $\hbar$ is the Reduced Plank constant, m^* the effective mass, ε_n the band energy, and $\mathbf{k}=(k_x, k_y, k_z)$.

Both Si and Ge have a diamond structure and their respective bandgaps are 1.12 eV and 0.66 eV. Experimental results have shown that for Si, the conduction band has six symmetrically related minima along orthogonal <100> directions, approximately 20% from the Brillouin zone boundary, near the X point (referred to as the Δ minima). For Ge, the conduction band minima occurs in the <111> directions (L minima). There are eight half-ellipsoids of revolution along the <111> axes. The Brillouin zone boundaries in the case of Ge are at the middle of the ellipsoids. Figure 2.6 shows the constant energy ellipsoids for both Si and Ge.
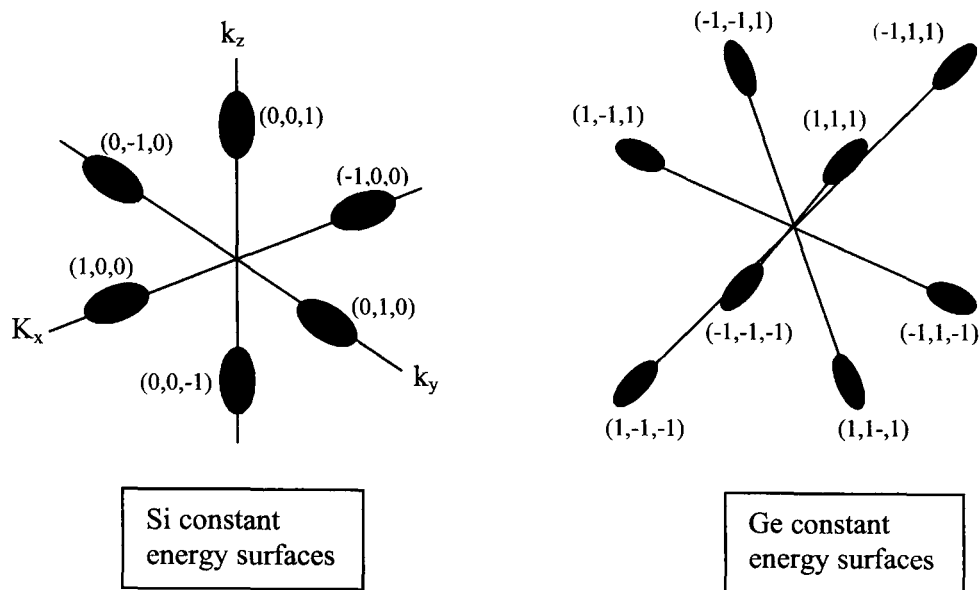
Figure 2.6. Constant energy ellipsoids for Si and Ge.

2.3.2 Heterostructures

The idea behind growing heterostructures is to manipulate the behaviour of electrons and holes by modifying the materials band structure. Different semiconductor materials have different energy gaps between their conduction and valence bands. By bringing two semiconductor materials together it has been found that the new alloys properties may lead to improved electrical characteristics allowing novel device material design with tailored performance. This concept is usually referred to as *'bandstructure-engineering'* and is fully exploited in the III-V semiconductor industry, for instance GaAs/GaAlAs heterostructures.

A heterostructure must involve layers that are crystallographically compatible as most semiconductor devices depend upon highly crystalline material. Therefore a heterostructure is only useful if atomic order is preserved where the two material interfaces meet. Generally this requires that not only do the semiconductor materials have to have the same crystalline structure (eg cubic as in the case of Si and Ge) but that

their atomic spacing is similar. The other point to note and of great importance is that the two materials must be chemically compatible in order for them to combine and make a heterostructure.

2.3.3 SiGe heterostructures

Of the group IV materials both Ge and C are chemically and crystalline compatible with Si. Silicon carbide is a major industry of its own, especially within the power transistor technology market sector, since C has a thermal conductivity of ~10 times that of Si. In the case of Ge the crystalline structure has an atomic spacing of ~4.2% larger than that of Si. This lattice mismatch is more than sufficient to disrupt the crystalline order at the SiGe heterostructures interface. However this problem may be overcome if the SiGe heterostructure is grown correctly and under certain stringent conditions whereby the magnitude of the lattice mismatch is minimised due to the growth of alloy layers.

If an alloy (such as SiGe) is grown epitaxially on Si there are two ways in which the layers can bond together. Firstly, both layers can retain their independent crystal structure. In this case fourfold bonding cannot be maintained along the layer interface, and it will be found that occasional atoms will be left with only three bonds attached. This usually occurs in the form of a misfit dislocation as is shown schematically in figure 2.7a. These misfit dislocations will not just be localised at the interface plane but they form threading dislocations which will terminate at the alloys surfaces. This will lead to threading dislocations passing through the active region of the structure causing a detrimental behaviour in the materials electrical properties.

Relaxed SiGe epilayer

Compressively
strained SiGe

Tensile strained Si

Si Substrate

Si Substrate

SiGe VS

Misfit
dislocations
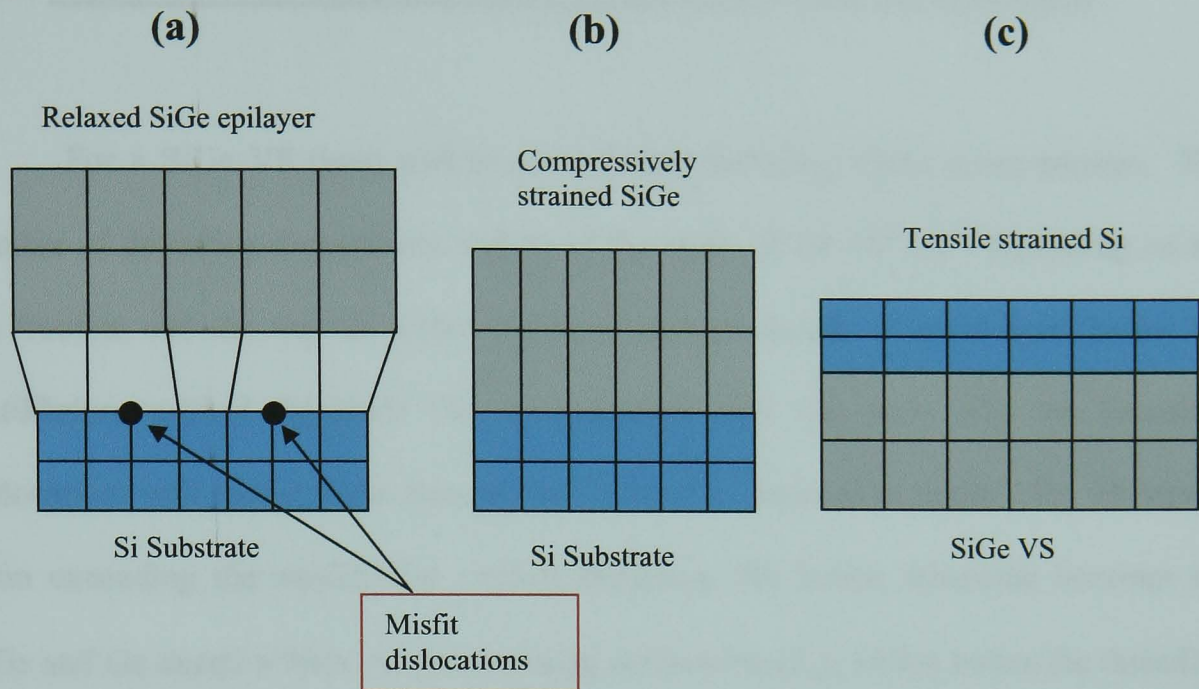
Figure 2.7.. Schematic diagram showing (a) relaxed SiGe epilayer, (b) compressively strained SiGe epilayer and (c) tensile strained Si layer.

Two alternative bonding arrangements are shown in figures 2.7 b & c. Due to the elasticity of the Si and Ge atoms, a sufficiently thin layer can distort to lattice match itself to the substrate material. Given that Ge has a larger lattice spacing compared to that of Si, the Ge (or SiGe) deposited on Si will compress itself so as to lattice match in the in-plane direction. However, to retain the fourfold bonding, the perpendicular (out of plane) lattice spacing is elongated. This is referred to as '*compressive strain*' and is depicted schematically in figure 2.7b. The inverse of this situations occurs when Si is deposited on Ge or SiGe, in which case the Si lattice will elongate parallel to the growth direction while to compensate for this the lattice spacing is compressed in the growth direction. This is referred to as '*tensile strain*' as is shown schematically in figure 2.7c. As the thickness of the layer is increased, the strain energy will build up until a certain point is reached where the interface will sheer and become partially relaxed or revert back to its fully relaxed structure by the formation of misfit dislocations as previously mentioned.

2.3.4 <u>Misfit dislocations and their effect on a strained (Ge) layer</u>

For a SiGe VS there will be pre-existing threading dislocations present. The number of threading dislocations will be of the order of 10^2-10^6 cm^{-2} depending on the Ge fraction and the way in which the layer was produced. If a Ge layer below the equilibrium critical thickness (h_c) is deposited onto the SiGe VS, the threading dislocations will pass straight through the Ge layer as depicted in figure 2.8a. However, upon exceeding the equilibrium critical thickness, the lattice mismatch between the SiGe and Ge exerts a force on the threading dislocation (F_σ), which forces the threading dislocation to glide along the SiGe/Ge interface, forming an interfacial misfit dislocation (figure 2.8b).
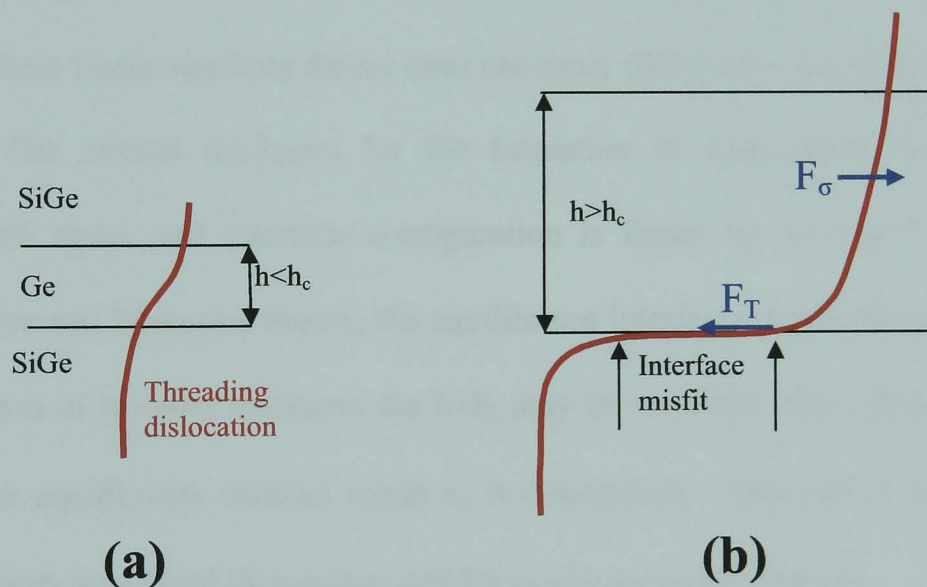
Figure 2.8. Schematic diagrams showing the way a threading dislocation can lead to interfacial misfits by exceeding the critical thickness.

The magnitude of F_σ determines the length of the misfit segment and will relax the strain energy within the Ge layer. From isotropic linear elastic theory, F_σ is given as

$$F_\sigma = 2Gbh\varepsilon \cos\lambda \frac{(1+\upsilon)}{(1-\upsilon)}$$

(2. 2)

Whilst from the self energy of the interfacial misfit dislocation created, a restoring line tension force (F_T) which is given by dislocation theory (equation 2.3) will be formed

$$F_T = Gb^2 \frac{(1-\upsilon\cos^2\theta)}{4\pi(1-\upsilon)} \ln\frac{\alpha h}{b}$$

(2. 3)

where b is the Burgers vector, h is the Ge thickness, G the shear modulus of the Ge, υ Poisson ratio, ε the lattice mismatch strain between the SiGe and Ge, λ the angle between the misfit dislocation Burgers vector and a line in the interface drawn perpendicular to the dislocation line direction, θ the angle between the dislocation line and its Burgers vector and α is a factor which describes the energy of the dislocation core, where linear elasticity theory does not apply [Matthews and Blakeslee, 1974].

The critical thickness for the formation of dislocations at a given lattice mismatch strain and interface configuration is found by solving $F_\sigma = F_T$. From the Matthews and Blakeslee theory, the equilibrium interfacial misfit dislocation density as a function of epilayer thickness for $h > h_c$ may be resolved. By solving $F_T = F_\sigma$ for any $h > h_c$, an equilibrium residual strain ε_o is determined. This can be translated into an equilibrium interfacial dislocation density ρ_{md} by using the relation:

$$\varepsilon_i - \varepsilon_o = (b\cos\lambda)\rho_{md}$$

(2. 4)

Where ε_i in the above equation is the initial lattice mismatch before any dislocations are formed and is defined as:

$$\varepsilon_i = \frac{a_{layer} - a_{substrate}}{a_{substrate}}$$

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Where a_{layer} is the epilayer lattice spacing and $a_{substrate}$ the substrate layer spacing.

From equation 2.4 and $b = \dfrac{a_{Si}}{\sqrt{2}}$, the Burgers vector (b) of the Si system, the amount of

relaxation (R) due to the misfit dislocation density may be determined from:

$$R = \left(\frac{a_{Si}}{2\sqrt{2}\varepsilon_o} \rho_{md} \right) \times 100$$

(2. 6)

Where a_{Si} is the Si lattice parameter.

2.3.5 The effect of strain on the SiGe Bandstructure

The bandgap of SiGe is strongly influenced by strain in the crystal due to the 4.2% difference in lattice size between Si and Ge. When the two materials are brought together in a thin film, one distorts elastically to accommodate the other in-plane lattice spacing. This leads to a movement in the edges of the materials bands and is referred to in terms of deformation potential.

In the case of electrons, strain is used to control the difference in continuity between the conduction bands ΔE_c of the two materials and lower the electrons effective mass. It is found that the larger the difference the better the carrier confinement achieved. Complications arise if there are multiple valleys in the conduction band such as are found in Si and Ge. These multiple valleys in the conduction band occur at different points in k-space, Δ in Si and L in Ge. The point at which the Si and Ge band structures cross is at x~85% for the unstrained $Si_{1-x}Ge_x$ alloy as depicted in figure 2.9.

The bandgap of the $Si_{1-x}Ge_x$ alloy layer is affected very strongly by strain. The introduction of strain leads to a splitting of the heavy-hole/light-hole valence bands

maxima. The main effect of compressive strain is the reduction of the indirect bandgap with increasing Ge fraction, along with a suppression of the Si-like to Ge-like band structure. The strain induced split heavy-hole and light-hole valence bands as a function of Ge fraction are also shown in figure 2.9.
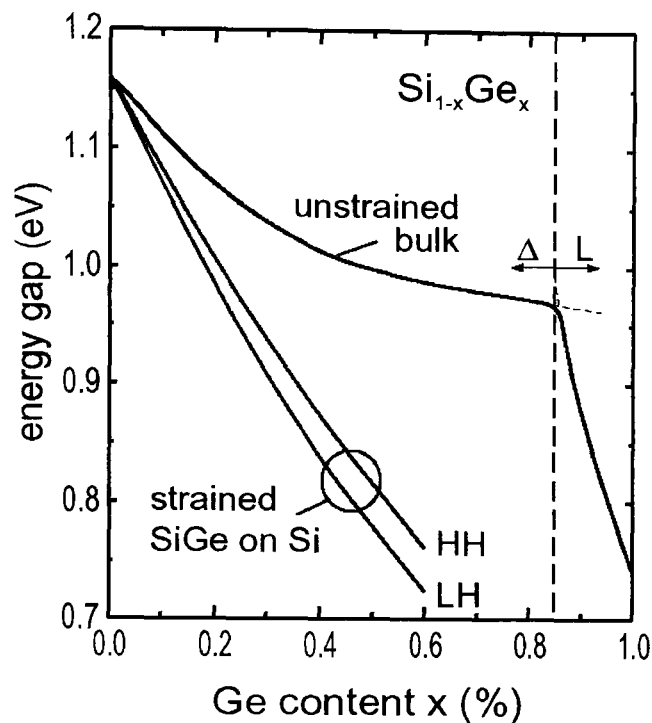
Figure 2.9.. SiGe energy gap variation as a function of Ge content.

It has been found that the strain in SiGe heterostructures has a much more pronounced effect on the valence bands near the Γ point leading to very interesting opportunities in band engineering. If we consider the cubic unstrained system, we find that the resulting bands are degenerate as in figure 2.10a. By introducing strain (compressive), as in the case for SiGe/Ge on a Si/SiGe substrate, the symmetry of the layer becomes tetragonal (figure 2.7b). Tetragonal distortion will affect the electronic orbitals along the growth direction. In this situation, the band becomes anisotropic (figure 2.10b) and the motion in the plane of the junction will then be governed by the light mass leading to an improved mobility of the holes. Such improvement comes

about because of the carrier's mobility being inversely proportional to $\dfrac{1}{m^{*2}}$ (where m*

is the effective mass) in the case of a 2D system [O'Reilly, 1989]. For strained SiGe,

the spin orbit band is calculated to be significantly separated (>100 meV) from the

heavy- and light-hole bands and so can usually be ignored for most device applications

[Riger & Vogle, 1993].
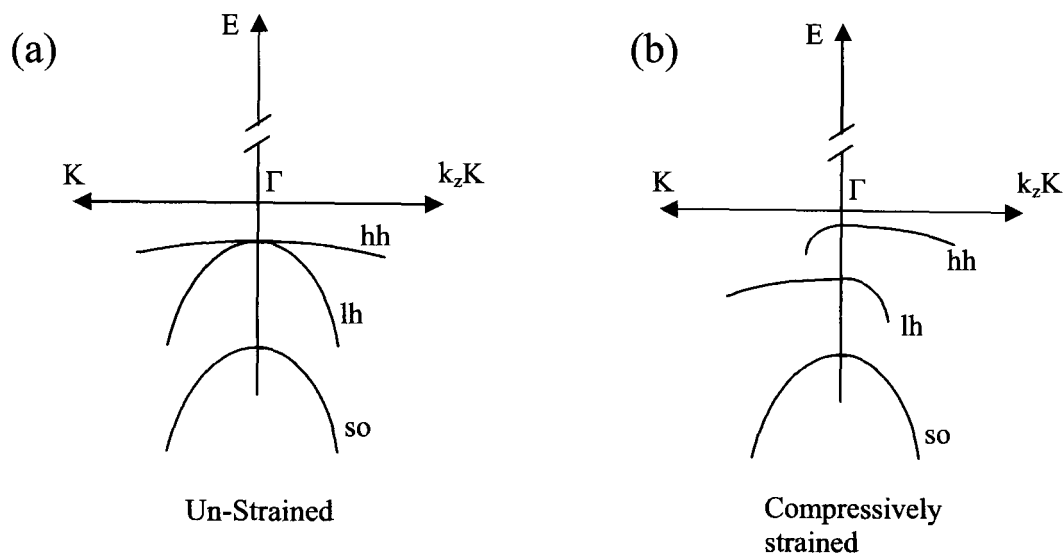
Figure 2.10. Schematic diagram depicting the heavy hole, light hole and spin orbit bands for un-stained (a) and compressively strained (b) SiGe.

2.3.6 Effective mass (m*)

Due to the fact that electrons in a semiconductor material interact with the

periodic potential of the lattice, their motion will not be that of the free electron case.

The simple derivation of the effective mass equation can be found in many introductory

Solid State textbooks. For this derivation and an explanation of the effective mass the

reader is referred to Blakemore [Blakemore, 1985]. In the case of semiconductors, (our

case Si and Ge), the effective mass plays a large part in the improvement of the

transport properties. The reason for this is that the conductivity mass is inversely

proportional to the mobility. It was previously mentioned that strain in the SiGe system

may lead to a lowering of the effective mass under the right conditions enhancing the transport properties of holes and electrons. The alloy composition also has an effect on the effective mass due to the band offsets obtained by merging two materials together as in the case of Si and Ge. Riger and Vogle [Riger & Vogle, 1993] have calculated the parallel and perpendicular conductivity masses associated with the lowest conduction band minima for all degrees of alloying and strain. According to their results, the smallest effective mass occurs for a Ge like gap indicating that, to obtain the lowest possible effective mass we would have to grow a pure, compressively strained, Ge layer on a SiGe buffer layer. Recent results have shown the effective mass measured for a strained Ge modulation doped structure to vary between $0.087-0.19m_o$ (where m_o is the free electron mass) for a carrier density range $0.5-2.5\times10^{12}$ cm^{-2}. Such effective mass values are much smaller than the unstrained bulk Ge heavy hole mass value of $0.28m_o$ [Irisawa et al, 2003].

2.3.7 Modulation doping

An obvious way of introducing carriers into classical device structures would be to dope the regions where electrons and holes were required. However it has been found that this leads to some undesirable degradation in the materials transport properties if this were the case. The main problem with this idea is that charge donors/acceptors are left behind when the electrons/holes are released, leading to scattering of the carriers through their Coulomb interaction which is referred to, and better known as 'impurity scattering'. A way around this problem which was first developed in the SiGe system by People et al [People et al, 1984] is known as 'remote' or 'modulation' doping. This technique incorporates the idea of placing the doping

region either beneath (referred to as inverted doping) or above (referred to as normal doping) the heterostructure's active channel region where the carriers are to be injected. It is also normal to find a thin layer between the active channel and the doping regions, referred to as the *'set back'* or *'spacer layer'*. People *et al* [People *et al*, 1984] first employed this technique on a pseudomorphic SiGe quantum well clad between the Si substrate and unstrained Si cap layer. By selectively doping the Si cladding layer a mobility enhancement was obtained, which is consistent with the formation of a 2DHG in the SiGe system.

Modulation doping leads to some significant benefits. It separates the carriers from their donor sites leading to a reduction of scattering by ionised impurities as well as allowing the carriers to be confined to two dimensions. By varying the size of setback layer the carrier concentration in the active channel of the structure can be modulated. The size of the setback layer will also have an effect on the amount of ionised impurity scattering. The larger the setback the less the scattering, but there is a trade off between the number of carriers required and the amount of ionised impurity scattering that can be tolerated. People, Bean and Lang [People, Bean and Lang, 1985] performed some preliminary studies on the modulation doping of pseudomorphic SiGe heterostructures. Their results clearly showed a balance between carrier density and mobility for various setback layer thicknesses. The ultimate objective from a device point of view is to obtain as high a carrier concentration for the largest mobility as is physically possible from the material available.

In practice it is often found that not all of the carriers are transferred from the doping supply layer to the channel. Furthermore, ionised impurities such as surface and growth interrupt contamination layers may be present within the structure. When mobility and carrier density measurements are made on modulation doped

heterostructures using a standard van der Pauw arrangement (see section §3.6.3), such ionised impurity layers and the doping supply layer may well lead to parallel conducting channels. Such parallel conduction will contribute towards the mobility and carrier density values obtained for measurements made at temperatures typically above 150 K [Xie *et al*, 1993]. For lower temperatures (≤70 K), the ionised impurities will be confined to their donor atoms eliminating their overall contribution to the measured mobility and carrier density. This low temperature process of ionised impurities being confined to their donor atoms is referred to as '*carrier freeze out*'. The measured low temperature mobility and carrier density will therefore be the carriers confined within the channel [People *et al*, 1984].

2.3.8 The SiGe heterostructure quantum well

In the case of a SiGe or Ge modulation doped heterostructure the valence band structure takes on the form of a triangular quantum well as depicted schematically in figure 2.11.

$$\chi(Z) = \left(\frac{b^3}{2}\right)^{\frac{1}{2}} z.\exp^{-\frac{1}{2}bz}$$
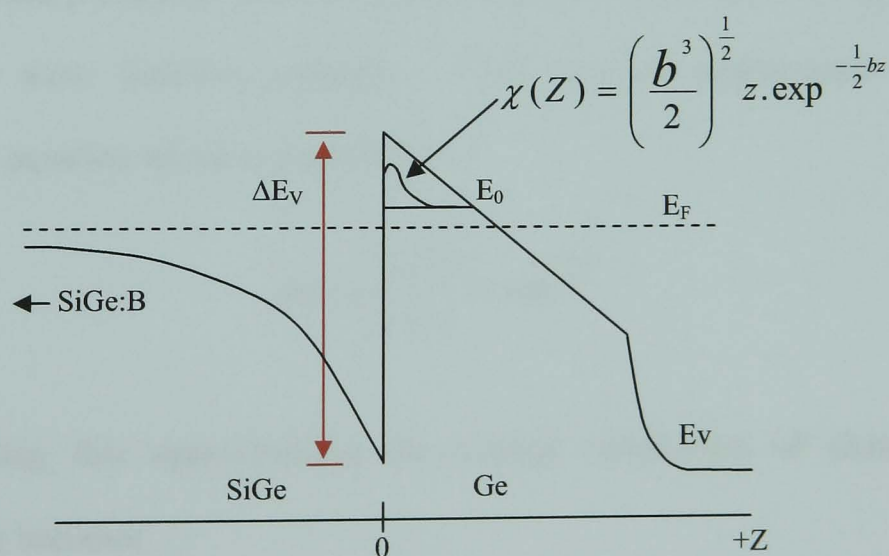
Figure 2.11. Valence band diagram showing the triangular potential well formed in a modulation doped SiGe:B/SiGe/Ge/SiGe heterostructure.

The reason for this triangular shaped well is due to the holes being transferred from the doping layer to the active channel region causing the valence band to bend. As the holes move from the doping region to the channel an electric field is formed creating a space charge region. For a triangular well as depicted in figure 2.9 the electrostatic potential $\varphi(z)$ is linear for $z>0$ and is given by:

$$\varphi(z) = -Fz$$

(2. 7)

but is infinite for $z=0$. F in the above equation is the electric field.

This is a quantum mechanical problem that satisfies the Schrödinger equation

$$\left[\frac{-\hbar^2}{2m^*} \frac{d^2}{dz^2} - e\varphi(z) \right] \chi_n(z) = E_n \chi_n(z)$$

(2. 8)

where

$$E_n = E - \frac{\hbar^2 K_\parallel^2}{2m^*}$$

(2. 9)

A method of numerical self consistent solution can be used to solve this quantum mechanical problem but is very cumbersome [Ando, Fowler and Stern, 1982]. Fang and Howard [Fang and Howard, 1966] derived a much simpler technique by using an analytical wave function approach. They used an approximate solution to Schrödinger's equation which is given below:

$$\chi(z) = \left(\frac{b^3}{2} \right)^{\frac{1}{2}} z.\exp^{-\frac{1}{2}bz}$$

(2. 10)

By using this approximation the average penetration of charge into the semiconductor becomes

$$Z_0 = \frac{b}{3}$$

<div align="right">(2. 11)</div>

Where "b" is the variational parameter. The variational parameter is obtained by minimizing the total energy of the system for given values of the inversion- and depletion-layer charge. The variational parameter is given by Emeleus *et al* [Emeleus *et al*, 1993] as:

$$b = \left[\frac{12 m^* e^2}{\hbar \varepsilon_0 \varepsilon_r} \left(N_{depl} + \frac{11}{32} n_s \right) \right]^{\frac{1}{3}}$$

<div align="right">(2. 12)</div>

The Poisson and Schrödinger equations form the basis for the 1D Poisson/Schrödinger package [Snieder] used for modelling the bandstucture, carrier confinement and wave function of the structures used in this work. However, the 1D Poisson/Schrödinger package works on a single band approximation and would not normally be very appropriate for valence band calculations where degeneracy exists. However, as previously mentioned in section §2.3.5, strain leads to the splitting of the heavy- and light-hole (HH and LH) valence bands along with the degeneracy. Under compressive strain and for doping levels used in this work the holes in a strained Ge structure will be confined to the HH bands (typically HH_1 only) [O'Reilly, 1989]. In this case the structure can be thought of as a one band system and so the 1D Poisson/Schrödinger package can be used for modelling of such structures.

3. Experimental Techniques

In this chapter the experimental techniques and equipment used for the work described in this thesis will be discussed. Initially, the solid-source MBE growth system used for generating the SiGe/Ge heterostructures will be considered before reviewing the methods applied to analyse the structural and electrical properties of the grown heterostructures. Both destructive and non-destructive techniques have been used in order to quantify parameters such as composition, relaxation and material quality. These techniques include high resolution X-ray diffraction (HRXRD), Secondary Ion Mass Spectrometry (SIMS), Transmission Electron Microscopy (TEM), and Atomic force microscopy (AFM). The methods used to determine the heterostructures electrical properties, will also be discussed. This includes resistivity and Hall measurements that have been carried out for temperatures in the range of 10 K up to room temperature. Such measurements are used to determine the hole mobility and sheet carrier densities.

3.1 Solid-Source MBE growth

Molecular-beam epitaxy is a highly complex process that has been developed and refined over many years to produce highly planar, good crystalline and impurity free, (except where required), semiconductor material. It may be described in brief as a process involving the reaction of one or more thermally produced beams of atoms and molecules that impinge onto a crystalline surface under Ultra-High Vacuum (UHV) conditions ($\sim 10^{-10}$ Torr). It is not the author's intention to go into the growth kinetics and other related growth aspects in detail here since section §2.1 gave an introduction

into the main growth modes for the SiGe system. The aim here is to outline the MBE equipment used to produce the heterostructures for this work.

3.1.1 The VG V90s SS-MBE system

The Vacuum Generators (VG) V90s solid-source molecular-beam epitaxy system was used to grow the semiconductor heterostructures investigated in this work. Figure 3.1 shows a descriptive schematic of the VGV90S system.
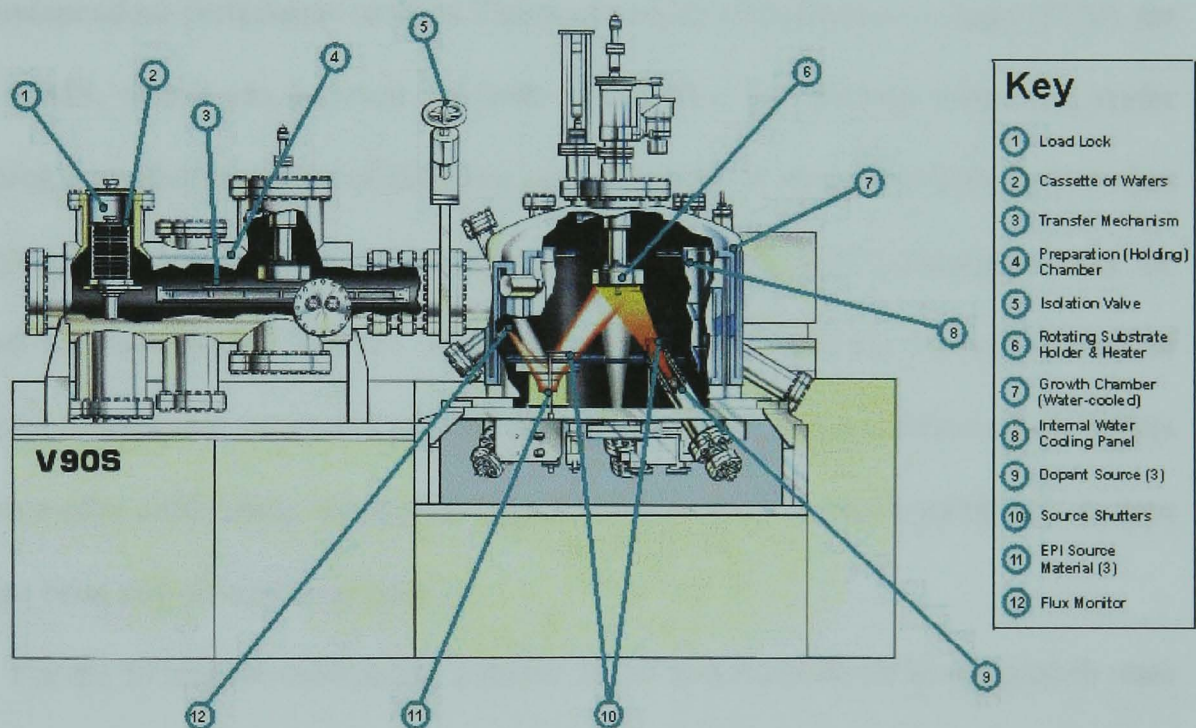
Figure 3.1. Schematic picture of the VG V90S Solid-Source Molecular Beam Epitaxy (SS-MBE) system.

The V90s system is designed for controlled deposition of epitaxial Si and Ge in any ratio, usually defined as $Si_{1-x}Ge_x$ for ($0<x<1$), plus the dopant sources boron (B) and antimony (Sb) being employed in the Warwick system. This process is performed under UHV conditions so as to minimise the incorporation of impurities from the

residual gases that would arise from the interaction with the Si and Ge fluxes prior to deposition. The Si and Ge are deposited from electron-beam (e-beam) evaporators whilst the dopants are produced from Knudsen type effusion cells. The Si and Ge deposition is controlled via flux monitors that measure the amount of material being produced. This information is then fed back into a computer that controls the power applied to each source. By varying the power to each source the amount of flux from each source can be varied to give the required amount of Si or Ge. In the case of the dopants, calibration wafers are grown at the beginning of a series using different but monitored powers and temperatures. These structures are then analysed and quantified using independent techniques such as Electrochemical Capacitance-Voltage (ECV) for B and SIMS, which can be used for both B and Sb. By growing either one wafer containing a number of layers of different concentrations or numerous individual wafers of varying concentrations a calibration curve for power and temperature may be obtained for each dopant source. Using this calibration curve the correct amount of dopant for subsequent structures may be deposited. In the scenario where many wafers are grown after calibration, the dopant sources may be re-calibrated periodically in case there has been any change over time.

For the Si and Ge calibration, a series of test structures for believed growth rates are produced, usually in the form of a periodic Si/SiGe/Si superlattice. From such a structure, the SiGe concentration, along with the thickness of the layers may be determined using X-ray diffraction (see section §3.2). From this information and the intended flux rates, the true flux rates of the Si and Ge sources may be found.

3.1.2 Substrate preparation

The importance of cleaning the starting substrate, be it a standard Si substrate or a SiGe Virtual Substrate (VS) cannot be overestimated. The critical role of cleaning substrate surfaces for the growth of semiconductor material, and the fabrication of semiconductor microelectronic devices, has been recognised since the beginning of solid state technology. As understanding of the fundamentals has progressed, different cleaning procedures have been developed in order to keep up with today's modern semiconductor material and their combinations. The objective behind wafer cleaning is to remove unwanted particulates and chemical impurities without causing any damage to the actual wafer surface. There are many different cleaning processes including dry-and wet-chemical cleans, as well as vapour-phase methods. In the work of this thesis, wet-chemical cleans combined with high temperature *in-situ* (flux or desorb) cleans were used and will be outlined below.

Given that some of the structures were grown on n-doped (001) silicon substrates, while others on SiGe VS's, different chemical cleans were used in order to achieve a good quality re-growth interface. For the n-doped (001) silicon substrates used as the starting substrate, a clean based on Hydrogen Peroxide mixtures was used. Such a cleaning process employs two steps, known as RCA standard cleans (SC-1 and SC-2). As well as the chemical stages of the clean a combination of de-ionised water rinses and dilute HF dips are performed. Below is the actual cleaning procedure used:

Step I

- 20 second 2% HF dip

- 3 stage de-ionised (DI) water cascade rinse

- 20 minute boil at 80°C in DI:NH$_4$OH:H$_2$O$_2$ in the ratio (5:1:1)

- 3 stage DI water cascade rinse

Step II

- 20 second 2% HF dip

- 3 stage DI water cascade rinse

- 20 minute boil at 80°C in DI:HCl:H$_2$O$_2$ in the ratio (6:1:1)

- 20 second 2% HF dip and then spun dry at ~100 rpm for 1 minute.

Following the spin dry, the wafer is then loaded into VG V90. Step I of the clean removes organic surface films that may be present as well as exposing the surface for desorption of trace metals such as Au, Ag, Cu, Ni, etc. Step II dissolves alkali ions and hydroxides of Al^{+3}, Fe^{+3}, Mg^{+2}.

For the SiGe VS's, the standard Si substrate chemical clean was found to be far too aggressive, leading to surface damage and problems with the re-growth. Therefore, a different chemical clean was required. The clean was based on the Piranha etch and was found to yield good results. Below is the Piranha etch used for the SiGe VS's:

- 3 minute Piranha clean (H$_2$SO$_4$:H$_2$O$_2$) in the ratio (3:1) at the self heated temperature of ~130°C

- 1 minute dip in 2%HF solution and spun dry at ~100 rpm for 1 minute

- Loaded into the VG V90.

The chemicals used for all the cleaning procedures mentioned above were of the Merck Selectipure VLSI grade widely used in the semiconductor industry. By not using

chemicals of such a high standard of chemical purity, the advantages of cleaning the wafer prior to growth may be lost but in more severe cases unwanted contaminants from poor quality chemicals may be added.

All the substrates cleaned underwent a final dilute HF dip. This is known to terminate the surface with hydrogen.

There are two in-situ high temperature cleans employed by the growers for cleaning the substrate prior to growth. These are a flux clean and a desorb. In the case of the flux clean, a very thin layer of Si (~0.5 nm) is deposited which transforms itself into SiO given the substrate is held at a high temperature of 900°C. Once SiO is formed it is then driven off by having the substrate temperature at 900°C. This process is repeats itself many times before growth starts. In the case of the desorb, the wafer temperature is raised above 840°C and left for 30 minutes to allow any residuals on the wafer surface to be forced off.

3.2 X-ray

High Resolution X-ray Diffraction (HRXRD) is a very common non-destructive technique when analysing semiconductor material parameters. By using this technique the composition and strain/relaxation may be determined as well as the thickness of strained layers from their thickness fringes. For the work described in this thesis, HRXRD was used to measure the relaxation and composition of the SiGe virtual substrates (VS), as well as for calibrating the growth system from SiGe superlattice structures grown just prior to the desired structure.

3.2.1 **Philips high resolution diffractometer**.

The X-ray diffractometer used in this work was a High Resolution Philips system. Figures 3.2a & b show a schematic layout and the plan view of the Philips X-ray system. The system can be broken down into four main parts:

- Goniometer or base unit

- Incident beam optics

- Sample holder or stage

- Diffracted beam optics

The goniometer is mounted on the base plate along with the omega and 2theta co-axial drives. The incident beam optics consists of a $CuK_{\alpha 1}$ X-ray tube source which has a wavelength of 0.154 nm. This is a very useful operational source wavelength, as there are many materials with an inter-planar spacing that diffract X-rays at this wavelength. The $CuK_{\alpha 1}$ source also possesses a very high intensity which will increase the observed signal from the diffracted crystal sample. The tube was typically operated at 40 kV and 30 mA.

The incident beam optics consist of a 4-crystals Bartels monochromator (Ge 220), which is used to control the analytical divergence of the wavelength spread in the incident beam. Both the source and incident beam optics are mounted rigidly on the base plate in order to keep the beam horizontal, therefore intercepting the vertical diffractometer axis.
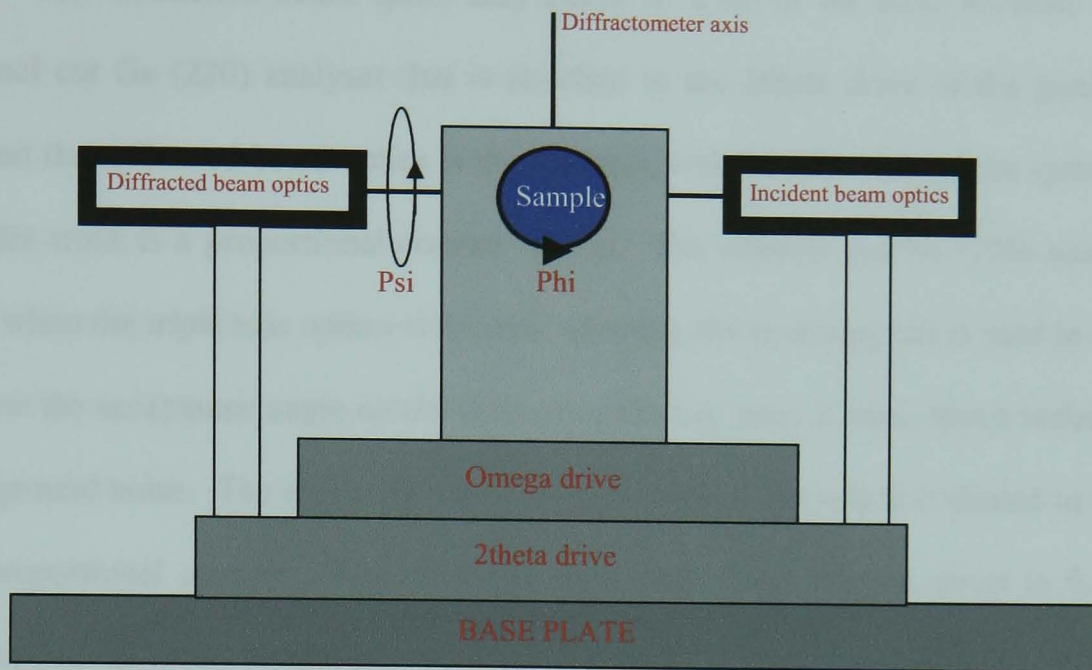
(a)
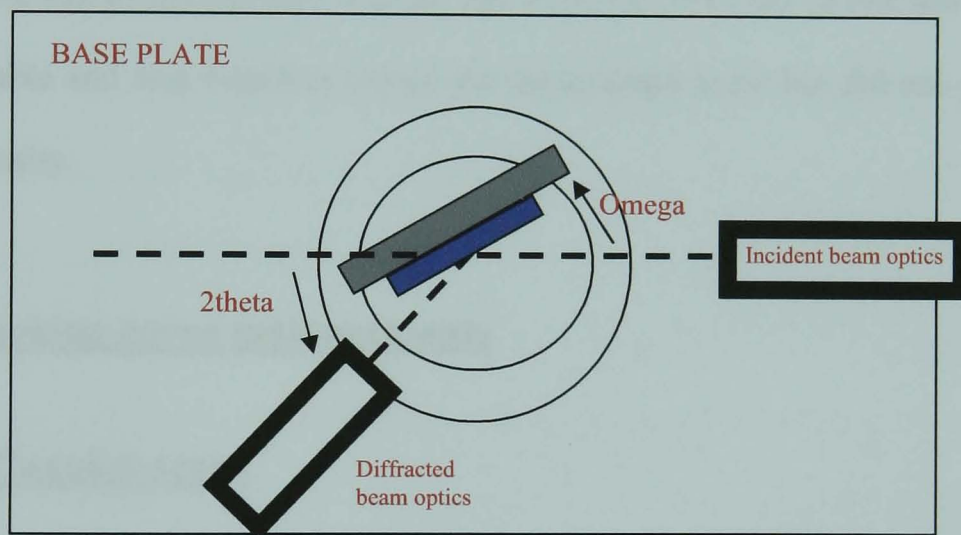
(b)

Figure 3.2. (a) Shows a schematic diagram of the Philips High Resolution X-Ray Diffractometer (HRXRD) used for this work, while 3.2b shows it in plan view.

The sample stage is enabled to move in the z-direction so that the sample surface can be made to coincide with the diffractometer axis. It may also move in the horizontal direction, referred to as the 'Psi' direction, so that the reflecting sample planes can be set vertically to the incident beam, while a rotation of the sample stage called 'Phi', allows the chosen direction in the horizontal plane.

The diffraction beam optics may either be a slit or for more accurate work, a channel cut Ge (220) analyser that is attached to the 2theta drive of the goniometer. Behind the diffracted beam optics is the detector, which in the case of the system used for this work is a proportional counter device. The channel cut Ge (220) analyser is used when the triple axis option is desired, whereas, the receiving slit is used in order to narrow the acceptance angle on the detector, reducing stray X-rays, hence reducing the background noise. The receiving slit is a single vertical slit which is placed in front of the proportional counter. Typical width sizes range from 1.8 mm down to 0.45 mm, corresponding to an acceptance angle of 0.8 to 0.2 degrees respectively. Without a receiving slit in front the proportional counter, the opening to the detector would be 6 mm. The size of slit typically used for this work was 0.45 mm as this was the smallest slit available and was found to reduce the background noise but did not suppress the peak intensity.

3.2.2 Rocking curve measurements

3.2.2.1 Coupled scans

Rocking curve measurements involve making a single scan which collects all the available intensity from the reciprocal lattice points. With the equipment and software available there are two coupled scans possible. These are when the two axis parameters are varied simultaneously and are referred to as either an:

- Omega/2Theta scan

or

- 2Theta/Omega scan

In both cases the 2Theta axis is rotated at twice that of the Omega rotation. The difference between the two scans is the way in which data is recorded. In the case of the Omega/2Theta scan the data is in the form of intensity as a function of Omega. The 2Theta/Omega produces data in the form of intensity as a function of 2Theta. In the case of the measurements performed in this work, Omega/2Theta scans were used, giving intensity as a function of the lattice "d" value for a fixed orientation of lattice planes.

3.2.3 Kinematical and Dynamical theories for X-ray diffraction

There are two basic theories for X-ray diffraction, namely, kinematical and dynamical. The kinematical theory is the simpler of the two and makes the assumption that there is a negligible amount of energy transferred to the diffracted beam. By making this assumption, rediffraction effects are ignored. Such a theory is reasonably accurate for the geometry of diffraction in all cases and when scattering is very weak, as is the case for very thin crystals where surface and diffuse scattering is being observed. However, when scattering is strong, which is typically the case for the majority of semiconductors, this assumption becomes invalid. By using the dynamical theory a more accurate result is obtained. In this case the diffracted beam from a set of reflecting planes are considered to be at the right angle to be rediffracted by the same planes, and so their energy is spread over a triangular region within the sample. This type of rediffraction process is referred to as the 'Borrmann fan' and is shown schematically in figure 3.3. Such a process leads to a very complicated expression in intensity as will be shown in §3.2.4. The dynamical theory has been found to be very accurate for

determining X-ray rocking curves, but given the complicated expressions required to model the rocking curves, commercial simulation packages based on these equations have been developed.
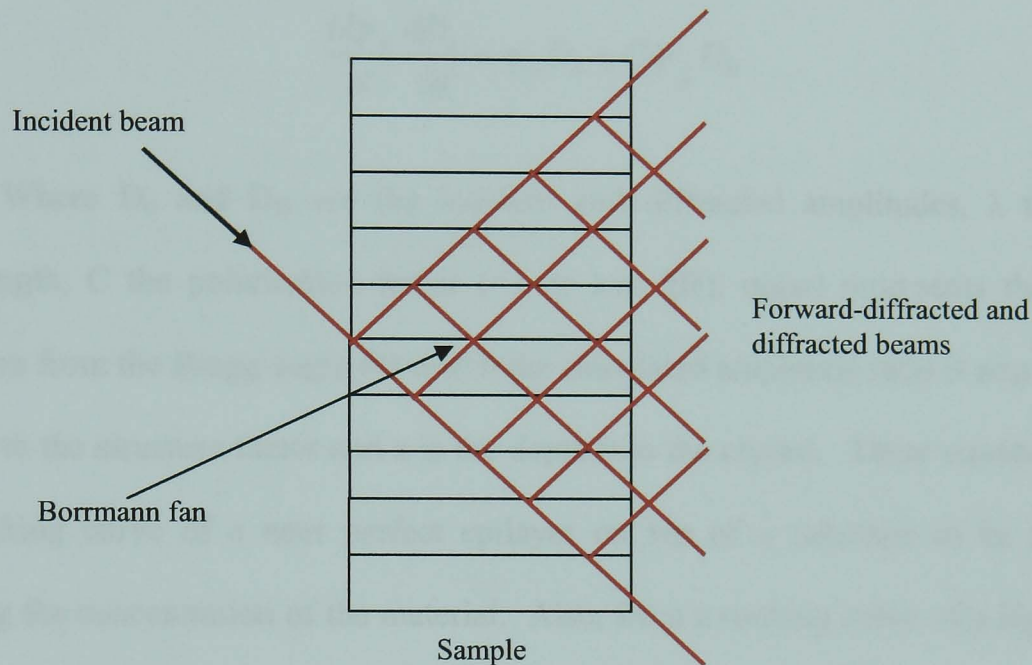
Figure 3.3. Schematic diagram showing the diffraction and rediffraction of an X-ray beam from a set of reflecting planes which is referred to as the Borrmann fan

3.2.4 <u>Determination of alloy layer concentration and thickness</u>

In the case of an alloy layer deposited upon a substrate leading to a simple cubic structure, the thin alloy layer concentrations can be determined from a simple symmetric (004) Omega/2Theta scan. Once the rocking curve has been measured there are a number of simulation packages available which make use of the dynamical theory. The most appropriate theory which is applicable for modelling the diffraction from perfect substrates, and substrates with epitaxial layers on top, is the theory proposed by S.Tagaki [Tagaki, 1962] and D.Taupin [Taupin, 1964] independently. The solution for

the Tagaki-Taupin equations is given by Fewster and Curling [Fewster and Curling, 1987], which take the form of two differential equations given as:

$$\frac{i\lambda\gamma_H}{\pi}\frac{dD_H}{dz} = \psi_o D_H + C\psi_H - \alpha_H(\omega)D_H$$

(3. 1)

$$\frac{i\lambda\gamma_o}{\pi}\frac{dD_o}{dz} = \psi_o D_o + C\psi_{-H} D_H$$

(3. 2)

Where D_o and D_H are the incident and diffracted amplitudes, λ the X-ray wavelength, C the polarisation factor (=1 or $|\cos 2\theta|$), $\alpha_H(\omega)$ represents the angular deviation from the Bragg angle for which the calculated amplitude ratio is required, ψ is related to the structure factor and z is the depth into the crystal. These equations allow the rocking curve of a near perfect epilayer on top of a substrate to be simulated yielding the concentration of the material. Also, from a rocking curve of a high quality strained epilayer on a substrate there will be small periodic oscillations around the main layer peak. These are known as 'thickness fringes' and are a very good way of determining the individual layer thicknesses.

3.2.5 Vergard's law

In the case of alloys it is common for both the lattice parameter and Poisson ratio to be approximated by a linear interpolation between the end points of the alloy system. This assumption is known as "Vergard's law". People [People, 1985] suggested that the Poisson ratio for the SiGe alloy system varies between 0.273 for Ge to 0.280 for Si. For SiGe, the real lattice parameter deviates from Vergard's law by ~2%. Dismukes et al[Dismukes et al, 1964] found that a quadratic form of variation

produced the most acceptable result for the variation in SiGe lattice parameter, from which Halliwell [Fewster, 1993] has fitted to this curve the following expression:

$$a_{Si_{1-x}Ge_x} = xa_{Ge} + (1-x)a_{Si} - 0.00436x^3 + 0.03265x^2 - 0.02829x$$

(3. 3)

where 'a' is the lattice parameter (Å) and 'x' the mole fraction.

Figure 3.4 shows a plot of Vergard's law and the above function correcting for Vergard's law. From this plot it can be seen that the lattice constant is found to be slightly less than Vergard's law throughout much of the SiGe alloy. The corrected form is the curve used for the work of this thesis once the lattice parameter was determined.
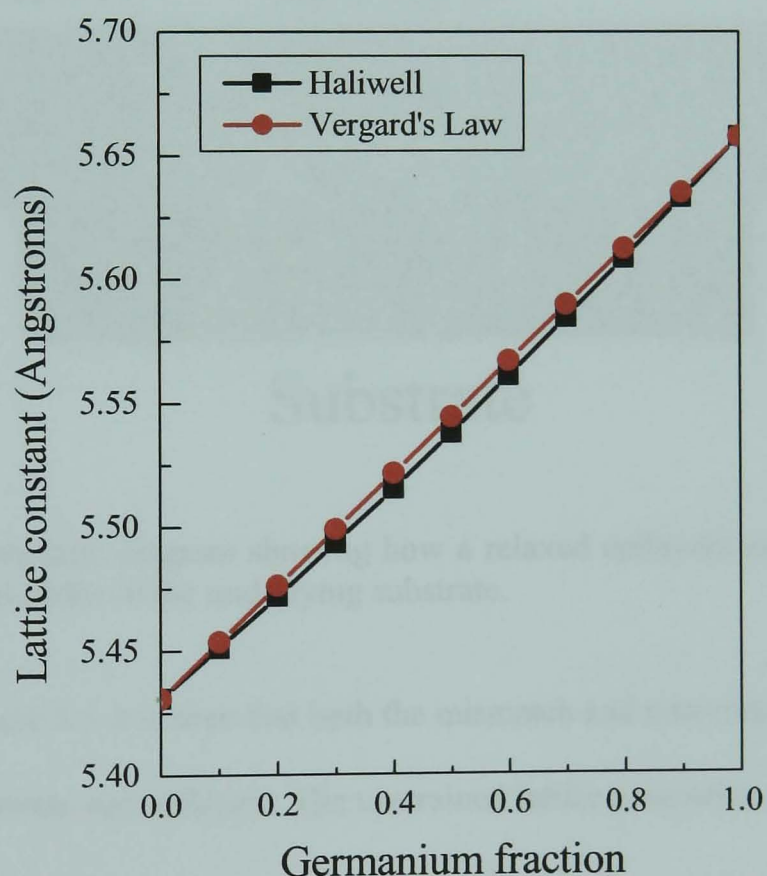
Figure 3.4. Plot of Vergard's law and Haliwell's expression (equation 3.3) showing the change in SiGe lattice constant for varying Ge fraction.

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3.2.6 Relaxation measurements

As has been already discussed in section §2.3.3, when a thin layer SiGe layer is deposited onto Si, tetragonal distortion is found to occur. Once the amount of SiGe material deposited on top of the Si exceeds the critical thickness (§2.1.3), the material will relax by misfit dislocations, forming a coherent relaxed layer as shown in Figure 3.5.
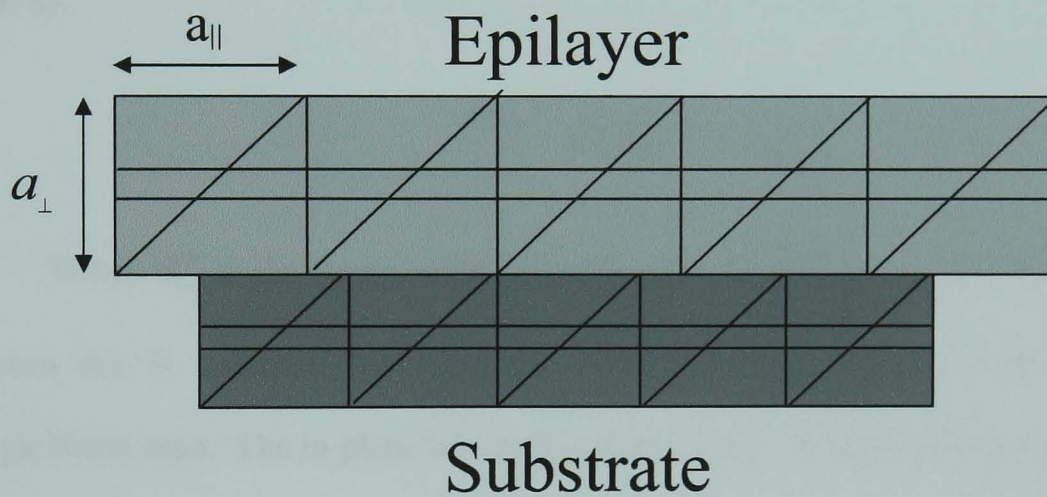
Figure 3.5. Schematic diagram showing how a relaxed epilayers in- and out-of-plane lattice parameters differ to the underlying substrate.

From figure 3.5 it is seen that both the mismatch and misorientation are different between the substrate and epilayer. The unstrained lattice parameter of the layer (a_{SiGe}) is related to the in-plane lattice parameter $(a_{SiGe}^{\perp})$ and perpendicular lattice parameter $(a_{SiGe}^{\parallel})$ through the relation:

$$a_{SiGe} = \left[\frac{(1-\upsilon)}{(1+\upsilon)}\right]a_{SiGe}^{\perp} + \left[\frac{2\upsilon}{(1+\upsilon)}\right]a_{SiGe}^{\parallel}$$

(3. 4)

Where υ is Poisson's ratio.

In order to determine the fraction of germanium present, and amount of relaxation of the layer, the in-plane $\left(a_{SiGe}^{\perp}\right)$ and out-of-plane $\left(a_{SiGe}^{\parallel}\right)$ lattice parameters must be determined. In order to calculate the in-plane and out-of-plane lattice parameters, a minimum of two symmetric and two asymmetric omega/2Theta scans have to be performed at grazing incidence (g.i) and grazing exit (g.e) geometry. For this work the symmetric scans used were in the (004) direction, while the asymmetric scans consisted of a grazing incidence (115) directional scan and a grazing exit $(\bar{1}\bar{1}5)$ directional scan. The perpendicular lattice parameter is derived from Bragg's law and is given by:

$$a_{SiGe}^{\perp} = \frac{2\lambda}{\sin\left(\theta_{004}^{Si} + \Delta\omega_{004}\right)}$$

(3. 5)

Where θ_{004}^{Si} is the Bragg angle for the Si substrate and $\Delta\omega_{004}$ the angular spacing between the Si substrate peak and the constant Ge layer peak of the symmetric omega/2theta scan. The in-plane lattice parameter is more complicated and is given by:

$$a_{SiGe}^{\parallel} = \frac{\sqrt{2}\lambda}{\sqrt{4\left(a_{SiGe}^{\perp}\right)^2 \sin^2\left(\theta_{115}^{Si} + \Delta\omega_{115} - 25\lambda^2\right)}} a_{SiGe}^{\perp}$$

(3. 6)

Where θ_{115}^{Si} is the (115) Bragg angle of the Si substrate and $\Delta\omega_{115}$ the mean angular separation between the Si and Ge peaks for grazing incident (g.i.) and grazing exit (g.e.) geometry and is given by:

$$\Delta\omega_{115} = \frac{1}{2}\left(\Delta\omega_{115}(g.i.) + \Delta\omega_{115}(g.e.)\right)$$

(3. 7)

By using the mean value of peak separation, any tilt between the (115) planes of the epilayer and substrate is compensated. A full derivation for deriving the in-plane lattice parameter is given by Hartmann *et al* [Hartmann *et al*, 2000].

Once the in-plane and out-of-plane lattice parameters have been determined, the final Ge concentration can be found from Vergard's law to a good approximation, or more accurately from Haliwell's corrected version of Vergard's law as given in equation 3.3. From the determined lattice parameters the amount of relaxation may then be determined from the relation:

$$R = \left(\frac{a^{\parallel}_{SiGe} - a_{Si}}{a_{SiGe} - a_{Si}} \right) \times 100$$

(3. 8)

Where a_{Si} the substrate lattice parameter, and a_{SiGe} the fully relaxed lattice parameter (cubic) of the epilayer.

3.3 Secondary Ion Mass Spectrometry (SIMS)

Secondary Ion Mass Spectrometry is a destructive technique, whereby the sample investigated undergoes bombardment from a mono-energetic beam of primary ions that are typically within the energy range of 100 eV to 30 keV. As a result, sputtering of particles from the sample surface occurs. A small fraction of these sputtered particles is ionised, and it is these ions, known as secondary ions, which are measured and used to build up a depth profile of the sample.

There are two main types of SIMS technique, namely static- and dynamic-SIMS, with the latter being the technique used for this work. In the case of static SIMS, the primary ion dose is typically kept below 5×10^{12} ions/cm^2 and so the analysis is confined

to the first few monolayers. For optimum conditions as little as 0.1 % of a monolayer can be detected and is commonly used as a qualitative method for finding the molecular composition (ppm) at the samples surface. In the case of dynamic SIMS, the minimum dose for the primary beam is of the order of 10^{17} ions/cm^2. Under these conditions, material is more readily removed and by rastering the primary beam, depth profiling can be achieved as each successive layer of atoms removed is analysed.

3.3.1 Dynamic SIMS

Dynamic SIMS is one of the most powerful and frequently applied techniques for the chemical analysis of semiconductors and related materials. With dynamic SIMS, an area of the sample surface is eroded by sputtering with a scanned mono-energetic beam. Many different species may be used for the primary beam, but the two commonly used and most understood are oxygen (O_2^+) and caesium (Cs^+). Reactive species such as these are used in order to enhance the ionisation probability of secondary ions. Both do produce positive and negative ions, but in the case of caesium an enhancement in negative ions is achieved, while for oxygen, positive ions are enhanced. The use of these two primary ions can result in a secondary ion yield enhancement greater than 5 orders of magnitude. Under such conditions a number of the sputtered atoms or molecular clusters are ionised directly, with a significant fraction of these being collected by an electrostatic field and transported into a double focusing magnetic sector (DFMS) or quadrapole mass spectrometer (QMS).

For dynamic SIMS, the object is to establish steady-state conditions of erosion rate while retaining a constant primary ion dose within the receding near-surface region of the material. When such steady-state conditions are achieved, high precision depth

profiling can be performed. For a primary ion dose above the static SIMS region but below the dynamic SIMS regime, conditions typical for the initial part of a dynamic SIMS profile, a pre-equilibrium region exists. In this case the surface chemistry, erosion rate and ion yield will vary drastically and this may persist for several nanometers.

3.3.2 The Atomika 4500 SIMS Tool

The instrument used for all the SIMS measurements performed for this work was an Atomika 4500 and is schematically depicted in figure 3.6. As can be seen from figure 3.6, the system consists of four principal parts, namely the main analysis chamber, two floating low energy ion guns (FLIG™) [Dowsett et al, 1997], one being oxygen and the other caesium and a load lock separated from the main chamber by a pneumatic gate valve. The two floating low energy ion guns are mounted at 90° with respect to each other with each gun capable of producing a mono-energetic primary in beam within the energy range 150 eV – 5 keV. The load lock is pumped down to high vacuum ($\sim10^{-6}$-10^{-7} mbar) while the main analysis chamber is kept under UHV ($\sim10^{-9}$-10^{-10} mbar) conditions.

The ion beam from the FLIG is strongly focused so as to allow analysis of an area as small as $\sim$50 μm in diameter. Both of the primary ion beams are mass analysed in order to achieve beam purity and the primary gun optics also includes a 2° beam bend in order to suppress any neutrals. This neutral ion suppression is the key to obtaining high dynamic range analysis. The two guns are separated from the main chamber by pneumatic valves, enabling both guns to run continuously so allowing rapid switching from one beam to the other.
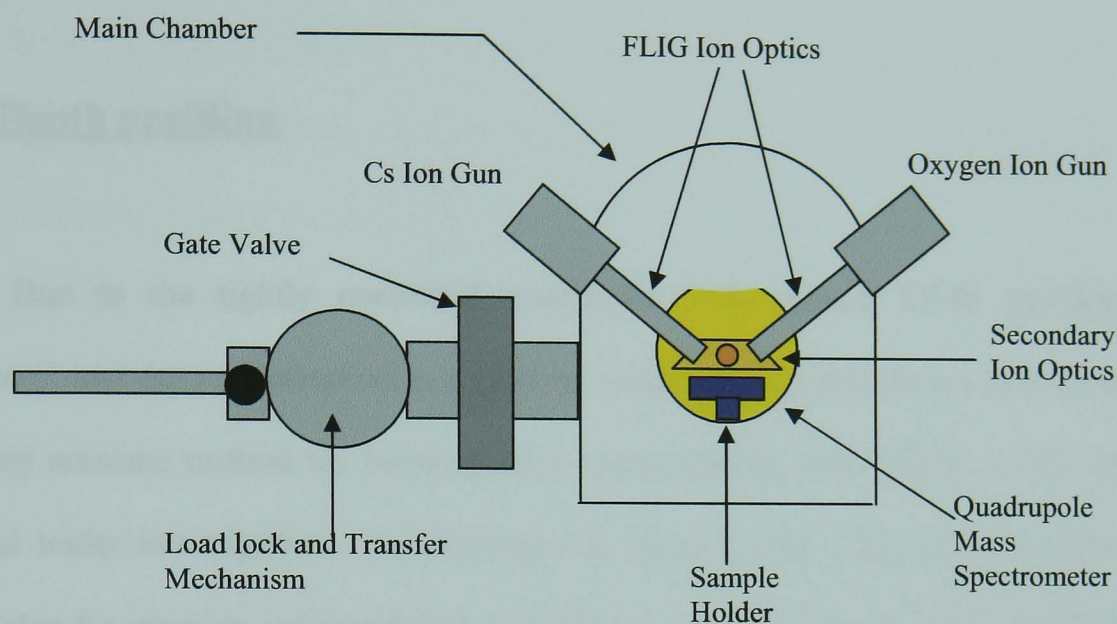
Figure 3.6. Schematic diagram showing the instrumental layout of the Atomika 4500.

The samples are mounted onto a sample holder by a spring clip from behind. Four, six and thirteen hole holders are available so several samples plus reference materials can be loaded and profiled sequentially. By being able to profile samples continuously, better continuity between measurements is observed and the subsequent analysis becomes more accurate. Once the samples are mounted, they are usually wiped clean with lint free cloth, damped with propan-2–ol, before being blown dry with dry N_2. They are then loaded into the load-lock and pumped down to high vacuum (HV). Once under HV, the samples are transferred into the main analysis chamber (UHV) where the holder mounts onto a eucentric sample manipulator. This manipulator allows the angle between the primary beam and the sample to be varied from normal to grazing incidence, allowing a wider range of profiling conditions. The eucentricity of the manipulator also allows the samples angle of incidence to be varied without appreciable shift in ion beam position.

Finally, the secondary ion optics is of the acceleration-deceleration type and is designed for optimum secondary ion collection efficiency [Wittmaack, 1982].

3.3.3 Depth profiling

Due to the tightly controlled conditions under which SIMS profiling is performed, and the sophistication in equipment available for such measurements, SIMS is a very accurate method for building up a concentration versus depth profile of the material under investigation. As discussed in section §3.1, modern equipment and knowledge for growing semiconductor material is so well advanced, very homogenous material with sharp interfaces are readily produced. For typical depth profiles, the primary ion beam is rastered over an area which is typically in the range 150-300 μm^2, eroding a certain depth increment per scan, and producing a flat bottomed crater. The edges of the crater will not be perfectly vertical and so ions from the crater walls will be collected simultaneously with the ions from the crater bottom. Such ions lead to a smearing of the true profile. In order to exclude the crater edge ions, electronic gating is applied to select ions from the crater bottom only. During profiling, the variation in ion yield as a function of time is recorded and by suitable quantification procedures may be converted into a concentration profile as a function of depth which is more meaningful. In the case of the Atomika 4500, background detection limits of 10^{16} cm^{-3} for most dopant species are achievable under ultra low energy SIMS conditions, but this is dependent on the conditions being used and the material under investigation.

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3.3.4 <u>Depth resolution</u>

Depth resolution is a very important parameter in modern device structure analysis. It is a measure of the ability to distinguish between features at different depths and the ability to resolve one or more parameters from a profile of a sharp feature, such as an interface or multi-layer structure. Once equilibrium is achieved between the primary beam and surface, as discussed in section §3.3.1, the depth resolution should remain constant thereafter. However, there are other factors that will have an effect on the depth resolution. One important factor is the change in erosion rate between different materials such as Si and SiO_2, where SiO_2 is known to have an erosion rate of approximately twice that of Si. A change in erosion rate between two materials will lead to a distortion in the profile shape, and appear to show features in the profile at incorrect depths if not taken into account. In order to achieve the highest depth resolution possible it is important to start with an atomically flat surface and use a primary beam, (along with suitable conditions), that will not induce surface roughening. It should also be noted that the depth resolution limit cannot be better than the depth sputtered to obtain a single data point. Therefore the erosion and sampling rates need to be carefully matched to the sample being investigated at any one time. The Atomika 4500 has been designed to readily achieve sub-nanometer resolution for most good quality material profiled under optimum conditions.

3.3.5 <u>Depth quantification</u>

As mentioned in section §3.3.3, in order to obtain a quantitative depth profile, the collected ion yield as a function of time must be converted into concentration as a

function of depth. Assuming a constant erosion rate throughout the profiled sample, the depth for the present work was obtained by measuring the depth of the crater using a Sloan Dektak electro-mechanical profiler, an instrument specifically designed for such measurements. The way in which the Dektak operates is as follows. The sample containing the profile crater is mounted onto the Dektak sample plate and held in place by vacuum. A stylus is then lowered onto the sample surface at a force of about 20 mN. The plate upon which the sample is mounted is then traversed and its level adjusted mechanically so that the sample is as close to perpendicular with respect to the stylus as possible. The sample is again passed under the stylus, but this time the area of the sample passing under the stylus includes the crater needing to be measured. The mechanical profile is converted into an electrical signal and uploaded onto a computer where by means of a computer package the final levelling and subsequent depth of the crater can be determined. Once the depth is known it is then applied to the SIMS profile.

It has been previously mentioned that some samples do vary in erosion rate if they are composed of slightly different materials. In such cases it is more difficult to put a depth scale onto the actual profile. One region where erosion rate change cannot be accounted for is at the interface between two different materials.

3.3.6 Dopant quantification

A common method for dopant impurity quantification is by use of a known standard being measured under identical conditions to the unknown samples. For the most accurate determination, the reference material should in essence be as similar as possible to the unknown dopant in matrix stoichrometry and morphology. The most

common material used for reference is a wafer implanted with an accurately known dose of impurity. Firstly, the profile of the reference implant is depth calibrated as discussed in section §3.3.5. An absolute sensitivity factor (ASF) is then determined from this profile in the following way. From the implant's profile, the total number of impurity ions collected are summed together and then multiplied by the depth increment (Δz), which is the difference between two consecutive depth measurement points. This may be expressed as:

$$K_{\text{Re}f} = \Delta z \sum_{A}^{B} I_{\text{Re}f}$$

(3. 9)

To find the ASF of the reference we then divide the known dose of the reference material by K_{ref} as shown below.

$$ASF = \frac{Dose}{K_{\text{Re}f}}$$

(3. 10)

We then multiply the unknown sample's dopant ion yield by the calculated ASF to convert the ion yield of the particular dopant species into concentration. Each dopant species will need its own reference sample and hence ASF value determined separately.

3.4 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is recognised as a very powerful tool for investigating the structural properties of semiconductor materials. Its main benefit over most techniques is the ability to image the specimen directly. This enables defects and dislocation formation within the material to be observed as well as roughening effects which may have occurred. Cross sectional TEM (XTEM) and plan view TEM

was used in the studies for this thesis and a brief description of the microscope used and sample preparation techniques are discussed in the following sections.

3.4.1 The JEOL JEM2000FX Transmission Electron Microscope (TEM)

The electron microscope used for the work presented in this thesis was a JEOL JEM 2000FX. The transmission electron microscope primarily consists of an electron gun for illumination, a number of electromagnetic lenses in order to focus and manipulate the electron beam through the electron transparent specimen and onto a screen or other means of display for capturing the final image. Figure 3.7 shows a schematic diagram of the JOEL 2000FX TEM instrument. The main parts of the microscope and its different lenses within are outlined below.

Situated at the top of the instrument is the electron gun. This is commonly a thermionic source comprising of a filament heated to temperatures in excess of 2700 K. At such temperatures electrons are thermally emitted. These emitted electrons are collimated and accelerated through a selected potential difference within the range of 40-400 keV. The electron energy used is determined by the specimen under investigation. For the samples investigated in this work a typical energy of 200 keV was selected. The main advantages of higher energies are that it provides higher resolution.
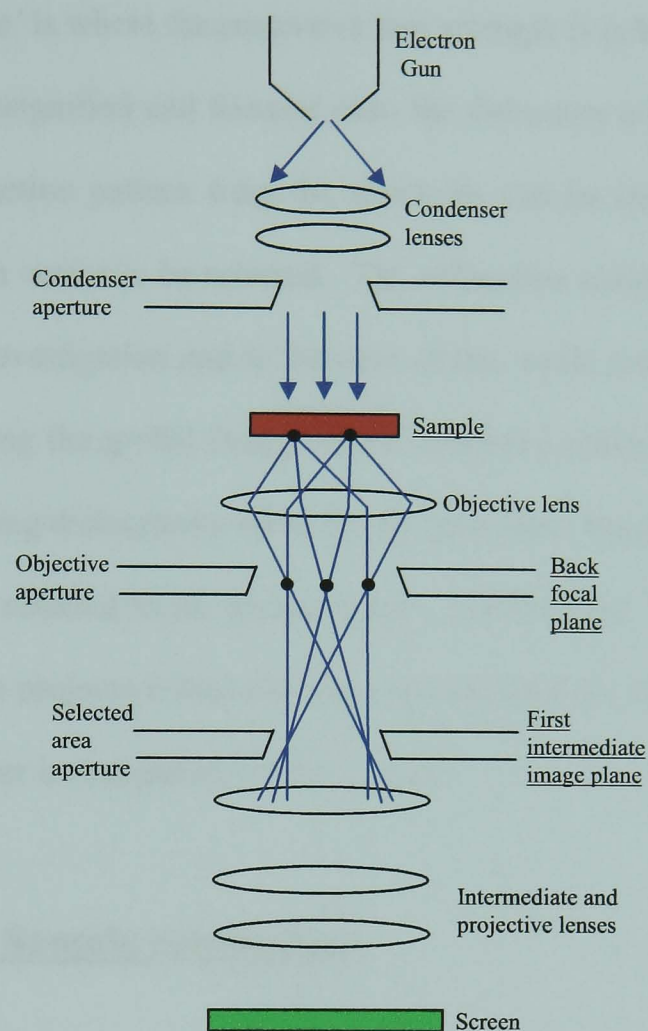
Figure 3.7. Schematic layout of the JEOL 2000FX Tansmission Electron Microscope.

Below the electron gun are a series of condenser lenses. In most systems as in the case for the JOEL microscope used for this work there are two condenser lenses. These lenses de-magnify the electron beam emitted from the source and control the diameter of the beam used to illuminate the sample. They also collimate the beam into a parallel incident beam. Below the condenser lenses is a condenser aperture that centres the convergence angle of the beam onto the sample. Next, the sample itself is mounted on a double tilt goniometer thus allowing different Bragg diffraction planes to be used. Immediately below this is the objective lens which determines the maximum magnification that may be obtained from the microscope; x500 K in the case of the JEOL JEM 2000FX. Finally, below this are the intermediate and projective lenses.

These may be operated in one of two ways depending on the image required. Firstly, *'diffraction mode'* is where the projective lens strength is reduced so that the back-focal plane image is magnified and focused onto the florescent screen. When in diffraction mode, the diffraction pattern from the specimen can be imaged allowing the correct Bragg diffraction vector to be selected. The diffraction vector used is dependent on the material under investigation and in the case of this work, cross sectional TEM samples were viewed using the **g**=004 Bragg vector condition which is well suited to the SiGe system for showing dislocations while for the plan view, the **g**=220 was used. The other viewing option, referred to as *'Image mode'*, is where the first intermediate image is magnified by the projective lens and then focused onto the florescent screen. In image the structure under investigation can be viewed.

3.4.2 X-TEM Sample preparation

The samples used for XTEM had to be prepared methodically and correctly in order to obtain accurate results. A brief summary of the procedure used to prepare the samples for this work will be given below. The samples have to be electron transparent and must therefore be thinned which requires patience and careful removal of the excess material. Initially, two pieces of the material were glued together, epi-surface to epi-surface with supporting silicon material attached on the outside. The material is then waxed to a flat holding block and ground down perpendicular to the epilayer surfaces from one side and polished using diamond paste until a mirror surface is obtained. This was primarily achieved by using progressively finer and finer wet and dry paper on a grinding wheel rotating at ~250RPM. The wet and dry paper used started at P200 grit and finished with P1200 grit. To remove the scratches left behind

from the wet and dry paper, the samples were lapped using 6 μm and 1μm diamond paste. After one side was polished the sample was flipped over and the process repeated. This time the material had to be thinned to ~25-50 μm with the wet and dry before being polished with the diamond paste. After polishing the second side a copper support ring was attached with the two samples interface running down the centre of the copper ring. The sample contained within the copper ring was then removed from the holder and beamed using an argon ion beam at a shallow angle so as to create a small hole within the interface region between the two samples. Once the hole was achieved an area of material surrounding the hole was believed to be of electron transparency and this was the area ready for viewing within the microscope.

In the case of the plan view samples, a piece of the sample (~1 cm^2) was taken and waxed face (epilayer) down to the glass slide. The sample was ground down and polished from the back side using the same procedure as used for XTEM until it was ~25-50 μm thick. A copper ring was then glued to the polished backside of the sample. The excess material outside of the copper ring was chipped away and the material enclosed by the copper ring carefully removed from the glass slide by gently applying heat. The excess wax was removed by warming the ringed sample in IPA. The Sample was then Ar ion beamed from the ringed side until a small hole was visible and the surrounding material close to the hole believed to be thin enough to view on the microscope.

3.5 <u>Atomic Force Microscopy (AFM)</u>

The Atomic Force Microscope (AFM) is a relatively new and powerful tool in today's modern research field. From AFM measurements, the surface of many

materials that have appeared planar to the eye or optical microscope, have in fact been shown to be very far from planar, with a large amount of surface morphology being discovered. From such detail, investigation at the atomic level has proved especially important in the semiconductor field, given the atomic dimensions now being craved in this field of research. For the work carried out in this thesis, AFM was performed on the samples in order to investigate the surface morphology of the grown structures with the aim of gaining a stronger understanding of how the material was forming during growth. Below is outlined a brief explanation of how the AFM works and some of the benefits it offers to materials research.

3.5.1 The Atomic Force Microscope

The principle behind the operation of the AFM is surprisingly simple. A fine tip with a radius of ~10-20 nm is scanned over the samples surface and by using piezoelectric scanners the cantilever beam will rise and fall with the surface topography of the specimen. By using feedback to control the piezoelectric scanners, a constant force or height above the samples surface can be maintained. By having a constant force, height information from the sample may be obtained whilst for a constant height, force information can be obtained. The tip is typically constructed from Si_3N_4 or Si and is mounted on the end of a cantilever. The Nanoscope AFM, as used for this work employs an optical detection system in which the tip is attached to the underside of a reflective cantilever. A diode laser is focused onto the back of the reflective cantilever. As the tip passes over the samples surface the cantilever is raised and lowered in conjunction with the surface. As the cantilever moves the laser beam is deflected with the subsequent beam collected using a dual element photodiode. The photodiode acts as

a photo-detector and the laser intensity detected by the photodiode varies accordingly with the distance the cantilever moves. The measured light intensity is converted into a voltage. This voltage is then used to control the tip to be either applied to the surface under a constant force or kept off the samples surface at a set distance. From the voltage data the computer package can build up a comprehensive picture of the samples surface.

One major advantage that AFM has over similar techniques for measuring surface topography, such as scanning tunnelling microscope (STM) and scanning electron microscopy (SEM), is that the measurements can be performed in air rather than under vacuum, allowing the technique to compete well on cost and ease of use. Typical scan sizes used were in the range 500 nm × 500 nm up to 20 μm × 20 μm. The vertical resolution is atomic as would be expected.

The AFM is used in one of two modes of operation, namely, '*contact mode*' or '*tapping mode*'. In the case of '*contact mode*', which happens to be the mode typically used, the tip is kept in close contact with the surface while it is scanned over the area of interest. In the case of '*tapping mode*' the tip is alternately lowered onto the surface to provide high resolution and then lifted while the sample is moved before being lowered again. This process is performed continuously until the area of interest has been covered. '*Tapping mode*' overcomes such problems associated with friction, adhesion, and electrostatic forces but is far more complicated to perform.

3.6 Electrical characterisation of semiconductor materials

Electrical properties are undoubtedly one of the principal, if not the foremost areas of interest for any semiconductor material, given their applications to devices and their impact on today's modern environment. In order to investigate the electronic characteristics of the SiGe structures grown for this work, resistivity and Hall measurements were routinely performed. Epitaxially grown MOS device material is un-doped originally, with the doping being added afterwards, usually through implantation and subsequent annealing. However, in order to characterise the electrical properties of the epitaxially grown material prior to a full device process run, modulation doping has to be employed (see section §2.3.7). This is performed in order to optimise the samples growth conditions and structure, whilst avoiding the expensive and time consuming processing procedures. By growing modulation doped structures the main characteristic crucial to device performance can be determined, this being mobility for a specific carrier density.

3.6.1 The van der Pauw resistivity measurement

In 1958 van der Pauw [van der Pauw, 1958] developed a technique for measuring the resistivity and Hall effect of any semiconductor sample of arbitrary shape. The measurement involves the positioning of four contacts at the outermost edges of the sample. A constant current is then passed between two of the adjacent contacts which in turn induces a voltage across the other two adjacent contacts. It is important that no current flows through the voltage contacts so as to avoid contact

resistance problems. Van der Pauw determined that in order for this measurement to be valid the following four conditions had to be upheld.

1. The contacts must be located at the circumference of the sample
2. The contacts are sufficiently small
3. The samples thickness must be homogeneous
4. The sample surface must be connected singularly without any holes or discontinuities.

In order to measure the samples sheet resistance, a simple Greek cross design as depicted in figure 3.8 was used. The actual fabrication process involved in making such a sample will be discussed in section §3.6.3.
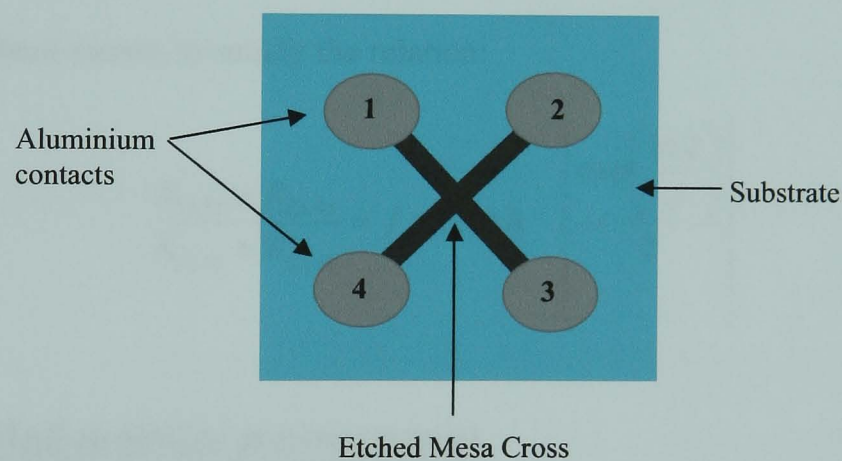
Figure 3.8. Plan view showing the cross arrangement used for the resistivity and Hall measurements.

The VdP resistivity measurements were performed by passing a current between two adjacent contacts of the cross (i.e. contacts 1 and 2) and measuring the voltage induced across the two remaining contacts (contacts 3 and 4) giving the effective resistance $R_{12.34}$. The resistivity of the sample may then be found from:

$$\rho = \frac{\pi d}{\ln 2} \left[\frac{R_{12,34} + R_{24,41}}{2} \right] f(Q)$$

<div align="right">(3. 11)</div>

where

$$R_{12,34} = \frac{V_{34}}{I_{12}}$$

$$R_{23,41} = \frac{V_{41}}{I_{23}}$$

$$Q = \frac{R_{12,34}}{R_{23,41}}$$

<div align="right">(3. 12)</div>

and d the samples thickness. In order to correct for any asymmetry in the Greek cross (which would be inevitable given the process used for fabrication), four VdP measurements were made on each sample, (indexing by 90° around the contacts) in each case. By doing this the mean samples effective resistance was determined.

The function f[Q] is known as the correction factor and the solution of this function has been shown to satisfy the relation:

$$\frac{R_{12,34} - R_{23,41}}{R_{12,34} + R_{23,41}} = f \, \mathrm{arccos} \, h \left\{ \frac{\exp\left(\frac{\ln 2}{f} \right)}{2} \right\}$$

<div align="right">(3. 13)</div>

3.6.2 The Hall mobility measurement

Following on from the VdP resistivity measurements, the fabricated Greek cross structure may also be used to determine the Hall mobility. This is obtained by applying a magnetic field perpendicular to the sample while passing a current (I) through two opposite contacts (1 & 3). The induced voltage is measured using the two remaining

contacts (2 & 4), and is the known as the Hall Voltage (V_H). From this measurement the samples Hall coefficient (R_H) may be determined from:

$$R_H = \frac{10^4 V_H}{IB} = \frac{r_H}{n_p q}$$

(3. 14)

The Hall factor (r_H) is defined as the ratio of the Hall mobility (μ_H) and the drift mobility (μ_d) and is dependent on scattering mechanisms, band structure and temperature. If the Hall factor is unknown it is common practice to replace it with 1 and so the Hall coefficient is then given as:

$$R_H = \frac{1}{n_p q}$$

(3. 15)

Equation 3.15 also shows the inversely proportional relationship between carrier concentration (n_p) and Hall coefficient (R_H). Finally the Hall mobility is found from:

$$\mu_H = \frac{R_H}{\rho}$$

(3. 16)

3.6.3 Sample preparation

In order to perform the Van der Pauw measurements on the samples, a Greek cross structure similar to the schematic diagram of figure 3.9 was created. A piece of the material about 2 cm^2 was cleaved from the wafer and cleaned by rinsing in DI water and then Iso-propanol (IPA). The material was then loaded into the sputtering equipment and aluminium dots (1 mm in diameter and on a square pitch of 10 mm) were sputtered across the sample through an alumina mask.

A Greek cross pattern was etched into the sample surface by means of lithographic procedures and acid etching. In order to achieve this, the whole of the

samples surface was covered with a polymer based resist which was then exposed to UV radiation though a Greek cross patterned mask. After exposure, the polymer resist exposed to the UV was removed leaving only the polymer resist in the shape of a Greek cross pattern on the samples surface. The Greek cross mask creates a cross between four nearest neighbour aluminium dots as well as covering the four aluminium dots in order to protect them from the subsequent etch. The sample was then etched using a CP-4A etch that consists of $HF:HNO_3:CH_3COOH$ in the ratios 3:5:3. The polymer resist mask pattern protects the material beneath while the remaining exposed area is removed at approximately 35 μm/min. The sample was typically etched for ~3 s. After etching the photoresist was removed leaving a Greek shaped cross with four aluminium contacts at the corners of each arm. The sample was rinsed in DI water and IPA before being blown dry under dry N_2. Finally the sample is annealed for 10 minutes at 400°C under a dry N_2 atmosphere in order to drive the aluminium into the sample and forming ohmic contacts to the channel.

For a detailed explanation of the actual sample preparation the reader is referred to the PhD Thesis of M^{C}Gregor [M^{C}Gregor, 1997].

3.6.4 Cryostat

The cryostat used to measure the samples was a Leybold Ltd. closed cycle cryostat system. This system enabled electrical measurements to be carried out within the temperature range of 10-300 K. The sample was mounted on a copper sample holder that was directly mounted onto the expander head so as to form a good thermal contact as cooling of the sample was by thermal conduction. The sample temperature was monitored by a calibrated Si diode that was mounted close to the sample holder.

Given the nature of the measurements the samples had to be electrically isolated from the sample holder, and this was achieved by placing a thin lamella of insulating silicate beneath. A vacuum of $\sim 10^{-5}$ Torr was achieved using a small turbo pump system before cryo-pumping commenced. The vacuum was required in order to prevent heat conduction during cooling while heat radiation to the sample was reduced by the inclusion of an aluminium heat shield surrounding the sample. Once again, a more thorough explanation of the actual measurement set up is found in the PhD Thesis of M^{C}Gregor [M^{C}Gregor, 1997].

4. Ge channel heterostructures- Results and Discussion

The introduction of Ge into Si based technology has yielded improved electron and hole carrier mobilities leading to an enhanced current drive in FET devices. Much of the work in the early years was based on psuedomorphic $Si_{1-x}Ge_x$ layers grown on Si for x up to ~0.5. As the requirements for faster, higher current drive devices at smaller dimensions has evolved, the Ge fraction has also been increased in order to see if further improvements in pMOS are obtainable.

In this chapter, work carried out by the author into optimising modulation doped pure Ge channel heterostructures with the aim of producing improved device quality material for FET applications will be discussed. The initial part of this chapter covers some preliminary results obtained from structures grown completely using Solid-Source Molecular Beam Epitaxy (SS-MBE). Following on from this, results using a 'hybrid-epitaxy' method combining Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPE-CVD) [Rosenblad *et al*, 2000] and Ultra High Vacuum-Chemical Vapour Deposition (UHV-CVD) [Samavedam and Fitzgerald, 1997] grown virtual substrates with the heterostructure grown on top using SS-MBE will be examined. This 'hybrid-epitaxy' approach has demonstrated some exciting results, comparable with recently reported results using different single epitaxy growth techniques. The results presented here help pave the way for this type of integrated technique to be further developed with possibilities for future device technology.

4.1 <u>SS-MBE grown structures</u>

As described in chapter 2, the most realistic way of obtaining a Ge channel heterostructure with a sufficiently thick channel to be of any use for device applications is to use a Virtual Substrate (VS). Initial growths in order to achieve this were performed using the VG V90s solid-source MBE tool. A set of VS's of varying thicknesses within the range 150 nm up to 1.8 μm were produced. On top of the VS, a Ge channel, inverted modulation doped heterostructure was deposited, allowing the VS quality for device applications to be investigated by measuring the heterostructure's electrical properties. The typical layer structure intended for the samples used in this work is schematically depicted in figure 4.1 with the actual individual sample ID numbers and parameters given in table 4.1.

| 2 nm Si |
| 20 nm $Si_{0.3}Ge_{0.7}$ |
| 8 nm Ge Channel |
| 15 nm $Si_{0.3}Ge_{0.7}$ |
| 5 nm $Si_{0.3}Ge_{0.7}$, 2×10^{18} cm^{-3} B |
| Constant composition $Si_{0.3}Ge_{0.7}$ layer |
| Linearly graded SS-MBE grown virtual substrate |

SS-MBE Growth interrupt and 30 minute 800°C anneal →
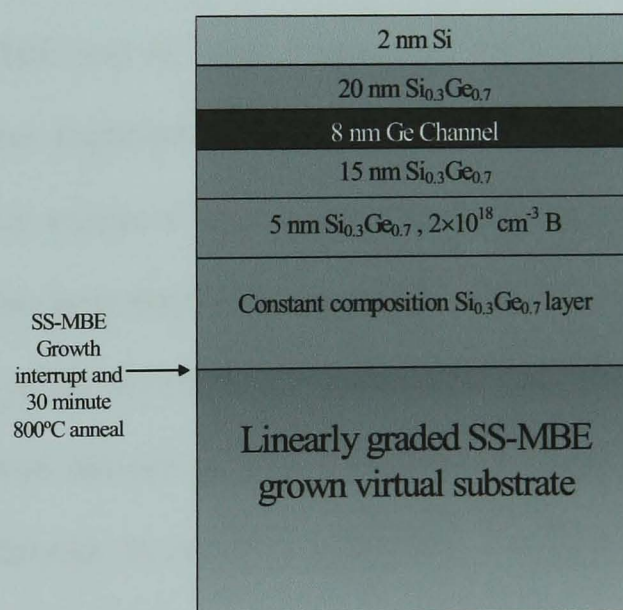
Figure 4.1. Schematic diagram of the SS-MBE grown VS and Ge channel heterostructure.

Sample ID	Linearly Graded VS thickness (nm)	VS constant composition layer thickness (nm)	Doping layer thickness (nm)	Spacer layer thickness (nm)	Ge channel layer thickness (nm)	Capping layer thickness (nm)
622/27	100	50	8	15	8	20
622/28	200	100	8	15	8	20
622/64	1000	200	8	15	8	20
622/66	1000	200	8	15	8	20
622/82	1800	200	8	15	8	20

Table 4.1. Summary of the SS-MBE grown VS's and Ge channel heterostructres including the intended layer parameters.

By growing the virtual substrates at different thicknesses the only parameter changed was the grading rate. Thin VS's of less than 2 µm were studied for the initial work. A problem is the length of time it takes to grow layers of several microns thickness using SS-MBE and so large numbers of thick layers were not a realistic option. Inherent source depletion problems in e-beam systems, especially for thicker layers would inevitably require a large number of re-calibrations, typically after each growth. Also, given the poor thermal conductivity associated with SiGe, thin VS's are preferable. For state of the art MOSFET devices, the high current density of heavily scaled, deep sub-micron devices generates large local power densities. If the heat cannot be dissipated through the substrate efficiently, a process known as 'self heating' occurs, where the device begins to warm up, leading to increased resistances and an overall degradation of the device performance.

For 45 nm CMOS technology node, leading device manufacturers are exploring different substrate materials in order to boost device performance. Potential advanced

substrate materials include silicon-on-insulator (SOI) and strained Si layers grown on a relaxed $Si_{0.7}Ge_{0.3}$ VS. Welser [Welser, 1994] has measured the thermal properties of SiO_2, Si and $Si_{0.7}Ge_{0.3}$, and found that SiGe and SiO_2 have very similar thermal conductivities of 0.06-0.1 $Wcm^{-1}K^{-1}$ and 0.014 $Wcm^{-1}K^{-1}$ respectively [Welser, 1994]. For an SOI substrate, the oxide layer on top of the Si is typically 100 nm, whereas for a $Si_{0.7}Ge_{0.3}$ VS layer, the total thickness can be of the order of several microns. The SiO_2 therefore holds the advantage given that the heat generated only has to pass through a thin layer (100 nm) of poor thermal conductor before reaching the underlying Si compared to a several micron SiGe VS on top of Si.

SiGe VS's also suffer from a poor surface topography due to a large scale roughening referred to as 'cross-hatch'. This 'cross-hatch' occurs due to the pile-up of threading components of misfit dislocations present to relieve the strain. Such misfit dislocation pile-ups will have associated strain-fields leading to the cross-hatch formation as discussed in section §2.2.3 [Hsu *et al*, 1992]. Such large scale 'cross hatch' roughness (with its large periodicity of ≥ 500 nm) is believed to have negligible effect on the electrical measurements such as those performed in this work [Feenstra and Lutz, 1995]. According to Feenstra and Lutz, the most dominant roughness scattering will be from roughness close to the Fermi wavelength of the carriers. The Fermi wavelength is defined as

$$\lambda_F = \frac{2\pi}{k_F}$$

(4. 1)

Where k_F is the carrier wave vector and is given by:

$$k_F = \sqrt{\pi n_P}$$

(4. 2)

where n_p is the carrier density. For the intended heterostructure used for this work (see figure 4.1), a carrier sheet density of 1×10^{12} cm^2 was typical. Using equations 4.1 and 4.2, the Fermi wavelength is found to be ~35 nm. Hence roughness of the order of 35 nm is therefore expected to be the most influential on the types of structures used for this work.

The starting Si substrates used were n-type (001) Si, and they underwent a standard chemical cleaning process consisting of an RCA stage I and II, followed by a dilute HF dip prior to loading into the growth system. The precise cleaning conditions are given in section §3.1.2.

The final HF dip is used to passivate the wafer surface with hydrogen and has also been found to reduce an inherent boron spike [Kubiak *et al*, 1986]. Once the cleaned wafers were introduced into the load-lock, the system was pumped down to High Vacuum (HV) conditions. After HV was obtained the wafers were transferred into the prep chamber and then, when Ultra High Vacuum (UHV) is regained, transferred to the growth chamber. An *in-situ* high temperature desorb was then performed which involves the wafer being heated to ~860°C for 30 minutes in order to drive off any residuals such as hydrogen, oxygen and fluorine left on the wafer surface. Following this, the temperature was then lowered to the required growth temperature, which, for these particular structures was 550°C. Growth commenced with the linearly graded VS region which varied in thickness for each sample. Once the graded region was completed, an interrupt was introduced to allow for a high temperature, 800°C anneal for 30 minutes. When growing a graded SiGe layer, the material close to the surface remains elastically strained at all times. The thickness of such strained material is referred to as an equilibrium critical thickness. In order to try and relax this equilibrium critical thickness the high temperature anneals were employed.

Fitzgerald *et al* [Fitzgerald *et al*, 1992] showed that the equilibrium critical thickness (h_c) for the introduction of dislocations into a graded layer is given by:

$$h_c^2 = \frac{3D\left(1 - \frac{\upsilon}{4}\right)\ln\left(\frac{eh_c}{b}\right)}{YC_f}$$

(4. 3)

Where C_f is the grading rate, Y Youngs modulus, υ Poissons ration, b the magnitude of the Burgers vector and D is given by:

$$D = \frac{Gb}{[2\pi(1-\upsilon)]}$$

(4. 4)

with G the shear modulus. Figure 4.2 shows a plot of equation 4.3 on how the critical thickness varies with grading rate for the SiGe system.
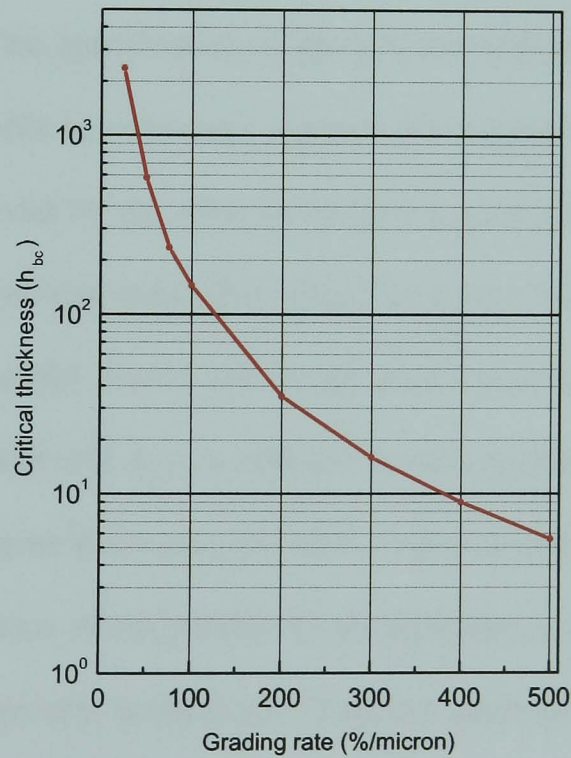
Figure 4.2. Plot showing the equilibrium critical thickness as a function of Ge grading rate for a linearly graded SiGe VS.

From figure 4.2 it is evident that as the grading rate increases the critical thickness decreases. Given the high grading rates used for these structures it was estimated that the critical thickness varied between 40 nm for the thinnest VS (100 nm linearly graded) and 180 nm for the 1.8 μm layer. The in-situ anneal was performed in order to fully relax the strained critical thickness layer present prior to any further growth. Following the anneal, the samples were left to cool for ~30 minutes with the aim of reaching the required temperature for re-growth, upon which a further constant compositional layer was deposited prior to the modulation doped heterostructure. All the active heterostructures were intended to be identical and were grown at a nominal growth temperature (T_G) of 425°C. The low growth temperature was used to suppress roughening [Cullis et al, 1994] and Ge segregation [Grützmacher et al, 1993] known to occur for high Ge layer concentrations at increased growth temperatures. Unfortunately, due to the specification of the pyrometer fitted to the growth system at the time, it was only able to accurately measure the temperature of Si wafers down to ~450°C, but was believed by the growers to give a good indication down to ~400°C. The growth temperature was controlled using the power levels applied to the heater typically used for a Si wafer. Given that the pyrometer was calibrated for the emissivity of Si, whilst a SiGe wafer will have a different emissivity, there is to be expected some inaccuracy in the true growth temperature with respect to the intended, although this is still unknown. One factor of the growth temperature that is known to be very good is the reproducibility of growth temperature using the same power levels from wafer to wafer.

4.1.1 VS layer composition and strain

The virtual substrate composition and state of relaxation is a major influencing factor in obtaining high Ge fraction heterostructures. To investigate that the required Ge content of the $Si_{0.3}Ge_{0.7}$ VS's had been achieved and that full relaxation obtained, HRXRD measurements were performed on the structures. Two (004) symmetric scans and two asymmetric scans using the (115) and $(\bar{1}\bar{1}5)$ directions were performed in order to determine the terminating Ge content and state of relaxation of the VS. The experimental procedure is described in more detail within §3.2.6. The following table (Table 4.2) shows the results obtained from the measurements.

Sample ID	Final Ge fraction (%)	Relaxation (%)	Calculated relaxed lattice parameter (a_L) (Å)	Final Ge fraction after correcting for Vergads Law (%)
622/27	75.0	99.5	5.59997	76.5
622/28	74.6	99.3	5.59966	76.4
622/64	67.0	99.7	5.58288	69.4
622/66	66.4	99.5	5.58296	69.5
622/82	72.6	97.9	5.59614	75.0

Table 4.2. VS composition and state of relaxation found from the High resolution X-ray diffraction measurements performed.

From these results it is seen that the final composition of the VS does vary from sample to sample, and in some cases is significantly different from the intended

$Si_{0.3}Ge_{0.7}$ layer composition. The state of relaxation achieved for all the structures however was of the magnitude required.

Samples 622/27 and 622/28 were grown following a series of samples at a much lower Ge fraction, nominally 50% Ge. The previous calibration for these samples had been found to be lower than intended ($Si_{0.54}Ge_{0.46}$). Given the time constraints, the samples were grown without the system undergoing further calibration for a higher Ge fraction. The X-ray measurements aptly demonstrate the importance of calibrating the system prior to growth. Before the growth of samples 622/64, 622/66 and 622/82, the growth system was calibrated for a Ge fraction much closer to the required 70% Ge value given the inaccuracies found in wafers 622/27 and 622/28. This was achieved by growing a strained 3 period Si/SiGe superlattice for a nominal Ge fraction of 60%. The reason why a 60% superlattice was used instead of a 70% was twofold. Firstly, the SiGe layers had to be thick enough so that they could be readily resolved by a single symmetric scan, and secondly the layers had to remain below the Matthews and Blakeslee criteria for critical thickness. From a single (004) symmetric scan performed on such calibration wafers, the Ge fraction may be determined along with the layer thicknesses by using a simulation package to fit to the rocking curve obtained. Figure 4.3 shows a typical symmetric (004) rocking curve for a strained 3 period superlattice structure used for calibration. From figure 4.3, the spacing of the first large peak relative to the Si peak, and the further large peaks relative to each other enables the Ge fraction to be determined, while the smaller peaks in-between are referred to as *'thickness fringes'* and are used to determine the individual Si and SiGe layer thickness. The software used was Philips's High Resolution Simulation (HRS) software, version 1.3. Using the information obtained from the calibration wafer rocking curve, the actual

growth rates for the Si and Ge e-guns was determined, and used to calibrate the growth system prior to the required growth.
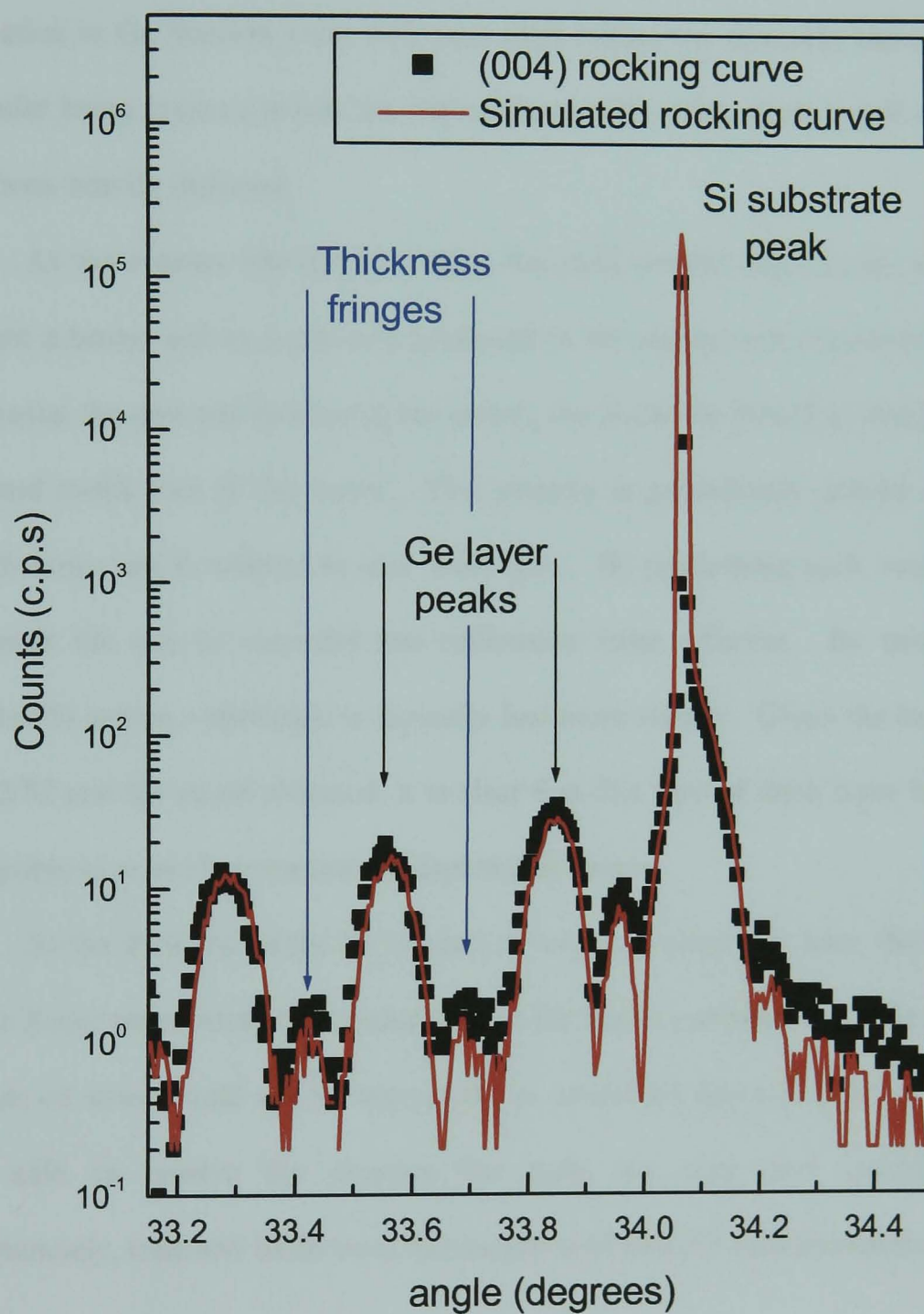
Figure 4.3. 004 X-ray rocking curve and HRS simulation for a strained 3 period SiGe/Si superlattice structure typically used for calibration purposes during this work.

By performing a calibration immediately before the growth of samples 622/64 and 622/66, the VS Ge composition was found to be as intended. However, even by taking this extra care over the calibration, the thick 1.8 μm VS was found to deviate from the intended Ge fraction significantly. It is believed that the reason for this large fluctuation in Ge fraction, even with such high calibration measures taken, was due to the wafer being grown towards the end of the growth series where the Si source would have been heavily depleted.

As the e-beam hits the Si source, the melt created only occurs locally to the incident e-beam, and so a crater is produced in the source over a period of time. By defocusing the spot and increasing the power, the Si can be forced to melt over a wider area and re-fill part of the crater. This process is periodically carried out during a growth series and is referred to as a *'melt back'*. By performing such *'melt backs'*, the Si source life can be extended and calibration more efficient. By using a heavily depleted Si source, calibration is typically lost more readily. Given the large thickness of 622/82 and the result obtained, it is clear that this type of thick layer becomes very susceptible to error if grown using a depleted Si source.

As the thickness of the Ge channel is very thin, nominally 8nm, this was too thin for the X-ray measurements to detect, and so the actual composition of the channel, and its state of strain could not be measured. A reciprocal space map (rsm) should have been able to resolve the channel but these are very time consuming scans. Unfortunately, time and funds were not readily available for such measurements.

4.1.2 VS structural integrity.

The structural integrity of the VS's had to be determined given that this will have a large bearing on the materials device prospects. In order to do this, pieces of the samples were prepared for cross sectional Transmission Electron Microscopy (XTEM) analysis as discussed in section §3.4.2. From the resulting XTEM images it was shown that the VS's contained very large amounts of dislocations throughout both the linearly graded VS and the active heterostructure. Also observed for the sample's with a VS ≤ 1 μm was very large scale surface roughness. Figures 4.4a & b show the XTEM images of samples 622/27 and 622/28 taken under the two-beam bright field condition with an acceleration potential of 200 keV, and a Bragg diffraction vector of $\mathbf{g}$=004.

(a)

Ge Channel

Growth Interrupt interface

Constant composition & Active layer

Si Substrate

Linearly Graded Buffer

100 nm

(b) Ge Channel

Growth Interrupt interface

Constant composition & Active layer

Linearly Graded Buffer

100 nm
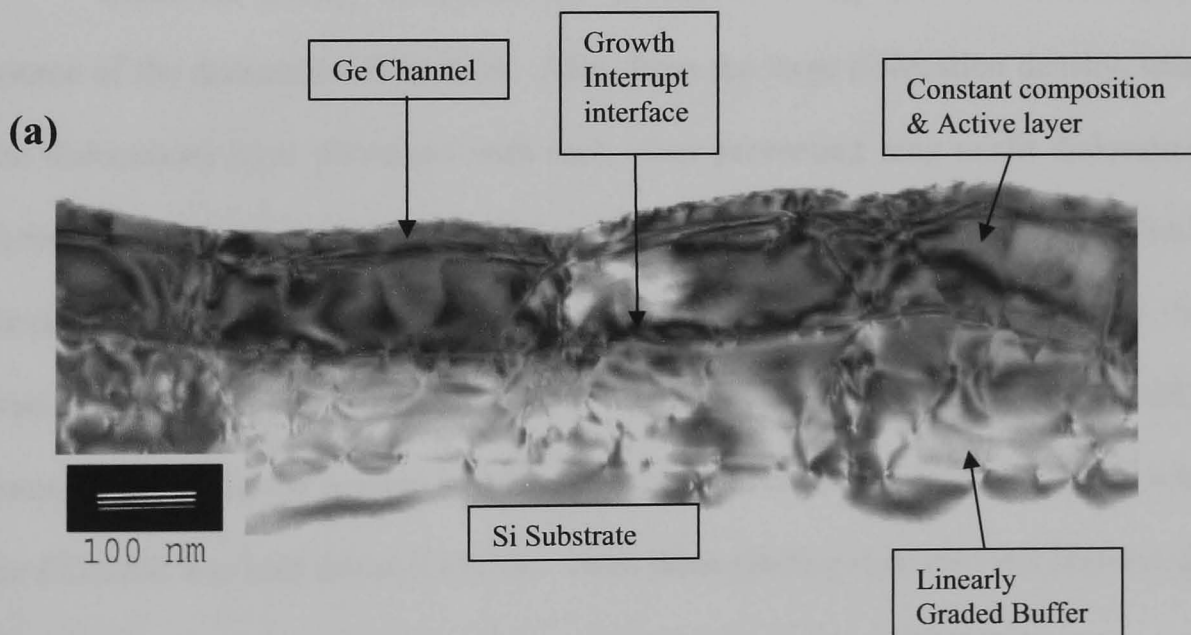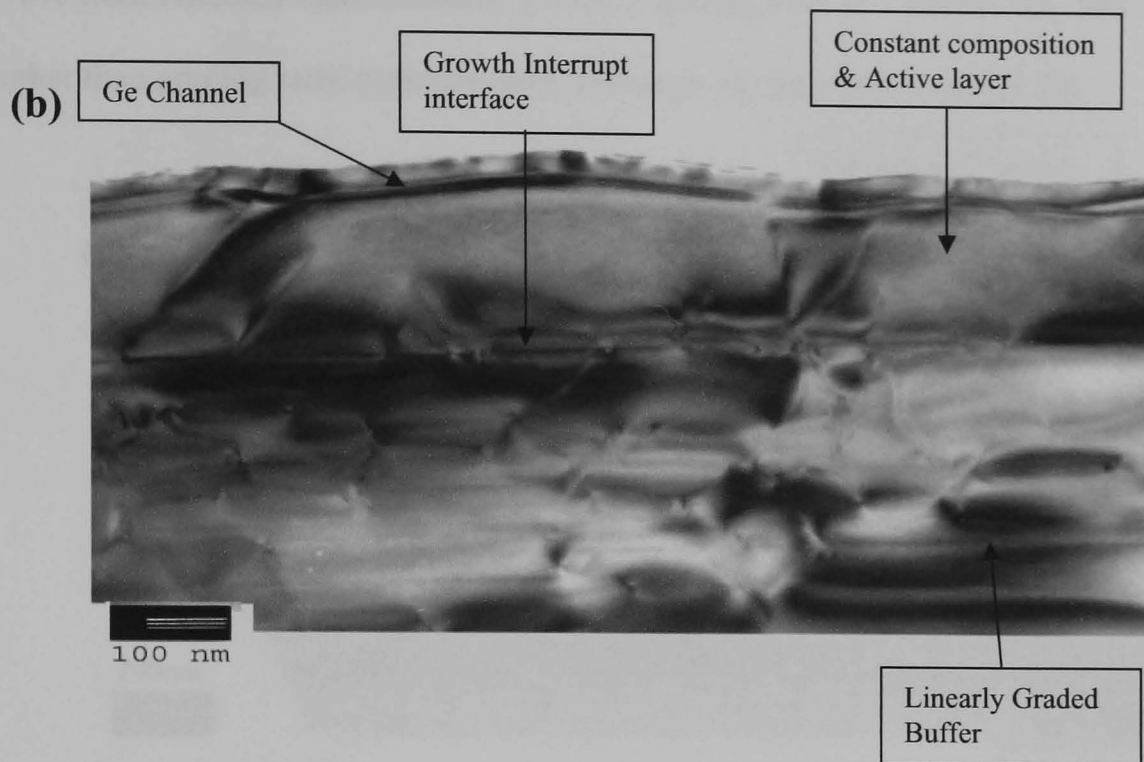
Figure 4.4. (a) XTEM of sample 622/27 (150 nm VS) showing the poor material quality of both the VS and active layer whilst (b) the XTEM of sample 622/28 (250 nm VS) showing the high number of dislocations present within the material.

Given the density of dislocations present it is very difficult to determine the source of the dislocation formation. Also, from the large dislocation density, many of the dislocations have interacted with each other preventing long misfit dislocations to form. The formation of long misfit segments is a desired property as they limit the threading dislocation density enabling a good quality VS's to be grown. As the Ge fraction for both these samples was determined to be ~80% from HRXRD measurements, the Ge grading rate for 622/27 can be estimated to be 0.8 %/nm, whereas for 622/28 it was half this at 0.4%/nm. Both these grading rates are very high compared to typical values used, which are of the order of 10%/μm ($\equiv$0.01%/nm).

XTEM images of samples 622/64 and 622/66 (figures 4.6a & b) again show a very high dislocation network within the VS region, with large surface roughening also being observed. The terminating Ge content of the structures was determined to be

~70% from HRXRD measurements, giving a grading rate of ~0.07%/nm, still ~7 times higher than grading rates typically used, although ~6 times less than 622/28.
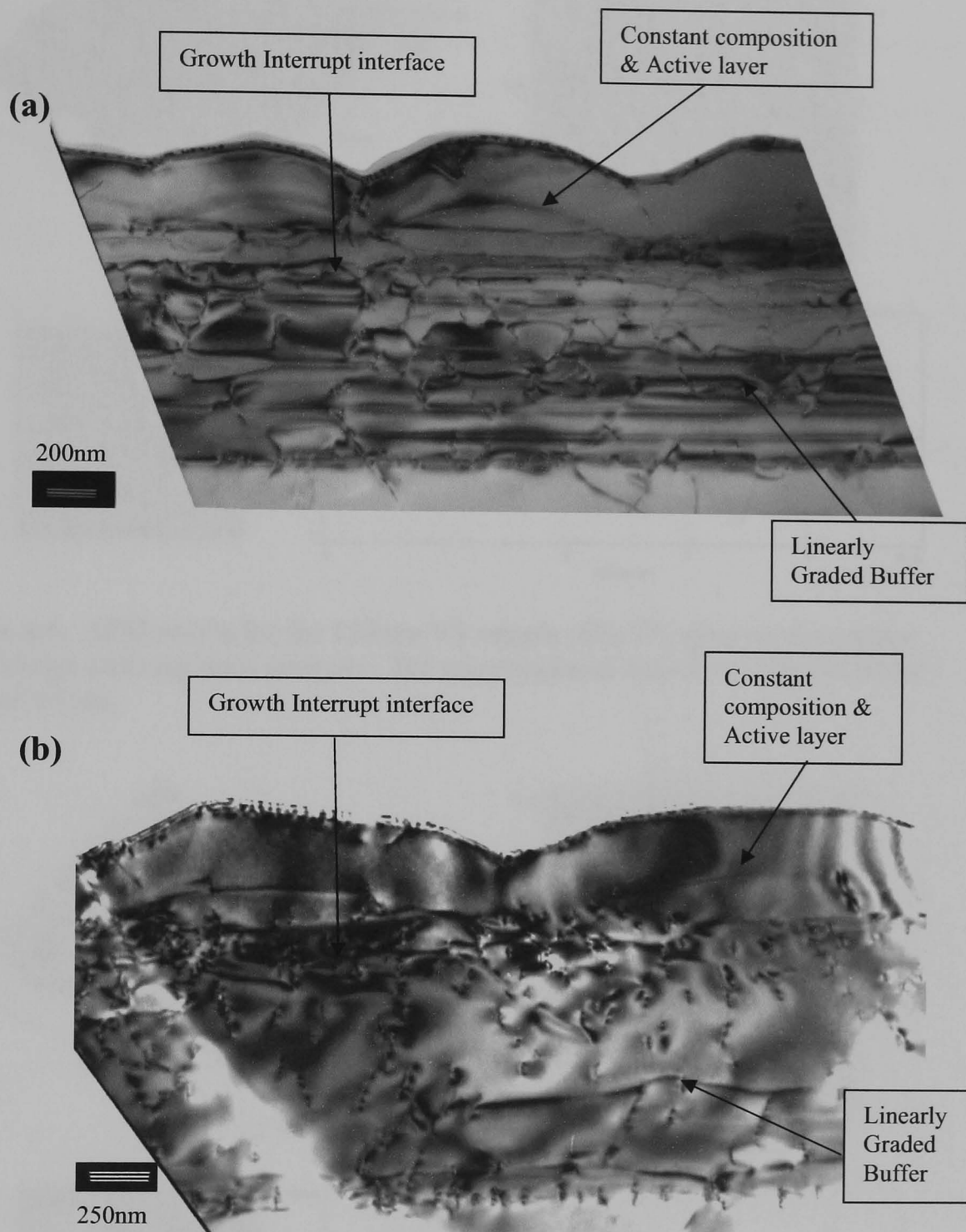
Figure 4.5. XTEM of the 1.2 μm VS samples (a) 622/64 and (b) 622/66 showing the high number of dislocations and large scale surface roughening.

AFM from these samples reiterated the poor surface quality seen from XTEM. Figures 4.6a and b and 4.7a and b show AFM images of the 150 nm (622/27) and 300 nm (622/28) VS samples surfaces respectively.
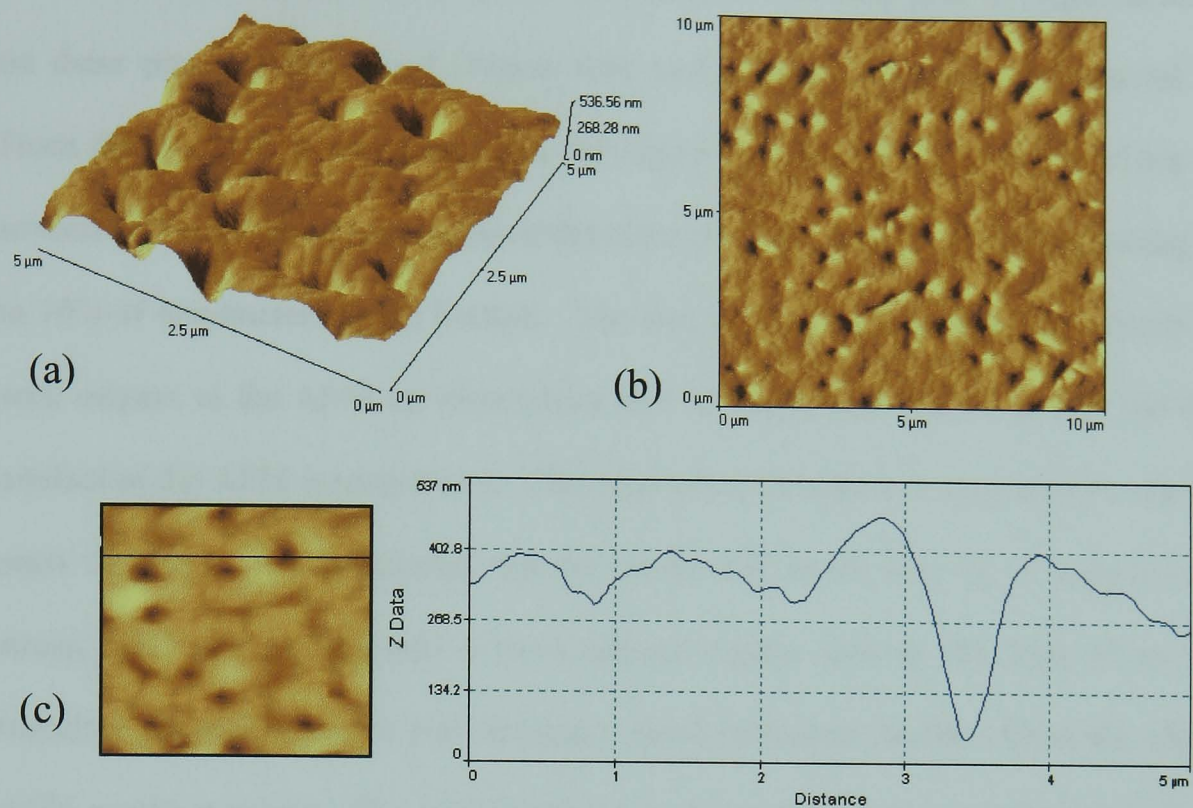
Figure 4.6. AFM results for the 150 nm VS sample (622/27) showing the surface morphology and roughness analysis. The rms roughness was observed to be of the order of 45 nm.
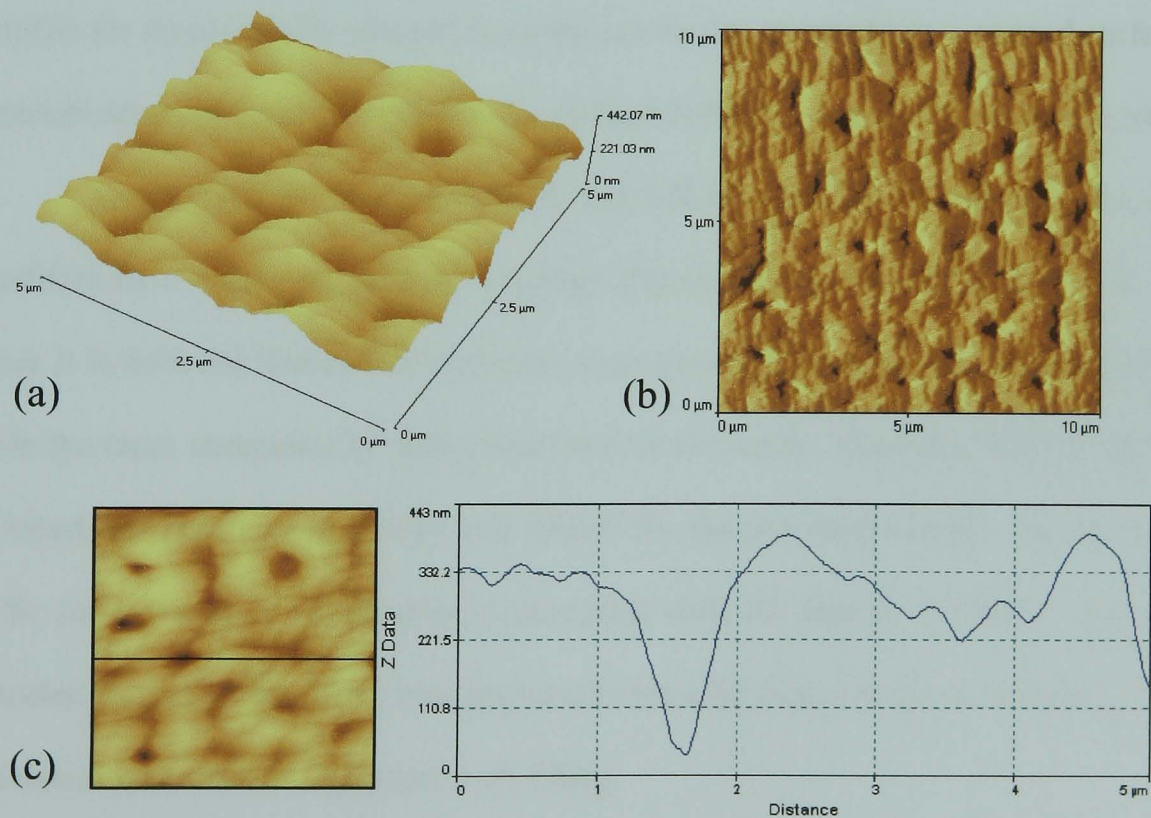
Figure 4.7. AFM results for the 300 nm VS sample (622/28) showing the surface morphology and roughness analysis. The rms roughness was observed to be of the order of 30 nm.

What was evident from these AFM images were deep pits. Roughness analysis on these pits was performed (Figure 4.6c and 4.7c) to determine their lateral sizes. From this analysis it was found that the depths of the pits ranged from 10 nm up to several 100 nm with a cross sectional diameter of ~500 nm at the surface reducing down to 10's of nanometers at the bottom. The size of the pits observed is extremely large with respect to the AFM tip dimensions and therefore believed to be real and not an artefact of the AFM measurement. This type of pit formation is suggested to arise from mass transport. It is postulated that Ge atoms will move away from regions of high stress, such as a pit, towards a more relaxed region such as the peak of an island, therefore deepening the pit and forming a groove between islands. From the observed AFM results it appears that significant mass transport has occurred, leaving very deep grooves/pits in the morphology of 622/27 and 622/28. Yang and Srolovitz [Yang and Srolovitz, 1993] have modelled this behaviour to show how a nominally flat surface profile for an elastically stressed material can be transformed into a cusped surface with smooth tops and crack like grooves by surface diffusion, similar to the present results.

In the case of samples 622/64 and 622/66, the AFM images of the samples surfaces have a very periodic morphology (figures 4.8a and b and 4.9a and b). In this case it is believed that as the structures were grown, the layers transformed themselves into the more energetically favourable state of 3D facets. Once the faceted surface was formed, the subsequent growth will follow the faceted morphology. Figures 4.8c and 4.9c show the scale of roughness associated with the faceted surfaces. This type of faceted formation has been seen previously for a $Si_{0.5}Ge_{0.5}$ layer on Si and is discussed in detail by Jesson *et al* [Jesson *et al*, 1996].
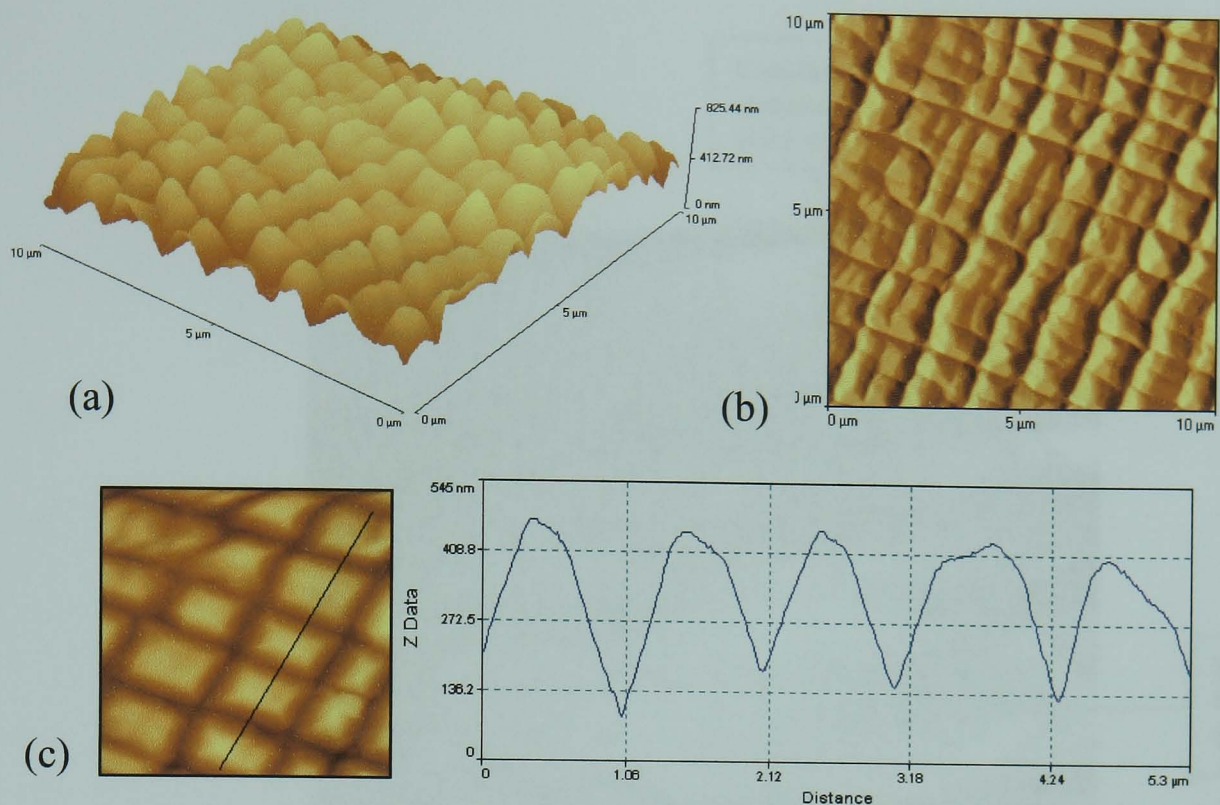
Figure 4.8. AFM results for the 1.2 μm VS sample (622/64) showing the surface morphology and roughness analysis. The rms roughness was observed to be of the order of 65 nm.
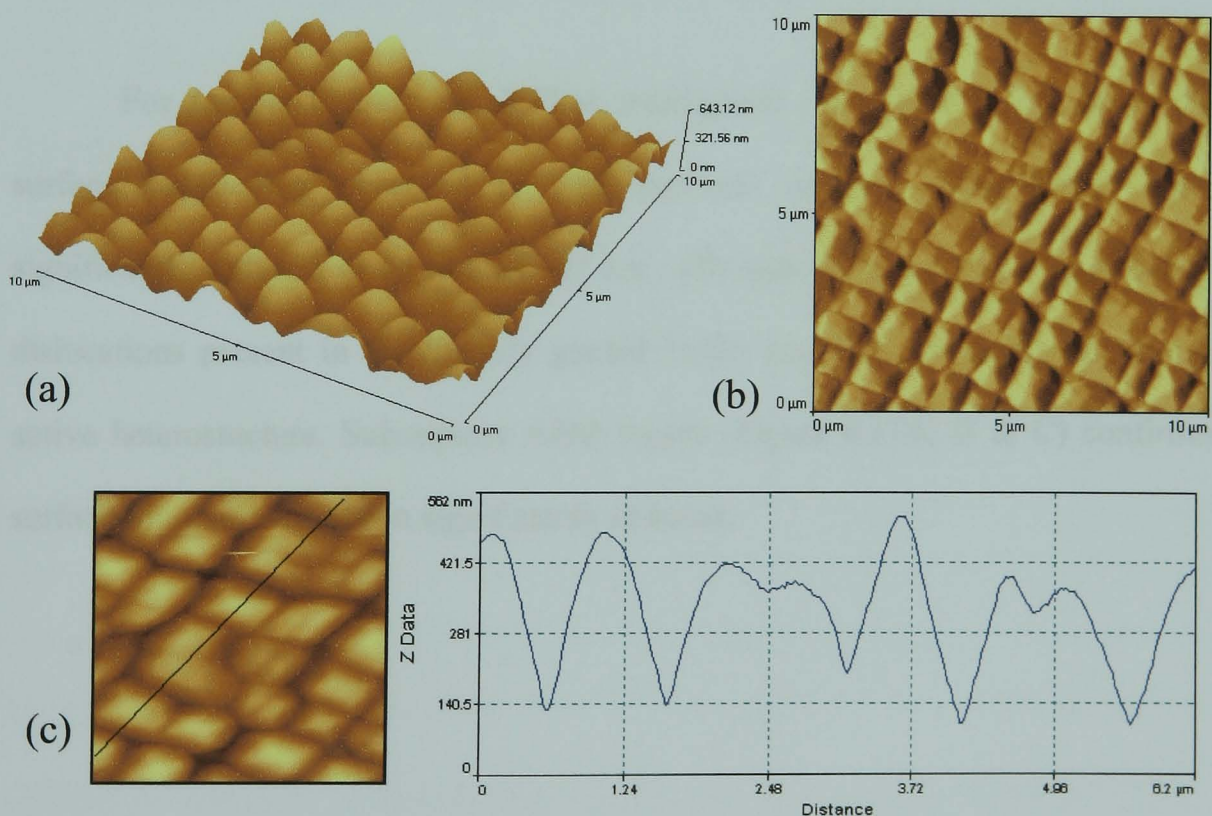
Figure 4.9. AFM results for the 1.2 μm VS sample 622/66 showing the surface morphology and roughness analysis. The rms roughness was observed to be of the order of 65 nm.
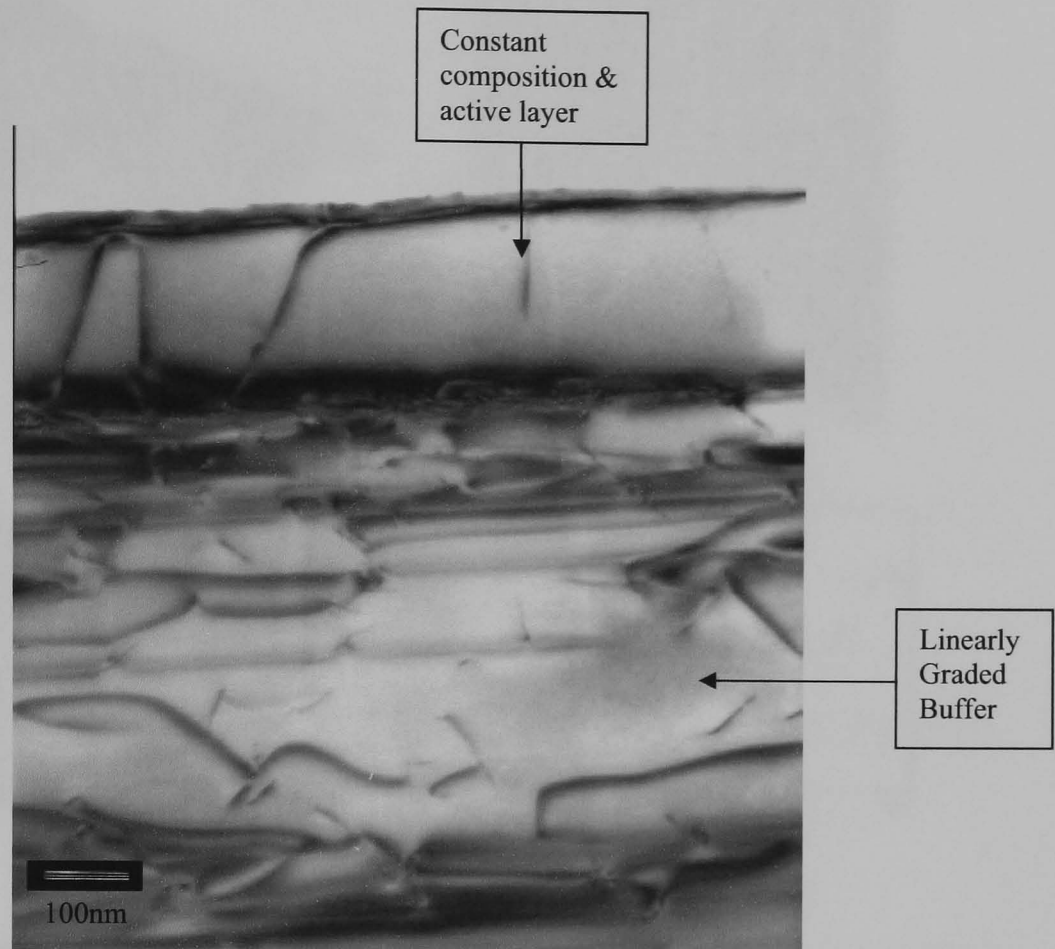
Figure 4.10. XTEM of sample 622/82 (2 μm VS) showing the large number of misfit dislocations present in the VS and dislocations penetrating into the active layer.

For sample 622/82, the XTEM micrograph (see figure 4.10) shows that the surface roughening observed for the previous samples (rms≥30 nm) has been significantly reduced to an rms of ~15 nm, although there are still a large amount of dislocations present in the linearly graded buffer and then traversing up through the active heterostucture. Subsequent AFM results (Figure 4.11A, B & C) confirmed the surface roughness had been significantly reduced.

(a) (b) (c)
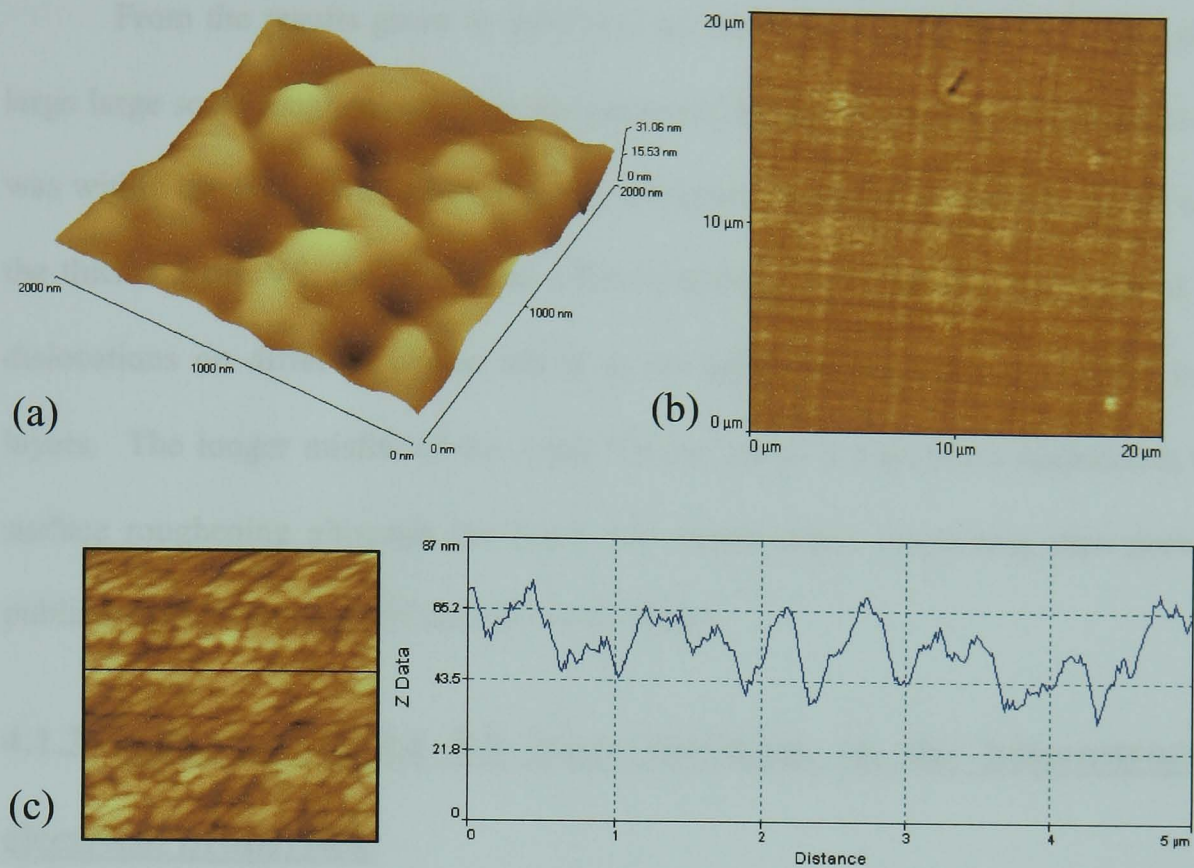
Figure 4.11. AFM results for the 2 μm sample (622/82) showing the surface morphology and roughness analysis. The rms roughness was observed to be of the order of 15 nm.

The rms roughness observed from AFM for the SS-MBE structures is summarised in table 4.3.

Sample ID	VS thickness (μm)	Approximate rms roughness (nm)
622/27	0.15	45
622/28	0.3	30
622/64	1.2	65
622/66	1.2	65
622/82	2	15

Table 4.3. Summary of the rms roughness observed for samples 622/27, 622/28, 622/64, 622/66 and 622/82 as measured from a 1 μm AFM scan.

From the results given in table 4.3, all the VS structures up to 1.2 μm showed large large scale roughening. This has occurred due to the methods in which the strain was within the layers was relieved (mass transport and facet formation). In the case of the thicker 2 μm VS, the strain was relieved through the formation and glide of misfit dislocations on different planes which is the preferred way for strain relief in such layers. The longer misfits of the 2 μm VS has led to a significant suppression in the surface roughening although the layer still shows larger roughening than previously published VS's structures [Capewell *et al*, 2002].

4.1.3 Influence of the VS layer thickness on the heterostructures electrical properties.

Van der Pauw measurements were used to measure the electrical properties of the strained Ge channel heterostructure and to (indirectly) monitor the quality of the VS leading to the possibility of finding a minimum thickness VS useable for a pure Ge 2D hole gas (2DHG) structure.

Standard van der Pauw measurements were performed on all the as-grown samples between 10 K and room temperature. Figure 4.12 shows the samples mobility and carrier density determined from the Hall measurements. From the results given in figure 4.12, it is seen that all the samples show evidence of 2DHG carrier confinement in which the sheet carrier density approaches a constant value at low temperatures as the charge carriers occupy the reduced energy states of the confinement potential and ionised carriers from parallel conduction paths are frozen out (see §2.3.7). The measured Hall mobilities appear to vary between samples with no obvious trend with

buffer layer thickness. One observation from figure 4.12 is that the 2 μm sample (622/82) has a lower carrier concentration with respect to the other structures measured.
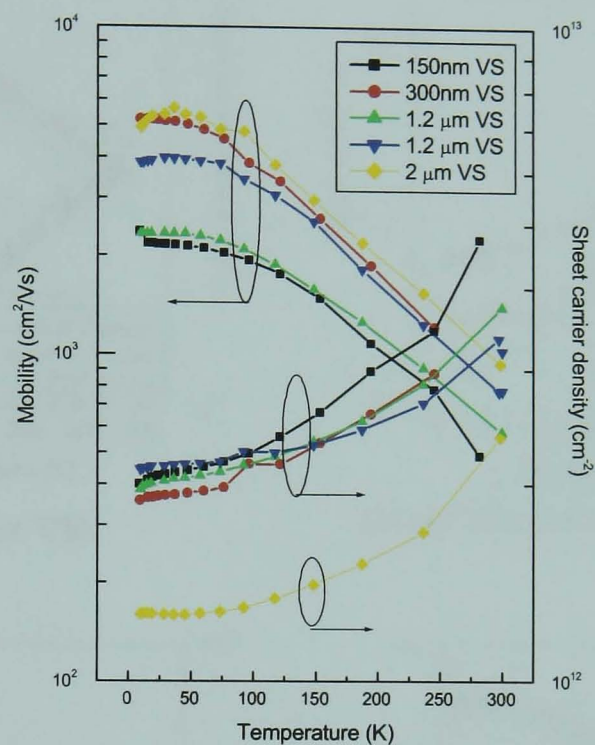
Figure 4.12. Measured as-grown mobility and carrier density data for the SS-MBE modulation doped structures 622/27, 622/28, 622/64, 622/66 and 622/82 on varying VS thicknesses.

It had been shown previously by Hammond [Hammond, 1998] for similar work on strained $Si_{0.5}Ge_{0.5}$ heterostructures that a post growth anneal of the samples improved the electrical results. Such anneals of 30 minute durations were performed on all the samples within the temperature range 650-850°C. Due to the limited amount of sample 622/82 given that this structure was only grown on half a wafer, the annealing studies were omitted at this stage of the work.

Figure 4.13a-d shows the annealed Hall results for samples 622/27, 622/28, 622/64 and 622/66.

94
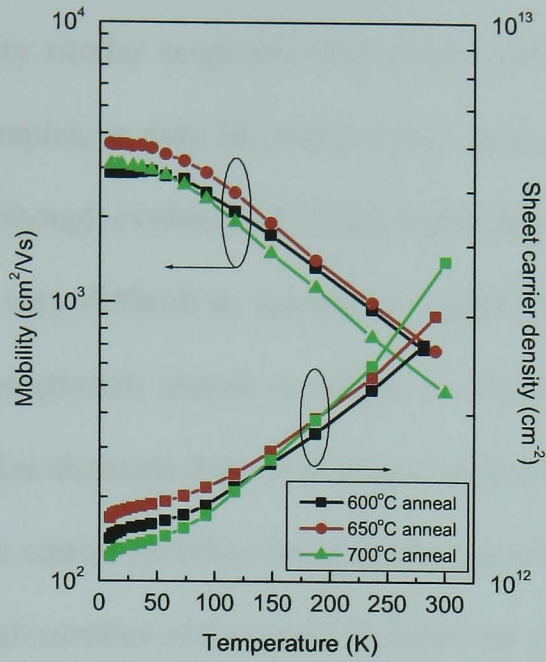
(a). 622/27 (150 nm VS)
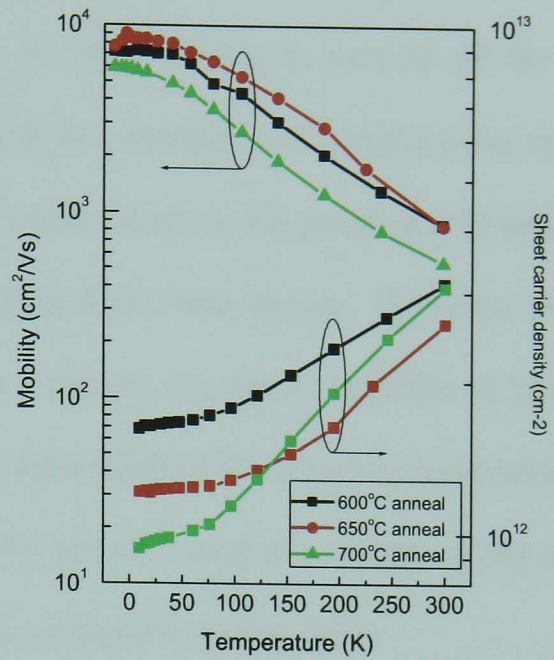
(b.) 622/28 (300 nm VS)

(c). 622/64 (1.2 um VS)
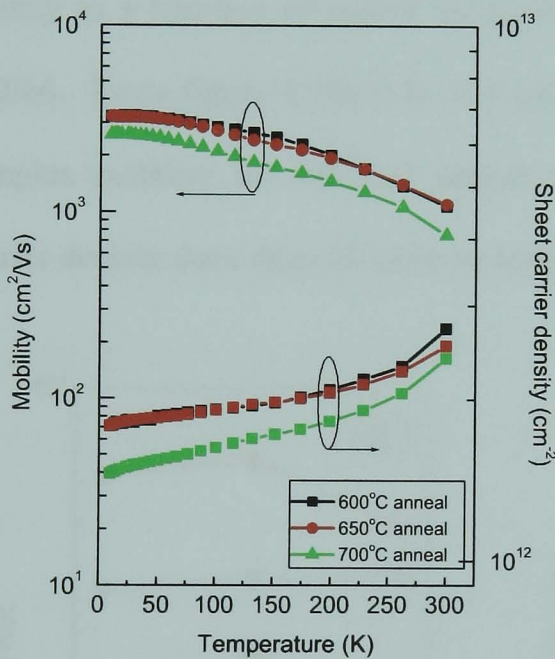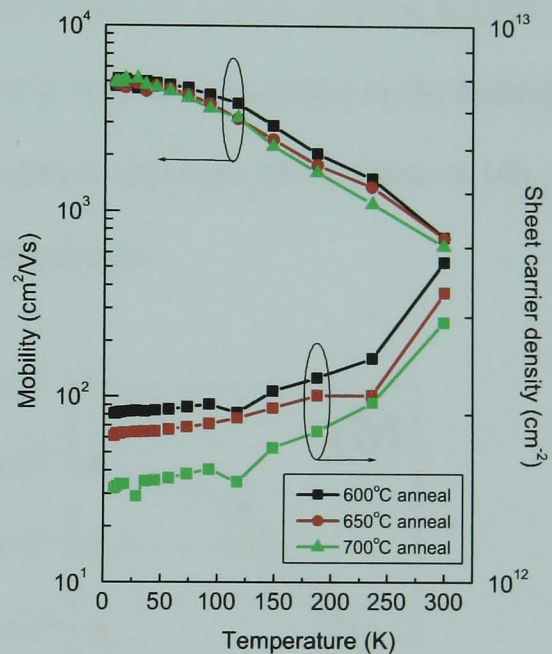
(d). 622/66 (1.2 um VS)

Figures 4.13a-d. Measured Hall results for the SS-MBE grown structures after annealing at different temperatures for 30 minutes under dry N_2.

Little improvement in mobility was observed for the samples with the only significant change occurring in the carrier density, which appears to reduce during higher temperature anneals. This is indicative of out-diffusion of the boron doping layer and inter-diffusion of the Ge channel with the surrounding $Si_{0.3}Ge_{0.7}$ buffer,

thereby reducing the band offset of the confinement channel. As sample 622/82 showed very similar as-grown Hall results and poor structural quality as seen for all the other samples, it may be inferred that annealing of this structure will yield similar results. Although evidence of 2DHG behaviour was observed, given the poor material quality it is very difficult to interpret or surmise anything from these results. However, since a post-growth anneal sequence is expected to improve the carrier mobility of strained SiGe channels deposited at low temperature (Hammond 1998), it may be postulated that the carrier mobility limiting mechanism of the present samples is scattering due to the high number of threading dislocations present in the poor quality VS's.

Figure 4.14a shows a plot of the 10 K mobility while figure 4.14b the carrier density as a function of anneal temperature for structures 622/27, 622/28, 622/64 and 622/66. From figure 4.14a it is seen that there is very little variation in the individual samples mobility for different anneal temperatures although from figure 4.14b, the carrier density does drop off with increasing temperature.
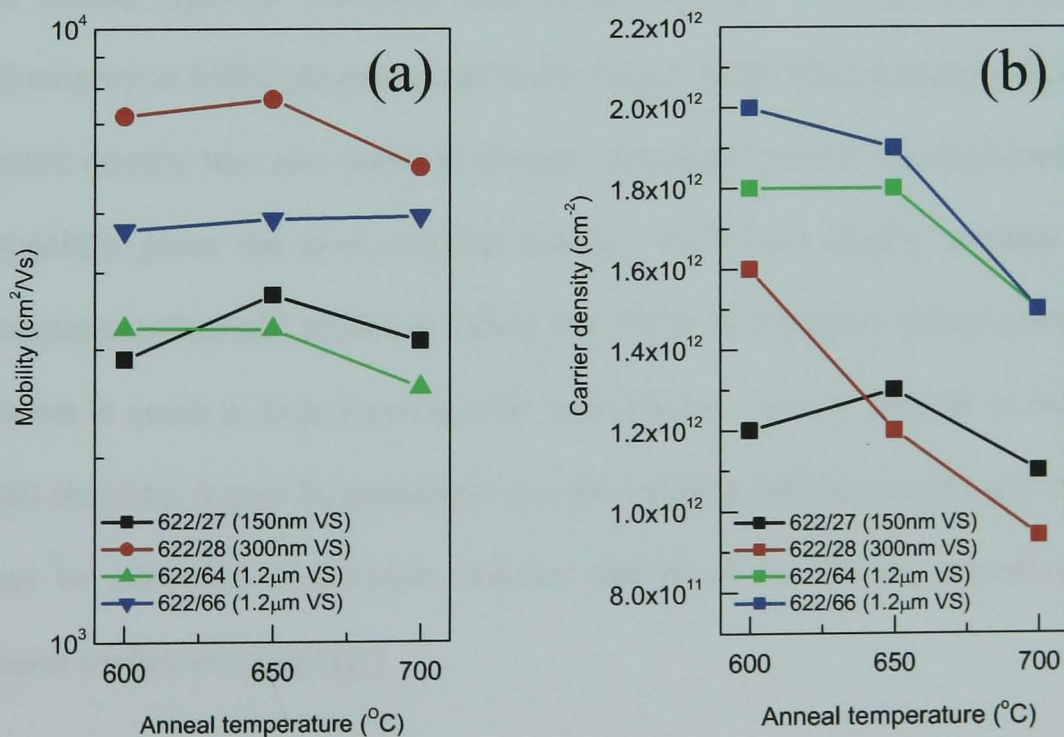
Figure 4.14a & b. Plot of mobility and carrier density as a function of anneal temperature for samples 622/27, 622/28, 622/64 and 622/66.

4.1.4 Summary

A first series of pure Ge channel, inverted modulation doped heterostructures on thin VS's have been grown using SS-MBE. XTEM analysis of these structures indicates that the VS's contained a very high density of dislocations unsuitable for the growth of a high quality heterostructure layers. As well as the high number of dislocations present, AFM showed the surface morphology contained large roughening, bordering on 3D growth and pits from mass transport.

All the structures showed some evidence of what appeared to be quantum carrier confinement (2DHG behaviour) from room temperature down to low temperatures (10 K). Given the poor material quality, all the electrical results were found to be inferior to previously published results where room temperature Hall mobilities between 1175 and 1320 cm^2/V [Irisawa *et al*, 2001] along with low temperature mobilities of 13,000 cm^2/Vs (10 K) [Irisawa *et al*, 2001] up to 55,000 cm^2/Vs (4 K) [Xie *et al*, 1993] for similar types of structures have been observed. Post growth annealing for 30 minutes up to 650°C showed some improvement in the Hall mobility although the sheet carrier density was also found to change with anneal which was attributed to diffusion, especially given the poor material quality. Such poor quality material may lead to "transient enhanced" diffusion which is a form of enhanced diffusion due to defects, known to occur in Si processing after implantation. Due to the lack of improvement in Hall mobility, it may be postulated that the mobility limiting mechanism of the samples may be attributed to the poor material quality of the VS (ie. threading dislocations and/or surface morphology).

4.1.5 <u>Conclusion</u>

From the results shown in section §4.1, it was clear that to make any headway towards achieving a high quality pure Ge 2DHG, significant improvements in the growth of the VS would be required before any kind of active heterostructure optimisation could be performed. The aim of this thesis was to investigate the strained pure Ge channel heterostructure and optimise its 2DHG behaviour and not the development of thin VS's.

Thin VS's are a research area of their own and results showing good quality thin VS's (≤ 2 μm) with Ge fraction >50% have been published since the start of this work. The thin VS's developed have not been of the linearly graded type like the ones tried in this work but have varied from incorporating a low temperature Si layer prior to the SiGe growth [Ueno *et al*, 2000] to terrace grading [Capewell *et al*, 2002]. The low temperature Si approach uses an initial polycrystalline Si layer to act as a sink for the dislocations with the aim of inducing the threading dislocations down towards the substrate. In the case if the terrace grading approach, a linearly graded region where the germanium is graded over ~10% Ge is immediately followed by a constant composition to allow the misfits formed in the graded region to glide as far as possible. This growth pattern is then repeated until the final Ge composition desired is achieved.

4.2. <u>Re-Growth studies: SSMBE growth on CVD VS</u>

A new approach of combining SS-MBE with pre-grown high quality CVD VS's was decided upon as a logical step forward. By adopting this 'hybrid-epitaxy' approach, the source depletion problems and time constraints for growing a high quality

thick VS structure would be alleviated, allowing more time for the study of pure Ge channel heterostuctures.

If a method of re-growing the heterostructure on top of a pre-grown VS (hybrid-epitaxy) was to be adopted and optimised, it was imperative that an optimised chemical pre-clean solution for a SiGe VS was to be found. Thick VS's of low threading dislocation density have been produced by a number of CVD techniques. LEPECVD VS's were obtained from a collaborating group (ETH-Zürich). These substrates were linearly graded at 10% Ge per micron to a terminating Ge content of 70%, followed by a 1 μm layer of constant composition (70% Ge). The surface was capped with a 1-2 nm Si layer. Other VS's grown by UHV-CVD were also obtained from MIT. These VS's were again linearly graded, but this time to a terminating Ge content of 60%, with a further 1 μm of constant composition (60% Ge). These were not capped with Si.

4.2.1 Influence of pre-cleaning

The first wafer grown (Sample ID: 65014) using the 'hybrid-epitaxy' technique was carried out on LEPECVD VS with a terminating Ge content of 70%. The VS underwent a full RCA stage I an II clean prior to being loaded into the VG V90S (refer to section §3.1.2).

Following the transfer into the growth chamber the wafer was subject to an *in-situ* flux clean at ~900°C. The wafer was then left to cool for approximately 30 minutes before restarting growth, so as to reach the required re-growth temperature of 450°C. The re-growth structure is schematically depicted in figure 4.15 and consisted of a 200 nm $Si_{0.3}Ge_{0.7}$ constant composition layer, 5 nm $Si_{0.3}Ge_{0.7}$:B doping layer

(B@2×10^{18} cm^{-3}), 15 nm Si$_{0.3}$Ge$_{0.7}$ spacer layer, 8 nm Ge channel, 20 nm Si$_{0.3}$Ge$_{0.7}$ cap layer, and finally terminated with ~2 nm Si.

*LEPECVD/
SS-MBE re-growth
interface* →

2 nm Si
20 nm Si$_{0.3}$Ge$_{0.7}$
8 nm Ge Channel
15 nm Si$_{0.3}$Ge$_{0.7}$
5 nm Si$_{0.3}$Ge$_{0.7}$, 2×10^{18} cm^{-3} B
200 nm Si$_{0.3}$Ge$_{0.7}$
1 μm LEPCVD grown constant composition Si$_{0.3}$Ge$_{0.7}$ layer
7 μm linearly graded LEPECVD grown virtual substrate
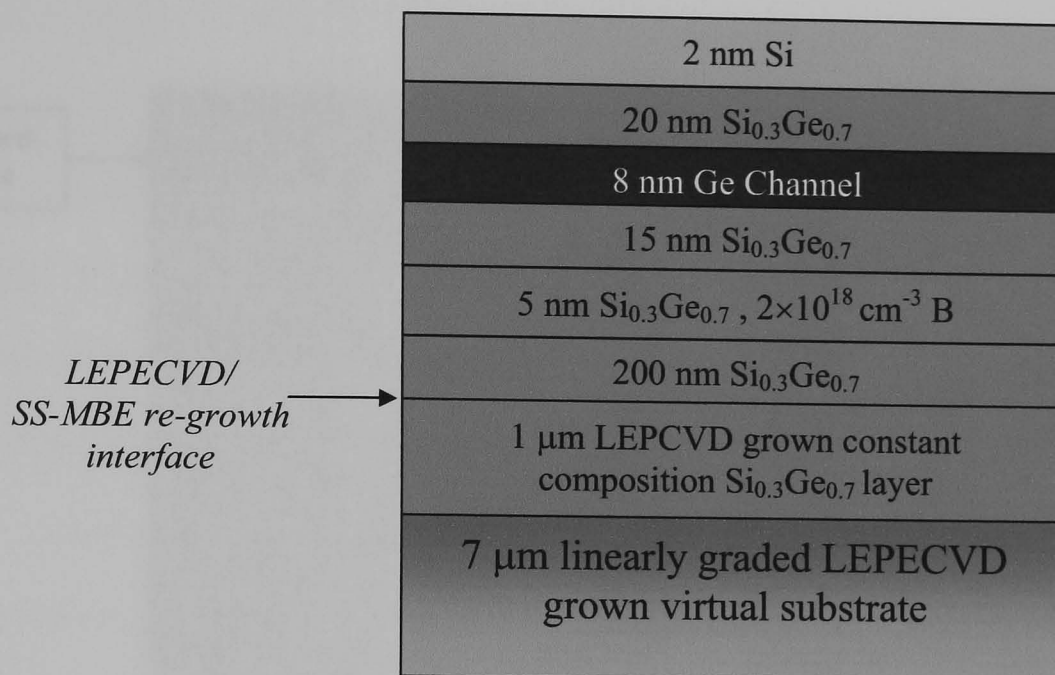
Figure 4.15. Schematic layout of the LEPECVD/SS-MBE structures.

XTEM was carried out to investigate the structural quality. Figure 4.16a shows a micrograph for the VS, re-growth interface and active layer taken under the two-beam bright field condition with a Bragg diffraction vector of **g**=004. From figure 4.16a, the 1 μm constant compositional layer of the VS, which should be directly below the re-growth interface and misfit dislocation free, appears to contain a large number of misfit dislocations. This strongly suggests that the constant compositional Si$_{0.3}$Ge$_{0.7}$ layer on top of the linearly graded VS has been etched away and the misfit dislocations observed are from within the linearly graded region of the VS. Figure 4.16b shows a magnified micrograph for the same sample. From this image it is seen that surface contamination at the re-growth interface is a source for dislocation formation Such contamination of the surface is indicative of a poor pre-epitaxy clean whereby contaminants such as oxygen, carbon and boron are incorporated into the re-growth surface and create defect nucleation sites. The damaged interface has a detrimental

effect on the re-growth, leading to defect propagation and a very poor material quality heterostructure.
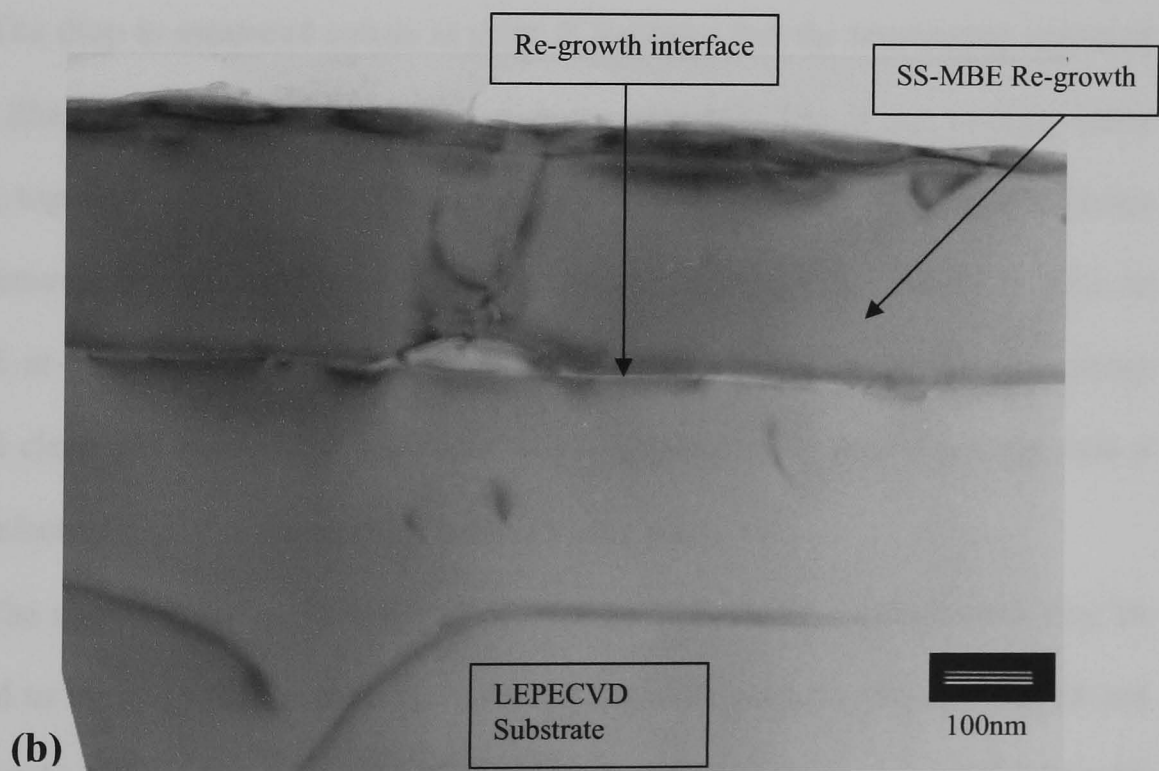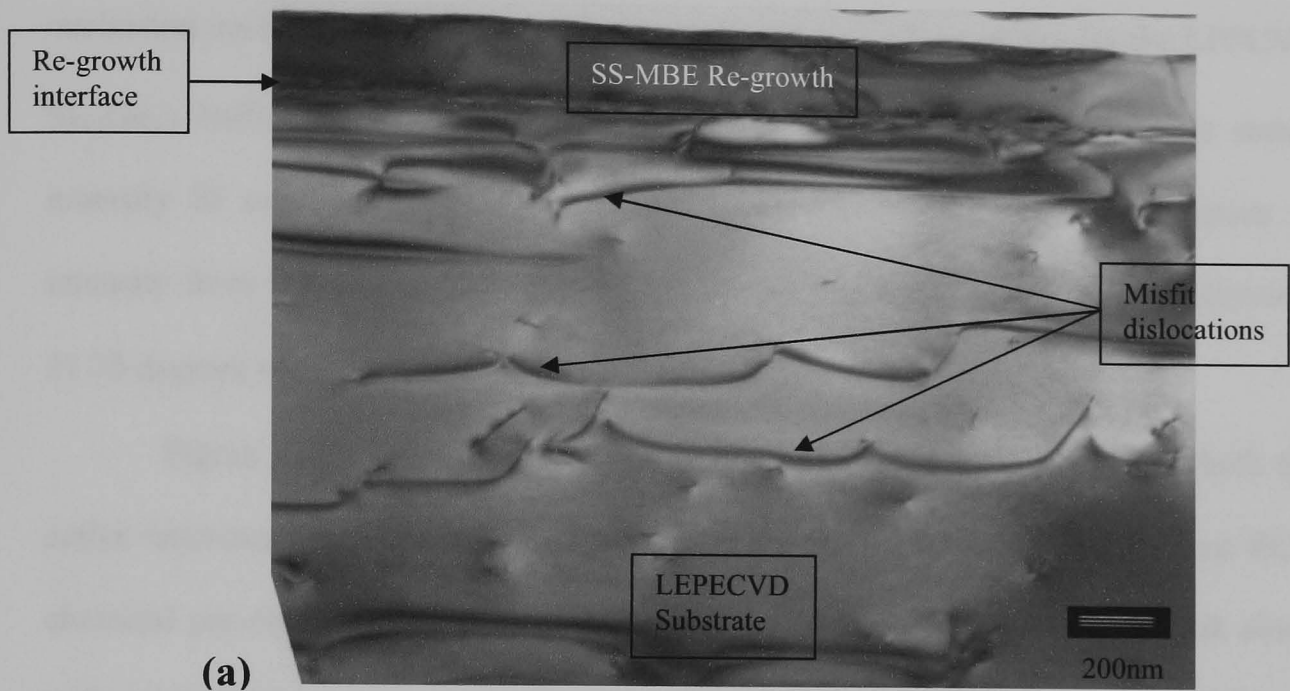
Figure 4.16a & b. XTEM micrographs of sample 65014. (a) Shows a magnified view of the re-growth interface while (b) shows the VS and re-grown heterostructure more clearly.

X-ray analysis was performed in order to see if the layer composition deposited by SS-MBE matched that of the supplied VS. If there was a significant mis-match in the lattice spacing of the re-growth material compared to the VS, strain induced defect nucleation could occur. Figure 4.17a shows the (004) rocking curves for the LEPCVD $Si_{0.3}Ge_{0.7}$ buffer prior to re-growth. From these rocking curves we see the strong intensity Si substrate peak at approximately 33 degrees followed by a plateau in intensity from the graded SiGe layer. Finally there is another peak at approximately 31.75 degrees which corresponds to the 1 μm constant composition layer.

Figure 4.17b shows the (004) rocking curves for sample 65014 in which the active heterostructure was re-grown via SS-MBE on a LEPECVD VS after an RCA chemical pre-clean. From this rocking curve we observe the Si substrate peak along with a measured intensity to the left of the Si peak from the linearly increasing SiGe VS layer. However, a loss of signal is observed in the profile at point X before it recovers again. The drop in measured counts at point X indicates that the terminating region of the VS (that of highest Ge fraction) has been removed. The X-ray rocking curve analysis, together with the XTEM image of Figure 4.16b provide conclusive evidence of the removal of the terminating, high Ge content region of the initial VS prior to SS-MBE re-growth. It is believed that this removal occurred during the pre-epitaxy chemical clean and resulted in the active heterostructure being grown directly onto a highly defective region of the linearly-graded buffer layer.

The rise in signal as we move further away from the Si substrate peak may be attributed to the re-grown layer at the intended $Si_{0.3}Ge_{0.7}$ fraction, and is therefore not lattice matched to the VS. From the XTEM and X-ray rocking curve results, it may be concluded that a chemical clean consisting of RCA stages I and II was far too reactive, leading to a large amount of the VS being etched away.
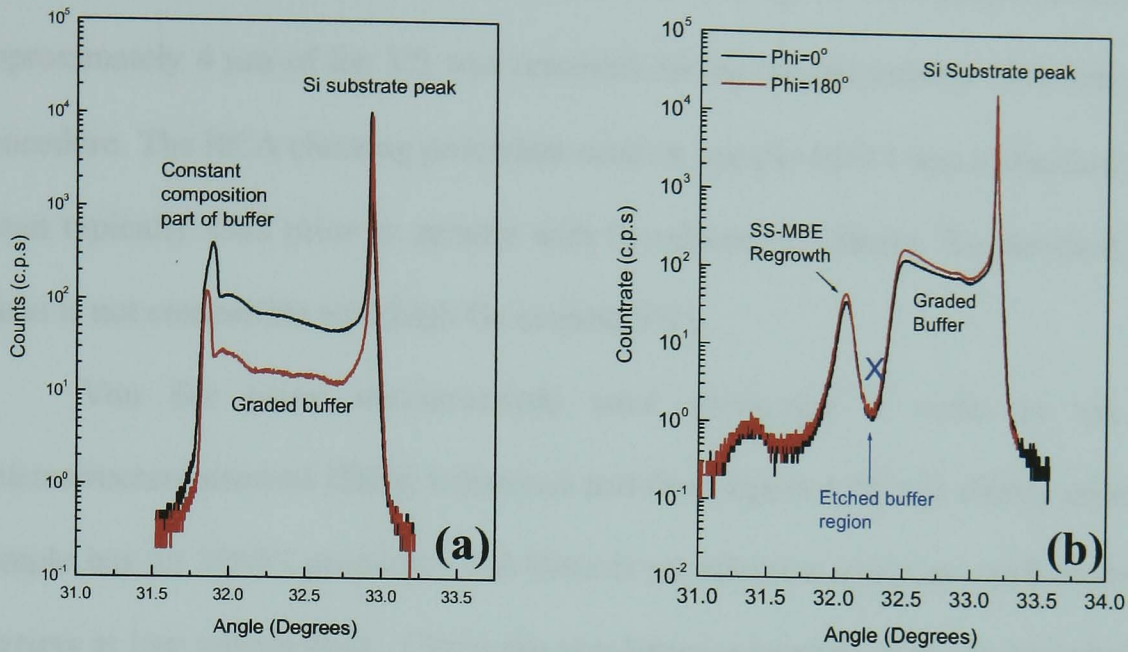
Figure 4.17. (004) Rocking curves for (a) $Si_{0.3}Ge_{0.7}$ linearly graded buffer and (b) sample 65014.

The etch rates of RCA SC-1 at 75° when used in conjunction with SiGe layers of different Ge fraction are given below.

SiGe layer Ge fraction   **Etch Rate**

- 0% (pure Si)   →   ~5 nm/min

- 20% Ge   →   ~10 nm/min

- 40% Ge   →   ~30 nm/min

- 60% Ge   →   ~500 nm/min

- 80% Ge   →   ~900 nm/min

- 100% Ge (pure Ge)   →   ~4 μm/min

The above values are taken from the Berkeley web site:

http://microlab.berkeley.edu/labmanual/chap1/1.6.html#Ge

Given the above etch rates and the X-ray rocking curves it may be estimated that approximately 4 μm of the VS was removed during the pre-epitaxy chemical cleaning procedure. The RCA cleaning procedure used on sample 65014 was a standard Si based clean typically used prior to epitaxy with Si substrates. Clearly, the standard Si RCA clean is not compatible with high Ge content VS's.

Van der pauw measurements were performed in order to see if the heterostructure showed 2DHG behaviour and from figure 4.18 it is clearly seen that the sample has no 2DHG properties and there is no effective quantum confinement of the carriers at low temperature. Given the non-lattice mismatch of the re-growth interface due to the etching from the clean this result is consistent with expectations.
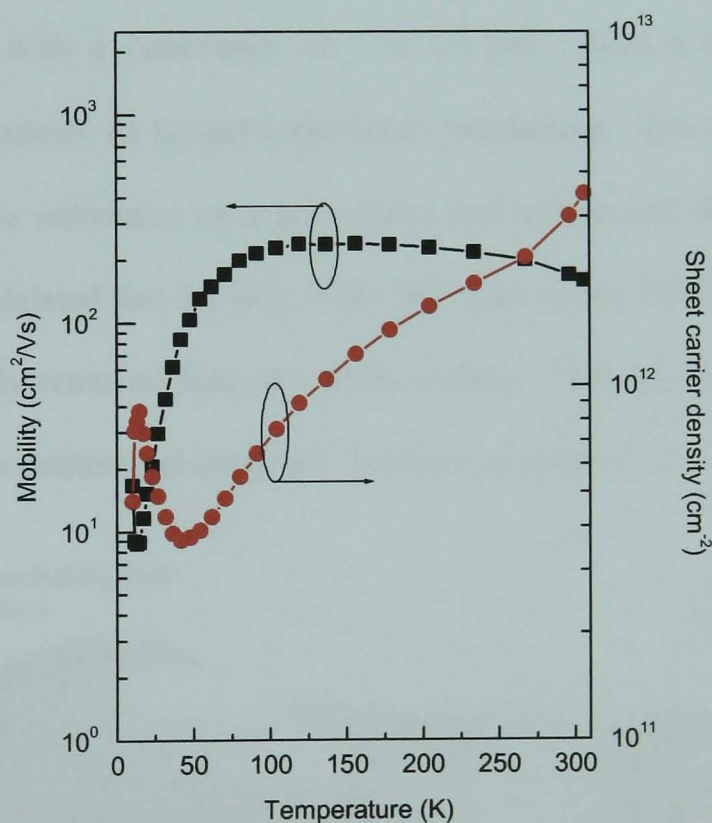
Figure 4.18. Measured as-grown Hall result for sample 65014.

Given the poor result for sample 65014, a second sample (Sample ID: 65052) was grown, this time employing a slightly modified pre-clean to the VS. In this case only RCA stage II was used. After loading the wafer a high temperature *in-situ* flux clean was employed but this time a lower temperature of ~860°C. Following this, the re-grown material was identical to the specification used in sample 65014.

After the wafer was removed from the system, XTEM using the **g**=004 Bragg diffraction vector was performed on the structure to investigate the re-growth interface quality (figure 4.19). Once again the re-growth interface appears to be the nucleation source for large defects within the re-grown heterostructure, although this time there is no evidence of any large scale etching as in the previous sample (65014). A very thin white region is visible at the re-growth interface along with undulations in the re-growth interface morphology with a periodicity of 1 to 1.5 µm. Such a periodicity does correspond to the periodicity of typical cross hatch roughening. The white band seen from the micrograph is indicative of a poor clean and subsequent defect nucleation supports this. It is postulated that the lack of the SC1 part of the RCA clean has led to organics not being fully removed from the wafer surface. Such poor quality material will inevitably lead to a detrimental influence on electrical properties.

Large dislocation nucleating from the re-growth interface

Re-growth interface

200nm
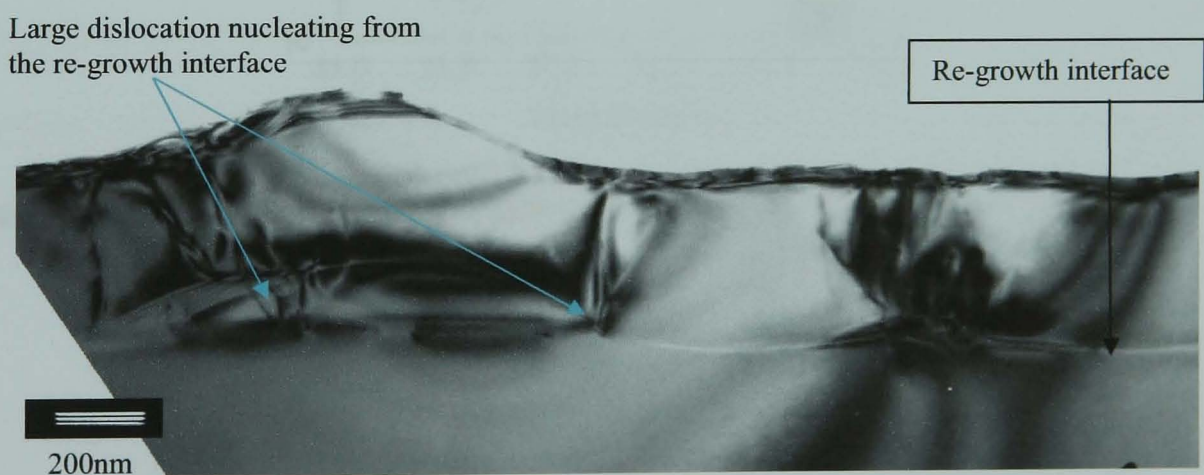
Figure 4.19. XTEM image for sample 65052 depicting the poor re-growth interface quality.

HRXRD measurements were performed on the sample and figure 4.20 depicts the (004) symmetric rocking curves. From the rocking curves, the loss of intensity seen for sample 65014 (figure 4.17b) within the SiGe VS region is not observed, suggesting good lattice matching and confirms the XTEM result that the chemical clean has not etched away a significant amount of material. From (004) symmetric and (115), $(\bar{1}\bar{1}5)$ asymmetric scans, the Ge fraction of the VS was determined to be 70.9% and 99% relaxed. These measured values compared well with the VS's intended parameters.
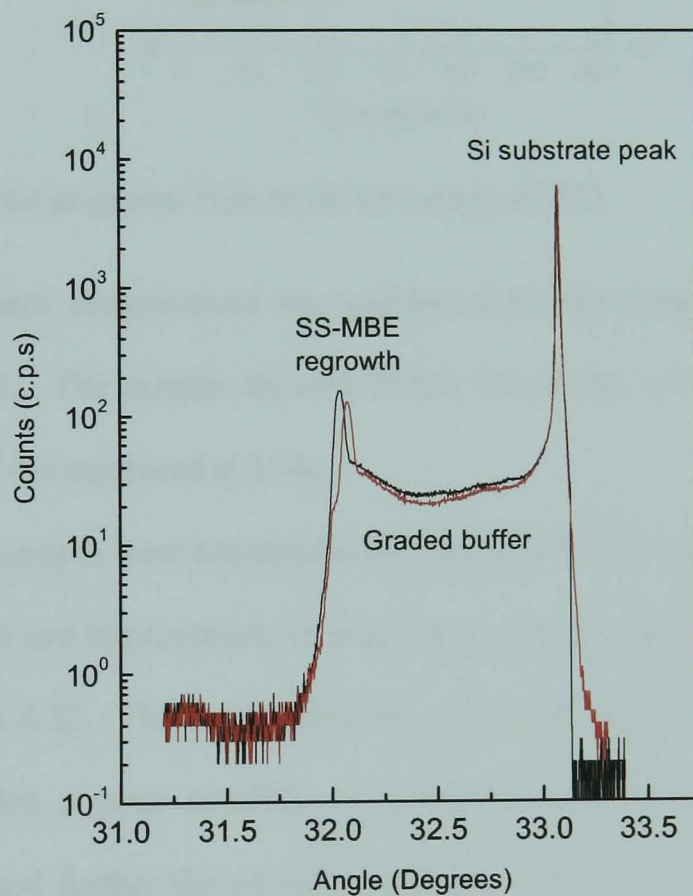
Figure 4.20. (004) Rocking curves for sample 65052.
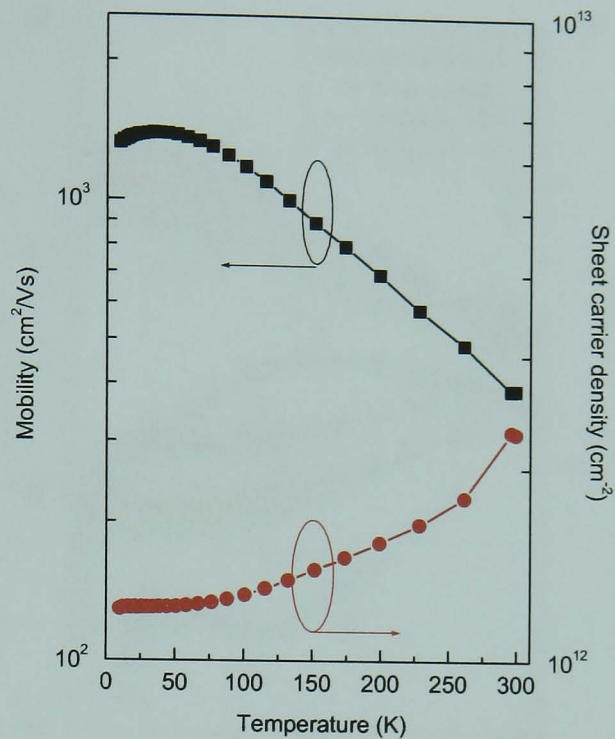
Figure 4.21. Measured as-grown Hall result for sample 65052.

A Van der Pauw measurement was performed on this sample and the result is shown in figure 4.21. The sample showed 2DHG behaviour, with a maximum hole mobility of 1350 cm^2/Vs measured at 35 K.

Pieces of the sample were annealed in the range 600-750°C for 30 minutes under dry N_2 and a factor of two improvement in mobility was observed. The annealed results are shown in figures 4.22. The largest mobility enhancement was found for a 600°C anneal, which yielded a peak mobility of 2800 cm^2/Vs at 10 K. As the anneal temperature was raised further the electrical characteristics began to deteriorate until 2DHG behaviour was lost for a 750°C anneal.
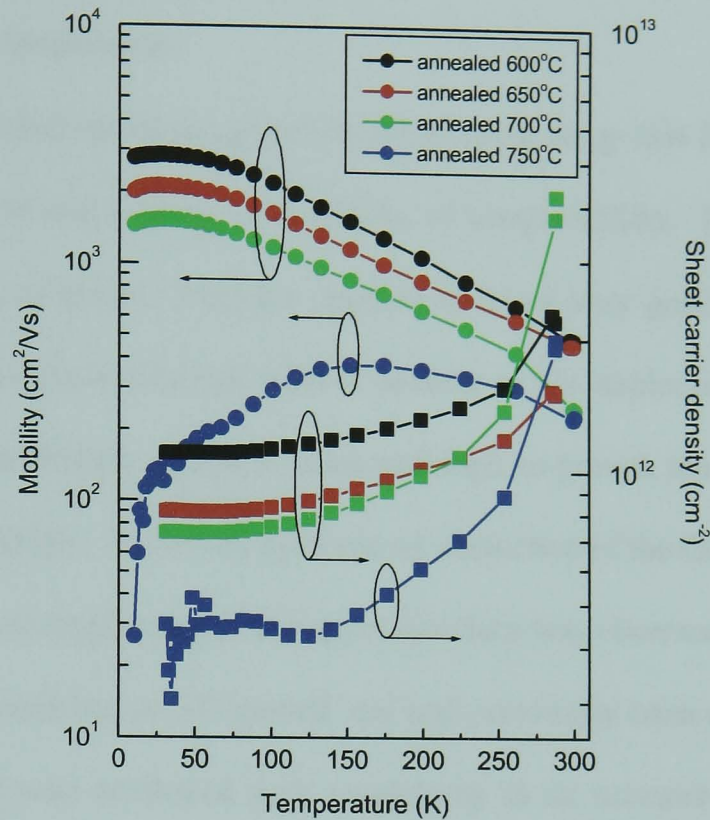
Figure 4.22. Measured Hall results for sample 65052 following a set of different temperature anneals for 30 minutes under dry N_2.

Given that both of the cleaning procedures were not fully effective, a different, less reactive clean was desired. Following private communications with collaborators, a clean using the Piranha etch was decided upon. A UHV-CVD VS underwent the Piranha etch (refer to §3.1.2) prior to being loaded in to growth system. Once into the main growth chamber the wafer was given an *in-situ* desorb by raising the temperature to 860°C for 30 minutes. The growth temperature was then lowered to 770°C and a 200 nm layer of $Si_{0.4}Ge_{0.6}$ was deposited. The aim of the high temperature re-growth was to obtain a high quality lattice matched layer directly on top of the pre-cleaned VS. After the initial 200 nm growth, a 30 minute growth interrupt was employed to allow the wafer to cool to the intended growth temperature (T_G) of 480°C. The heterostructure

(doping layer, spacer layer, Ge channel, cap layer and Si terminating layer) were then deposited at the lower temperature.

XTEM was carried out on the grown structure using the g=004 Bragg diffraction condition. Figure 4.23a and b show micrographs of sample 65105. It is clearly seen (figure 4.23a) that the re-growth interface appears to be of very good quality and no visible signs of dislocation nucleation centres present or Ge depletion/etching. This result indicates that the Piranha chemical clean and high re-growth temperature appear to have worked successfully. However, upon closer inspection of the Ge channel, figure 4.23b, a large amount of roughening of the upper interface was observed. The extent of this roughening was bordering on 3D growth and had previously been observed by Xie *et al* [Xie *et al*, 1993] who attributed such roughening to an excessively high growth temperature.

8 nm Ge Channel

100nm

(a)

CVD-SSMBE interface

Roughening at the
upper interface

8 nm Ge
Channel

(b)

20nm
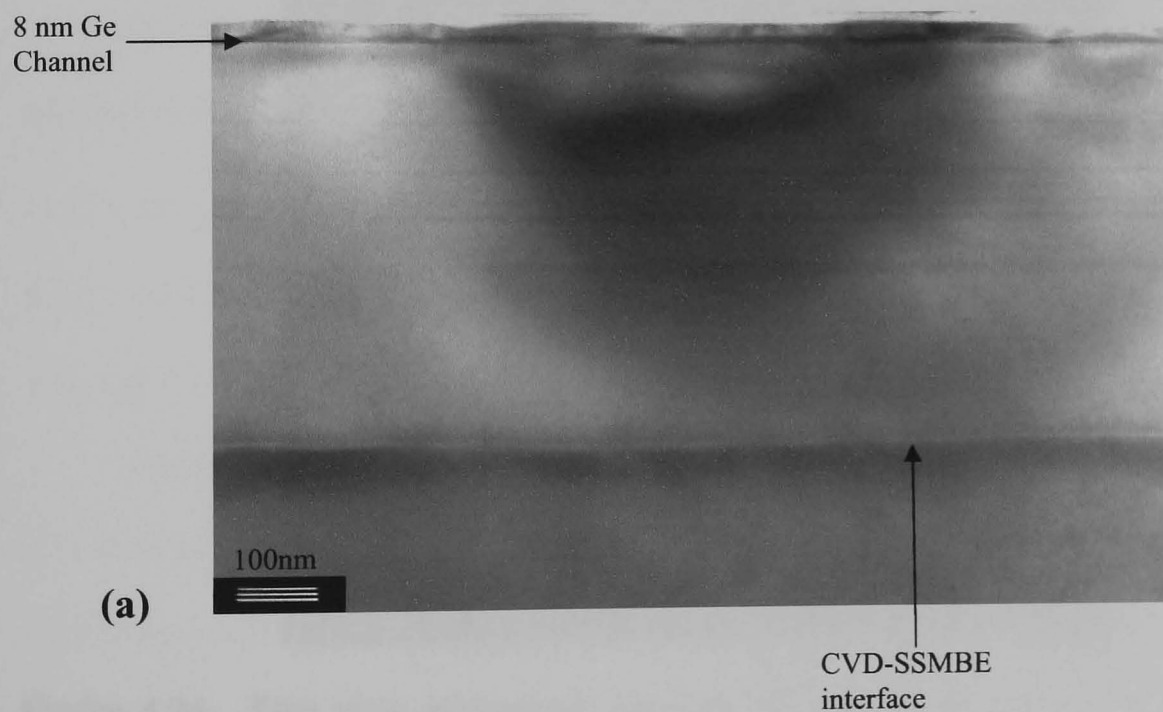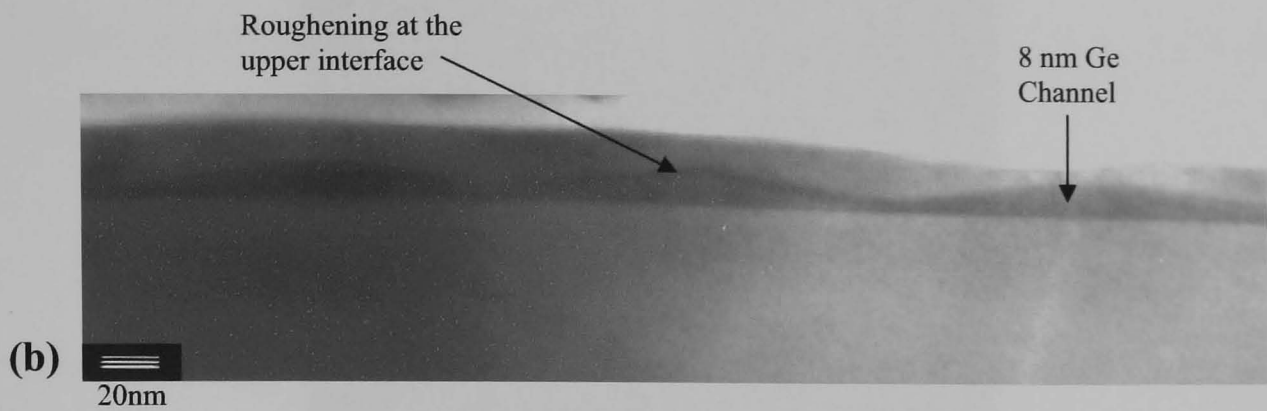
Figure 4.23a & b. XTEM images for sample 65105. Micrograph (a) shows the defect free CVD/SS-MBE re-growth interface while Micrograph (b) shows the large upper interface roughening of the channel arising from too high a growth temperature.

Plan view TEM was performed on sample 65105 and the resulting image is depicted in figure 4.24. From figure 4.24 it is clearly evident that surface morphology consists of short wavelength surface undulations (~100 nm apart) which are attributed to the upper interface roughening of the Ge channel.

100nm
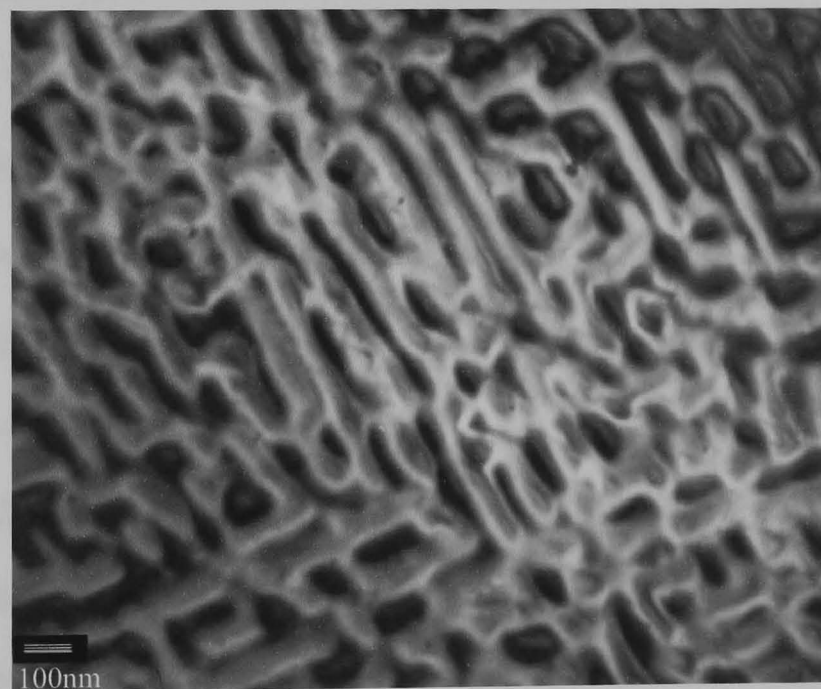
Figure 4.24. Plan view micrograph showing the surface topography of the 8 nm channel sample 65105.

The surface morphology of the as-grown structure (65105) was further investigated by AFM and the profile obtained is given in figure 4.25.
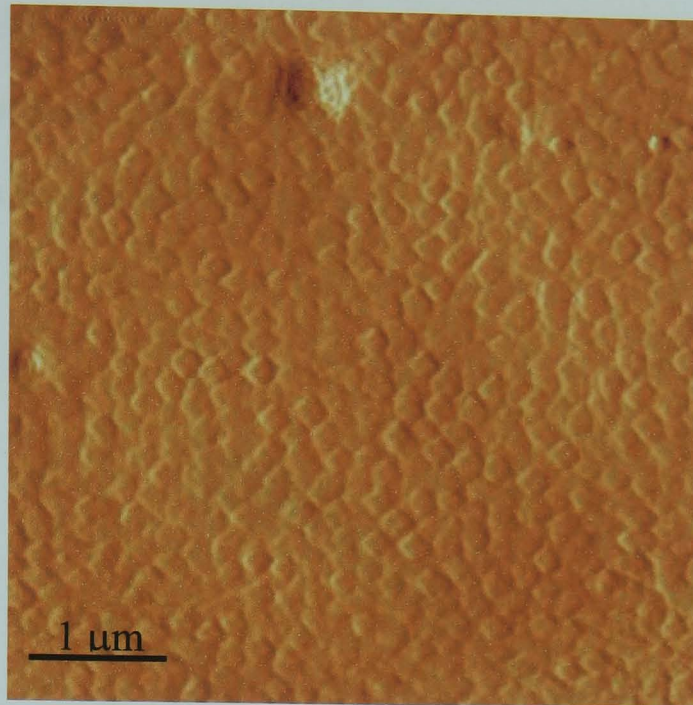
Figure 4.25. AFM image showing the onset of faceting for the 8 nm channel heterostructure 65105. The rms roughness was measured to be ~2 nm.

From figure 4.25 the onset of faceting was observed confirming the growth temperature was too high for this type of heterostructure.

HRXRD measurements indicated that the re-grown Ge fraction was lattice matched to the supplied VS. From two (004) symmetric and two asymmetric (115) and $(\bar{1}\bar{1}5)$ rocking curves, the final Ge fraction of the VS was determined to be 60.8% and 99.3% relaxed. This is in excellent agreement with the 60% Ge composition of the underlying UHV-CVD VS.

Figure 4.26 shows the as-grown and annealed Hall results for sample 65105. Van der Pauw measurements performed on the structure showed 2DHG behaviour, with a significant improvement on the results observed for the identical active heterostructure of sample 65052, which was grown on a non-optimised chemical cleaning procedure. Following anneals within the range 600-700°C for 30 minutes under dry N_2, a slight improvement in the mobility was observed, although for 700°C the sheet carrier density began to fall significantly. The reduction in carrier density may be attributed to boron

out-diffusion from the doping supply layer together with inter-diffusion of the Ge channel and the surrounding $Si_{0.4}Ge_{0.6}$ matrix, thereby leading to a reduction within the valence band offset between the channel and SiGe layer.
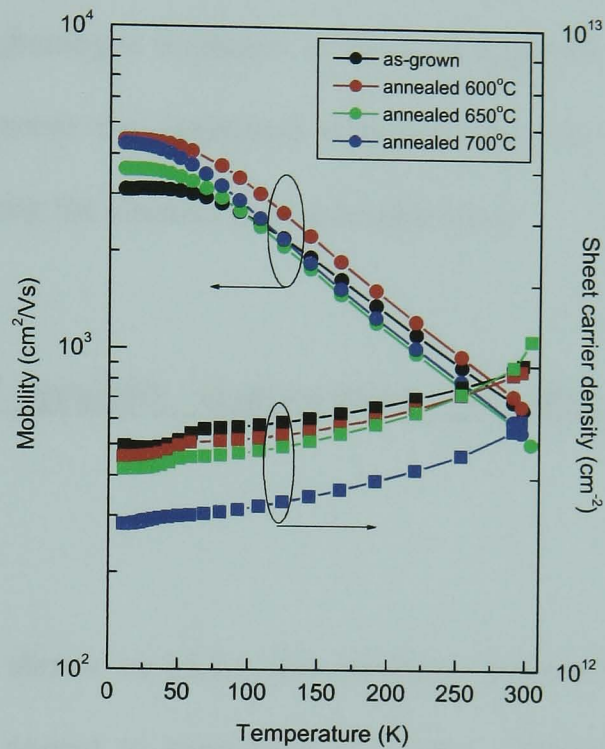
Figure 4.26. As-grown and annealed Hall results for sample 65105. Annealing was performed for 30 minutes under dry N_2.

4.2.2 <u>Summary</u>

A new approach using a hybrid-growth technique combining CVD VS's with the active channel heterostructure being grown using SS-MBE has been demonstrated. Initial cleaning techniques employing RCA stages I and II were found to be too aggressive given the high Ge content within the VS. The re-growth interface was observed to be a nucleation source for dislocations, with the re-grown heterostructure showing poor material quality leading to either no active 2DHG structure or a 2DHG with poor electrical characteristics. A chemical clean using an etch known as the

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"Piranha etch" combined with a high temperature re-growth was found to lead to good quality re-grown material. Given the much improved re-growth interface using the Piranha clean alongside the high temperature re-growth, it was felt that the limiting factor for the structures was the large roughening observed at the upper interface of the Ge channel. As this roughening is indicative of too high a growth temperature, the next logical step was to preserve the optimised chemical pre-clean and high re-growth temperature whilst reducing the channel growth temperature.

4.2.3 Influence of growth temperature on the active channel characteristics.

From the results shown in §4.2.1, the problems associated with cleaning the interface and re-growth appear to have been overcome. However, due to the high re-growth temperature used in order to obtain good quality, low defect material, the lower temperature required for the active layer still appears to be too high, leading to the roughness seen on the Ge channels upper interface. In order to address this problem a series of samples were grown using slight variations in the re-growth method to reduce the active layer growth temperature. As previously mentioned in §4.1, the temperature measurement apparatus, namely the pyrometer, was not suited to measuring temperatures below 450°C. Also, the pyrometer was only calibrated for Si and not SiGe, given that the growth system was typically used to grow thin psuedomorphic SiGe channels, less than 40% Ge composition and of the order of 10 nm in thickness. From the XTEM result for sample 65105 (figure 4.22b) it was now obvious that these structures would have to be grown at a temperature less than 480°C, while it was possible that a growth temperature as low as 300°C may well be required.

Sample ID	Ge channel thickness (nm)	Cooling Profile	Intended growth temperature (°C)
65105	8	Interrupt	480
66046	8	Ramp	480
66048	8	Ramp	400
66050	8	Ramp	300

Table 4.4. Summary of the intended active heterostructure growth temperature and cooling profiles.

A set of three samples (66046, 66048 and 66050) were grown using a slightly different methodology to try and achieve the optimum growth temperature, whereby the Ge channel roughening would be suppressed without lowering the temperature too much and losing epitaxial quality. All the samples underwent the same *ex-situ* and *in-situ* cleaning procedure as sample 65105, followed by 300 nm of $Si_{0.4}Ge_{0.6}$ at a growth temperature of 770°C. Throughout this experiment, only the growth temperature of the active heterostructure was varied. Table 4.4 summarises the intended growth temperatures and cooling profile used for the sample 65105 as well as the set of three samples 66046, 66048 and 66050.

In the case of sample 66046, after the initial 300 nm $Si_{0.4}Ge_{0.6}$, a further 200 nm $Si_{0.4}Ge_{0.6}$ was grown while the temperature was linearly ramped down to the intended growth temperature of 480°C. The idea behind lowering the temperature while continuing to grow was to avoid contamination build up on the surface known to occur if the sample was just left to cool with an interrupt [Kubiak *et al*, 1986]. Figure 4.27 shows a XTEM micrograph of the Ge channel from this structure. From the XTEM it is seen that the Ge channel upper interface has once again roughened, although not to the extent previously observed for sample 65105 (figure 4.22b). Van der Pauw measurements were performed on the as-grown sample and the results are given in

figure 4.28. The sample does not show any mobility improvement compared to the as-grown sample 65105 with a peak mobility 3000 cm^2/Vs being observed at 10 K whilst sample 65105 showed a peak mobility of 3100 cm^2/Vs at the same temperature. Such similarity in the two results indicates that the mobility limiting mechanism is indeed roughness scattering of the Ge channel and not due to the incorporation of contaminants during the growth interrupt.
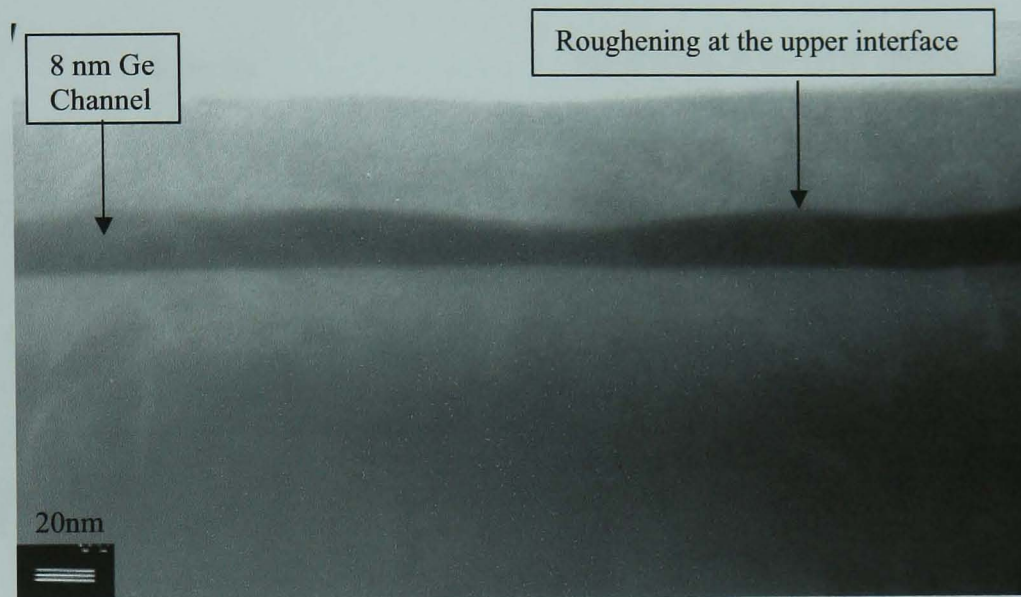
Figure 4.27. XTEM micrograph of sample 66046 showing roughening of the 8 nm channels upper interface.
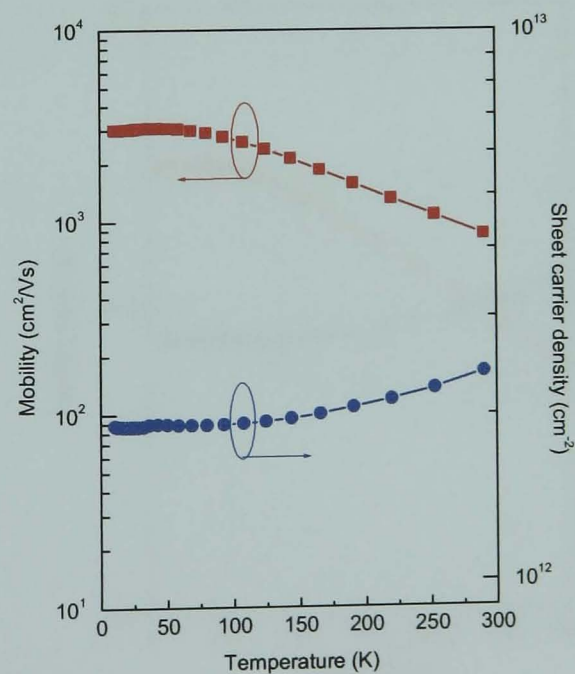
Figure 4.28. Measured as-grown Hall result for sample 66046.

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Sample 66048 differed from 66046 in that after the initial 300 nm of re-grown $Si_{0.4}Ge_{0.6}$, the temperature was lowered over 200 nm from 770°C to an intended temperature of 400°C. Once again the XTEM, given in figure 4.28 shows that the upper Ge channel interface has roughened while the as-grown Hall data given in figure 4.30 shows very similar results to that of sample 66046. This therefore suggests that there was very little difference between the true growth temperatures for these two samples.
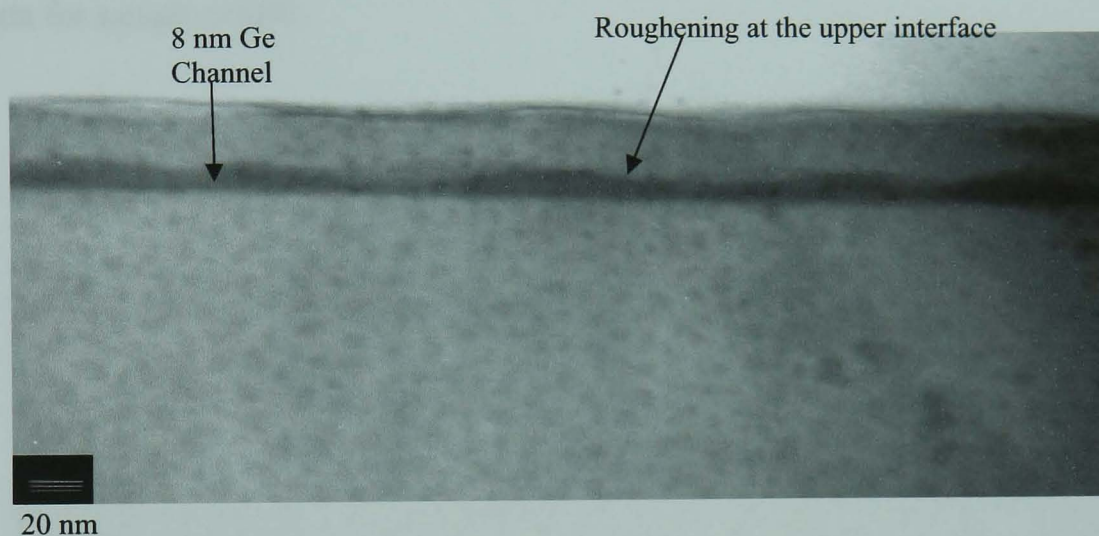
Figure 4.29. XTEM micrograph of sample 66048 depicting the 8 nm channels upper interface roughening.
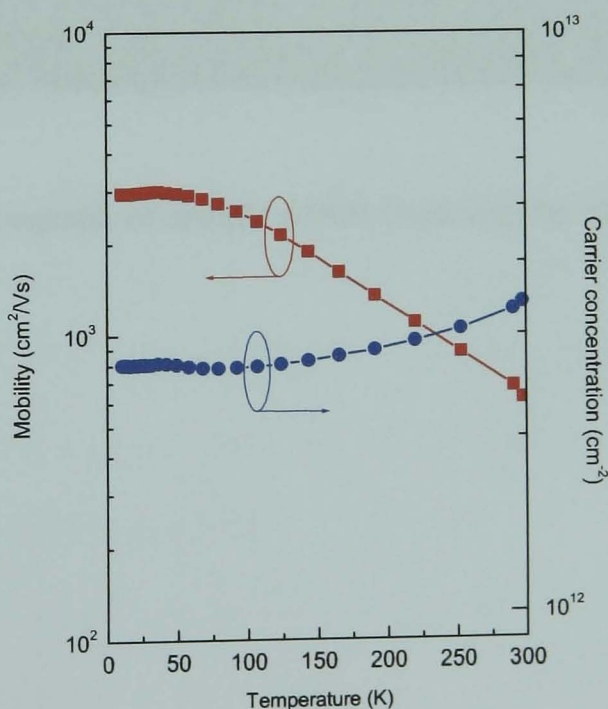
Figure 4.30. Measured as-grown Hall result for sample 66048.

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Finally, sample 66050 was grown using a similar growth specification to 66048 except the intended growth temperature of the Ge confinement channel was 300°C. It was again found that the Ge channel upper interface appeared to have roughened although slightly less than the previous samples suggesting some progress had been made. However, the Hall results were found to be identical to the previous two samples. Figure 4.31 shows the XTEM micrograph whilst figure 4.32 the as-grown Hall data for sample 66050.
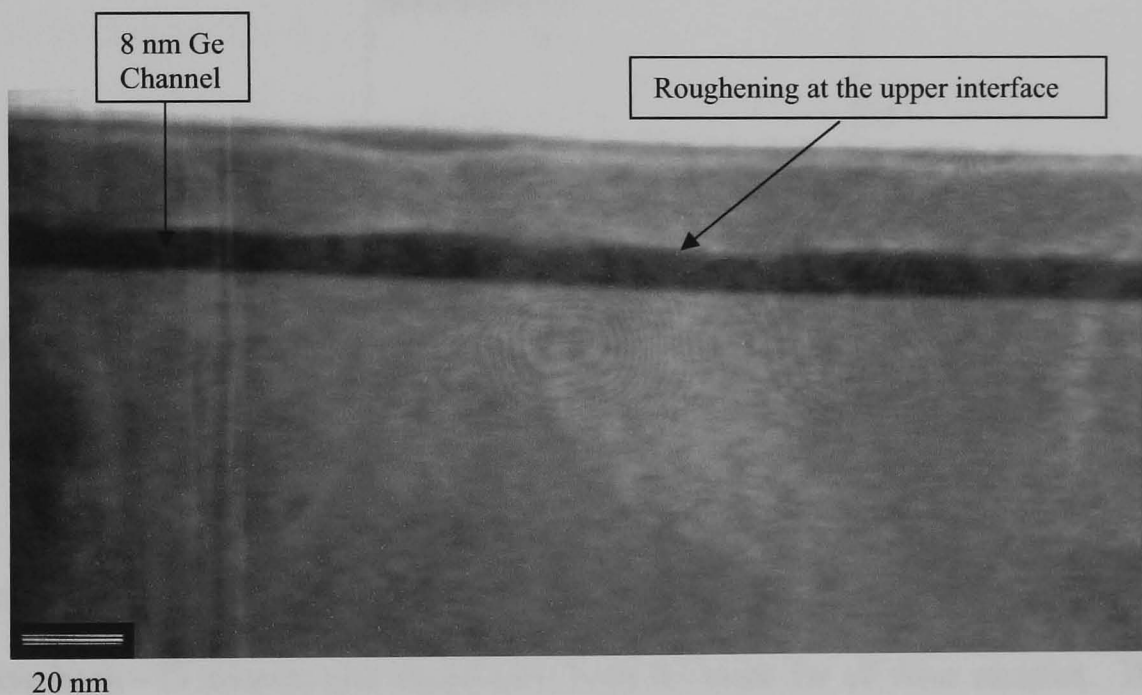
Figure 4.31. XTEM micrograph of sample 66050 depicting the slight upper interface roughening.
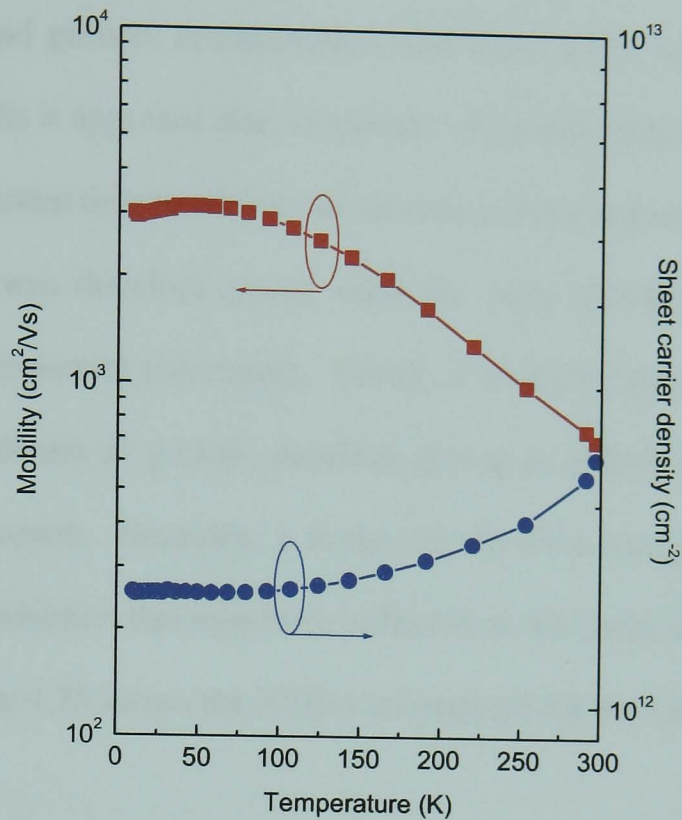
Figure 4.32. Measured as-grown Hall result for sample 66050.

Given that a growth rate of ~1 Ås^{-1} was used, then the time between the high temperature (770°C) SiGe re-growth and the lower temperature heterostructure growth will have been ~33 minutes and would have been the same for all three samples. This arises from the fact that the cooling time of the wafer was governed by the growth of 200 nm at ~1Ås^{-1}. From the similarity between the XTEM micrographs for all three structures (66046, 66048 and 66050) and the Hall results, this suggests that the intended growth temperatures of the samples was not met, but a common temperature based on 33 minutes of cooling was obtained instead.

Having made little progress in reducing the Ge channel roughening by varying the growth method, it was decided that a growth interrupt after the initial 500 nm of re-growth, but prior to the heterostructure would be employed. Growth interrupts can

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lead to a build up of contamination [Kubiak *et al*, 1986]. By employing a combination of temperature ramp and growth, contamination was hoped to be spread over a wide area, but from the results it appeared that 30 minutes of growth while cooling appeared not to have been a sufficient time to achieve the desired growth temperature.

Sample 68073 was therefore grown using the same growth specifications as 66050 except for two important parameters. Firstly, a 30 minute growth interrupt was used after the initial 500 nm of growth, therefore giving an effective cooling time of ~1hr after starting re-growth. Secondly, a further 20 nm SiGe was grown in order to bury any surface contamination that may have collected on the wafer surface during the growth interrupt. Figure 4.33 shows the XTEM micrograph for the 8 nm Ge channel of sample 68073.

Figure 4.33. XTEM micrograph of sample 68073 showing the suppression of the upper channel roughness.

From this micrograph it is very clear that the upper interface for 68073 is much smoother than observed for any of the previous structures. This suggests that the new growth method incorporating the growth interrupt had the desired effect of reducing the growth temperature. Figure 4.34 shows the surface morphology of the as-grown sample 68073 from which it is seen that the faceting observed for an identical structure (figure 4.25) grown at a higher temperature had been suppressed.
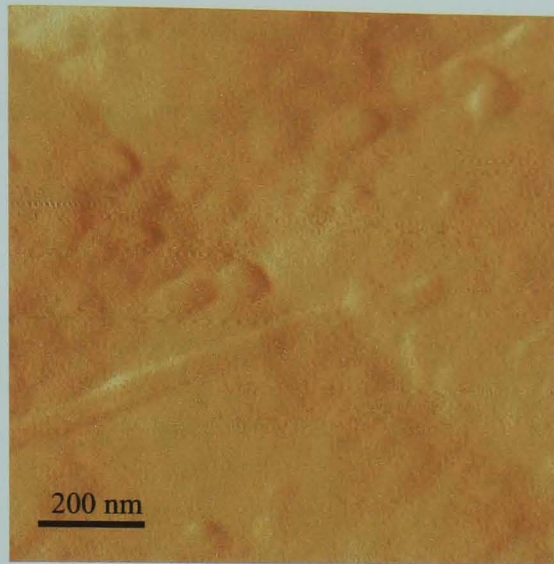
Figure 4.34. AFM image showing the surface of the as-grown 8 nm channel heterostructure 68073. The rms roughness was measured to be 1.5 nm.

Figure 4.35 shows the measured mobility and carrier density as a function of temperature for sample 68073. The as-grown Hall results for 68073 show a significant improvement on the previous samples with a peak mobility of 7260 cm^2/Vs at 10 K, compared to a maximum value of 3100 cm^2/Vs. This suggests that the upper interface roughening was the major contributing factor limiting the mobility of the previous samples.
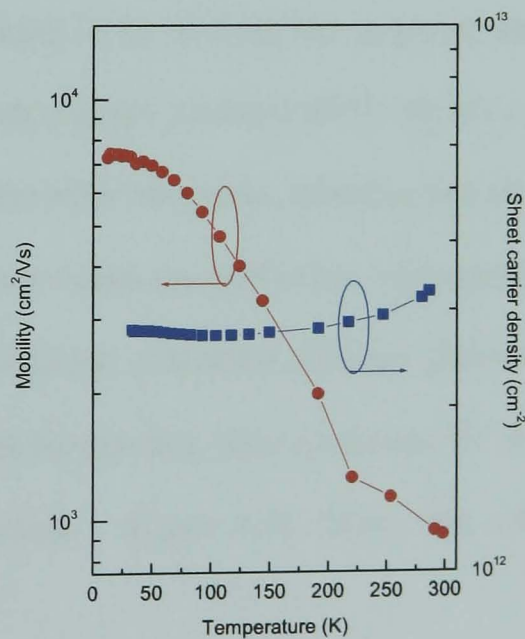
Figure 4.35. Measured Hall result for the as-grown sample 68073.

Table 4.5 shows a summary of the room temperature and low temperature mobilities for the 8 nm channel structures grown using varying growth techniques to suppress the upper interface roughening.

Sample	Room temperature mobility (cm^2/Vs)	Low temperature ($\sim$10 K) mobility (cm^2/Vs)
65105	650	3000
66046	850	3100
66048	650	2900
66050	700	3100
68073	900	7300

Table 4.5. Summary of room and 10 K temperature mobility for the 8 nm channel structures grown using different cooling procedures prior to the channel growth.

From these results the room temperature mobilities are found to be similar suggesting that there is a common limiting mechanism at this temperature. Optical phonon scattering was identified to be the more dominant scattering mechanism at room temperature in Ge heterostructures [Madhavi et al, 2001], and it may be assumed that this will be a strong contributing factor limiting the as-grown samples here. However, at low temperature the smooth channel structure 68073 shows a mobility enhancement of more than double that of the other structures, inferring that the rough upper interface was the limiting factor for the previous samples at low temperature.

The 1D Poisson/Schrödinger simulation package [Snieder] was used to model the bandstructure, carrier distribution and wave functions for the holes in the present 8 nm Ge channel heterostucture. Figure 4.36 shows the schematic layout of the heterostructure modelled.

| 2 nm Si |
| 20 nm $Si_{0.4}Ge_{0.6}$ |
| 8 nm Ge Channel |
| 15 nm $Si_{0.4}Ge_{0.6}$ |
| 5 nm $Si_{0.4}Ge_{0.6}$, 2×10^{18} cm^{-3} B |
| 20 nm $Si_{0.4}Ge_{0.6}$ with T_G=350 °C |
| 200 nm $Si_{0.4}Ge_{0.6}$ with T_G=800 °C |
| 7 μm $Si_{0.4}Ge_{0.6}$ Buffer as supplied |

Growth interrupt →

← 860 °C in-situ desorb
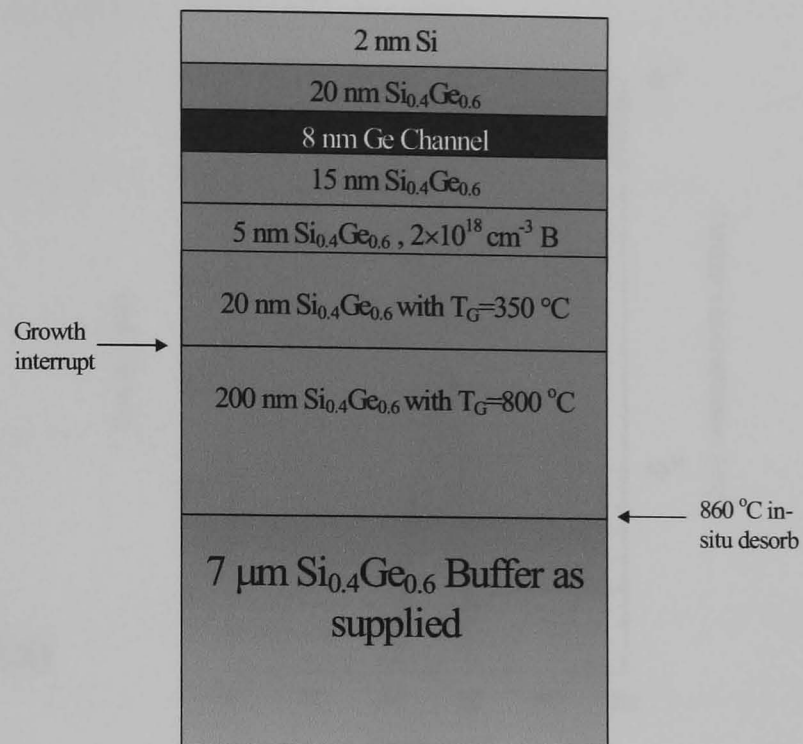
Figure 4.36. Schematic layout for the complete structure of sample 68073.

Figure 4.37a shows the modelled bandstructure and carrier distribution behaviour for the 8 nm Ge channel structure while figure 4.37b demonstrates where the Heavy Hole (HH_1) wave function lies within the channel. Only the HH_1 wave function is given, since it forms the minimum energy level of the system and will be populated by the majority of charge carriers confined within the potential well.
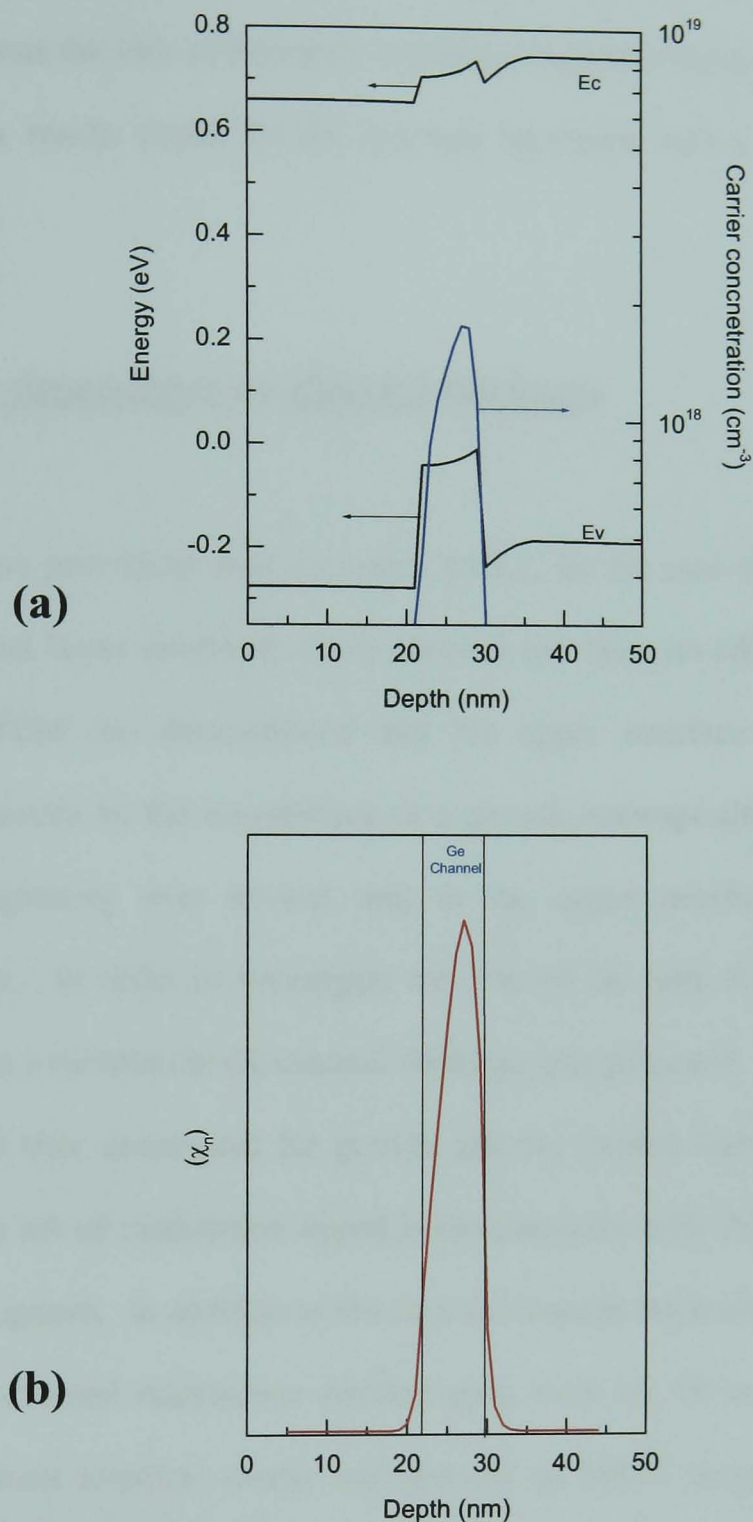
Figure 4.37a & b. 1D Poisson/Schrödinger simulations for the intended 8 nm channel structure. (a) Shows the bandstructure and carrier distribution while (b) the Heavy Hole (HH$_1$) wave function.

It is clear from figure 4.37b that the wave function lies almost symmetrically within the channel, insinuating both the upper and lower interfaces will have a similar

amount of influence on the carriers in the channel. This modelled wave function behaviour re-affirms the idea of the upper interface roughness being a limiting factor in the Hall mobility results found for the previous structures with a very rough upper channel interface.

4.2.4 Mobility dependence on channel thickness

As we have previously seen in section §4.3.2, for the case of an 8 nm channel, both the upper and lower interfaces of the channel will have an effect on the carriers. Additionally, XTEM has demonstrated that the upper interface quality has been significantly improved by the introduction of a growth interrupt although microscopic roughening (roughening over several nm) at the upper interface would have a detrimental effect. In order to investigate the role of the both the upper and lower channel interfaces a variation in Ge channel thickness was proposed.

Given the time constraints for growth and the limited number of UHV-CVD VS's available, a set of modulation doped heterostructures with differing Ge channel thicknesses were grown. In addition to the 8nm Ge channel thickness of sample 68073, the intended Ge channel thicknesses decided upon were 16, 20 and 30 nm. All the structures underwent identical cleans and growths as 68073 except for the varying channel thickness. The sample ID's and respective channel thicknesses are:

68073 (8nm channel)

68072 (16 nm channel)

68075 (20 nm channel)

68076 (30 nm channel)

All the samples were analysed by XTEM using the **g**=004 Bragg diffraction vector. Figure 4.38a-c shows the XTEM micrographs for samples 68072, 68075 and 68076.

(a. 16 nm channel)

16 nm germanium channel

Upper interface roughening

20nm

(b. 20 nm channel)

20 nm Ge channel

Upper interface roughening

20nm

(c. 30 nm channel)

30 nm Ge channel

Upper interface roughening

20nm
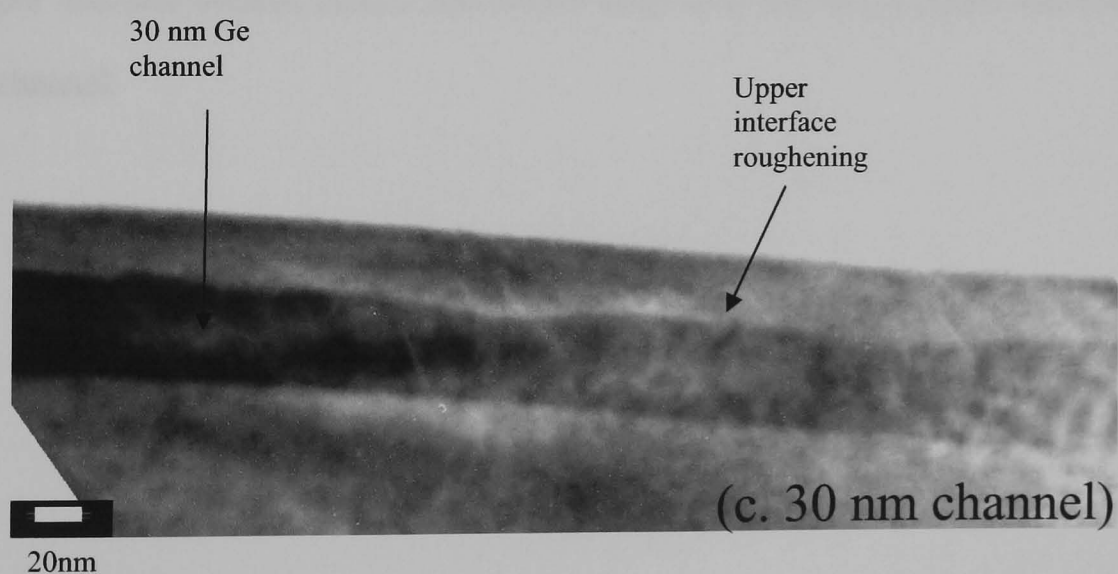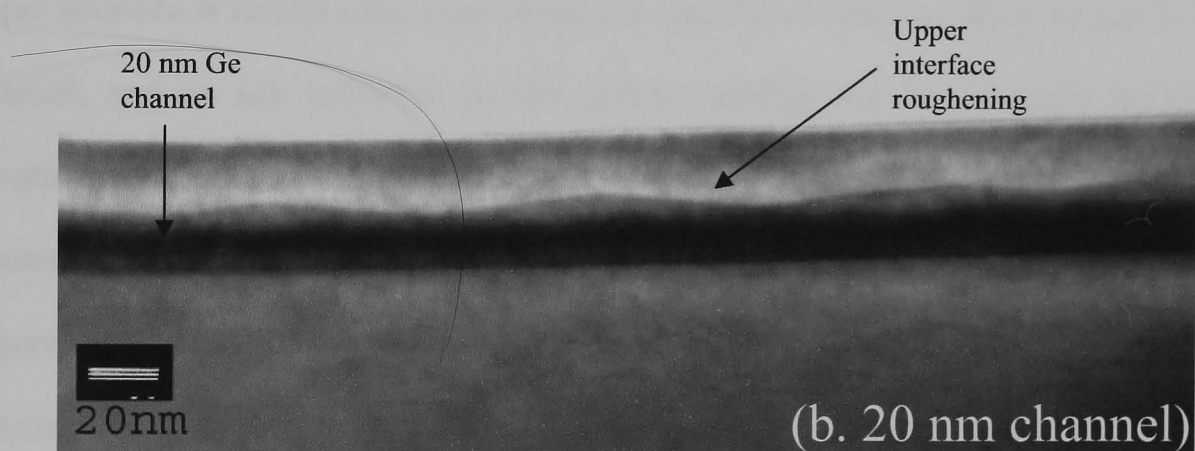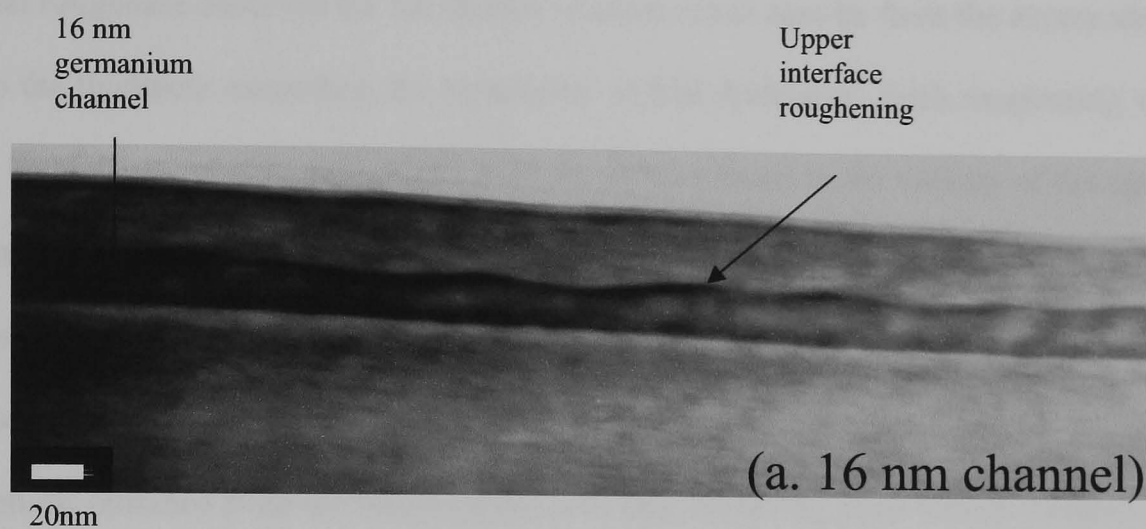
Figure 4.38. XTEM micrographs for samples (a) 68072, (b) 68075 and (c) 68076. The upper interface of all three channels is seen to roughen under the strain.

It is clearly seen for all three structures that the upper interface has roughened compared to the 8 nm channel structure of figure 4.33. Given the smoothness observed for the upper interface of the 8 nm structure using the growth interrupt, the upper channel roughness observed for the thicker channels must now be from the excess strain due to the thickness exceeding the metastable critical thickness. Such roughening will cause local strain relaxation and lead to strain fields present in the vicinity of the upper interface. In order to see how much effect the upper interface would have on the carriers, the 16, 20 and 30 nm structures were modelled using the 1D Poisson/Schrödinger package. The carrier distribution and wave function predictions obtained from the simulations show that, by having such a thick channel, the upper interface is further away from where the majority of carriers will be located in the channel, and so any influence on the carrier mobility due to the upper interface roughness, should be significantly reduced. Figure 4.39a shows the intended 16 nm Ge channel 1D Poisson/Schrödinger modelled bandstructure and carrier distribution while Figure 4.39b the HH_1 wave function. Modelling of the 20 nm and 30 nm channel structures showed a similar result to the 16 nm structure, with the notable exception that the upper interface became further and further away from the actual carrier distribution in the channel.
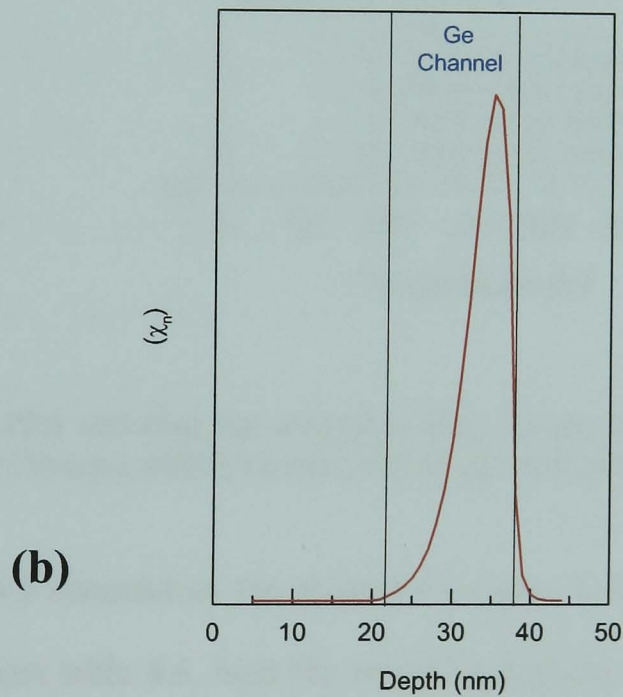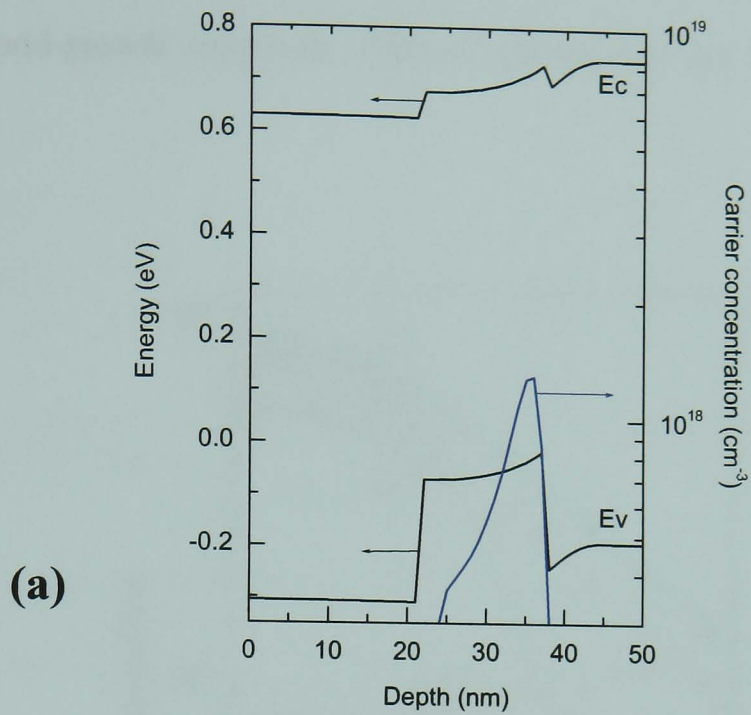
Figure 4.39a & b. 1D Poisson/Schrödinger simulations for the intended 16nm channel structure. (a) Shows the bandstructure and carrier distribution while (b) the Heavy Hole (HH₁) wave function.

The as-grown Hall mobility and carrier sheet density for 68072, 68073, 68075 and 68076 from room temperature down to 10 K are shown in figure 4.40. The results

all show a significant mobility improvement at 10 K (7260 – 8680 cm²/Vs) compared to the early hybrid-growth structures (2900 – 3100 cm²/Vs) not including the growth interrupts.
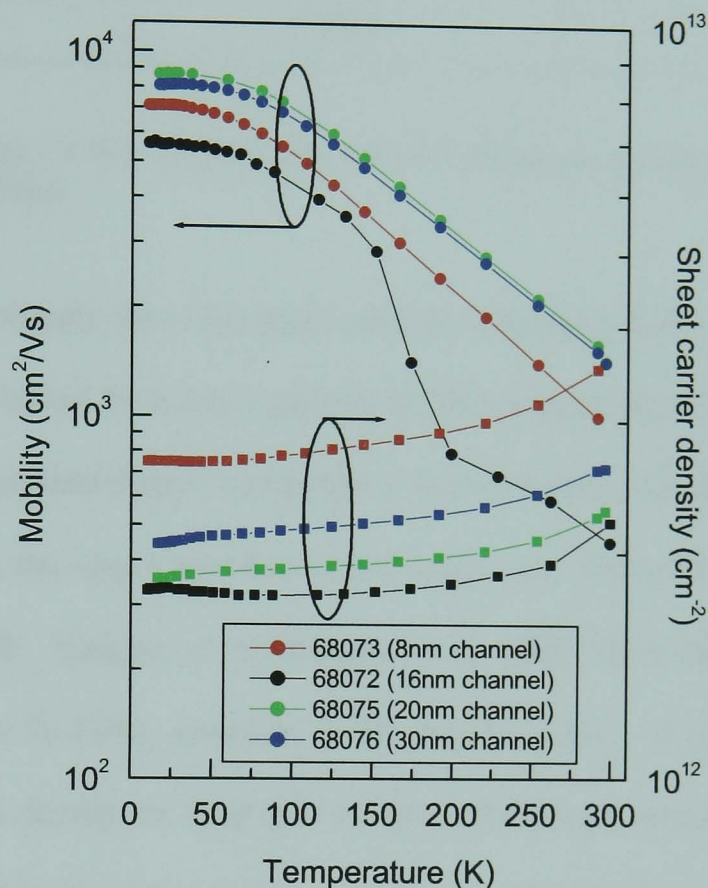
Figure 4.40. Plot showing the as-grown Hall results from 300 K down to 10 K for samples 68072 (16 nm), 68073 (8 nm), 68075 (20 nm) and 68076 (30 nm).

Table 4.6 summarises the as-grown samples 10 K and room temperature Hall mobilities. From table 4.6, both the room temperature and 10K mobility appears to improve slightly with increasing the channel thickness from 8 nm up to 20 nm. However the variation observed is not overly significant which suggests that there may be a common factor limiting the mobility of the samples.

Ge Channel thickness (nm)	Room Temperature as-grown mobility (cm^2/Vs)	10K as-grown mobility (cm^2/Vs)
8	920	7260
16	1010	7130
20	1440	8680
30	1430	8080

Table 4.6. Summary of the varying Ge channel thickness structures 300 and 10 K as-grown Hall mobilities.

As we have already seen, the upper interface roughness had been suppressed in the 8 nm channel structure by using a growth method incorporating a growth interrupt, and from 1D Poisson/Schrödinger modelling it was found that for the thicker channel structures (>16 nm), the upper interface would have very little effect, so long as the roughness was small. Knights *et al* [Knights *et al*, 2001] have shown that for low growth temperatures in SiGe, grown-in point defects occur. If point defects were present in sufficient density to limit the electrical behaviour, annealing the samples should lead to a reduction in the number present, resulting in an enhancement in the mobility. Anneals for 30 minutes within the temperature range of 600-700°C were performed under dry N_2. Figures 4.41a-d show the Hall results for the four samples (68072, 68073, 68075 and 68076) after annealing.

(a). 8 nm channel

(b). 16 nm channel

(c). 20 nm channel

(d). 30 nm channel
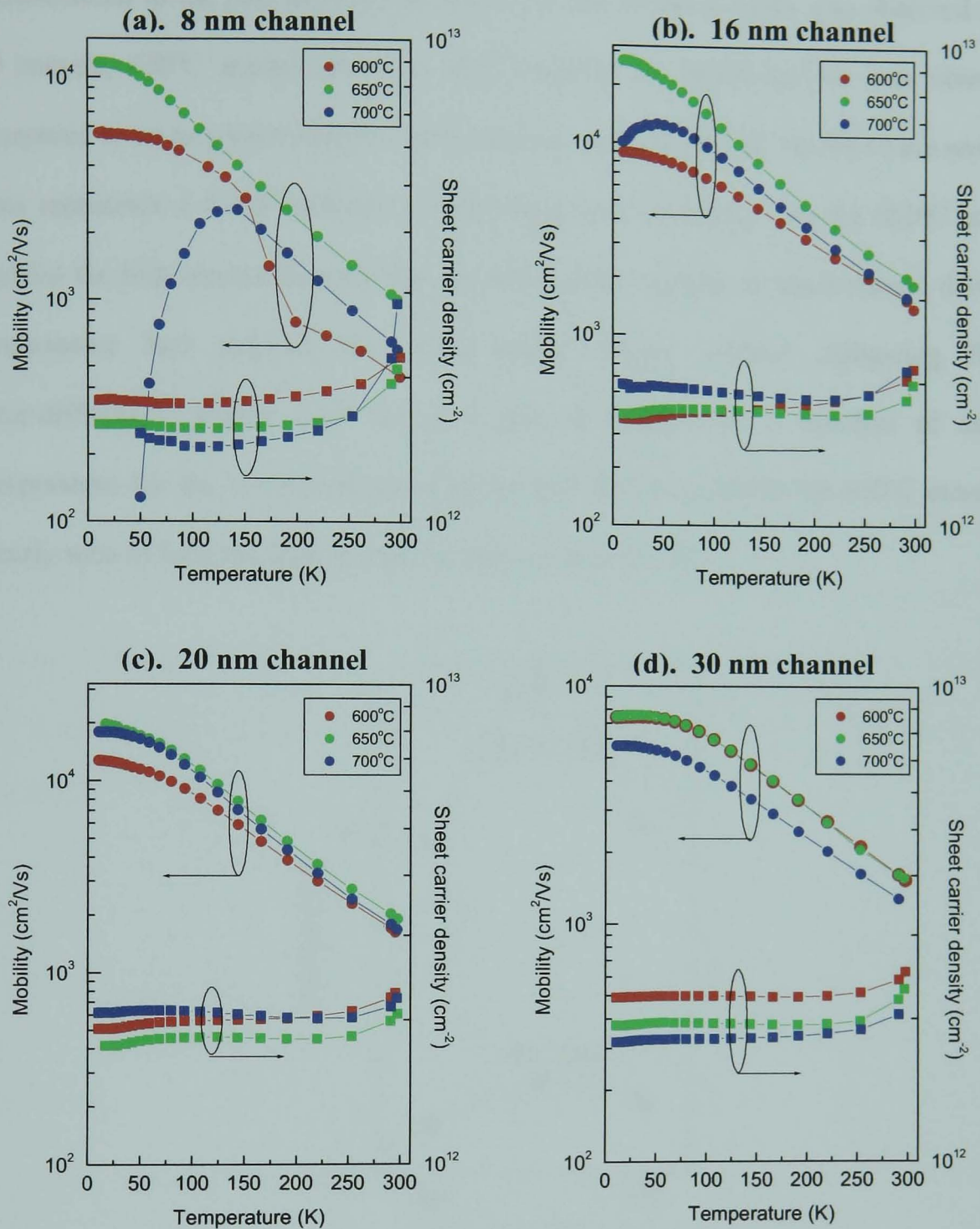
Figure 4.41. Plots showing the Hall results for samples 68073 (8nm), 68072 (16nm), 68075 (20nm), and 68076 (30nm) after annealing at different temperatures for 30 minutes under dry N_2.

From the annealing results, significant improvements in the Hall mobility was observed for the 8, 16 and 20 nm channel structures. For the 8, 16 and 20 nm samples, a 600°C anneal for 30 minutes led to some improvement in the samples mobility whilst a 700°C anneal for 30 minutes under dry N_2 had a detrimental effect. The largest

enhancement in the Hall mobility for the 8, 16 and 20 nm samples was observed for a 30 minute, 650°C anneal where a 10 K mobility of 26,900 cm²/Vs was observed compared to an as-grown mobility 10 K mobility of 7130 cm²/Vs for the 16 nm sample. This represents a 4 fold mobility improvement with annealing. As the 650°C anneal yielded the best electrical properties for three of the samples it was believed that this temperature had reduced the point defect density without instigating Si-Ge inter-diffusion. Figure 4.42 shows a plot of mobility as a function of anneal temperature for the 16 nm channel structure (68072) from which the 650°C anneal is clearly seen to have the largest enhancement on the mobility.
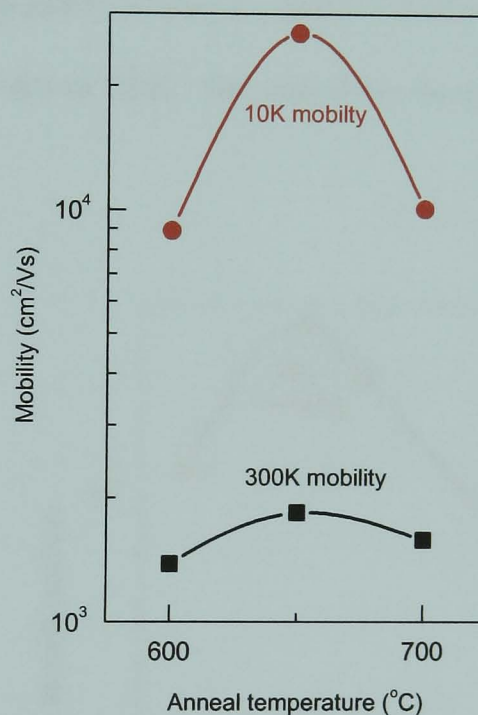
Figure 4.42. Plot of mobility as a function of anneal temperature for the 16 nm channel sample (68072).

In the case of the 30 nm channel structure, no improvement with annealing was observed suggesting that other factors were coming into play with the thicker channel. Table 4.7 summarises the 10 K and room temperature Hall mobilities and sheet carrier density for the annealed structures.

Ge Channel thickness (nm)	Room Temperature mobility (cm^2/Vs)	10K mobility (cm^2/Vs)
8	1010	11600
16	1840	26900
20	1910	19900
30	1560	7480

Table 4.7. Summary of the varying Ge channel thickness structures 300 and 10 K Hall mobilities after undergoing a 650°C anneal under dry nitrogen.

Figure 4.43 is a plot showing the four samples 10 K and 300 K mobilities as a function of channel thickness. As can be seen from this plot, there appears to be an enhancement in sample mobility as the Ge channel thickness increases up to ~20 nm at room temperature and 16 nm at 10 K. Beyond these thicknesses, the mobility begins to decrease.
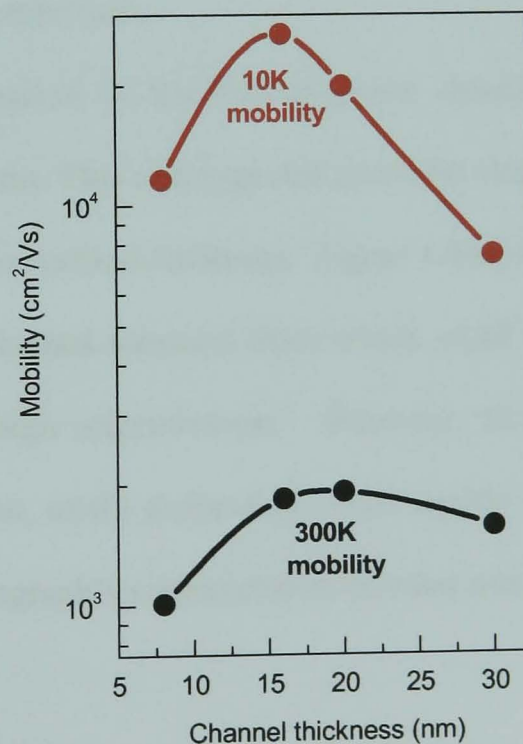
Figure 4.43. Plot showing the 10 K and room temperature mobilities as a fuction of channel thickness.

Ismail *et al* [Ismail *et al*, 1994] found that for pure Si channels grown on a relaxed $Si_{1-x}Ge_x$ (x=0.25-0.34) VS's (in excess of the Matthews Blakeslee critical thickness), misfit dislocations formed at the SiGe/Si interface. From Raman measurements they found that the Si channel had relaxed by less than 2%. Such a small amount of relaxation could not account for the large decrease in mobility they observed with increasing channel thickness. However, they did find an increase in misfit dislocation segment density with increasing channel thickness, from which they attributed the higher number of misfits as the dominant limiting effect at low temperature.

For the present structures, investigation needed to be performed in order to see whether lattice effects such as misfit dislocations were present and a possible limiting mechanism on the low temperature mobility. In order to determine if there was a correlation between misfit dislocations and the channel thickness, plan view cross sectional microscopy was performed.

Plan view TEM analysis of the 8nm as-grown channel structure indicated no observable misfit dislocations. This was expected given the structure was designed to be grown below the equilibrium critical thickness. Figure 4.44a shows the plan view TEM micrograph of the 8 nm channel structure from which small surface features are just visible when viewed at high magnification. However, for the 16, 20 and 30 nm as-grown channel structures, misfit dislocations were readily observed. Figures 4.44b & c show plan view micrograph's representative of what was observed for the 20 and 30 nm structures.

20 nm

(a). 8 nm channel structure

500 nm

(b). 20 nm channel structure

500 nm

(c). 30 nm channel structure
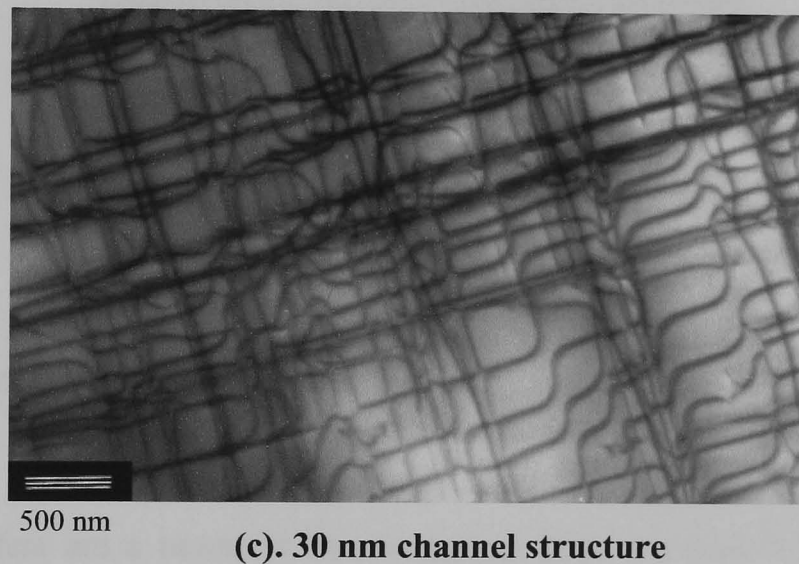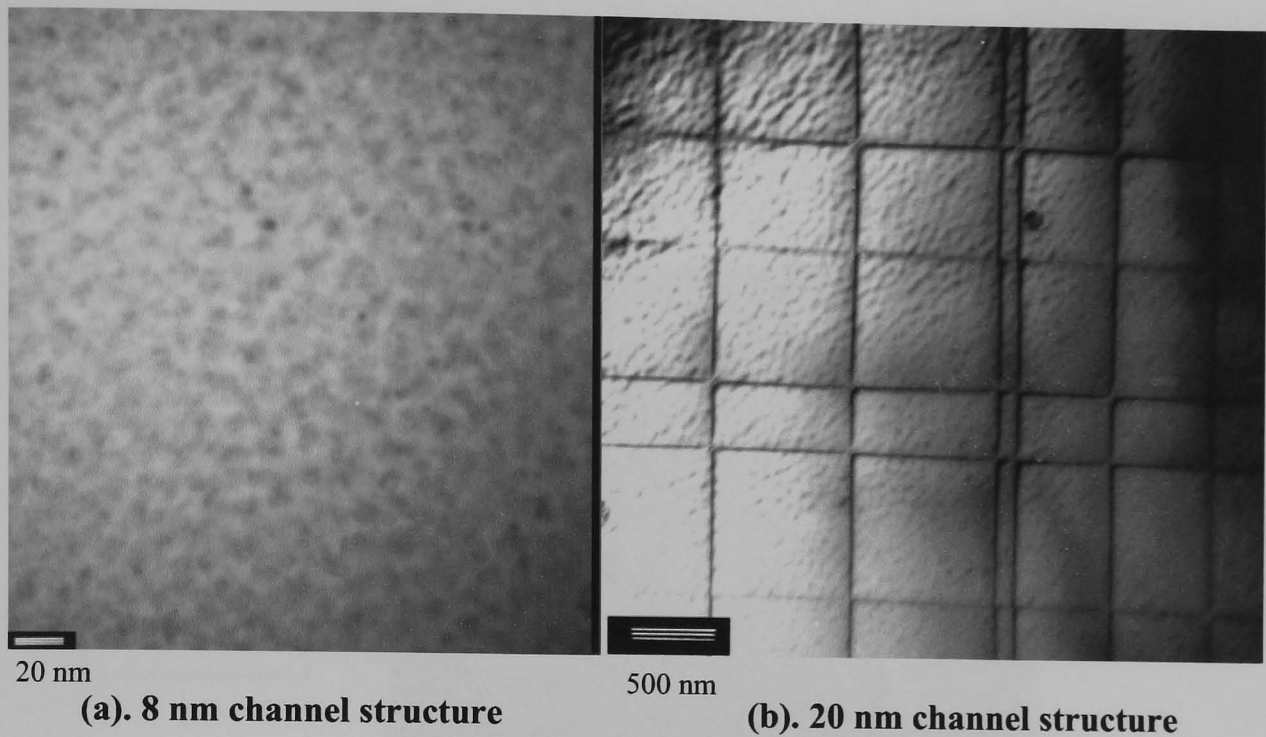
Figure 4.44. Plan view micrographs taken using the **g**=220 Bragg diffraction vector showing the surface morphology of the (a) 8 nm as-grown sample 68073 and (b) the misfit dislocations present within the as-grown 20 nm sample 68075 and (c) the 30 nm sample 68076.

In the case of the 16 nm channel structure the plan view TEM surprisingly revealed that the starting VS was an off-cut substrate. Figure 4.45 shows the plan view micrograph for sample 68072 (16 nm channel structure). From this micrograph it can be seen that the misfit dislocations do not run orthogonal to each other, but glide along

the off-cut angle leading to the misfits either diverging or converging towards each other.

Misfit dislocations

Surface morphology

500nm
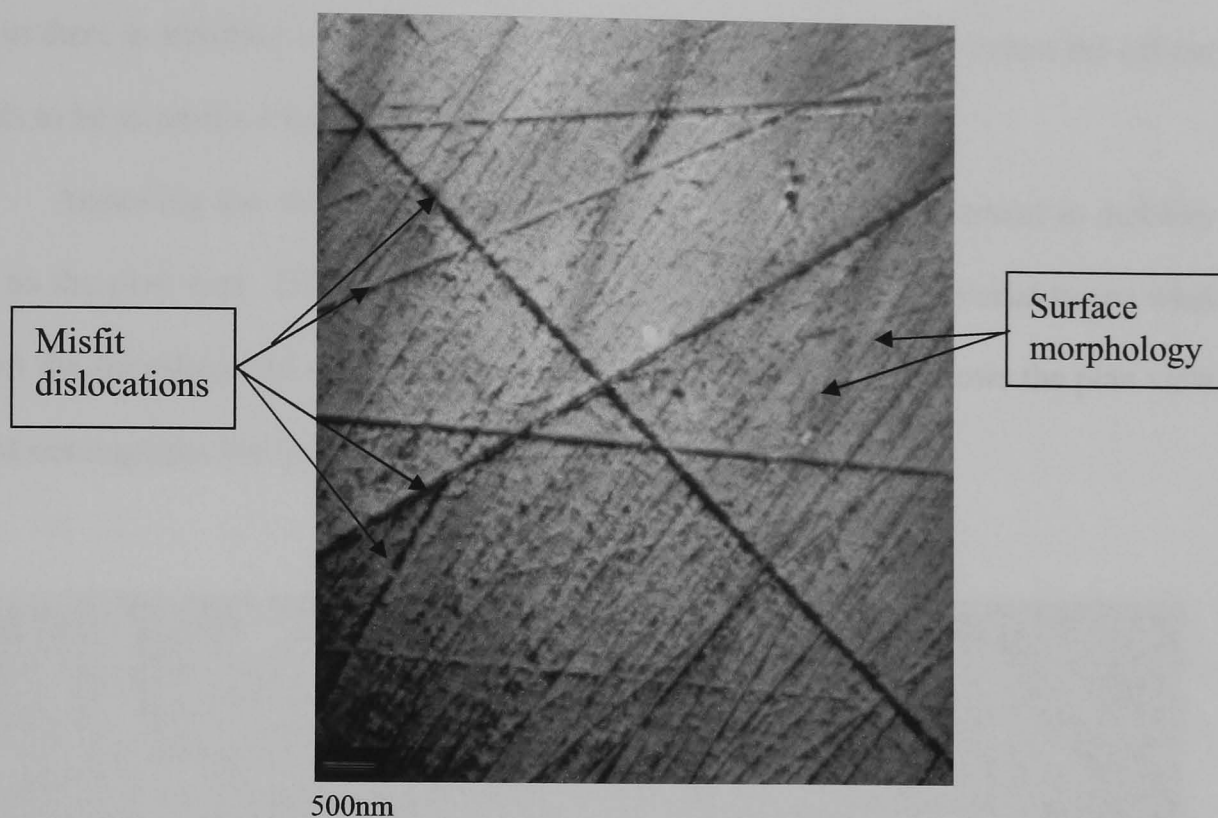
Figure 4.45. Plan view micrograph of the as-grown 16 nm sample (68072) indicating the structures surface texture and showing the lower channel interface misfit dislocations.

Off-cut wafers are a necessity for integrating III-V materials with group IV materials. It was not the author's intention to use an off-cut VS, but no indication of such was given when the VS's were supplied. The main difference between an off-cut VS with respect to an on-axis VS is the dislocation blocking mechanisms that take place during growth. Off-cut VS have been found to lead to less threading dislocations, non-parallel misfit dislocations very much like those shown in figure 4.45 and a smoother surface morphology. To the best of the authors knowledge there is no published data to suggest that the off-cut wafer will have any detrimental/enhancing effects on the types of structures used for this work. The major difference is in the

dislocation relaxation kinetics of the relaxed VS and does not affect the electrical characteristics of the strained Ge channel. It may however be an interesting experiment for further work to obtain a set of varying off-cut VS's and grow identical structures to see in there is anything to gain by using an off-cut wafer and to what extent the off-cut needs to be to produce the best result.

Annealing the samples had been shown to lead to an improvement in mobility and so the plan view TEM was performed on the 650°C annealed material to see what effect the annealing had on the misfit dislocations. Figure 4.46a-d shows the plan view TEM micrographs for the 8, 16, 20 and 30 nm annealed structures.
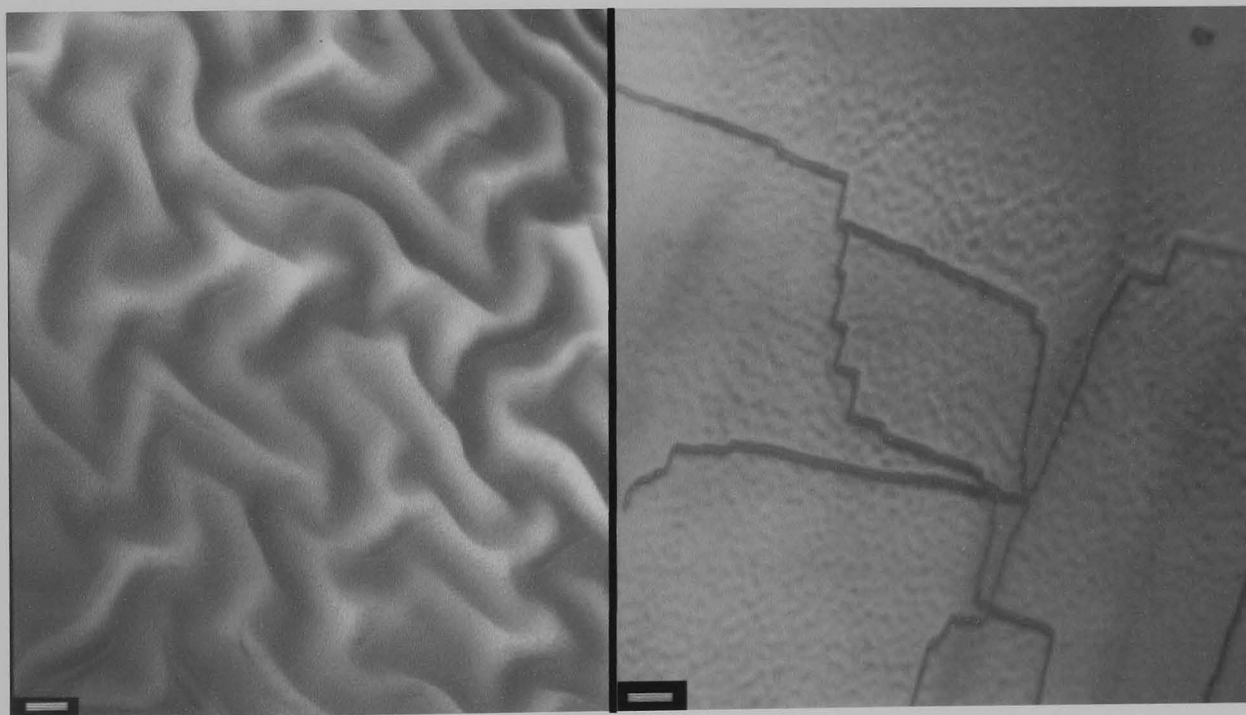
200 nm

200 nm

(a). 8 nm channel structure   **(b). 16 nm channel structure**

(c). 20 nm channel structure   **(d). 20 nm channel structure**
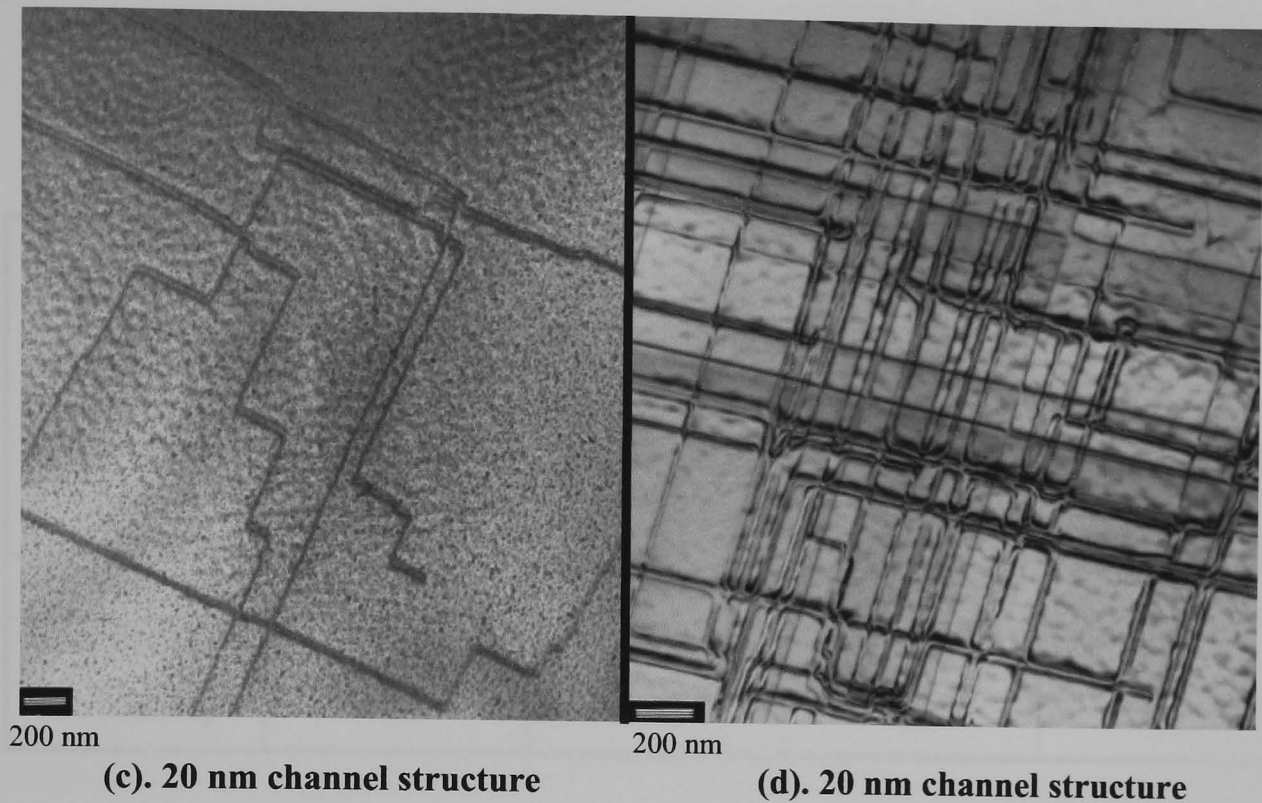
Figure 4.46. Plan view micrographs after 650°C ex-situ anneal showing (a) the surface ripples present for the 8 nm sample 68073 and the misfit dislocations (b) 16 nm sample 68072, (c) 20 nm sample 68075 and (d) 30 nm sample 68076.

From the micrograph of the 8 nm structure no misfit dislocation were observed but a small amount surface roughening was detected. This may be attributed to the onset of elastic relaxation which has been previously observed in SiGe layers grown on Si [Cullis *et al*, 1994]. For the 16 and 20 nm structures the misfit dislocation densities had increased with shorter misfits in a network formation being observed. Given the high density of misfits in the as-grown 30 nm structure it was difficult to ascertain if the density had increased within the annealed structure.

By summing the length of misfit dislocations within a certain area, and then dividing by this area, a misfit dislocation density was calculated (ρ_{md}). From equations 2.2, 2.3 and 2.4, along with the respective calculated misfit dislocation density (ρ_{md}), the amount of relaxation occurring from the misfit density on the Ge channel for each structure was determined. Table 4.8 shows the calculated misfit dislocation densities

along with the estimated relaxation for the as-grown and 650°C annealed samples 68072, 68075 and 68076.

Ge Channel thickness (nm) [Sample ID]	Estimated misfit dislocation density of as-grown samples (cm^{-1})	Estimated Ge channel relaxation from misfit dislocations for as-grown samples (%)	Estimated misfit dislocation density of annealed samples (cm^{-1})	Estimated Ge channel relaxation from misfit dislocations for annealed samples (%)
16 [68072]	1×10^3	0.1	1.5×10^4	1.6
20 [68075]	4×10^3	0.5	2.5×10^4	3
30 [68076]	$>10^5$	>35	$>10^5$	>35

Table 4.8. Summary of estimated misfit dislocation density and relaxation for the varying Ge channel thickness structures before and after annealing.

From the results given in table 4.8 it can be deduced that misfit dislocations will not lead to any significant relaxation until the Ge channel thickness ≥20 nm. As we have already observed from figure 4.43, there is a significant drop in 10 K mobility with increasing channel thickness beyond 16 nm which also coincides with an increase in the misfit dislocation line density. The drop in mobility as the Ge channel increases from 16 up to 20 nm is therefore believed not to be from relaxation but may be attributed to an increase in misfit dislocation scattering. In the case of the 30 nm structure (68076), the misfit dislocation density is sufficient to lead to a large amount (>35%) of relaxation, and the associated misfit density scattering was believed to be the reason for the poor mobility at this channel thickness.

Closer inspection of the 30 nm channel structures mobility for the as-grown and annealed material, there appeared to be no difference. It is believed that the lack of mobility enhancement after annealing is due to the samples state of relaxation, which limits the structures mobility more than the reduction in point defects upon annealing.

For the 8 nm channel structure, although an improvement in mobility was observed with annealing, the improvement was not as great as the 16 and 20 nm channel structures. For this structure therefore, it is believed that after the point defect reduction the major mobility limiting mechanism at 10 K was associated with surface roughening combined with diffusion effects, as this was believed to be more dominant in the 8 nm channel structure and a more comprehensive analysis is given in section §4.2.6.

In the case of the room temperature mobilities, the 16, 20 and 30 nm structures all show very similar results. This suggests that the mobility at this temperature shares a common limiting mechanism. It has previously been shown that optical phonon scattering [Madhavi *et al*, 2001] becomes more important at room temperature for Ge, and it is therefore believed to be the major contributing factor limiting the room temperature mobility here. The 8 nm channel structure mobility is once again observed to be lower than the other structures and this suggests that the upper channel interface is still having an influential effect to limit the room temperature hole mobility.

4.2.5 Carrier concentration discrepancy

From the Hall measurements, all the samples seem to yield a much higher measured sheet carrier density than intended. The intended heterostructure was designed to have a 5 nm doping layer with a boron concentration of 2×10^{18} cm^{-3} from which the measured sheet carrier density should have been 1×10^{12} cm^{-2}, assuming that all the carriers were transferred into the channel. From the Hall measurements the low temperature (10 K) sheet carrier density was determined to be of the order of 1.8×10^{12} cm^{-2}, and even higher at room temperature where parallel conduction would be present (see section §2.3.7). Low energy SIMS was carried out on the samples in order

to discover where the extra carriers might be arising from. Figure 4.47 shows the boron profile for the as-grown and 650°C annealed material of sample 68072. The profile shown is typical of what was observed for all the structures. From the SIMS profile a very thin (~2 nm), boron spike at the surface for all the samples, with a peak concentration of around $1 \times 10^{18} \text{cm}^{-3}$ is observed. However, as was mentioned in §3.3.1, the first few nanometers typically falls into a pre-equilibrium region of the SIMS profile, and so this surface boron spike can only be estimated. From the annealed profile the surface Boron appeared to diffuse into the sample. It is believed that such a thin layer of boron, approximately 20 nm from the channel, may contribute slightly to the measured carrier density but was not however the main source for the extra carriers.
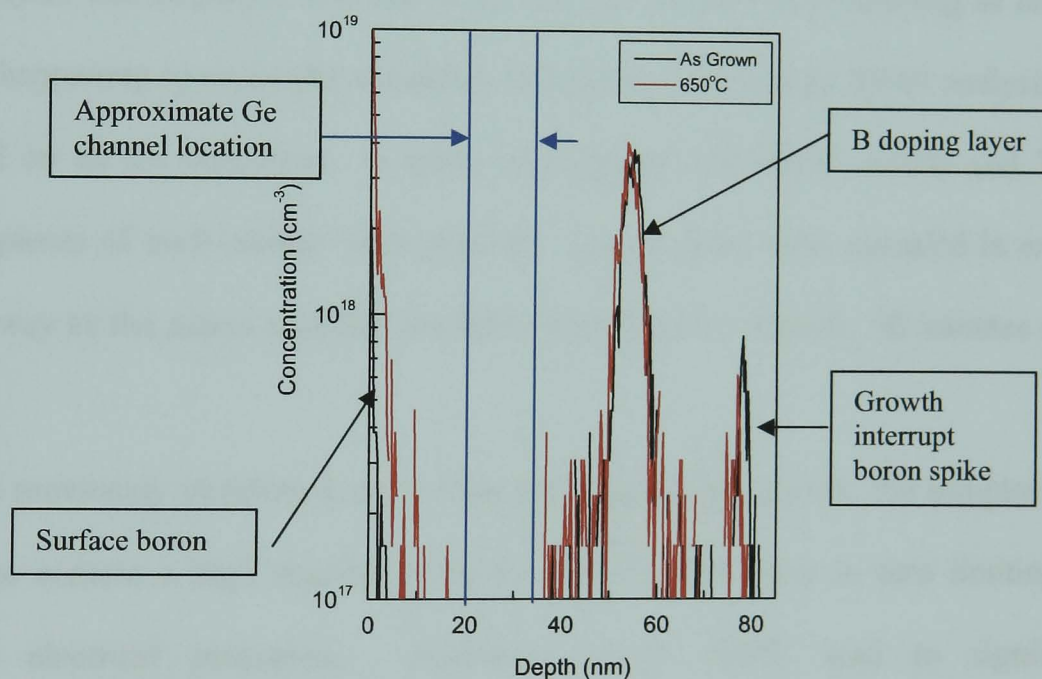
Figure 4.47. Low energy SIMS profile of sample 68072 (16 nm structure) showing the boron distribution within the structure for the as-grown and 650°C annealed structure.

The SIMS profiles did however show that the peak concentration for the intended boron doping layer was about 1.6 times larger than the intended ($\sim 3.6 \times 10^{18} \text{ cm}^{-3}$) for all the structures. This extra amount of doping agrees well with the higher measured Hall carrier density. Finally, a small build up of boron was observed at

the growth interrupt as expected, and so the 20 nm of re-growth after the interrupt, prior to the heterostructure, appears to have been justified. The other important feature about the profiles shown in figure 4.47 is the apparent lack of any sufficient diffusion of the boron doping layer with annealing. This agrees well with the small changes in measured sheet carrier density from the Hall measurements on the as-grown and annealed structures.

4.2.6 <u>Si-Ge inter-diffusion effects</u>

As annealing was found to have a pronounced effect on the sample's properties, SIMS analysis was employed in order to try and gain further understanding as to what might be happening to cause the annealing influence. Low energy SIMS analysis was performed on all the structures. A piece of as-grown and 600°C, 650°C and 700°C annealed pieces of each sample were profiled. The samples were annealed in exactly the same way as the pieces used for the Hall measurements, namely, 30 minutes under dry N_2.

As previously mentioned, due to the low temperature growth, the samples were believed to contain a high number of point defects which were in turn limiting the material's electrical properties. Annealing up to 650°C lead to significant improvements with respect to the as-grown structures and this was attributed to the annealing reducing the number of point defects present. However, beyond this temperature, the structure began to degrade. Figures 4.48a-d show the Si and Ge SIMS profiles for all the as-grown and annealed samples.

From these profiles it appears that diffusion of Si into the Ge channel has occurred, even for the lowest temperature anneal, and is more pronounced the thinner

the channel structure. Although there is some Si diffusion for the lowest anneal, the amount of Si present in the Ge channel does increase with increasing anneal temperature as would be expected.
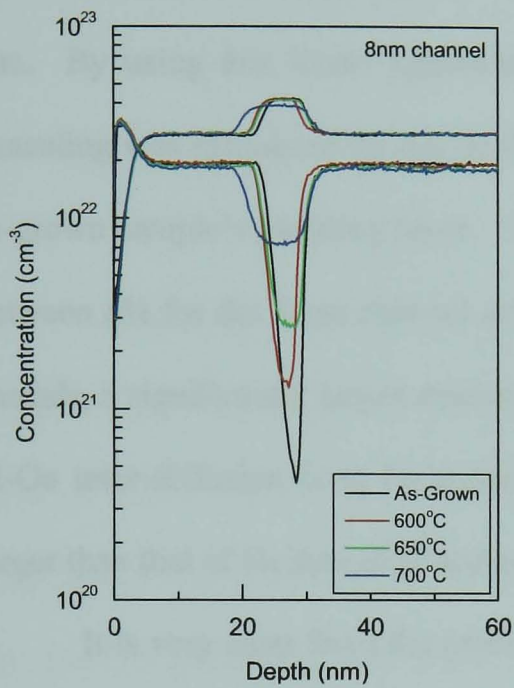
(a). 68073
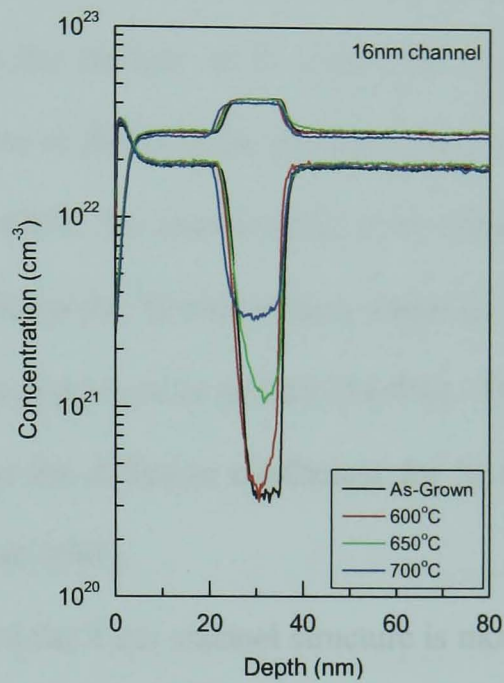
(b). 68072
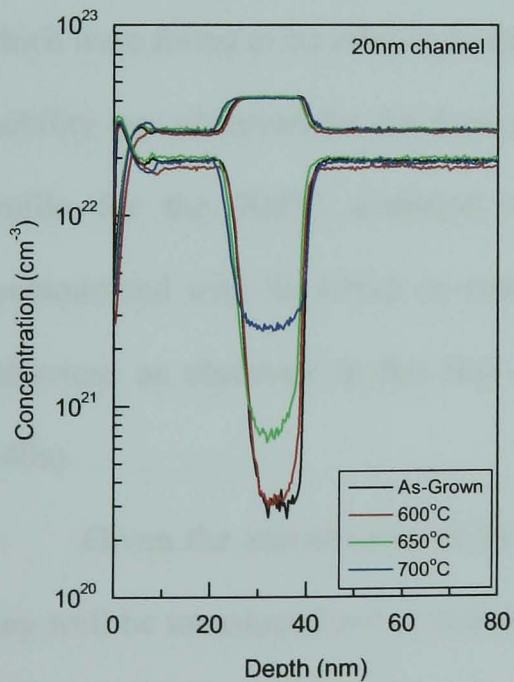
(c). 68075
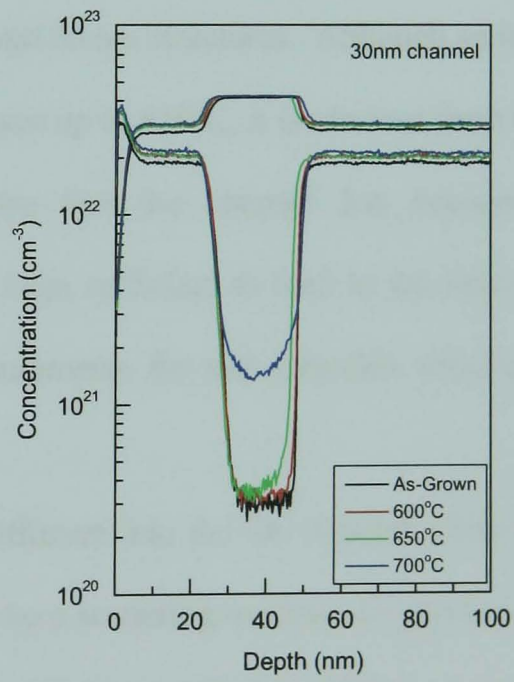
(d). 68076

Figure 4.48. Low energy (500eV) normal incidence SIMS profiles of samples (a) 68073, (b) 68072, (c) 68075 and (d) 68076.

The amount of Si present in the channel after annealing was estimated by assuming none was present in the as-grown channel region and the cladding layers contained 40% Si. The Si profiles were then pinned to the cladding layer concentration and the rest of the profile assumed to follow a linear behaviour in ion yield and erosion rate. By using this linear approximation the amount of Si within the channel after annealing was calculated by taking the ratio of the Si in the channel to the Si from the as-grown sample's cladding layer. Up to 650°C the amount of Si in the channel varies between 6% for the 8 nm channel and <1% for the 30 nm channel, while for the 700°C anneals, a significantly larger amount of Si appears to be present (14-4%). This type of Si-Ge inter-diffusion is to be expected as the diffusion coefficient for Si into Ge is larger than that of Ge into Si [Räisänen *et al*, 1981].

It is very clear from the profiles that the 8 nm channel structure is most affected by the annealing, and this is in very good agreement with the measured electrical results which were found to be inferior to the 16 and 20 nm structures. Although an increase in mobility was observed for the 8 nm structure up to 650°C, it is obvious from the SIMS profile for the 700°C annealed structure that the channel has become heavily contaminated with Si, which in turn has been sufficient to lead to the loss of 2DHG behaviour as observed in the Hall measurements for this annealed structure (figure 4.40a).

Given the introduction of Si by diffusion into the Ge channel, alloy scattering may well be introduced and is believed to be a scattering mechanism which inhibits the mobility within a SiGe channel structure [Whall and Parker, 2000]. From the Hall results it is not until the 700°C anneal that a sufficient amount of Si is introduced to cause a detrimental effect on the samples mobilities. Along with the diffusion of Si at the channel interfaces comes the loss of interface sharpness, valence band offset and

reduction in strain between the cladding layer and Ge quantum well, especially for the 700°C anneal which shows a large amount of Si migration. Such a loss in interface sharpness, valence band offset and strain will have a detrimental effect on the structures mobility and carrier confinement.

4.2.7 **Conclusions**

By using the Pirahna clean and high re-growth temperature previously found to yield a good re-growth interface and subsequent material quality, the active layer however had to be deposited at a lower temperature in order to suppress segregation and roughening. Initial growths lead to large scale roughening of the Ge channels upper interface suggesting the growth temperature was too high. Following studies employing different temperature ramps and finally including a growth interrupt, a temperature was found at which the roughening was suppressed but crystalline integrity was maintained. The electrical results for the 8 nm channel thickness structure showed a marked improvement over previous results strongly implying that the interface roughening was limiting the material. 1D Poisson/Schrödinger modelling suggested that the upper interface of for the 8 nm channel had a very strong influence on the confined carriers.

A set of samples with varying channel thicknesses greater than 8 nm were grown so as to investigate the effect of using a thicker channel and moving the upper interface further away from the carriers confined in the channel. Given the low temperature required to suppress the roughening and the similarities between the varying channel thickness structures as-grown electrical results, point defects were believed to be limiting the structures. Anneals for 30 minutes in the range of 600-650°C under dry N_2

showed significant mobility improvements from 8000 cm^2/Vs up to a maximum of 26,900 cm^2/Vs at 10 K. Exceeding 650°C led to degradation in the electrical properties.

As the thicker channel structures were believed to be in excess of the critical thickness, Plan view TEM was performed to investigate whether misfit dislocations were forming at the lower interface of the Ge channel. Such misfit dislocations were a possible source of scattering, limiting the electrical properties of the material. For the 16 and 20 nm channel structures, no significant relaxation was calculated from the misfit dislocation line densities, although it was thought that these misfits were a scattering mechanism reducing the low 10 K Hall mobility. For the thickest channel structure (30 nm), the misfit dislocation density observed was sufficient to lead to the structure relaxing by about 35%, and so the lower mobility observed for this structure was believed to arise from a combination of increased misfit dislocation scattering and partial relaxation. In the case of the room temperature mobilities for all the structures, optical phonon scattering was believed to be the mobility limiting mechanism.

Low energy SIMS was used and it was found from the profiles that the higher than intended carrier density observed by Hall measurements was due to excessive doping within the boron doping layer. Annealing was also found from SIMS to introduce Si into the Ge channel for all anneals, although at 700°C the amount of Si became very significant, leading to the channel in the most severe cases becoming a SiGe alloy. In this situation alloy scattering would become source of scattering and a major limiting factor in the mobility.

4.3 Ge Channel Device Prospects.

4.3.1 Channel mobility and carrier density

For Ge channel modulation doped heterostructures like the structures used for this work, it is typically found that that they posses parallel conduction paths, especially at room temperature. This means that the carrier densities observed at room temperature from Hall measurements will not be just the channel carrier density, but a combination of all carriers within the heterostructure (see section §2.3.7). It is believed that if the channel mobility is sufficiently high, as in the case of the structures 68072, 68073, 68075 and 68076, the channel mobility will dominate and the measured mobility will be closer to the true channel mobility. To a very good approximation the measured low temperature (~10 K) carrier density can be assumed to be the true channel carrier density because at such temperatures the carriers in parallel conducting paths are believed to freeze out (see section §2.3.7).

In order to measure the room temperature mobility and carrier density directly for such types of structure, a high magnetic field (12 T), magneto conductivity transformation measurement and maximum entropy mobility spectrum analysis technique has been developed at Warwick [Kiatgamolchai, 2000]. This technique not only allows for the channel mobility and carrier density to be obtained, but the mobility and carrier density for all the parallel conducting layers too. The measurement process and calculations are complicated and it is not the author's intention to try and explain this measurement technique, but the Thesis of Somchai Kiatgamolchai [Kiatgamolchai, 2000] is a good reference for the technique. The mobility spectrum measurements and analysis were performed on behalf of the author by Dr Oleg Mironov, Dr Somchai Kiatgamolchai and Dr M. Myronov on material prepared by the

author. Given the time and effort required for these measurements only two samples were deemed suitable for these measurements, namely the 16 nm and 20 nm structures annealed at 650°C as these provided the best Hall results. The Room temperature channel mobility and carrier density for these two samples are given in table 4.9 along with there previously measured Hall results for comparison.

Sample	Mobility spectrum analysis channel mobility (cm^2/Vs)	Mobility spectrum analysis carrier density (cm^{-2})	Hall mobility (cm^2/Vs)	Hall carrier density (cm^{-2})
68072 (16nm)	2400	1.1×12^{12}	1840	2.0×12^{12}
68075 (20nm)	2700	1.0×10^{12}	1910	2.1×10^{12}

Table 4.9. Comparison of room temperature mobility and carrier density results for the best two annealed structures obtained from Hall measurements and the maximum entropy technique.

Figure 4.49 shows a room temperature mobility spectrum plot of the 20 nm structure showing partial conductivity as a function of mobility. The 2DHG mobility peak is clearly indicated whilst the two smaller peaks to the left of the 2DHG peak are believed to arise from holes within parallel conducting layers which will may include ionised carriers within the doping supply layer and possibly the VS (see section §2.3.7). The negative peak in mobility represents electron mobility and is possibly due to the n-type dopant within the starting silicon substrate.
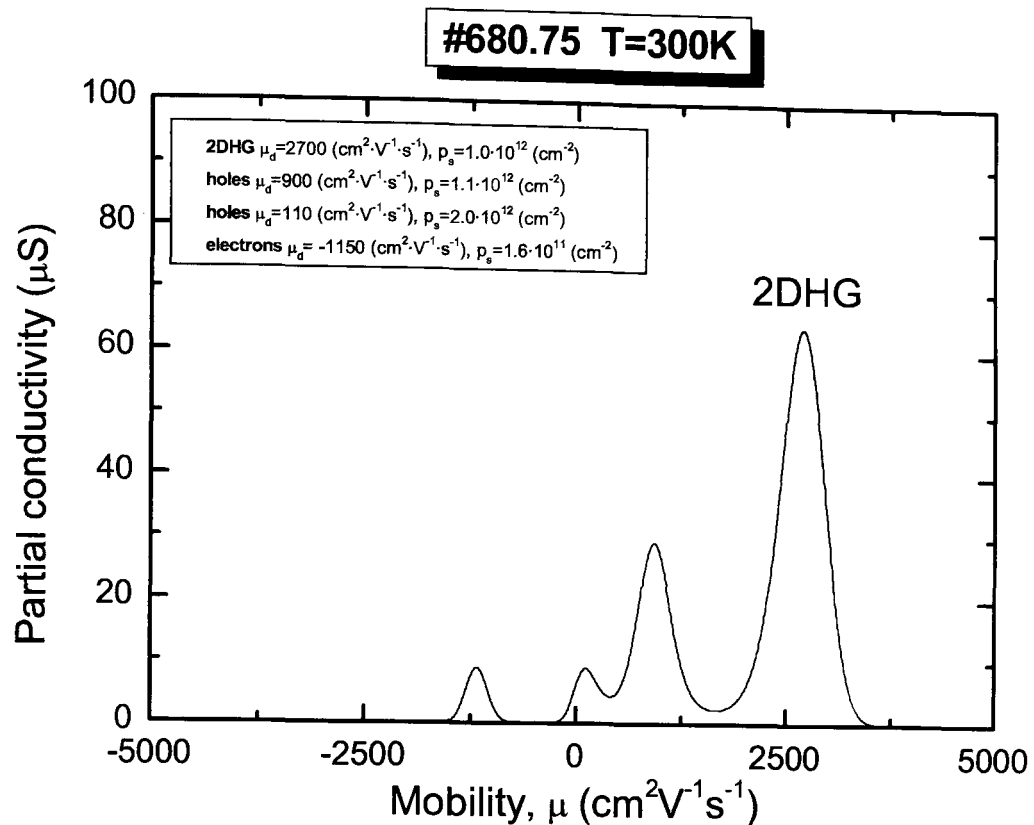
Figure 4.49. Mobility spectrum plot showing the room temperature mobility for the 20 nm structure 68075.

4.3.2 Ge device outlook

Modern Si MOSFET devices have a working carrier density of $\sim1\times10^{13}\,cm^{-2}$. Device manufacturers are forever pushing for faster devices at densities of $\sim1\times10^{13}\,cm^{-2}$ needed to achieve the advances for future generation processors. From the mobility spectrum results given in §4.3.1, certain aspects of these results can be related to modern device characteristics. The mobility spectrum results obtained show the best mobility and carrier density combination seen for such structures to date. The combination of good mobility with carrier density bodes well for the implementation of such material in a device structure.

One way of comparing modulation doped material with current devices to a simple approximation is by looking at the effective mobility as a function of (vertical) effective field present in real devices. Using the measured carrier concentration of 1.0×10^{12} cm^{-2} (N$_b$) and assuming a background doping of 1×10^{16} cm^{-3} (N$_{dep}$) with a depletion depth of 300 nm, the effective field for the present modulation doped structures may be obtained using the equation:

$$E_{eff} = \frac{q}{\varepsilon_o \varepsilon_{Ge}} \left(\frac{1}{3} N_b + N_{dep} \right)$$

(4. 5)

Where ε_{Ge} is the relative permittivity of Ge and q the electronic charge $(1.6 \times 10^{-19}$ C).

The calculated effective field was ~0.07 MV/cm. For a current Si pMOS device at such and effective field the effective mobility is of the order of 200 cm^2/Vs. This value is significantly less than the 2700 cm^2/Vs measured for the 20 nm modulation doped structure for this work. Figure 4.50 shows a plot of effective mobility as a function of effective field for some current Ge MOSFET devices, modulation doped heterostructures, a Si pMOSFET and the present result. Although the results obtained for this work are for a buried channel and by using an inverted doped structure we are using the mobility obtained at the lower interface, the mobility found is equivalent to the best mobility published for a pure Ge MOSFET. The results shown in figure 4.49 give a clear indication that the Ge channel is now showing potential for device applications with the aim of improving the hole mobility of current device technology.
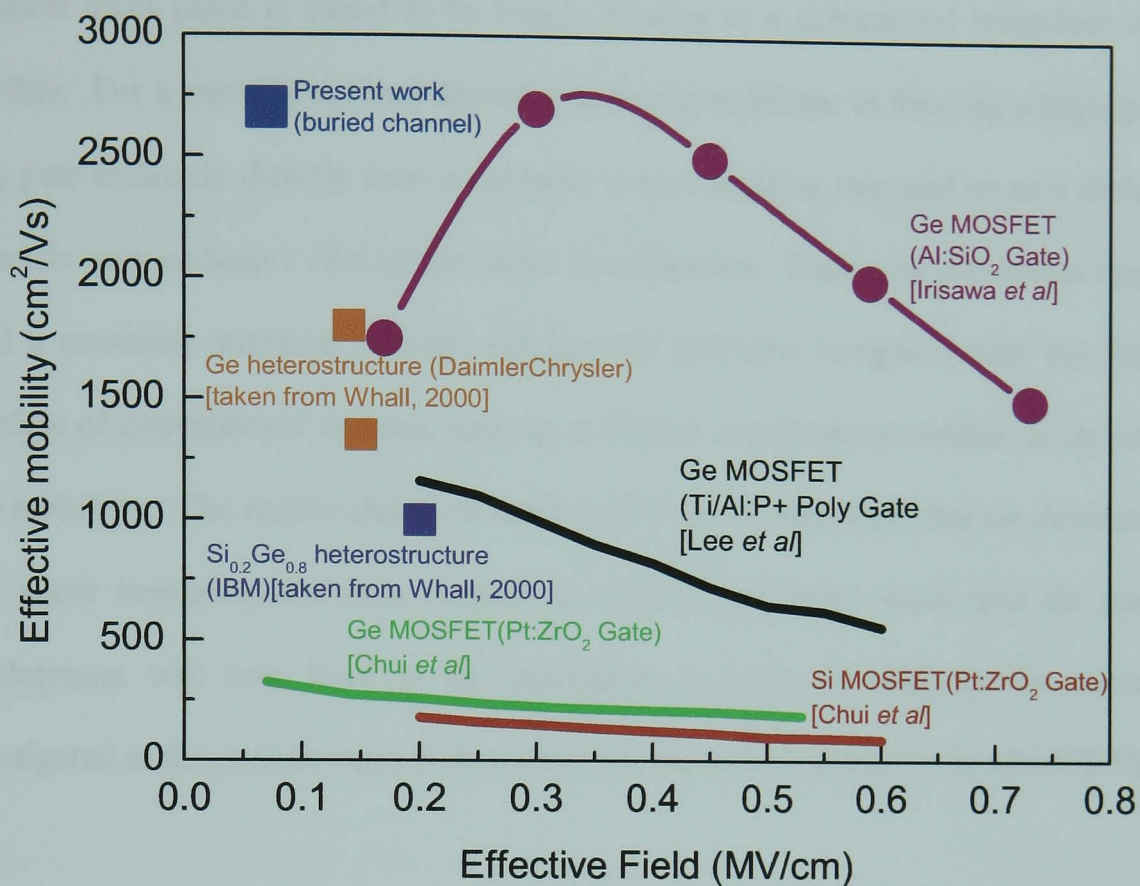
Figure 4.50. Plot of effective mobility as a function of effective field for the present 20 nm structures result compared with current Ge MOSFETS and a Si MOSFET.

4.3.3 Summary

The results given in §4.3 suggest strong possibilities for pure Ge channel device technology. Hall measurements from a modulation doped structure cannot be compared directly to those from a device structure. The best way to gauge an indication of the modulation doped structures device possibilities is to compare the effective mobility at an effective field. One significant difference between a typical MOSFET device structure and the modulation doped structures used for this work is that the conducting channel is at the surface and the carriers are located towards the upper interface, whilst in the present structures, it was the lower interface of the buried channel where carrier

transport occurred. Typically for MOS devices, the channel/oxide interface where the transport takes place is found to be rough, leading to a detrimental behaviour in the mobility. For a pure Ge channel device, processing problems in forming a high quality SiO_2 gate dielectric directly onto a Ge have been a limiting step and so new dielectric materials such as high k (ZrO_2) are under investigation. Such new dielectrics may yet yield a smoother interface between the Ge and dielectric compared with the Si/SiO_2 interface of conventional devices, leading to further improvement within Ge device for hole mobilites. The results shown in section §4.3 are an indication that Ge devices may well show improvements over current Si devices but much work into the process development will now have to be undertaken in order to integrate the structures investigated in the present work if they are to be turned into working Ge MOSFETS.

5. Optical charge compensation and the quantification of CVD grown SiGe layers by Secondary Ion Mass Spectrometry (SIMS)

5.1. Introduction

Secondary ion mass spectrometry (SIMS) is a destructive technique, whereby the sample investigated undergoes bombardment from a mono-energetic beam of primary ions that are typically within the energy range of 100 eV to 30 keV. As a result, sputtering of particles from the samples surface occurs. A small fraction of these sputtered particles are ionised, and it is these ions, known as secondary ions, which are measured and used to build up a depth profile of the sample. The technique of low energy secondary ion mass spectrometry is described in section §3.3.

Low energy secondary ion mass spectrometry is an important tool for determining the spatial distribution and concentration of impurity layers in Si. With the expanding SiGe devices market, quantification of such structures is becoming increasingly important. Key quantifiable parameters include determination of the Ge fraction along with the depth and interface quality between the Si and SiGe layers.

In this section we describe the SIMS analysis of SiGe heterostructures. Samples were obtained from a commercial source and a novel technique was developed to overcome charging effects which were seen to occur in highly intrinsic SiGe structures.

5.2. The effect of doping SiGe layers

In order to investigate the SIMS quantification of SiGe layers, samples were obtained from Taiwan Semiconductor Manufacturing Company (TSMC), a leading epitaxial specialist and the Worlds largest CMOS foundry. The samples were grown via Low Pressure Chemical Vapour Deposition (LPCVD) on a commercial epitaxial reactor. The intended structural formats of the layers along with their individual identification numbers are given in Figure 5.1. It should be noted that the two samples were identical in nature except that sample DN60 included a boron background doping at intended concentration of $\sim 2 \times 10^{19}$ cm^{-3}.

100 nm Si
100 nm $Si_{0.8}Ge_{0.2}$
100 nm Si
100 nm $Si_{0.84}Ge_{0.16}$
100 nm Si
100 nm $Si_{0.88}Ge_{0.12}$
100 nm Si
100 nm $Si_{0.92}Ge_{0.08}$
100 nm Si
100 nm $Si_{0.995}Ge_{0.045}$
100 nm Si
Si Substrate

Boron Doped

100 nm Si
100 nm $Si_{0.8}Ge_{0.2}$
100 nm Si
100 nm $Si_{0.84}Ge_{0.16}$
100 nm Si
100 nm $Si_{0.88}Ge_{0.12}$
100 nm Si
100 nm $Si_{0.92}Ge_{0.08}$
100 nm Si
100 nm $Si_{0.995}Ge_{0.045}$
100 nm Si
Si Substrate

(a) DN0   **(b) DN60**
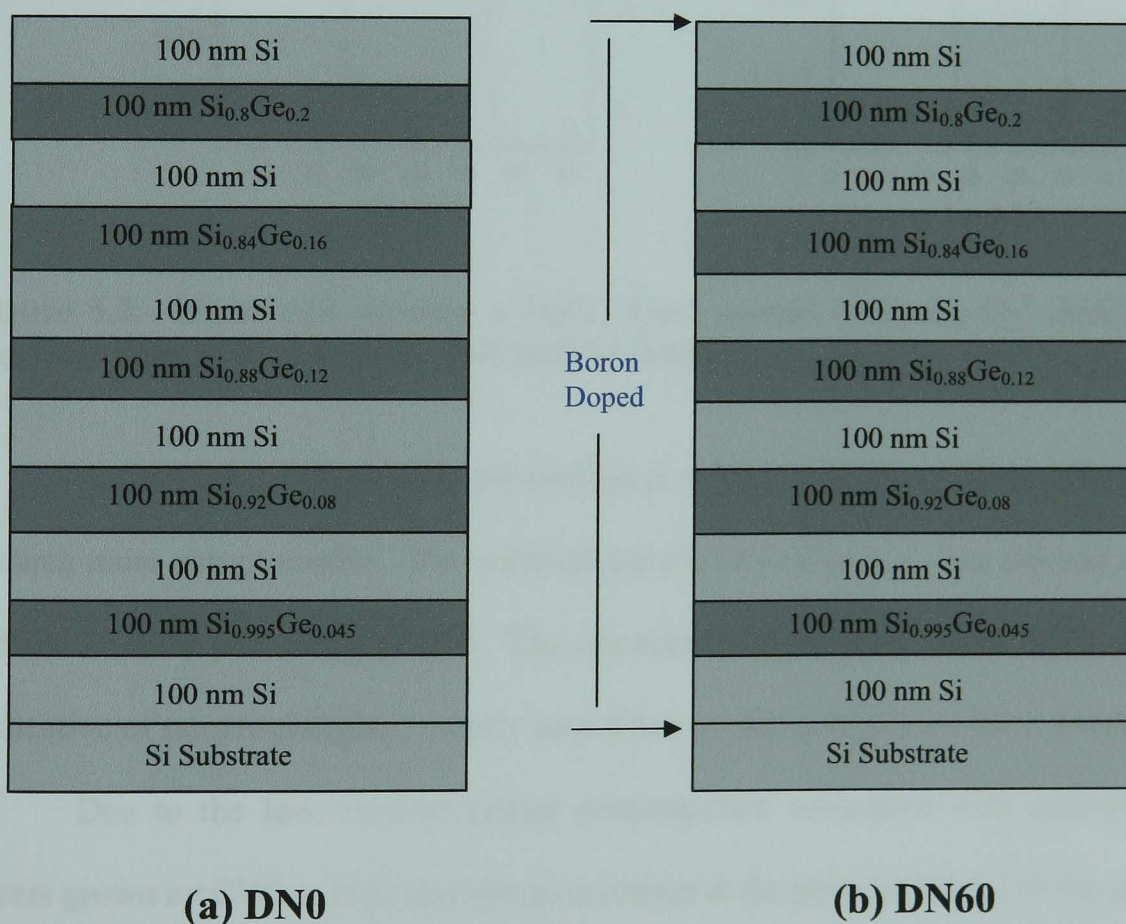
Figure 5.1. Schematic diagrams showing the intended layer structures of the SiGe samples for charge compensation analysis. Both samples were grown by CVD and supplied by TSMC.

SIMS analysis of the structures was undertaken with an O_2^+ primary beam, at normal incidence, and with an energy of 1 keV, primary beam current of 45 nA and crater size 300 μm.

Figure 5.2a and b shows the SIMS profiles of the $Si_{0.8}Ge_{0.2}$ layer from the doped and undoped multilayer structures.
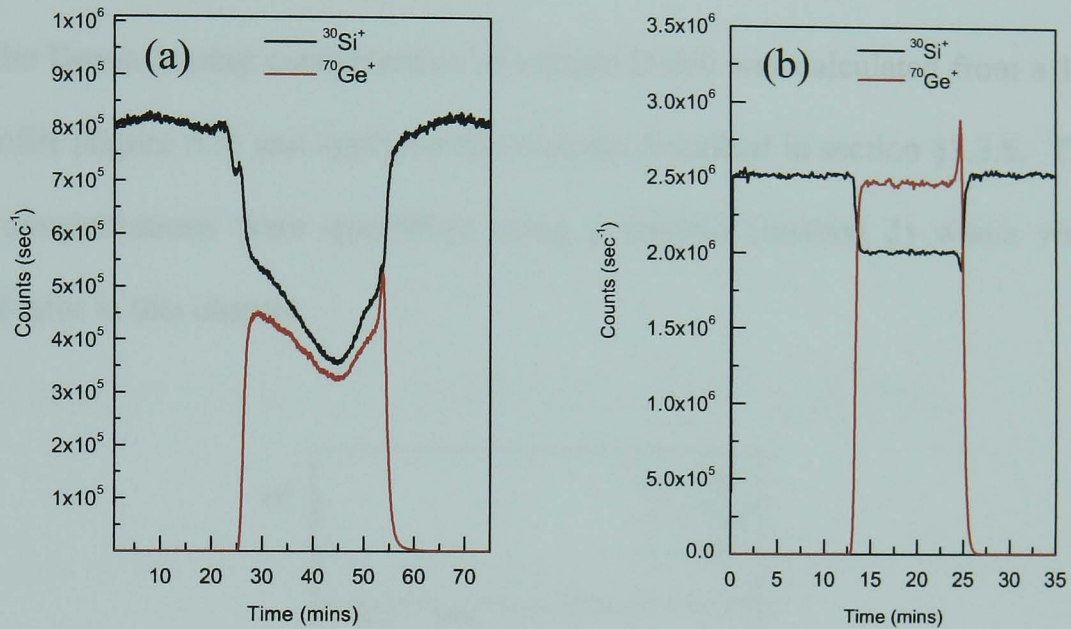
Figure 5.2. Linear plot showing a 1keV, 45nA normal incidence O_2^+ profile of the $Si_{0.8}Ge_{0.2}$ layer from sample (a) DN0 and (b) DN60.

A significant difference in the profiles is evident with the doped sample showing a much more abrupt profile. The undoped sample DN0 shows a clear dip and recovery within the SiGe part of the profile. The characteristics observed in the SIMS profile is indicative of sample charging, usually seen when profiling highly resistive samples.

Due to the low residual carrier concentration associated with undoped SiGe layers grown by CVD, a high spreading resistance at the point of impact of the ion beam is believed to be induced. In order to simulate the loss in ion yield observed within the SiGe profile of figure 5.2a, a change in target bias of ~10 V was required. The technique for estimating the surface potential change by means of offsetting the sample

bias and so moving off the maximum of the samples energy spectrum for a particular mass was first suggested by Dowsett *et al* [Dowsett *et al*, 1986]. From the measured primary beam current (45 nA) and the target bias required to induce a surface potential change equal to that observed in figure 5.2a (10 V's), then by applying Ohms law (V=IR), a resistance within the charge path to ground (sample holder) of $\geq 2.5 \times 10^8 \, \Omega$ is calculated to a first approximation.

The Boron doping concentration of sample DN60 was calculated from a 1 keV SIMS profile (figure 5.3) and applying the analysis described in section §3.3.6. The Si and Ge concentrations were quantified using a method (method 2) which will be described later in this chapter.
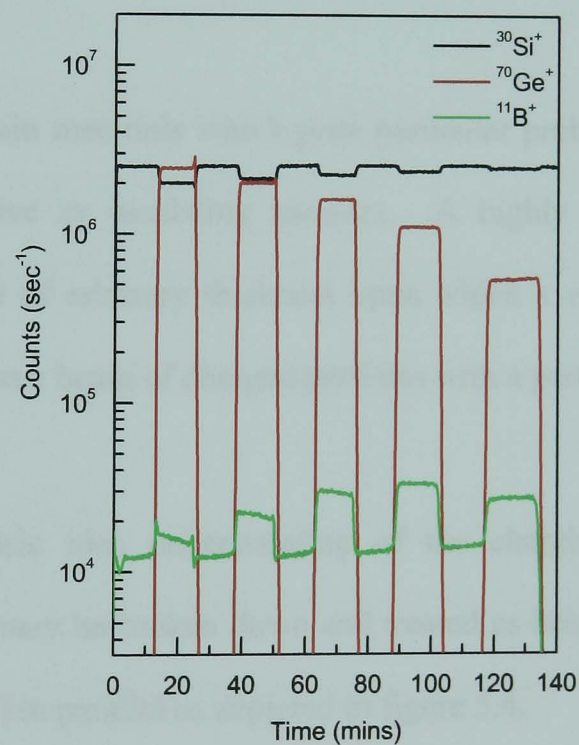
Figure 5.3. Quantified 1 keV 100 nA O_2^+ SIMS profile of sample DN60.

From figure 5.3 it is seen that the boron concentration varies between the SiGe and Si layers. This is believed to be an effect of the SIMS and not a true representation

of the boron concentration within the sample. Boron doped SiGe will have a different ionisation probability and erosion rate compared with boron in Si, and it is the combination of these two variables which is leading to the different boron ion yields being observed between the Si and SiGe layers.

The results of the two profiles for the doped and undoped samples show that a problem exists when profiling intrinsic layers of SiGe. This problem arises due to the high resistance of the sample leading to charging effects smearing the true profile shape. In order to obtain highly accurate SIMS quantification of undoped SiGe layers, a new approach to overcome the charging effect is required.

5.3 Charge compensation of resistive and insulating samples

There are certain materials which pose particular problems for SIMS profiling, notably highly resistive or insulating samples. A highly resistive sample can be described as a sample of arbitrary thickness upon which a voltage difference appears across the sample when a beam of charged particles with a particular current density hits the surface.

To give a basic idea understanding of the charging process, consider an insulating sample. It may be broken down and treated as being analogous to a resistor (R) and a capacitor (C) in parallel as depicted in figure 5.4.
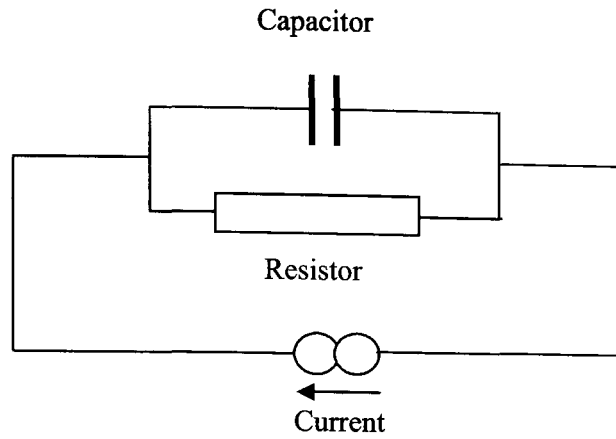
Figure 5.4. Schematic diagram showing a resistor and capacitor in parallel, analogous to charging of samples when profiled using SIMS.

When such a sample is bombarded with a beam of ions or charged particles, an electric potential will build up on the samples surface. This charge will arise from the primary beam, the secondary induced electrons or a combination of both. For a poorly conducting sample, the steady-state will be obtained when the current through the capacitor ceases. Charging of a sample will lead to detrimental behaviour in the resulting profile with some or all of the following effects possible [Werner and Warmoltz, 1984]:

- Signal instability

- Broadening of the energy spectrum peak and some signal reduction

- Peak shifting of the energy spectrum if the particle energy is an element-specific parameter

- Ratio of peaks with different energy distribution changes

- Strong signal reduction up to complete loss of signal.

There has been much work carried out to alleviate charging effects observed for certain samples. One approach is coating the sample surface with a conducting layer such as Gold and has been shown to work well [McPhail *et al*, 1986]. Other methods include raising the samples temperature in order to lower its resistivity, illumination of the sample surface in order to stimulate the material or focusing low energy electrons within the energy range of 100 eV to1 keV onto the area being eroded by means of a low energy electron gun [Wittamaack, 1979] have all been demonstrated. However, these charge compensating techniques are specific to the equipment being used, such as a heated stage to thermally induce carriers, or require peripheral equipment such as a gold evaporator.

The type of sample also determines the method of charge compensation which may be required. Due to the nature of the problem within the low residual carrier density SiGe layers, especially in the case of the buried layers within the multilayer structures, gold coating the samples surface or using a low energy electron gun were not suitable or found not to work. A known, non destructive method of reducing the resistance of a semiconductor layer is to create electron-hole charge carriers via illumination [Sze, 1985]. In the following section we describe a novel technique of overcoming charging effects during SIMS profiling using optical stimulation.

5.4 <u>Optical light charge compensation</u>

In order to observe the effects of optical stimulation, light from a standard quartz-halogen lamp (QHL) was allowed to illuminate the surface of the undoped sample, DN0, while SIMS profiling was performed. The QHL unit was supplied with the instrument and the light generated by the unit was passed down a fibre optic before

being projected onto the samples surface through one of the view ports on the Atomika 4500's main chamber. Table 5.1 shows the main parameters for the QHL.

Device	Beam divergence (sr)	Total optical power output (mW)	Beam diameter at sample (mm)	Optical power density at sample (mW/mm^2)
Quatz-Halogen Light (QHL)	1.4	>200*	-	4×10^{-3}

* measured at the end of the fibre optic

Table 5.1. Measured optical properties of the quartz-halogen lamp.

Figures 5.5 (a) and (b) show the SIMS profiles of the undoped sample DN0 with and without QHL illumination.
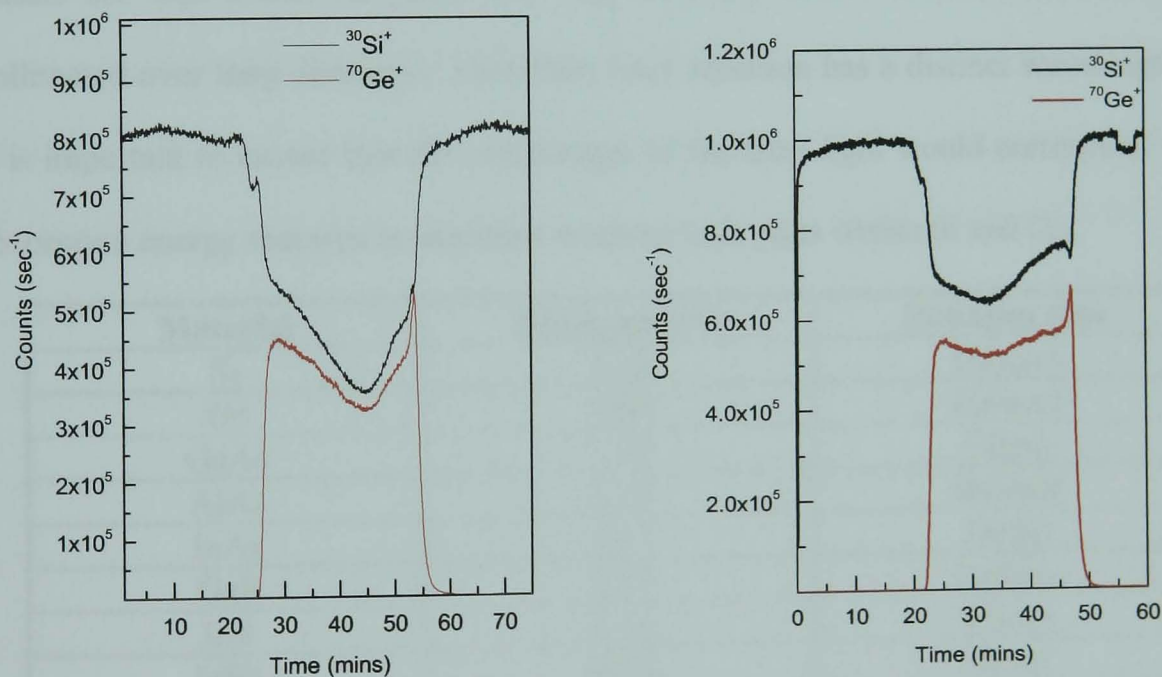
Figure 5.5. (a) Linear plot for a 1keV 45nA SIMS profile of sample DN0 without QHL sample illumination and (b) linear plot of the same profile with QHL illumination.

The comparison plots of figures 5.5a and b clearly show that a partial suppression of any charging effects has occurred. However, a comparison of figure 5.5b

to the SIMS profile of the doped sample, DN60 (see figure 5.2b), clearly indicates that the total suppression of sample charging effects is not occurring.

Although the power output from the QHL source was believed to be very high, the beam divergence for this source was large. The combination of a large beam divergence along with the sample being situated at least 0.5 meters from the light source, results in a significant reduction of the illumination intensity at the sample surface.

5.5 An alternative optical charge compensation – laser illumination

In order to increase the illumination efficiency at the sample surface, an illumination source of high intensity with collimation over large distances is required. Lasers are well known to yield very high intensity beams of radiation that remain collimated over long distances. However, laser radiation has a distinct wavelength and it is important to ensure that the wavelength of the laser light would correspond to the absorption energy required to stimulate electron-hole pairs within Si and Ge.

Material	Bandgap (eV)	Bandgap type
Si	1.12	Indirect
Ge	0.66	Indirect
GaAs	1.42	Direct
AlAs	2.15	Indirect
InAs	0.35	Direct
GaP	2.27	Indirect
InP	1.34	Direct
InSb	0.23	Direct

Table 5.2. Bangap values and types for some of the more common semiconductor materials. (taken from Singh, 1994)).

Table 5.2 shows the room temperature energy-gaps along with the type of energy-gap (direct/indirect) for some commonly used semiconductor materials. Using

this information, the wavelength required to stimulate carriers in either Si or Ge can be calculated.

Assuming that the transition of electrons in the material will occur from the top of the valence band to the bottom of the conduction band, the wavelength of radiation required may be obtained from the relation:

$$\lambda_{illu\,min\,ation} \le \frac{hc}{E_c - E_v} = \frac{hc}{E_g}$$

(5. 1)

Where:

$\lambda_{illumination}$ = illumination wavelength
E_c = bottom of the conduction band energy
E_v = top of the valence band energy
E_g = Energy gap
h = Planks constant
c = speed of light

As Si has the largest energy gap (Eg=1.12 eV) of the two semiconductors of interest in this work, then from equation 5.1 the wavelength of radiation required to allow electrons to move from the top of the valence band to the bottom of the conduction band was calculated to be ~1.1 μm. Taking this value of wavelength, the readily available options were a red laser pointer (635 nm), He-Ne laser (633 nm) and a red laser diode (635 nm), all of which provide sufficient energy to stimulate carriers out of the valence band and into the conduction band for our material. The absorption of photon radiation at this energy will excite electron-hole pairs whereby increasing the density of charge carriers within the undoped sample and therefore significantly lowering the resistance. In this manner, charging effects can be suppressed.

The one other problem now foreseen was the power level of the illumination required. The power density of the illumination has to be sufficient to saturate the sample for a range of primary beam energies, currents and incident beam angles that are

obtainable and readily used when profiling samples using the Atomika 4500. Table 5.3

lists some of the important properties of the red laser pointer, HeNe laser and the red

laser diode used for this work.

Device	Beam divergence (sr)	Total optical power output (mW)	Beam diameter at sample (mm)	Optical power density at sample (mW/mm^2)
Red Laser pointer	~0	2.2	4	0.2
HeNe Laser	~0	1.62	1.5	0.9
Red Laser Diode	~0	2.56	2.5	0.54

Table 5.3. Measured optical properties of a red laser pointer, HeNe laser and red laser diode.

5.6 Charge compensation of sample DN0 by laser illumination

In order to investigate and optimise the effects of laser illumination on sample

DN0, a series of profiles were decided upon in which the incident beam current, energy

and angle of incidence would be varied. All three of these parameters will change the

erosion rate of the sample during ion bombardment. In order to fully compensate any

charging effects it is important that the efficiency of electron-hole generation via

illumination is sufficiently high to compensate an increased erosion rate.

5.6.1 Incident beam current variation

The incident beam current is one of the main parameters which dictate the

erosion rate of the sample during SIMS profiling. A series of profiles was performed

using different incident beam currents in order to investigate the charge compensation capabilities of three different laser types. The laser types used are detailed table 5.3.

5.6.1.1 Red laser pointer

Figure 5.6 (a) shows a linear plot of a 1 keV, 45 nA O_2^+ SIMS profile of sample DN0 with charge compensation being applied from the laser pointer. It is seen from this profile that total charge compensation is obtained. However, when the incident beam current was raised to 180 nA, the laser pointer became insufficient to stabilise the surface potential fully, leading to charging effects again being observed within the profile (figure 5.6b).

(a)   **(b)**
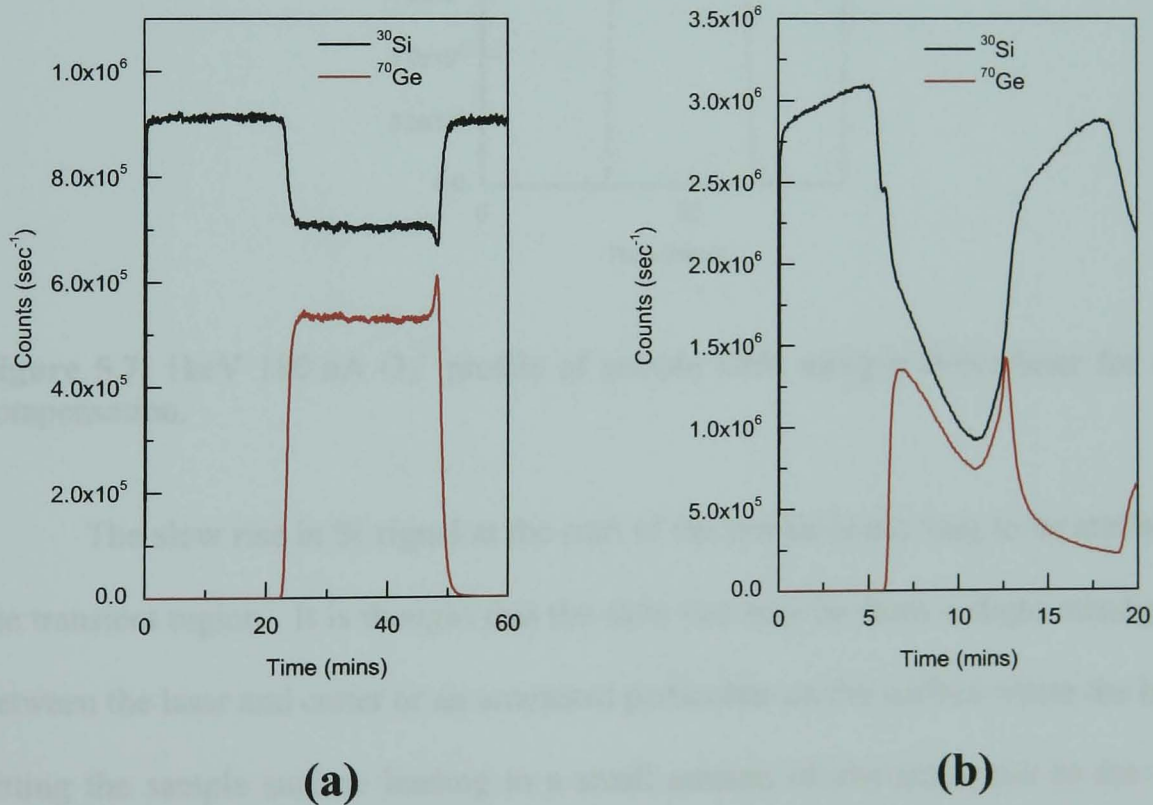
Figure 5.6. (a) Shows a 1keV 45nA O_2^+ SIMS profile for sample DN0 using a laser pointer for charge compensation while (b) is for a 180nA O_2^+ 1keV profile under identical conditions.

5.6.1.2 HeNe laser

By applying the HeNe laser to the 180 nA profile the charging effects were suppressed showing that the laser intensity is an important parameter of the charge compensation. Figure 5.7 shows a 180 nA, 1 keV profile of the $Si_{0.8}Ge_{0.2}$ layer of sample DN0 using the HeNe laser for charge compensation.
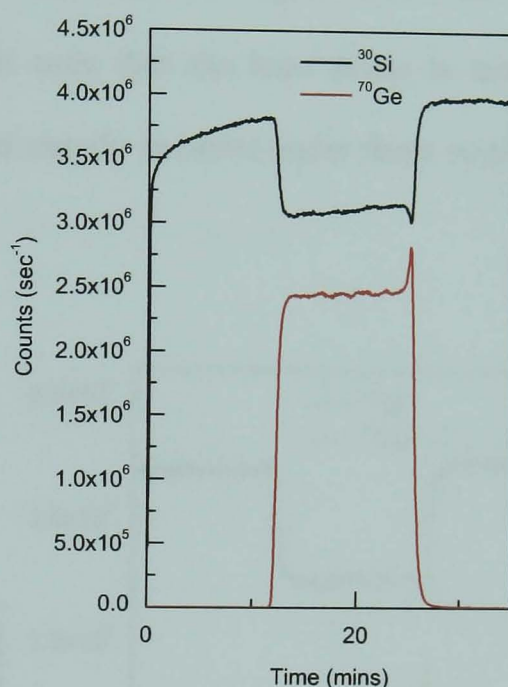
Figure 5.7. 1keV 180 nA O_2^+ profile of sample DN0 using a HeNe laser for charge compensation.

The slow rise in Si signal at the start of the profile is too long to be attributed to the transient region. It is thought that the slow rise may be from a slight misalignment between the laser and crater or an unwanted particulate on the surface where the beam is hitting the sample surface leading to a small amount of charging prior to the charge compensation taking effect and equilibrium conditions are reached.

5.6.1.3 Laser diode

To overcome the infrastructure problems associated with the HeNe laser, a small laser diode was acquired with similar optical properties to the HeNe laser although the overall power density was 40% less. In order to make sure that the red laser diode was of sufficient power density to charge compensate under typical operating conditions, a 1 keV, 100 nA profile was performed. Figure 5.8 shows the profile of sample DN0's $Si_{0.8}Ge_{0.2}$ layer and it is seen that the laser diode is more than adequate to charge compensate the undoped sample material under these conditions and a sharp profile is observed.
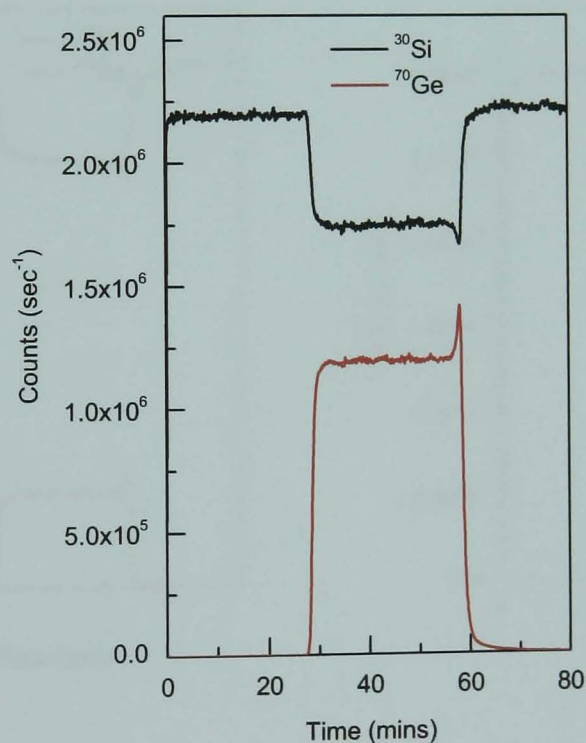
Figure 5.8. 1keV 100nA O_2^+ SIMS profile of sample DN0 with sample illumination from the laser diode.

5.6.2 Incident beam energy variation

A further parameter which has a significant effect on the sample erosion rate is the primary beam energy. In the previous section §5.6.1, the profiles were all performed for a 1 keV primary beam energy. In order to investigate the effects of beam energy, sample DN0 was profiled at a further two beam energies of 500 eV and 3 keV, while maintaining a beam current of 100 nA. Such beam energies are typical configurations for SIMS analysis using the Atomika 4500. In light of the successful charge compensation observed at 100 nA with the laser diode this laser type was used for to investigate the effects of beam energy.

(a)   (b)
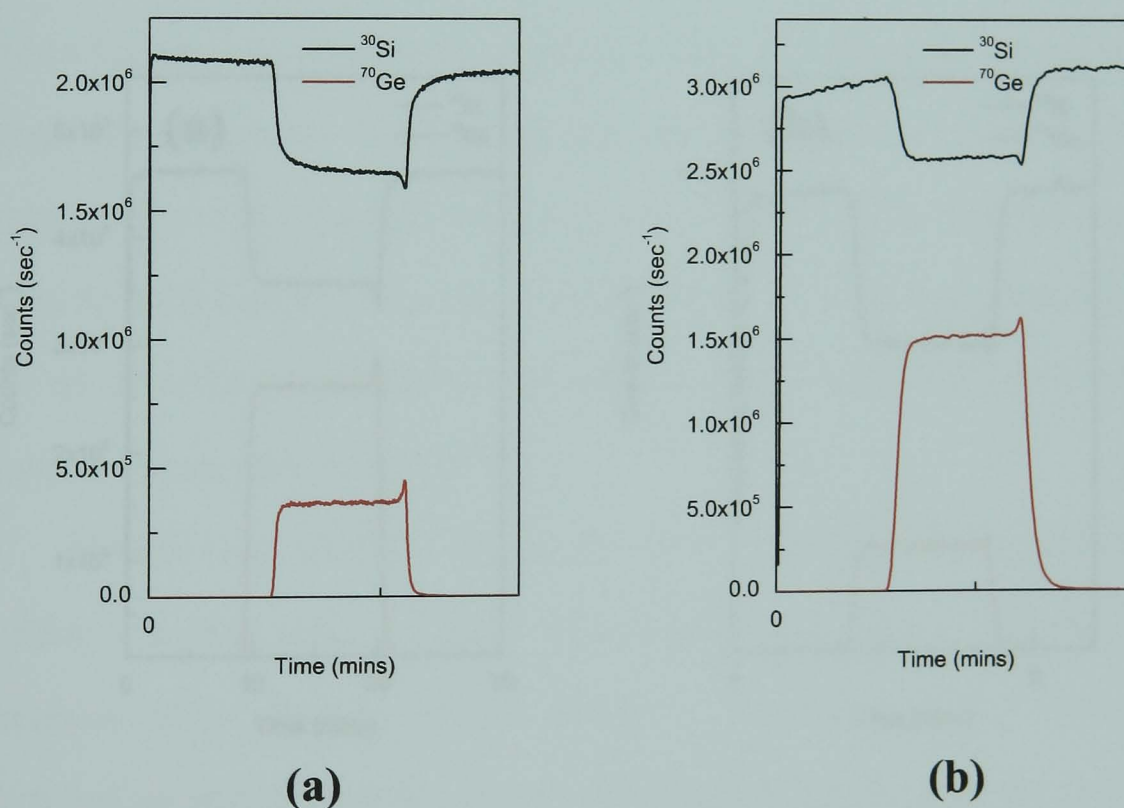
Figure 5.9. (a) Shows a 500 eV 100 nA profile of sample DN0 under laser diode illumination while (b) shows a profile under identical conditions except the incident beam energy was 3 keV.

Figure 5.9 (a) and (b) show the 500 eV and 3 keV profiles respectively for sample DN0's $Si_{0.8}Ge_{0.2}$ and it is seen that for both energies the laser diode is able to

fully suppress charging effects, even at the increased erosion rate of the 3 keV incident beam.

5.6.3. Angle of incident beam variation

SIMS analysis at increased incident angles also has a pronounced effect on the erosion rate. A set of profiles was performed on the undoped sample DN0 using two different angles of incidence in order to see if full charge suppression using the red laser diode could be achieved. The angles of incidence used were 30° and 60°. Figures 5.10 (a) and (b) show 1keV, 100nA SIMS profiles with 30° and 60° primary beam angles of incidence respectively.
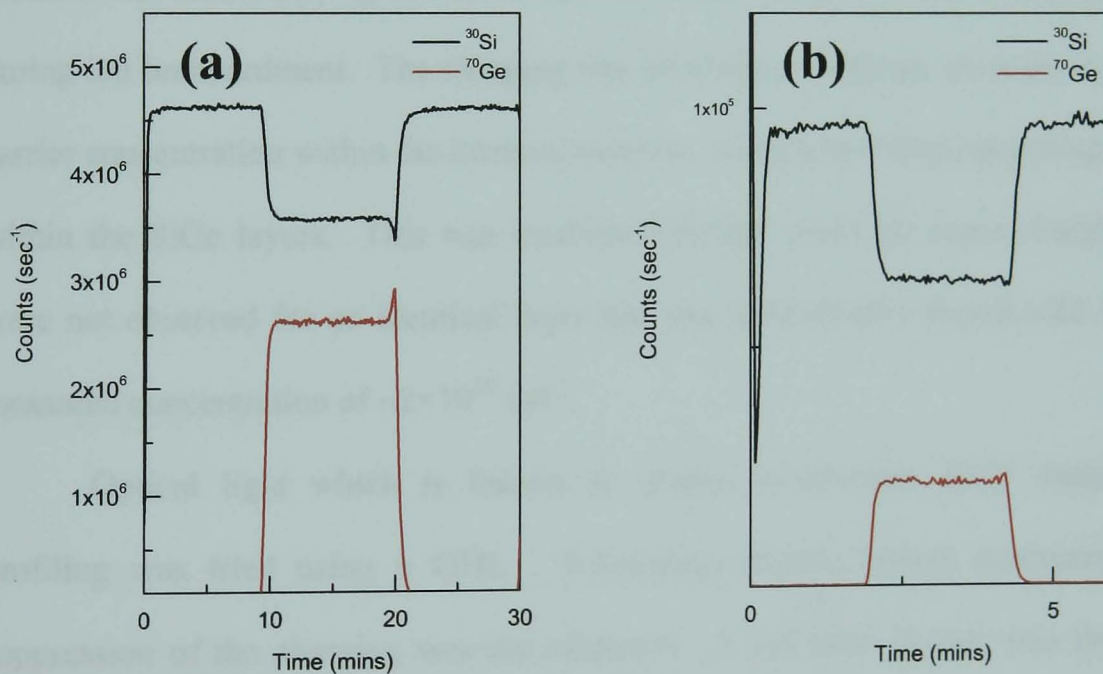
Figure 5.10. (a) Shows a 30°, 1 keV 100 nA profile of sample DN0 under laser diode illumination while (b) shows a 60° incident beam profile under identical conditions.

From the two profiles it is seen that the laser diode appears to fully suppress any charging effects. It is also seen that the magnitude of the ion yield for the 60° profile is

much lower than that of the 30° profile. This is due to the incident beam angle and nothing to do with the laser charge compensation.

5.7 <u>Summary</u>

Due to the highly intrinsic nature of undoped SiGe epitaxial layers grown using modern state-of-the-art LPCVD reactors, accurate profiles are unobtainable using conventional SIMS techniques. In this section we describe, for the first time, a novel method of charge suppression thereby enabling accurate SIMS profiles of such highly intrinsic SiGe layers.

A major limitation of profiling undoped CVD grown SiGe layers with an incident O_2^+ beam is a significant distortion of the true profile due to charging effects during ion bombardment. The charging was believed to originate from the low residual carrier concentration within the intrinsic material, leading to a large spreading resistance within the SiGe layers. This was confirmed further when the same charging effects were not observed for an identical layer that was intentionally doped with boron at a measured concentration of $\sim 2 \times 10^{19}$ cm^{-3}.

Optical light which is known to charge compensate III-V samples while profiling was tried using a QHL. Preliminary results looked promising but full suppression of the charging was not obtained. A red laser pointer was then applied which had an increased power density and was found to suppress the charging for primary beam currents up to ~45 nA. However, at larger incident beam currents the laser pointer was found to be inadequate to fully compensate charging effects at increased SIMS erosion rates. A HeNe laser and red laser diode with further increased power densities were subsequently applied and were found to yield total charge

compensation for a range of indent beam currents, energies and angles of incidence, all of which are important variables when profiling SiGe layers.

5.8 Conclusions

A novel technique enabling the accurate SIMS profiling of highly intrinsic SiGe layers has been developed. Demonstrated results offer excellent charge compensation capabilities over a significant range of beam energies, beam currents and incident beam angles. The technique employs the illumination of the sample surface during SIMS profiling with laser illumination. The laser wavelength and minimum power density were determined to be 1.1 μm and >0.54 mW mm^{-2} respectively.

In recent years the incorporation of SiGe layers in state-of-the-art device structures such as the SiGe heterojunction bipolar transistor has lead to a significant increase in the SiGe commercial market share. The results of the present chapter will have profound implications on the analysis of such device structures.

5.9 Further work

The red laser diode was found to be of sufficient wavelength to stimulate carriers across the energy gap of Si, SiGe and Ge. However some III-V materials, such as Indium Phosphide, and the emerging market of CVD grown diamond structures have energy gaps significantly larger than the red lasers calculated capability. The increased band-gap of such materials will negate the effectiveness of a red laser diode during SIMS analysis. In order to achieve total charge compensation in such material systems,

laser illumination with a decreased wavelength will be required. The effectiveness of a blue laser to charge compensate large band-gap materials should be investigated.

5.10 <u>Two methods for the quantification of Ge fraction within SiGe layers</u>

The following part of this chapter discusses two methods for quantifying the Ge fraction present within $Si_{1-x}Ge_x$ layers for with x ranging from 0 to 0.3. There has been very little work performed on the quantification of SiGe layers using SIMS, but as the SiGe semiconductor market increases this needs to be addressed. Typically, HRXRD and RBS have been used for determining the Ge fraction within SiGe layers. Both techniques are limited in their determination of the Ge spatial distribution and cannot determine doping levels ($<10^{20}$ cm^{-3}) or distribution within the layer. SIMS measurements of such layers would offer both the Ge and doping concentration if an accurate protocol for Ge concentration was developed along with the Ge and doping spatial distributions from one profile. Previously reported studies of Ge quantification using SIMS have been carried out at much higher energies (≥ 3 keV) than the present work and use a relative sensitivity factor (RSF) or normalised ion yield intensities [Newey et al,1997] [Prudon et al, 1997]. Such methods involve having to ratio the measured Si and Ge ion yields from the layers to a matrix channel. The Ge fraction determined was found to change from day to day and this was attributed to changes in aperture position within the secondary ion column between sample profiles over time. Further problems encountered originated from changes in the matrix due to the material properties. Large errors were found for material referenced to RSF values obtained from a SiGe layer with a differing state of strain.

In this work two methods were developed in order to try and accurately quantify the Ge fraction present within SiGe layers without the need for any matrix normalisation or materials strain dependence. For both methods the SiGe layers have to be of a sufficient thickness to allow for a constant ion yield with time to be obtained in both the Si and Ge profiles. Outlined below are the two methods:

5.10.1 Method 1

For this method, a previously calibrated piece of $Si_{1-x}Ge_x$ material where x is known (x_{known}) is profiled under identical conditions to that of the unknown $Si_{1-x}Ge_x$ layer. An accurate determination of the reference materials Ge fraction may be obtained using X-ray diffraction techniques, as described in section §3.2. Once the profiles have been completed, the mean Ge ion yield from the known SiGe layer ($<Y_{Gek}>$) along with the mean Ge ion yield from the unknown SiGe layer ($<Y_{Geun}>$) is found. Using these values along with the known Ge concentration (x_{known}), the Ge fraction of the unknown sample ($x_{unknown}$) may be determined using the following expression.

$$x_{unknown} = \left(\frac{\langle Y_{Geun} \rangle}{\langle Y_{Gek} \rangle} \right) \times x_{known}$$

(5. 2)

5.10.2. Method 2

This method does not require the use of a $Si_{1-x}Ge_x$ reference layer, thereby eliminating any errors introduced by using such a standard. For this method, a proportional relationship between the Si ion yields from a $Si_{1-x}Ge_x$ layer to the Si ion yield from a pure Si layer profiled under identical conditions was established. The Ge

fraction is determined by first finding the Si atomic fraction present in the unknown $Si_{1-x}Ge_x$ layer from the relation:

$$Si\ fraction = \frac{Si\ ion\ yield\ from\ unknown\ SiGe\ layer}{Si\ ion\ yield\ from\ Si\ layer}$$

$$(5.\ 3)$$

The Ge atomic fraction is then found by assuming a linear relationship between the Si and Ge present within the layer and may be written as:

$$Ge\ fraction = 1 - Si\ fraction$$

$$(5.\ 4)$$

A set of samples were produced by a semiconductor epitaxial growth specialist for this work and their identification numbers are #23, #24 and #25. Their intended structural formats are given in figure 5.11.

| 30 nm $Si_{0.70}Ge_{0.30}$ |
| Si |
| Si Substrate |

| 100 nm $Si_{0.80}Ge_{0.20}$ |
| Si |
| Si Substrate |

(a) #23

(b) #24

| 200 nm $Si_{0.80}Ge_{0.20}$ |
| Si |
| Si Substrate |
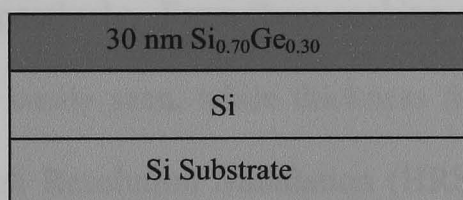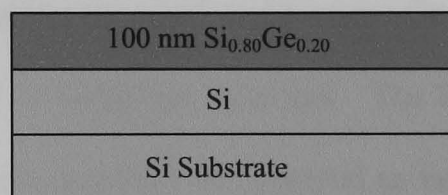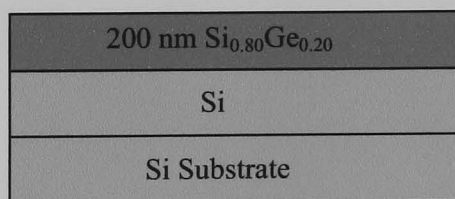
(c) #25

Figure 5.11. Schematic diagrams showing the intended layer structures of the samples grown for Ge quantification.

The samples were received with no calibration data and so the layers had to be quantified by techniques with a proven protocol for determining Ge fractions and layer

thicknesses accurately. The technique applied was High Resolution X-ray Diffraction (HRXRD).

5.11 X-ray quantification

The three samples (#23, #24 and #25) were supplied as 8 inch diameter wafers. The wafers were cleaved and a piece taken from near the centre of each sample was extracted for X-ray analysis. Given the intended SiGe layer thicknesses and their Ge fractions, it was believed that the layers would be relaxed. However, from (004) X-ray rocking curves, all the samples showed typical characteristics of being strained. Figure 5.12 (a), (b) and (c) show the (004) rocking curves for samples #23, #24 and #25 respectively. From these rocking curves sharp Si substrate peaks and broader Ge peaks are easily seen, while thickness fringes indicative of strain are observed. The Philips High Resolution Simulation (HRS) software (which assumes the material to be fully strained), produced simulated rocking curves which accurately overlaid the measured rocking curves. The intensity of the simulation count compared to the measured count has been deliberately reduced so that it is easier to see the accuracy of fit between the respective curves.
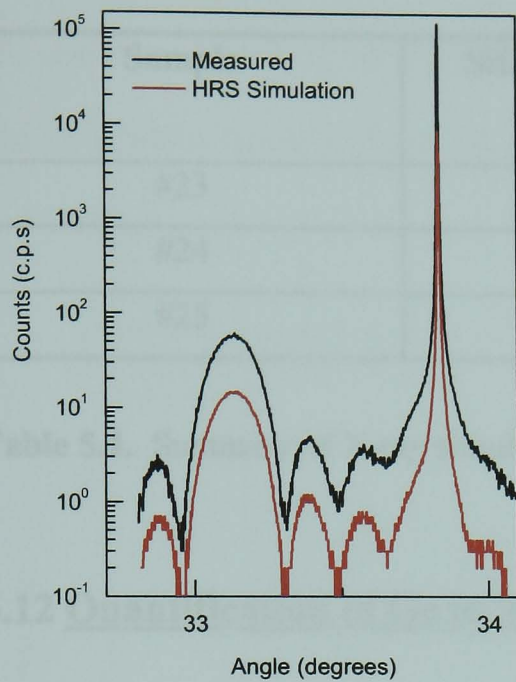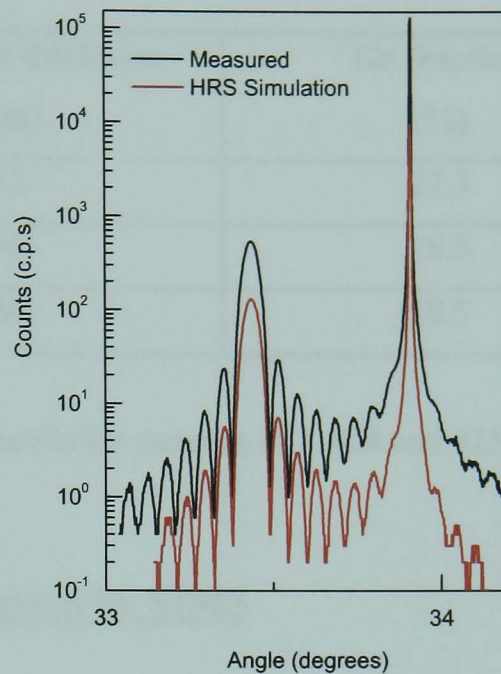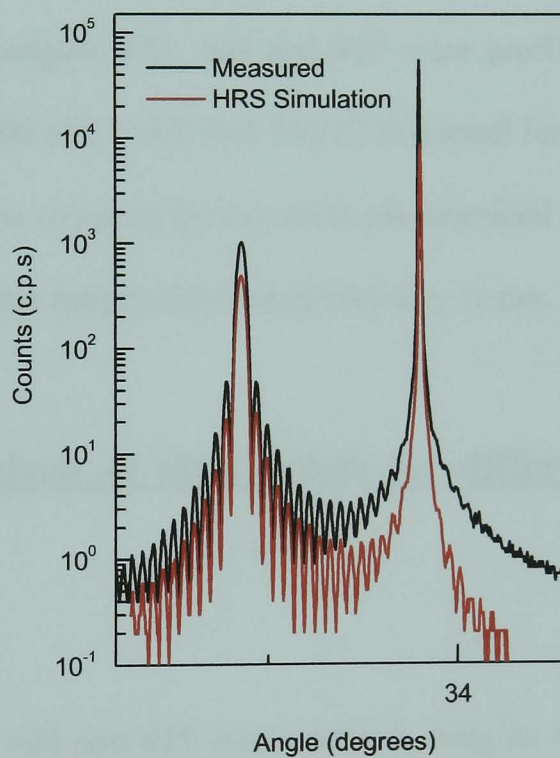
Figure 5.12. Measured X-Ray rocking curves and their HRS simulations for (a) sample #23, (b) sample #24 and (c) sample #25.

From the simulations the actual layer structures were deduced and the results given in table 5.4. All three results are believed to be within ±1 atomic %.

Sample	SiGe layer thickness (nm)	Ge fraction (%)
#23	31	27.3
#24	98	18.5
#25	198	18.5

Table 5.4. Summary of X-ray simulation results for samples #23, #24 and #25.

5.12 Quantification of Ge in SiGe layers by SIMS

Having used an independent method for the quantification of the Ge fraction within the SiGe layers, samples #23, #24 and #25 were profiled under a number of primary beam energies (500 eV, 1 keV and 3 keV) at normal incidence. These profiles were carried out in order to compare the two methods described in section §5.10 for the determination of Ge with the independent result found by X-ray.

5.12.1 Ge SIMS analysis of SiGe layers for different primary beam energies

The samples #23, #24 and #25 were profiled using an O_2^+ incident beam with charge compensation in the form of the red laser diode (635 nm). Sample DN0 was also profiled under the same conditions so that the $Si_{0.8}Ge_{0.2}$ layer closest to the surface could be used for reference in the case of applying method 1 to the data. TSMC had previously characterised sample DN0 by RBS and they specified the layer to be $Si_{0.8}Ge_{0.2}$. The Ge fraction data from TSMC was believed to be accurate to within ±1

atomic %. Figures 5.13 (a), (b), (c) and (d) show the 500 eV profiles of sample #23, #24 and 25 and DN0, figure 5.14 (a), (b), (c) and (d) the 1 keV profiles of #23, #24, #25 and DN0 while figure 5.15 (a), (b), (c), and (d) the 3 keV profiles of #23, #24 and #25 and DN0.
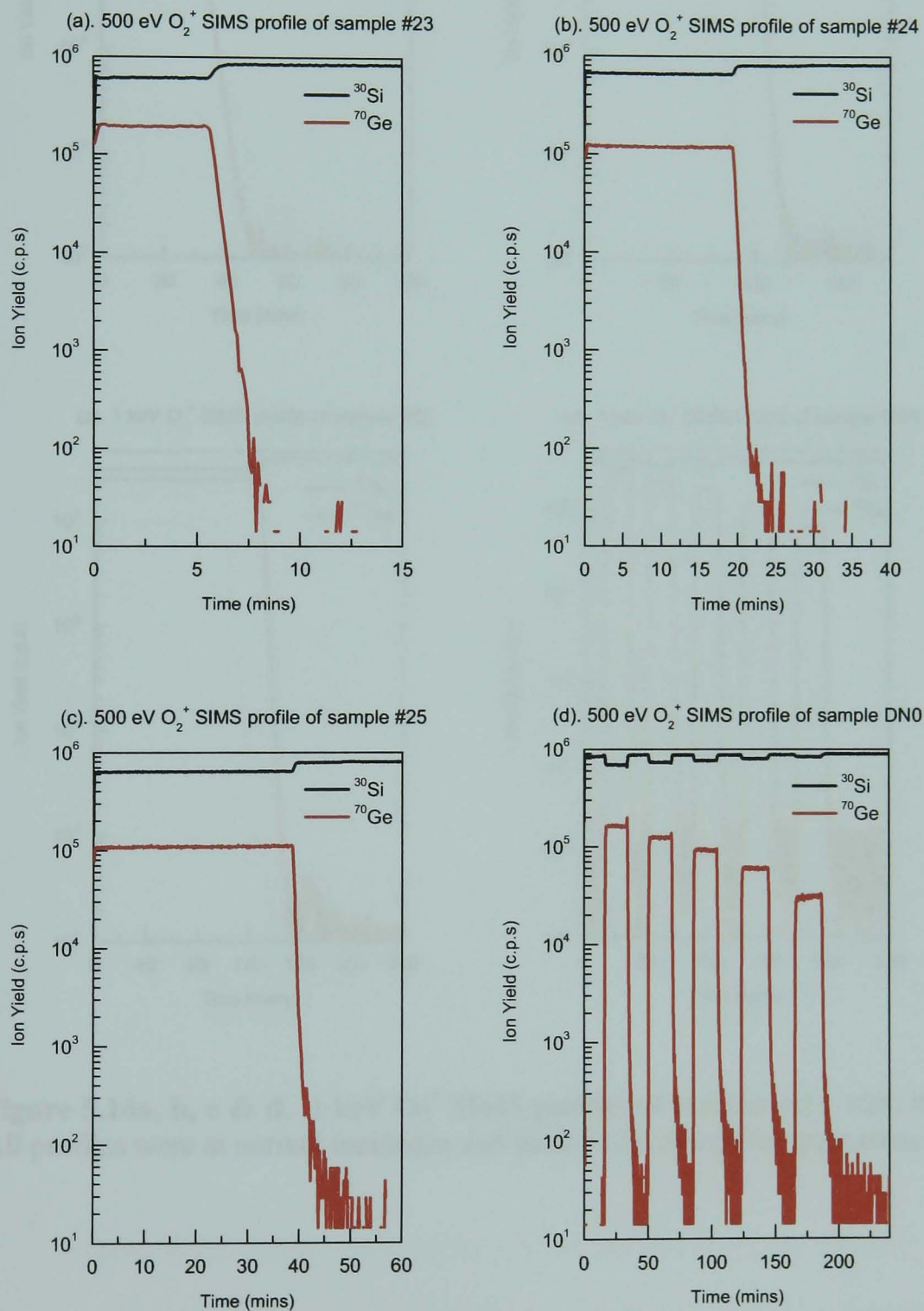
Figure 5.13a, b, c & d. 500 eV O_2^+ SIMS profiles of samples #23, #24, #25 and DN0. All profiles were at normal incidence and laser diode charge compensation applied.
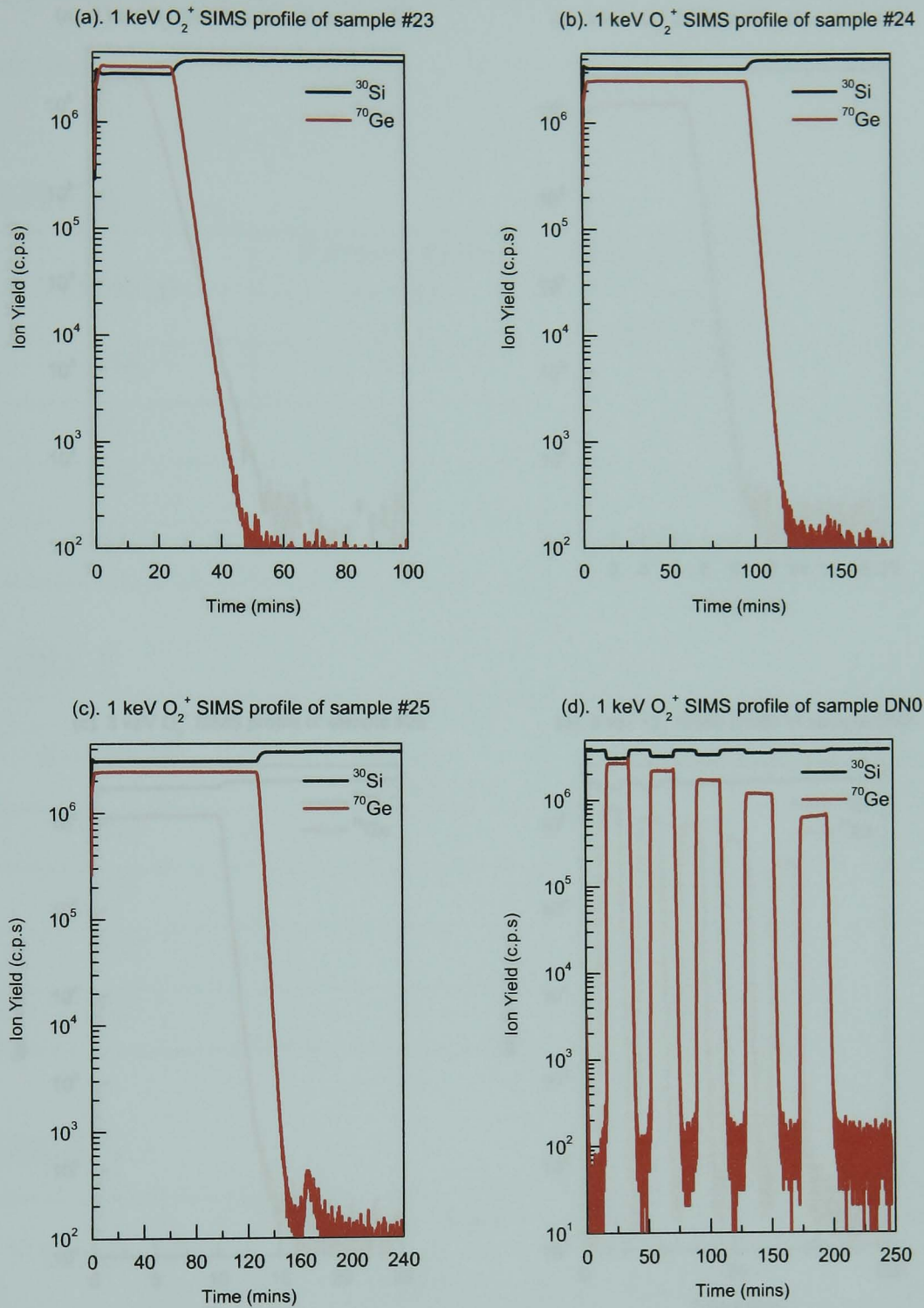
Figure 5.14a, b, c & d. 1 keV O_2^+ SIMS profiles of samples #23, #24, #25 and DN0. All profiles were at normal incidence and laser diode charge compensation applied.
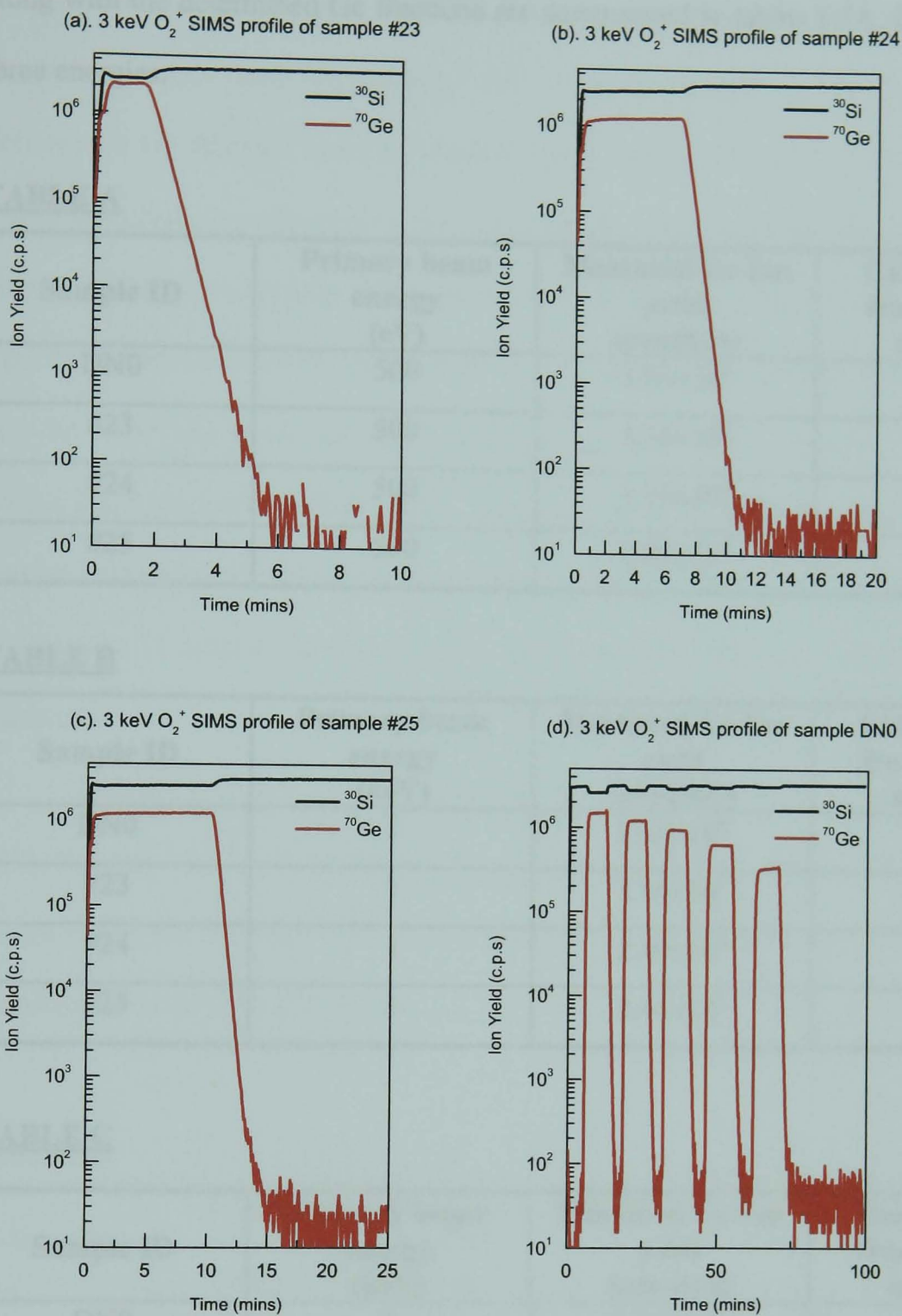
Figure 5.15a, b, c & d. 3 keV O_2^+ SIMS profiles of samples #23, #24, #25 and DN0. All profiles were at normal incidence and laser diode charge compensation applied.

From these profiles the mean Ge ion yields from the plateau regions were determined. In the case of sample DN0, the plateau region used was that of the $Si_{0.8}Ge_{0.2}$ layer. By applying method 1 and equation 5.2 (section §5.10.1), the Ge fraction for samples #23, #24 and #25 was determined. The measured Ge ion yields

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along with the determined Ge fractions are summarised in tables 5.5A, B and C for all three energies.

TABLE A

Sample ID	Primary beam energy (eV)	Measured Ge Ion yield (counts/s)	Calculated Ge fraction using method 1
DN0	500	1.63×10^5	-
#23	500	1.94×10^5	0.238
#24	500	1.19×10^5	0.146
#25	500	1.09×10^5	0.134

TABLE B

Sample ID	Primary beam energy (keV)	Measured Ge Ion yield (counts/s)	Calculated Ge fraction using method 1
DN0	1	2.68×10^6	-
#23	1	3.34×10^6	0.249
#24	1	2.49×10^6	0.186
#25	1	2.44×10^6	0.182

TABLE C

Sample ID	Primary beam energy (keV)	Measured Ge Ion yield (counts/s)	Calculated Ge fraction using method 1
DN0	3	1.52×10^6	-
#23	3	2.10×10^6	0.276
#24	3	1.22×10^6	0.16
#25	3	1.19×10^6	0.157

Tables 5.5. (A), (B), (C). Summary of Si ion yields and calculated Ge fractions for samples #23, #24 and #25 using Method 1

From the results given in tables 5.5A, B and C, the calculated Ge fractions for the same sample vary significantly for different energies. The variation of the determined Ge fraction between primary beam energy ranges between 4-26%. The results also show significant deviation from the Ge fractions determined by X-ray, with only a couple of the results falling within the experimental error of the X-ray results. This large error is believed to arise from non-uniformity across the sample holder which may be either due to the samples not lying perfectly flat on the holder or the sample holder itself not being perfectly flat. In either case there will be a difference in angle between each sample and the incident beam and secondary detection column leading to a variation in emitted secondary ions and collection efficiency between individual samples.

Having analysed the profiles using method 1, the profiles of all three samples (#23, #24 and #25) were further analysed using method 2 (§5.10.2). The mean Si ion yields along with the calculated Si and Ge fractions for all three different energies are summarised in tables 5.6A, B, and C.

TABLE A

Sample	Primary beam energy (eV)	Si ion yield from SiGe layer (Counts/s)	Si ion yield from bulk (Counts/s)	Si Fraction (%)	Ge Fraction using method 2 (%)
#23	500	6.08×10^5	8.57×10^5	71	29
#24	500	6.62×10^5	8.19×10^5	80.7	19.3
#25	500	6.37×10^5	8.02×10^5	79.6	20.6

TABLE B

Sample	Primary beam energy (keV)	Si ion yield from SiGe layer (Counts/s)	Si ion yield from bulk (Counts/s)	Si Fraction (%)	Ge Fraction using method 2 (%)
#23	1	2.84×10^6	3.92×10^6	72.4	27.6
#24	1	3.22×10^6	3.20×10^6	80.7	19.3
#25	1	3.07×10^6	3.77×10^6	81.4	18.6

TABLE C

Sample	Primary beam energy (keV)	Si ion yield from SiGe layer (Counts/s)	Si ion yield from bulk (Counts/s)	Si Fraction (%)	Ge Fraction using method 2 (%)
#23	3	2.44×10^6	3.26×10^6	74.9	25.1
#24	3	2.54×10^6	3.10×10^6	82	18
#25	3	251×10^6	3.03×10^6	82.7	18.3

Tables 5.6 A, B and C. Summary of Si and Ge ion yields along with the calculated Si and Ge fractions for samples #23, #24 and #25 using Method 2.

From the results given in tables 5.6 A, B and C, the Ge fractions for each sample show far less variation between different beam energies as well as appearing to agree well with the previously determined X-ray results. All the results except for the 3 keV measurement of sample #23 fall within the experimental error of the X-ray results (±1 atomic %). The 3 keV Ge fraction determined by SIMS for sample #23 showed a difference of ~8% compared to the measured X-ray result. The improved accuracy appears to reaffirm the possibility that a variation across the samples holder was the main reason for the loss of accuracy by using method 1

In order to further quantify the accuracy of method 2, the procedure was used to quantify the Si and Ge fractions for all five SiGe layers within the TSMC sample DN0 at all three beam energies. Tables 5.7 A, B and C summarise the measured ion yields at different beam energies for the various layers along with the determined Si and Ge fractions for each layer.

Table A

Intended layer Ge fraction (%)	Mean Si ion yield from SiGe layer (counts)	Mean Si ion yield from bulk Si (counts)	Si fraction (%)	Ge Fraction using method 2 (%)
20	7.10×10^5	8.84×10^5	80.2	19.8
16	7.37×10^5	8.84×10^5	83.4	16.6
12	7.67×10^5	8.84×10^5	86.8	13.2
8	8.13×10^5	8.84×10^5	92	8
4	8.42×10^5	8.84×10^5	95.2	4.8

Table B

Intended layer Ge fraction (%)	Mean Si ion yield from SiGe layer (counts)	Mean Si ion yield from bulk Si (counts)	Si fraction (%)	Ge Fraction using method 2 (%)
20	3.07×10^6	3.80×10^6	80.8	19.2
16	3.21×10^6	3.80×10^6	84.5	15.5
12	3.32×10^6	3.80×10^6	87.5	12.5
8	3.53×10^6	3.80×10^6	93	7
4	3.67×10^6	3.80×10^6	96.7	3.3

Table C

Intended layer Ge fraction (%)	Mean Si ion yield from SiGe layer (counts)	Mean Si ion yield from bulk Si (counts)	Si fraction (%)	Ge Fraction using method 2 (%)
20	2.62×10^6	3.32×10^6	78.8	21.2
16	2.81×10^6	3.32×10^6	84.5	15.5
12	2.90×10^6	3.32×10^6	87.4	12.6
8	3.07×10^6	3.32×10^6	93.5	6.5
4	3.18×10^6	3.32×10^6	95.6	4.4

Tables 5.7 (A), (B), (C). Summary of Si ion yields from SiGe layers and bulk Si ion yields along with the calculated Si and Ge fractions for sample DN0 using Method 2.

From the results given in tables 5.7A, B and C, the Ge fractions calculated for the 500 eV and 1 keV profiles are all found to fall within experimental error of the values given for the structure by it manufacturer (±1 atomic %). However, the 3 keV profiles once again show more deviation in accuracy with a difference of up to 6% being observed for some of the determined layers.

5.13 Summary

The Ge fractions of a set of SiGe layers (samples #23, #24 and #25) were determined by applying two methods of analysis to the raw profile data. The method (method 2) whereby the Ge was determined directly from the ratio of Si ion yields lead to accurate results within the experimental error of values previously obtained by X-ray analysis. Such strong agreement is believed to originate from the direct use of ion yields from the same sample and not using a separate sample as reference. By using a

reference sample, as in the case of method 1, an error from its measurement will be introduced directly. This error is most likely to arise from a variation between the samples holders mounting holes for individual samples leading to a difference in ionisation yield, whilst another possibility although less likely, is the reference material having a slightly different matrix stoichrometry compared to the unknown sample. Such an error will be carried through to the analysis yielding inaccurate results. The results obtained using method 2 was found to be more accurate for the lower incident beam energies, namely 500 eV and 1 keV. The results obtained when the incident beam energy was raised to 3 keV were found to deviate from the independently measured X-ray values by more than the experimental error. At present the reason for this loss of accuracy are still not known.

Method 2 was also applied to the SiGe multilayer structure DN0. The individual layers had been previously quantified by the manufacturer and the SIMS analysis once again showed very good agreement for the 500 eV and 1 keV measurements but the 3 keV analysis was again found to fall outside the specified layer values and their known error.

5.14 Conclusion

A successful protocol for the determination of Ge fraction within $Si_{1-x}Ge_x$ layers with x ranging from 0 to 0.3 has been clearly demonstrated for incident beam energies $\leq 1keV$. The successful protocol compared the ratio of Si ion yield from an unknown SiGe layer to the Si ion yield from bulk Si standard. The results were found to yield values for the Ge fraction to within the known error ($\pm$ 1 atomic %) of the layer values determined by an independent technique.

The outcome of this work allows the accurate determination of *both* the Ge content and the Ge spatial distribution to be obtained from a single SIMS measurement. To date, whilst SIMS has been extensively used for the determination of Ge spatial distributions within a sample, further characterisation techniques (HRXRD) have been required to obtain an accurate determination of the absolute Ge content. Furthermore, the determination of Ge fraction using the above technique requires a relatively small sample area, typically 100 μm^2, compared to the large sample area required for HRXRD analysis, typically 10mm^2. The reduction in characterisation area will have profound consequences in the die-per-wafer yield of SiGe device circuitry.

5.15 <u>Further work</u>

The current work identifies an accurate method of determining the Ge fraction of SiGe samples with Ge contents <30%, using analytical SIMS techniques. Due to the increasing importance of higher Ge fractions within advanced substrates, it is the author's opinion that the methodology presented in this chapter should be extended to enable the quantification of SiGe samples with Ge fractions exceeding 30%.

6. Summary

The work carried out on optimising a strained Ge channel heterostructure was the first time such research had been undertaken at Warwick. Previous work had been focused primarily on psuedomorpic $Si_{1-x}Ge_x$ layers (x up to 0.36) on Si substrates [Grasby et al, 1999] along with an initial study of a strained $Si_{0.2}Ge_{0.8}$ layer on a $Si_{0.65}Ge_{0.35}$ VS [Myronov et al, 2002]. Given the predicted enhanced transport properties of the strained Ge channel Heterosystem, due to the benefits of lower effective carrier mass and elimination of alloy scattering, work on the Ge channel was undertaken with the aim of demonstrating improved hole transport properties.

The initial work involved producing the VS and strained Ge heterostructure by SS-MBE. Given the growth duration of thick layers using SS-MBE and the inherent source depletion problems associated with e-beam systems, a decision to keep the VS to <2 μm was taken. A series of identical strained Ge (8 nm) heterostructures were produced on a range of VS's with varying thicknesses (150 nm-2 μm). XTEM analysis showed that the VS's contained a very high dislocation density throughout which made them unsuitable for growth of a high quality Ge heterostructure. AFM of the sample surfaces showed that the surface morphology of the layers contained large roughening, with typical rms roughness values of 10-150 nm, bordering on 3-D growth and pits believed to have arisen from atomic mass transport mechanisms. Evidence of quantum confinement (2DHG behaviour) was observed from Hall measurements in the temperature range of 10-300 K. The hole mobility results ranged between 500-800 cm^2/Vs at room temperature and 2000-8000 cm^2/Vs at 10 K which were inferior to previously published results for similar structures. The analogous record

value for such a heterostructure was recorded by Känel *et al* who demonstrated a Hall mobility of 87,000 cm^2/Vs at 4K [Känel *et al*, 2002].

A new *'hybrid-epitaxy'* approach of combining pre-grown high quality CVD VS's with SS-MBE for the 8 nm strained Ge heterostructure was adopted, alleviating the source depletion problems and time constraints for growing a high quality thick VS. The first problem encountered was pre-cleaning of the VS prior to heterostructure growth. Initial Si based cleans employing RCA stages I and II were found to be too aggressive given the high Ge content of the VS's (60-70% Ge). Structural analysis by XTEM showed the re-growth interface to be a nucleation source for dislocations leading to either no 2DHG behaviour or a 2DHG with extremely poor electrical properties. X-ray analysis further demonstrated that the clean combining both RCA stages I and II had etched away large amounts of the starting VS prior to SS-MBE re-growth. A chemical clean known as the "Piranha etch" was found to be less reactive with the VS and by combining this with a high temperature re-growth a good quality interface between the VS and SS-MBE material was achieved.

Hall measurements of the heterostructure using the Piranha etch and high re-growth temperature were found to be once again inferior to previously published results with a room temperature mobility of ~450 cm^2/Vs and a 10 K mobility ~3000 cm^2/Vs. XTEM measurements indicated that the upper interface of the Ge channel had severely roughened. 1D Poisson/Schrödinger modelling suggested that the upper interface of the 8 nm channel had a very strong influence on the confined carriers. Such roughening has been observed previously at increased growth temperatures and attributed to elastic relaxation of the strained layer [Cullis *et al*, 1994, Xie *et al*, 1993].

A series of samples were produced using identical chemical pre-cleans and re-growth conditions. However, various growth temperature ramps were implemented

so as to minimise the growth temperature of active layer. An optimised growth procedure using a 30 minute growth interrupt was found to suppress the temperature-induced roughening. By suppressing the roughening of the upper channel interface a 2.5 times increase in 10 K mobility and 2 times enhancement in 300 K mobility was demonstrated. Further samples were produced using the optimised growth process in which the channel thickness was varied from 16 nm to 30nm. Roughening of the upper interface was once again observed from XTEM in the thicker channels (<16 nm). In the case of the thicker channels, interface roughening was again observed and was attributed to elastic relaxation due to excessive strain build up in channels which significantly exceeded the critical thickness. In addition, plan view TEM of such structures indicated the onset of plastic relaxation due to the nucleation of misfit dislocations at the lower in channel interface. 1D Poisson/Schrödinger modelling of the thicker channel structures suggested that the upper channel interface had very little influence on the confined carriers.

Given the low growth temperature the carrier mobility of the material was believed to be compromised due to the inclusion of as-grown point defects. Post-growth annealing of the heterostructures demonstrated a significant improvement in carrier mobility and an optimised post-growth annealing procedure of 650°C for 30 minutes under dry N_2 was demonstrated. Increased Hall mobilities of 26,900 cm^2/Vs at 10 K and 1910 cm^2/Vs at room temperature were observed.

Due to the spatial separation of the as-grown remote impurity ions from the 2DHG confinement channel, Hall mobility measurements on such heterostructures provide a net carrier mobility made up from components derived from the confined quantum gas together with the parallel conduction paths of the remote impurity ions [Kiatgamolchai, 2000]. Magneto-conductivity transformation measurement and

maximum entropy mobility spectrum analysis enable the separation of the individual carrier layer mobilities at room temperature allowing the channel mobility to be extracted. Mobility spectrum analysis demonstrated a room temperature hole mobility of 2700 cm^2/Vs at a carrier density of 1.0×10^{12} cm^{-2}, compared to an analogous mobility of just 200 cm^2/Vs typically observed in bulk silicon. These results show a strong indication that Ge channel devices have the potential to yield significant improvements over current state-of-the-art Si based CMOS devices.

The second part of this thesis involved the quantification of $Si_{1-x}Ge_x$ layers ($x \leq 0.3$) using SIMS. However, due to the highly intrinsic nature of undoped SiGe epitaxial layers, accurate profiles were unobtainable using conventional SIMS techniques. The problem encountered was a significant distortion of the true profile shape due to charging effects during ion bombardment. The charging was believed to originate from the low residual carrier concentration leading to a large spreading resistance within the SiGe layer. A novel technique employing the illumination of the sample surface during SIMS profiling with a red laser was used to generate electron-hole pairs. In this manner, local charging effects were eliminated and accurate SIMS profiles of highly intrinsic SiGe layers were obtained. The laser wavelength and minimum power density were determined to be 1.1 μm and >0.54 mW mm^{-2} respectively. The demonstrated results offer excellent charge compensation capabilities over a significant range of beam energies, beam currents and incident beam angles and provides a significant improvement in the capability of conventional SIMS analytical techniques.

Having overcome the charging problem, the determination of Ge concentration using SIMS profiles was initiated. The first method (method 1) profiled a previously calibrated piece of $Si_{1-x}Ge_x$ material where x is known under identical conditions to that

of the unknown $Si_{1-x}Ge_x$ layer. To obtain the unknown Ge fraction the mean Ge ion yield from the unknown sample is divided by the mean Ge ion yield of the known sample before being multiplied by the known samples Ge fraction.

The second method (method 2) initially determines the Si fraction by assuming a proportional relationship between the mean Si ion yields from an unknown $Si_{1-x}Ge_x$ layer to the mean Si ion yield from a pure Si layer profiled under identical conditions. Once the Si fraction is determined the Ge fraction is obtained by assuming a linear interpolation between the endpoints of the SiGe alloy.

Having applied the two analytical methods, method 2 demonstrated results within the experimental error of independent analysis (HRXRD) of the same samples. The results obtained were found to be more accurate for lower incident beam energies, namely 500 eV and 1 keV. When the incident beam energy was raised to 3 keV the results were found to deviate from the independently measured X-ray values by more than the experimental error. The outcome of this work allows the accurate determination of *both* the Ge content and the Ge spatial distribution to be obtained from a single low energy SIMS measurement

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