PHASE NOISE REDUCTION TECHNIQUES FOR RF SIGNAL GENERATOR

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Summary

Nowadays, the demand for more communication channels and higher data rate in digital transmission systems has established a need for lower timing jitter or phase noise. Timing jitter is the unwelcome companion of all communication systems that use voltage transitions to represent timing information. In the frequency domain, phase noise or sideband noise of the local oscillator degrades the dynamic range of the radio receivers. This research investigates and introduces new techniques to reduce the unwelcome effects of the phase noise and timing jitter.

In the frequency domain sideband noise reduction techniques, such as transposed gain amplifiers and the transposed gain oscillator are investigated and studied in detail. It was found that the convolving of the primary local oscillator and its re-generated offset frequency make the phase noise reduction possible. From studies, it is shown that the oscillating waveforms play an important role in the noise modulation sensitivity of the oscillator. A new structure of the transposed gain amplifier is also introduced. It has a low pass frequency response and the transposed gain oscillator based on this amplifier can have, in theory, the LO noise suppression performance down to system noise floor without path delay difficulties.

The novel jitter reduction circuit based on time domain averaging techniques is introduced. The timing variation of the signal is converted into the zero crossing jitter and integrated by analog integrators. The novel technique employs the averaging on both leading and trailing edges. This new jitter reduction shows 6dB per octave attenuation of the signal's sideband frequency and does not depend on the type of analog integrator being used. The structure of the circuit is cascadable for higher sideband noise reduction. It is possible to implement this technique using integrated circuit technologies.

To my parents,

to Phetngarm, Wanpatchanee,

and to

all of my teachers.

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Contents

List of Publications

[1] M. J. Underhill, S. Bunnjaweht and I. D. Robertson, " Investigation of Transposed Gain Oscillators using Low Frequency Limiters and AJC Jitter Suppression Tecnology," *Proceeding 16th EFTF*, St. Petersburg, March 2002.

[2] M. Chongcheawchamnan, S. Bunnjaweht, D. Kpogla, D. W. Lee and I. D. Robertson, " Microwave I-Q Vector Modulator Using a Simple Technique for Compensation of FET Parasitic," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 6, pp. 1642-1646, June 2002.

[3] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, " Sideband Noise Reduction in Transposed Gain Oscillators, " *IEEE Proceeding ISCAS2003*, May 2003.

[4] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, " IF-LO Delay Mismatch and Noise Reduction in Transposed Gain Oscillator," *Proceeding EFTF18th*, April 2004.

[5] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, " Novel Jitter and Phase Noise Reduction Circuit, " *Proceeding EFTF18th*, April 2004.

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List of Abbreviations

ADS	Advanced Design System (Agilent)
AJC	Anti Jitter Circuit
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
dB	Decibel
dBc	Decibel relative to carrier
dBm	Decibel relative to 1 mW
FCS	Frequency Control Symposium
EFTF	European Frequency Time Forum
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FM	Frequency Modulation
GaAs	Gallium Arsenide
GHz	Giga Hertz
GPS	Global Positioning System
HP	Hewlett Packard
Hz	Hertz
IC	Integrated Circuits
IF	Intermediate Frequency
IMD	Intermodulation Distortion
ISF	Impulse Sensitivity Function
LNA	Low Noise Amplifier
LF	Low Frequency
LO	Local Oscillator
LP-TGA	Low Pass Response Transposed Gain Amplifier
LTI	Linear Time Invariance
mA	Milli Ampere
mW	Milli Watt
MHz	Mega Hertz

ns	Nano Second
PLL	Phase Locked Loop
PM	Phase Modulation
p-p	Peak-to-Peak
PSD	Power Spectral Density
PTFE	Poly Tetra Fluoro Ethylene
RF	Radio Frequency
rms	Root Mean Square
SPICE	Simulation Program with Integrated Circuit Emphasis
TGA	Transposed Gain Amplifier
TGO	Transposed Gain Oscillator
UFFC	Ultrasonics Ferroelectrics and Frequency Control
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
WJ	Watkins Johnson

Chapter 1

Introduction

The recent exponential growth in wire and especially wireless communication has increased the demand for more available channels and higher data rate in communication systems. This demand has dictated higher phase noise performance of the local oscillator circuits. In the digital communication systems, lower jitter clock generators are required. The importance of low noise signal generation is easy to understand when one realises that it is phase noise that degrades the quality of data transmission, limits the precision of the GPS systems, degrades the picture quality of the television, reduces the operating range of radar. The importance of phase noise in signal generators has made it one of the most extensively studied subjects in electronics. Phase and frequency fluctuations have therefore been the subject of numerous studies [1.1-1.9]. During the last four decades, there are many analysis models and design methods concerning frequency instability of the oscillator or its phase noise.

1.1 Frequency Instability

Any practical oscillator has fluctuations in its amplitude and frequency. Frequency instabilities and amplitude fluctuations of an electrical oscillator are mainly due to noise and interference sources. Thermal, shot and flicker noise in electronics devices are sources of the first group. Power supply noise, substrate noise (integrated circuits) and electromagnetic interference are examples of the second group. The frequency instabilities can be characterised in different ways. Jitter and phase noise are the most commonly used parameters for quantifying frequency instabilities.

1.1.1 Instability in the Frequency Domain

An ideal oscillator should give output as $V_{out}(t) = V_o cos[\omega_o t + \phi_o]$, where the amplitude V_o, the frequency ω_o, and phase reference ϕ_o are all constants. The one side spectrum of an ideal oscillator with no random fluctuations consists of an impulse at

ω_o as shown in Figure 1.1. But, the output of a practical oscillator is more generally given by:-

$$V_{out}(t) = V_O[1 + A(t)]f[\omega_O t + \phi(t)] \tag{1.1}$$

where $\phi(t)$ and $A(t)$ are functions of time, V_o is the maximum output voltage and f is a periodic function which represents the shape of the steady-state output waveform of the oscillator.

The output signal has a power spectrum with harmonics of ω_o if the waveform f is not sinusoidal. The fluctuations represented by $\phi(t)$ and $A(t)$ give rise to sidebands close to the frequency of oscillation, ω_o, and its harmonics. These sidebands are generally called phase noise sidebands.

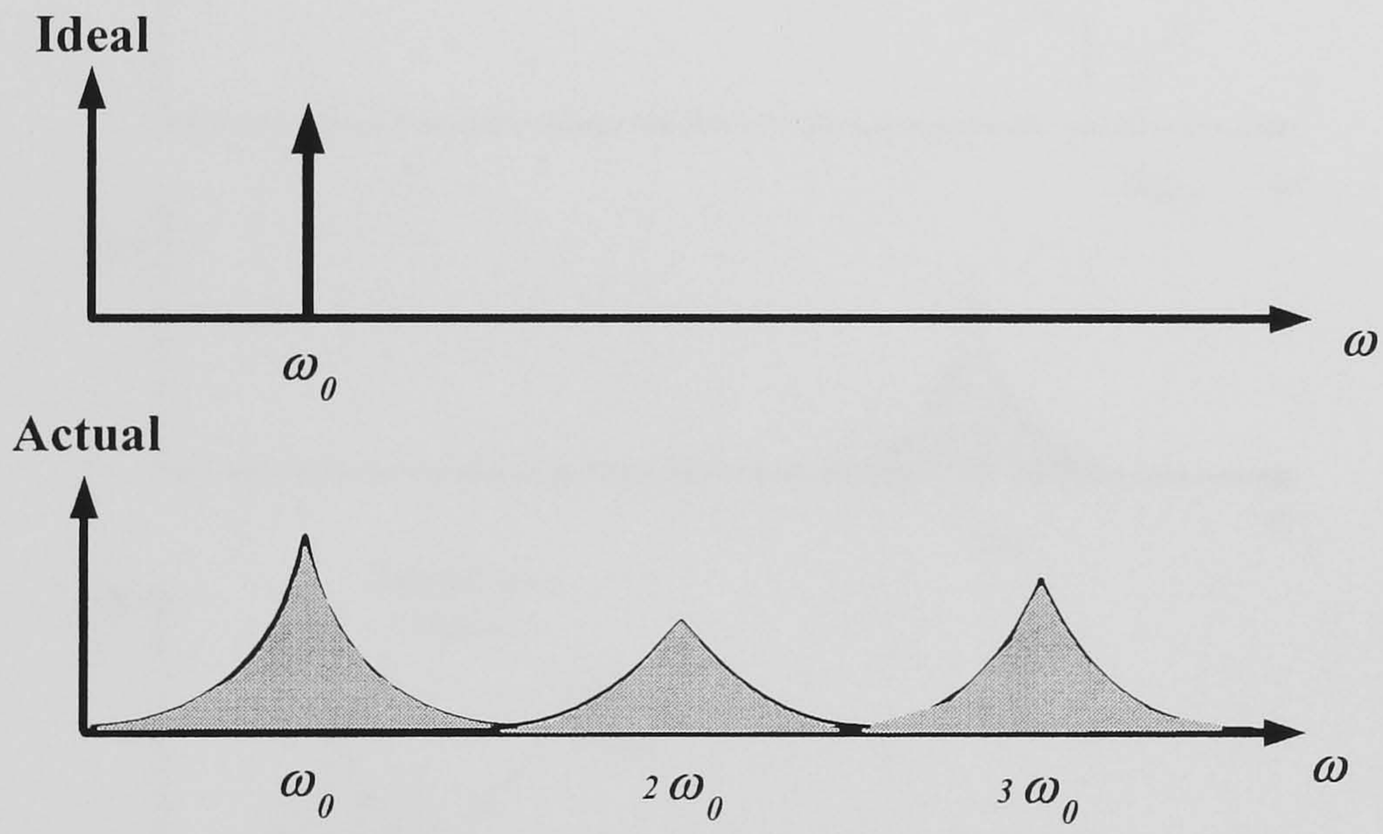


Figure 1.1 Spectrum of an ideal and practical oscillator.

The adverse effect of phase noise can be seen in the front-end of a superheterodyne - receiver. Figure 1.2 shows a typical front-end block diagram, consisting of a low noise amplifier (LNA), a mixer and a local oscillator (LO). Suppose the receiver tunes to a weak signal in the present of a strong signal in an adjacent channel. If the LO has large phase noise, as shown in Figure 1.3, some down conversion of the interfering signal into the same IF (intermediate frequency) as that of the desired signal will occur as shown in Figure 1.3. The resulting interference greatly degrades the dynamic

range of the receiver. Therefore, improving the phase noise of the oscillator clearly improves the signal-to-noise ratio of the desired signal.

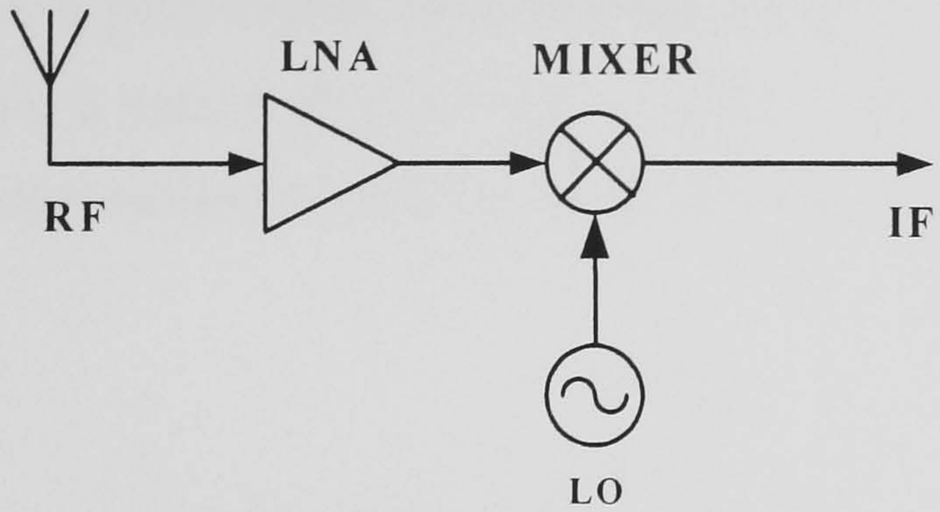


Figure 1.2 Typical front-end block diagram.

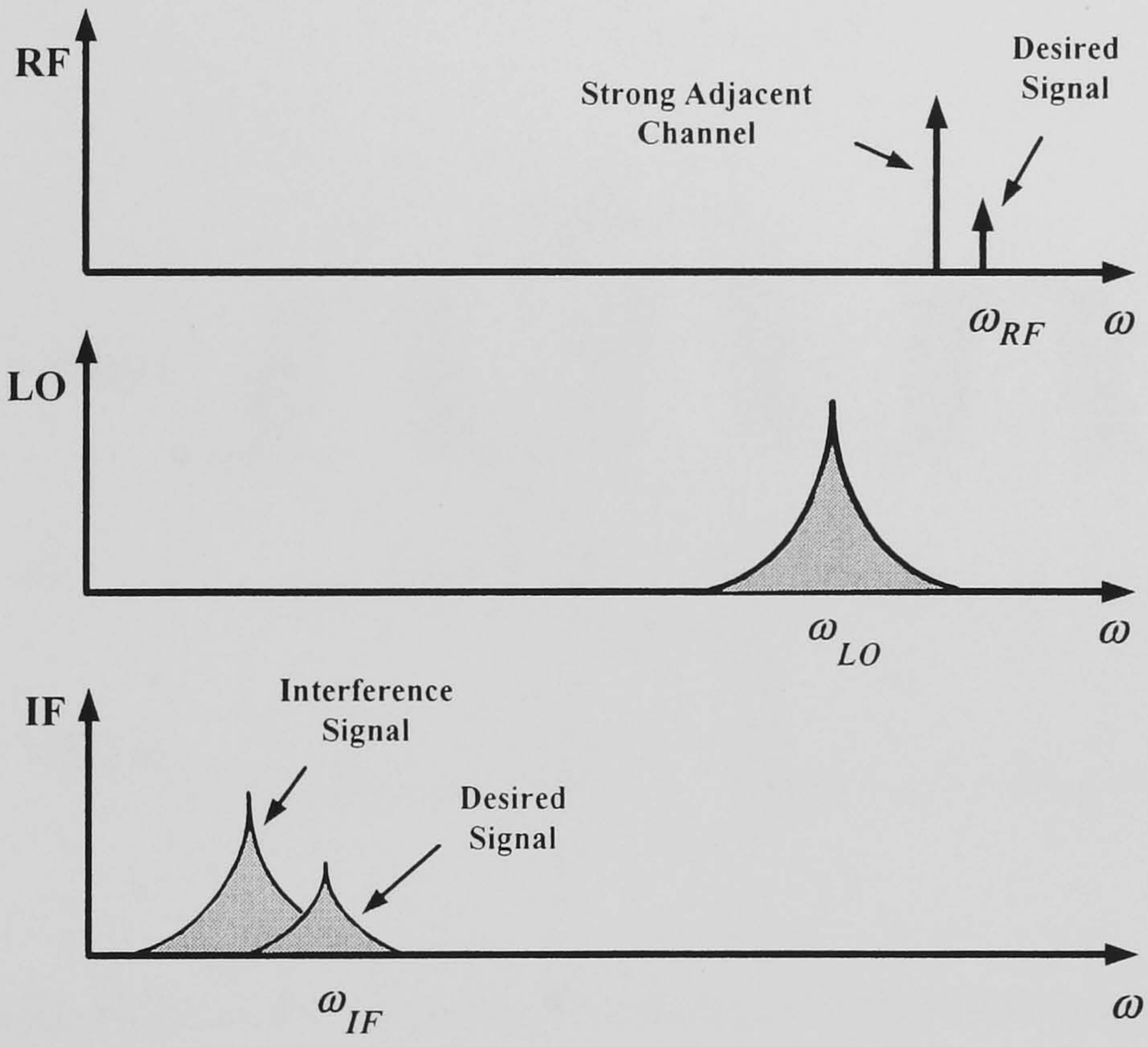


Figure 1.3 Effect of phase noise in presence of adjacent strong signal.

1.1.2 Instability in the Time Domain

From the time domain viewpoint, the spacing between clock signal transitions is ideally constant. In reality, however, the transition spacing will be variable due to fluctuation in $\phi(t)$. This uncertainty is known as timing jitter, which is shown in Figure 1.4(b). In synchronous digital circuits such as a microprocessor or data transmission systems, there are clock signals that control the operation of different

logic blocks. The importance of timing jitter can be seen from a simple flip-flop circuit in Figure 1.4(a). If the clock signal has zero timing jitter as shown with the solid line in Figure 1.4(b), the data needs to be stable only for $t_{setup} + t_{hold}$. However, if the clock line shows a peak-to-peak zero crossing deviation of τ_{max}, then the data needs to be stable for a period of $t_{setup} + t_{hold} + 2\tau_{max}$. This decrease in the timing margins will reduce the maximum operating speed of a microprocessor circuit.

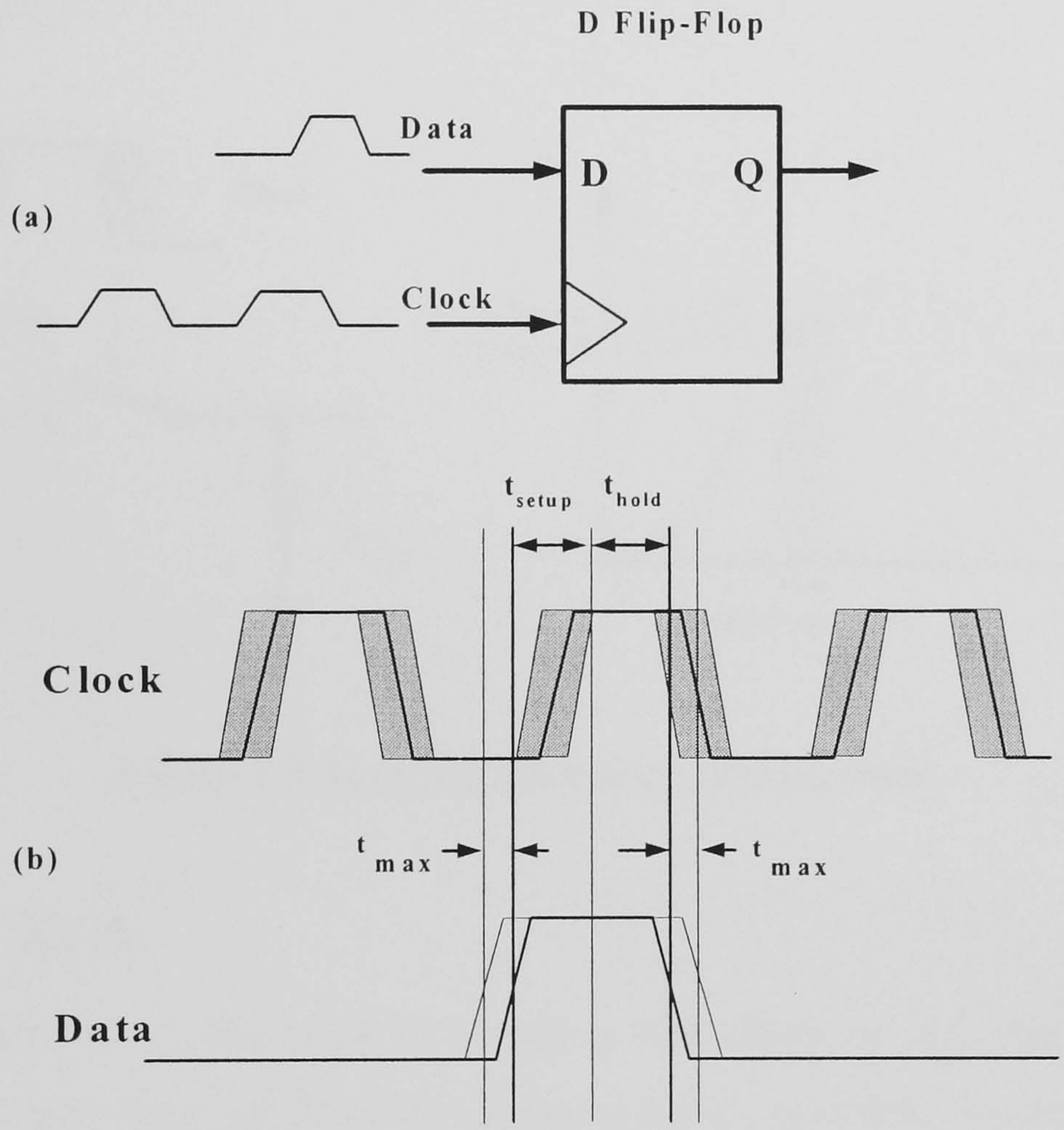


Figure 1.4 Flip-flop in a digital circuit (a) and the effect of timing jitter in a digital system (b).

Another example of the destructive effect of clock jitter can be seen in a data acquisition system. Figure 1.5 shows a sample-and-hold circuit, in which the accuracy of the sampling process is affected by jitter in the clock signal. The uncertainty in sampling time is translated directly to uncertainty in the sampled value of output signal.

In practical situations, both amplitude $A(t)$ and phase $\phi(t)$ disturbances are physical noise. The primary characteristic of noise is its randomness, this is due to the physical

mechanisms which generate it. Three leading types of noise are to be found in all electronics systems. They are; 1) thermal noise: random motion of the carriers in the conductor 2) shot noise: random flow of the carriers through a potential barrier 3) flicker noise: its origin is not well characterised, however it seems to come from the macroscopic defects of the material. To characterise these noise sources, one must refer to the theory of random variables and stochastic processes. The mathematical tools will be simplified by making assumptions according to the statistical properties of the disturbances.

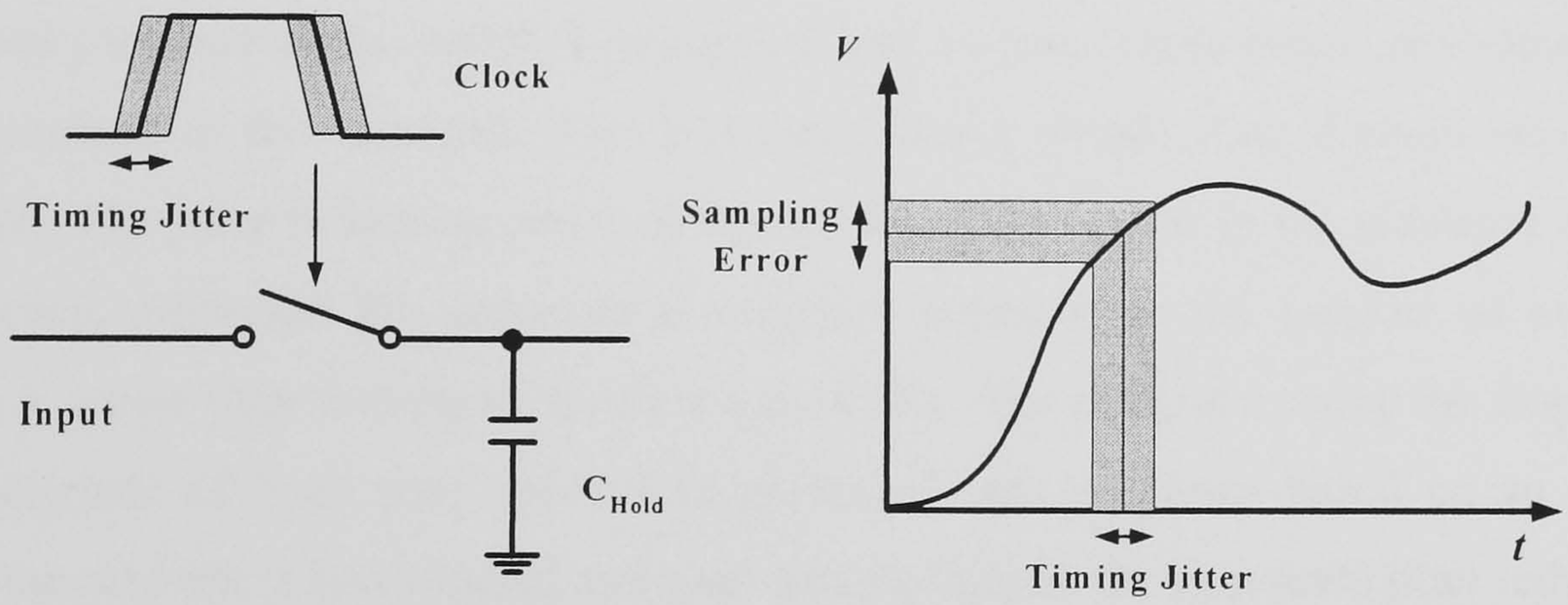


Figure 1.5 Sampling error due to timing jitter.

1.2 Novel Work

The main objective of this work is to reduce the effect of $\phi(t)$, the phase noise disturbance, in both time and frequency domains. In this research, two noise reduction methods are undertaken. The techniques are transposed gain oscillators and the jitter reduction circuits. The transposed gain oscillator offers a unique method of noise reduction of it primary LO (local oscillator). Low noise microwave oscillators can be implemented using a low frequency amplifier based on silicon devices.

It is the convolution process in the transposed gain oscillator that made possible the LO sideband noise reduction mechanism. The LO phase noise suppression mechanism has been quantitatively characterised in this research. The research also shows that the usage of the upper sideband signal of the transposed gain oscillator as an output signal with the LO noise suppressed is feasible. This feature enhances the

utility of the oscillator since it can give an output signal at a frequency higher than the pumped LO signal.

The DC (direct current) response transposed gain amplifier and oscillator are introduced. The LO amplifier has a low pass characteristic even though the main amplifier is a band pass response amplifier. In theory, the transposed gain oscillator using a new transposed gain amplifier can give suppression of the LO sideband noise down to the system noise floor without suffering from a delay mismatch difficulty.

A novel jitter reduction circuit is introduced and its jitter suppression performance is characterised in this research. This technique uses a simple time domain averaging method. The jitter reduction circuit behaves like an integrator to the sideband off set frequency. Although the suppression response depends on the number of average times *n*, a new jitter reduction circuit is cascadable. The integrator using the stop band characteristic of band pass network is presented. An integrator based on an active inductor network is investigated and used successfully in the simulated jitter reduction circuit.

1.3 Structure of this Thesis

Chapter 2 describes the review of phase noise analysis models. In this chapter, both linear time invariant and linear time variant models are considered. The design of amplifiers based on an optimum waveform of the linear time invariant model is employed in this research. The present noise reduction techniques are also reviewed. In Chapter 3, the amplifier design methodology based on the optimum oscillator waveform is presented. The conventional and the novel low pass response transposed gain amplifiers are presented in Chapter 3. Chapter 4 presents an analysis of the LO noise reduction mechanism in transposed gain oscillators. An expression for carrier to noise ratio is derived. A novel jitter reduction technique is presented in Chapter 5. The jitter reduction performance is characterised by its sideband noise suppression capability. Chapter 6 concludes the work and the contribution of this thesis. The areas of future work are also identified.

Chapter 2

Phase Noise Analysis Models and Phase Noise Reduction Techniques

The qualitative behaviour of phase noise is well known. An oscillator's output spectrum consists of a peak at the carrier angular frequency ω_0, surrounded by the symmetrical noise sideband. It does not matter how the oscillator circuits are implemented, the noise skirt shows the following characteristics. Firstly, the output noise spectral density of the oscillators is inversely proportional to the square of the frequency offset from the carrier signal, except very close to the carrier frequency. At this region, the influence of the up-converted flicker noise dominants. This same noise appears in the time domain as jitter around the oscillation's zero crossing points. This jitter can only be explained as noise in the phase of the oscillation, rather than noise that is superimposed on the signal waveform. Thus, oscillator noise is usually mentioned as phase noise. The postulation of phase noise implies that the sideband spectrum above and below the carrier are equal in amplitude and opposite in phase [2.1].

2.1 Phase Noise Characterisation

There are many phase noise analysis models that have been developed for different types of oscillator, but each of these models makes a restrictive assumption that makes it applicable only to a limited class of oscillators. A signal's short-term instabilities are usually characterised in terms of the single sideband noise spectral density. It has units of decibel below the carrier per hertz (dBc/Hz) and is defined as [2.2]:-

$$\mathcal{L}_{total}\left\{\Delta\omega\right\} = 10\log\left\{\frac{P_{sideband(\omega_o+\Delta\omega,1Hz)}}{P_{carrier}}\right\} \qquad (2.1)$$

where $P_{sideband}$ $(\omega_0 + \Delta\omega, 1\ \text{Hz})$ represents the single sideband power at a frequency offset, $\Delta\omega$, from the carrier in a measurement bandwidth of 1Hz as shown in Figure 2.1, and $P_{carrier}$ is the total power under the power spectrum curve. The definition in (2.1) includes the effect of both amplitude and phase fluctuations, $A(t)$ and $\phi(t)$.

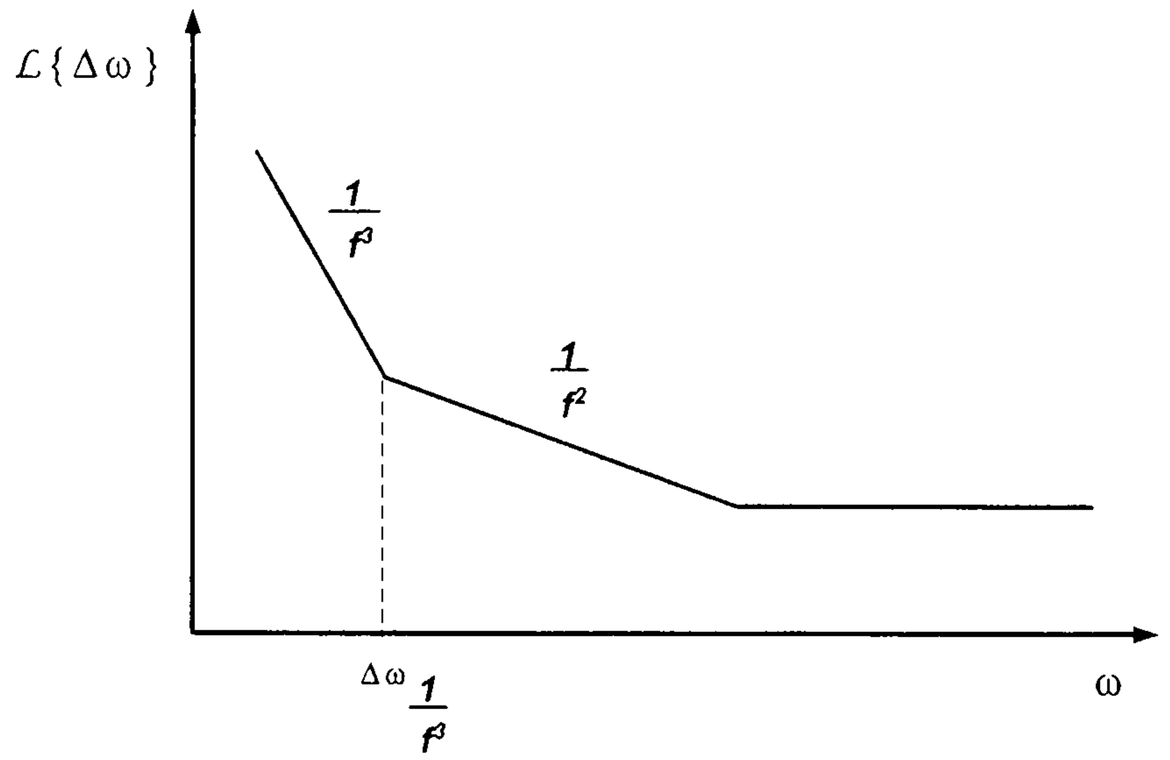


Figure 2.1 Typical plot of phase noise of an oscillator versus offset from carrier.

However, equation (2.1) shows the sum of both amplitude and phase variations. It does not show them separately. In most practical oscillators $\mathcal{L}_{total}\{\Delta\omega\}$ is dominated by its phase variation $\mathcal{L}_{phase}\{\Delta\omega\}$, which will be simply denoted as $\mathcal{L}\{\Delta\omega\}$. The effect of amplitude noise can be reduced by amplitude limiting while the phase noise cannot be reduced in the same way.

2.2 Phase Noise in the Resonator Based Oscillators

A typical resonator-based oscillator is shown in Figure 2.2 in which the oscillation frequency is determined by $1/2\pi\sqrt{LC}$. A transconductance amplifier G_m with positive feedback provides a negative resistance to cancel the loss in the LC tank circuit and R_t is a total loss resistance in the circuit including load.

The classic semi-empirical model proposed by Cutler and Leeson [2.3-2.4], which is based on the LTI (Linear Time Invariance) assumption, for tuned tank oscillators, predicts the following behaviour for $\mathcal{L}\{\Delta\omega\}$:-

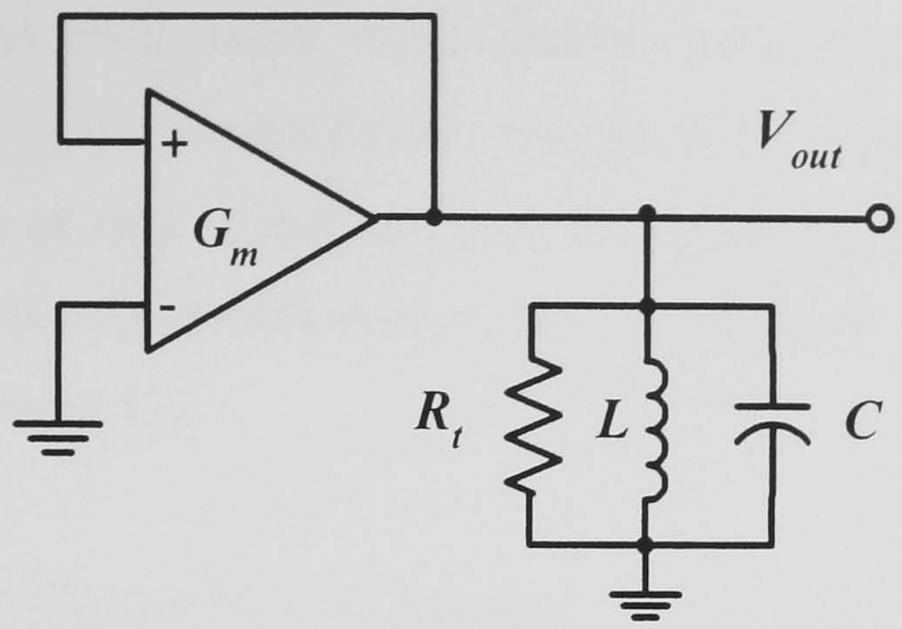


Figure 2.2 Resonator-based oscillator.

$$\mathcal{L}\{\Delta\omega\} = 10\log\left\{\frac{2\mathrm{FkT}}{\mathrm{P_s}}\left[1+\left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \qquad (2.2)$$

where F is an empirical parameter called excess noise number, k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipation in the resistive part of the tank circuit (R_t), ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all the loadings in place (also known as loaded Q), $\Delta\omega$ is the offset frequency from the carrier and ω_{1/f^3} is the frequency of corner between the $1/f^3$ and $1/f^2$ regions. In order to design low phase noise oscillators, from equation (2.2), there are two variables that have to maximised (P_s, Q_L) and two variables that have to minimised (F, T). The cross over frequency between phase and additive noise and indeed its very existence have been confirmed by experiments [2.1]. There are more phase noise analysis techniques, which are based on a linearised oscillator model [2.5 - 2.9]. All LTI approaches give a familiar form of results.

Until now, the Leeson method has continued to be the principal analysis model for oscillator designs ranging from conventional LC resonator to advanced sapphire disk dielectric resonator. There are optimised oscillator design techniques based on the linearised oscillator model [2.10-2.12]. The definition of P_s in equation (2.2) may give somewhat different results, however the generalised formula and the optimum Q_L has been introduced by Everard in [2.12].

The linearised phase noise models have some limitations. It is generally difficult to calculate F, the noise factor, *a priori*. There are some reasons behind these difficulties. Firstly, much of the noise in a practical oscillator arises from periodically

varying processes and then some noise sources in the oscillator circuit are cyclostationary instead of the assumed static sources. This is the usual case when the active device is driven at large signal and then the operating point is shifted. It has been reported that phase modulation noise is not a monotonic function of the input signal level of amplifiers [2.13].

2.3 Time-Variant Phase Noise Model

The theory that treats the generation of phase noise in oscillators as a linear, time varying process was introduced by Hajimiri and Lee in 1998. Successful design based on this technique has been reported [2.14]. A key result of the more general theory is the introduction of the impulse sensitivity function (ISF), a periodic function that describes the sensitivity of oscillator phase and amplitude perturbations (or jitter) due to fluctuations produced by noise in the oscillator circuit. The noise sources in an oscillator circuit generally affect both the amplitude and phase of the carrier signal. A pair of equivalent systems, one for the amplitude response and one for the phase response due to a perturbation noise source, can be defined [2.15]. Each system can be considered as a single-input, single-output system as shown in Figure 2.3. The input of each system is a perturbation current or voltage and the outputs are the excess amplitude, $A(t)$, and excess phase, $\phi(t)$, as defined by equation (1.1). Both systems in Figure 2.3 are time-variant.

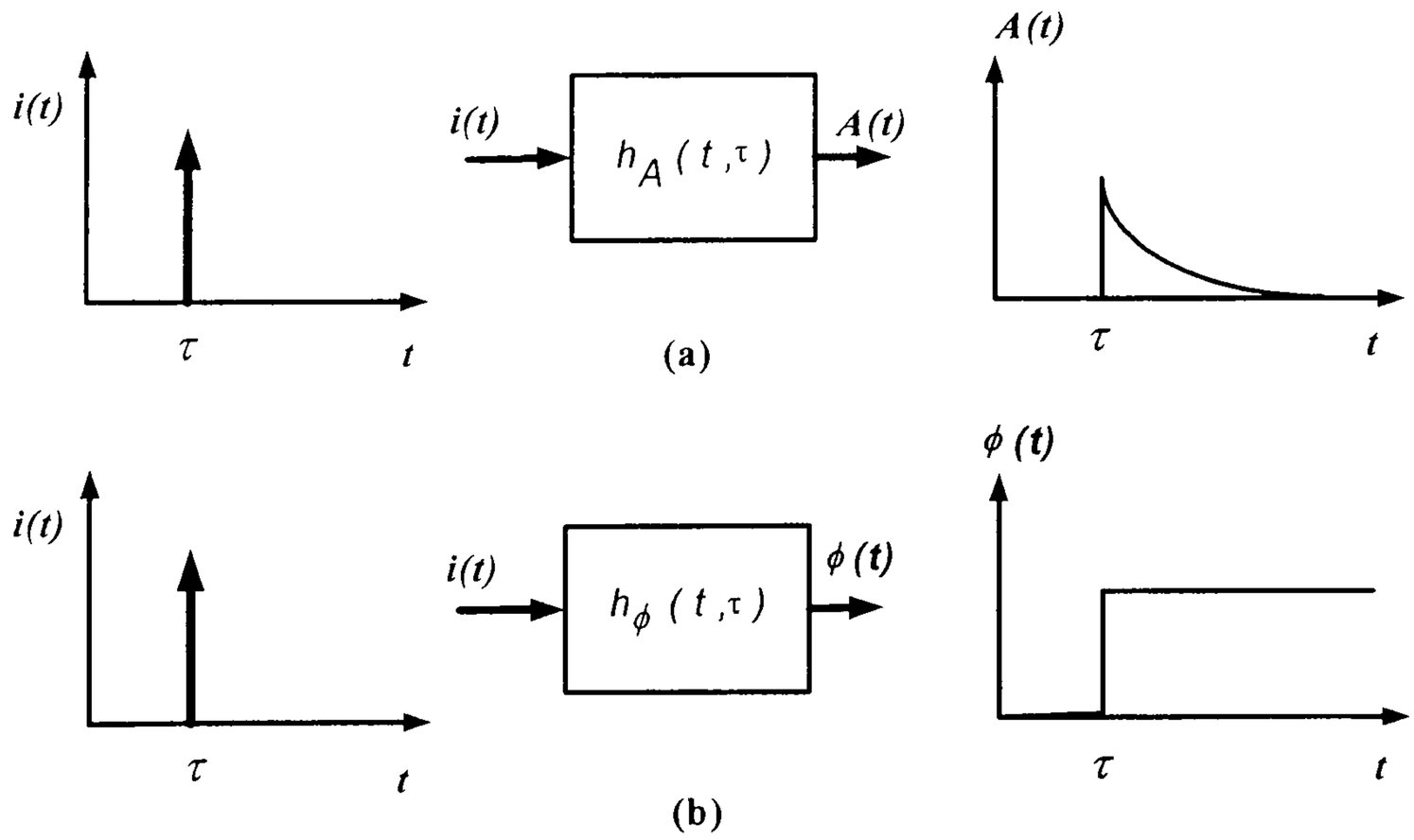


Figure 2.3 Equivalent systems for (a) amplitude and (b) phase response due to noise perturbation.

The example of time variant phase noise analysis model of an ideal *LC* parallel oscillator is shown in Figure 2.4. The oscillator has a maximum voltage of *Vmax* and the oscillation is sustained by the negative conductance –*Gm*. If an impulse (noise) is injected at the voltage maximum, the voltage across the resonator changes. There is no effect on the current through the inductor. So, the tank voltage changes instantaneously, as shown in Figure 2.5 (a). If the impulse is applied at the maximum voltage across the capacitor, there will be no phase shift and only an amplitude change will result. Conversely, if this impulse is injected at the zero crossing, it has maximum effect on the excess phase, $\phi(t)$, and minimum effect on the amplitude, as shown in Figure 2.5 (b).

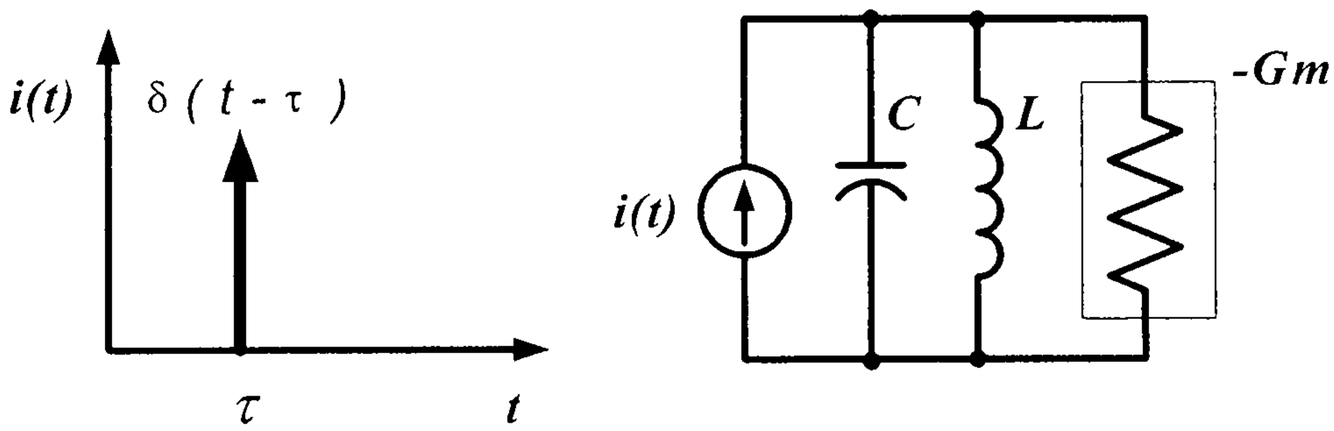


Figure 2.4 Impulse injected parallel LC oscillator.

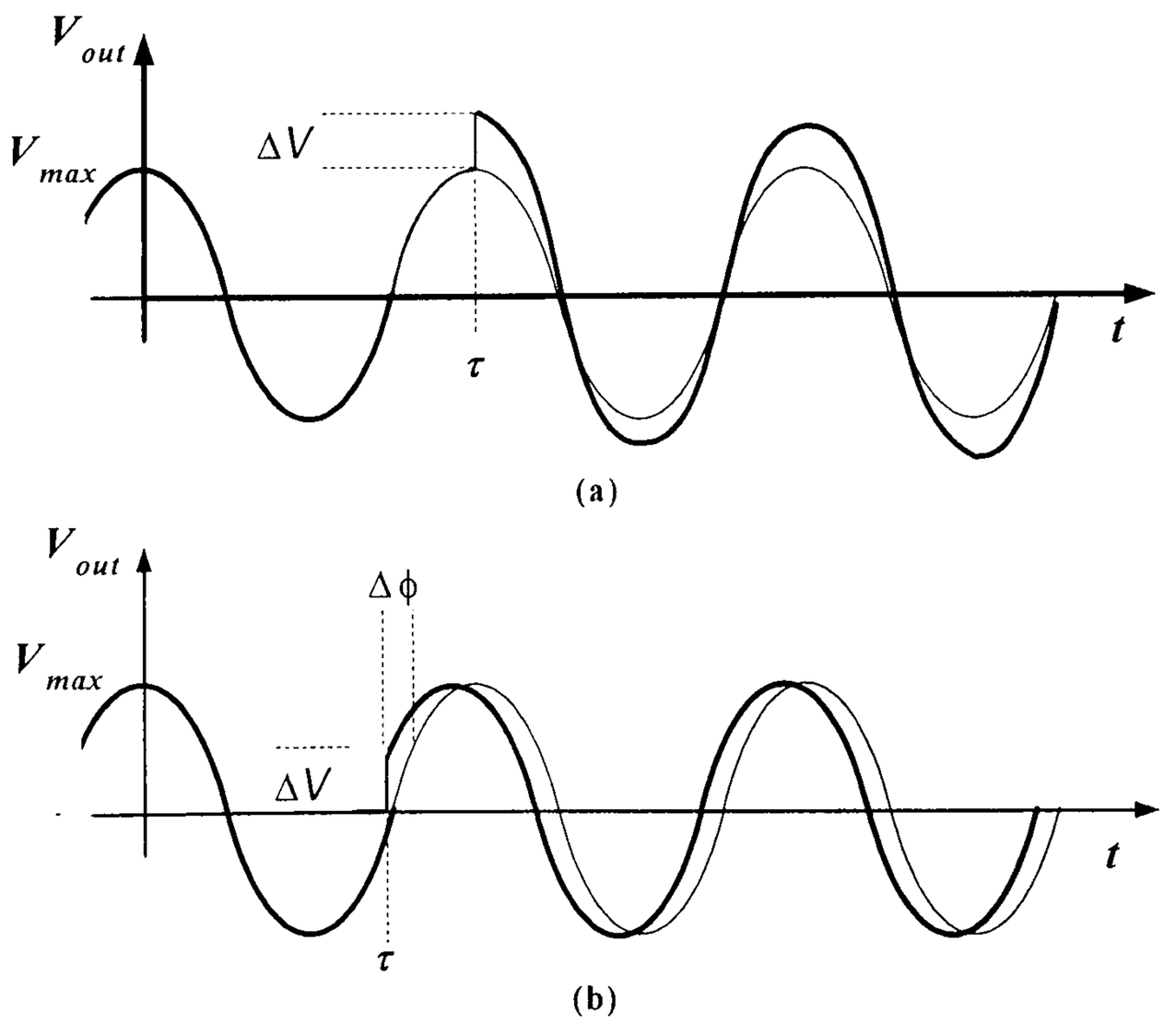


Figure 2.5 (a) Impulse response of a parallel *LC* oscillator, impulse is injected at maximum voltage and (b) at the zero crossing of oscillating voltage.

In practical oscillators, there is some form of amplitude restoring mechanism. Then, this results in an important difference between amplitude and phase responses of practical oscillators. After it passes through some transient behaviour, the excess amplitude finally converges to zero. But, fluctuations in the excess phase are not put out by any restoring or limiting mechanism and hence live on. From this concept, Hajimiri and Lee define impulse sensitivity function (ISF), the sensitivity of the oscillator to a disturbance impulsive input, as:-

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{\max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{\max}} \tag{2.3}$$

where V_{max} is the voltage swing across the capacitor and $q_{max} = C_{node}\, V_{max}$ is the maximum charge swing on the interested node.

The function $\Gamma(x)$ or ISF is a periodic, dimensionless, frequency- and amplitude-independent function. The ISF depends on particular the oscillator. Figure 2.6 shows the block diagram of time-variant phase noise generation process. The variables c_0, c_1 to c_n are real value Fourier coefficients of the oscillator's ISF.

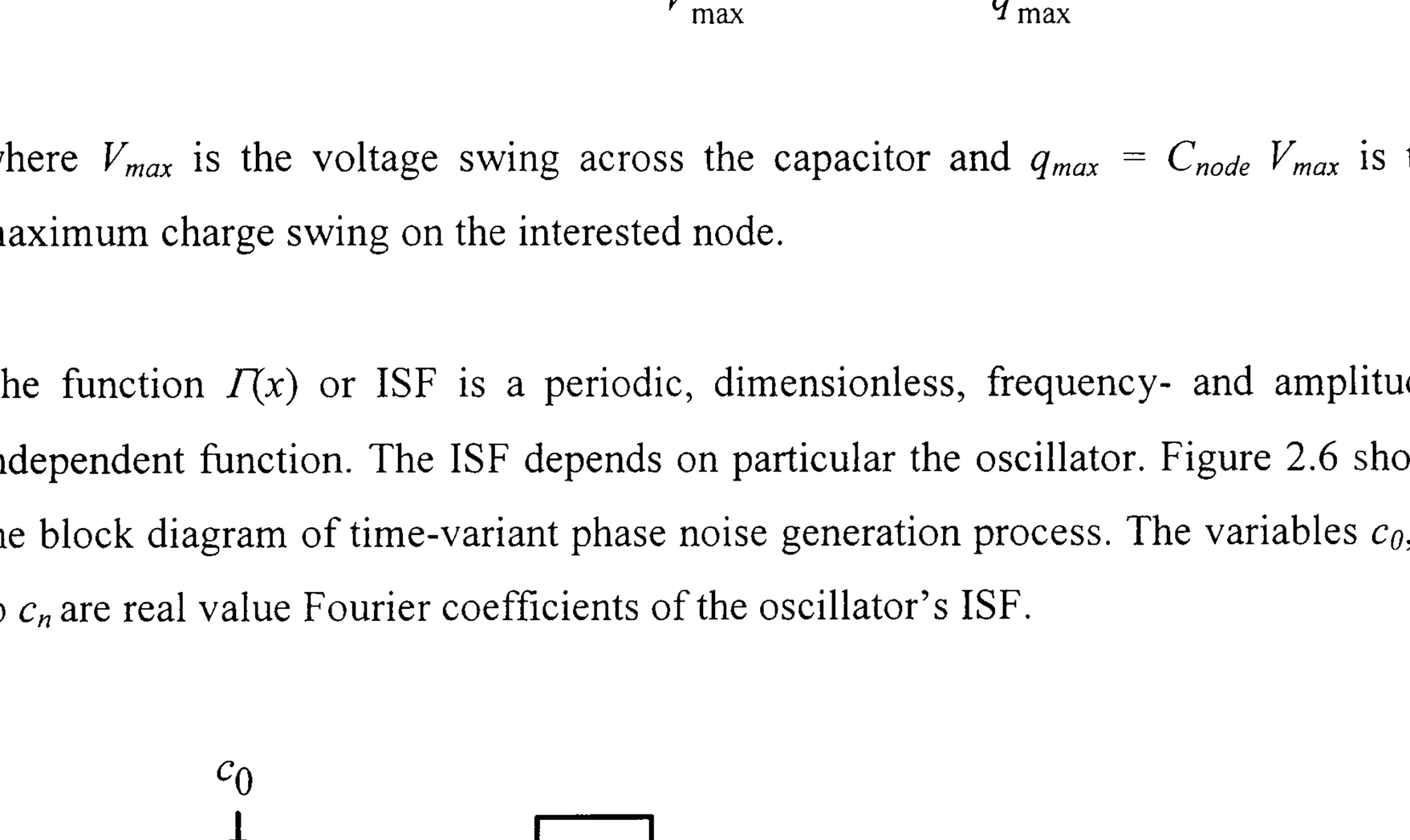


Figure 2.6 Block diagram of time-variant phase noise generation process.

In the steady state operation, the oscillators operate in the strong nonlinear mode. The small signal class A operating point of the amplifiers is changed to class C operation or higher. Nonlinearity in the steady state oscillation forces the oscillator to perform mixing and modulating functions at the same time. The mixing process downconverts the thermal noise at frequencies close to the oscillator's harmonics to a low frequency baseband signal as shown in Figure 2.7. Baseband noise spectral density $S_\phi(\omega)$ is given by the sum of phase noise contributions from device noise in the vicinity of the integer multiple of ω_0 , weighted by the coefficients c_n. Low frequency noise, such as flicker noise, is weighted by the coefficient c_0 and gives rise to the $1/f^3$ region of the phase noise spectrum. White noise components are weighted by other c_n coefficients and produce a $1/f^2$ phase noise region. The total sideband noise power is the sum of the individual terms, as depicted by the dark line in Figure 2.7. These sidebands become close-in phase noise in the oscillator output spectrum $S_v(\omega)$ through the phase modulation process.

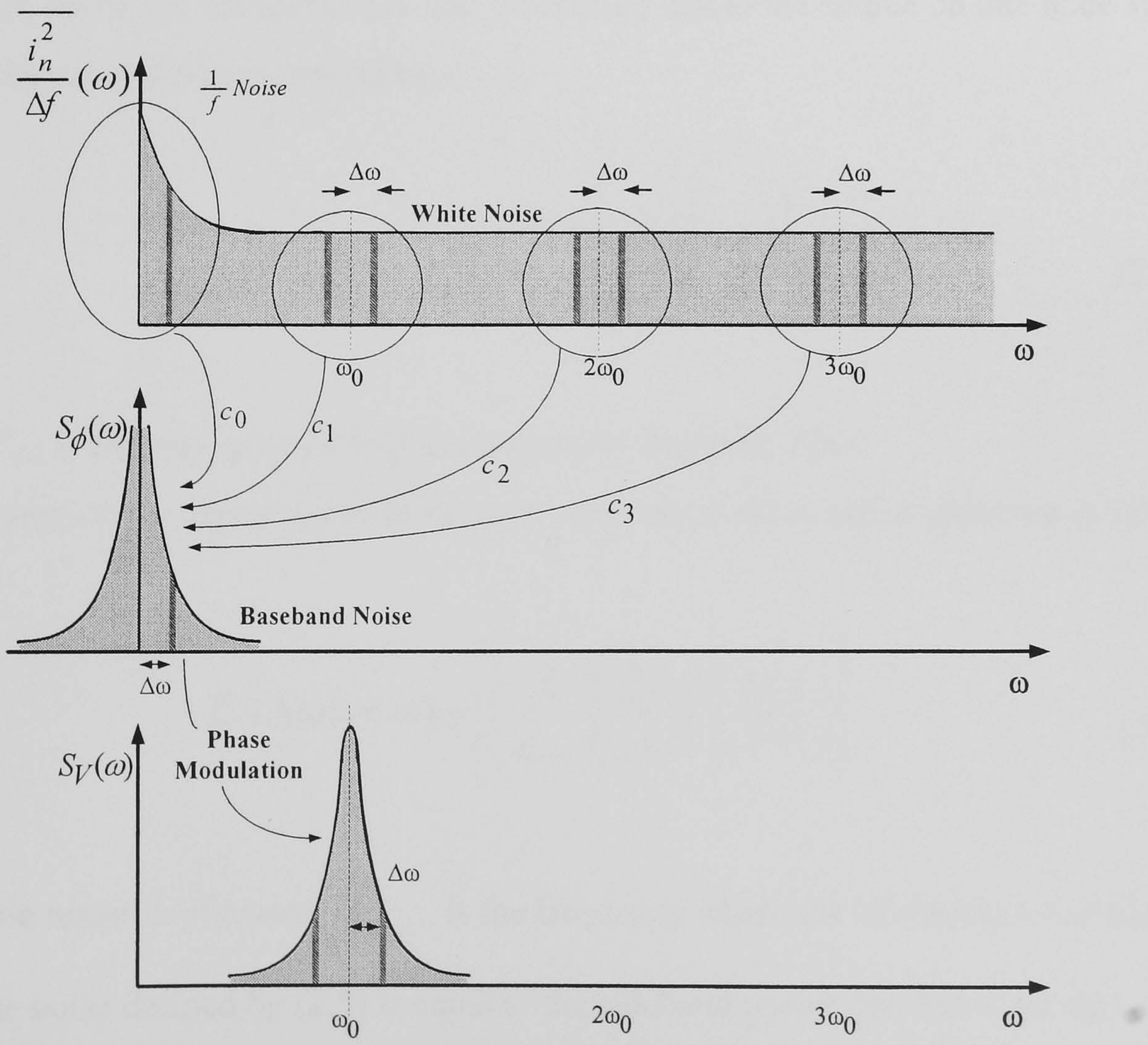


Figure 2.7 Conversion of noise to phase fluctuation and phase noise sideband.

For the Hajimiri and Lee linear time variant model, the total single-sideband phase noise spectral density due to one noise source at an offset frequency $\Delta\omega$ is given by the sum of the powers of the accentuated components in Figure 2.7. The single-sideband spectral density in the $1/f^2$ region of the phase noise spectrum, $\mathcal{L}\{\Delta\omega\}$, is defined by [2.15]:-

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{n=0}^{\infty} c_n^2}{4q_{\max}^2\Delta\omega^2}\right) \tag{2.4}$$

where $\overline{i_n^2}/\Delta f$ is an input white noise power spectral density. From equation (1.17), I_n is the peak amplitude, so that, $I_n^2/2 = \overline{i_n^2}/\Delta f$ for $\Delta f = 1$ Hz.

In terms of impulse sensitivity function, ISF, the single-side band phase noise spectral density in dB below the carrier per unit bandwidth due to the source on one node at an offset frequency $\Delta\omega$ is expressed by:-

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\right)\left(\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right)\right] \tag{2.5}$$

where Γ_{rms} is the rms value of impulse sensitivity function, $\Gamma(x)$.

The expression for phase noise in the $1/f^3$ portion of phase noise spectrum is given by:-

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\left(\frac{c_0^2}{q_{\max}^2}\right)\left(\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right)\left(\frac{\omega_{1/f}}{\Delta\omega}\right)\right] \tag{2.6}$$

The phase noise $1/f^3$ corner, ω_{1/f^3}, is the frequency where the sideband power due to the white noise defined by (2.5) is equal to the sideband power that has come up from the $1/f$ noise given by (2.6). The relation between $1/f$ noise corner frequency and $1/f^3$ corner frequency can be shown by:-

$$\omega_{1/f^3} = \omega_{1/f}\left(\frac{c_0^2}{2\Gamma_{rms}^2}\right) \approx \omega_{1/f}\left(\frac{c_0}{c_1}\right)^2 \tag{2.7}$$

From equation (2.7), we can see that the $1/f^3$ phase noise corner due to the internal noise source is not equal to the $1/f$ device noise corner, but is smaller by a factor of $\left(\frac{c_0}{\Gamma_{rms}}\right)^2$, where c_0 is the DC value of the ISF. This is the most important aspect of the time-variant phase noise analysis model.

2.4 Present Techniques for Sideband Noise Reduction

Feedback and feedforward are two general noise reduction techniques that have been used with amplifiers and oscillators. Both techniques are employed in the transistor level and the circuit level. Certain techniques have been used on the transistor level amplifier to achieve very low residual noise but have not been used in oscillators.

2.4.1 Transistor Level Active Feedback Noise Reduction

The device noise can be sensed and reduced with negative feedback [2.16-2.17] Figure 2.8 shows a bipolar junction transistor in the common emitter configuration. Current fluctuations in the transistor contribute to phase and amplitude noise. An undecoupling emitter resistor gives a local feedback noise reduction. Further noise reduction is achieved by sensing the emitter current and feeding back a signal to the base terminal.

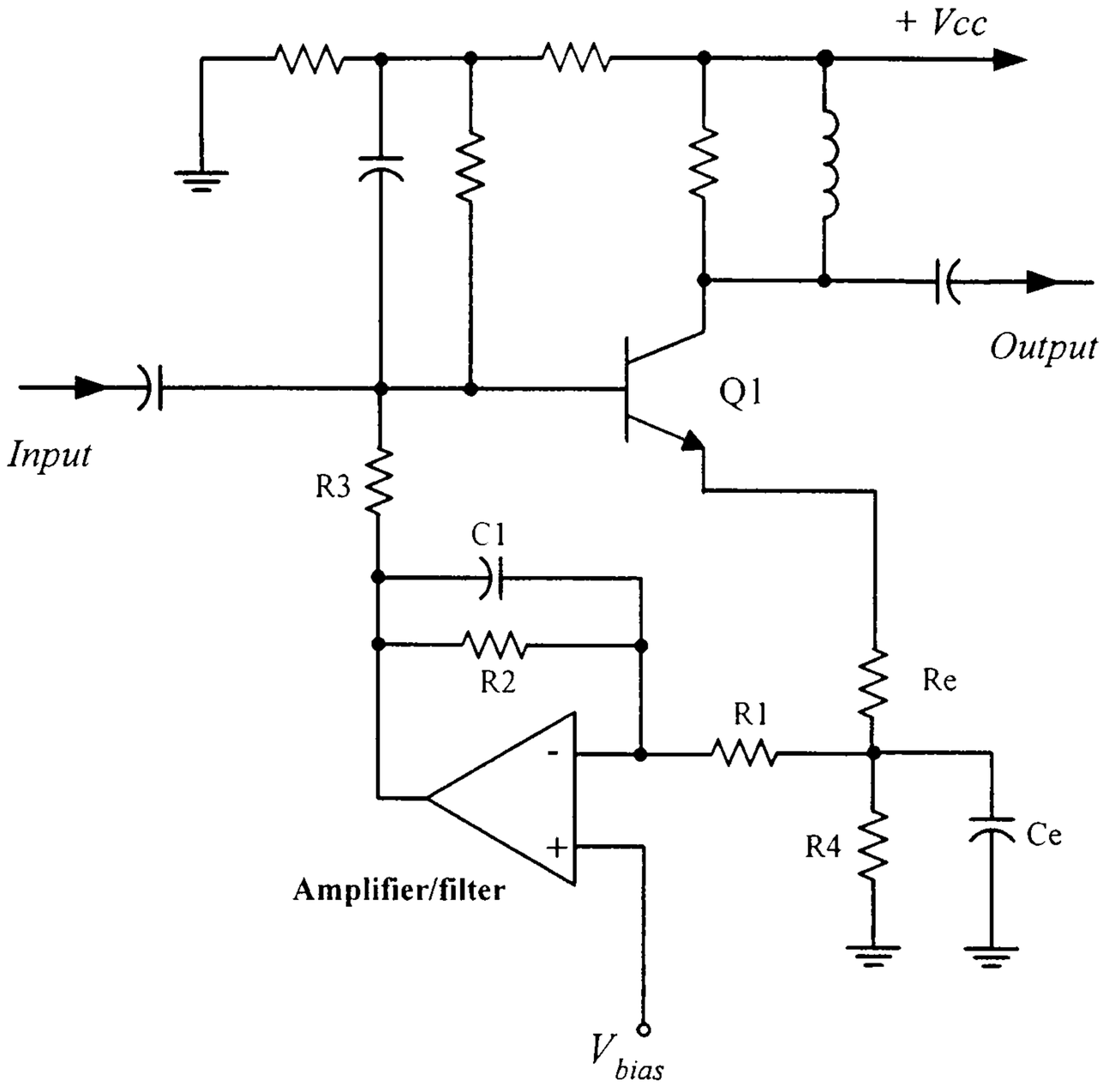


Figure 2.8 Noise reduction technique using active transistor feedback.

2.4.2 Feedforward Noise Reduction

Figure 2.9 shows a feedforward amplifier. Feedforward operation is as follows [2.17]: Noise and IMD (intermodulation distortion) generated by the main amplifier is sampled and compared to the input signal at a subtracting junction η_2. This produces a signal at the input to an auxiliary amplifier. At the η_2 junction only the carrier is removed, however the input signal of the auxiliary amplifier contains noise and IMD generated in the main amplifier. This signal is amplified by the auxiliary amplifier to a level comparable with the main amplifier's output signal. With the appropriate phase and amplitude match at the output directional coupler, the main amplifier's noise and IMD product can be removed by vector subtraction. The noise reduction bandwidth of the feedforward amplifier is inherently wide, and often set by delay matching [2.17]. The noise floor of the feedforward amplifier approaches the thermal noise limit set by the auxiliary amplifier noise figure and the input signal loss due to directional coupler η_1.

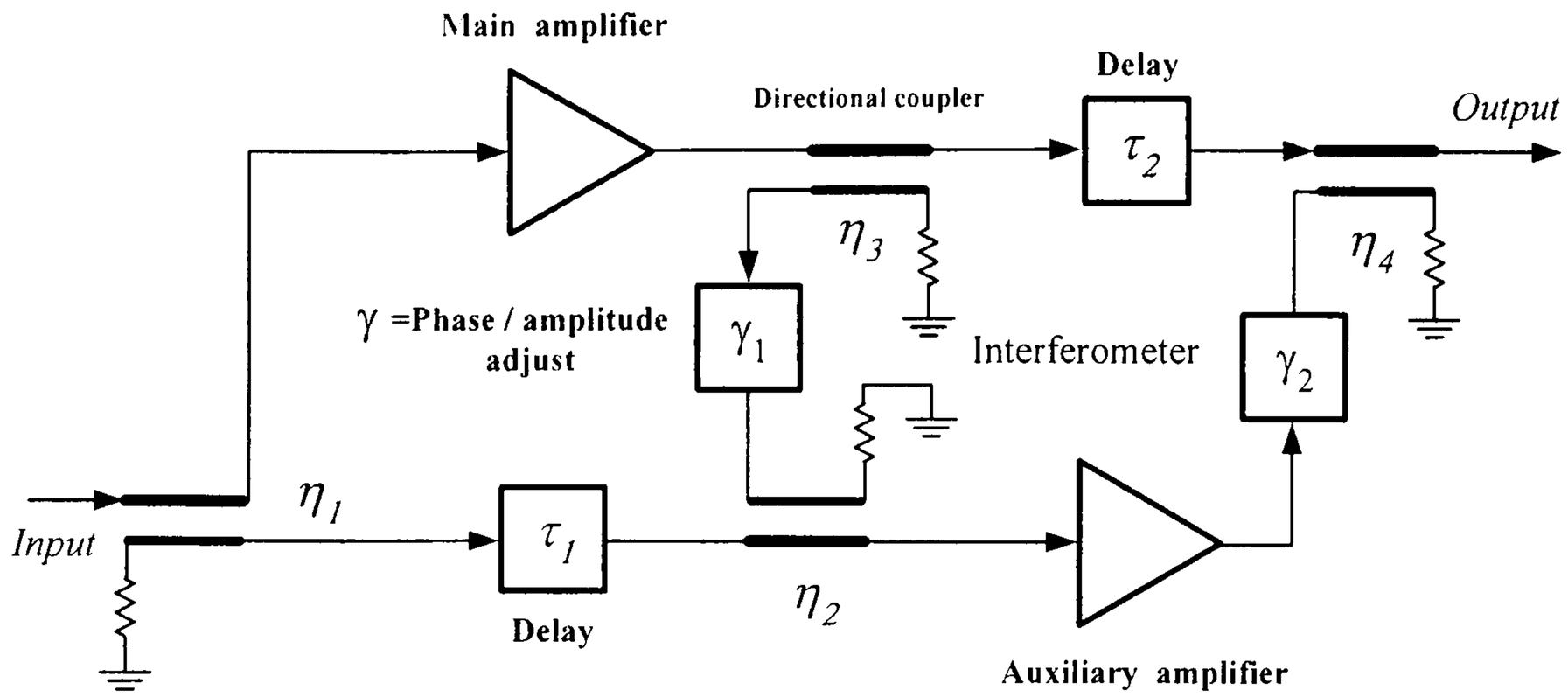


Figure 2.9 Feedforward amplifier block diagram.

2.4.3 Transposed Gain Amplifier

Figure 2.10 shows the block diagram of a transposed gain amplifier [2.17]. Using a local oscillator the input microwave signal is downconverted to the IF signal, where a low phase noise silicon BJT amplifier can be employed to perform the amplification function. The IF signal is then upconverted to the input frequency by the same local oscillator. The local oscillator phase noise can introduce phase modulation to an output signal due to IF and LO signal paths group delay mismatch. This problem is solved by introducing a delay line with the same group delay characteristic of the amplifier in between the local oscillator and the mixer 2 [3.2].

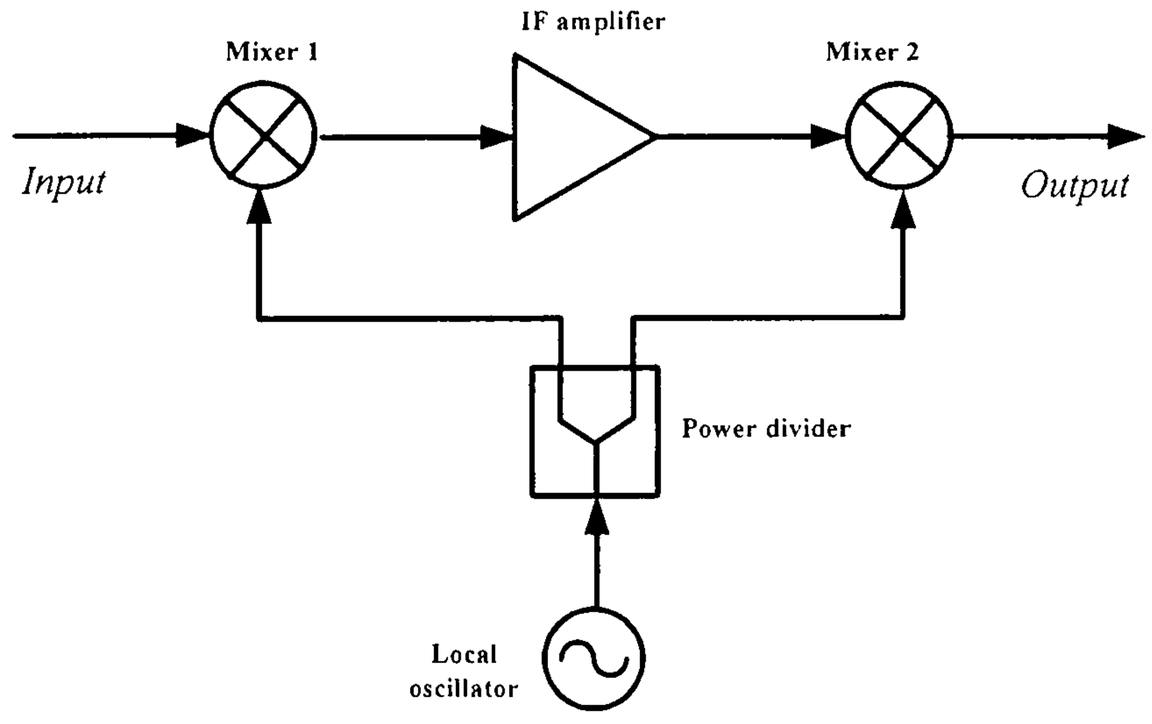


Figure 2.10 Transposed-gain amplifier.

2.4.4 RF Detection and LF Cancellation Technique

Galani [2.25], Driscoll and Weiner [2.18] developed a technique which detected the noise at the input and the output of a GaAs amplifier and applied LF (low frequency) cancellation via a voltage controlled variable phase shifter [2.12], [2.17]. This technique is depicted in Figure 2.11. The flicker noise levels exhibited in the loop phase comparator constitutes the primary limitation in noise reduction capability.

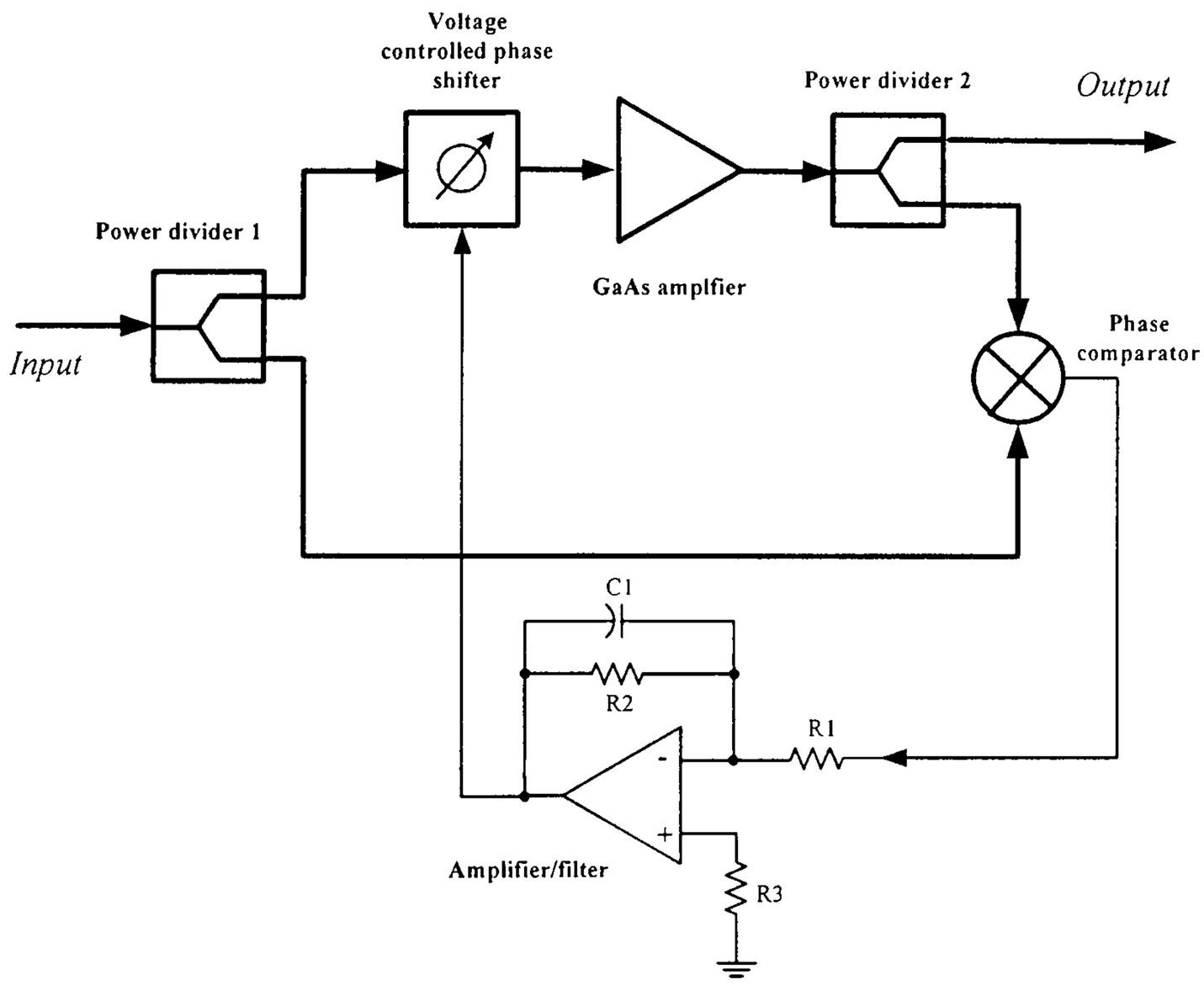


Figure 2.11 Wide bandwidth GaAs amplifier phase noise reduction feedback technique.

2.4.5 High-Q Cavity: External Discriminator

Figure 2.12 shows an oscillator noise reduction technique using the external discriminator [2.17]. The frequency discriminator is formed by comparing the signals transmitted and reflected from a resonant cavity. The phase-frequency relationship of the cavity converts frequency fluctuations from the VCO (voltage controlled oscillator) into phase fluctuations and the phase comparator converts these into voltage. This voltage is then amplified and locks the VCO frequency to the cavity resonance.

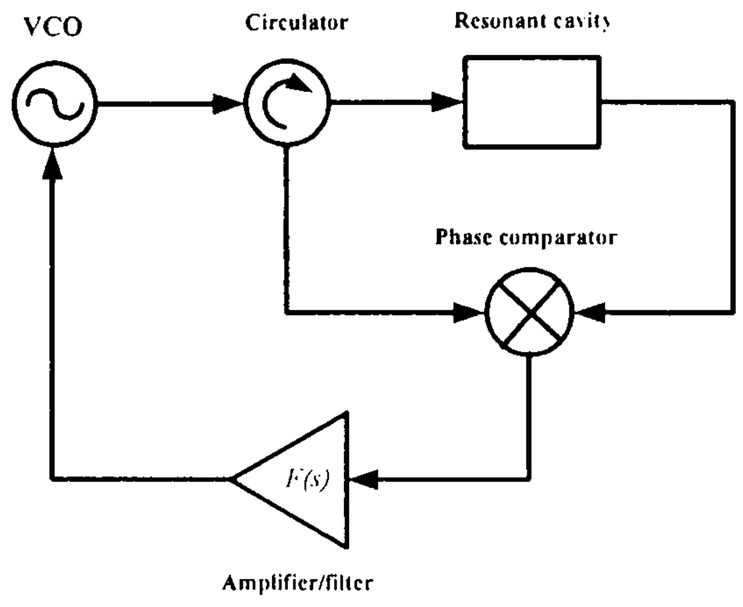


Figure 2.12 External frequency discriminator noise reduction technique.

2.4.6 High-Q Cavity: Internal Discriminator

Figure 2.13 shows one of the internal discriminator techniques [2.17], [2.25-2.26]. The frequency discriminator formed by the cavity resonator and phase bridge converts frequency fluctuations to voltage fluctuations. This noise voltage is injected into the oscillator loop via a voltage controlled phase shifter. The phase noise of the oscillator is reduced from the free running condition to the limits set by loop gain and discriminator noise floor.

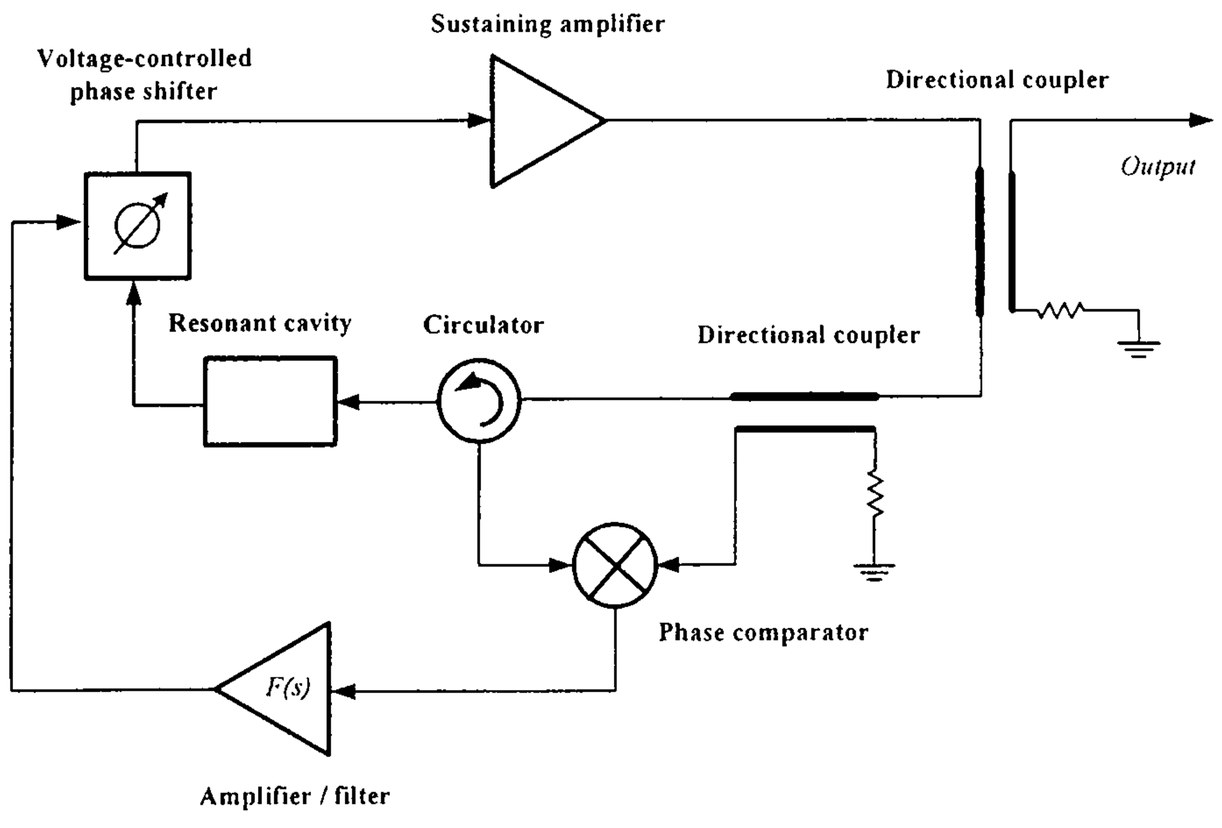


Figure 2.13 Internal frequency discriminator noise reduction technique.

2.4.7 Interferometric Carrier Suppression

The noise floor of the two previous techniques is determined by the noise of the phase comparator, which is most often a double-balanced mixer. In order to overcome the

noise floor imposed by mixer-based phase comparator, the introducing of a preceding amplifier is desirable. Figure 2.14 shows the interferometric carrier suppression [2.17], [2.19], [2.20].

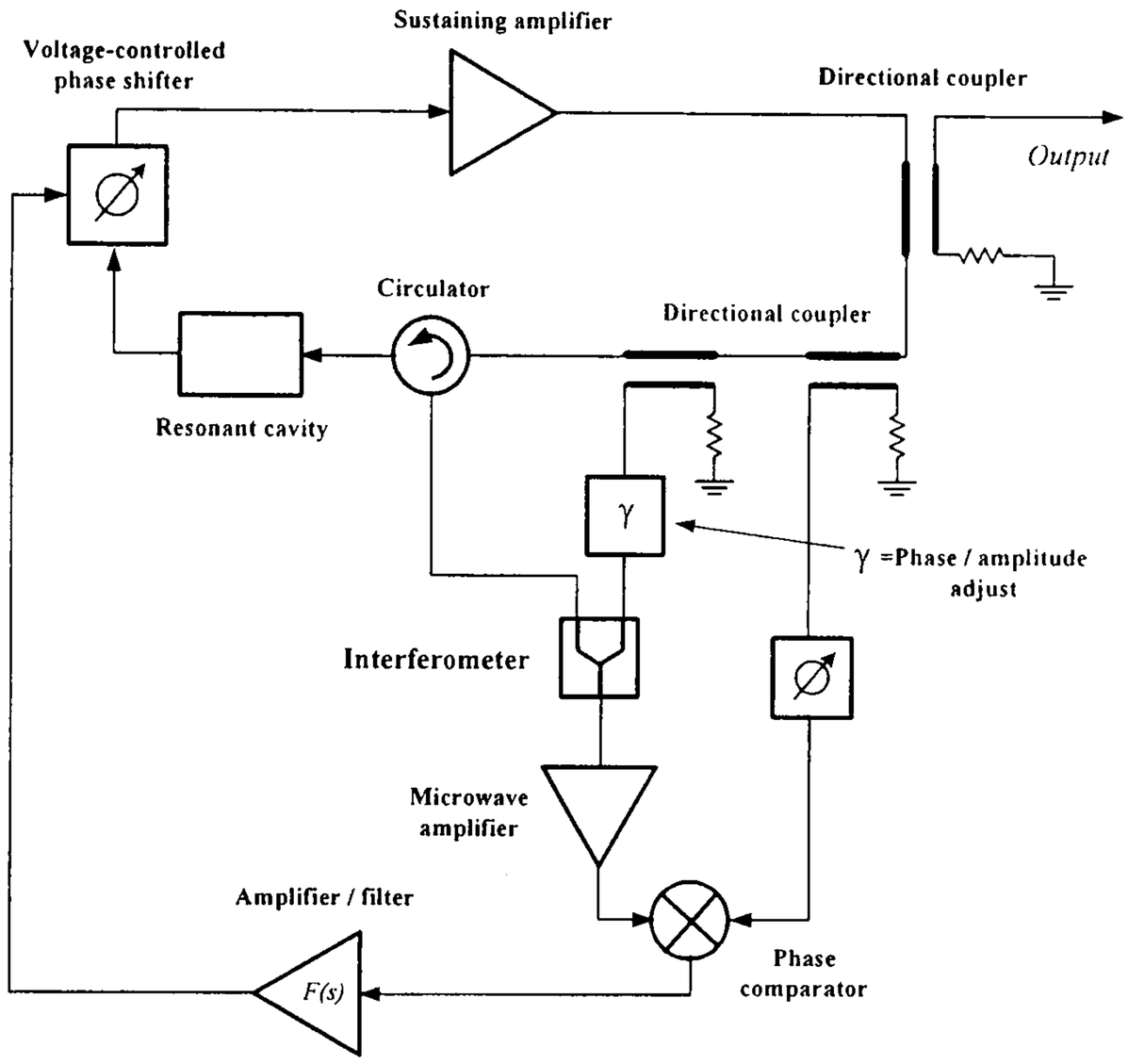


Figure 2.14 Oscillator with reduced phase noise based on a Carrier Suppression Interferometer.

2.4.8 Feedforward Amplifier as a Sustaining Amplifier

The feedforward amplifier was used as a sustaining amplifier by Broomfield and Everard [2.12], [2.21]. It was shown that the feedforward amplifier technique could be used to reduce the upconverted flicker noise in an amplifier similar to the way it reduces IMD and thermal noise. Figure 2.15 shows the low noise oscillator driven by the feedforward amplifier.

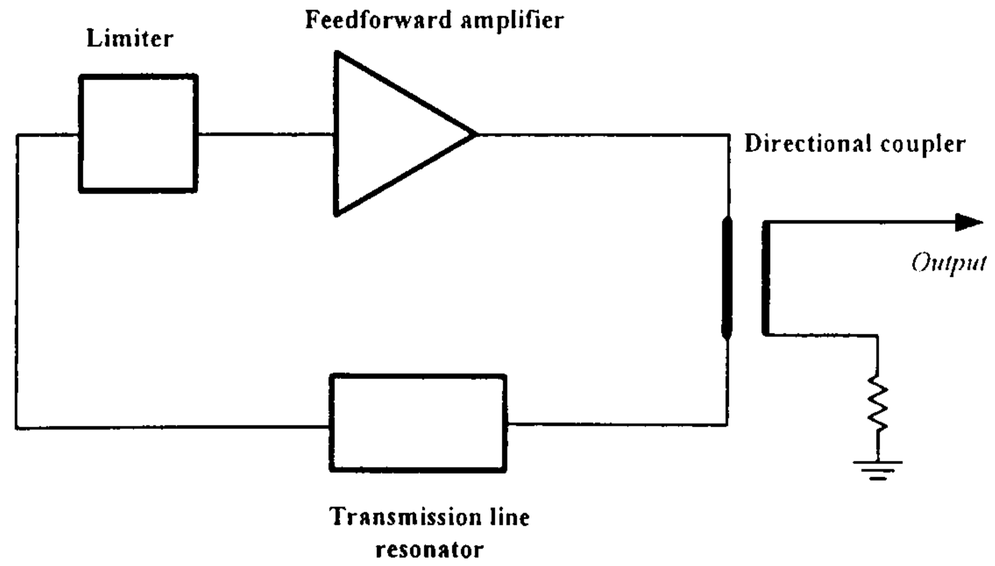


Figure 2.15 Block diagram of the feedforward oscillator.

2.4.9 Anti Jitter Circuit

The AJC or anti jitter circuit was patented by M. J. Underhill and has been described in various EFTF papers [2.22-2.24], UFFC journal papers [2.27] and recently in FCS papers [2.28]. The Anti-Jitter Circuit (AJC) is a direct carrier phase noise and jitter reduction technique. Figure 2.16 shows the block diagram and principle of operation waveform of the anti jitter circuit.

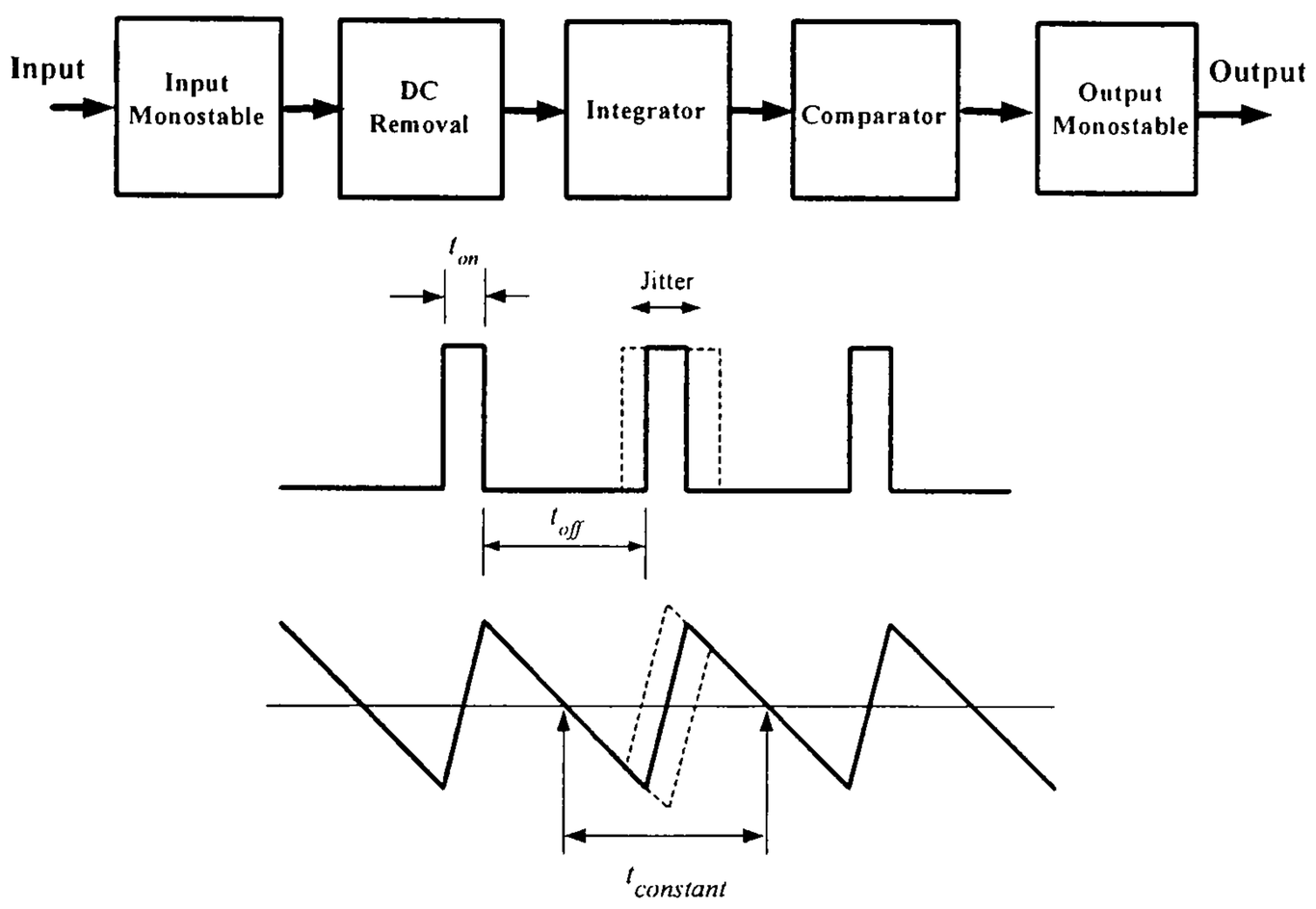


Figure 2.16 Block diagram of the anti jitter circuit and its noise reduction principle [2.23].

The AJC noise reduction technique operates in the time domain. The circuit operates as follows; the sinusoidal input signal is first converted into a square wave in order to drive the input monostable circuit. Then the integrator converts the pulse train, with its DC component removed, into a sawtooth waveform. This sawtooth waveform has a constant ramp and its amplitude is modulated by the FM (PM) noise of the input signal. The comparator reference voltage is equal to the average value of the sawtooth waveform, the output pulse train of the comparator is re-timed by the output monostable to reduce the residual leading (or trailing) edge jitter. There are five processes in an AJC :- 1) Formation of pulse train of constant area input pulses from a pulse forming network. 2) DC removal by feedback, feedforward, AC coupling, or by a combination of these. 3) Integration of the input pulse train to give a sawtooth waveform. 4) Comparator Switching at approximately the mean level of the sawtooth voltage. 5) Formation of new output pulses of chosen length triggered from a fixed level on the integrator sawtooth low jitter slope.

2.5 Conclusions

In this chapter, the phase noise characterisation and the analysis models are presented. The analysis models comprise the classical linear time invariant and the linear time variant model. From the linear time variant model, it has been shown that the oscillating waveform plays an important role in the noise modulation mechanism. In addition to optimisation of the loaded Q and minimising the amplifier noise figure, using the optimum waveform to minimise ISF is supposed to achieve the low noise operation of the oscillators.

The present noise reduction techniques are reviewed in section 2.4. The purpose of this research is to investigate and employ new methods to implement low noise RF signal generating circuits. In this research, the transposed gain and the anti jitter circuit techniques have been adopted. These techniques can be implemented using the conventional electronics circuitry without using special components and are possible to implement as an integrated circuit.

The implementation of the transposed gain oscillator building blocks is based on minimum impulse sensitivity function, which is previously mentioned. How the oscillator waveform affects the noise modulation sensitivity is investigated by time domain simulations. The LO sideband noise suppression mechanism is analysed and evaluated in Chapter 4. In Chapter 5, a novel jitter reduction circuit based on AJC operation is introduced and evaluated.

Chapter 3

The Transposed Gain Amplifier

The amplification of the input high frequency RF or microwave signals by low frequency amplifiers is made possible by the transposed gain method. This technique was used in 1971 by Seidel to produce a low noise auxiliary amplifier in a two-stage feedforward system [3.1]. Using a local oscillator the input microwave signal is down-converted to the IF signal, where a high performance low frequency amplifier can be used to perform the desire amplification. The signal is then up-converted to the input frequency by the same LO signal. Figure 3.1 shows the block diagram of the transposed gain amplification technique [3.1].

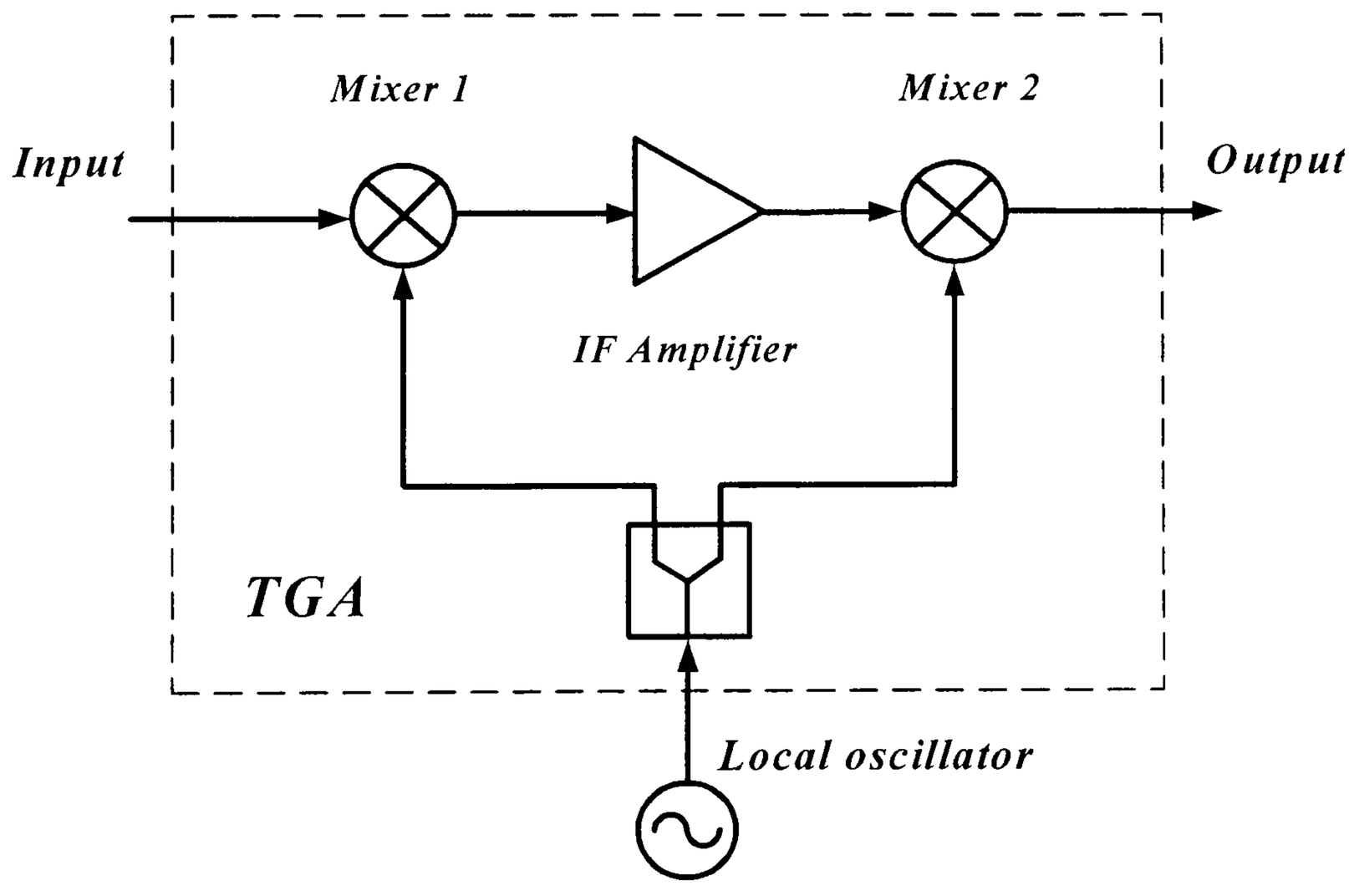


Figure 3.1 Transposed gain amplifier.

Recently, the transposed gain amplifier has been used as an oscillation sustaining amplifier in microwave oscillators [3.2-3.4]. The noise floor and flicker noise corner of the mixers sets the phase noise limit of the amplifier. These can be made low as silicon devices can be used.

3.1 Transposed Gain Amplifier Performance

The characteristics of the transposed gain amplifier or TGA are nonlinear in nature since it gives two output signals, one of these has a different frequency from the input signal. This unwanted sideband can be suppressed to a certain degree by an external band pass filter. The filter's bandwidth is determined by the IF amplifier bandwidth. The performances of the transposed gain amplifier depend on two key components, an RF amplifier and two mixers. In the following sections, the desired characteristics of these elements are described.

3.1.1 RF Amplifiers Waveform

The mixer operation and technology should be the limiting factor of the transposed gain amplifier. Thus, the RF (IF) amplifiers have to be designed for the optimum performance. Since the signal waveforms play an important role in the transformation of *1/f* and the other sources of low-frequency noise into an oscillator's phase noise spectrum [3.5-3.6], designing schemes based on minimum noise modulation sensitivity are supposed to give good performances. There are certain waveforms that have zero average value of ISF [3.7], one of the waveforms of this class is the half-wave symmetric co-sinusoids signal which contains only odd harmonics [3.8]. In this case, the slopes of the rising and falling edges are opposite and equal. This waveform can be described as:-

$$f(t) = \sum_{n=1,3,5\ldots}^{\infty} a_n \cos(n\omega t + \theta_n) \tag{3.1}$$

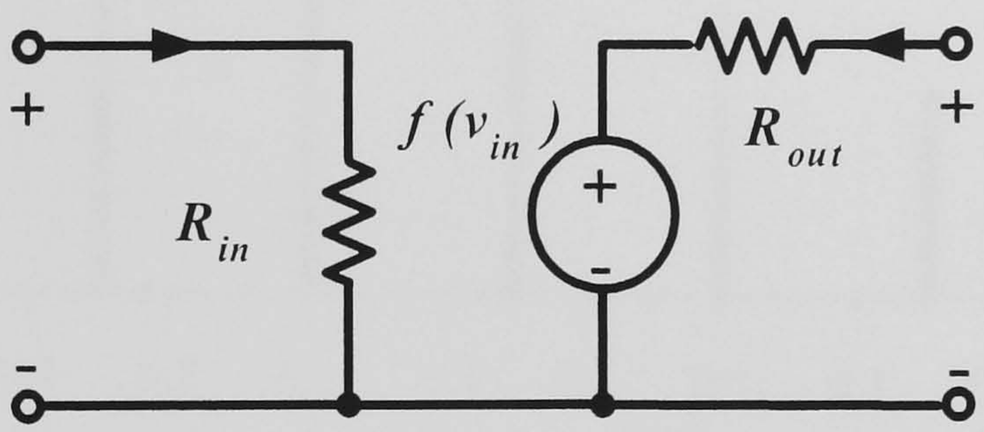
where a_n is an arbitrary amplitude and θ_n is the phase shift.

The signal waveforms that are described by equation (3.1) have an additional advantage, there is no DC term in its Fourier components. There are high performance balanced mixers using active baluns, which have frequency response down to low frequency [3.9-3.10], therefore the DC component due to amplifier's distortion seriously affects the mixer operation. The LO to RF/IF isolations are deteriorated. In case of low Q transposed gain oscillator, the output signal is impaired.

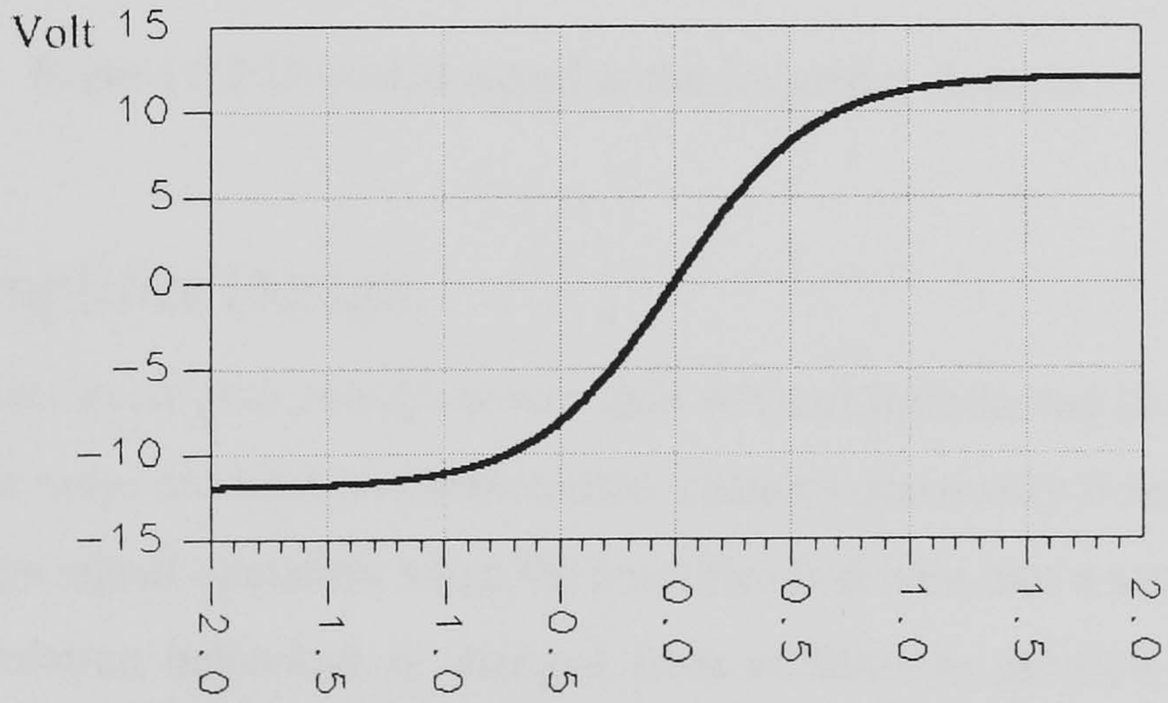
There are amplifiers, for example push-pull and differential amplifiers, which produce an output signal according to (3.1) [3.11]. A typical transfer characteristic of these amplifiers shown in Figure 3.2 and its voltage transfer characteristic can be expressed as:-

$$v_o = V_S \tanh\left[\frac{A(v_i + v_{off})}{V_S}\right] + i_o R_o \tag{3.2}$$

where A is a small signal gain, Vs is the magnitude of maximum voltage of controlled voltage source, V_{off} is the input offset voltage, i_o is the output current and R_o is the output resistance of an amplifier.



(a)



(b)

Figure 3.2 (a) Amplifier model and (b) its transfer characteristic.

Figure 3.2 (b) shows a typical plot of output open circuit voltage versus input voltage (A = 10, V_s = 12, V_{off} = 0). The over driven output voltage is limited to V_s and it

contains only odd harmonics as shown by equation (3.1). The offset or unbalance in the transfer characteristic give rise to a DC component in the frequency domain. In consequence, the DC component is multiplied with the local oscillator signal and produces more LO signal leakage. If the amplifier with a transfer characteristic shown in Figure 3.2 has a small offset of 0.1V, then the output signal in the frequency domain due to input signal of 150 MHz at 0 dBm input power is shown in Figure 3.3. As can be seen, a considerable amount of DC component is produced.

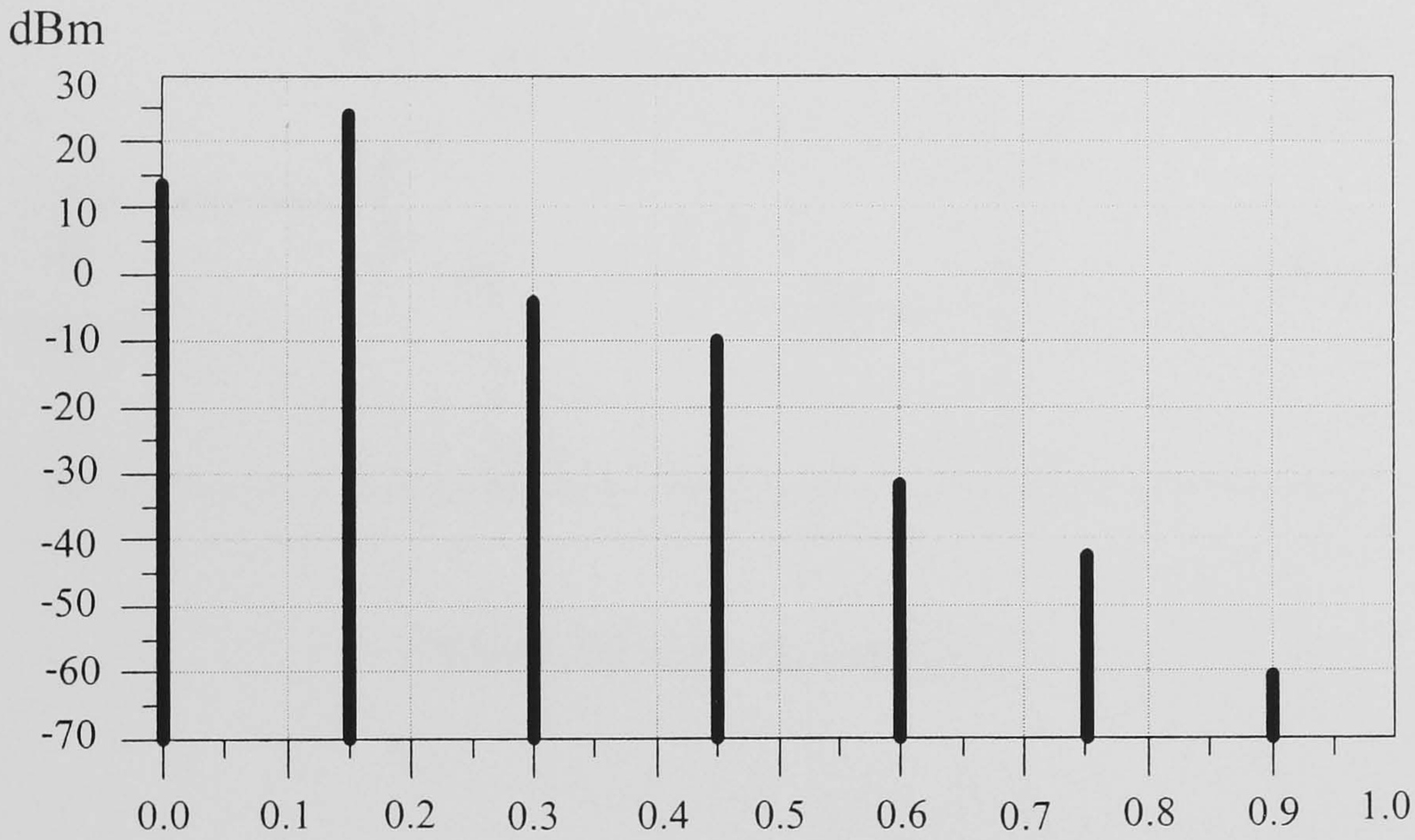


Figure 3.3 Distorted signal in the frequency domain.

3.1.2 RF Amplifier Design

The RF amplifiers must give enough power gain without introducing excessive noise modulation. The noise modulation characteristic changes drastically from small signal operation to large signal operation when the amplifier is driven into a saturation level. The noise modulation behaviour is changed from additive to multiplicative, which introduces excess phase noise in the output signal [3.5]. At saturated power level, the amplifiers behave differently from their small signal conditions. Also, the feedback parasitic capacitor, C_{cb} in case of bipolar transistors or C_{dg} for FETs, induce a strong AM to PM noise modulation at high-level signal. However, there are ways to

minimize this effect. Some previous works show that some circuit topologies have minimum noise modulation [3.6], [3.12], [3.13]. Based on these studies, common base and cascode configuration, which is shown in Figure 3.4, is the circuit of choice. According to the conditions for minimum noise modulation sensitivity [3.6-3.7] and equation (3.1), a push-pull structure is chosen. Figure 3.5 shows the block diagram of the RF amplifier used for the transposed gain amplifier's performance investigation.

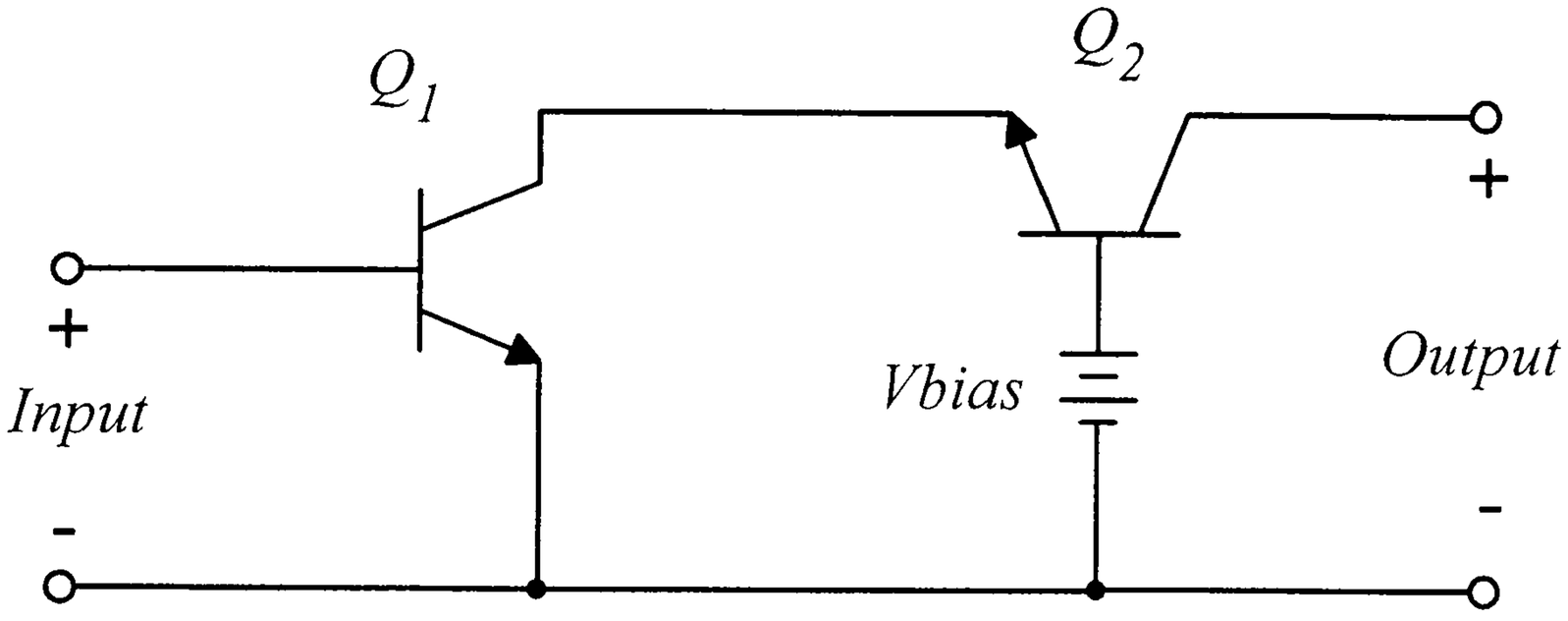
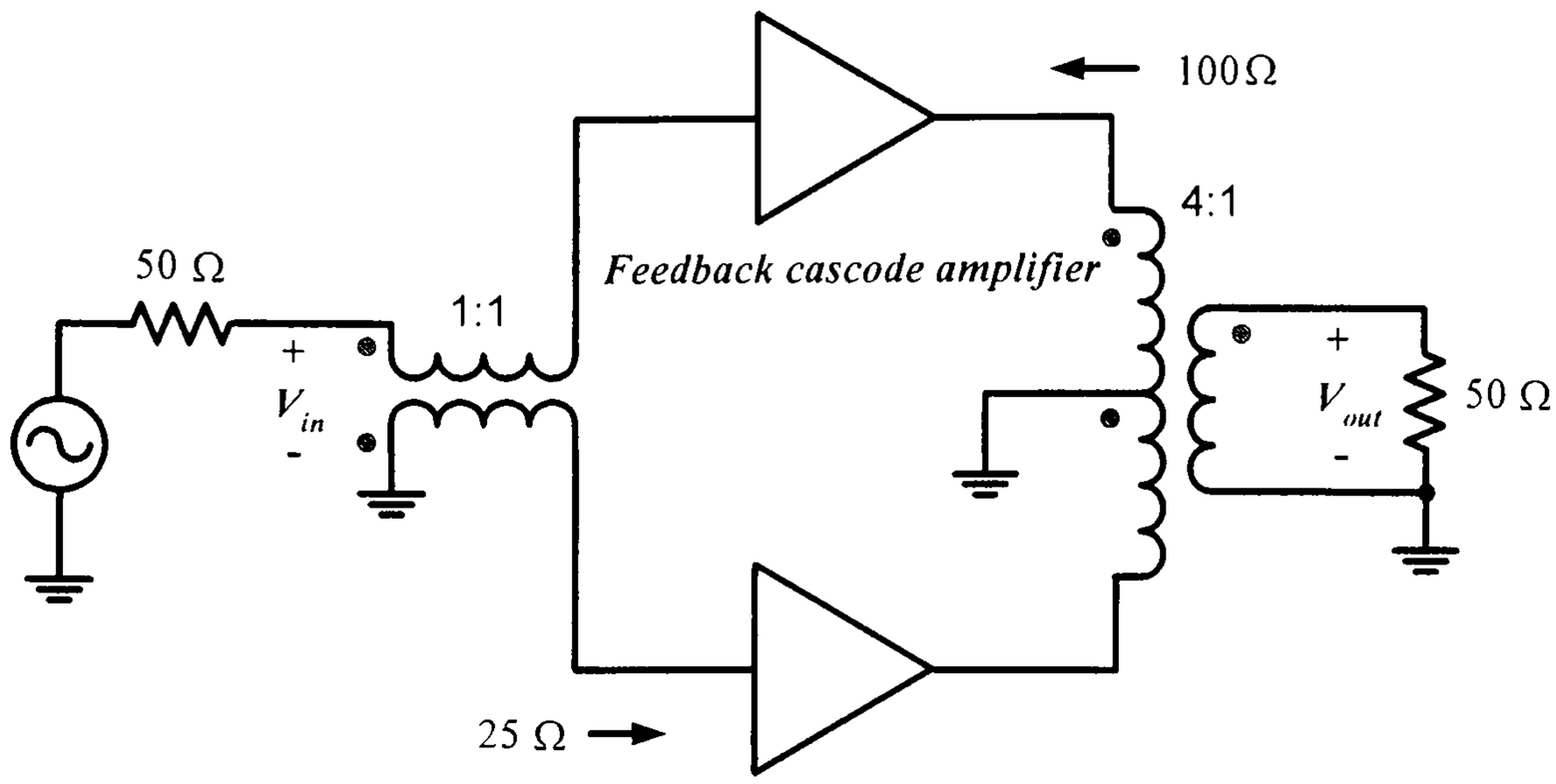


Figure 3.4 Cascode amplifier.

The push-pull amplifier in Figure 3.5 comprises two feedback cascode amplifiers and two baluns. The input balun, trifilar wound 1:1 transformer, provides the anti phase signals for push-pull operation [3.14-3.15]. The output transformer converts the two anti phase signals, which are amplified by the feedback cascode amplifiers, into a single ended output and also performs impedance matching. The combination of feedback cascode amplifier and push-pull operation gives extremely low even order distortion provided that both amplifiers have identical performance. Thus, the desired output signal according to equation (3.1) can be achieved.



Feedback cascode amplifier

Figure 3.5 Push-pull cascode amplifier.

3.1.3 Push-Pull Feedback Cascode Amplifiers

The basic cascode amplifier is shown in Figure 3.4. It has the properties of a unilateral device [3.16]. Since there is virtually no reverse transmission because the parasitic feedback element, C_{cb} (Q2), is shunted to ground, then Q1 and Q2 determine the input and output impedance of the circuit respectively. The circuit has wideband frequency response due to the common base characteristic of Q2. At low frequency, if the base resistance r_b is neglected, the input resistance is simply r_π of Q1, which is defined as [3.17]:-

$$r_\pi = \frac{\beta_0 kT}{qIc} \tag{3.3}$$

where β_0 is a DC current gain , $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, $q = 1.6 \times 10^{-19}$ C is the electronic charge and Ic is the Q1 collector current.

The output resistance of the basic cascode circuit is given by:-

$$R_o = \beta_0 r_{o2} \tag{3.4}$$

where r_{o2} is a output resistance of Q2. The cascode circuit thus displays a very high output resistance. The intrinsic voltage gain of the cascode circuit is defined by:-

$$A_v = G_m R_L \tag{3.5}$$

where $G_m = g_{m1} = qI_c / kT$ is the transconductance of Q1 and R_L is the load resistance.

The input resistance of the common base circuit, Q2, is $1/gm$, so the voltage gain of Q1 is unity. The common base circuit has current gain less than unity. Then, the current amplification of the cascode circuit comes from Q1 when Q2 provides voltage gain. The small-signal low frequency two-port equivalent circuit at low frequency without the energy storage element of the cascode circuit is shown in Figure 3.6 [3.17-3.18].

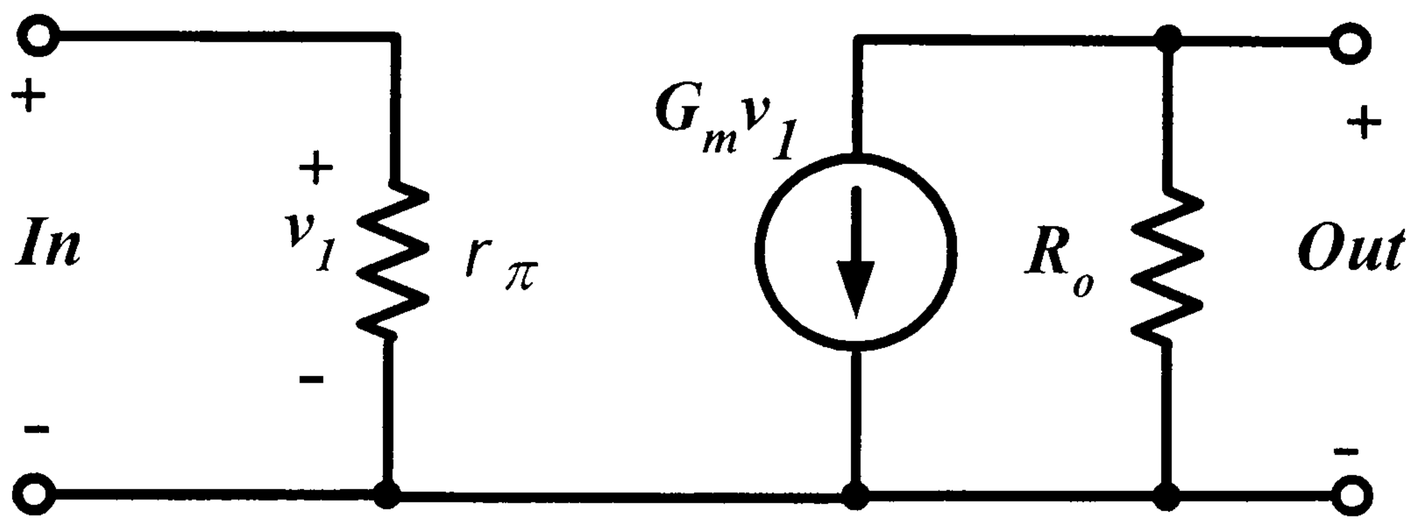


Figure 3.6 Two-port small-signal equivalent for the bipolar cascode circuit.

Equations (3.4)-(3.5) show that in order to utilize the cascode circuit as an RF amplifier in Figure 3.5, the modification of its input and output resistance is needed. Since there are three variables to modify, then at least two feedback loops are required.

Figure 3.7 shows the simultaneous use of shunt and series feedback, compound feedback, which gives rise to wideband resistive input-output impedances.

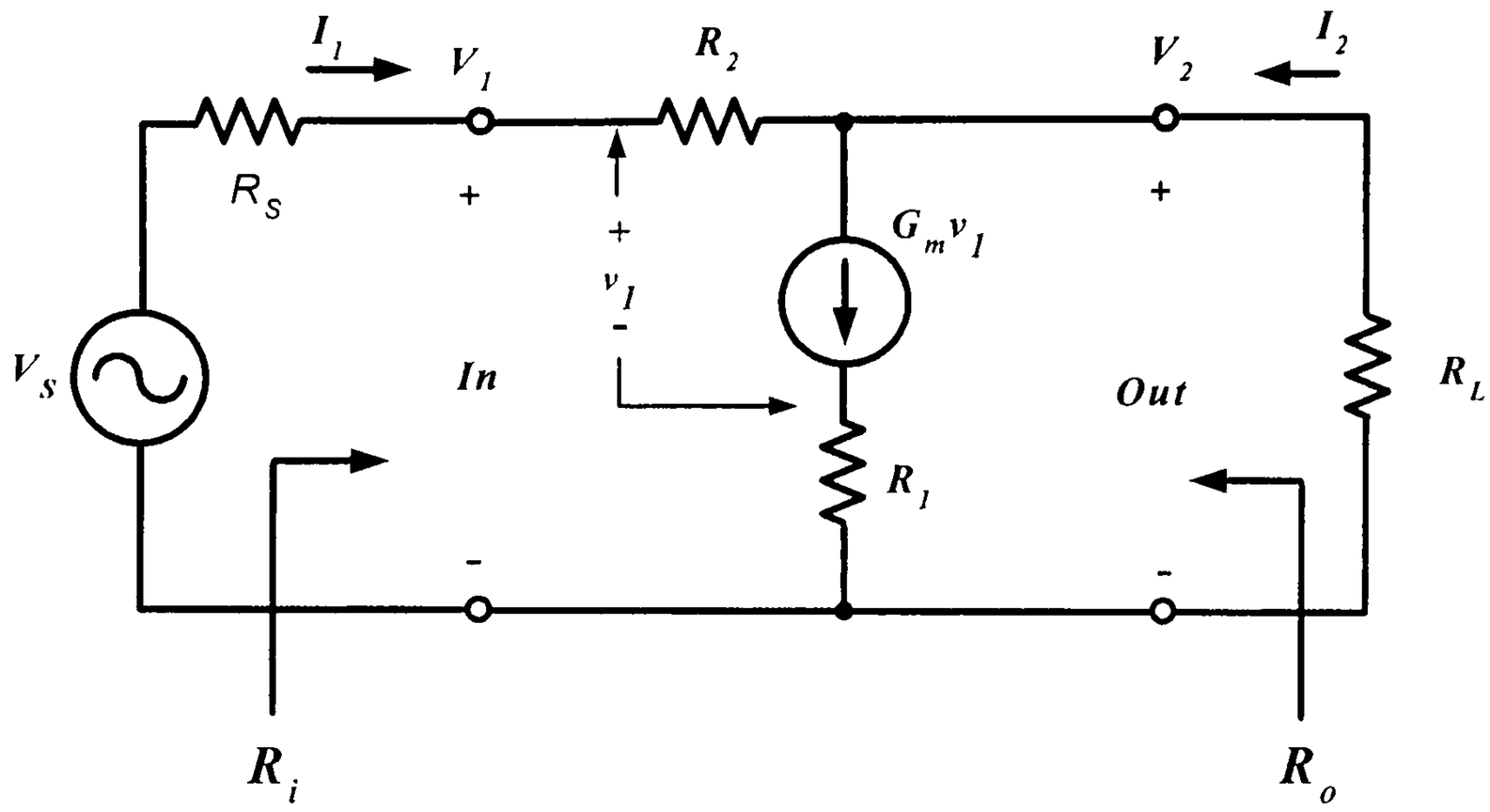


Figure 3.7 The small-signal equivalent circuit for the compound feedback amplifier.

The series feedback effects make the effective common emitter input impedance higher than R_S. Also, R_O in equation (3.4) is very large compared to R_L. If r_π is neglected the output resistance of common base circuit, the input resistance, output resistance and the voltage gain of the feedback cascode amplifier can be approximated as follows:-

$$R_i = \frac{V_1}{I_1} = \frac{GmR_1(R_L + R_2) + R_L + R_2}{Gm(R_L + R_1) + 1} \tag{3.6}$$

$$R_o = \frac{V_2}{I_2} = \frac{GmR_1(R_2 + R_S) + R_2 + R_S}{Gm(R_S + R_1) + 1} \tag{3.7}$$

$$A_v = \frac{V_2}{V_1} = \frac{-(R_2 - R_1)GmR_L + R_L}{GmR_1(R_L + R_2) + R_L + R_2}. \tag{3.8}$$

The amplifier is implemented by discrete components and the feedback resisters are chosen after the *Gm* is defined. The Philips wideband transistors BFG541A and F14 dual aperture MMG Neosid [3.19] ferrite core wideband transformers are used in the amplifier implementation. The transistors are biased with 60 mA collector current, which provides optimum f_T under the safe operating area. This bias current gives the

Gm of 2.32 siemens. The design objective is maximum gain at the input and output resistance of 25 and 100 ohm respectively. Equations (3.6)-(3.8) are plotted as a function of the feedback resistors, thus the initial value of R_1 and R_2 can be selected. If the 3.3 and 680 ohm resistors are chosen for R_1 and R_2, the feedback cascode amplifier gives a voltage gain of 23.24, and input and output resistance of 28.06 and 91.56 ohm respectively.

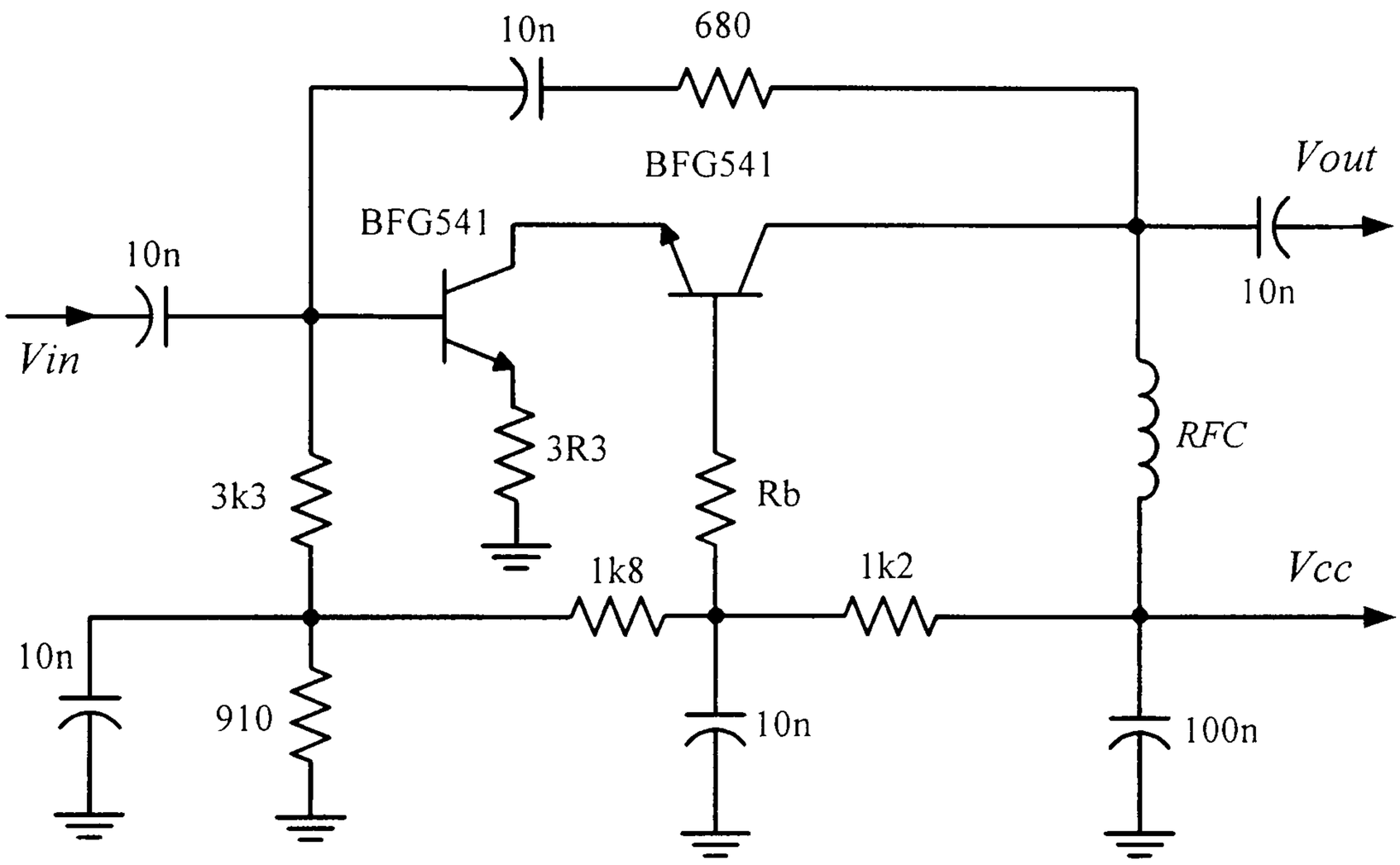


Figure 3.8 Feedback cascode amplifier.

The practical feedback cascode amplifier circuit is shown in Figure 3.8. Using discrete and high f_T transistors, the stability problem is a common situation. The amplifier stability factor, K, is less than unity at high frequency due to the internal parasitic feedback of SOT223 package of Q2 [3.20].

The input impedance of the common base circuit has a negative real part at certain frequencies due to the inductive feedback from base bonding wires. The stability problem can be solved by the series resistive loading technique at base terminal [3.21-3.22]. This resistor has no effect on the amplifier pass-band response [3.23].

The push-pull cascode amplifier comprising two identical feedback cascode amplifiers and two baluns according to the block diagram in Figure 3.5 and Figure 3.8 with the optimised feedback resistors is shown in Fig 3.9. The s-parameters of the input and output baluns are measured by a vector network analyser. The measured 2-port and 3-port s-parameters files are used for the circuit optimisation. The Harmonic balance simulation shows that the cascode push-pull amplifier has 39.8 dBm third order intercept point and a 1 dB gain compression of 23.7 dBm. The amplifier drains 130 mA bias current from a 12 volt power supply. The measured transducer gain, input and output return loss is shown in Figure 3.10. Using a HP noise figure measurement system, push-pull cascode amplifier has a noise figure of 4 dB at 180 MHz. Figure 3.11 shows a fabricated amplifier.

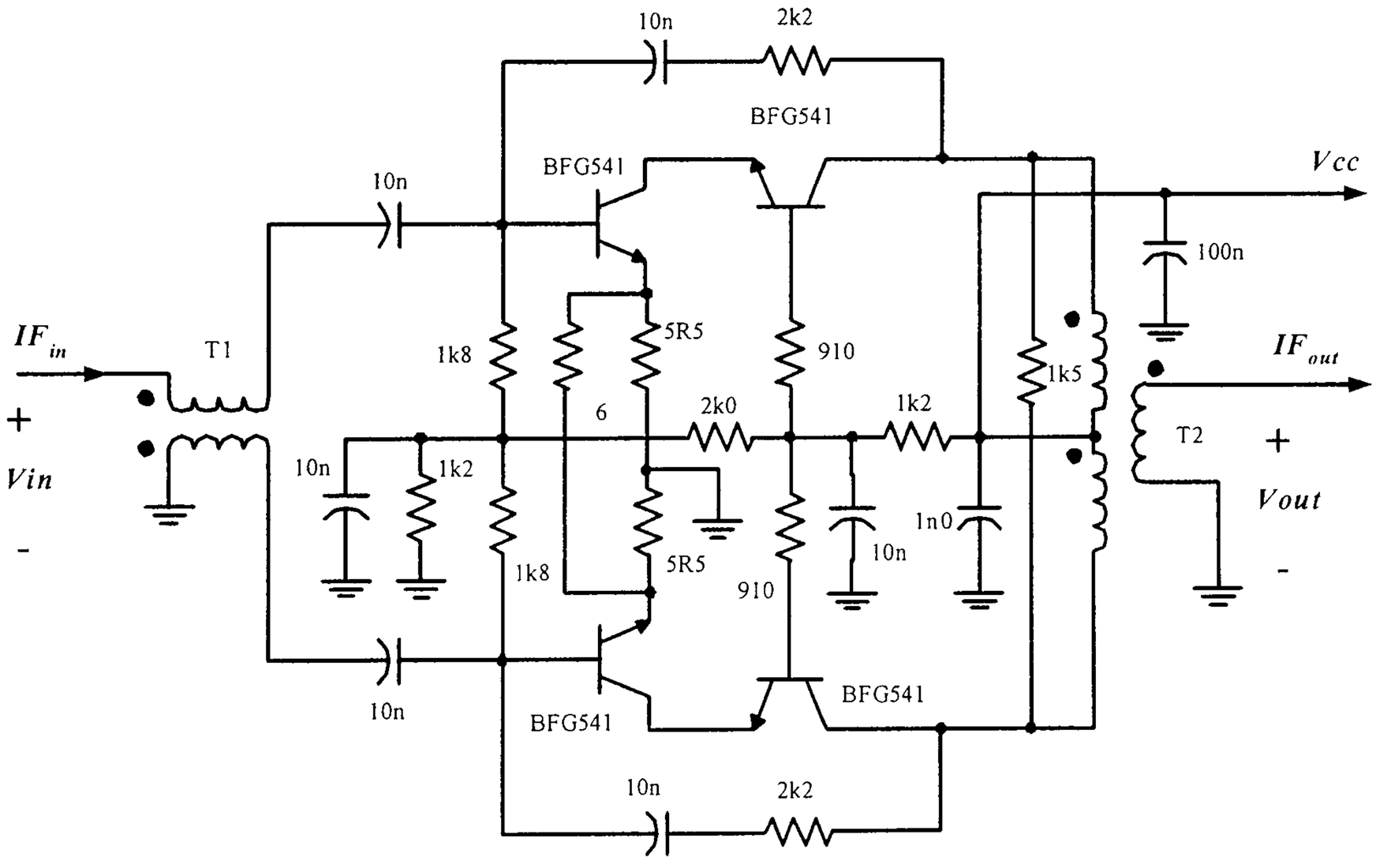
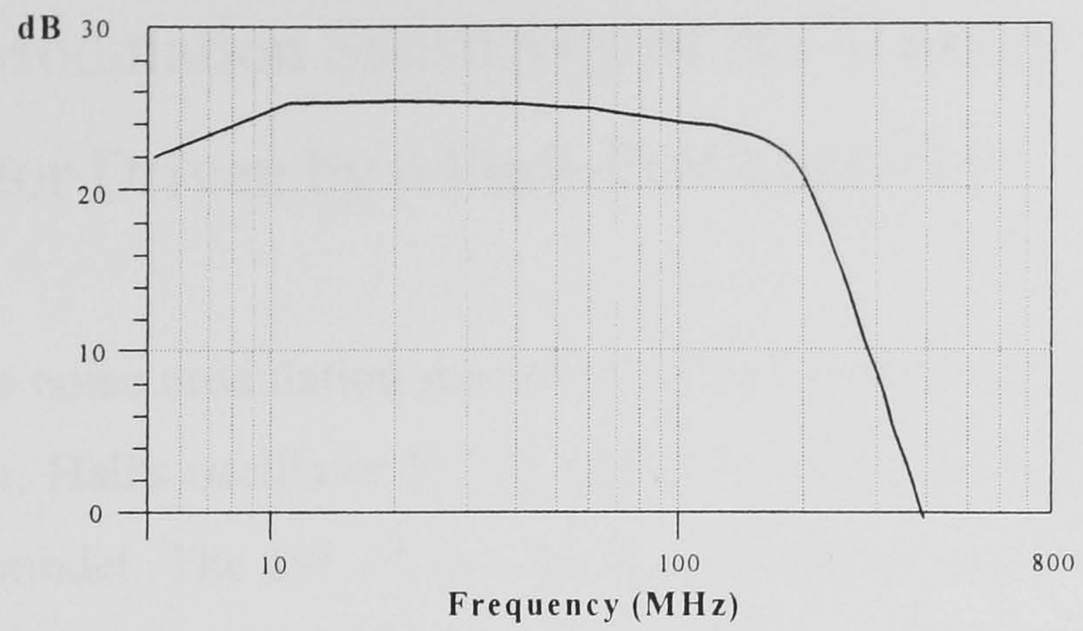
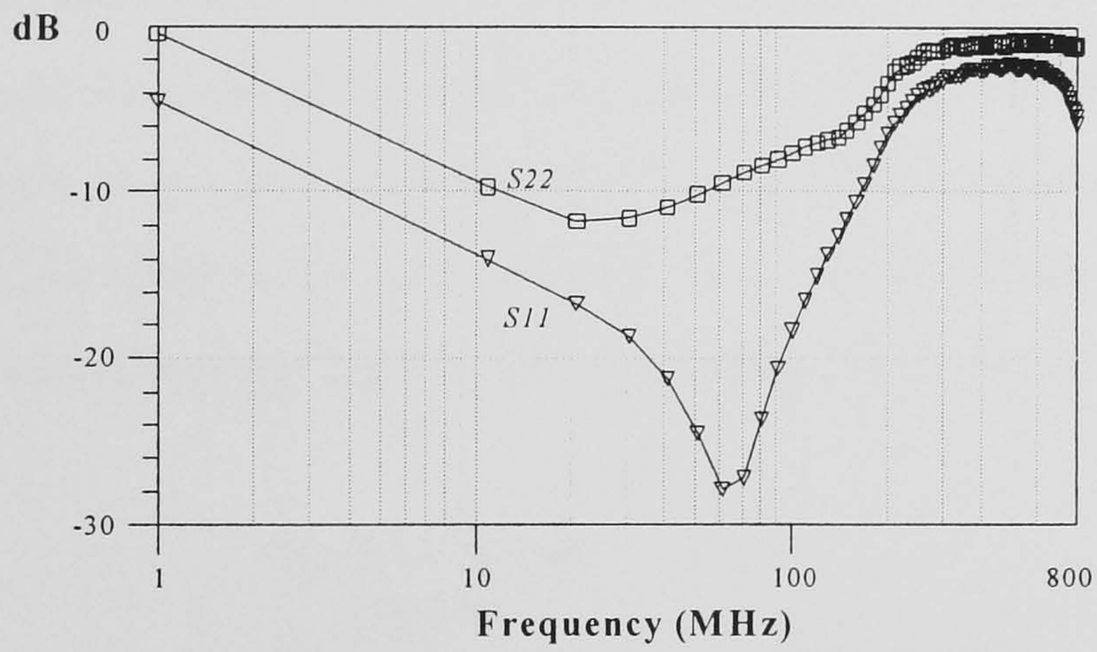


Figure 3.9 Push-pull cascode amplifier.



(a)



(b)

Figure 3.10 Transducer gain and input-output return loss of the push-pull cascode amplifier.

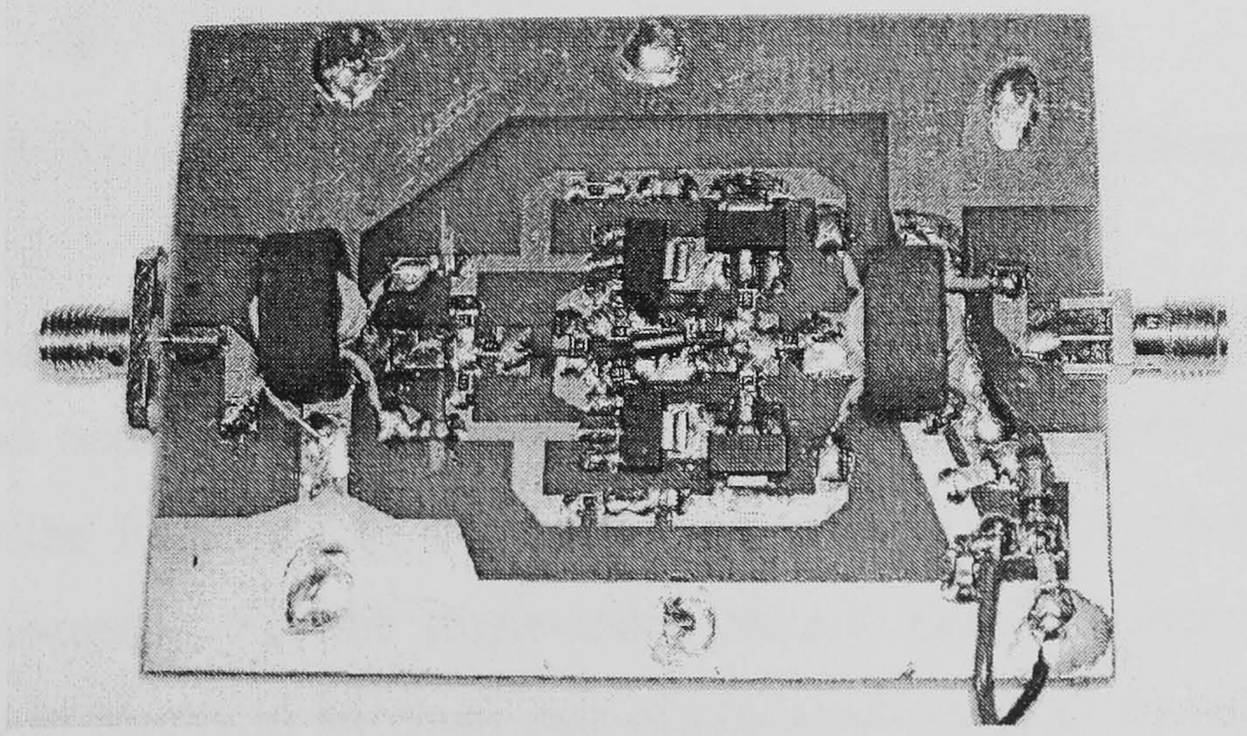


Figure 3.11 Push-pull cascode amplifier fabrication using the discrete components.

3.1.4 Noise Modulation Sensitivity of the Transmission Type Oscillator Driven by a Push-Pull amplifier

To investigate the noise modulation sensitivity of an oscillator driven by the feedback cascode amplifier, Hall's oscillator [3.24], which is shown in Figure 3.12, is used as an investigation model. The ISF of two oscillators, one is sustained by a single-end cascode and the other by a push-pull cascode amplifier, are compared. Both oscillators consist of an amplifier, a directional coupler, a resonator and a phase shift network. The resonator has a loaded Q of 20 and the directional coupler's coupling coefficient is chosen to make both amplifiers operate at the same output power level. The loaded Q, close loop phase shift and feedback power are optimised according to Everard [3.25-3.26]. The directional coupler is a cross-coupled transformer type [3.27] and the transformers are modelled by two controlled sources technique [3.28].

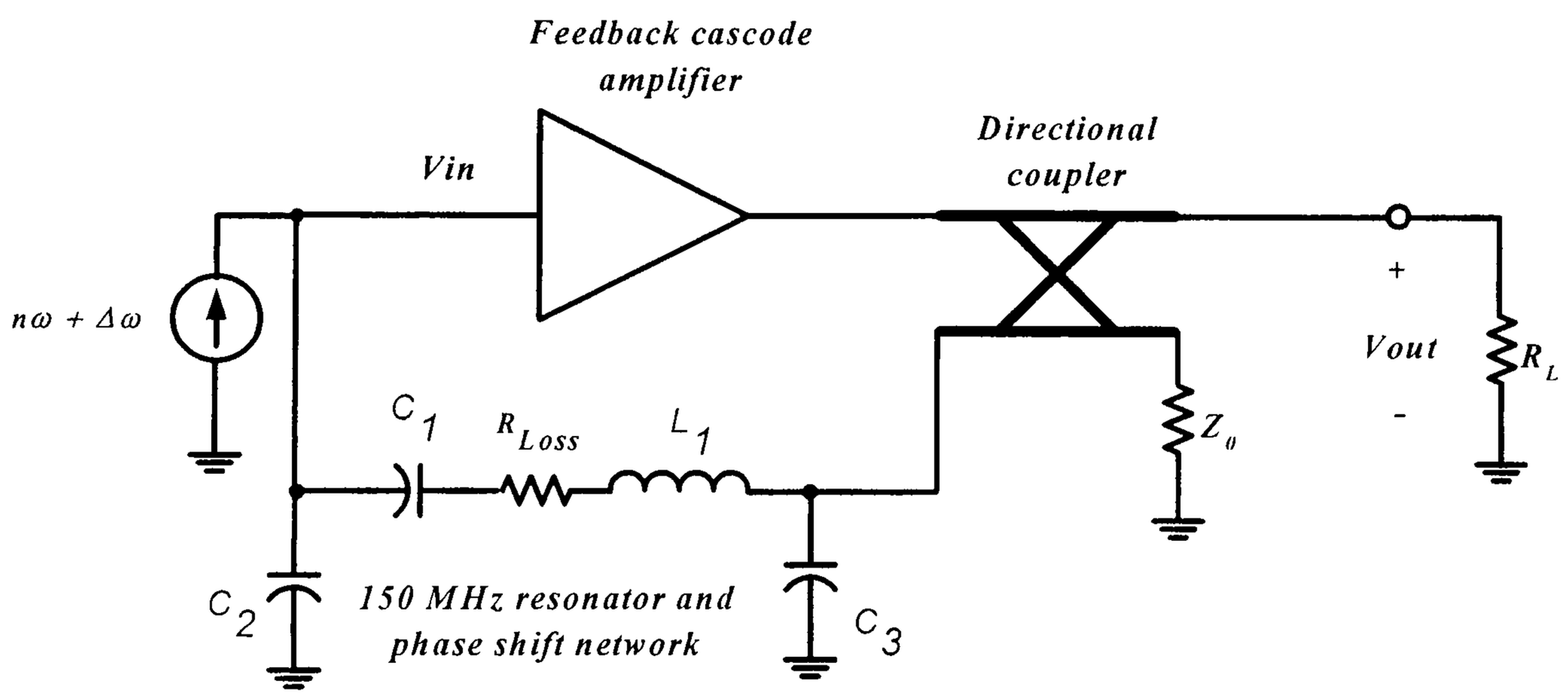


Figure 3.12 The oscillator model for the amplifier noise modulation investigation.

Noise modulation sensitivity simulation is performed by injecting sinusoidal current into the input node of the oscillator in Figure 3.12. The injected current source is 0.5mA with the frequency of $n\omega+\Delta\omega$, which is close to the nth harmonic of the oscillation frequency. For the single-ended cascade amplifier driven oscillator, the signal injection results in an equal pair of sidebands close to the carrier due to the injected signal at $\Delta\omega$ and $n\omega+\Delta\omega$, which is shown in Figure 3.13.

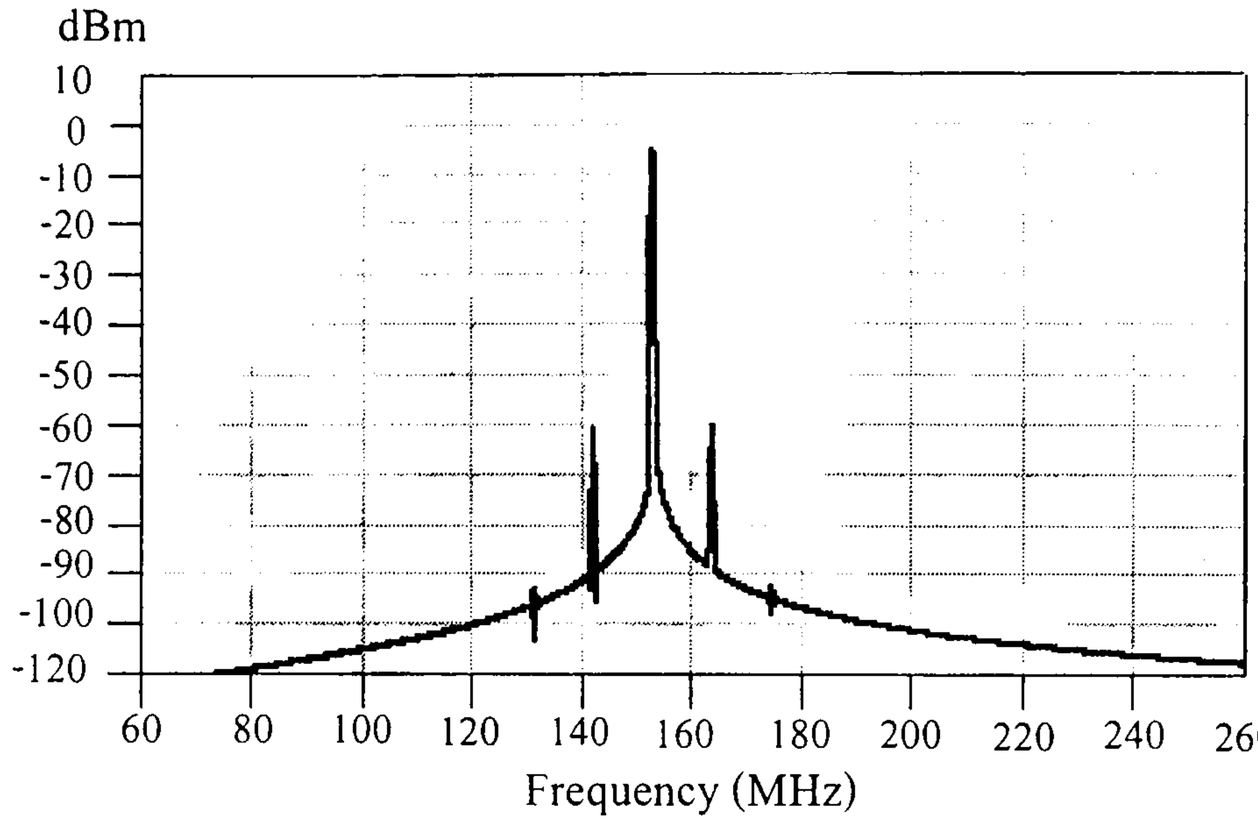


Figure 3.13 Output sideband of the oscillator driven by single-ended cascode amplifier when the injecting signal frequency is $3\omega o + \Delta\omega$.

The push-pull cascode amplifier driven oscillator shows very small sidebands when the injecting current frequency is close to even harmonics, while the single-ended cascode amplifier driven oscillator shows a considerable higher sideband power for all injecting signals at $\Delta\omega$ and $n\omega+\Delta\omega$.

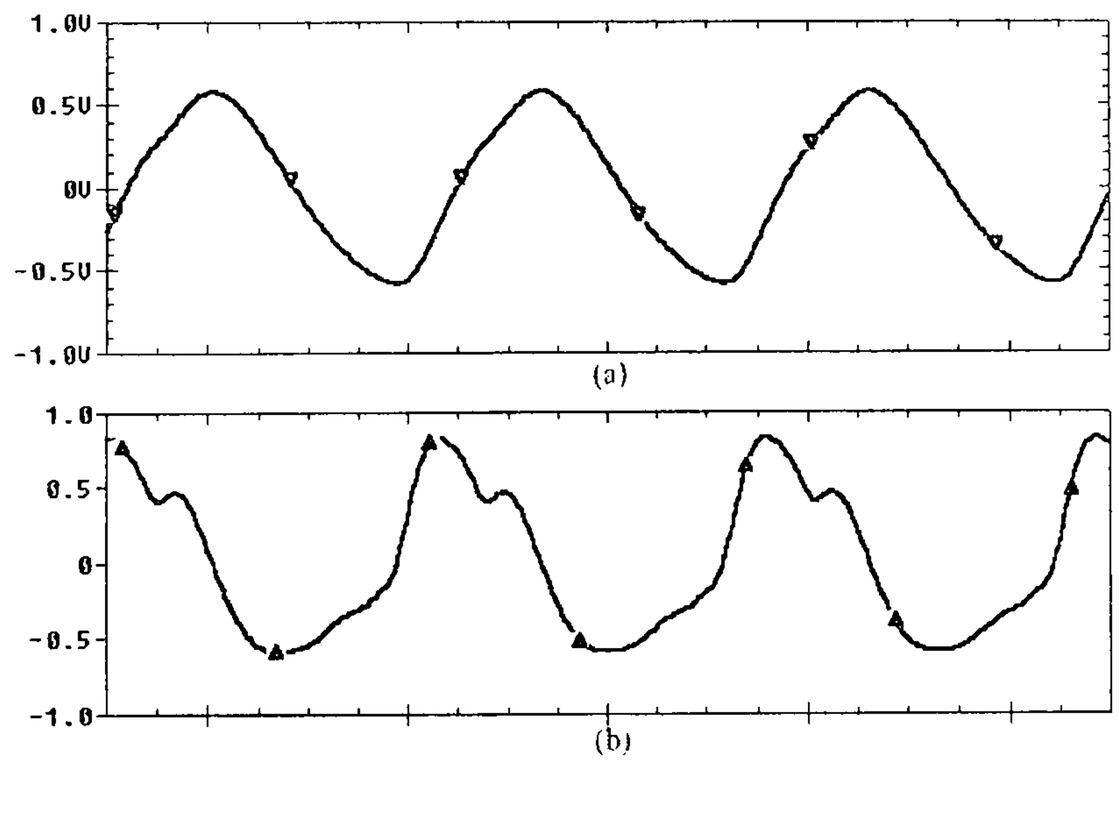


Figure 3.14 (a) Input node voltage and (b) ISF of a single-end driven oscillator.

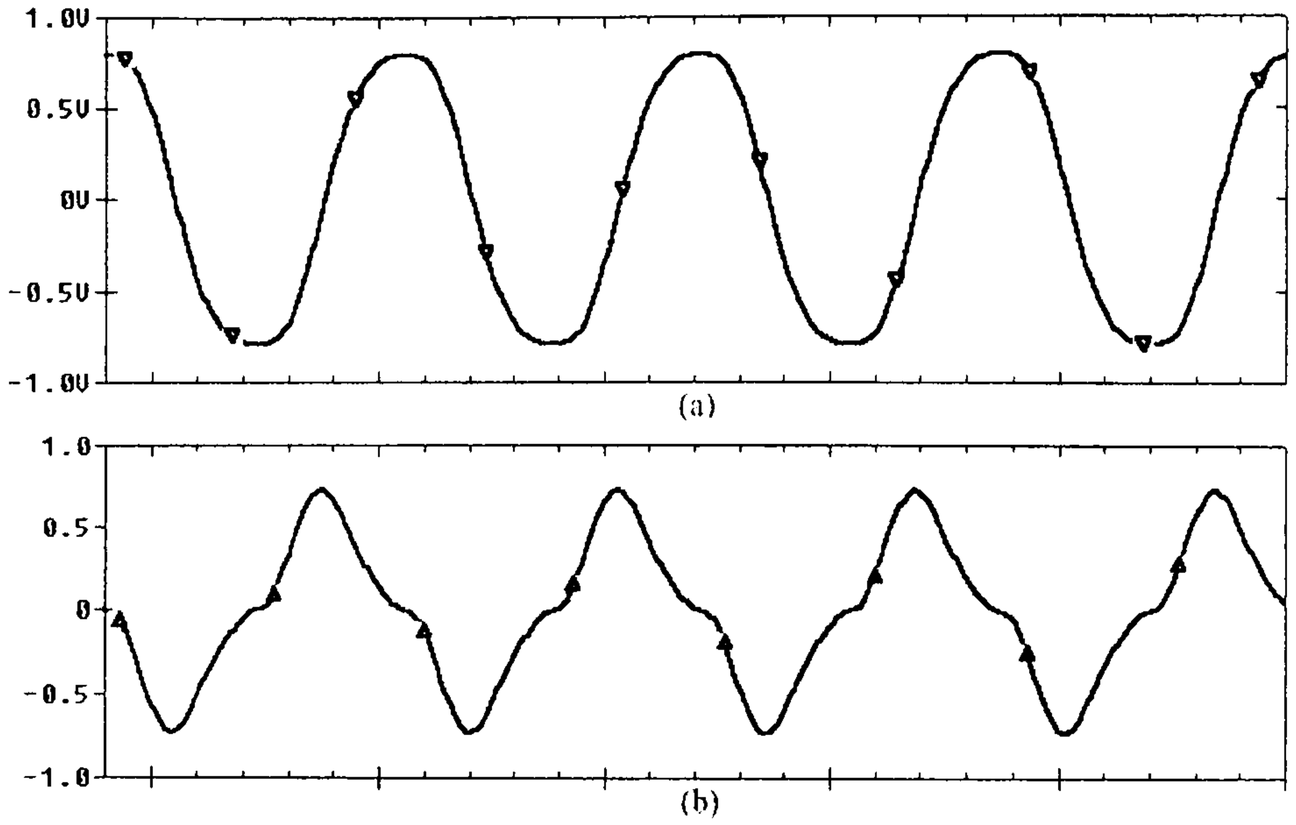


Figure 3.15 (a) Input node voltage and (b) ISF of a push-pull driven oscillator.

Figure 3.14 and Figure 3.15 show the input node voltage and the node impulse sensitivity function, ISF, of the two oscillators. The calculation of the ISF is based on the derivative method [3.6]. The ISF of the push-pull cascode driven oscillator has a symmetry waveform compared to an asymmetric ISF of the single ended driven oscillator, thus its noise conversion sensitivity at even harmonics of ω_o is very low, which is confirmed by the Fourier components, c_n, of the two oscillators shown in Figure 3.16 and Figure 3.17 respectively.

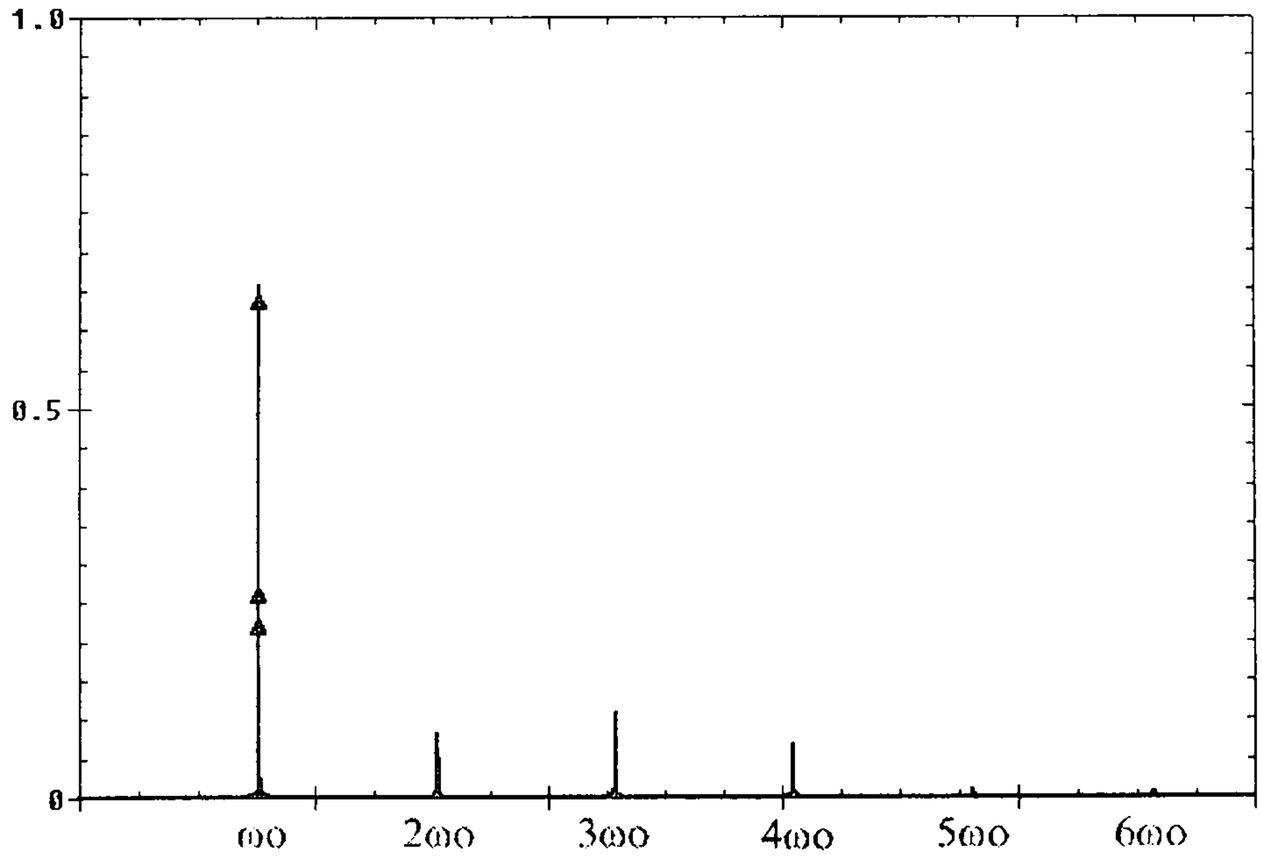


Figure 3.16 Fourier coefficient of ISF of the single-ended driven oscillator.

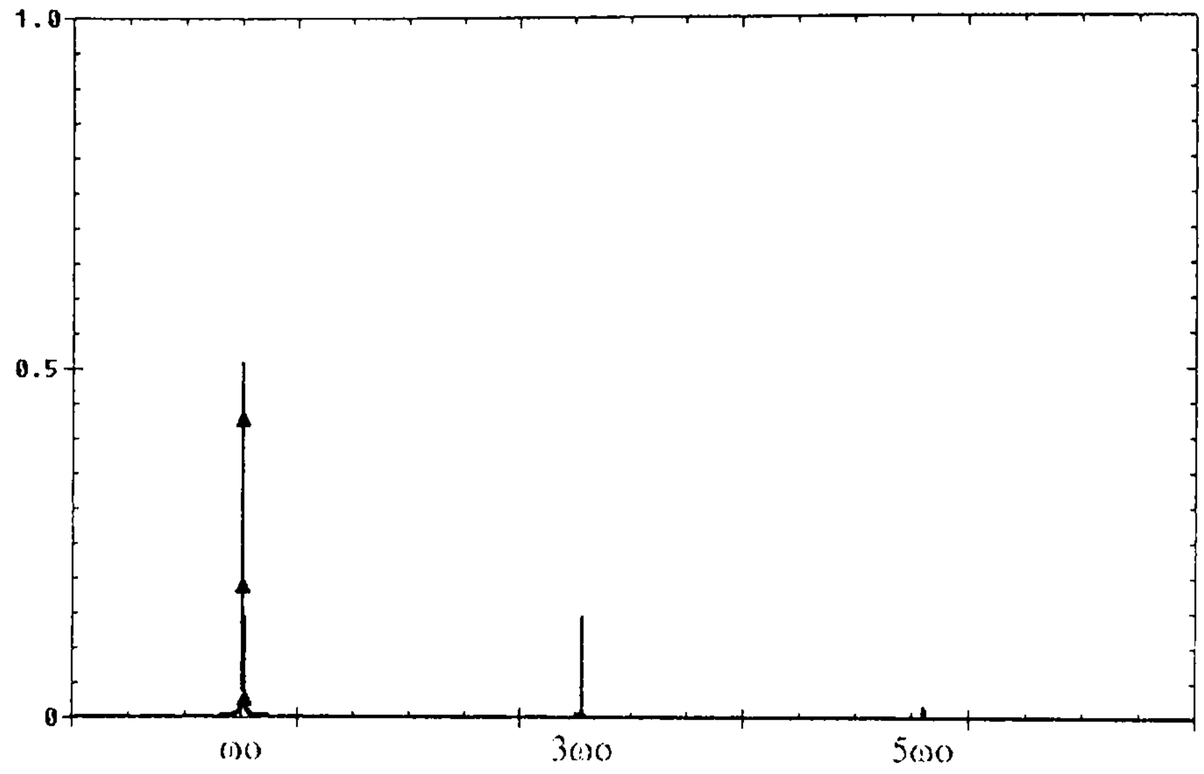


Figure 3.17 Fourier coefficient of ISF of the push-pull driven oscillator.

From the simulation results, the push-pull cascode driven oscillator shows smaller Fourier coefficients, thus lower noise conversion occurs. Since it has lower noise modulation sensitivity, lower phase noise can be anticipated from the push-pull driven oscillator compare to the single ended topology. This performance is also expected to retain in the transposed gain oscillator driven by the push-pull cascode amplifier.

However, the ISF depends on the driven signal waveform, which means that the noise modulation sensitivity is a power dependent variable. Thus, the noise modulation sensitivity of the oscillators (or amplifiers) depends on its operating power. It has been reported that the noise modulation of the amplifiers varies with the driven signal [3.13]. In the case of the Hall oscillator, the feedback ratio determines the steady state waveform, which in turn defines the noise modulation sensitivity.

3.2 Mixers

Both mixers play a key role in the TGA: mixer 1 determines the noise floor and noise figure of the system and its $1/f$ noise source is the dominant noise source of the overall amplifier [3.3-3.4]. The output power level of the TGA depends on mixer 2's characteristics. Even though only one sideband is needed, the output signal of mixer 2 should not exceed the conversion compression power level. Mixer 2 performs the upconversion function of the TGA, and thus the isolation of LO and RF ports is of prime importance because it determines the power level of the LO signal at the output port. In the frequency domain, this leakage signal lies in the middle of lower and

upper output sideband. The leakage signal is closer to the desired signal than the unwanted sideband.

Because of these necessities, a double-balanced diode mixer is the circuit of choice. In addition, noise modulation phenomena have less effect in balanced mixers compared to other mixer configurations as the balanced structures give minimum noise modulation sensitivity. A double-balanced diode mixer schematic is shown in Figure 3.18. It consists of four diodes and balun transformers T1 and T2.

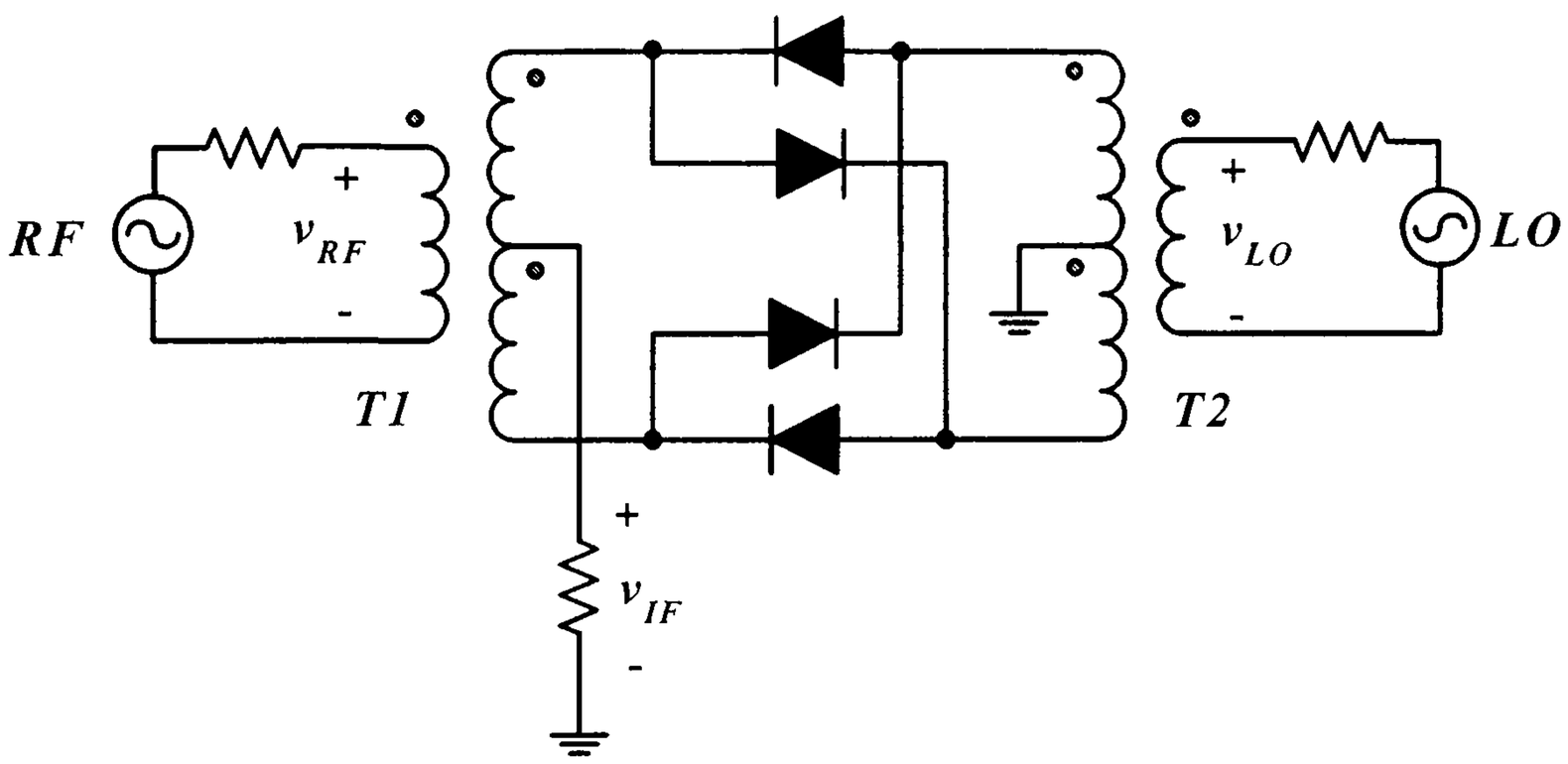


Figure 3.18 Double-balanced diode mixer with transformer baluns.

The local oscillator voltage v_{LO} is assumed to be large enough to turn the diodes completely on and off during every half-cycle and v_{LO} is assumed much greater than v_{RF} so that v_{LO} controls the diode states at all times. The diodes, then, act like switches and the output signal results from the multiplication of v_{RF} and a switching function. The output voltage is approximated by [3.15]:-

$$v_{IF}(t) = v_{RF} S(t) \tag{3.9}$$

where

$$S(t) = 2 \sum_{n=1,3,5\ldots}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos n\omega_{LO} t. \qquad (3.10)$$

The frequency domain signal of equation (3.10) contains only the frequencies $nf_{LO} \pm f_{RF}$. Neither f_{LO} nor f_{RF} appears in the output.

Typically, double-balanced diode mixers like that of Figure 3.18 need 7 dBm LO power and give a 1 dB conversion compression point of 0 dBm. If higher output power is needed, a higher level of mixer should be utilized. Figure 3.19 shows a class 2 type 1 [3.29] mixer which has a 1 dB conversion compression of 13 dBm at 20 dBm LO power.

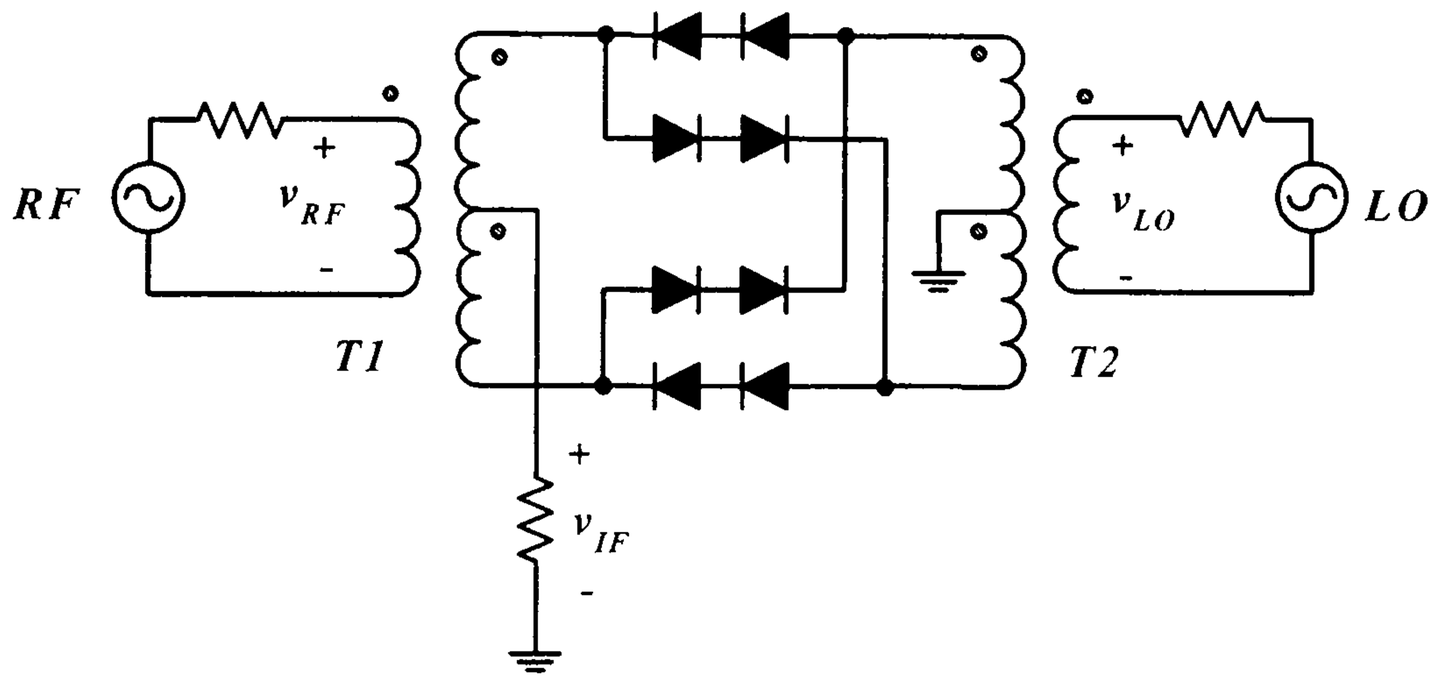


Figure 3.19 High level double-balanced diode mixer.

Figure 3.20 shows a SME 1400B-17 WJ Communications (former Watkins-Johnson) high level double-balanced diode mixer used in the transposed gain amplifier and oscillator experiments. The electrical characteristic of the diodes and baluns determine the mixer performance. The semiconductor device used almost exclusively nowadays in RF and microwave diode mixers is the silicon Schottky barrier diode or related structures [3.22], [3.30]. Below 3 GHz, balun transformers, which are typically wound on ferrite cores (beads, toroids or multi-apertures), can be designed to exhibit extremely broadband performance [3.31-3.32]. Mostly, the transformer performance is influenced by a variety of factors, such as core material, wire size and winding length, size and aspect ratio.

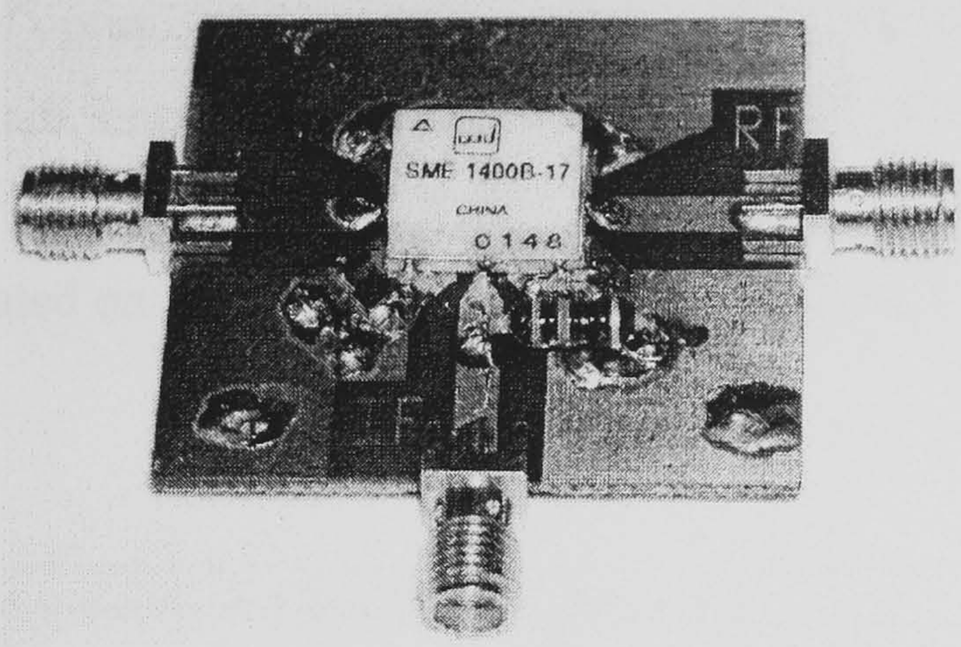


Figure 3.20 SME 1400B-17 double-balanced diode mixer assembled on FR-4 substrate.

Although there are high intercept point Gilbert's cell mixers operating up to microwave frequency [3.9-3.10], [3.33], their noise figure still cannot compete with the balanced diode mixers.

3.3 Power Divider Networks

Both resistive and Wilkinson power dividers can be used in the transposed gain amplifier as the LO output power divider. The resistive power dividers have higher loss and lower isolation, thus Wilkinson power dividers are preferred. The schematic of a broadband 2 sections Wilkinson power divider is shown in Figure 3.21 [3.34].

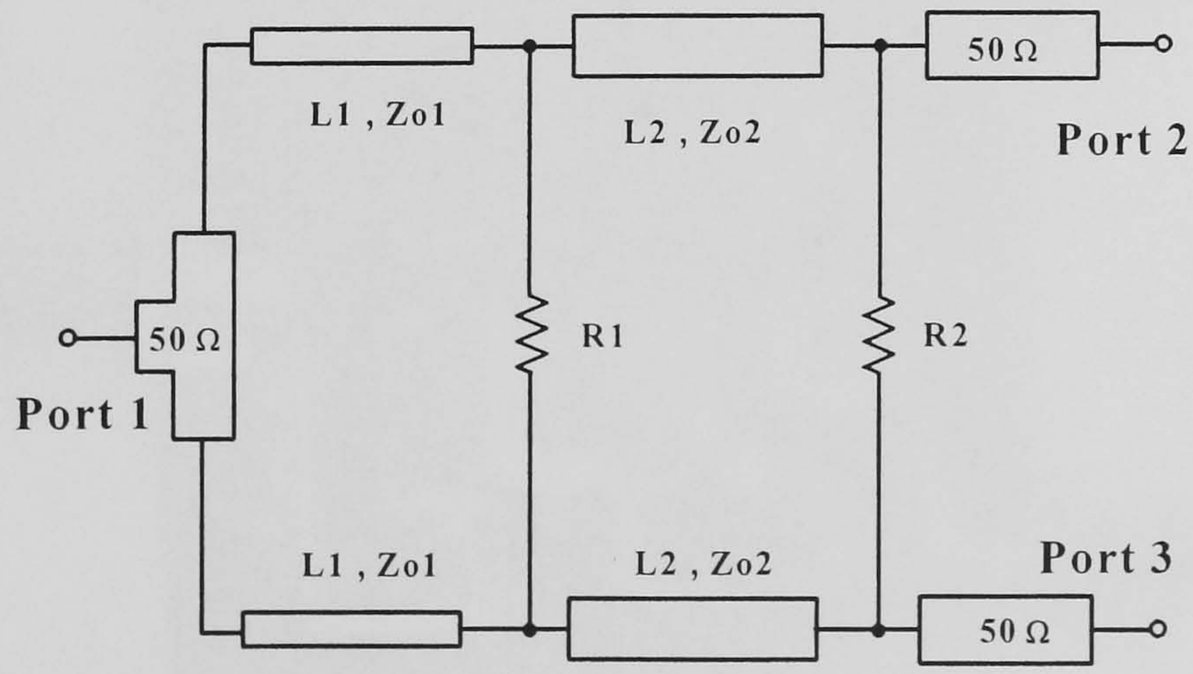


Figure 3.21 Broadband Wilkinson power divider.

The power divider is optimised to operate over the 400-1200 MHz frequency range for the transposed gain amplifier experiments. Figure 3.22 shows the measurement results of the power divider using a 1.6 mm glass-epoxy substrate. The Wilkinson power divider fabricated on FR4 material is shown in Figure 3.23.

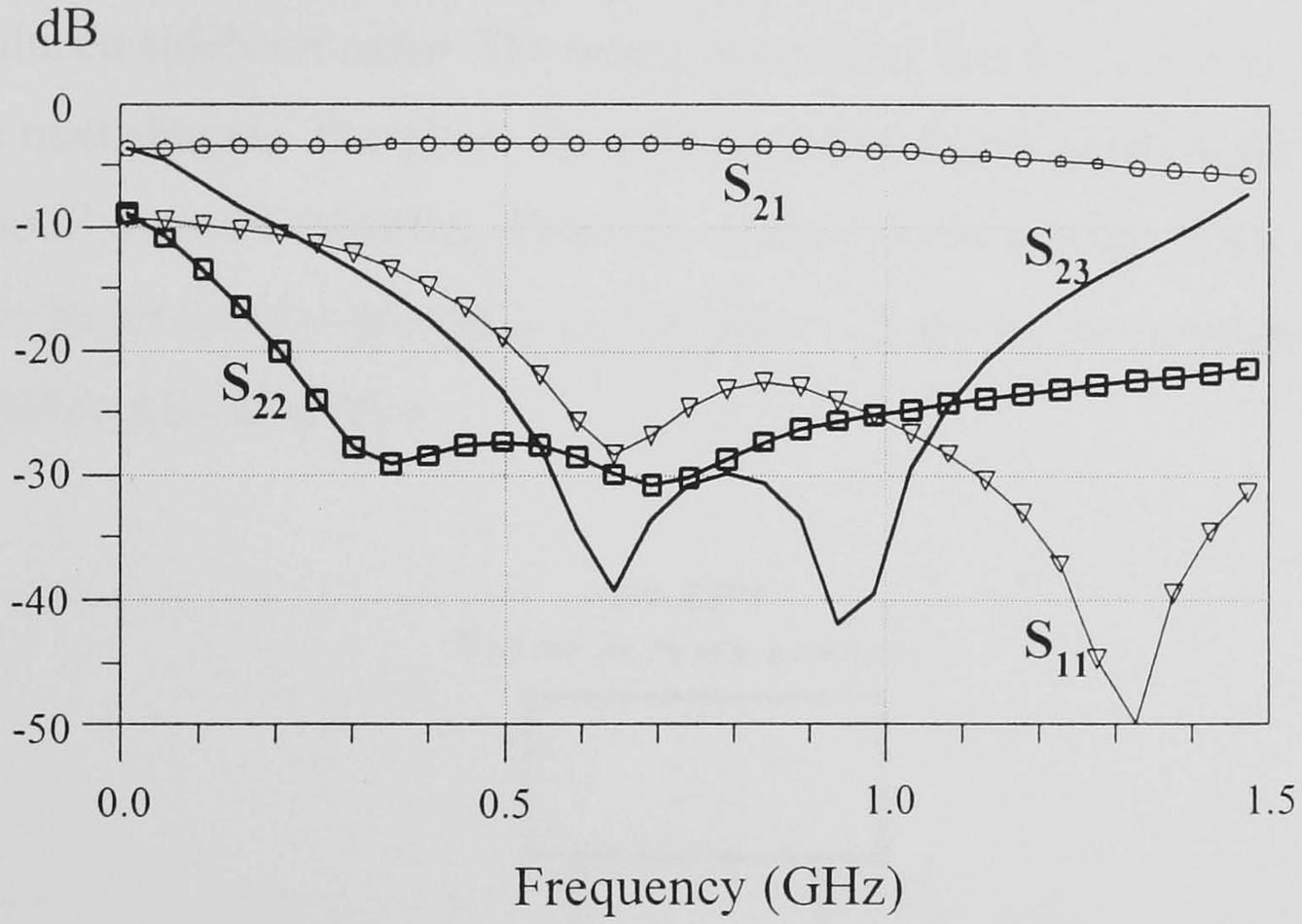


Figure 3.22 Measurement results of the wideband Wilkinson power divider.

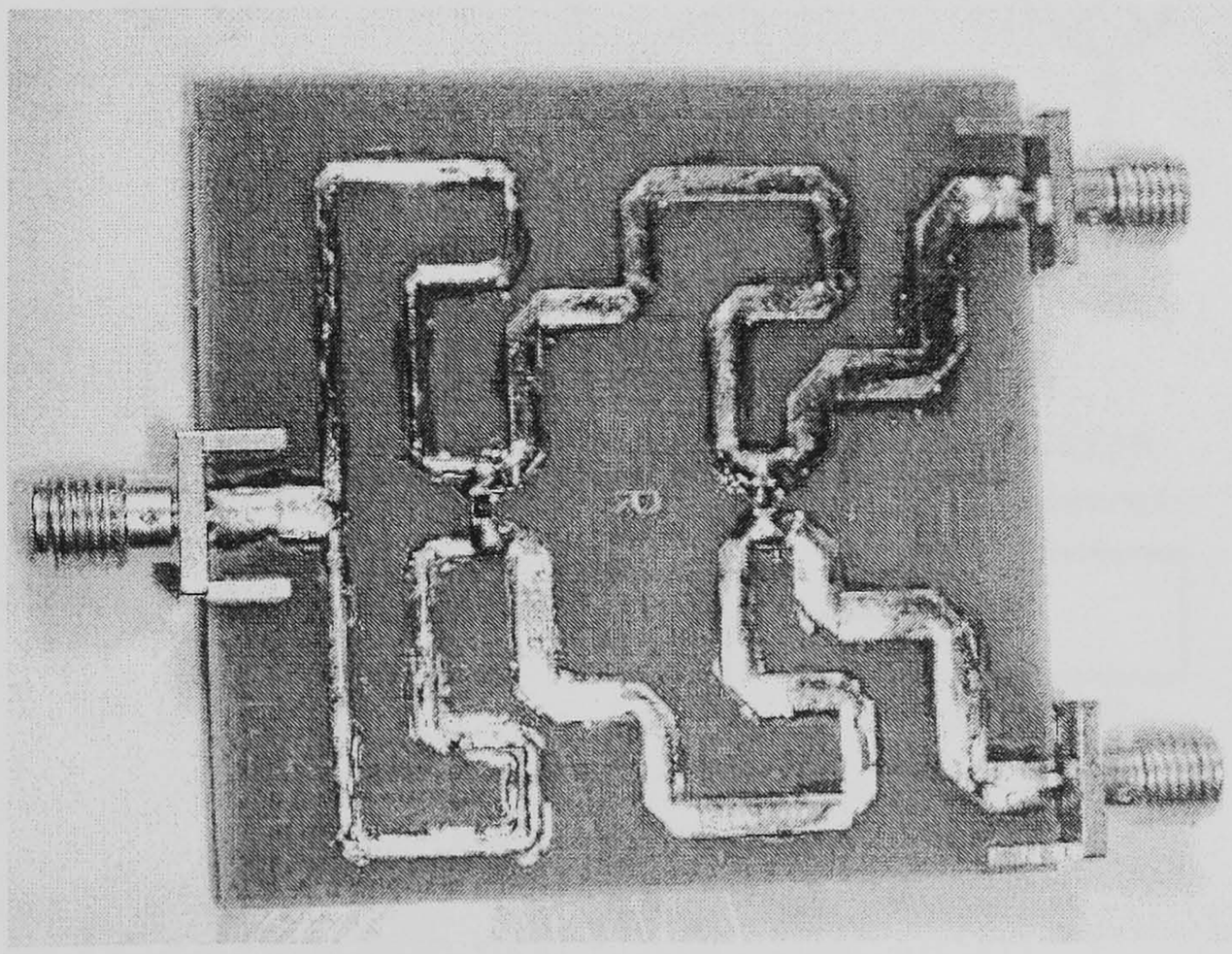


Figure 3.23 0.4-1.2 GHz Wilkinson power divider fabricated on FR4 substrate.

3.4 Transposed Gain Amplifier Experiments

Figure 3.24 shows the set up block diagram for a 200 MHz bandwidth transposed gain amplifier experiment. The local oscillator signal of 800 MHz comes from a HP RF signal generator. A delay line made of RG-316 PTFE coaxial cable is inserted between the power divider and the second mixer in order to preserve the output signal from LO induced sideband noise. The important role of this delay line is mentioned in detail in the next chapter. The phase delay of the delay line is equal to the group delay of the push-pull cascode amplifier. From the measurement and the simulation results, the amplifier group delay is around 2.2 ns. Figure 3.25 shows the measurement results of the transposed gain amplifier.

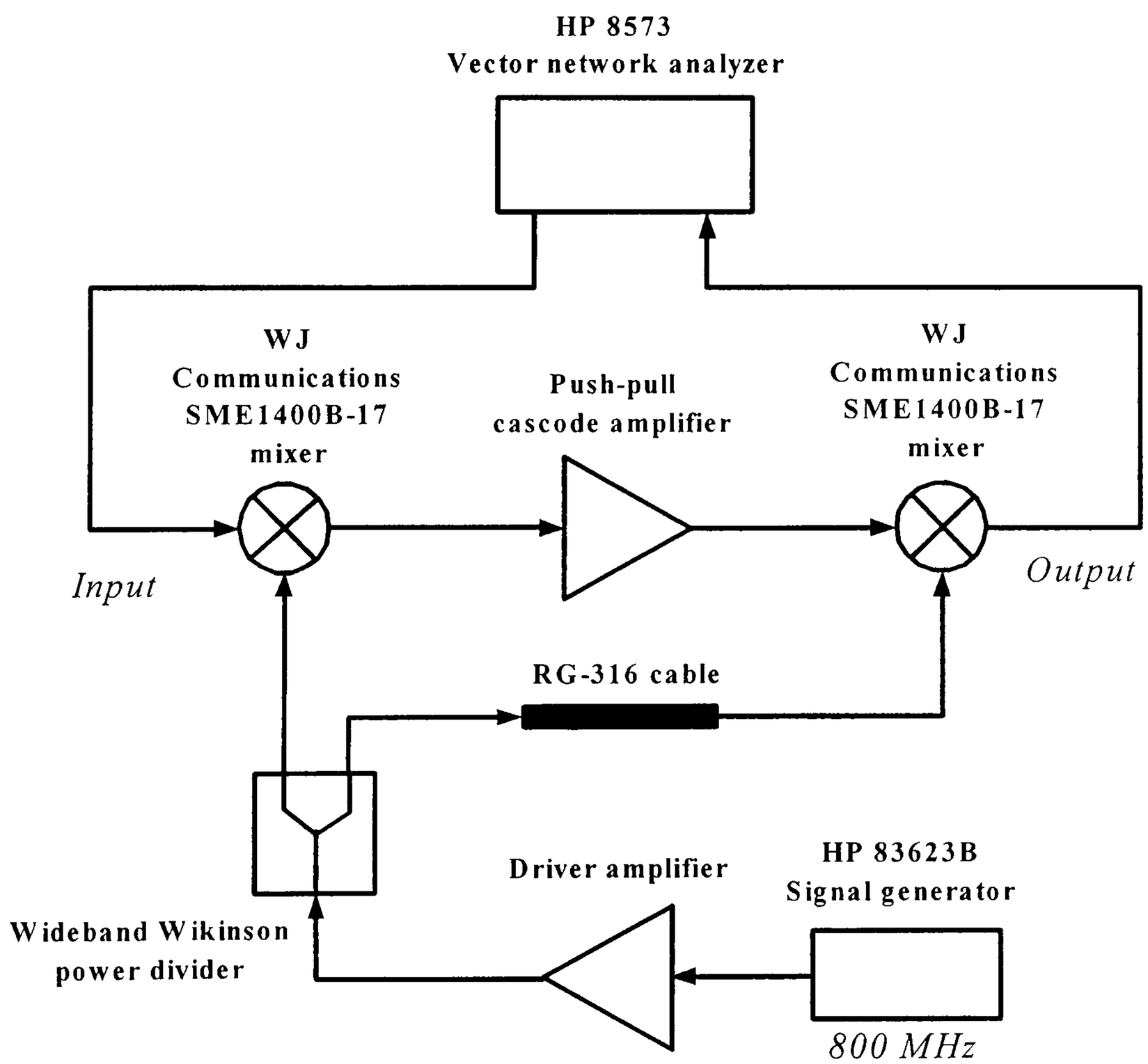


Figure 3.24 Transposed gain amplifier experiment set up.

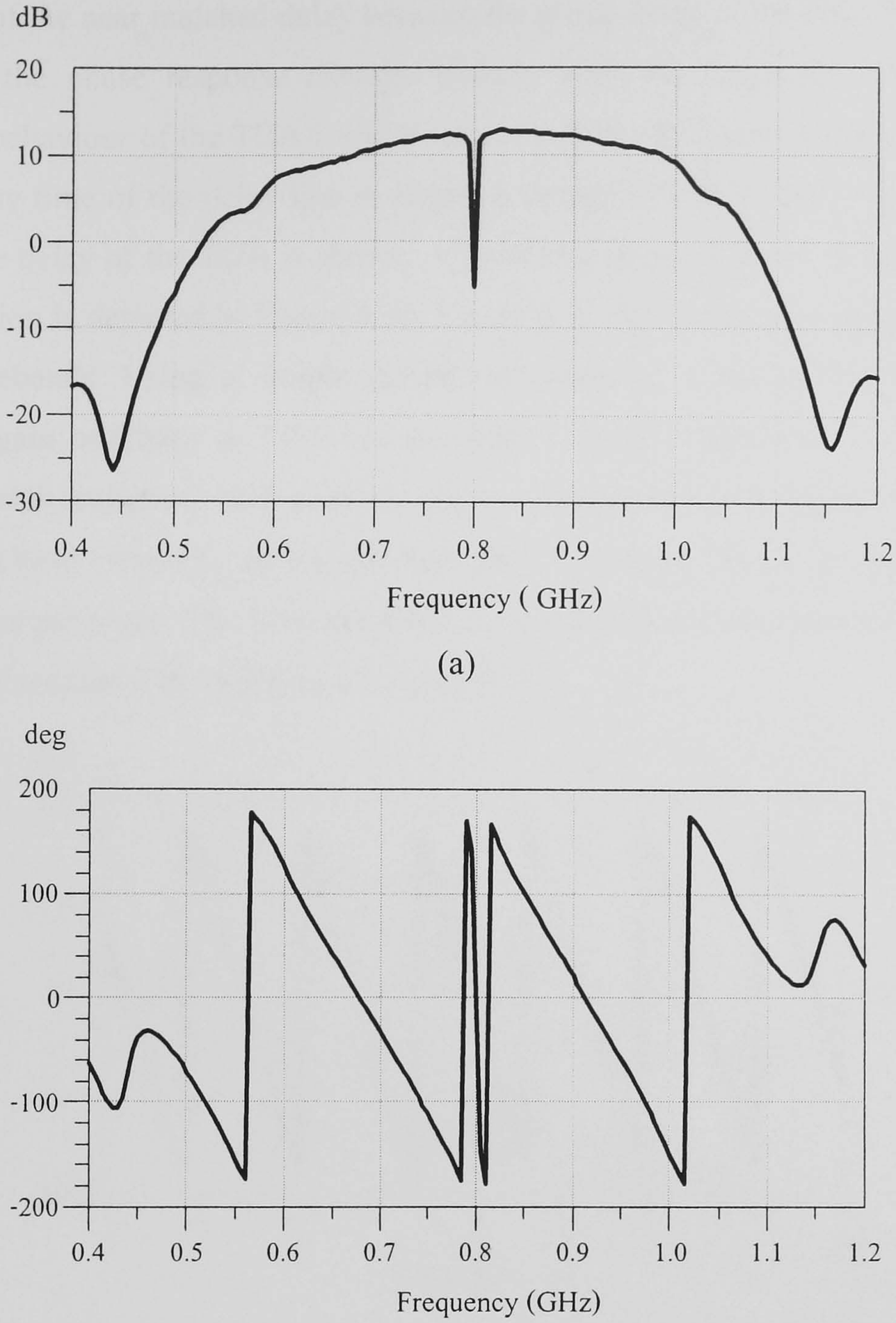


Figure 3.25 Transducer gain (a) and phase response of the transposed gain amplifier (b).

As can be seen, there are two sideband responses around the notched LO carrier frequency. The magnitude of the power gain is approximately equal to the power gain of the push-pull cascode amplifier minus two times the mixer losses. The input-output isolation of the TGA is exceptional high. The TGA gains its high isolation from the reverse transfer characteristic of the IF amplifier plus two times the RF-IF port isolation of the double-balanced mixer.

In the case of the near matched delay between the group delay of the amplifier and the delay line, the phase response changes linearly with the frequency. There is an interesting behaviour of the TGA's phase response. If the RF input frequency is fixed and the delay time of the delay line is varied, a strong relation of the phase response and the time delay of the TGA is shown. A simulated phase response due to the time delay variation is depicted in Figure 3.26. Figure 3.25 (b) shows zero-phase one time in both sidebands. Using a simple parallel resonator as a feedback network, the transposed gain oscillator or TGO can be made at these frequencies. If there is no delay mismatch and phase shift problem due to coupling network, Figure 3.26 shows many zero-phase crossings during the time delay variation. Thus, the TGO can be made at these positions. The TGA can provide closely space zero-phase frequency for a multimode resonator by changing the delay time.

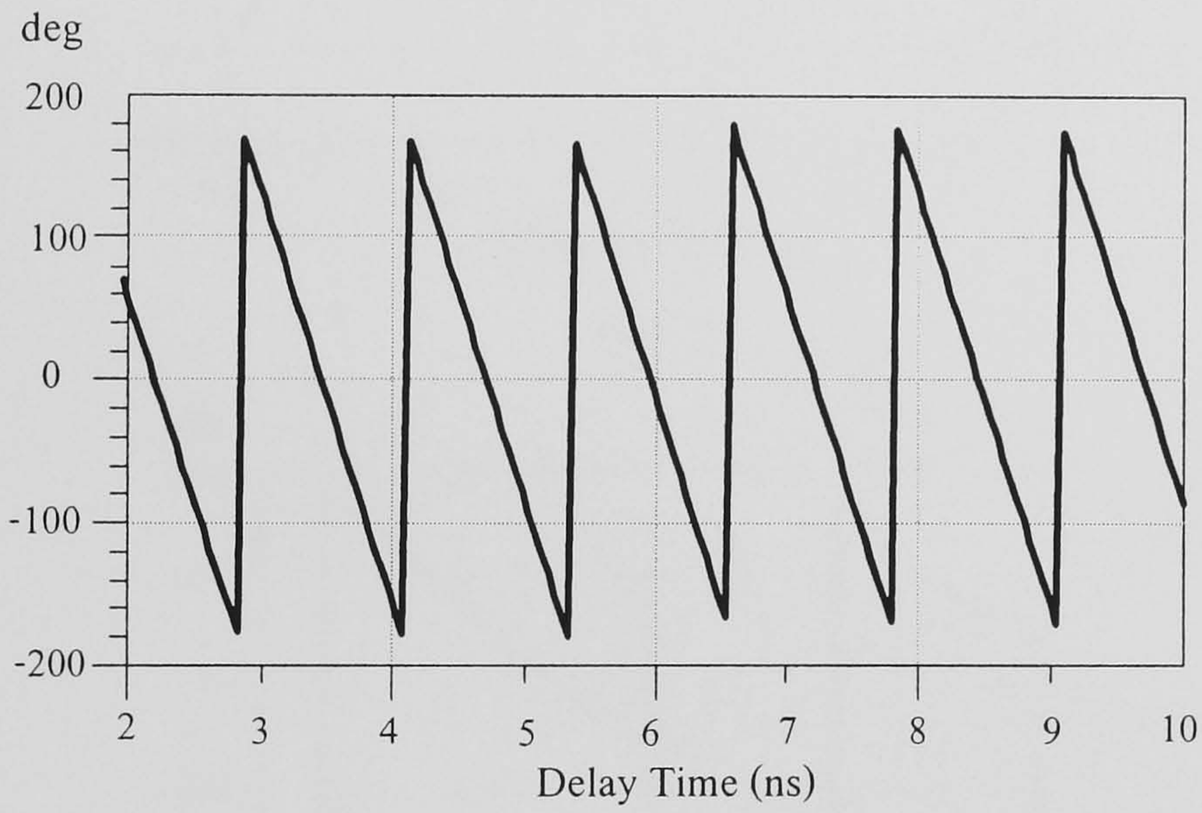
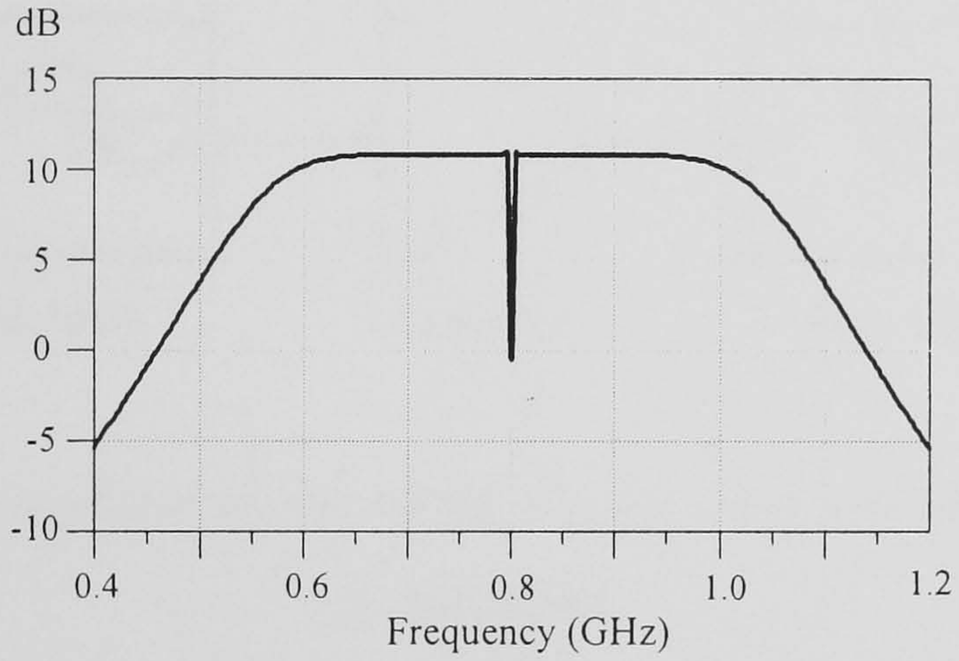


Figure 3.26 Phase response of the transposed gain amplifier as a function of delay line time delay.

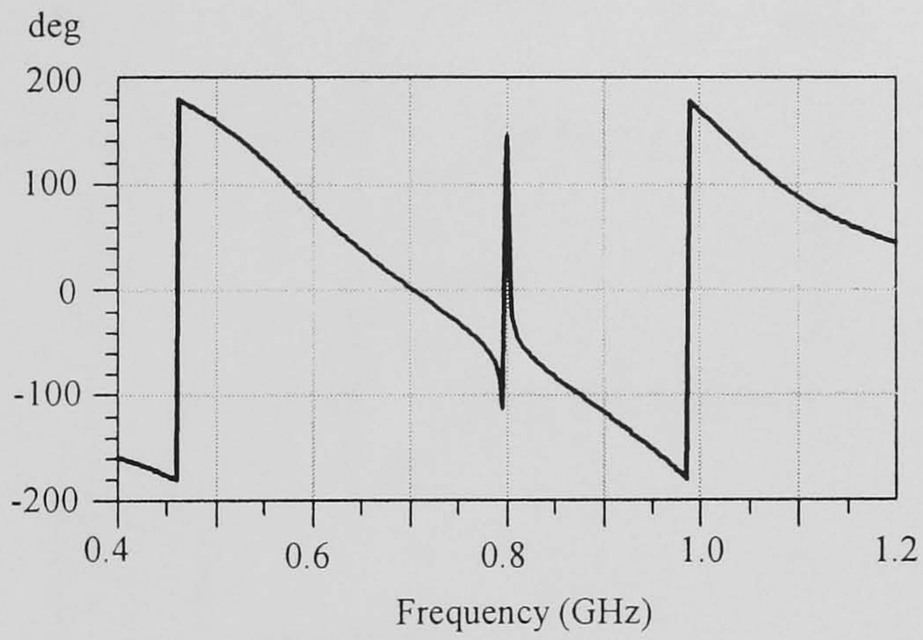
3.5 The Low Pass Response: Novel TGA Techniques

Figure 3.27 shows a typical ideal response of the TGA. There are two sidebands response around the notched LO carrier frequency. These sideband characteristics depend on the magnitude response of the IF amplifier and the mixer losses (or gain). The notched frequency on the pass band response is equal to the LO frequency. Except the notched frequency, the total magnitude response has a double-side band pass characteristic. This magnitude response occurs because the high-side cut off frequency of the IF amplifier is far lower than the LO frequency. The IF amplifier has

no power gain at the LO frequency. However, if the amplifier, in this case it may be called an RF amplifier, has power gain at the LO frequency the magnitude response is different. The total magnitude response of the new TGA depends on mixers characteristic as well. In theory, the magnitude response of the amplifier becomes low pass down to the DC signal. This response can be employed as an analog signal processing core circuit to suppress the LO sideband noise.



(a)



(b)

Figure 3.27 Ideal magnitude (a) and phase (b) response of a conventional band pass TGA.

3.5.1 Low Pass Response TGA Operation

To investigate the low pass response TGA or LP-TGA, the behavioural models are employed. Figure 3.27 shows the behavioural model of the RF amplifier. The amplifier has the transfer characteristic as shown in Figure 3.2 (b). The amplifier model is band limited by a 4^{th} order Butterworth 10 MHz high pass filter and a 2000 MHz low pass filter. The block diagram of the low pass response TGA is shown in

Figure 3.28. There are two amplifiers, which have the same characteristic, and two mixers. The attenuator is included in order to prevent amplifier 2 from being driven into the saturation region. For the performance investigation, the following parameters are used, the input signal frequency is varied from DC to 1600 MHz and the pumped LO frequency is 800 MHz. At DC, mixer 1 generates an IF output signal of 800 MHz. At above DC signal, mixer 1 produces two sidebands.

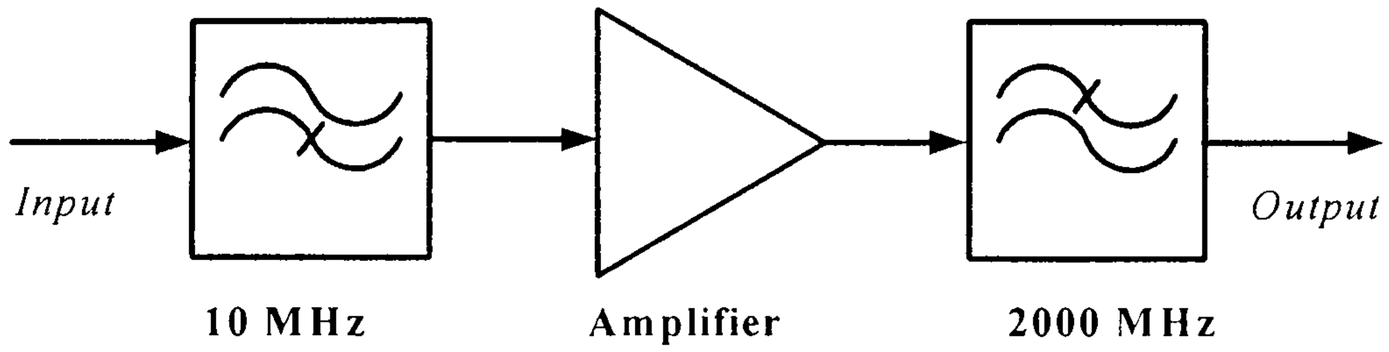


Figure 3.28 RF amplifier model for the low pass response TGA performance investigation.

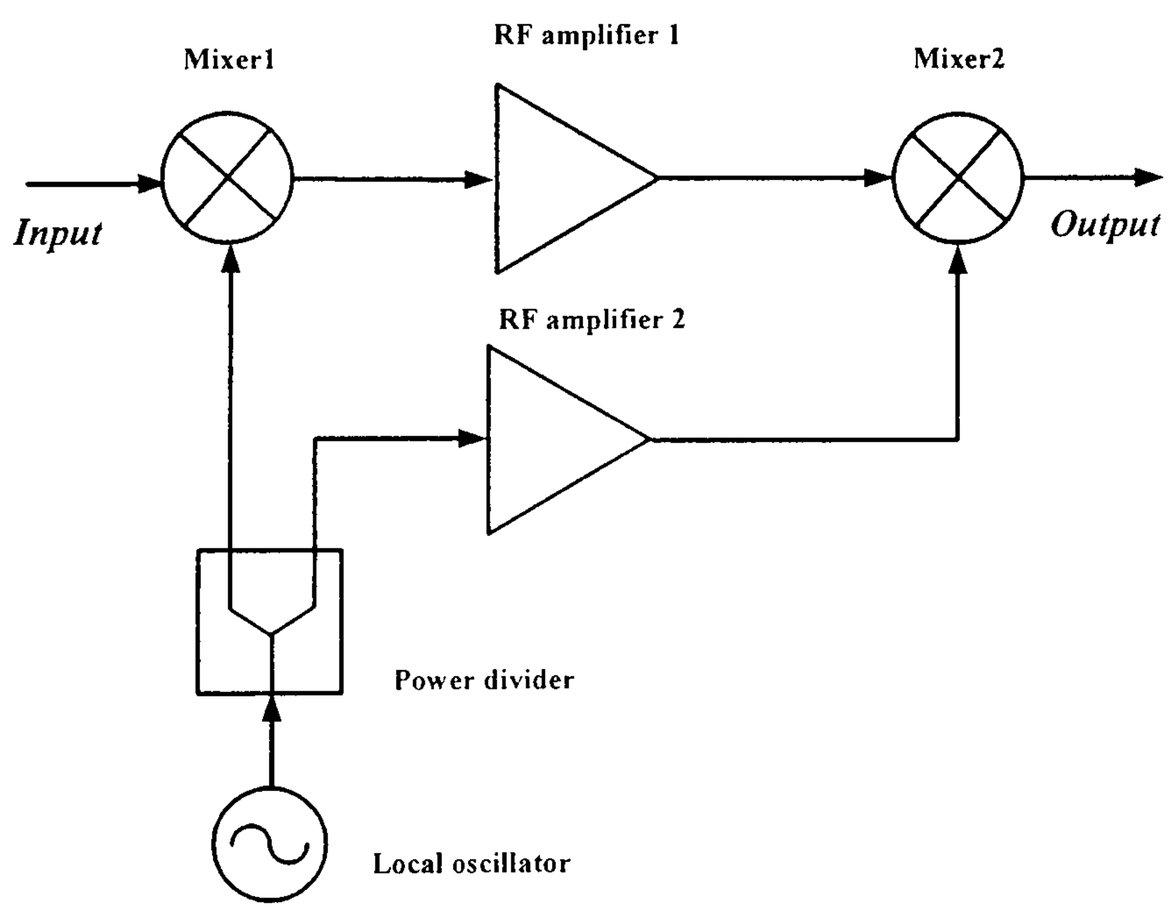


Figure 3.29 Building block of the low pass response TGA.

Using large signal s-parameter simulations, the magnitude and phase response of the low pass response TGA is shown in Figure 3.30 (a) and (b). Both the magnitude and phase responses exhibit discontinuity at the LO frequency. The notch width on the magnitude response curve depends on the difference between the low frequency cut off of the RF amplifier and the DC frequency.

As can be seen, the ideal LP-TGA has a linear phase response over a wide range of the input frequency. If the amplitude loss due to the mixer's operation is neglected, the magnitude response of the low pass TGA differs from the frequency response of the amplifier in Figure 3.27. The low frequency response of the new TGA is extended to DC frequency. However, the pass band response of the LP-TGA is modified from the original RF amplifier response.

(a)

(b)

Figure 3.30 Magnitude (a) and phase (b) response of the low pass response TGA.

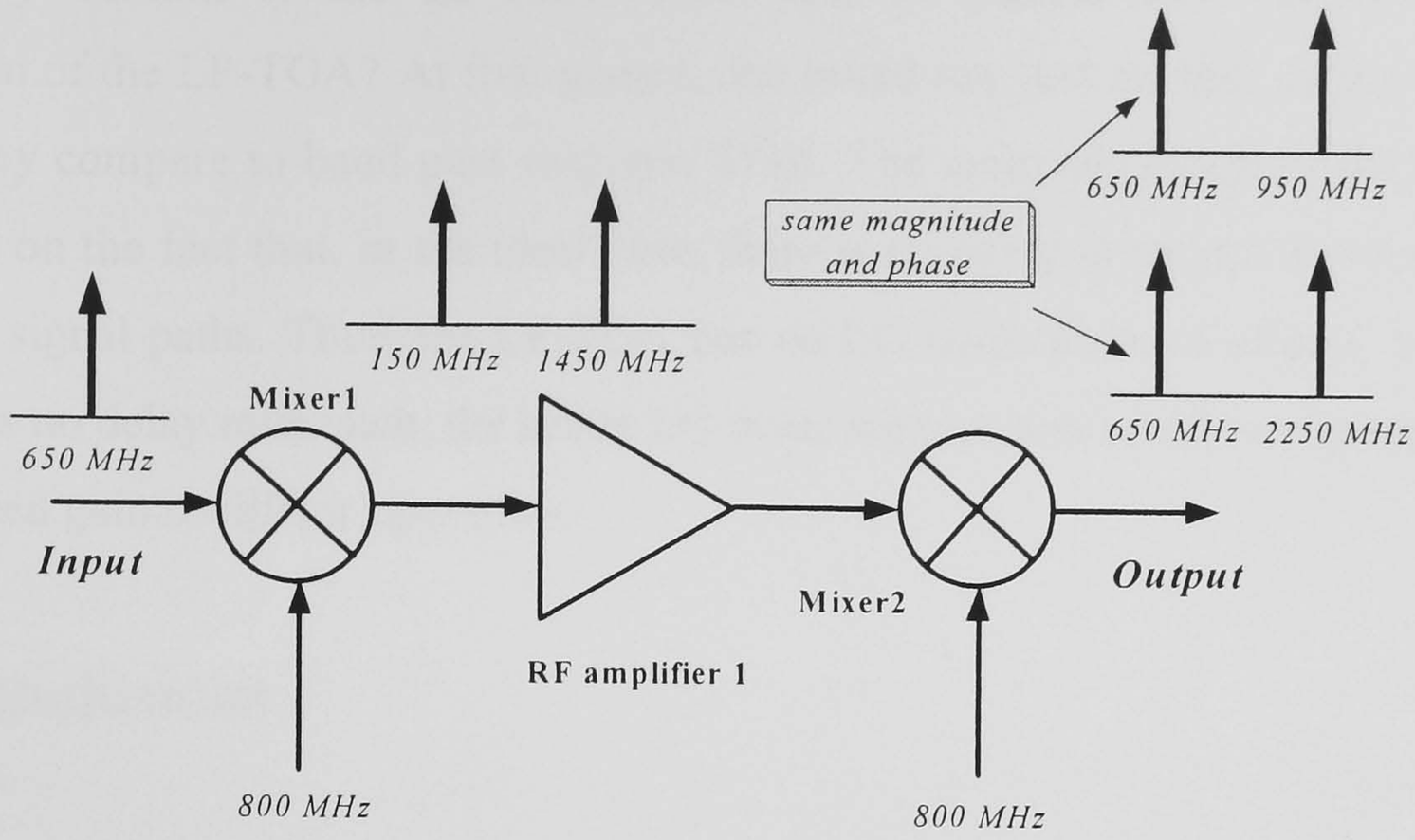


Figure 3.31 Mixing process in the low pass response TGA.

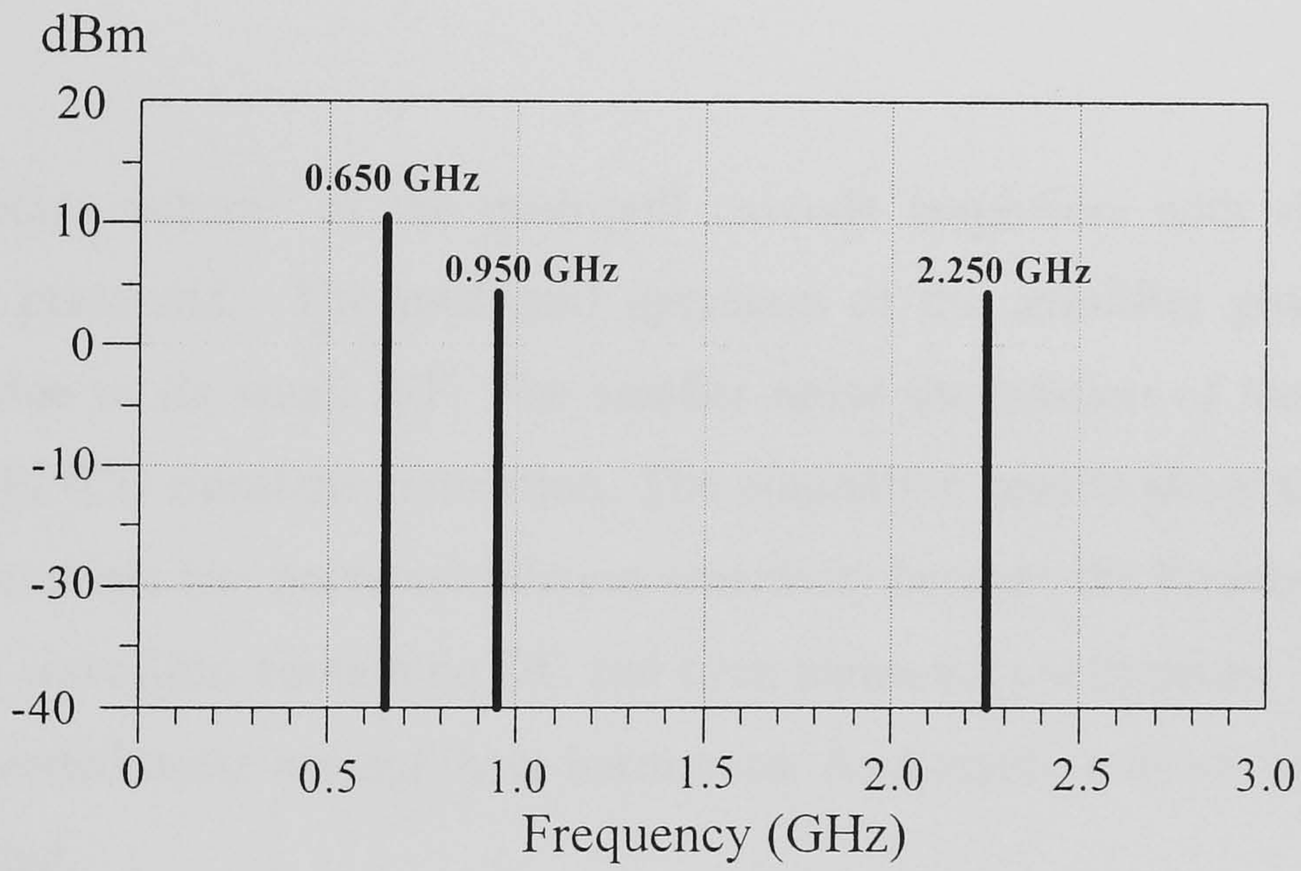


Figure 3.32 Simulated output signal in the frequency domain of the LP- TGA.

The modification of the pass band response happens at mixer 2. If the input frequency is fixed, this behaviour can be examined. Assume that the input frequency is equal to 650 MHz, the first mixer produces two sidebands at 150 and 1450 MHz. When these signal are upconverted by the same 800 MHz LO signal, mixer 2 gives four output products but two are at same frequency and same phase. These two products are an amplified version of the 650 MHz input signal. Figure 3.31 shows the mixing operation of the LP-TGA. Figure 3.32 shows the simulated output signal in the

frequency domain of the LP-TGA. What can be gained from the complicated operation of the LP-TGA? At first glance, one might say just another output sideband frequency compare to band pass response TGA. The main advantage of the LP-TGA is based on the fact that, in the ideal case, there is no delay mismatch between the IF and LO signal paths. Thus, the LP-TGA has no LO noise induced effects. Since LP-TGA has no delay mismatch, the better LO noise suppression could be expected in the transposed gain oscillator operation.

3.5 Conclusions

In this chapter, the transposed gain operation of the transposed gain amplifier has been investigated. The important role of the IF and LO signal path delays in the TGA is addressed. Phase response of the TGA is a strong function of the LO path delay.

The design scheme of the push-pull cascode amplifiers with simple design equations is presented. The push-pull operation of the amplifier gives less noise modulation due to its small ISF. The smaller noise modulation of the amplifier is proven by PSPICE transient simulation. The simulation results show that push-pull driven oscillator has less noise modulation sensitivity because the Fourier components of the output waveform contain no DC and even harmonic coefficients. Thus, there is no downconverted noise around these harmonics. As a result, a lower noise sideband can be expected.

A LP-TGA has been introduced. In this new scheme, two RF amplifiers which has the same group delay time at both IF and LO frequencies are employed in both IF and LO signal paths. The frequency response of the new amplifier starts from DC even though both RF amplifiers have a band pass characteristic. There is no path delay mismatch in the LP-TGA, thus there is no sideband noise induced by the LO phase noise.

Chapter 4

The Transposed Gain Oscillators

The transposed gain oscillator is not strictly a feedback or feedforward phase noise reduction technique. It is a combination of feedforward and feedback methods. Pan and Arnold patented ' High-Q multi-mode resonator controlled source' in 1981, which used the transposed gain of a low frequency RF amplifier to sustain the oscillation of a bulk acoustic wave resonator [4.1]. At that time, the main object when the circuit was invented was to sustain the oscillation of the oscillator circuit. The feedforward path of the oscillator, which is shown by the dash-line, is called the transposed gain amplifier or TGA. More recently, various authors have considered transposed gain and measured phase noise performance [4.2-4.5].

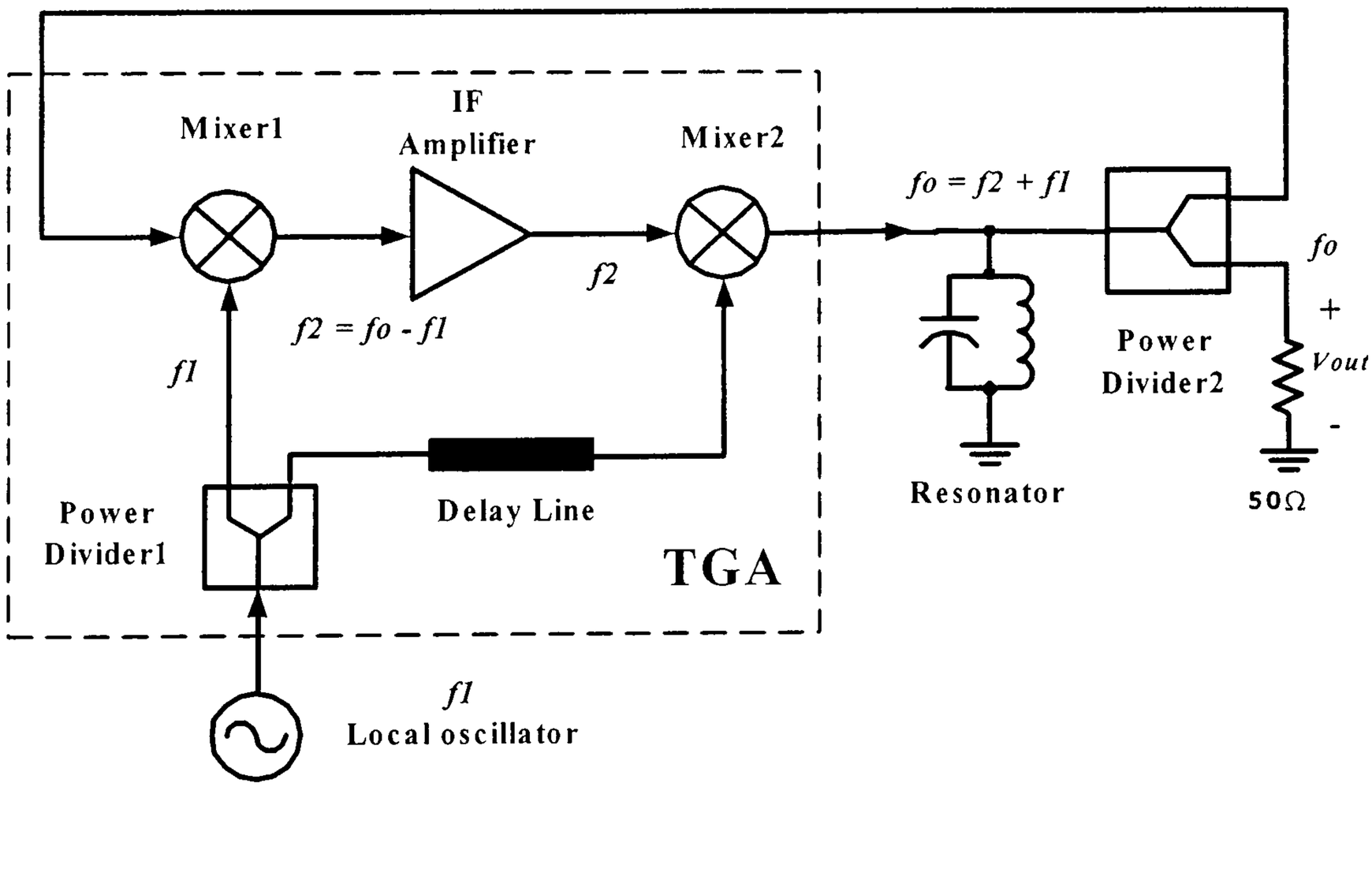


Figure 4.1 Transposed gain oscillator.

4.1 Oscillator Operation

The transposed gain oscillator, also known as the double frequency conversion oscillator, is called transposed-gain because the oscillation-sustaining loop gain is achieved by a transposition of low frequency IF amplifier gain to higher RF frequencies on both sides of the local oscillator signal. The frequency of the local oscillator is then applied at a frequency close to that required for the gain. By utilizing two mixers, the downconverted microwave signal can be amplified by a low frequency IF amplifier and then upconverted back to the resonator frequency using the same LO signal. This signal path can be considered as a feedforward path. A delay line in this path performs a delay compensation for the IF amplifier's delay. The upconverted signal is then fed back to the downconversion mixer via the resonator. This resonator (feedback path) determines the oscillation frequency, f_o.

The output frequency, f_o is stabilised by the operation in both feedforward and feedback paths. If the frequency f_1 from the local oscillator begins to rise, then the frequency f_2 at the output of the second mixer decreases proportionally to compensate for this rise in the LO frequency. A similar compensation is also gained when the LO frequency begins to decrease. Thus, the double frequency conversion oscillator achieves precise control of the output frequency, $f_1 + f_2$, even though the circuit is driven by a non-stable or noisy local oscillator [4.1].

4.2 Phase Noise Reduction in Transposed Gain Oscillators

In general, it can be assumed that there is no amplitude fluctuation, $A(t)$, on the carrier because of oscillator limiting mechanisms. Only phase fluctuation $\phi(t)$ gives rise to sidebands close to the frequency of oscillation and its harmonics in a frequency modulation mode. Therefore, the LO carrier with phase noise can generally be represented by an FM signal.

The phase noise reduction mechanism of the transposed gain oscillator is similar to the principle of the "delay and multiply" FM signal demodulator. In case of the quadrature FM detector, the multiplication of the FM signal and its delayed version gives two output signals which are second harmonics with double modulation index and low frequency term. The low frequency term is linear in frequency deviation and

reproduces the modulating signal [4.6]. This low frequency term also gives phase noise information and DC signal in phase noise measurements. If two FM signals with identical modulating frequency and modulation index, but with carrier frequencies that are different and no time delay between them, are multiplied together, the multiplying product also gives a two terms signal. One term consists of an FM signal, whose modulation index is doubled and whose carrier frequency equals to the sum of two carrier frequencies. The other is a difference term, and this term gives an RF carrier for which all FM sideband components are removed. This suppression is performed at mixer 2 and it is depicted in Figure 4.2.

Since there is no amplitude fluctuation, the noise-corrupted LO can be represented by a frequency modulation signal which can be written as [4.7-4.8]:-

$$f_1(t) = V_1 \cos\left[\omega_1 t + \beta \sin(\omega_m t)\right] \tag{4.1}$$

where V_1 is the carrier maximum voltage, ω_1 is the carrier frequency which has peak frequency deviation equal to $\Delta\omega$, ω_m is a modulating signal and β is a modulation index ($\Delta\omega / \omega_m$). The downconverted signal, f_2, retains the same modulation index and modulating signal but has a different carrier frequency. The downconverted signal can be expressed as:-

$$f_2(t) = V_2 \cos\left[\omega_2 t + \beta \sin(\omega_m t)\right] \tag{4.2}$$

where V_2 is a signal maximum voltage, ω_2 is the lower sideband output frequency of mixer 1.

If a perfect multiplier is assumed, the output voltage of mixer 2 in the time domain is given by:-

$$V_{out}(t) = f_1(t) f_2(t) \tag{4.3}$$

or in the frequency domain

$$V_{out}(\omega) = \frac{1}{2\pi}\left[F_1(\omega) * F_2(\omega)\right]. \tag{4.4}$$

The convolution of f_1 and f_2 spectral density gives rise to the output signal of mixer 2. However, it is more convenient to analyse this operation in the time domain. In this case, the output voltage of mixer 2 in the time domain is defined by:-

$$V_{out}(t) = V_1 V_2 \left\{\cos[\omega_1 t + \beta \sin(\omega_m t)]\cos[\omega_2 t + \beta \sin(\omega_m t)]\right\}. \tag{4.5}$$

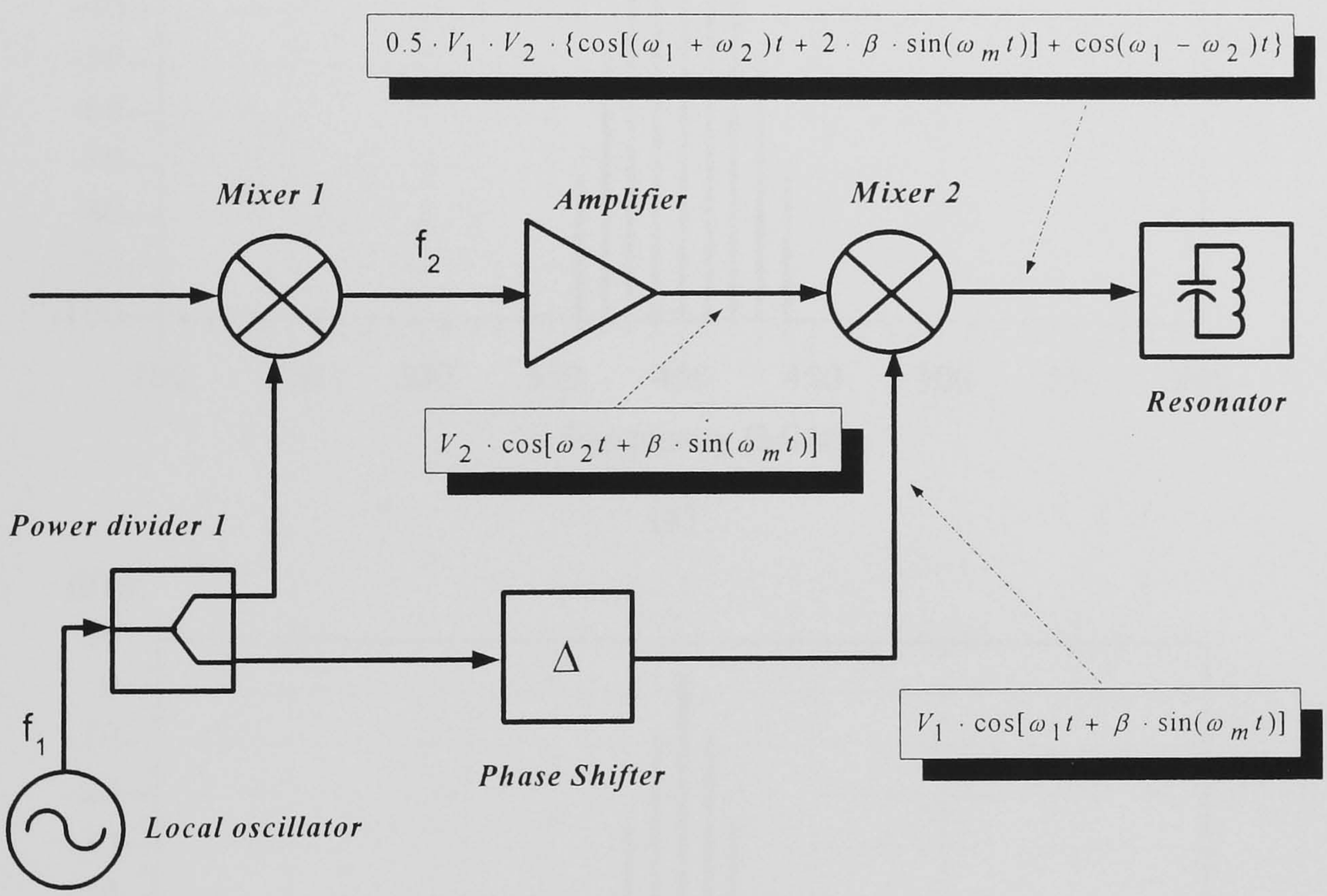


Figure 4.2 Sideband suppression in transposed-gain oscillator.

From the identity $cosAcosB = 0.5[cos(A+B) + cos(A-B)]$, equation (3.4) can be rewritten as:-

$$V_{out}(t) = 0.5V_1V_2\{\cos[(\omega_1 t + \beta\sin(\omega_m t)) + (\omega_2 t + \beta\sin(\omega_m t))] + \cos[(\omega_1 t + \beta\sin(\omega_m t)) - (\omega_2 t + \beta\sin(\omega_m t))]\}. \tag{4.6}$$

Equation (4.6) simplifies to:-

$$V_{out}(t) = 0.5V_1V_2\{\cos[(\omega_1+\omega_2)t + 2\beta\sin(\omega_m t)] + \cos(\omega_1-\omega_2)t\}. \quad (4.7)$$

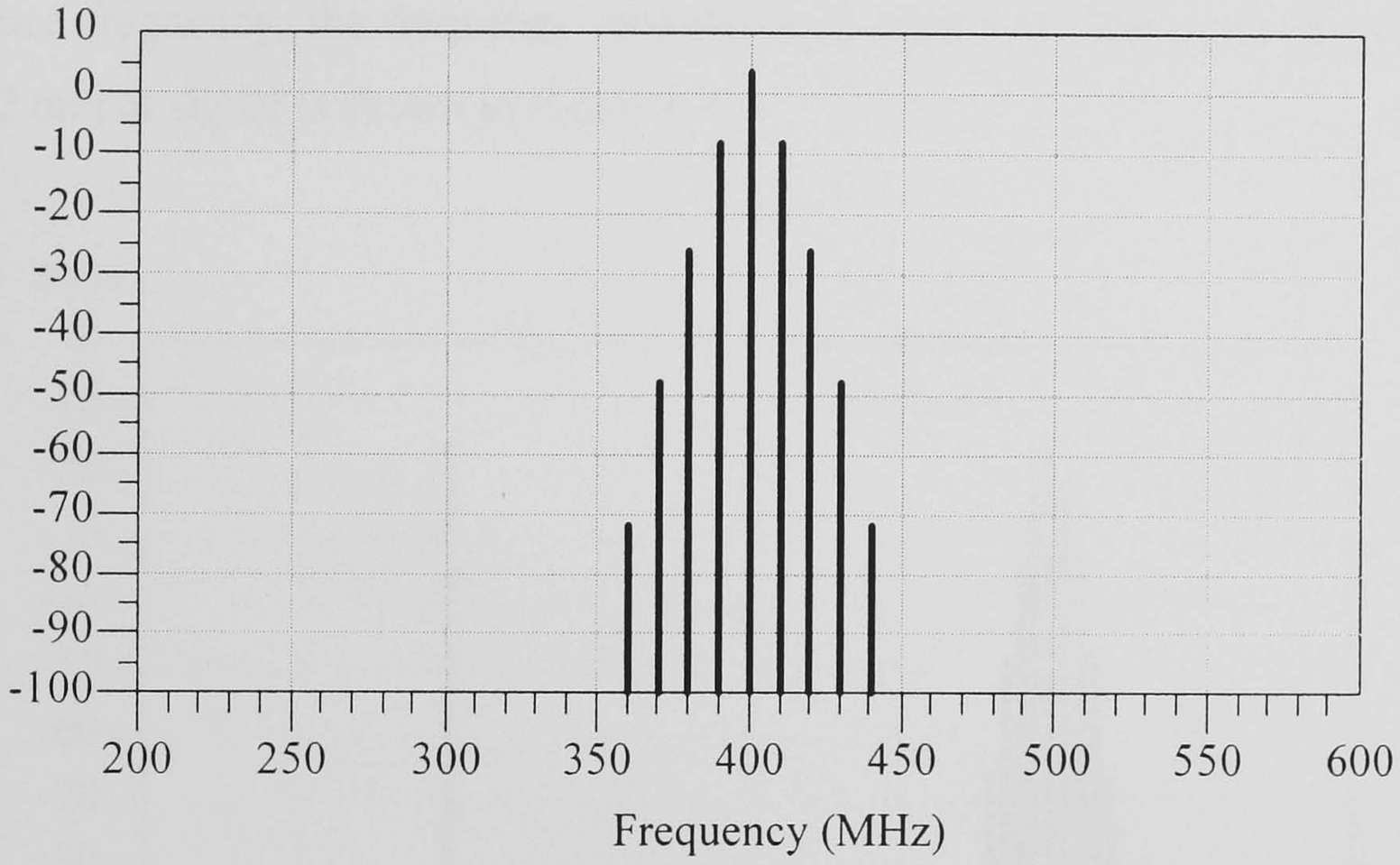


Figure 4.3 Power spectrum of f_1 (a) and f_2 signals (b).

Figure 4.3 (a) shows the power spectrum of an example LO signal and (b) the power spectrum of f_2 or the IF signal. The two carriers are 400 and 200MHz frequency modulation signals with a 10 MHz modulating frequency and a modulation index of 0.5 ($\beta = 0.5$).

The Fourier transform of equation (4.7) gives two signals. The first term, the sum frequency term, has a doubled modulation index. For the second term, the difference frequency, the frequency modulation is removed. The power spectrum of mixer 2 output signal is shown in Figure 4.4.

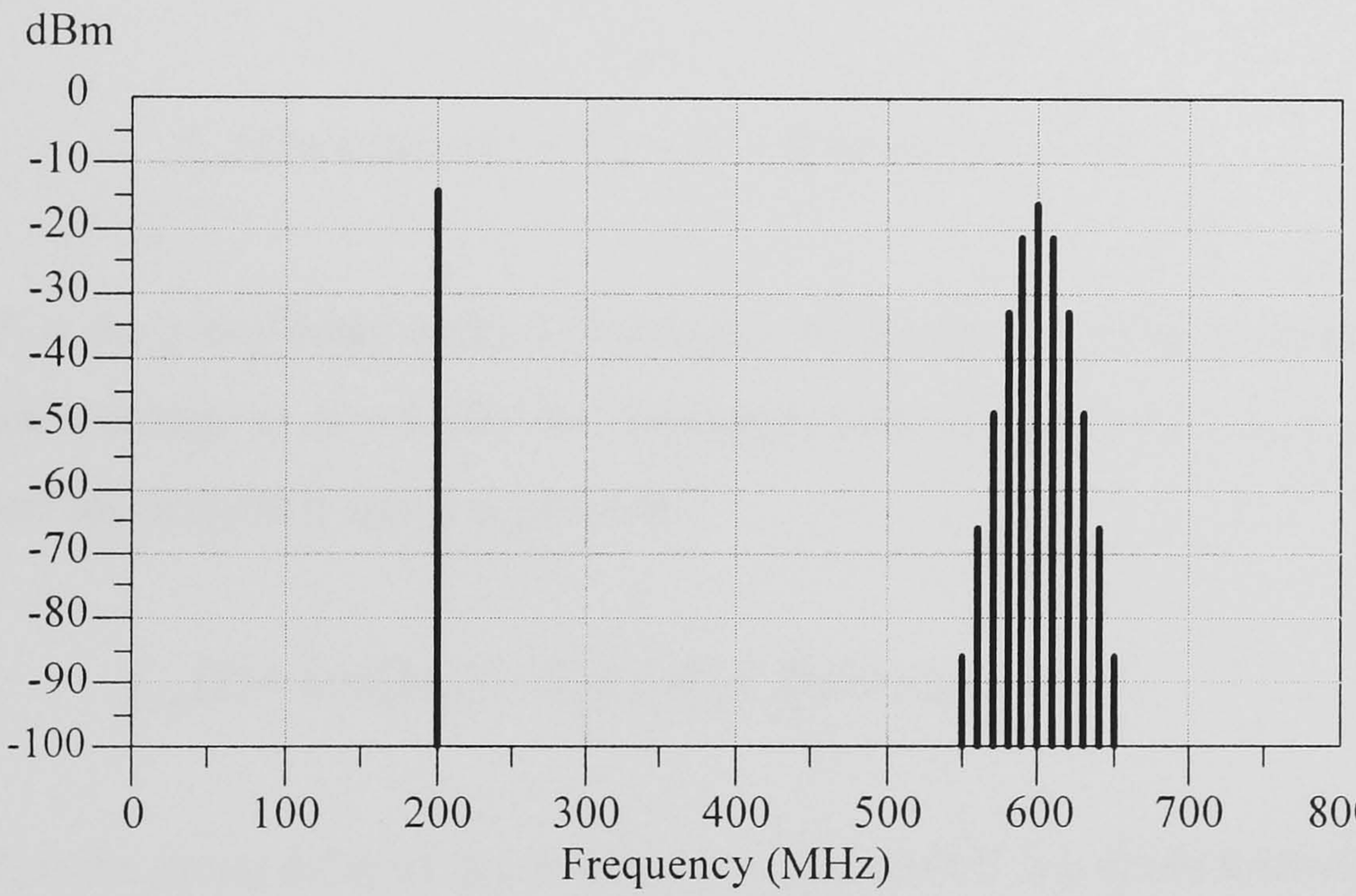


Figure 4.4 Output product of mixer 2.

In the transposed gain oscillator, the higher frequency term is suppressed to a certain degree by the band-pass characteristic of the resonator. Thus, from equation (4.7) the transposed gain oscillator can give high LO phase noise suppression. This sideband noise suppression performance is not directly related to resonator's Q.

4.3 Delay Effects

The path delays are found to play an important role in determining LO noise suppression, including which of the two output frequencies achieves noise cancellation. To analyze this, the signal paths are considered linear and both paths assumed to have a linear phase response given by [4.9]:-

$$\theta(\omega) = -T\omega - \theta_0 \tag{4.8}$$

where $-\theta_0$ is the phase at $\omega = 0$ and T is the constant group delay.

The spectrum of the LO signal in equation (4.1) is the carrier frequency and an infinite number of sidebands, each separated from the carrier by integer multiples of the modulating frequency ω_m. The signal path response to $f_1(t)$ is the superposition of these sidebands shifted by the function in equation (4.8). Then, the delayed f_1 signal can be written as [4.9]:-

$$f_{1d}(t) = \cos[\omega_1(t - T_1) - \theta_1 + \beta \sin \omega_m(t - T_1)] \tag{4.9}$$

where T_1 is the group delay of the LO path (power divider and delay equaliser) and θ_1 is a phase intercept at $\omega = 0$. The low frequency path also imposes a delay on the $f2$ signal and the delayed f_2 signal is given by:-

$$f_{2d}(t) = \cos[\omega_2(t - T_2) - \theta_2 + \beta \sin \omega_m(t - T_2)] \tag{4.10}$$

where T_2 is the group delay of the IF frequency path and θ_2 is a phase intercept.

Letting $V_1 = V_2 = 1$, substitution of (4.9) and (4.10) into (4.3) yields a delayed version of the mixer2 output signal, which is expressed as:-

$$\begin{aligned} & f_{12d}(t) \\ & = 0.5\{\cos[\omega_1[t - \tau_p(\omega_1)] + \omega_2[t - \tau_p(\omega_2)] + 2\beta[\sin \omega_m[t - (\tfrac{T_1+T_2}{2})]\cos \omega_m(\tfrac{T_2-T_1}{2})\} \\ & + \{\cos[\omega_1[t - \tau_p(\omega_1)] - \omega_2[t - \tau_p(\omega_2)] + 2\beta[\cos \omega_m[t - (\tfrac{T_1+T_2}{2})]\sin \omega_m(\tfrac{T_2-T_1}{2})\}\} \end{aligned} \tag{4.11}$$

where $\tau_p(\omega)$ is a phase delay defined by:-

$$\tau_p(\omega) = T + \frac{\theta_0}{\omega} \tag{4.12}$$

As can be seen, from (4.11), the lower sideband product no longer has totally suppressed sideband noise. The sideband reduction depends on the group delay time difference.

4.3.1 Sideband Suppression Factor

Assuming that the unwanted output product is attenuated by the resonator, the desired signal can be written as:-

$$f_o(t) = 0.5\cos[(\omega_{LSB}) + 2\beta\Delta\tau(\cos\omega_m t)] \tag{4.13}$$

where $\omega_{LSB} = \omega_1 - \omega_2$ and $\Delta\tau$ is a sideband suppression factor. We define this sideband suppression factor as:-

$$\Delta\tau = \sin\omega_m[\frac{(T_2 - T_1)}{2}] \tag{4.14}$$

If there is a delay mismatch between two signal paths, the LO phase noise will not be completely suppressed.

4.3.2 Carrier to Sideband Ratio

With unequal path delays, the carrier power to residual noise sideband power totally depends on the sideband suppression factor. To analyse the carrier to sideband power ratio, we approximate (4.13) as a narrow band modulation [4.10]:-

$$f_o(t) = 0.5\cos\omega_{LSB}t + 0.5\beta\Delta\tau\cos(\omega_{LSB} + \omega_m)t - 0.5\beta\Delta\tau\cos(\omega_{LSB} - \omega_m)t\ . \tag{4.15}$$

Equation (4.15) contains the voltage spectrum of 3 signals. Thus, the power ratio of carrier to one sideband is a ratio of a squared value of the carrier component coefficient and the squared value sideband coefficient. If the carrier to sideband ratio due to delay mismatch is evaluated by a single tone FM signal, the carrier to single sideband power can be defined as:-

$$\frac{C}{SB} = \frac{1}{(\beta\Delta\tau)^2}. \tag{4.16a}$$

Equation (4.16) can be expressed in term of a frequency deviation ($\Delta\omega$) and a modulating frequency (ω_m) as:-

$$\frac{C}{SB} = \frac{1}{(\frac{\Delta\omega}{\omega_m}\Delta\tau)^2}. \tag{4.16b}$$

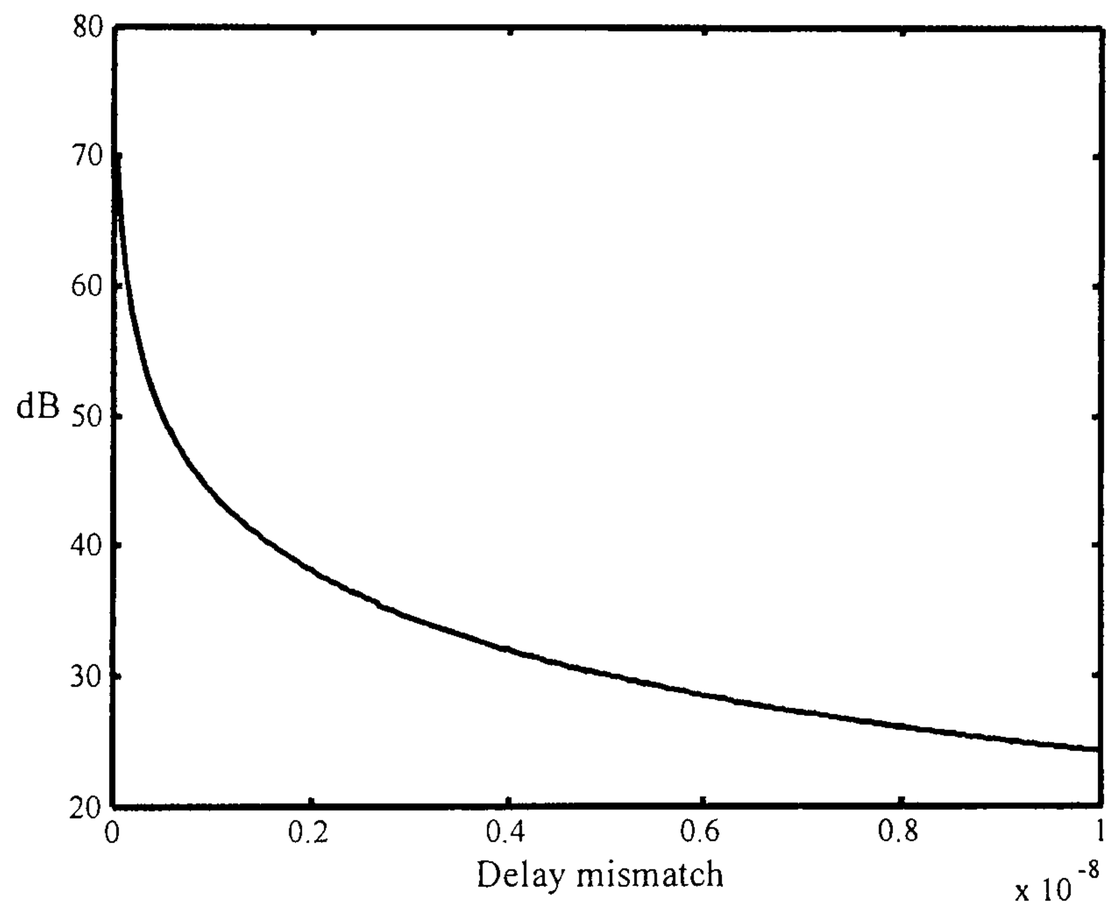


Figure 4.5 An example plot of carrier to single sideband ratio versus delay mismatch.

As an example, if there is a 2 ns delay mismatch between the two signal paths, calculation using equation (4.16) yields C/SB = 6335.82 or 38.02 dB. The effect of group delay mismatch on the sideband noise suppression is shown in Figure 4.5 (for f_m = 10MHz, β=0.2). However, LO path delay also determines the phase response of the TGA (section 3.4) the LO sideband noise suppression follows equation (4.16) at zero-phase frequencies.

4.3.3 Upper Sideband Output

One of the features of the double frequency conversion oscillator is its ability to give a clean upper sideband output signal. This has been pointed out in section 4.1. This allows the oscillator to give a higher output frequency than its pumped LO. From the previous sections, the analysis doesn't show how the sideband noise of the upper sideband output can be suppressed.

Considering (4.10), if we set up a specific condition as:-

$$-\beta \sin \omega_m t = \beta \sin \omega_m (t - T_U)$$

then solving for T_U yields:-

$$T_U = \frac{T_m}{2} \tag{4.17}$$

where $T_m = 1/f_m$ and f_m is the modulating frequency.

Substitution of equation (4.2) with T_U added into equation (4.7) results in the expression:-

$$\begin{aligned} f_o(t) &= 0.5\{\cos[\omega_1 t + \beta \sin \omega_m t]\cos[\omega_2 t - \beta \sin \omega_m t]\} \\ &= 0.5\{\cos(\omega_1 + \omega_2)t + \cos[(\omega_1 - \omega_2)t + 2\beta \sin \omega_m t]\}. \end{aligned} \tag{4.18}$$

As can be seen, the modulating signal is now suppressed at the upper sideband frequency. However, if the f_2 path delay deviates from the optimum value, T_U, the modulating signal cannot be fully suppressed at the upper sideband output. In this case, equation (4.16) still gives the carrier to sideband noise ratio provided that the offset delay, T_U, is included. Thus, we have to modify the sideband suppression factor as follows:-

$$\Delta\tau = \sin \omega_m [\frac{(T_U + T_2) - T_1}{2}] \tag{4.19}$$

In practical cases, T_U is determined by the LO phase noise distribution in the $1/f$ region of the noise sidebands. Normally, the upconverted phase noise corner frequency can be approximated from the local oscillator noise characteristics, since $1/f^n$ low frequency noise in active devices appears in the phase noise spectrum as $1/f^{n+2}$ regions [4.7]. Thus, the optimum offset delay time is high compared to a typical RF amplifier's group delay, meaning that a delay equaliser may be needed. This equaliser must not change the LO phase noise distribution in order to reduce the sideband noise correctly.

4.4 Oscillator Design and Simulations

Normally, all sine-wave oscillators must, as a minimum, contain a) an active device with enough power gain at the operating frequency to supply not only output signal but also its own driving signal, b) a frequency-determining network and c) an amplitude-limiting and stabilisation mechanism [4.7], [4.10]. The block diagram in Figure 4.1 shows all these requirements even though an IF amplifier may give no power gain at the operating frequency and the amplitude limiting mechanism is determined by mixer 2.

Since there are at least two non-harmonic related frequencies in the feedback loop, the detailed design strategy is different compared to conventional feedback or transmission oscillators. However, if a transposed-gain amplifier is considered as a conventional amplifier, the feedback amplifier block diagram shown in Figure 4.6 is also a good starting point. This feedback system consists of a gain block G and a frequency selective element with a linear transfer function $H(j\omega)$. The transfer function for this linear system is:-

$$\frac{V_{out}(j\omega)}{V_i(j\omega)} = \frac{GH(j\omega)}{1-GH(j\omega)} \tag{4.20}$$

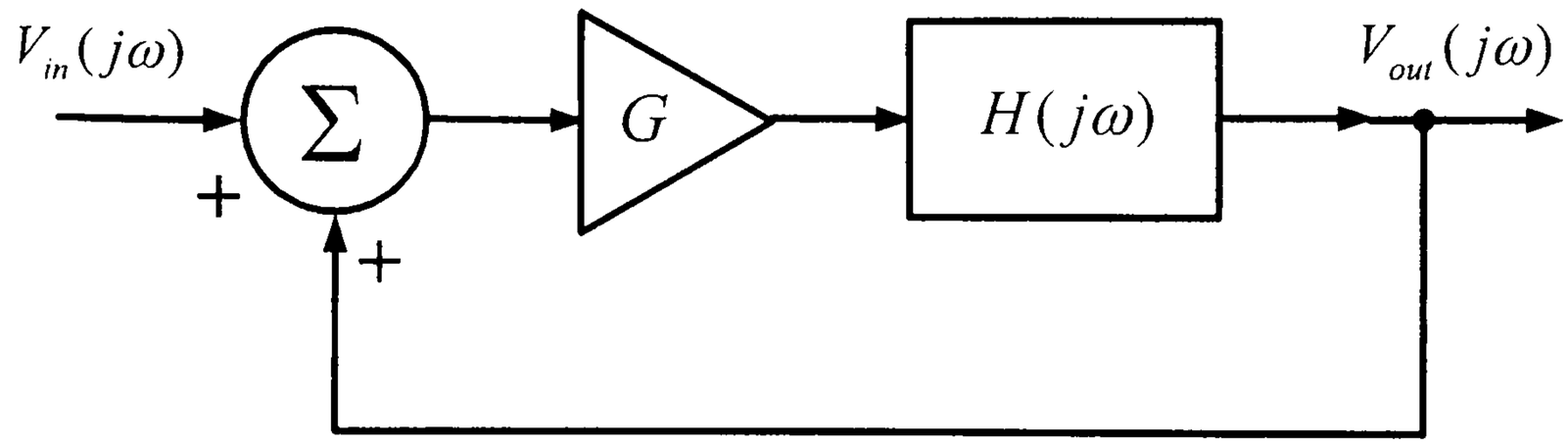


Figure 4.6 A feedback amplifier block diagram.

where V_{in} is the input voltage and V_{out} is the output voltage. The only way that the feedback system of Figure 4.6 can have non-zero output without any input excitation is for the denominator of equation (4.20) to be zero, that is:-

$$GH(j\omega) = 1 \tag{4.21}$$

Equation (4.21) is a necessary condition for stable oscillations. This condition is sometimes referred to as the Barkhausen criterion [4.10].

In the transposed gain oscillator the gain block is a transposed gain amplifier, TGA, which consists of an RF amplifier and two mixers as shown in Figure 4.1. The characteristics of the TGA are nonlinear in its nature since it gives two output signals, one of these has a different frequency from V_i. However, the unwanted sideband is filtered out by a bandpass characteristic of $H(j\omega)$. Thus, it is clear that the output spectrum is dominated by the fundamental component of input signal, $V_i(j\omega)$.

4.4.1 Design Example

From the block diagram of the TGA, one can use frequency domain simulations to find the large signal S-parameters and a relationship between input voltage (or current) and output voltage (or current) at a certain drive signal level at the needed frequency. The large signal S-parameter of the circuit, when the device model is well characterised, gives also a good starting point. At the zero phase frequency of S_{21}, the transposed gain oscillator can be made. The TGA has a very low S_{12}, thus the resonator as an external feedback network solely determines the oscillation frequency. To investigate the effects of the path delay mismatch and sideband suppression, the

behavioural model is employed. Figure 4.7 shows behavioural model of an amplifier and mixers TGA used for TGO sustaining amplifier.

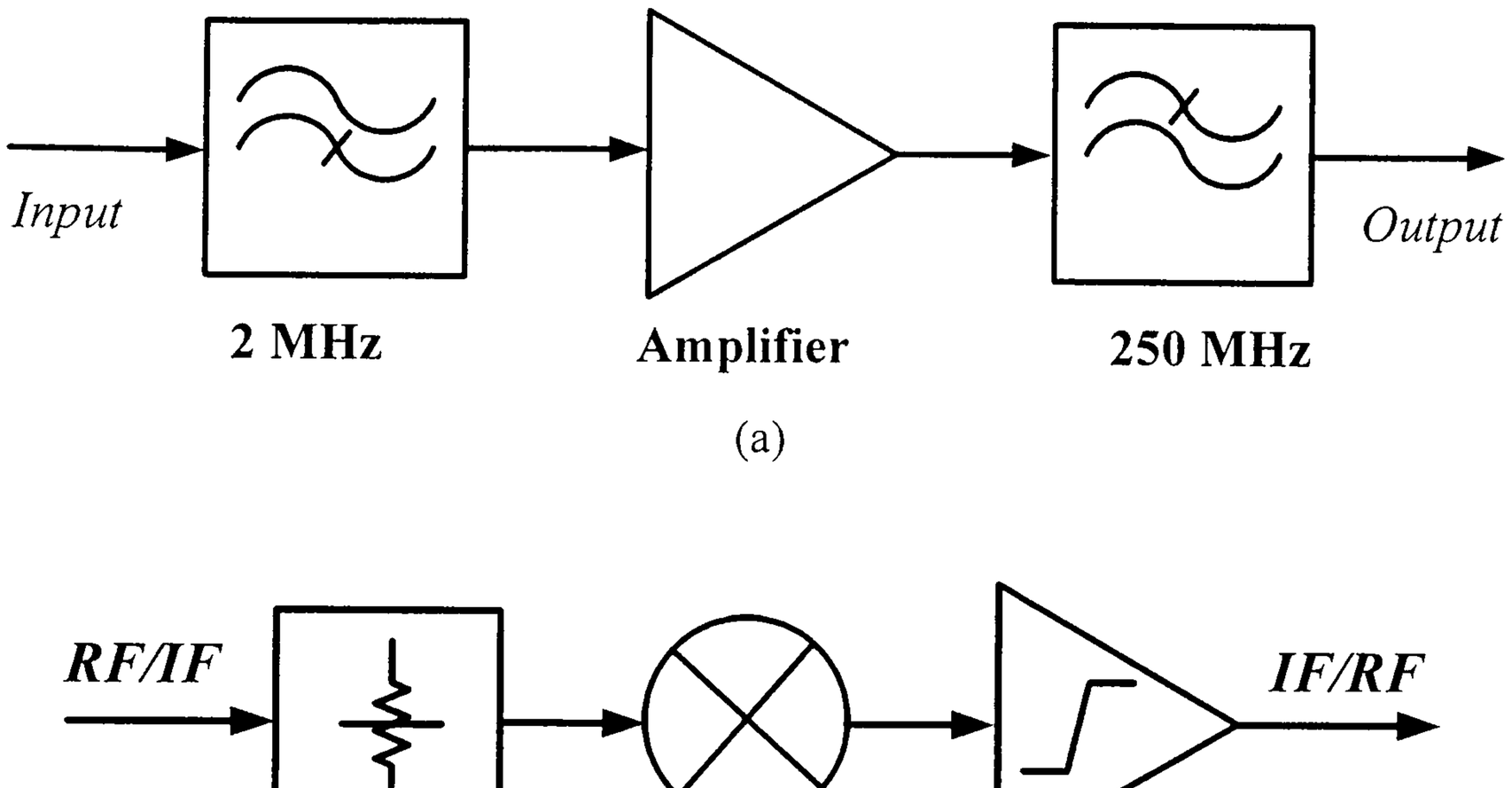


Figure 4.7 (a) IF amplifier and (b) mixer model.

The amplifier model has a transfer characteristic as shown in figure 3.2. The TGA is band limited by both filters. This same amplifier model is utilized in the mixer model to simulate the limiting effect of the balanced mixer. The multiplying operation and the attenuator determine the conversion loss of the mixer.

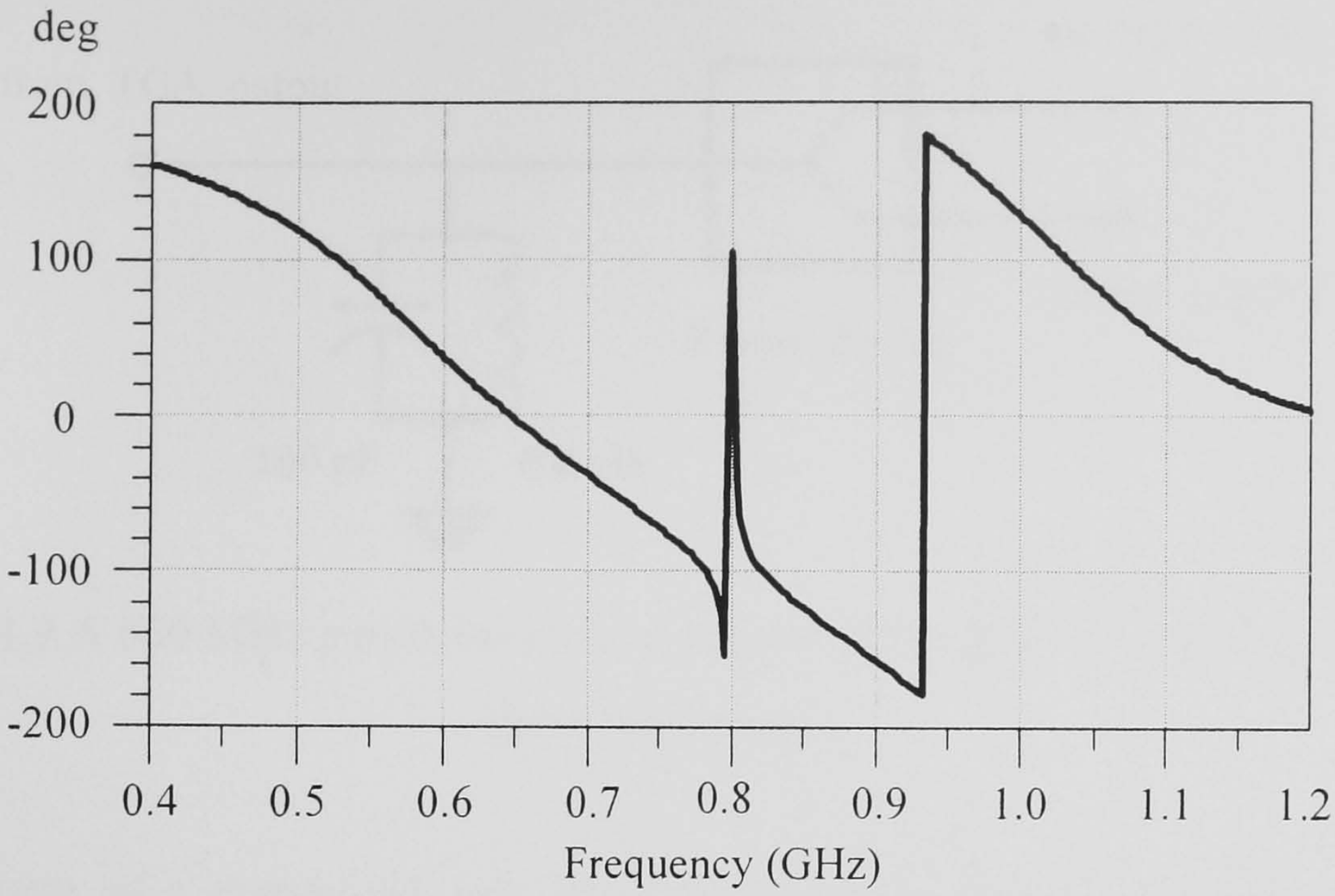


Figure 4.8 Phase response of an example TGA.

Figure 4.8 shows phase response of the TGA using mixer and amplifier model in Figure 4.7. The response has a zero phase at around 650 MHz, thus a simple parallel resonator in the feedback path should make the TGA oscillate. After the TGA zero phase frequency is properly determined, the designing procedure can start from equation (4.21). The TGO design problem facing us is how much loop-gain and additional phase shift are needed if the zero phase frequency is not the same as a desired frequency since resonant circuits give zero phase at a resonance frequency. Then, the rest of the design is a synthesis of resonator and output coupling network which all phase shift due to interconnection is included, $H(j\omega_o)$.

4.4.2 Simulations

Even though traditional SPICE transient simulation is a time and memory consuming method, time domain simulation is the necessary tool for studying the transient behaviour of oscillator circuits. For transient circuit simulations, the needed additional phase shift is obtained by the time delay elements because the conventional phase shifter doesn't work at certain phase angles, i.e.90°, due to the noncausal problem. The required feedback network, $H(j\omega_o)$, which is implemented by a parallel resonator with loaded Q of 10 at 650 MHz and a 3-dB power divider is shown in Figure 4.9.

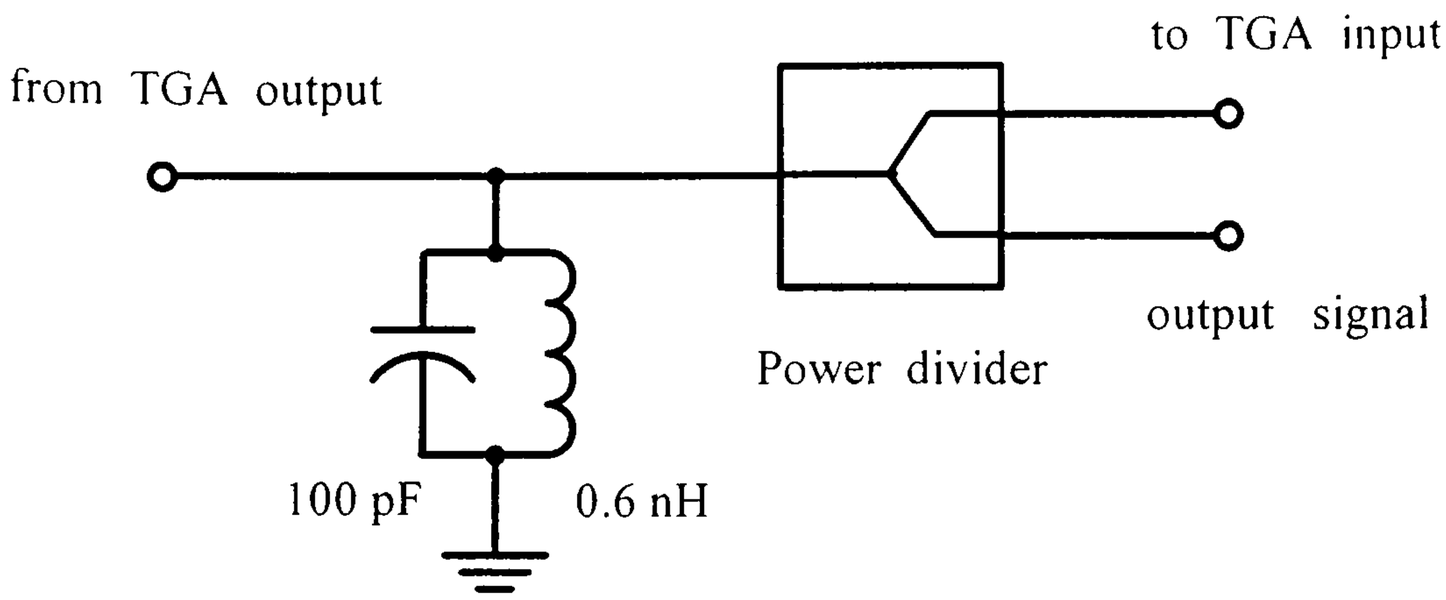


Figure 4.9 A 650 MHz parallel resonator and two ways power divider as an output-coupling network.

An example of a transposed gain oscillator circuit is shown in Figure 4.10. The oscillator comprises a 250MHz single-side bandwidth transposed gain amplifier, a 650 MHz resonator and 800 MHz local oscillator. A delay compensation network of 2.3 ns is applied to the feedforward path to compensate for the group delay of the RF amplifier.

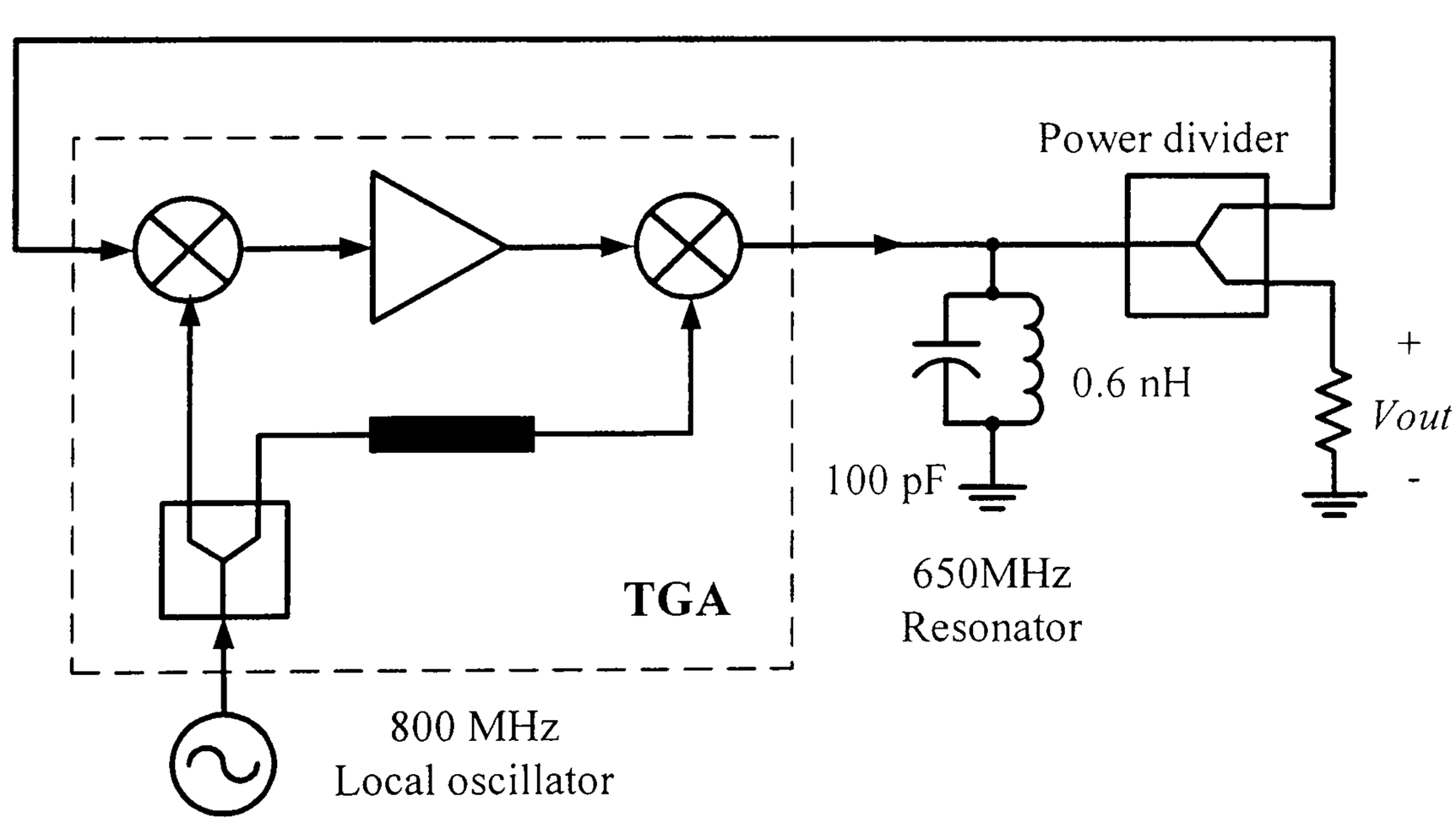


Figure 4.10 Example circuit of 650 MHz transposed gain oscillator.

In order to use transient simulation efficiently and get the correct simulation results, one must know the limitation of time domain simulations and know how to set up the simulation parameters properly [4.11-4.12]. The oscillation of the close-loop system

in Figure 4.10 is started by a pwl (piecewise linear) current source. Using Kaiser's window for the FFT operation, the simulation results of the example circuit using ADS transient simulation when the LO is modulated by a 10 MHz signal and $\beta = 0.5$, are shown in Figure 4.11 and Figure 4.12. There is an IF-LO delay mismatch in this TGO simulation. As can be seen, the output signal has considerable LO sideband suppression.

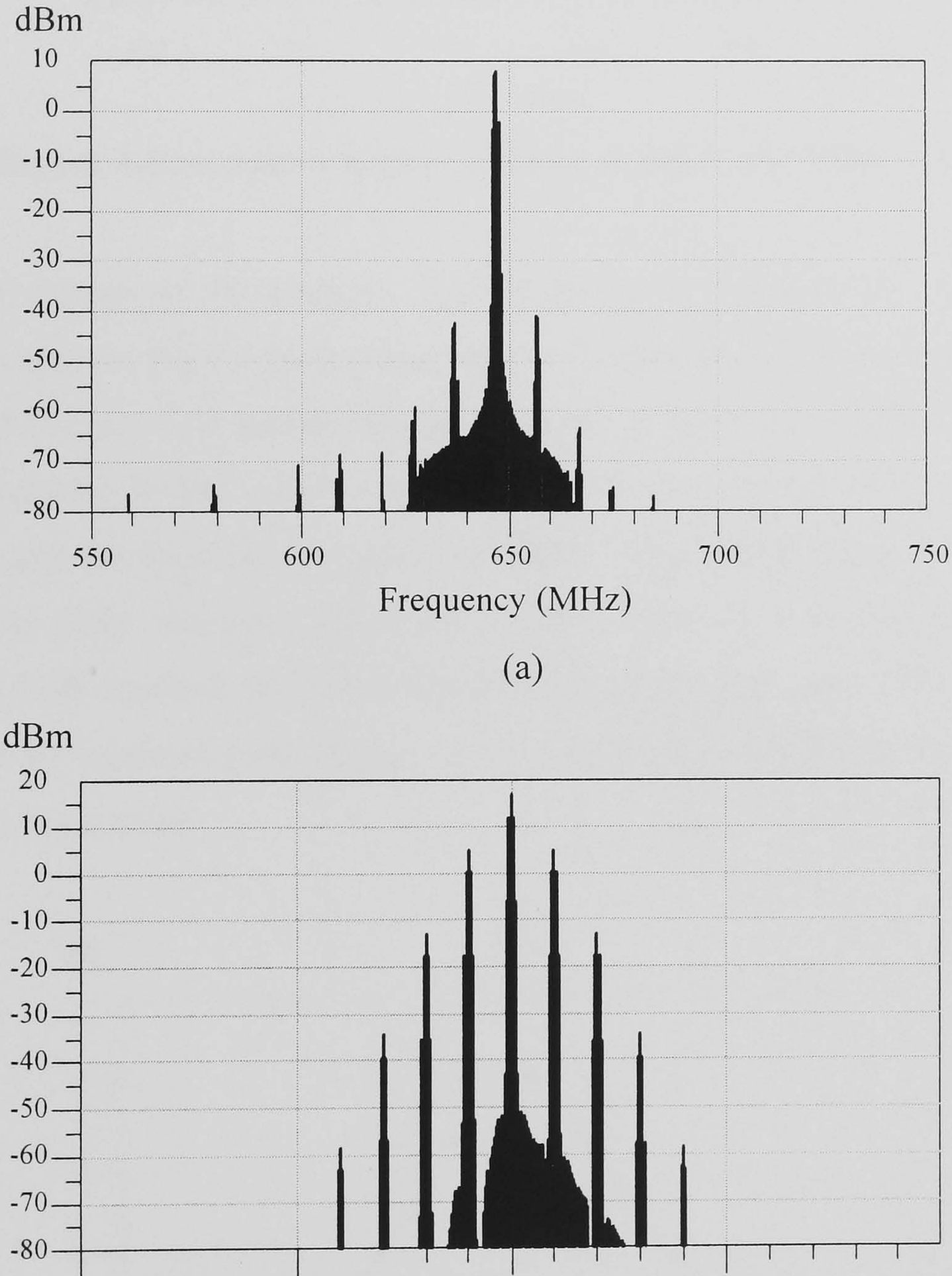


Figure 4.11 (a) Output power spectrum of TGO compare to (b) the LO power spectrum.

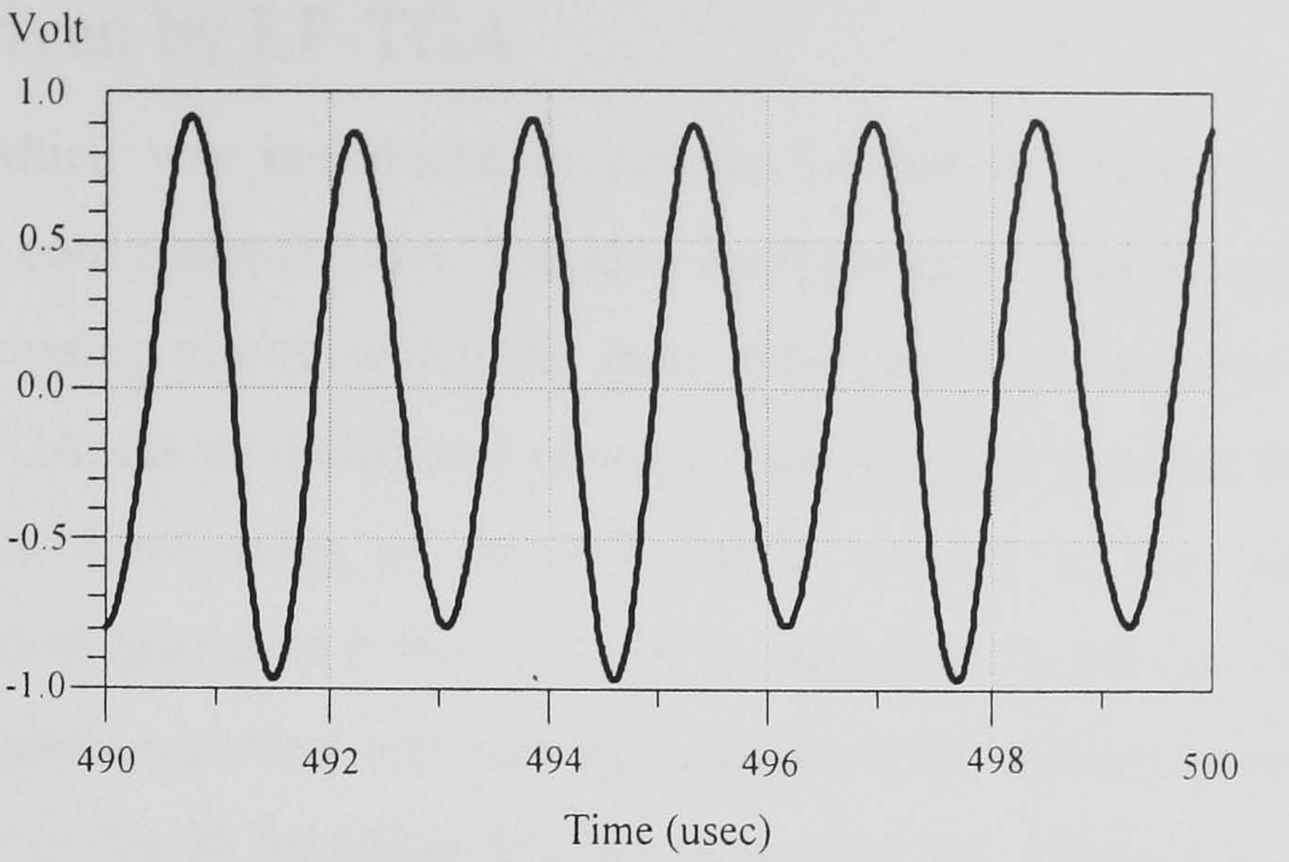


Figure 4.12 Output voltage of a design example 650 MHz TGO.

The output voltage of the example TGO is shown in Figure 4.12. There is some amplitude variation due to the residual upper sideband signal. From Figure 4.11 (a) and (b), the LO sideband suppression performance of the TGA depends on the delay mismatch between IF and LO path as observed in the section 4.3. The resonator has a very small attenuation at the first pair of sideband frequencies. Figure 4.13 shows the insertion loss of the resonator. At the first sideband frequency, the sideband power is less than 0.4 dB changed due to the insertion loss of the resonator. Thus, the transfer function of the feedback path, $H(j\omega_o)$, is not directly responsible for the reduction of the LO side band noise.

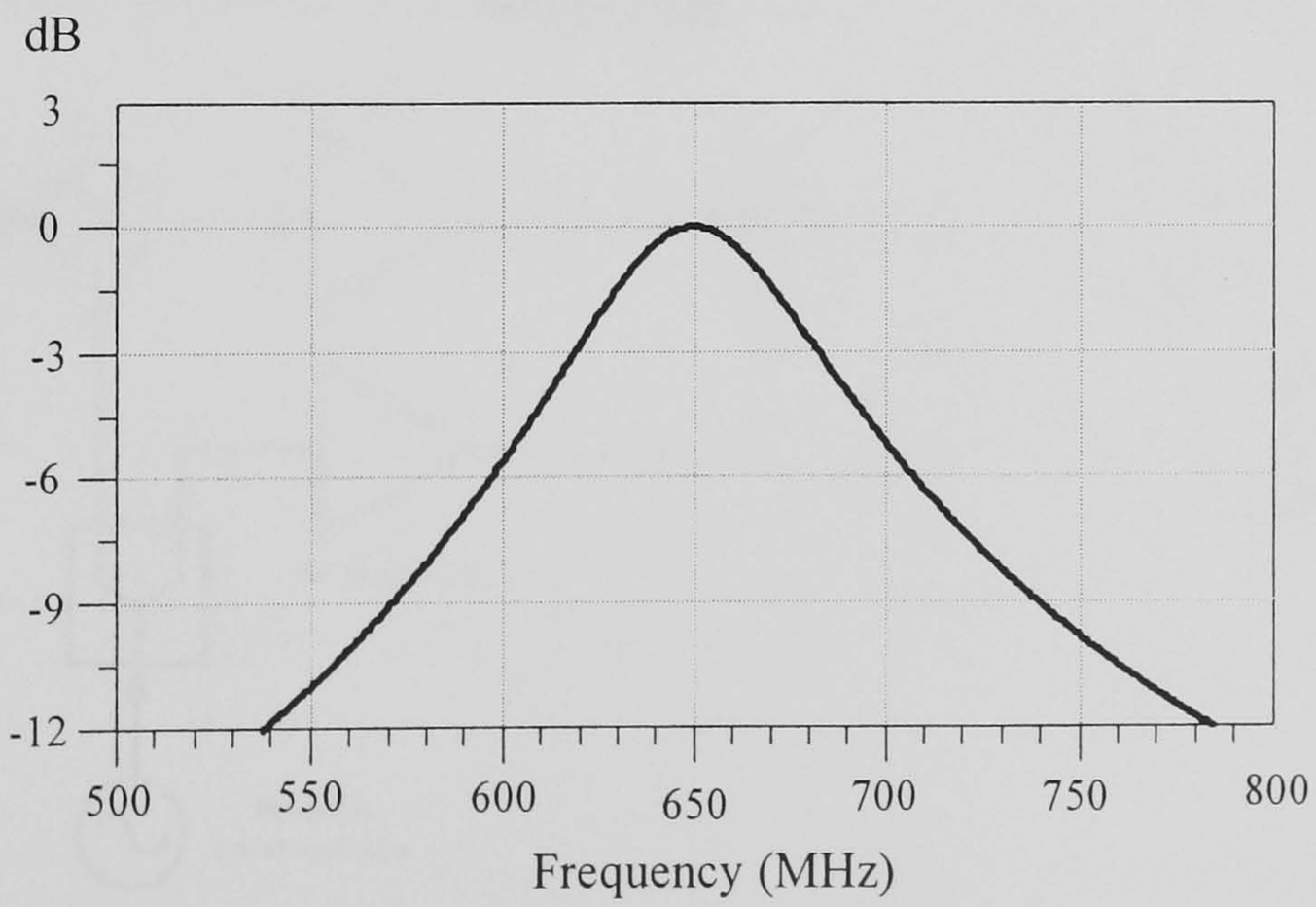


Figure 4.13 Insertion loss of the feedback path.

4.5 TGO Driven by LP-TGA

The LP-TGA which was introduced in section 3.4 has no delay mismatch effect compared to the conventional TGA. The new configuration of TGA can be employed as a signal processing circuit which the main function is to suppress LO sideband noise. The LP-TGA has no distributed element therefore it is possible to design as an integrated circuit. Convolving of the LO and IF signals in the transposed gain oscillator is an ideal operation if the LP-TGA is employed. In the conventional TGA, it is not easy to obtain a perfect match at all times when the different devices are used. Aging behaviour of the IF amplifier and the delay line are different in nature. In the practical cases, a variable phase shifter is needed to work with the fixed line. Because of the linear phase response of the LP-TGA, as shown in Figure 3.29, a phase shifter or delay equaliser also needed. This phase shifter is in the feedback path, it is used for adjusting the phase of the output signal to make the TGO oscillate. Figure 4.14 shows the block diagram of the LP-TGA driven transposed gain oscillator under investigation. Both RF amplifiers in the block diagram have the same characteristic and are supposed to have the same aging. The output voltage of the mixer 2 is described by equation (4.7). Thus, there is no LO induced sideband in the output signal. However, if the amplifiers operate at different power levels the group delay is not the same value.

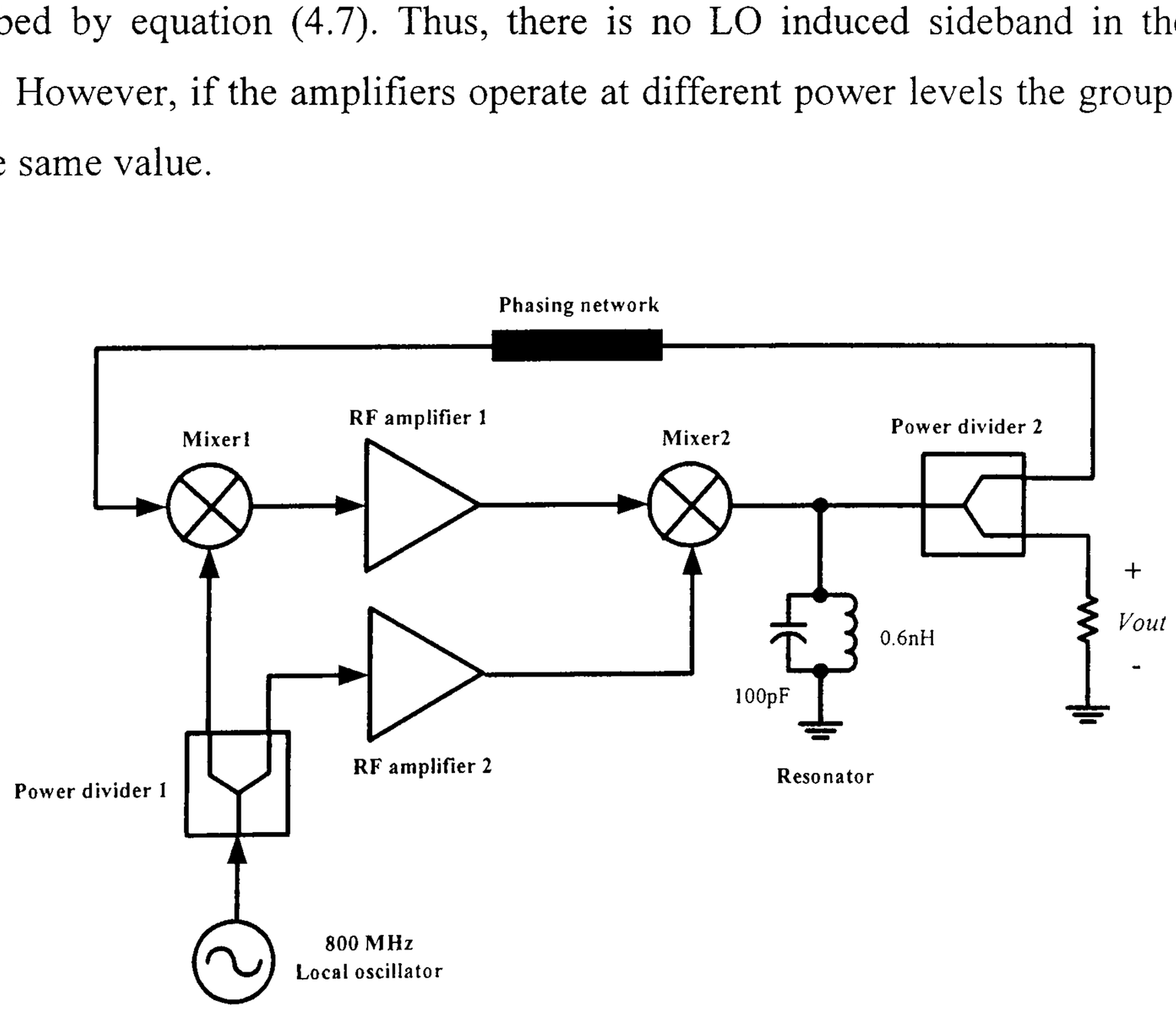


Figure 4.14 LP-TGA driven transposed gain oscillator.

The oscillator is driven by an 800 MHz FM LO signal, the LO signal is modulated by a 10 MHz signal and $\beta = 0.5$ as shown in Figure 4.11. Figure 4.15 shows the simulated output signal of the LP-TGA driven transposed gain oscillator in the frequency domain. The LO sideband is suppressed to the level of numerical noise from the FFT operation. Figure 4.16 shows the wideband output frequencies from the LP-TGA driven transposed gain oscillator. The LP-TGA driven TGO gives many spurious frequencies due to intermodulation products.

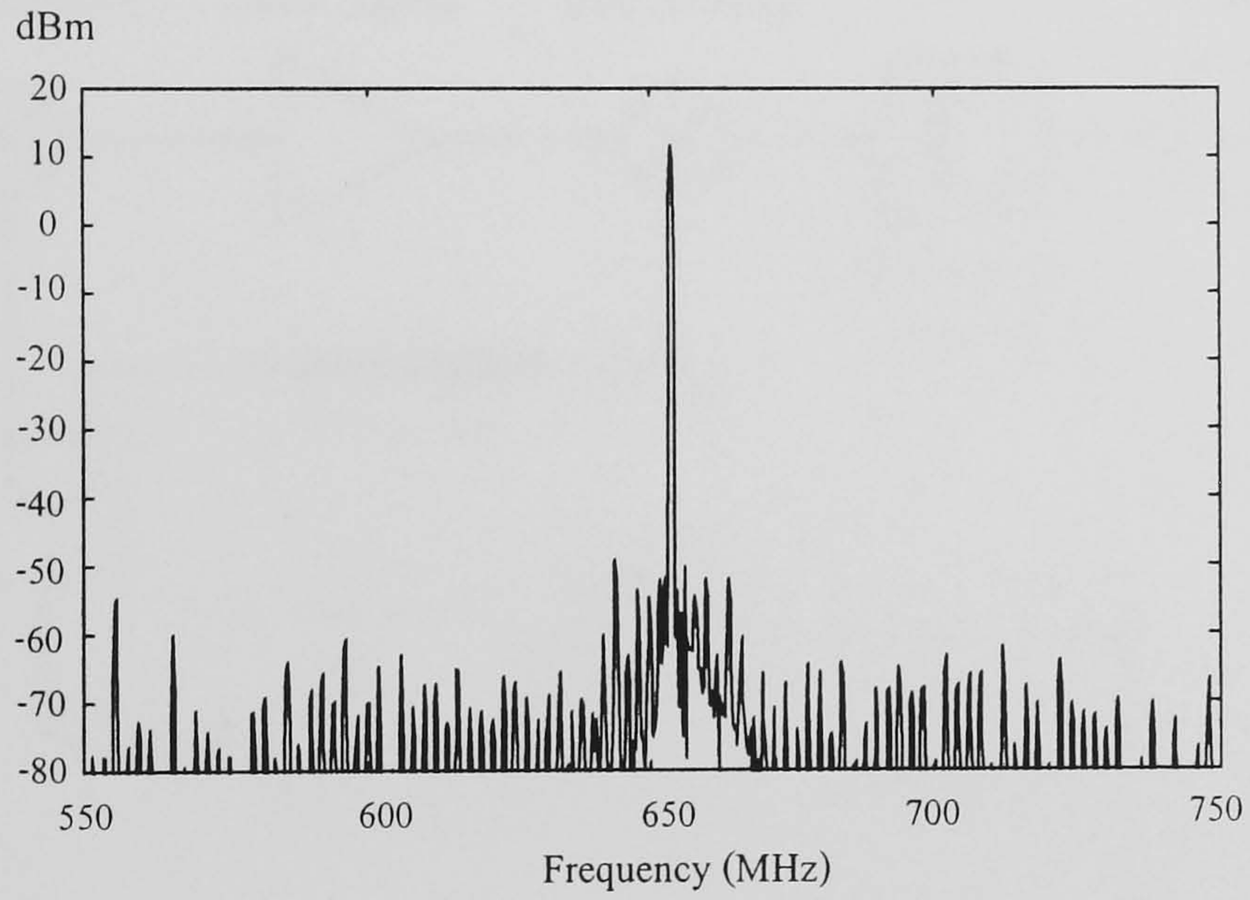


Figure 4.15 Output power spectrum of the LP-TGA driven transposed gain oscillator with the same LO as shown in Figure 4.11 (b).

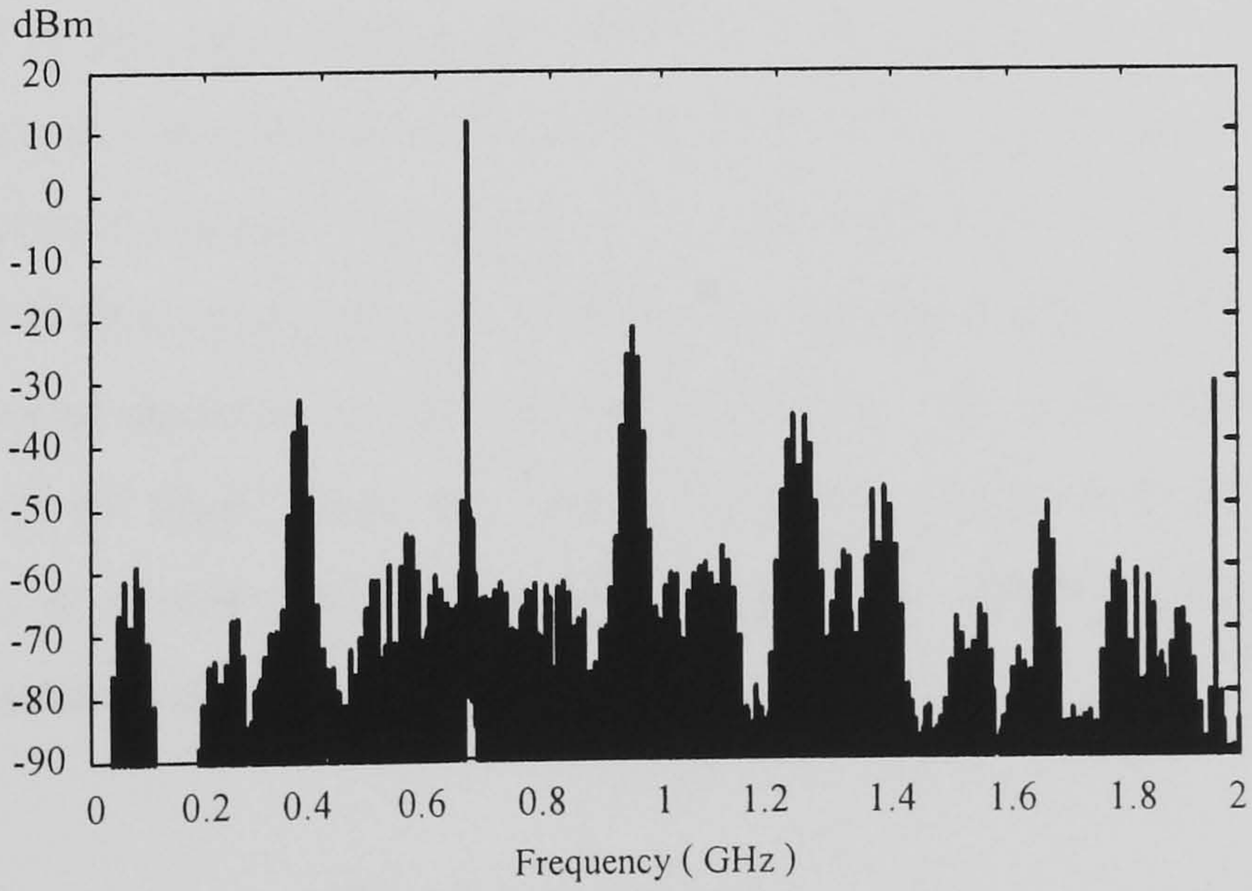


Figure 4.16 Wideband output power spectrum of the LP-TGA driven transposed gain oscillator.

4.6 Voltage Controlled Transposed Gain Oscillator Experiment

Figure 4.17 shows the set up block diagram for a 670 MHz voltage controlled transposed gain oscillator experiment. The local oscillator signal comes from an Agilent E4422B RF signal generator. The LO signal is frequency modulated by a 1 MHz tone with a modulation index of 0.25.

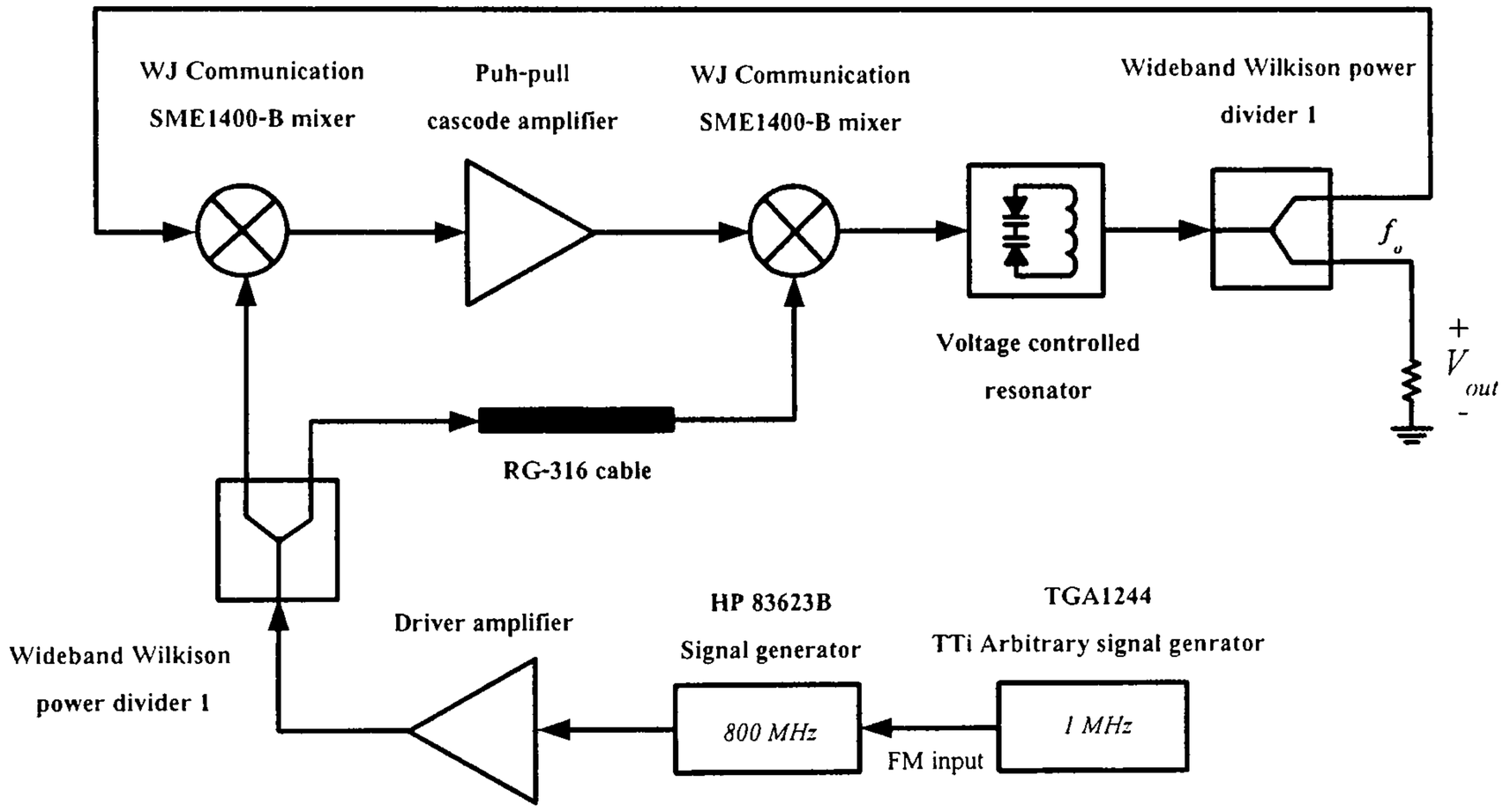


Figure 4.17 670 MHz transposed gain oscillator experiment set up.

4.6.1 Voltage Controlled Resonator

The resonator in the transposed gain oscillator experiments is a voltage-controlled capacitive matching parallel resonant circuit. The tuning elements are two varactor diodes with the back-to-back connection for low distortion operation [4.13-4.14]. The ratio of loaded to unloaded Q, Q_L/Q_0, is set to the optimum value [4.15]. The unloaded Q of the resonator depends on the varactor diode loss. The equivalent circuit of the diode is shown in Figure 4.18 (a), where Ls is the anode and cathode terminal inductance, r_s is a series resistance and CD_{eff} is the effective capacitance. The effective capacitance is defined by:-

$$CD_{eff} = \frac{1}{(jXC_T\omega_0)} \tag{4.22}$$

where XC_T is a total reactance of the two diodes and its parasitic inductive reactance.

This reactance is given by:-

$$XC_T = \frac{1}{(j\omega_0 \frac{CD}{2})} + j\omega_0 2Ls \tag{4.23}$$

where CD is the diode capacitance and L_s is lead inductance. The series effective capacitance is converted into the parallel equivalent form to calculate the input-output matching capacitors.

The unloaded Q of the diodes can be express as:-

$$QD_0 = \frac{XC_T}{2r_S}. \tag{4.24}$$

Figure 4.18 (c) shows the parallel equivalent circuit of the two diodes where the circuit parameters are:-

$$RD_{pe} = 2r_S(1+QD_0^2) \tag{4.25}$$

and

$$CD_{pe} = CD_{eff}\left(\frac{QD_0^2}{QD_0^2+1}\right). \tag{4.26}$$

The input matching capacitors convert the series source resistance, R_G, into parallel impedance, which has real part equal to $2RD_{pe}$.

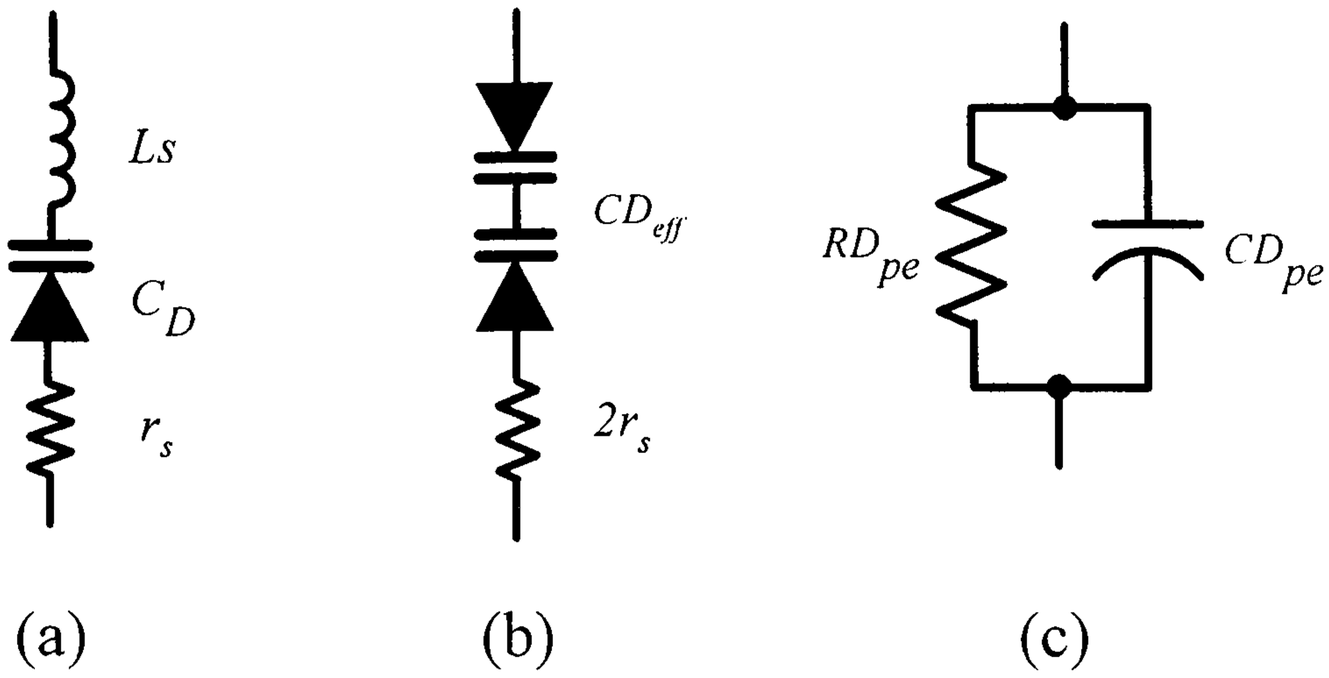


Figure 4.18 (a) A varactor diode and parasitic elements, (b) the equivalent circuit of the back-to-back connection and (c) parallel equivalent of (b).

The input matching capacitor is given by:-

$$C_{si} = \frac{1}{(R_G Q_{si} \omega_0)} \tag{4.27}$$

where R_G is a source resistance and Q_{si} is defined by

$$Q_{si} = \sqrt{\left(\frac{2RD_{pe}}{R_G}\right) - 1}\ . \tag{4.28}$$

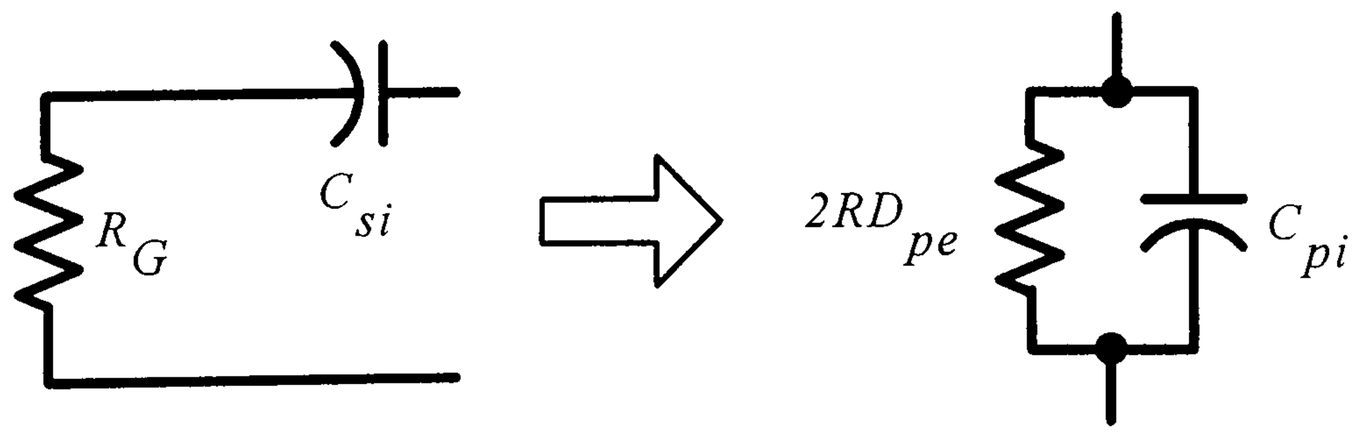


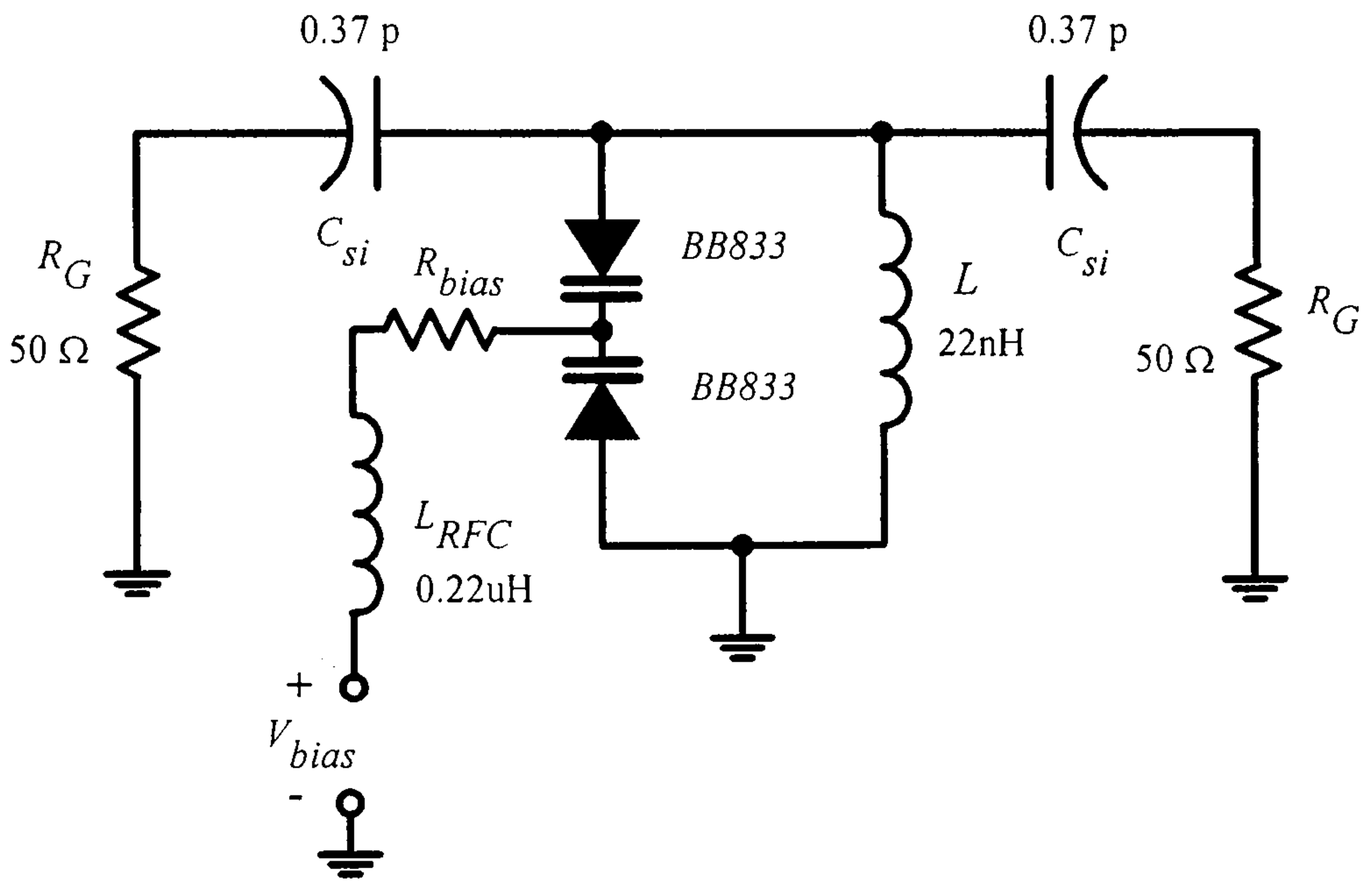
Figure 4.19 Series to parallel impedance transformation of the input matching capacitor.

The equivalent parallel capacitor, C_{pi}, is given by:-

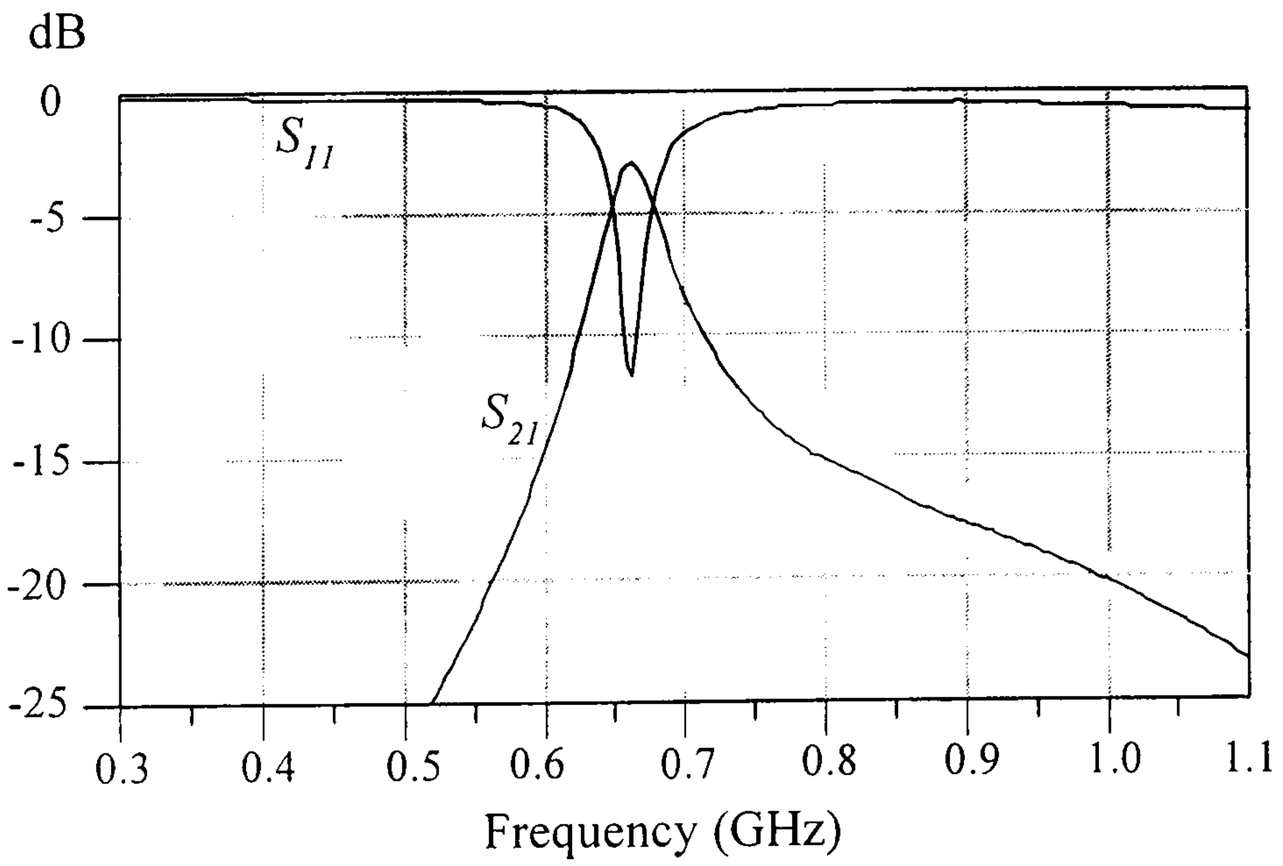
$$C_{pi} = C_{si} \frac{Q_{si}^2}{(Q_{si}^2 + 1)}. \tag{4.29}$$

Finally, the inductor is calculated by:-

$$L = \frac{1}{\omega_0^2 (CD_{pe} + 2C_{pi})}. \tag{4.30}$$



(a)



(b)

Figure 4.20 A 670 MHz voltage controlled resonator (a) and measurement results when the DC bias voltage is 4.5 volt (b).

The input matching capacitors convert the series source resistance, R_G, into parallel impedance, which has a real part of $2RD_{pe}$. Figure 4.19 shows series to parallel transformation of the input (and output) matching capacitor. The schematic of a 670 MHz voltage controlled resonator is shown in Figure 4.20(a). Figure 4.20(b) shows the measurement results of the voltage controlled resonator.

The varactor bias resistor generates thermal noise voltage, this noise voltage in one Hz bandwidth is calculated by:-

$$V_n = \sqrt{4kTR} \tag{4.31}$$

where $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, T is temperature and $R = R_{bias}$.

For a high sensitivity voltage controlled oscillator the maximum resistor value is given by [4.16]:-

$$R_{\max} = \left[\frac{S_\phi(f)}{kT}\right] \cdot \left[\frac{f_m}{K_o}\right]^2 \tag{4.32}$$

where $S_\phi(f)$ is the noise sideband power in one Hz bandwidth at a frequency f_m spaced from carrier, divided by carrier power and K_o is a tuning sensitivity (Hz/V) of the voltage controlled oscillators.

4.6.2 Experimental results

The fabricated 670 MHz voltage controlled oscillator is shown in Figure 4.21. The resonator comprises a back-to-back connection of BB833 varactor diodes and 22nH CoilCraft air-core inductor. The loaded Q of the resonator is around 15. A Phase shifter is included in the feedback path to set a zero-phase at oscillation frequency. In the feedfoward path, the delay mismatch is set to 16 ns by a PTFE transmission line.

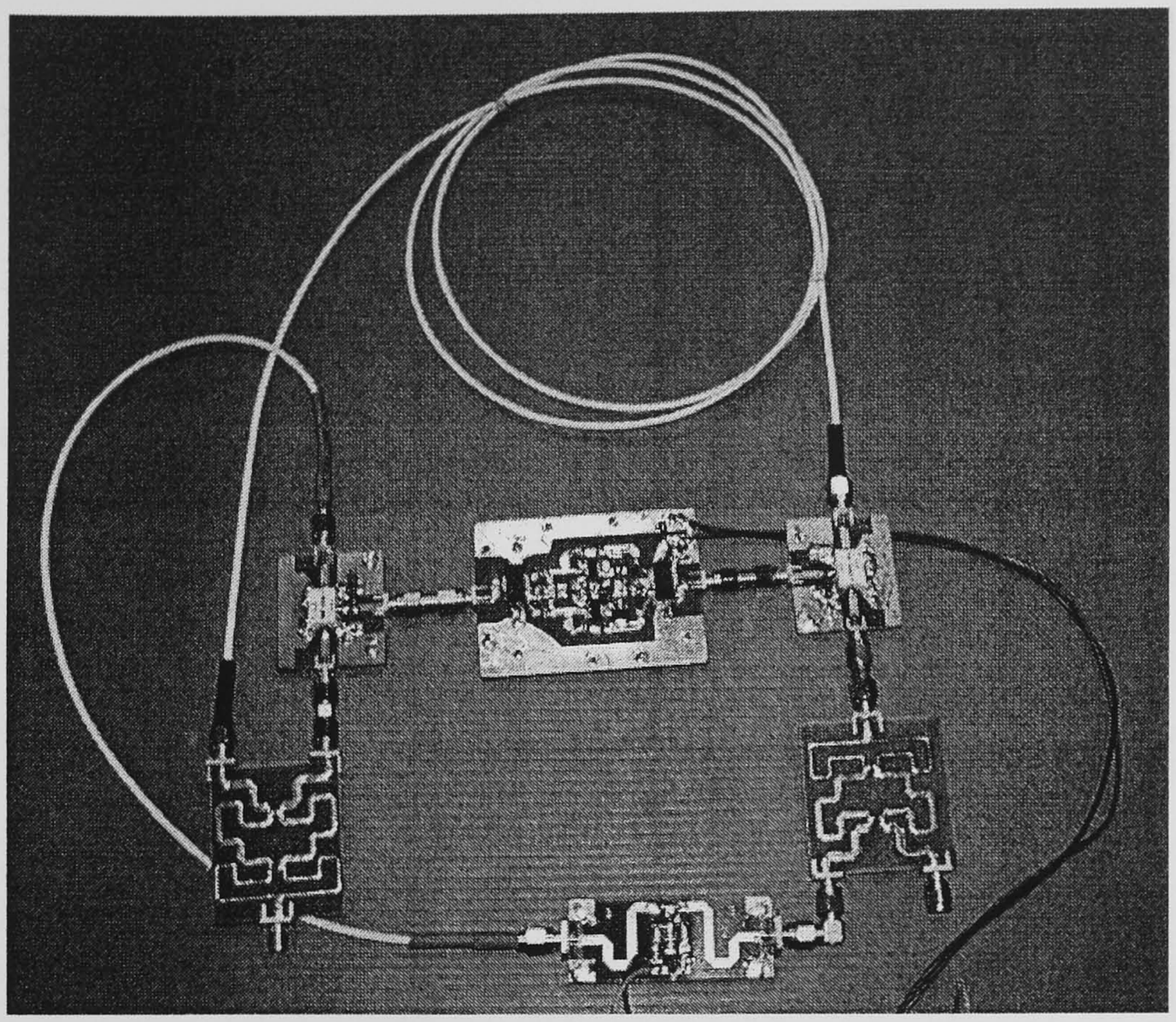


Figure 4.21 670 MHz transposed gain oscillator.

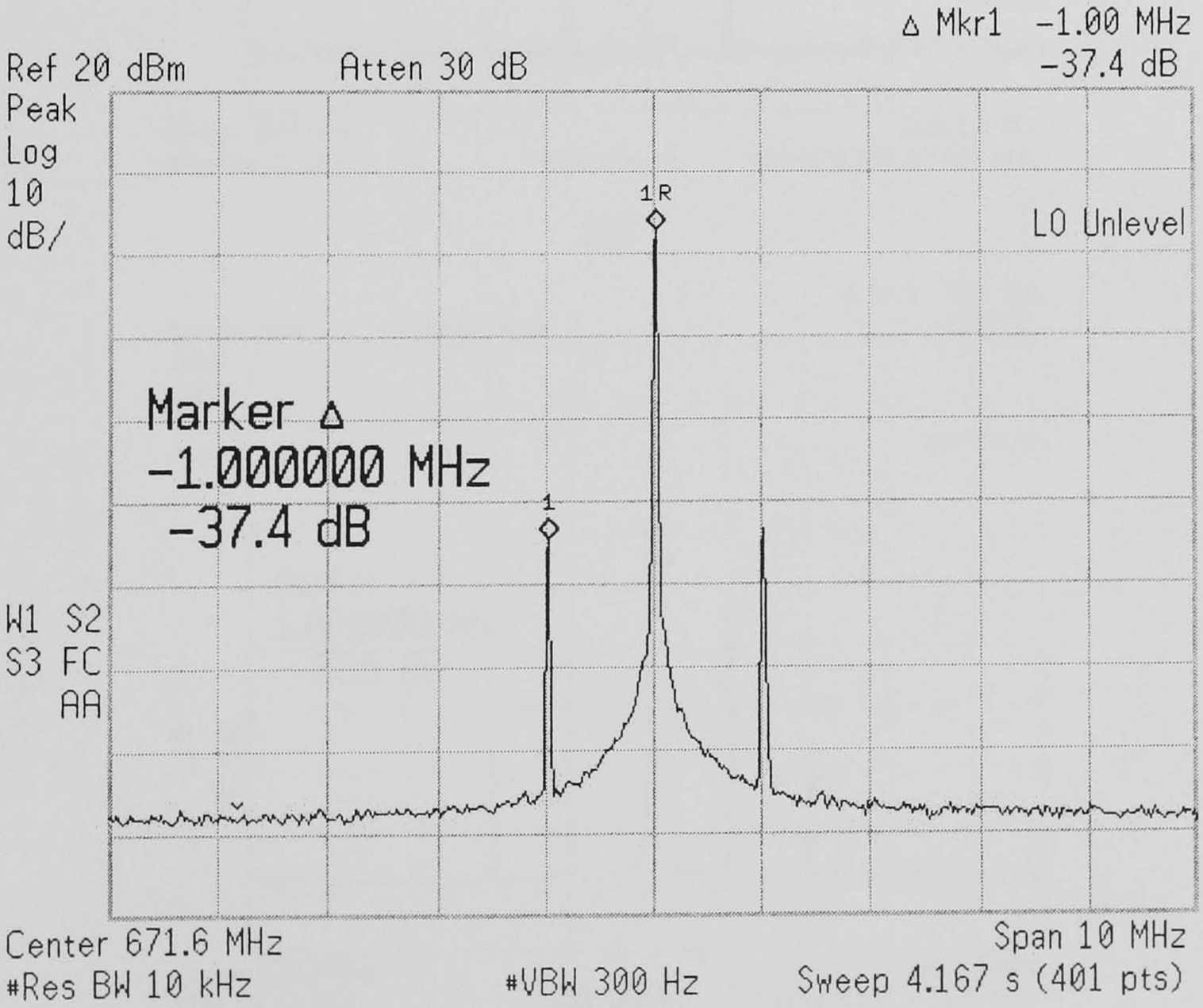


Figure 4.22 Output power spectrum of voltage controlled TGO.

Figure 4.22 shows the output power spectrum of the voltage controlled transposed gain oscillator. A carrier to first sideband ratio of 37.4 dB was observed. Using equation (4.16), the calculated carrier to sideband ratio is 39.95 dB. The LO has carrier to first sideband ratio of 18.11 dB, this is corresponding to $\beta = 0.25$. For the residual upper sideband output, the carrier to the first side band ratio is around 12 dB, the modulation index equals to 0.5. As can be seen, the residual upper sideband signal has modulation index doubled as predicted by equation (4.7). Figure 4.23 shows the LO leakage and the upper sideband power spectrum.

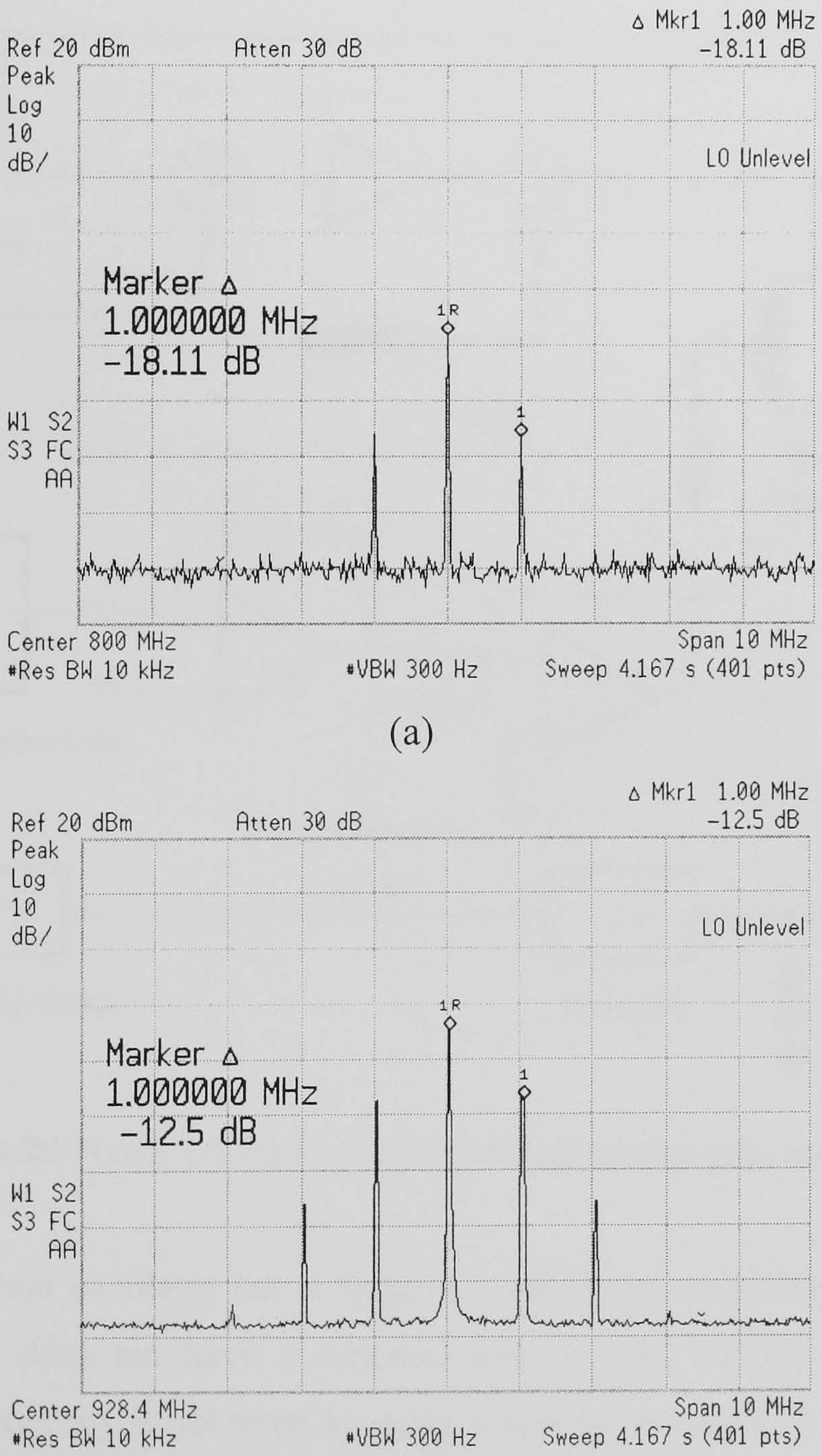


Figure 4.23 (a) Leakage local oscillator and (b) upper sideband output power spectrum.

4.7 Conclusions and Discussion

In this chapter, the LO sideband noise suppression mechanism in a transposed gain oscillator has been quantitatively investigated. An expression for carrier to sideband ratio around the zero-phase frequency of the transposed gain amplifier has been derived. The noisy local oscillator carrier is modelled by an FM signal. In a practical situation, although the modulating frequency is an indeterministic signal, the LO noise suppression is still the same. The LO sideband noise reduction mechanism of the transposed gain oscillator is proven by simulatíons and by the experiment using the voltage controlled oscillator.

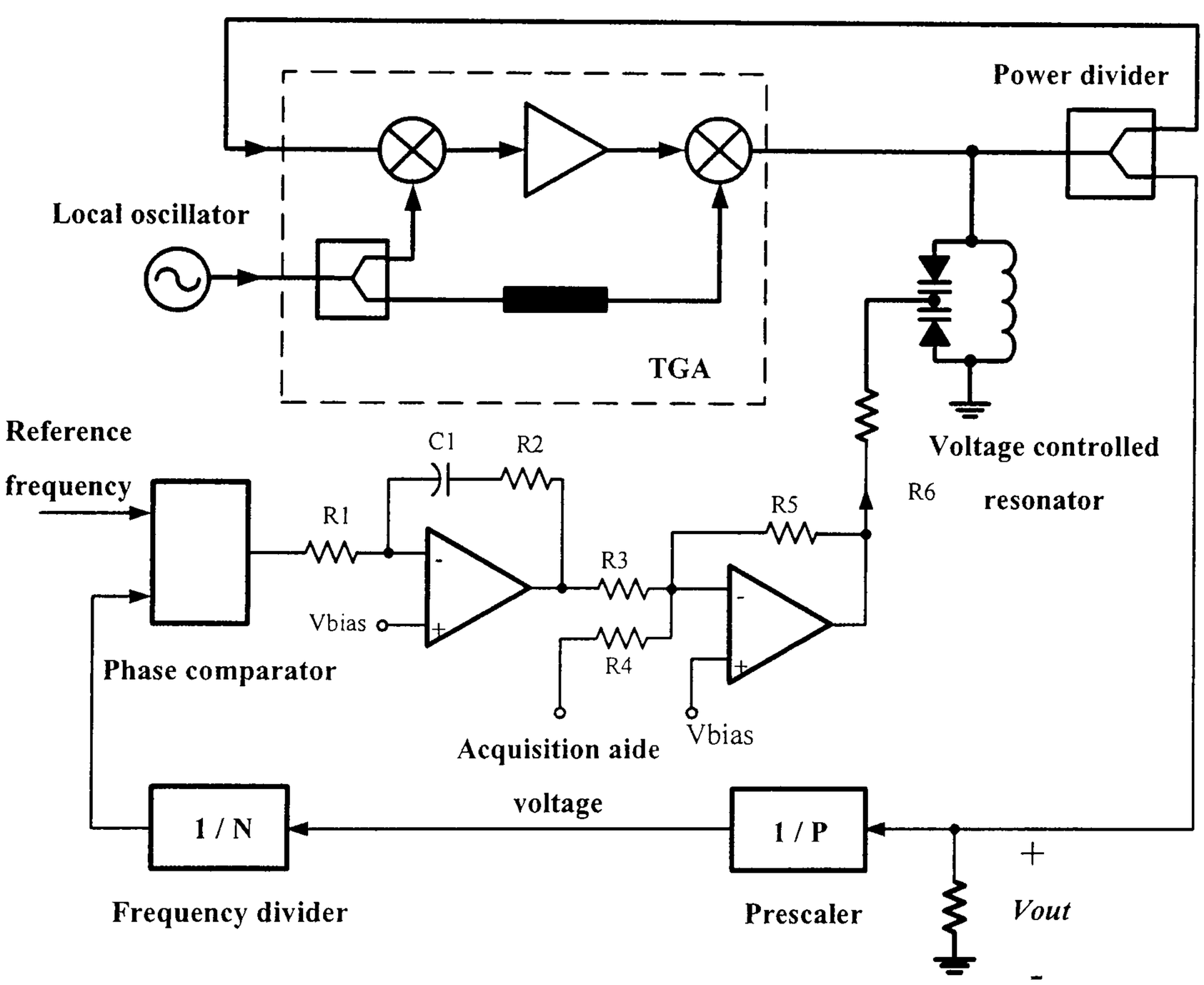


Figure 4.24 Phase locked-loop stabilised transposed gain oscillator.

The transposed gain oscillator has a frequency stabilising capability. However, the output frequency does not have a coherent relation with the LO frequency. The precise output frequency is achieved by using a high Q resonator. The determination of output frequency can be done by a phase locked-loop technique. The transposed gain oscillators ceased oscillation when the resonator resonant frequency deviated far

from the zero-phase frequency of the transposed gain amplifier. During the starting process, the phase comparator may drive the voltage controlled oscillator to the extreme frequency and the oscillation stopped. Thus, the acquisition aide circuit is required to cope with the start-up problem. Figure 4.24 shows a block diagram of a phase locked loop stabilised transposed gain oscillator with a simple acquisition aide circuit.

The LP-TGA driven transposed gain oscillator has been investigated in section 4.5. From the simulation results, it was found that the oscillator can give high degree of LO noise suppression without delay mismatch problem. The LP-TGA driven TGO needs a phase delay network in the feedback path to set the oscillation condition. The sideband noise reduction in the LP-TGA driven transposed gain oscillator is the same as for a conventional TGO. However, in theory, there is no delay mismatch problem.

Chapter 5

Jitter Reduction Circuit

The Anti-Jitter Circuit (AJC) is a direct carrier phase noise and jitter reduction technique. The AJC was patented by M. J. Underhill and has been described in EFTF papers [5.1-5.3] and in UFFC journal [5.25]. The functional block diagram of the AJC is shown in Figure 5.1. The circuit operates as follows; the sinusoidal input signal is first converted into a square wave in order to drive the input monostable circuit. Then the integrator converts the pulse train, with its DC component removed, into a sawtooth waveform. This sawtooth waveform has a constant ramp and its amplitude is modulated by the FM (PM) noise of the input signal. The comparator reference voltage is equal to the average value of the sawtooth waveform, the output pulse train of the comparator is re-timing by the monostable to eliminate the residual leading (or trailing) edge jitter. The removal of the DC component of the monostable output signal prevents the integrator from being driven into saturation because of its high DC gain.

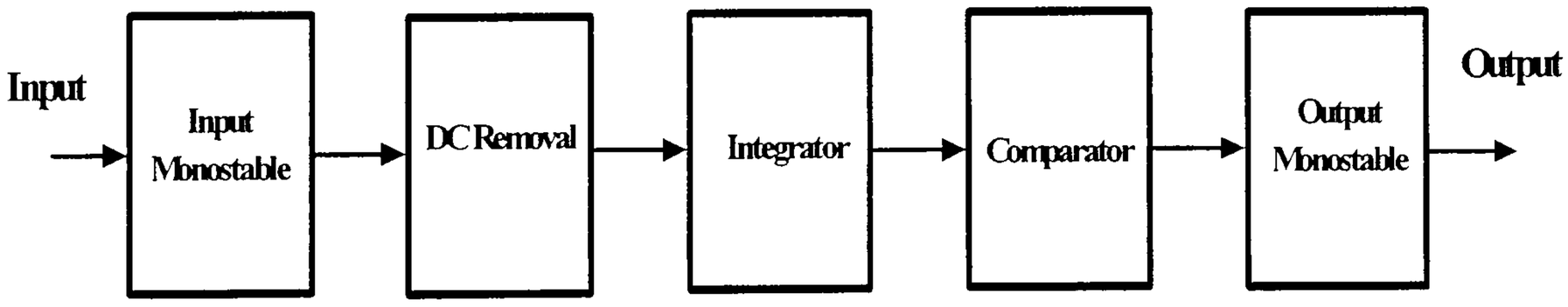
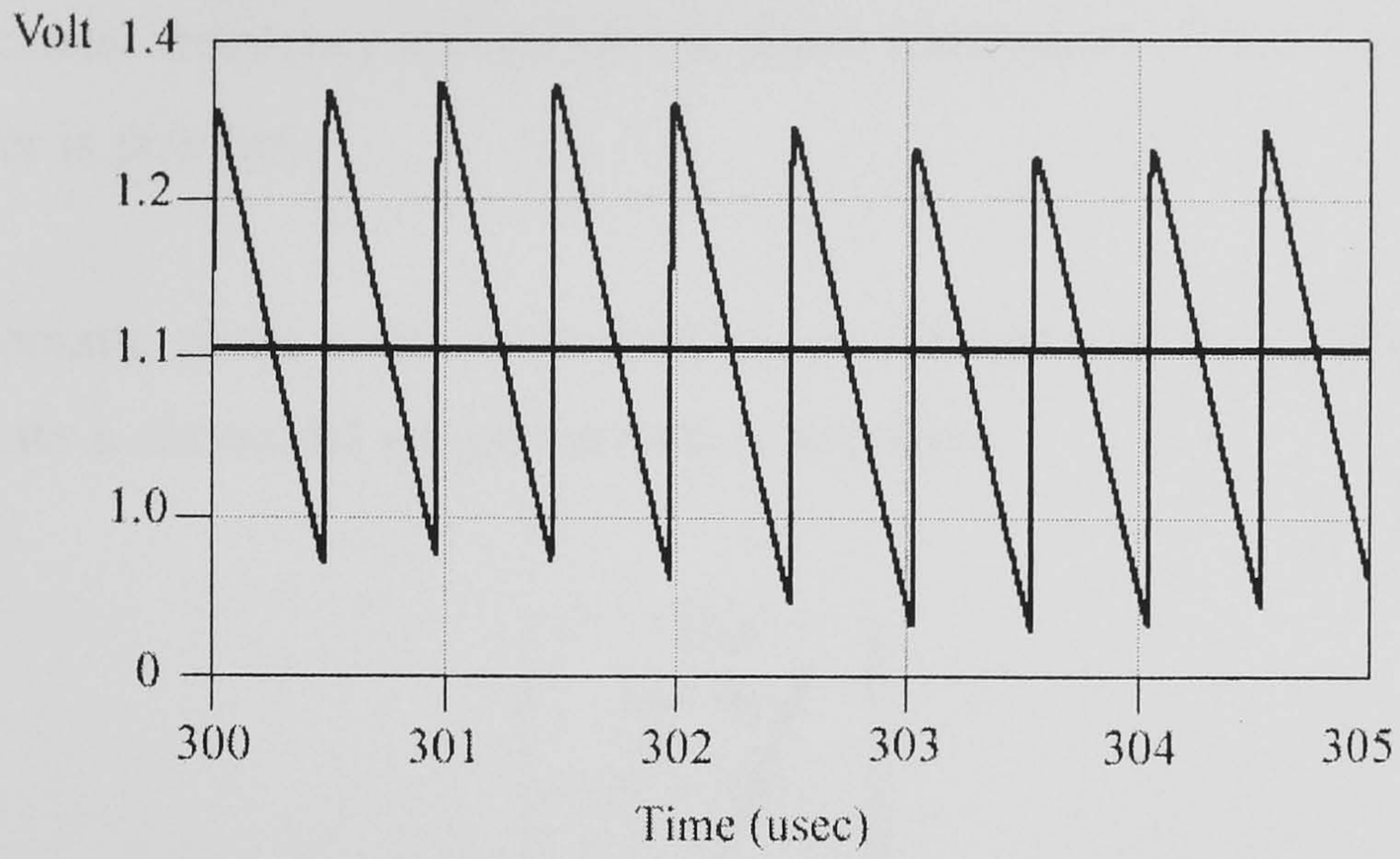


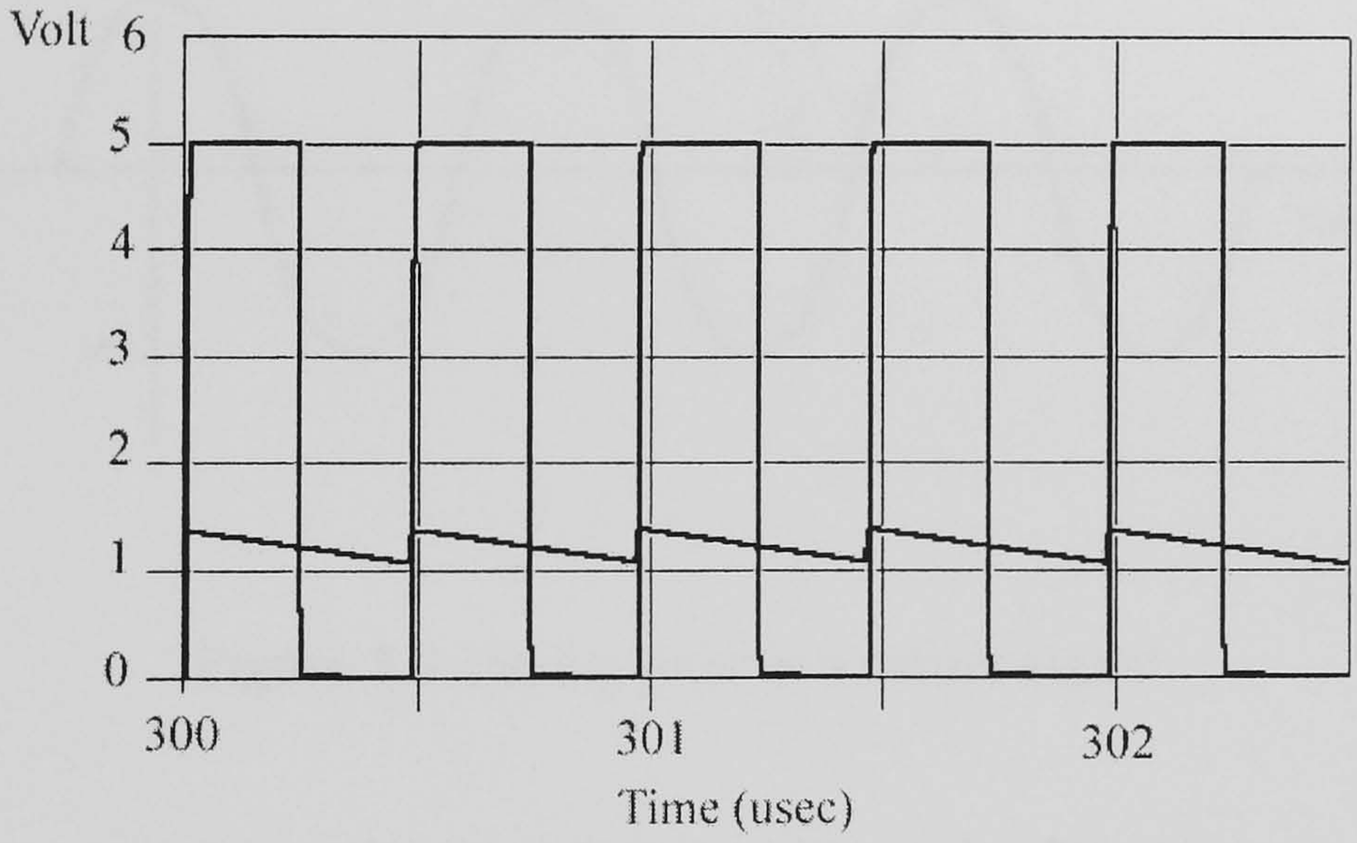
Figure 5.1 Anti-jitter block diagram.

Figure 5.2 shows the simulated waveforms in the typical AJC circuit. The sawtooth waveform in Figure 5.2 (a) is an output signal of the integrator, the waveform shows additionally amplitude variation. This variation is due to any FM (or PM) modulation of the input signal. One aspect of the integrator output voltage is that the average value of the output signal is crossed by the constant ramp at constant interval. Utilizing this character, time domain jitter reduction is made possible. The constant interval of the crossing is detected by the voltage comparator, thus the output signal

with jitter reduced can be reconstructed. The triggering point of the voltage comparator is when the voltage of the ramp is equal to its average value.



(a)



(b)

Figure 5.2 (a) Typical output waveform of the integrator and its average value and (b) input signal and output signal of the comparator.

5.1 Jitter Reduction Technique

The phase fluctuations of the carrier signal give rise to fluctuations of the zero crossing of the carrier signal and can be expressed as:-

$$v(t) = A(t)\cos\left[2\pi f_o t + \phi(t)\right] = A(t)\cos\left[2\pi f_o\left(t + \frac{\phi(t)}{2\pi f_o}\right)\right]. \qquad (5.1)$$

where f_o is a carrier frequency and $\phi(t)$ is the phase fluctuations. From equation (5.1), the timing jitter is $\phi(t)/2\pi f_o$.

In the time domain, phase noise is the random perturbation of the oscillator period. Figure 5.3 shows a sinusoidal waveform with timing jitter.

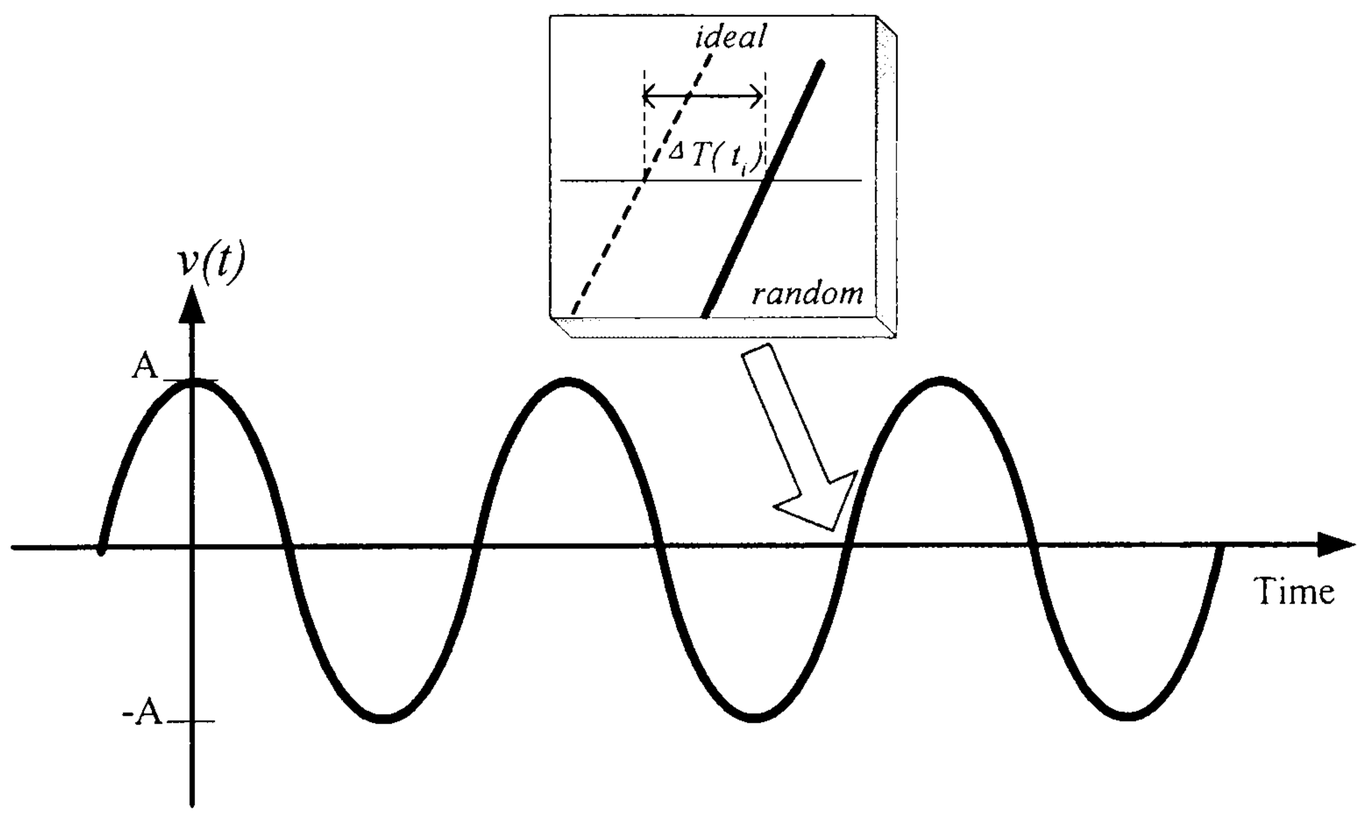


Figure 5.3 Timing jitter in a carrier signal.

At the zero crossing, the timing jitter happens discretely. Therefore, the waveform in Figure 5.3 can be expressed in terms of random timing variations as [5.4]:-

$$v(t) = A(t)\cos\left\{2\pi f_o\left[t - X(t)\right]\right\} \qquad (5.2)$$

where $A(t)$ is the amplitude and $X(t)$ is the discrete-time random process due to the random phase fluctuations.

Equation (5.2) can be re-written as:-

$$v(t) = A(t)\cos(2\pi f_o)\cos\left[2\pi f_o X(t)\right] + A(t)\sin(2\pi f_o t)\sin\left[2\pi f_o X(t)\right]. \quad (5.3)$$

The timing error is much smaller than the oscillation period, $T = 1/f_o$. Thus, $X(t)$ can be approximated with a discrete-time impulse function,

$$X(t) \Rightarrow X(nT)\ n \in \text{integer}. \quad (5.4)$$

Equation (5.3) can be simplified as:-

$$v(t) \cong A(t)\cos(2\pi f_o t) + A(t)\sin(2\pi f_o t)\left[2\pi f_o X(t)\right]. \quad (5.5)$$

From equation (5.5), the carrier power and noise power are obviously separated. The second term, the phase noise term is a low frequency noise component modulated up to the carrier frequency. Phase noise to carrier power can be deduced from equation (5.5) as:-

$$\frac{NoisePower}{CarrierPower} = \frac{0.5(A2\pi f_o)^2\left[S_{X(nT)}(f)\right]}{0.5A^2} = (2\pi f_o)^2\left[S_{X(nT)}(f)\right] \quad (5.6)$$

where the carrier signal is a deterministic signal with power of $A^2/2$.

Because $X(nT)$ is a random process, its power spectral density, $S_{T(t)}(f)$, is used to find the noise power. Thus, the noise power is $0.5(A \cdot 2\pi f_o)^2[S_{X(nT)}(f)]$. In order to estimate the phase noise of $v(t)$, the estimation of the power spectral density (PSD) of the random process, $X(nT)$, is needed. From equation (5.1)-(5.6), it is obvious that if the PSD of $X(nT)$ is reduced then timing jitter (and phase noise) is also reduced.

It is more convenient to view the timing variation or jitter when the carrier signal is converted into a square wave or a clock signal. Phase jitter is defined as the standard deviation, $\sigma\Delta_\phi$, of the phase difference between the first cycle and ith cycle of the clock waveform. Timing jitter can be expressed in terms of phase jitter by $\sigma_{\Delta T} = (T/2\pi)\sigma\Delta\phi = (1/2\pi f_o)\ \sigma\Delta\phi$ where the clock period, T, is $2\pi/2\pi f_o$. A perturbation in the phase during one period of oscillation changes the starting point of the next one. As

can be seen, $\Delta T(t)$ is a random function that cause the jitter phenomena. The square wave signal with the timing jitter modeled by uniform distribution is shown in Figure 5.4.

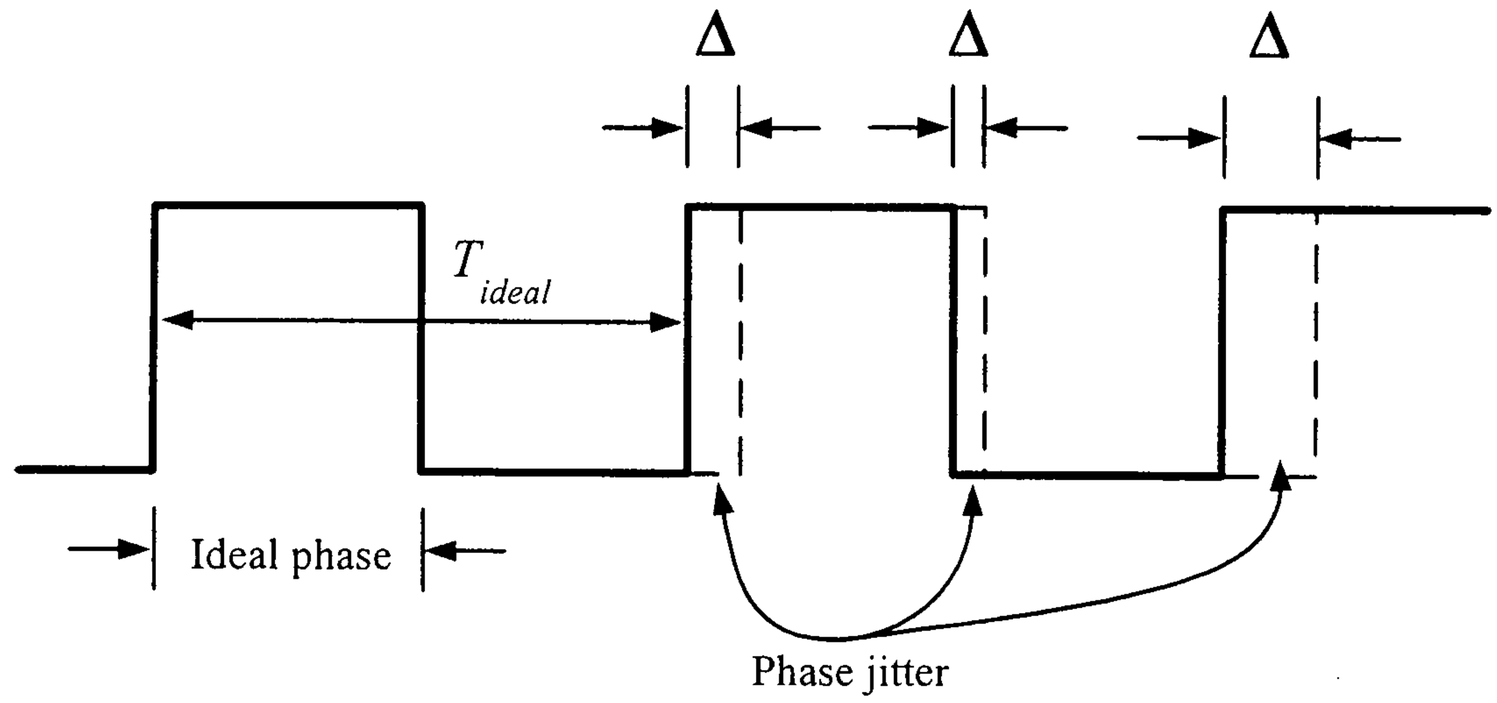


Figure 5.4 Ideal period and timing jitter of a clock signal.

The uniform distribution jitter can be defined as [5.5]:-

$$T_{jitter} = T_{ideal} + \sum_{j=0}^{1} \Delta_j \tag{5.7}$$

where Δ is a random variable distributed uniformly from α to $-\alpha$, α is equal to the peak-to-peak of the jitter of the clock signal, T_{ideal} is the period of the jitterless clock. It is assumed that all jitter sources are independent and identical in statistics. There are algorithms applied to compensate for timing distortions due to jitter [5.6].

From these viewpoints, the signal jitter can be reduced if the PSD of $X(nt)$ or the mean square value of $\Delta T(t)$ is reduced. The reduction can be done by averaging. The time domain averaging process is usually considered because of its simplicity. The time-domain average of the periods of equation (5.7) is [5.5]:-

$$T_{average} = \frac{\sum_{i=0}^{n-1} T_{jitter(i)}}{n} \tag{5.8}$$

where n is a averaging number.

The averaging of equation (5.8) gives the output signal as a clock signal with reduced T_{jitter}. After n averaging, the output of the process can be expressed as:-

$$T_{average} = T_{ideal} + \frac{\sum_{i=0}^{n-1}\sum_{j=0}^{1}\Delta_{ij}}{n}. \tag{5.9}$$

The second term in equation (5.9) is an error after average. By the central limit theorem [5.7], it is shown that the variance after averaging process in equation (5.9) is less than the original signal. This means that jitter has been reduced by an averaging process. It is possible to minimize the second term of equation (5.9), but it cannot be reduced to zero. From this concept, the novel jitter circuit has been developed. The implementation of the idea is based on the anti-jitter circuit operation. The digital realisation of this concept has been presented [5.5].

5.2 Novel Jitter Reduction Circuit

The functional block diagram of the novel jitter reduction circuit is shown in Figure 5.5. The circuit operates as follows; the sinusoidal input signal is first converted into a square wave in order to drive pulse splitter circuit. Then the integrators convert the positive and negative pulse train into sawtooth waveforms. These sawtooth waveforms have a constant ramp and its amplitude is modulated by the FM (PM) noise of the input signal. From the block diagram, the averaging operation in equation (5.9) is performed by both integrators. The integrators average the leading and trailing edge jitters of the pulse splitter's output signals. The comparators reference voltage is equal to the mean value of the sawtooth waveform. The output signal of the jitter reduction circuit is reconstructed by the phase comparison of the comparators output waveforms.

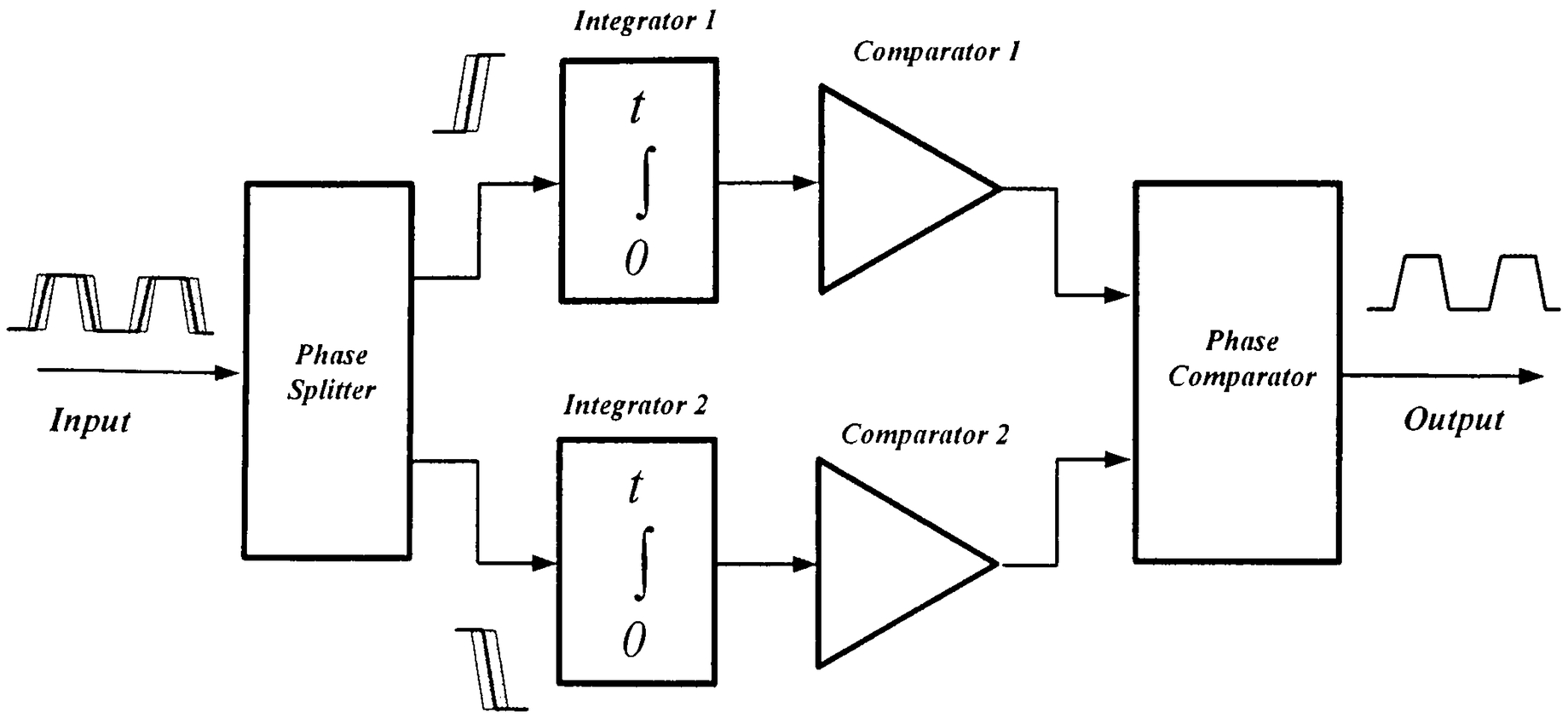


Figure 5.5 Block diagram of the novel jitter reduction circuit.

5.3 Circuit Building Blocks

According to the block diagram of Figure 5.5 and the waveforms in Figure 5.2, the circuit resembles one of the basic techniques for demodulating an FM signal [5.8], but the comparator is placed at the output of the integrator instead of the envelope demodulator. If the jitter reduction circuits have to be implemented by all analog circuitry, the balanced direct differentiation circuit in [5.8] can be used as the phase splitter block in figure 5.5. Normally, the complementary output phase splitter is performed by the monostable circuits.

5.3.1 Integrator Circuits

The integrators integrate the output signal of the phase splitter, which contains timing jitter, into a sawtooth waveform with a constant mean DC level. The integrator's ramp crosses over the reference level with a constant period. The crossing period can be detected by the high speed voltage comparator. Since the integrator is a basic building block of the most continuous-time filters, these basic building blocks also can be employed as integrators in Figure 5.5. Figure 5.6 shows the operational transconductance amplifier based continuous-time lossy integrator [5.9] that can perform the integrating function in the jitter reduction circuits.

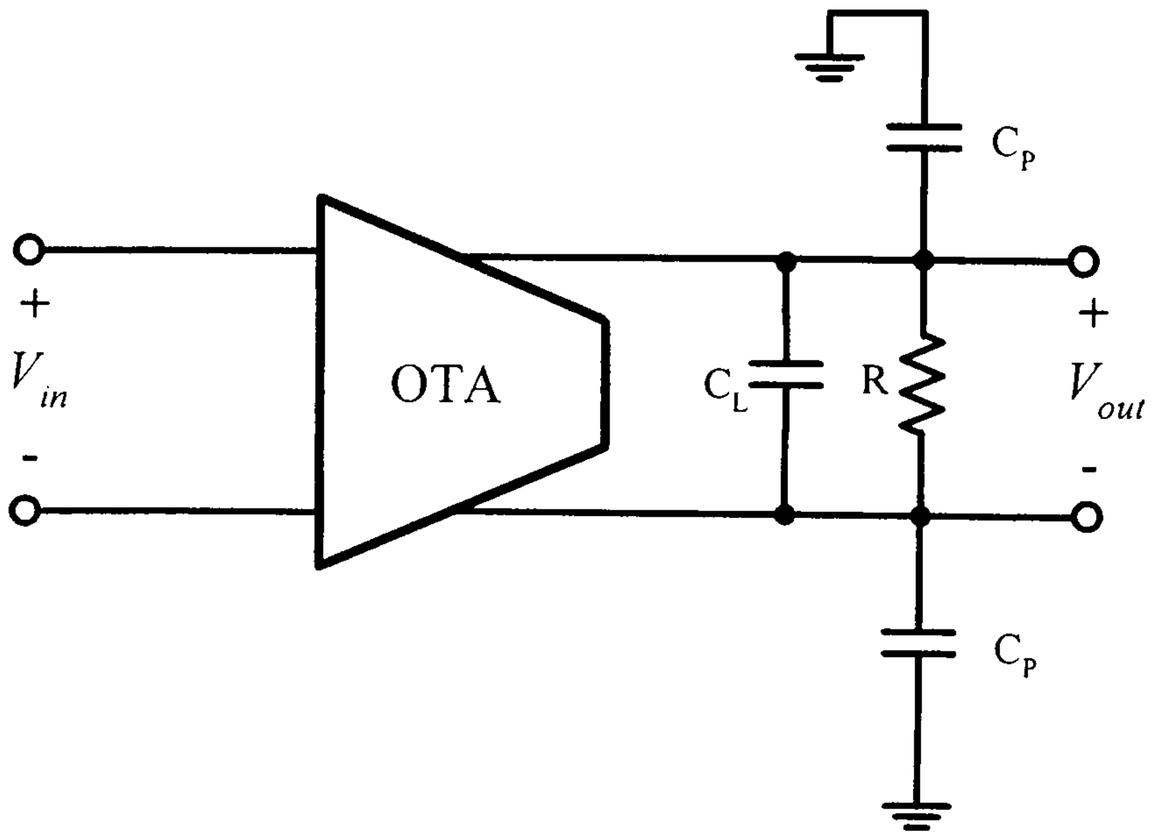


Figure 5.6 Continuous-time lossy integrator.

The ideal transfer function of the lossy integrator shown in Figure 5.5 is given by:-

$$\frac{v_o}{v_i}(s) = g_m R \frac{1}{1+sRC} \tag{5.10}$$

where $C = C_L + C_P/2$.

This transfer function corresponds to the typical first-order low pass filter with DC gain equal to g_mR and pole frequency at $\omega = 1/RC$. Figure 5.7 shows the transistor level lossy integrator circuit used in this research. The circuit employs the multi-tanh technique to linearise the output transconductance [5.10-5.12].

The DC response of the integrator is not a desired characteristic because of the drifting and offset problems. Compared to the band pass response, the ideal integrator gives higher output noise voltage due to its wider equivalent noise bandwidth [5.13].

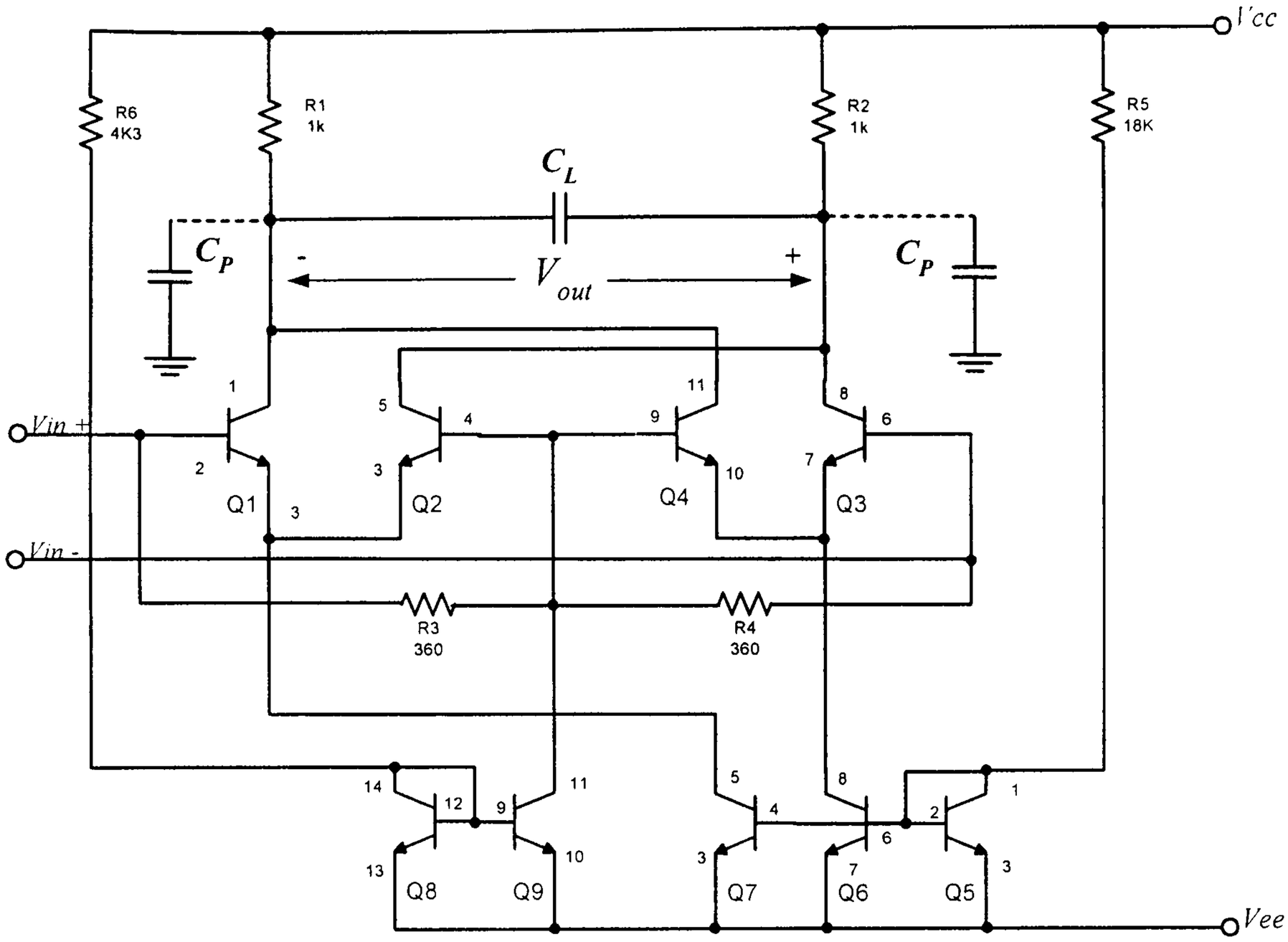


Figure 5.7 Multi-tanh linearised gm-C integrator.

Because of these practical aspects an active resonant circuit can be used as an integrator. The stop band response of 6 dB per octave and a 90 degree constant phase shift in the stop band region of the resonant circuit can perform an integration function. Figure 5.8 shows the magnitude and phase response of a 1 MHz, Q = 5, parallel resonant circuit. As can be seen, at a frequency 10 times higher than the resonance frequency, the phase function of the resonant circuit is close to an ideal integrator response.

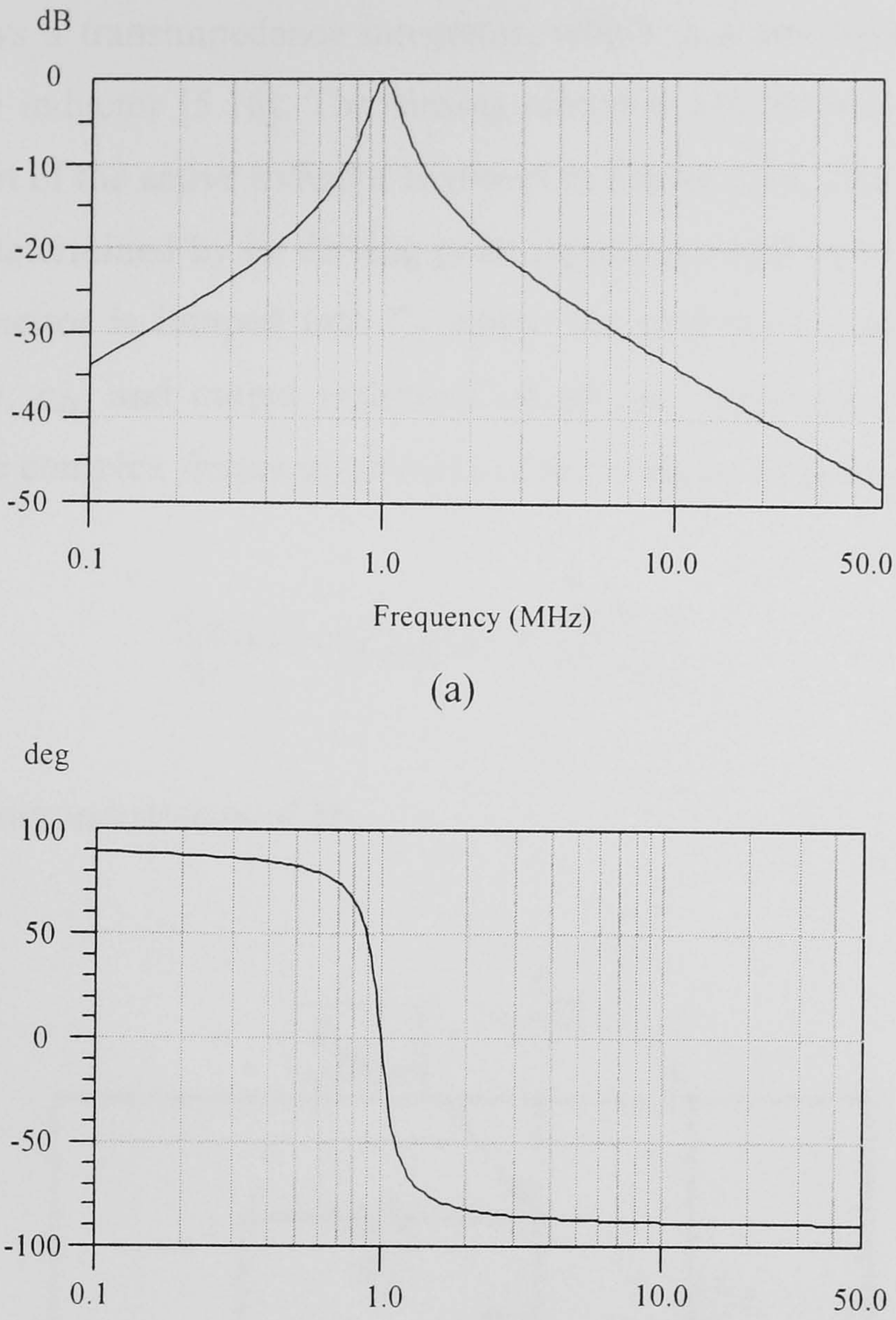


Figure 5.8 (a) Magnitude and (b) phase response of a 1MHz, $Q = 5$, parallel resonator.

5.3.2 Band Pass Network as an Integrator

The stop band characteristic of a band pass network can be employed to produce an integrating function. The conventional bilinear transfer function networks or the active inductor-capacitor circuits give a response of 6 dB per octave and a 90 degree constant phase shift in the stop band region. An active inductor is an inductive transistor circuit. Using proper topologies, active inductor can be designed to have stable, high-Q performance with large tunablity and bandwidth [5.14-5.15].

Figure 5.9 shows a transimpedance integrator, which is a combination of capacitor and lossy active inductor [5.16]. The biasing circuit is not shown. The small signal equivalent circuit of the active inductor is shown in Figure 5.10. The output voltage of the inductor is determined by its driving point impedance and input current i_{in}. If the gate-source capacitor is lumped into C_1 where the gate-drain capacitor, c_{gd}, drain-source capacitor, c_{ds}, and output resistance of M_1 are neglected, the driving point impedance in the complex frequency domain of the inductor is given by:-

$$\frac{v_{out}}{i_{in}}(s) = Z_{ind}(s) = \frac{sC_1R_1+1}{sC_1+g_m} \tag{5.11}$$

where g_m is a transconductance of M_1.

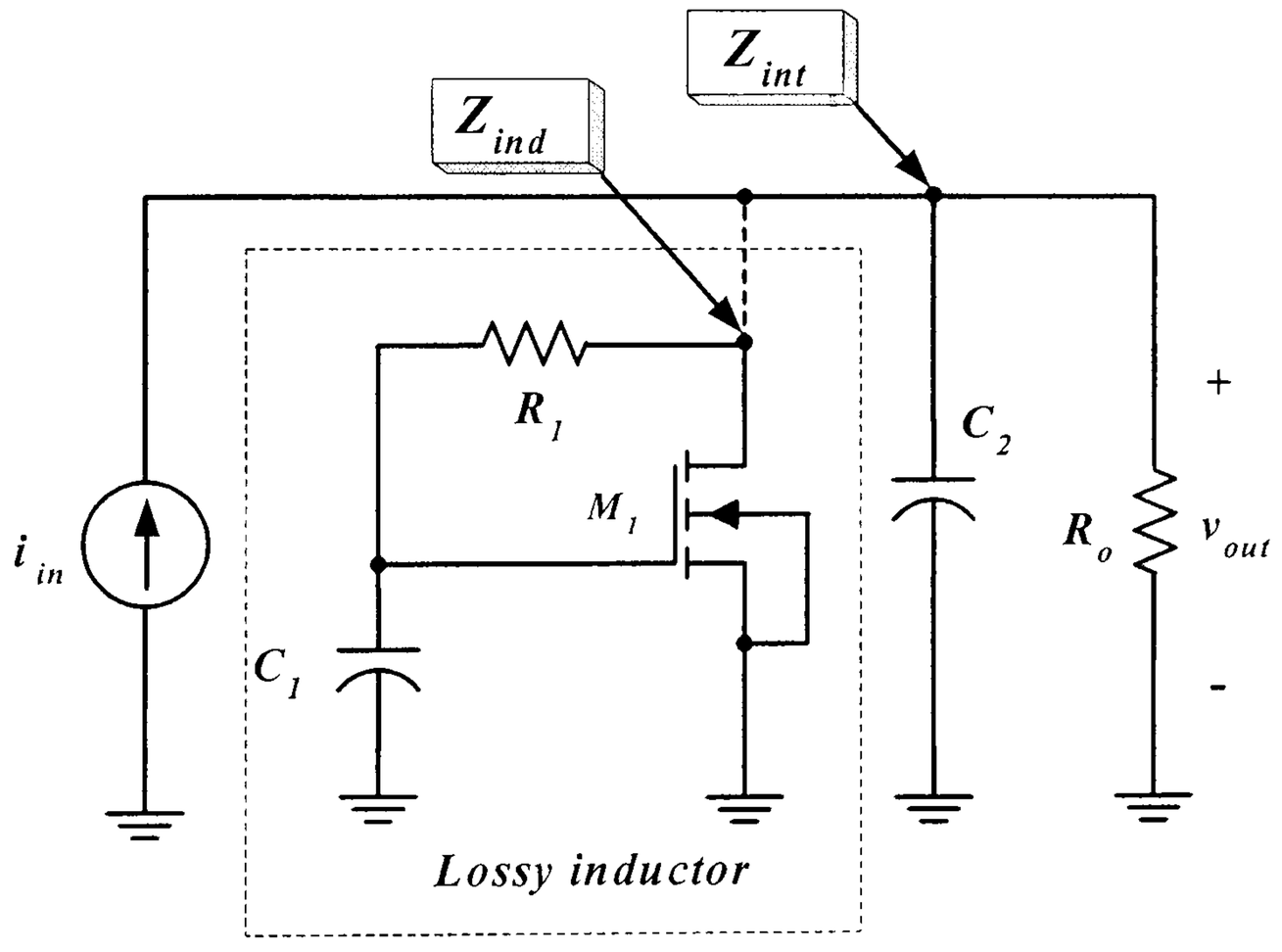


Figure 5.9 Active inductor-capacitor integrator.

The small signal equivalent circuit when an integrating capacitor is added is shown in Figure 5.11. The driving point impedance in the complex frequency domain becomes:-

$$\frac{v_{out}}{i_{in}}(s) = Z_{\text{int}}(s) = \frac{(sC_1R_1+1)R_o}{s^2C_1C_2R_1R_o + s(C_2R_o + C_1R_o + R_1C_1)+1+R_o g_m} \tag{5.12}$$

where R_o is a load resistance.

The frequency response of equation (5.12) shows two deflection points, the first one is a zero frequency which is defined by:-

$$\omega_z = \frac{1}{R_1 C_1}. \tag{5.13}$$

The second deflection point occurs at pole frequency of equation (5.12), which can be solved directly from the denominator.

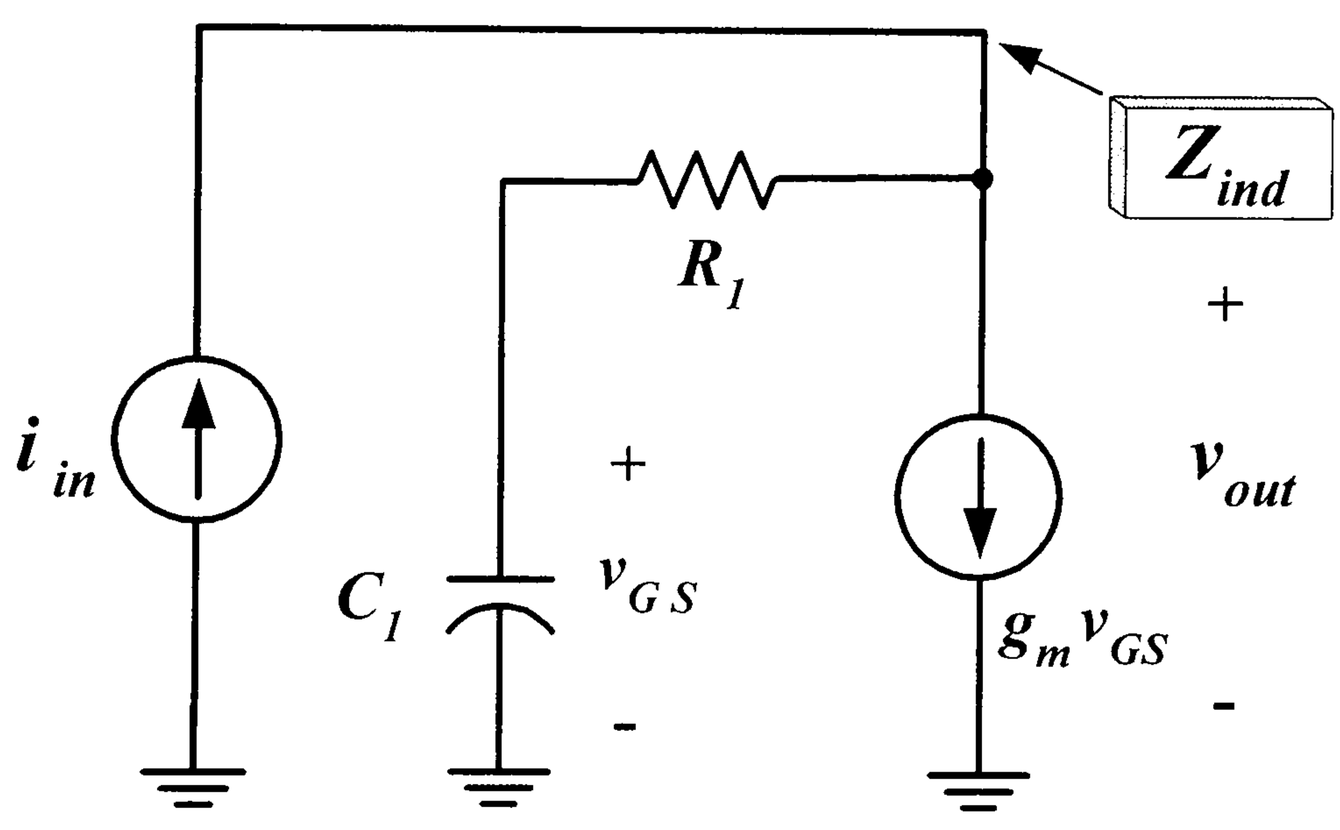


Figure 5.10 Lossy active inductor.

The combination of the lossy inductor and capacitor C_2 forms a resonant circuit. The resonance frequency can be observed from the phase cross over of $Z_{ind}(j\omega)$. At this frequency, the susceptance of $Y_{ind}(j\omega)$ is equal to the susceptance of capacitor C_2 or:-

$$\omega C_2 - \mathrm{Im}(Y_{ind}) = 0. \tag{5.14}$$

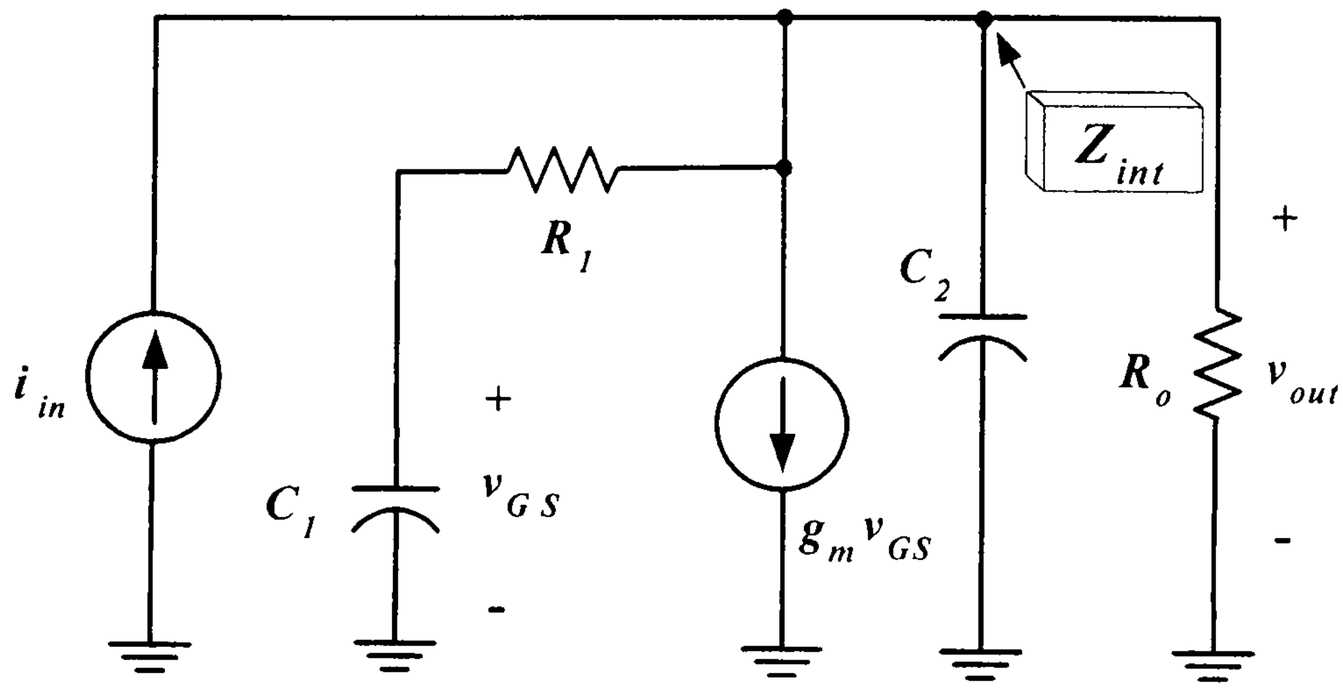


Figure 5.11 Integrator small signal model.

The admittance of $Y_{ind}(j\omega)$ is given by:-

$$Y_{ind}(j\omega) = \frac{1}{Z_{ind}(j\omega)} = \frac{g_m + \omega^2 C_1^2 R_1}{1+\omega^2 R_1^2 C_1^2} - \frac{j(\omega C_1 R_1 g_m - \omega C_1)}{1+\omega^2 R_1^2 C_1^2}. \tag{5.15}$$

Substitution of the imaginary part of $Y_{ind}(j\omega)$ into (5.14) and solving for ω_o yeilds:-

$$\omega_o = \sqrt{\frac{(R_1 C_1 g_m - C_1 - C_2)}{C_2 R_1^2 C_1^2}}. \tag{5.16}$$

In order to achieve a correct integration, the operating frequency must be at least 10 times higher than ω_o. As an example, if the following components R_1 = 3.9kΩ, C_1 = 47 nF, C_2 = 220pF and gm = 10 mS are chosen, the resonance frequency is 78.228 KHz. The log-magnitude and phase plot of the integrator using these components is shown in Figure- 5.12. As can be seen from plotting, at frequencies above 1 MHz the phase response is close to 90°, which is the ideal case of the integrator.

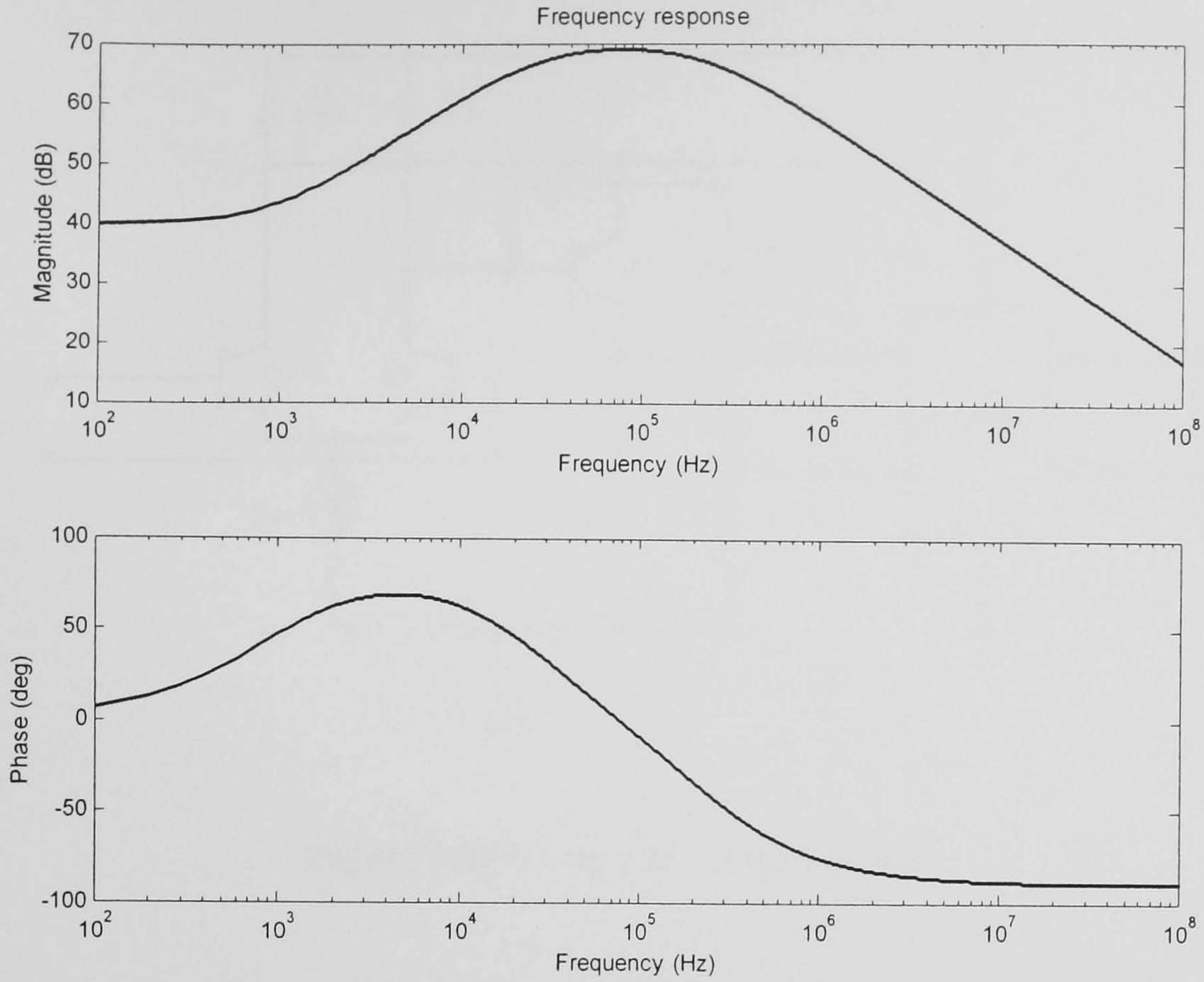


Figure 5.12 Frequency response of an example integrator.

The integrating capacitor C_2 is charged by the output signal from the pulse splitter in each cycle. During the impulse period, C_2 is discharged by the drain current of M_1 at a constant rate.

5.4 Jitter Reduction Performance

The block diagram of a jitter reduction circuit in Figure 5.5 is evaluated using time-domain simulation for sideband noise reduction. The input signal is 2 MHz FM with a variable modulating frequency and a modulation index of 0.5. The sinusoidal carrier is converted into a square wave signal by the voltage comparator which shown in Figure 5.13. The comparator uses a PNP regenerative pair to enhance operating speed. Using HARRIS® UHF-1 process as the transistors model [5.24], the comparator circuit works well up to the low-band VHF (70MHz).

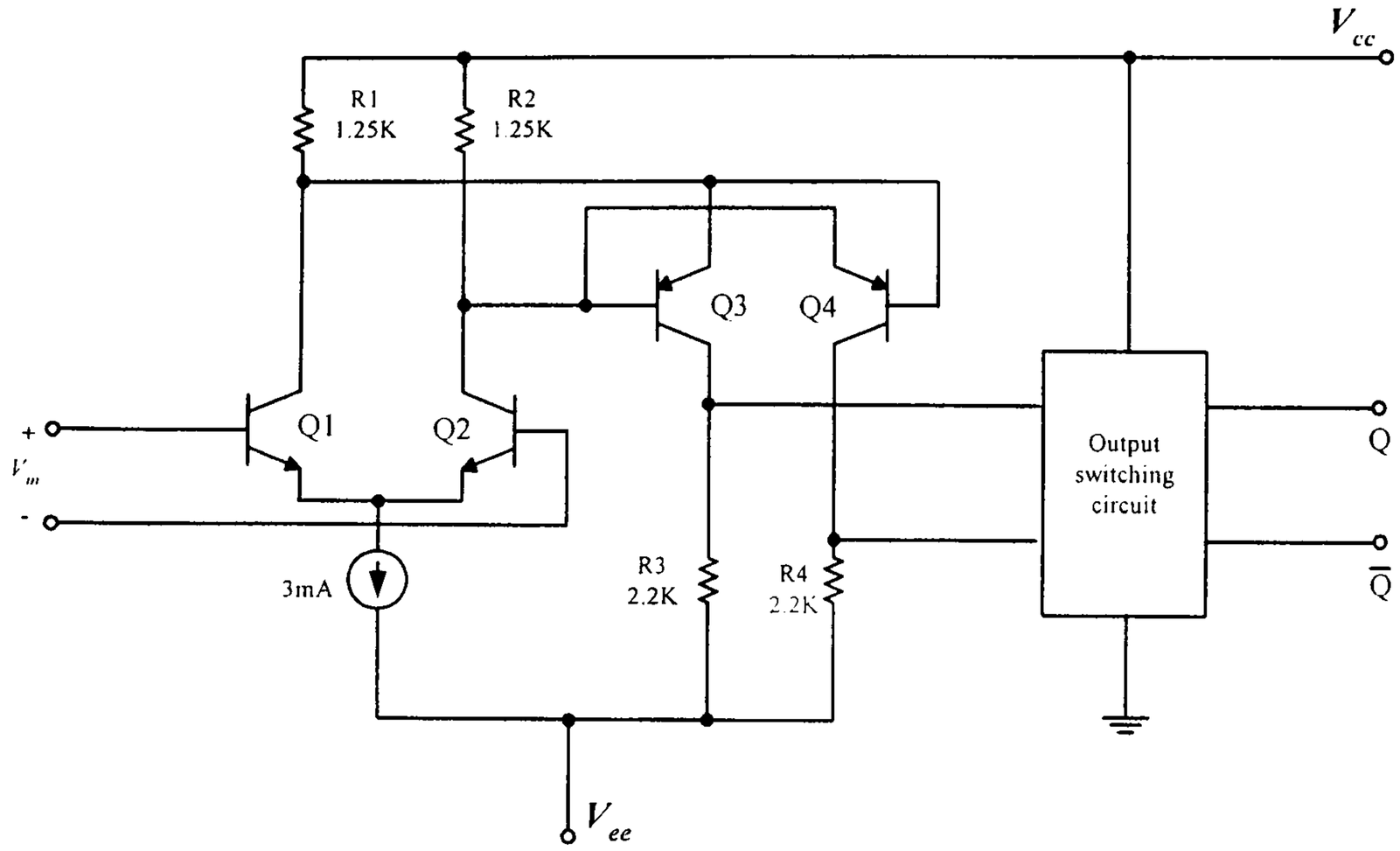


Figure 5.13 Comparator circuit model.

A behavioural model is employed as switching circuits and Agilent ADS® transient simulator has been used to investigate the performance of the jitter reduction circuit. The phase comparator must operate at the correct transition of the integrators output ramp signal. The suppression achieved on the noise sidebands is measured in the frequency domain by comparing the input and output spectra as observed by fast Fourier transformation of the time domain signals.

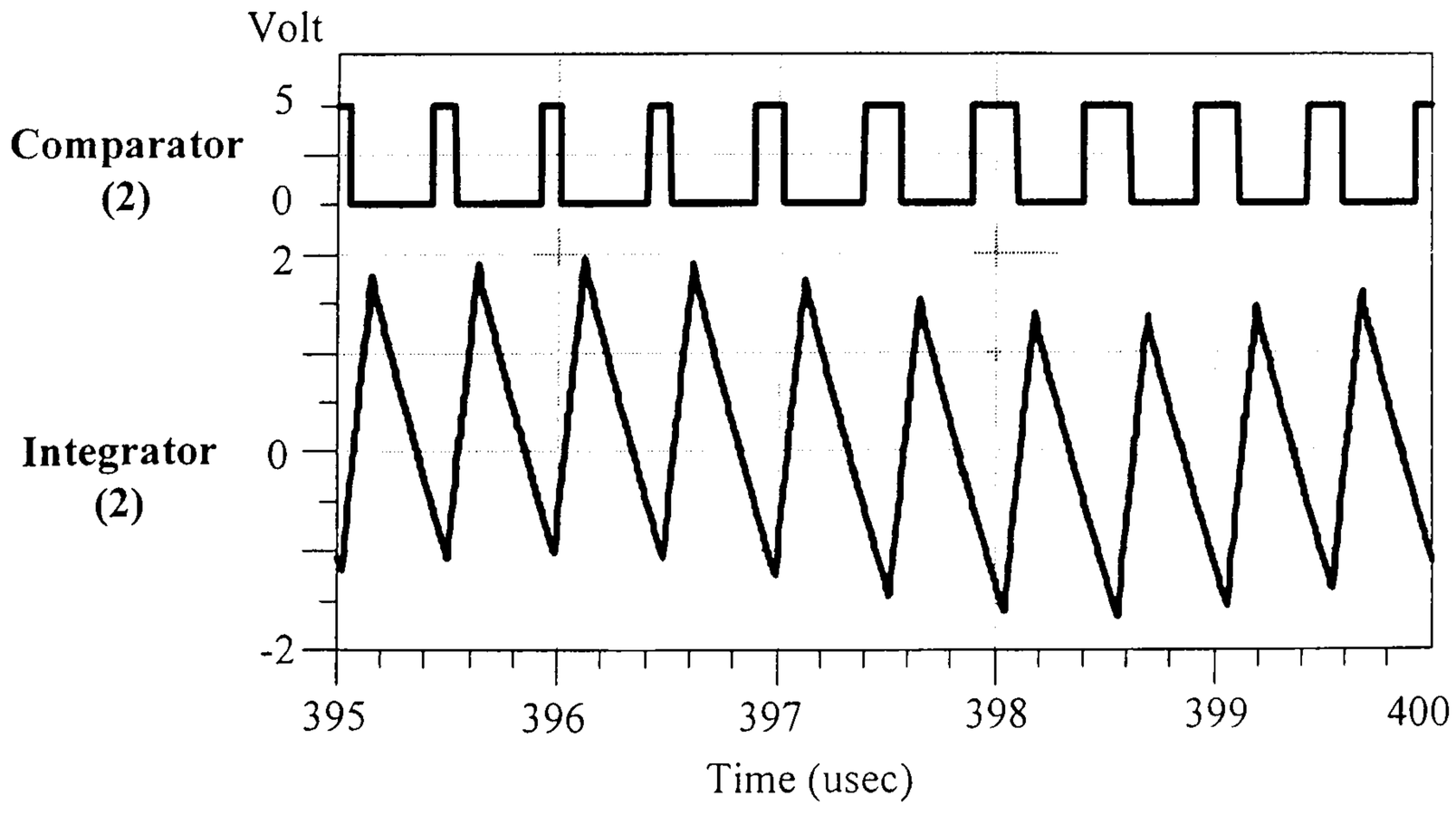


Figure 5.14 Comparator 2 input-output signal.

Figure 5.14 shows the simulated input and output voltage of the comparator 2 in Figure 5.5. Figure 5.15 shows the input-signal of the phase comparator. As can be seen, the upper trace shows constant pulse width after the process.

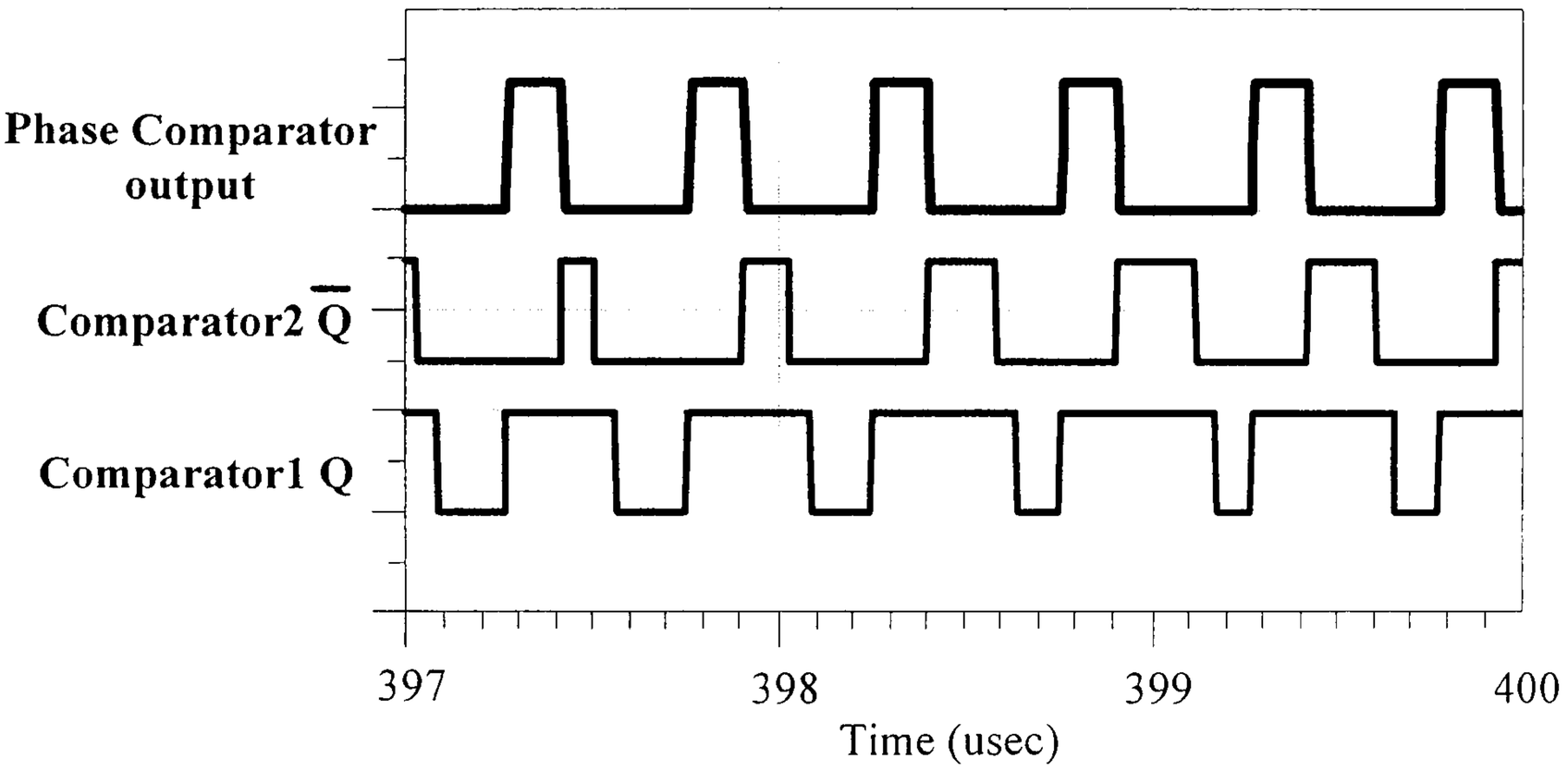


Figure 5.15 Phase comparator input-output signal.

The simulation shows that the jitter reduction circuit has suppression almost the same as the integrator response. By inspection, above 100 KHz of the offset frequency, the sideband suppression is around 6 dB per octave of the offset frequency. This response does not depend on the type of integrator circuits. All integrator circuits give the same sideband suppression.

5.5 Jitter Reduction Circuit Experiments

The block diagram in Figure 5.5 is implemented using integrated and discrete components. Firstly, the voltage comparator, AD8561, converts the sinusoidal input signal into square wave signal. The phase splitter is performed by the high speed CMOS, 74HCT123, monostable circuit as shown in Figure 5.16. If the sine wave operation is not required, the splitter circuit can operate directly from the square wave input signal.

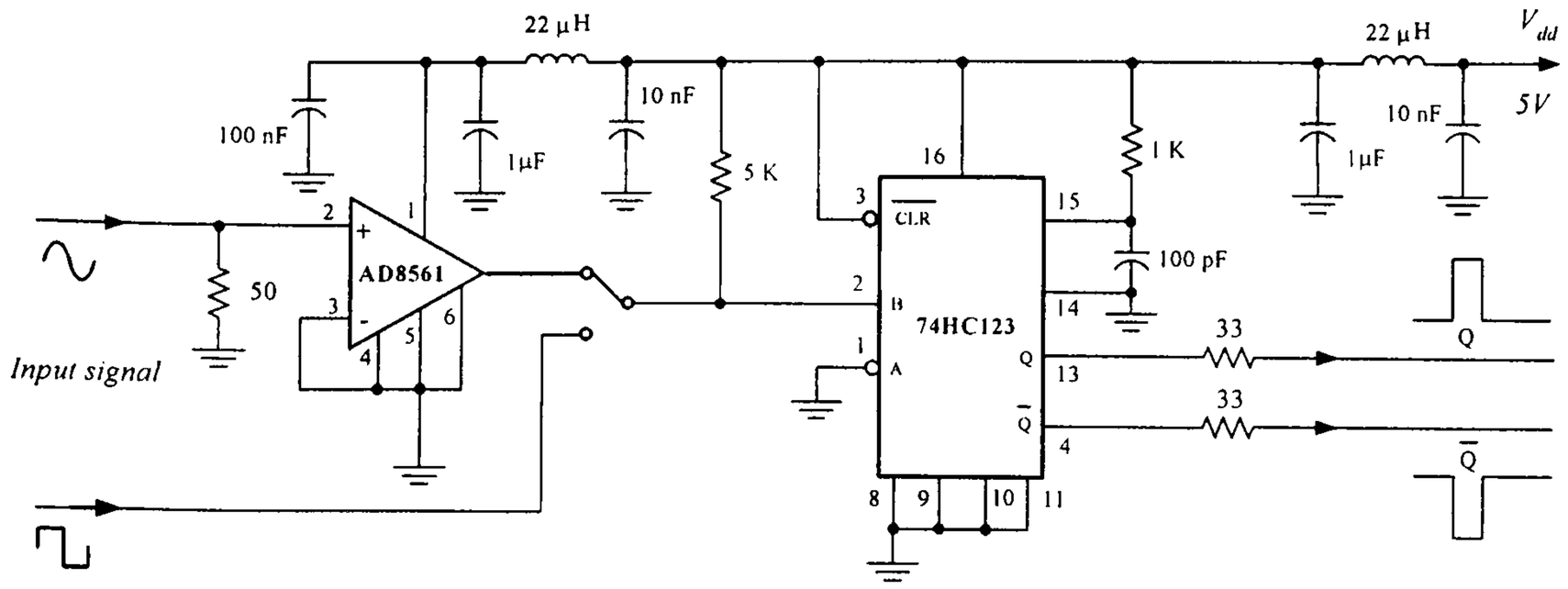


Figure 5.16 Sine to square and phase splitter circuit.

A simple bilinear transfer function band pass circuit is used for the integrators. Figure 5.17 shows an integrator circuit. The transfer function of the band pass network is given by [5.17]:-

$$\frac{v_{out}}{v_{in}}(s) = \frac{sC_1R_2}{(sC_2R_2+1)(sC_1R_1+1)} \tag{5.17}$$

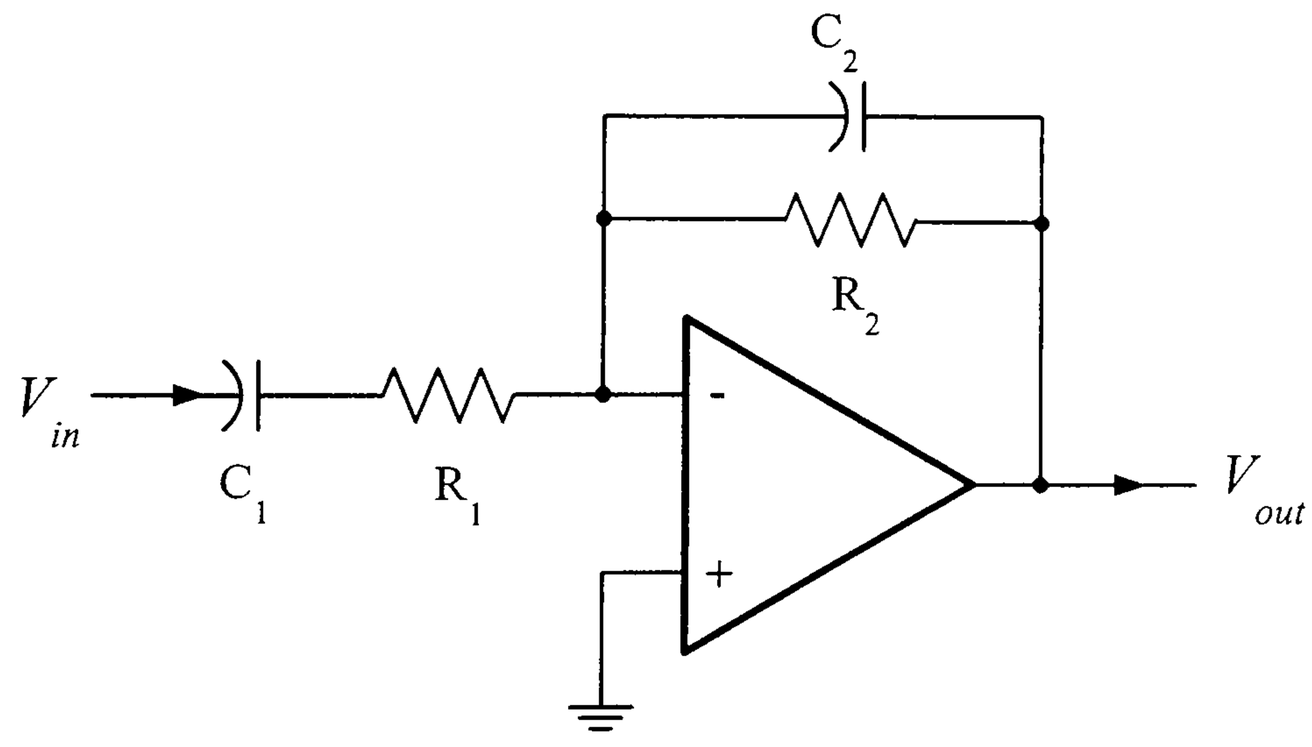


Figure 5.17 Band pass network as an integrator.

From equation (5.17), the network has one zero at DC and two poles. The operating frequency of the integrator is ten times higher than the highest pole frequency of the transfer function. If the following components R_1 = 50 Ω, R_2 = 10kΩ, C_1 = 220nF and

C_2 = 220pF are chosen and the phase reversal of the inverting amplifier is neglected, the frequency response of the integrator is depicted by plotting in Figure 5.18.

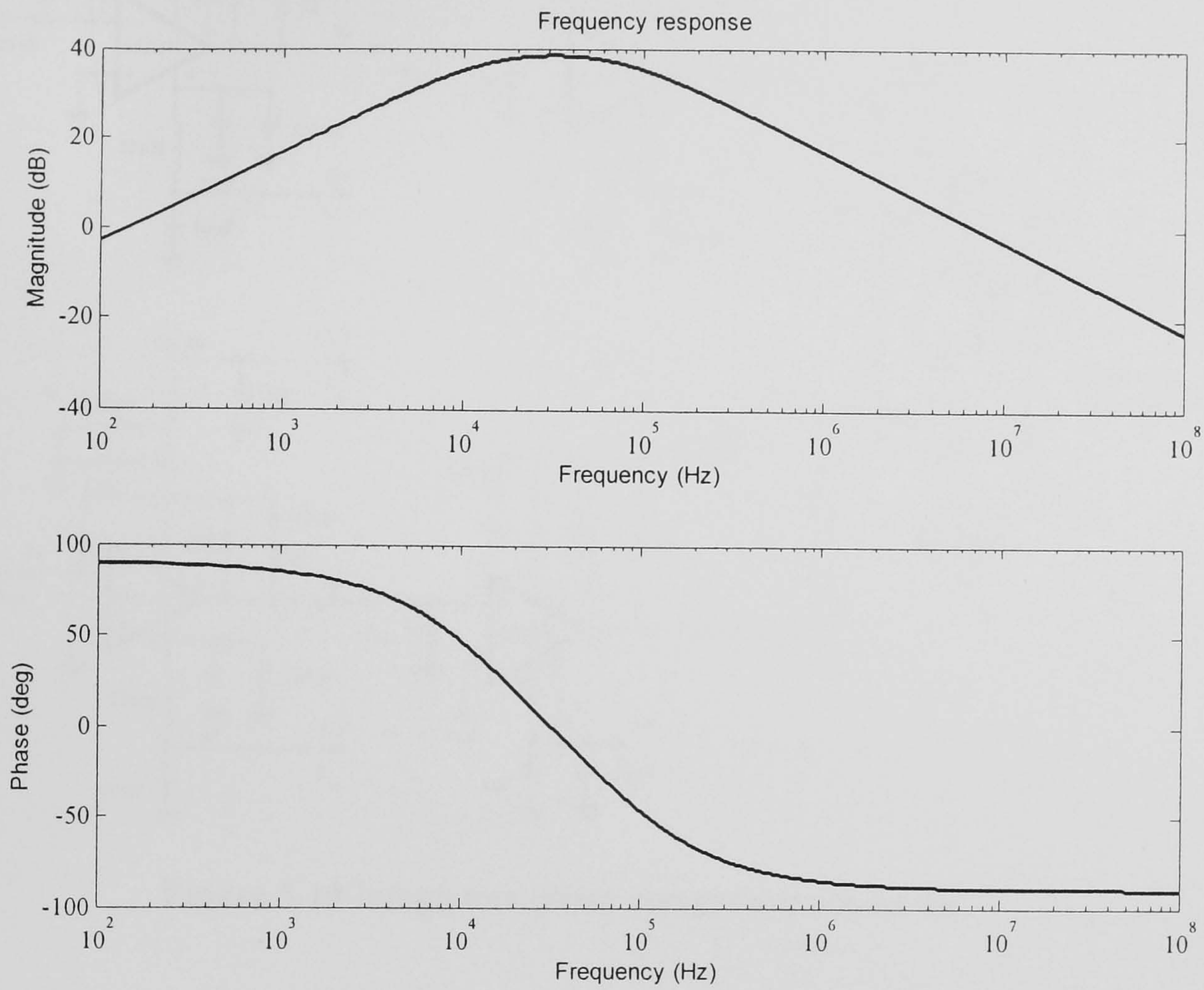


Figure 5.18 Frequency response of the integrator.

The jitter reduction circuit employs LM7171BIN, a 200 MHz gain-bandwidth product op-amp, as integrators. A 22 ohm resistor is put in series with the integrating capacitor in order to equalise phase shift due to the nondominant poles of the op-amp.

Phase comparator 3 [5.18], is a positive edge-triggered sequential phase comparator, using the 74HC4046A high speed CMOS PLL (phase-locked loop) integrated circuit. The schematic of the integrator-comparator part is shown in Figure 5.19. A prototype jitter reduction circuit as detailed in Figure 5.16 and 5.19 was fabricated on the Oxtek™ high frequency prototype board [5.19]. Figure 5.20 shows a fabricated jitter reduction circuit.

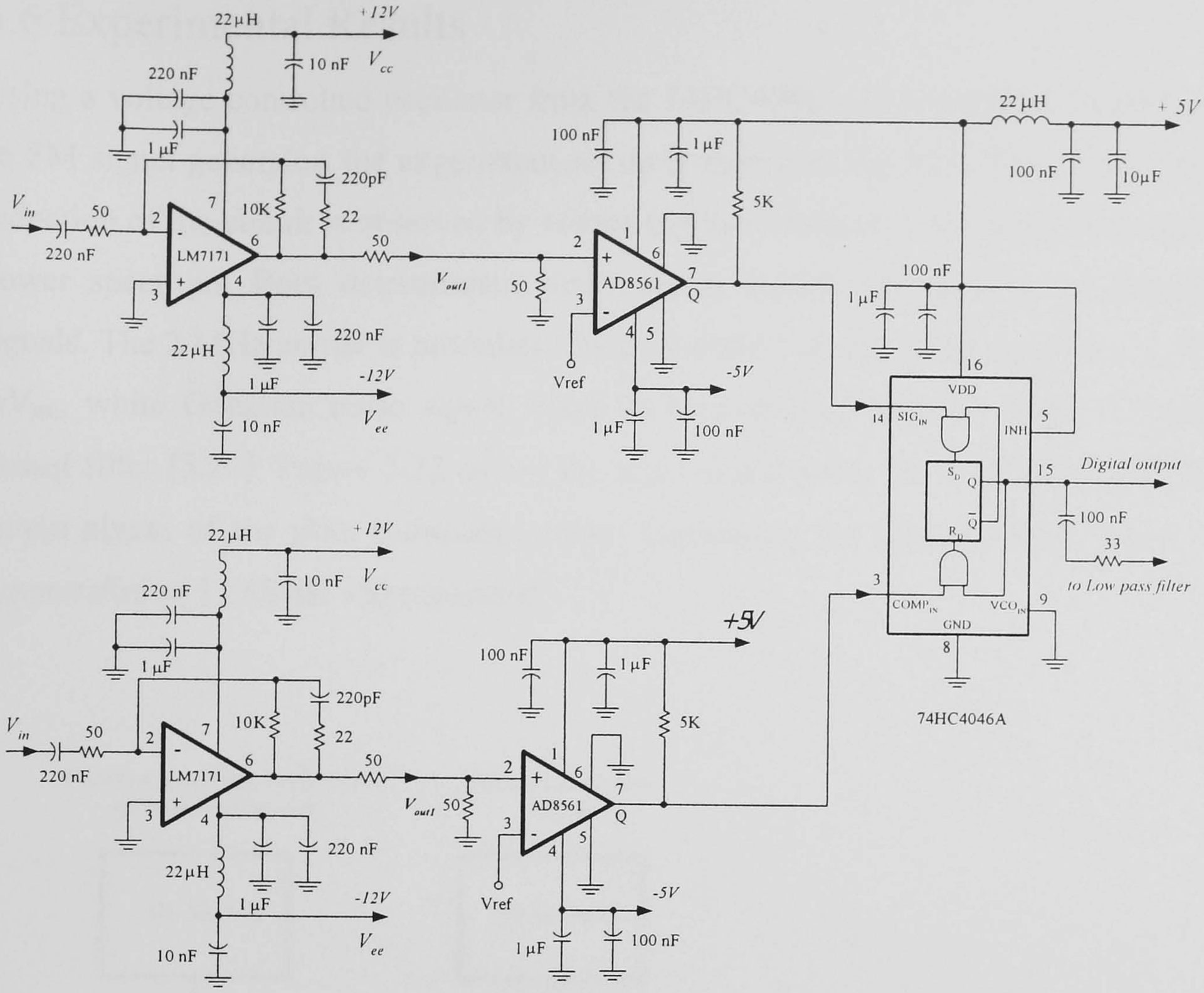
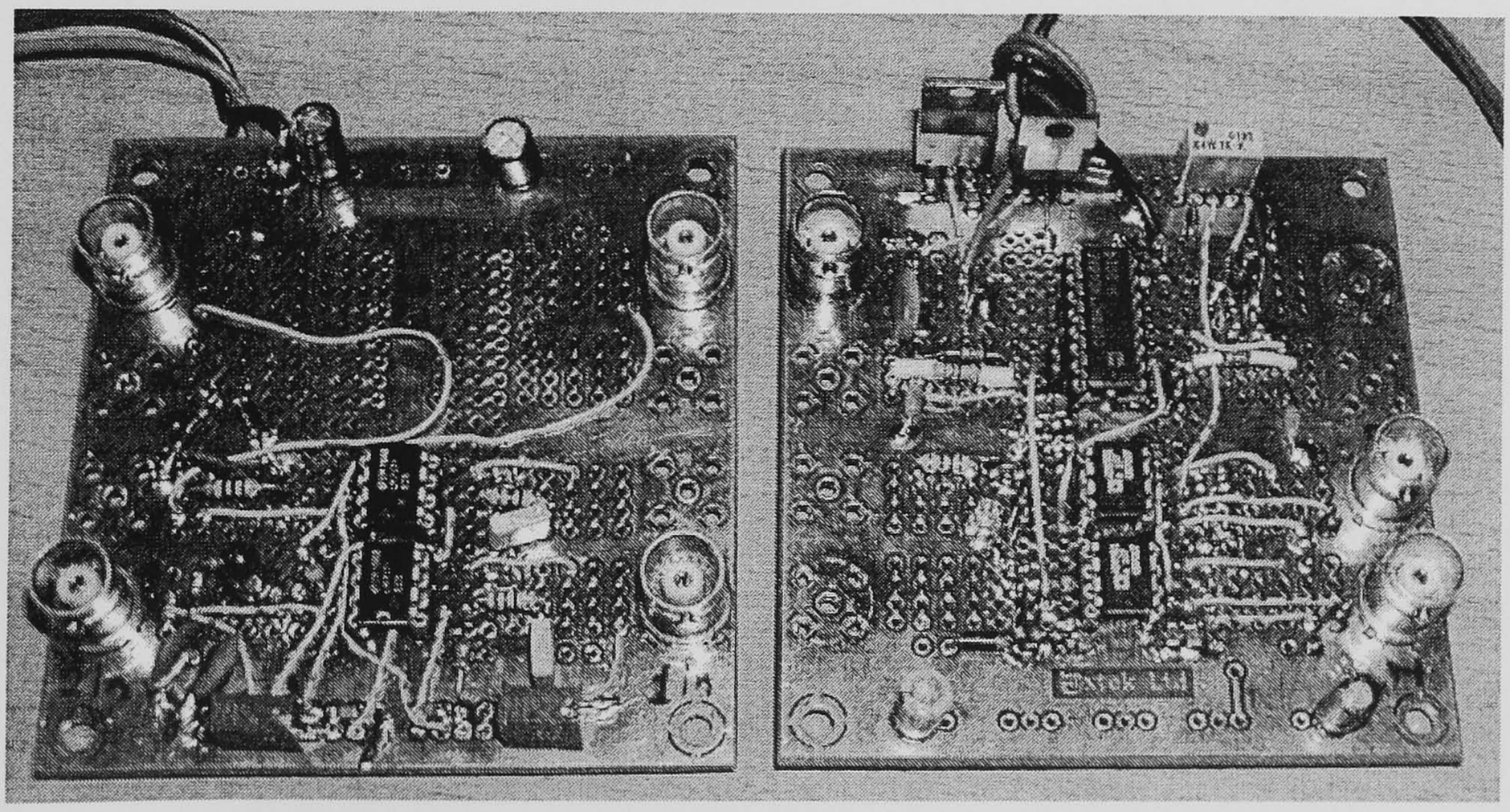


Figure 5.19 Integrators-phase comparator schematic.



Integrators Phase comparator

Figure 5.20 Experimental jitter reduction circuit.

5.6 Experimental Results

Using a voltage controlled oscillator from the 74HC4046A PLL integrated circuit as an FM signal generator, the experiment set up is shown in Fig 5.21. The timing jitter reduction of the circuit is observed by comparing the sideband of the input and output power spectrum. Both deterministic and random signals are used as modulating signals. The 2 MHz carrier is modulated by a 50-400 KHz sinusoidal signal and a 280 mV_{rms} white Gaussian noise signal which is band limited by a 10 MHz 7^{th} order Bessel filter [5.20]. Figure 5.22 shows the input signal when *fm* = 300 KHz and the output signal of the jitter reduction circuit. Comparing the first sideband power, a suppression of 11.68 dB was measured.

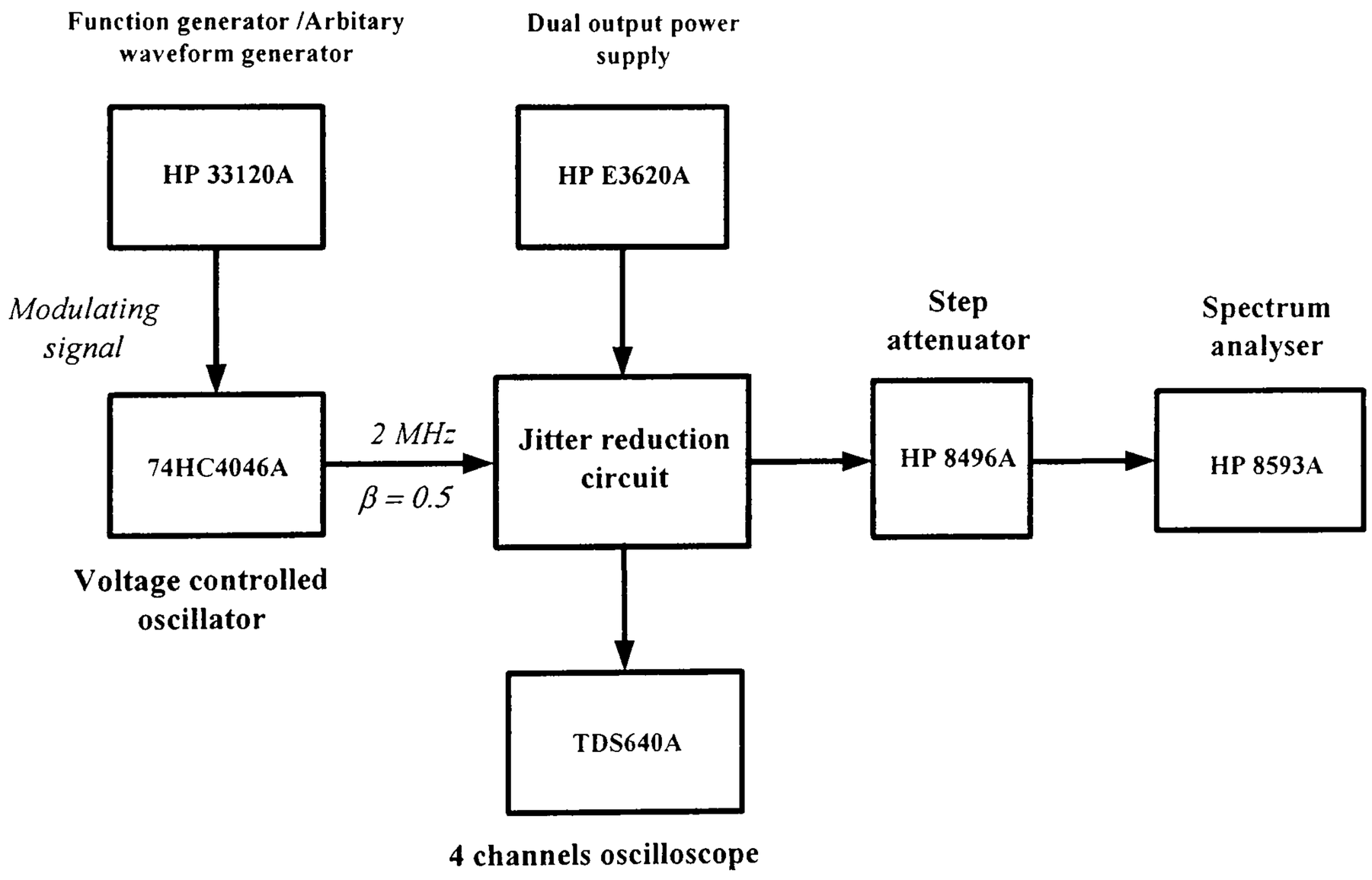
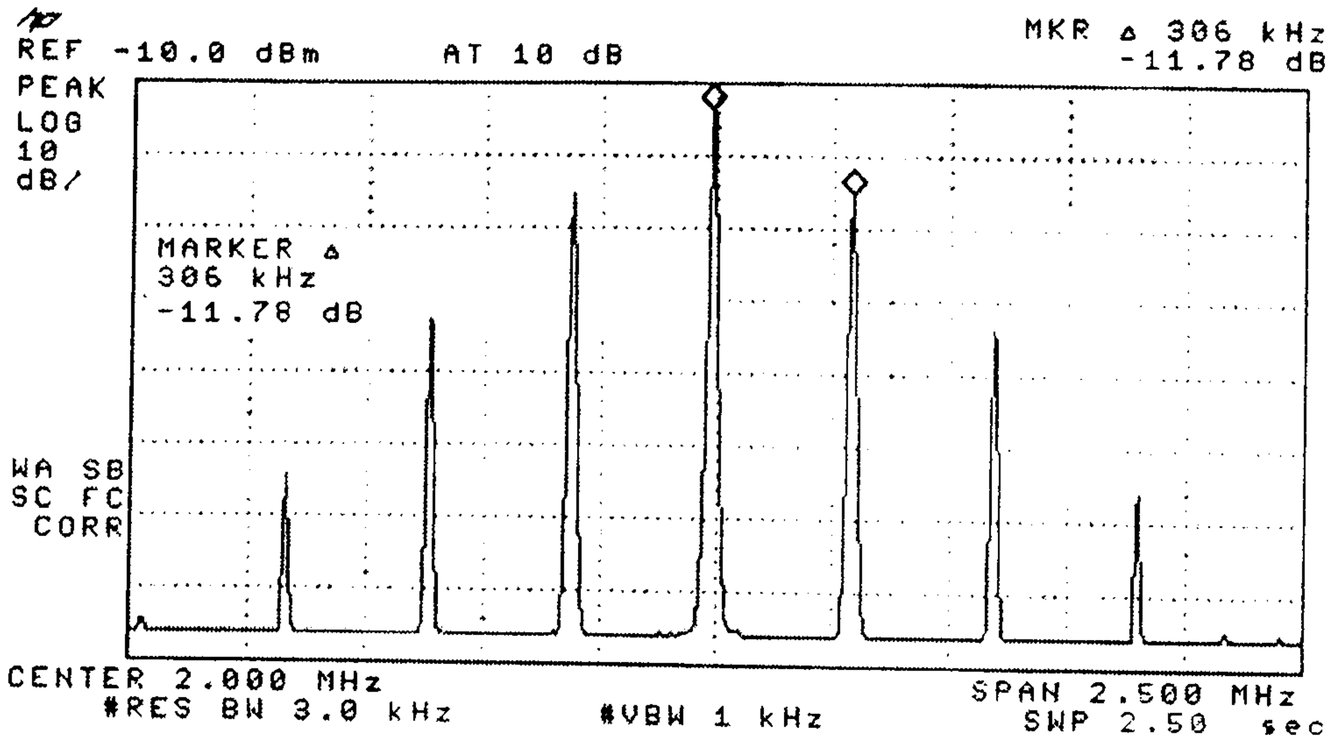
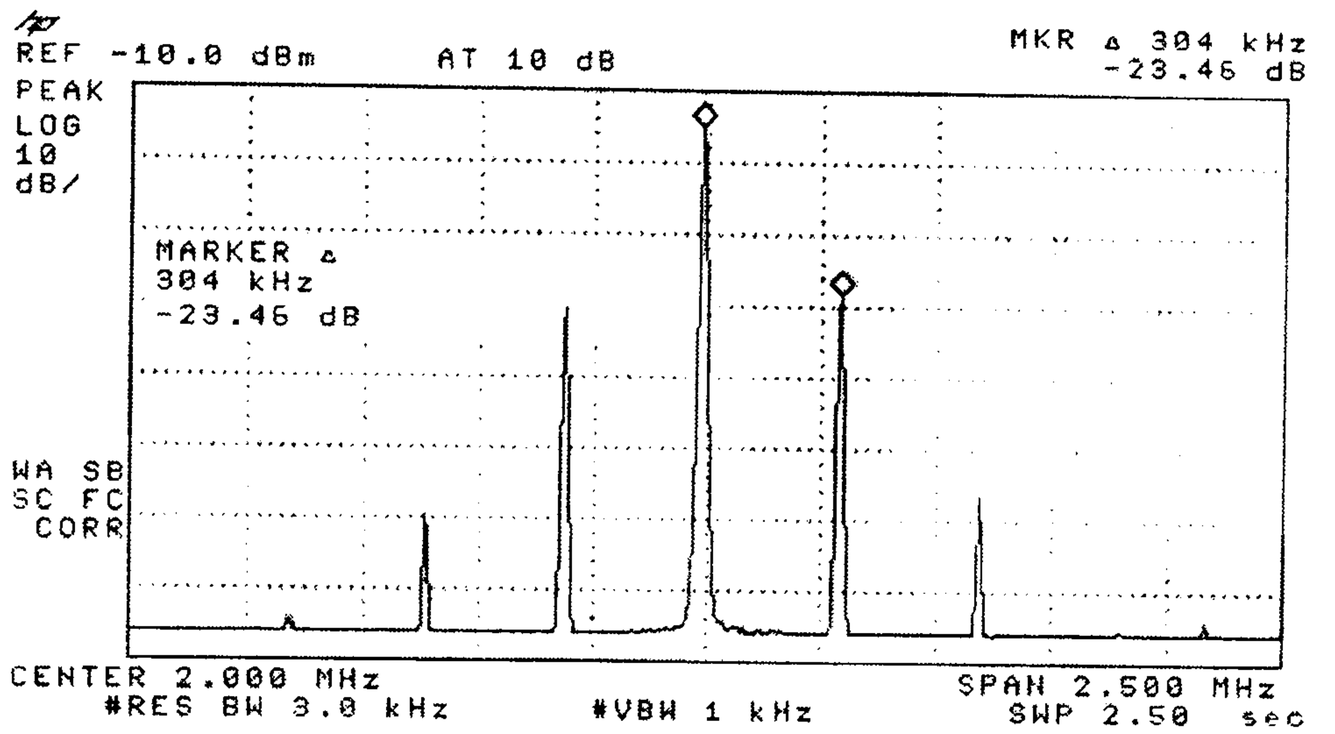


Figure 5.21 Jitter reduction circuit experiment set up.



(a)



(b)

Figure 5.22 (a) Input power spectrum of the experimental jitter reduction circuit compare to the output power spectrum (b).

The measurement result of the spectrum of the input-output signal when the carrier is modulated by white Gaussian noise is shown in Figure 5.23. Due to the lower sideband noise of the second harmonic of the output signal, the output signal shows a somewhat asymmetric power spectrum. This small asymmetrical sideband is not relevant to the jitter suppression performance. The second harmonic is greatly reduced if the 50 percent duty cycle is maintained. Figure 5.24 shows the simulated sideband suppression and the measured sideband suppression of the jitter reduction circuit. As can be seen, the jitter reduction circuit has the response of first a order low pass filter to the sideband noise power. The experimental results in the time domain are shown

in Figure 5.25. Figure 5.25 (a) is a Q signal of the phase splitter circuit and Figure 5.25 (b) is a phase comparator output voltage. Timing jitter in the input signal is reduced from 54 ns_{p-p} to 22 ns_{p-p} as shown in Figure 5.25 (b).

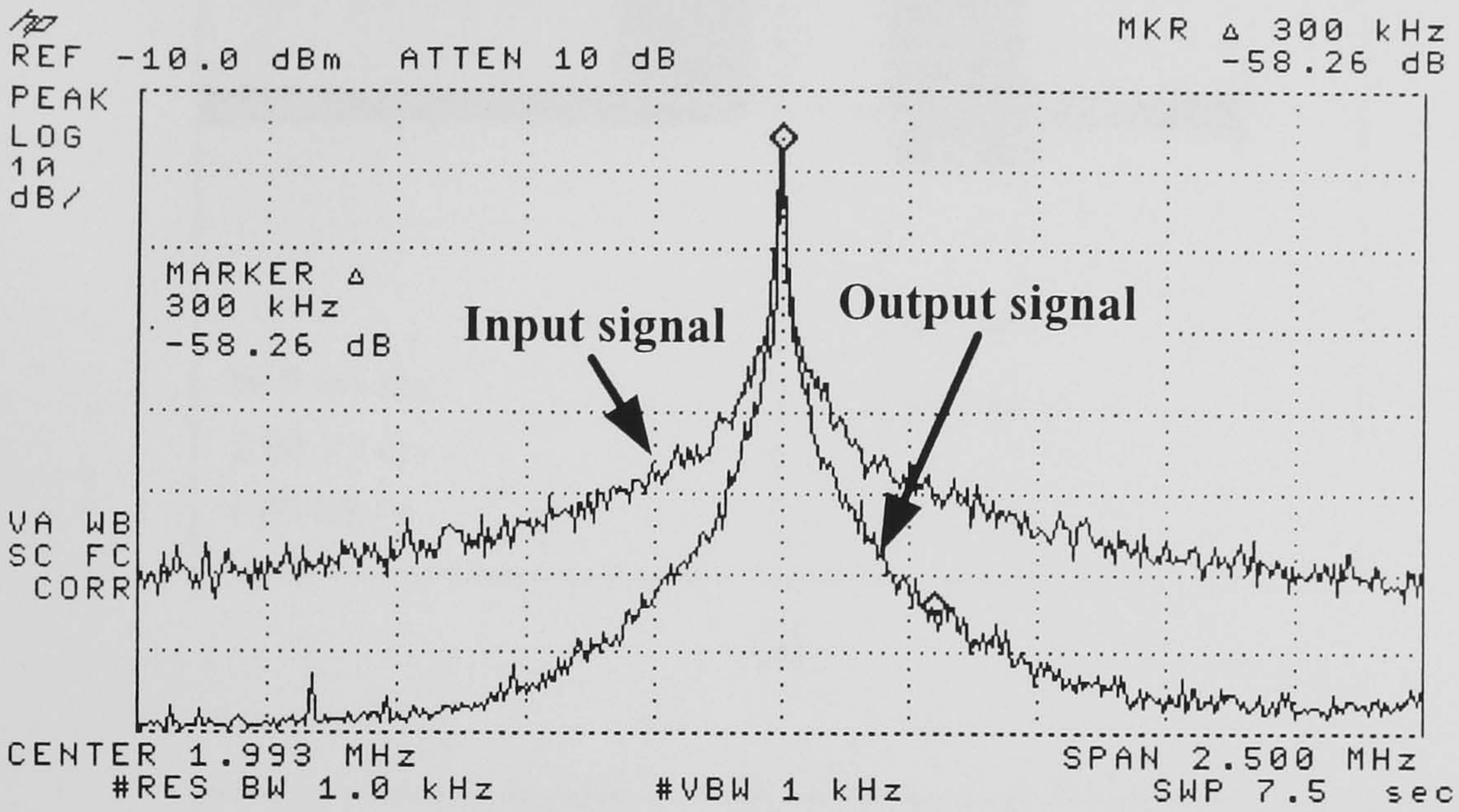


Figure 5.23 Measured input and output signal spectrum of the noise modulated carrier.

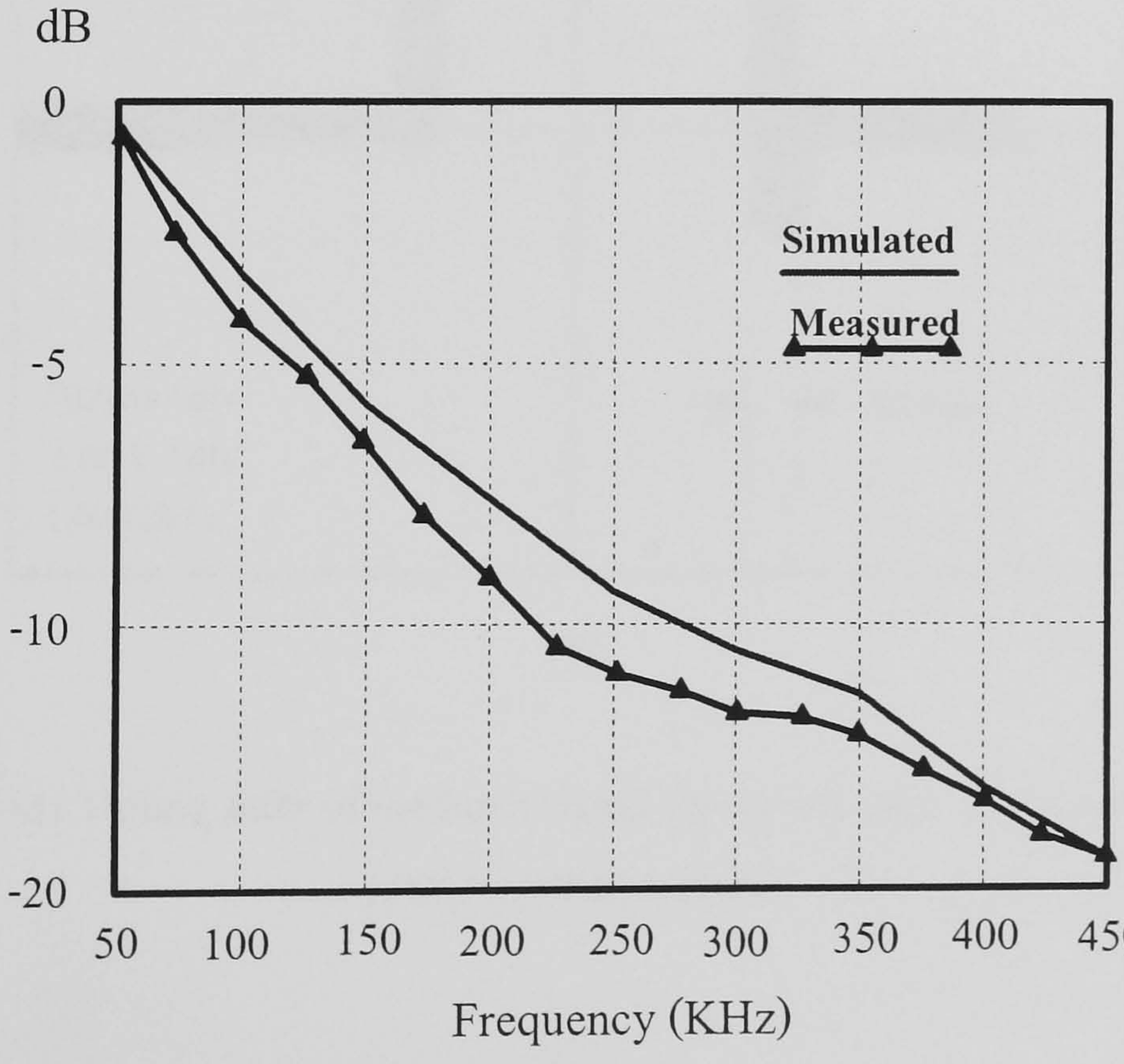
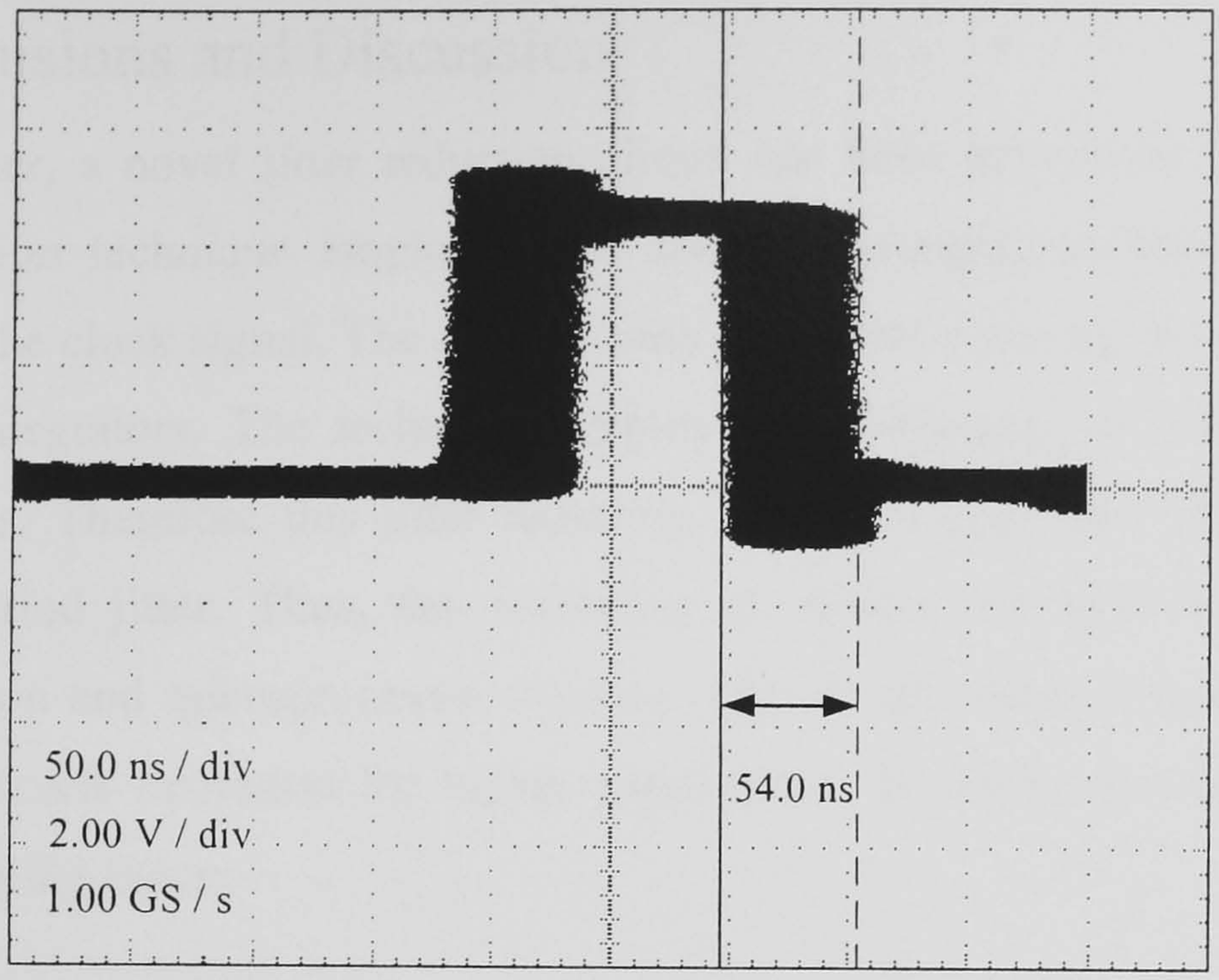
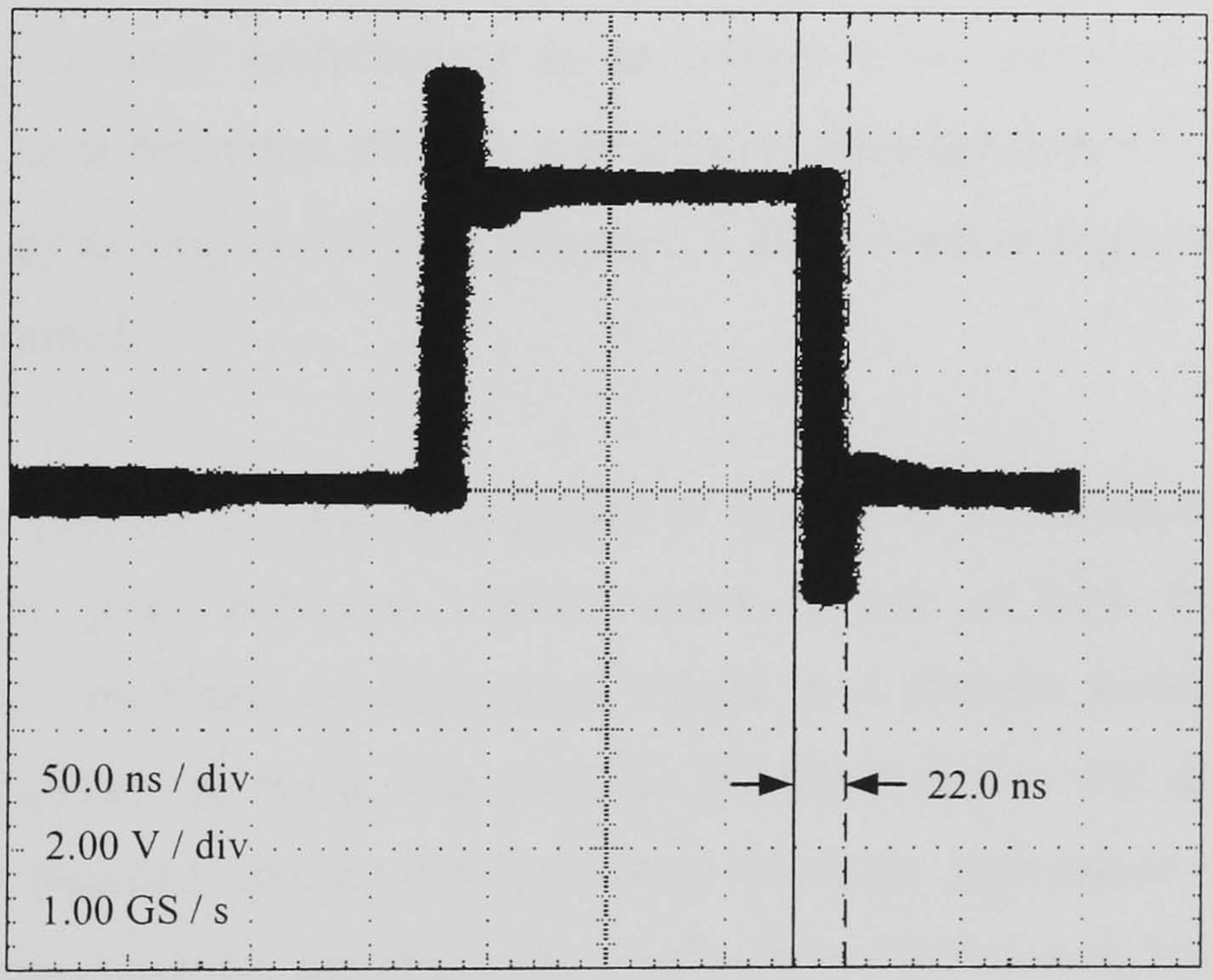


Figure 5.24 Comparison of the simulated phase noise suppression and the measured phase noise suppression.



(a)



(b)

Figure 5.25 (a) Timing jitter of the input signal (b) timing jitter of the output signal of jitter reduction circuit.

5.7 Conclusions and Discussion

In this chapter, a novel jitter reduction circuit has been introduced. This sideband noise reduction technique employs time domain averaging to reduce the timing variation of the clock signal. The discrete time at the zero crossing instant is averaged by analog integrators. The technique employs the averaging on both leading and trailing edges. Therefore this jitter reduction technique can cope with both timing jitter and period jitter. Thus, this technique is suitable for both high speed data communication and microprocessor systems. The circuit structure and its simplicity allow the cascade operation for higher suppression. However, the noise floor is a principal limiting factor.

Practical integrators for the jitter reduction circuit are shown and the constraint of using ideal or high DC gain integrator is pointed out. An active inductor-capacitor resonator shows good performance as an integrator for practical jitter reduction circuits. The jitter reduction circuit's performance does not depend on the integrator circuit topology as long as the ideal response, 6 dB per octave and constant 90° phase shift, is maintained.

Although the prototype circuit is designed to operate at low frequency, it does not mean that the jitter reduction circuit cannot operate at high frequencies. The implementation problems of high speed circuit in a discrete fashion are parasitic element and switching noise. The parasitic inductors due to the devices lead and bonding wire building up considerable voltage when the high speed signal current is flown. This phenomenon can cause the comparators operation to fail, thus the jitter reduction circuit fails to operate.

During this research, the jitter reduction circuit's building blocks were studied, designed and simulated at the transistor level based on the present circuit and the available technologies [5.21-5.23]. Most of the studied circuits show promising capabilities. Based on this knowledge, high frequency operation of the jitter reduction circuit is possible in the integrated circuit form.

Chapter 6

Conclusions

Phase noise and the timing jitter are fundamental properties of the signal sources. The sideband and phase noise of the carrier signal generator is of critical concern in communication and timing systems. Rapidly increasing data transmission rates and tighter timing margins are creating a need for lower jitter clock signal. In some cases, the sideband noise levels of the carrier or clock recovery circuits are above system demands and phase noise reduction techniques must be applied. The current techniques for phase noise reduction are mentioned in section 2.4. The key comparison criteria are system complexity, noise reduction bandwidth, operating frequency range, applicability and system stability. Unfortunately, none of the techniques possess all of these abilities.

Two phase noise and jitter reduction techniques have been adopted in this research, they are transposed gain oscillators and the time domain sideband noise reduction techniques. Both of the sideband noise reduction techniques have distinctive characters. In theory, the transposed gain oscillator can achieve the sideband noise suppression ratio down to the oscillator's noise floor. A noisy oscillator can be used as a local oscillator or a primary oscillator of the transposed gain oscillator. The limitation of the local oscillator's sideband suppression in principle is the group delay mismatch between the LO-IF signal paths. The group delay mismatch effect and LO's sideband noise suppression capability have been analysed and investigated by experiments [6.1-6.2]. Since the transposed gain techniques mostly use the double balance mixer, the noise modulation sensitivity of the transposed gain oscillator depends on the IF amplifiers. Moreover, the IF signal imbalance gives rise to the LO signal leakage. This poses a big problem in the low Q oscillator since the leakage LO is closer to the needed output sideband than the unwanted sideband. In chapter 4, it has been shown that balance amplification can solve this problem. The LP-TGA or the low pass response transposed gain amplifier is also introduced. The LP-TGA employs two RF amplifiers in the IF and LO signal paths, which have the same RF

character, thus it is supposed to give no delay mismatch difficulty. In theory, the LP-TGA driven transposed gain oscillator can give LO sideband noise suppression down to the circuit noise floor without the delay problem.

The novel jitter reduction techniques introduced in this thesis are based on time domain jitter averaging principle. Depending on the jitter problem, the equivalent noise voltage and phase noise model are often used. The equivalent noise model considers the jittering clock as a perfect clock with noise voltage added to it and the phase noise model considers the jittering clock as a clock signal whose phase is modulated by noise. However, these two models provide the same amount of timing jitter [6.3]. The novel jitter reduction circuit is developed to reduce the equivalent noise voltage, and thus phase noise of the clock signal. The variation of the zero crossing of the clock signal due to phase jitter is averaged by analog integrators. The novel jitter reduction circuit's performance does not depend on the integrator circuit topology as long as the ideal response, 6 dB per octave and constant 90° phase shift, is maintained. The sideband noise is suppressed at a rate of 6dB per octave of the offset frequency [6.4-6.5]. The novel jitter reduction circuit is simple which can be applied to a signal path as a drop-in building block and the structure of the circuit is cascadable for higher sideband noise suppression.

6.1 Suggestions for Future Work

Having researched the circuits for the phase noise and timing jitter reduction, there are promising techniques which need further investigation. The following are suggestions for possible phase noise reduction schemes.

6.1.1 Sideband Noise Reduction by Harmonics Mixing

From the analysis of sideband noise reduction mechanism of the transposed gain oscillator in Chapter 4, it was found that the convolution process of the LO and IF signals which have the same modulation index make sideband noise suppression possible. However, the output signal has a frequency different from the LO frequency.

If we can generate, or more precisely, estimate the second harmonic which has the same noise distribution or modulation index of the input signal and multiply it with

the input signal we will get two mixing products one of which is the same as input frequency but the sideband noise is removed. This scheme is depicted in Figure 6.1.

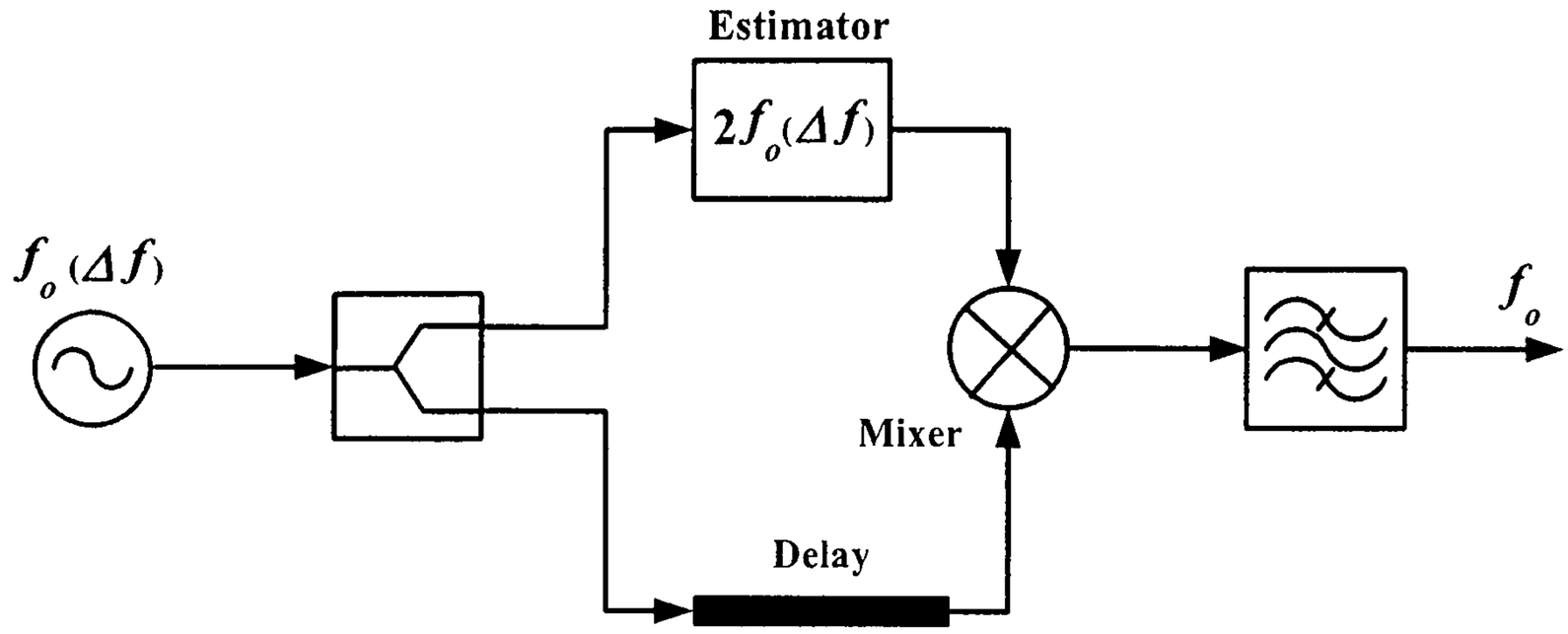


Figure 6.1 Harmonic mixing sideband noise suppression.

The big challenge is the harmonic generator or estimator because we cannot use the conventional frequency multiplier to perform this function. The modulation index or sideband noise distribution is also multiplied if the conventional frequency multiplier is utilized. However, it is possible to generate the second harmonic signal with the modulation index of the input signal is retained. For example, the modulation index or sideband noise distribution of the jitter reduction circuit output signal is not multiplied by the harmonic number.

6.1.2 Modified Transposed Gain Oscillator

Normally, the output frequency of the transposed gain oscillator is different from the LO frequency by the IF frequency. If the resonant frequency of the RF parts is stabilized at a third harmonic of the LO frequency, then the IF frequency is a second harmonic of the LO signal and has the same sideband characteristic. Thus, the transposed gain oscillator can also be used as an estimator for $2f_o(\Delta f)$ that shown in Figure 6.1. Figure 6.2 shows the proposed modified transposed gain oscillator.

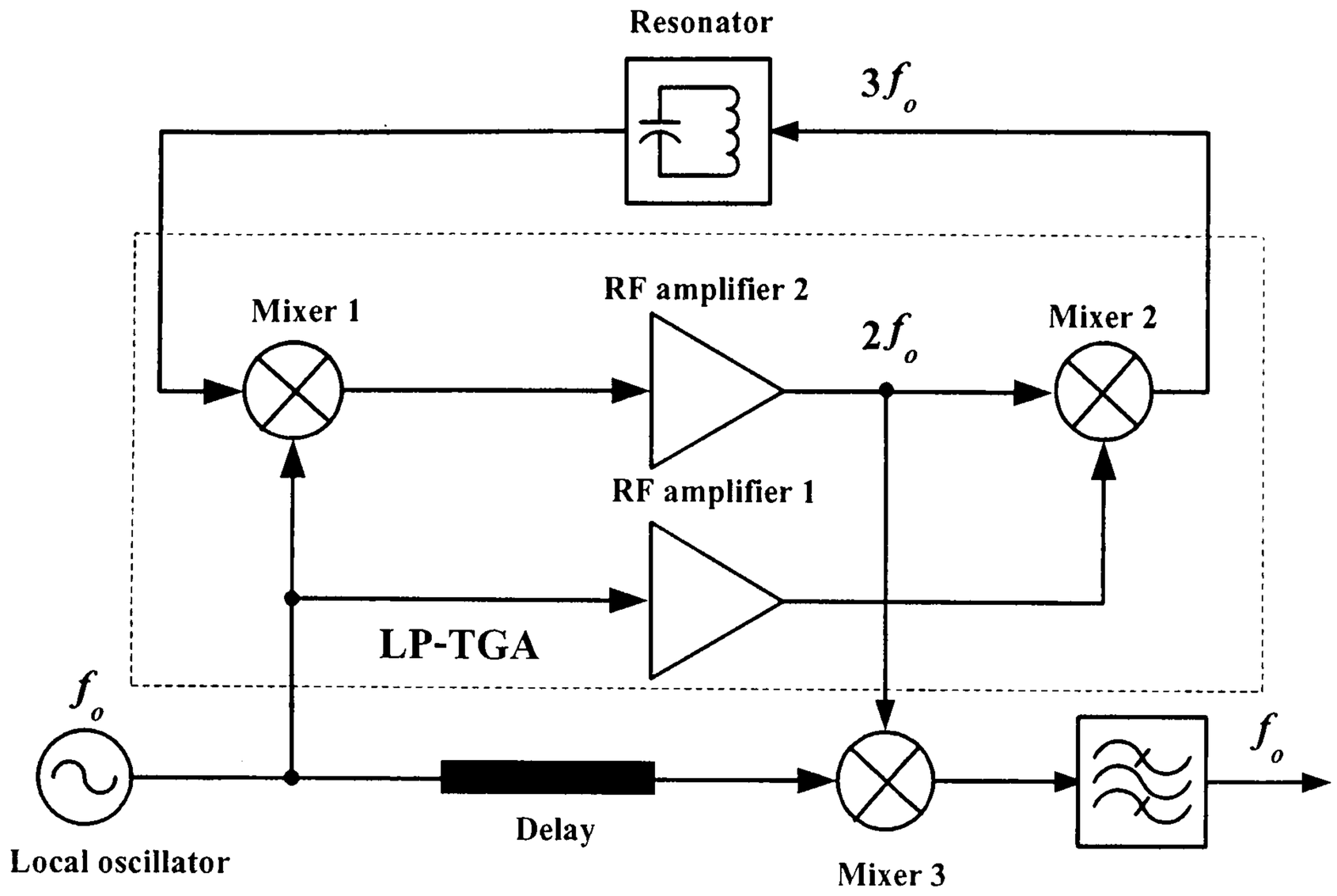


Figure 6.2 Sideband noise suppression using modified transposed gain oscillator.

6.1.3 Harmonic Injection Locking Oscillator

The injection locking oscillator can be used as a sideband noise reduction circuit. This phenomenon was found during the research on the jitter reduction circuit. If the injection locking oscillator is injected by the second harmonic of its free running frequency, the second harmonic of the output frequency is the same as injected frequency but the sideband noise is reduced. Figure 6.3 shows the block diagram of the sideband noise reduction using injection locking oscillator. The time domain simulation result of the circuit is shown in Figure 6.4. The free running frequency of the oscillator is 1 MHz and the injected signal is a 2 MHz FM signal with a modulation index of 0.5 and the modulating signal is equal to 200 KHz. It can be seen that the first sideband is suppressed by 17.12 dB. Comparing to the sideband suppression of the novel jitter reduction circuit at 200KHz offset frequency in Figure 5.24, the harmonic injection locking oscillator give more than 10 dB higher suppression ratio.

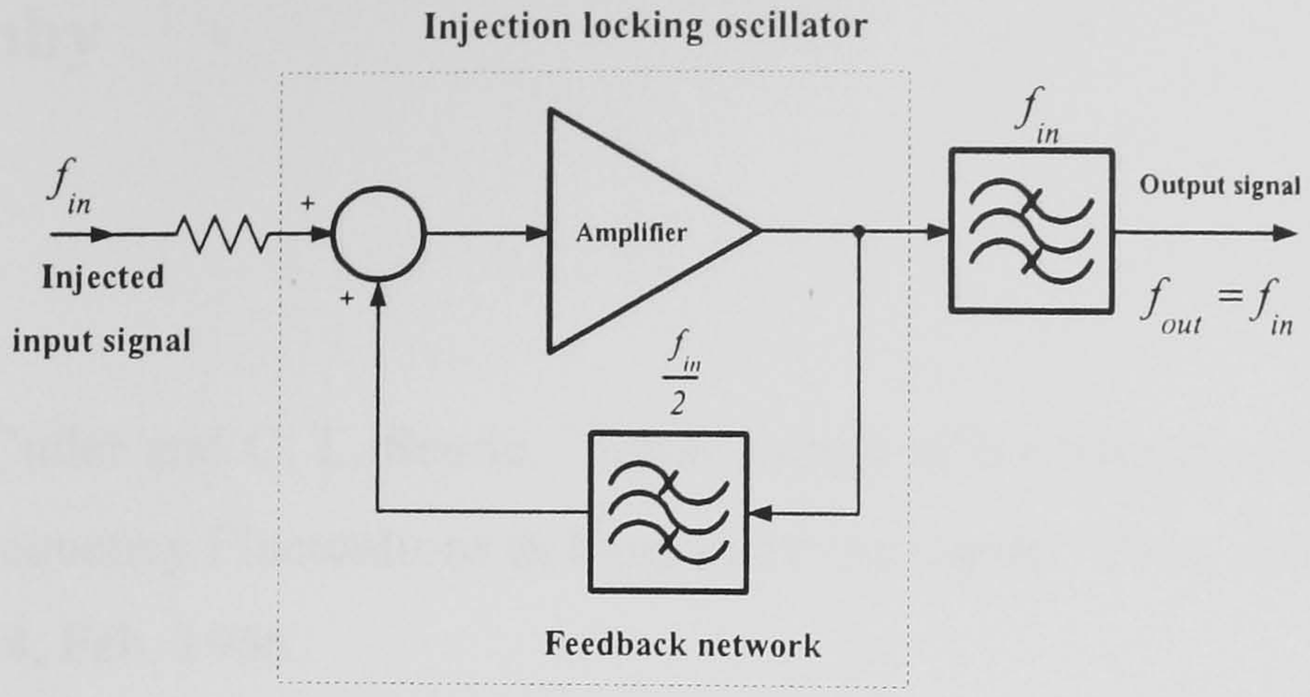


Figure 6.3 Sideband noise suppression using injection locking oscillator.

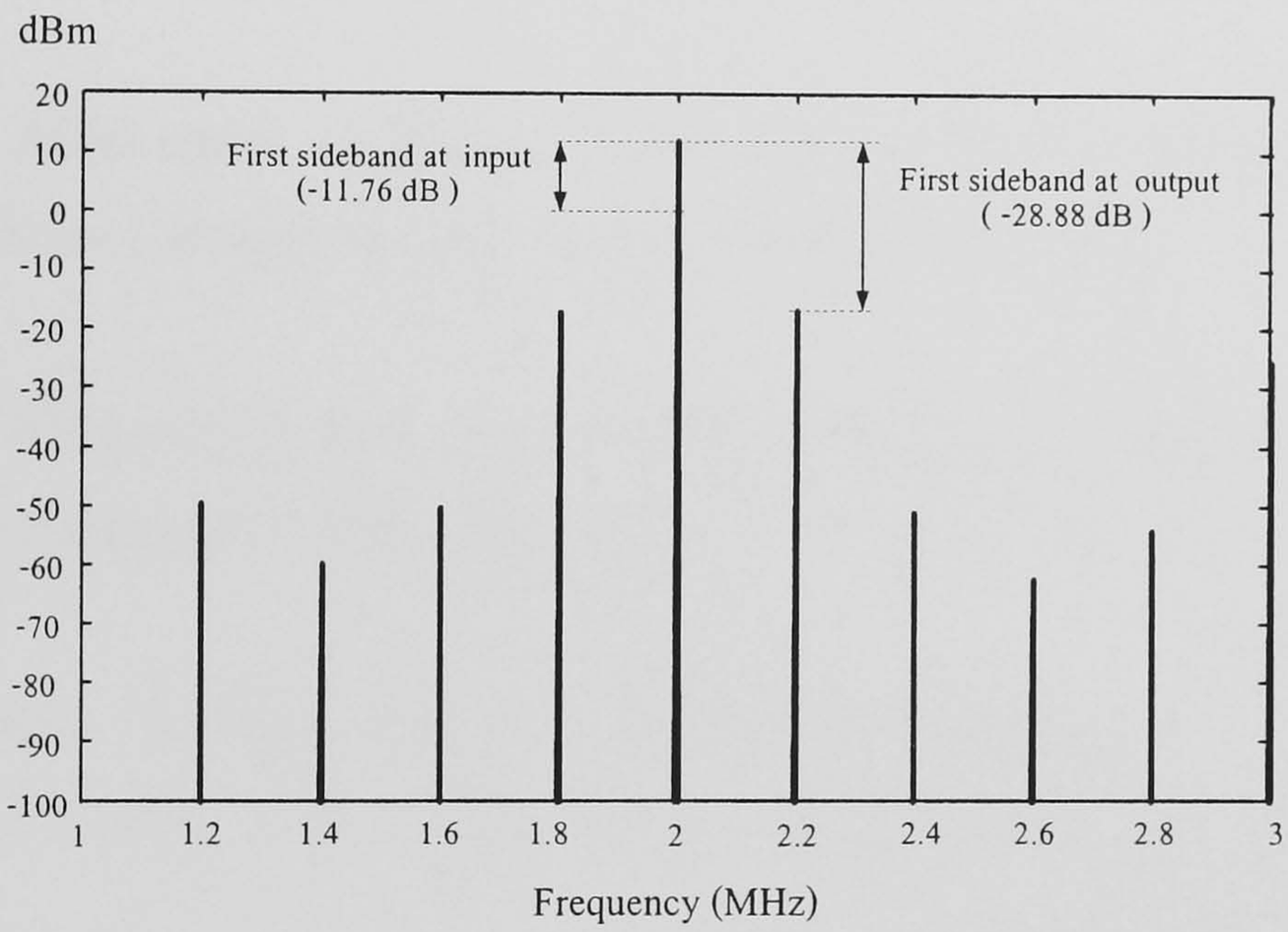


Figure 6.4 Simulated sideband noise suppression of the injection locking oscillator.

Having described the potential future work, it is possible to use these techniques as a practical sideband noise suppression circuit. However, considerable further study and extensive experiments are required before the technique is employed as a usable circuit and operated with confidence.

Bibliography

Chapter 1

[1.1] L. S. Cutler and C. L. Searle, "Some Aspect of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," *Proc. IEEE*, vol. 54, pp. 136-154, Feb. 1966.

[1.2] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proc. IEEE*, vol. 54, pp. 329-330, Feb. 1966.

[1.3] A. A. Abidi and R. G. Meyer, "Noise in Relaxation Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 794-802, Dec. 1983.

[1.4] T. C. Weigandt, B. Kim and P. R. Gray, "Analysis of Timing Jitter in CMOS Ring Oscillators," *Proc. ISCAS*, Jun. 1994.

[1.5] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-31, pp. 331-343, March 1996.

[1.6] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-33, pp. 179-194, Feb. 1998.

[1.7] Q. Huang, "Phase Noise to Carrier Ratio in LC Oscillators," *IEEE Trans. Circuits Syst.-I*, vol.47, No.7 pp. 965-980, July 2000.

[1.8] T. H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial," *IEEE J. Solid- State Circuits*, vol. SC-35, No. 3, pp. 326-336, Feb. 1998.

[1.9] A. Demir, A. Mehrotra and J. Roychowdhury, " Phase Noise in Oscillators: An-Unifying Theory and Numerical Methods for Characterization, " *IEEE Trans. Circuits Syst.-I*, vol.47, No.5 pp. 655-674, May 2000.

Chapter 2

[2.1] Q. Huang, " Phase Noise to Carrier Ratio in LC Oscillators, " *IEEE Trans. Circuits Syst.-I*, vol.47, No.7 pp. 965-980, July 2000.

[2.2] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*, Boston, MA: Kluwar Academic Publisher, 2000.

[2.3] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proc. IEEE*, vol. 54, pp. 329-330, Feb. 1966.

[2.4] L. S. Cutler and C. L. Searle, "Some Aspect of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," *Proc. IEEE*, vol. 54, pp. 136-154, Feb. 1966.

[2.5] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-31, pp. 331-343, March 1996.

[2.6] J. Craninckx and M. Steyaert, "Low-noise Voltage Controlled Oscillators Using Enhanced LC-Tanks," *IEEE Trans. Circuits Syst.-II*, vol.42, pp. 794-904, Dec. 1995.

[2.7] A. A. Abidi, "How Phase Noise Appears in Oscillators," *Analog Circuit Design-RF Analog to Digital Converters; Sensor and Actuator Interfaces; Low-Noise Oscillators, PLLs and Synthesizers,* Boston, MA: Kluwar Academic Publisher, 1997.

[2.8] R. G. Meyer, *Phase Noise in LC Oscillators*, EECS Class Note, University of California, Berkeley.

[2.9] W. P. Robins, *Phase Noise in Signal Sources*, Peter Peregrinus Ltd., London, 1982.

[2.10] J. K. A. Everard, "Low Noise Oscillators," *Proceedings of IEEE/MTT-S*, pp. 1077-1080, 1992.

[2.11] M. J. Underhill, "Reduction of Phase Noise in Single Transistor Oscillators," *Proc. EFTF*, pp. 476-490, 1996.

[2.12] J. K. A. Everard, *Fundamentals of RF Circuit Design*, Chichester, UK: John-Wiley & Sons, 2001.

[2.13] M. C. Delgado Aramburo, et al., "Comparison of 1/f PM Noise in Commercial amplifiers," *Proc. IEEE Freq. Contr. Symp.*, pp. 470-477, 1997.

[2.14] A. Momtaz, et al., "A Fully Integrated SONET OC-48 Transceiver in Standard CMOS," *IEEE J. Solid-State Circuits*, vol. SC-36, pp. 1964-1973, Dec. 2001.

[2.15] T. H. Lee and A. Hajimiri, "Ocillator Phase Noise: A Tutorial," *IEEE J. Solid-State Circuits*, vol. SC-35, No. 3, pp. 326-336, Feb. 1998.

[2.16] F. L. Walls, E. S. Ferre-Pikal and S. R. Jefferts, "The Origin of 1/f PM and AM Noise in Bipolar Junction Transistor Amplifiers," *Proc. IEEE Freq. Contr. Symp.*, pp. 294-304, 1995.

[2.17] C. McNeilage, et al., "Review of Feedback and Feedforward Noise Reduction Techniques," *Proc. IEEE Freq. Contr. Symp.*, pp. 146-155, 1998.

[2.18] M. M. Driscoll and R. W. Weinert, "Spectral Performance of Sapphire Dielectric Resonator-Controlled Oscillators Operating in the 80K to 275K Temperature Range," *Proc. IEEE Freq. Contr. Symp.*, pp. 401-412, 1995.

[2.19] E. N. Ivanov, M. E. Tobar, R. A. Woode, "Ultra Low Noise Microwave Oscillator with Advanced Phase Noise Suppression System," *IEEE Microwave and Guided Waves Letters Vol.6, No. 9*, pp. 312-314, 1996.

[2.20] E. N. Ivanov, M. E. Tobar, R. A. Woode, "Tunable Microwave Oscillator for Low Phase Noise Applications," *Proc. IEEE Freq. Contr. Symp.*, pp. 985-993, 1997.

[2.21] J. K. A. Everard and C. D. Broomfield, "Transposed Flicker Noise Suppression in Microwave Oscillators Using Feedforward Amplifiers," *IEE Electronics Letters*, 26, No. 20 pp. 1710-1711, Sept. 2000.

[2.22] M. J. Underhill and M. J. Blewett, "Spectral Improvement of Direct Digital Frequency Synthesisers and Other Frequency Sources," *Proc. 10th EFTF*, Brighton, pp. 452-460, March 1996.

[2.23] M. J. Underhill and M. J. Blewett, "Performance of a Delay Compensation Phase Noise and Time Jitter Reduction Method," *Proc. 11th EFTF*, Neuchatel, pp. 364-368, March 1997.

[2.24] M. J. Underhill, "Phase Noise Limits of the Anti-Jitter Circuit and On-Chip RC Oscillators," *Proc. 14th EFTF*, Torino, March 2000.

[2.25] Z. Galani, et al., "Analysis and Design of a Single-Resonator GaAsFET Oscillator with Noise Degeneration," *IEEE Transaction on Microwave Theory and Techniques, vol. 32, No.12*, pp. 1556-1565, Apr. 1984.

[2.26] D. P. Tsarapkin, V. S. Komarov, "Stable Microwave Oscillator with Combine Stabilization," *Proc. Moscow Power Eng. Instit.*, Issue 51 pp. 82-86, 1973.

[2.27] M. J. Underhill, "The Adiabatic Anti-Jitter Circuit," *IEEE Transaction on Ultrasonics, Ferroelectrics and Frequency Control, vol. 48, No.3*, pp. 666-674, May 2001.

[2.28] M. J. Underhill, "The Noise and Suppression Transfer Functions of the Anti-Jitter Circuit," *Proc. IEEE Freq. Contr. Symp.*, pp. 490-498, May 2003.

Chapter 3

[3.1] C. McNeilage, et al., "Review of Feedback and Feedforward Noise Reduction Techniques," *Proc. IEEE Freq. Contr. Symp.*, pp. 146-155, 1998.

[3.2] J. K. A. Everard and M. A. Page-Jones, "Transposed Gain Microwave Oscillators with Low Phase Residual Flicker Noise," *Proc. IEEE Freq. Contr. Symp.*, pp. 374-378, 1995.

[3.3] M. M. Driscoll and R. W. Weinert, "Spectral Performance of Sapphire Dielectric Resonator-Controlled Oscillators Operating in The 80K to 275K Temperature Range," *Proc. IEEE Freq. Contr. Symp.*, pp. 401-412, 1995.

[3.4] M. A. Page-Jones and J. K. A. Everard, "Enhanced Transposed Gain Microwave Oscillators," *Proc. 10th EFTF*, Brighton, pp. 275-278, March 1996.

[3.5] R. J. Besson, et al., "Phase Noise Figures Comparison in Transistor Amplifiers of Different Types," *Proc. 10th EFTF*, Brighton, pp. 447-451, March 1996.

[3.6] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-33, pp. 179-194, Feb. 1998.

[3.7] J. E. Post, Jr., I. R. Linscott and M. H. Oslick, "Waveform Symmetry Properties and Phase Noise in Oscillators," *Electronics Letters*, vol. 34, Aug. 1998.

[3.8] K. A. Stroud, *Fourier Series and Harmonic Analysis*, Leckhampton, UK: Stanley Thornes Publishers, 1984.

[3.9] K. W. Kobayashi. et al., , "InAiAs/InGaAs HBT X-band Bouble-balanced Upconverter," *IEEE J. Solid-State Circuits*, vol. SC-29, pp. 179-194, Oct. 1994.

[3.10] K. W. Kobayashi. et al., , "A 5-10 GHz Octave-band AlGaAs/GaAs HBT-Schottky Diode Dow-converter MMIC," *IEEE J. Solid-State Circuits*, vol. SC-31, pp. 1412-1418, Oct. 1996.

[3.11] B. Razavi, *RF Microelectronics*, New Jersey: Prentice Hall, 1998.

[3.12] F. L. Walls, E. S. Ferre-Pikal and S. R. Jefferts, "The Origin of 1/f PM and AM Noise in Bipolar Junction Transistor Amplifiers," *Proc. IEEE Freq. Contr. Symp.*, pp. 294-304, 1995.

[3.13] M. C. Delgado Aramburo, et al., "Comparison of 1/f PM Noise in Commercial Amplifiers," *Proc. IEEE Freq. Contr. Symp.*, pp. 470-477, 1997.

[3.14] W. E. Sabin and E. O. Schoenike, *HF Radio Systems & Circuits*, Atlanta, GA: Noble Publisher, 2000.

[3.15] H. L. Krauss, Charles W. Bostain and F. H. Raab, *Solid State Radio Engineering,* New York: John Wiley & Sons, 1980.

[3.16] R. S. Carson, *High Frequency Amplifiers*, Wiley, 1982.

[3.17] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed, Singapore: John Wiley and Sons, 1993.

[3.18] R. C. Jaeger and G. A. Hellwarth, "On the Performance of the Differential Cascode Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 169-174, Apr. 1973.

[3.19] Data sheet, MMG Neosid Limited, Lectchworth, Hertfordshire.

[3.20] Transistor Model Library, PSPICE v. 9.1, OrCAD Inc. 1999.

[3.21] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed, Upper Saddle River, NJ: Prentice Hall, 1997.

[3.22] I. D. Robertson, Ed., *MMIC Design*, IEE Circuits and Systems serires7, Exeter, UK: Short Run Press, 1995.

[3.23] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, New – York: Cambridge University Press, 2000.

[3.24] J. A. Hall and H. J. Peppiatt, "Microwave Oscillator Having Directional Coupler in Feedback Path," U.S. Patent 4,245,193 May. 1971.

[3.25] J. K. A. Everard, "Low Noise Oscillators," *Proceedings of IEEE/MTT-S*, pp. 1077-1080, 1992.

[3.26] J. K. A. Everard, *Fundamentals of RF Circuit Design*, Chichester, UK: John-Wiley & Sons, 2001.

[3.27] W. E. Sabin and E. O. Schoenike, *HF Radio Systems & Circuits*, Atlanta, GA: Noble Publisher, 2000.

[3.28] P. Kreuzgruber, et al., "Modelling of Three-port RF Transformers," *IEE Proceedings-G*, vol. 138, pp. 325-328, Jun 1991.

[3.29] *RF & Microwave Signal Processing*, Merrimac, West Caldwell, New Jersey, Apr. 1996.

[3.30] G. D. Venderlin, A. M. Pavio and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques,* Singapore: John Wiley & Sons, 1990.

[3.31] *How RF Transformers Work*, Application note, Mini-Circuits Division of Scientific Components, Brooklyn, New York, 2001.

[3.32] K. Stoll, *Double-Aperture transformers for RF Application up to 2.5 GHz*, Siemens Matsushita Components, 2000.

[3.33] J. R. Long, "A low-voltage 5.1-5.8 GHz Image-Rejection Downconverter RFIC," *IEEE J. Solid-State Circuits*, vol. SC-35, pp. 1320-1328, September 2000.

[3.34] G. L. Matthaei, L. Young and E. M. T. Jones, *Microwave Filters, Impedance Matching Networks and Coupling Structures*, Dedham, MA: Artech House Inc., 1980.

Chapter 4

[4.1] Jing-Jong Pan and M. P. Arnold, "High-Q Multi-Mode Resonator Controlled Source," U.S. Patent 4,245,193 Jan. 1981.

[4.2] M. M. Driscoll and R. W. Weinert, "Spectral Performance of Sapphire Dieletric Resonator-Controlled Oscillators Operating in The 80K to 275K Temperature Range," *Proc. IEEE Freq. Contr. Symp.*, pp. 401-412, 1995.

[4.3] J. K. A. Everard and M. A. Page-Jones, "Transposed Gain Microwave Oscillators with Low Phase Residual Flicker Noise," *Proc. IEEE Freq. Contr. Symp.*, pp. 374-378, 1995.

[4.4] J. K. A. Everard and M. A. Page-Jones, "Ultra Low Noise Microwave Oscillators with Low Phase Residual Flicker Noise," *Proc. IEEE International Microwave Symposium*, pp. 693-696, 1995.

[4.5] M. A. Page-Jones and J. K. A. Everard, "Enhanced Transposed Gain Microwave Oscillators," *Proc. 10th EFTF*, Brighton, pp. 275-278, March 1996.

[4.6] H. L. Krauss, Charles W. Bostain and F. H. Raab, *Solid State Radio-Engineering*, New York: John Wiley & Sons, 1980.

[4.7] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*, Boston, MA: Kluwar Academic Publisher, 2000.

[4.8] A. V. Oppenheim, A. S. Willsky and S. H. Nawab, *Signal and Systems*, 2nd ed, Upper Saddle River, NJ: Prentice Hall, 1997.

[4.9] H.J. Blinchikoff, A.I. Zverev, *Filtering in the Time and Frequency Domains*, New York: John Wiley, 1976.

[4.10] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Addison-Wesley Publising Company Inc., 1971.

[4.11] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. SC-31, pp. 331-343, March 1996.

[4.12] K. S. Kundert, "Introduction to RF Simulation and Its Application," *IEEE J. Solid-State Circuits*, vol. SC-34, pp. 1964-1973, Sept. 1999.

[4.13] R. G. Meyer and M. L. Stephens, "Distortion in Variable-Capacitance Diodes," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 47-54, Feb. 1975.

[4.14] J. A. Crawford, *Frequency Synthesizer Design Handbook*, Norwood, MA: Artech House Inc., 1994.

[4.15] J. K. A. Everard, "Low Noise Oscillators," *Proceedings of IEEE/MTT-S*, pp. 1077-1080, 1992.

[4.16] M. J. Underhill, Phase Lock Loop and Frequency Synthesis, Course Notes, University of Surrey, UK.

Chapter 5

[5.1] M. J. Underhill and M. J. Blewett, "Spectral Improvement of Direct Digital Frequency Synthesisers and Other Frequency Sources," *Proc. 10th EFTF*, Brighton, pp. 452-460, March 1996.

[5.2] M. J. Underhill and M. J. Blewett, "Performance of a Delay Compensation Phase Noise and Time Jitter Reduction Method," *Proc. 11th EFTF*, Neuchatel, pp. 364-368, March 1997.

[5.3] M. J. Underhill, "Phase Noise Limits of the Anti-Jitter Circuit and On-Chip RC Oscillators," *Proc. 14th EFTF*, Torino, March 2000.

[5.4] G. Chien, *Low-Noise Local Oscillator Design Techniques using a DLL-based Frequency Multiplier for Wireless Applications*, Ph.D. dissertation, University of California, Berkley, 2000.

[5.5] Terng_Yin Hus, et al.,"Design of a Wide-Band Frequency Synthesizer Based on TDC and DVC Techniques", *IEEE J. Solid State Circuits vol. SC-37, No. 10* pp1244-1255, Oct. 2002.

[5.6] H. Meyr, M. Moeneclaey and S. A. Fechtel, *Digital Communication Receivers-Synchronization, Channel Estimation and Signal Processing*, New York: Wiley, 1998.

[5.7] A. Papoulis, *Propbability, Random Variales, and Stochastic Processes*, 3rd ed., McGraw-Hill Inc., Singapore, 1991.

[5.8] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Addison-Wesley Publising Company Inc., 1971.

[5.9] J. Silva-Martinez, M. Steyaert and W. Sansen, *High-Performance CMOS Continuous-Time Filters*, Kluwer Academic, Norwell, MA, 1993.

[5.10] B. Razavi, *RF Microelectronics*, New Jersey: Prentice Hall, 1998.

[5.11] H. Tanimoto, M. Koyama and Y. Yoshida,"Realization of a 1-V Active Filter Using a Linearization Technique Employing Plurality of Emitter-Coupled Pairs", *IEEE J. Solid State Circuits vol. SC-26, No. 7*, pp937-945, July, 1991.

[5.12] G.A DeVeirman, and R. G. Yamasaki,"Design of a Bipolar 10-MHz Programmable Continuous-Time 0.05° Equiripple Linear Phase Filter", *IEEE J. Solid State Circuits vol. SC-27, No. 3*, pp937-945, March, 1992.

[5.13] R. S. Carson, *Radio Communication Concept: Analog*, John Wiley & Sons, New York, 1990.

[5.14] S. Hara, T. Tokumitsu, and M. Aikawa, " Broad-Band Monolithic Microwave Active Inductors", *IEEE Transaction on Microwave Theory and Techniques, vol. 37,* pp 1979-1984, December, 1989.

[5.15] S. Lucynszyn, and I. D. Robertson, " Monolithic Microwave Narrow-Band Filter Using Ultrahigh-Q Tunable Active Inductors", *IEEE Transaction on Microwave Theory and Techniques, vol. 42,* pp 2617-2622, December, 1994.

[5.16] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, New-York: Cambridge University Press, 2000.

[5.17] M. E. van Valkenburg, *Analog Filter Design*, Holt Saunders, Japan, 1982.

[5.18] Data sheet, *74HC/HCT4046A*, Philips Semiconductors, 1997.

[5.19] Oxtek Limited, Oxford, UK.

[5.20] Service Guide, HP 33120A Function Generator / Arbitrary Waveform Generator, Hewlett Packard, U.S.A., 1996.

[5.21] B. Razavi, Y. Ota and R. G. Swartz, "Design Technique for Low-Voltage High-Speed Digital Bipolar Circuits", *IEEE J. Solid State Circuits vol. SC-29, No. 3*, pp. 332-339, March, 1994.

[5.22] B. Razavi, "A 2.5-Gb/s 15-mW Clock Recover Circuit", *IEEE J. Solid State Circuits vol. SC-31, No. 4*, pp. 472-480, April, 1996.

[5.23] B. Razavi, "A 2-GHz 1.6-mW Phase-Locked Loop", *IEEE J. Solid State Circuits vol. SC-32, No. 5*, pp. 732-735, April, 1997.

[5.24] Data sheet, *HFA3046*, Harris Corporation, August, 1996.

[5.25] M. J. Underhill, "The Adiabatic Anti-Jitter Circuit," *IEEE Transaction on Ultrasonics, Ferroelectrics and Frequency Control, vol. 48, No.3*, pp. 666-674, May 2001.

Chapter 6

[6.1] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, " Sideband Noise Reduction in Transposed Gain Oscillators, " *IEEE Proceeding ISCAS2003*, May 2003.

[6.2] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, " IF-LO Delay Mismatch and Noise Reduction in Transposed Gain Oscillator," *Proceeding EFTF18th*, April 2004.

[6.3] M. Shimanouchi," An Approach to Consistent Jitter Modeling for Various Jitter Aspects and Measurement methods," *ITC Proceedings*, pp 848-857, 2001.

[6.4] S. Bunnjaweht, M. J. Underhill and I. D. Robertson, "Novel Jitter and Phase Noise Reduction Circuit, " *Proceeding EFTF18th*, April 2004.