Loughborough University

Thesis Access Form

Copy No……..……**Location**……..…

Author……..……Yingtao Tian ……..…….

Title…… Electrodeposition of Indium Bumps for Ultrafine Pitch Interconnections……..

Status of access OPEN / ~~RESTRICTED~~ / ~~CONFIDENTIAL~~

Moratorium Period:……years, ending……../……200…….

Conditions of access approved by (CAPITALS):……Dr. Changqing Liu……

Supervisor (Signature)……...……...

Department of……Wolfson School of Mechanical and Manufacturing Engineering ……

Author's Declaration: *I agree the following conditions:*

Open access work shall be made available (in the University and externally) and reproduced as necessary at the discretion of the University Librarian or Head of Department. It may also be digitised by the British Library and made freely available on the Internet to registered users of the EThOS service subject to the EThOS supply agreements.

*The statement itself shall apply to **ALL** copies including electronic copies:*

This copy has been supplied on the understanding that it is copyright material and that no quotation from the thesis may be published without proper acknowledgement.

Restricted/confidential work: All access and any photocopying shall be strictly subject to written permission from the University Head of Department and any external sponsor, if any.

Author's signature……Yingtao Tian…….Date……10-Nov-2010.……...……...

users declaration: for signature during any Moratorium period (Not Open work): ***I undertake to uphold the above conditions:***			
Date	Name (CAPITALS)	Signature	Address

Electrodeposition of Indium Bumps for Ultrafine Pitch Interconnections

By

Yingtao Tian

A Doctorial Thesis

Submitted in partial fulfilment of the requirements
for the award of
Doctor of Philosophy of Loughborough University

August 2010

Research Student Office, Academic Registry
Loughborough University Leicestershire LE11 3TU UK
Switchboard: +44 (0) 1509 263171 Fax: +44 (0) 1509 223938

CERTIFICATE OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this thesis, that the original work is my own except as specified in acknowledgments or in footnotes, and that neither the thesis nor the original work contained therein has been submitted to this or any other institution for a degree.

…… (Signed)

…… (Date)

For My Parents

In Memory of My Grandfather

Abstract

Microelectronics integration continuously follows the trend of miniaturisation for which the technologies enabling fine pitch interconnection are in high demand. The recent advancement in the assembly of Hybrid Pixel Detectors, a high resolution detecting and imaging device, is an example of where novel materials and processes can be applied for ultra-fine pitch interconnections. For this application, indium is often used for the fine pitch bump bonding process due to its unique properties that make it especially suitable, in particular in a cryogenic environment where some types of detector have to serve. Indium bumps are typically fabricated through vacuum evaporation at the wafer level; however, this thesis investigates an alternative low cost manufacturing process at the wafer scale for the deposition of indium micro-bumps through electroplating. The work has placed its emphasis on the requirements of future technologies which will enable a low temperature ($<150^{o}C$), high density interconnection (> 40,000 IOs$/cm^2$) with a high throughput and high production yield.

This research is a systematic investigation of the wafer-scale indium bumping process through electrodeposition using indium sulphamate solution. An intensive experimental study of micro-bump formation has been carried out to elaborate the effects of two of the main electroplating factors that can significantly influence the quality of bumps in the course of electrodeposition, namely the current distribution and mass transport. To adjust the current density distribution, various waveforms of current input, including direct current (DC), unipolar pulse current and bipolar pulse reverse current, were employed in the experiments. To assist mass transportation prior to or during electroplating, acoustic agitation including ultrasonic agitation at 30 *kHz* frequency as well as megasonic agitation at 1 *MHz*, were utilised.

The electrochemical properties of the indium sulphamate solution were first investigated using non-patterned plain substrates prior to indium bumping trials. This provided understanding of the microstructural characteristics of indium deposits produced by electroplating and, through cathodic polarisation measurements, the highest current density suitable for electrodeposition was achieved as approximately 30 mA/cm^2 when electroplating was carried out at room temperature and with no agitation applied. The typical surface morphology of DC electroplated indium contained a granular structure with a surface feature size as large as 10 μm. Pulse and pulse reverse electroplating significantly altered the surface morphology of the

deposits and the surface became much smoother. By introducing acoustic agitation, the current density range suitable for electrodeposition could be significantly expanded due to the greater mass transfer, which led to a higher speed of deposition with high current efficiency.

Wafer-scale indium bumping (15 μm to 25 μm diameter) at a minimum pitch size of 25 μm was successfully developed through electroplating trials with 3 inch test wafers and subsequently applied onto the standard 4 inch wafers. The results demonstrate the capability of electroplating to generate high quality indium bumps with ultrafine pitch at a high consistency and yield. To maximise the yield, pre-wetting of the ultrafine pitch photoresist patterns by both ultrasonic or megasonic agitation is essential leading to a bumping yield up to 99.9% on the wafer scale. The bump profiles and their uniformity at both the wafer and pattern scale were measured and the effects of electrodeposition regimes on the bump formation evaluated. The bump uniformity and microstructure at the feature scale were also investigated by cross-sectioning the electroplated bumps from different locations on the wafers. The growth mechanism of indium bumps were proposed on the basis of experimental observation. It was found that the use of a conductive current thief ring can homogenise the directional bump uniformity when the electrical contact is made asymmetrically, and improve the overall uniformity when the electrical contact is made symmetrically around the periphery of the wafer. Both unipolar pulse electroplating and bipolar pulse reverse electroplating improved the uniformity of the bump height at the wafer scale and pattern scale, and the feature scale uniformity could be significantly improved by pulse reverse electroplating. The best uniformity of 13.6% for a 4 inch wafer was achieved by using pulse reverse electroplating. The effect of ultrasonic agitation on the process was examined, but found to cause damage to the photoresist patterns if used for extended periods and therefore not suitable for use throughout indium bumping. Megasonic agitation enabled high speed bumping without sacrifice of current efficiency and with little damage to the photoresist patterns. However, megasonic agitation tended to degrade some aspects of wafer scale uniformity and should therefore be properly coupled with other electroplating parameters to assist the electroplating process.

Key Words: Ultrafine pitch bumping; Indium bump bonding; Electrodeposition / Electroplating; Direct current; Pulse electroplating; Pulse reverse electroplating; Bump uniformity; Bumping yield; Ultrasonic agitation; Megasonic agitation; Wafer/Pattern/Feature scale.

Publications

1. Y. Tian, C. Liu, D. A. Hutt, B. Stevens, D. Flynn, and M. P. Y. Desmulliez, "High Density Indium Bumping Using Electrodeposition Enhanced by Megasonic Agitation" in *11th Electronics Packaging Technology Conference, Singapore*, December 2009, pp. 31-35.
2. Y. Tian, D. A. Hutt, C. Liu, and B. Stevens, "High Density Indium Bumping through Pulse Plating Used for Pixel X-Ray Detectors" in 2009 *International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, Beijing, China., July 2009 pp. 456-460. (Second Best Paper Award).
3. J. Kaufmann, M. Desmulliez, Y. Tian, D. Price, M. Hughes, N. Strusevich, C. Bailey, C. Liu, and D. A. Hutt, "Megasonic agitation for enhanced electrodeposition of copper," *Microsystem Technologies*, vol. 15, no. 8, pp. 1245-1254, 2009.
4. Y. Tian, J. Kaufmann, C. Liu, D. A. Hutt, B. Stevens, and M. P. Y. Desmulliez, "Megasonic Enhanced Wafer Bumping Process to Enable High Density Electronics Interconnection," in Proc. of *2nd Electronics System-Integration Technology Conference*, Greenwich, UK, 2008, pp. 725-729.
5. Y. Tian, C. Liu, D. A. Hutt, and B. Stevens, "Electrodeposition of Indium for Bump Bonding" in *58th Electronic Components and Technology Conference*, Florida, USA, May 2008, pp. 2096-2100.

Acknowledgement

This research is financially supported by a Doctoral Training Account (DTA) from the UK Engineering and Physical Sciences Research Council (EPSRC) through the Innovative Electronics Manufacturing Research Centre (IeMRC) in Loughborough University under the grant DTA/13/2006.

I would like to take this opportunity to express my sincerest gratitude and appreciation to my supervisors, Dr. Changqing Liu and Dr. David Hutt, for their great support and guidance through the course of my PhD research. I also would like to express my sincerest thanks to my co-supervisor, Mr. Bob Stevens, from Rutherford Appleton Laboratory, for the discussions, valuable suggestions and help in experimental work through the past three years.

I would like to thank Dr. Geoff Wilcox and Dr. Gary Critchlow in Materials Department, Loughborough University, for their kindness and help in access of laboratory facilities. I also would like to thank Prof. David Gabe in Materials Department for his valuable suggestions on electroplating. I wish to give my special acknowledgement to Dr. Geoff West in Loughborough Materials Characterisation Centre (LMCC) for his training and help for the usage of the dual-beam system. The great help from Prof. Marc Desmulliez, Dr. David Flynn, Dr. Jens Kaufmann and Mr. Mark Leonard in the MIcroSystems Engineering Centre (MISEC), Heriot-Watt University, on the wafer sample preparation is highly appreciated. Thanks are also extended to Dr. Yi Zhang of Diado Metal Ltd (UK) for his experiences on electroplating. Mr. Andy Sandaver deserves my sincere gratitude for his kind assistance in experiments through the three years research.

I also would like to thank other members in the Interconnection Group, Prof. Paul Conway, Dr. David Whalley, Dr. Patric Webb and Dr. Xiaoyun Cui for their valuable discussion and suggestions. I am most grateful to the discussions and helps from my colleges, Mr. Yi Qin, Mr. Owain Williams, Mr. Benedikt Knauf, Dr. Lina Huertes, Dr. Tze-Yang Hin, Dr. Jun Liu, Dr. Hui Xu, and Mr. Hrushikesh Abhyankar.

Finally, I am forever indebted to my families for their great love, support and encouragement.

Table of Contents

List of Figures

List of Tables

Glossary

cm	centimetre
f	frequency of acoustic wave
i	current density
i_{avg}	average current density of pulsating current waveform
i_L	limiting current density
i_p	pulse peak current density
$i_{p(a)}$	pulse peak current density in the anodic cycle
$i_{p(c)}$	pulse peak current density in the cathodic cycle
i_{pL}	pulse limiting current density
k	conductivity of the electrolyte
k_1	a proportionality constant
k_2	a constant related to the amount of energy required for nucleation
m	mass of the substance altered at an electrode
mA	milliampere
ms	millisecond
n	number of electrons transferred during the electrode equilibrium process
nm	nanometre
t	electroplating time
t_{off}	pulse-off duration
t_{on}	pulse-on duration
$t_{on(a)}$	pulse-on duration in the anodic cycle
$t_{on(c)}$	pulse-on duration in the cathodic cycle
z	valence number of the reaction ions
C_B	concentration of reactant in bulk solution
C_0	concentration of reactant at electrode surface
D	diffusion coefficient of the reactants
E^{Θ}	standard cell potential
E(eq)	equilibrium potential
E(I)	potential when current is flowing

F	Faraday constant (96485 *C/mol*)
F_a	adhesion force
F_D	drag force
F_{RD}	reverse force
I	total current flowing through the electrolyte
L	characteristic length of the electrodeposition system
M	molar mass of the metal
M_a	adhesion moment
M_R	removal moment
P_t	Total Height of Profile
Q	total electrical charge
R	gas constant
R_a	Average Roughness
T	temperature
V	voltage
V_n	nucleation rate
V_p	pattern vacancy rate
W_a	Wagner number
α	charge transfer coefficient
β	transmission angle
δ	thickness of Nernst Diffusion Layer
η	overpotential
μm	micrometre
μs	microsecond
v	viscosity of the liquid
φ	duty cycle of pulsating current
ω	period of acoustic wave

Chapter 1 Background and Introduction

1.1 Background to Wafer Level Interconnection

Microelectronic packaging is the science of integrating individual electrical components, such as transistors, resistors, capacitors and diodes, into functional circuits through effective and reliable interconnections [1, 2]. Figure 1-1 demonstrates the typical hierarchy of microelectronic packaging on different levels. The zero level packaging involves in chip metallisation and provisions for chip package interconnections, which is also called wafer level packaging. The first level packaging is to establish interconnections between the micro-chip and a substrate which can form either single or multiple chip modules. Then, assembly of chip modules and other components on printed circuit board (PCB) is referred as the second level packaging. The third level packaging includes several PCBs plugged into a motherboard forming a sophisticated device, *e.g.* a computer.

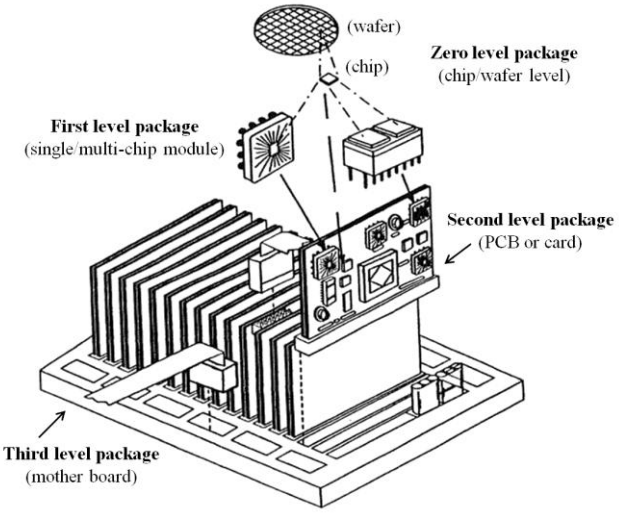


Figure 1-1 Typical hierarchy of microelectronic packaging levels [1]. (Reproduced with permission from Ref. 1)

For the wafer level packaging, the mainstream interconnection technologies currently employed in semiconductor industry include wire bonding, tape automated bonding (TAB) and flip chip solder bonding. Wire bonding is performed by attaching a fine wire between the I/Os around the perimeter of the chip and the associated packaging pins while TAB involves in additional bumping on the chip and substrate. Flip chip utilises area arrayed solder bumps on the entire chip area corresponding to the I/Os to match the connection pins on the substrate. The term flip chip is derived from the joining process that the chip carrying solder bumps needs to be faced-down to the substrate. Flip chip can offer distinct advantages including higher packaging density, shorter interconnect leading to faster signal response and uniform power and heat distribution [2]. Although the chip market is currently dominated by wire bonding and TAB, flip chip has been recognised as the development trend of wafer level interconnection technique for next generation electronics products (Figure 1-2) [3].

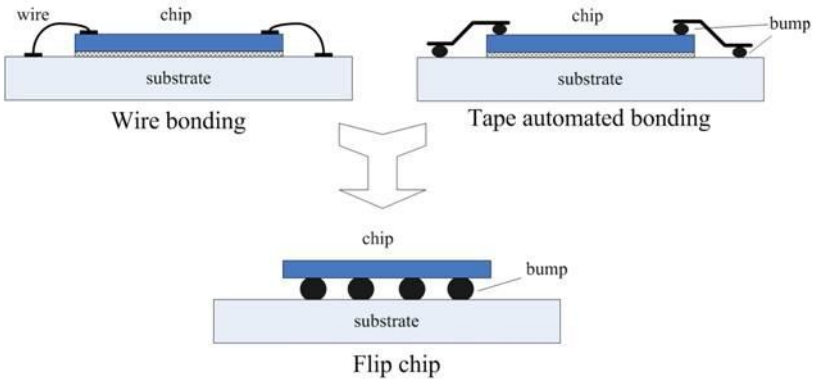


Figure 1-2 Development of wafer level interconnection technologies.

1.2 Indium Bump Bonding Used in Pixel Detectors

The demand for miniaturisation in microelectronic packaging continuously drives the pitch size of interconnections to shrink to that of the bump pitch. For area array flip chip on board, this is projected to decrease to 80 μm by 2015 according to the International Technology Roadmap for Semiconductors (ITRS) 2005 [3]. The emerging wafer level packaging application is able to achieve ultrafine pitch interconnection beyond the current industrial standard by virtue of the advantages of

the rigid substrate. In particular, assembly of Hybrid Pixel Detectors used for imaging devices (*e.g.* X-ray or infrared radiation detection) demonstrates the leading-edge ultrafine pitch interconnection technology to which indium bump bonding has been successfully applied.

1.2.1 Background to Pixel Detector Applications

The development of Hybrid Pixel Detectors in imaging applications in recent years has widely stretched the interconnection technologies. It was originally motivated by the demands from high energy physics research which are to simultaneously fulfil the requirements of investigating short-lived particles and coping with continuously increasing energy level and interaction rate of modern devices. In order to track the decay processes of the particles, sometimes even in the picosecond range, the so-called Hybrid Pixel Detector needs to have a fast enough response speed to distinguish different types of particles passing through the decay point. The pixel stands for the smallest sensing element which is able to grab information and deliver it to the readout circuitry. The pixel detector also needs to have enough sensing elements available to achieve the high accuracy necessary for analysis. The requirement of accuracy necessitates a very small size for each individual pixel and therefore, large numbers must be arrayed to cover the area of interest [4]. Moreover, pixel detectors have provided support in many applications other than high energy physics, for example, X-Ray detection and infrared imaging. As shown in Figure 1-3, the assembly of a pixel detector requires direct connection between the sensor chip and readout circuit chips which is an ASIC (Application Specific Integrated Circuit). A hybrid pixel detector typically consists of millions of sensor elements and readout circuit chips which are fabricated separately and then assembled together. Both the sensor chips and readout ASICs are processed at the wafer level. The idea can be traced back to 1985 when it was pointed out by Gaalame that a large array of photon detectors could be realised by connecting sensor chips to silicon readout integrated circuits through bump bonding techniques [5]. However, the integrated circuit and packaging technology were not mature enough to fabricate large area array detectors for high energy physics usage at that time. The first pixel detector was realised through 38 μm diameter solder bump connections, by the Omega project launched by

CERN (European Laboratory for Particle Physics) in the early 1990s [6], and the encouraging testing results stimulated investigators to explore this method further.

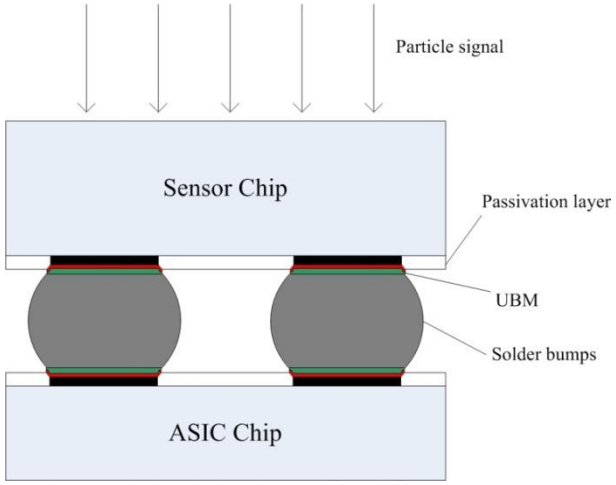


Figure 1-3 Structure of typical pixel detector unit.

The evolution of pixel detectors has been reinforced by the advancement in integrated circuit technology and miniaturisation of electronic packaging. To achieve a high manufacturing efficiency and high yield, the hybrid integration method has been employed. Relatively small detector assemblies, which are called modules, are fabricated independently on the wafer level and then arranged in a 'mosaic' to fit into the sensitive area defined by the experiments.

Given the huge number of interconnections within each module and high level of integration, bump bonding is the only available technique to meet the requirements. For example, the current state-of-the-art ATLAS pixel detectors used in CERN have approximately 2000 modules and for each of the modules, 16 readout chips have to be bonded onto a single sensor unit. The pixel in the module is $50 \times 400\ \mu m^2$ in size and the connection density is about 5,000 cm^{-2}. Each of the sensors is approximately 2×6 cm^2 in area and is subdivided into about 50,000 pixels. Thus, the total pixels in the whole detector exceed 10^8 and each of the pixels are bonded through solder bumps with a 25 μm diameter and a minimum pitch size of 50 μm [7-9]. Such high density interconnection is beyond the limit of current main stream industrial standards and can only be realised through precisely controlled wafer level bump bonding. Furthermore, the next generation application is moving to a less than 50 μm pitch

interconnection and this result in more than 40,000 I/Os per cm^2, which poses extreme challenges to bump bonding technology.

In addition to the requirement of very high interconnection density, the bumping process must have a very high yield to ensure the productivity of the large number of modules. Bearing the numerous quantities of bumps in mind, even a very small percentage of failed bumps will cause the pixel detector to malfunction. Moreover, reliability issues need to be considered at the design stage to avoid failure of module assemblies. Currently, the most popular pixel detectors are based on silicon processing technology, *i.e.* the ASIC circuit chip and sensor chip are fabricated based on silicon wafers. Because the sensor and ASIC chips are fabricated separately, other semiconductor materials rather than silicon could be employed as the substrate for the sensor chip. For example, pixel detectors based on GaAs and CdTe have been developed to fulfil new demands in X-Ray, γ-ray and infrared detection applications [10-13]. However, mismatch of the CTE (Coefficient of Thermal Expansion) between these different materials will be a noticeable reliability issue during the assembly process and the product life. For some types of device which need to perform under cryogenic environments, such as liquid nitrogen, the bump bonding process is crucial to achieve a successful assembly.

Several advantages make indium bump bonding the primary solution for pixel detector assemblies. Firstly, it allows a low temperature process. The melting point of indium is 156.6 $^{\circ}C$ which is lower than most of the tin-based lead-free solders (*e.g.* $SnAg_{3.0}Cu_{0.5}$ 220 ^{o}C, $SnCu_{0.7}$ 227 ^{o}C). Robust bonding could be easily achieved at room temperature or, in the occasion of reflowed indium bumps, the package will still bear less thermal impact than using most of the lead-free solders. Secondly, indium can stay ductile at very low, even liquid helium temperatures, thus, indium bump bonded devices could still perform well in cryogenic environments and feature high reliability. This makes indium bump bonding the only choice for devices needed to be used in cryogenic conditions. Thirdly, indium bump bonding is capable of fabrication at an ultra-fine pitch with high yield: a comparison investigation was conducted by the Fermi National Accelerator Laboratory and the current achievable minimum size of indium bump through evaporation is 12 μm diameter, height of 8-10 μm at 18 μm pitch [14]. Moreover, for X-Ray diffraction, spectroscopy, microscopy and low energy experiments, the pixel detectors require low signal to noise level within the 4

keV to 20 *keV* energy band. Indium does not have $K_{\alpha(1,2),}$ K_{β}, $L_{\alpha(1,2),}$ $L_{\beta(1\text{-}2)}$, $M_{\alpha 1}$ emission lines within the detected energy band, which indicates a low 'noise' level of detectors.

1.2.2 Wafer Bumping Techniques

The crucial step for bump bonding technology is how to effectively deliver a uniform quantity of material onto the desired areas of the wafer, *i.e.* the wafer bumping process. The cost, efficiency and yield need to be considered when choosing the bumping technique. So far, the three most mature techniques are evaporation, stencil printing and electroplating. The technical features, advantages and disadvantages are discussed in the following section.

1.2.2.1 Evaporation

Evaporation wafer bumping has matured through over around 50 year's industrial experience and was invented by IBM in the 1960s. The process is based on vacuum physical vapour deposition and is also named as the C4 (Controlled Collapse Chip Connection) process by IBM [15-17]. Initially, a metal mask made of molybdenum is necessary to define the area for the solder bumps during the deposition. Molybdenum is used because of its excellent dimensional stability at high temperature. However, to maintain the desired stability, the bump dimensions and pitch sizes are limited depending on the size and thickness of the molybdenum mask. To achieve a finer pitch size, a photoresist pattern has been utilised to replace the metal mask [18]. Dry film or liquid photoresist is laminated or spin coated on the wafer and exposed under UV light to create patterns with a reusable photomask for which the resolution is much better than the molybdenum mask. The exposed area is removed or retained depending on whether the photoresist is 'negative' or 'positive'. The metal is then deposited by evaporation covering all areas of the wafer and resist. After evaporation, the photoresist pattern is removed by solvent, lifting off the unwanted material so that the metal remains on the bond pads. Finally, the solder bumps are reflowed to form the truncated sphere ball shape.

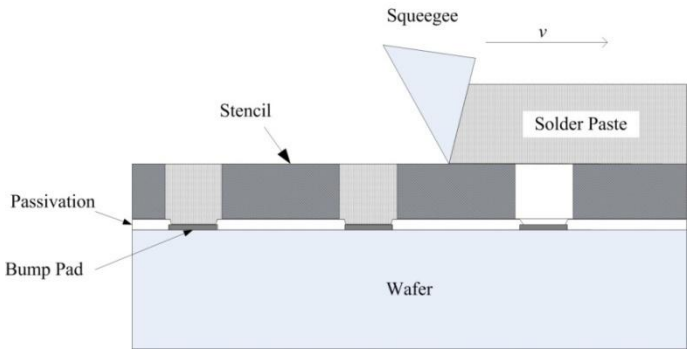


Figure 1-4 Schematic of the principle of the stencil printing bumping process.

1.2.2.2 Stencil Printing

Stencil printing for wafer bumping is derived from its application for surface mount assembly. To start the process, a stencil with apertures, which may be made of metal or polymeric materials, is placed on the printer frame. The apertures in the stencil correspond to the bumping area. A wafer needs to be placed underneath and aligned with the stencil. The solder bump materials are deposited in a paste which is evenly applied on the stencil. A metal squeegee travels along the stencil surface with controlled speed and angle, and extrudes the solder paste through the apertures onto the wafer surface (Figure 1-4). After the wafer is released from the stencil, the bumps need to be reflowed to form spheres. This method has been widely used in wafer level packaging, but the pitch size is limited at around 100 μm [19-23].

1.2.2.3 Electroplating

Electroplating has been playing a significant role in the increasing development of microelectronics manufacturing since the 1960s and has mainly featured as the through mask electroplating of magnetic heads, through mask electroplating of solder bumps, dual-damascene copper electroplating for advanced chips and through hole filling for 3-D interconnection [24-29].

Unlike the previous two ‘dry’ wafer bumping processes, electroplating involves a ‘wet’ electrochemical step to deposit the solder bumps. After the necessary preparation, a blanket layer of metal is deposited on the wafer acting as ‘seed layer’ for bump growth. The seed layer needs to be very thin and to cover all the area of the

wafer. After that, the wafer is covered with a patterned photoresist through a carefully controlled lithography process. The photoresist pattern acts as a mask to selectively expose the conductive area to the electrolyte. Then, the wafer is immersed into an appropriate electrolyte and acts as the cathode. A soluble or insoluble anode is utilised to complete the circuitry. Normally, electrical connection is made through the edge of the wafer. After the bump deposition is complete, the photoresist pattern is removed and the seed layer needs to be etched away. Once the solder bump is finally isolated, a reflow step is performed to form a spherical solder ball [27, 30-32].

1.2.2.4 Comparison of Current Techniques

Evaporation is justified as a low efficiency, costly and limited method due to the following reasons. Firstly, only 5% of material is deposited on the usable sites and 95% of materials end up on the evaporator wall and masks. The cost of the raw materials and cleaning of the waste make this method expensive. Secondly, the issues of CTE mismatch between the metal mask and wafer deteriorates when the pitch size decreases and wafer size increases. The photoresist mask is the only option for fine pitch bumping. Thirdly, because of the relatively low vapour pressure of tin, the evaporation rate of tin is much slower than other solder materials, such as lead, copper and silver. The evaporation method is usually applied for high lead content solder bumps, such as 95Pb5Sn and 97Pb3Sn. It is not suitable for tin-rich solder bumps as it is unaffordable and time-consuming [1, 18].

Stencil printing offers a low-cost, automated, highly flexible and re-workable solution for wafer bumping. However, manufacturing of high resolution stencils becomes difficult when the pitch size decreases. Currently, the pitch size of the stencil is limited to around 120 μm, and some specific applications can achieve 100 μm [21, 22]. Another reason which stops stencil printing from being applied to high density interconnection applications is the relatively poor yield. Rework often becomes necessary when the pitch size in the stencil hits the limit [21].

The main advantage of electroplating exists in the capability of depositing ultra-fine pitch solder bumps through a simple lithography process and electroforming. Electroplating has been identified as a cost-effective, reliable, and scalable method to generate ultra-fine pitch solder bumps with very high yield. Removal of the seed layer

after electroplating may pose difficulties in some applications and the bump uniformity will be the main problematic issue when the wafer size is enlarged [32].

1.2.3 Bump Bonding Techniques Used in Pixel Detectors

Currently, two types of bump bonding techniques are being employed in pixel detector assemblies, which are electroplated eutectic tin-lead solder bumps (*e.g.* Sn63Pb37) and indium bumps deposited by evaporation.

1.2.3.1 Eutectic Sn-Pb Solder Bump Bonding

Eutectic tin-lead solder bumping was an ideal candidate for microelectronics and has been largely utilised in SMT (Surface Mounting Technology), BGA (Ball Grid Array) on board level packaging and bump bonding on wafer level packaging. As mentioned above, eutectic Sn-Pb solder deposited through evaporation is not cost-effective, and stencil printing struggles with the ultra-fine pitch bumping. Electroplating becomes the only technique to apply eutectic Sn-Pb solder bumps for assemblies of pixel detectors. However, under the impact of RoHS (Restriction of Hazardous Substances), not all of the pixel detectors are excluded from the regulations and for long-term development, Pb content solder bumps will not be tolerated. Moreover, reflow of the solder bumps at over 250 ºC is necessary to form smooth truncated spheres and another reflow is needed to form the joint with other parts. Thus, reliability becomes a serious issue because of the thermal shock during the reflow processes, especially in the case of different materials used for the sensor and readout chips [8].

1.2.3.2 Indium Bump Bonding

Indium is a crystalline, silvery white metal, which is very soft (Hardness 0.9 *HB*, softer than lead), ductile and diamagnetic. It is most frequently associated with zinc and is commercially recovered from sphalerite residue. It has low melting point (156.6 °*C*), high boiling point (2072 °*C*) and thus a low vapour pressure. The molten indium metal wets clean glass, glazed ceramics, metals and certain metal oxides. Indium has a low coefficient of friction and antiseizure properties which allow its wide application in thin-films to form lubricated layers such as coated bearings in high performance aircraft [33]. With the development of the electronics industry, indium has been commonly used as a *p*-type doping agent in semiconductors. Its

current primary application is to form transparent electrodes from indium tin oxide (ITO) in liquid crystal displays (LCD) [34].

Indium bump bonding has been developed on the basis of evaporation to achieve a low temperature, high density contact, ultra-fine pitch and robust interconnection for pixel detectors [7, 14, 35-37]. A typical indium bump bonding process is shown in Figure 1-5. Two photolithography steps are used to create the mask for evaporation and an indium bump needs to be deposited on both of the sensor and ASIC readout chip sides. Cr as the under bump metallisation (UBM) is evaporated onto the bond pads in the same vacuum cycle. The opening for indium deposition can be as low as 30 μm, but the thickness of indium is restricted to less than 10 μm, because thicker indium will pose difficulties in the following lift-off step. Steps *a)* to *e)* are repeated exactly on both of the sensor and readout chips. Then, indium-to-indium bonding is formed by compression at room temperature leaving a 10 μm gap between the chips. Although it has been tested that the best bonding can be achieved at 100 ^oC, which means none of the parts in the whole package will be exposed to temperature over 100 ^oC, room temperature bonding is also robust enough for reliable interconnection [35]. This room temperature bonding process was initially developed for applications which are very sensitive to thermal impact, *e.g.* infrared detectors.

Another indium bump bonding process involving reflow has also been developed for applications which are not sensitive to moderate thermal exposure and to increase the distance between the sensor and readout chips after bonding. The process features two lithography steps for the UBM sputtering and indium evaporation respectively. The majority of indium is deposited onto the sensor chip side, while only a thin indium layer (1~2 μm) is evaporated onto the readout chip to improve the adhesion. The opening of the photoresist mask for indium evaporation needs to be enlarged to deposit enough material at the limited thickness so that when it is reflowed the requested ball diameter is achieved. Afterwards, the sensor chip carrying indium bumps is reflowed at about 180 ^oC to form smooth spherical indium bumps. Finally, flip chip attachment is conducted at ~200 ^oC while the bumps are melted. Another advantage of this process is the self-alignment between the two chips during the final bonding driven by surface tension [36-38].

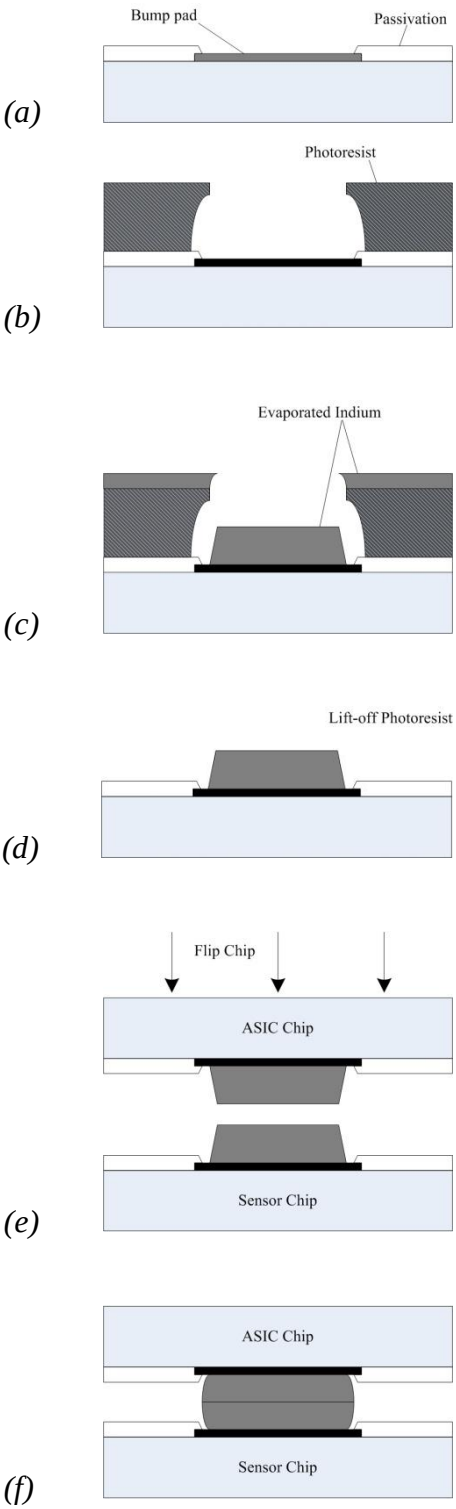


Figure 1-5 Schematic of typical indium bump bonding process.

However, the multiple evaporation and lithography steps make the process complicated and expensive while only special applications justify using this technology. Material cost is noticeable because indium is a noble metal and the majority of material is wasted in the evaporation process. Sputtering and evaporation necessitate vacuum operation conditions requiring high capital investment in facilities in the early stage, which is not flexible and efficient. As for the removal of photoresist, because the lift-off resist is not soluble in acetone and the dimension of the deposited metal is quite small, the removal process commonly needs many hours to complete. Moreover, indium deposited on the unwanted photoresist area can possibly re-deposit on the wafer which will seriously deteriorate the yield. So, the evaporation based indium bump bonding is not attractive to industry from the point of view of scaling up the production. Although it has been successfully applied to fabricate pixel detectors, *e.g.* the ATLAS detector in CERN, it is still worthy to explore alternative processes which could be more flexible, productive and economical.

1.3 Aims and Objectives of the Research

The research presented is dedicated to investigate an alternative manufacturing method for the deposition of indium bumps at the wafer level based on the use of electroplating. This research is based on a collaboration with Rutherford Appleton Laboratory (RAL) in the UK and is projected to fabricate indium bumps for the assembly of a type of X-ray detector. Electroplating is promising as it may offer lower-cost, the capability of ultra-fine pitch bumping and high yield. As shown in Figure 1-6, the proposed electroplating procedure only requires one simple photolithography step. A blanket thin seed layer is deposited first onto the wafer after cleaning and passivation. Once the seed layer is deposited, a thick photoresist is spun and developed to form the required pattern. Next, indium bumps are electroplated onto the seed layer through the pattern sequentially. Then the photoresist is removed with a solvent and the seed layer is stripped except for the portion under the bumps. Finally, the wafer is reflowed to form the truncated spherical indium bumps ready for flip chip assembly. This process can be applied for bumping on both of the sensor and ASIC chips which are bonded at room temperature.

Electroplating of indium bumps has been pioneered by a few researchers. Merken and John et al [36, 39] conducted a serial experimental study of electroplating

indium bumps through $InCl_3$:H_2O aqueous solution on 3 inch wafers for hybrid integration of infrared sensitive detectors. Electroplated indium bumps with 13 μm diameter and 25 μm pitch were successfully assembled in a 256 × 256 pixel array module. Another study conducted by Jiang et al [38] was also used for the fabrication of infrared focal plane arrays (FPA). In that work, indium electroplating was performed in indium sulphamate solution at room temperature and the minimum size of bump was 11 μm on 25 μm pitch with a stack of Ti/Pt/Au UBM was deposited by e-beam evaporation first.

Although the electroplating approach for indium bumping on the wafer level has been successfully demonstrated, fundamental studies of the electroplated indium bumping process are still missing in the literature. It has been pointed out that the main challenge of the electroplating bumping process is the uniformity and consistency of the distributed deposits, which will determine the bumping yield and consequently the ensuing flip chip assembly and joint reliability. The uniformity and consistency of the bumps obtained may be defined in terms of their features including the material density, bump height, volume and profile after reflow. The uniformity of the electrodeposited bumps is crucial to achieve highly reliable joints since non-uniformly deposited bumps could not meet functional and dimensional requirements. For example, large variations in height and volume between bumps could result in electrical open circuits for small bumps and shorts for large bumps. This need of precision and rigidity becomes more significant for pixel detectors since they require very small bump size at ultra-fine pitch size with high yield.

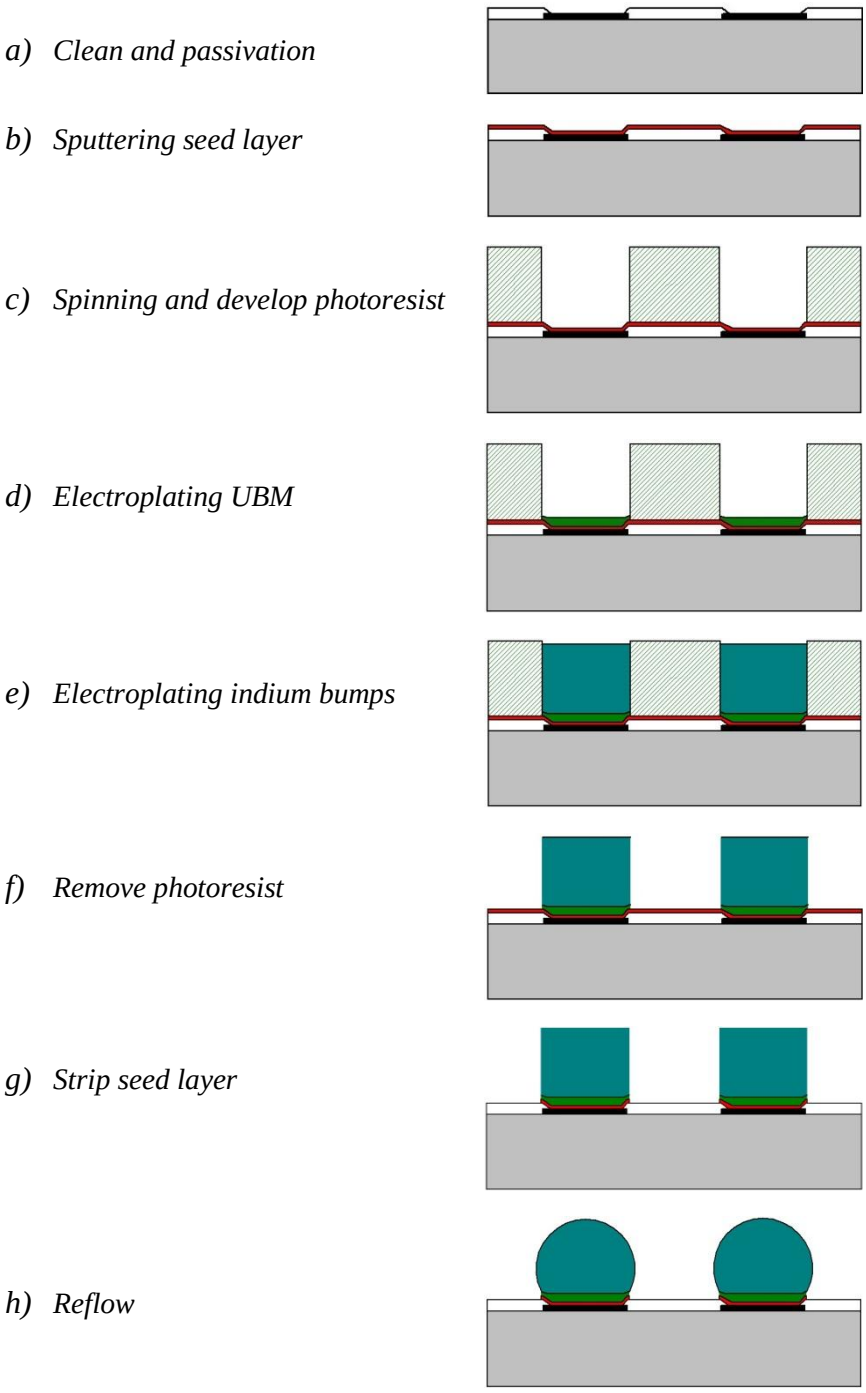


Figure 1-6 Schematic diagram of electroplated indium bumping procedure

The factors that could affect the bump uniformity and consistency may be complex, but it has been fundamentally understood that ultimately the current density and current density distribution across the cathode wafer during the electrodeposition process will determine the course of the electroplating and consequent deposit

formation across whole electroplating areas. In practice, normally the electric contact to the wafer will be through the edges of the wafer, and a very thin seed layer is deposited onto the wafer to serve as the current path, as shown in Figure 1-6. For the sake of cost and efficiency, the thickness of the seed layer is normally below 1 μm, thus the resistance of the seed layer should not be neglected in the calculation of the actual electroplating current. A potential drop from the edges to the centre area of the wafer caused by the seed layer resistance will result in an uneven current density across the wafer, which is known as the terminal effect. Consequently, the deposition rate will be different from the edge area to the centre of a wafer to be electroplated and thus the bump height will also be uneven. Moreover, the bump growth mechanism may differ from the expected course under different current density and the quality of the deposit will vary as well.

Another decisive factor of the uniformity is the mass transport condition. The electrode reaction is influenced by mass transport and the rate of mass transfer is spatially nonuniform over the wafer surface. As a result, the deposition rate, morphology and microstructure of deposits could also vary due to the localised discharge characteristics. During the electroplating process, especially for a very large area, the metal ions will be consumed at different rate across the electrode surface due to the various current densities. If the ion diffusion could not replenish thoroughly, for instance an electroplating bath without any agitation, the solution concentration difference will in turn give rise to non-uniform current distribution. As discussed above, the uneven current density distribution can deteriorate the bump uniformity. Further, the mass transport condition can also play a significant role in determining the bumping yield. As the feature size defined by the photoresist is very small, the interface at which the deposition reactions take place, *e.g.* between the electroplating solution in contact with the substrate (defined as numerous tiny apertures by the resist) will become a dominant issue to be carefully dealt with during the electroplating process. When the wafer cathode with millions of apertures is dipped into the solution, even some tiny air bubbles inside the apertures can potentially keep the solution isolated from the substrate. If the electrolyte could not wet the substrate at the bottom of these tiny wells sufficiently, as a consequence there may be no metal deposited in these areas. Therefore, full coverage or immersion of the electroplated areas across the whole wafer needs to be addressed in order to control the process for optimised

high consistency and uniformity. Also, when the electroplating parameters and variables become unstable in some local areas due to the uneven potential field, hydrogen gas bubbles may occur near the cathode surface. In addition, due to the nature of the surface in terms of its chemistry or contamination, degassing may occur which will also disturb the deposition process leading to a condition of difficult control for optimisation. There are therefore many factors which must be considered.

In this research, all the aspects which can affect the indium bumping process are taken into account during comprehensive experimental work. The research work focuses on the fundamental studies regarding the two main factors for the electroplating bumping process, which are current density and mass transport. The experiments include the following sections:

- Characterisation of the indium deposited through DC, unipolar pulse and bipolar pulse reverse electroplating using sulphamate solution. This is to build up a knowledge of indium deposition using sulphamate solution, which is lacking in the literature.
- Investigate indium electroplated bumping at various current densities and current waveforms. Both the direct current (DC) and pulsating current waveforms are employed in the electroplating processes.
- Study the influences of a novel agitation method on the mass transport condition during electroplating. Acoustic agitation up to megahertz range has been used to enhance the mass transfer and hence to affect the electroplating process.

1.4 Structure of This Thesis

In total there are 7 chapters in this thesis. The first chapter is to introduce the background information of ultrafine pitch interconnection which is used in the leading-edge pixel detector applications and indium bump bonding technology. The motivation of this research and the technical challenges are also discussed. Finally, aims and objectives are pointed out at the end of this chapter.

In this thesis, instead of an independent chapter, a literature review on a specific issue is given at the beginning of certain chapters. Chapter 2 and 3 explore the proper electrodeposition parameter window using DC, unipolar pulse electroplating and bipolar pulse reverse electroplating for indium bumping and

evaluate how the various current waveforms affect the bump deposition, respectively. The parameters suitable for DC, pulse and pulse reverse electroplating are optimised based on the results. Then, in chapter 4, the electroplating of indium at the wafer level to form indium bumps is described. The bump uniformity and yield are evaluated and the fundamentals of indium bump growth under various parameters are investigated. Chapters 2 to 4 mainly focus on the issues related to current density during the bumping process.

Chapter 5 investigates the influences of acoustic agitation on the mass transfer condition, and its effects on the indium bumping process. Low frequency ultrasonic agitation and 1 megahertz megasonic agitation are introduced into the electroplating bath. The experiments are conducted both on non-patterned substrates and at the patterned wafer level. The effects of acoustic agitation on the indium bump growth and microstructure are studied. Also, the influences of acoustic agitation on uniformity and yield of indium bumping through electroplating are investigated. In Chapter 6, a general discussion about the indium deposition and indium bumping using sulphamate solution is provided by integrating the experimental results and relevant studies in the literature. There will be only a limited discussion of the results in Chapters 2 to 5 while a complete discussion is given in Chapter 6. Finally, the conclusions from this research and suggestions for future works are given in Chapter 7.

Chapter 2 Indium Electrodeposition through Direct Current

2.1 Introduction

This chapter illustrates the experimental results of indium deposition from indium sulphamate solution under direct current (DC). The aim of this chapter is to identify the proper operation window for this bath for applications in the later experimental work. The basic principles of electrodeposition are introduced prior to the experimental details.

2.1.1 Basic Principles of Electrodeposition [40, 41]

It is known that the conduction of electric current in conductors could be electronic or ionic which depends on the movement of electrons and ions respectively. Electronic conduction is found in all metals while ionic conduction is found in electrolytes. In general, any ionic solid could be imagined as a unit cell in which many cations are surrounded by a number of anions, and the anions are also surrounded by a number of cations. According to the energy band theory, the band of levels corresponding to the merger of bonding electron orbits is known as the valence band which is usually completely filled, and the level corresponding to the non bonding electron orbits is named the conduction band which is usually only partially filled. Different materials' conduction bands have different Fermi energy levels. Thus, when two metals are contacted together, electrons will flow from the one with the higher Fermi level to the one with the lower Fermi level until the Fermi levels become equal in energy. By analogy, when a metal is immersed into a solution of ions, a similar situation will

occur to form a potential difference between them. Taking an example of copper and aqueous copper sulphate solution, when copper is immersed into copper sulphate solution, an electric potential difference is developed between the metal and the solution. Some of the copper ions will deposit onto the copper surface by accepting electrons from the metal conduction band thereby leaving the metal with a small positive charge (Equation 2-1). Meanwhile, the solution will gain a small amount of negative charge. This process is named the reduction process.

$$Cu^{2+} + 2e \rightarrow Cu \tag{2-1}$$

When it comes to more active metals such as zinc, some zinc atoms will leave the metal surface as ions and spontaneously give the solution a small positive charge (Equation 2-2). This process is named the oxidation process.

$$Zn \rightarrow Zn^{2+} + 2e \tag{2-2}$$

If the two parts of the cell are combined together via a salt bridge, which is referred to as the Daniell cell or zinc-copper couple, the reduction and oxidation processes will occur in separated places simultaneously. Conventionally, the electrode at which oxidation occurs is called the anode while the electrode at which reduction occurs is named the cathode. The copper atoms deposit on the cathode by withdrawing electrons from the zinc anode via an external lead. The overall cell reaction is given by Equation 2-3.

$$Cu^{2+} + Zn \rightarrow Cu + Zn^{2+} \tag{2-3}$$

For the Daniell cell, the cell potential is given by the Nernst equation (Equation 2-4).

$$E = E^{\Theta} + \frac{RT}{nF} \ln \frac{[Cu^{2+}]}{[Zn^{2+}]} \tag{2-4}$$

where E^{Θ} is the standard cell potential, related to the standard Gibbs free energy, R is the gas constant, T is the temperature, n is the number of electrons transferred during the process, F is the Faraday constant (96485 *C/mol*), $[Cu^{2+}]$ and $[Zn^{2+}]$ are the concentrations of copper and zinc ions respectively.

When an external potential, which is more than the cell potential calculated by the Nernst equation, is intentionally applied so as to make the zinc cathode and the copper anode, then the current flow could be reversed so that the zinc ions will

attempt to be deposited. If the external potential exactly balances the cell potential calculated by the Nernst equation, even though no apparent current will flow from the anode to cathode, there will still be current flows at each electrode, but they are equal. This current is named as the exchange current. A system with a high exchange current density has fast reaction kinetics and could respond to a potential change rapidly. Thus, electrodeposition is realised.

According to Faraday's law in electrochemistry, the total amount of chemical change on an electrode surface is proportional to the quantity of electrical charge passing through the circuit. However, only the reactions for depositing the desired metals are of interest while the other side-reactions are considered as waste. So, an index called the cathodic current efficiency (CCE) is adopted to describe how effectively the electroplating bath performs. The current efficiency is defined as the ratio of the desired chemical change to the overall chemical change. In theory, the mass of electroplated metal is determined by:

$$m = \left(\frac{Q}{F}\right)\left(\frac{M}{z}\right) = \left(\frac{It}{F}\right)\left(\frac{M}{z}\right) \tag{2-5}$$

where m is the mass of the substance altered at an electrode, Q is the total electrical charge, F=96485 *C/mol* is the Faraday constant, M is the molar mass of the metal, z is the valence number of the reaction ions, I is the total current flowing through the electrolyte, and t is the electroplating time. In practice, a high current efficiency is demanded for a cost-effective electroplating process.

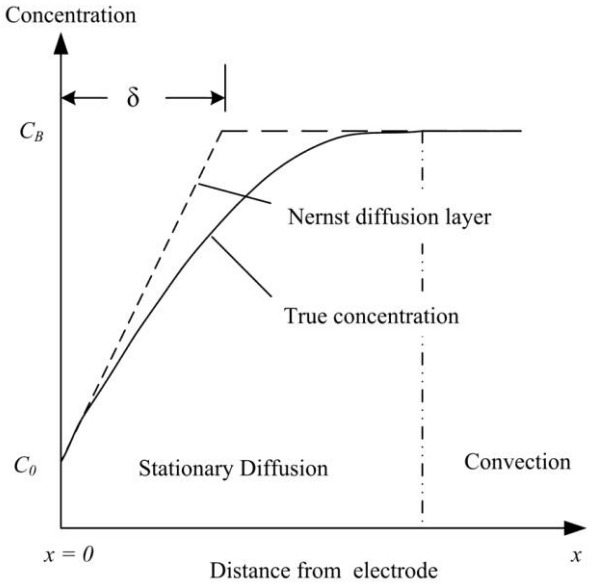


Figure 2-1 Schematic of the diffusion layer close to the electrode surface in DC electroplating.

When an electrode is immersed into the solution, a concentration gradient of the reacting species is established near the solid surface. As demonstrated in Figure 2-1, the concentration of the reactants gradually decrease from the bulk solution (C_B) to the electrode surface (C_0). A Nernst Diffusion Layer (δ) is often used to replace the true gradient close to the electrode so that the concentration deceases linearly to the surface. Thus, the current density can be derived as:

$$i = zFD\left(\frac{\partial C}{\partial x}\right)_{x=0} = zFD\frac{C_B - C_0}{\delta} \tag{2-6}$$

where D is the diffusion coefficient of the reactants. When the C_0 becomes zero, *i.e.* the reactants on the cathode surface are completely consumed, the value corresponding to the maximum gradient is called the limiting current density (i_L) which can be derived as:

$$i_L = zFD\frac{C_B}{\delta} \tag{2-7}$$

When the electrodeposition is conducted at the limiting current density, the reacting species will be reduced as soon as it reaches the cathode surface, and the reaction is therefore controlled by the diffusion.

During the electroplating process, the electrode potential will differ from the equilibrium value and thereafter an overpotential is formed:

$$\eta = E(I) - E(eq) \tag{2-8}$$

where the *E(I)* is the potential when current is flowing and *E(eq)* is the equilibrium potential. For any reduction reaction to take place, the overpotential is essential to overcome the kinetic barrier which the reactants must possess. The overpotential required to start the reaction is called the activation overpotential or charge-transfer overpotential for which the reaction is controlled by charge transfer. More often, during the deposition process, the consumed ions cannot be replenished as fast as they are deposited, then a concentration gradient of the reactants is established resulting in a concentration overpotential, hence the mass transfer plays a role in deposition.

The relation between current density and charge-transfer overpotential is determined by Butler-Volmer equation:

$$i = i_0 \left[\exp\left(\frac{(1-\alpha) zF\eta}{RT} \right) - \exp\left(-\frac{\alpha zF\eta}{RT} \right) \right] \tag{2-9}$$

where the i_0 is the exchanging current density, α is the charge transfer coefficient, R is the gas constant, T is the temperature and F is the Faraday constant. It can be seen that the overpotential increases with current density.

Linear sweep voltammetry is usually employed to investigate the relationship between the electrode potential and current density. Figure 2-2 plots an idealised polarisation curve for electrodeposition. When the current density is relative low, the reaction is mainly controlled by charge transfer and the deposits are likely to be deposited as ridges and blocks. When the current density moves towards the limiting value, the influences of mass transfer become more important and the morphology of the deposit tends to be nodular or even powdery.

The current distribution is often noteworthy because it can affect the uniformity of the deposits. The current distribution is usually categorised as primary, secondary and tertiary. The primary current distribution is determined by the geometrical configuration of the electroplating system, *e.g.* the size of the electrodes and the distance between them. The secondary current distribution prevails when the activation overpotential is taken into account while the tertiary current distribution prevails when the concentration overpotential is concerned. Moreover, a concept of throwing power is usually used to describe the ability of an electrolyte to give rise to a uniform deposit despite the geometrical irregularities on the cathode surface.

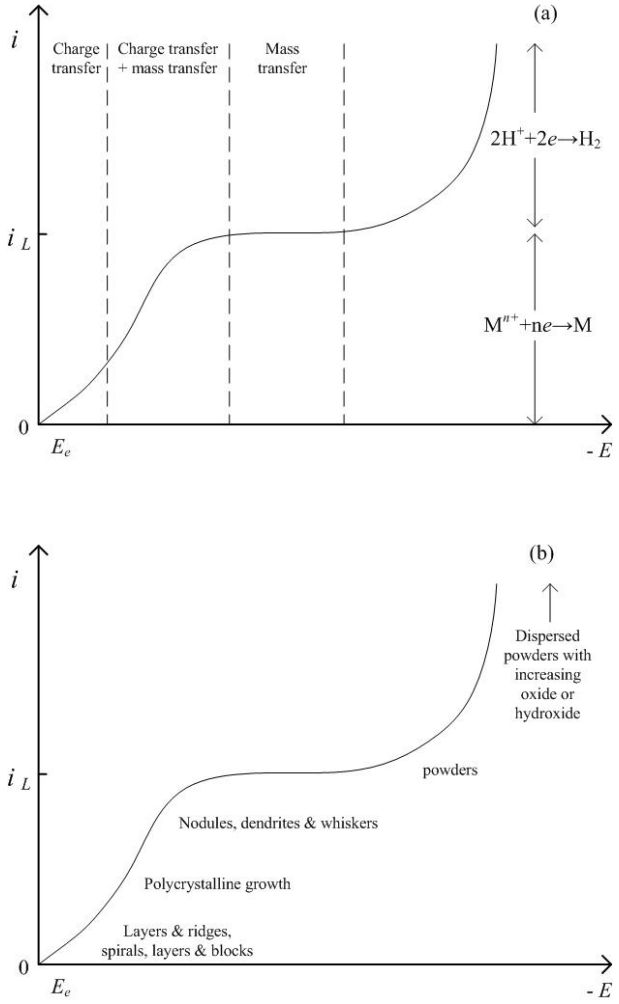


Figure 2-2 Idealised steady state current density versus electrode potential curve for metal deposition: a) Showing the various regions of kinetic control; b) Indicating the regions of various growth morphologies [42]. (From F. C. Walsh, and M. E. Herron, "Electrocrystallization and electrochemical control of crystal growth: fundamental considerations and electrodeposition of metals," Journal of Physics D: Applied Physics, vol. 24, no. 2, pp. 217-225, 1991. © 1991 IOP Publishing Ltd. Reproduced with permission)

Organic additives are usually added into the electrolyte in small quantities, but can significantly affect the deposition process. The potential benefits of organic additives include grain refinement, increase of the electroplating parameter window, levelling of the deposit, increase in the current efficiency, brightening of the deposits, change in the mechanical properties of deposits, and reduction of the tendency for dendrite growth [43, 44].

2.1.2 Background to Indium Electroplating

2.1.2.1 Chemical Properties of Indium

Indium reacts directly with arsenic, antimony, the halogens, oxygen, phosphorus, sulphur, selenium and tellurium when heated. Metallic indium is not oxidized by oxygen at room temperature, but it reacts with oxygen at higher temperature to form indium trioxide (In_2O_3). It dissolves very slowly in cold dilute mineral acids and more actively in hot dilute or concentrated acids. Alkalis and hot water do not attack the bulk metal, but, finely divided indium reacts with water to form the hydroxide.

The only stable indium ion in aqueous solution is the In(III) ion and the standard electrode potential (E^{Θ}) of indium relative to the standard hydrogen electrode is [33, 45]:

$$In^{3+}(aq) + 3e = In\ (m), \qquad E^{\Theta} = -0.34\ V. \tag{2-10}$$

2.1.2.2 Indium Electroplating Solutions

Indium has been successfully electroplated onto a number of metals, such as lead, zinc, copper, cadmium, nickel, tin, precious metals and iron. Both acid and alkaline solutions can be used for indium electrodeposition. The acid solutions include sulphate, sulphamate, fluoborate, chloride and perchloride. The alkaline solutions usually contain many chemicals including cyanide and tartrate [46-49]. In general, the acid baths are easily prepared and stable and offer higher cathode current efficiencies while the alkaline solutions feature superior throwing power. Currently, cyanide, sulphate, sulphamate and fluoborate solutions have been more widely used, while other solutions, such as indium chloride, do not appear to have been used much in industrial applications. A review of the operation details of the former four types of solutions will be demonstrated below.

Cyanide Solutions: Indium is the only trivalent metal that could be readily electrodeposited from a cyanide solution. The first commercial indium electroplating bath was a cyanide formulation developed to plate bearing surfaces in the late 1930's. To make up the cyanide solution, indium hydroxide ($In(OH)_3$) was firstly precipitated by dropping ammonium hydroxide or sodium hydroxide into indium chloride ($InCl_3$). After purification, the dried $In(OH)_3$ was then dissolved in an alkaline cyanide

solution and stabilised by a sugar such as D-glucose, dextrose or sorbitol. The cyanide solution is used in applications requiring extremely high throwing power and adhesion. Since the cyanide is a high pH bath, insoluble anodes are required and it is necessary to replenish the indium metal by adding indium cyanide frequently. The cathode efficiency is initially about 90%, but it decreases to about 50-75% as the bath ages rapidly. The disadvantages of cyanide based solutions also include the difficulties of preparation of the hydroxide feedstock and the serious toxicity during the electrodeposition process and resultant disposal [47, 50].

Sulphate Solutions: Acid sulphate solutions have been extensively studied and widely used because of their relative simplicity. Normally, the electrolyte just consists of $In_2(SO_4)_3$ without addition agents. Generally, soluble anodes, *i.e.* pure indium metal, are utilised at about 100% anode efficiency; however, the cathode efficiency is usually within 60-80%, so, the indium concentration will slightly increase during the electroplating process. Hence, either a combination of soluble and insoluble anodes, *e.g.* a split In-Pt anode with area ratio of 70 to 30, is required, or the electrolyte must be diluted with water or removed periodically to keep the composition stable [46, 51].

Sulphamate Solutions: Indium sulphamate solution was developed to overcome several disadvantages of the cyanide bath. Soluble anodes are normally employed and possess a relatively constant cathode efficiency of 90% which remains stable during the life of the bath. Sulphamate baths are very stable compared to others and are considered as one of the easiest baths to control and operate. The preferred pH value is between 1.5 to 2.0. When the pH rises to more than 3.5, a milky white precipitate of indium hydroxide occurs as a 'built-in' pH indicator. Moreover, the indium sulphamate baths possess a throwing power only slightly less than the cyanide bath and the deposit are normally uniform and bright matte in appearance. At the end of electroplating, indium is easily recovered as indium hydroxide by adjusting the pH to more than 5.0 with sodium hydroxide. The sulphamate electroplating bath is commercially said to be the 'best' one for indium electroplating [52].

Fluoborate Solutions: The fluoborate bath features the promising ability to obtain very fine-grained deposits. Meanwhile, the fluoborate solution has the advantages of simple formulation from a stable concentration, and low fluctuations in bath composition. The bath employs pure indium anodes at hundred percent anode efficiency and the pH is controlled by additions of fluoboric acid to the range of 0.5 to

1.5. The main shortcoming of this bath is the low cathode efficiency usually of 40-75%. Hence, like the sulphate solution, a split cathode system, indium and platinum, is usually employed to balance the difference between anode and cathode efficiencies [50].

Table 2-1 Characteristics of cyanide, sulphate, sulphamate and fluoborate indium solutions [50].

Types	*Operation temperature*	*Cathode efficiency*	*Throwing power*	*Anode*	*Wettability*	*Toxicity*	*Maintenance*
Indium Cyanide	Room temperature	50-75%	Excellent	Steel	Easy	Very high	Difficult
Indium Sulphate	Room temperature	30-70%	Poor	In-Pt	Difficult	Modest	Normal
Indium Sulphamate	Room temperature	90%	Excellent	Pure Indium	Easy	Modest	Easy
Indium Fluoborate	21-32 ºC	40-75%	Good	In-Pt	Difficult	Modest	Easy

Table 2-1 lists the characteristics of these four types of indium electroplating solutions. Cyanide solution should normally be avoided due to the cyanide toxicity problems, although it offers very good quality of deposit. The sulphate electrolyte is the simplest one; however, it necessitates the split anode system which will increase the control complexity for a wafer bumping process. Also, the fluoborate based solution is less attractive for the electroplating bumping process due to the low cathode efficiency. In contrast, indium sulphamate solution offers high deposition efficiency, easy maintenance, and long operation life. So, considering all the aspects, sulphamate solution is the most suitable one for indium electrodeposition and was employed in this research.

2.2 Experimental Details

The electrodeposition of indium was conducted using an indium sulphamate based solution, which was supplied by the Indium Corporation of America®. The ready-to-use solution is stable, easy to maintain and operate and has an excellent throwing power and a wide latitude of operational parameters. The electroplating operates at room temperature. Table 2-2 summarises the formulation and other features of the electrolyte. A pure indium (99.99%) plate with 2 × 2.5 cm^2 in area was employed as the anode, having 100% anodic current efficiency [50], whilst 2 × 2 cm^2 copper sheet

acted as the cathode substrate. Preparation of the substrates consisted of two separate steps, cleaning and activation. The substrate was first alkaline soaked to remove oils, grease and other soils from the surface by using a solution consists of NaOH, Na_2CO_3 and Na_3PO_4. Then it was acid activated by immersion into 10% sulphuric acid (volume percent, specific gravity of 1.83, supplied by Fisher Scientific) at room temperature for 5 minutes followed by deionised water rinse. After that, the base metal was immersed into 5 *wt*% sulphamic acid solution for 1-3 minutes. This was to protect the indium sulphamate electroplating bath from drag-in of the etching chemicals from the previous step. The anode and cathode were perpendicularly dipped into the bath facing each other (Figure 2-3*a*). No extra agitation was applied. The primary experiments were conducted in a beaker containing about 250 *mL* solution. The current was generated by a Potentiostat (PARSTAT 2273, Ametek). All of the electroplating trials were carried out at room temperature as the indium sulphamate solution had the risk to decompose at high temperature as informed by the supplier. Figure 2-3*b* shows the actual set-up for indium electroplating experiments.

Table 2-2 Composition and features of indium sulphamate solution supplied by Indium Corporation of America [53]

Indium sulphamate	105.36 g/L
Sodium sulphamate	150 g/L
Sulphamic acid	26.4 g/L
Sodium chloride	45.84 g/L
Dextrose	8.0 g/L
Triethanolamine	2.29 g/L
Temperature	Room temperature
pH	1.0-3.5 (1.5-2.0 preferred)
Colour of solution	Clear

Due to protection of commercial interests, very little information about indium electroplating using a sulphamate solution can be found in the literature. To understand how the solution performs during the electroplating process, a cathodic potentiodynamic polarisation was conducted in the potential range between the open

circuit and about -2.0 *V* vs. standard calomel electrode (SCE). The potential was scanned at a rate of 0.5 *mV/s* and the corresponding current density was recorded. Then a proper electroplating parameter range was established on the basis of the cathodic polarisation curve. The process was established in the 250 *mL* bath scale and a series of indium electrodeposition trials were then carried out under various parameters.

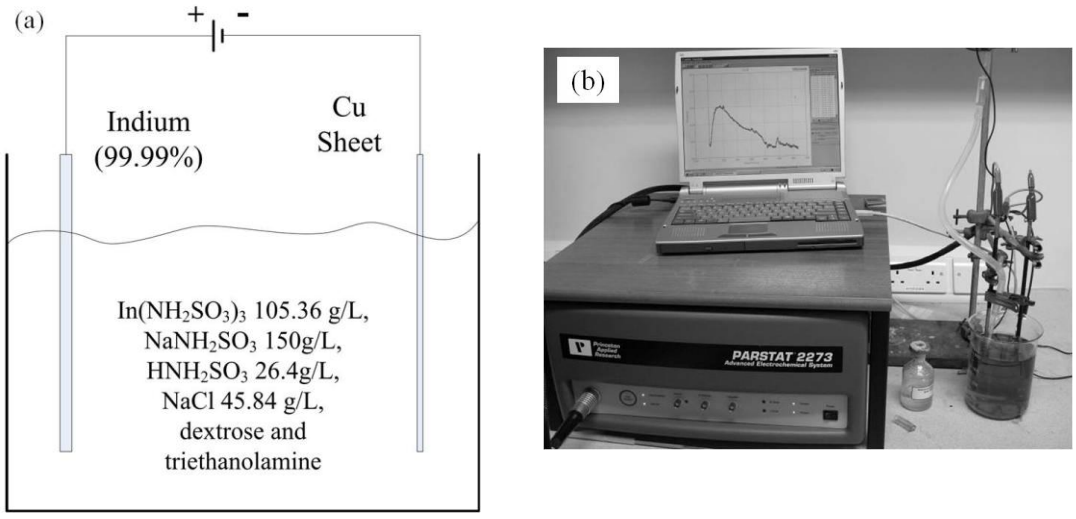


Figure 2-3 Configuration of indium electroplating bath: (a) schematic structure; (b) the actual experimental set-up.

The surface morphology of electroplated indium were characterised by Scanning Electron Microscopy (SEM). The surface roughness of electrodeposited indium was measured by a Talysurf CLI 2000 non-contact surface profiler (from Taylor Hobson, see Figure 2-4*a*). The surface undulation was obtained through the optical interference pattern produced by the scanning unit. A 200 μm × 200 μm area was selected on each sample and scanned following the format shown in Figure 2-4*b*. The step spaces were 0.5 μm in the *X* direction and 20 μm in the *Y* direction, therefore there were overall 11 line scan in the area. The measurement accuracy was ±0.01 μm and an averaged surface profile was generated afterwards on the basis of the 11 line profiles. The Total Height of Profile (P_t) stands for the height difference between the highest peak and lowest valley within a specific line profile. The Average Roughness (R_a) is the arithmetic average value of the absolute vertical deviation from the mean

line within a specific line profile. P_t and R_a were investigated as the two main parameters regarding to the surface roughness.

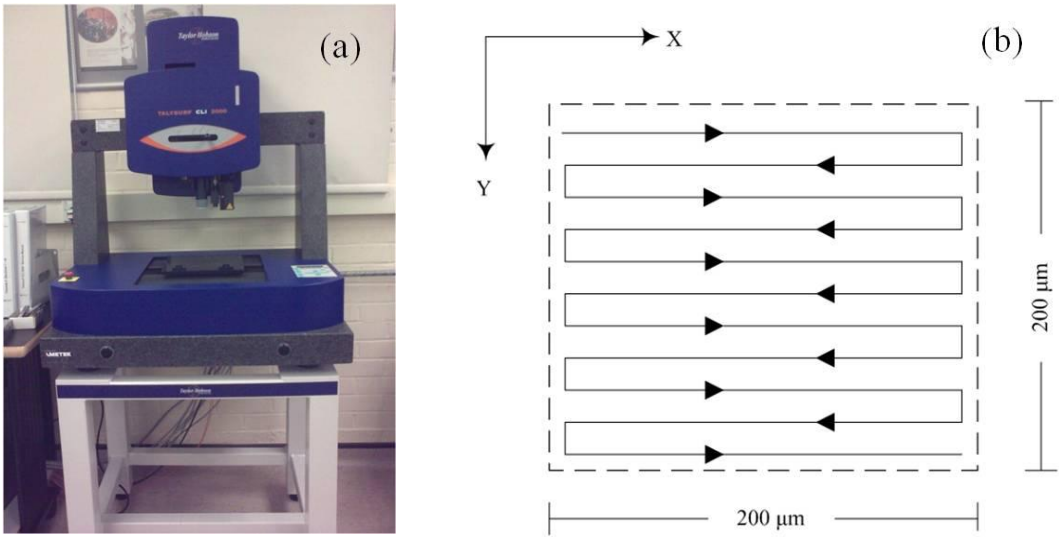


Figure 2-4 (a) Set-up of the Talysurf CLI 2000 surface profiler; (b) Scanning format of the electroplated indium surface profile.

2.3 Electrochemistry of Indium Sulphamate Solution

To understand how the indium sulphamate solution performs during the electroplating process, a cathodic polarisation was conducted at a small volume scale (approximately 200 *mL*). The configuration of the electrochemical circuit is shown in Figure 2-5. A saturated calomel electrode (SCE) was employed as reference while the external potential was scanned from the open circuit to -2.0 *V* (vs. SCE) at a speed of 0.5 *mV/s*. The SCE reference electrode has a potential of +0.241 *V* against the standard hydrogen electrode (SHE). Because of the distance between the reference electrode and cathode was kept within 1~2 *cm*, the potential drop within the electrolyte could be ignored. Moreover, because the solution is very sensitive to cupric ions, the polarisation was only investigated in the minus potential range to avoid any copper being dissolved into the solution.

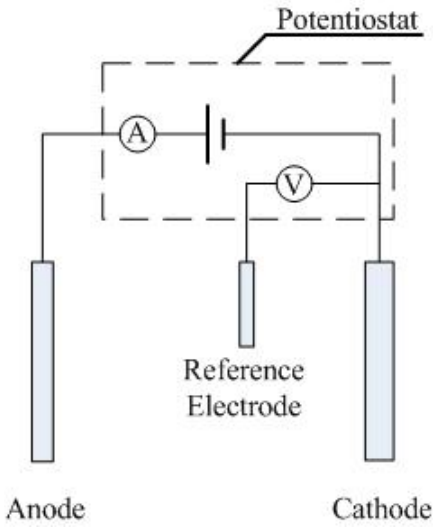


Figure 2-5 Configuration of the measurement circuit during the potentiodynamic cathodic polarisation process in the indium sulphamate system with indium anode and copper cathode.

Figure 2-6 plots the relative cathodic potential against the current density. When the external potential was applied, indium deposition on the cathode face did not start immediately. A so-called activation overpotential needs to be built-up to begin the reduction of metal ions. According to Figure 2-6, indium deposition started when the cathodic potential was over approximately -650 *mV*. The current density dramatically increased with the potential until it reached about 30 mA/cm^2 when the cathodic potential was about -1000 *mV*. Then the current density dropped although the potential kept rising. As the current density decreased with the increasing potential, hydrogen bubbles were observed on the cathode surface. After that, indium deposition accompanied with hydrogen evolution occurred and the current-potential curve became unstable. Therefore, it can be seen that the highest current density can be reached before hydrogen evolution occurs is 30 mA/cm^2.

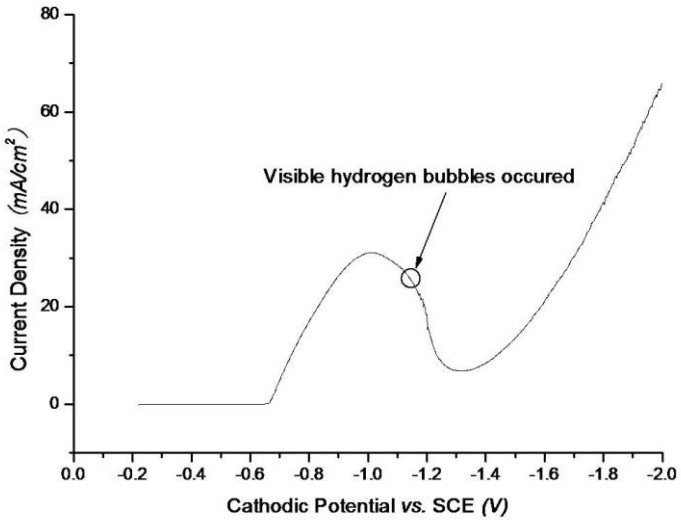


Figure 2-6 Cathodic polarisation curve obtained in indium sulphamate solution using indium anode and copper cathode at room temperature without agitation (by scanning from open circuit to -2.0 *V* against SCE at scanning rate of 0.5 *mV/s*).

2.4 Results of Indium Deposition Through DC Electroplating

On the basis of the cathodic polarisation, a proper indium electroplating current density operation range can be worked out. Considering the intended application, it is undesirable to deposit indium accompanied by hydrogen evolution. On the one hand, the current efficiency is compromised by hydrogen evolution so that the reaction status is not stable which can cause the electroplating process to be less-controlled. On the other hand, in the application of ultra-fine pitch indium bumping, the presence of any gas bubble may interrupt the coverage of the solution into micro-scale patterns, obstruct the deposition into deep apertures, increase the possibility of defects, and finally reduce the yield. So, to find out the influence of current density on the electroplated indium microstructure, a series of galvanic indium electroplating trials were conducted below and above 30 mA/cm^2 as previously indicated in the cathodic polarisation curve. Table 2-3 summarises the experimental parameters used in these trials of indium electrodeposition. All the electroplating experiments were conducted without the presence of any type of agitation at room temperature. Moreover, all of

the electroplating trials were conducted through the same Coulomb of electron charge, *i.e.* 10 mA/cm^2 for 60 minutes and 20 mA/cm^2 for 30 minutes etc.

Table 2-3 Parameters of DC electrodeposition of indium onto copper substrate using sulphamate solution and indium anode at room temperature without additional agitation

Expt. No.	*Current Density*
1	5 mA/cm^2
2	10 mA/cm^2
3	15 mA/cm^2
4	20 mA/cm^2
5	25 mA/cm^2
6	30 mA/cm^2
7	35 mA/cm^2
8	100 mA/cm^2

As mentioned above, the anodic current efficiency is treated as 100% because of the usage of a pure indium anode. To determine the cathodic current efficiency (CCE), the samples were weighed before and after electroplating by using a Mettler Toledo XS205 DualRange analytical balance with accuracy up to 0.01 *mg*. Thus, the CCE was calculated by:

$$CCE = \frac{actual\ weight}{theoretical\ weight} \times 100\% \tag{2-11}$$

The theoretical weight was calculated by Equation 2-5. The cathodic current efficiencies corresponding to various current densities are illustrated in Figure 2-7. The cathodic current efficiencies were over 90% when the current density increased from 5 mA/cm^2 to 20 mA/cm^2. When the current density was 25 mA/cm^2, the cathodic CCE decreased to 80%. Further, when the current density reached 30 mA/cm^2, the current efficiency deteriorated to below 40% and continuing hydrogen bubble evolution was observed at the cathode surface. After that, the current efficiency continuously decreased while the current density increased. Moreover, by measuring the weight change after electroplating, it was calculated that the deposition rate was about 0.3 μm per minute, when the current density was 10 mA/cm^2.

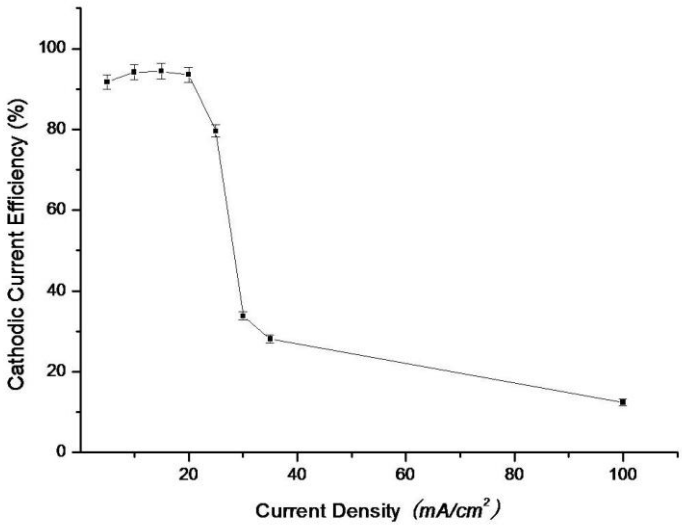
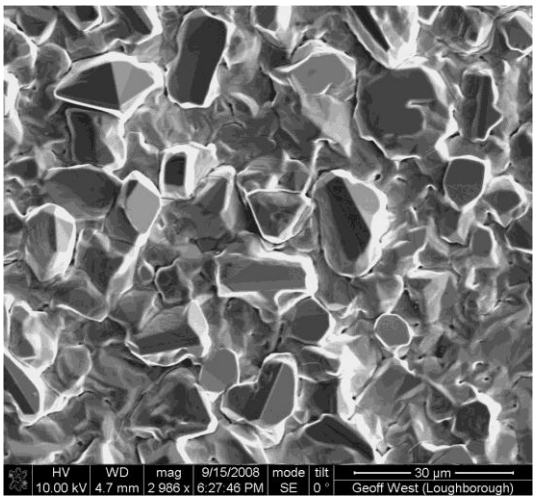
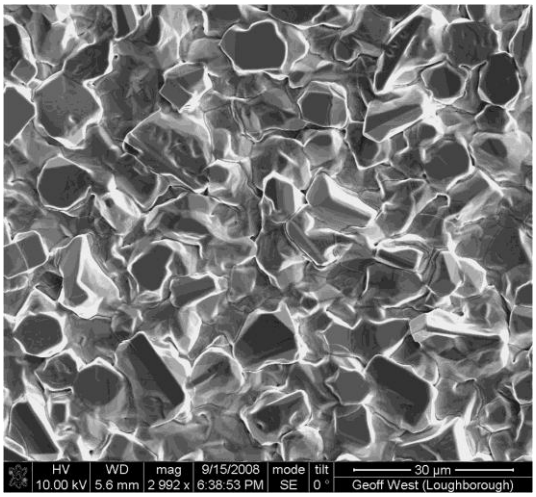


Figure 2-7 Cathodic current efficiencies corresponding to various current densities for the DC electroplating of indium onto copper substrate using sulphamate solution at room temperature without additional agitation.

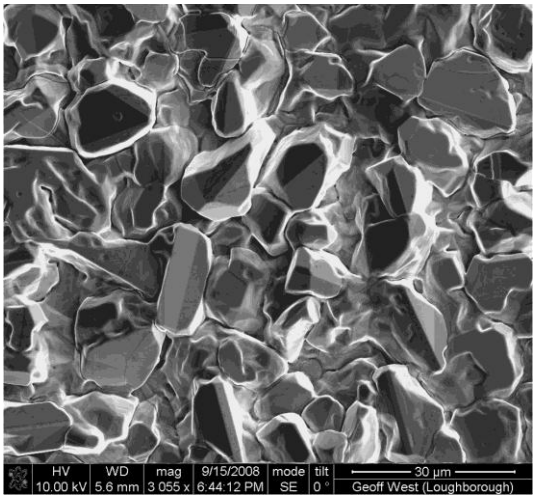
To the naked eye, the overview of the electroplated indium appeared neither smooth nor shiny, and had noticeable roughness with a frosted or matt-like finish. Figure 2-8 shows the SEM images of surface morphology of the DC electroplated indium deposited under various parameters. It can be seen that granular growth is dominant when the current density is below the limiting value. When the current density falls into the 5 – 20 mA/cm^2 range, the deposits tend to grow rather than create new nuclei and grains with as large as 10 μm surface feature size can be easily identified. With the increase of the current density over 25 mA/cm^2, more pinholes can be found in the deposit which is further evidence of the hydrogen evolution (indicated by the arrows in Figure 2-8*e*). Further, in the case of the current density of 35 mA/cm^2, the deposit loses the crystalline feature and contains many defects corresponding to very low cathodic current efficiency (Figure 2-7). In the extreme condition, a dendritic structure was obtained at 100 mA/cm^2 while the current efficiency was only about 14%.



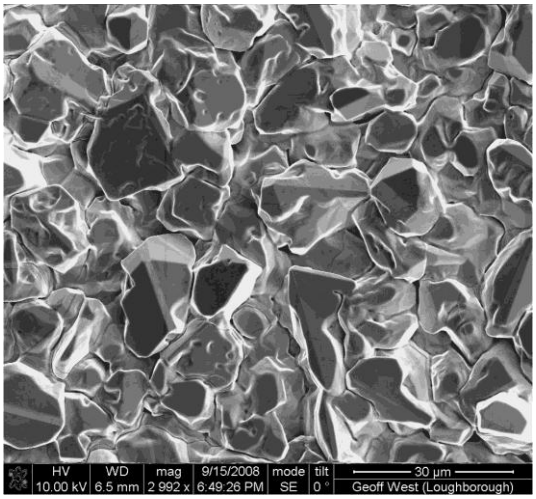
(a) $i = 5\ mA/cm^2$



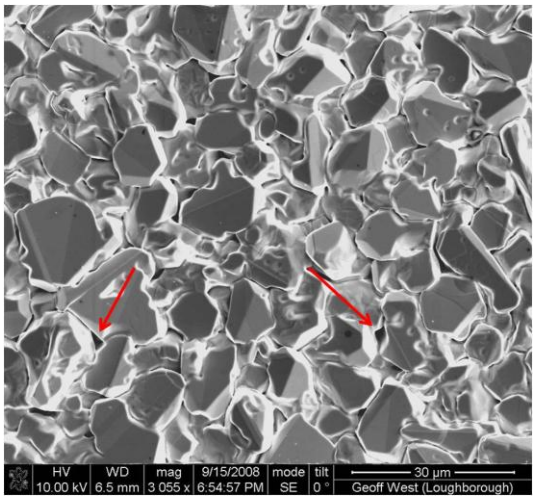
(b) $i = 10\ mA/cm^2$



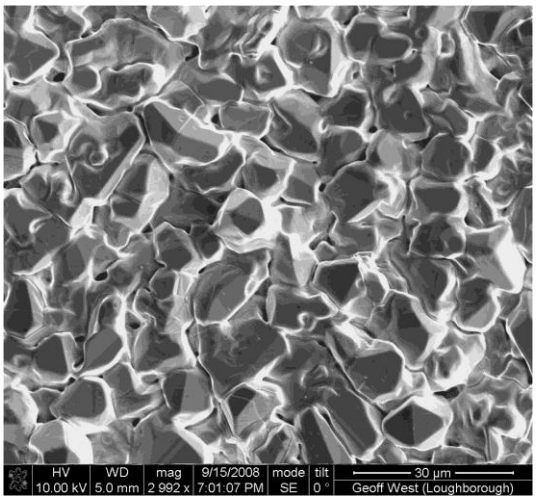
(c) $i = 15\ mA/cm^2$



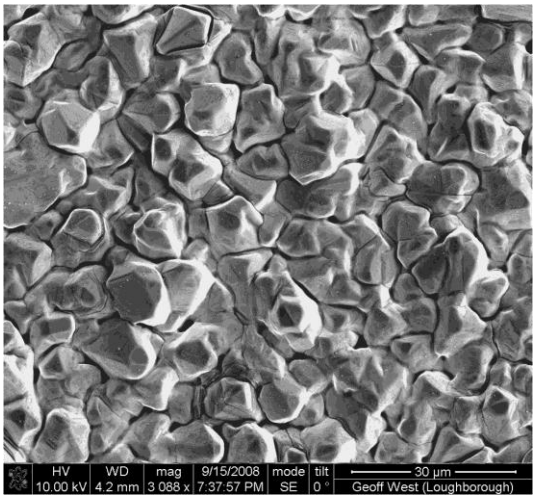
(d) $i = 20\ mA/cm^2$



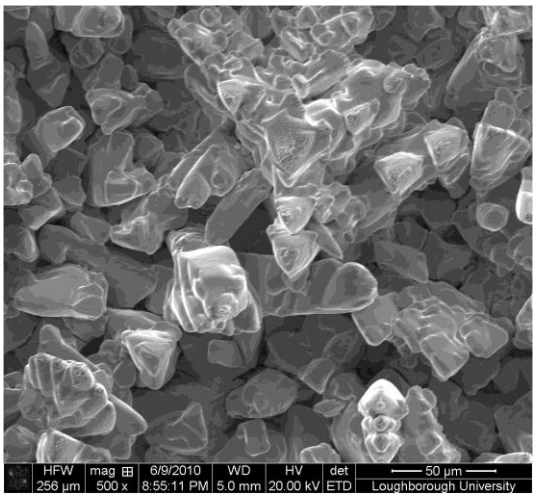
(e) $i = 25\ mA/cm^2$



(f) $i = 30\ mA/cm^2$



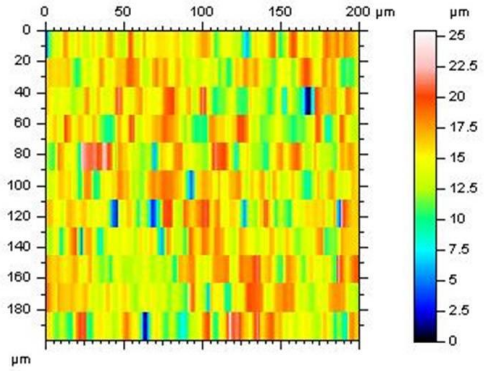
(g) $i = 35\ mA/cm^2$



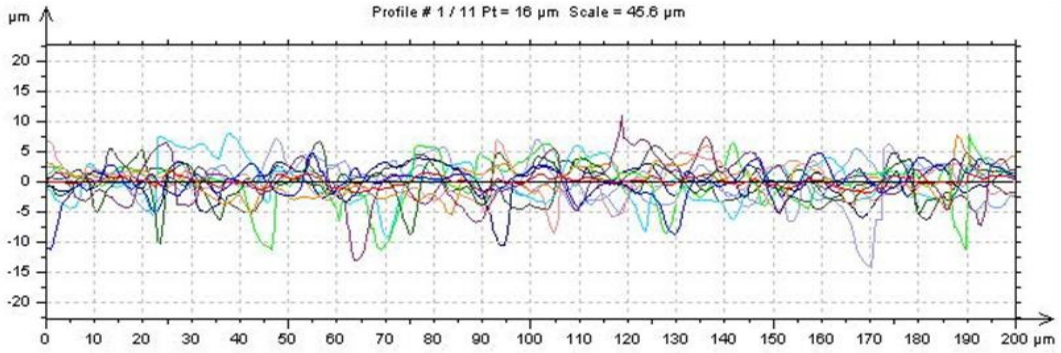
(h) $i = 100\ mA/cm^2$

Figure 2-8 Surface morphology of DC electroplated indium on copper substrate at various current densities using sulphamate solution at room temperature without additional agitation.

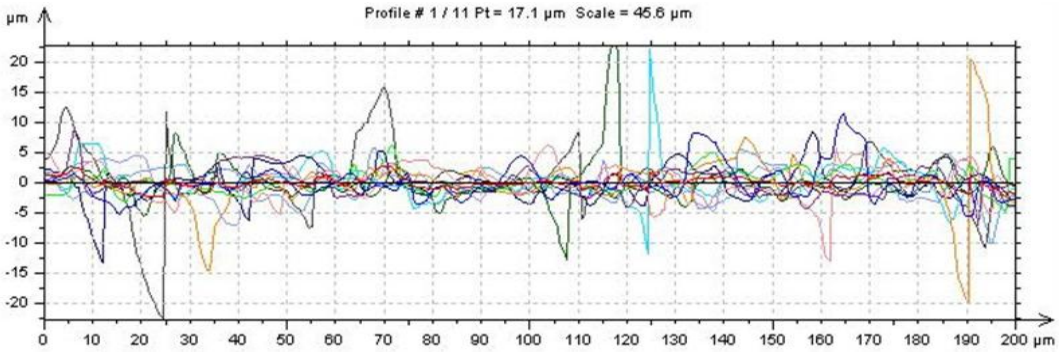
Figure 2-9 illustrates the surface uniformity of indium through DC electroplating at 10, 15 and 20 mA/cm^2 current densities as measured using the Talysurf CLI 2000. The contour map illustrates the distribution of data of the total 11 line profiles collected from the surface (Figure 2-9*a*). The measured maximum Total Height of Profile (P_t) was about 24 μm, 40.7 μm, and 34.3 μm respectively. Meanwhile, the measured Average Roughness (R_a) values were about 2.89 μm, 2.68 μm, and 3.88 μm respectively for the three current densities. The large value of P_t reflects noticeable non-uniformity on the electroplated indium surface.



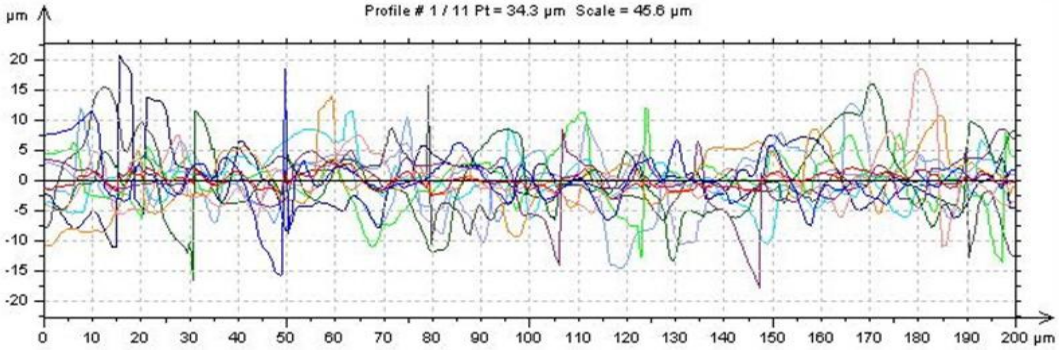
(a) Contour map of surface profile, DC 10 mA/cm^2.



(b) DC, 10 mA/cm^2, maximum P_t = 24 μm, R_a = 1.92 μm.



(c) DC, 15 mA/cm^2, maximum P_t = 40.7 μm, R_a = 2.24 μm.



(d) DC, 20 mA/cm^2, maximum P_t = 34.3 μm, R_a = 2.69 μm.

Figure 2-9 Surface roughness measurement of DC electrodeposited indium in sulphamate solution at current densities of 10, 15 and 20 mA/cm^2.

2.5 Summary

Primary experiments of indium electrodeposition through application of direct current were conducted at the lab-scale. The normal electroplating parameter range was worked out via the potentiodynamic cathodic polarisation results. A highest current density of 30 mA/cm^2 was identified. Electroplating trials were carried out to investigate the morphology and microstructure of the deposits. On the basis of the results, to obtain indium deposits at high cathodic current efficiency, it is suggested to operate the electroplating with the current density ranging from 5 to 20 mA/cm^2 in the future. Moreover, the deposition rate was measured as 0.3 μm per minute when the current density was 10 mA/cm^2.

Chapter 3 Indium Electrodeposition Through Pulsating Current Waveforms

3.1 Introduction

Following the earlier results on DC electroplating, this chapter describes an investigation of the influences of pulsating current on indium electrodeposition. In order to take advantage of the pulsating current waveforms, various unipolar pulse and bipolar pulse reverse current waveforms with constant average current were applied to alter the deposition process and its influence on the microstructure, surface morphology and surface uniformity. The basic fundamentals of pulse electroplating are introduced prior to demonstrating the experimental details and results.

3.1.1 Background to Pulse Electroplating

Pulse electroplating is defined as the deposition of metals by a periodic variation of current or voltage. In general, pulse electroplating is divided into ordinary pulsed current electroplating and periodic reversal current electroplating, or unipolar waveforms and bipolar waveforms, and the electrodeposition can be either galvanostatic or potentiostatic. Pulse electroplating makes use of an almost unlimited number of waveforms constructed by a number of independent combinations of anodic/cathodic current and duration of pulses compared to DC electroplating for which the current density represents the only independent parameter. The pulse electroplating technology has the highest degree of freedom to utilise special conditions during electrodeposition. Figure 3-1 illustrates a few examples of pulsating current waveforms. However, the large range freedom of pulse electroplating parameters induces a high degree of complexity to implement the pulsating current for

an application. The main features of typical pulse current and pulse reverse waveforms are shown in Figure 3-2. In the case of the unipolar pulse current (Figure 3-2*a*), i_p is the peak current density which is an important factor in pulse electroplating. t_{on} represents the duration of the peak current and t_{off} stands for the period that there is no current applied. The average current density can be calculated by:

$$i_{avg} = i_p \times \frac{t_{on}}{t_{on} + t_{off}} \tag{3-1}$$

The duty cycle (φ) is defined as $\varphi = [(t_{on}/(t_{on} + t_{off}))\times 100\%]$. In the case of bipolar pulse reverse electroplating (Figure 3-2*b*), the average current density is defined by:

$$i_{avg} = \frac{(i_{p(c)} \times t_{on(c)}) - (i_{p(a)} \times t_{on(a)})}{t_{on(c)} + t_{on(a)} + t_{off}} \tag{3-2}$$

where $i_{p(c)}$ and $i_{p(a)}$ are the peak current densities of the cathodic and anodic cycles respectively; $t_{on(c)}$ and $t_{on(a)}$ are the pulse-on time of the cathodic and anodic cycles respectively. In this case, the duty cycle is defined as $[(t_{on(c)}/(t_{on(c)} + t_{on(a)} + t_{off})) \times 100\%]$. Although the waveform varies with the peak current density and the pulse duration, the actual deposition rate is determined by the average current density according to Faraday's law.

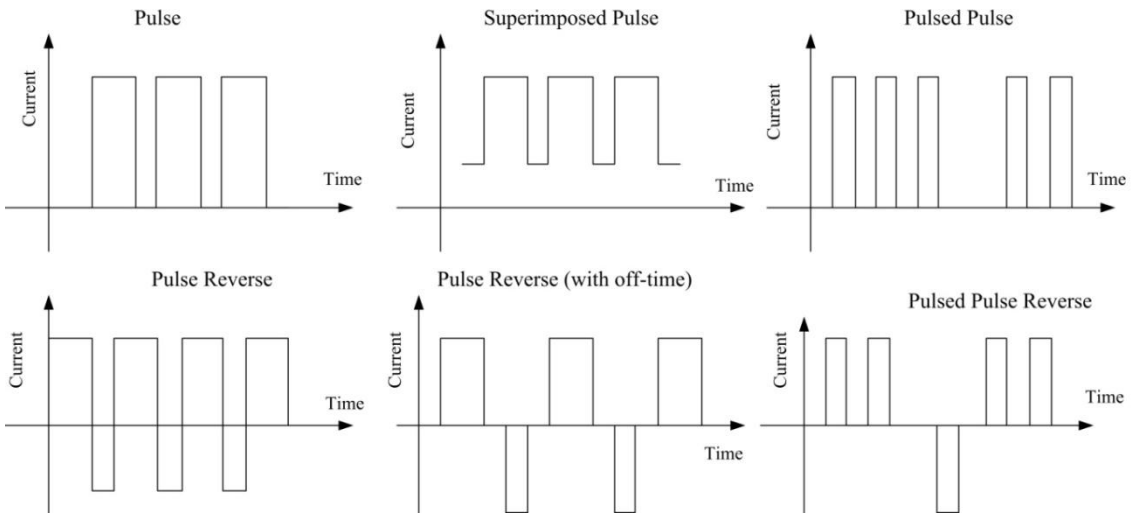


Figure 3-1 Schematic diagrams of various pulsating current waveforms [54].

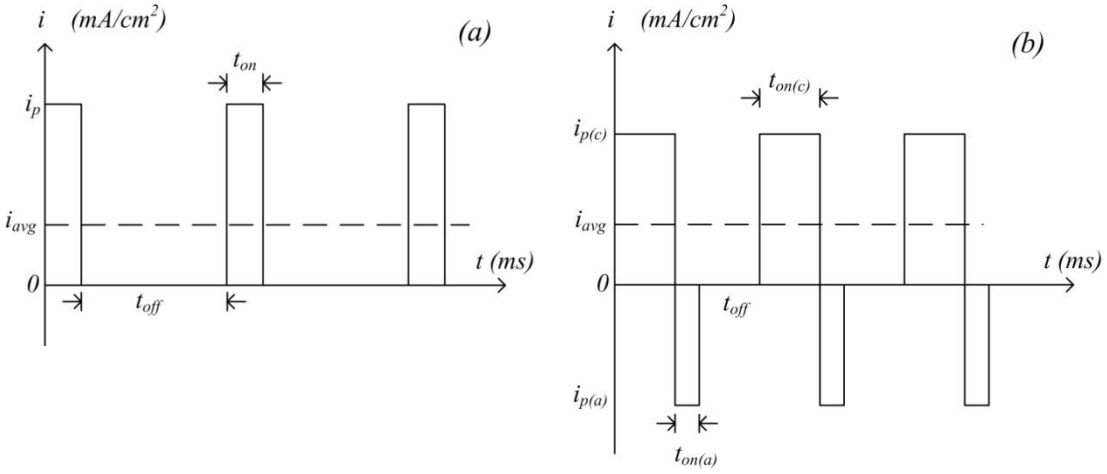


Figure 3-2 Features of typical unipolar pulse current and bipolar pulse reverse waveforms.

It is known that an electrical double layer will be formed at the electrode-electrolyte interface, which features two parallel layers of charge in the immediate vicinity of the interface. The electric double layer could be approximated to a plate capacitor with a resistance within a distance of a few angstroms and therefore with a high capacitance. Based on the theoretical calculation and approximation, the charging and discharging time would be in the order of microseconds [55]. For the DC electroplating condition, the charging time can be ignored compared with the long lasting constant current application time. During the pulse electroplating process, it is crucial to formulate the waveforms with consideration of the charging and discharging of this electric double layer, when the pulse is generated. In general, for practical applications, the charging time should be much shorter than the pulse duration, and the discharging time should also be much shorter than the off-time between two current pulses. Otherwise, the current waveform will be strongly distorted due to the capacitance effect.

Another issue concerns mass transport, which plays a significant role in terms of the deposit quality, microstructure and productivity. In pulse electroplating with shorter pulse durations compared to DC electroplating, two distinct cathodic diffusion layers will be established instead of only one as in DC (Figure 3-3). During the pulse electroplating process, the concentration of the metal ions near the vicinity of the cathode decreases during the pulse on-time and relaxes during the off-time corresponding to the pulsating current frequency. When the duration of the pulse is

short, the pulsating diffusion layer does not have chance to extend very far into the bulk solution and, in particular, it is unable to extend to the region under the control of convection. During the off-time, metal cations will be supplied towards the cathode through the outer stationary diffusion layer, and this allows the relaxation of the pulsating diffusion layer. In the pulsating diffusion layer, the depletion of the metal ions limits the pulse peak current density, while the depletion of the metal cations in the stationary diffusion layer limits the average current density. Since the concentration gradient in the pulsating layer could be very high, the pulse current density is able to reach extremely high values with shorter pulse duration. When a pulsed current is applied, the pulse could last until the concentration of the reacting species reaches zero, and this duration is called the transition time. This transition time manifests itself experimentally by a sudden increase of the electrode potential which leads to an additional cathodic reaction such as hydrogen evolution. Once the pulse duration exceeds the transition time, mass transfer becomes the dominant factor of the metal deposition. If the current efficiency is of concern, the pulse duration should not exceed the transition time. Given the electrolyte composition, temperature, agitation condition, pulse on- and off-times, the value of the transition time relies on the applied pulse current density.

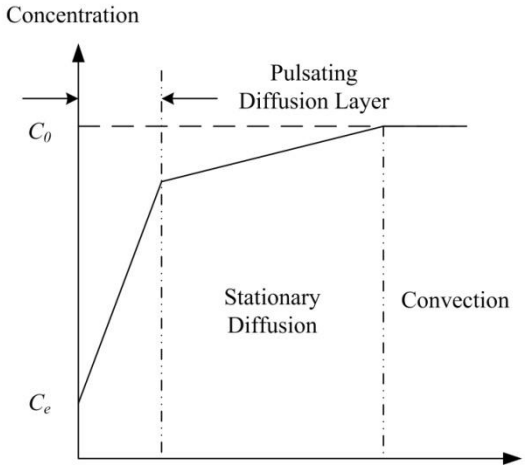


Figure 3-3 Concentration profiles in the diffusion layer near to the electrode surface during pulse electroplating [54].

The current distribution during pulse electroplating differs from the case of the DC condition. The current distribution in an electrochemical system can be

distinguished as primary, secondary and tertiary current distribution which depends on different factors. During pulse electroplating, the primary current distribution should not be affected by the pulsating current since it is only influenced by the geometry of the electrodeposition system rather than the variation of current density. The secondary current distribution is established when the activation overpotential is taken into account. A dimensionless index called the Wagner number is defined as:

$$W_a = \frac{k}{L}\left(\frac{d\eta}{di}\right) \tag{3-3}$$

where k is the conductivity of the electrolyte, η is the overpotential, i is the current density, and L is a characteristic length of the electrodeposition system. The larger the numerical value of the W_a, the more uniform is the current distribution. When the W_a becomes zero, only the primary current distribution is considered. In the absence of significant mass transport effects, the Wagner number, which governs the secondary current density distribution, depends on the pulse peak current density instead of the average current density. Since the peak current density is always higher than the average current density, the Wagner number will be smaller in pulse electroplating than in DC electrodeposition, thus the secondary current density distribution is less uniform for pulse electroplating. However, in the presence of significant mass transport, the current distribution may be more uniform than in DC electroplating. The pulse limiting current density i_{pL} is defined as the value of i_p for which the concentration of the reactants decreases to zero just at the end of the pulse duration [54]. When the pulse duration is of the order of, or exceeds, the transition time, or the pulse current density overcomes the limiting pulse current density, the deposition becomes partially controlled by the mass transport and the concentration overpotential needs to be taken into account. Due to the high instantaneous current densities applied in pulse electroplating, the reaction rate in the pulse-on duration may become limited by the non-steady state mass transport. Then a tertiary current distribution may therefore prevail in pulse electroplating under certain conditions, which will result in a more uniform current distribution.

As the pulse duration can be very short, *e.g.* in the order of milliseconds, it becomes possible to use very high pulse current density which is beyond the limiting current density in the DC condition and achieve a good quality of deposits in the same deposition time. Then, a relatively higher overpotential usually occurs near the

cathode surface resulting in an increased nucleation rate of the crystallisation, as such obtaining a finer grain size of deposit. Further, the pulse-off time provides the solution an interval to replenish the reactants consumed during the pulse-on time before the next iteration of the pulse. This unique feature of the unipolar current waveform offers many advantages compared with direct current.

With the additional anodic cycle, the bipolar pulse reverse electroplating has the potential to obtain a more uniform current distribution compared with DC electroplating with the same average current density. As shown in Figure 3-2*b*, in a typical pulse reverse current waveform, an anodic cycle is applied following the cathodic deposition cycle to dissolve part of the deposit. Because the deposit acts as the anode during the reverse cycle, it will be preferentially dissolved on the protruding sites resulting in a levelling effect. Also, the metal dissolved into the solution can be seen as an assistance to the diffusion and reduce the concentration gradient caused by the depletion during the cathodic deposition cycle. To ensure the deposition moves forward, the parameters of the pulse reverse current need to be so configured that the quantity of the electrical charge in the cathodic cycle should be considerably greater than the quantity in the anodic cycle. The relevant features discussed above, such as the transition time, are still applicable in pulse reverse electroplating.

3.1.2 Applications of Pulse Electroplating and Pulse Reverse Electroplating

By using pulse electroplating, small grained, even nanocrystalline structured deposits can be obtained under certain conditions which thereafter result in an improvement in mechanical properties of the coatings. Submicron sized or even nanoscale copper was achieved through various current waveforms and the microstructure, *e.g.* twinning, also relied on the pulse current parameters [56]. Similarly, nickel films having an average grain size of 25 *nm* were produced with a pulse current which could significantly improve wear resistance and micro-hardness of the deposits [57]. Another study conducted by Qu *et al* [58] also demonstrated that it was possible to obtain a microstructure with ultrafine grains ranging from 50 *nm* to 200 *nm*, depending on the pulse current densities, when the pulse duration was 10 μs, using a nickel sulphamate bath without any additives. The grain refinement effect through pulse electroplating was also observed in alloy deposition. Nakanishi *et al* [59]

obtained less than 10 *nm* sized CoNiFe alloy crystals by adjusting the duty cycle to 50% while the pulse peak current density was kept at 10 mA/cm^2. It was reported that nanocrystalline Cu-Co heterogeneous alloys were obtained through pulse electroplating and the surface was smoother than that under the DC condition [60]. Moreover, pulse reverse electroplating was treated as an alternative to using complex additives in the electrodeposition of pure nickel and nickel alloy thin films used in MEMS devices. By pulse reverse electroplating, smoother deposits with low residual internal stress have been obtained through various bath compositions without complex additives [61].

With the advantages illustrated above, pulse current and periodic pulse reverse current were employed as efficient tools for electrodeposition through lithographic photoresist masks [25, 32, 62-64]. Pulse electroplating and pulse reverse electroplating showed an improvement in surface finish, uniformity, elimination of defects during the deposition of solder bumps, filling of trenches and MEMS fabrication [65-68]. Another important application is through-hole or via electroplating which is crucial for next generation high density electronic packaging technologies. Pulse reverse electroplating is considered as a promising method to get more uniform deposits as it frequently provides greater improvements in throwing power than simple pulse electroplating [69, 70]. Uniform, defect-free deposits in high aspect ratio through-holes formed by a so-called bottom-up filling process can be obtained by adjusted pulse reverse electroplating, even without any additives [29, 71-74].

3.1.3 Aim of This Chapter

The aim of utilising pulsating current waveforms over DC electroplating for indium deposition was to exploit the potential advantages of pulsating current on the refinement of grain size, microstructure, current distribution and surface morphology. However, a very limited number of papers about indium electrodeposition using pulsating current can be found in the literature. Most of the applications of indium electrodeposition fall into areas with security sensitivity or with core commercial interests, for example, the defence department and crucial components manufactured in the automotive industry [46-48, 51]. For the indium sulphamate solution employed in this research, there is also limited information regarding its performance during

pulse electroplating, even from the supplier. This chapter reports an investigation of the indium deposition process through pulse electroplating and pulse reverse electroplating on non-patterned substrates prior to the indium bumping studies. Various pulsating current waveforms are employed and the results are compared with the DC electroplating.

3.2 Experimental Details

Indium electroplating was conducted using the same indium sulphamate solution supplied by Indium Corporation of America, which has been described in Chapter 2. Pure copper sheet with 4 cm^2 area was utilised as the cathode substrate. After alkaline degreasing using the solution described before, the sample was acid activated by immersion into 10% sulphuric acid (volume percent, specific gravity of 1.83, supplied by Fisher Scientific) at room temperature for 5 minutes followed by a rinse with deionised water. Then, the copper substrate was immersed into 5 *wt%* sulphamic acid solution for 1-3 minutes activation. The same configured electroplating bath described in Chapter 2 was employed for the pulse electroplating trials. All the electroplating trials were conducted at room temperature for 30 minutes, as the average current densities were kept at 10 mA/cm^2. No additional agitation was applied for all the experiments. The pulsating current was generated by the Potentiostat (PARSTAT 2273, Ametek) to carry out unipolar pulse electroplating and pulse reverse electroplating. In this chapter and thereafter, for the sake of convenience, the term 'pulse electroplating' is used to present the electrodeposition through 'unipolar pulse current'.

3.2.1 Pulse Electroplating

In pulse electroplating trials, the average current density was chosen and remained constant at 10 mA/cm^2 while the cycle duration and peak current density was varied to form different waveforms. Thus, the results were comparable with the DC electroplating which had the same current density value. In order to take the advantages of pulse electroplating, the desired pulse current density should exceed the highest current density value in the DC condition, as indicated by the cathodic polarisation curve (Figure 2-6, page 31). Therefore, the parameters were selected in such a way that the minimum pulse current density was 30 mA/cm^2.

To investigate the effect of pulsed peak current density, the pulse duration time was set as 1 *ms* but the pulse off-time increased from 2 *ms* up to 99 *ms* while the average current density was kept at 10 mA/cm^2. Thus, the peak current density increased from 30 mA/cm^2 to 1000 mA/cm^2. Figure 3-4 demonstrates the representative current waveform with 1 *ms* pulse-on time and 4 *ms* pulse-off time. Table 3-1 lists the parameters of pulsating current waveforms used for the indium electroplating. To determine the cathodic current efficiency, the samples were weighed before and after electroplating by using a Mettler Toledo XS205 Dual Range analytical balance with accuracy up to 0.01 *mg*, and the current efficiencies corresponding to various parameters calculated using Equation 2-11 (page 32). All of the current efficiency data corresponding to certain electroplating parameters was averaged from two electroplating trials.

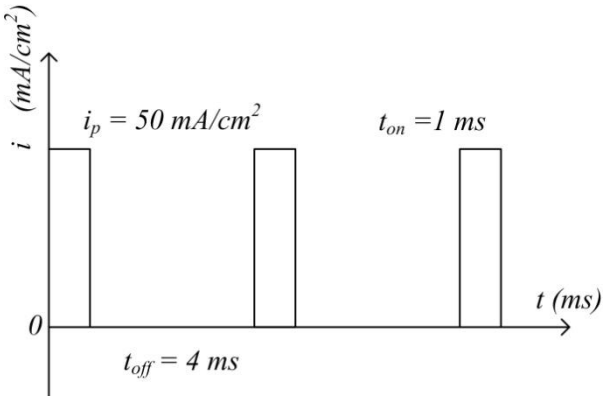


Figure 3-4 The representative pulse current waveform with 1 *ms* : 4 *ms* cycle ratio.

Table 3-1 Parameters of unipolar pulse current waveforms for indium electrodeposition in sulphamate solution.

No.	t_{on} *(ms)*	i_p *(mA/cm^2)*	t_{off} *(ms)*	*Frequency (Hz)*	*Duty cycle (%)*	i_{avg} *(mA/cm^2)*
1	1	30	2	333	33.3	10
2	1	40	3	250	25	10
3	1	50	4	200	20	10
4	1	60	5	166	16.7	10
5	1	80	7	125	12.5	10
6	1	100	9	100	10	10
7	1	120	11	83	8.3	10
8	1	160	15	62.5	6.25	10
9	1	200	19	50	5	10
10	1	300	29	33	3.3	10
11	1	500	49	20	2	10
12	1	1000	99	10	1	10

3.2.2 Pulse Reverse Electroplating

Similar to pulse electroplating through the parameters explained above, the pulse reverse current waveforms were formed by adding anodic cycles to the 200 *Hz* and 100 *Hz* frequency waveforms shown in Table 3-1. To investigate the effects of anodic cycles on the indium electroplating, the average current density of pulse reverse electroplating was also kept at 10 *mA/cm^2*. Table 3-2 shows the parameters for pulse reverse electroplating, according to the features of the waveform in Figure 3-2*b*. Because the indium sulphamate solution is sensitive to copper ion contamination, the sample was pre-electroplated with indium for 2 minutes at 10 *mA/cm^2* DC, which was to prevent the copper substrate from being dissolved into the solution during the anodic cycles. The current efficiencies were also derived as described above.

Table 3-2 Parameters of bipolar pulse reverse current waveforms for indium electrodeposition in sulphamate solution.

No.	$i_{p(c)}$ *(mA/cm²)*	$t_{on(c)}$ *(ms)*	$i_{p(a)}$ *(mA/cm²)*	$t_{on(a)}$ *(ms)*	t_{off} *(ms)*	**Frequency** *(Hz)*	i_{avg} *(mA/cm²)*
13	50	1.5	50	0.5	3	200	10
14	100	1.5	100	0.5	8	100	10
15	100	1.5	50	1	7.5	100	10

3.2.3 Characterisation

Electrodeposition through the pulsating current waveform was expected to give grain refinement and therefore surface smoothing, which has been observed in several practical applications. Accordingly, the influences of pulse electroplating and pulse reverse electroplating on the uniformity of indium deposition should be reflected through the surface profile of the electroplated indium. The surface profile of the deposited indium was measured by using the Talysurf CLI 2000 surface profiler following the route demonstrated in Figure 2-4 (page 29). Moreover, the surface morphology and microstructure were also characterized by Scanning Electron Microscopy (SEM) and Focused Ion Beam assisted SEM (FIBSEM).

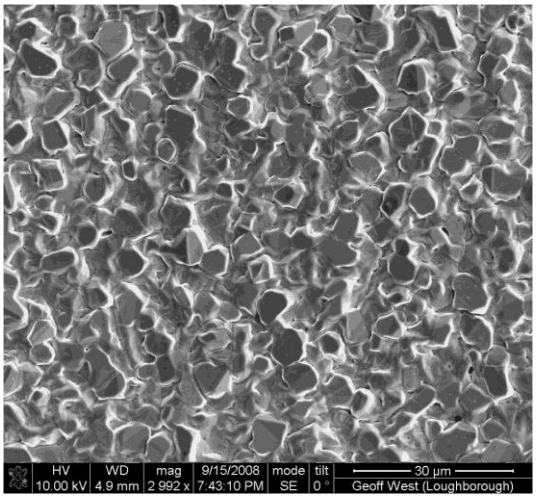
3.3 Results of Indium Deposited Through Pulsating Current

3.3.1 Pulse Electroplating

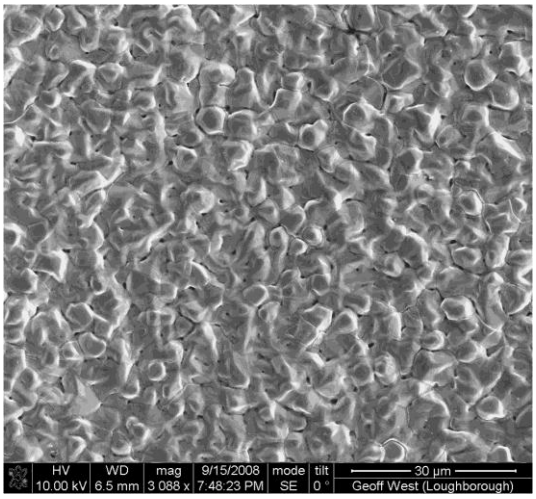
The surface morphologies of indium electroplated using pulse current waveforms are shown in Figure 3-5. With the decrease of duty cycle ratio, the peak current density increased as the average current density remained constant. It can be clearly seen that the morphologies of deposits were significantly changed by utilising pulse current compared to DC. Generally speaking, surface feature refinement can be observed in all of the pulse electroplating conditions. In the case of waveform *No. 1* shown in Table 3-1, the pulse peak current density was 30 *mA/cm²*, and relatively large features and the crystal growth facet can still be observed. However, once the pulse peak current density overcame 30 *mA/cm²*, the typical large sized surface features were no longer present. Instead of the granular morphology seen in DC electroplating, the

indium grains preferentially grew as cones in pulse electroplating when the pulse current density was between 40 and 300 mA/cm^2.

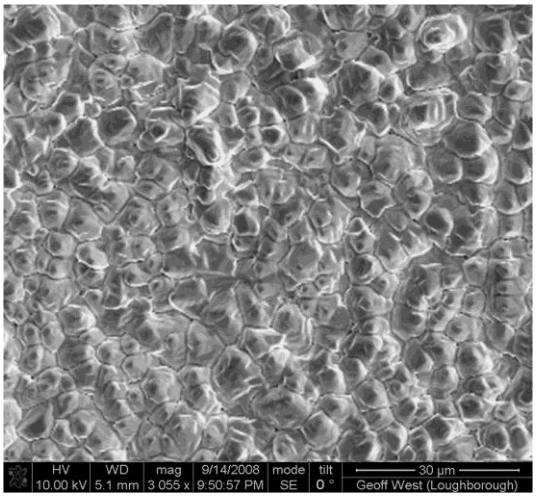
Moreover, it was found that no hydrogen bubbles were visible during the electroplating process when the peak current density was below 160 mA/cm^2. In the case of waveform *No. 8, i.e.* a peak current density of 160 mA/cm^2, hydrogen bubbles were observed all through the pulse electroplating process covering the whole surface, but the hydrogen evolution did not affect the surface morphology. When the peak current density reached 300 mA/cm^2, massive hydrogen bubbles were observed throughout the electroplating process and indium was deposited accompanied with hydrogen evolution. When the peak current density was 300 mA/cm^2 or above, the so called 'pitting' effect could be observed causing significant non-uniformity on the surface. Figure 3-6 shows the 'pitting' effect caused by the hydrogen bubble evolution when the peak current density was 300 mA/cm^2.

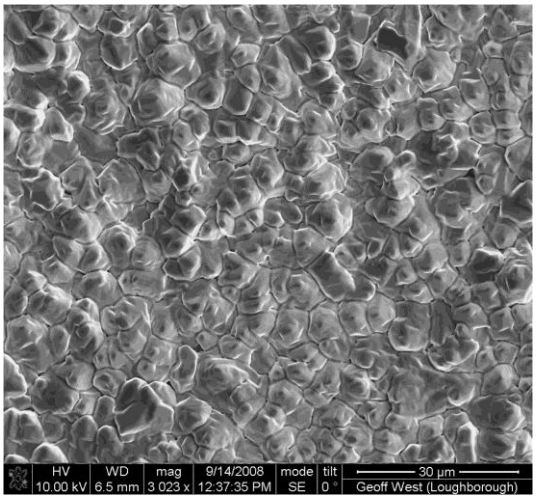


(a) 1 *ms* : 2 *ms*, 333 *Hz*

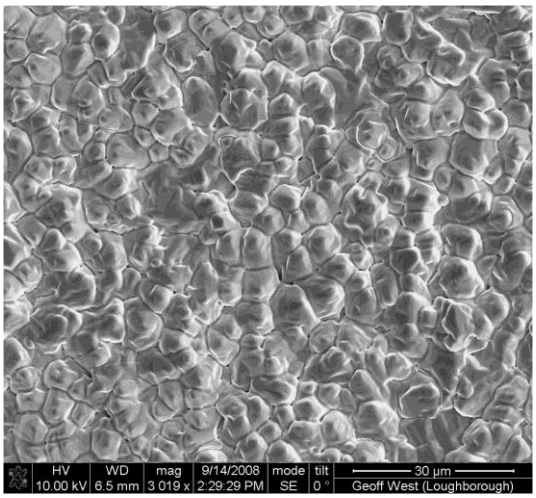


(b) 1 *ms* : 3 *ms*, 250 *Hz*

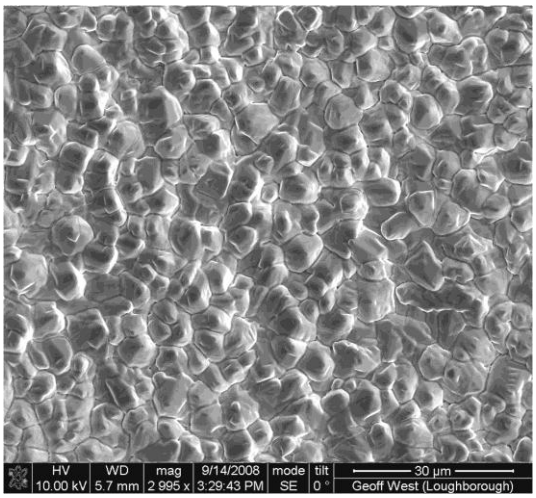




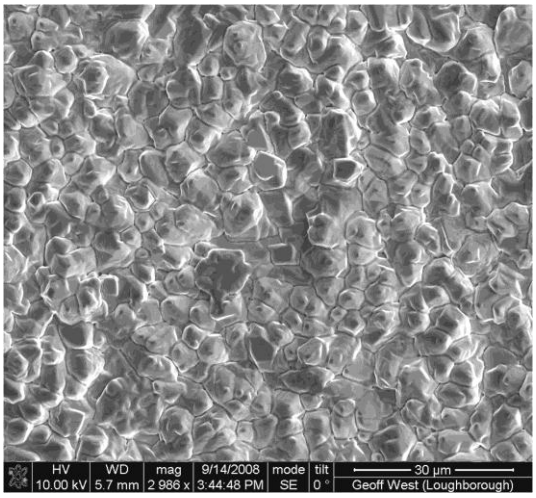
(c) 1 *ms* : 4 *ms*, 200 *Hz*



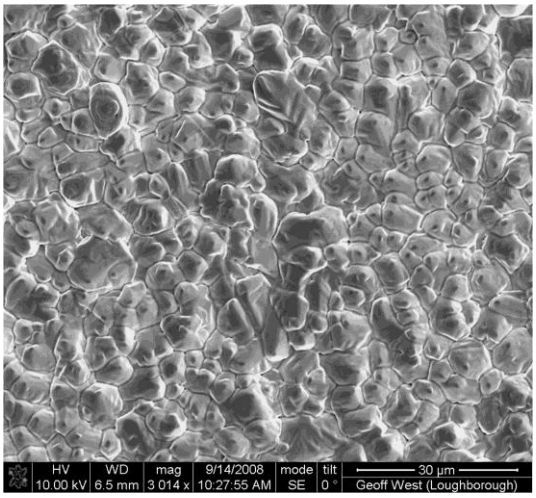
(d) 1 *ms* : 5 *ms*, 166 *Hz*



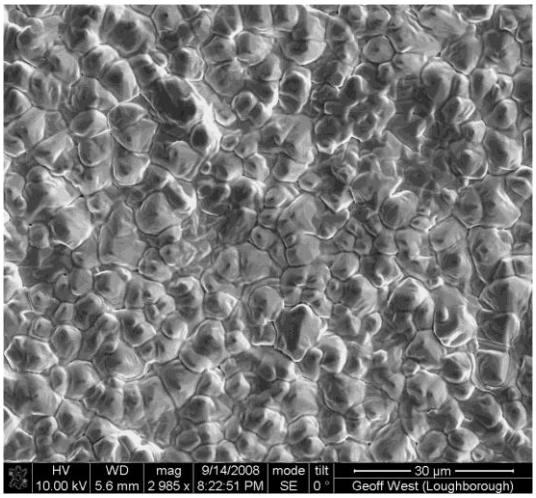
(e) 1 *ms* : 7 *ms*, 125 *Hz*



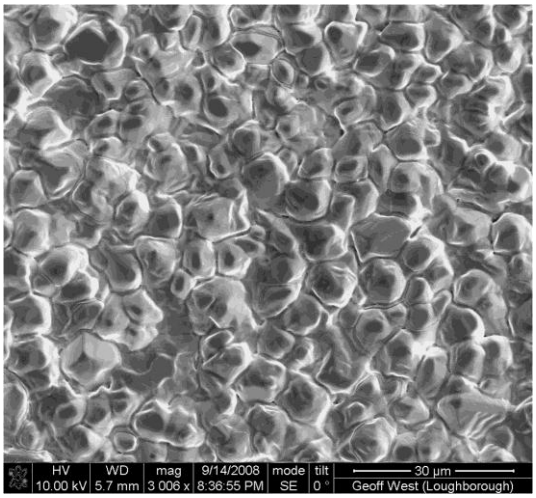
(f) 1 *ms* : 9 *ms*, 100 *Hz*



(g) 1 *ms* : 11 *ms*, 83 *Hz*

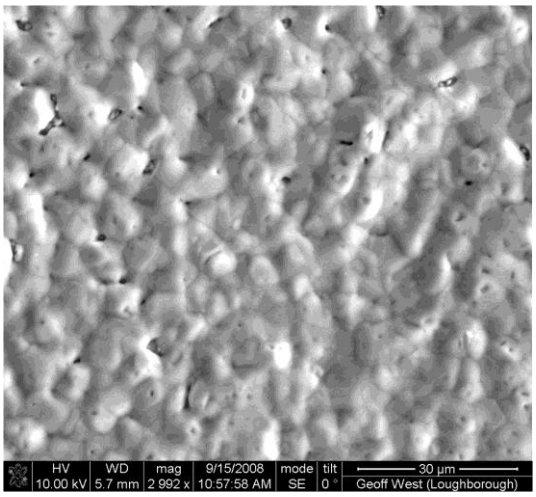


(h) 1 *ms* : 15 *ms*, 62.5 *Hz*

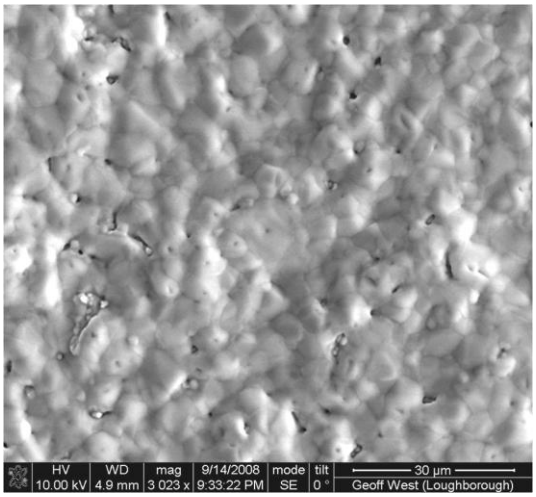


(i) 1 *ms* : 19 *ms*, 50 *Hz*

(j) 1 *ms* : 29 *ms*, 33 *Hz*



(k) 1 *ms* : 49 *ms*, 20 *Hz*



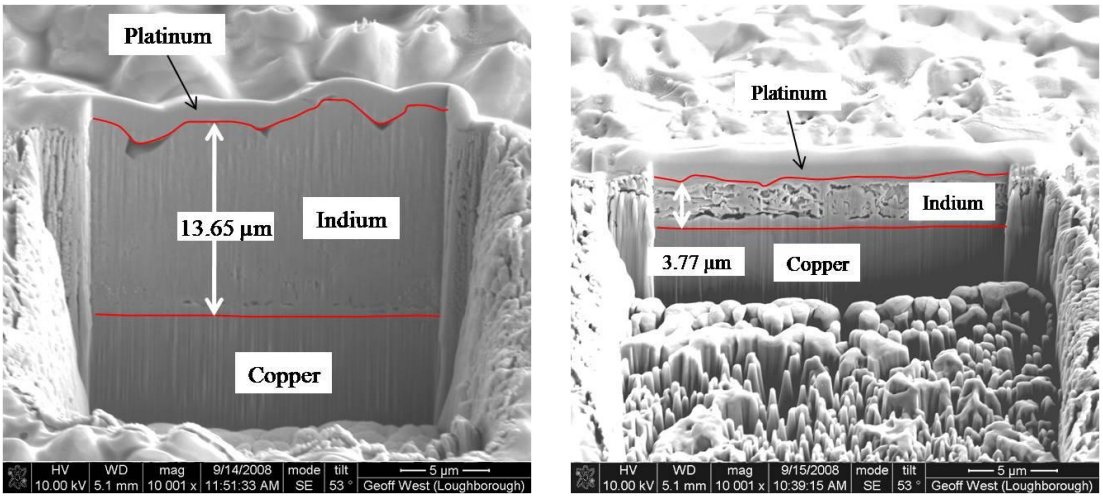
(l) 1 *ms* : 99 *ms*, 10 *Hz*

Figure 3-5 Surface morphologies of electroplated indium using various unipolar pulse current waveforms with constant pulse duration (1 *ms*) and average current density (10 *mA/cm*^{2}).

Figure 3-6 'Pitting' effect observed on the surface of electroplated indium caused by the hydrogen bubble evolution when the peak current density i_p = 300 *mA/cm*^{2}.

The hydrogen evolution was reflected in the loss of the cathodic current efficiency. By measuring the weight change after electroplating, the current efficiencies corresponding to various current waveforms were calculated according to Equation 2-11 and the results are given in Table 3-3. It can be seen that more than 90% current efficiency can still be achieved when the peak current density was below or

equal to 100 mA/cm^2. When the pulse current density was greater than 100 mA/cm^2 but smaller than 160 mA/cm^2, although no visible hydrogen bubbles were observed on the surface, the decrease of the current efficiency indicated the existence of the side reaction. The side reaction could be decomposition of water that might not be able to form visible gas bubbles in the solution, or decomposition of other components in the solution such as organic additives. Therefore, when the pulse current density was greater than 100 mA/cm^2, the cathodic current efficiencies were decreased with the peak current densities.



(a) i_p = 50 mA/cm^2 *(b)* i_p = 500 mA/cm^2

Figure 3-7 Cross section analysis of pulse electroplated indium with various peak current densities produced using FIBSEM.

The decrease of current efficiency can also be demonstrated through the change of thickness of indium. Figure 3-7 compares the cross sectional views (prepared by FIB) of pulse electroplated indium with 50 and 500 mA/cm^2 peak current densities. A layer of platinum was deposited on the top of the area of interest to prevent any damage to the surface caused by the ion beam during the preparation process. The boundary lines between In/Pt and In/Cu were added manually. For both of the cases, the electroplating trials were conducted for 45 minutes. It was measured that when the peak current density was 50 mA/cm^2, the thickness of deposit was about 13.65 μm, while it was only about 3.77 μm in the case of i_p = 500 mA/cm^2. Also, the deposit appeared highly porous in the latter case.

Figure 3-8 shows the surface roughness measurement of the electroplated indium for the peak current density of 50 mA/cm^2. The upper contour map illustrates the distribution of data collected from the surface, and the lower chart shows the total 11 line profiles. From this, the maximum Total Height of Profile (P_t) 6.05 μm from the averaged base line, and the Average Roughness (R_a) 0.58 μm were obtained. Table 3-3 also shows the values of P_t and R_a of pulse electroplated indium for other pulse electroplating conditions. It should be noted that, because of the 'pitting' effect caused by the hydrogen bubble evolution when the peak current density exceeded 300 mA/cm^2, the surface profile measurement was not applicable for waveforms *Nos. 10, 11* and *12*.

Table 3-3 Cathodic current efficiencies (CCE), maximum Total Height of Profile *(P_t)* and Average Roughness *(R_a)* for indium electrodeposits produced using various pulse electroplating parameters.

No.	t_{on} *(ms)*	i_p *(mA/cm^2)*	t_{off} *(ms)*	i_{avg} *(mA/cm^2)*	CCE *(%)*	*Max.* P_t *(μm)*	R_a *(μm)*
1	1	30	2	10	91.63	7.36	0.66
2	1	40	3	10	91.42	5.26	0.7
3	1	50	4	10	92.08	6.05	0.59
4	1	60	5	10	91.84	6.27	0.67
5	1	80	7	10	90.90	6.08	0.64
6	1	100	9	10	90.57	8.36	0.73
7	1	120	11	10	81.57	7.98	0.76
8	1	160	15	10	65.70	8.76	0.91
9	1	200	19	10	48.40	7.31	0.86
10	1	300	29	10	37.16	n/a	n/a
11	1	500	49	10	25.59	n/a	n/a
12	1	1000	99	10	22.36	n/a	n/a

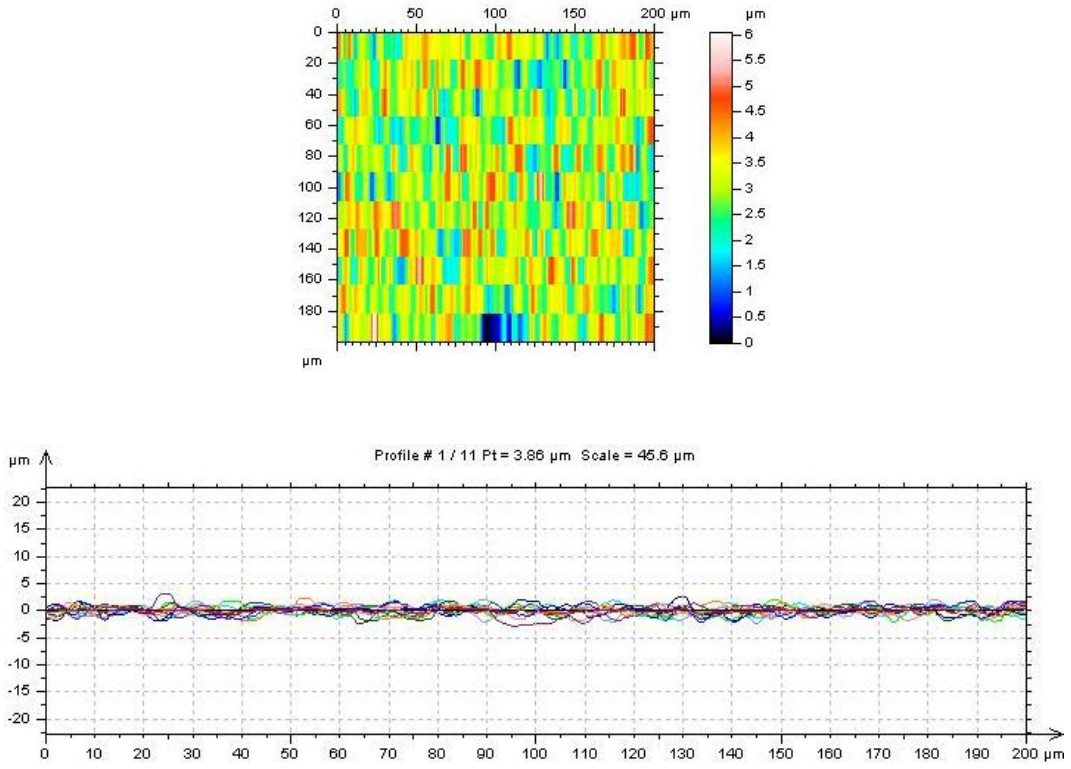


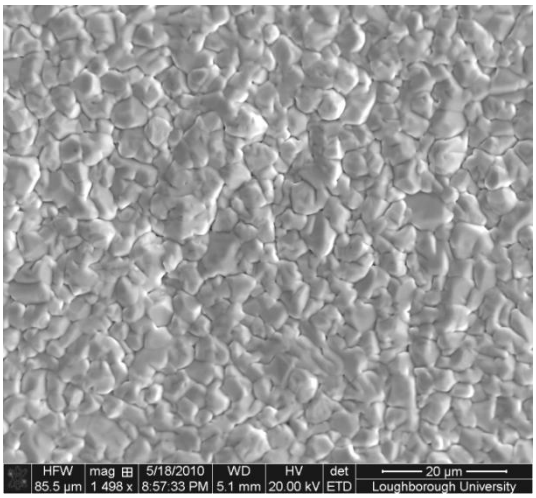
Figure 3-8 Surface roughness measurement of pulse electroplated indium (i_p = 50 *mA/cm*^{2}).

3.3.2 Pulse Reverse Electroplating

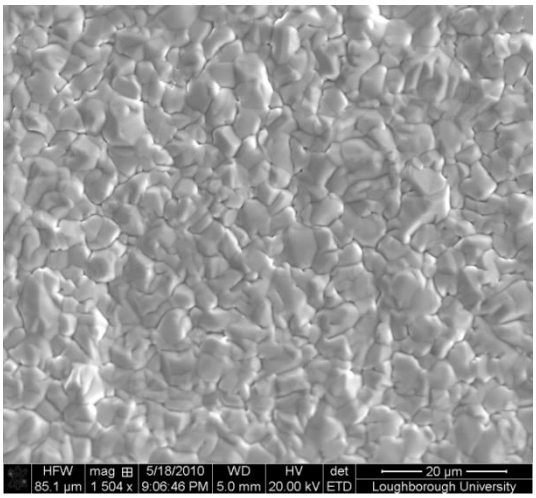
The surface morphologies of electroplated indium produced using the three types of pulse reverse current waveforms are shown in Figure 3-9. In all of the three pulse reverse electroplating conditions, surface feature refinement can be observed in comparison to DC electroplating. Interestingly, the surface morphology obtained from the three pulse reverse electroplating waveforms is significantly different compared to conventional pulse electroplating. The conical growth preference observed in pulse electroplating is not found in pulse reverse electrodeposition, instead, the electrodeposited indium presents a refined surface feature.

Because both of the cathodic and anodic pulse current densities were set lower than or equal to 100 *mA/cm*^{2}, there were no visible hydrogen bubbles during the electrodeposition processes. The overall cathodic current efficiencies are shown in Table 3-4. It can be seen that the overall cathodic current efficiencies were as high as 90% in all of the three pulse electroplating conditions. Figure 3-10 shows the surface roughness measurement results of the electroplated indium through the waveform *No.*

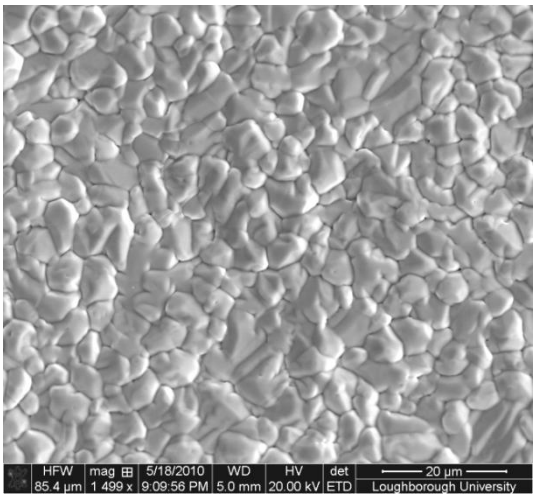
13 giving an average roughness (R_a) of 0.6 μm. The measurement results for waveforms *Nos. 14* and *15* are also included in Table 3-4.



(a) $i_{p(c)}$ = 50 mA/cm^2, $t_{on(c)}$ = 1.5 ms; $i_{p(a)}$ = 50 mA/cm^2, $t_{on(a)}$ = 0.5 ms; t_{off} = 3 ms.



(b) $i_{p(c)}$ = 100 mA/cm^2, $t_{on(c)}$ = 1.5 ms; $i_{p(a)}$ = 100 mA/cm^2, $t_{on(a)}$ = 0.5 ms; t_{off} = 8 ms.



(c) $i_{p(c)}$ = 100 mA/cm^2, $t_{on(c)}$ = 1.5 ms; $i_{p(a)}$ = 50 mA/cm^2, $t_{on(a)}$ = 1 ms; t_{off} = 7.5 ms.

Figure 3-9 Surface morphology of electrodeposited indium through various pulse reverse current waveforms with a constant average current density of 10 mA/cm^2.

Table 3-4 Cathodic current efficiencies (CCE), maximum Total Height of Profile (P_t) and Average Roughness (R_a) of electrodeposited indium through various pulse reverse current waveforms.

No.	$i_{p(c)}$ *(mA/cm²)*	$t_{on(c)}$ *(ms)*	$i_{p(a)}$ *(mA/cm²)*	$t_{on(a)}$ *(ms)*	t_{off} *(ms)*	CCE *(%)*	*Max.* P_t *(μm)*	R_a *(μm)*
13	50	1.5	50	0.5	3	90.4	6.24	0.6
14	100	1.5	100	0.5	8	89.83	6.19	0.71
15	100	1.5	50	1	7.5	91.05	7.56	0.83

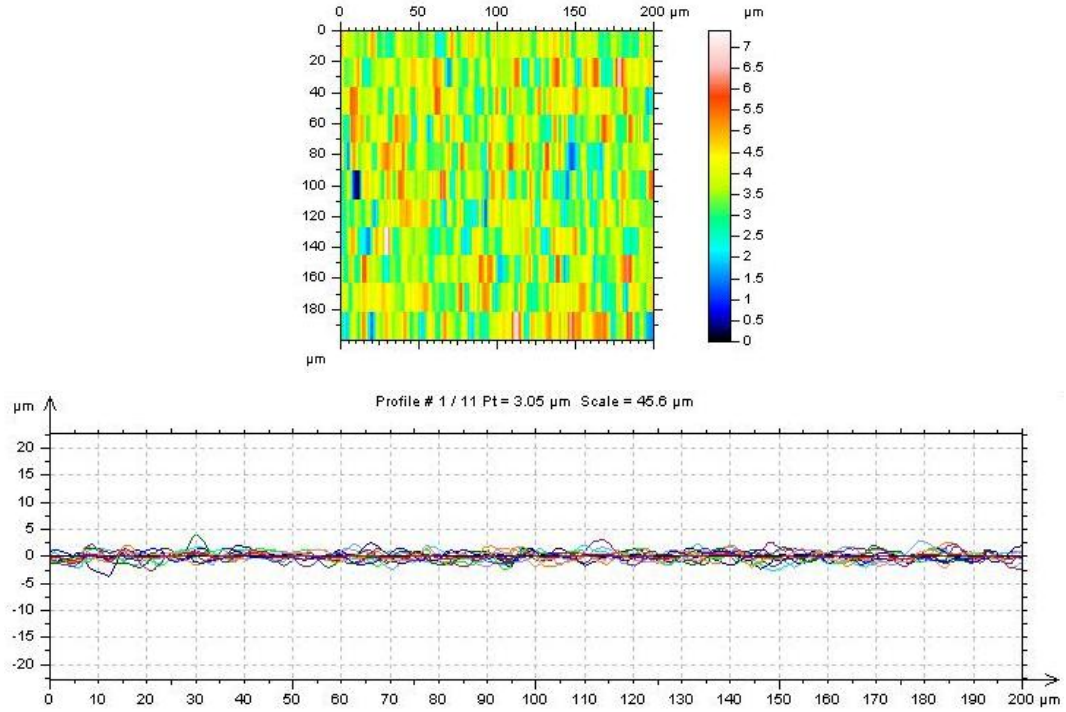


Figure 3-10 Surface roughness measurement of indium obtained using pulse reverse electroplating (waveform *No. 13*, $i_{p(c)}$ = 50 *mA/cm²*, $t_{on(c)}$ = 1.5 *ms*; $i_{p(a)}$ = 50 *mA/cm²*, $t_{on(a)}$ = 0.5 *ms*; t_{off} = 3 *ms*).

3.4 Summary

In this chapter, experiments utilising unipolar pulse electroplating and bipolar pulse reverse electroplating of indium were conducted using the same indium sulphamate solution at room temperature without any additional agitation. The surface morphology, surface uniformity and electroplating efficiency were analysed using

SEM, FIBSEM, surface profilometry and high accuracy analytical balance. The following conclusions can be drawn on the basis of the data demonstrated above.

- The surface feature size of electrodeposited indium was significantly reduced compared to DC electroplating by using both unipolar and bipolar pulsating current waveforms;
- The surface morphology of electroplated indium through pulse electroplating was dominated by conical structures while a refined microstructure prevailed in the pulse reverse electroplating situation;
- The surface roughness of electrodeposited indium was significantly improved through pulse electroplating and pulse reverse electroplating compared to DC electroplating, while little difference was found between using the unipolar and bipolar pulsating current waveforms;
- In order to take the advantage of pulse electroplating and ensure a high electroplating efficiency, it is recommended that, for the 1 *ms* pulse duration, the pulse current density should be in a range between 40 and 100 mA/cm^2.

Chapter 4 Wafer Level Indium Bumping by Electrodeposition

4.1 Introduction

This chapter presents the results of indium bump deposition through DC, unipolar pulse and bipolar pulse reverse electroplating. The background of the electroplating bumping method is introduced, and a literature review of the uniformity issue is discussed afterwards. The experiments mainly focus on the influences of various current waveforms on the indium bumping process regarding the bump morphology, microstructure and uniformity.

4.1.1 Development of the Electroplating Bumping Method

Electroplating as a method for bumping was introduced in the early 1970s in the applications of die packaging through Tape Automated Bonding (TAB) [75]. Then, with the evolutionary development of electrochemical fabrication techniques, electrodeposition of solder bumps for flip chip interconnection was developed as an alternative to the vacuum evaporation method and has been widely adopted [27, 30]. The larger sized wafer processing introduced in recent years imposed extreme challenges for the evaporation method to overcome the thermal mismatch between metal mask and wafers [76, 77]. In addition, the evaporation process is not suitable to deposit tin-rich alloys because the relatively low vapour pressure of tin restrains its evaporation rate and the evaporation process may need an unrealistic long time which is unacceptable for industrial production [2]. A successful example of electroplated solder bumping was the eutectic tin-lead alloy solder bump fabricated through

electrodeposition which has been commonly applied for microelectronic packaging interconnections. However, due to the health and environment concerns and RoHS legislative requirements, the most commonly electroplated Pb-containing solder materials have been banned in most microelectronic products [3]. Tremendous efforts have been made in the development of lead-free solder materials. Various solder materials have been investigated for flip chip bumping such as copper, tin-silver, tin-copper, tin-indium, tin-bismuth and tin-silver-copper alloys [32, 78-84].

Unlike the traditional electroplating system, which usually consists of several tanks containing electroplating electrolytes and pre-/post-treatment chemicals, the electroplating systems employed in microelectronic packaging for solder bumping require different types of electroplating chamber sequenced in a highly automated processing system. Considering the tiny dimension of solder bumps (~100 μm or less) and enormous quantity of production, yield and uniformity are of special importance for manufacturing. Thus, the electroplating system is required to be designed with consideration of every detail and the electroplating process should be repeatable with reasonable tolerance. Moreover, comprehensive understanding of the yield and uniformity issues is essential for the electroplating bumping process to succeed.

4.1.2 Bumping Yield and Uniformity

In this research, the bumping yield concerns the number of bumps that are missed after electroplating. In other words, the bumping yield is defined as that whether the bump is present or not, and such definition also has been widely adopted by other investigators [1, 39, 76]. To ensure a high yield, the electroplating process must be carefully controlled with attention to every detail. For example, in the industrial mass production, plasma descum process is usually applied prior to electrodeposition to ensure that no residual photoresist is left in the bottom of the bumping pattern openings. Very often, more than one metal needs to be deposited sequentially within an electroplating unit, such as multilayered tin-based binary or tertiary alloys. So, sufficient cleaning of the wafer between the two steps is necessary to achieve a high yield. Also, in the case of fine pitch bumping, an additional wetting step is needed to ensure the substrate has good contact with the electrolyte.

The uniformity of the deposited bumps is one of the problems which the electroplating bumping approach suffers from and it deteriorates when ultrafine pitch

patterns and large diameter wafer are employed. The uniformity defines variations of height, shape, volume and composition of deposited bumps, which can be categorised into within wafer uniformity and wafer-to-wafer uniformity. Within a wafer, the uniformity mainly depends on the current density distribution and diffusion boundary layer distribution across the entire wafer. As to wafer-to-wafer uniformity within a single production batch or multiple batches, it is mainly affected by the reliable control of the electroplating parameters, such as temperature and composition of the electrolyte and the method utilised to define the accurate ending point of the process [2]. It is also very important to ensure the same specifications of the wafers to be processed prior to bumping, for instance, the thickness of seed layers between wafers. However, most packaging applications request good bump uniformity within an individual die, which is likely to affect the functions and reliability of electronic packages. Therefore, this research concentrates on the bump uniformity within a wafer by electroplating.

4.1.3 Current Density Distribution

The miniaturisation of microelectronics systems requires higher density interconnections at ever smaller pitch size and has led to electrodeposition to produce solder bumps of some tens of microns in diameter becoming a crucial enabling technique. In many applications, the thickness of the substrate for electroplating is continuously reduced, thus the resistance of the substrate can no longer be neglected and can substantially affect the electroplating process during wafer bumping. As the resistance of substrate can result in a noticeable potential drop at the electroplating interface between electrolyte and substrate, the location of the electrical contact with the electrode, *e.g.* through the periphery of the substrate (*e.g.* wafer), is important and can lead to a phenomenon known as the ‘terminal effect’ [85]. Figure 4-1 illustrates schematically the two-dimensional current flow in the electrolyte above a cathodic resistive substrate during electrodeposition which is a qualitative model obtained by using COMSOL. It clearly shows that the current densities (the radiant lines in the figure) are distorted along the cathode surface leading to uneven current distribution.

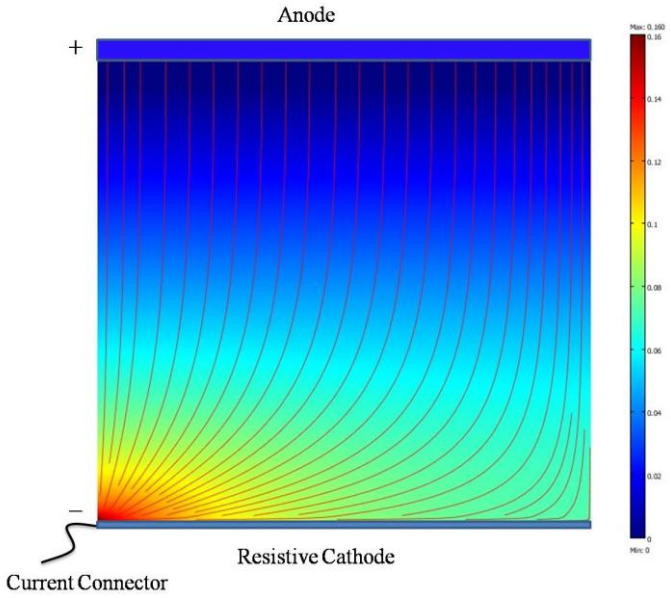


Figure 4-1 Schematic of 2-D distribution of current flow in an electrolyte during electroplating onto a resistive substrate.

For the electroplating bumping process, a very thin layer of metal acting as the cathode is needed and its resistance is not negligible. This thin metal film is normally deposited prior to bumping and known as the seed layer. In electroplating, the wafer is peripherally contacted to provide the current flow and enable high productivity. Thus, due to the terminal effect, the varied potentials induce different current densities across the wafer leading to a different electroplating rate at different locations across the wafer. The bumps near the edge of wafer normally grow faster, hence taller than those at the centre of the wafer due to the existence of a potential gradient. The variation of bump height imposes a non-uniformity issue to the electroplating bumping process.

The terminal effect of electroplating for a blanket (un-patterned) resistive substrate has been extensively studied through theoretical calculation and experimental validation. Tobias and Wijsman [85] as the pioneers of electroplating onto resistive substrates have, based on a plane parallel electrode system, concluded that the current density distribution along resistive electrodes is dependent on the magnitudes of certain dimensionless parameters which are determined by the geometrical features of the electroplating system, the resistance of the electrodes and the conductivity of the electrolyte. This model uses the potential theory such that the

current density can be determined by the local gradient of the electric potential which obeys a Laplace relation in the electrolyte and the potential in the resistive substrate can be calculated from Ohm's law. The potential distribution in the electrolyte and metal substrate are then connected at the electrode-electrolyte interface through an electrochemical kinetic relation, *i.e.* the Butler-Volmer equation. Tobias' model is described as a 'steady-state' process so that the thickness of the substrate may be ignored and the resistance of the substrate remains constant during the deposition process. This steady-state model found limited use in the prediction of deposit thickness distribution on a printed circuit board [86-88]. Matlosz *et al* [89, 90] extended Tobias' model to simulate electrodeposition of thin films on printed circuit boards, which also considered the phenomena that the resistance of the electrical path through the substrate would be reduced by the additional conductance contributed by the metal that has been deposited. The terminal effect is most profound at the beginning of electrodeposition, thereafter the electrodeposits can become conductive enough to provide uniform current density distribution as the deposition progresses.

In the case of electroplating using a photoresist mask or pattern, which is commonly applied in wafer bumping, the influences of pattern or mask need also to be taken into account. Dukovic [91] suggested the current density distribution through the mask during electrodeposition should be investigated by considering a hierarchy of size scales:

1. Workpiece scale — characteristic of the whole object to be electrodeposited, for example, an entire wafer.
2. Pattern scale — characteristic of patterns or regions on the workpiece.
3. Feature scale — characteristic of individual features such as bonding pads or through holes and their size and geometry.
4. Roughness scale — characteristic of microscopic roughness of surfaces.

Usually, the workpiece, *e.g.* a wafer, contains many different patterns, each are composed of many small features and, each small feature acts as the part of a separated electrode. Figure 4-2 illustrates a wafer with certain patterns (*i.e.* chips) and feature scales. From the point of view of the workpiece scale, the current density distribution at each square pattern is of great interest; thus an individual region may correspond, for instance, to an ASIC chip for pixel detectors. From the view of the pattern scale, it is important how the current within each square is distributed compared to the separated circular features. At the feature scale, the current density

distribution refers to the electrodeposition rate at each individual aperture. These three length scales for determining the current distributions could be simultaneously solved on the basis of the potential theory model proposed above, while the effect at the roughness scale is under the control of bath chemistry and additives in the solution [92]. Therefore, the geometric complexity of electroplating via a mask can be reduced by using the hierarchical length scales model [93, 94].

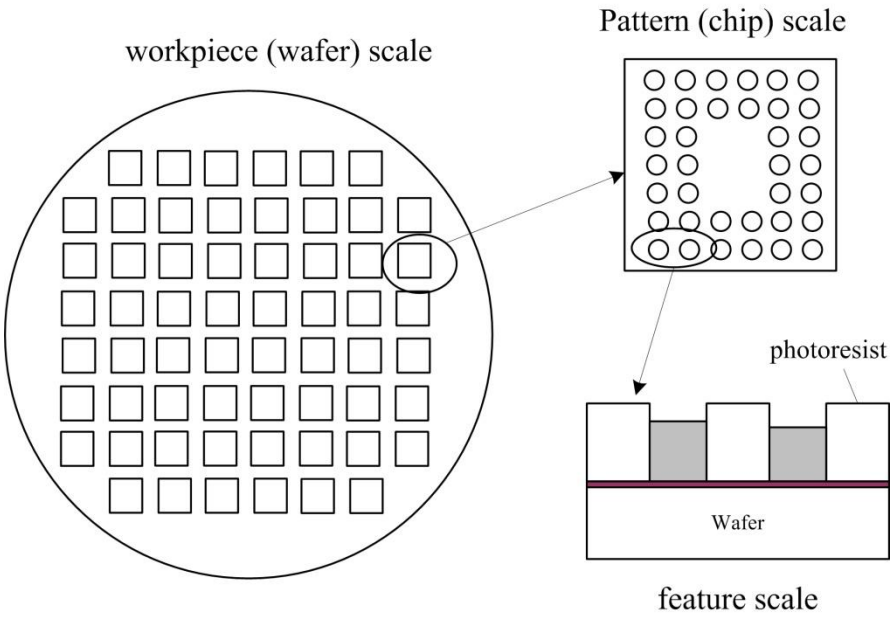
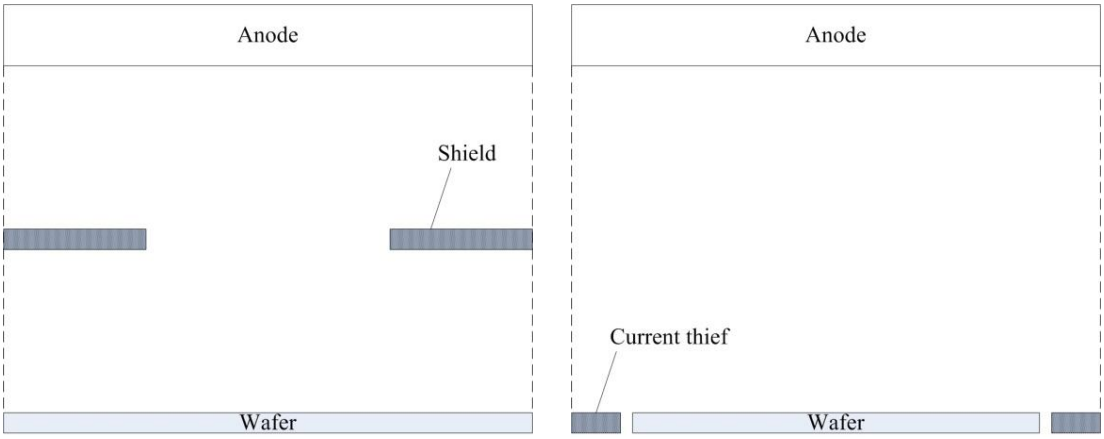


Figure 4-2 Schematic diagram of multiple length scales regarding current distribution for wafer bumping using a photoresist mask.

The current density distribution at the workpiece scale mainly depends on the geometrical configuration of the electroplating system. Because of the terminal effect, electrical connections and contact with the cathode (*i.e.* wafer) can physically govern the potential field and distribution on the wafer scale. Normally, symmetrical connection to the cathode is preferred to form an evenly distributed potential field, therefore resulting in a more even current density distribution. Electric shielding was also investigated as a useful approach to modify the primary current distribution at the workpiece scale within an electroplating bath by inserting a non-conductive shield between anode and cathode. This non-conductive shield is usually made with certain geometries corresponding to the shape of a cathode. Figure 4-3*a* shows the schematic

configuration of a typical wafer electroplating system with an electric shield having a circular hole in the middle. Non-conducting elements can be either positioned close to the cathode or the anode surface to shape the potential field distribution within the electrolyte. Both of the theoretical and experimental studies illustrated that the uniformity at the workpiece scale of current density distribution can be effectively improved by using the electric shielding as per the specific application [95-98].



(a) electric shield *(b)* current thief

Figure 4-3 Schematic configuration of electroplating system with: (a) electric shield, and (b) current thief.

Another method for adjusting the current distribution at the workpiece scale can be achieved by using auxiliary electrodes. As mentioned above, the edge of the cathode normally draws a higher current density due to the terminal effect. Therefore, an additional conductor can be connected from the edge, *e.g.* along the periphery of wafer so that undesirable high current crowding can be redirected to this additional conductor, to leverage the current flow across the wafer area [99-105]. This method is therefore called current thieving based on the fact that high current is stolen by the additional conductor introduced. In the case of wafer electroplating, a metal ring acting as an additonal conductor is usually applied surrounding the edge of wafer for 'current thieving', thereby it is also called a current thief ring, as shown in Figure 4-3*b*. The current thief ring can be controlled using the same or separate power supply depending on actual applications.

The influence of photoresist patterns on the electrodeposition process has been recognised as an important factor which may change the current density distribution

on the pattern and feature scale, thus the bump shape and uniformity. Mehdizadeh *et al* [106, 107] found that the deposition rate of copper onto a patterned substrate had a certain relation with pattern density and proposed a factor called 'active-area density', which was the ratio between the actual electroplating area and the superficial area, in order to predict the current distribution at the workpiece and pattern scale. Unevenly distributed patterns induce non-uniform current distribution leading to a non-uniform deposition rate, which can be described as a pattern density effect. In general, the regions having smaller features tend to draw higher current density [106-109].

The current distribution at a pattern scale can be improved by carefully designing electroplating patterns and conditions. On the one hand, the effect of pattern density could be compromised by choosing a relatively lower electroplating rate and selecting more evenly populated photoresist patterns [106]. On the other hand, the conditions for mass transport play another important role in determining the uniformity of current density distribution at the pattern scale [25].

The current distribution at a feature scale primarily defines the shape of growth front of bumps and homogeneity of the aperture filling [110]. In general, current crowding occurs near the entrance of apertures due to the existence of the photoresist, as shown in Figure 4-4. Thus, the current distribution perpendicular to current lines becomes non-uniform. The edge of bumps normally attract a higher current density leading to a faster deposit growth and the deposited bumps may appear with a 'rabbit ear' shape [111]. Moreover, the geometric appearance of the photoresist pattern also plays an important role in current distribution at a feature scale. The angle of side walls of photoresist apertures can affect the current crowding near the opening of apertures, therefore influencing the shape of resultant deposits [112]. Coincidently, the crowded current also induces an increased flow of reacting species which would affect the non-uniformity at the feature scale. By using the hierarchical model, Dukovic [93] calculated current distribution at the feature scale and concluded that smaller features can normally attract higher current density. As mentioned above, the current distribution at the roughness scale is likely to be determined by the chemical composition of the electrolyte and organic additives, for a given electrochemical system, and is not considered further here.

On the feature scale, current distribution relies on potential and concentration gradient of reactant ions within an aperture. Additives acting as levelling agents are usually employed to achieve an even deposition rate at the feature scale [2]. The

levelling agent performs as an inhibitor of the electrodeposition reaction and its activity is dependent on the mass transport. The peak sites are more easily accessible for the additives than the recesses of the surface profile, therefore the deposition on the peak sites are more strongly hindered. In addition, the hydrodynamic conditions also affect the bump growth within apertures. It has been found that the evolution of the deposited bump shape and levelling effectiveness of the additives can be strongly influenced by diffusion conditions when electroplating is conducted close to the limiting current density [112].

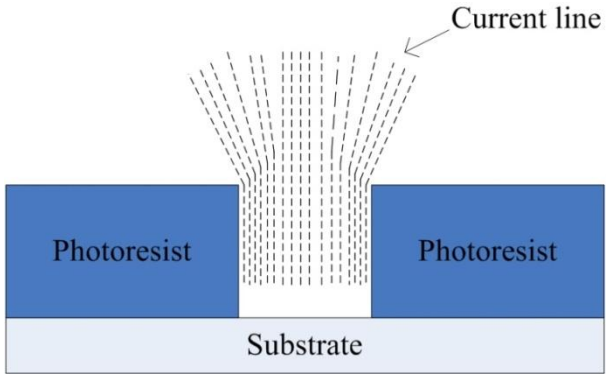


Figure 4-4 Schematic of current crowding effect near the entrance of the photoresist feature.

4.1.4 Mass Transport

Mass transport determines the limiting current density thus the maximum electrodeposition rate which is usually treated as a decisive factor for productivity. In the application of electroplating using a mask, mass transport often plays an important role in the evolution of the shape and microstructure of deposits [110]. During a bumping process, the mass transport condition at various scales across a wafer, *i.e.* at workpiece, pattern and feature scales, is of particular interest to be associated with bumping uniformity, which is also referred to as diffusion boundary layer distribution. The thickness of the diffusion boundary layer is dependent on the hydrodynamic field in the electroplating system. Therefore, a uniform distribution of the hydrodynamic field at the wafer scale is desired to achieve an even distribution of the diffusion boundary layer, which is usually governed by the fluid dynamics of an electroplating system.

4.1.5 Aim of This Chapter

This chapter considers the development of an indium bumping process by electroplating, through a thorough investigation of the influences of current distribution using both DC and pulsating current waveforms. As discussed above, electroplating bumping processes need to be carefully controlled to ensure an acceptable yield and uniformity of bumps. There are several technical approaches to adjust the current distribution at various scales; however, an optimum cannot be achieved without a fundamental understanding of the characteristics of electrodeposited indium bumps. For this reason, this chapter focuses on the formation of indium bumps under direct current electroplating, unipolar pulse electroplating and bipolar pulse reverse electroplating, whilst the influence of mass transport will be dealt with in Chapter 5. In this chapter, the parameters used for electroplating are based on the results from the electroplating onto non-patterned substrates demonstrated in the previous two chapters. In order to obtain more homogenous deposits, both pulse and pulse reverse electroplating are employed as compared to DC electroplating.

The electroplated indium bumps are characterised in terms of their morphology, shape, microstructure and uniformity at different length scales. Considering different scales of current distribution, the bumping uniformity is quantified at wafer, pattern and feature scale. As the indium sulphamate solution from a commercial supply is used and stable in its chemical composition, uniformity on the roughness scale is not considered. Therefore, bump uniformity, *i.e.* the variation of bump height, is measured at wafer, pattern and feature scale, and treated as the main index for the overall bumping uniformity.

4.2 Experimental Details

Indium bumping by electroplating was first conducted on 3 inch glass test wafers for the sake of cost reduction and easy handling in the preliminary investigation. Both DC and pulse current electroplating were carried out and the deposited bumps and their morphology, microstructure, growth characteristics and uniformity were examined. Because this research was also targeting the fabrication of a real pixel detector in

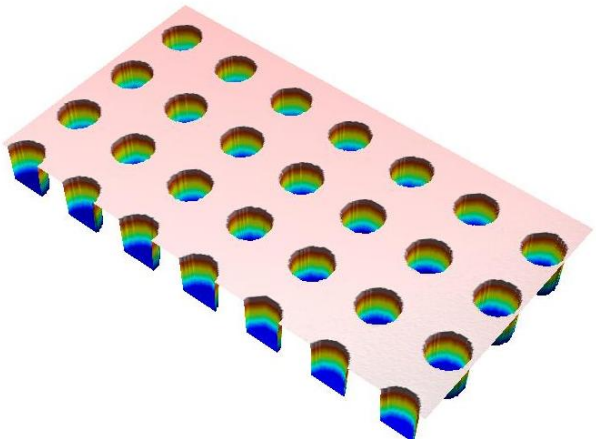
collaboration with RAL, the indium bumping process was subsequently extended onto 4 inch wafers.

4.2.1 Sample Preparation

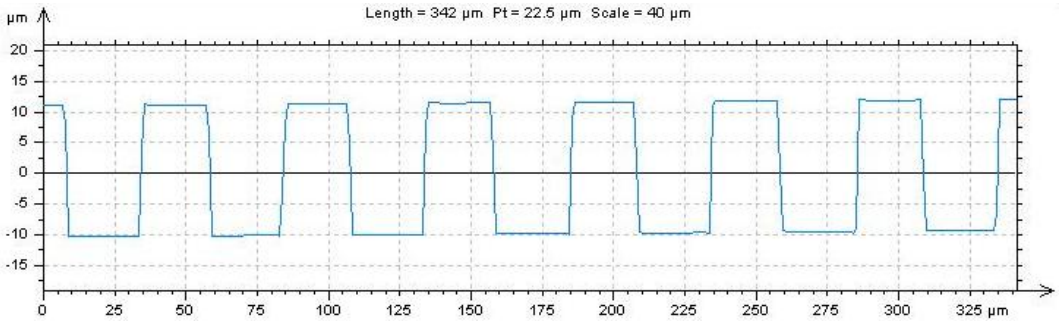
As mentioned above, two sets of wafer samples were prepared for the experiments. Dummy glass wafers (3 inch) were used for the primary experiments at a lower cost compared to commercial 4 inch silicon wafers. Glass wafers were firstly cleaned using acetone assisted by an ultrasonic bath. Then, a thin Ti/Cu seed layer was evaporated onto their surfaces by using an electron-beam evaporator, which consists of about 100 *nm* Ti and 100 *nm* Cu. Ti was used as an interlayer to improve the adhesion of the copper film onto the glass. It should be noted that copper is not normally utilised as an appropriate UBM for indium bump bonding. Copper is used as a part of seed layer in this research due to its excellent electrical conductivity and convenience of preparation. Once the seed layer was deposited, a thick photoresist was spun and developed to form the required patterns which were pre-defined using a mask. A positive photoresist *AZ 9260*, was chosen as it was easy to be removed after electroplating. Table 4-1 lists the parameters for the patterning process for 3 inch glass wafers to produce a photoresist layer about 20 μm thick. Between baking and exposure, the photoresist needed to be left in air at least two hours for rehydration and stabilisation before being exposed under ultraviolet (UV) light. Such developed photoresist patterns were evaluated using a Zygo NewView 5000 white light interferometer. Figure 4-5 shows a three dimensional view and profile of one type of photoresist pattern developed through the given parameters. It was found that the sidewall of apertures was more than 85º indicating that the patterning process was reliable and capable of ultrafine pitch indium bumping.

Table 4-1 Parameters for *AZ 9260* photoresist patterning process for 3 inch glass wafers.

Procedures	**Parameters**
Dispensing cycle	70 *rpm*, 20 *s*.
Spread cycle	400 *rpm*, 20 *s*.
Final cycle	1000 *rpm*, 30 *s*.
Soft baking	80 *ºC*, 60 *s*.
Hard baking	110 *ºC*, 240 *s*.
Exposure (UV)	1800 J/cm^2.
Development (AZ 400K 1:4 in H_2O)	260 *s*.



(a) 3D view of the photoresist pattern on 3 inch glass wafers



(b) Cross-section profile of the photoresist pattern at the centre of feature.

Figure 4-5 Three dimensional view and cross-section profile of photoresist pattern produced using Zygo white light interferometer.

4 inch silicon wafer samples were purchased from Compart Technology Ltd, UK, and a similar procedure for patterning was utilised as described above for glass, except that the duration of the spread cycle and final cycle were increased. In this case, a large amount of photoresist was needed to achieve 20 μm thickness due to a larger area of coverage.

4.2.2 Electroplating Indium Bumping Procedure

The electroplating bumping process flow can be illustrated as in Figure 4-6. Followed by wafer patterning steps, indium bumps were electroplated onto the seed layer through apertures in the photoresist patterns. The photoresist was then dissolved in acetone to reveal the indium bumps on the wafer. Next, the seed layer was etched away to isolate electroplated bumps and wafers were then reflowed to form truncated spherical indium bumps.

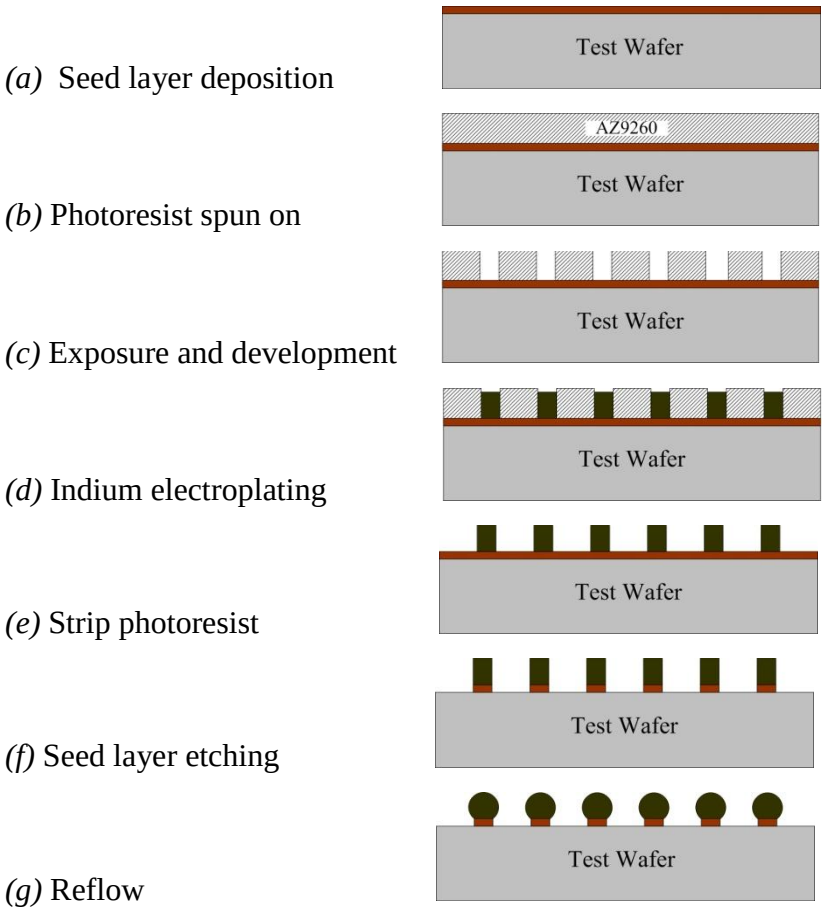


Figure 4-6 Schematic of the electroplating indium bumping process using indium sulphamate solution on patterned wafer.

4.2.3 Configuration of the Electroplating Systems

For electroplating with 3 inch wafers, a 500 *mL* electroplating bath was used as illustrated in Figure 4-7 and was placed in an ultrasonic bath (30 *kHz*) so that the pattern could be pre-wetted prior to the deposition. The pre-wetting step by ultrasonic agitation is essential for ultrafine pitch bumping by electroplating according to the preliminary experiments. Prior to electroplating of indium, the ultrasonic bath was switched on for 5 seconds to allow an effective penetration of the electroplating solution into the apertures. As soon as the ultrasonic power was switched off, the electroplating process was started. Ultrasonic agitation and its effects on the bumping process will be discussed later in Chapter 5. The anode used for electroplating was an 8 *cm* × 8 *cm* 99.99% pure indium plate. Similar to the previous electroplating trials, the anode plate and test wafers were vertically placed in the electroplating bath facing each other. No agitation was provided during the electroplating processes.

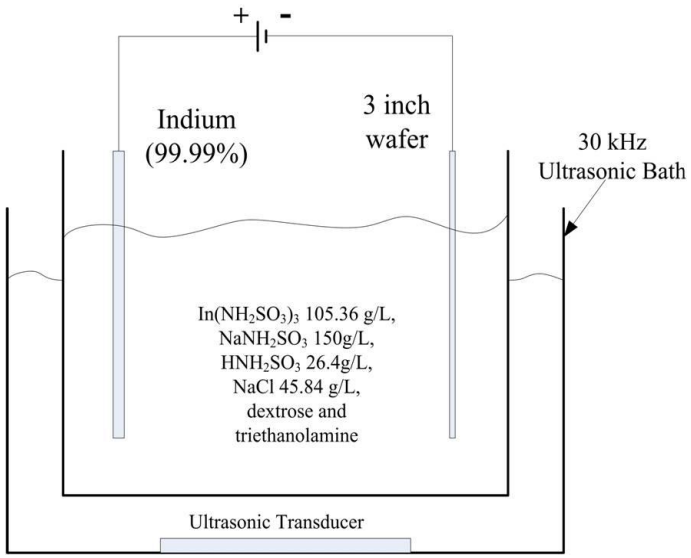
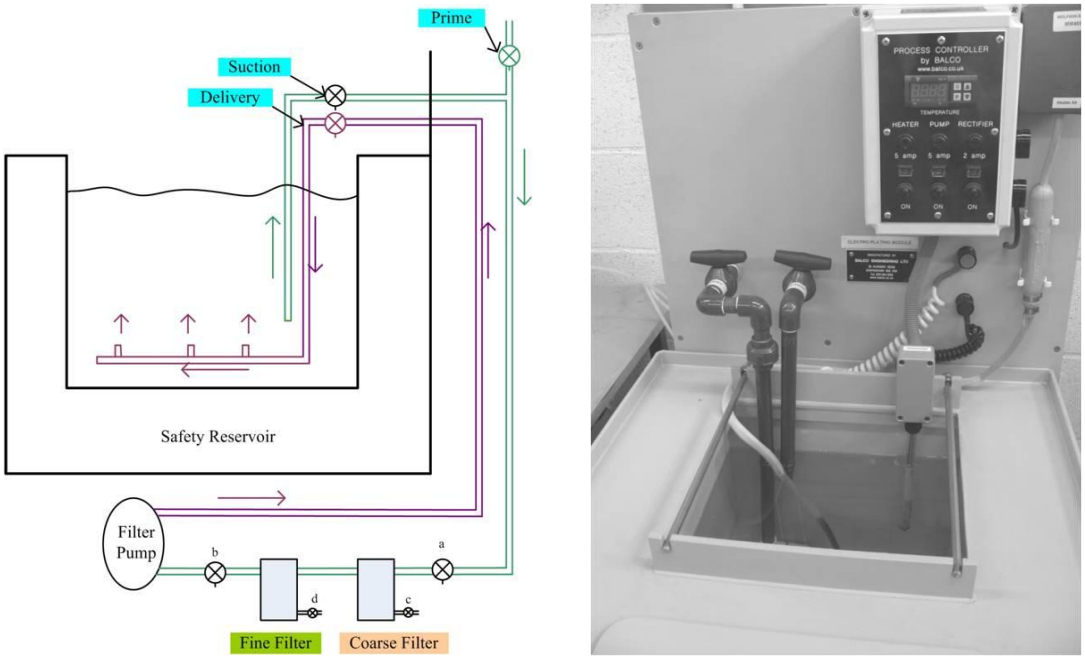


Figure 4-7 Configuration of electroplating bumping bath for 3 inch samples using indium sulphamate solution with ultrasonic bath (for pre-wetting of photoresist patterns).

An electroplating tank was commercially designed and supplied capable of electroplating 8 inch silicon wafer samples, as demonstrated in Figure 4-8. A 35 × 35 × 35 cm^3 tank of approximately 42 *L* capacity was filled with indium sulphamate solution. The electroplating tank was fitted with a circulation system using a pump

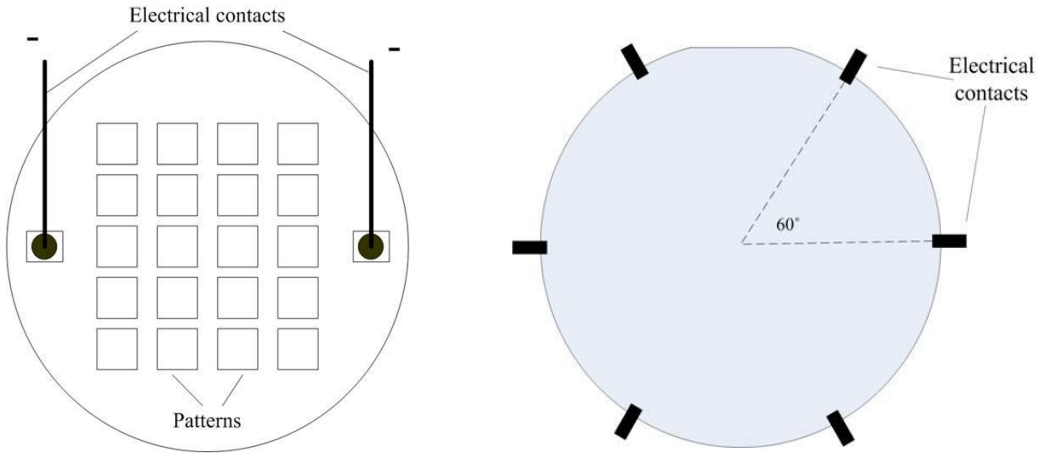
and two cartridge filters designed for 10 μm and 0.5 μm filtration, respectively. A coil heater and thermometer were built into the tank enabling temperature monitoring during the electroplating process. The anode used in this tank was an indium plate (99.99% indium purity) with a diameter of 10 *cm*.

During electroplating, electrical power was delivered to the 3 and 4 inch wafer samples through different configurations, respectively. For 3 inch wafers, two metal wires were soldered to the seed layer near the edge of the wafers, diametrically opposite to each other, to provide electrical contact (Figure 4-9*a*). For 4 inch wafers, the electrical contact was made through 6 gold plated tips evenly distributed along the periphery (Figure 4-9*b*) which was expected to provide more uniform current distribution. With the intention to set-up for electroplating 4 inch wafer samples as a viable industrial-scale bumping process, a wafer holder was designed to enable an evenly distributed electrical current across the wafer and to protect the wafer edge and back from corrosive electrolyte. The materials for making this wafer holder were required to have no chemical/electrochemical reaction with the electroplating solution and not lead to contamination of the electrolyte.



(a) Configuration of the electroplating tank *(b)* Electroplating tank set-up

Figure 4-8 Electroplating plant for indium bumping on 4 inch wafer: (a) configuration of the electroplating plant; (b) the actual set-up of the plant.



(a) 3 inch wafer *(b)* 4 inch wafer

Figure 4-9 Electrical contact configurations for: (a) 3 inch glass wafer; (b) 4 inch wafer.

Figure 4-10 provides a drawing of the assembled holder with a view of some details. Rigid polyurethane was utilised for making the non-conductive parts as this material has an excellent chemical resistance and machining properties. As can be seen in Figure 4-10, a wafer sample coated with a copper seed layer and photoresist pattern rested on a pedestal, which was sealed by O-rings *1* and *2* to ensure the wafer edge was isolated from the solution when the whole device was immersed into an electrolyte. Electrical contact was realised through six gold-plated pins (supplied by Connector Solutions Ltd.) loaded with springs in order to connect to a stainless steel ring. This ring was connected to the power supply through a tunnel in the handle. A circular cover was then placed and screwed onto the pedestal to expose the central circular area when the patterned wafer was located in the electroplating solution. Dimensional details of each part of the assembly can be found in Appendix 1, and an image of the actual device is shown in Figure 4-11.

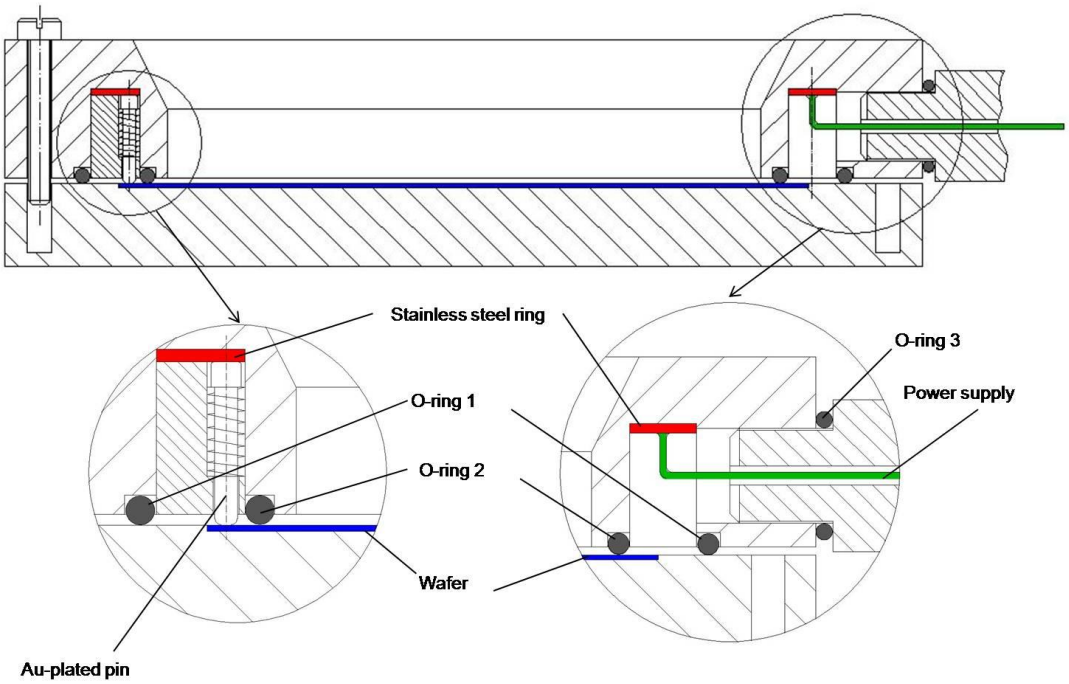


Figure 4-10 Assembly of wafer holder for electroplating on 4 inch silicon wafer samples.

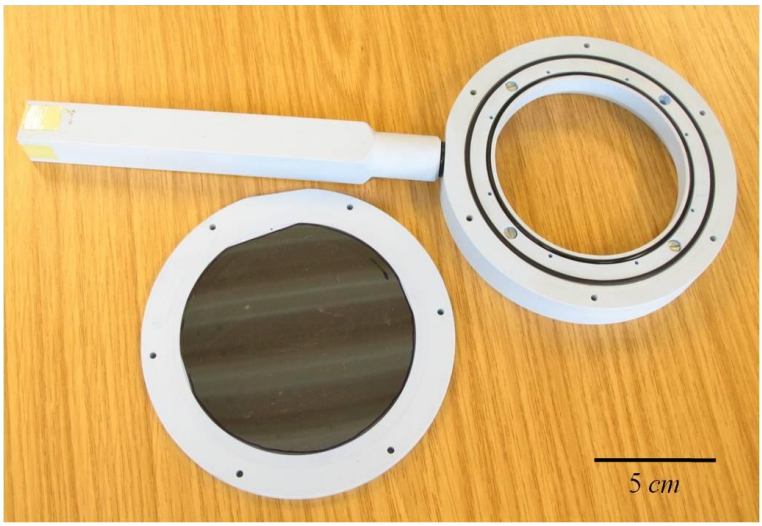


Figure 4-11 Actual wafer holder made from rigid polyurethane.

4.2.4 Photoresist Pattern Layout

Several types of pattern were designed for different sized wafer samples from which photomasks were prepared for the lithography process. Because the *AZ 9260* was a 'positive' photoresist, the corresponding photomask was made as a 'negative' (dark field). In other words, the photoresist exposed to the UV light was damaged and removed by the *AZ 400K* developer (see Figure 4-12). A current thief ring design was taken into account for both 3 inch and 4 inch photomasks which was a blanket circular area surrounding the patterns (Figure 4-13). For the 3 inch wafers, 6 types of patterns with various diameters and pitch sizes were included in one wafer sample to investigate the details of the patterns' effects on the capability of indium bumping by electroplating. For 4 inch wafers, 5 different photomasks containing various patterns were also produced to allow a systematic evaluation of the bumping process at different scales. The details of these photomasks are listed in Table 4-2 and the geometrical configuration can be found in Appendix 2. The photomasks were made on Agfa 180 μm high resolution polyester film.

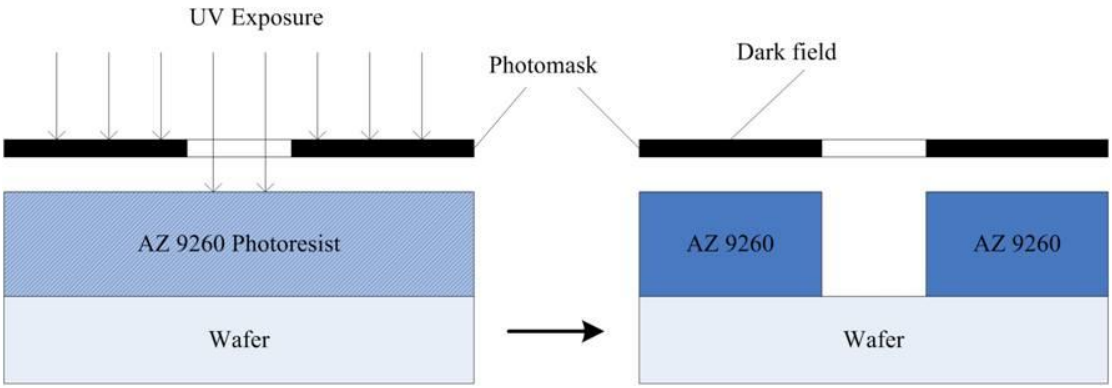


Figure 4-12 Schematic of process of A*Z 9260* photoresist development.

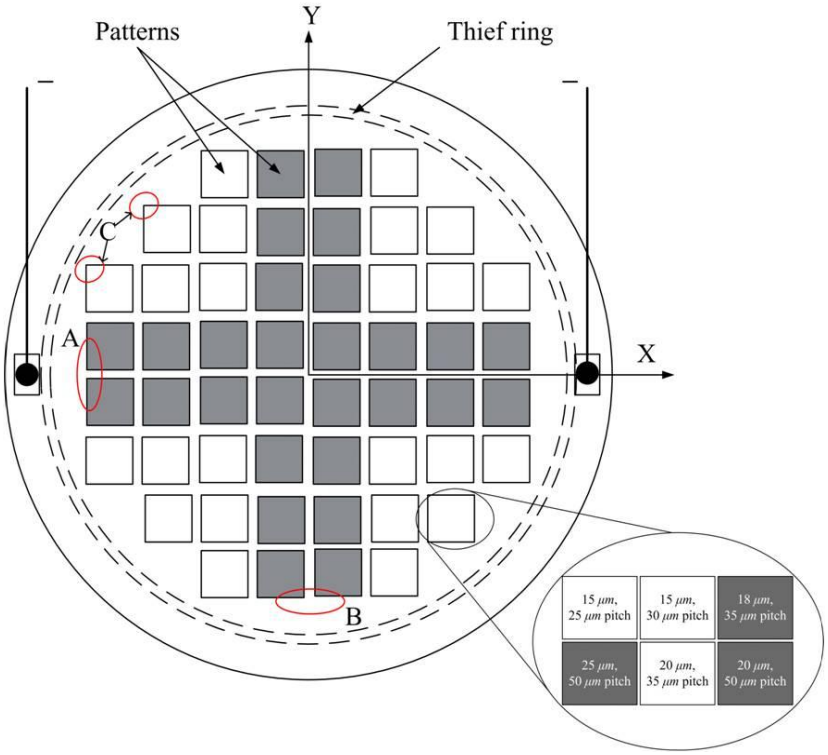


Figure 4-13 Configuration of photoresist patterns and electrical contact on 3 inch wafer samples.

Table 4-2 Details of photomasks for 3 inch and 4 inch wafer patterning.

Type		**Thief Ring (Y/N)**	**Contain Features (bump diameter / pitch size, *μm*)**
3 inch		No	25 / 50 ; 20 / 50 ; 20 / 35 ; 18 / 35; 15/30; 15/25.
		Yes	25 / 50 ; 20 / 50 ; 20 / 35 ; 18 / 35.
4 inch	No. 1	No	20 / 50.
	No. 2	Yes	25 / 50 ; 20 / 40 ; 18 / 36 ; 15 / 30.
	No. 3	Yes	25 / 50 ; 20 / 40 ; 18 / 36 ; 15 / 30.
	No. 4	Yes	20 / 36 ; 20 / 60 ; 20 / 120 ; 20 / 220 .
	No. 5	Yes	20 / 50.

4.2.5 Electroplating Parameters

Based on the preliminary results presented in the previous chapters, the electroplating parameters used in bumping are listed in Table 4-3. For DC electroplating, indium

bumps obtained through different current density were compared. Three pulse current waveforms were employed and the average current densities for pulse electroplating and pulse reverse electroplating were kept at 10 mA/cm^2. All of the electroplating trials were carried out at room temperature. To deposit indium bumps through pulse reverse electroplating, the patterned wafer samples were pre-electroplated using current waveform *No. 3* in Table 4-3 for 5 minutes to prevent Cu seed layers from being dissolved into the indium sulphamate electrolyte. The electroplated samples were then continuously electroplated for 55 minutes through the two pulse reverse current waveforms. The DC electrodeposition at 20 mA/cm^2 was conducted for 30 minutes while the rest of the electroplating trials were carried out for 60 minutes. Power supply and various current waveforms were provided by the Potentiostat (PARSTAT 2273 Ametek). As stated earlier, all the wafer samples to be electroplated were pre-wetted using the ultrasonic bath, but the rest of the electroplating was carried out without any agitation.

Table 4-3 Parameters of DC, pulse and pulse reverse electroplating for indium bumping using sulphamate solution.

	Type I: DC Electroplating					
No.	i_{avg} (mA/cm^2)					
1	10					
2	20					
	Type II: Pulse Electroplating					
No.	t_{on} *(ms)*	i_p (mA/cm^2)	t_{off} *(ms)*	Frequency *(Hz)*	*Duty cycle (%)*	i_{avg} (mA/cm^2)
3	1	50	4	200	20	10
4	2	50	8	100	20	10
5	1	100	9	100	10	10
	Type III: Pulse Reverse Electroplating					
No.	$i_{p(c)}$ (mA/cm^2)	$t_{on(c)}$ *(ms)*	$i_{p(a)}$ (mA/cm^2)	$t_{on(a)}$ *(ms)*	t_{off} *(ms)*	*Frequency (Hz)*	i_{avg} (mA/cm^2)
6	50	1.5	50	0.5	3	200	10
7	100	1.5	100	0.5	8	100	10

4.2.6 Seed Layer Etching and Reflow

After completing the electrodeposition step, it was crucial to strip the photoresist patterns and remove the seed layer to reveal the isolated indium bumps. It should be noted that liquid indium metal as a special solder material is able to wet glass and ceramics. Therefore, unlike the Sn-based solders, which do not wet passivated Si, *i.e.* Si_3N_4 [39], the reflow of electroplated indium bumps is more challenging. However, it was found that pure titanium which forms an interlayer of the UBM as part of the seed layer can act as the non-wettable base for reflowing indium bumps. Therefore, if the copper layer could be removed prior to the reflow step, it was possible to form indium bumps by reflowing.

Two approaches were investigated to remove the copper seed layer: argon plasma and wet chemical etching, the results of which are described in more details in section 4.3.5. A Plasmalab 80 Plus (Oxford Instruments) was utilised to generate the argon plasma and removed the copper seed layer and a thin layer of exposed indium at the same time. Because the seed layer was very thin, this was not expected to significantly reduce the height of the indium bumps on the wafer after etching. Alternatively, etching in an acidic solution was used which is relatively easy to operate. As has been mentioned, the standard potential of In^{3+} is -0.34 *V* (relative to standard hydrogen electrode), which means indium is active in aqueous acidic solutions. Therefore, chemical etching will inevitably affect indium in the reactions depending on the chemistry of the solution to be used. For a similar reason, it is acceptable if only small amounts of indium are removed due to the reactions.

Once the copper seed layer was removed, the indium bumps were reflowed. Figure 4-14 shows temperature profile for reflowing indium bumps. The state-of-the-art indium bump bonding process utilises formic acid vapour to fill the oven to eliminate possible oxidation, but this was not available. Hydro X/20 water washable flux was applied with small amount on the wafer. The samples were heated up to 200 *ºC* in the air and held for 2 minutes to allow liquid indium to form a spherical shape by surface tension. After that, the residual flux was cleaned with deionised water at 60~70 *ºC*.

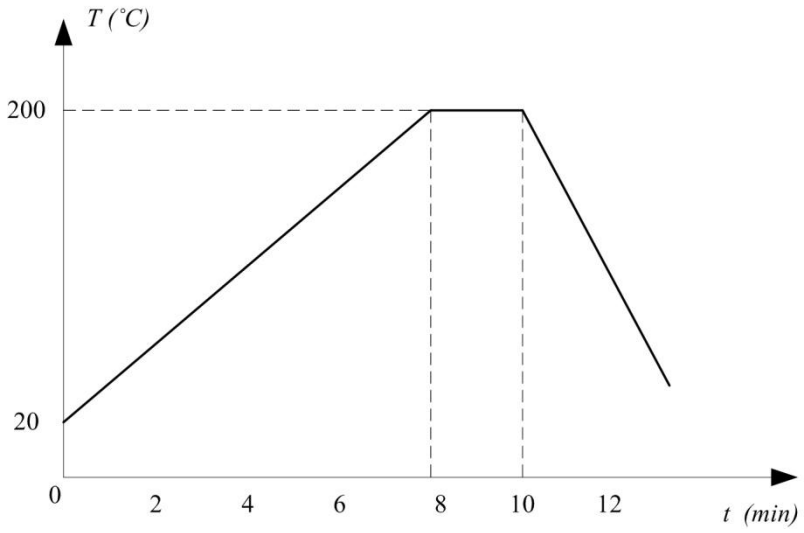


Figure 4-14 Reflow temperature profile for indium bumps after seed layer etching.

4.2.7 Characterisation

Surface morphology and geometric shape of the electroplated indium bumps were observed by Scanning Electron Microscopy (SEM). Because indium is very soft (Hardness 0.9 *HB* [33]), it is extremely difficult to perform traditional mechanical polishing to obtain a smooth surface or cross-section for metallographic analysis, as the indium can be easily contaminated and embedded by the abrasive particles. Thus, Focused Ion Beam (FIB) was utilised to assist the preparation of the cross-sectional view for microstructure analysis. Also, the ion beam secondary electron image is able to show the grain orientation contrast which can provide detailed information in terms of grain boundaries, grain size and preferential orientations. In addition, the composition at the interface was identified by Energy Dispersive X-ray Spectroscopy (EDX). The yield of the electroplated bumps was observed through SEM by counting the missing bumps within a certain area.

A Zygo NewView 5000 white light interferometer was also employed to observe the profile and the height of the electroplated bumps. The uniformity of the electroplated bumps was determined at the wafer scale, pattern scale and feature scale. Thus, the uniformity of the electroplated bumps could be defined as:

$$Uniformity = \frac{Max.\,Bump\ Height - Min.\,Bump\ Height}{2 \times Average\ Bump\ Height} \times 100\% \quad (4\text{-}1)$$

The details of the measurement are illustrated later in this chapter.

4.3 Indium Bumping Process Development

In this section, indium bumping through DC, unipolar pulse current and bipolar pulse reverse current electroplating were developed using 3 inch glass test wafers. The purpose of this section were to gain a knowledge base of the indium bumping technique in terms of bump morphology, microstructure, bump height uniformity, and the influences of photoresist patterns, current thief ring and seed layer removal on the reflow and bump formation process. In this section, bump height uniformity is only evaluated at the wafer scale for 3 inch wafer samples.

4.3.1 Indium Bumping Through DC Electroplating

Electroplating indium bumps using direct current was conducted at 10 and 20 mA/cm^2 respectively. A pre-wetting step by ultrasonic agitation was used for the fine-pitch bumping to achieve a higher yield. Figure 4-15 shows the incompletely electroplated patterns obtained mainly because of insufficient wetting prior to electroplating. It can be seen that the silver areas marked by a black arrow were electroplated with indium whilst the rest of the patterns were not or partially electroplated.

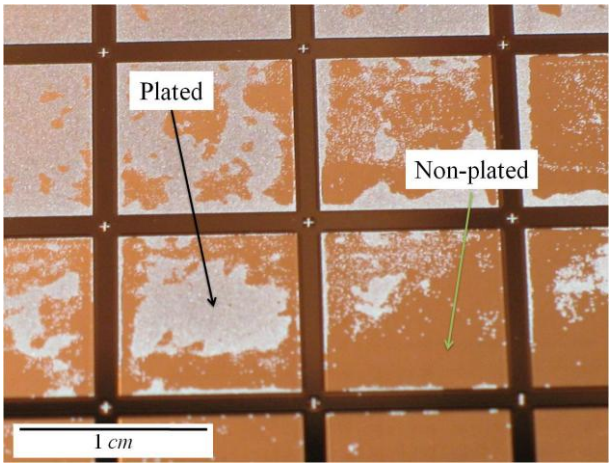
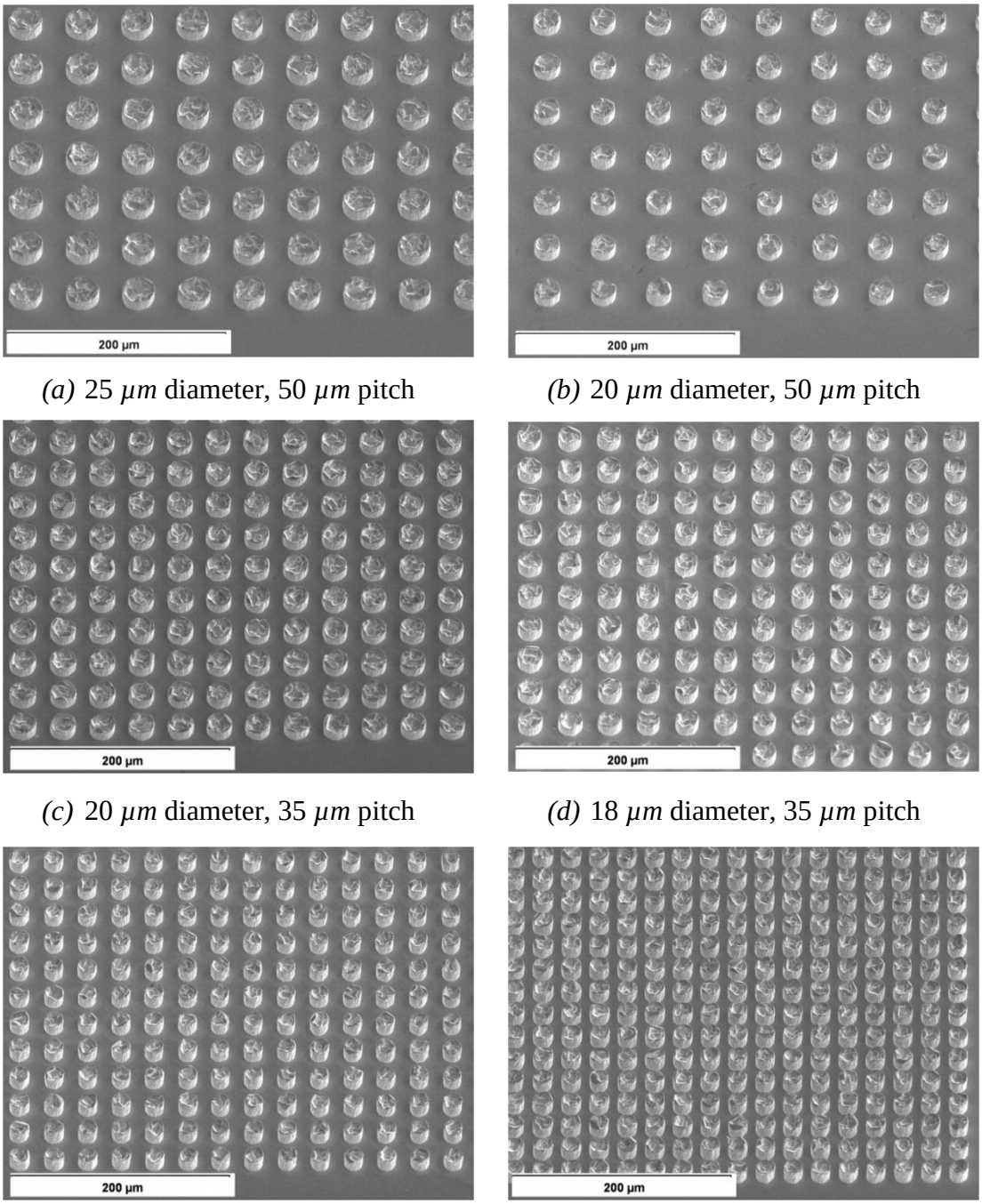


Figure 4-15 Poor wetting induced incompletely electroplated patterns.

When the current density was set at 10 mA/cm^2, the morphology of indium bumps near the centre of patterns with various diameters and pitch sizes was as shown in Figure 4-16. Bump sizes decreased from 25 μm to 15 μm while the pitch sizes shrunk from 50 μm to 25 μm. Assisted by ultrasonic pre-wetting, a bumping yield of more than 99.9% could be achieved indicating the capability of electrodeposition to generate high density indium bumps with high yield. Figure 4-17 shows the high magnification images of as-electroplated indium bumps with various diameters and pitch sizes. It can be seen that the as-electroplated bump has very coarse grains and uneven or irregular surface finish, where the edge of the bumps is higher than the central area. Typical large sized deposit's features similar to those shown in Figure 2-8 (page 35) are also found in the electroplated bumps, with an average size reaching ~10 μm. Such a large deposit's feature size can be seen to influence the overall bump uniformity when their size is 20 μm or less.

In the case of electroplating at 20 mA/cm^2, no noticeable difference in the bump morphology, as shown in Figure 4-18, can be seen. Electroplated bumps also had an uneven bump top finish and a large deposit feature size. In both cases, bump edges were obviously higher than the central area, indicating current crowding near the edge of wafers, as shown in Figure 4-19.



(a) 25 *µm* diameter, 50 *µm* pitch

(b) 20 *µm* diameter, 50 *µm* pitch

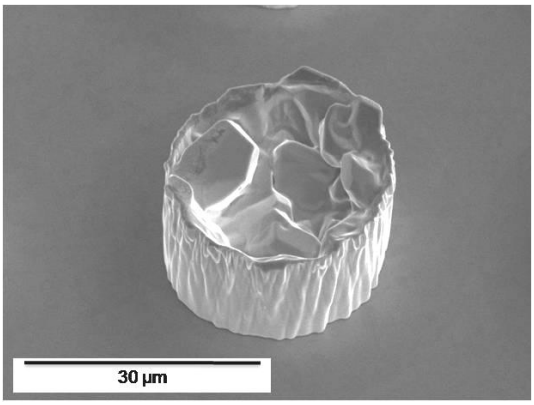
(c) 20 *µm* diameter, 35 *µm* pitch

(d) 18 *µm* diameter, 35 *µm* pitch

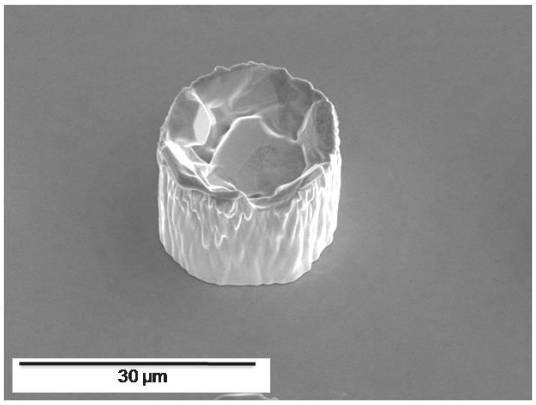
(e) 15 *µm* diameter, 30 *µm* pitch

(f) 15 *µm* diameter, 25 *µm* pitch

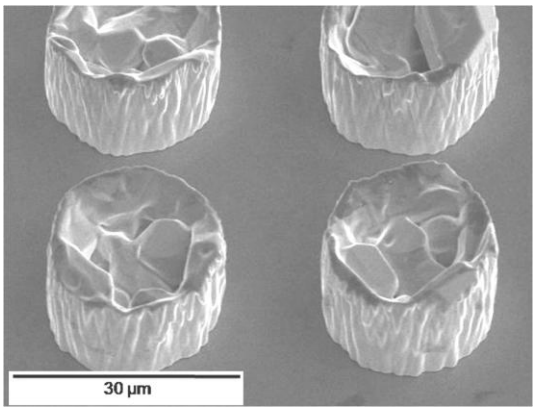
Figure 4-16 Overview of as-electroplated indium bumps (DC, 10 *mA/cm*^{2}) using indium sulphamate solution.



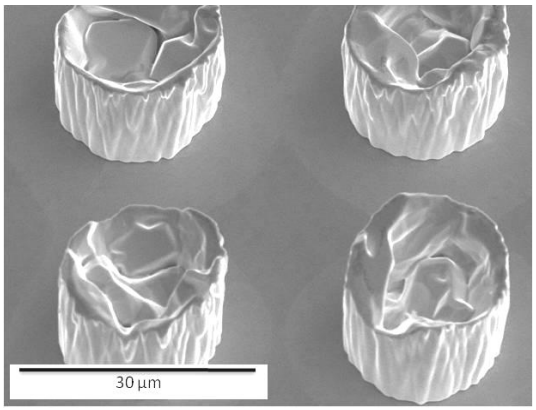
(a) 25 *µm* in diameter, 50 *µm* pitch



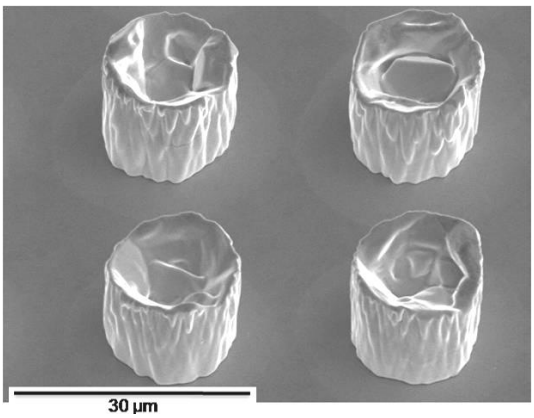
(b) 20 *µm* diameter, 50 *µm* pitch



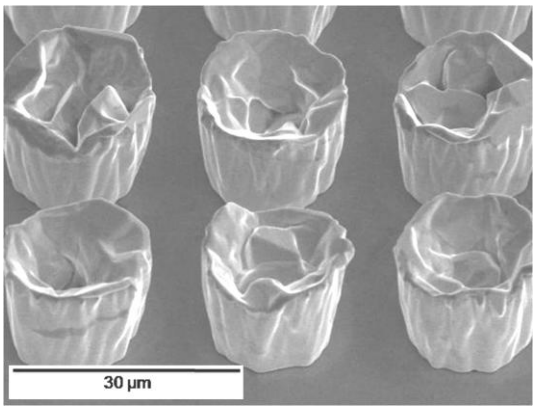
(c) 20 *µm* diameter, 35 *µm* pitch



(d) 18 *µm* diameter, 35 *µm* pitch

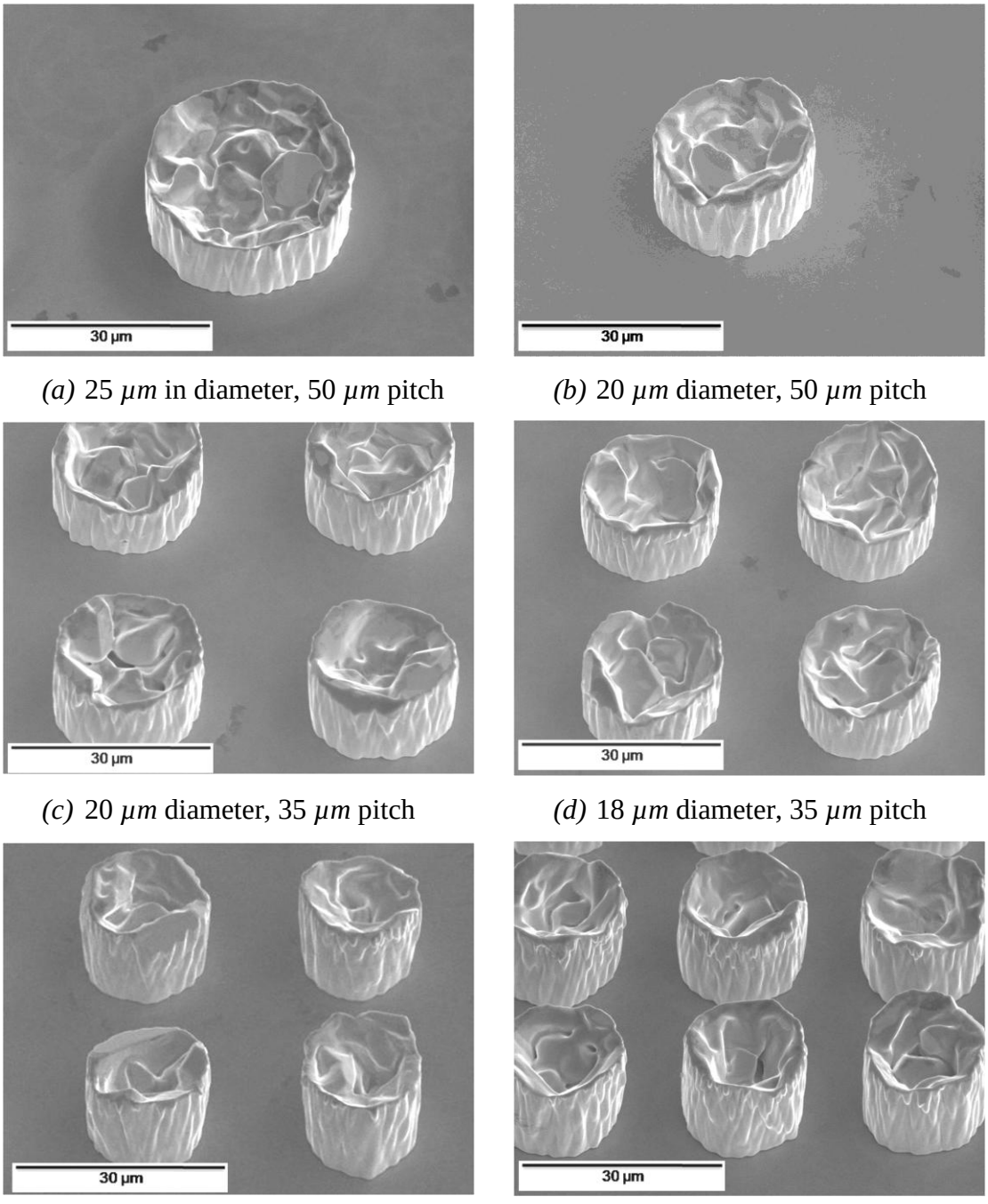


(e) 15 *µm* diameter, 30 *µm* pitch



(f) 15 *µm* diameter, 25 *µm* pitch

Figure 4-17 High magnification view of as-electroplated indium bumps using indium sulphamate solution through DC at 10 *mA/cm*^{2}.



(a) 25 μm in diameter, 50 μm pitch

(b) 20 μm diameter, 50 μm pitch

(c) 20 μm diameter, 35 μm pitch

(d) 18 μm diameter, 35 μm pitch

(e) 15 μm diameter, 30 μm pitch

(f) 15 μm diameter, 25 μm pitch

Figure 4-18 High magnification view of electroplated indium bumps using sulphamate solution through DC at 20 mA/cm^2.

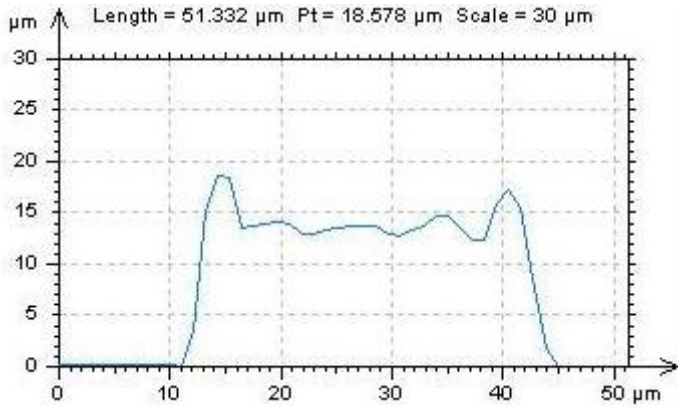
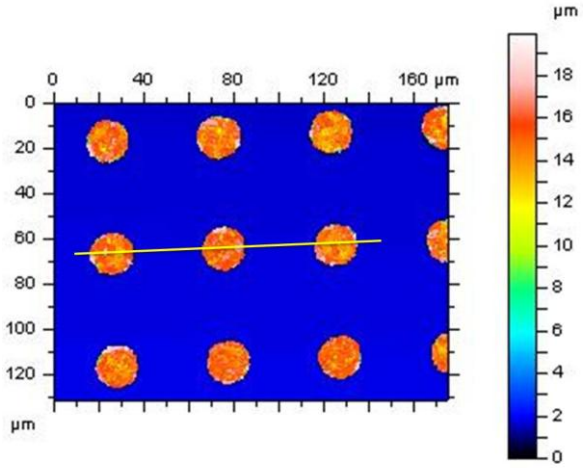
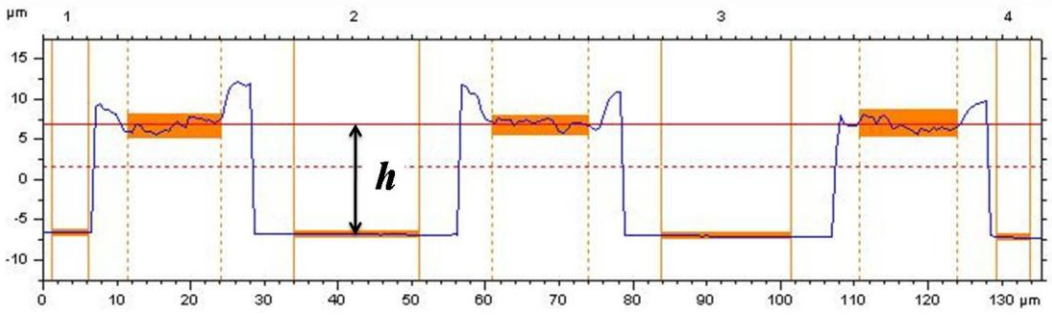


Figure 4-19 Profile of indium bump obtained by Zygo white light interferometer : electroplated at DC 10 *mA/cm*^{2}.



(a) Zygo image of bump height analysis



(b) Bump height measurement through cross section profile

Figure 4-20 Bump height measurement methodology using Zygo white light interferometer (indium bumps were electroplated through DC 10 *mA/cm*^{2} using sulphamate solution).

The bump height uniformity was measured using the Zygo white light interferometer at different areas across the wafer. As shown in Figure 4-13, the measurement of bump height was mainly carried out on the shaded patterns along *X* and *Y* directions respectively. The bump height at a certain area was obtained by averaging the height of adjacent ones. For example, as shown in Figure 4-20, the bump height (*h*) for the selected area was determined as an average value of 9 individual bumps within the view. A line profile for each bump was taken across the centre, *e.g.* the line shown in Figure 4-20*a*, and the height was determined by averaging the line (mean value) at feature scale (Figure 4-20*b*).

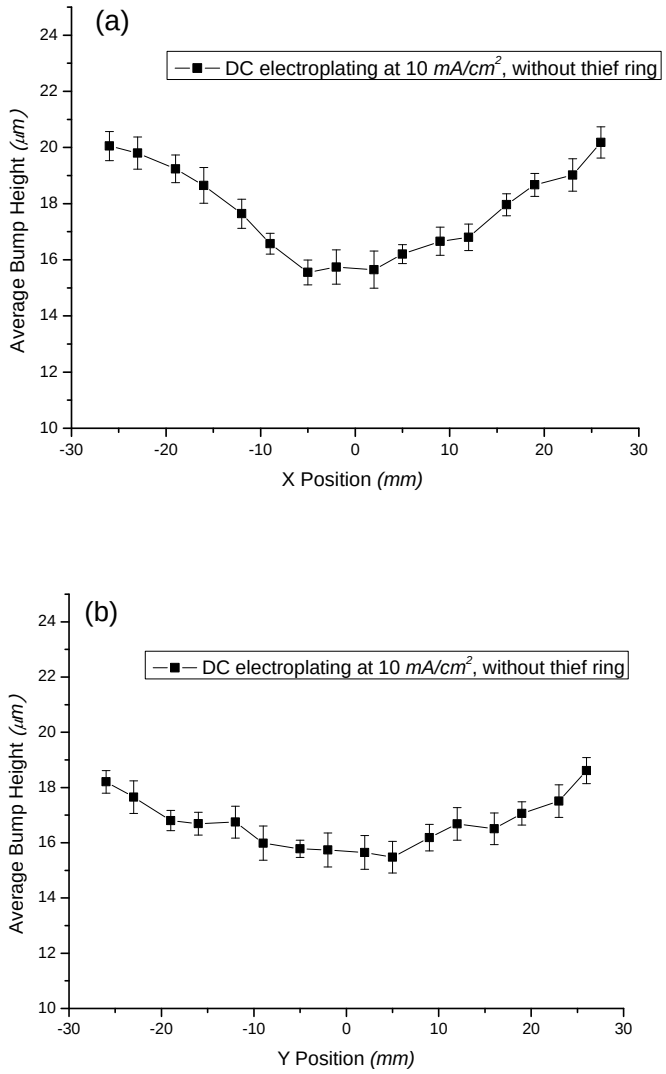


Figure 4-21 Bump height measurement of DC electroplated indium bumps on 3 inch wafer (10 *mA/cm²*, without thief ring) through: (a) X direction, and (b) Y direction.

In the case of electroplating with 3 inch wafers without a thief ring design, at both 10 and 20 mA/cm^2 current densities, the bump heights along X and Y directions are shown in Figure 4-21 and Figure 4-22, respectively. The zero point on the *X* and Y axes as a reference stands for the central point of the wafer. When the current density was 10 mA/cm^2, the height uniformity across the *X* and *Y* direction was measured as 21.43% and 13.5% respectively. When the current density was 20 mA/cm^2, the uniformity was 25.07% and 17.46%, respectively. The error bar presents the standard deviation of the bump height in a certain area. It can be seen that the bump height uniformity deteriorated more along the *X* direction for both cases compared with the value along the *Y* direction. Also, the uniformity deteriorated with increase of current density indicating that the bumping process should be carried out at a lower current density for an improved uniformity.

In both cases, the highest bumps were found in the area *A* shown in Figure 4-13 which has the shortest distance from the electrical contact point. The points along the *X* direction were a relatively short distance away from the contact points compared to those along the *Y* direction. Due to the terminal effect, the average bump height along the *X* direction was higher than that along the *Y* direction. However, although the area *B* shown in Figure 4-13 was further away from the electrical contact points compared with the central area, the bumps in the area *B* were still higher than those in the central area due to current crowding near the wafer edge, which was caused by the current crowding induced by the geometric configuration of the electroplating system, *e.g.* difference in the size of the anode and cathode.

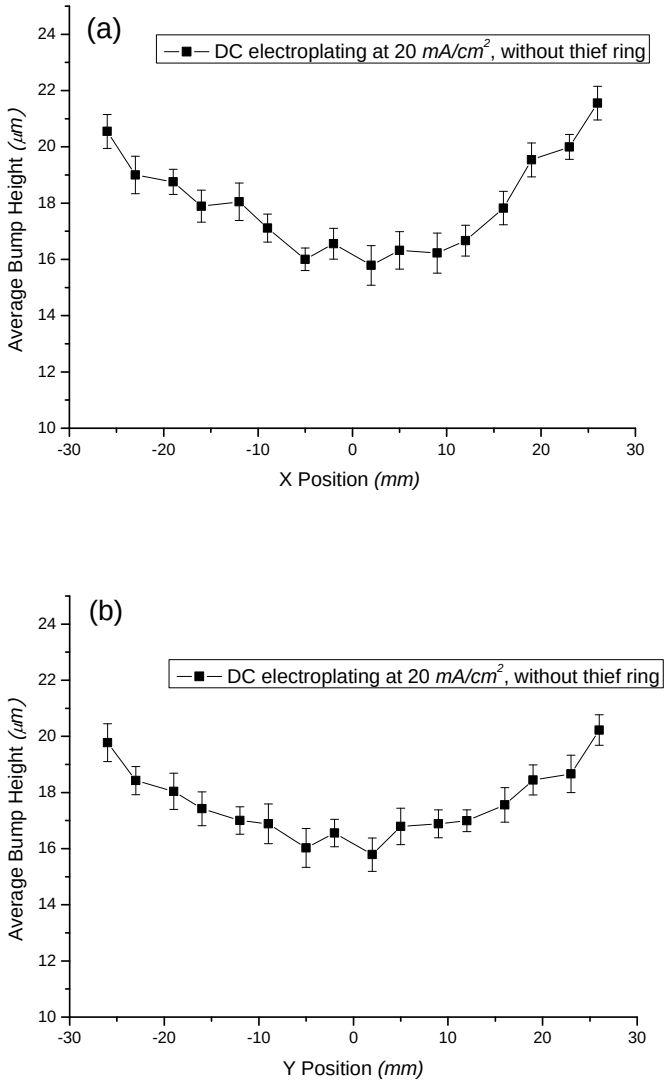


Figure 4-22 Bump height measurement of DC electroplated indium bumps on 3 inch wafer (20 *mA/cm*^{2}, without thief ring) through: (a) X direction, and (b) Y direction.

As predicted, the uniformity can be significantly improved when a thief ring is added to the pattern layout, as shown by the dashed circles in Figure 4-13. In Figure 4-23 and Figure 4-24, for the current density of 10 *mA/cm*^{2}, the uniformity was 16.15% and 15.84% along *X* and *Y* directions, respectively, and for 20 *mA/cm*^{2}, it was 19.05% and 18.22%, respectively. A higher current can still induce higher non-uniformity with the presence of a current thief. Interestingly, however, the highest bumps were now found in the area *C* shown in Figure 4-13.

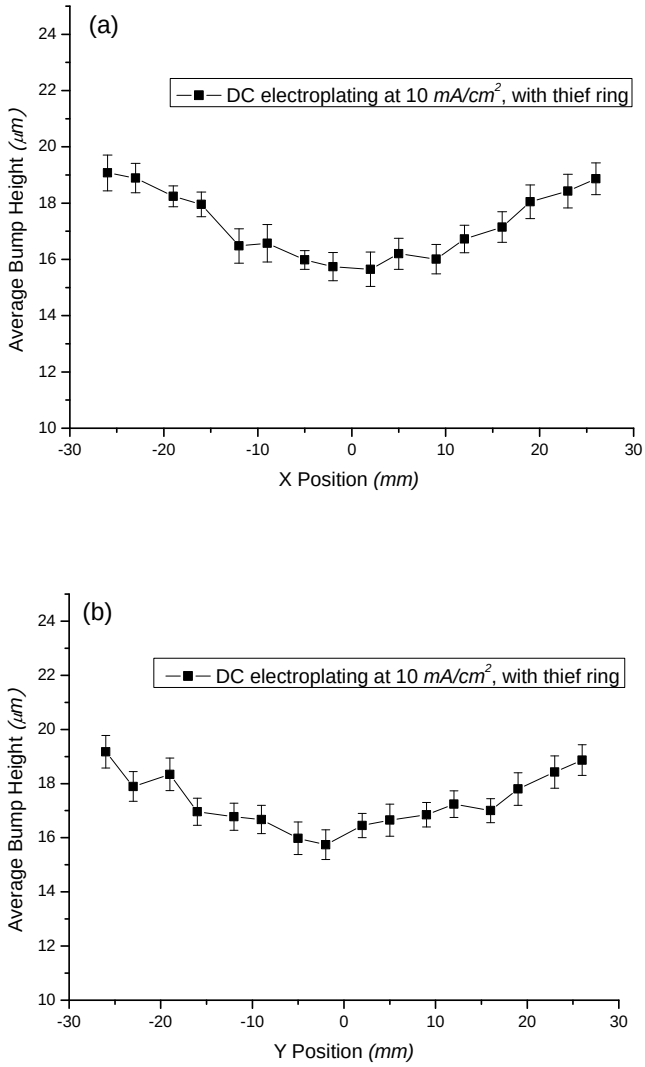


Figure 4-23 Bump height measurement of DC electroplated indium bumps on 3 inch wafer (10 *mA/cm²*, with thief ring) through: (a) X direction, and (b) Y direction.

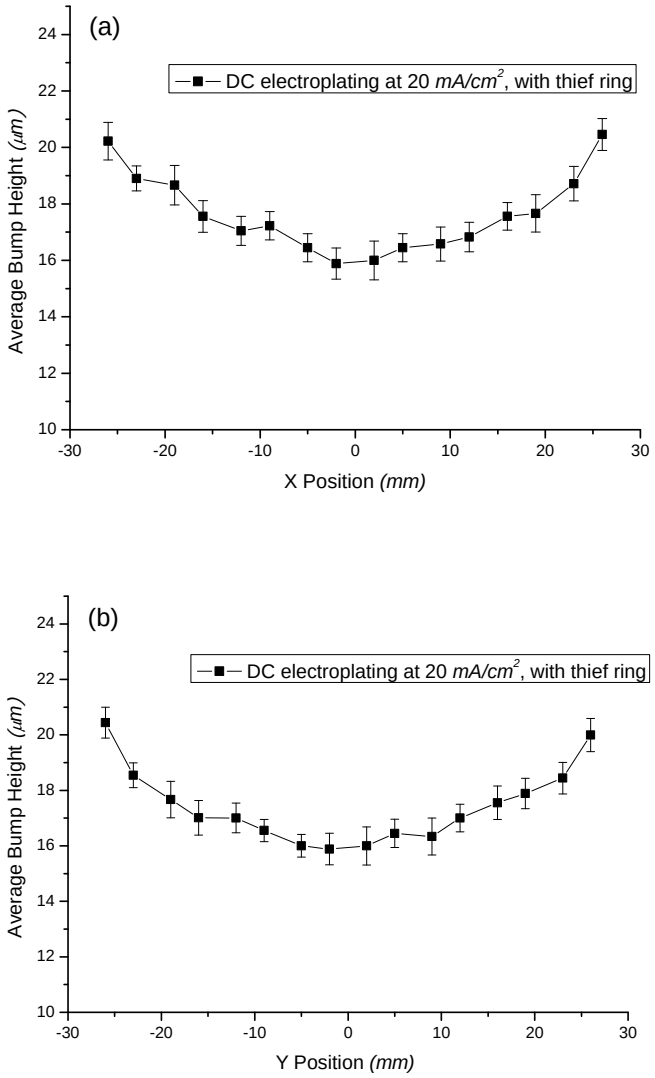


Figure 4-24 Bump height measurement of DC (20 *mA/cm*^{2}) electroplated indium bumps on 3 inch wafer (with thief ring) through: (a) X direction, and (b) Y direction.

It is apparent that the uniformity along the X direction was improved for both 10 and 20 *mA/cm*^{2} due to the placement of current thief rings. However, no improvement was seen across the Y direction due to the thief ring, in fact, the uniformity through the Y direction deteriorated in the presence of the current thief ring. Moreover, little difference in bump height distribution was seen between *X* and *Y* direction despite the different distances to the connection points. This behaviour can also be attributed to the presence of the current thief ring. At the beginning of the electroplating process, the thickness of the seed layer on the ring was very thin and the current distribution across the wafer would be strongly affected by the terminal

effect. However, once indium was deposited onto the ring, the thickness of the metallic coatings including indium increased, so did the electrical conductivity, thereby providing a continuous electrical contact around the circumference of the wafer. This compromised the directional effects caused by the two individual contact points such that the deposition along *X* and *Y* directions had no significant difference. This observation is supported by the fact that the largest bump height was found in the area *C* shown in Figure 4-13, which was not close to the connection points, but very close to the thief ring. A summary of the uniformities through different directions under various circumstances is illustrated in Table 4-4.

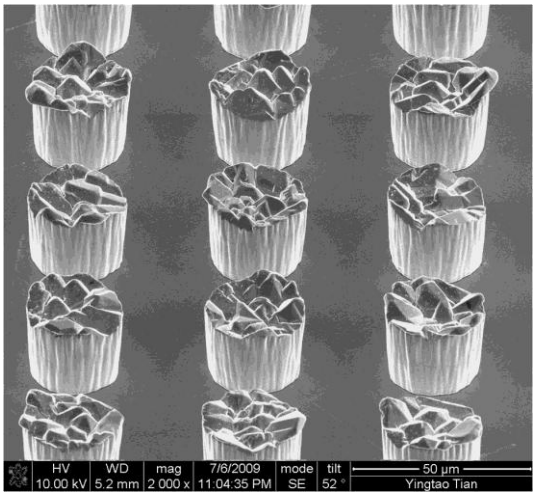
Table 4-4 Summary of the wafer scale DC electroplated bump height uniformity on 3 inch samples.

Current Density (mA/cm^2)	**Thief Ring (Y/N)**	**Bump Height Uniformity (%)**	
		X Direction	*Y Direction*
10	No	21.43	13.5
	Yes	16.15	15.84
20	No	25.07	17.46
	Yes	19.05	18.22

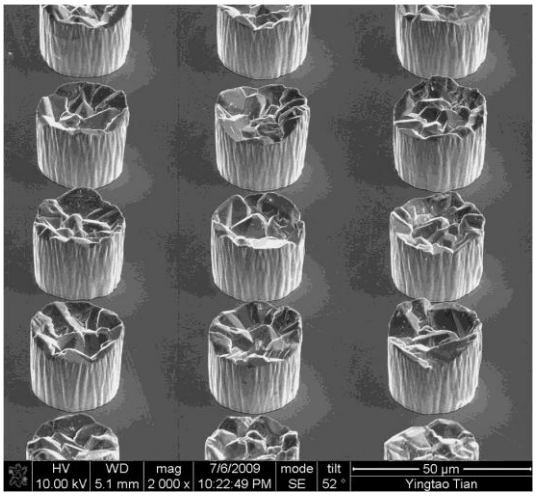
4.3.2 Indium Bumping Through Pulse Electroplating

Based on the above results, the average current density of pulse electroplating was selected as 10 mA/cm^2, and 3 inch wafers for pulse electroplating experiments contained a current thief ring. Figure 4-25 shows indium bumps deposited using the three pulse electroplating current waveforms listed in Table 4-3. The morphology of these bumps changed so that the conical morphology was observed which may be attributed to the increase of current density during the pulses. In general, the edge of the bumps was still higher than the centre of bumps indicating that the current crowding effect near the photoresist pattern opening still existed, as shown in Figure 4-26 (a typical Zygo bump profile), however, the pulse electroplating seemed to slightly reduce the difference on the feature scale compared with DC electroplating. As has been found in pulse electroplating with non-patterned substrates, neither pulse

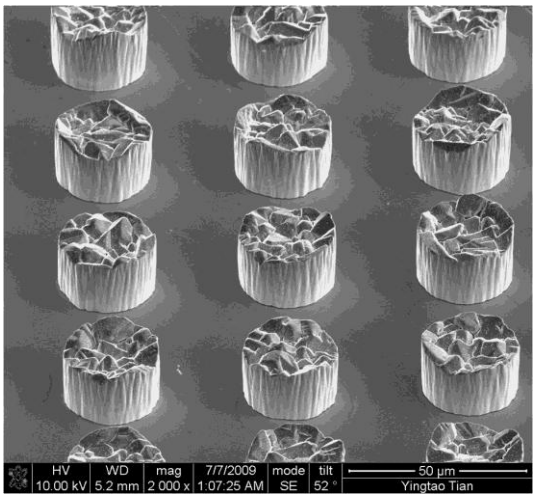
current density, frequency, nor duty cycle had any noticeable influence on bump morphology in pulse electroplating.



(a) 25 *µm*, 50 *µm* pitch, through waveform *No. 3*.



(b) 25 *µm*, 50 *µm* pitch, through waveform *No. 4*.



(c) 25 *µm*, 50 *µm* pitch, through waveform *No. 5*.

Figure 4-25 Overview of indium bumps deposited using different pulse electroplating waveforms: (a) waveform No. *3*; (b) waveform No. *4*; and (c) waveform No. *5*.

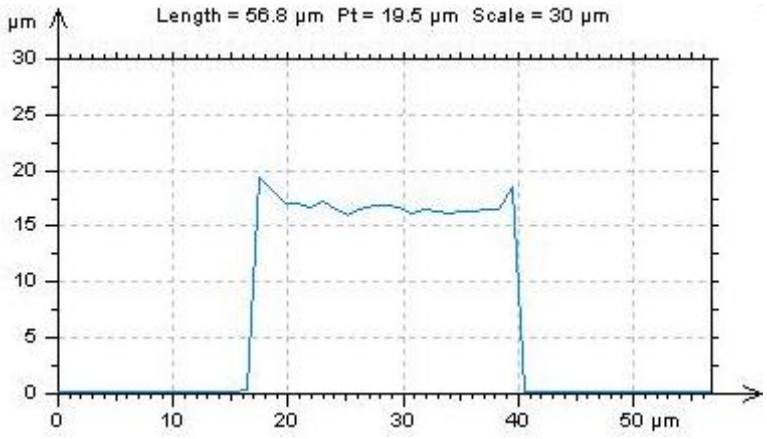


Figure 4-26 Profile of an indium bump deposited using pulse electroplating waveform *No. 3*.

Height measurement of the bumps obtained from pulse electroplating are presented in Figure 4-27, Figure 4-28 and Figure 4-29. As an average current density of 10 mA/cm^2 was used, the results should be comparable with DC electroplating bumping at the same current density. The bump height uniformity was 10.41 % and 10.09% along *X* and *Y* directions respectively if using current waveform *No.3*; it was 12.37% and 12.99% for waveform *No. 4*, and 12.58% and 13.16% for *No. 5*. These results showed that the uniformity of indium bumps deposited by pulse electroplating was improved in comparison to DC electroplating at the same current density, *i.e.* 10 mA/cm^2. Also, similar to DC electroplating, because of the use of a current thief ring, the bump height uniformity along *X* and *Y* directions had no significant difference. However, among three waveforms used, the current waveform *No. 3* gave the best uniformity. Table 4-5 summaries the evaluation of uniformity of indium bumps deposited using the three types of pulse electroplating waveforms.

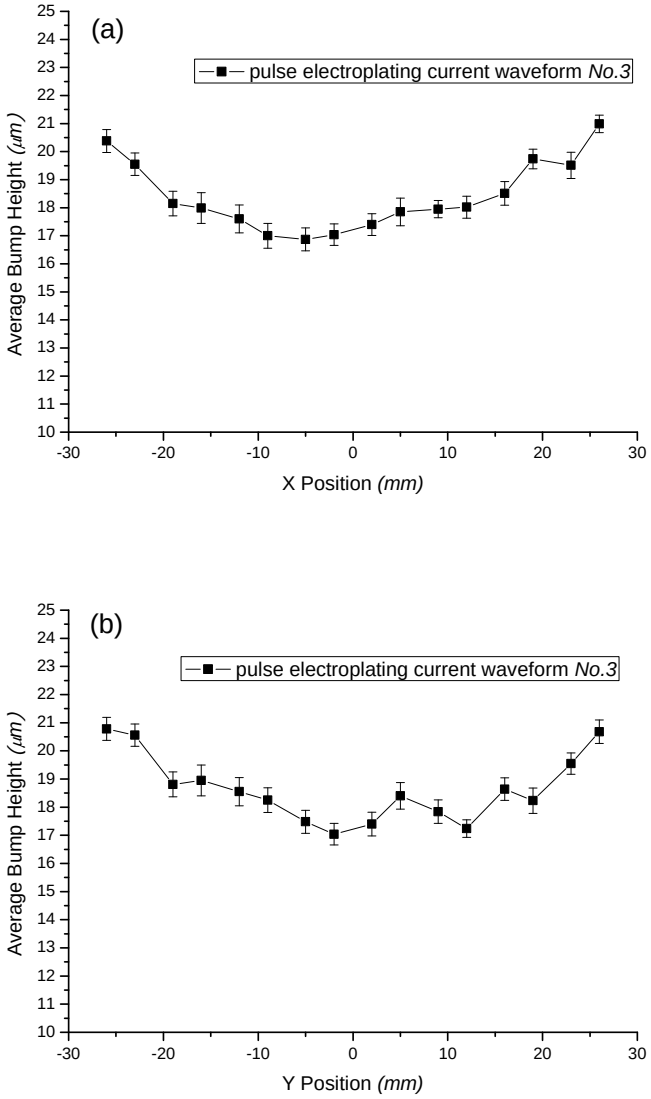


Figure 4-27 Height measurement of indium bumps obtained using pulse electroplating waveform *No. 3* on 3 inch wafer through: (a) X direction, and (b) Y direction.

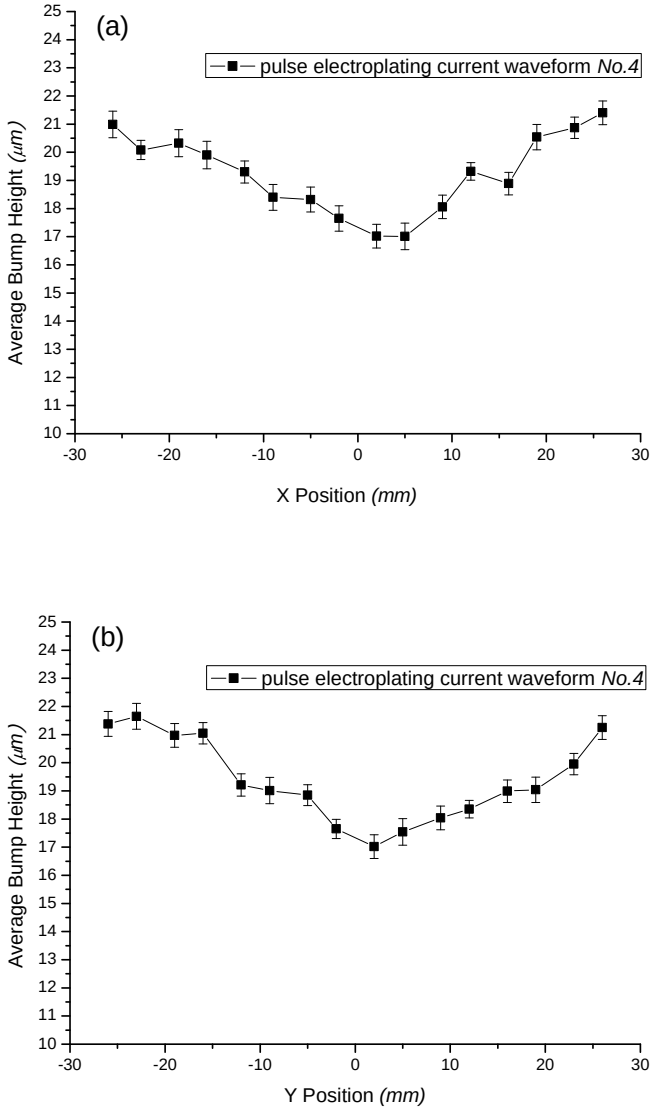


Figure 4-28 Height measurement of indium bumps obtained using pulse electroplating waveform *No. 4* on 3 inch wafer through: (a) X direction, and (b) Y direction.

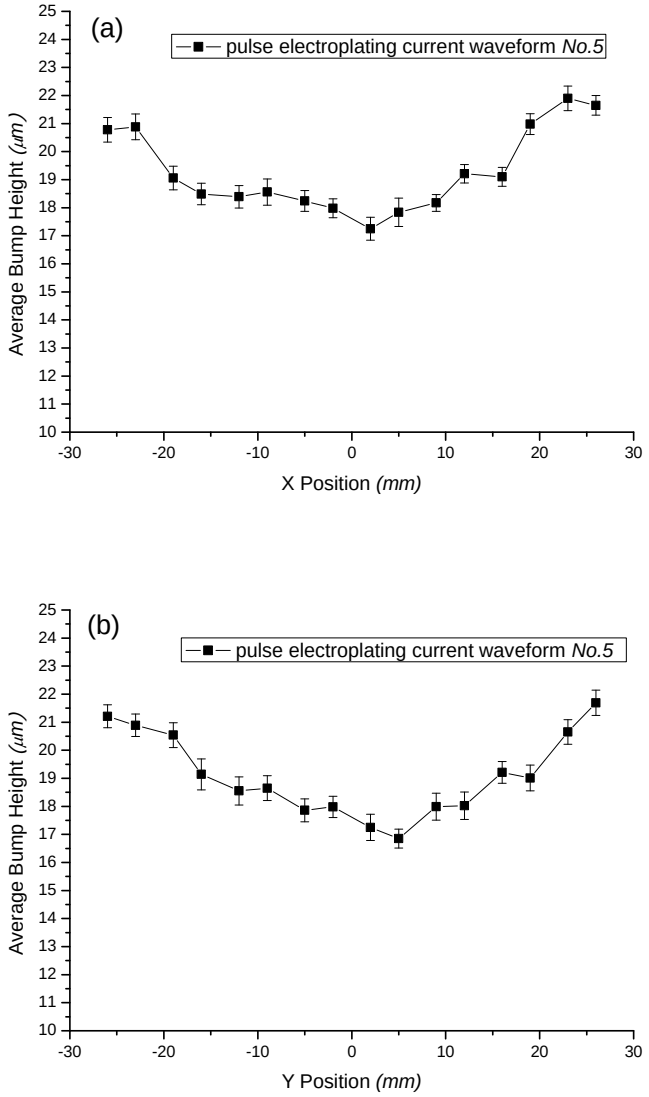


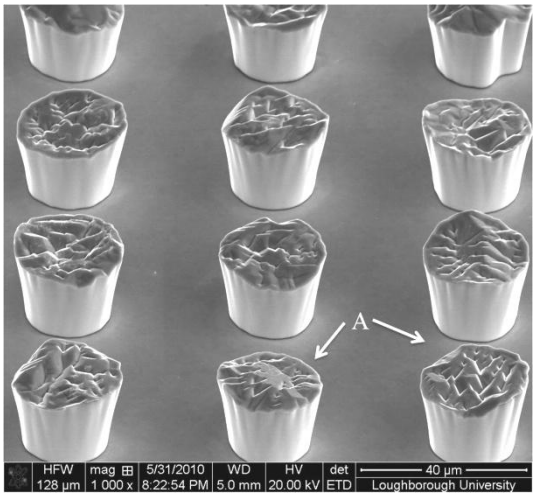
Figure 4-29 Height measurement of indium bumps obtained using pulse electroplating waveform *No. 5* on 3 inch wafer through: (a) X direction, and (b) Y direction.

Table 4-5 Uniformity of indium bumps deposited through various pulse electroplating waveforms on 3 inch wafers.

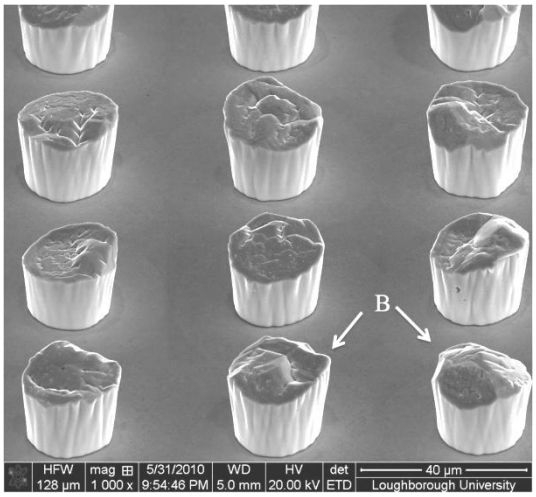
Waveform *No.*	**Bump Height Uniformity *(%)***	
	X Direction	*Y Direction*
3	10.41	10.09
4	12.37	12.99
5	12.58	13.16

4.3.3 Indium Bumping Through Pulse Reverse Electroplating

Pulse reverse electroplating on 3 inch wafers with a thief ring design was also carried out. As mentioned before, pulse electroplating waveform *No. 3* was performed for 5 minutes prior to the pulse reverse electroplating to avoid the contamination of the bath with copper ions. Thus, the pulse reverse electroplating bumping process was the combination of both waveforms. Indium bumps deposited through the pulse reverse electroplating waveforms are shown in Figure 4-30. From this, the edges of bumps do not appear noticeably higher than the centre in most cases. Instead, some of the bumps have an asymmetric flat top finish (see the arrows *A* in Figure 4-30), while some others even have a slightly protruding centre (see the arrows *B* in Figure 4-30). This obvious change of bump profile was confirmed by Zygo bump profiling shown in Figure 4-31. This may be explained as a result of the introduction of the anodic reverse cycle. As has been observed already, indium bumps deposited through DC and unipolar pulse current usually had concave bump finish which was caused by current crowding around the opening of the apertures where photoresist material played a part. However, in pulse reverse electroplating, the bump edge, *i.e.* the protruding sites at the feature scale, attracted a higher current density during the reverse anodic cycles resulting in a 'levelling' effect. Thus, the bump edge could not grow as high as in DC and unipolar pulse electroplating and the flattened bump top was observed. On the other hand, the current crowding effect may occur during the anodic cycles. Therefore, the bump edge was preferentially and heavily dissolved so that the bump centre was left higher than the edge.



(a) 20 *µm*, 50 *µm* pitch, through waveform *No. 6*.



(b) 20 *µm*, 50 *µm* pitch, through waveform *No. 7*.

Figure 4-30 Indium bumps electrodeposited using pulse reverse current waveforms *Nos. 6* and *7*.

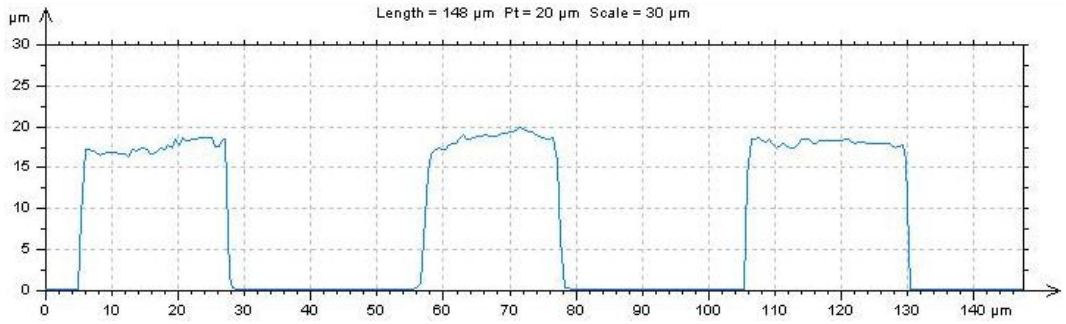


Figure 4-31 Profile of indium bumps electrodeposited using pulse reverse current waveform *No. 7*.

The bump height uniformity for waveform *No. 6* and *No. 7* are presented in Figure 4-32 and Figure 4-33, respectively. For waveform *No.6*, the height uniformity along the *X* direction was measured as 10.60% and the value along the *Y* direction was 11.26%. For waveform *No. 7*, the uniformity was measured as 11.82% and 11.35% along the *X* and *Y* directions respectively. It could be seen that the uniformity was not significantly changed by the bipolar pulse reverse current waveform in comparison with the unipolar pulse electroplating. However, a noticeable improvement was apparent compared with DC electroplating. A summary of the bump height uniformity measurements for pulse reverse electroplating is given in Table 4-6.

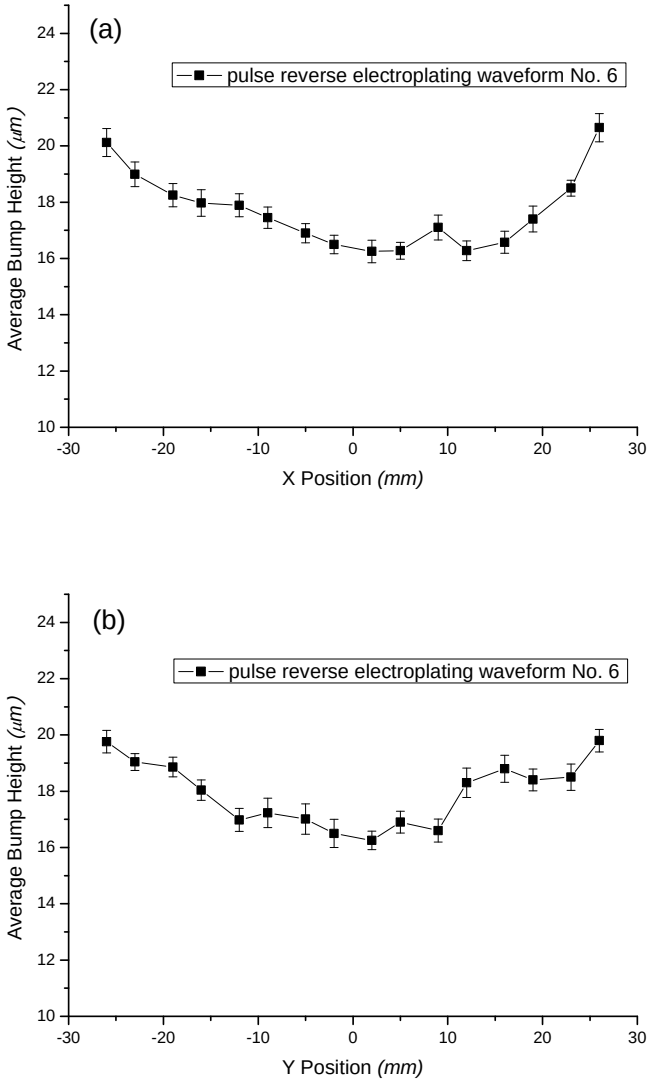


Figure 4-32 Height measurement of indium bumps obtained using pulse reverse electroplating waveform *No. 6* on 3 inch wafer through: (a) X direction, and (b) Y direction.

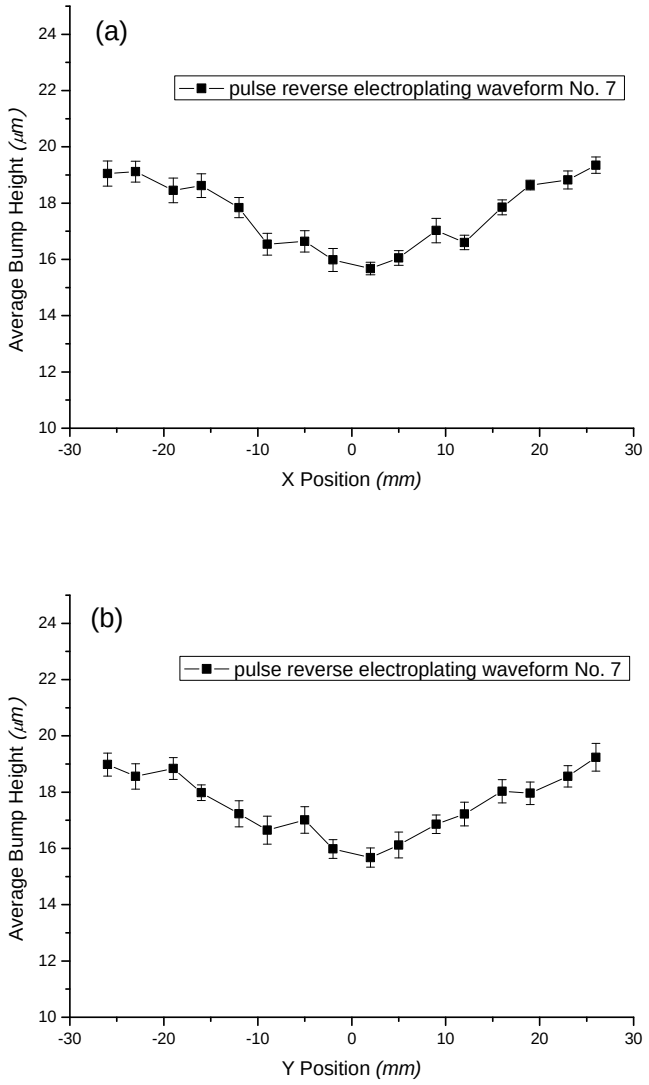


Figure 4-33 Height measurement of indium bumps obtained using pulse reverse electroplating waveform *No. 7* on 3 inch wafer through: (a) X direction, and (b) Y direction.

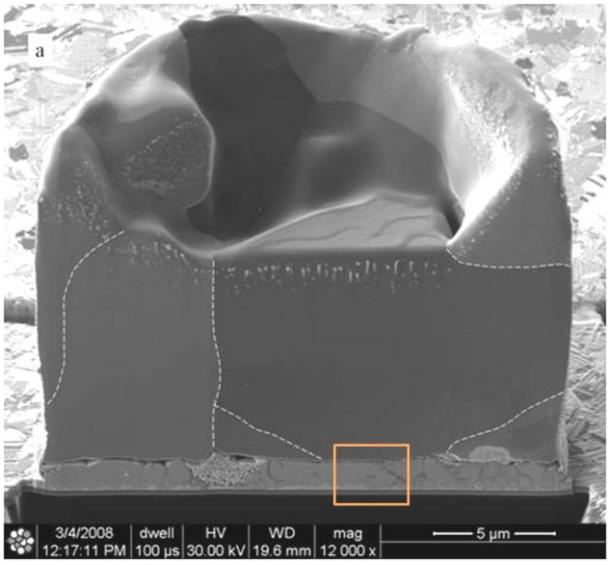
Table 4-6 Uniformity of indium bumps deposited through various pulse reverse electroplating waveforms on 3 inch wafers.

Waveform *No.*	**Bump Height Uniformity *(%)***	
	X Direction	*Y Direction*
6	10.6	11.26
7	11.82	11.35

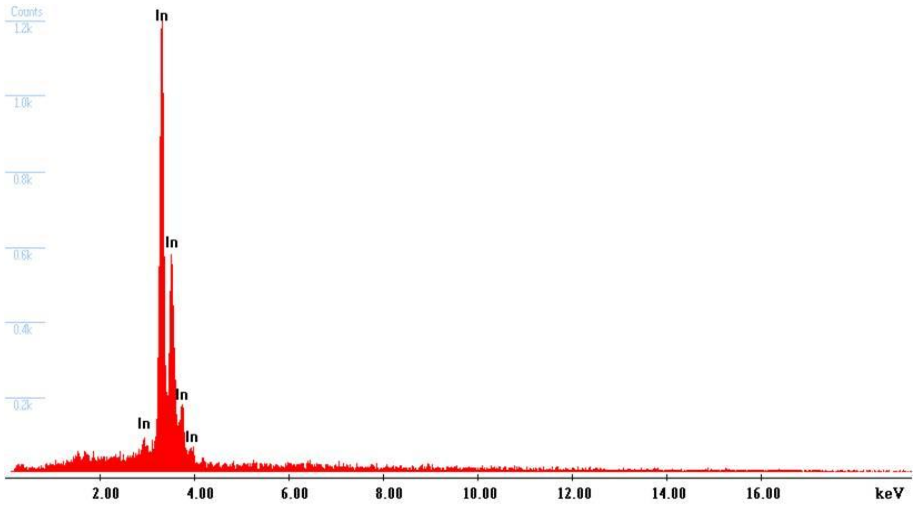
4.3.4 Microstructure Study

Cross-sectional views of electrodeposited indium bumps were prepared using Focused Ion Beam assisted SEM to analyse their microstructure. For DC electroplating at 10 mA/cm^2, as seen in Figure 4-34*a*, indium was continuously deposited on the exposed seed layer defined by the photoresist apertures and the main body of the indium bumps contained no defects. However, as commonly observed, there was a thin layer of material with a different morphology between the copper seed layer and indium bump (see the boxed area in Figure 4-34*a*). An EDX spectrum from this thin layer indicated that it only consists of indium (Figure 4-34*b*). It is therefore believed that this layer was formed at the beginning of indium deposition, and the formation of this layer will be discussed in Chapter 6. Grain size and orientation can also be studied by FIB as indicated in the contrast in the images between grains. Accordingly, it can be seen from the grains outlined by the dashed line, the grain size in the bump reached approximately 10 μm, which agrees with the earlier investigation of DC indium electroplating with a non-patterned substrate. The concave shape of the bump top profile is also seen from this cross-sectional view which is consistent with the profile shown in Figure 4-19.

Cross-sectional views of indium bumps deposited by pulse electroplating are also presented in Figure 4-35. In the FIB sample preparation process, a layer of platinum is usually deposited on the top of the bumps to protect the surface from damage caused by the applied ion beam, as indicated by the red line in this figure. The dotted lines were added to highlight the boundaries between different grain orientations. Although the top surface of pulse electroplated indium bumps had a conical morphology, which is similar to the results demonstrated in Chapter 3, only a small amount of grain refinement was observed from this cross-sectional view. Figure 4-36 shows the cross-section of an indium bump obtained through pulse reverse electroplating (waveform *No. 6*). In this case, the grain refinement is more obvious. In addition, the protruded bump centre is also observed due to the 'levelling' effect of the anodic cycle. However, it should be noted that not all of the bumps had this type of profile from pulse reverse electroplating.



(a) Cross-sectional view of indium bump electroplated with 10 mA/cm^2 DC.



(b) EDX spectrum collected from the initial thin layer at the interface.

Figure 4-34 Cross-sectional view of indium bump deposited with 10 mA/cm^2 DC electroplating and EDX analysis of the interlayer.

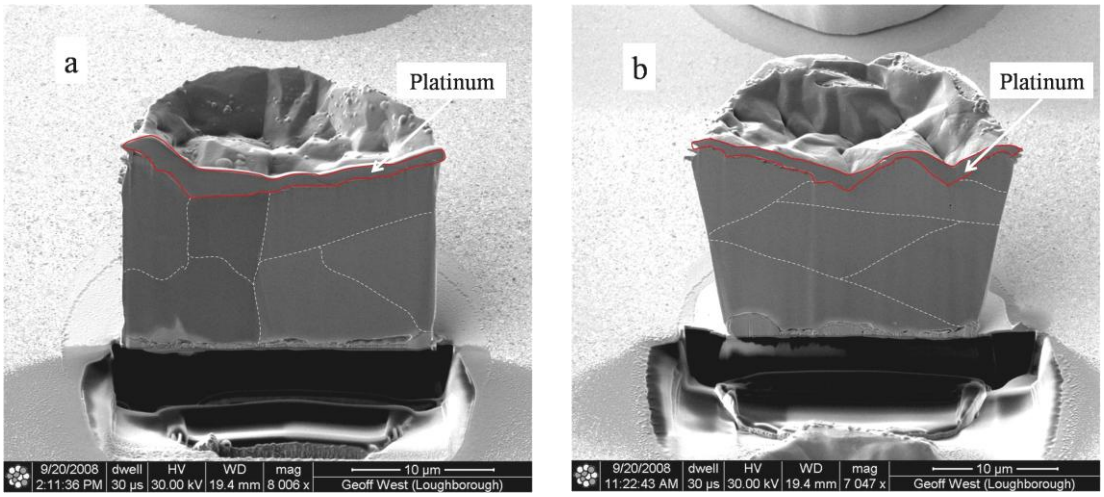


Figure 4-35 Cross-sectional view of indium bumps deposited using pulse electroplating waveforms: (a) waveform *No. 3*; (b) waveform *No. 5*.

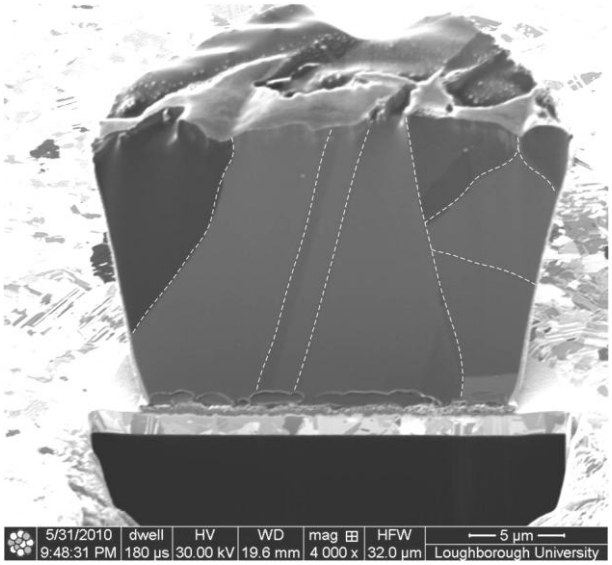


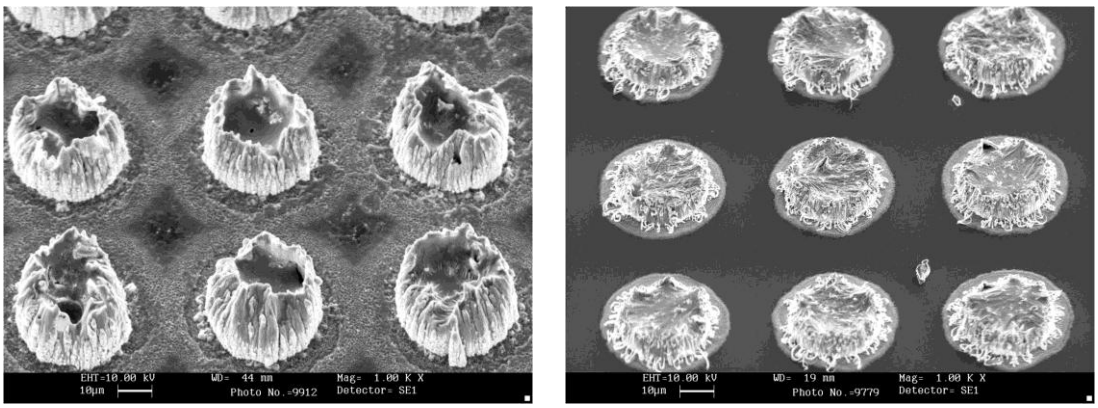
Figure 4-36 Cross-sectional view of indium bump deposited using pulse reverse current waveform *No. 6*.

4.3.5 Seed Layer Removal and Indium Bump Reflow

After electroplating, it is necessary to remove the seed layer and isolate the indium bumps for subsequent reflow to form spherical truncated bumps. As mentioned before, in this study, the copper seed layer was etched away, leaving the titanium layer as it was non-wettable during the bump reflow. For an actual application, the process needs to be re-designed and the titanium layer also needs to be removed before flip

chip assembly. Two methods were investigated for the removal of the copper seed layer: argon plasma and chemical etching.

Argon plasma etching was carried out using an Oxford Plasmalab 80 Plus etcher. A 300 *W* RF forward power was chosen and argon pressure was set at 0.05 *Torr*. As seen in Figure 4-37*a*, when the argon plasma was applied for 5 minutes, the copper layer was still present, but a large amount of indium from the bumps had been etched away. To completely remove the copper layer, the etching time was extended to 10 minutes. However, it was observed that indium bumps were damaged by the argon plasma (Figure 4-37*b*). Most of the indium was lost which was not desirable.

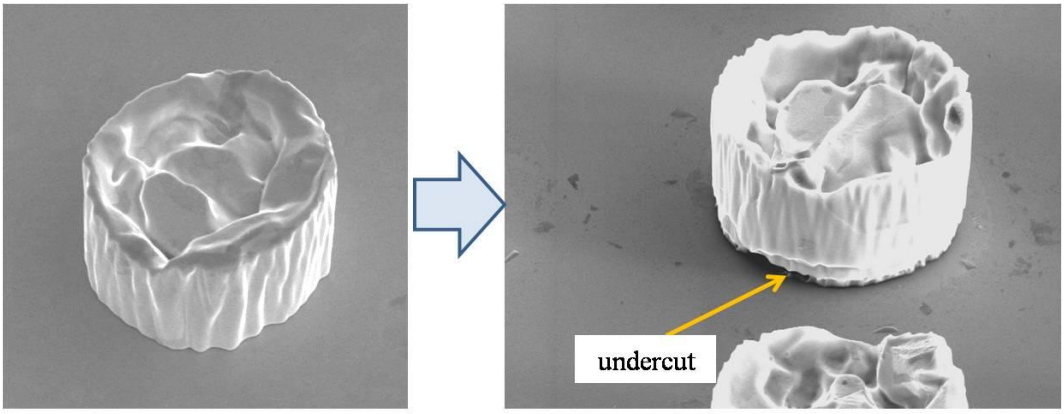


(a) 5 minutes etching *(b)* 10 minutes etching

Figure 4-37 Indium bumps damaged by argon plasma etching.

Thereafter, several chemical etching solutions were investigated to remove the copper seed layer in the presence of indium. According to the literature, cupric chloride based solution is commonly used for copper etching in PCB manufacturing, and an ammonium persulfate based solution has been successfully applied for copper etching with the presence of tin-lead solder bumps [2]. However, it was found that these two types of solution preferentially attacked the indium bumps which make them unsuitable for this application. Based on the electrochemical kinetics, indium will be attacked by most of the mineral acidic solutions, as such the successful etchant must be able to avoid preferential reaction with indium in order to retain an acceptable volume of the indium bump material after etching. Have modified several potential solutions, a solution of 23% nitric acid was found to be effective in removal of the copper seed layer without a significant loss from the indium bumps. Figure 4-38

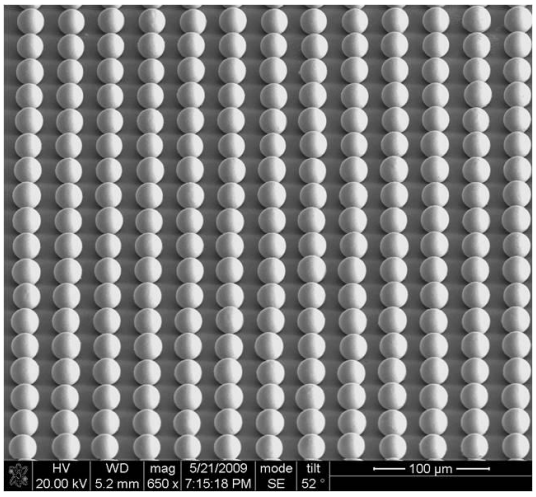
shows an indium bump after the copper seed layer was completely removed, with an acceptable undercut observed.



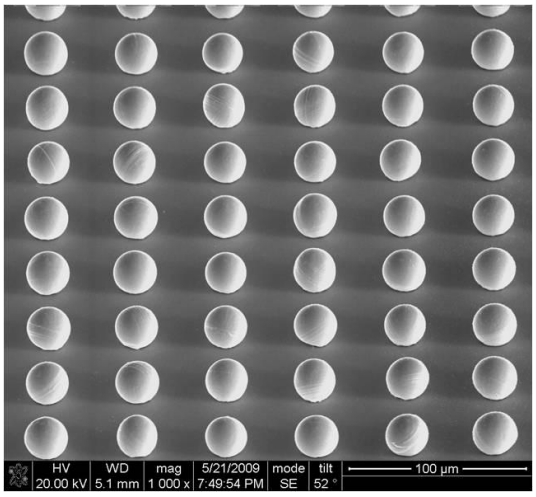
(a) Before etching *(b)* After etching

Figure 4-38 Indium bump before (a) and after (b) chemical etching of the copper seed layer.

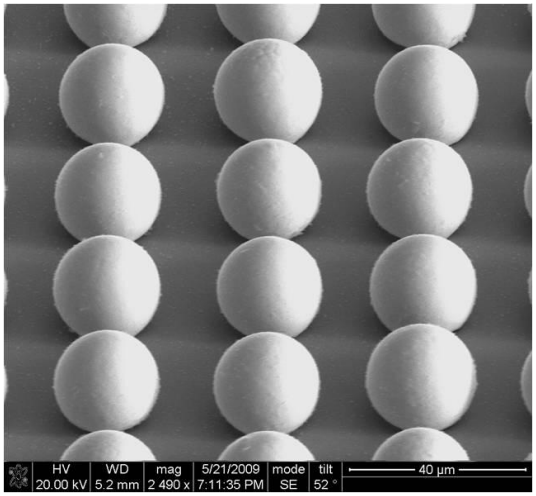
After the copper seed layer was removed, indium bumps were then reflowed through a temperature profile shown in Figure 4-14. The water soluble flux Hydrox-20 supplied by Henkel Technologies was employed and applied to protect the bumps from oxidation. Figure 4-39 demonstrates the spherical indium bumps obtained after reflow, which were formed due to the surface tension of liquid indium during the reflow process. The yield of indium bumps after reflow was strongly affected by the previous etching process. The reflow temperature profile and cleaning step could also influence the final yield. For this reason, the bump height uniformity was evaluated after electroplating rather than after reflow to avoid the influences of the immature seed layer etching process. In order to achieve a high yield, chemical etching, reflow and cleaning all needed to be carefully monitored. When using Hydrox-20 flux, a cleaning in water at 60~70 ^{o}C after reflow should be carried out immediately, otherwise, the residual contaminants left behind become very difficult to remove. As expected, the titanium layer performed very well as the non-wettable material during the reflow to enable the final formation of indium bumps.



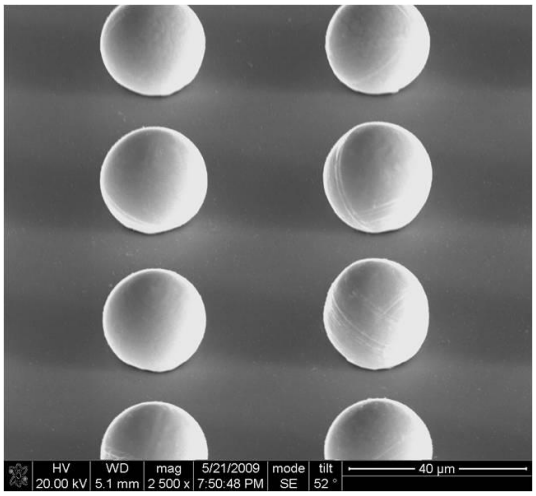
(a) Indium bumps with 20 μm diameter, 35 μm pitch.



(b) Indium bumps with 20 μm diameter, 50 μm pitch.



(c) Indium bumps with 20 μm diameter, 35 μm pitch (higher magnification).



(d) Indium bumps with 20 μm diameter, 50 μm pitch (higher magnification).

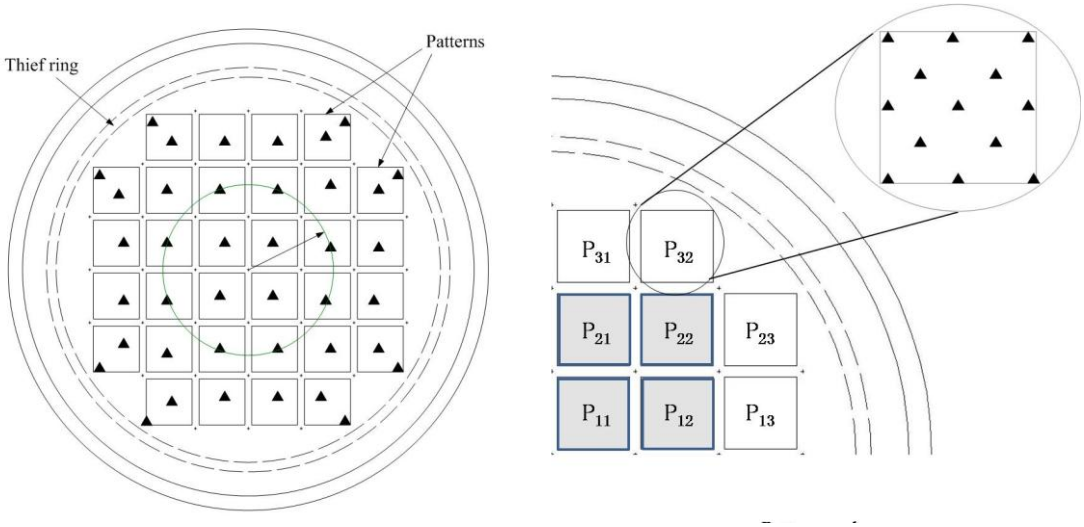
Figure 4-39 Spherical indium bumps formed on titanium substrate after reflowed in the air with assistance of Hydrox-20 flux.

4.4 Evaluation of Indium Bump Uniformity Using 4 Inch Wafers

As demonstrated above, ultra-fine pitch indium bumping through electrodeposition has been successfully developed on 3 inch test wafers. The results showed that the electroplating method was capable of generating high quality indium bumps with a high yield. However, to consider the application to larger size of wafers, the

feasibility study of such a bumping process at a larger scale, using an electroplating system (see Figure 4-8 and Figure 4-11) for evaluation of bump uniformity using standard 4 inch silicon wafer samples, was carried out. The uniformities at wafer and pattern scales were inspected under various electroplating current waveforms.

Using the wafer holder shown in Figure 4-11, the electrical contact was symmetrically arranged along the periphery of the wafer to be bumped (see Figure 4-9*b*). As such, the wafer scale bumping uniformity was evaluated in a different manner to that used for 3 inch wafers, *i.e.* according to the distance of patterns from the centre of the wafer (Figure 4-40*a*). The black triangles marked in Figure 4-40*a* indicate the measuring area and the bump heights obtained from patterns with same radius from the wafer centre were averaged. The uniformity within each pattern was measured according to the distance from the centre of the pattern. The uniformity within different patterns at different distances from the wafer centre was also compared. Because the wafer was circularly symmetric, the uniformity at the pattern scale was measured based on the same quarter of each wafer, with the patterns indexed as shown in Figure 4-40*b*. It should be noted that, when the uniformity at wafer scale is demonstrated, the uniformity at pattern scale has to be ignored. In other words, the non-uniformity at the pattern scale will not be considered in the evaluation of the uniformity at wafer scale.



(a) Wafer scale *(b)* Pattern scale

Figure 4-40 Methodology of evaluation of indium bump uniformity on 4 inch wafer at: (a) wafer scale; (b) pattern scale.

4.4.1 Bump Uniformity by DC Electroplating

Based on the results of bump evaluation with 3 inch glass wafers, the electroplating bumping should be carried out at a lower current density in order to achieve a higher uniformity of electroplated bumps. Therefore, to ensure a high indium bumping uniformity on 4 inch wafer samples, the DC electroplating was only conducted at 10 mA/cm^2. In order to evaluate the influences of the current thief ring, the DC electroplating was performed using 4 inch wafers with and without the thief ring design for which the layout of patterns were defined by masks *No. 1* and *No. 5* in Table 4-2 (also see Appendix 2).

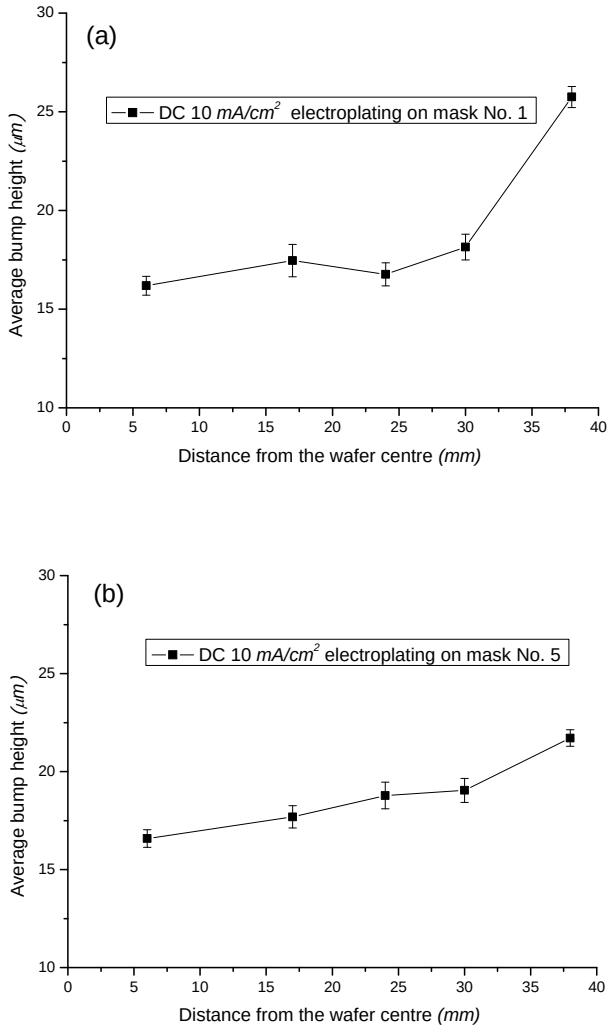


Figure 4-41 Height uniformity of indium bumps at 4 inch wafer scale with different patterns electroplated through DC 10 mA/cm^2 using sulphamate solution: (a) photomask *No. 1* without thief ring design; (b) photomask *No. 5* with thief ring design.

In the case of DC electroplating without a thief ring, the bump uniformity at the 4 inch wafer scale was measured as 28.29%, as shown in Figure 4-41*a*. The electroplated indium bumps also appeared non-uniform at the pattern scale. The measured uniformity within the pattern P_{11} (see Figure 4-40) was 18.12%, as shown in Figure 4-42*a*, which shows the averaged bump height versus distance to the pattern corner by plotting the data across the diagonal line, *i.e.* the longest distance within the pattern. Figure 4-42*b* demonstrates the uniformity at the pattern scale from a quarter of test wafer. From the results, it appears that the closer the pattern is to the electrical contact points, the worse the uniformity is. It was noticed that the pattern centre had the lowest bump height while the highest ones were located at the corner. As shown in Figure 4-43, the bumps near the corner of the pattern were usually over-electroplated in morphology like a 'mushroom' while the bumps at the centre still maintained a column shape. The worst case occurred at the corner of patterns which had the shortest distance to the electrical contact.

In comparison, as shown in Figure 4-41*b*, with the presence of a current thief ring, the uniformity at the wafer scale was reduced to 19.65%. The bump height distribution at the pattern scale did not appear to show any changes compared to Figure 4-42*a*, *i.e.* the corner of the pattern also attracted a high current density and therefore had taller bumps. However, due to the 'levelling' effect caused by the current thief, the overall uniformity at the pattern scale was improved, as shown in Figure 4-44.

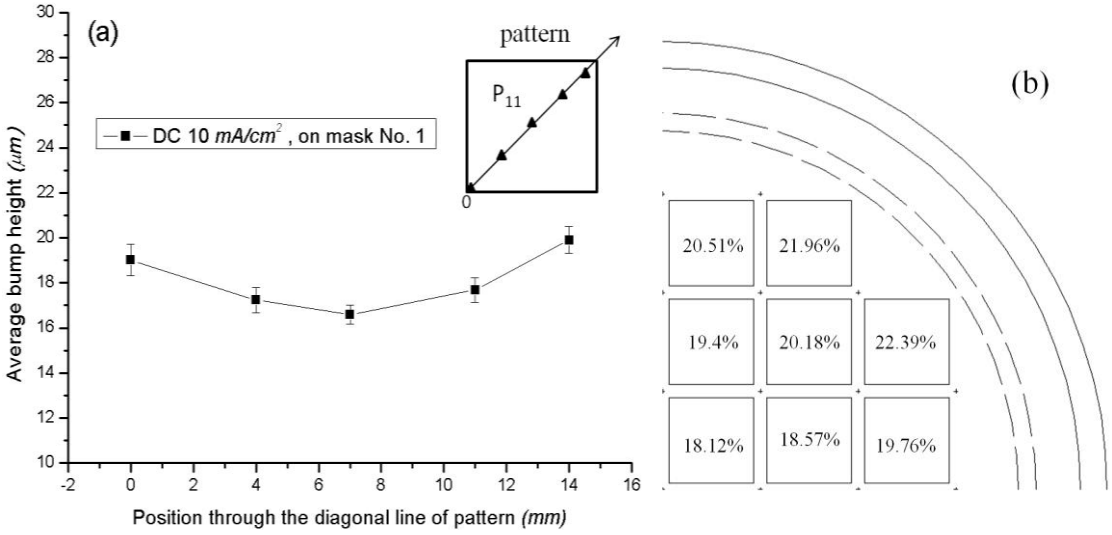


Figure 4-42 The pattern scale uniformity of indium bumps electroplated through DC at 10 *mA/cm*^{2} on 4 inch wafer without thief ring: (a) bump uniformity within pattern P11; (b) pattern scale uniformities distribution in a quarter of wafer.

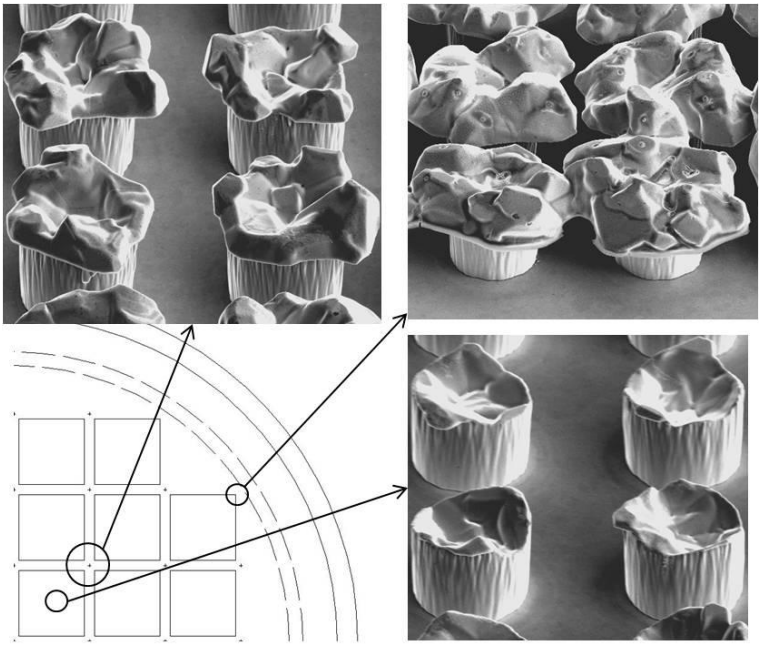
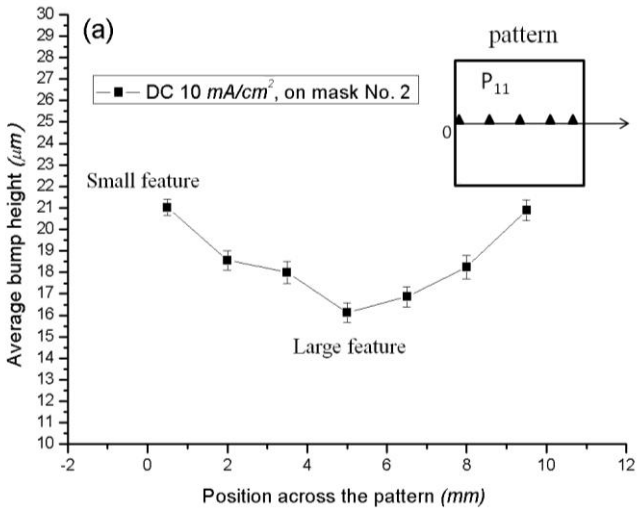


Figure 4-43 Morphology change of DC (10 *mA/cm*^{2}) electroplated indium bumps from different patterns selected from a quarter of the 4 inch wafer pattern without thief ring design.

Figure 4-44 Pattern scale uniformity distribution of DC(10 *mA/cm*^{2}) electroplated indium bumps on a quarter of the 4 inch wafer pattern with a thief ring design.

4.4.2 Influences of Feature and Pitch Size on Indium Bump Uniformity at the Pattern Scale

In order to investigate the influences of feature size on the uniformity at the pattern scale, a series of experiments were carried out using the patterns designed with various feature and pitch sizes. As can be seen in Appendix 2, the feature size in the patterns defined by mask *No. 2* increased from 15 *μm* (near the edge of the pattern) to 25 *μm* (near the centre of the pattern) while the pitch size was double of the corresponding feature size. The patterns defined by mask *No. 3* had inverse layout, *i.e.* the centre of the pattern was populated with the smallest features.



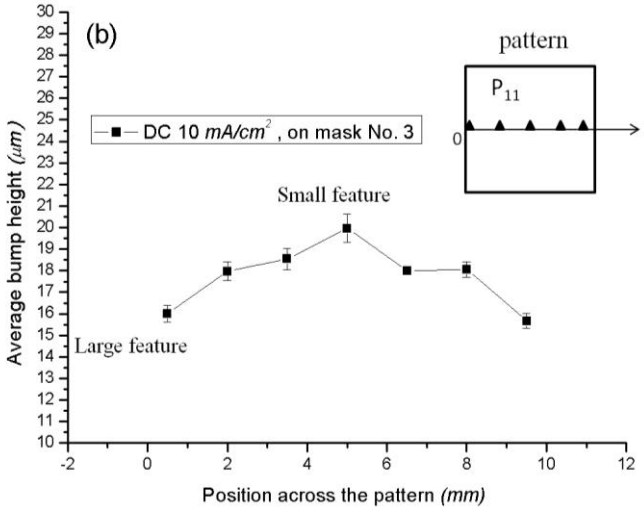


Figure 4-45 The uniformity of DC (10 *mA/cm*^{2}) electroplated indium bumps at the pattern scale measured on 4 inch wafers for the patterns defined by: (a) masks *No. 2* and (b) *No. 3*.

It was found that the uniformity within the pattern P_{11} defined by mask *No. 2* was 26.32% (see Figure 4-45*a*) which deteriorated in comparison with the DC electroplating using mask *No. 5*. In contrast, the uniformity within the pattern P_{11} defined by mask *No. 3* was 16.2% , but in reverse profile (Figure 4-45*b*). Using mask *No.2*, the smallest bumps were located along the periphery of the pattern having the largest bump height, and the non-uniformity was increased by using such an arrangement. With mask *No. 3*, the highest bumps were located at the centre of the patterns despite the fact that the current crowding was expected near the edge of the pattern. This phenomenon indicated that the smaller feature can induce a higher current density and therefore resulting in a higher bump no matter where it is located. This finding can guide an industrial practice in arranging different sized features within a pattern, for instance, smaller features should not be too close to the pattern boundary.

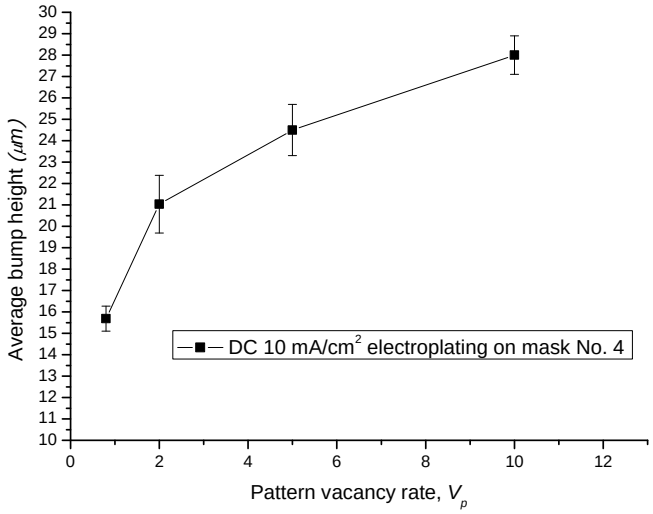


Figure 4-46 Non-uniformity of the DC (10 *mA/cm*^{2}) electroplated indium bumps within pattern P_{11} in mask *No. 4* caused by the bump vacancy rate.

In the patterns defined by mask *No. 4*, all the features had the same diameter but different pitch size. The distances between two features were designed as 0.8, 2, 5 and 10 times the feature diameter. This was used to investigate how the pattern density affects the bumping uniformity. Here, for the convenience of expression, a factor of pattern vacancy rate (V_p) is defined as:

$$V_p = \frac{Distance\ between\ two\ \ features}{Feature\ diameter} \tag{4-2}$$

When V_p is 0, this represents an electroplating onto a non-pattern substrate. Figure 4-46 plots the average height of indium bumps having different pitch sizes within pattern P_{11} defined by mask *No. 4*, for which the uniformity was measured as 27.62%. The uniformity also deteriorated when the pattern was located near the edge of wafer. Thus, significant change of pitch size within a pattern can be an adverse factor in determining the uniformity on the pattern scale.

4.4.3 Uniformity of Pulse Electroplated Indium Bumps

The influences of pulse electroplating on bumping uniformity were also evaluated using current waveform *No. 3, 4* and *5* in Table 4-3. All the wafer samples were prepared using mask *No. 5*, *i.e.* a homogenous pattern with thief ring. The uniformity

at the wafer scale and pattern scale corresponding to the three types of pulse electroplating current waveforms are plotted in Figure 4-47. The uniformity at the wafer scale for current waveforms *No. 3*, *4* and *5* were 14.3%, 15.2% and 14.96% respectively, which were considerably improved in comparison with DC electroplating. It was also found that the uniformity within the inner patterns (shaded patterns in Figure 4-40) was significantly improved by using unipolar pulse current, indicating the influence of pulse electroplating on uniformity at the pattern scale is more pronounced than that on uniformity at the wafer scale.

4.4.4 Uniformity of Pulse Reverse Electroplated Indium Bumps

Pulse reverse electroplating on 4 inch wafers was also carried out following a short period of unipolar pulse electroplating to minimise the risk of prior contamination to the solution. As can be seen in Figure 4-48, the uniformity at the wafer scale for the pulse reverse current waveforms *No. 6* and *No. 7* were measured as 13.6% and 14.07% respectively. Figure 4-48 also shows the uniformity at the pattern scale on the 4 inch wafer. By using pulse reverse electroplating, the uniformity at the wafer scale and pattern scale were much improved in comparison to DC electroplating. However, little difference was found between the unipolar pulse electroplating and bipolar pulse reverse electroplating in terms of the bumping uniformity at different scales.

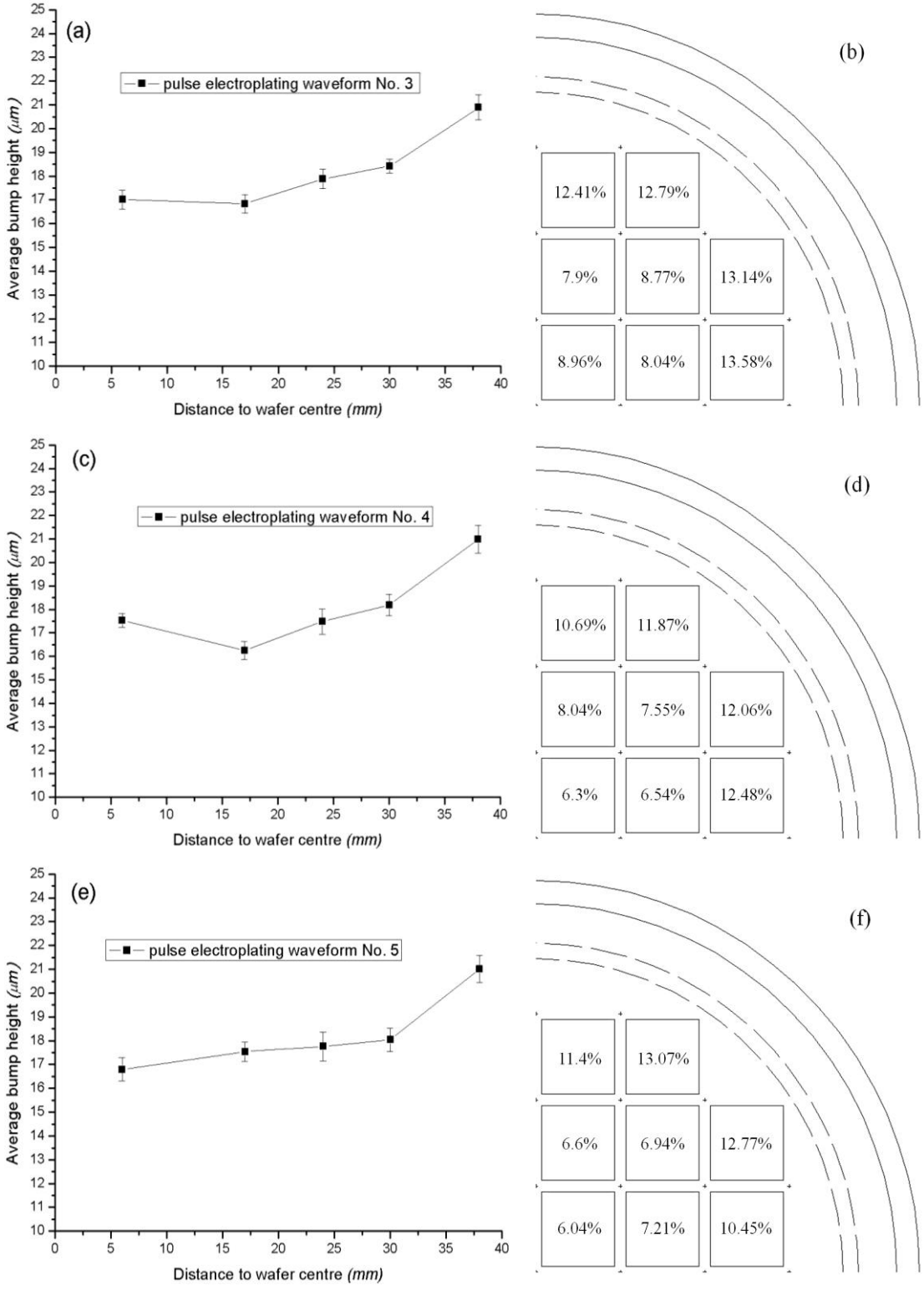


Figure 4-47 Uniformity measurement of pulse electroplated indium bumps on 4 inch wafers at wafer and pattern scale under the various pulse electroplating waveforms: (*a*) pulse current waveform *No. 3*, wafer scale; (*b*) pulse current waveform *No. 3*, pattern scale uniformity distribution in a quarter of wafer; (*c*) pulse current waveform *No. 4*, wafer scale; (*d*) pulse current waveform *No. 4*, pattern scale uniformity distribution in a quarter of wafer; (*e*) pulse current waveform *No. 5*, wafer scale; and (*f*) pulse current waveform *No. 5*, pattern scale uniformity distribution in a quarter of wafer.

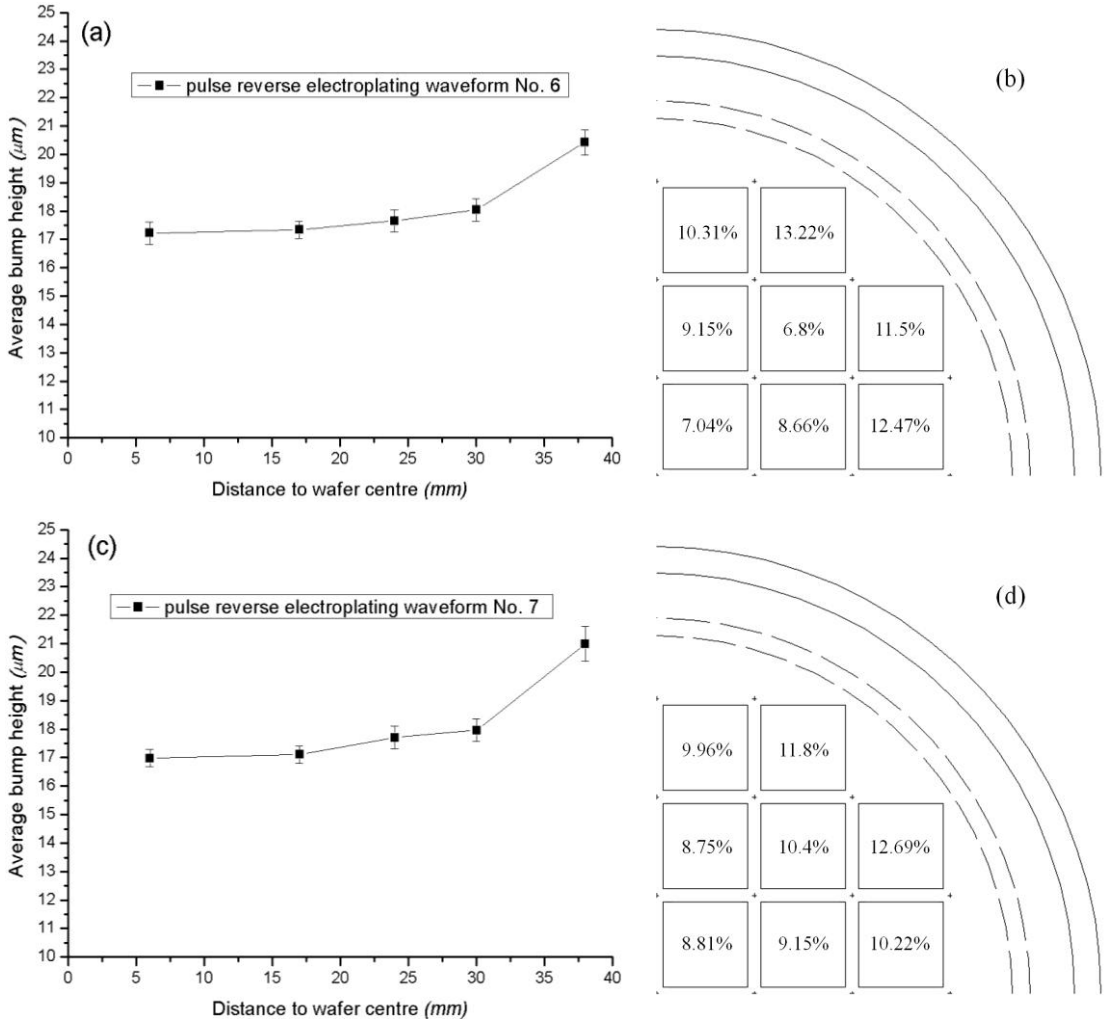


Figure 4-48 Uniformity measurement of pulse reverse electroplated indium bumps on 4 inch wafers at wafer and pattern scale of various current waveforms: (*a*) pulse reverse current waveform *No. 6*, wafer scale; (*b*) pulse reverse current waveform *No. 6*, pattern scale uniformity distribution in a quarter of wafer; (*c*) pulse reverse current waveform *No. 7*, wafer scale; and (*d*) pulse current waveform *No. 7*, pattern scale uniformity distribution in a quarter of wafer.

4.5 Summary

As illustrated above, ultrafine pitch indium bumping through electrodeposition has been successfully established. Indium bump deposition through DC electroplating, unipolar pulse electroplating and bipolar pulse reverse electroplating has been carried out. The influences of pulsating current waveforms on indium bump morphology, microstructure and bump height uniformity have been investigated through extensive

experiments. Based on the experimental results, the following conclusions can be drawn at this stage.

- The experimental results have shown that the electroplating approach is capable of realising ultrafine pitch indium bumping with high yield.
- The pre-wetting step is essential to achieve a high yield for which ultrasonic agitation has been proved as an effective way to fulfil the requirement.
- The methodology of the electrical contact can significantly affect the bump uniformity across the wafer. An asymmetrically distributed electrical contact can induce directional non-uniformity.
- The current thief ring design has been proved as an effective way to improve the bump height uniformity. Especially, it can provide an electrical path around the patterns and is able to homogenise the directional non-uniformity in the case of electroplating onto a 3 inch test wafer when the electrical contact is made asymmetrically.
- The results from DC electroplating indicated that the wafer and pattern scale bump height uniformities deteriorated when the current density increased.
- By using unipolar pulse electroplating, the indium bump uniformity on both wafer and pattern scales can be significantly improved. The best uniformity on a 4 inch wafer through pulse electroplating was 14.3%.
- Pulse reverse electroplating can also significantly improve the bump uniformity on both the wafer and pattern scale in comparison to DC electroplating, but at the equivalent level with pulse electroplating. The best uniformity obtained through pulse reverse electroplating on a 4 inch wafer was 13.6%.
- In the case of DC electroplating, the indium bumps have a concave shape where the bump edge is much higher than the centre. The growth front of the indium bumps is more even in the case of pulse electroplating in comparison to DC electroplating. By using the pulse reverse electroplating, the feature scale uniformity can be significantly improved that it is able to obtain indium bump with protruded centre.

- The microstructure studies showed that there were no defects in the main body of indium bumps through all of the electroplating conditions. In the case of pulse and pulse reverse electroplating bumping, grain refinement was observed to some extent in comparison to DC electroplating, which is in agreement with the earlier results of indium deposition onto non-patterned substrates.

Chapter 5 Effects of Acoustic Agitation on Indium Bump Formation

5.1 Introduction

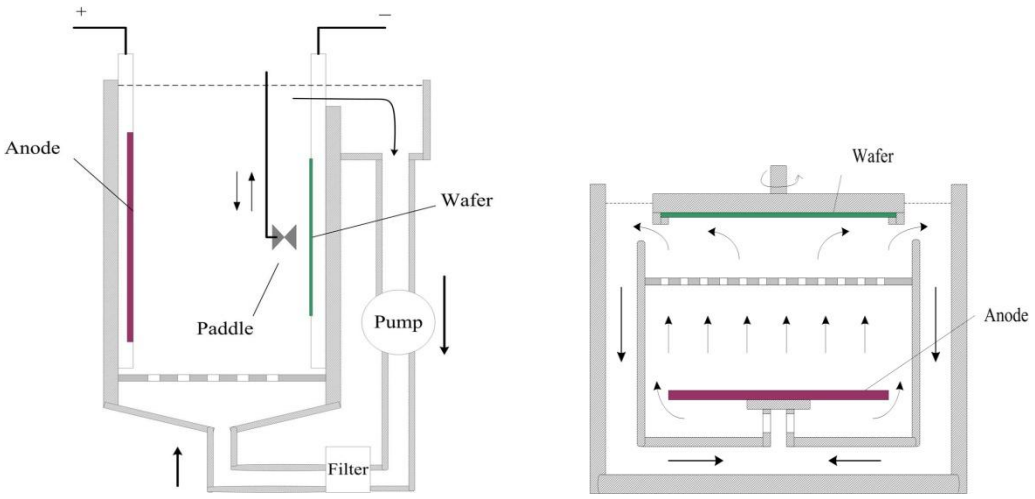
This chapter presents the results of an evaluation of the use of acoustic agitation to improve mass transport during the electrodeposition of indium bumps. Acoustic agitation with different frequency and power were employed in indium electroplating onto both plain and patterned substrates and the influences of the configuration of the electroplating system, acoustic frequency and power were investigated.

5.1.1 Agitation Methods Used in Electroplating Bumping Processes

As mentioned before, mass transport plays a significant role during electroplating. On the one hand, mass transport determines the limiting current density for a given electrolyte and therefore the electrodeposition rate and efficiency which are sometimes crucial to the manufacturing output and investment cost. On the other hand, the mass transport condition often affects the microscopic characteristics of the deposits. In the electroplating bumping process, mass transport determines the bump shape, microstructure and when an alloy deposit is demanded, composition. More importantly, the uniformity of the mass transport condition across the wafer, *i.e.* the homogeneity of the diffusion boundary layer on the wafer scale, can strongly affect the bump uniformity. Therefore, to achieve the desired mass transport condition, additional agitation is usually taken into account in designing the electroplating system.

Currently, two types of electroplating system with different agitation methods are popularly employed for microelectronic fabrication: paddle electroplating bath and fountain electroplating cell. The paddle electroplating bath was initially developed for electroplating of thin film recording heads [113]. The typical structure of the paddle electroplating cell is shown in Figure 5-1*a*. Both the anode and cathode (wafer) can be positioned horizontally or vertically. Typically, the paddle consists of two triangle bars facing against each other with a small gap between them. The paddle is normally positioned very close to the cathode surface and travels back and forth in front of the cathode to reduce the gradient of reactant species in the diffusion boundary layer during the electrodeposition process. This type of electroplating cell has been widely adopted in the fabrication of oriented magnetic heads [114-118] and the paddle electroplating cell has also been employed in Pb/Sn and lead-free solder bump deposition for flip chip assembly [27, 76].

The schematic structure of the fountain type electroplating cell is shown in Figure 5-1*b*. The anode is usually immersed into the bottom of the tank while the wafer is held by a fixture facing down over the electrolyte. The electrolyte is pumped from the bottom of the tank resulting in the flow of the liquid through a distributor impinging on the cathode surface to improve the mass transport and sufficiently replenish the reactant species. The cathode is usually rotated at high speed at the same time to make the diffusion boundary layer more evenly distributed across the wafer.



(a) Paddle electroplating cell *(b)* Fountain electroplating cell

Figure 5-1 Schematic configuration of the paddle and fountain electroplating cells.

The paddle agitation process has been matured for many years and is cost-effective to incorporate into the electroplating system. However, the paddle can only oscillate at low frequency (typically around 10 *Hz*) due to the limit of the mechanical movement. Thus, the diffusion boundary layer can only be reduced to a relatively small extent. In a study conducted by Wu [119], in a simple copper sulphate electroplating bath with commercial paddle, the diffusion boundary layer across a blanket wafer was reduced from ~60 μm to ~10 μm when the paddle was oscillating at 10 *Hz*. Moreover, the efficiency of the paddle agitation is compromised by the photoresist pattern. According to Wu's study, the diffusion boundary layer was limited at ~20 μm when the wafer was covered by a photoresist pattern with 50 μm thickness and 130 μm diameter opening. Therefore, with paddle agitation, the diffusion boundary layer would be expected to be of the same order as the pattern size in this research.

The fountain electroplating cell has been extensively employed in wafer metallisation such as Damascene electroplating and solder bump deposition [120-123]. Such a electroplating cell can be integrated into a high level automated processing line. The diffusion boundary layer and therefore limiting current density are related to the local velocity of the solution on the wafer surface. In the case of a blanket wafer, *e.g.* copper Damascene electroplating for wiring, a uniform diffusion boundary layer across the wafer can be achieved through high speed rotation. However, in the case of electroplating through the mask, *e.g.* solder bump deposition, the local diffusion boundary layer varies from the centre to the edge of the wafer because of the presence of the photoresist [2].

As discussed above, the conventional paddle and fountain agitation approaches are restricted by their indigenous drawbacks, especially in the case of electroplating through ultrafine pitch photoresist patterns. Therefore, development of a new method is still desirable to fulfil the demand of high uniformity of ultrafine pitch bumping.

5.1.2 Fundamentals of Acoustic Agitation

Conventionally, sound waves having frequency beyond human hearing (> 20 *kHz*) are called ultrasound. Those below 100 *kHz* are called power ultrasound which has been commonly employed in welding, surface treatment, cleaning, cutting, drilling, non-

destructive detection, synthesis and electrochemical fabrication [124]. Sonochemistry has been derived as a division of chemistry representing the chemical applications assisted by ultrasound. In recent years, with the development of the very high frequency acoustic apparatus for the cleaning of semiconductor components and diagnostic equipment for medical use, the term megasound representing the sound waves in the megahertz (*MHz*) range has been widely adopted [125-130].

Acoustic agitation is the method of using high frequency sound waves (typically ranging from 20 *kHz* to 2 *MHz*) to alter the mass transport condition in chemical or electrochemical applications. It has been found that the mechanisms of how the sound waves improve the mass transport are dependent on the frequency. Thus, acoustic agitation can be categorised into ultrasonic agitation, for the application using ultrasound in the kHz range, and megasonic agitation which is for the application of megasound over 1 *MHz* frequency.

When ultrasonic energy is applied into a solution, like any sound waves, ultrasound is transmitted through the liquid via a series of compression and rarefaction waves induced in the molecules of the solution. If the sound is powerful enough, the rarefaction cycle may exceed the attractive forces of the molecules of the liquid and thus cavitation bubbles will form. Once the bubbles are formed, the bubbles will be expanded in ensuing rarefaction cycles while being compressed during compression cycles. This process is known as rectified diffusion which features that a small amount of vapour or gas from the liquid enters the bubble during its expansion phase and is not expelled thoroughly during compression. Thus, the bubbles grow over successive cycles to an equilibrium size defined by the particular frequency and power applied. Once the size of the bubbles reach a critical value in a given condition, the bubbles will collapse in succeeding compression cycles and generate energy for chemical and mechanical effects (Figure 5-2). The collapse of the cavitation bubbles is a remarkable phenomenon induced by the power of ultrasound, for example, in aqueous systems with 20 *kHz* ultrasound, each cavitation bubble collapses with a temperature of about 5000 ^{o}C and pressure in excess of 2000 atmospheres [131].

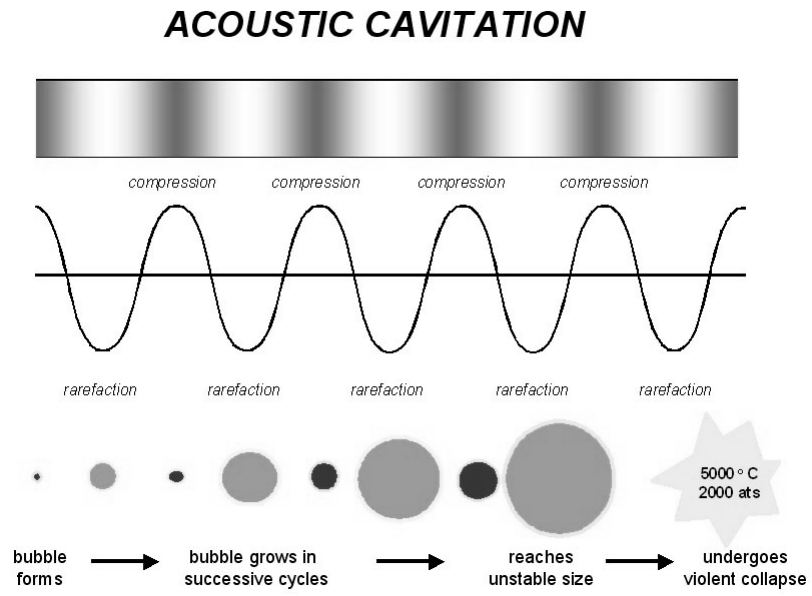


Figure 5-2 Generation of an acoustic bubble [131]. (Courtesy of Prof. T. J. Mason, Coventry University, reprinted with permission)

If the cavitation bubbles are formed and collapse in the bulk liquid, the collapse of the bubbles will generate shear forces which could produce mechanical effects and the bubble itself will be subjected to extreme conditions of temperature and pressure leading to chemical effects. However, when the collapse occurs on or near a heterogeneous solid/liquid interface, the result will be a powerful micro liquid jet impinging upon the surface (Figure 5-3). This effect is the reason why ultrasound is used for surface cleaning and other electrochemical applications.

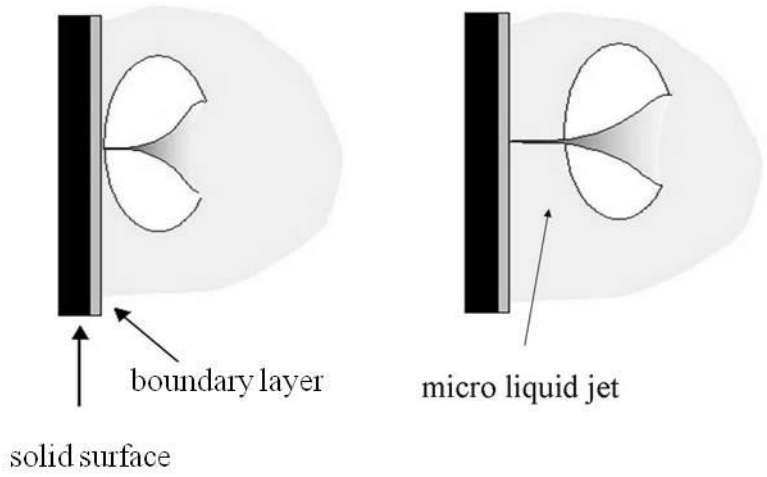
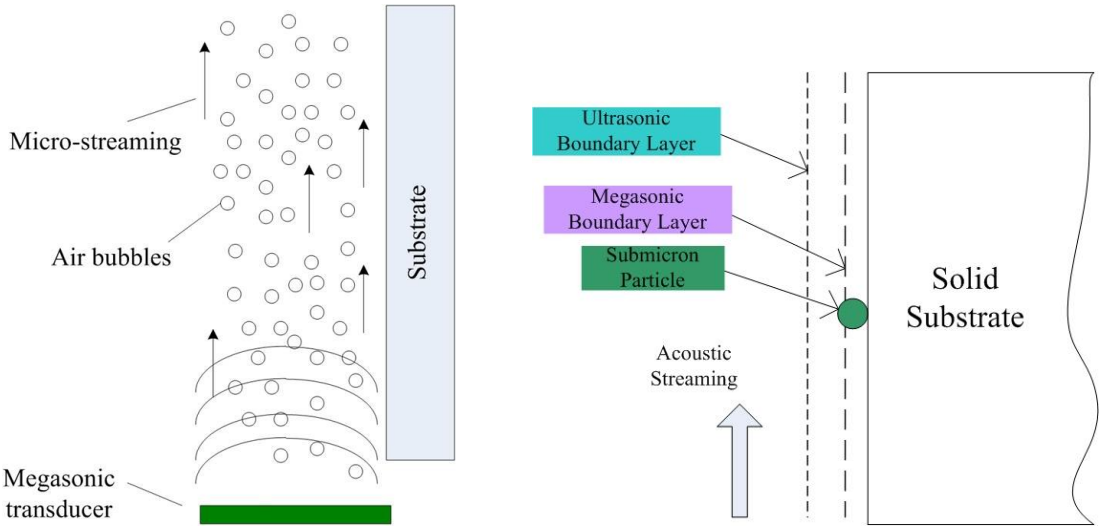


Figure 5-3 Cavitation bubble collapse at or near a solid surface [131]. (Courtesy of Prof. T. J. Mason, Coventry University, reprinted with permission)

In general, ultrasonic cavitation effects prevail when the frequency is below 500 kHz, while another phenomenon named acoustic streaming dominate at higher frequency up to the megahertz range. Because the threshold of the cavitation bubble formation and collapse increases exponentially with the acoustic frequency, it needs much higher power to maintain acoustic cavitation under higher frequency [124]. When it comes to the megahertz range, where the term of megasonic agitation is adopted, the rarefaction may not be able to overcome the molecular attractive forces so that the probability of forming cavitation bubbles becomes much lower than for ultrasonic agitation. Also, for any pre-existing air bubbles in the liquid, the surrounding liquid will be rapidly oscillated in a stable pattern and the pre-existing bubbles will be unlikely to grow over the megasound cycles. If the oscillation occurs on or close to an asymmetrical liquid-solid boundary, there will be shear force applied to the liquid molecules along the boundary rather than the powerful liquid micro-jet caused by the cavitation bubble collapse. Therefore, the liquid is impelled by the shear force following the direction of the megasonic wave propagating across the surface (Figure 5-4*a*).

It is known that, when the liquid flows along the solid substrate, on a microscopic scale, the fluid friction at the surface causes a very thin boundary layer of solution moving more slowly than the bulk liquid. In the application of cleaning, this boundary layer effectively shields the substrate surface from fresh chemistry and shields contaminants from the removal forces of the bulk fluid. In the case of electrodeposition, this boundary layer effectively shields the reactive ion replenishment from the bulk solution. Within this layer, no matter how rigorous the convection in the bulk liquid is, the mass transport is controlled by the diffusion condition. In general, the boundary layer is represented by the so-called Nernst diffusion layer for which the concentration gradient is proportional to the distance from the solid surface.



(a) Acoustic streaming

(b) Reduced boundary layer by acoustic agitation

Figure 5-4 Schematic of acoustic streaming effect and reduced boundary layer by acoustic agitation.

In theory, when acoustic agitation is applied to an electrolyte, the thickness of the Nernst diffusion layer near the electrode surface is estimated as:

$$\delta = \sqrt{\frac{2\nu}{\omega}} \tag{5-1}$$

where ν is the viscosity of the liquid and ω depends on the acoustic frequency f as $\omega = 2\pi f$: the higher the frequency, the thinner the diffusion layer will be [132]. Combined with experimental investigation and numerical calculation, taking the water as the solution for example, the thickness of δ at 1 *MHz* is evaluated to be around 0.6 μm, which is much smaller than in the ultrasonic condition (*e.g.* when f = 40 *kHz*, $\delta \approx 3.8\mu m$) [132, 133]. Thus, the diffusion boundary layer near the substrate is significantly reduced, even down to the submicron scale (Figure 5-4*b*).

5.1.3 Applications of Acoustic Agitation

Applying ultrasonic agitation into electrochemical processes has been found to improve the mass transport due to the liquid micro-jet caused by the cavitation bubbles, decreasing the thickness of the diffusion layer and thus assisting the electrode reactions. Some of the particular advantages which accrue from the use of

ultrasound in electrochemistry include degassing at the electrode surface, disruption of the diffusion layer which therefore reduces depletion of electro-active species, improved mass transport of ions across the diffusion layer, and continuous cleaning and activation of the electrode surfaces [124]. In particular, for electrodeposition and electroless plating in the presence of ultrasound, the literature contains many articles demonstrating the advantages of ultrasound in electrodeposition which include increased hardness, increased coating thickness, increased reaction efficiency and deposition rates, use of less toxic electroplating solutions, greater adhesion and minimisation of levellers, brighteners or other additives [134-139].

By virtue of the significantly reduced boundary layer, megasonic agitation has been widely utilised for cleaning in semiconductor industry applications, especially for removing submicron sized particles [125-129, 140]. Moreover, due to the significant improvement of mass transport, introducing megasonic agitation into the LIGA process results in faster development rate, more uniform and high aspect ratio microstructures, even nanostructures [133, 141].

For electroplating applications, megasonic agitation is a relatively new technology for improving mass transport which became noteworthy in recent years. The first study of megasonic agitation assisted electroplating was for copper Damascene electroplating into nano-meter sized trenches. It was found that, by using megasonic agitation, it was possible to completely fill the trench through a simple copper electrolyte without complex organic additives [142, 143]. Another study conducted by Jensen *et al* [144] indicated that the distribution of deposited Ni in groove features was improved by using 1 MHz acoustic agitation. Kaufmann *et al* [145, 146] investigated the capability of megasonic agitation of electroplating into through holes with a conductive sidewall and successfully obtained high quality deposits with an aspect ratio over 2.1 : 1. However, to the author's knowledge, no study of the ultrafine pitch bumping through electrodeposition assisted by megasonic agitation has been reported so far.

5.1.4 Aim of This Chapter

This chapter evaluates the capability of acoustic agitation for improving mass transport condition during the indium electroplating bumping process considering the bump uniformity and consistency. As emphasised before, a uniformly distributed

diffusion boundary layer across the wafer is highly desirable to achieve high uniformity of bumps on the wafer scale. However, conventional agitation approaches still encounter the problem of how to sufficiently penetrate the solution into the ultrafine pitch apertures and maintain a homogenous diffusion boundary layer on the wafer scale. Considering the effects of acoustic agitation introduced above, the improvement of mass transport and the significant change in the diffusion boundary layer seem promising for the ultrafine pitch indium bump forming through electrodeposition.

This chapter will describe experimental work introducing ultrasonic (30 *kHz* frequency) agitation and megasonic agitation (1 *MHz* frequency) into the indium bumping processes. The influences of acoustic agitation on the indium deposition onto non-patterned substrates are investigated first. Then, both ultrasonic and megasonic agitation are employed to assistant in generating ultrafine pitch indium bumps. The bump morphology, microstructure and uniformity are examined and compared with the results shown in the previous chapter.

5.2 Experimental Details

5.2.1 Acoustic Apparatus

The ultrasonic energy was generated by a conventional cleaning bath (model: U950, supplied by Ultrawave Ltd, UK) with the transducer positioned horizontally beneath the bottom of the tank. The bath was able to produce a homogenous ultrasonic field within 26 × 23 cm^2 area with fixed frequency of 30 *kHz*. The power was fixed at 60 *W* so that the intensity of the ultrasound was 0.1 W/cm^2. Figure 5-5 shows the ultrasonic bath employed in the experiments.

Figure 5-5 Ultrasonic cleaning bath, 30 *kHz, 60W*.

A 10 × 10 cm^2 (4 inch × 4 inch) submersible megasonic transducer plate (supplied by SONOSYS GmbH) was utilised to produce a uniform megasonic field in the electrolyte. The transducer was made of piezo-ceramics and was completely encapsulated in PFA (Perfluoroalkoxy). The power unit could be adjusted from 0 to 500 *W* resulting in the maximum output intensity of 5 W/cm^2. However, the frequency was fixed at 1 *MHz*. The megasonic power supply and transducer are shown in Figure 5-6.

(a) Megasonic power supply *(b)* 4 inch megasonic transducer

Figure 5-6 Megasonic apparatus (1 *MHz*, 500 *W*).

5.2.2 Experimental Setup

Electrodeposition of indium was conducted on both non-patterned copper sheet and patterned wafer samples. The pre-treatment of the copper sheet followed the procedures described in Chapter 2. As for the indium bumping trials, two sets of wafer samples were prepared for ultrasonic and megasonic agitation respectively. The wafer samples were patterned with *AZ 9260* photoresist following the same procedure shown in Table 4-1. For the ultrasonic agitation, because of the lack of flexibility in the cleaning bath, the electroplating trials had to be conducted in a beaker which fitted into the tank. Therefore, 3 inch glass wafers were employed and the electroplating bath was configured as shown in Figure 4-7. It should be noted that, although a small part of the sonic energy was reflected by the beaker when the ultrasound wave propagated through it, the energy attenuation did not change the frequency and the energy transmitted into the solution was enough to create cavitation bubbles.

As for the indium bumping in the presence of megasonic agitation, standard 4 inch silicon wafers were employed and the electroplating was conducted in the large volume electroplating tank described earlier. The configuration of the electroplating tank for 4 inch wafer bumping with the presence of megasonic agitation is illustrated in Figure 5-7. The anode and cathode were vertically immersed into the electrolyte with an approximate distance of 25 *cm*, and the megasonic transducer was placed on the bottom of the tank. In theory, the transducer can be positioned horizontally or vertically in the tank. However, considering the size of the transducer, it might obstruct the current flow if it was placed vertically between the electrodes, and was therefore used as shown.

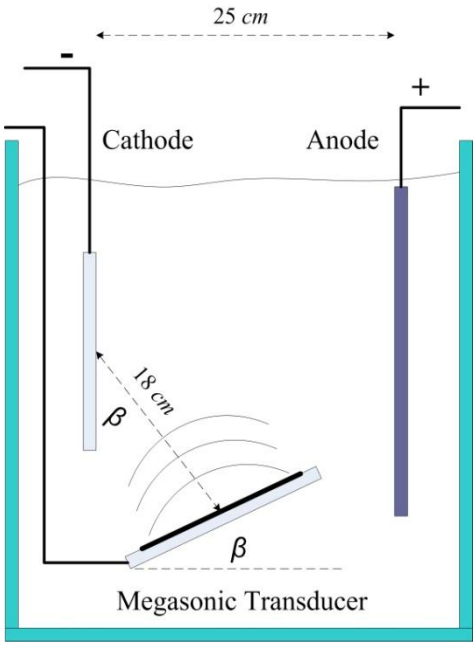


Figure 5-7 Schematic of the configuration of the electroplating tank for 4 inch wafer bumping with the presence of megasonic agitation.

It should be noted that the megasonic transducer should not be positioned absolutely parallel to any solid surface because the reflected sound wave may cause damage to the transducer surface. Therefore, in practice, a default 5° angle is normally set between the transducer and the tank bottom or sidewall. In this study, a transmission angle (β) was defined as the angle between the megasonic transducer and the bottom of the tank which was also the angle between the direction of megasonic energy propagating and the cathode surface. The transmission angle might affect the efficiency of the megasonic energy propagating into the photoresist apertures and was therefore taken into account in experimental design. The distance between the centre of megasonic transducer and centre of cathode was approximately 18 *cm* when the transmission angle $\beta = 30^{o}$. The wafer holder demonstrated in Chapter 4 was also utilised during the electroplating process.

5.2.3 Electroplating Parameters

To understand how the solution performs with acoustic agitation, cathodic potentiodynamic polarisation was firstly conducted on non-patterned substrates by sweeping the potential from the open circuit to -2.0 *V* (relative to SCE) with a

scanning rate of 0.5 *mV/s*. Then, the limiting current densities under 30 *kHz* ultrasonic agitation and 1 *MHz* megasonic agitation were determined. All of the electroplating trials were carried out with direct current to avoid any influences from complex current waveforms. For all of the indium bumping trials, pre-wetting of the photoresist patterns were realised by switching on the acoustic apparatus for a few seconds prior to the actual start of the deposition. Table 5-1 lists the parameters of the indium electrodeposition onto various substrates. Because of the lack of flexibility of the ultrasonic bath, the indium deposition and bump forming with ultrasonic agitation were conducted at 10 mA/cm^2 with fixed frequency and energy intensity. For the megasonic agitation, the energy intensity was increased from 1.25 W/cm^2 to 5 W/cm^2 to investigate the influence of megasonic power while the transmission angle β varied between 15º to 30º. Moreover, electroplating using a very high current density was conducted with megasonic agitation.

5.2.4 Characterisation

For deposition onto a non-patterned substrate, the surface morphology of the deposited indium was observed by Scanning Electron Microscopy (SEM) while the surface profile was inspected with the Talysurf CLI 2000 profiler following the procedure shown in Figure 2-4. The current efficiencies under various conditions were obtained by measuring the weight change before and after electroplating. The bumping yield was also observed through SEM by counting the missed bumps in certain areas. The bump height was measured using the Zygo NewView 5000 white light interferometer and the uniformity was calculated using Equation 4-1. Also, cross-sectional views of the electroplated bumps were prepared by Focused Ion Beam (FIB).

Table 5-1 Parameters of indium electrodeposition and indium bumping in the presence of acoustic agitation.

	Type I. Indium electrodeposition on non-patterned substrate			
No.	Current Density (mA/cm^2)	Acoustic Intensity (W/cm^2)	Acoustic Frequency	Transmission Angle (β)
1	10	0.1	30 *kHz*	N/A
2	10	1.25	*1 MHz*	30º
3	10	2.5		30º
4	10	3.75		30º
5	10	5		30º
6	10	2.5		15º
7	10	5		15º
8	30	2.5		15º
9	40	2.5		15º
10	50	2.5		15º

	Type II. Indium electrodeposition on patterned wafers				
No.	Current Density (mA/cm^2)	Acoustic Intensity (W/cm^2)	Acoustic Frequency	Transmission Angle (β)	Sample Size
11	10	0.1	30 kHz	N/A	3 inch
12	10	1.25	1 MHz	30º	4 inch
13	10	2.5		30º	
14	10	3.75		30º	
15	10	5		30º	
16	10	2.5		15º	
17	10	5		15º	
18	30	2.5		30º	
19	50	2.5		30º	

5.3 Influences of Ultrasonic Agitation on Indium Deposition and Bumping

5.3.1 Cathodic Polarisation with Ultrasonic Agitation

Figure 5-8 plots the current density against the relative cathodic potential in the presence of ultrasonic agitation. It can be seen that, once the deposition started, the current density continuously increased. Compared with the polarisation without agitation where a clear plateau was observed at 30 mA/cm^2, there was no such feature observed here to indicate the highest current density. Instead, the slope of the relationship gradually decreased when the current density approached 40 mA/cm^2 which meant the deposition was moving towards mass transfer controlled region. However, after this, there was a sudden increase of the slope again indicating the occurrence of a side-reaction. The slope changing point could be treated as an approximate reference to define the appropriate parameter window for indium electrodeposition in the presence of ultrasonic agitation. After that, the curve became unstable and hydrogen evolution was observed.

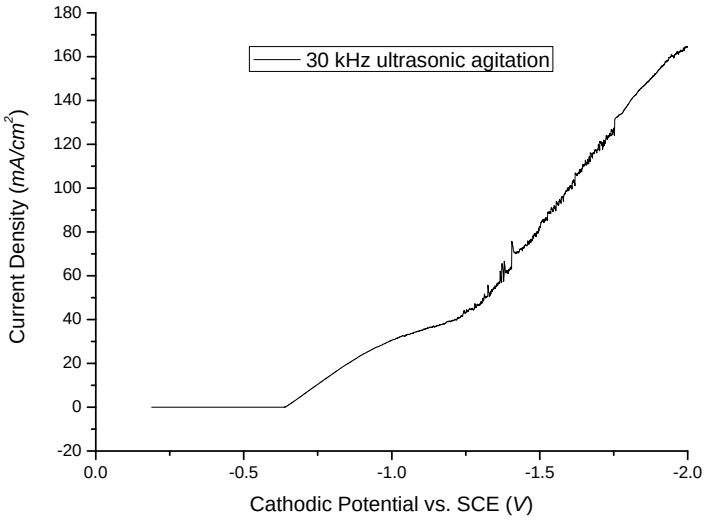


Figure 5-8 Cathodic polarisation curve with presence of 30 *kHz* ultrasonic agitation.

5.3.2 Indium Deposition with Ultrasonic Agitation

Figure 5-9 demonstrates the surface morphology of indium deposited at 10 mA/cm^2 DC with the assistance of ultrasonic agitation. It can be seen that the morphology was

significantly changed by ultrasonic agitation in comparison to the situation of only DC electroplating. The typical large granular surface morphology in DC electroplating was not observed, instead, the deposit appeared nodular. It seemed that the highly oriented growth was disturbed by the ultrasonic agitation. Also, surface feature refinement was observed to some extent. The cathodic current efficiency was measured as 92.3%. The change in the morphology was reflected in the surface profile (Figure 5-10). The measured maximum Total Height of Profile (P_t) and Average Roughness (R_a) were 8.36 μm and 1.09 μm respectively. Apparently, the surface of the electrodeposited indium was smoothed compared to DC electroplating by introducing the ultrasonic agitation.

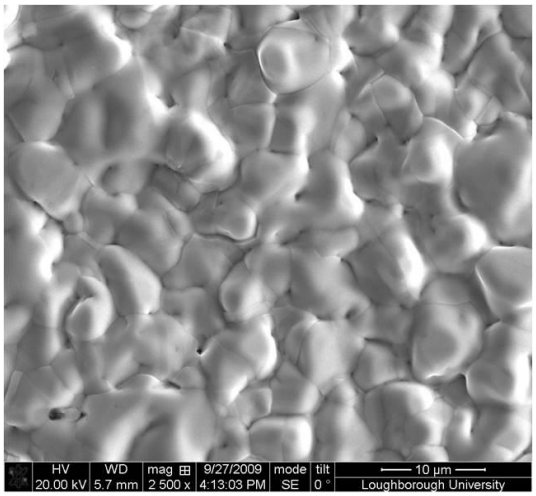


Figure 5-9 Surface morphology of DC (10 mA/cm^2) electroplated indium with 30 kHz ultrasonic agitation

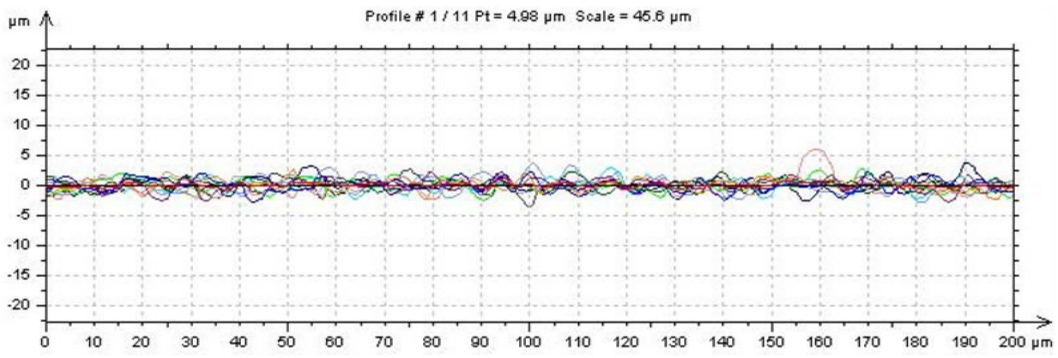


Figure 5-10 Surface roughness of DC (10 mA/cm^2) electroplated indium with 30 kHz ultrasonic agitation measured by Talysurf profiler.

5.3.3 Indium Bumping with Ultrasonic Agitation

Indium bumps were deposited at 10 mA/cm^2 with the presence of ultrasonic agitation. The ultrasonic bath was switched on from the very beginning until the end of electroplating so that the photoresist pattern was wetted as the electroplating started, and the solution was agitated throughout. As demonstrated before, a very high yield can be achieved by pre-wetting the wafer in the ultrasonic bath. It was observed that there were plenty of air bubbles sticking on the wafer surface as the wafer was dipped into the solution because the photoresist was hydrophobic. Once the ultrasound was applied, all the bubbles disappeared immediately. This can partially be explained as the bubbles collapsed due to the acoustic cavitation under the ultrasonic energy transmitted into the solution, and partially may be attributed to the photoresist surface modification under the activation of ultrasonic energy.

Not only can the ultrasound induce the cavitation effect, but also it can heat the solution if the energy is transmitted into the solution for a long time. To maintain the electroplating temperature at room temperature, the water bath outside the electrolyte container was replaced regularly to keep the temperature constant.

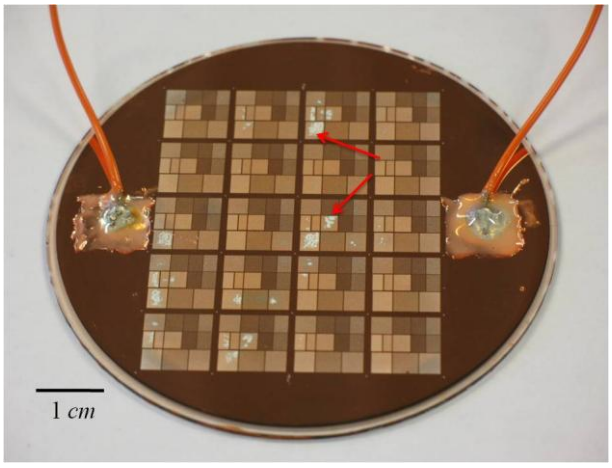
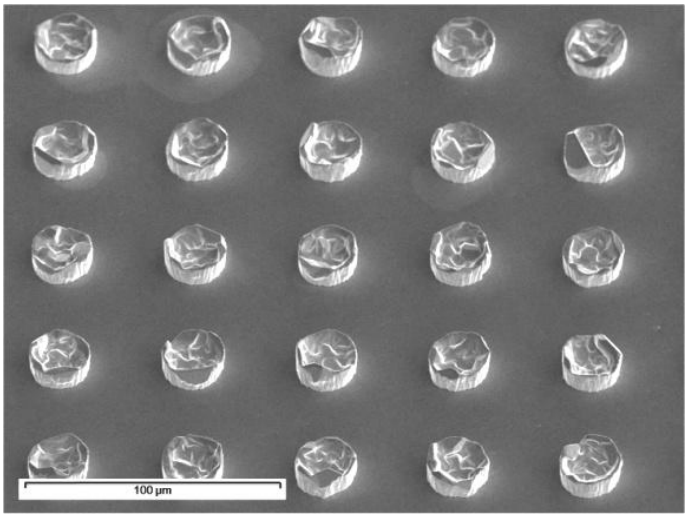


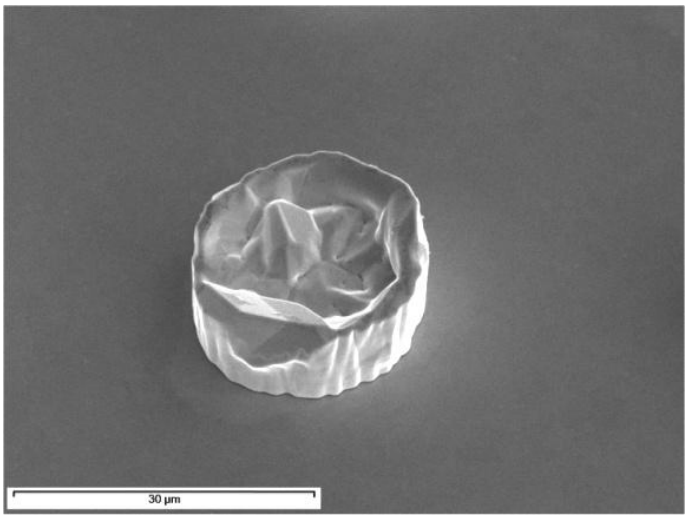
Figure 5-11 Photoresist pattern damaged by ultrasonic energy

After electroplating, it was also found that part of the photoresist pattern was damaged by the powerful cavitation bubbles. The red arrows in Figure 5-11 point to the areas where the photoresist was damaged by the ultrasonic energy. This was caused by the very high vapour pressure and temperature when the bubble reached its

critical size and collapsed. The damage occurred at some point during the electroplating process and the locations were randomly distributed on the surface. It was noted that the damaged area did not develop proportionally with agitation time. In other words, as the agitation time increased, the damaged area did not increase correspondingly with it. This can be explained as the degassing effect of the ultrasonic cavitation. As the cavitation progressed, there was less and less air dissolved in the electrolyte, and the cavitation bubble decreased in the collapsing power and quantity [124].



(a) Overview of electroplated indium bumps



(b) Close-up of electroplated indium bump

Figure 5-12 DC electroplated indium bumps at 10 *mA/cm*^{2} with the presence of ultrasonic agitation (20 *µm* diameter, 50 *µm* pitch).

Figure 5-12 shows the as-electroplated indium bumps under ultrasonic agitation with 20 μm diameter and 50 μm pitch in the areas where the photoresist pattern still survived. It was found that the indium bump had an uneven top finish and featured a hollow in the centre. This was caused by the current crowding effect near the feature opening. The uneven bump profile indicated that the improvement on the mass transport did not diminish the current crowding on the feature scale. The overview indicates a very high bumping yield in the intact pattern areas. However, the probability of the damage to the photoresist makes the ultrasonic agitation unacceptable for wafer bumping applications.

5.4 Influences of Megasonic Agitation on Indium Deposition

5.4.1 Polarisation with Megasonic Agitation

In order to investigate the influences of megasonic agitation on the indium electroplating process, the cathodic polarisation was firstly conducted by scanning the potential from open circuit to -2.0 V (relative to the SCE) in the large volume tank with 1.25 W/cm^2 megasonic agitation (β = 15º). Figure 5-13 plots the relative cathodic potential against the current density and compares with the other electroplating formats. With the presence of megasonic agitation, the supply of reactant ions to the cathode surface was strongly improved such that the current density continuously increased with potential. When the current density approached 80 mA/cm^2, the slope of the curve decreased which indicated that mass transfer started to play an important role during the reaction. After that, the current density increased more rapidly again with potential and hydrogen bubbles were observed. It was noticeable that, in both the curves for acoustic agitation, the polarisation data appeared noisy at the high potential period. This was caused by the disturbance of hydrogen bubbles when both the indium reduction and hydrogen reduction reactions occurred on the cathode surface.

Comparing the three relationships shown in Figure 5-13, it was found that, when the current density was high, the same current density corresponded to different potentials. It can be seen that the overpotential in the high potential region was reduced by using acoustic agitation. This can be explained by the depolarisation caused by the improvement of mass transfer and hydrogen bubbles detaching from the cathode surface. On the one hand, the acoustic agitation can effectively compress the

Nernst diffusion boundary layer and therefore reduce the concentration overpotential. On the other hand, the acoustic agitation can help in removing the reduced hydrogen bubble from the cathode surface. Thus, the reaction of hydrogen reduction $2H^+ + 2e \rightarrow H_2$ tends to move towards the right-hand side. As a result, the hydrogen reduction is accelerated by acoustic agitation. Then, more electrons on the cathode are therefore consumed by hydrogen ions resulting in lower overpotential. Moreover, because the ultrasonic cavitation can induce a stronger degassing effect than megasonic streaming [124], the hydrogen bubbles stay a shorter time in the case of ultrasonic agitation. Therefore, the overpotential in the case of ultrasonic agitation is lower than the megasonic agitation.

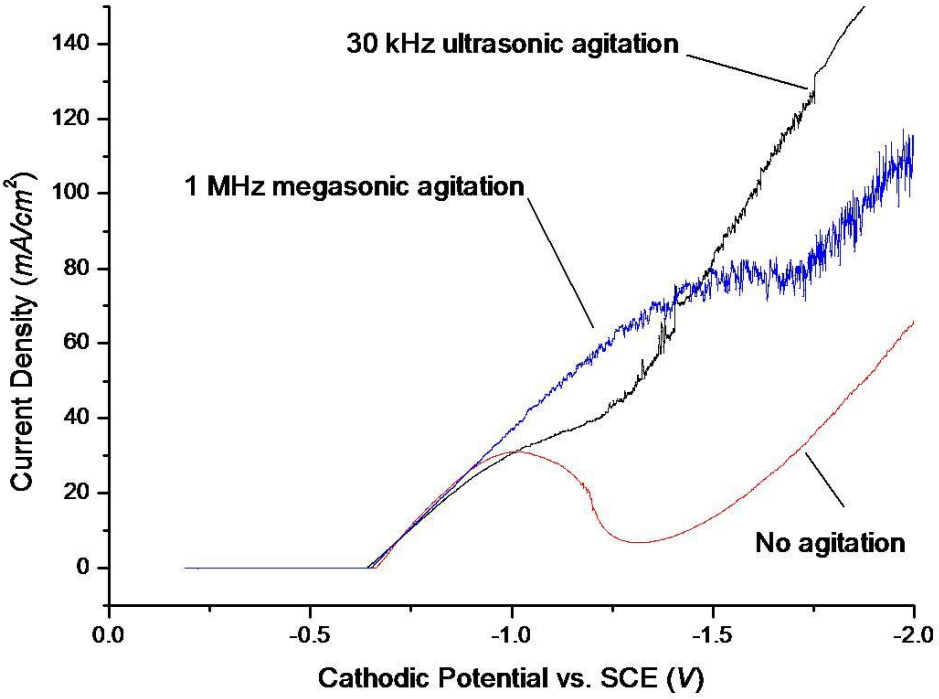
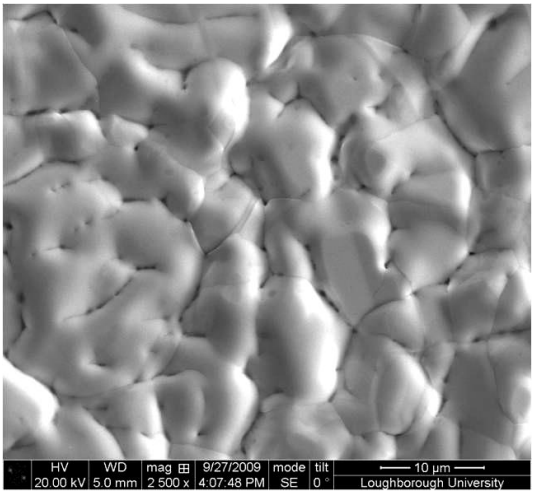


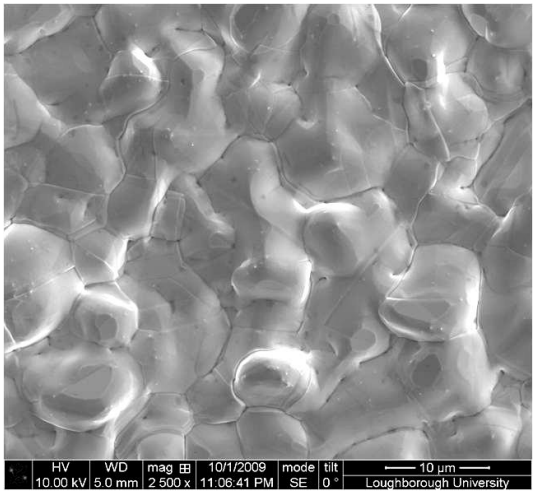
Figure 5-13 Comparison of cathodic polarisation curves for different agitation conditions in indium sulphamate solution with indium anode and copper cathode at room temperature.

5.4.2 Indium Deposition with Megasonic Agitation

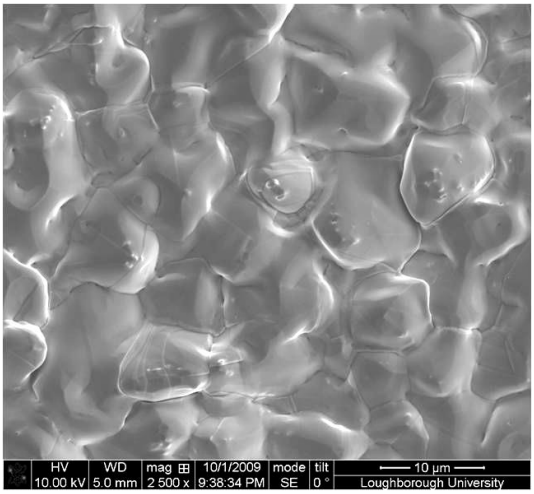
In order to investigate how the megasonic power affects the indium deposition process, electroplating trials on non-patterned substrates were conducted at 10 mA/cm^2 with megasonic intensity of 1.25 W/cm^2, 2.5 W/cm^2, 3.75 W/cm^2 and 5 W/cm^2. The megasonic transducer was tilted to 30º (β = 30º) against the bottom of the electroplating tank. Figure 5-14 shows the surface morphology of the electroplated indium corresponding to various megasonic intensities. It can be seen that the indium was dominated by nodular morphology. The change on the surface morphology was also reflected in the roughness. Figure 5-15 demonstrates the surface profile measurement of indium electroplated at a current density of 10 mA/cm^2 with 2.5 W/cm^2 megasonic agitation. The measured maximum Total Height of Profile (P_t) and Average Roughness (R_a) were 7.5 μm and 0.81 μm respectively. The cathodic current efficiency was measured as 95.14% in this case. The measured surface profiles under other megasonic intensities are listed in Table 5-2. Compared with the DC electroplating without agitation, the surface was smoothed by using megasonic agitation while the cathodic current efficiency was slightly elevated.



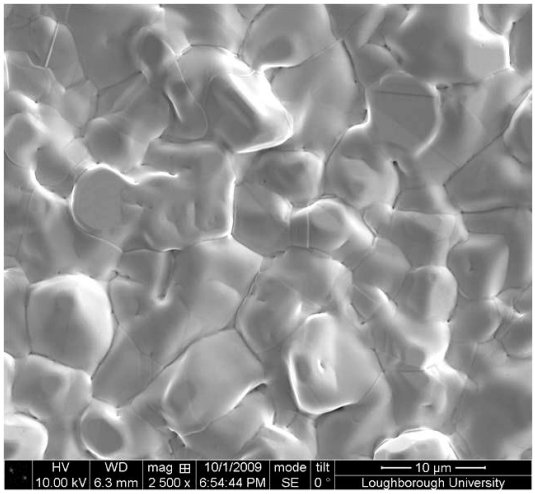
(a) 1.25 *W/cm²*



(b) 2.5 *W/cm²*



(c) 3.75 *W/cm²*



(d) 5 *W/cm²*

Figure 5-14 Surface morphology of indium electrodeposited through DC 10 *mA/cm²* with various intensity of megasonic agitation, *β* = 30º.

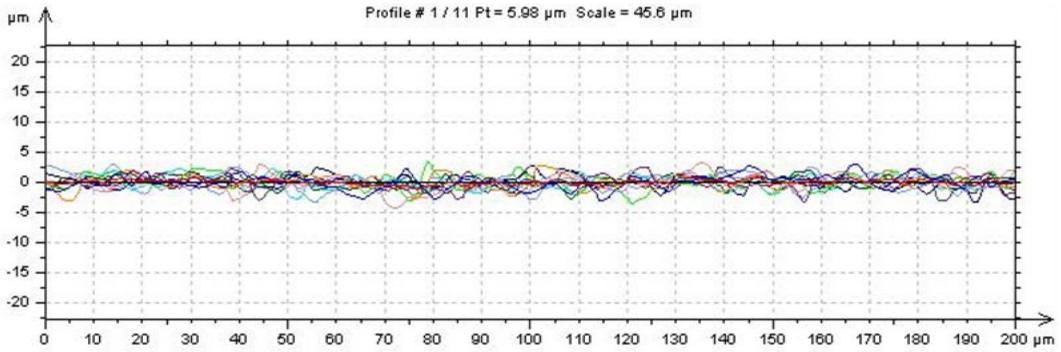


Figure 5-15 Surface roughness measurement of electrodeposited indium through DC 10 *mA/cm²* with 2.5 *W/cm²* megasonic agitation (*β* = 30º).

Table 5-2 Cathodic current efficiencies, maximum Total Height of Profile *(P_t)* and Average Roughness *(R_a)* of deposited indium through DC electroplating with various acoustic agitation conditions.

No.	**Current Density (mA/cm^2)**	**Acoustic Intensity (W/cm^2)**	**Acoustic Frequency**	***β***	**Current Efficiency (%)**	**Max. P_t (μm)**	**R_a (μm)**
1	10	0.1	30 *kHz*	N/A	92.3	8.36	1.09
2	10	1.25	1 *MHz*	30º	93.22	7.18	0.79
3	10	2.5		30º	95.14	7.5	0.81
4	10	3.75		30º	94.58	6.96	0.76
5	10	5		30º	94.6	8.84	0.81
6	10	2.5		15º	95.47	6.64	0.59
7	10	5		15º	93.7	6.89	0.62
8	30	2.5		15º	96.44	12.7	1.08
9	40	2.5		15º	94.5	35.3	2.62
10	50	2.5		15º	95.32	40.14	2.86

It can be seen that the surface morphology was significantly changed by using megasonic agitation; however, the different megasonic intensities had little effect on the surface morphologies found, see Figure 5-14. This is reflected in the similar changes in cathodic potential when various megasonic intensities were applied. Figure 5-16 illustrates the cathodic potential change when sequentially applying 1.25, 2.5, 3.75 and 5 W/cm^2 megasonic agitation to the electroplating process at 10 mA/cm^2. It can be seen that the cathodic potential was elevated by megasonic agitation, but, the offset remained relatively constant while the megasonic intensity increased. It should be noted that the driving force of the deposition reaction is the cathodic potential rather than the current density. Therefore, although the megasonic intensity increased, indium deposition was conducted throughout at almost the same cathodic potential.

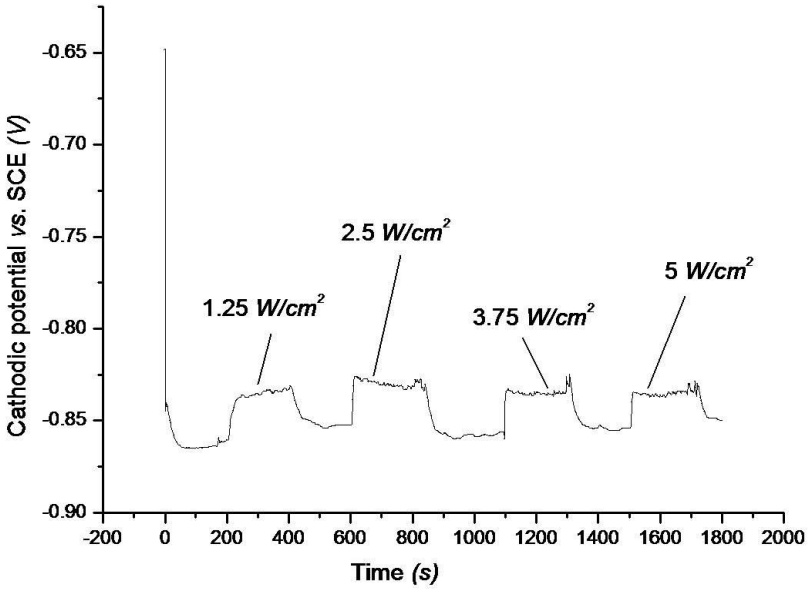
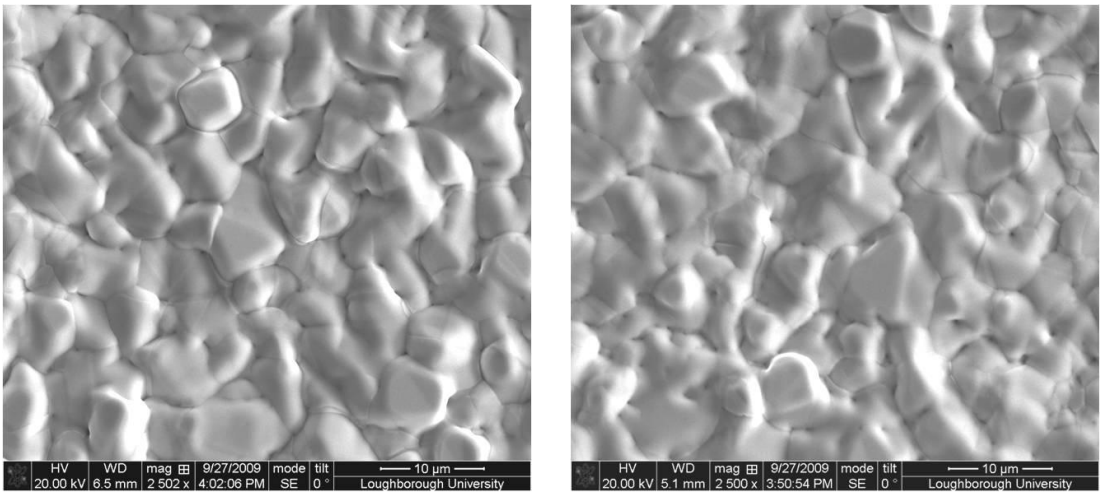


Figure 5-16 Cathodic potential changed by various megasonic intensity at 10 mA/cm^2 current density.

With β = 15º, indium electroplating at DC 10 mA/cm^2 with 2.5 W/cm^2 and 5 W/cm^2 intensity megasonic agitation were conducted to investigate the influences of the direction of megasonic agitation. Figure 5-17 shows the surface morphology of the electroplated indium when β was 15º. It can be seen that the surface of the indium was still dominated by nodular morphology, but the nodular protrusions were relatively flattened in comparison with the situation of β = 30º. The surface measurement indicated that the averaged roughness was slightly reduced by changing the megasound propagating direction, as listed in Table 5-2. Moreover, little influence on the cathodic efficiency was found corresponding to the change of transmission angle.



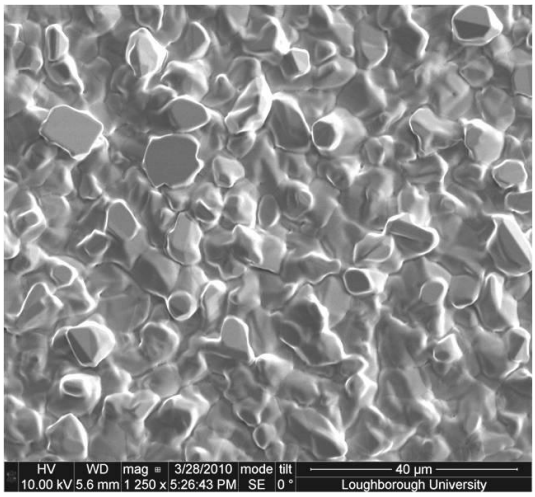
(a) 2.5 W/cm^2 *(b)* 5 W/cm^2

Figure 5-17 Surface morphology of indium electrodeposited at DC 10 mA/cm^2 with various intensity of megasonic agitation, β = 15º.

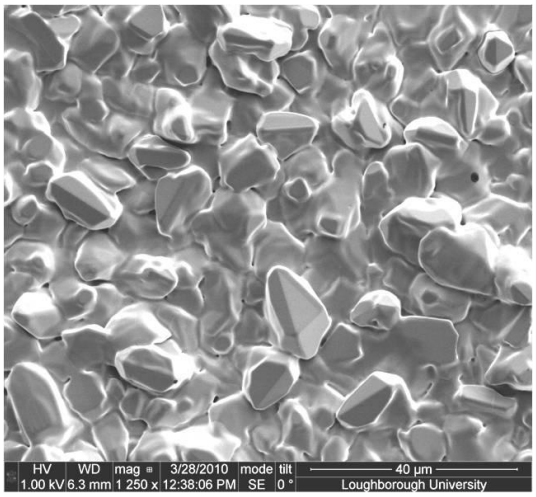
To take the advantage of megasonic agitation, indium electroplating at higher current densities was carried out. Figure 5-18 shows the surface morphology of the indium electroplated through 30, 40 and 50 mA/cm^2 current density with the presence of 2.5 W/cm^2 megasonic agitation (β = 15º). Interestingly, the electroplated indium appeared more granular and the surface feature size increased proportionately with the current density. Correspondingly, the enlarged surface feature size deteriorated the surface flatness and the average roughness also increased proportionately to the current density. When the current density was 30 mA/cm^2, the maximum Total Height of Profile (P_t) and Average Roughness (R_a) were 12.7 μm and 1.08 μm respectively. In the case of electroplating at 40 mA/cm^2, the maximum P_t and R_a were increased to 35.3 μm and 2.62 μm respectively, as listed in Table 5-2. Figure 5-19 demonstrates the surface profile measurement of the electroplated indium. Moreover, the cathodic efficiencies were measured as 96.44%, 94.5%, and 95.32% corresponding to the current densities of 30, 40 and 50 mA/cm^2, as listed in Table 5-2.

The influences of megasonic agitation on the cathodic potential were more profound as the current density increased. Figure 5-20 plots the cathodic potentials with and without megasonic agitation for the cases of 40 and 50 mA/cm^2 DC electroplating. The cathodic potential was significantly reduced allowing the indium electroplating to be conducted at higher current density for which the solution could still supply sufficient reactant species. The current densities in this set of

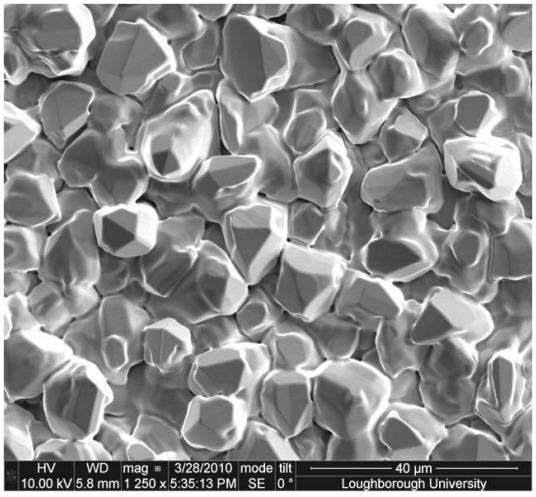
electroplating trials were no longer beyond the limiting value with presence of megasonic agitation. Therefore, by using megasonic agitation, it is possible to achieve high speed deposition without sacrificing current efficiency.



(a) $i = 30\ mA/cm^2$

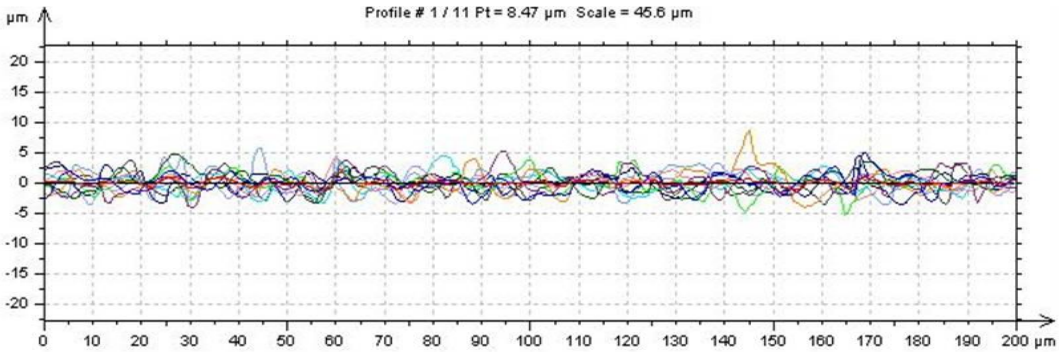


(b) $i = 40\ mA/cm^2$

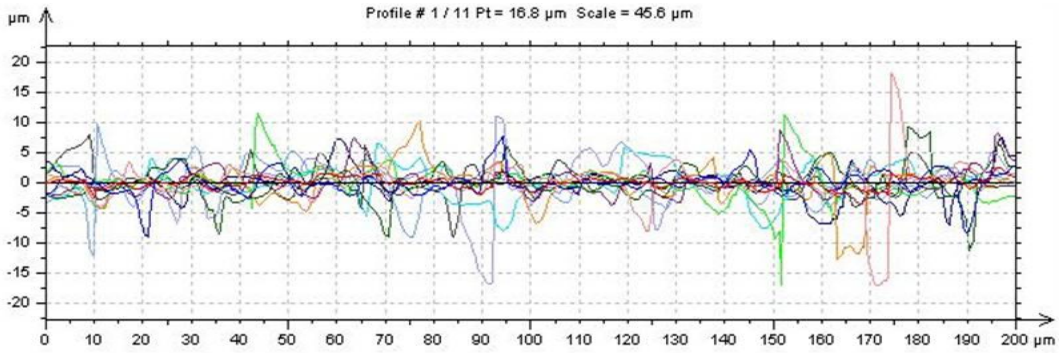


(c) $i = 50\ mA/cm^2$

Figure 5-18 Surface morphology of indium electrodeposited at high current densities with 2.5 W/cm^2 megasonic agitation, $\beta = 15^o$.



(a) $i = 30\ mA/cm^2$



(b) $i = 40\ mA/cm^2$

Figure 5-19 Surface roughness measurement of electrodeposited indium at various current densities with 2.5 W/cm^2 megasonic agitation (β = 15°).

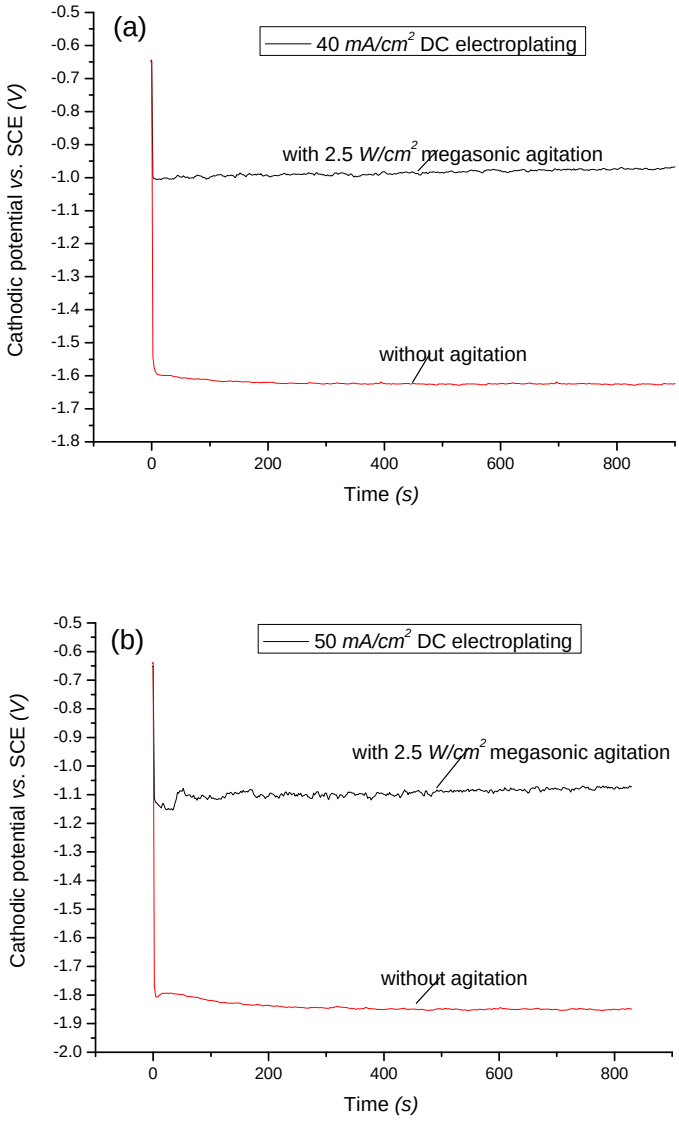


Figure 5-20 Change in cathodic potential at different DC electroplating current densities by applying 2.5 W/cm^2 megasonic agitation (β = 15°): (a) 40 mA/cm^2; and (b) 50 mA/cm^2.

5.5 Indium Bumping with Megasonic Agitation

5.5.1 Influences of Electroplating System Configuration

Megasonic agitation was employed for pre-wetting the ultrafine pitch photoresist patterns prior to the indium bump deposition. It was found that the geometrical configuration of the electroplating tank could strongly affect the pre-wetting

efficiency. As shown in Figure 5-21, with the wafer holder configuration *A* (which was used in previous bumping trials), the edge of the wafer holder acted as an obstacle to the pathway of the megasonic energy propagating to the wafer surface. Because the wavelength of megasound in the solution is about 1.5 *mm*, it is very hard for megasound to bypass the object on its pathway having centimetre dimensions. The photoresist patterns near the lower edge of the wafer holder could not receive enough energy resulting in insufficient coverage by the solution, such that the yield was not acceptable for wafer bumping, as shown in Figure 5-21. According to the dimensions of the designed photomask and the wafer holder, it was calculated that the megasonic energy would be able to cover all of the patterns by tilting 30 º against the horizontal.

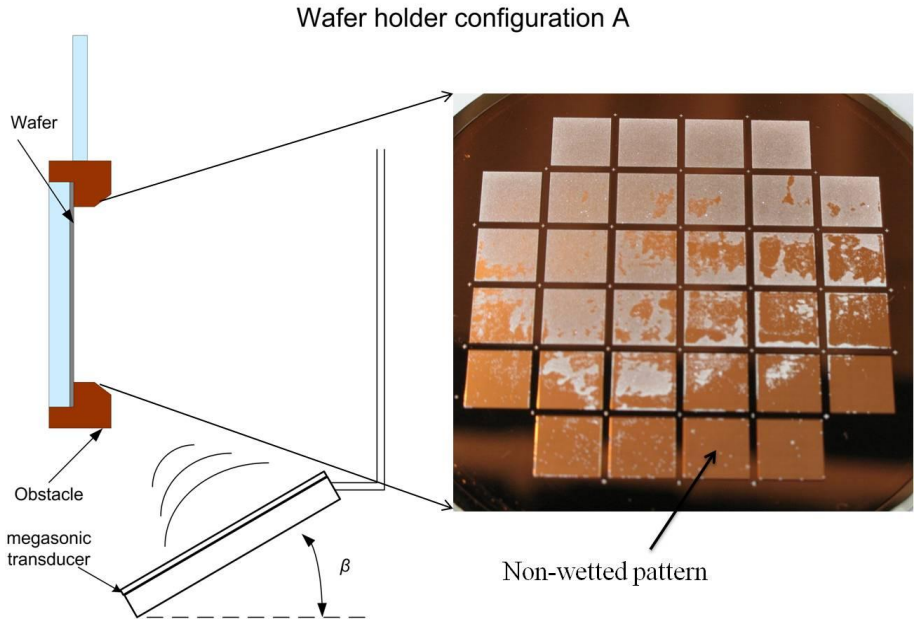


Figure 5-21 Influences of the obstacle to megasonic energy propagation created by the wafer holder on the pre-wetting of the ultrafine pitch features.

Although sufficient wetting of the photoresist pattern could be achieved by tilting the transducer to an appropriate angle, a so-called ‘pitting’ effect was still observed on the wafer surface, when the wafer holder configuration *A* was adopted in the ensuing bumping process. Many gas bubbles were observed sticking on the wafer surface all through the electroplating process. As shown in Figure 5-22, the bubbles induced a ‘pitting’ effect and left incompletely electroplated patterns. The indium bumps in the bubble sites had insufficient material and smaller height which can be

seen in the circled area in Figure 5-23. The bubbles were caused by the megasonic streaming effect rather than hydrogen evolution because the current efficiency was still very high and consistent with the situations listed in Table 5-2. Considering the requirement of high yield, the pitting effect is not acceptable for indium bumping.

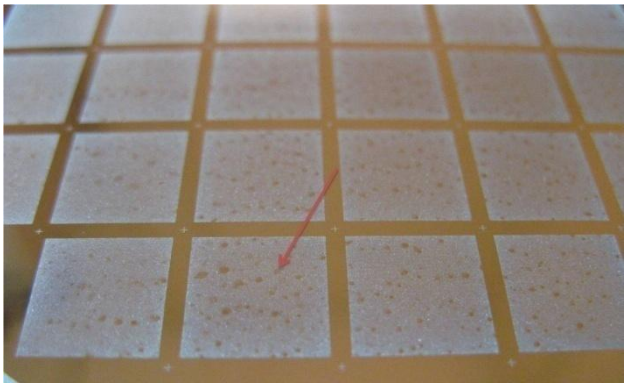


Figure 5-22 Pitting effect caused by the gas bubbles on the patterned wafer after DC electroplating at 10 *mA/cm*^{2} with presence of megasonic agitation using wafer holder configuration *A*.

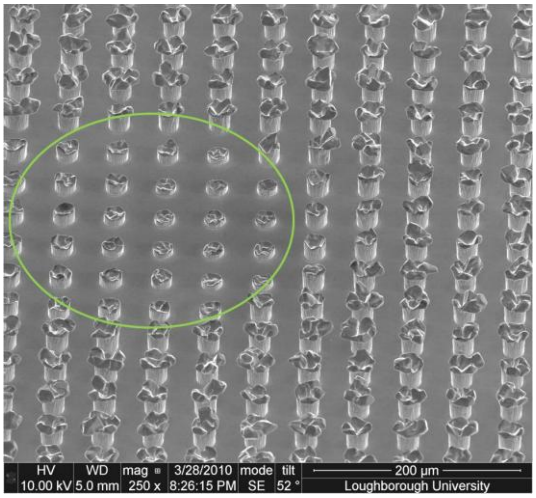


Figure 5-23 Non-uniform indium bumps on the bubble sites after DC electroplating at 10 *mA/cm*^{2} with presence of megasonic agitation using wafer holder configuration *A*.

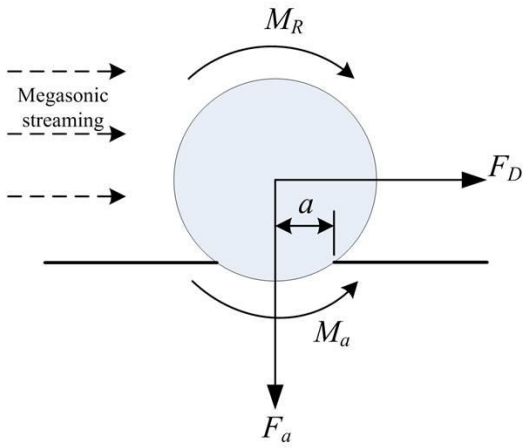


Figure 5-24 Mechanism of particle removal in megasonic cleaning: F_a is the adhesion force; F_D is the drag force; M_R is the removal moment and M_a is the adhesion moment.

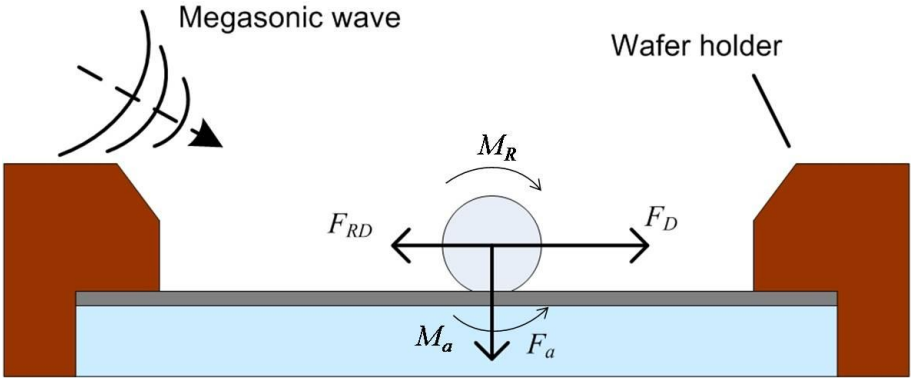


Figure 5-25 Mechanism of the pitting effect in the wafer holder

The possible reason for the pitting effect can be attributed to the wafer holder configuration. A rolling mechanism has been widely accepted to explain the particle removal in megasonic cleaning [147]. As shown in Figure 5-24, taking an individual particle for example, there are two main forces taking part in the removal: adhesion force (F_a) and drag force (F_D). When the removal moment M_R exceeds the adhesion moment M_a, the particle will be rolled away from the surface. This mechanism also can be applied to detach bubbles from the surface. However, in the case of wafer bumping, the edge of the wafer holder acted as an obstacle to the pathway of megasonic streaming flow along the surface. A large proportion of the longitudinal component of the megasonic wave along the wafer surface was reflected by the holder edge in front of the pathway and contributed to a reverse force (F_{RD}), as shown in

Figure 5-25. Therefore, once the bubble attached to the wafer, it was hard to overcome the adhesion force since the drag force was compromised by the reflected energy.

To overcome the pitting effect, a new design of the wafer holder was adopted by removing the protruding edge, as the configuration *B* shown in Figure 5-26. The wafer was kept at the same level as the holder edge such that there was no obstruction to the pathway of the megasonic streaming flow. Experimental results indicated that a high yield could be achieved with the wafer holder configuration *B* and no pitting effect was observed after electroplating with megasonic agitation (see the completely electroplated wafer patterns in Figure 5-26). Therefore, this wafer holder configuration was utilised in all of the following indium bumping trials.

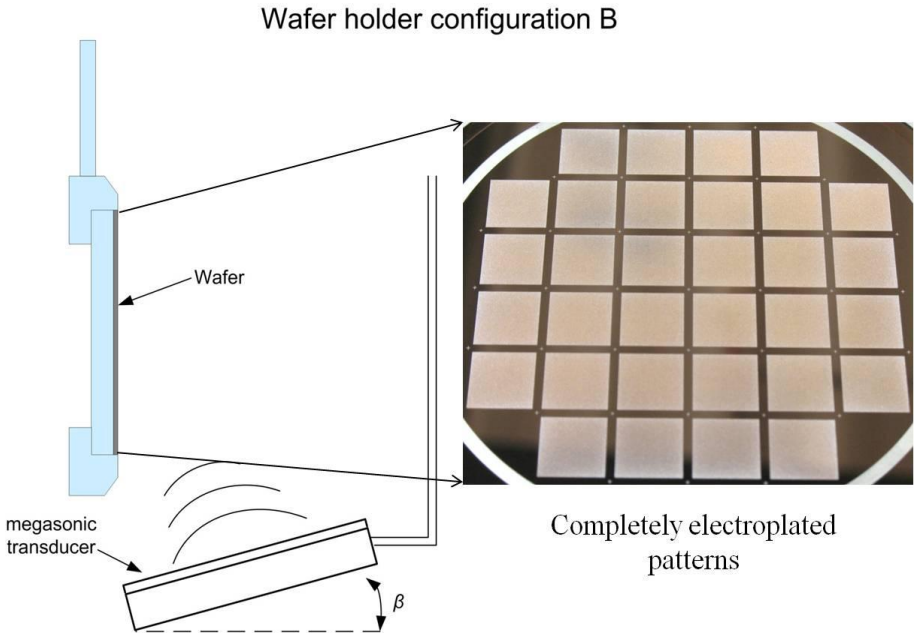
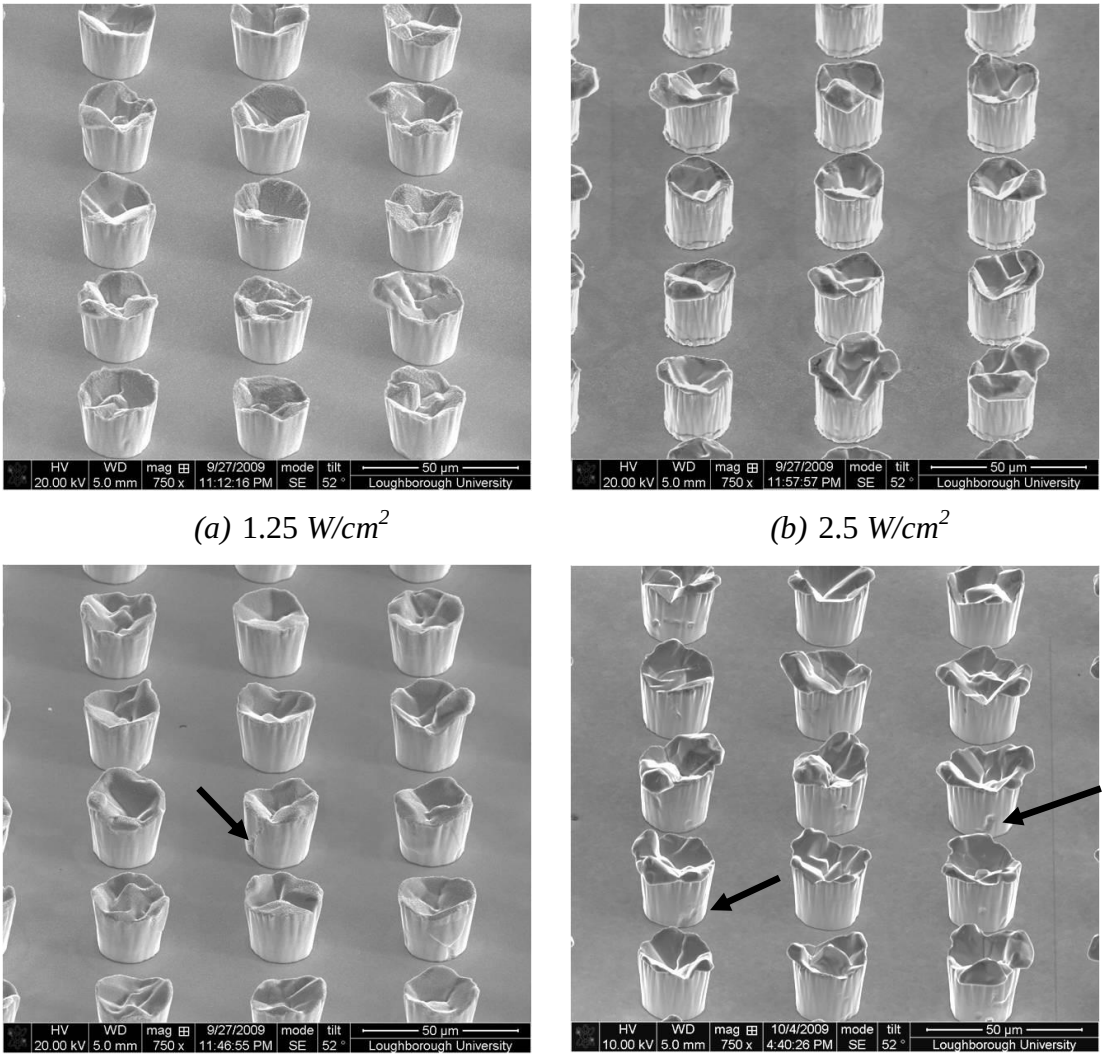


Figure 5-26 Amended design of wafer holder and completely electroplated patterns.

The impacts of megasonic agitation on the photoresist pattern were also examined. The experimental results indicated that the high frequency megasound showed no effect on the fragile photoresist patterns. After immersing the patterned wafer into a 5 W/cm^2 megasonic field for 60 minutes, which was the maximum output intensity of the power supply and longest electroplating time in all experiments, no damage to the photoresist pattern was observed. Therefore, megasonic agitation is suitable for wafer bumping applications as the yield reaches high levels. Moreover, as

with ultrasonic agitation, high frequency megasonic agitation could also bring heat to the solution. However, due to the large volume of the electroplating solution, the temperature elevation was less than 5 ^oC under the highest megasonic intensity and longest electroplating time, *i.e.* 5 W/cm^2 megasonic agitation for 60 minutes. So, the thermal effect of the megasonic agitation was ignored in this study.



(a) 1.25 W/cm^2 *(b)* 2.5 W/cm^2

(c) 3.75 W/cm^2 *(d)* 5 W/cm^2

Figure 5-27 Indium bumps electroplated at DC 10 mA/cm^2 with various megasonic intensity (β = 30º).

5.5.2 Influences of Megasonic Agitation on Indium Bump Growth

Indium bump deposition trials at DC 10 mA/cm^2 with various megasonic intensities were investigated. All of the wafer samples were patterned using the mask *No. 5*. The overview of indium bumps electroplated at 10 mA/cm^2 current density with various megasonic intensities, but fixed transmission angle (β = 30º), are shown in Figure 5-27. It can be seen that the indium bumps still have an uneven top finish that is, the bump centre is lower than the bump edge. The megasonic intensity did not cause a noticeable change to the bump profile. However, it was found that, with an increase of megasonic intensity, the consistency of the bumps tended to deteriorate due to defects that occurred on the sidewall, as indicated by the arrows in Figure 5-27*c* and *d*.

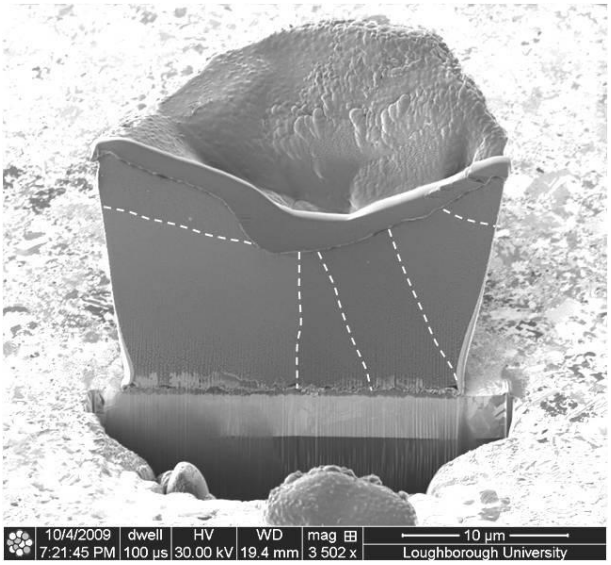


Figure 5-28 Cross-sectional view of indium bump electroplated at DC 10 mA/cm^2 with 5 W/cm^2 megasonic intensity (β = 30º).

Figure 5-28 shows the cross-section of an indium bump electroplated with 5 W/cm^2 megasonic agitation. It can be seen that the defects observed on the sidewall did not occur inside the bump. The bump material appeared consistent with other electroplating conditions demonstrated in previous chapters. The grain size in the bump could still reach the order of 10 μm. Moreover, the bump still had remarkable non-uniformity on the feature scale.

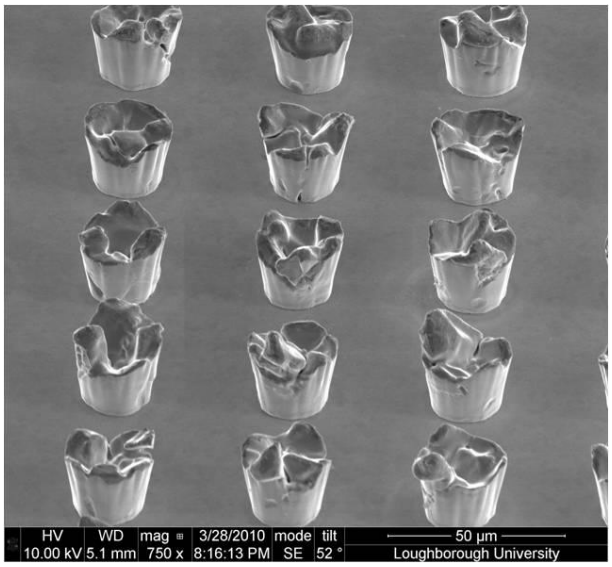
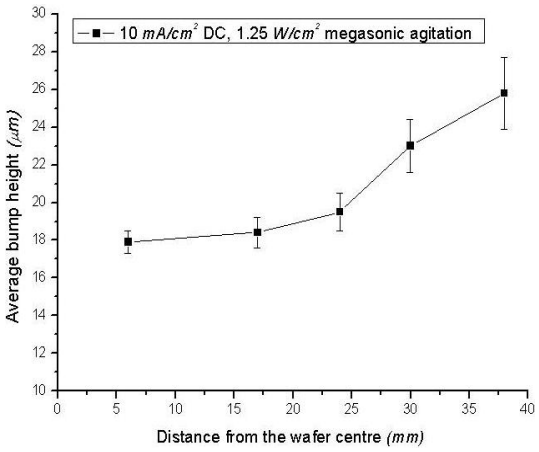
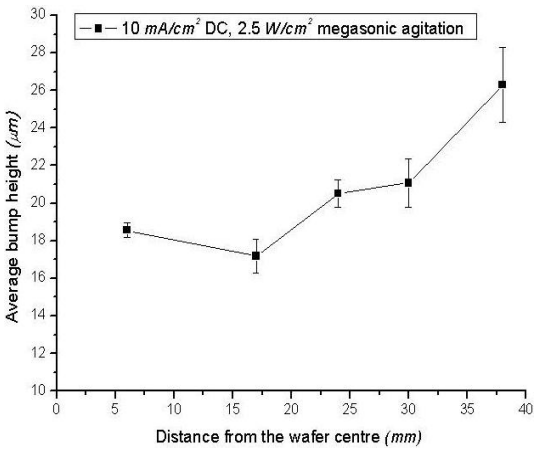


Figure 5-29 Indium bumps electroplated at DC 10 mA/cm^2 with 5 W/cm^2 megasonic intensity when β = 15º.

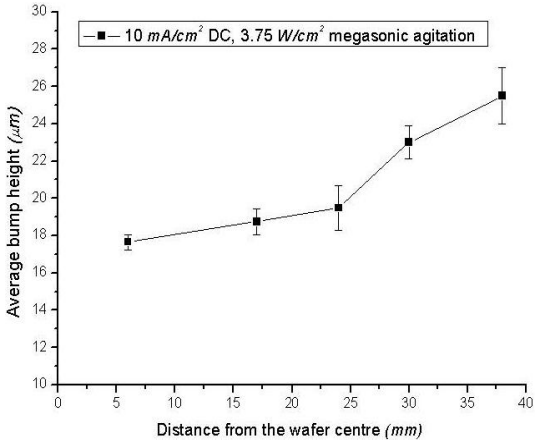
Figure 5-29 shows the indium bumps electroplated at 10 mA/cm^2 DC with 5 W/cm^2 megasonic intensity when β = 15º. It was found that the consistency and feature scale uniformity deteriorated when the transmission angle was reduced. The defects on the sidewall were thought to be attributed to micro air bubbles trapped in the photoresist apertures. The current efficiency in this case was measured as 93.23% indicating that the defects were mainly caused by air bubbles rather than hydrogen reduction. Therefore, it is recommended that the megasonic wave should be delivered through a larger transmission angle to provide more energy into the apertures.



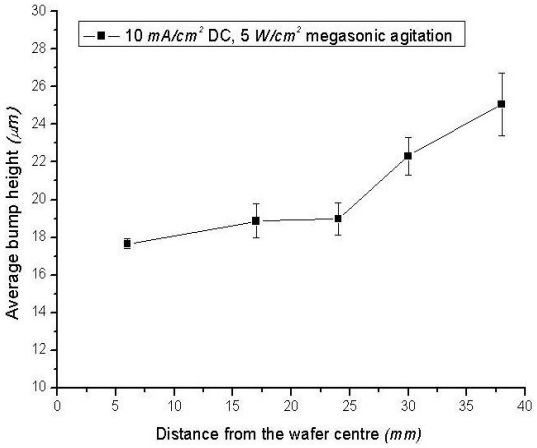
(a) 1.25 W/cm^2 megasonic intensity



(b) 2.5 W/cm^2 megasonic intensity

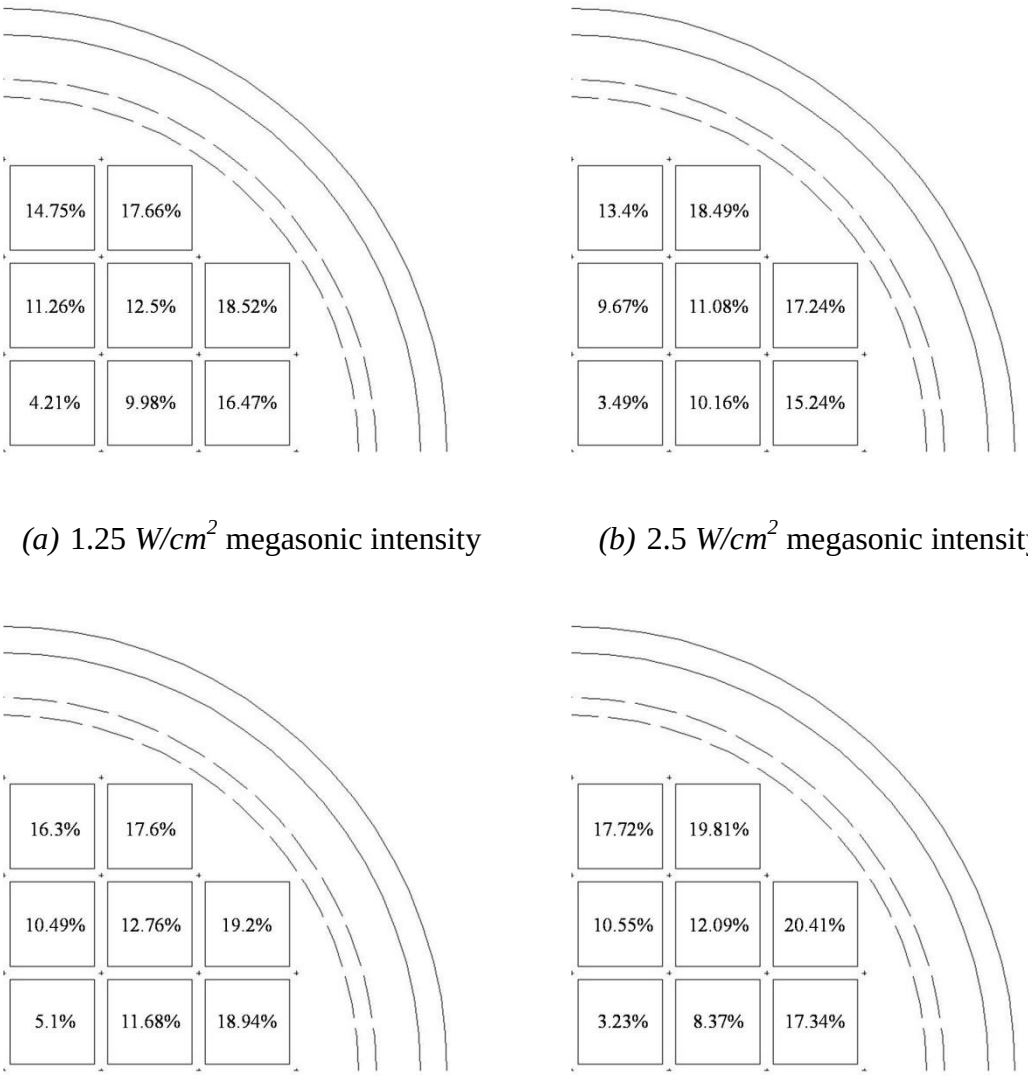


(c) 3.75 W/cm^2 megasonic intensity



(d) 5 W/cm^2 megasonic intensity

Figure 5-30 Measurement of wafer scale uniformity of indium bumps electroplated at DC 10 mA/cm^2 with different intensities of megasonic agitation (β = 30°).



(a) 1.25 W/cm^2 megasonic intensity

(b) 2.5 W/cm^2 megasonic intensity

(c) 3.75 W/cm^2 megasonic intensity

(d) 5 W/cm^2 megasonic intensity

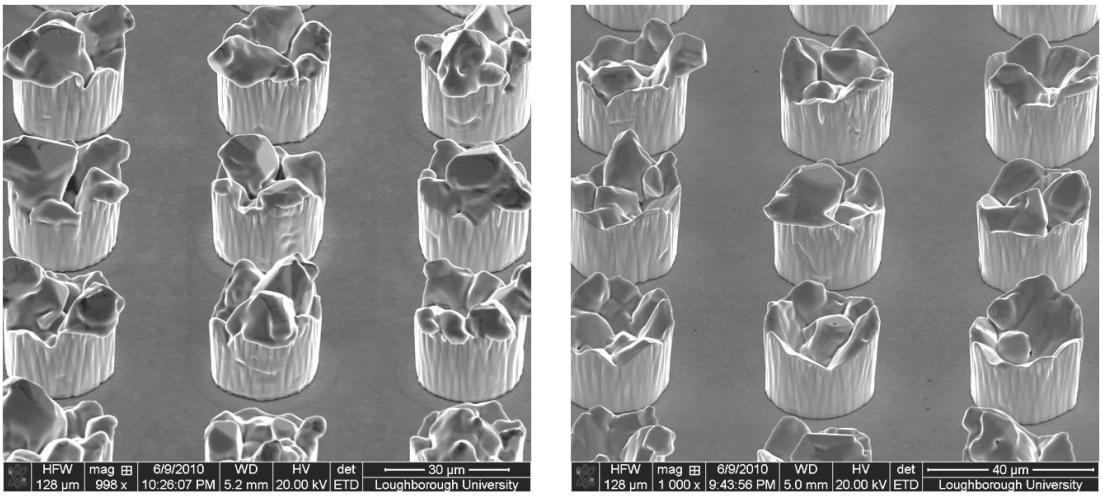
Figure 5-31 Measurement of pattern scale uniformity of indium bumps electroplated at DC 10 mA/cm^2 with presence of various intensities of megasonic agitation (β = 30º).

The uniformity of the electroplated bumps was measured according to the methodology shown in Figure 4-40 on both the wafer and pattern scales. The wafer scale uniformities of electroplated bumps at 10 mA/cm^2 current density with 1.25, 2.5, 3.75 and 5 W/cm^2 megasonic agitation are shown in Figure 5-30. The measured uniformity was 25.08%, 24.36%, 23.75% and 24.11% corresponding to the 1.25, 2.5, 3.75 and 5 W/cm^2 megasonic agitation. It can be seen that the wafer scale uniformity deteriorated slightly in comparison to the DC electroplating without agitation. It was also found that, when the megasonic agitation was applied and other electroplating

parameters remained the same, the non-uniformity was mainly caused by the large bumps near the wafer boundary. Also, the pattern scale uniformity deteriorated more rapidly from the wafer centre to the edge, as shown in Figure 5-31. The uniformity within the patterns close to the wafer centre was improved compared with DC electroplating without agitation.

5.5.3 High Speed Indium Bumping with Megasonic Agitation

Indium bumping trials at current densities of 30 and 50 mA/cm^2 were conducted to explore the feasibility of high speed bump deposition with the presence of megasonic agitation. Figure 5-32 shows an overview of the indium bumps electroplated at 30 and 50 mA/cm^2 with 2.5 W/cm^2 megasonic agitation (β = 30º). The bumping yield was more than 99.9% and the current efficiencies were measured as 94.18% and 93.89% corresponding to the 30 and 50 mA/cm^2 electroplating conditions respectively. The high current efficiency indicated that sufficient megasonic energy was delivered into the photoresist apertures and there was no significant side reaction occurring. Large sized crystals were observed at the bump and the feature scale uniformity deteriorated in comparison to the situation of no-agitation.



(a) i = 30 mA/cm^2 *(b)* i = 50 mA/cm^2

Figure 5-32 Indium bumps electroplated at 30 and 50 mA/cm^2 current densities with presence of 2.5 W/cm^2 megasonic agitation, β = 30º.

The uniformity of the electroplated bumps was measured on both the wafer scale and pattern scale. As demonstrated in Figure 5-33, the wafer scale uniformity was measured as 25.83% and 29.69% corresponding to the 30 and 50 mA/cm^2 electroplating conditions. It can be seen that the wafer scale uniformity deteriorated with the increase of the current density. Moreover, by applying the megasonic agitation, the pattern scale uniformity also became worse when the indium bumps were electroplated at higher current density, as shown in Figure 5-34.

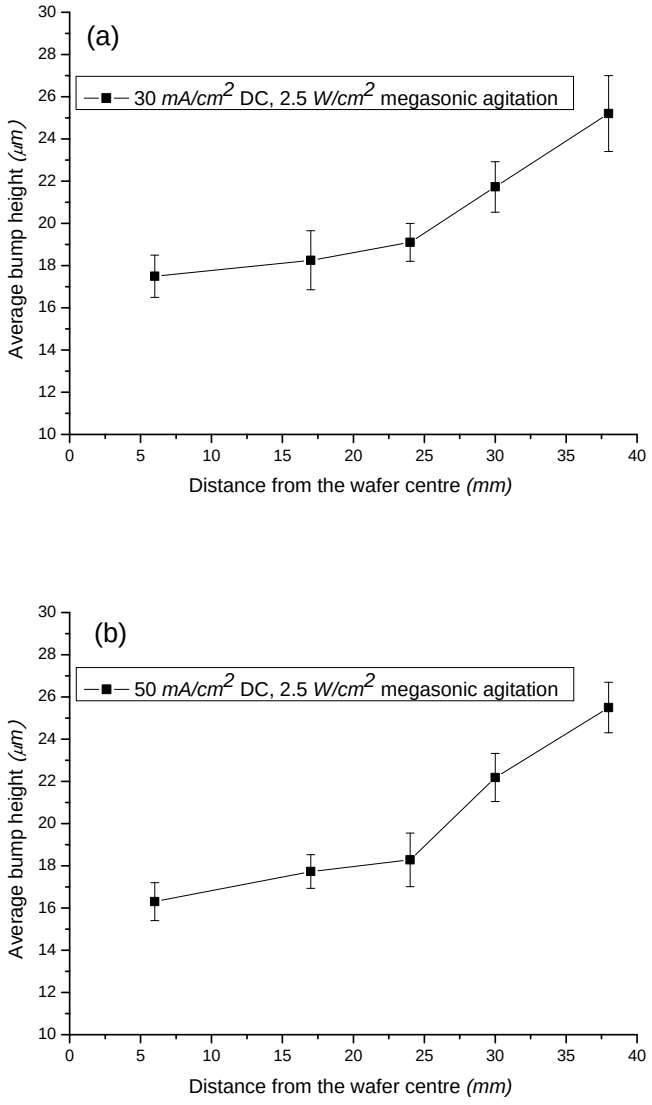


Figure 5-33 Wafer scale uniformity of indium bumps electroplated at various current densities with presence of 2.5 W/cm^2 megasonic agitation (β = 30°): (a) 30 mA/cm^2; and (b) 50 mA/cm^2.

(a) $i = 30\ mA/cm^2$ *(b)* $i = 50\ mA/cm^2$

Figure 5-34 Pattern scale uniformity of indium bumps electroplated at various current densities with presence of 2.5 W/cm^2 megasonic agitation, $\beta = 30^o$.

5.6 Summary

Acoustic agitation with different frequencies was applied to indium deposition and bump forming processes. The influences of the surface morphology, microstructure, electroplating efficiency and deposit uniformity were investigated. Based on the experimental results, several conclusions can be drawn as following:

- Ultrasonic agitation is a capable approach for pre-wetting the ultrafine pitch patterns. However, the probability of damage to the photoresist pattern increases with loading time which makes ultrasonic agitation unacceptable for wafer bumping.
- Megasonic agitation is also able to fulfil the requirement of pre-wetting for high yield. In all of the experiments, no damage to the photoresist pattern was observed with the presence of megasonic agitation. However, the geometric configuration of the electroplating system can significantly affect the efficiency of pre-wetting.
- To apply megasonic agitation all through the bumping process, the configuration of the electroplating system needs to be adjusted to form a clear pathway for the megasonic wave. Otherwise, the megasonic streaming effect will be compromised and thereafter the bumping yield deteriorates.

- At lower current densities, the wafer scale uniformity deteriorates slightly by introducing the megasonic agitation into the bumping process. However, the pattern scale uniformity can be improved.
- The probability of defects occurring along the bump sidewall increases with megasonic intensity and is inversely proportional to the transmission angle (β) which the megasonic sound wave propagates to the wafer surface.
- High speed bumping has been realised through higher current density with assistance of megasonic agitation. However, the uniformity issue becomes more serious at both the wafer scale and pattern scale.

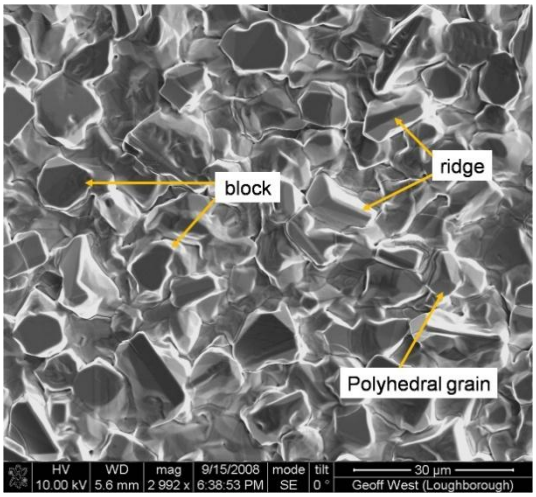
Chapter 6 Discussion

This chapter is to integrate the experimental results, which have been presented in previous chapters, in connection with the relevant studies from the literature, thereby providing an overview and discussion of this research. The characteristics of indium electroplated through DC, unipolar pulse electroplating and bipolar pulse reverse electroplating are firstly compared. Then, the influences of various electroplating parameters and configuration of the electroplating system on bumping uniformity are summarised. The mechanism of indium bump growth by DC and pulse electroplating are explained through an investigation of the deposition processes and the influences of acoustic agitation on indium deposition are discussed. Finally, issues of scaling up the bumping process are discussed with respect to the bumping uniformity and possible solutions are proposed.

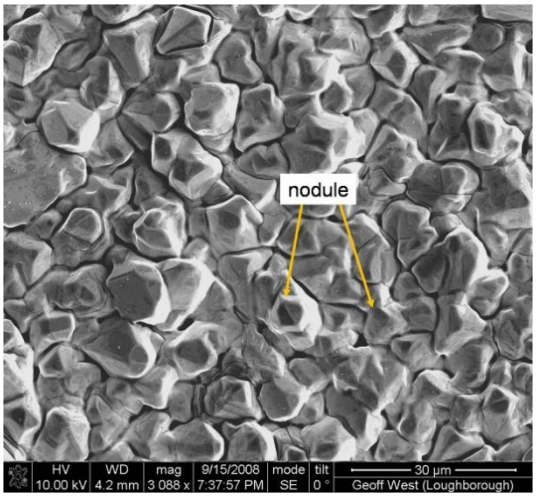
6.1 Feasibility of Indium Deposition Using Sulphamate Solution

As mentioned before, very limited information about indium electroplating can be found in the literature while the majority of the studies were reported before the 1980s [45-48, 51, 148-150]. Due to the commercial interests and trade secrets, the work on indium electroplating using sulphamate solution is not very well documented and published in the public domain. On the basis of experimental results demonstrated above, it can be seen that it is relatively straightforward to deposit indium using a sulphamate solution that is commercially available. According to the electrochemistry of indium electroplating, indium is obtained through the reaction of $In^{3+} + 3e \rightarrow In$ [45]. Based on the cathodic current efficiency measurement, it is recommended that

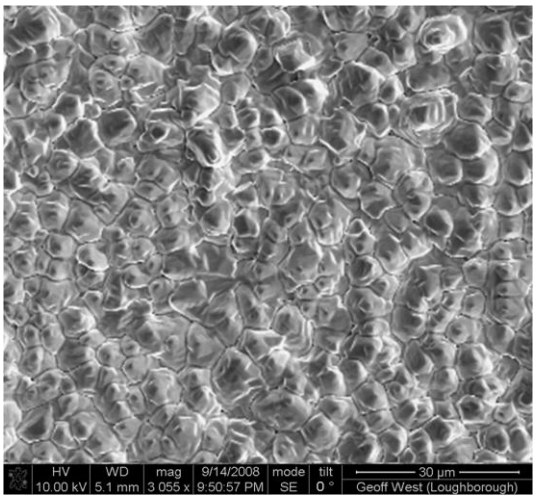
the indium deposition should be carried out at no more than 20 mA/cm^2 for which more than 90% current efficiency can be achieved at room temperature without the presence of any additional agitation.



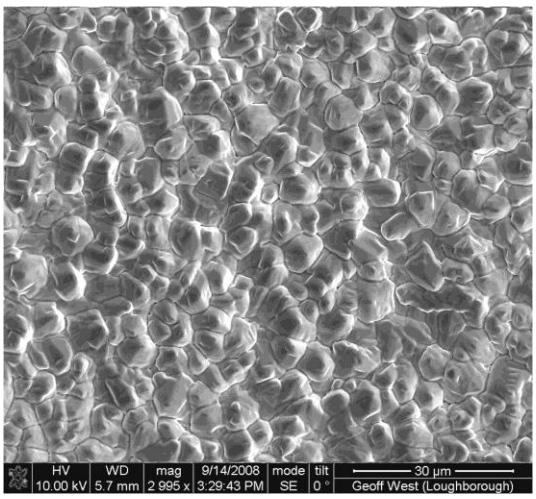
(a) DC electroplating, i =10 mA/cm^2.



(b) DC electroplating, i = 35 mA/cm^2.



(c) Pulse electroplating, i_p = 50 mA/cm^2, i_{avg} = 10 mA/cm^2.



(d) Pulse electroplating, i_p = 100 mA/cm^2, i_{avg} = 10 mA/cm^2.

Figure 6-1 Comparison of surface morphology and surface feature size of indium electrodeposited using DC and pulse current waveforms.

It has been found that, under an average current density of 10 mA/cm^2, the cathodic current efficiency for pulse electroplating can still reach more than 90% in the case of $i_p \leqslant 100$ mA/cm^2. The experimental results have demonstrated that the indium sulphamate solution is stable, easy to use and maintain during the operation of

the electroplating process, and such advantages make the sulphamate solution a primary candidate for indium electrodeposition.

6.2 Comparison of Microstructure Characteristics of Indium

It is known that, in most cases, the electrocrystallisation process is kinetically governed by the combined effects of charge transfer and mass transfer [40]. In this study, indium deposits appeared to have various morphologies subject to the use of different electroplating parameters. As can be seen in Figure 6-1*a*, ridges, blocks and polyhedral grains were present in the electroplated indium when the current density was below 30 mA/cm^2. According to the idealised polarisation curve of electroplating in Figure 2-2 (page 23), the formation of ridges and polyhedral grains are likely to be formed at a lower current density due mainly to the charge transfer control with an insignificant effect from mass transfer [42]. However, the presence of block deposits still appeared in indium electroplating even at a higher current density, which may also reflect the levelling effects caused by the two additives, *i.e.* dextrose and triethanolamine. In such a case, the grain growth along the direction perpendicular to the substrate surfaces may be hindered. Therefore, some lattice faces that are associated with certain crystal orientations became the facets present as morphological features in the final surface finish. In contrast, when the current density was greater than 30 mA/cm^2, indium tended to be deposited as a number of nodules (Figure 6-1*b*), which indicates that the electroplating was governed predominately by mass transfer due to the applied higher current density.

In the pulse electroplating, the pulse duration was fixed as 1 *ms* while the pulse-off time increased from 2 *ms* to 99 *ms*. This was to investigate how the solution performed under various peak current densities, and to understand how the pulsating current can affect the indium deposition process. The pulse current density in this work started from 30 mA/cm^2, while the average current density remained as 10 mA/cm^2. With the increase of pulse peak current density, surface feature refinement was observed in pulse electroplating, as shown in Figure 3-5 (page 51) and also provided in Figure 6-1*c & d* for comparison.

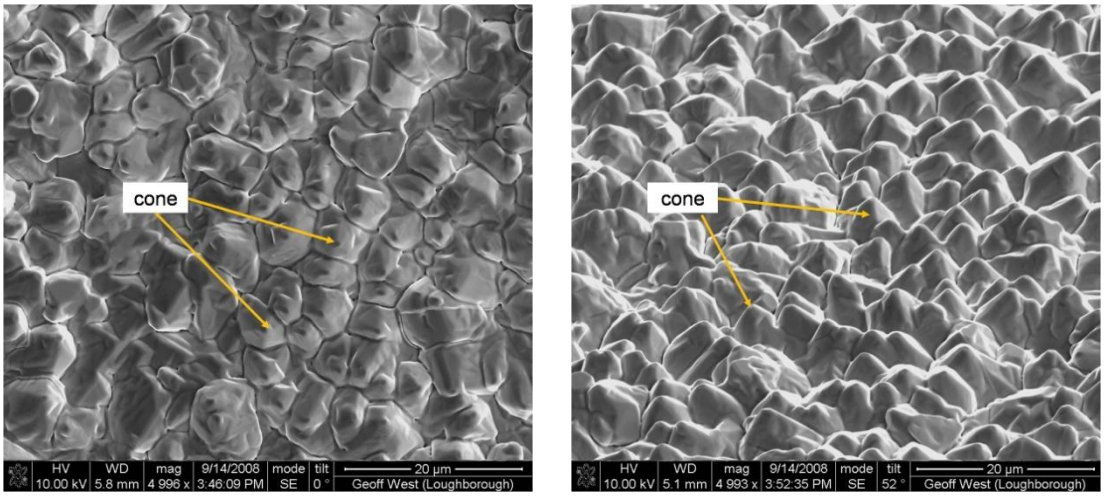
Pulse electroplating induced surface feature refinement has been systematically observed in various electrodeposition systems which can be attributed to the improved nucleation rate at a higher pulse peak current density [57-59].

According to Puippe [54], the nucleation rate (V_n) during the electroplating is determined by:

$$V_n = k_1 \exp\left(-\frac{k_2}{\eta}\right) \tag{6-1}$$

where k_1 is a proportionality constant, k_2 is related to the amount of energy required for nucleation and η is the overpotential. It can be seen that the nucleation rate increases exponentially with the overpotential. Having the same average current density, the pulse current densities in all of the waveforms used for indium electrodeposition were much higher than the DC current density so that the overpotential during the pulse-on duration was much higher in the pulse electroplating process. This explains the significant surface feature refinement due to the enhanced nucleation rate under the higher pulse current densities.

When the pulse peak current density was 30 *mA/cm*^{2}, the deposits still mainly appeared as granular and the lattice facets were clearly observed which showed similarity with the DC electroplated indium, although the surface feature refinement was apparent (see Figure 3-5*a*, page 51). When the peak current density reached 40 *mA/cm*^{2}, the deposit included many nodules and cones, and mainly cones under the higher pulse current density. However, as demonstrated in Figure 3-5*c* to *j*, it was hard to find differences in the surface morphologies of the electroplated indium with pulse current waveforms when i_p varied between 50 to 300 *mA/cm*^{2}. The 52º tilted view in Figure 6-2*b* clearly shows the conical morphology of indium when the i_p = 100 *mA/cm*^{2}. Although the surface morphology remained the same within a large range of peak current densities, the cathodic current efficiency started to decrease rapidly when the i_p was greater than 100 *mA/cm*^{2}, as listed in Table 3-3 (page 53). The decrease in cathodic current efficiency also indicated the deterioration of deposit quality. As shown in Figure 3-7 (page 52), the cross sectional analysis conducted by FIB revealed a porous structure when i_p = 500 *mA/cm*^{2}, when the current efficiency was only about 25%. This has suggested that the pulse current density should not exceed 100 *mA/cm*^{2}.



(a) Sample tilt 0^o *(b)* Sample tilt 52^o

Figure 6-2 SEM micrographs of conical morphology of deposited indium by pulse electroplating (i_p = 100 mA/cm^2, i_{avg} = 10 mA/cm^2, t_{on} = 1ms, t_{off} = 9 ms) with sample surfaces tilted: a) 0^o, b) 52^o.

The smoothness of deposited indium was significantly improved by pulse electroplating, and this was confirmed by the measured maximum Total Height of Profile (P_t) and maximum Average Roughness (R_a) (see Table 3-3, page 53). The improvement on surface smoothness is expected due to the significant surface feature refinement through pulse electroplating. As has been stated above, the much higher pulse peak current density can reinforce the formation of new nuclei, thereby continuous growth of the existing large sized features may be hindered due to the periodically applied pulse current, as has been reported for copper electroplating [54].

It should be noted that, for the configuration of the pulse electroplating parameters used here, with the increase of pulse peak current density, the pulse-off time was also extended in order to sustain the constant average current density (Table 3-1, page 47). It has been reported that the pulse-off time may play a role in the electrodeposition process, such as recrystallisation [151-153]. In order to avoid any possible such side-effect of pulse-off time, the pulse current needs to be adjusted in such a way that the amount of charge transmitted within the pulse-on duration remains constant, which can only result in a little change in the pulse-off time. As shown in Figure 6-3, the hatched area of current waveform *1* equals that of the shaded area of waveform *2* so that the increase in pulse current density does not significantly increase the pulse-off time. Due to the data collection limitation of the potentiostat

used in this research, the influence of pulse-off time on the pulse electroplating process could not be investigated in this work.

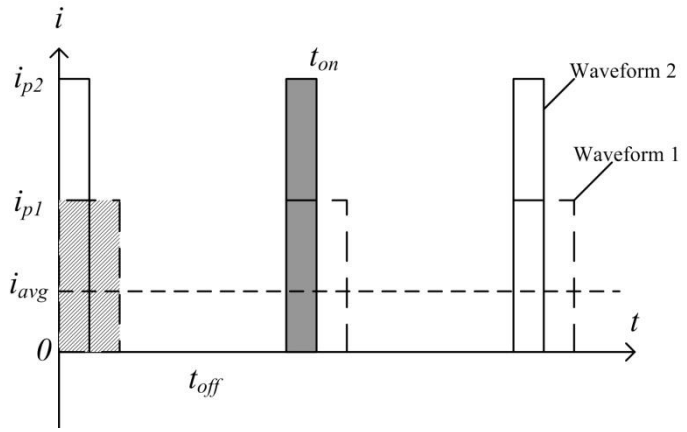
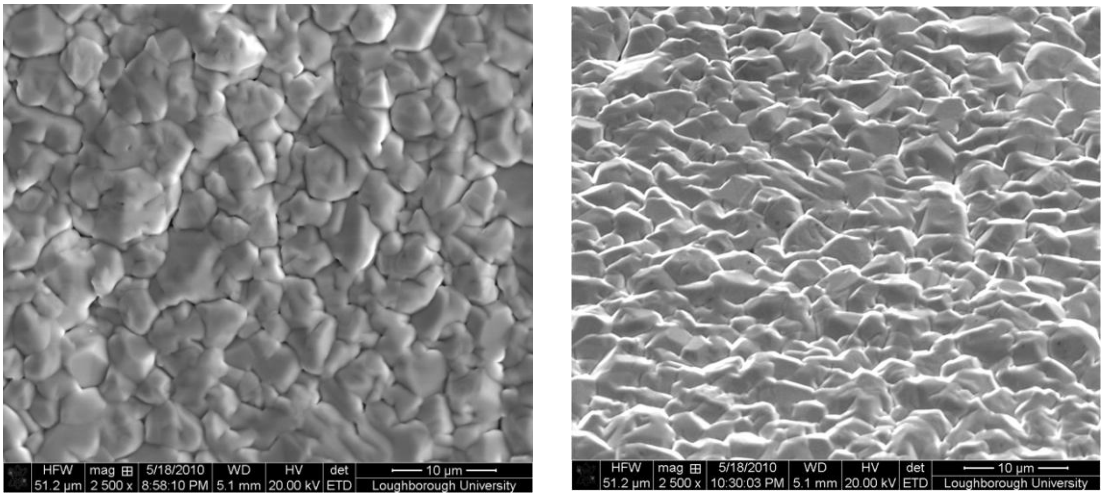


Figure 6-3 Schematic of pulse current waveform configuration to avoid the influence of pulse-off time on the electroplating process: Waveform 1: Low pulse current density with shorter pulse-off time; Waveform 2: Higher pulse current density with slightly longer pulse-off time. i_{p1} is the pulse peak current density of waveform *1* and i_{p2} is the pulse peak current density of waveform *2*.

As can be seen from the results in Chapter 3, the surface morphology of deposited indium through pulse reverse electroplating differed from the unipolar pulse electroplating situation. As predicted by theory, the protruding conical top was preferentially dissolved during the anodic cycle of pulse reverse electroplating [54, 154]. The typical conical morphology in pulse electroplating did not appear in pulse reverse electroplating. Instead, the deposited indium through pulse reverse electroplating was mainly polycrystalline in structure but with finer surface feature size. Figure 6-4 illustrates from different viewing angle the surface morphology of indium electroplated using waveform *No. 13* ($i_{p(c)}$ = 50 *mA/cm*^{2}, $t_{on(c)}$ = 1.5 *ms*; $i_{p(a)}$ = 50 *mA/cm*^{2}, $t_{on(a)}$ = 0.5 *ms*; t_{off} = 3 *ms*.).



(a) Sample tilt 0º *(b)* Sample tilt 52º

Figure 6-4 Surface morphology of pulse reverse electroplated indium viewed from different angles (waveform *No. 13:* $i_{p(c)}$ = 50 *mA/cm*^{2}, $t_{on(c)}$ = 1.5 *ms*; $i_{p(a)}$ = 50 *mA/cm*^{2}, $t_{on(a)}$ = 0.5 *ms*; t_{off} = 3 *ms*.).

In fact, the parameters used in pulse reverse electroplating were selected on the basis of the results obtained from pulse electroplating for the sake of surface uniformity and current efficiency. As generally recommended above, either the cathodic or the anodic pulse current density should not exceed 100 *mA/cm*^{2}. Obviously, the surface feature size of indium through the selected pulse reverse electroplating was significantly reduced compared with DC electroplating (see Figure 3-9, page 55). The reason for surface feature refinement could also be attributed to the improved nucleation rate caused by the very high cathodic pulse current density as observed in the unipolar pulse electroplating.

Similar to pulse electroplating, any changes of electroplating parameters in the cathodic or anodic pulse current density did not have significant influences on the surface morphology for the range of values tested here. As shown in Figure 3-9 (page 55), it was hard to quantify the difference in surface morphology between the deposits obtained through waveform *No. 13* and *No. 14*, where both the cathodic and anodic pulse current densities increased from 50 *mA/cm*^{2} to 100 *mA/cm*^{2}. In addition, comparing waveform *No. 14* and *No. 15*, which reduced the anodic pulse current density from 100 *mA/cm*^{2} to 50 *mA/cm*^{2}, very little difference could be seen between them except that the surface feature size was slightly increased.

The surface smoothness of deposited indium through pulse reverse electroplating was significantly improved in comparison to that obtained by DC electroplating (see Figure 2-9 on page 36 and Figure 3-10 on page 56). On the one hand, similar to pulse electroplating, the enhanced nucleation rate induced by higher pulse current density contributed to surface smoothing. On the other hand, the additional anodic cycle preferentially dissolved the peak sites of existing deposits which resulted in a further levelling effect. However, from the data shown in Table 3-3 (page 53) and Table 3-4 (page 56), the surface roughness of deposited indium through pulse reverse electroplating was very close to that obtained by pulse electroplating, taking waveforms *No. 3* and *No. 13* for example, the R_a was 0.59 μm and 0.6 μm respectively. This can be explained due to the fact that the dissolution of the uneven sites of deposits through the additional anodic cycle was not significant as more metal was deposited during the cathodic cycle in the case of pulse reverse electrodeposition.

6.3 Ultrafine Pitch Indium Bumping Using Sulphamate Solution

6.3.1 Evaluation of Feasibility

The indium bumping process has been successfully developed through electrodeposition using a sulphamate solution and the experimental results have demonstrated that it is able to produce high quality indium bumps with an ultrafine pitch (down to 15 μm diameter and 25 μm pitch size) and with a yield of over 99.9% based on the presence of bumps. The minimum pitch size is determined by the photolithography step, *i.e.* the pitch size can be further reduced as long as the photoresist pattern can be developed to precisely define the aperture openings. For example, Merken and John *et al* [36, 39] deposited indium bumps on a 3 inch wafer using indium chloride solution and the minimum bump size obtained was 7 μm. Due to the limitation of facilities available for this research, the minimum bump size achieved was 15 μm.

Figure 6-5 and Figure 6-6 summarise the bump height uniformity on both the wafer scale and pattern scale through various electroplating parameters used in this research. The pattern scale uniformity in Figure 6-6 was the average value of the

patterns along the two radii of the wafer as indicated in the figure. The experimental results demonstrated that the best uniformity on the 4 inch wafer scale obtained by DC, pulse and pulse reverse electroplating were 19.65%, 14.3% and 13.6% respectively. As mentioned before, there are only two studies of ultrafine pitch indium bumping through electroplating reported in the literature. In the study conducted by Merken and John *et al* [36, 39], on 3 inch wafers in the presence of a current thief ring, a 15% bump uniformity was achieved which was equivalent to the results obtained from this research (see Table 4-4, page 91). Jiang *et al* [38] demonstrated the indium bumping process using sulphamate solution, however, no uniformity study was reported.

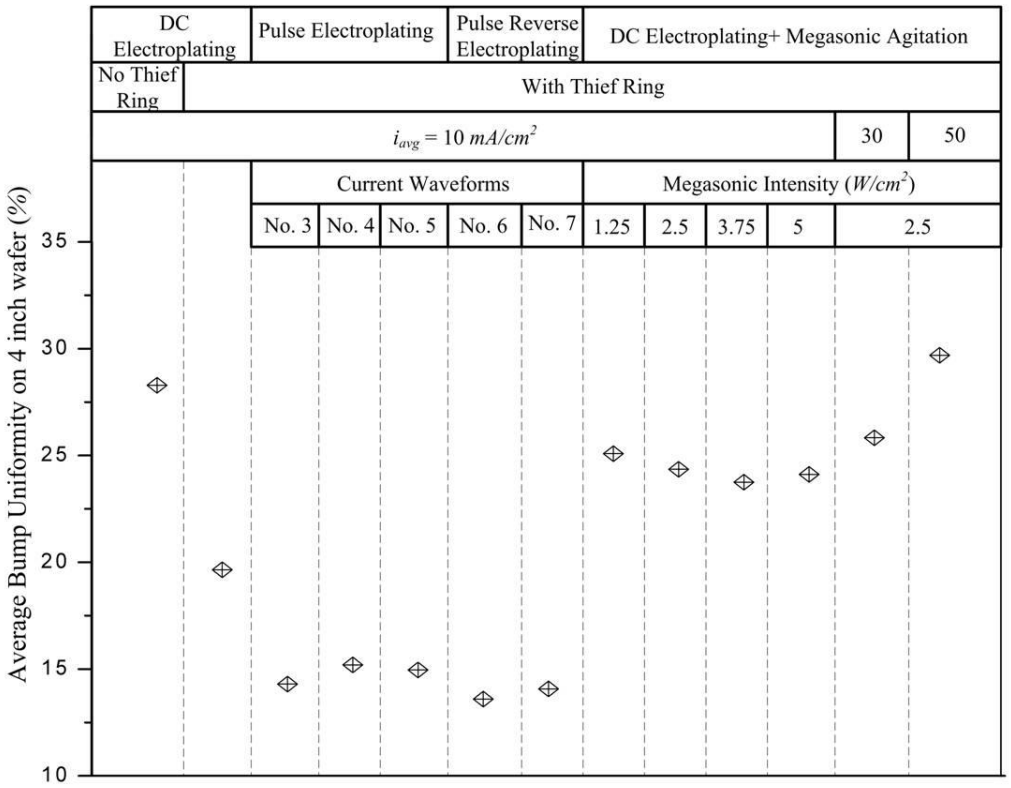


Figure 6-5 Summary of average bump height uniformity on 4 inch wafer scale through various electroplating parameters.

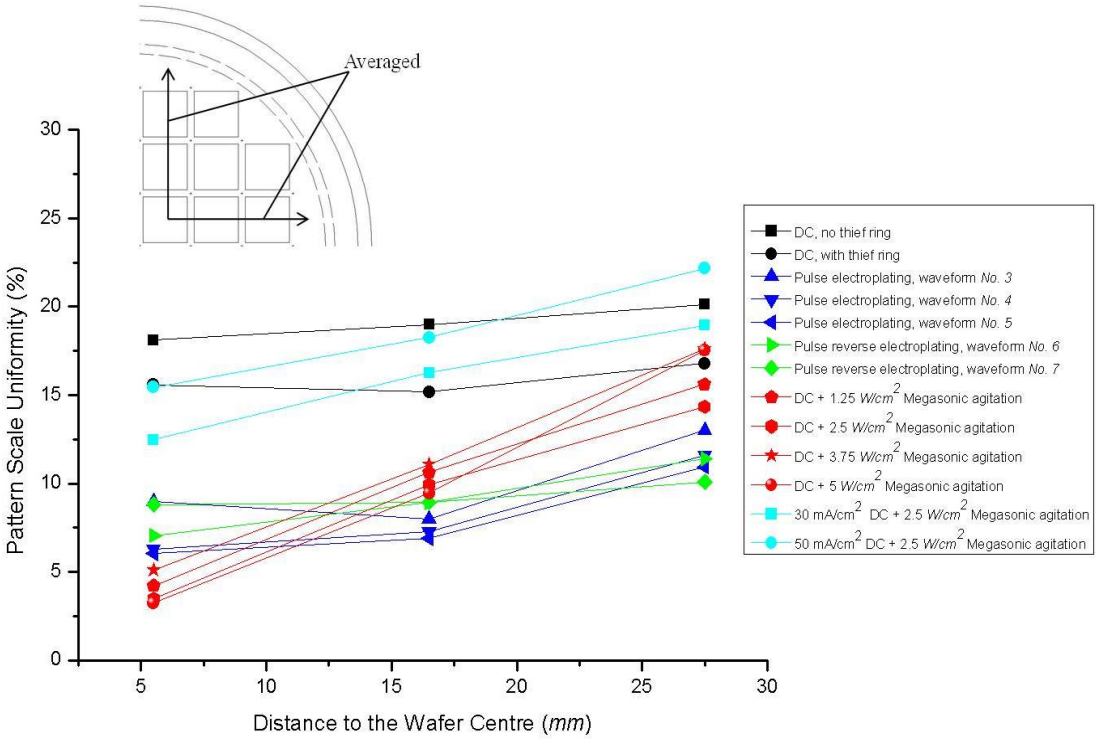


Figure 6-6 Summary of average bump height uniformity on pattern scale through various electroplating parameters.

To achieve a high bumping uniformity, as mentioned before, several factors need to be taken into account in the experiments including seed layer thickness, electrical contact, the presence of current thief, current shield, current density, geometric configuration of photoresist patterns and agitation. The experiments on 3 inch wafers indicated that a smaller current density is favourable in obtaining a better uniformity. The resistance within the thin seed layer is the origin of the terminal effect which remains unchanged during the deposition process resulting in non-uniform bumps across the wafer [110]. In general, the terminal effect will be more profound when the seed layer becomes thinner as the Ohmic resistance of the seed layer is inversely proportional to the thickness [88, 89, 97, 155]. The resistance of the thin film is strongly dependent on the deposition process which was outside the focus of this research. Thus, the seed layers used in this research were prepared in the same E-beam evaporation system using the same parameters to achieve consistent conditions for electroplating to commence.

6.3.2 Effects of Current Thief Ring Design

The electrical contact to the wafer can also physically affect the current density distribution across the wafer. As demonstrated by the bumping uniformity on a 3 inch wafer, where the contact was made through two points on the periphery of the wafer (Figure 4-9*a*, page 73), the electroplated indium bumps showed noticeable directional non-uniformity. Therefore, a symmetrical contact is demanded to achieve better uniformity on the wafer scale, for example, through the 4 inch wafer connection type shown in Figure 4-9*b* (page 73).

A current thief was designed into the wafer pattern configuration and showed improvement on both the wafer scale and pattern scale (see Figure 6-5 and Figure 6-6). It can be seen from the 3 inch wafer bumping experiments, a current thief ring surrounding the entire pattern area can homogenise the directional non-uniformity caused by the asymmetrical electrical contact. Both of the bumping results on the 3 and 4 inch wafer showed that a current thief ring can reduce the current crowding effect induced by the geometric configuration of the electroplating system and therefore improve the bumping uniformity on both the wafer and pattern scale. For example, the bump uniformity on a 4 inch wafer scale was improved from 28.29% to 19.65 in the case of DC electroplating, as illustrated in Figure 6-5, while the pattern scale uniformity was also improved to a noticeable extent (Figure 6-6). The trend of uniformity improvement using a current thief agrees well with the simulation studies conducted by other researchers [96, 100]. A current shield was not utilised in this research because the set-up of the megasonic transducer restricted the space available to adjust the configuration.

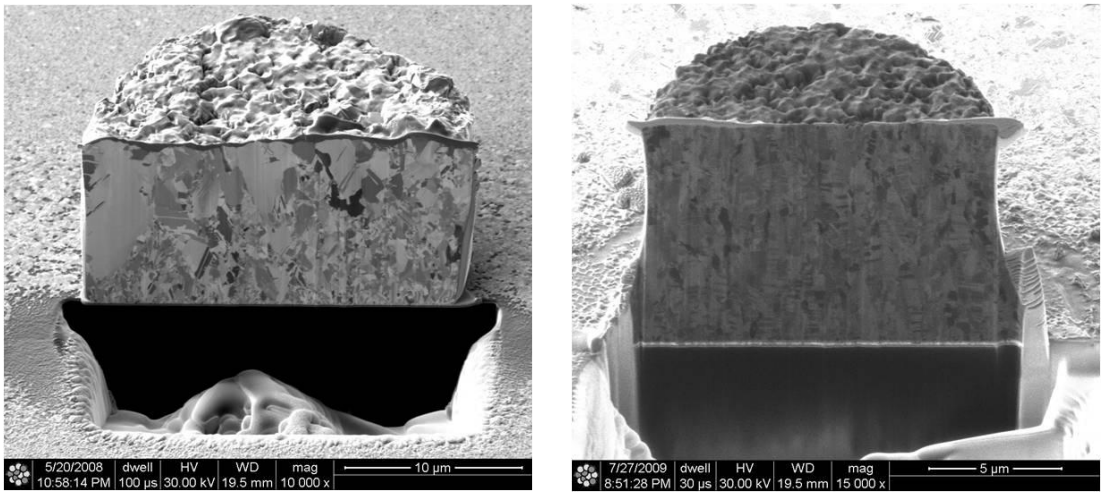
6.3.3 Effects of Pattern Geometric Characteristics

The geometric characteristics of the photoresist pattern play an important role in determining the pattern scale uniformity. As demonstrated in Figure 4-45 (page 112) and Figure 4-46 (page 113), it can be concluded that the decrease in feature size and increase in the pattern vacancy rate (V_p) can both induce an increased indium bump height. Simulation studies from previous researchers also demonstrated similar trends [106-109]. This can provide guidance in designing the photoresist patterns. On the one hand, the pattern design should avoid including features having large differences

in size. On the other hand, if the pattern has large and small features, the latter should not be located near the periphery of the pattern as such an arrangement can deteriorate the uniformity.

6.3.4 Influences of Pulse Electroplating

The unipolar pulse electroplating and bipolar pulse reverse electroplating have demonstrated the improvement in bump height uniformity on both the wafer scale and pattern scale (see Figure 6-5 and Figure 6-6) and the fundamentals of the uniformity improvement will be discussed below. On the feature scale, the uniformity can also be improved using pulse electroplating and pulse reverse electroplating, as shown in Figure 4-35 (page 103) and Figure 4-36 (page 103). The uneven bump profile obtained by DC electroplating indicates the limitation of the two additives on levelling ability. Figure 6-7 shows the profiles of Cu and Au bumps obtained through two commercial solutions designed for electroplating into through-holes or bumping which contain complex additives having a strong levelling effect. In comparison to Figure 4-34*a* (page 102), there is much room for indium sulphamate solution to improve the uniformity on the feature scale by adjusting the organic additives. Relevant studies on new additives in future work would be beneficial to achieve a more uniform growth front.



(a) Cu bump *(b)* Au bump

Figure 6-7 Cross-sectional view of bump profiles obtained from commercial solutions with complex additives having strong levelling ability: (a) Cu bump; (b) Au bump (Courtesy of Dr. David Flynn, Heriot-Watt University).

In order to understand the fundamentals of how the pulsating current waveforms affect the bumping process, investigation of the indium bump growth process was conducted through both DC electroplating (at 10 mA/cm^2) and unipolar pulse electroplating (waveform *No. 3*, i_p = 50 mA/cm^2). Micrographs of the indium bumps were taken at 30 *s*, 120 *s*, 500 *s* and 1000 *s* respectively. As for the bipolar pulse reverse electroplating, because a short period of unipolar pulse electroplating was performed prior to each of the bipolar pulse reverse electroplating trials, the pure influences of bipolar pulse reverse waveform could not be separated from the combination. So, in this section, only the influences of unipolar pulse electroplating on the bumping process were concerned.

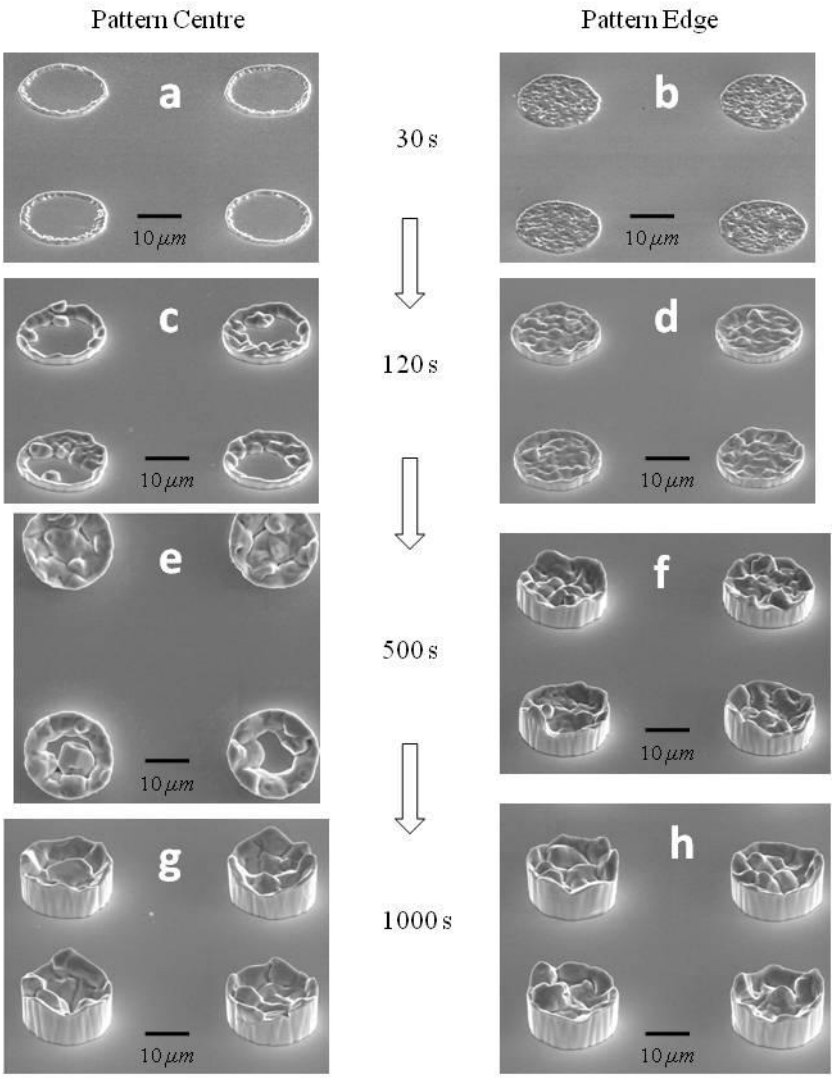


Figure 6-8 Morphology of indium bumps at different stages during DC electroplating at 10 *mA/cm²*.

For the bumping by DC electroplating, when the deposition was performed for 30 s, at the centre of a pattern, only the periphery of the opening areas were covered by indium, as shown in Figure 6-8*a*, forming an indium metal ring rather than a conformal column. However, in the features near the pattern boundary, the whole opening areas were deposited with indium; as can be seen in Figure 6-8*b*, the indium started forming the column shape and growing. This phenomenon was commonly observed in all of the patterns across the wafer, no matter how far the pattern was from the electrical contact. Even after 120 s of electroplating, the indium was not deposited as a column shape at the centre of the pattern (see Figure 6-8*c*), while the bumps near the edge of pattern continuously grew vertically (Figure 6-8*d*). After 500 *s*, in some of the apertures at the centre of the pattern, the aperture opening areas were still not fully covered by indium, as shown in the top view of the indium bumps in Figure 6-8*e*. After 1000 *s*, they were completely covered by indium but the growth front was noticeably uneven (Figure 6-8*g*). Moreover, the electroplated indium bumps near the pattern boundary had profound non-uniformity on the feature scale as well (see Figure 6-8*h*).

In comparison, for the case of pulse electrodeposition, it was found that the entire area of the aperture openings were covered with indium clusters after 30 *s*, as shown in Figure 6-9*a*, even at the centre of the pattern. At the edge of the pattern, more indium clusters were present indicating an uneven current density distribution at the pattern scale (Figure 6-9*b*). With the pulse electroplating progressing, the electroplated indium started to form column shape bumps, as can be seen from the top views of the bumps at the pattern centre and edge (Figure 6-9*c* & *d*). After 500 *s* and 1000 *s*, as shown in different areas in Figure 6-9*e*, *f*, *g* and *h*, the bumps grew more uneven at the feature scale with electroplating time.

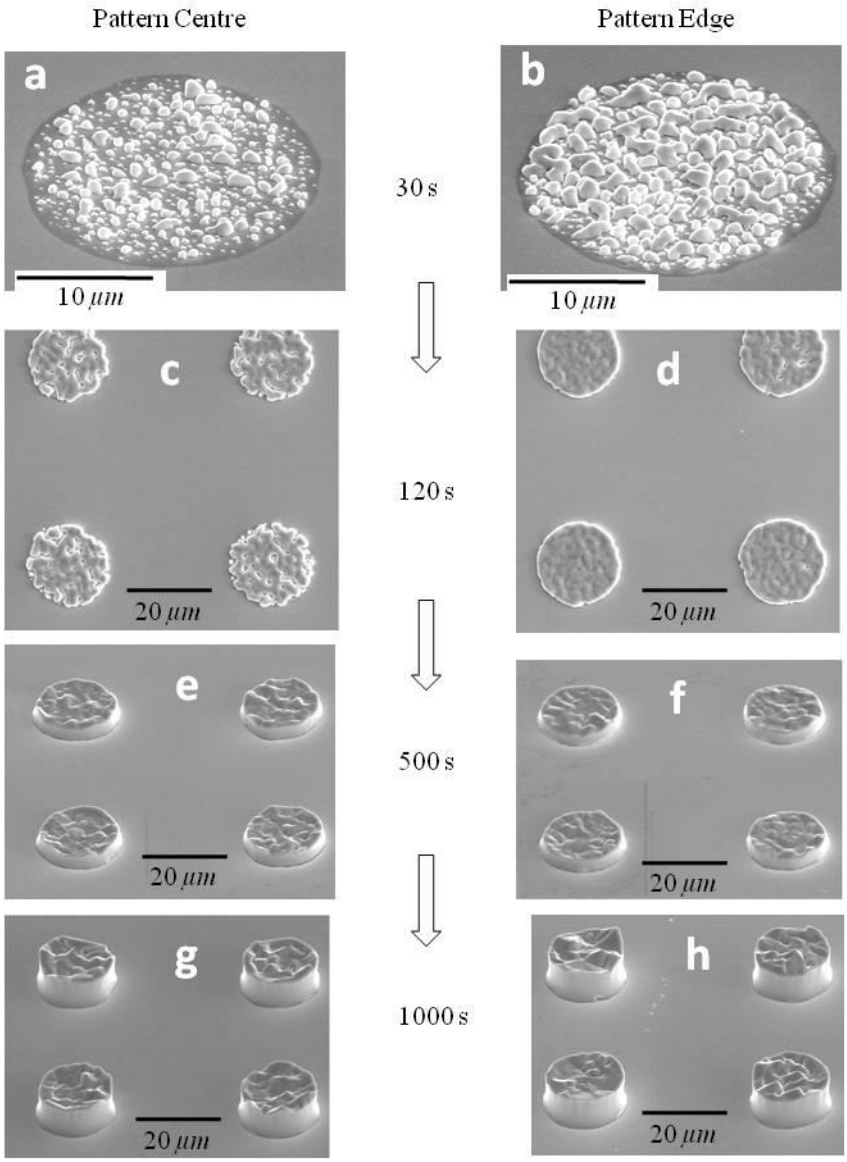


Figure 6-9 Morphology of indium bumps at different stages during pulse electroplating (waveform No. 3, i_p = 50 mA/cm^2, i_{avg} = 10 mA/cm^2, i_{avg} = 10 mA/cm^2, t_{on} = 1ms, t_{off} = 4 ms).

Figure 6-10 plots the bump profiles at the different electroplating stages during the DC and pulse electroplating processes. It is clearly seen that the indium grows more uniformly at the feature scale through pulse electroplating. The uneven growth through DC electroplating occurred from its very initial stage of deposition. The uniformity at both the wafer and pattern scale at different time were measured and the bump uniformity at both wafer and pattern scale are plotted in Figure 6-11. Here, the pattern scale uniformity was measured in pattern P_{11} (see Figure 4-40, page 107). In the case of DC electroplating, the deposition is extremely non-uniform across

the wafer at the beginning stage (Figure 6-11*a*). The uniformity of pulse electroplated bumps is improved on both the wafer scale and pattern scale all through the electroplating process (Figure 6-11*b*), in comparison to DC electroplating. Interestingly, when the electroplating was performed for 500 *s*, the bumps generated by both DC and pulse electroplating achieved the highest uniformity at both wafer and pattern scale. It still remains unclear what the causes for this occurrence from current study are.

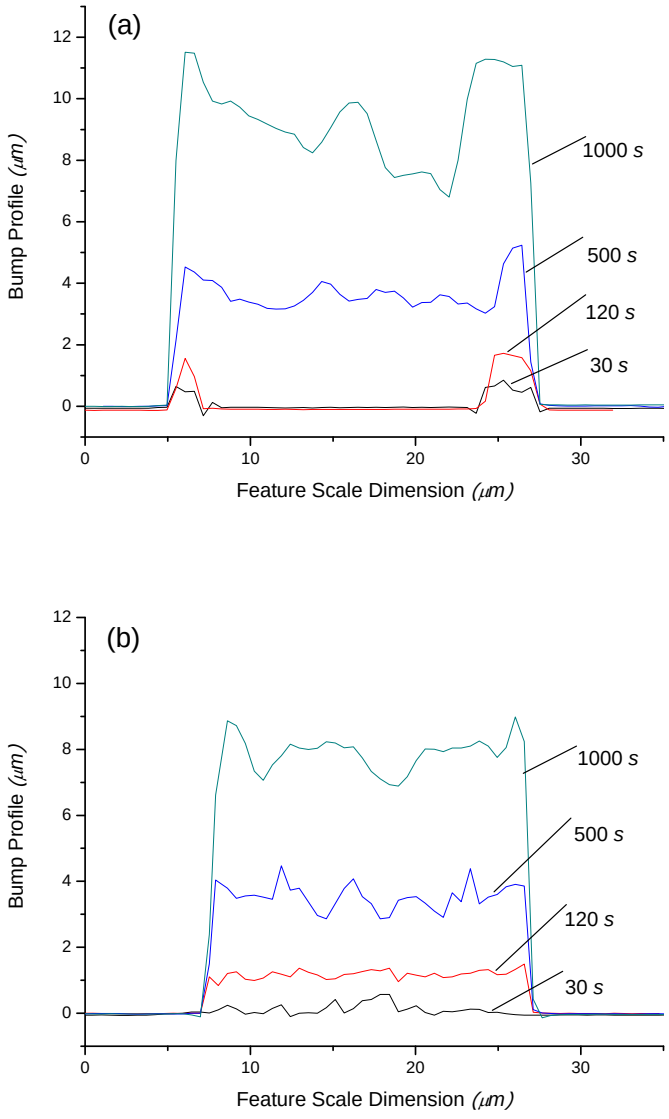


Figure 6-10 Indium bump growth process (at the centre of pattern) through: (a) DC electroplating at 10 mA/cm^2; (b) pulse electroplating, i_p = 50 mA/cm^2, i_{avg} = 10 mA/cm^2, t_{on} = 1*ms*, t_{off} = 4 *ms*.

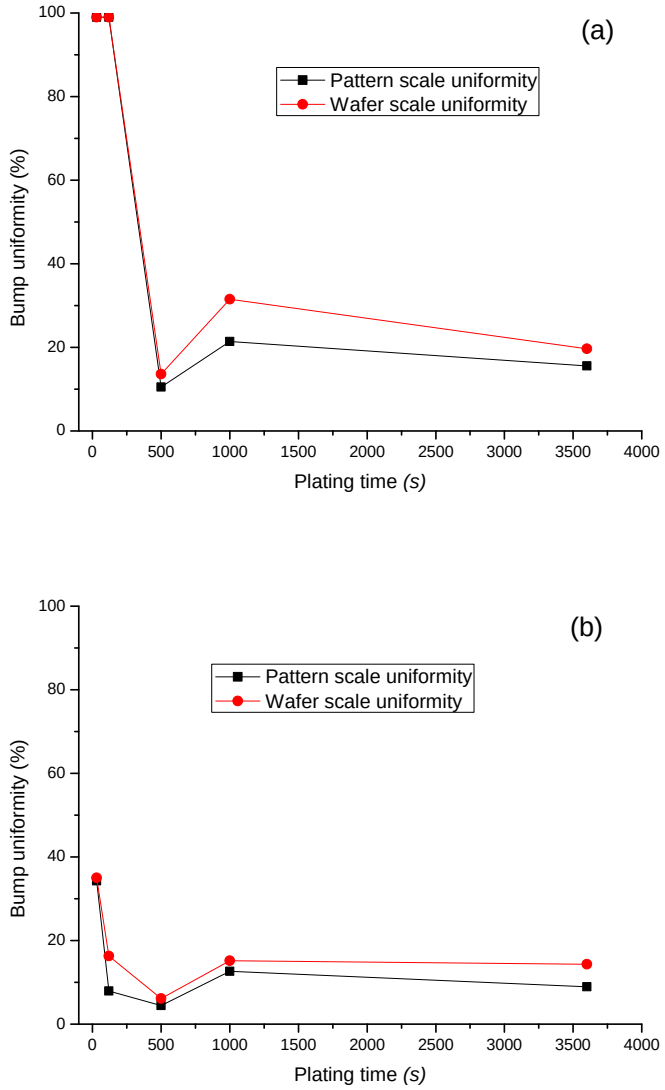


Figure 6-11 Uniformity versus time of electroplated indium bumps at both wafer and pattern scale: (a) DC electroplating at 10 *mA/cm*^{2}; (b) pulse electroplating, i_p = 50 *mA/cm*^{2}, i_{avg} = 10 *mA/cm*^{2}, t_{on} = 1*ms*, t_{off} = 4 *ms*.

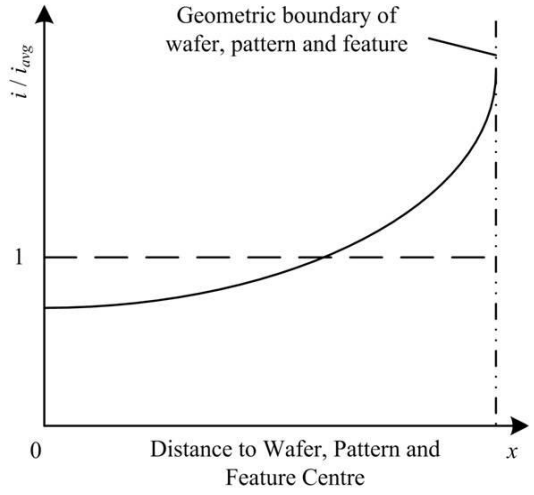


Figure 6-12 Schematic of current density distribution at wafer, pattern and feature scales.

To explain the above findings, the current distribution at the wafer, pattern and feature scale has been simulated by other researchers on the basis of a hierarchic model (see Figure 4-2, page 63). The current crowding at the geometrical periphery of the wafer, pattern and feature has been widely reported [65, 91-94, 106, 107, 111, 155]. As illustrated in Figure 6-12, at the pattern scale, the current density is higher at the edge of the pattern but lower at the centre resulting in a higher deposition rate near the periphery of the pattern. Similarly, at the feature scale, the current concentrates along the periphery of each aperture confined by photoresist.

The possible reason for the incomplete electroplated indium bumps in the pattern centre can be explained by the uneven overpotential induced due to the current crowding effect. At the initial stage of DC electroplating, for the apertures at the centre of a pattern, the current is highly concentrated along the periphery of the apertures due to the current crowding. This exhibited an extreme effect such that the nucleation at the central area of the aperture openings was prohibited due to a much lower local overpotential which is unable to overcome the energy required for nucleation, as illustrated in Figure 6-13. Consequently, this resulted in uncovered central areas of the apertures with the indium significantly and preferentially deposited around the periphery forming a 'ring' of deposit as seen in Figure 6-8*a* & *c*. Such growth phenomena as a result of preferential nucleation at the early stage of electroplating onto a resistive substrate has shown excellent agreement with the findings on copper electrodeposition reported by Willey [156], which also concluded

that the non-uniform nucleation was induced by an uneven potential field. Evidence of this was also found in the transitional area within a pattern: as shown in Figure 6-14, after electroplating with DC at 10 mA/cm^2 for 30 s, between the pattern centre and boundary, the feature area in the transitional area was partially electroplated. Due to current crowding at the pattern scale, the features near the edge of the pattern experienced a higher overpotential and this enabled them to nucleate and electroplate across the entire aperture, although still showing preferential electroplating around the periphery of the apertures due to feature scale current crowding. This phenomenon has not been reported previously.

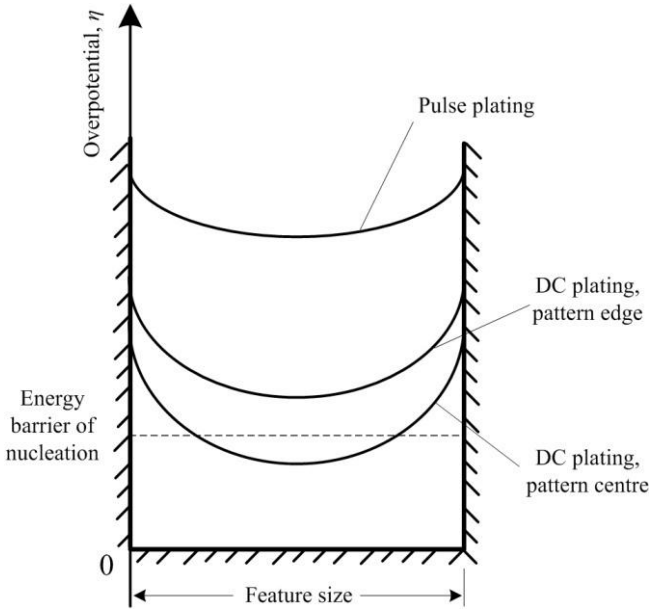


Figure 6-13 Schematic diagram of feature scale overpotential distribution caused by the current crowding under DC and pulse electroplating conditions.

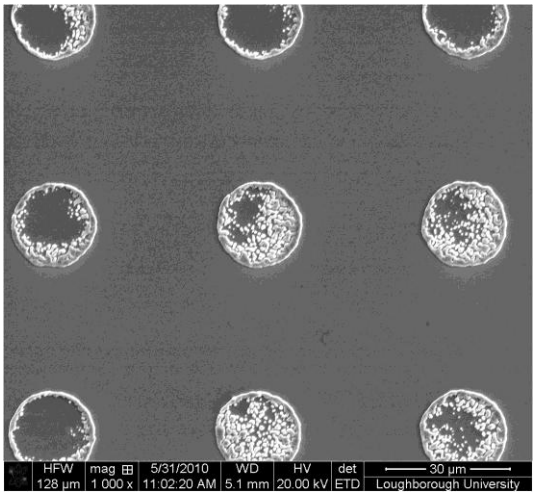


Figure 6-14 DC electroplated indium at 10 *mA/cm*^{2} in the transitional area within a pattern

The nucleation and growth process for pulse electroplating shown in Figure 6-9 (page 174) could be explained from the following two aspects. First, in comparison to DC electroplating, the overpotential induced by the pulse current was much higher, as illustrated in Figure 6-13, and the difference in the nucleation rate at the feature scale from the centre to edge of an aperture was therefore not so pronounced. In addition, according to Equation 6-1, the nucleation rate is significantly improved as the pulse current density is much higher than that in the DC electroplating, which has led to a significant refinement in the microstructure of deposits by pulse electroplating, as has been reported in the literature. Secondly, as shown in Figure 3-3 (page 41), a thinner pulsating diffusion layer is usually established during pulse electroplating and the mass transport within an aperture can therefore be significantly improved resulting in a uniform deposition across the aperture openings. This has agreed very well with a previous study by Kim [65], who has reported that more uniform bump shape can be achieved using pulse electrodeposition in a Sn/Cu electroplating bath. Thus, the front of indium bump deposits in pulse electroplating grew more evenly compared to that in DC electroplating (Figure 6-10), which agrees with the surface smoothing effect as has been observed in the electrodeposition of indium onto a non-patterned plain substrate (see Figure 2-9 on page 36, Figure 3-8 on page 54 and Figure 3-10 on page 56). The non-uniformity at the wafer and pattern scale, *i.e.* higher bumps at the wafer/pattern edge than the centre, were still noticeable with pulse electroplating, but was much less pronounced.

The previous experimental results revealed that the grain size within the indium bump obtained by DC electroplating can still reach up to 10 μm, which was of the same order as the indium electrodeposited onto non-patterned plain substrates. However, using pulse electroplating and pulse reverse electroplating, the surface feature refinement was observed but only to a certain extent. During the bump growth in DC electroplating, a disruptive change of morphology occurred after a certain period of electroplating. As shown in Figure 6-15, after 500 *s* electroplating, some relatively large crystals of deposited indium appeared with certain preferential orientations, which stood out from the even base that was formed at the initial stage. In Figure 6-16, the cross-section view of these bumps provides the microstructural characteristics which can clearly reveal the bump growth process. Two distinct layers can be seen (see the red circles in Figure 6-16), both of which are composed of pure indium, as has been analysed with EDX previously (Figure 4-34*b*, page 102).

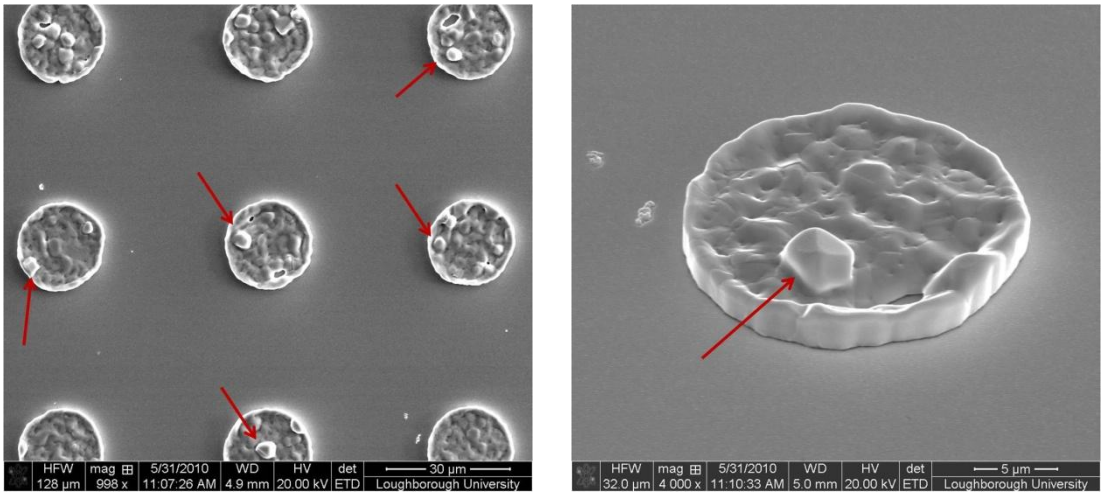


Figure 6-15 Large sized grains formed at 500 *s* during DC electroplating bumping at 10 mA/cm^2.

The crystal lattice structure of indium is tetragonal, and copper is face-centred cubic (FCC) (Figure 6-17). In general, at the beginning of electroplating, the electrodeposited indium metal may be initiated by conforming with the crystal structure of the copper substrate to form the initial sets of nuclei followed by subsequent growth, which is usually known as epitaxial growth [41]. The electrodeposited indium may be distorted to follow FCC lattice structure of copper instead of its original state as a tetragonal crystal at the very initial stage of

electrochemical crystallisation (Figure 6-18). However, it was found that the thickness of the initial layer could reach around 0.5 μm which was beyond the normal range of epitaxial growth and it was unlikely to form such a thick initial layer following the lattice structure of copper substrate. Nevertheless, the difference in lattice constants between the two metals inevitably causes a noticeable internal stress within the deposited indium, which can initially be accumulated by the deformation of the indium due to its low strength. After a certain degree of deformation in the deposition, the strained tetragonal lattices will no longer permit any further distortion to accommodate the accumulated inner stresses. Therefore, the deposit fissured at certain stage as observed in Figure 6-16. This can be attributed to the internal stresses accumulated in the indium that has exceeded the limit of its strength. With the progress of electroplating, the electrodeposited indium can no longer form as a distorted tetragonal structure, and therefore starts to grow as a normal tetragonal crystal. The indium nucleated as a tetragonal layer can then preferentially grow up as it requires less energy for indium ions to incorporate into it. Considering the relatively small feature size (~ 20 μm), such large tetragonal crystals (see Figure 6-15) can be more easily accessed by the flux of reacting species from the electroplating solution, thereby continuous growth of the larger grains is preferred rather than the formation of new nuclei (Figure 6-19). Thus, an indium bump often only contains a few grains which can reach as large as 10 μm as revealed in the situation of electrodeposition onto non-patterned substrates.

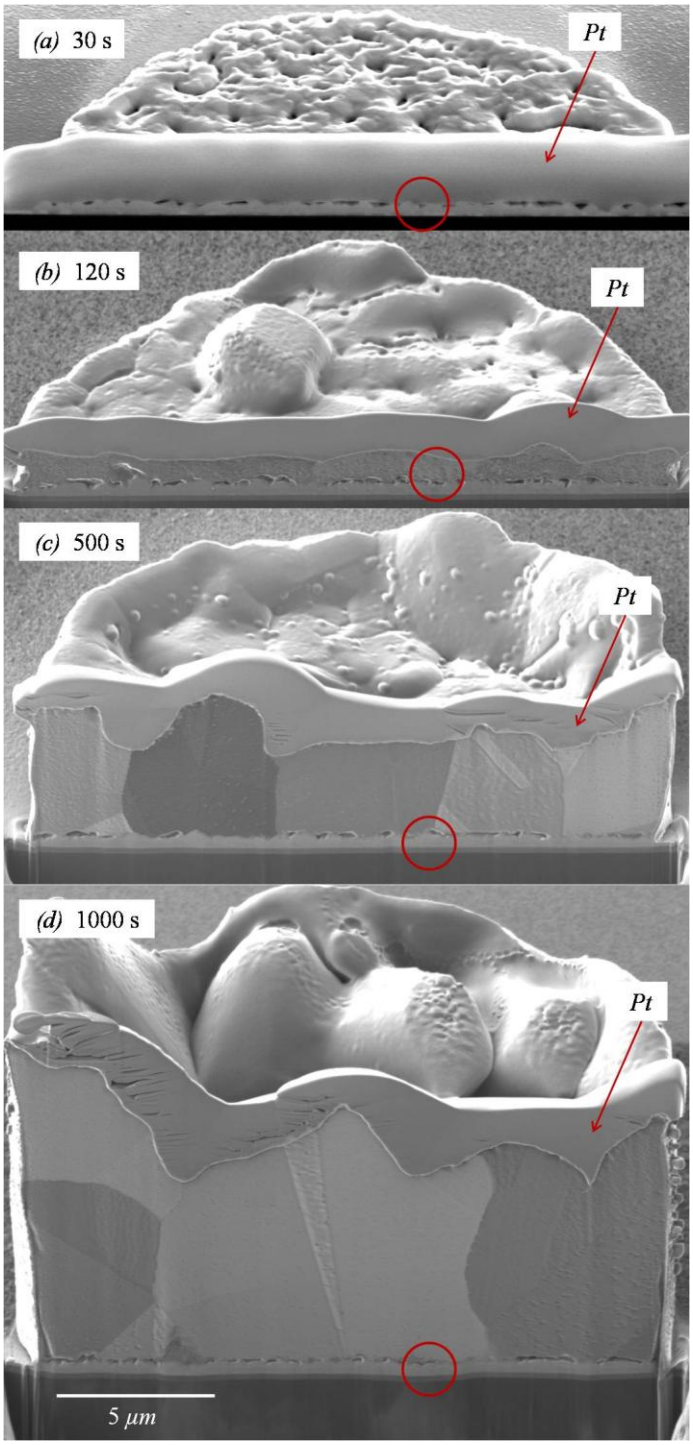
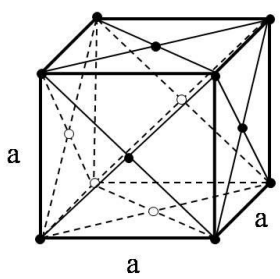
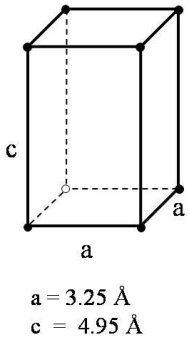


Figure 6-16 Cross sectional views of indium bumps at different stages of deposition at DC 10 *mA/cm*^{2}.



(a) Copper, face-centred cubic



(b) Indium, tetragonal

Figure 6-17 Crystal lattice structure of: (a) copper; and (b) indium.

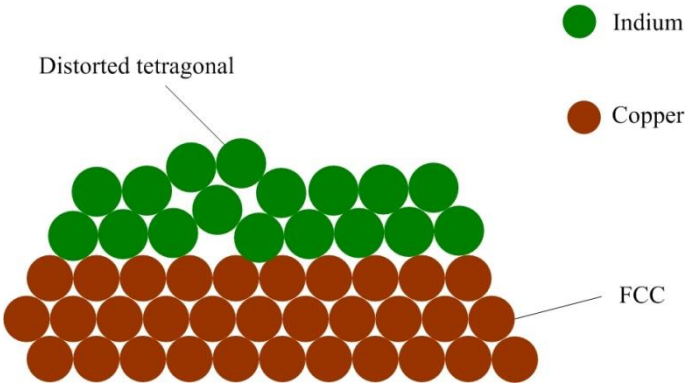


Figure 6-18 Distortion of indium lattice at the initial stage of electroplating onto copper substrate.

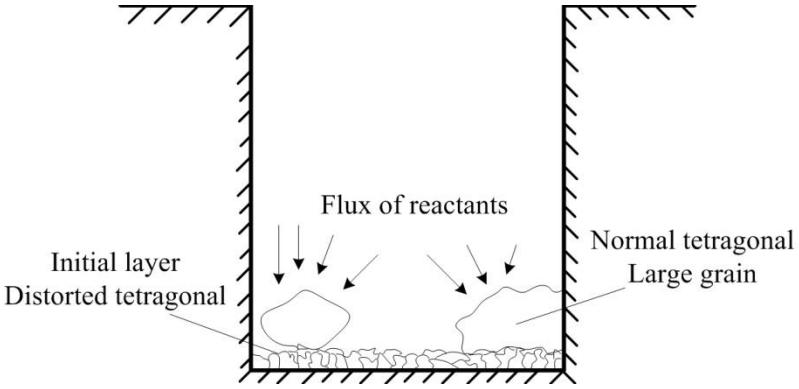


Figure 6-19 Preferential electrodeposition within the feature scale resulting in large grains.

Cross-sectional views of the microstructure of indium bumps at different stages of pulse electroplating given in Figure 6-20, also consist of two layers, with each having different morphology similar to the DC electroplating. With the progress

of electroplating, the grain size under both DC and pulse electroplating conditions reached and finished at an equivalent order. Similar evidence for such a phenomenon can be found by comparing Figure 4-34 (page 102), Figure 4-35 (page 103), Figure 6-16 and Figure 6-20. This can be attributed to recrystallisation during the electroplating process, as has been reported in other electroplating systems, which has concluded that recrystallisation occurred simultaneously during the electroplating of copper column bumps at room temperature [157]. Many other studies also confirmed this, but termed it as self-annealing of electroplated metals (*e.g.* copper) that can take place during the pulse-off period in pulse electrodeposition [56, 158, 159]. Because indium has a relatively low melting point (*i.e.*156 ºC), it is extreme likely for indium to undergo a recrystallisation at room temperature in the course of and after electroplating.

Based on the above discussion, the bump growth mechanism in DC and pulse electroplating are proposed as follows. For the DC electroplating, as illustrated in Figure 6-21*a* and *c*, in the pattern centre, the entire aperture area cannot be completely covered by indium nuclei at the early stage due to the uneven potential field induced by the current crowding (Figure 6-13). In the pattern edge, the aperture area can be covered by indium and starts to build up columnar bumps (Figure 6-21*b* and *d*). The initial layer of indium is deposited as distorted tetragonal resulting in a disruptive layer in the cross section view. After a certain stage, indium starts to be deposited as the normal tetragonal structure leaving noticeable large grains in the aperture. For pulse electroplating, as illustrated in Figure 6-22*a*, at the beginning stage, indium nucleation occurs evenly across the entire aperture area due to the high pulse current density. The initial layer of indium is also deposited with a distorted lattice resulting in the disruptive layer in cross-section as well (Figure 6-20). Because the nucleation rate is much higher than DC electroplating, the growth front of the indium bump is populated by smaller nuclei which can form larger grains due to recrystallisation in the course of and after electroplating (Figure 6-22*c* and *d*).

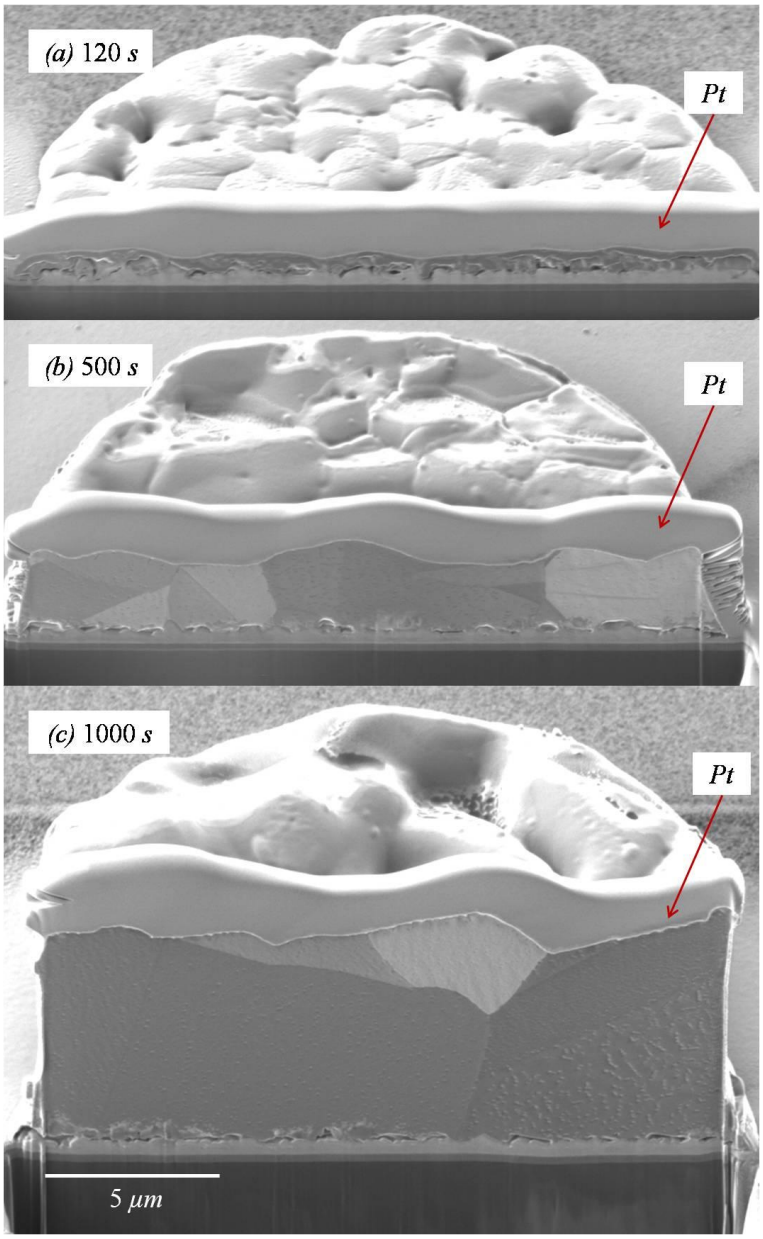


Figure 6-20 Cross-sectional views of pulse electroplated indium bumps at different stages.

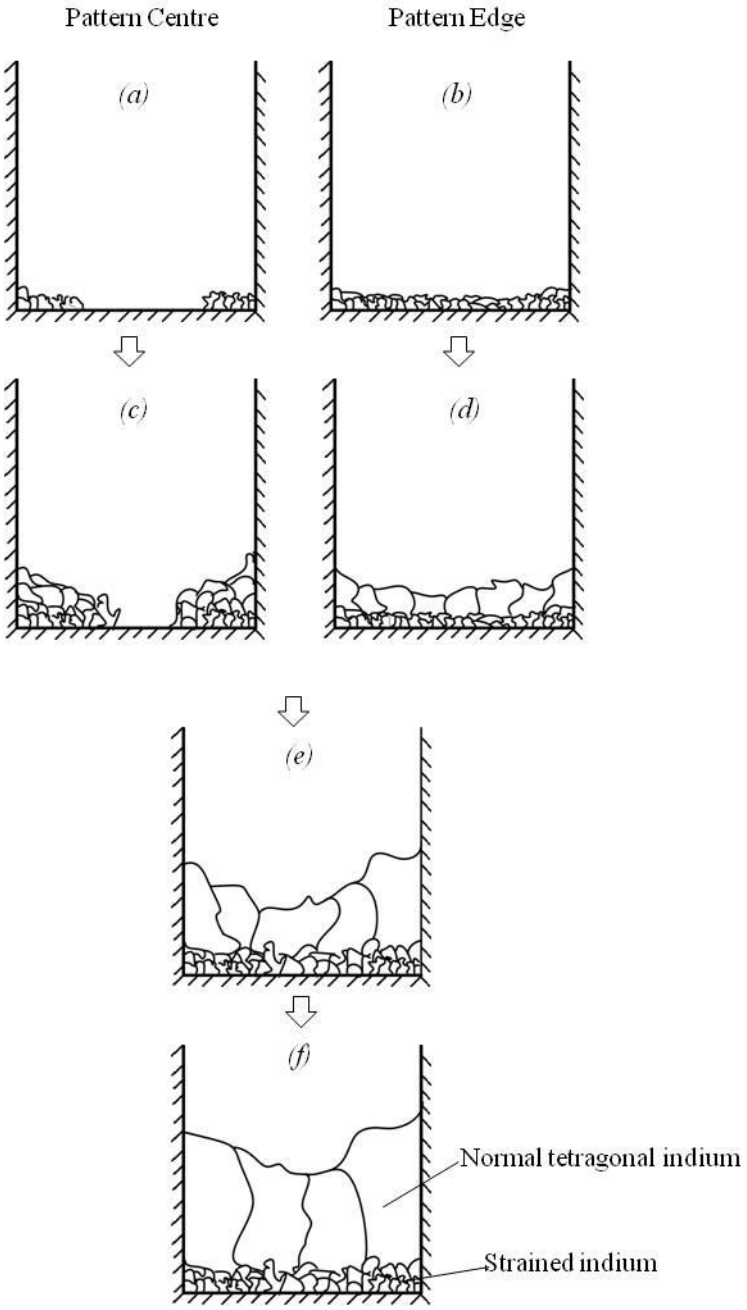


Figure 6-21 Schematic flow of the indium bump growth in the photoresist aperture by DC electroplating in different areas.

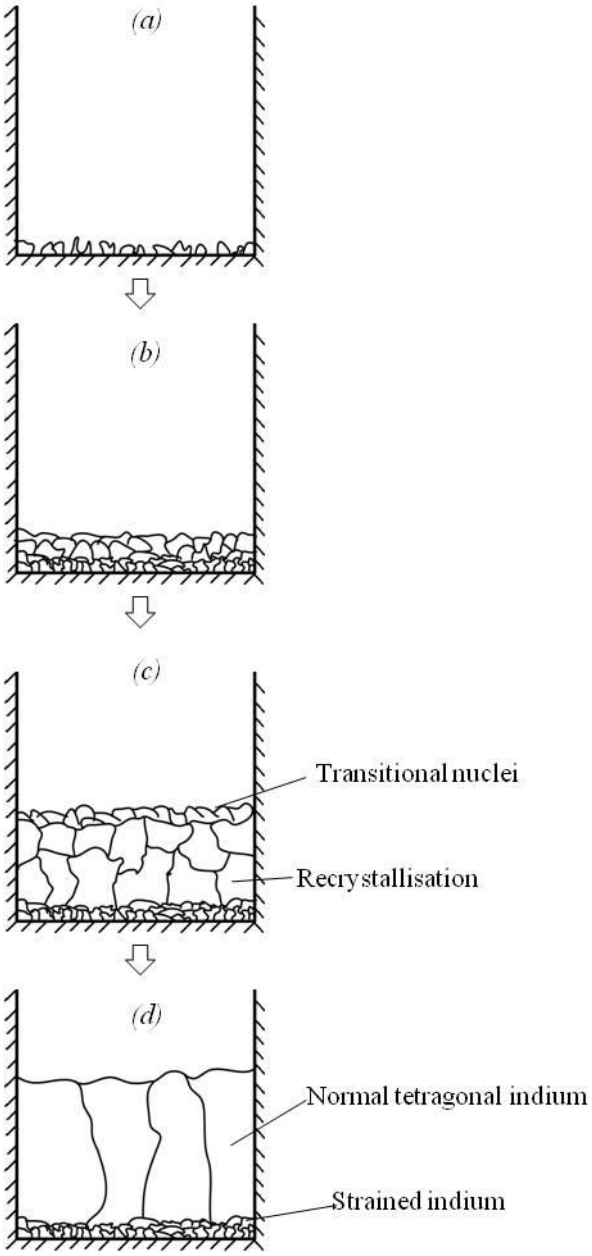


Figure 6-22 Schematic flow of indium bump growth in photoresist aperture during pulse electroplating

6.3.5 Effects of Acoustic Agitation

The influence of agitation on the electroplating process is more pronounced under higher current densities. As shown in Figure 6-5 and Figure 6-6, with DC electroplating, by using megasonic agitation, indium bumps can be electrodeposited 5

times faster than without agitation. However, the bump uniformity deteriorates when the current density increases. The results of bumping on 3 inch wafers also indicated that a smaller current density is favourable for better uniformity (Figure 4-21 on page 86 and Figure 4-22 on page 88). A similar phenomenon was also found by Merken in the study of indium bumping using electroplating from indium chloride solution [39].

Because of the powerful ultrasonic cavitation effect, the fragile photoresist patterns can be damaged by introducing the ultrasonic agitation into the electroplating process. The damage on the *AZ 9260* photoresist was observed on the samples prepared following the procedures listed in Table 4-1 (page 69). However, it is likely to be a risk for other types of photoresist employed in microelectronics applications, as damage to surfaces is commonly observed in the applications of lower frequency ultrasonic agitation, for example, material loss has been reported on ceramic surfaces after exposure to 20 *kHz* ultrasound in DI water for 60 minutes [160]. So, it is not recommended to use low frequency ultrasonic agitation all through the process of electroplating through photoresist patterns. In the results shown in Chapter 4, a high yield can be achieved by pre-wetting the photoresist patterns using ultrasonic agitation. The photoresist can survive if the ultrasound is only applied for a very short period, *i.e.* 5 seconds in the experiments.

Megasonic agitation was applied all through the electroplating process (maximum electroplating time was 60 minutes) but no damage was observed on the *AZ 9260* photoresist. As introduced in Chapter 5, because the threshold of the cavitation bubble formation and collapse increases exponentially with the acoustic frequency, it is unlikely to form cavitation bubbles when the 1 *MHz* megasonic energy is applied into the solution [124]. Therefore, it is unlikely for the photoresist to experience the rigorous liquid jet and high temperature induced by the cavitation bubble. Megasonic agitation has little effect on the fragile photoresist in most applications using megasonic cleaning, the megasonic energy shows no harm to fragile components embedded in the wafer [129, 130]. So, to reduce the risk of damage to the sample, it is suggested to pre-wet the ultrafine pitch photoresist patterns with high frequency megasonic agitation rather than ultrasonic agitation where possible.

Because the photoresist was partially damaged by the ultrasonic agitation, there was no need to evaluate the uniformity of the indium bumps as the yield was not acceptable. In the presence of megasonic agitation there were no yield issues, but the

electroplated bumps still remained uneven on the feature scale (Figure 5-28, page 152). In the patterns near the central area of the wafer, *i.e.* the shaded patterns in Figure 4-40*b* (page 107), the bump height uniformity was significantly improved on the pattern scale, as shown in Figure 6-6. However, the pattern scale uniformity deteriorated in the periphery patterns and the largest bump height was obtained in the area *A* shown in Figure 6-23. Also, it was found that the bumps were heavily over-electroplated and even bridged near the outer corner of the periphery patterns. On the wafer scale, the electroplated indium was less uniform in comparison to the DC electroplating without additional agitation, and the non-uniformity was mainly attributed to the large bumps in the periphery patterns.

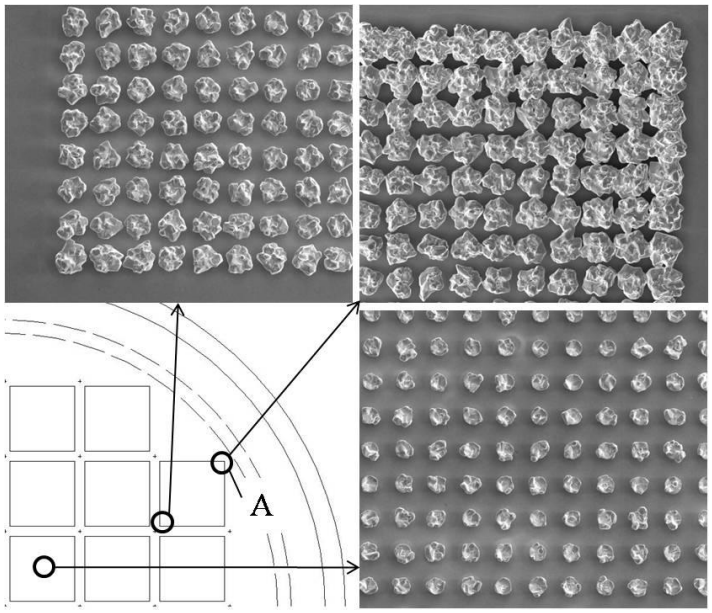


Figure 6-23 Over-electroplated indium bumps on different areas of the 4 inch wafer in the presence of megasonic agitation.

On the one hand, because of the geometric configuration of the electroplating system in all of the experiments, the current crowding effect inevitably occurred along the boundary of periphery patterns on the wafer scale. The improved mass transport by megasonic agitation emphasised the importance of the primary current distribution on the wafer scale. As discussed above, the advantage of megasonic agitation is to improve the mass transport and to reduce the concentration overpotential. Thus, when the current density becomes larger, the influences of megasonic agitation on

electroplating will be more pronounced. A good demonstration can be taken from the reduction of cathodic potential in the case of electroplating through different current densities, as shown in Figure 5-20 (page 146). Due to the terminal effect, for a certain point on the wafer, the local potential is inversely proportional to the distance between the point and the wafer edge. Thus, the current density is much higher near the wafer edge than in the wafer centre, and the current density defined by the power supply is actually an averaged value across the wafer. When the megasonic agitation is applied, the mass transport is significantly improved and the higher potential near the wafer edge can induce higher current density and therefore faster deposition.

According to Equation 5-1 (page 124), the Nernst diffusion boundary layer has no relation to the acoustic intensity. However, an increase in intensity can induce an increase in the number of bubbles in the liquid [124]. Also, the increase in intensity can increase the probability for the bubbles to collapse, *i.e.* the probability for acoustic cavitation effect to prevail. Therefore, the risk of damage to photoresist will also increase with the intensity. The defects on the bump sidewall shown in Figure 5-27 (page 151) can be attributed to the air bubbles reinforced by the higher megasonic intensity. Due to the high current efficiency (> 90%), it is unlikely for the side-reaction (*e.g.* hydrogen evolution) to occur. So, with the increased megasonic intensity, air bubbles are formed in the bulk solution and possibly pushed into the aperture, or formed in the aperture and stick to the inner wall leading to electroplating defects. Based on the experimental results, it is suggested to apply the megasonic agitation for wafer bumping with intensity no greater than 2.5 W/cm^2.

Indium deposition onto plain substrates and patterned wafers through high current densities, which were beyond the limiting value in the absence of agitation, were also conducted with the assistance of megasonic agitation in this research. Usually, high speed electrodeposition can be realised by increasing the ion concentration and adding proper additives into the solution [161-163]. This study demonstrates a new approach to achieve high deposition rate by using megasonic agitation. For the indium bumping through very high current density, because of the photoresist patterns, the transmission angle that the megasonic energy propagates into the aperture plays an important role to achieve high current efficiency and yield. Based on the results, it is suggested to tilt the megasonic transducer to a larger transmission angle against the wafer. In this research, high quality indium bumps with ultra-fine pitch and high yield were successfully obtained through extremely high

current density, *i.e.* the deposition rate can be 5 times faster in comparison to the DC electroplating at 10 mA/cm^2. This indicated the feasibility of high speed bumping process by using megasonic agitation. However, the issue of bump uniformity became more serious under very high current density (Figure 5-33, page 157). As discussed above, approaches including novel current thief, current shield, pulse electroplating and pulse reverse electroplating may be beneficial in pursuing high speed bumping with a better uniformity.

6.4 Summary and Issues for the Scaling up of the Indium Bumping Process

In summary, based on the experimental results and above discussion, better bumping uniformity on wafer scale and pattern scale can be achieved by using a current thief ring, reducing current density, and using pulse electroplating or pulse reverse electroplating. The best bump height uniformity on the 4 inch wafer scale achieved was 13.6% by using pulse reverse electroplating (i_{avg} = 10 mA/cm^2) in a pattern that included a thief ring design. The feature scale uniformity can also be improved by using pulse electroplating and pulse reverse electroplating. Acoustic agitation is capable of pre-wetting the ultrafine pitch photoresist patterns leading to a very high bumping yield, more than 99.9% yield has been continuously achieved. When the current density is relatively low, megasonic agitation can improve the pattern scale uniformity while the wafer scale uniformity slightly deteriorates. Moreover, by using megasonic agitation, indium bumping can be realised at higher deposition rates without any other modification of the electroplating system.

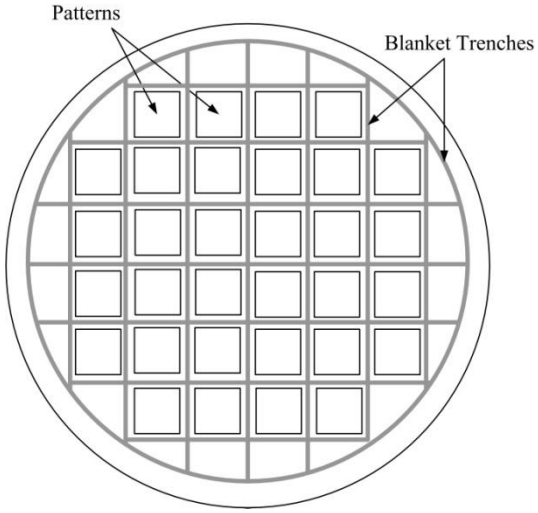


Figure 6-24 Proposed layout of current thief surrounding each patterns.

The results in this research have shown that, by using DC electroplating with a current thief ring, the uniformity deteriorates from about 16% to about 20% when the electroplating process is transferred from a 3 inch wafer to a 4 inch wafer. To scale up the process for industrial manufacture, *e.g.* electroplating bumping onto 6 or 8 inch wafers, the uniformity issue will be more serious. At this stage, the detailed relationship between uniformity and wafer size is not known and depends on several parameters, so it is not possible to predict accurately how this will change with increased wafer diameter. The terminal effect induced by the resistive seed layer will be more pronounced because the enlarged wafer can physically increase the Ohmic resistance within the seed layer leading to a larger potential drop between the edge and the centre of the wafer. Also, the geometric characteristics of the electroplating system need to be configured to adjust the primary current distribution on the wafer scale because the current crowding effect can play a significant role in determining the bumping uniformity.

To improve the bumping uniformity in a scaled-up electroplating system, several approaches are proposed according to the results of this research. First, a current thief ring surrounding the entire pattern area, like the layout shown in Appendix 2, would be helpful to reduce the current crowding effect near the wafer edge. During the electroplating of the 3 inch wafers it was noted that the addition of a thief ring also helped extend the electrical contact around the periphery of the wafer, especially as it became thicker during electroplating. Extending this idea further, a

new layout of current thief is proposed as shown in Figure 6-24. In this example, each of the patterns is surrounded by current thief lines that will function as a more conductive current path when the deposit is built up. Using this approach, the terminal effect caused by the resistance within the seed layer and the current non-uniformity on both the wafer and pattern scale can potentially be improved and could assist in improving the quality of electroplating on larger wafers. Further investigation of this is needed and the extra material cost of the thief area and loss of chip area should be considered. A proper current shield corresponding to a specific photoresist pattern layout can be a good way to improve the bumping uniformity. As the megasonic transducer used in the electroplating bath restricted the space available, it was not possible to incorporate a current shield in this research, however, it has been proved as an effective method by other researchers [95-97]. The results in this research have demonstrated that pulse electroplating and pulse reverse electroplating can significantly improve the bumping uniformity at wafer, pattern and feature scale and should also be beneficial in electroplating onto larger wafers. Finally, considering the investment cost of the high frequency power unit, additives having a stronger levelling effect can be an alternative approach to improve the feature scale uniformity.

Chapter 7 Conclusions and Future Work

7.1 Thesis Conclusions

In this thesis, electroplating of indium bumps for ultrafine pitch interconnection has been successfully developed through intensive experimental studies. It is the first systematic investigation of ultrafine pitch indium bump formation through electrodeposition using a sulphamate solution. Because there was very limited information about indium electrodeposition using sulphamate solution available in the literature, investigation of the electrochemical performance of the solution was carried out prior to the indium bump deposition. The microscopic characteristics of electrodeposited indium through various current waveforms, *i.e.* direct current, unipolar pulse current and bipolar pulse reverse current, were first investigated on the basis of plain substrates. After this, two main factors, current density distribution and mass transport, were examined in the indium bump deposition process regarding the yield, uniformity and consistency. The influences of various current waveforms on the morphology, microstructure and uniformity of indium bumps were investigated while the mass transport condition remained the same. Acoustic agitation, *i.e.* both ultrasonic (30 *kHz*) and megasonic (1 *MHz*) agitation, was then employed as a novel method to alter the mass transport condition during the DC electroplating process.

The conclusions from the research work presented in this thesis are grouped into three parts: characteristics of indium electrodeposited using sulphamate solution, influences of various current waveforms on indium bump growth, and influences of acoustic agitation on the indium bumping process.

7.1.1 Characteristics of Indium Deposited Through Sulphamate Solution

Indium deposition was conducted using a sulphamate solution on non-patterned copper substrates. The experimental results led to the following conclusions.

- It was shown that, without the presence of any additional agitation, the cathodic current efficiency remained over 90% when the current density did not exceed 20 mA/cm^2, and decreased rapidly if the current density was beyond 25 mA/cm^2. The DC electroplated indium appeared granular in morphology and the surface feature size could be as large as 10 μm. The surface had noticeable roughness such that the measured maximum Total Height of Profile (P_t) was 40.7 μm and the measured maximum Average Roughness (R_a) was 3.88 μm.
- By using unipolar pulse electroplating, the indium surface morphology was dominated by a conical morphology and the surface features were significantly refined compared to DC electrodeposition. More than 90% current efficiency could be achieved when the pulse peak current density was below or equal to 100 mA/cm^2 with an average current density of 10 mA/cm^2. The surface smoothness was also improved compared to DC by using pulse electroplating such that the maximum P_t was 8.36 μm and the maximum R_a was 0.73 μm.
- By using bipolar pulse reverse electroplating, where the pulse peak current density was selected to be below or equal to 100 mA/cm^2 with an average current density of 10 mA/cm^2, the indium surface appeared polycrystalline in structure and surface feature refinement was observed in comparison to DC electroplating, equivalent to that seen for unipolar pulse electrodeposition. The surface roughness was reduced compared to DC electroplating, but at the same level as unipolar pulse electroplating.

7.1.2 Influences of Various Current Waveforms on Indium Bump Growth

The indium bumping process was successfully developed on 3 inch test wafers and extended to standard 4 inch wafers. The electroplated bumps were characterised in terms of the bumping yield, bump profile, microstructure, and within-wafer bump height uniformity. The characteristics were compared between DC electroplating, unipolar pulse electroplating and bipolar pulse reverse electroplating. Based on the experimental results, the main conclusions to be drawn areas follows:

- It has been demonstrated that electroplating is capable of generating high quality indium bumps with high yield and ultrafine pitch size. Using the facilities available in this research, we have successfully electrodeposited indium bumps of 15 μm diameter and 25 μm pitch with more than 99.9% yield using the criterion of the presence or absence of bumps.
- Primary experiments showed that the pre-wetting step was essential to achieve a high bumping yield in the indium sulphamate electroplating system. Ultrasonic agitation has been proved as an effective approach to pre-wet the ultrafine pitch photoresist pattern and thereafter more than 99.9% yield was achieved.
- The layout of electrical contacts can significantly affect the bump uniformity. Asymmetrically distributed contact terminals can induce directional differences of bump height uniformity across the wafer. Therefore, it is recommended that the electrical contact should be symmetrically distributed along the periphery of the wafer.
- It has been shown that a current thief ring is able to homogenise the directional non-uniformity when the electrical contact is made asymmetrically. This is achieved by the electroplated thief ring acting as an additional electrode spreading the electrical contact around the wafer periphery. It has also been shown that the current thief ring can improve the bump height uniformity on the wafer scale and pattern scale. In the case of DC electroplating at 10 mA/cm^2, the bump height uniformity on 4 inch wafer scale improved from approximately 28.29%

to 19.65% by adding a current thief ring design surrounding the whole patterned area.

- The bumping results through DC electroplating showed that the bump uniformity deteriorated when the current density increased. The bump uniformity can be improved by using pulsating current waveforms. By using pulse electroplating and pulse reverse electroplating, the best bump uniformity of 14.3% and 13.6% was respectively obtained on the 4 inch wafer scale. The pattern scale uniformity can also be improved by using pulse electroplating and pulse reverse electroplating.
- Microstructure studies indicated that there were no defects in the main body of electroplated indium bumps in DC, pulse electroplating and pulse reverse electroplating circumstances. However, a disruptive layer was commonly observed near the bottom of the bump at the initial stage of electroplating. Indium bump growth mechanism was proposed and the internal stress within the initial deposited layer was thought as the primary cause of the discontinuous growth.
- Grain refinement was observed only to a small extent in the pulse and pulse reverse electroplated indium bumps for which the recrystallisation might play a role in the course of or after deposition.
- The DC electroplated indium bumps had an uneven growth front with the edge of the bump much higher than the centre. The profile of the bump top can be levelled by using pulse electroplating and the bumps with protruding centre could be obtained by using pulse reverse electroplating.

7.1.3 Influences of Acoustic Agitation on Indium Bumping Process

Both ultrasonic agitation (30 *kHz*) and megasonic agitation (1 *MHz*) were introduced into the indium electroplating and bumping processes. All of the electroplating trials were conducted through direct current. Based on the experimental results, the main conclusions to be drawn are as follows.

- Due to the significant improvement in mass transport, the cathodic polarisation curves showed that the parameter operation window for

electrodeposition could be expanded by using both ultrasonic and megasonic agitation.

- In the presence of both ultrasonic and megasonic agitation, the surface morphology of electroplated indium was changed from granular to nodular, and surface feature refinement was observed to some extent. Meanwhile, the surface smoothness was improved in both cases. High speed electrodeposition can be enabled by using megasonic agitation.
- It was found that the risk of damage to the photoresist pattern increased with the time of application of ultrasonic agitation. The deteriorated yield made ultrasonic agitation for long periods unacceptable for the indium bumping process, but it could be used for short periods to pre-wet the photoresist patterns. In contrast, megasonic agitation had little effect on the fragile photoresist pattern and no damage was observed after applying the maximum intensity (5 W/cm^2) for 60 minutes. Moreover, megasonic agitation can also fulfil the requirement of pre-wetting the ultrafine pitch photoresist patterns to obtain a high yield.
- The configuration of the electroplating system can significantly affect the efficiency of megasonic agitation. Geometrical obstacles on the pathway of the megasonic energy propagation can compromise the megasonic streaming effect and therefore induce 'pitting' effects resulting in deteriorated bumping yield.
- An increase in the megasonic intensity can increase the quantity of micro-bubbles in the solution resulting in defects on the bump sidewall. In the indium sulphamate electroplating system used in this research, the experimental data indicated that the megasonic intensity should not exceed 2.5 W/cm^2. Moreover, a decrease in the transmission angle of megasonic energy applied to the wafer can increase the possibility of defects occurring on the bump sidewall.
- When the current density was 10 mA/cm^2, by using megasonic agitation, the bump uniformity was slightly decreased on the wafer scale while the bump uniformity was significantly improved within the patterns near the central area of the wafer.

- High speed indium bumping was realised by using megasonic agitation without sacrificing the current efficiency. Indium bumping through a current density of 50 mA/cm^2 was successfully conducted with 93.89% current efficiency. However, the uniformity deteriorated on both wafer scale and pattern scale.

7.2 Suggestions for Future Work

The findings in this research have led to the following recommendations for further studies:

- The uneven profile of the indium bump growth front indicated the limitation of the two additives (Dextrose and Triethanolamine) on levelling ability. Although the bump profile can be improved by using pulsating current waveforms, the cost of the high specification power supply might be an issue for industrial users. Therefore, the development of new additives having a stronger levelling ability can be beneficial to the indium bumping in large volume production.
- In the cross-sectional view of the indium bumps, a distinct separating layer was observed and the fundamental nature of its formation needs to be further understood. In the current pixel detector assemblies using indium bump bonding, copper is not included in the UBM stack. The most popular combination is Ti-Ni-Au which also has a surface having FCC crystal structure. It would therefore be constructive to study the crystal structure of the initial deposited layer using high resolution TEM to verify the growth mechanism of indium and its evolution as electroplating proceeds.
- The feasibility of high speed bumping has been demonstrated by using megasonic agitation and DC electroplating. However, the uniformity issue becomes more serious as the current density increases. Introducing megasonic agitation into pulse electroplating and pulse reverse electroplating might be promising to achieve a better uniformity.

References

[1] J. H. Lau, *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, New York: McGraw-Hill, 2000.

[2] M. Datta, T. Osaka, and J. W. Schultze, *Microelectronic Packaging*, London: CRC Press, 2005.

[3] *International Technology Roadmap for Semiconductors (ITRS)*, SIA/Sematech International, 2005.

[4] L. Rossi, P. Fischer, T. Rohe, and N. Wermes, *Pixel Detectors: From Fundamentals to Applications*, Berlin: Springer-Verlag, 2006.

[5] S. Gaalema, "Low Noise Random-Access Readout Technique for Large Pin Detector Arrays," *IEEE Transactions on Nuclear Science*, vol. 32, no. 1, pp. 417-418, 1985.

[6] F. Anghinolfi, P. Aspell, K. Bass, W. Beusch, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, E. Chesi, C. Claeys, J. C. Clemens, M. Cohen Solal, I. Debusschere, P. Delpierre, D. Di Bari, B. Dierickx, C. C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M. C. Habrard, E. H. M. Heijne, L. Hermans, R. Hurst, P. Inzani, J. J. Jaeger, P. Jarron, F. Krummenacher, F. Lemeilleur, V. Lenti, V. Manzari, G. Meddeler, M. Morando, A. Munns, F. Nava, F. Navach, C. Neyer, G. Ottaviani, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, R. Potheau, E. Quercigh, N. Redaelli, L. Rossi, D. Sauvage, G. Segato, S. Simone, G. Stefanini, G. Tonelli, G. Vanstraelen, G. Vegni, H. Verweij, G. M. Viertel, and J. Waisbard, "A 1006 element hybrid silicon pixel detector with strobed binary output," *IEEE Transactions on Nuclear Science*, vol. 39, no. 4, pp. 654-661, 1992.

[7] G. Alimonti, A. Andreazza, A. Bulgheroni, G. Corda, S. Di Gioia, A. Fiorello, C. Gemme, M. Koziel, F. Manca, C. Meroni, P. Nechaeva, A. Paoloni, L. Rossi, A. Rovani, and E. Ruscino, "Analysis of the production of ATLAS indium bonded pixel modules," *Nuclear Instruments & Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 565, pp. 296-302, 2006.

[8] T. Fritzsch, R. Jordan, M. Töpper, J. Röder, I. Kuna, M. Lutz, F. Defo Kamga, J. Wolf, O. Ehrmann, H. Oppermann, and H. Reichl, "Experience in fabrication of multichip-modules for the ATLAS pixel detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 565, no. 1, pp. 309-313, 2006.

[9] J. Grosse-Knetter, "The ATLAS pixel detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 568, no. 1, pp. 252-257, 2006.

[10] G. Pellegrini, M. Chmeissani, M. Maiorino, G. Blanchot, J. Garcia, M. Lozano, R. Martinez, C. Puigdengoles, M. Ullan, and P. Casado, "Performance limits of a 55-/spl mu/m pixel CdTe detector," *IEEE Transactions on Nuclear Science,* vol. 53, no. 1, pp. 361-366, 2006.

[11] J. Breibach, K. Lübelsmeyer, T. Mäsing, and C. Rente, "Development of a bump bonding interconnect technology for GaAs pixel detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators,Spectrometers,Detectors and Associated Equipment,* vol. 470, no. 3, pp. 576-582, 2001.

[12] A. Rogalski, "Infrared detectors: an overview," *Infrared Physics & Technology,* vol. 43, no. 3-5, pp. 187-210, 2002.

[13] A. I. Ayzenshtat, D. L. Budnitsky, O. B. Koretskaya, L. S. Okaevich, V. A. Novikov, A. I. Potapov, O. P. Tolbanov, A. V. Tyazhev, and A. P. Vorobiev, "GaAs as a material for particle detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 494, no. 1-3, pp. 120-127, 2002.

[14] S. Cihangir, and S. Kwan, "Characterization of indium and solder bump bonding for pixel detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 476, no. 3, pp. 670-675, 2002.

[15] L. F. Miller, "Controlled Collapse Reflow Chip Joining," *IBM Journal of Research & Development,* vol. 13, no. 3, pp. 239-250, 1969.

[16] K. C. Norris, and A. H. Landzberg, "Reliability of Cotrolled Collapse Interconnections," *IBM Journal of Research & Development,* vol. 13, no. 3, pp. 266-271, 1969.

[17] L. S. Goldmann, "Geometic Optimization of Controlled Collapse Interconnections," *IBM Journal of Research & Development*, vol. 13, no. 3, pp. 251-265, 1969.

[18] M. Juergen Wolf, G. Engelmann, L. Dietrich, and H. Reichl, "Flip chip bumping technology: Status and update," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 565, no. 1, pp. 290-295, 2006.

[19] J. Kloeser, K. Heinricht, E. Jung, L. Lauter, A. Ostmann, R. Aschenbrenner, and H. Reichl, "Low cost bumping by stencil printing: process qualification for 200 μm pitch," *Microelectronics Reliability*, vol. 40, no. 3, pp. 497-505, 2000.

[20] J. R. Morris, and T. Wojcik, "Stencil printing of solder paste for fine-pitch surface mount assembly," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 14, no. 3, pp. 560-566, 1991.

[21] R. W. Kay, S. Stoyanov, G. P. Glinski, C. Bailey, and M. P. Y. Desmulliez, "Ultra-Fine Pitch Stencil Printing for a Low Cost and Low Temperature Flip-Chip Assembly Process," *IEEE Transactions on Components and Packaging Technologies*, vol. 30, no. 1, pp. 129-136, 2007.

[22] D. Manessis, R. Patzelt, A. Ostmann, R. Aschenbrenner, and H. Reichl, "Technical challenges of stencil printing technology for ultra fine pitch flip chip bumping," *Microelectronics Reliability*, vol. 44, no. 5, pp. 797-803, 2004.

[23] L. Li, S. Wiegele, P. Thompson, and R. Lee, "Stencil printing process development for low cost flip chip interconnect," in 48th IEEE Electronic Components & Technology Conference, May, Seatle, USA, 1998, pp. 421-426.

[24] S. Krongelb, L. T. Romankiw, and J. A. Tornello, "Electrochemical process for advanced package fabrication," *IBM Journal of Research & Development*, vol. 42, no. 5, pp. 575-585, 1998.

[25] M. Datta, and D. Landolt, "Fundamental aspects and applications of electrochemical microfabrication," *Electrochimica Acta*, vol. 45, no. 15-16, pp. 2535, 2000.

[26] P. C. Andricacos, and N. Robertson, "Future directions in electroplated materials for thin-film recording heads," *IBM Journal of Research & Development*, vol. 42, no. 5, pp. 671-680, 1998.

[27] M. Datta, R. V. Shenoy, C. Jahnes, P. C. Andricacos, J. Horkans, J. O. Dukovic, L. T. Romankiw, J. Roeder, H. Deligianni, H. Nye, B. Agarwala, H. M. Tong, and P. Totta, "Electrochemical Fabrication of Mechanically Robust PbSn C4 Interconnections," *Journal of The Electrochemical Society,* vol. 142, no. 11, pp. 3779-3785, 1995.

[28] C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM Journal of Research & Development,* vol. 42, no. 5, pp. 567-574, 1998.

[29] P. Dixit, and J. Miao, "Aspect-Ratio-Dependent Copper Electrodeposition Technique for Very High Aspect-Ratio Through-Hole Plating," *Journal of The Electrochemical Society,* vol. 153, no. 6, pp. G552-G559, 2006.

[30] E. K. Yung, and I. Turlik, "Electroplated solder joints for flip-chip applications," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 14, no. 3, pp. 549-559, 1991.

[31] M. Bigas, and E. Cabruja, "High density of electrodeposited Sn/Ag bumps for flip chip connection," *Microelectronic Engineering,* vol. 83, no. 3, pp. 399-403, 2006.

[32] H. Honma, "Plating technology for electronics packaging," *Electrochimica Acta,* vol. 47, no. 1-2, pp. 75-84, 2001.

[33] N. Felix, "Indium and Indium Compounds," *Metallurgie Hoboken-Overpelt, Hoboken, Belgium. Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany*, 2005.

[34] M. Yamaguchi, A. Ide-Ektessabi, H. Nomura, and N. Yasui, "Characteristics of indium tin oxide thin films prepared using electron beam evaporation," *Thin Solid Films,* vol. 447-448, pp. 115-118, 2004.

[35] C. Gemme, A. M. Fiorello, G. Gagliardi, M. Gilchriese, P. Netchaeva, L. Rossi, E. Ruscino, F. Vernocchi, and M. Varasi, "Study of indium bumps for the ATLAS pixel detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 465, no. 1, pp. 200-203, 2001.

[36] J. John, L. Zimmermann, P. D. Moor, and C. V. Hoof, "High-density hybrid interconnect methodologies," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 531, no. 1-2, pp. 202-208, 2004.

[37] T. Rohe, C. Broennimann, F. Glaus, J. Gobrecht, S. Heising, M. Horisberger, R. Horisberger, H. C. Kastli, J. Lehmann, and S. Streuli, "Development of an Indium bump bond process for silicon pixel detectors at PSI," *Nuclear Instruments & Methods in Physics Research, Section A (Accelerators, Spectrometers, Detectors and Associated Equipment),* vol. 565, pp. 303-308, 2006.

[38] J. Jiang, S. Tsao, T. O'Sullivan, M. Razeghi, and G. J. Brown, "Fabrication of indium bumps for hybrid infrared focal plane array applications," *Infrared Physics & Technology,* vol. 45, no. 2, pp. 143-151, 2004.

[39] P. Merken, J. John, L. Zimmermann, and C. Van Hoof, "Technology for very dense hybrid detector arrays using electroplated indium solderbumps," *IEEE Transactions on Advanced Packaging,* vol. 26, no. 1, pp. 60-64, 2003.

[40] Milan Paunovic, and M. Schlesinger, *Fundamentals of Electrochemical Deposition*, 2nd ed., Hoboken, New Jersey: John Wiley & Sons, 2006.

[41] F. A. Lowenheim, *Electroplating*, London: McGraw-Hill, 1978.

[42] F. C. Walsh, and M. E. Herron, "Electrocrystallization and electrochemical control of crystal growth: fundamental considerations and electrodeposition of metals," *Journal of Physics D: Applied Physics,* vol. 24, no. 2, pp. 217-225, 1991.

[43] L. Oniciu, and L. Mureşan, "Some fundamental aspects of levelling and brightening in metal electrodeposition," *Journal of Applied Electrochemistry,* vol. 21, no. 7, pp. 565-574, 1991.

[44] T. C. Franklin, "Some mechanisms of action of additives in electrodeposition processes," *Surface and Coatings Technology,* vol. 30, no. 4, pp. 415-428, 1987.

[45] R. Piercy, and N. A. Hampson, "The electrochemistry of indium," *Journal of Applied Electrochemistry,* vol. 5, no. 1, pp. 1-15, 1975.

[46] F. C. Walsh, and D. R. Gabe, "Electrode reactions during the electrodeposition of indium from acid sulphate solutions," *Surface Technology,* vol. 6, no. 6, pp. 425-436, 1978.

[47] F. C. Walsh, and D. R. Gabe, "The electrodeposition of indium," *Surface Technology,* vol. 8, no. 2, pp. 87-99, 1979.

[48] F. C. Walsh, and D. R. Gabe, "The electrodeposition of indium alloys," *Surface Technology*, vol. 13, no. 4, pp. 305-314, 1981.

[49] R. Piercy, and N. A. Hampson, “Effects of surface treatment on typical electrochemical properties of an indium microelectrode,” *Electrodeposition and Surface Treatment,* vol. 2, pp. 501-504, 1973/1974.

[50] J. A. Slattery, “Indium plating,” *Metal Finishing,* vol. 100, no. 1, pp. 250-252, 2002.

[51] N. A. Kermali, and D. R. Gabe., “Diffusion coating of indium on copper,” *Surface Technology,* vol. 15, pp. 1-10, 1982.

[52] "Indium Sulphamate Plating Bath," 15th Feburary 2010; http://www.indium.com/techlibrary/pds.php.

[53] “Indium Sulfamate Plating Bath,” *Indium Coporation,* Operation Instruction released in 2007.

[54] Jean-Claude Puippe, and Frank. Leaman, *Theory and Practice of Pulse Plating,*, Orlando, FL: American Electroplaters and Surface Finishers Society, 1986.

[55] J. C. Puippe, and N. Ibl, “Influence of charge and discharge of electric double layer in pulse plating,” *Journal of Applied Electrochemistry,* vol. 10, no. 6, pp. 775-784, 1980.

[56] X. Zhang, K. N. Tu, Z. Chen, Y. K. Tan, C. C. Wong, S. G. Mhaisalkar, X. M. Li, C. H. Tung, and C. K. Cheng, “Pulse Electroplating of Copper Film: A Study of Process and Microstructure,” *Journal of Nanoscience and Nanotechnology,* vol. 8, pp. 2568-2574, 2008.

[57] Y. F. Shen, W. Y. Xue, Y. D. Wang, Z. Y. Liu, and L. Zuo, “Mechanical properties of nanocrystalline nickel films deposited by pulse plating,” *Surface and Coatings Technology,* vol. 202, no. 21, pp. 5140-5145, 2008.

[58] N. S. Qu, D. Zhu, K. C. Chan, and W. N. Lei, “Pulse electrodeposition of nanocrystalline nickel using ultra narrow pulse width and high peak current density,” *Surface and Coatings Technology,* vol. 168, no. 2-3, pp. 123-128, 2003.

[59] T. Nakanishi, M. Ozaki, H.-S. Nam, T. Yokoshima, and T. Osaka, “Pulsed Electrodeposition of Nanocrystalline CoNiFe Soft Magnetic Thin Films,” *Journal of The Electrochemical Society,* vol. 148, no. 9, pp. C627-C631, 2001.

[60] S. K. Ghosh, T. Bera, C. Saxena, S. Bhattacharya, and G. K. Dey, “Effect of pulse plating and additive on phase separation in Cu-Co nano-granular alloys,” *Journal of Alloys and Compounds,* vol. 475, no. 1-2, pp. 676-682, 2009.

[61] P. T. Tang, "Pulse reversal plating of nickel and nickel alloys for microgalvanics," *Electrochimica Acta,* vol. 47, no. 1-2, pp. 61-66, 2001.

[62] M. Datta, "Electrochemical processing technologies in chip fabrication: challenges and opportunities," *Electrochimica Acta,* vol. 48, no. 20-22, pp. 2975-2985, 2003.

[63] E. Lennon, and F. Ayela, "Electrodeposition through thick photoresist moulds for the fabrication of a sharp chromium microtip," *Journal of Micromechanics and Microengineering,* vol. 12, no. 2, pp. 122-127, 2002.

[64] Jean-Marie Quemper, Elisabeth Dufour-Gergam, Nad`ege Frantz-Rodriguez, Jean-Paul Gilles, Jean-Paul Grandchamp, and A. Bosseboeuf, "Effects of direct and pulse current on copper electrodeposition through photoresist molds," *Journal of Micromechanics and Microengineering,* vol. 10, no. 2, pp. 116-119, 2000.

[65] B. Kim, and T. Ritzdorf, "Electrical Waveform Mediated Through-Mask Deposition of Solder Bumps for Wafer Level Packaging," *Journal of the Electrochemical Society,* vol. 151, no. 5, pp. C342-C347, 2004.

[66] Chen-Kuei Chung, and W.-T. Chang, "Deep nickel metal deposition on multiscale feature sizes of a small hole and large sector cavities using electroforming," *Journal of Micro/Nanolithography MEMS and MOEMS,* vol. 8, no. 2, pp. (021111-1)-(021111-6), 2009.

[67] M. Georgiadou, and D. Veyret, "Optimization of trench filling during copper electrodeposition by additives and pulse plating," *Proceedings of the Institution of Mechanical Engineers Part B: Journal of Engineering Manufacture,* vol. 217, no. 6, pp. 857-863, 2003.

[68] P. Dixit, C. W. Tan, L. Xu, N. Lin, J. Miao, J. H. L. Pang, P. Backus, and R. Preisser, "Fabrication and characterization of fine pitch on-chip copper interconnects for advanced wafer level packaging by a high aspect ratio through AZ9260 resist electroplating," *Journal of Micromechanics and Microengineering,* vol. 17, no. 5, pp. 1078-1086, 2007.

[69] J.-M. Lee, and A. C. West, "Impact of Pulse Parameters on Current Distribution in High Aspect Ratio Vias and Through-Holes," *Journal of The Electrochemical Society,* vol. 152, no. 10, pp. C645-C651, 2005.

[70] A. M. Pesco, and H. Y. Cheh, "The Current Distribution within Plated Through-Holes II: The Effect of Periodic Electrolysis," *Journal of The Electrochemical Society,* vol. 136, no. 2, pp. 408-414, 1989.

[71] S. H. Cha, S.-S. Kim, S. K. Cho, and J. J. Kim, "Copper Bottom-Up Filling by Electroplating Without any Additives on Patterned Wafer," *Electrochemical and Solid-State Letters,* vol. 10, no. 2, pp. D22-D24, 2007.

[72] W.-C. Tsai, C.-C. Wan, and Y.-Y. Wang, "Frequency Effect of Pulse Plating on the Uniformity of Copper Deposition in Plated Through Holes," *Journal of The Electrochemical Society,* vol. 150, no. 5, pp. C267-C272, 2003.

[73] P. Dixit, X. Luhua, M. Jianmin, John, H. L. Pang, D. Witarsa, P. Lim, P. Backus, and R. Preisser, "Mechanical and microstructure characterization of high aspect ratio electroplated through-wafer copper interconnects," *2006 8th Electronics Packaging Technology Conference (IEEE Cat. No.06EX1538),* 2006.

[74] P. Dixit, J. Miao, and R. Preisser, "Fabrication of High Aspect Ratio 35 mu m Pitch Through-Wafer Copper Interconnects by Electroplating for 3-D Wafer Stacking," *Electrochemical and Solid-State Letters,* vol. 9, no. 10, pp. G305-G308, 2006.

[75] A. D. Aird, *Method of Manufacturing a Semiconductor Device Utilizing a Flexible Carrier,* U.S Patent 3689991, 1972

[76] R. Kiumi, J. Yoshioka, F. Kuriyama, N. Saito, and M. Shimoyama, "Process development of electroplate bumping for ULSI flip chip technology," in 52nd Electronic Components and Technology Conference, California, USA, May, 2002, pp. 711-716.

[77] T. Oppert, E. Zakel, and T. Teutsch, "Wafer Bumping & Wafer Level Packaging for 300mm Wafer," in 31st International Conference on Electronics Manufacturing and Technology, Putrajaya, Malaysia, 2006, pp. 42-42.

[78] P. Elenius, L. Leal, J. Ney, D. Stepniak, and Y. Shing, "Recent advances in flip chip wafer bumping using solder paste technology," in 49th Electronic Components and Technology Conference,, San Diego, USA, June, 1999, pp. 260-265.

[79] G. Viswanadam, and H. Leow Khim, "Wafer level lead free solder bumping process and characterization," in International Symposium on Electronic Materials and Packaging (EMAP). , Hong Kong, China, 2000, pp. 7-11.

[80] M. Bigas, and E. Cabruja, "Characterisation of electroplated Sn/Ag solder bumps," *Microelectronics Journal,* vol. 37, no. 4, pp. 308-316, 2006.

[81] S. Kang, P. Gruber, and D.-Y. Shih, "An overview of Pb-free, flip-chip wafer-bumping technologies," *JOM Journal of the Minerals, Metals and Materials Society,* vol. 60, no. 6, pp. 66-70, 2008.

[82] X. Lin, and L. Luo, "Sub-100 μm SnAg Solder Bumping Technology and the Bump Reliability," *Journal of Electronic Packaging,* vol. 131, no. 1, pp. 1-6, 2009.

[83] K.-S. Kim, T. Imanishi, K. Suganuma, M. Ueshima, and R. Kato, "Properties of low temperature Sn–Ag–Bi–In solder systems," *Microelectronics Reliability,* vol. 47, no. 7, pp. 1113-1119, 2007.

[84] H. Oulfajrite, A. Sabbar, M. Boulghallat, A. Jouaiti, R. Lbibb, and A. Zrineh, "Electrochemical behavior of a new solder material (Sn–In–Ag)," *Materials Letters,* vol. 57, no. 28, pp. 4368-4371, 2003.

[85] C. W. Tobias, and R. Wijsman, "Theory of the Effect of Electrode Resistance on Current Density Distribution in Electrolytic Cells," *Journal of The Electrochemical Society,* vol. 100, no. 10, pp. 459-467, 1953.

[86] J. F. D'Amico, M. A. DeAngelo, and F. R. McLarnon, "Copper Electrodeposition onto Moving High Resistance Electroless Films," *Journal of the Electrochemical Society,* vol. 132, no. 10, pp. 2330-2336, 1985.

[87] W. H. Smyrl, and J. Newman, "Current Distribution at Electrode Edges at High Current Densities," *Journal of The Electrochemical Society,* vol. 136, no. 1, pp. 132-139, 1989.

[88] O. Lanzi, and U. Landau, "Terminal Effect at a Resistive Electrode under Tafel Kinetics," *Journal of The Electrochemical Society,* vol. 137, no. 4, pp. 1139-1143, 1990.

[89] M. Matlosz, P. H. Vallotton, A. C. West, and D. Landolt, "Nonuniform Current Distribution and Thickness during Electrodeposition onto Resistive Substrates," *Journal of The Electrochemical Society,* vol. 139, no. 3, pp. 752-761, 1992.

[90] P. Vallotton, M. Matlosz, and D. Landolt, "Experimental investigation of the terminal effect in lead electrodeposition onto resistive substrates," *Journal of Applied Electrochemistry,* vol. 23, no. 9, pp. 927-932, 1993.

[91] J. O. Dukovic, "Computation of current distribution in electrodeposition, A review," *IBM Journal of Research and Development,* vol. 34, no. 5, pp. 693-705, 1990.

[92] B. DeBecker, and A. C. West, "Workpiece, Pattern, and Feature Scale Current Distributions," *Journal of The Electrochemical Society,* vol. 143, no. 2, pp. 486-492, 1996.

[93] J.O.Dukovic, "Feature-scale simulation of resist-patterned electrodeposition," *IBM Journal of Research and Development,* vol. 37, no. 2, pp. 125-141, 1993.

[94] T. Park, T. Tugbawa, D. Boning, C. Chidambaram, C. Borst, and G. Shin, "Chip-Scale Modeling of Electroplated Copper Surface Profiles," *Journal of the Electrochemical Society,* vol. 151, no. 6, pp. C418-C430, 2004.

[95] R. J. Contolini, A. F. Bernhardt, and S. T. Mayer, "Electrochemical Planarization for Multilevel Metallization," *Journal of The Electrochemical Society,* vol. 141, no. 9, pp. 2503-2510, 1994.

[96] J.-M. Lee, J. J. T. Hachman, J. J. Kelly, and A. C. West, "Improvement of current distribution uniformity on substrates for microelectromechanical systems," *Journal of Microlithography, Microfabrication, and Microsystems,* vol. 3, no. 1, pp. 146-151, 2004.

[97] J.-M. Lee, H. McCrabb, E. J. Taylor, and R. Carpio, "Current Distribution for the Metallization of Resistive Wafer Substrates under Controlled Geometric Variations," *Journal of the Electrochemical Society*, vol. 153, no. 4, pp. C265-C271, 2006.

[98] S. Mayer, R. Hill, A. Harrus, E. Patton, R. Contolini, S. Taatjes, and J. Reid, *Method and apparatus for uniform electroplating of integrated circuits using a variable field shaping element*, U.S. Patent 6402923, 2002.

[99] Y.-S. Choi, and T. Kang, "Three-Dimensional Calculation of Current Distribution in Electrodeposition on Patterned Cathode with Auxiliary Electrode," *Journal of The Electrochemical Society,* vol. 143, no. 2, pp. 480-485, 1996.

[100] S. Mehdizadeh, J. Dukovic, P. C. Andricacos, L. T. Romankiw, and H. Y. Cheh, "Optimization of Electrodeposit Uniformity by the Use of Auxiliary Electrodes," *Journal of The Electrochemical Society,* vol. 137, no. 1, pp. 110-117, 1990.

[101] Y. Cao, J.-M. Lee, and A. C. West, "Designs for minimizing resistive substrate effects on wafer metallization," *Plating and surface finishing*, vol. 90, no. 11, pp. 40-45, 2003.

[102] L. Graham, K. Hanson, T. Ritzdorf, and J. Turner, *Electroplating system having auxiliary electrode exterior to main reactor chamber for contact cleaning operations*, U.S. Patent 6921468B2, 2005.

[103] S. Kaja, C. Prasad, and R. R. Yu, *Process and apparatus for electroplating microscopic features uniformly across a large substrate*, U.S. Patent 6669833B2, 2003.

[104] J. Ang, *Method for electroplating metal films including use a cathode ring, insulator ring and thief ring*, U.S. Patent 5744019, 1998.

[105] T.-J. Cheng, T. Fowler, A. Giri, A. Nenadic, B. Samuel, and K. K. H. Wong, *Method for controlling local current to achieve uniform plating thickness*, U.S. Patent 6896784B2, 2005.

[106] S. Mehdizadeh, J. O. Dukovic, P. C. Andricacos, L. T. Romankiw, and H. Y. Cheh, "The Influence of Lithographic Patterning on Current Distribution: A Model for Microfabrication by Electrodeposition," *Journal of The Electrochemical Society*, vol. 139, no. 1, pp. 78-91, 1992.

[107] S. Mehdizadeh, J. Dukovic, P. C. Andricacos, L. T. Romankiw, and H. Y. Cheh, "The Influence of Lithographic Patterning on Current Distribution in Electrodeposition: Experimental Study and Mass-Transfer Effects," *Journal of The Electrochemical Society*, vol. 140, no. 12, pp. 3497-3505, 1993.

[108] A. C. West, M. Matlosz, and D. Landolt, "Normalized and Average Current Distributions on Unevenly Spaced Patterns," *Journal of the Electrochemical Society*, vol. 138, no. 3, pp. 728, 1991.

[109] R. Akolkar, and V. Dubin, "Pattern Density Effect on the Bottom-Up Fill during Damascene Copper Electrodeposition," *Electrochemical and Solid-State Letters*, vol. 10, no. 6, pp. D55-D59, 2007.

[110] M. Datta, and D. Landolt, "Fundamental aspects and applications of electrochemical microfabrication," *Electrochimica Acta*, vol. 45, no. 15-16, pp. 2535-2558, 2000.

[111] L. T. Romankiw, "A path: from electroplating through lithographic masks in electronics to LIGA in MEMS," *Electrochimica Acta*, vol. 42, no. 20-22, pp. 2985-3005, 1997.

[112] K. Kondo, and K. Fukui, "Current Evolution of Electrodeposited Copper Bumps with Photoresist Angle," *Journal of The Electrochemical Society*, vol. 145, no. 3, pp. 840-844, 1998.

[113] E. Castellani, J. Powers, and L. T. Romankiw, *Nickel-Iron (80:20) Alloy Thin Film Electroplating Method and Electrochemical Treatment and Plating Apparatus*, U.S. Patent 4102756, 1978.

[114] M. A. Alodan, and L. E. Stover, "Selective plating without masking," *Electrochimica Acta*, vol. 44, no. 21-22, pp. 3721-3724, 1999.

[115] R. Chesnutt, "Electroplated CoNiFe Alloy for Use in an Integrated Inductive magnetoresistive Recording Head," *Journal of Applied Physics*, vol. 73, no. 10, pp. 6223-6225, 1993.

[116] A. Yamaguchi, T. Mino, S. Yari, and S. Ichihara, *Electroplated Magnetic Thin Film Method of Manufacturing the Same, Electroplating Bath and Thin Film Magnetic Head*, U.S. Patent 7101633B2, 2006.

[117] T. Osaka, "Recent development of Magnetic recording head core materials by plating method," *Electrochimica Acta*, vol. 44, no. 21-22, pp. 3885-3890, 1999.

[118] T. Osaka, "Electrodeposition of highly functional thin films for magnetic recording devices of the next century," *Electrochimica Acta*, vol. 45, no. 20, pp. 3311-3321, 2000.

[119] B. Q. Wu, Z. Liu, A. Keigler, and J. Harrell, "Diffusion Boundary Layer Studies in an Industrial Wafer Plating Cell," *Journal of The Electrochemical Society*, vol. 152, no. 5, pp. C272-C276, 2005.

[120] R. W. Batz, S. Conrady, and T. L. Ritzdorf, *Apparatus for High Deposition Rate Solder Electroplating on A Microelectronic Workpiece*, U.S. Patent 6334937B1, 2002.

[121] K. M. Hanson, S. L. Eudy, T. L. Ritzdorf, G. J. Wilson, D. J. Woodruff, R. Harris, C. A. Weber, T. McGlenn, T. A. Anderson, and D. P. Bexten, *Processing Tools, Components of Processing Tools, and Method of Making and Using Same for Electrochemical Processing of Microelectronic Workpieces*, U. S. Patent 6921467B2, 2005.

[122] J. T. Hachman, J. J. Kelly, and A. C. West, *Apparatus and Method for Controlling Plating Uniformity*, U. S. Patent 6802950B2, 2004.

[123] P. M. Vereecken, R. A. Binstead, H. Deligianni, and P. C. Andricacos, "The chemistry of additives in damascene copper plating," *IBM Journal of Research & Development*, vol. 49, no. 1, pp. 3-18, 2005.

[124] T. J. Mason, and J. P. Lorimer, *Applied Sonochemistry: The Uses of Power Ultrasound in Chemistry and Processing*: Wiley-VCH, 2002.

[125] M. E. Bran, *Megasonic Cleaning Apparatus*, U.S. Patent 4998549, 1991.

[126] R. W. Grant, and R. E. Novak, *Megasonic Cleaning System*, U.S. Patent 5247954, 1993.

[127] J. Skrovan, and G. F. Hudson, *Megasonic Cleaning Methods and Apparatus*, U.S. Patent 6048405, 2000.

[128] M. Olim, "A Theoretical Evaluation of Megasonic Cleaning for Submicron Particles," *Journal of The Electrochemical Society*, vol. 144, no. 10, pp. 3657-3659, 1997.

[129] A. A. Busnaina, I. I. Kashkoush, and G. W. Gale, "An Experimental Study of Megasonic Cleaning of Silicon Wafers," *Journal of The Electrochemical Society*, vol. 142, no. 8, pp. 2812-2817, 1995.

[130] K. Bakhtari, R. O. Guldiken, P. Makaram, A. A. Busnaina, and J.-G. Park, "Experimental and Numerical Investigation of Nanoparticle Removal Using Acoustic Streaming and the Effect of Time," *Journal of The Electrochemical Society*, vol. 153, no. 9, pp. G846-G850, 2006.

[131] "An Introduction to Sonochemistry," Accessed in 17th September, 2008; http://www.sonochemistry.info/Research.htm.

[132] R. H. Nilson, and S. K. Griffiths, "Enhanced Transport by Acoustic Streaming in Deep Trench-Like Cavities," *Journal of The Electrochemical Society*, vol. 149, no. 4, pp. G286-G296, 2002.

[133] D. Kupper, D. Kupper, Y. M. Georgiev, T. Wahlbrink, W. Henschel, G. Bell, and H. Kurz, "Megasonic-assisted development of nanostructures: Investigations on high aspect ratio nanoholes," *Applied Physics Letters*, vol. 85, no. 21, pp. 5055-5057, 2004.

[134] J.-G. Jin, S.-K. Lee, and Y.-H. Kim, "Adhesion improvement of electroless plated Ni layer by ultrasonic agitation during zincating process," *Thin Solid Films*, vol. 466, no. 1-2, pp. 272-278, 2004.

[135] F. Touyeras, J. Y. Hihn, X. Bourgoin, B. Jacques, L. Hallez, and V. Branger, "Effects of ultrasonic irradiation on the properties of coatings obtained by

electroless plating and electro plating," *Ultrasonics Sonochemistry*, vol. 12, no. 1-2, pp. 13-19, 2005.

[136] Q. Chen, Z. Wang, J. Cai, and L. Liu, "The influence of ultrasonic agitation on copper electroplating of blind-vias for SOI three-dimensional integration," *Microelectronic Engineering*, vol. 87, no. 3, pp. 527-531, 2010.

[137] M. E. Hyde, and R. G. Compton, "How ultrasound influences the electrodeposition of metals," *Journal of Electroanalytical Chemistry*, vol. 531, no. 1, pp. 19-24, 2002.

[138] F. Touyeras, J. Y. Hihn, S. Delalande, R. Viennet, and M. L. Doche, "Ultrasound influence on the activation step before electroless coating," *Ultrasonics Sonochemistry*, vol. 10, no. 6, pp. 363-368, 2003.

[139] A. Chiba, T. Gotou, K. Kobayashi, and W.-C. Wu, "Influence of sonication of nickel plating in a nickel sulfamate bath," *Metal Finishing*, vol. 98, no. 9, pp. 66-69, 2000.

[140] K. Bakhtari, R. O. Guldiken, A. A. Busnaina, and J.-G. Park, "Experimental and Analytical Study of Submicrometer Particle Removal from Deep Trenches," *Journal of The Electrochemical Society*, vol. 153, no. 9, pp. C603-C607, 2006.

[141] J. D. Williams, and W. Wang, "Using megasonic development of SU-8 to yield ultra-high aspect ratio microstructures with UV lithography," *Microsystem Technologies*, vol. 10, no. 10, pp. 694-698, 2004.

[142] I. Suni, C. Tiwari, A. Busnaina, H. Lin, H. V. Reynolds, and C. Neely, "Copper Electroplating onto Silicon Wafers Using High-Frequency Acoustic Streaming," *Electrochemical Society Proceedings.* pp. 15-22, 2000.

[143] A. A. Busnaina, C. S. Tiwari, I. I. Suni, V. Reynolds, M. Nakoski, C. Neely, and T. Way, "Enhanced Copper Electroplating Using High Frequency Acoustic Streaming," *AESF SUR/FIN.* pp. 105-108, 2000.

[144] J. A. D. Jensen, P. Pocwiardowski, P. O. Persson, L. Hultman, and P. Moller, "Acoustic streaming enhanced electrodeposition of nickel," *Chemical Physics Letters*, vol. 368, no. 5-6, pp. 732-737, 2003.

[145] J. Kaufmann, M. Desmulliez, Y. Tian, D. Price, M. Hughes, N. Strusevich, C. Bailey, C. Liu, and D. Hutt, "Megasonic agitation for enhanced electrodeposition of copper," *Microsystem Technologies*, vol. 15, no. 8, pp. 1245-1254, 2009.

[146] J. Kaufmann, Marc P. Y. Desmulliez, and D. Price, "Megasonic Enhanced Electrodeposition," in Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS - DTIP, Nice, France, 2008, pp. 369-372.

[147] A. Busnaina, H. Lin, and N. Moumen, "Surface Cleaning Mechanisms and Future Cleaning Requirements," in IEEUSEMI Advanced Semiconductor Manufacturing Conference, 2000, pp. 328-333.

[148] B. Lovrecek, and V. Markovac, "Studies of the Electrochemical Kinetics of Indium: I. Kinetics of Deposition and Dissolution in the Inium + Indium Sulfate System," *Journal of The Electrochemical Society,* vol. 109, no. 8, pp. 727-731, 1962.

[149] V. Markovac, and B. Lovrecek, "Studies of the Electrochemical Kinetics of Indium: II. System Indium + Indium Sulfate at Higher C.D. ," *Journal of The Electrochemical Society,* vol. 112, no. 5, pp. 520-524, 1965.

[150] V. Markovac, and B. Lovrecek, "Studies of the Electrochemical Kinetics of Indium: III. Systems In + InCl3 and In + Combined Sulfate-Chloride Electrolyte," *Journal of The Electrochemical Society,* vol. 113, no. 8, pp. 838-841, 1966.

[151] S. H. Brongersma, E. Richard, I. Vervoort, H. Bender, W. Vandervorst, S. Lagrange, G. Beyer, and K. Maex, "Two-step room temperature grain growth in electroplated copper," *Journal of Applied Physics,* vol. 86, no. 7, pp. 3642-3645, 1999.

[152] D. Xu, V. Sriram, V. Ozolins, J.-M. Yang, K. N. Tu, G. R. Stafford, and C. Beauchamp, "In situ measurements of stress evolution for nanotwin formation during pulse electrodeposition of copper," *Journal of Applied Physics,* vol. 105, no. 2, pp. (023521-1)-(023521-6), 2009.

[153] C. Lingk, M. E. Gross, and W. L. Brown, "Texture development of blanket electroplated copper films," *Journal of Applied Physics,* vol. 87, no. 5, pp. 2232-2236, 2000.

[154] M. S. Chandrasekar, and M. Pushpavanam, "Pulse and pulse reverse plating--Conceptual, advantages and applications," *Electrochimica Acta,* vol. 53, no. 8, pp. 3313-3322, 2008.

[155] M. Purcar, B. Van den Bossche, L. Bortels, J. Deconinck, and G. Nelissen, "Three-Dimensional Current Density Distribution Simulations for a Resistive

Patterned Wafer," *Journal of The Electrochemical Society,* vol. 151, no. 9, pp. D78-D86, 2004.

[156] M. J. Willey, and A. C. West, "Nucleation on resistive substrates: Analysis of effect on film uniformity," *Electrochimica Acta,* vol. 52, no. 23, pp. 6484-6489, 2007.

[157] Jun Liu, Changqing Liu, Paul Conway, Jun Zeng, and C. Wang., "Growth and recrystallization of electroplated copper columns," in International Conference on Electronic Packaging Technology & High Density Packaging 2009 (ICEPT-HDP '09), Beijing, China, August 2009, pp. 695 - 700.

[158] J. Liu, "Simulation and Characterisation of Electroplated Micro-Copper Columns for Electronic Interconnection," PhD Thesis, Loughborough University, UK, 2010.

[159] C. Lingk, and M. E. Gross, "Recrystallization kinetics of electroplated Cu in damascene trenches at room temperature," *Journal of Applied Physics,* vol. 84, no. 10, pp. 5547-5553, 1998.

[160] A. Cobley, and T. Mason, "The Evaluation of Sonochemical Techniques for Sustaninable Surface Modification in Electronic Manufacturing," *Circuit World,* vol. 33, no. 3, pp. 29-34, 2007.

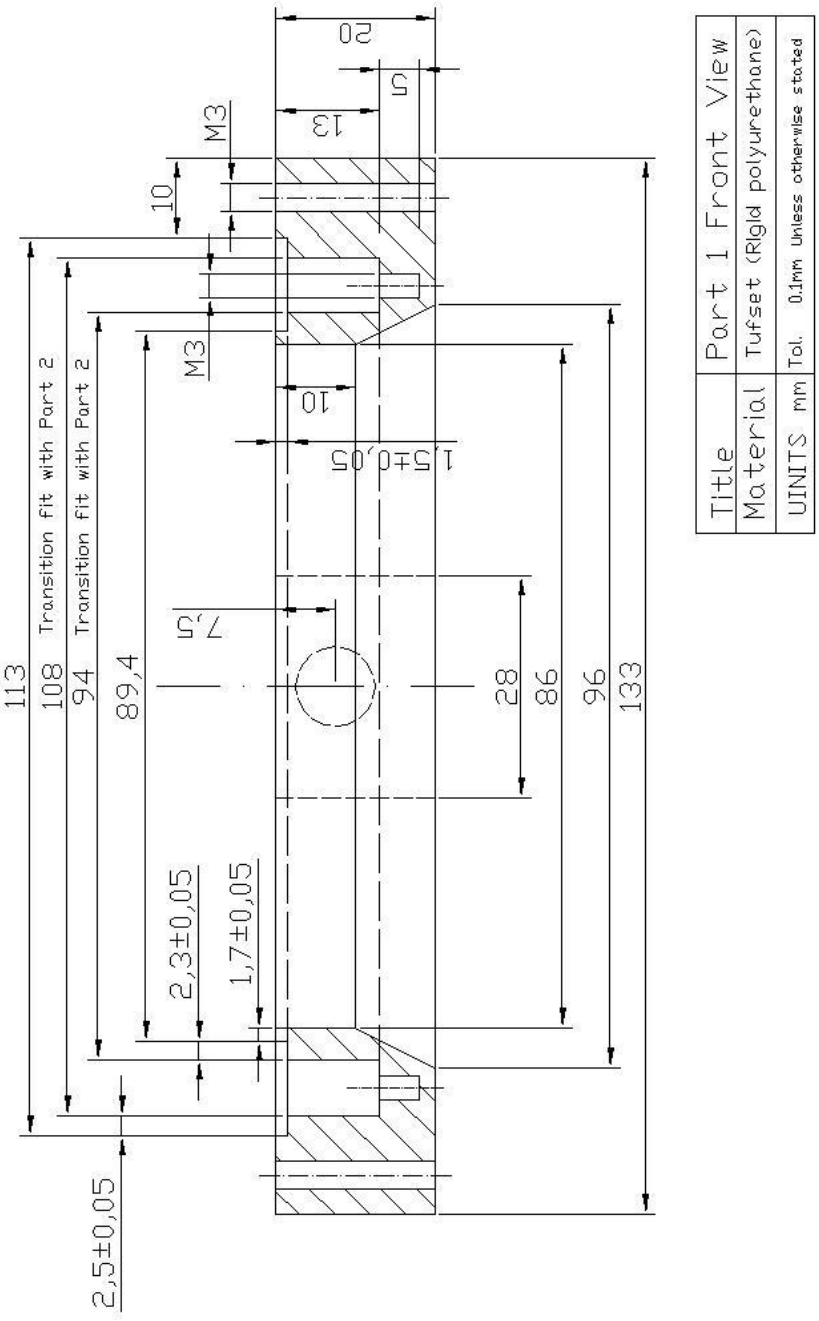
[161] Y. Tsuru, M. Nomura, and F. R. Foulkes, "Effects of chloride, bromide and iodide ions on internal stress in films deposited during high speed nickel electroplating from a nickel sulfamate bath," *Journal of Applied Electrochemistry,* vol. 30, no. 2, pp. 231-238, 2000.

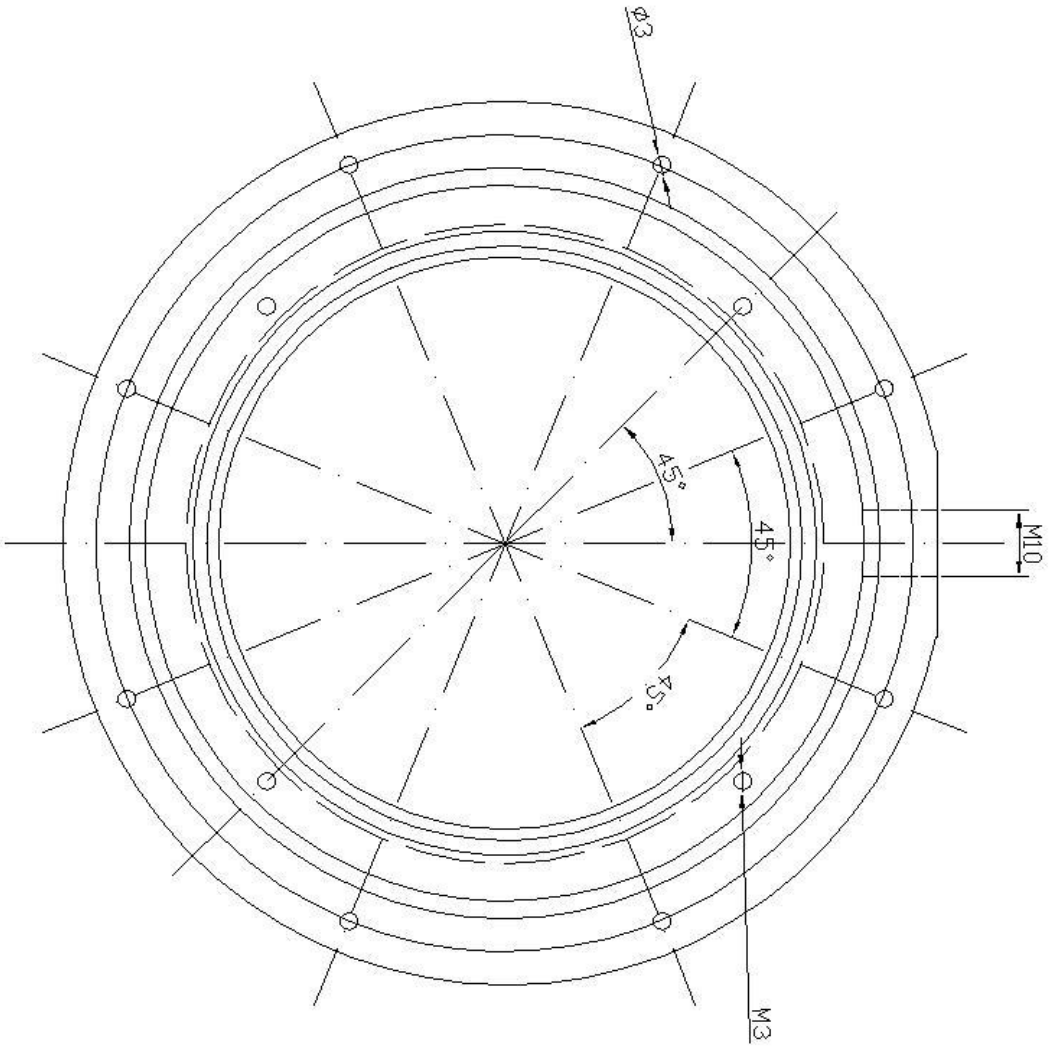
[162] A. A. Sonin, "Jet Impingement Systems for Electroplating Applications: Mass Transfer Correlations," *Journal of The Electrochemical Society,* vol. 130, no. 7, pp. 1501-1505, 1983.

[163] P. A. Kohl, "The High Speed Electrodeposition of Sn/Pb Alloys," *Journal of The Electrochemical Society,* vol. 129, no. 6, pp. 1196-1201, 1982.

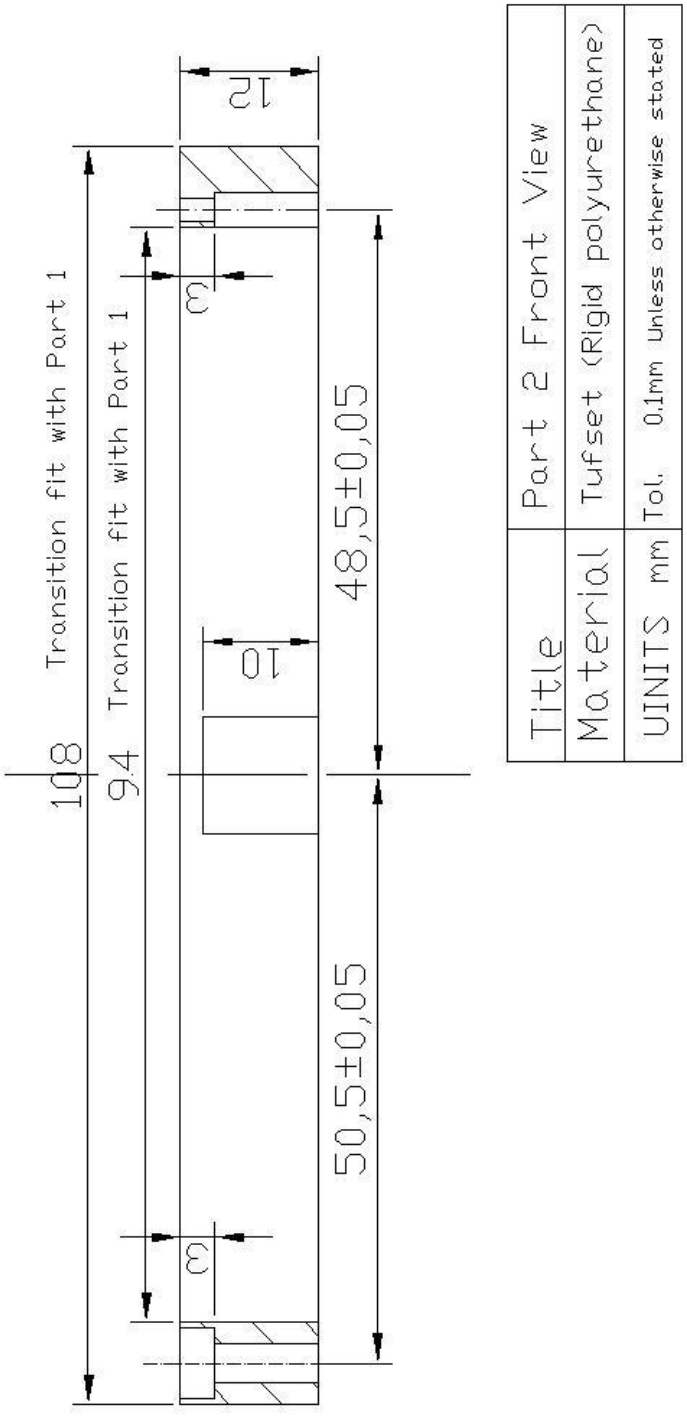
Appendix 1

Assembly parts of wafer holder for electroplating onto 4 inch wafer.

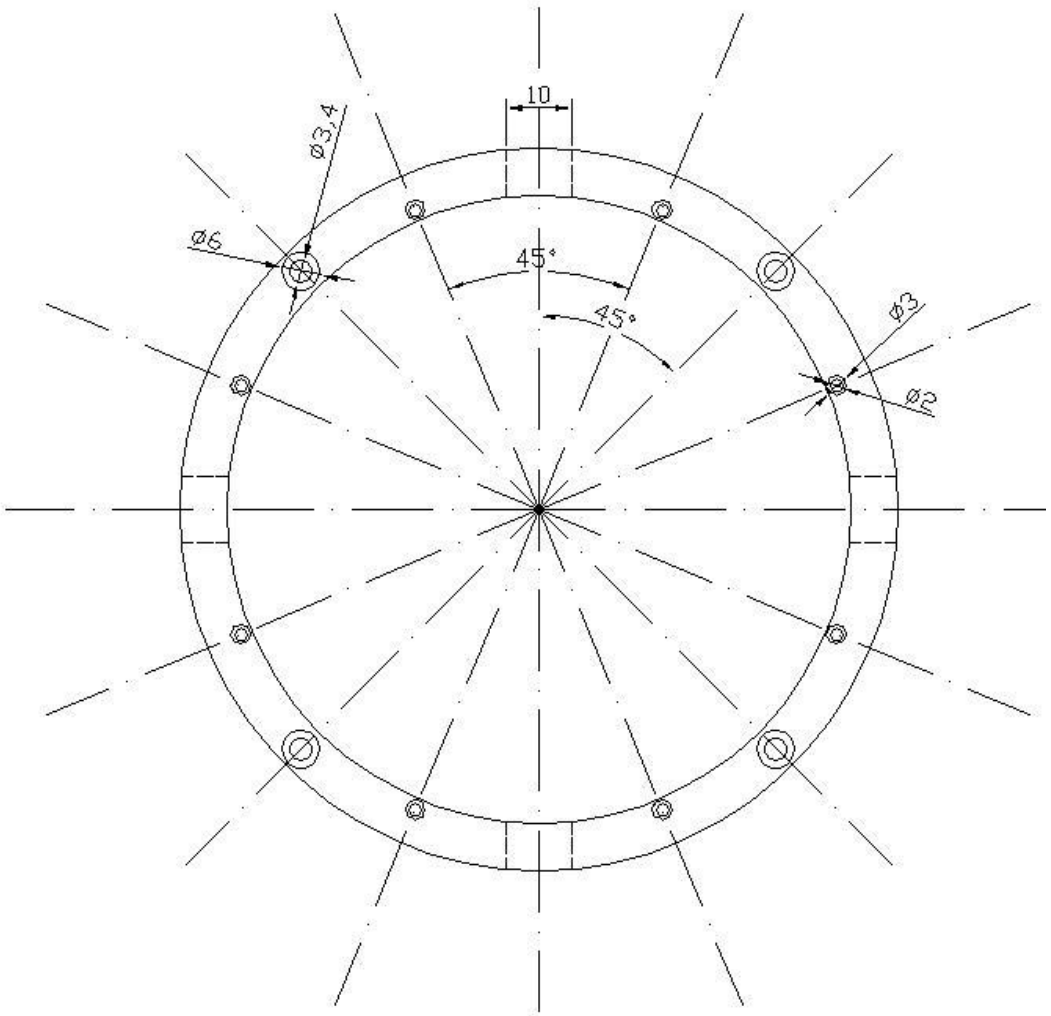




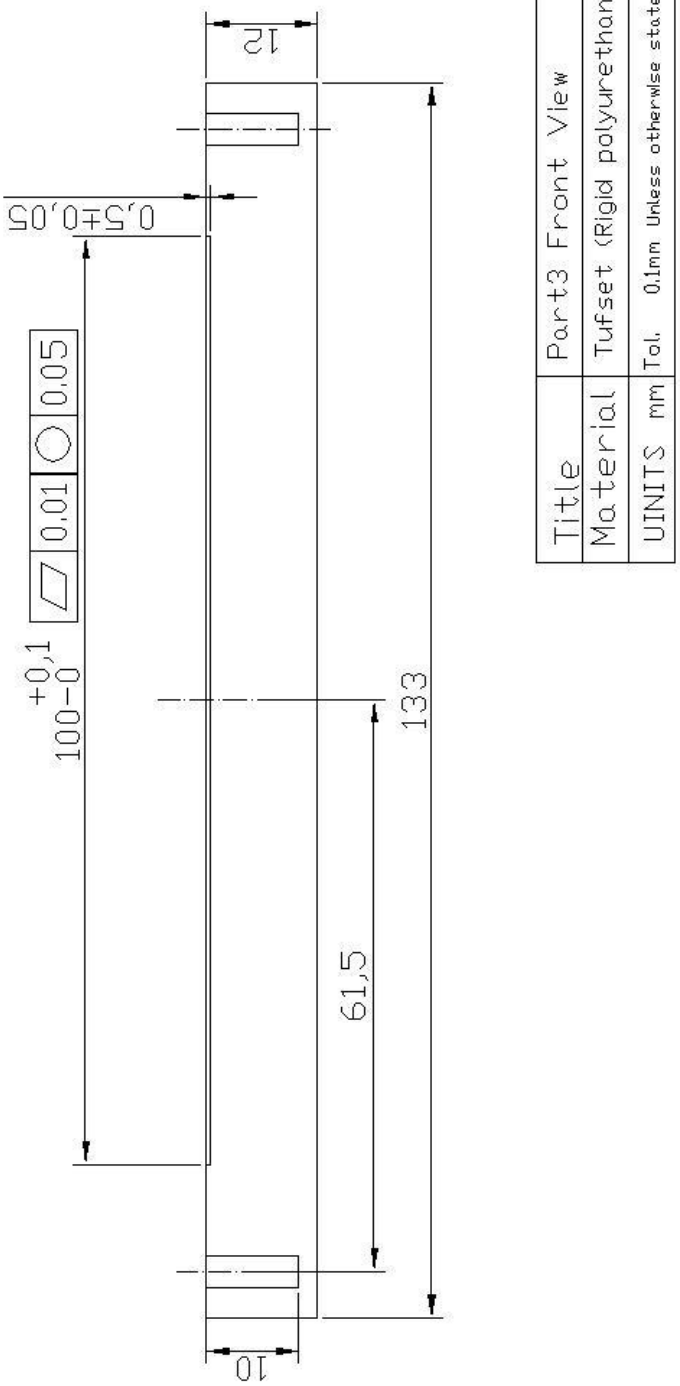
Title	Part 1 Top View
Material	Tufset (Rigid ployurethane)
UINITS mm	Tol. 0.1mm Unless otherwise stated

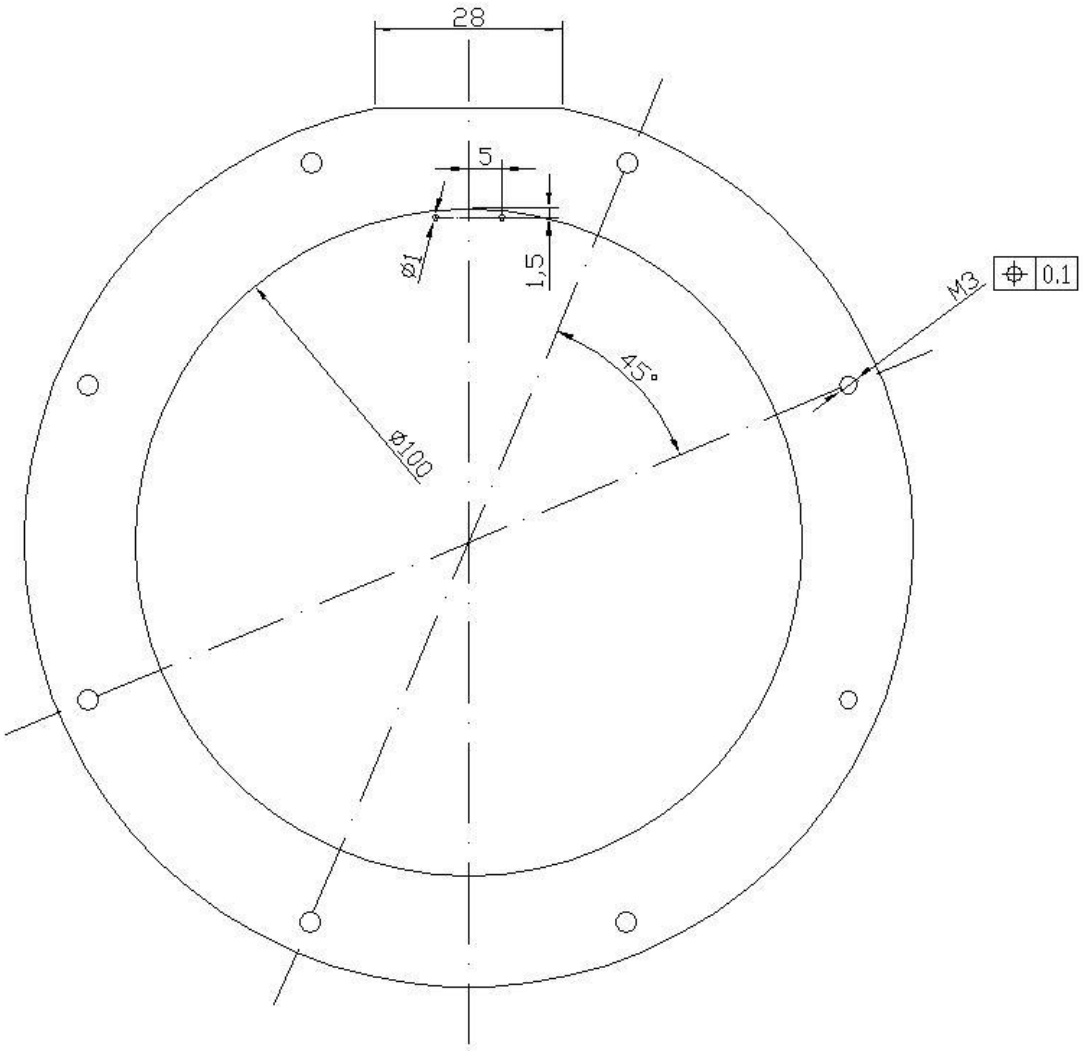


Title	Part 2 Front View
Material	Tufset (Rigid polyurethane)
UNITS mm	Tol. 0.1mm Unless otherwise stated

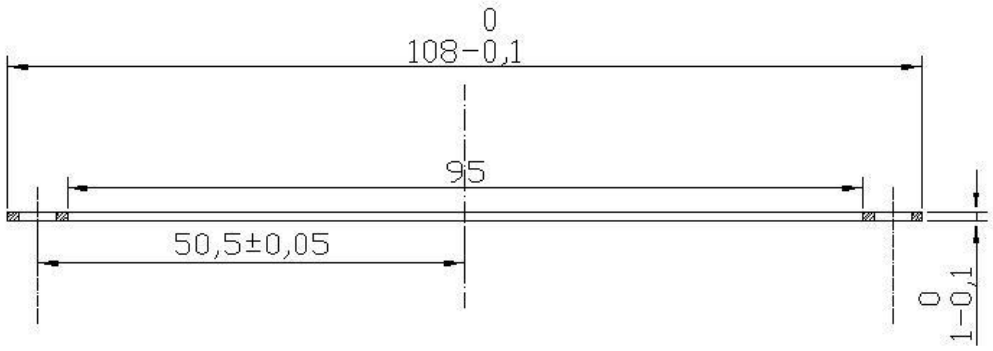


Title	Part 2 Top View
Material	Tufset (Rigid polyurethane)
UINITS mm	Tol. 0.1mm Unless otherwise stated

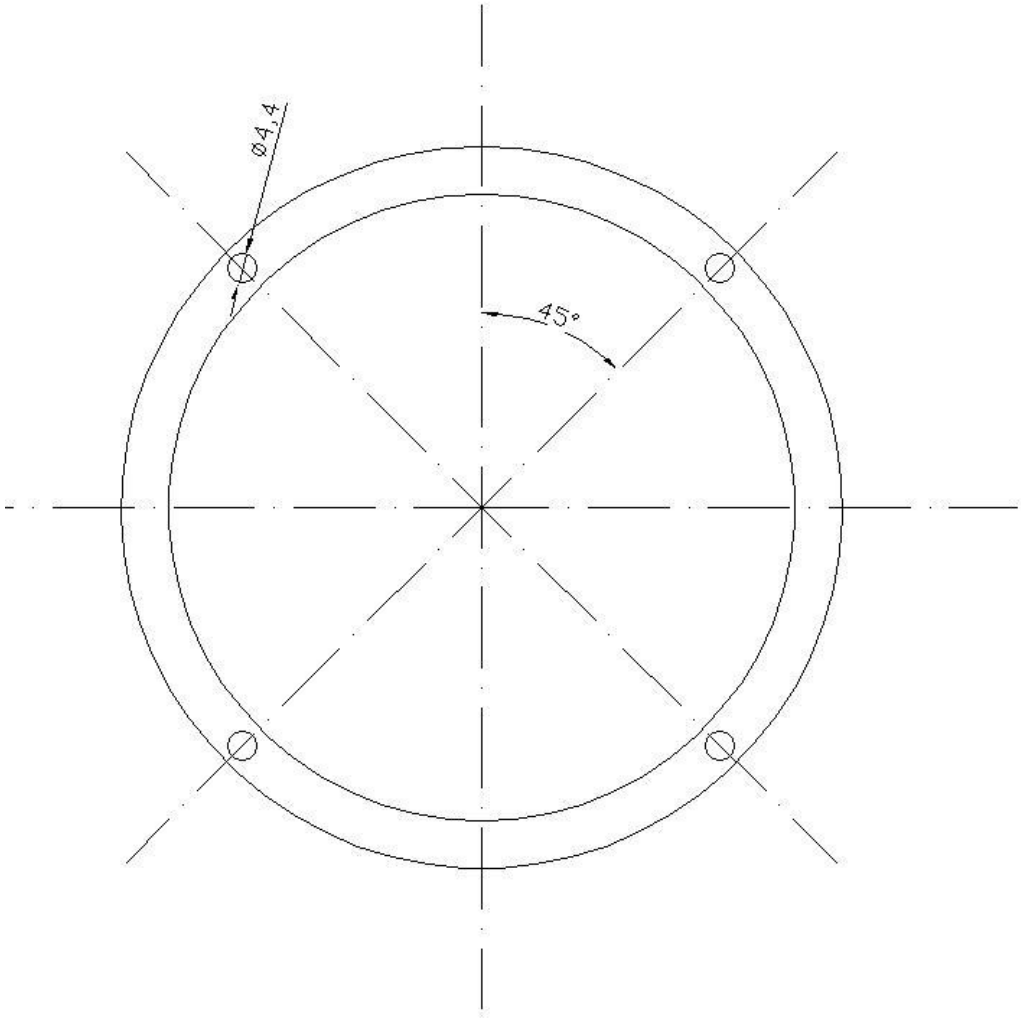

12
0,5±0,05
0,01
0,05
100+0,1-0
133
61,5
10
Title
Part3 Front View
Material
Tufset (Rigid polyurethane)
UNITS mm
Tol. 0.1mm Unless otherwise stated



Title	Part 3 Top View
Material	Tufset (Rigid polyurethane)
UINITS mm	Tol. 0.1mm Unless otherwise stated



Title	Steel Ring Front View
Material	Stainless steel
UINITS mm	Tol. 0.1mm Unless otherwise stated

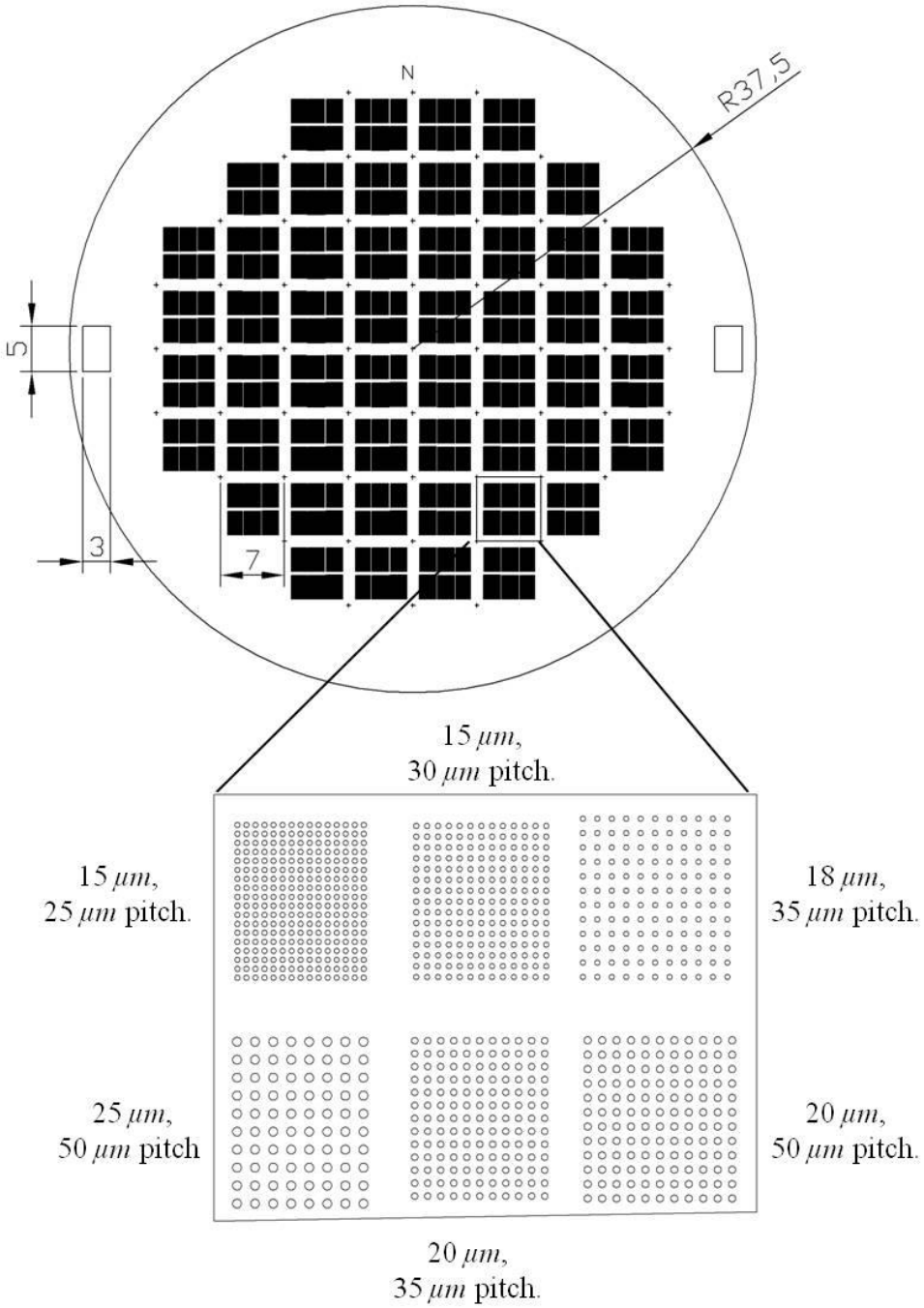


Title	Steel Ring Top View
Material	Stainless steel
UINITS mm	Tol. 0.1mm Unless otherwise stated

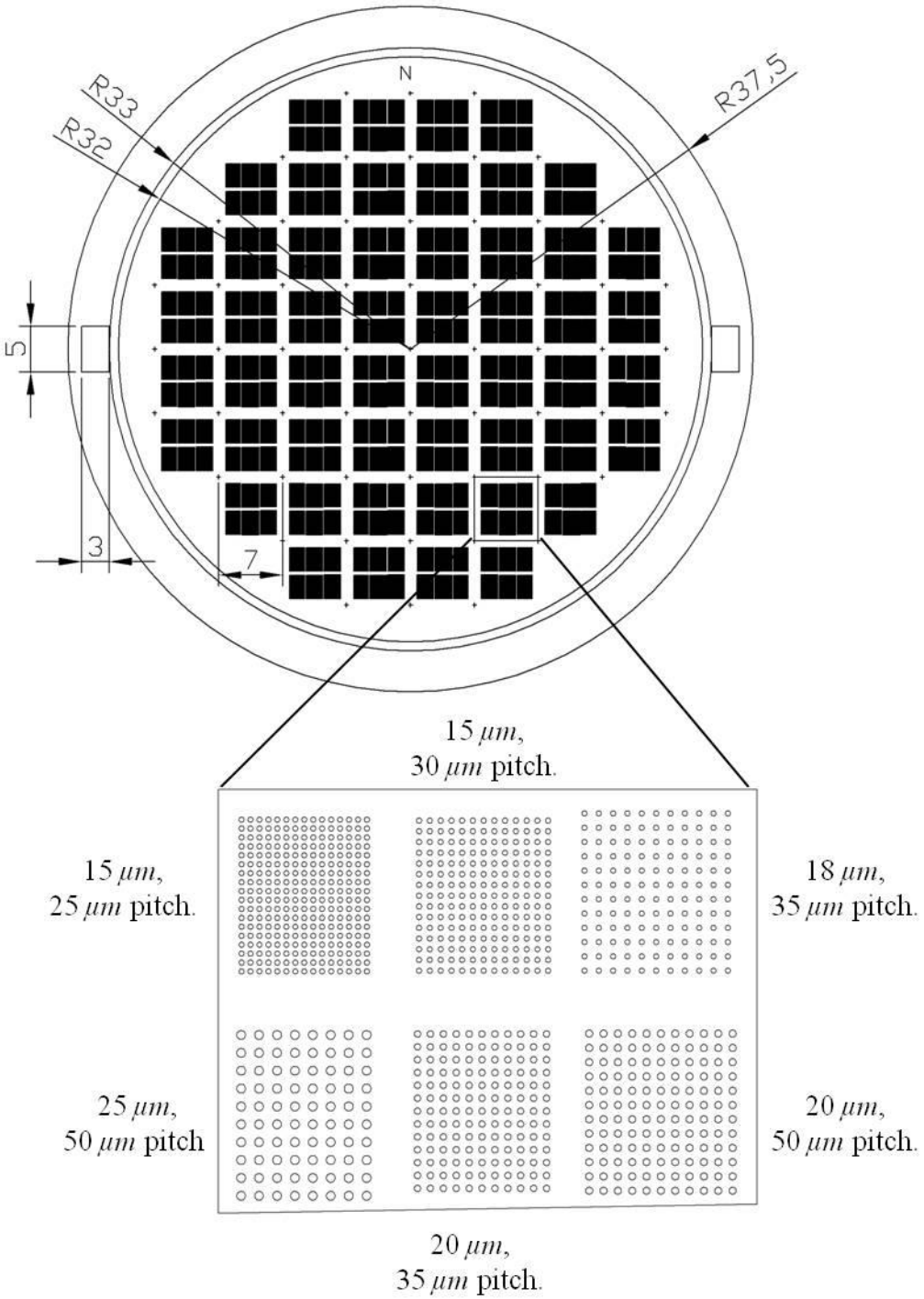
Appendix 2

Photomasks

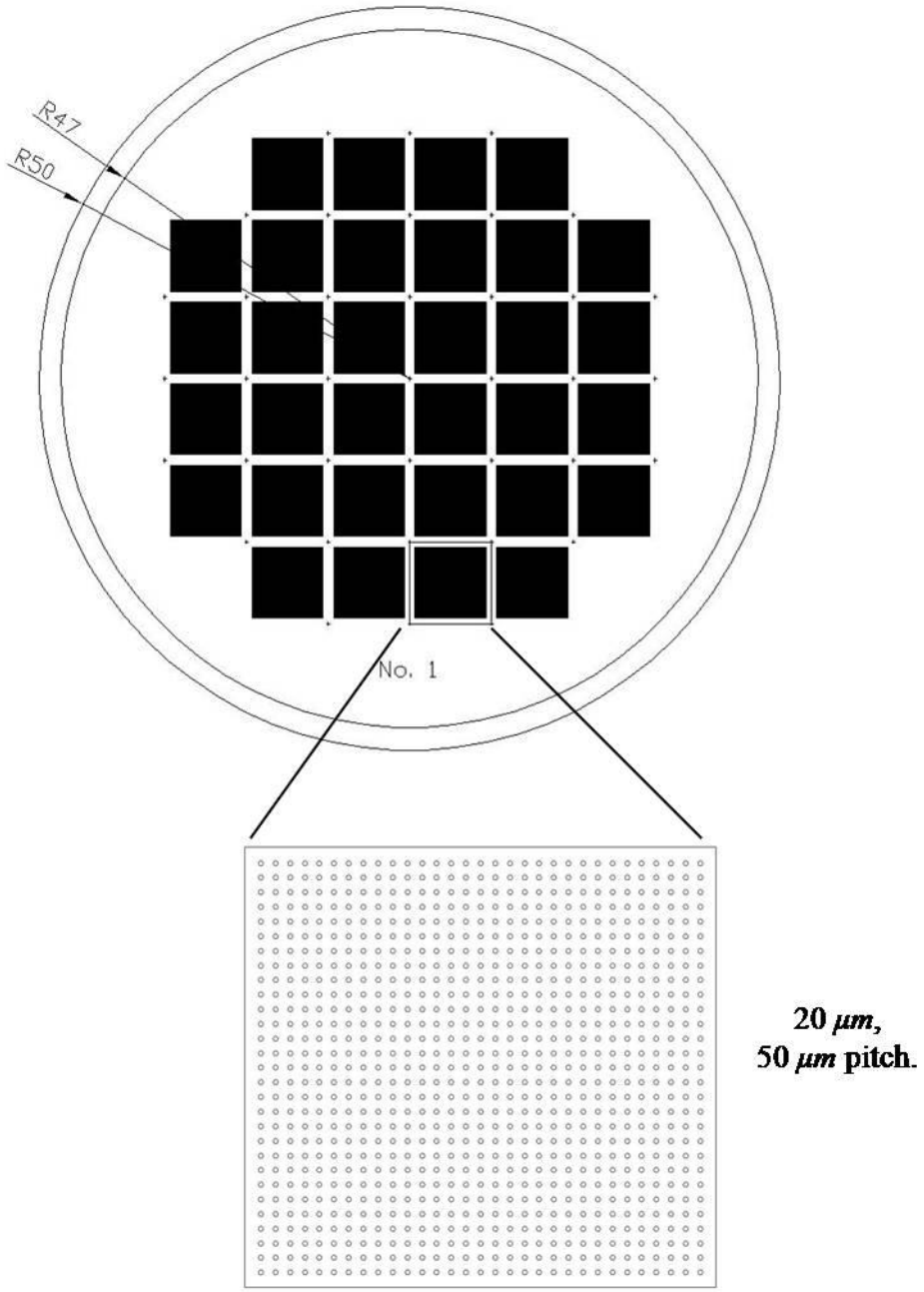
Note: All of the photomasks are in darkfield.



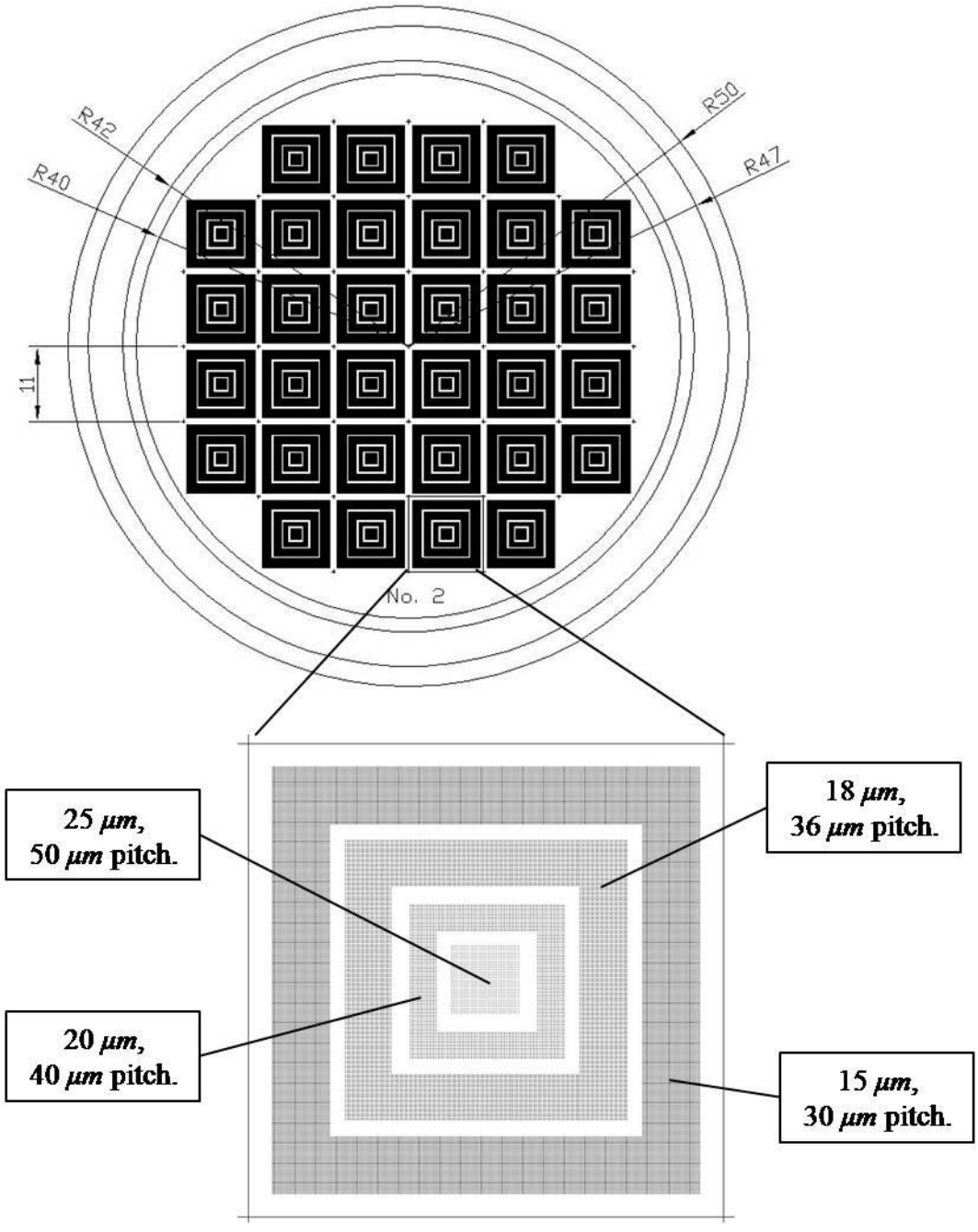
1. 3 inch photomask without thief ring.



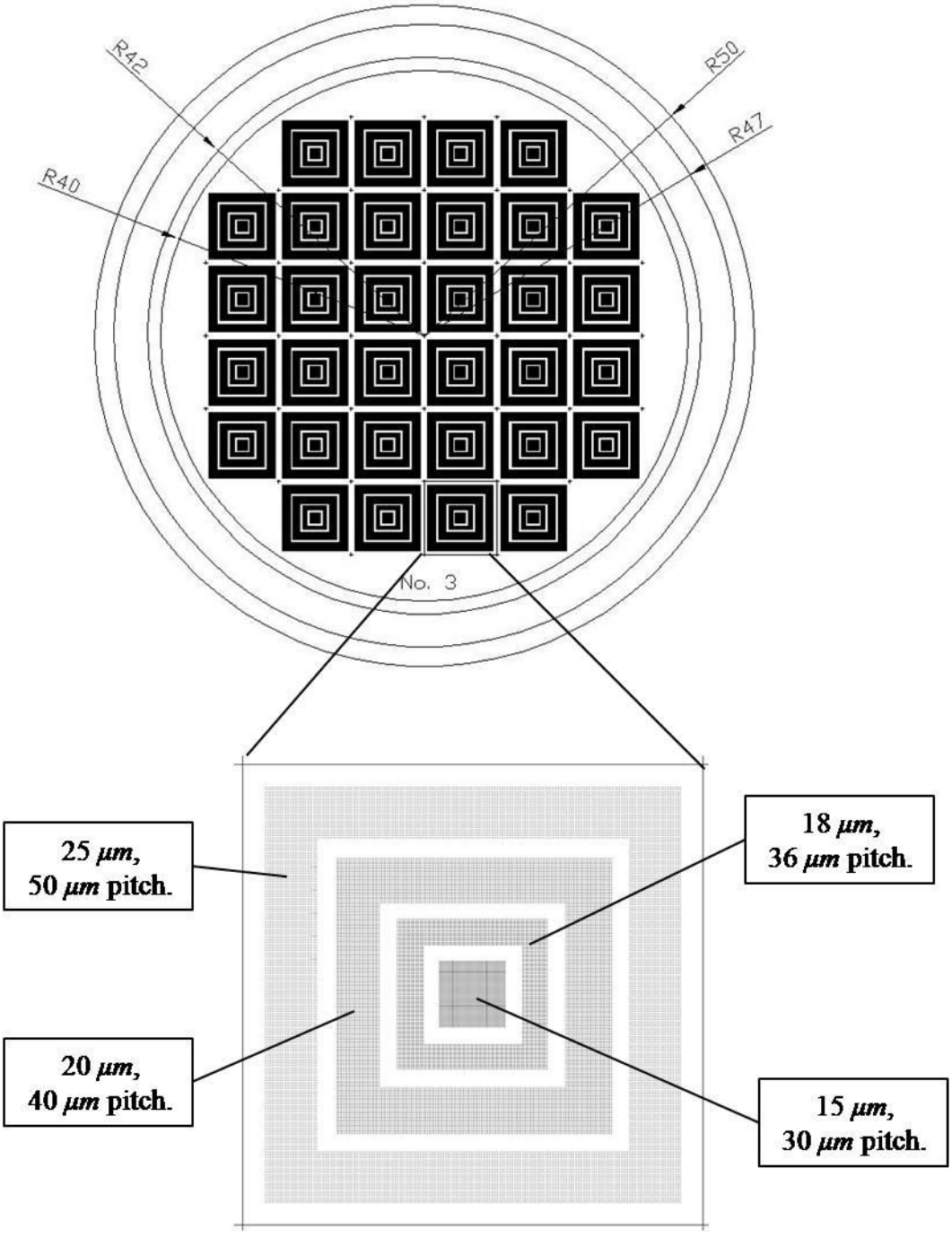
2. 3 inch photomask with thief ring.



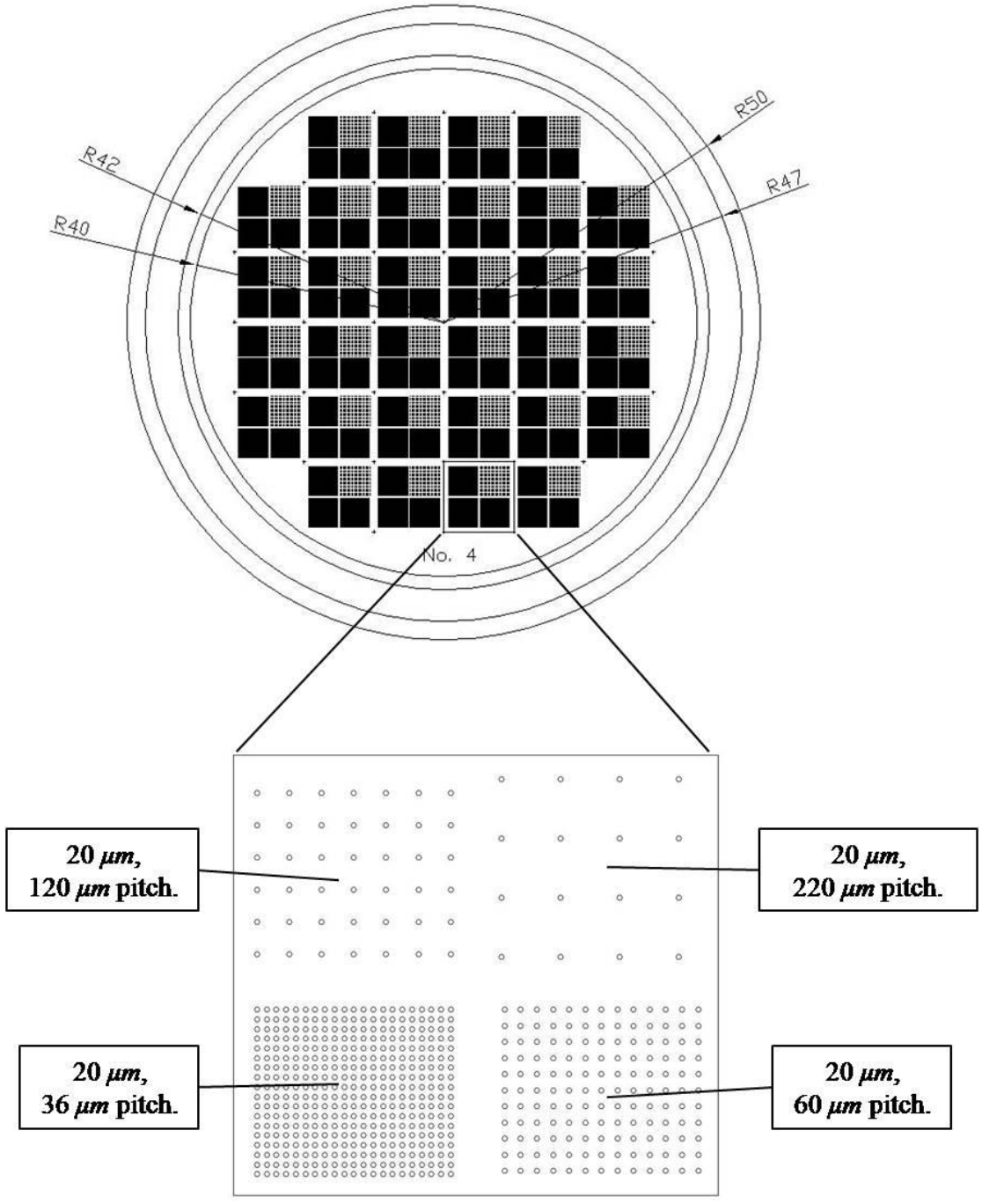
3. 4 inch photomask No. 1.



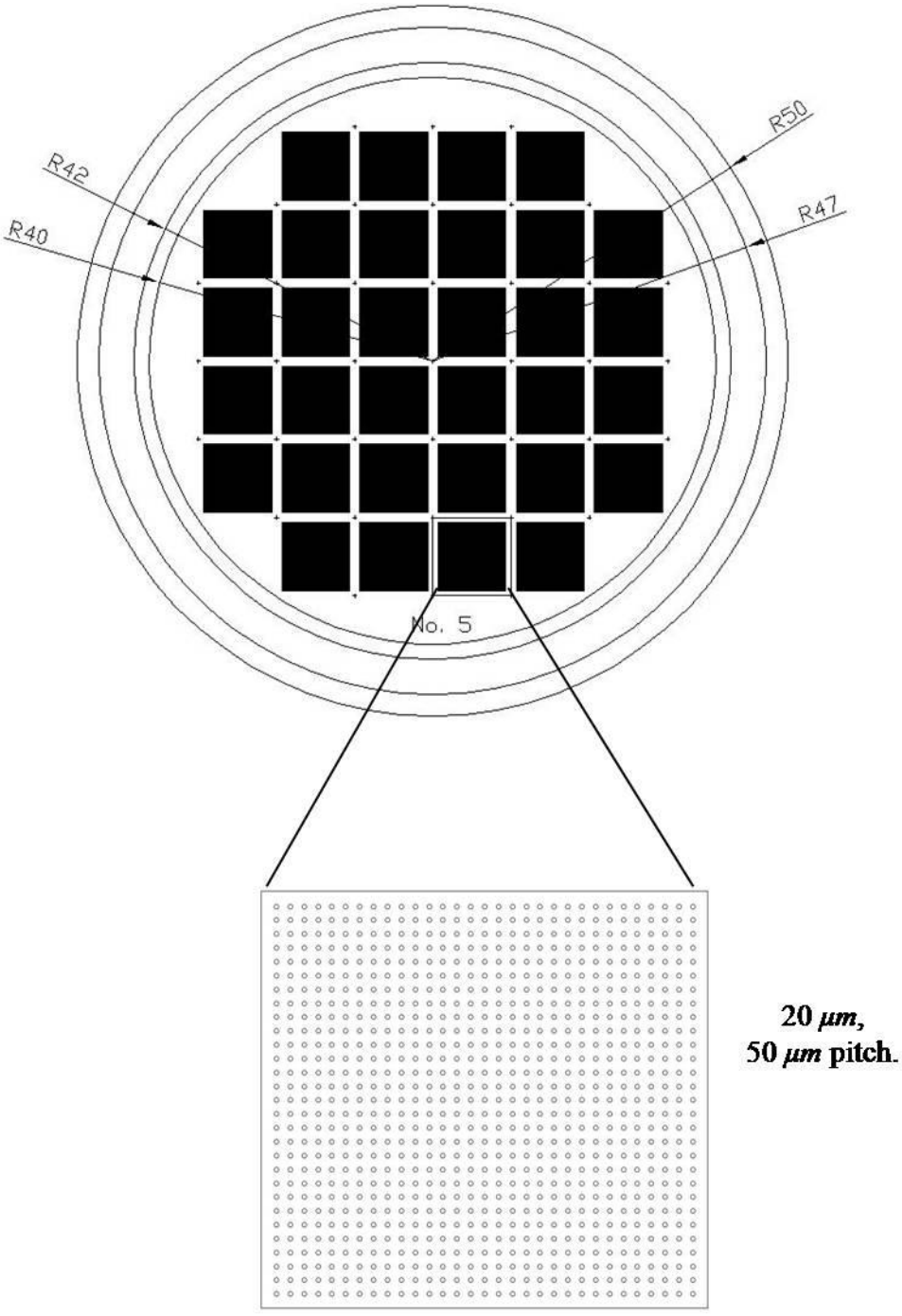
4. 4 inch photomask No. 2.



5. 4 inch photomask No. 3.



6. 4 inch photomask No. 4.



7. 4 inch photomask No. 5.