ADVANCED HIGH FREQUENCY SWITCHED-MODE POWER SUPPLY TECHNIQUES AND APPLICATIONS

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Abstract

This Thesis examines the operation and dynamic performance of a single-stage, single-switch power factor corrector, S^4PFC, with an integrated magnetic device, IM. Also detailed is the development and analysis of a high power light emitting diode, HP LED, power factor correction converter and proposed voltage regulation band control approach.

The S^4PFC consists of a cascaded discontinuous current mode, DCM, boost stage and a continuous current mode, CCM, forward converter. The S^4PFC achieves a high power factor, low input current harmonics and a regulated voltage output, utilising a single MOSFET. A steady-state analysis of the S^4PFC with the IM is performed, identifying the operating boundary conditions for the DCM power factor correction stage and the CCM output voltage regulation stage. Integrated magnetic analysis focuses on understanding the performance, operation and generated flux paths within the IM core, ensuring the device does not affect the normal operation of the converter power stage. A design method for the S^4PFC with IM component is developed along with a cost analysis of this approach. Analysis predicts the performance of the S^4PFC and the IM, and the theoretical work is validated by MATLAB and SABER simulations and measurements of a 180 W prototype converter.

It is not only the development of new topological approaches that drives the advancement of power electronic techniques. The recent emergence of HP LEDs has led to a flurry of new application areas for these devices. A DCM buck-boost converter performs the power factor correction and energy storage, and a cascaded boundary conduction current mode buck converter regulates the current through the LED arrays. To match the useful operating lifetime of the HP LEDs, electrolytic capacitors are not used in the PFC converter. Analysis examines the operation and dynamic characteristics of a PFC converter with low capacitive energy storage capacity and its implications on the control method. A modified regulation band control approach is proposed to ensure a high power factor, low input current harmonics and output voltage regulation of the PFC stage. Small signal analysis describes the dynamic performance of the PFC converter, Circle Criterion is used to determine the loop stability. Theoretical work is validated by SABER and MATLAB simulations and measurements of a 180 W prototype street luminaire.

Dedication

For my parents, for your constant drumming into me ‘never to give up’…. its been a long time in the making. And for all those school summers forced to do extra homework…. well…. this is the result!!

For Isabel, without you, your unquestionable support, your inspiration and your belief…this would have never been possible.

Copyright Statement

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Nomenclature

Symbol	Description	Unit
A_e	Effective core area	mm^2
A_l	Inductance factor	nH
A_w	Wire cross sectional area	mm^2
$A_{(n)}$	Input current harmonic	A
B	Flux density	T
$\hat{B}$	Peak Flux density	T
C	Capacitor	-
C_{oss}	MOSFET output capacitance	F
C_{iss}	MOSFET input capacitance	F
C_{rss}	MOSFET reverse transfer capacitance	F
C_{gs}	MOSFET gate source capacitance	F
C_{gd}	MOSFET gate drain capacitance	F
C_{ds}	MOSFET drain source capacitance	F
D	Duty cycle	-
E_c	Capacitor energy	J
f_{line}	Line frequency	Hz
f_{sw}	Switching frequency	Hz
f_c	Cross over frequency	Hz
f_p	Pole frequency	Hz
f_z	Zero frequency	Hz
G	Core air gap	mm
$G_c(s)$	Compensator transfer function	-
$G_{c\infty}(s)$	Compensator gain at high frequency	-
$G_{ea}(s)$	Error amplifier transfer function	-
$G_{vs}(s)$	Boost converter line-to-output transfer function	-
$G_{v_B}(s)$	Forward converter line-to-output transfer function	-
$G_v(s)$	S^4PFC line-to-output transfer function	-
$G_{vd}(s)$	CCM forward converter control-to-output transfer function	-
$G_{pmw}(s)$	PWM transfer function	-
$G_{oc}(s)$	Optocoupler transfer function	-
$G_{K_d}(s)$	Attenuator transfer function	-
$G_p(s)$	Buck boost control-to-output transfer function	-

h_{fe}	Amplification gain	dB
$H_z(s)$	Open loop transfer function	-
I_C	Capacitor current	A
$\hat{I}_C$	Peak capacitor current	A
I_D	Diode current	A
$\hat{I}_D$	Diode current	A
I_s	AC line current	A
$\hat{I}_s$	Peak AC line current	A
I_L	Inductor current	A
$\hat{I}_L$	Peak inductor current	A
I_{rec}	Rectified line current	A
$\hat{I}_{rec}$	Peak rectified line current	A
I_Q	MOSFET current	A
$\hat{I}_Q$	Peak MOSFET current	A
I_o	Output Current	A
$\hat{I}_{RM}$	Peak diode reverse recovery current	A
J	Current density	A/mm^2
L	Inductor	-
l_e	Effective core length	mm
l_w	Total wire length	m
M	Voltage transfer coefficient	-
n	Harmonic number	-
N_{fb}	Number of turns of feedback turns	-
N_L	Number of inductor turns	-
N_p	Number of primary transformer turns	-
N_s	Number of secondary transformer turns	-
N_r	Number of reset transformer turns	-
$N_{p,s}$	Primary/ Secondary transformer turns ratio	-
$N_{s,r}$	Secondary/ Reset transformer turns ratio	-
P_{in}	Power in	W
P_{in}	Power out	W
$P_{Q,cond}$	MOSFET conduction loss	W
$P_{Q,sw}$	MOSFET switching loss	W
P_Q	Total MOSFET power loss	W
$P_{D,cond}$	Diode switching power loss	W

$P_{D,sw}$	Diode switching power loss	W
P_D	Total diode power loss	W
P_{cu}	Copper loss	W
P_{core}	Core loss	mW/cm^3
P_s	Real power	W
Q	MOSFET	-
Q_r	Diode reverse recovery charge	C
Q_{sw}	MOSFET switching gate charge	C
Q_s	Diode on state storage charge	C
Q_o	Q-factor	-
Q_p	Reactive power	VAR
R	Resistor	-
$R_{ds_{on}}$	On-state MOSFET resistance	Ω
S	Diode snappiness factor	-
S_p	Apparent power	VA
S_d	Dielectric surface area	mm^2
T	Transformer	-
T_{line}	Time period of line frequency	s
T_{sw}	Time period of switching frequency	s
T_{on}	MOSFET on time	s
T_{off}	MOSFET off time	s
t_{on}	MOSFET turn on time	s
t_{off}	MOSFET turn off time	s
t_{rr}	Diode reverse recovery time	s
t_{rst}	Transformer reset time	s
V_B	Boost capacitor voltage	V
$\hat{V}_B$	Peak boost capacitor voltage	V
V_{bus}	Bus voltage	V
$\tilde{V}_{bus}$	Bus voltage high frequency ripple	V
V_L	Inductor voltage	V
$\hat{V}_L$	Peak inductor voltage	V
V_s	AC line voltage	V
$\hat{V}_s$	Peak AC line voltage	V
V_{rec}	Rectified line voltage	V
$\hat{V}_{rec}$	Peak rectified line voltage	V
V_Q	MOSFET voltage	V
$\hat{V}_Q$	Peak MOSFET voltage	V

V_D	Diode Voltage	V
$\hat{V}_D$	Peak diode Voltage	V
V_g	MOSFET gate voltage	V
$\hat{V}_g$	Peak MOSFET gate voltage	V
V_e	Effective core volume	mm^3
V_F	Diode forward voltage drop	V
V_o	Output voltage	V
v_{ce}	Current error amplifier voltage	V
v_e	Error amplifier voltage	V
x	Arbitrary coefficient	-
y	Arbitrary coefficient	-
z	Arbitrary coefficient	-
Z_o	Output impedance	Ω
ε	Dielectric constant	-
η_{PFC}	PFC stage efficiency	%
η_{CR}	Current regulator efficiency	%
ρ	Resistivity	Ωcm
μ_e	Effective permeability	-
μ_i	Initial permeability	-
$\sum(l/A)$	Core factor	mm^{-1}
ϕ_T	Transformer flux	Web
ϕ_L	Inductor flux	Web
ϕ_{IM}	Integrated magnetic	Web
θ	Phase angle	Degrees
ω_o	Pole at the origin	Rad/s
ω_p	Pole	Rad/s
ω_z	Zero	Rad/s
AC	Alternating current	A
ACCUFET	Accumulation field effect transistor	-
AI	Axial insert	-
BCM	Boundary conduction mode	-
BIBRED	Boost integrated buck rectifier energy DC/DC converter	-
BIFRED	Boost integrated flyback rectifier energy DC/DC converter	-
CCM	Continuous current mode	-
CCCM	Critical current conduction mode	-
CTR	Current transfer ratio	-
CCTV	Closed-circuit television	-

DC	Direct current	A
DCM	Discontinuous current mode	-
DMOSFET	Double diffusion MOSFET	-
EMC	Electromagnetic interference	-
ESR	Equivalent series resistance	-
ESL	Equivalent series inductance	-
EXFET	Extended trench field effect transistor	-
GaAs	Gallium arsenide	-
GaN	Gallium nitride	-
HID	High intensity discharge	-
HP LED	High power light emitting diode	-
HPFC	High power factor correctors	-
HPS	High pressure sodium	-
IGBT	Integrated gate bipolar transistor	-
IM	Integrated magnetic	-
InGaN	Indium gallium nitride	-
INVFET	Inversion trench field effect transistor	-
JFET	Junction field effect transistor	-
K_B	DCM transfer coefficient	-
LED	Light emitting diode	-
LISN	Line impedance stabilization network	-
LPS	Low pressure sodium	
MOSFET	Metal oxide field effect transistor	-
OPTO	Optocoupler	-
PCB	Printed circuit board	-
PI	Proportional integrator	-
PF	Power factor	-
PQ	Power quality	-
PWM	Pulse width modulation	-
RFI	Radio frequency interference	-
SBD	Schottky barrier diode	-
Si	Silicon	-
S^4PFC	Single-stage single-switch power factor corrector	-
SSPFC	Single-stage power factor correction	-
SiC	Silicon carbide	-
THD	Total harmonic distortion	-
UMOSFET	U-trench vertical MOSFET	-
UV	Ultra violet	-
VCD	Variable centre distance	-
YAG	Yttrium aluminum garnet	-
ZCS	Zero current switching	-
ZVS	Zero voltage switching	-

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other University or institute of learning.

Acknowledgement

No endeavour is ever successfully completed single handed, so I would like to extend my sincere gratitude to my two supervisors, Professor Andrew J. Forsyth and Doctor Roger Shuttleworth for their support, insight, guidance and great patience throughout these past years. Many thanks.

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I would like to also thank the mechanical workshop in The School of Electronic and Electrical Engineering, for manufacturing the the power converter chassis and the heat sink for the HP LED array.

Finally I would like to thank my friends in the Power Conversion Group at Manchester University for their support, friendship and assistance over the past couple of years.

"All men dream: but not equally. Those who dream by night in the dusty recesses of their minds wake in the day to find that it was vanity: but the dreamers of the day are dangerous men, for they may act their dream with open eyes, to make it possible."

T.E. Lawrence: *The Seven Pillars of Wisdom.*

About the Author

The authors interest in power electronics began during an industrial placement at the aerospace manufacturer TRW, Birmingham 2003, which led him to specialise in power electronics during his final year as an undergraduate. It was upon the completion of his first degree that two opportunities arose, an offer to study for a Doctor of Philosophy at the University of Birmingham and a position as a Knowledge Transfer Partner, KTP, at PSU Designs, Tipton. Realising that industrial experience is as essential for career progression as academic development, the KTP was adapted to incorporate the two.

After completing the KTP program, the author was appointed to the position of Research Assistant at the University of Manchester, 2005. Continuing with the PhD in power electronic systems part-time, other research was conducted in the field of fuel-cell electric vehicles, drive trains as well as power systems for high powered light emitting diode arrays. The author is currently employed at Pascall Electronics on the Isle of Wight, developing advanced switched-mode power electronic systems for the military aerospace and space industry.

The following publications have been written to date:

- D. R. Nuttall, S. V. Mollov, and A. J. Forsyth, "*Performance/Cost Comparison between Single-Stage and Conventional High Power Factor Correction Rectifiers*," in IEEE Power Electronics and Drives Systems, November 2005, Malaysia, pp.876-881.

- Calderon-Lopez, G., Forsyth, A.J., Nuttall, D.R., *"Design and Performance Evaluation of a 10-kW Interleaved Boost Converter for a Fuel Cell Electric Vehicle,"* Power Electronics and Motion Control Conference, vol 2, August 2006, pp. 1-5.

- F. Bryan, D. R. Nuttall, A. J. Forsyth, Y. Cheng, J. V., Mierlo, and P. Lataire, *"A Low-Cost Battery-Less Power Train for Small Fuel Cell Vehicle Applications,"* Vehicle Power and Propulsion Conference 2007, Texas, USA, pp. 1-7.

- Nuttall, D.R. Shuttleworth, R. Routledge, G., *"Design of a LED Street Lighting System,"* Power Electronics, Machines and Drives, 2008, York, UK, pp.436-440.

1 Advanced High Frequency Power Supply Techniques

1.1 Introduction

The proliferation of low power single-phase mains connected devices, has led to them becoming ubiquitous and a necessity for modern electronic equipment. These power supplies have become compact, reliable, robust, relatively inexpensive and are now incorporated into innumerable application areas. This has been made possible by the constant development of design techniques, modelling approaches and the emergence of new components. Power electronics engineers are under constant pressure to adopt new approaches to reduce converter component count, increase efficiency, reduce cost, increase converter power density and develop new applications. Two particular areas of interest in this thesis are; advanced power factor correction techniques and the recent emergence of high power light emitting diodes.

There is an ever present concern amongst utility operators regarding the magnitude of harmonic currents being drawn from the supply, the low power factor and the effect these have on voltage waveforms and power systems apparatus [1]. As a consequence, international legislation enforces power factor and harmonic current limits on equipment connected to the mains supplies. Table 1-1 shows an example of two such classes of harmonic limits. Class C , lighting equipment, limits of this standard are more stringent than Class D, domestic appliances consuming less than 600 W, as the second harmonic is bounded. Generally only the odd harmonics are considered.

The non-linear effects of mains connected power electronic loads produces currents in the mains supply which are not only at the fundamental frequency but at corresponding harmonics. These harmonic currents interact with the supply impedance causing distortion of the AC voltage waveform.

Power factor correction techniques have been widely recognized and successfully applied to electronic power converters in various guises in order to achieve a high power factor and low input harmonic currents [2-9]. Passive power factor correction is the simplest and most reliable way of correcting the non-linearity of a load. The use of linear inductors or

capacitors works very well with simple un-distorted loads, where the undesirable reactive component can be taken out with the addition of equal but opposite reactive components [10]. Furthermore, the passive approach itself does not generate any additional EMC noise [11]. Passive PFC approaches are either AC side solutions or DC, post rectifier, approaches.

Despite its simplicity, this approach has the disadvantage of generating a pulsed AC line current drawn from the distribution network, resulting in low rectifier efficiency and a less than ideal power factor [12]. This method is generally used for inexpensive and low-power electronic systems.

Table 1-1 Harmonic limits for; (a) Class C Equipment, (b) Class D Equipment [13]

(a)

Harmonic Order n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency
2	2
3	$30 \cdot PF^*$
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3

(b)

Harmonic Order n	Maximum permissible harmonic current per Watt mA/W	Maximum permissible harmonic current A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.20
$13 \leq n \leq 39$ (odd harmonics only)	3.85/n	See Table 1

$*\ PF^*$ is the circuit power factor

As opposed to passively wave-shaping the input current, power electronic equipment can be implemented to actively shape the input current, I_s to be sinusoidal and in phase with the input voltage, V_s. In principle if there is zero displacement between I_s and V_s a purely resistive load can be calculated, and the conditions for unity power factor can be satisfied. There is a vast array of literature dedicated to non-isolated active power factor correction. However it can be broadly classified as falling into the following topologies: boost, buck and

buck-boost converter rectifiers. All three operate on the principle of processing the accumulated energy in an inductor, during the transistor on-time, T_{on}, and transferring the energy to the output capacitor, during the transistor off-time, T_{off}.

These high output power, low output voltage converters are known as Power Factor Correctors, PFC, and require a relatively large output capacitance if the filtering of the second harmonic power pulsation is performed at the output of the PFC converter stage. The output voltage of these active PFCs are generally not at a suitable voltage for many practical applications, and require a further power stage to meet the load requirements. This implies that the power is processed twice: first by an input current shaping circuit, which also performs the low frequency storage, and a second circuit to perform the output voltage conversion, regulation and, optionally, provide galvanic isolation between the line and the output.

Figure 1-1 shows a simplified block diagram of an input rectifier, an active power factor corrector and a cascaded voltage regulator. This approach achieves a very high power factor, provides energy storage, galvanic isolation and accurate output regulation. Each power stage operates independently of one another through each of their respective control circuits. The PFC controller ensures a near unity power factor and the DC/DC controller ensures regulation and guarantees the required output transient response.

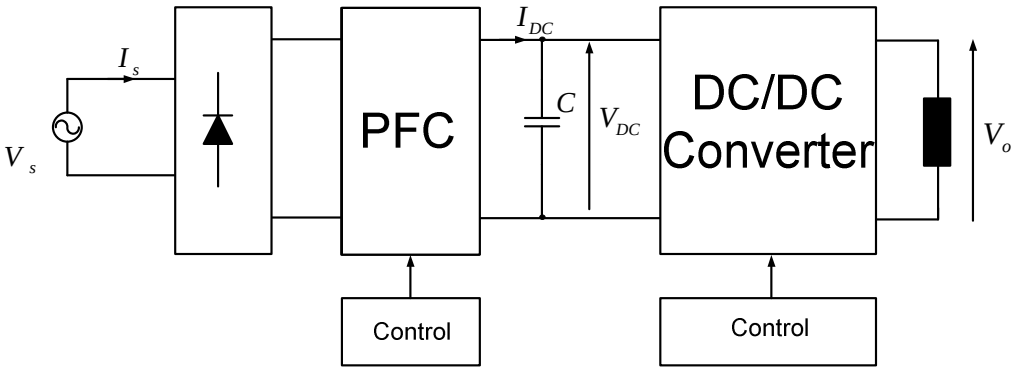


Figure 1-1 Conventional two-stage power factor correction block diagram

However, with the ever-increasing demand on the design engineer to improve the power density of the converter whilst reducing the cost, one is forced to investigate various methods to electrically integrate the circuits, for example the recent interest in Single-Stage Power Factor Correction, SSPFC. This concept combines the PFC stage and the secondary

voltage regulator stage into a single-stage, Figure 1-2. The apparent benefit is there is now only one power stage, that the conversion of power is more efficient and there is a significant reduction in component count [14]. A large number of single-stage power factor correctors have been proposed in recent years and are detailed in the literature survey in Section 1.2.4. Despite the number of single-stage topologies that have been proposed, the cost –performance benefits of the approach are not fully understood.

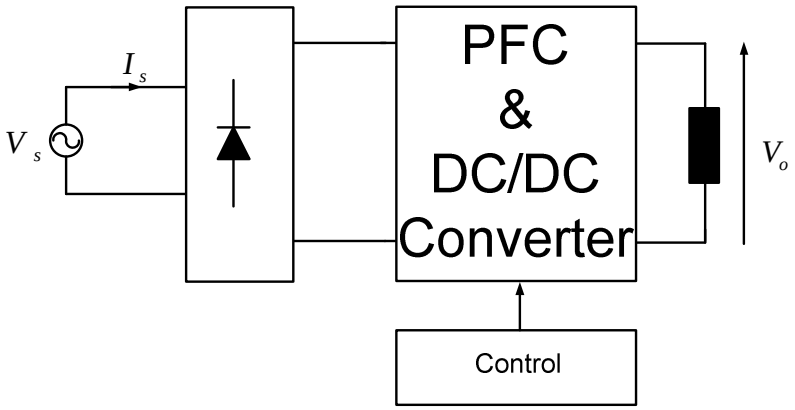


Figure 1-2 Proposed Single-Stage Power Factor Corrector

Another example of system integration is the development of Integrated Magnetic, IM, components [15-18]. There are broadly two classes of magnetic component used in high frequency power converters.

An inductor is a device primarily used for energy storage during a switching cycle. It generally has an air gap within the core to prevent core saturation and to store the energy. The power entering is not the same as the power leaving the core at any given moment.

A transformer performs instantaneous power transfer. Unlike the inductor, the power entering the device is the same as that leaving, neglecting any parasitic losses. Transformers are used for voltage and current scaling, galvanic isolation and on occasions, provide multiple outputs from a single source.

The IM approach involves the amalgamation of multiple magnetic components onto a single magnetic core. The implementation of this approach may give rise to the reduction of the size and cost of a power electronic converter [19-21]. Winding multiple magnetic

components onto a single core is not difficult, however the analysis, understanding and design, of such devices is complex.

The concept of integrating various magnetic components onto a single core is not a recent proposal as seen in [22-26]. An IM appears in numerous guises such as coupled inductors, which can exploit the phenomenon of current ripple steering [27] and ripple cancellation [28], or integrated transformers, that is two or more transformers on a single core, and finally integrated magnetics, the implementation of an inductive component and a transformer on the same core. The motivations for such approaches are to reduce the overall circuit component count, cost and to take advantage of any inherent functionality that arises with these methods [21].

It is not only the emergence of new design techniques and methods that is driving the development of power converter topologies, but also the emergence of new applications such as high power light emitting diodes, HP LEDs, [29]. The key characteristics of HP LEDs are; excellent reliability, instant turn on, dimmability, long life, approximately 50,000 hours, good colour and temperature rendering. Their efficacy is typically 100 lm/W in 2010, with manufacturers indicating that this value will improve [30].

The drive towards ever more powerful and adaptable, yet efficient, street luminaire systems is forcing the lighting industry to adopt new technologies. The most common street lighting systems today utilise high intensity discharge lamps, often Low Pressure Sodium, LPS. These lamps currently provide the highest optical output per unit of electrical input, 200 lm/W [31]. However, the amber colour of light that LPS lamps emit is not the most conducive for night lighting and white light has been shown to be the most beneficial in terms of obstacle perception, security and driver's reaction times [32, 33]. High Intensity Discharge, HID, lamps that emit white light are usually metal halide and have an efficiency of around 90 lm/W. However, these lamps take a number of minutes to reach ideal operating temperature and maximum efficiency, are not easily dimmable and have a maximum useful operating life time of 12,000 hours [31]. Street lamps in Europe currently burn on average for 4000 hours per year. This equates, for a typical city of 18000 lamps, each consuming approximately 150 W, to an electricity consumption of 11 GWh per annum.

Unlike conventional power or signal diodes, HP LEDs cannot be subjected to significant reverse voltage, 3V is typically the limit without irreversible damage occurring [34]. The simple option of connecting anti-parallel LED strings to the mains through current limiting impedances is not advisable since a severe 100 Hz optical flicker can occur, causing stroboscopic effects [35]. Stroboscopic effects are a serious issue for the lighting industry, since migraines and epileptic fits have been attributed to this phenomenon [36]. Optical illusions can occur, as rotating machinery subjectively appears to be stationary or apparently moving in an opposite direction, due to temporal aliasing [37, 38]. Additionally, closed-circuit television, CCTV, equipment can be affected if the refresh rate is not synchronised correctly, thereby corrupting the recorded image.

There are a number of commercially available solutions for driving high power LEDs. They broadly fall into the following categories; low power, <10 W indication lighting and illumination, medium power ≈ 20 W, halogen and spotlight replacements or indoor lighting, and finally high power 40-80 W, outdoor illumination and architectural lighting. To achieve the luminance level of a street light, typically 10,000 lumens, using HP LEDs requires a power supply that can deliver 180 W.

The requirements of this power supply would not only be to regulate the power to the HP LEDs, limit line harmonic currents and minimise total harmonic distortion, but achieve a long operational lifetime, comparable to the lifetime of the HP LEDs themselves. Therefore a string of LEDs supplied from the mains must be connected via an AC/DC converter regulator, to protect them from reverse voltage and mains voltage surges, a power factor corrector stage and a current regulating stage.

The light output from an HP LED is directly proportional to the device's forward current [39]. To ensure good control of light output and equal current through each LED, it is desirable to have the LEDs connected in a series string, and to control the current through the string so that it is constant despite mains voltage changes, see Figure 1-3.

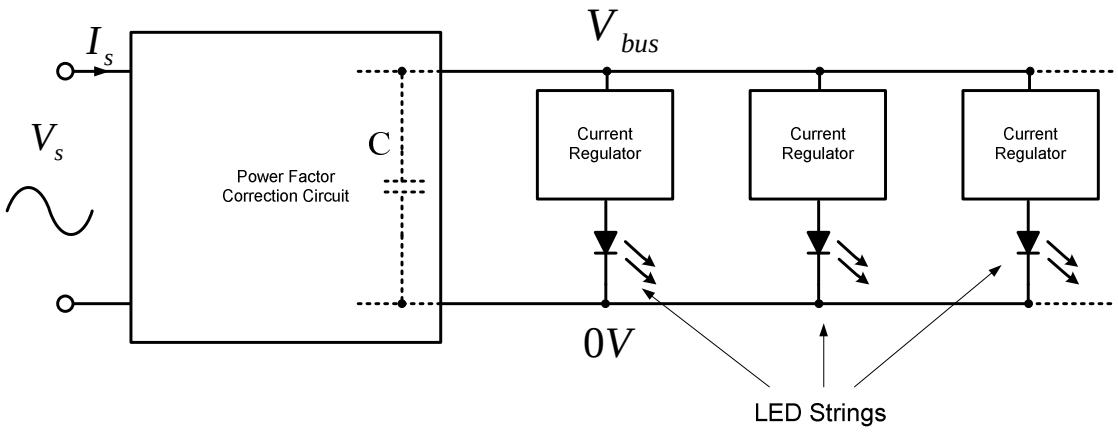


Figure 1-3 LED PSU block diagram

To achieve a long operational lifetime and overall system robustness, the PFC converter and current regulator must be able to operate for 50,000 hours. Typically, the life limiting factor for a switched mode power supply is the electrolytic capacitor that is used for voltage ripple limiting and energy storage. These devices degrade rapidly compared to HP LEDs, having a typical operating life of 7,000 hours [40], and are not suited for applications which are exposed to large ambient temperature variations, -40 ˚C to +40 ˚C, to which street lighting is subjected [41, 42]. However, inside a luminaire the upper temperature may reach 85 ˚C or more. There are electrolytic capacitors with longer lifetimes, 60,000 hours [43], however these are large and expensive. For an extended lifespan and low cost for the regulator, this component is not suitable.

Alternative capacitor technologies such as ceramic or metallised film are more suitable in terms of operational lifetime, [44] but they do not have the same charge storage capacity as an electrolytic device. In order to achieve a single 180 W HP LED driver, the power factor correction stage must limit line harmonic currents, minimise total harmonic distortion, all without the use of an electrolytic capacitor, whilst providing sufficient energy storage during the twice per cycle voltage zeros. Further, the elimination of the electrolytic storage capacitor not only impacts upon the power quality but may also result in additional demands on the control system performance.

By addressing these issues, the inherent capabilities of HP LED lighting can be exploited to provide benefits such as reactive lighting (dimmability), increased lumens per watt, and identification of luminaire failure/performance through intelligent communication.

Considering that street lighting authorities are obliged to pay a tariff for low power factor, ideally the fundamental component of the current should be in phase with the voltage to minimise cost. These techniques can all help reduce the current yearly carbon emissions of street luminaires.

1.2 Literature Review

The objectives of this section are to review the issues detailed in Section 1.1 and how current techniques and topologies can be implemented to address them. Power factor correction techniques are reviewed along with research being conducted to develop single-stage power factor correctors. Integrated magnetics methods are explored to see how this approach can further enhance a power topology. A review of control approaches and requirements is detailed for topologies operating as power factor correctors or voltage regulators. The characteristics of HP LEDs are reviewed along with the operational requirements and key issues of the HP LED driver. Finally a discussion of modern power electronic devices is conducted.

1.2.1 Power Factor Correction Techniques

A review of passive and active power converter topologies approaches follows. These circuits ensure a high PF and limited line current harmonics. The review is not an exhaustive list of topologies, but serves to provide a fair and representative selection.

As introductory texts to this subject, five particular publications highlight the general aspects and themes of the fundamental principles of power factor correction and power conversion techniques [8, 10, 45-47]. These references discuss the fundamental theory and analyses of power factor correction methods, and in particular highlight the two main approaches utilised when limiting unwanted harmonic currents and poor power factor. These solutions fall into two general categories; passive power factor correction and active power factor correction.

1.2.2 Passive Power Factor Correction

Passive power factor correction is the simplest and most reliable way of improving the power factor of a load. Passive PFC approaches can be categorised as either AC side or DC, post rectifier, approaches.

The less common approach of AC side PFC is an LC filter in series with the mains input. Figure 1-4 (a) shows this arrangement, the distortion in the line current is reduced by adding a large inductance. However, the output voltage, power and power factor will be reduced, due to the added series impedance. Figure 1-4 (b, c) shows resonant pass and resonant trap circuits that are sensitive to both frequency and load [48].

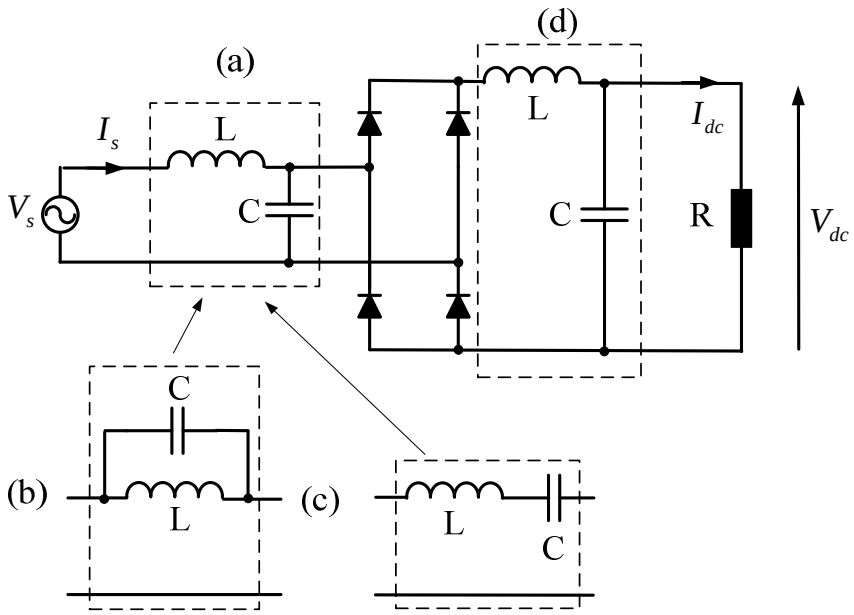


Figure 1-4 Passive power factor correction (a) AC side LC filter, (b) Parallel resonant PFC, (c) series resonant PFC, (d) DC side LC filter

The parallel resonant tank filter presents an infinite impedance to the third harmonic input current, resulting in a lower value of input peak current. An alternative approach is the series resonant filter that is designed to be resonant at the mains frequency. The quality factor, Q, is high in this method and the impedance of the circuit is high at frequencies far from the mains frequency, so that only mains frequency currents may pass, resulting in a near unity power factor. The most common passive approach is DC side PFC, after the AC rectifier diodes, Figure 1-4 (d). The maximum output power is independent on the inductance value, but the distortion cannot be reduced below 48% [11].

Other passive PFC approaches, such as the Valley-Fill approach [49], rely on the use of additional diodes and capacitors to change the effective circuit at various stages of the charge and discharge cycle. This topology is not strictly passive, as there is no LC filter, but it can be considered such as due to the passive switching action of the additional diodes.

The passive PFC approach can be further adopted to incorporate other functions such as integrated EMC control. The power electronic devices utilised in a power switching systems inherently produce electromagnetic interference, which can be transmitted by: radiation and conduction. To attenuate these unwanted effects, the topology presented in [50] attempts to integrate the functionality of a passive PFC and an EMC filter as one stage.

1.2.3 Active Power Factor Correction

The more common approach to perform PFC is to actively shape the input current, I_s, to be as near sinusoidal and in phase with the input voltage, V_s, as possible. In principle, if there is zero displacement between I_s and V_s, and the current is sinusoidal, then a purely resistive load is emulated, the conditions for unity power factor are satisfied.

The boost converter can be considered to be the most basic topology in use for active power factor correction and is also the most commonly implemented. The fundamental operation of this configuration as a power factor corrector is detailed in [10, 45, 46]. The converter can operate in Continuous or Discontinuous Current Mode, CCM / DCM respectively. A CCM boost PFC converter can easily achieve unity power factor, however there is a requirement for a large value of inductor, L, to maintain CCM in all operating conditions, and a relatively complex control circuit, see Section 1.2.5.

Operating in DCM however, can eliminate the need for a complex control circuit and reduce the size of the inductor [51]. Control circuit simplification is due to the inherent characterisitcs of the DCM. By analysing the input current in the discontinuous mode, the average current across a switching cycle is approximately proportional to the input voltage. Therefore if the duty ratio is constant throughout a line cycle, the circuit has a constant input resistance characteristic, the input current therefore tends to track the variations in input voltage [52]. Moreover, since the inductor current is zero before the start of the next switching cycle power loss is reduced, particularly diode reverse recovery loss, due to zero current switching, ZCS. This is the case for all active PFC converter topologies operating in DCM.

The boost PFC has the merits of high power conversion efficiency and low total harmonic distortion, THD, but it generates a higher DC voltage at its output, V_{DC}, compared to the input voltage, V_s. This is an advantage since it allows the input current to be shaped over

virtually the full utility line cycle. Some applications however may require a lower V_{DC}, in which case the boost topology alone would be unsuitable.

Another conventional topology suitable for PFC, is the buck converter [45, 53]. Like the boost topology, the buck converter is a highly efficient converter when operating in CCM. But other attributes are its ability to limit inrush currents, prevent short circuit conditions between line and output and obtain a lower DC output voltage with respect to its input. However to achieve CCM and low output current ripple tends to require a physically large inductor, often leading the buck converter to be dismissed as a PFC converter. Finally, the buck converter, like the boost has the ability to operate in DCM.

In the buck-boost converter, the output voltage can be higher or lower than the input voltage [45, 47], albeit inverted. In universal input PFC applications, this ability to both step-up and step-down V_{DC}, is a major attraction. Cascading a boost converter and a further down-stream buck converter can achieve the same outcome, but at a cost of a lower efficiency as the power is processed twice. The buck-boost also has similar attributes to the buck converter, as it has the ability to limit inrush current and prevent against over current conditions during short circuits. Finally, like the previous converters the buck-boost has the ability to operate in either CCM or DCM.

However the quality of the input current waveform and the ability to perform PFC differs greatly between the circuits [5]. Figure 1-5 shows the input current-voltage characteristics for a discontinuous current mode boost converter. It can be noted, that as long as the output voltage, V_{DC}, is larger than the peak of the line voltage, $\hat{V}_s$, then the correlation of V_s and I_s is near linear. The non-linearity is due to the fall time, δT_{sw}, of the inductor current to zero, which varies over a input line cycle, The effects of the non-linearity can be reduced by increasing V_{DC} with respect to $\hat{V}_s$, which diminishes δT_{sw} [5, 54].

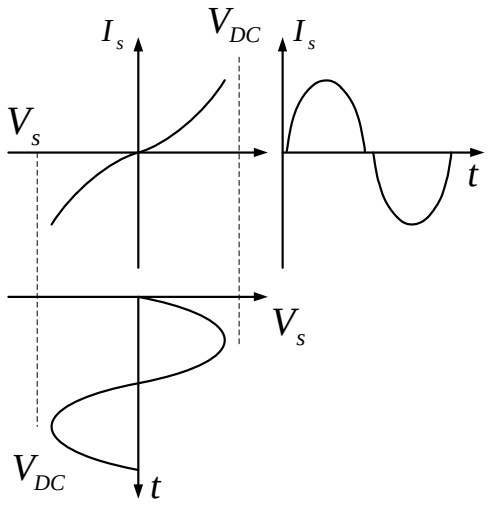


Figure 1-5 DCM boost converter input I-V characteristics

Unlike the boost converter, the buck-boost inductor is not always electrically connected to the line supply, therefore the fall time of the inductor, δT_{sw}, is not seen by the line input. The average input current of this converter is seen in Figure 1-6. It shows a linear relationship between I_s and V_s. This in turn forces the I_s to be sinusoidal and in phase with V_s and with a near unity power factor.

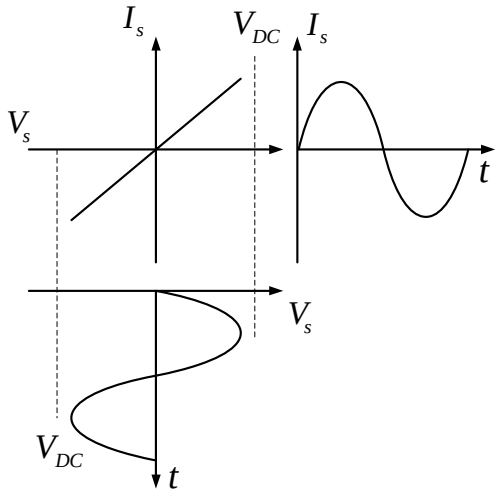


Figure 1-6 DCM Buck-boost input I-V characteristic

Automatic input current wave shaping is not without its issues, as the DCM inductor is relatively small and the power semiconductor devices are subject to larger switching current

and voltage stresses, which can limit the power throughput. Techniques such as interleaving is one approach to increasing this power limit [55, 56].

As well as limiting the input current harmonics and ensuring a low total harmonic distortion of the line current, the PFC stage also provides a means of energy storage [57]. The power flow into the energy storage capacitor, C, in Figure 1-7, is not constant, but is a sine wave at twice the line frequency, since the power is the instantaneous product of the rectified line voltage, V_{rec}, and current, I_{rec}. The output capacitor stores energy when the absolute instantaneous value of V_s is higher than V_{DC} and releases the energy when the instantaneous value of V_s is lower than V_{DC}, in order to maintain a constant power flow. This flow of energy in and out of C, results in a V_{DC} ripple voltage at the 2nd harmonic.

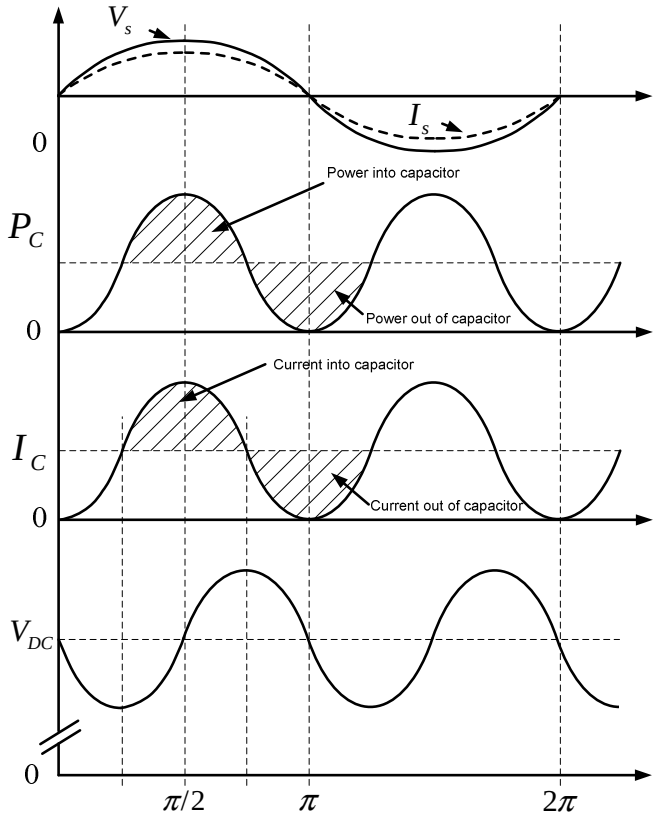


Figure 1-7 Energy storage performed by PFC capacitor

1.2.4 Single-Phase Single-Stage Power Factor Correction

The approaches discussed in the previous sections relate to achieving the harmonic specifications shown in [1], high power factor and second harmonic energy storage. However,

most practical applications require a further conversion of this intermediate voltage. A second converter stage is often used for fast dynamic regulation of output voltage, used to step up or down the voltage, and to limit voltage or current ripple to desired requirements. The most common approach is to cascade a second switching DC/DC converter to regulate the output voltage and current ripple as seen in Figure 1-1. As these two power stages are controlled separately, optimisation of the two power converters, in terms of high power factor and fast output voltage regulation, is possible. However, the two-stage approach has the disadvantage of increased cost and physical size due to the component count and the two control circuits [58]. The block diagram also implies that the power is processed twice, reducing the overall efficiency.

The single-stage approach for addressing power factor correction is depicted in Figure 1-2. It can be seen, the major advantage of this method is not only the power being apparently processed once but, more significantly, only one control block is required reducing the component compared with the two-stage approach.

A large number of single-stage PFC circuits have been proposed in recent years, and this section aims to present a representative survey. The concept of single-stage power factor correction converters dates back to [59]. The converter presented is a single phase offline converter providing independently controlled dual outputs, but has the disadvantages of a high component count. It suffers wide switching frequency variations and high voltage stresses. It nevertheless integrates a PFC converter with a cascaded DC/DC converter.

Many single-stage PFC converters are a cascaded combination of an input current shaper converter and a DC/DC converter. In some the energy storage is in series with the power flow, and in others the energy storage is in parallel with the power flow [60].

A common example of a series type single stage power factor corrector is the boost integrated buck rectifier energy DC/DC converter, BIBRED, and the boost integrated flyback rectifier energy DC/DC converter, BIFRED, proposed in [61, 62] and in Figure 1-8. These converters are purely a cascaded connection of a boost converter performing the role of the input current shaper, and either a buck or flyback converter performing the role of output voltage regulation.

Despite their apparent simplicity in design, and the need for only one control loop, a common operational failing with these converters is the DC bus voltage level, across C_b, at high line voltage and low load conditions, which makes these converters, if unmodified, unpractical to implement.

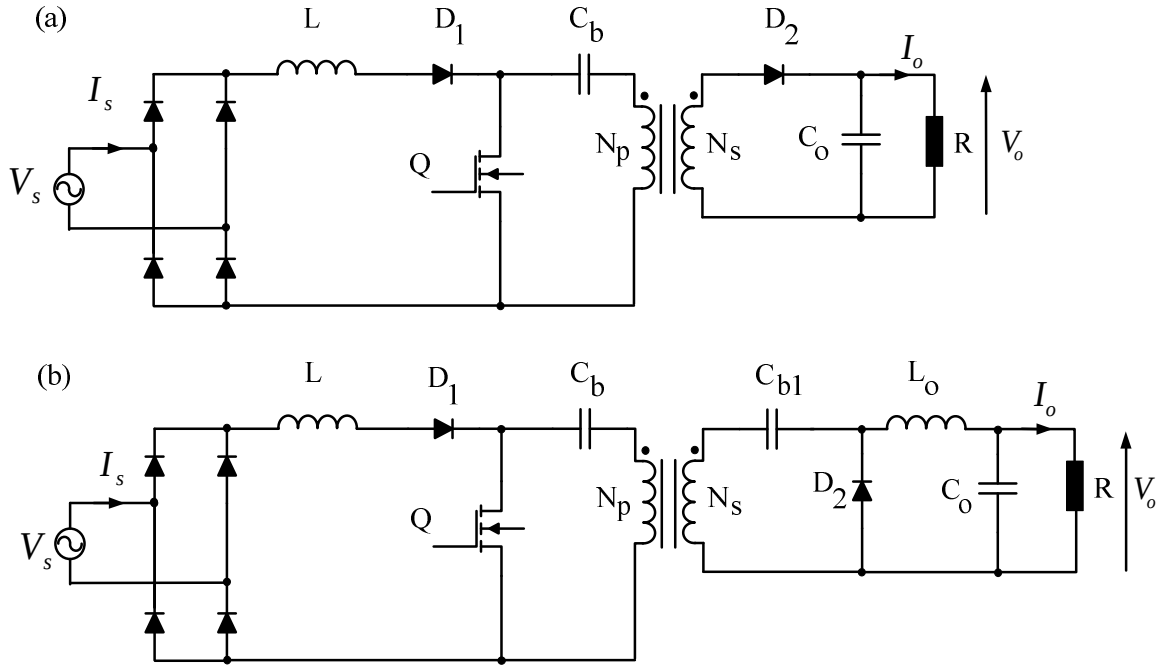


Figure 1-8 (a) BIFRED single-stage PFC, (b) BIBRED single-stage PFC

Numerous suggestions have been proposed to address this issue, in [63], a voltage feedback concept is described to suppress the high voltage at light load conditions. In the case of the BIFRED, an additional transformer winding is added in series with the discontinuous current mode, DCM, boost inductor.

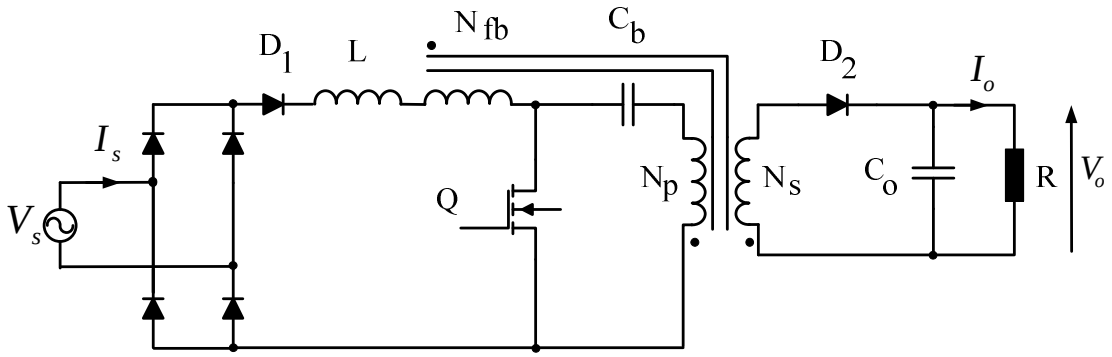


Figure 1-9 BIFRED with series voltage feedback winding

This extra winding, N_{fb} in Figure 1-9, feeds back the intermediate bus voltage when the boost inductor is energised, and as a consequence the input power can automatically be reduced, whilst maintaining the peak bus voltage within a satisfactory range. Based on this technique, the authors have derived several new single-stage PFCs based on a DCM boost converter. Despite the reduced bus voltage, the input current waveform is degraded due to the inductor current dead region caused by the additional feedback windings.

Other methods proposed to reduce the high voltage stresses are presented in [62, 64], are to modulate the switching frequency. The DC voltage transfer function of the CCM DC/DC converter depends only on the duty cycle to regulate the output voltage, and the DC voltage transfer function of the DCM input current shaper cell depends singularly on the switching frequency. It is therefore now possible, by varying the switching frequency, the intermediate bus voltage can be regulated without effecting the converter output. The penalty of such an approach is that often a large frequency range is required which makes it difficult to optimise wound components.

Alternative single stage PFC converter topologies are detailed in [54]. Similar to earlier converters, this approach is a cascade of two already existing converters, a boost and forward converter. Figure 1-10 shows there are now two primary windings connected with separate bulk energy storage capacitors in series with the isolation transformer of the DC/DC stage. This arrangement implements a series charging when the switch is on, and a parallel discharging of the capacitors when the power semiconductor is turned off. The results of these actions effectively introduce a ‘two-to-one’ voltage division on the original single storage capacitor. Analysis by [65], shows that the bus capacitor voltage can be maintained within 250 V of the peak line voltage, therefore enabling the adoption of low voltage components.

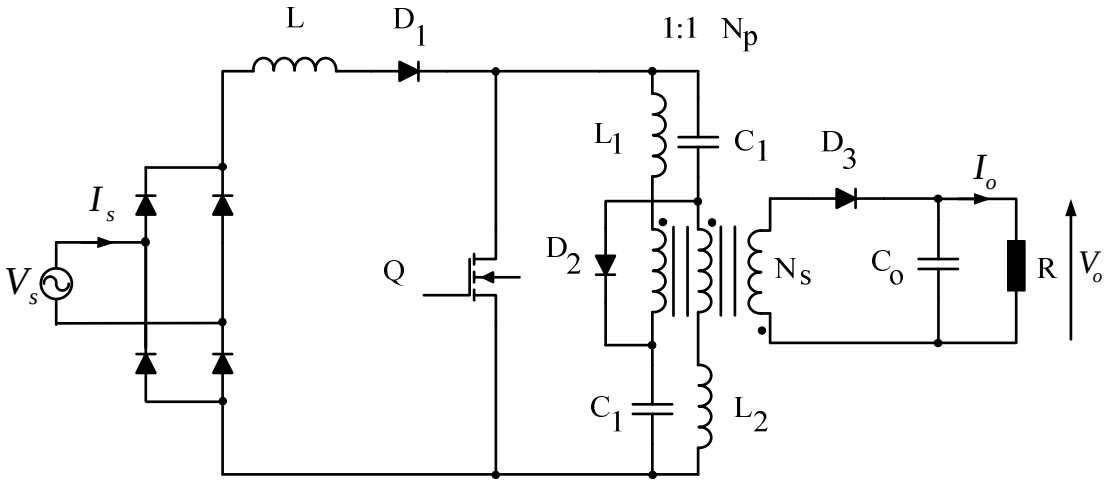


Figure 1-10 Cascaded single-stage PFC with two switch DC/DC converter

Besides the topological manipulation of the common boost and buck type approaches to series type power factor correction, the Cuk and Sepic converters have also been adapted to operate as a single stage power factor correctors [66-68].

The power imbalance and high bus voltage caused by the combination of DCM input current shapers and CCM DC/DC converters is addressed in [68]. A new family of single-stage, single switch PFC converters is introduced, that again cascade a boost type input stage and buck type DC/DC converter. However in the topologies presented, the energy storage capacitor is in parallel with the power flow, C_b in Figure 1-11. Furthermore the concept of similar current conduction operation modes for both stages, to limit peak voltages across the capacitor and power semiconductor components is introduced. In [68] it is suggested that both stages should be operating in discontinuous current mode in order to limit stresses at light load. In this state of operation, over the entire load range the DC bus voltage becomes independent of the load. What's more, the principle can be applied to other modes, continuous conduction mode for both stages [58].

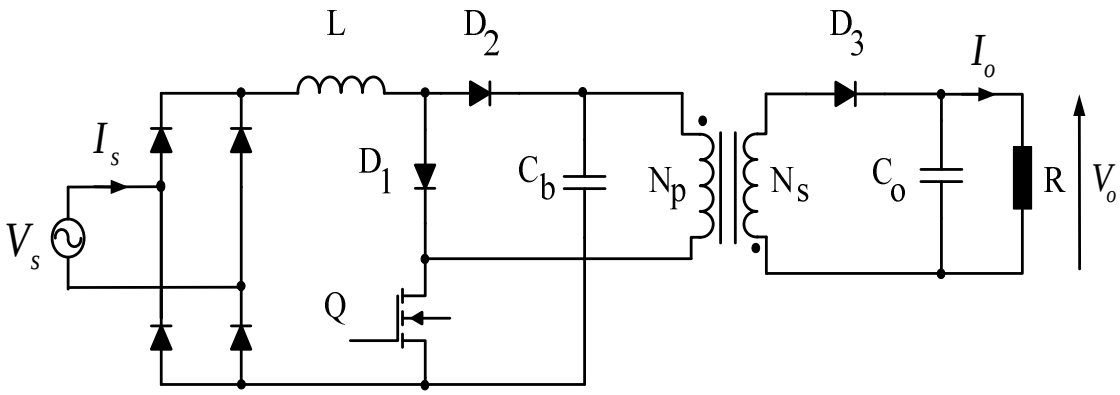


Figure 1-11 Parallel capacitor in single-stage PFC BIFRED

Using the DCM approach for both stages is likely to result in lower efficiency because of the higher conduction losses, and the common CCM approach generally has a lower power factor and a high distorted input current waveform.

Development and optimisation of this family of converters is conducted in [69-72]. In [73], it is proposed that to limit the maximum voltage, then the converters should be operated in boundary current conduction mode, BCM. In this state the converters would be able to adjust the operating mode according to the load conditions. It is found that the full load range can be divided into the three modes of operation; DCM, CCM and BCM, determined by the output condition.

Another parallel variation is proposed in [74], see Figure 1-12, again with the intention of reducing the stresses that occur in the single stage approach. The converter is formed by integrating a boost PFC with a two-switch clamped flyback converter. This topology simultaneously provides good output regulation and a high power factor. The current stresses in the two power switches are invariably lower than those of the single-stage, single-switch approaches detailed earlier. Also a high PF is achieved due to the absence of ‘dead banding’ of the input current at the input voltage zero crossing.

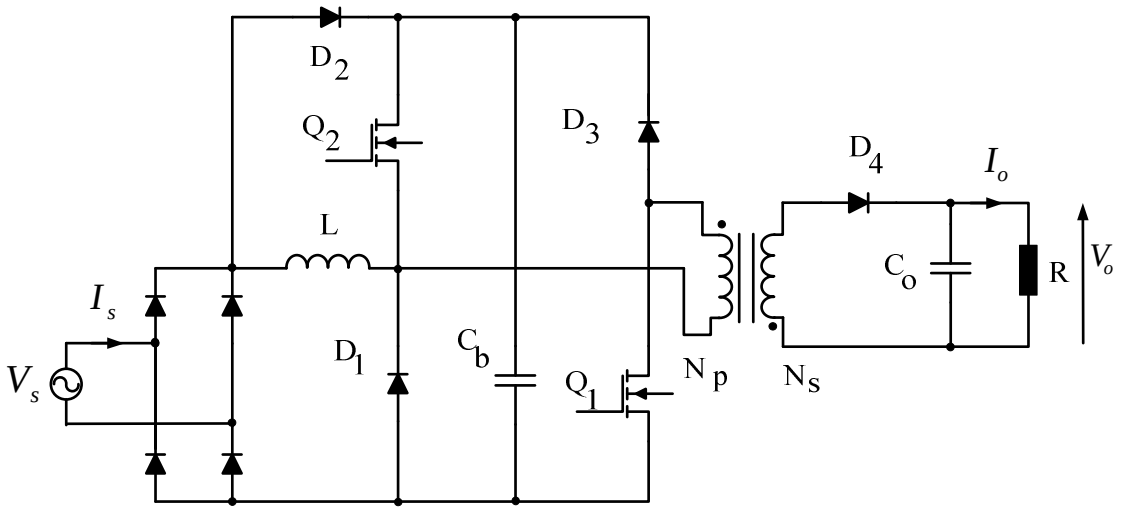


Figure 1-12 Single stage PFC converter prososed in [74]

The disadvantage of the parallel is the high component count, in which the multiple semiconductor devices share the high voltage and current stresses. Also the control strategy requires two loops to synchronise the switching components.

Recently, resonant converters have been proposed for single-stage PFC, [75-79]. To date the single stage PFC topologies presented have been limited to a power range of <300 W, for the reason that the topologies become too complex or the stresses become too great for semiconductor devices.

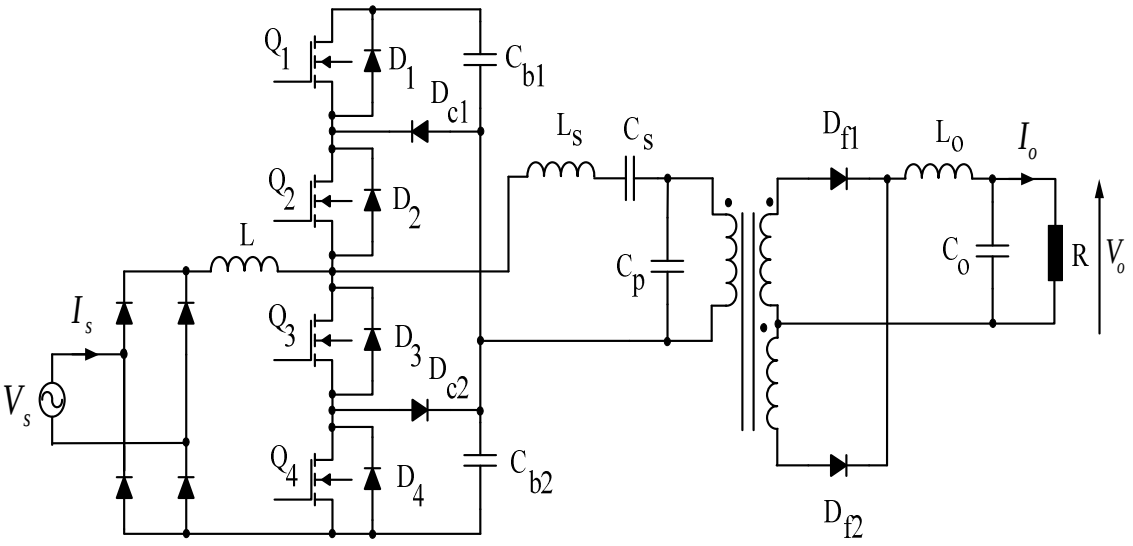


Figure 1-13 Single stage LLC PFC converter

The proposed converters comprise a series-parallel LLC three level resonant converter, see Figure 1-13. This approach provides the opportunity to operate at much higher power levels with the addition of lower voltage stresses. The topologies integrate the operation of a boost converter for current shapers, and a three level LLC resonant converter. Despite achieving an efficiency of upwards of 90 % at a power of 2.3 kW, the system again requires two control loops. The output voltage is regulated by the switching frequency of the resonant stage, and the DC bus is controlled by the duty cycle of the current shaper, which maintains a near unity power factor.

1.2.5 Power Factor Correction Regulation Control Strategies.

Continuous current mode operation often uses a two-loop control strategy such as average or peak current-mode control. The outer voltage loop senses V_{DC} and delivers a control signal to the inner current loop which is sensing the inductor current, I_L, and actively wave shaping the current I_s to be sinusoidal and in phase with the input line voltage V_s [80].

Peak current-mode control operates by comparing the positive current slope of the inductor with a predetermined reference level set by the outer voltage loop. When the instantaneous inductor current reaches the reference level, the power switch is turned off. Despite this approach being relatively simple to implement there are a number of issues. This method is susceptible to jitter noise on the sensed inductor current [81]. Above transistor duty cycles of 50 %, inherent instabilities create sub-harmonic oscillations regardless of the switching topology. This can be compensated for by the addition of a ramp to either the sensed inductor current or the current reference signal. However, at duty cycles near 90%, slope compensation results in a significant deviation between the ideal reference and the actual inductor current which may cause increased distortion of I_s [82].

Average current mode control, unlike peak current mode control, has an additional compensator [45]. The action of the current control loop forces the input current to match a reference signal. The amplified current error is compared to a saw tooth waveform generated by an external oscillator, to generate the PWM waveform. The gain bandwidth of the current amplifier can be tailored for optimum performance allowing the current to track a near sinusoidal waveform with a high degree of accuracy. This is claimed to result in a power stage with excellent noise immunity and no requirement for slope compensation. The voltage loop

however must have a relatively narrow bandwidth, compared to the current loop, otherwise the second harmonic output voltage ripple would result in a modulation of the input current, I_s, to keep the output voltage constant, therefore distorting I_s [46].

Hysteretic control presented in [83], is another method for regulating V_{DC} whilst performing power factor correction. For a converter operating in CCM with a two loop control system, the switch turns on when the inductor current falls below a predetermined minimum level, and turns off again when the current goes above an upper limit, resulting in variable frequency operation. This control approach does have the advantage that a compensation ramp is not required, however the method is susceptible to noise due to the switching edges, also the variable switching frequency makes magnetic design difficult to optimise [84], and finally, the inductor current, I_L, has to be sensed by some means.

An extension of hysteretic control is critical current mode control [85]. The inductor current is allowed to fall to zero, at which point the switch is turned on until a predetermined upper current level is reached. This approach allows the freewheeling diode to recover 'softly' as there is no recovery loss. Yet due to the near DCM operation the peak current levels tend to be higher resulting in higher conduction losses.

In PWM control methods for converter topologies operating in DCM, the internal current control loop can be eliminated, due to the automatic input current wave-shaping of discontinuous mode converter, Section 1.2.3. The voltage mode control approach is presented in [45]. Apart from the obvious advantages of a simplified control loop, and no current sensing components, this method uses a constant switching frequency, allowing for simple design of magnetic devices and EMC filtering. However, the circuit components are subject to higher peak current levels than a continuous conduction converter.

The second harmonic output voltage ripple in a PFC converter the limits the achievable dynamic response of the voltage control loop. To avoid loop instability, the voltage control loop of all approaches mentioned previously, must have a unity gain cross over, f_c, below the line frequency. It is for this reason, that PFC converters have a poor transient response to line and load fluctuations.

A number of modifications or enhancements to the voltage loop are proposed by [86], including a notch filter which is designed to attenuate only the twice mains frequency ripple component. This approach allows a very high power factor and a fast loop response to be achieved, but presents some practical difficulties in its implementation. High component tolerances are needed or a complex active tracking filter of the input mains frequency must be implemented.

A similar approach to a notch filter would be to ‘sample and hold’ the output signal of the voltage compensator. The voltage compensator processes the ripple frequency but the propagation of the disturbance through to the PWM is eliminated [87]. The disadvantages of this approach are the complexity of the control loop implementation, poor frequency response of the closed loop, and the difficulty of undertaking stability analysis due to the non linearity of the ‘sample and hold’.

The proposal in [86] to overcome the limitations caused by the second harmonic ripple is the so called regulation band approach. Upper and lower voltage limits are determined, and while V_{DC} is between these limits the control loop does not attempt to regulate V_{DC}. The control loop is essentially open loop during this condition. If V_{DC} were to exceed the limits then the voltage loop would generate a signal that would force V_{DC} to return to within the regulation band. This approach is simple to implement and results in the removal of the low frequency ripple from the feedback signal enabling a good power factor to be achieved. This method is simple to implement, has a fast transient response when operating within defined limits, however like the ‘sample and hold’ method there is a nonlinearity to contend with when analysing stability.

One final approach to enhance the voltage loop is ripple cancellation [88], where the reference voltage that is fed into the voltage compensator has a component superimposed that has the same frequency but is 180˚ out of phase with the output voltage. Despite realizing a fast transient response, practical implementation is difficult as the injected voltage has to accurately reflect the sensed feedback voltage, if not the input current of the converter will be distorted.

1.2.6 Magnetic Modelling and Integrated Magnetic Concepts

This section describes current integrated magnetic approaches, modelling techniques and magnetic materials.

Integrated magnetic components are often seen in the guise of coupled inductors [89]. One particular application of coupled inductors is the method of interleaving power converter stages to reduce input and output ripple elements and reduce the current level in individual devices. Numerous authors operate these converters in DCM with direct coupling of the magnetic devices [90-92].

One of the main aims of integrated magnetics however, is not only to reduce the magnetic component count but also to achieve electrical gains. Different coupling methods realise different behaviours. Inverse coupling can reduce RMS currents, the DC flux is eliminated and the AC flux in the core is lower, whereas with direct coupling, the device shows increased current ripple per phase, resulting in increased copper loss and no cancellation of the DC flux component [17, 89, 93, 94]. Unfortunately an added series inductor is required for the inverse coupling approach to filter the DC current component. A more common approach to magnetic coupling is found in EMC suppression common mode filters [95].

Transformers with multiple input and output windings may be classed as integrated magnetic devices and the concept can be developed further by combining inductive and transformer components on a single core.

A number of methods have been proposed for the analysis of magnetic components. One of the first proposed methods is that of the reluctance model. This approach is detailed in [15, 18, 96] and simplifies a magnetic structure into an equivalent electrical model. Since magnetic flux lines are closed paths, the flux becomes analogous to current. The primary assumptions are that the magnetic field is constant and is aligned to the direction of the path of integration. Non-linear ferrous materials and points close to saturation are not taken into consideration.

A similar modelling approach to a reluctance model is the inductance model, which is more useful as it converts the electromagnetic circuit into a purely electrical system [97]. To form the inductance model, a persistence model must be created from the reluctance model [26]. All parallel elements now become series elements and visa versa, and that all loops

become nodes, and nodes become loops. Each reluctance now becomes its inverse, a permeance. All voltage sources become current sources and the flux behaves as voltage drop across the respective permeances.

These methods are very effective for modelling separate magnetic components, but if the topology or integrated magnetic is complex or one has to consider the non-linearity of the ferromagnetic material then these methods can become unmanageable.

Another modelling method that can accommodate these non-linear effects and parasitics, is the Gyrator-Capacitor approach discussed in [97-99]. A gyrator is an ideal two port circuit element that reflects the impedance at one port as its reciprocal at the other, that is a capacitance at one port is reflected as an inductor at the other port. The gyrators replace the windings in this method and are represented as current controlled voltage sources. The core is modelled using the reciprocal of reluctance, that is a permeance.

To assist with the selection of the core materials and shapes, [100] compiles a table of the various magnetic materials and available core. Powder iron toroidal cores have a distributed airgap to allow high energy storage, whereas ferrite materials have very low high frequency loss characteristics [17].

New materials such as amorphous alloys allow for a much higher saturation flux density, approximately 1.6 T at 25 ˚C, compared to a ferrite, approximately 0.3 T at 25 ˚C. Despite the promising performance of these newer materials, they are invariably more expensive and so not widely available at present.

1.2.7 Devices and Components

Rapid progress has been made in the development of high voltage devices, semiconductor technology and capacitive components, through means of advanced processing techniques and novel device structures. Device improvements have enabled topologies that were previously dismissed, due to voltage/ current stress or cost, to become viable. The driving factors for such developments are the ever present demand for increased power density, low system cost and high reliability. This section reviews the current status, discusses the future trends of device technology and their impact upon emerging topologies.

1.2.7.1 Power Diodes

Traditionally the most commonly used high voltage diode is the silicon PiN structure. These devices typically have an on-state voltage drop of approximately 1 V which is acceptable at high voltages but is significant for low voltage applications. Being a minority carrier device, they have a poor reverse recovery characteristic arising from the large stored charge in the drift region during forward bias. This reverse recovery can form a significant contribution to the overall losses in the device and circuit, therefore limiting its use and application, especially at high frequency. Other adverse effects of reverse recovery include electromagnetic interference and thermal management. These devices are mature products, and their limitations are well understood and acknowledged.

Numerous techniques are used to improve PiN diode characteristics, such as optimising the doping profile in the epitaxial layer or by reducing the minority carrier lifetime [101]. Typical PiN rectifier power diodes exhibit performances of 2000 V, 200 A with a forward voltage drop of 1.25 V and reverse recovery times of approximately 25 ns. Any further reduction in recovery times, requires an improvement to either the current technology or a change of material.

An alternative to the PiN diode is the high voltage Schottky barrier diode, SBD. The conduction current of Schottky barrier diode consists of majority carriers, therefore, unlike the Silicon, Si, diodes, the stored charge is negligible and the diode turns off with a near zero reverse recovery current [102]. The materials used in these devices are either GaAs, GaN, but the leading candidate is Silicon Carbide, SiC. Superior electrical performance is achieved with these materials compared with Si due to high breakdown field, high electron mobility and high saturation velocity [103]. The material properties of SiC devices make it an ideal choice for high power, high temperature and high frequency applications. Experimental evaluations of a similarly rated Si diode and SiC diode in [103] reveal that despite elimination of switching losses, due to the high forward volt drop, 3 V, associated with SiC SBD, conduction losses are now the dominant loss factor.

Compared to Si diodes however, SiC material diodes can offer simplified power stage design due to the elimination of snubbers, reducing component count. Furthermore the reduction in power losses leads to lower operating temperatures, and reduced EMC emission

from switching transients. Cost however is a major barrier for market uptake, currently a 3 inch SiC wafer is 25 times more expensive that a Si wafer of the same diameter. Further SiC substrates contain a much higher level of defects, which reduces yields.

As well as investigating the performance of different materials, various device structures have been explored in order to improve device performance. Significant improvements in the trade off between on-state voltage drop and reverse recovery has been demonstrated by altering the injection efficiency using either a merged PiN/Schottky structure, MPS [104], self adapting P-emitter diode, SPEED, structure [105] or a static shield diode, SSD, structure [106]. These device structures provide a superior trade off curve between the on state voltage drop and reverse recovery charge when compared to PiN diodes.

1.2.7.2 High Power Light Emitting Diodes

The development of high efficiency Indium Gallium Nitride, InGaN, blue Light Emitting Diodes, LEDs, in the early 1990's was a break through for the development of ultra-bright white HP LEDs [107]. The spectrum of light generated by a white HP LED is shown in Figure 1-14, along with the sensitivity of the human eye. The HP LED produces the visible white spectrum by exciting an Yttrium Aluminium Garnet, YAG, phosphor layer placed over the surface of a blue HP LED die, Figure 1-14. The die of the HP LED produces a blue to the end of the visible spectrum near UV, of a wavelength at approximately 460 nm as seen in the peak in the white HP LED spectrum at this wavelength [108]. The interaction between the blue light and the phosphor produces visible radiation at longer wavelengths, approximately 500 to 750 nm through stokes shift [109].

The combination of blue light and phosphor generated light creates the perception of white light. This approach currently has a luminous efficiency of approximately 100 lm/W [108], however it is by no means the only way for HP LEDs to produce white light. Other approaches include mixing the colour from individual red, green and blue LEDs. This approach is the most efficient as no energy is lost in the Stokes Shift and enables a tuneable white point. However, systems using this effect often employ feedback to stabilise the colour produced. Another approach is for the LED die to generate UV light, at 300 nm wavelength, which then interacts with red, green and blue phosphors. This method produces a very stable

white point and high colour rendering, but degradation of the HP LED package is rapid due to the UV light damaging the phosphors [108].

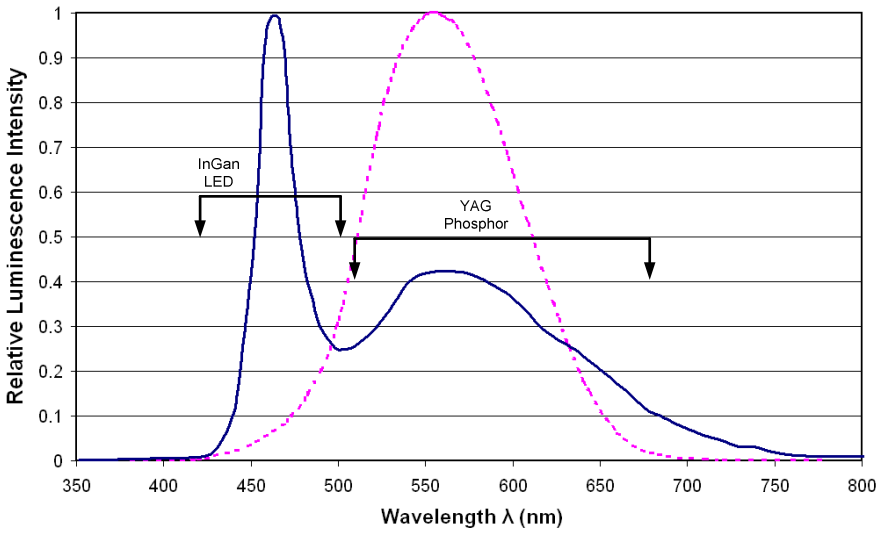


Figure 1-14 Typical HP LED spectral distribution (solid) and standard luminous sensitivity of the eye (dashed).

These three approaches have developed to the point that HP LEDs can be seriously considered for replacing conventional halogen and incandescent lamps in general illumination and street lighting. Voluntary European legislation regarding the phasing out of incandescent bulbs by 2012 makes this approach ever more attractive [110].

The key characteristics of HP LEDs are excellent reliability, instant turn on, dimmability, high operating hours, approximately 50,000, and good colour and temperature rendering [34]. Their efficiency is typically 100 lm/W in 2010, and manufacturers indicate that this value will improve. However, before wide spread adoption of the technology can be embraced, there are a number of outstanding issues that need to be addressed.

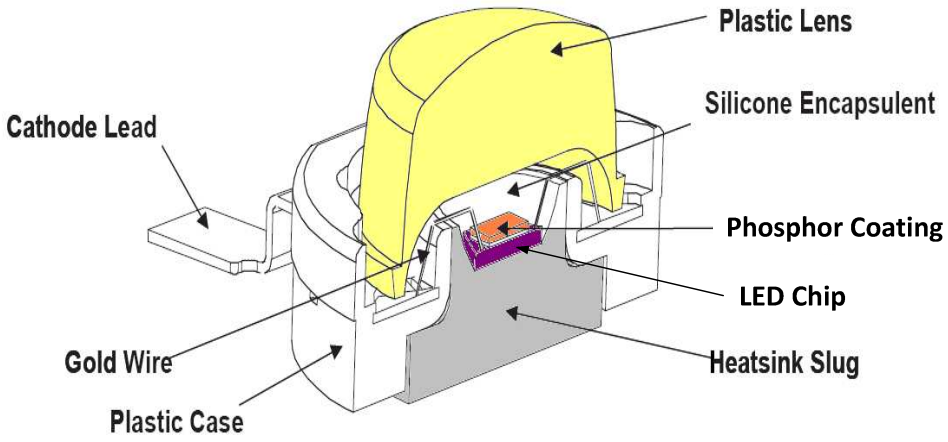


Figure 1-15 Schematic of a high power white LED.

Despite consuming less power than conventional HID lighting for the same light output, the advantages for implementation are not always clear cut. Currently, HP LEDs are invariably more expensive in terms of initial purchase cost, as they are a new technology. But as market penetration increases, this initial cost will reduce.

A more fundamental challenge is that of thermal management. Regardless of the quoted high lumens per Watt of converted electrical energy to useful visible light by the manufacturers, the die of a typical white HP LED can reach temperatures up to 185 ˚C [111]. This operating temperature is not conducive for long life and low luminaire maintenance. HP LED manufacturers quote a maximum operating junction temperature, T_j, of 85˚C to ensure 70 % luminance after an operating life of 50,000 hours, Figure 1-16. When the illuminance falls below 70 % of the initial light output the device is deemed to have failed. Therefore, to meet the quoted lifetimes of the HP LEDs and prevent excessive light degradation, the thermal conditions must be well regulated, and the die temperature must be kept within the manufacturer's specification [112-115].

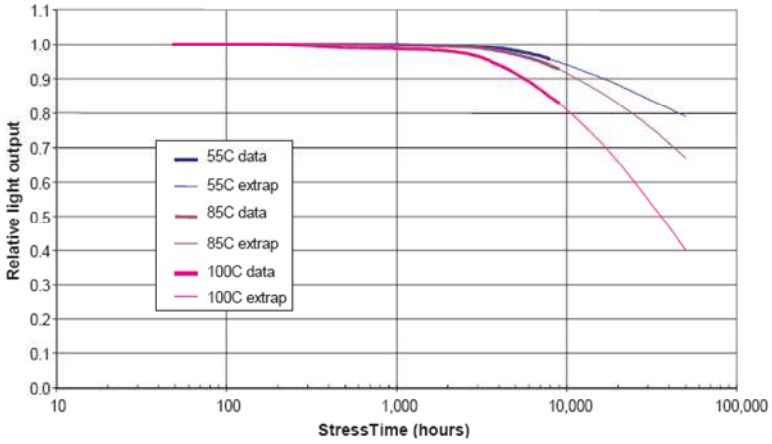


Figure 1-16 Relative HP LED light output lifetimes at various temperatures [29]

Once the thermal energy has been conducted away from the semiconductor junction to the attached heat sink, the energy must then be dissipated to the ambient environment. For street lighting applications, natural convection is the most suitable way of transferring heat to ambient, due to its simplicity and reliability.

1.2.7.3 MOSFET

Since the introduction of power MOSFETs in the early 1970s, there has been continued development in the improvements in the power density of the device, which closely reflect the advances achieved in power rectifiers, for example through the introduction of new materials and device structures. The key characteristics of a MOSFET are high input impedance, generally a low on-resistance, fast switching speeds and ruggedness [45].

The performance of the Si DMOSFET has approached its theoretical limit [101], therefore other structures have been developed. Recently the UMOSFET has become commercially available. This trench gate device has a superior channel density due to the elimination of the JFET resistance present in the DMOSFET arrangement, allowing lower on state resistances to be achieved. UMOSFET structures can be further developed to accumulation, inversion and extended trench field effect transistors (ACCUFET, INVFET and EXFET) [116, 117]. The primary features of these arrangements is that the trench UMOS gate extends in to the N substrate, and into the N^+ substrate in the case of the EXFET. In this design approach the current conduction occurs along the surface of an accumulation inversion layer formed along the trench sidewalls, resulting in extremely low on resistance. Of this series of

structures the ACCUFET has the lowest of on resistances. Further the ACCUFET has the advantage that it does not contain any parasitic P-N junctions.

Semiconductor material development that has greatly improved the performance of high power diodes has also been applied to MOSFETS. SiC power devices offer substantial performance improvements over Si, enabling increased power density, high efficiency and higher temperature operation [102].

SiC MOSFETs were first proposed in the early 1990s [118], these power devices were the vertical trench structure, UMOSFET. This construction is attractive due to its straight forward fabrication, however the electrical performance of the DMOSFET SiC is far superior. Due to higher bandgap of the material, SiC MOSFETs are achieving voltages approaching 1800V [118].

Whilst engineering samples of some devices are starting to become available, there are a number of areas that need addressing such as the improvement of the $Si0_2$- SiC interface. Reliability issues have been noted of the gate oxide under high field conditions. A second issue with SiC power MOSFETS is the low inversion channel mobility. This is the result of the high density of interface states present in the upper half of the bandgap [119]. In [120, 121], annealing with NO and N_2O can relieve this issue slightly, but inversion channel mobility in SiC remains approximately a order of magnitude less than in a Si MOSFET.

1.2.7.4 Capacitors

Technological developments in the semiconductor devices such as diodes and MOSFETs have generally gone hand in hand. However such progress in capacitor technology has not been so rapid. A wide range of capacitor types and technologies is available, and the most common are listed in Table 1-2 along with their typical performance figures.

Electrolytic capacitors, wet or solid types [44], are the most suitable for addressing DC filtering and energy storage. Limitations of these components include a significant equivalent series resistance, ESR, which may increase under high current ripple conditions and high temperature. This could compromise the filtering performance of the capacitor or may lead to control loop instability in some power supply applications. The relatively short life time of

these capacitors is a serious concern in many applications, furthermore, the lifetime falls rapidly at increased operating temperatures.

Table 1-2 Capacitor table comparison

Capacitor Type	Capacitance	Voltage (V)	Expected Lifetime (hrs)	Temperature (^{o}C)
Aluminium Electrolytic	0.1 µF - 1500 µF	2 to 500	7,000	-55 to +125
Ceramic	0.01 pF - 27 pF	2 to 500 k	50,000	-60 to +125
Film	0.5 pF - 30 pF	2 to 300 k	50,000	-40 to +85
Tantalum	1 nF - 9100 pF	2 to 2 k	2,000	-55 to +125

Ceramic capacitors types are often used for high frequency filtering and EMC [122]. The IEC 60384-8 and IEC 60384-9 classify these capacitors into two types, Class 1 and Class 2 respectively. Class 1 capacitors are required for frequency compensation of control loops, coupling and decoupling in high-frequency circuits where low losses and narrow capacitance tolerances are required. Class 2 capacitors are again used as coupling and decoupling capacitors, but where higher losses and a reduced capacitance stability are demanded.

Film capacitors fulfil a number of roles, from general filtering, snubbing applications, noise suppression, high voltage high frequency applications to more specialised applications such as mains filtering, or filtering between mains line and earth, known as X and Y capacitors respectively. Film capacitors may be either film/foil wound or metallised film types and use materials such as; polyester, polyphelyne sulphide, polypropylene, and polyester polypropylene [122]. Film/foil capacitors consist of two metal foil electrodes that are separated by a thin insulating plastic film. Features of such devices are high insulation resistance, excellent current and pulse capability as well as good capacitance stability. For metallised film capacitors, the capacitor plates consist of aluminium sprayed onto the dielectric surface by thin-film vacuum deposition. This process allows a smaller device, lighter weight and lower ‘self healing’ due to an internal short circuit from an overvoltage transient or device fault. Though suffering no permanent damage, capacitance may be reduced.

Tantalum capacitors are found in two forms, wet and solid. Wet electrolytic tantalum capacitors are preferred in applications where there is the requirement for stable electrical

parameters, high reliability and capacitance stability at high temperatures. The wet tantalum capacitor offers a very high number of microfarads per unit volume, three times more than an aluminium electrolytic. The dielectric used is tantalum pentoxide.

Solid tantalum electrolytes contain manganese dioxide, and they are the least expensive of the two types. Both the wet and the solid tantalums are polarised, but the former can withstand a 10% reversal of the rated voltage. The advantages of using the solid type are no probability of electrolyte leakage and superior capacitor characteristics. When using a solid tantalum, it is necessary to select a device that has high electrolytic conductivity to obtain low values of leakage current and dielectric loss. It is these issues that determine the choice between a wet or solid device.

Figure 1-17 shows the impedance/frequency comparison of 10 µF capacitors of the different types presented in Table 1-2. The capacitor impedances are all similar upto a frequency of approximately 10 kHz, beyond this point their behaviours differ. Unlike aluminium electrolytics, ceramic capacitors exhibit the most ideal frequency characteristics.

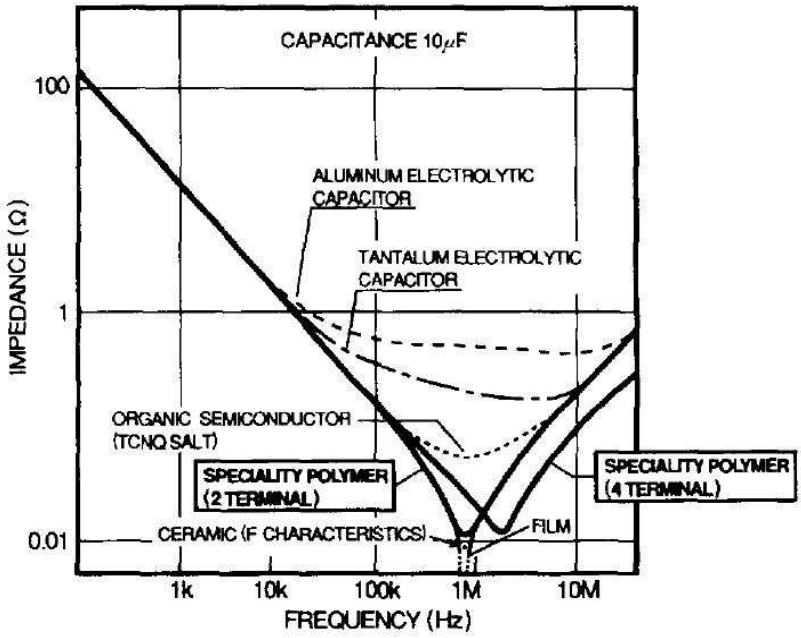


Figure 1-17 Capacitor impedance/frequency characteristics [44]

1.2.8 Street Lighting Considerations and Regulations

The regulatory requirements for street lights are summarised in this section. The classification of lighting types and location, motorways or strategic routes, detailed in [123], determines the optical requirements and light output performance of a street luminaire. Optical requirements detail the lighting quality such as control of glare, colour temperature, colour rendering, lifetime and illumination footprint, [42]. The level of illuminance for the route type, leads to the selection of lamp type and overall operating power level.

A general code of practice for designing street lights is covered in [124]. Considerations such as weight, dimensions, chassis material, appearance, vibration levels, and resistance to heat and fire are all detailed. This regulation also stipulates the accessibility of the power converter and lamps should the need arise for servicing or replacement. To protect the electrical connections and components [125] dictates that the system must be sealed to water and dust ingress and have a degree of protection to IP56 rating. The thermal design of the luminaire and its housing is also important since much of the electrical input power will be dissipated as heat, for example, to achieve a typical street light output of 12,000 lumens, approximately 150 LEDs are needed with a total power of around 180 W. Little of this 180 W is converted to optical power, and so it can be assured that most of the 180 W is converted to heat.

1.3 Summary of Literature Review

The main developments in the areas of single-stage power factor correction techniques, integrated magnetics and high power light emitting diodes are summarised. Non-isolated, passive and active PFC approaches are described. Active PFC methods produce the most sinusoidal input current and highest power factor. Numerous control approaches are detailed including current and voltage mode control. But the review suggests that there is no one single control approach suitable for all requirements. The concept of single-stage power factor correction is discussed. A vast amount of literature has been produced on this topic, and a number of complex topologies have been developed. However the most effective and simplest approaches are the topologies that have purely combined existing power converters. Integrated magnetic approaches are outlined, whereby a number of different magnetic devices are combined onto a single core, the associated modelling techniques, magnetic materials and core

structures are described. The development of advanced power components also stimulates the development of power electronic approaches and control techniques. The emergence of high-power light-emitting diodes is described which opens up the opportunity of making more efficient lighting systems, however this also creates new, demanding requirements for the associated power conditioning equipment.

With the ever growing demand for power electronic equipment to be more power dense and have a lower component count, the idea of single stage power factor correction appears to offer an attractive solution. However there is little published material with regards to an integrated magnetic component being used within a single-stage power factor corrector and its cost analysis. Secondly, with the emergence of HP LEDs and their superior operating characteristics, the literature review clearly indicates that the electrolytic capacitor needs to be eliminated from the associated power supply in order not to compromise the overall system lifetime. This however has an impact upon the control approach and the ability to meet input harmonic standards. Therefore it was decided to develop a HP LED driver that would fulfil these requirements.

1.4 Thesis Structure

Chapter 2 details the analysis and design of a single stage power factor corrector with an integrated magnetic component. The operation of the converter is analysed and a theoretical design is performed. The integrated magnetic component is designed and wound, and a SABER simulation is conducted of the S^4PFC and the IM. The SABER results confirm the analysis and design work.

Chapter 3 examines the dynamic behaviour and control requirements of the S^4PFC with an IM. The line-to-output and control-to-output characteristics of the converter are examined with the aim of identifying a suitable control approach. The design of the control loop is conducted and SABER and MATLAB simulations are performed to verify the control design.

Chapter 4 details the experimental verification of the S^4PFC. A prototype converter is developed and the laboratory setup is explained. Electrical schematics and printed circuit board layouts are shown, along with the results of the steady-state and dynamic experimental

testing. A discussion of the results is included along with the impact, performance and cost benefits of this approach.

Chapter 5 describes the analysis and development of a power converter for a high-power white-light emitting diode street light. A suitable topology is identified that can perform without an electrolytic capacitor to fulfil the requirement to operate for 50,000 hours. The operation of the converter is discussed and a theoretical design is performed. SABER simulations are conducted to verify the design.

The identification and analysis of the control approach for the HP LED driver is described in Chapter 6. The principles of operation and design are explained. The dynamic performance of the selected control approach is explained to determine its suitability for this application.

Chapter 7 details the experimental verification of the HP LED driver. A prototype converter is developed which includes the constant current converter required regulate the current through each of the individual LED strings. Electrical schematics and printed circuit board layouts are shown along with the laboratory setup. Results of the steady-state and dynamic testing are presented and discussions of the results are included.

Finally Chapter 8 presents the key conclusions of the thesis, detailing the contributions of this research and the recommendations for further work.

2 Single-Stage Single-Switch Converter Analysis with Integrated Magnetic

2.1.1 Introduction

This chapter details the analysis and design of a Single-Stage Single-Switch Power Factor Corrector converter, S^4PFC, with an Integrated Magnetic component, IM. The power topology is based upon a boost converter operating in Discontinuous Current Mode, DCM, for Input Current Shaping, ICS, and a cascaded forward converter for output voltage regulation. The steady-state operation of the converter is detailed, as well as the essential design equations. MATLAB and SABER simulations characterise the steady-state performance of the converter and verify the design equations. Analysis of the IM is performed, design methods identified and its expected operation detailed, which is also verified using SABER simulations.

2.1.2 Principles of Operation of S^4PFC

A steady-state analysis of the single-stage single-switch power factor corrector is detailed in this section. For simplicity, the following assumptions are made: all of the devices and components are ideal, and the switching frequency, f_{sw}, is much higher than the line frequency, f_{line}. Figure 2-1 shows a schematic of the S^4PFC, a boost converter is combined with a forward converter forming the single-stage converter proposed in [68].

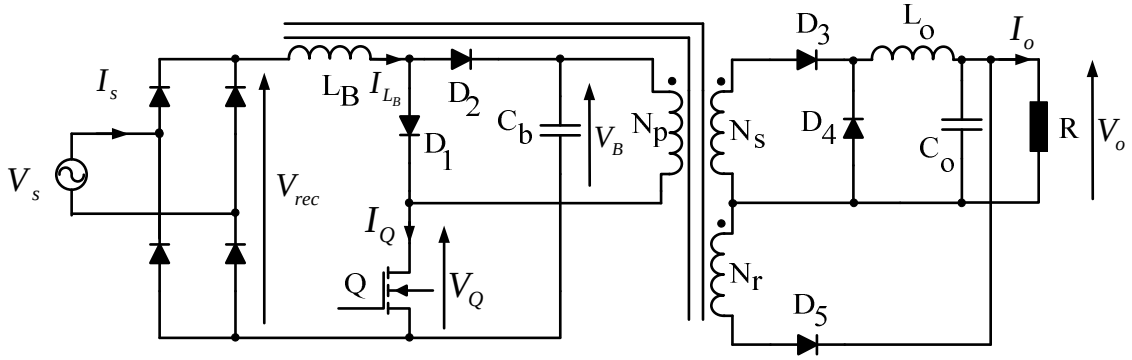


Figure 2-1 Single-stage, single-switch power factor corrector with an integrated magnetic component

To achieve a high power factor, the boost converter operates in discontinuous current-mode resulting in automatic shaping of the input current, I_s, whilst the duty ratio, D, regulates

the output voltage, V_o. Operating the boost stage in DCM eliminates the requirement for complex current mode control and also reduces the size of the boost stage inductor L_B [51]. The input voltage of the forward converter is consequently the boost capacitor voltage, V_B. The forward converter operates in CCM. In addition to combining two power stages with a simplified control, the concept of integrate magnetics is used to reduce component count by combining the boost inductor and forward converter transformer on to a single magnetic core, Figure 2-1. The winding arrangement of this device is such that the magnetic coupling between the inductor and transformer windings is small, therefore it will not affect the electrical performance of the topology, if they were to be independent.

Using a sequence of converter schematic diagrams and Figure 2-3, the state-by-state operation of the converter is now described. The S^{4}PFC is controlled by a single semiconductor power switch, Q. The current through L_B becomes zero during T_{off} in each switching cycle, resulting in a near resistive input impedance [52].

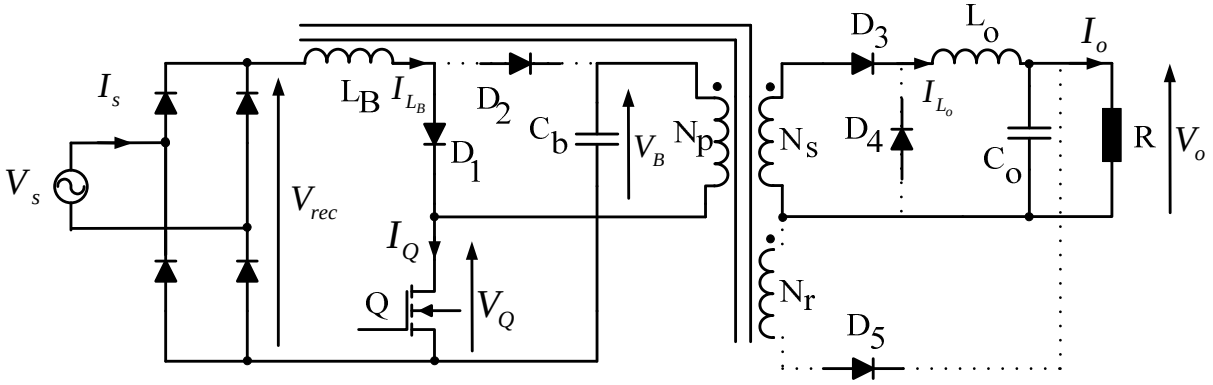


Figure 2-2 Schematic diagram of the S^{4}PFC with an IM during time $\mathbf{t_0}$ to $\mathbf{t_1}$

During $\mathbf{t_0}$ to $\mathbf{t_1}$ the MOSFET Q is on. The schematic for this mode is seen in Figure 2-2. V_{rec} is applied across L_B, and the boost inductor current I_{L_B} increases to a maximum value of

$$\hat{I}_{L_B} = \frac{V_{rec}}{L_B} DT_{sw} \qquad \textbf{Eqn 2-1}$$

where D is the duty ratio, T_{sw} is the switching period and V_{rec} is the rectified input voltage. During this period $I_{D_1} = I_{L_B}$.

During this time diode D_2 is reversed biased by the boost capacitor voltage, V_B, as C_B is discharged through the primary windings, N_P, of the transformer. The peak current of winding N_p is

$$\hat{I}_{L_p} = \frac{\hat{I}_{L_s}}{N_{p,s}} + \hat{I}_{L_{p,mag}} \qquad \textbf{Eqn 2-2}$$

where $N_{p,s}$ is the turns ratio of the transformer primary and secondary windings, and $\hat{I}_{L_{P,mag}}$ is the peak magnetising current of N_P which is determined by

$$\hat{I}_{L_{P,mag}} = \frac{V_B D T_{sw}}{L_p} \qquad \textbf{Eqn 2-3}$$

where L_p is the magnetising inductance of N_p. The total current through MOSFET, Q, is determined by

$$I_Q = I_{D_1} + I_{L_P} \qquad \textbf{Eqn 2-4}$$

where I_{D_1} is the current through D_1 and I_{L_p} is the primary winding current.

Noting the dot notation of the transformer windings, the peak current, $\hat{I}_{L_S}$ of the secondary transformer windings is

$$\hat{I}_{L_S} = \left(\hat{I}_{L_P} - \hat{I}_{L_{P,mag}}\right) N_{p,s} = \hat{I}_{L_O} \qquad \textbf{Eqn 2-5}$$

$\hat{I}_{L_o}$ is the peak current through the output inductor, L_o.

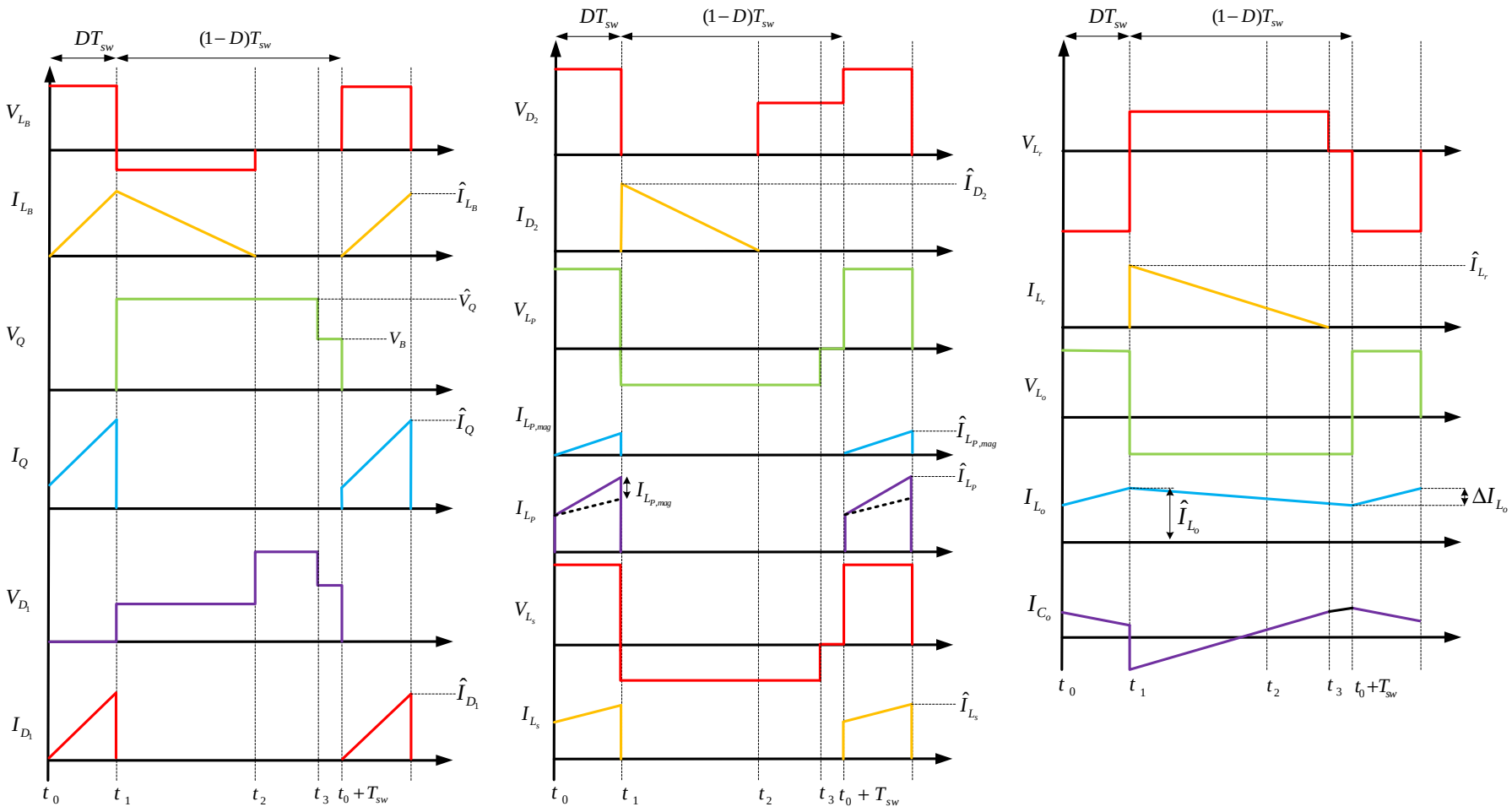


Figure 2-3 Key waveforms of the S[4]PFC with an IM

Due to its orientation the secondary reset winding, N_r, during this time and the peak voltage across this winding is determined by **Eqn 2-6**

$$\hat{V}_{L_r} = V_B N_{p,r} \qquad \textbf{Eqn 2-6}$$

where $N_{p,r}$ is the turns ration of the transformer primary and reset winding

During time $\mathbf{t_1}$ to $\mathbf{t_2}$, Q is turned off. The schematic for this mode is shown in Figure 2-4. The boost inductor charges the boost capacitor, C_B, diode, D_2, is forward biased and the transformer magnetising energy escapes through N_r to the load.

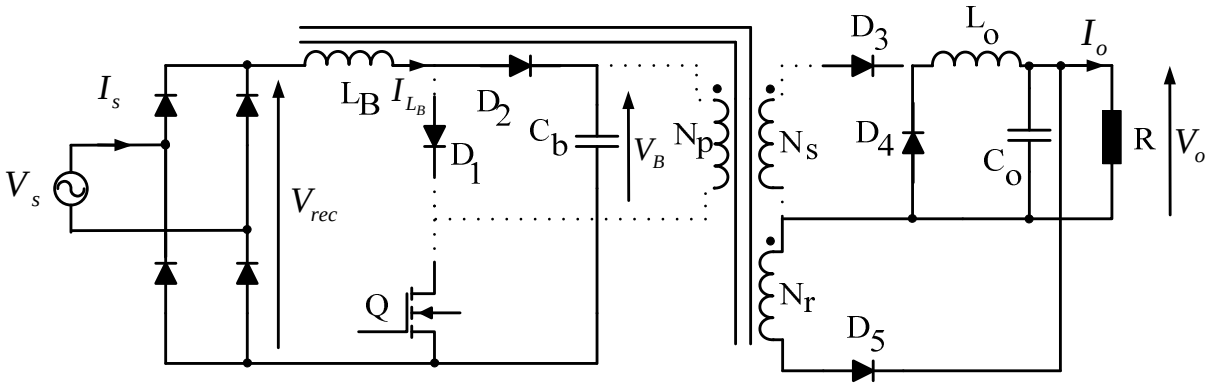


Figure 2-4 Schematic diagram of the S^4PFC with an IM during time $\mathbf{t_1}$ to $\mathbf{t_2}$

The voltage V_Q across the transistor during this period is the boost capacitor voltage plus the voltage referred from the conducting reset winding.

$$V_Q = V_B + \frac{V_o}{N_{p,r}} \qquad \textbf{Eqn 2-7}$$

where V_o is the output voltage of the S^4PFC. D_1 is reversed biased by the primary voltage. The time taken for I_{L_B} to fall to zero may be calculated as

$$t_2 - t_1 = \frac{L_B \hat{I}_{L_B}}{(V_B - V_{rec})} = \delta T_{sw} \qquad \textbf{Eqn 2-8}$$

where δ is the proportion of the switching period for I_{L_B} to fall to zero.

The voltage across winding N_r forward biases diode D_5, allowing the energy stored in the magnetic core to be transferred to the output of the S^{4}PFC. The peak current in the reset winding at t_1, $\hat{I}_{L_r}$, may be written as

$$\hat{I}_{L_r} = \frac{\hat{I}_{L_{p,mag}}}{N_{p,r}} \qquad \textbf{Eqn 2-9}$$

Eliminating $\hat{I}_{L_{p,mag}}$ using **Eqn 2-3** results in

$$\hat{I}_{L_r} = \frac{V_B D T_{sw}}{\sqrt{L_p L_r}} \qquad \textbf{Eqn 2-10}$$

As with a conventional forward converter, N_P and N_S are not conducting, and diode D_3 is reversed biased, which enables diode, D_4, to freewheel and conduct the current I_{L_o}.

During time **t_2 to t_3** Q is still off, I_{L_B} is zero and the current I_{L_r} in the reset winding continues to fall, reaching zero at time t_3. The circuit configuration for the converter during this period can be seen in Figure 2-5.

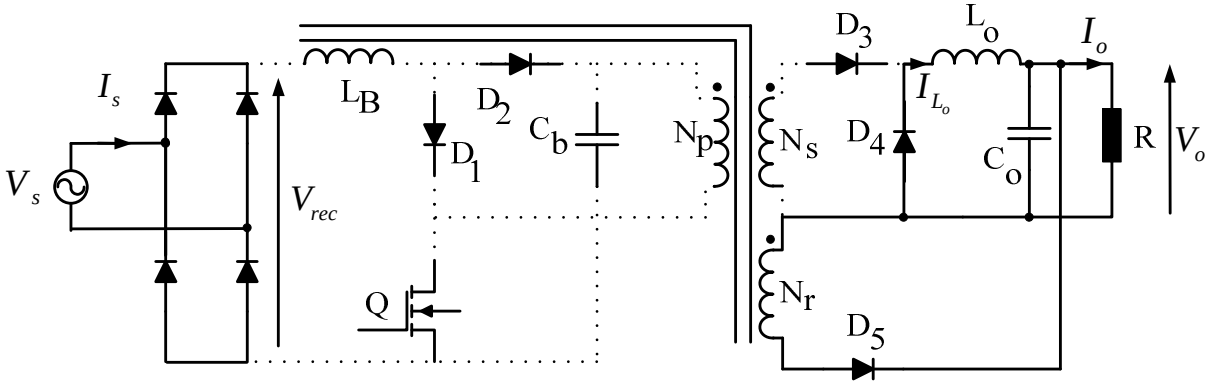


Figure 2-5 Schematic diagram of S^{4}PFC with an IM during time **t_2** to **t_3**

The reverse voltage across D_1 is

$$V_{D_1} = \frac{V_o}{N_{p,r}} \qquad \textbf{Eqn 2-11}$$

The off state voltage across V_Q is

$$V_Q = V_B + \frac{V_o}{N_{p,r}} \qquad \textbf{Eqn 2-12}$$

The reverse voltage across diode D_2 is

$$V_{D_2} = V_B - V_{rec} \qquad \textbf{Eqn 2-13}$$

During the brief time period from t_3 to t_0+T_{sw} diode D_4 is still conducting the freewheeling current of L_o, and there is no other current flow in the circuit. V_Q is now equal to the PFC stage capacitor voltage V_B. The voltages across the all of the integrated magnetics windings are zero, and $V_{D_1} = V_B - V_{rec}$.

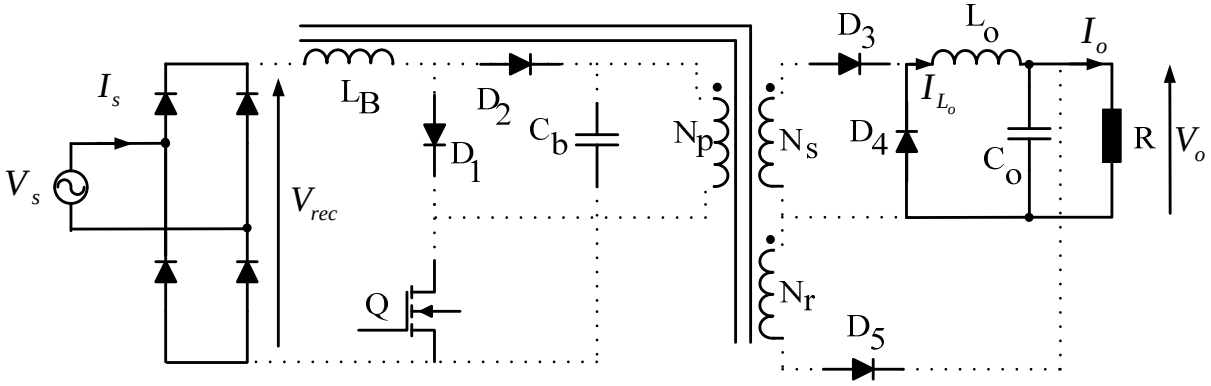


Figure 2-6 Schematic diagram of S^{4}PFC with an IM during time $\mathbf{t_3}$ to $\mathbf{t_0+T_{sw}}$

So far, the analysis of the S^{4}PFC has been concerned with only the steady-state DCM conditions with a constant V_{rec} and duty ratio. However, over a line period the input voltage is time-varying and can be defined as

$$V_s(t) = \hat{V}_s \sin \omega t \qquad \textbf{Eqn 2-14}$$

where $\hat{V}_s$ is the peak line voltage, ω is the angular frequency of the line voltage. The rectified voltage V_{rec} is described as

$$V_{rec}(t) = \hat{V}_s \left|\sin \omega t\right| \qquad \textbf{Eqn 2-15}$$

With a constant duty cycle, over half a line period, $T_{line}/2$, the boost inductor current I_{L_B} is show in Figure 2-7.

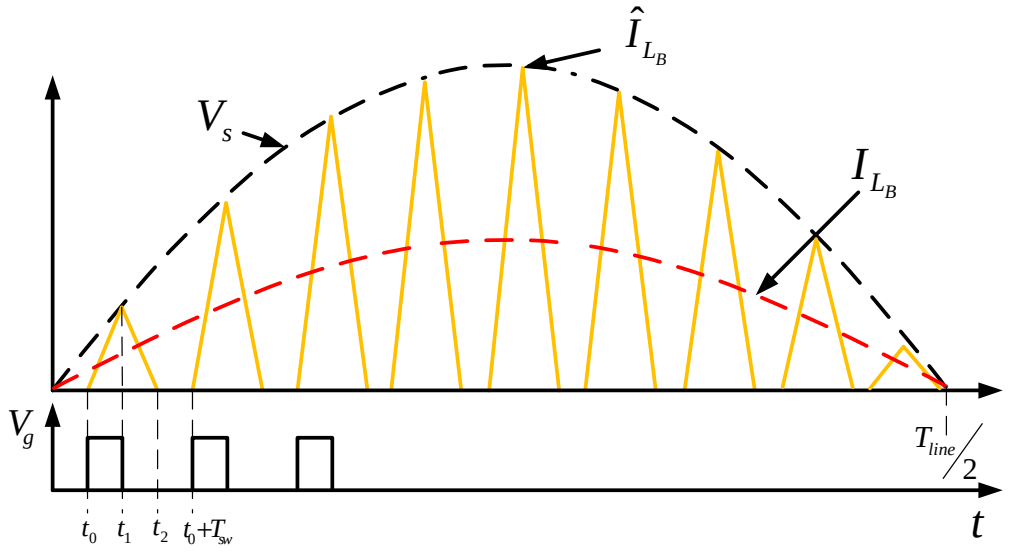


Figure 2-7 Inductor current waveform during a half line cycle

Using **Eqn 2-1** and **Eqn 2-15** the peak inductor current in a switching cycle now becomes

$$\hat{I}_{L_B}(t) = \frac{\hat{V}_s |\sin \omega t|}{L_B} DT_{sw} \qquad \textbf{Eqn 2-16}$$

The duration of the trailing edge of the boost inductor current during t_1 to t_2 in Figure 2-7, δT_{sw} may be calculated by equating the volt-seconds of L_B.

$$\delta T_{sw} = \frac{V_s}{|V_B - V_s|} DT_{sw} \qquad \textbf{Eqn 2-17}$$

where δ is the portion of the switching period for I_{L_B} to fall to zero.

Therefore from **Eqn 2-16** and **Eqn 2-17** the local average inductor current during a switching cycle can be expressed as

$$I_{L_B}(t) = \frac{\hat{I}_{L_B}}{2}(D+\delta) = \frac{\hat{V}_s D^2}{2L_B f_{sw}} \frac{|\sin \omega t|}{1 - \frac{\hat{V}_s}{V_B}|\sin \omega t|} \qquad \textbf{Eqn 2-18}$$

Figure 2-7 shows the instantaneous peak inductor current, which is always sinusoidal, however upon plotting **Eqn 2-18**, Figure 2-8, it is clear that the wave-shape of the local average inductor current, I_{L_B}, is dependent upon the ratio $\hat{V}_s / V_B$, the smaller the ratio the more sinusoidal I_{L_B} becomes. This effect is due to the time taken for I_{L_B} to fall to zero during the transistor off time. A small $\hat{V}_s / V_B$ implies a small value for δ, **Eqn 2-17.**

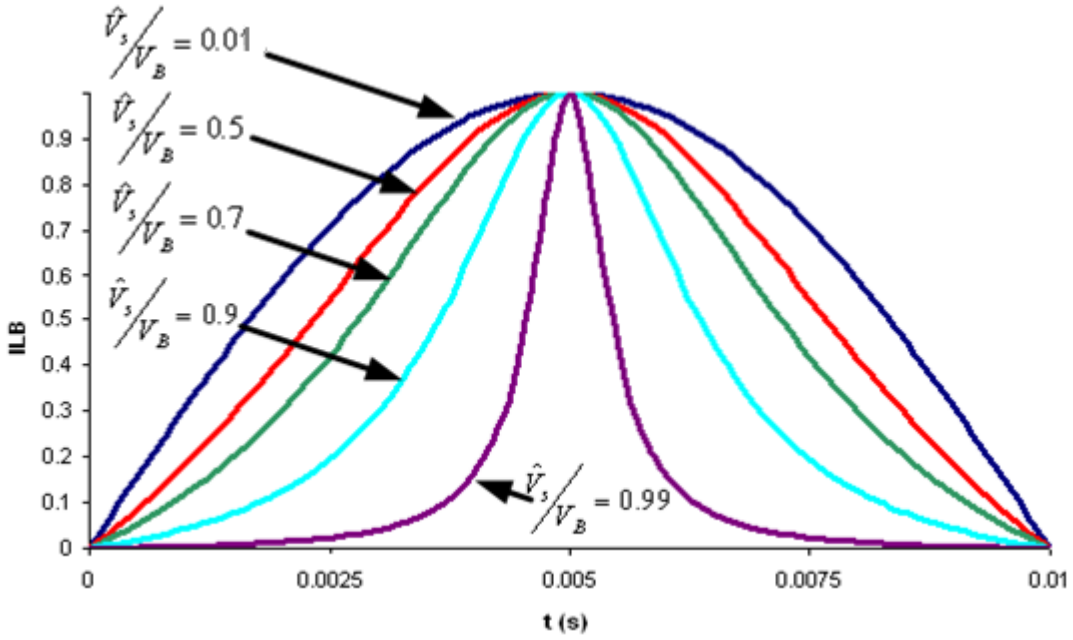


Figure 2-8 A normalised plot of I_{L_B} over various ratios of $\hat{V}_s / V_B$

Using **Eqn 2-18** the input line current I_s is expressed as

$$I_s(t) = \frac{\hat{V}_s D^2}{2L_B f_{sw}} \frac{\sin \omega t}{1 - \frac{\hat{V}_s}{V_B}|\sin \omega t|} \qquad \textbf{Eqn 2-19}$$

As $I_s(t)$ is not necessarily a sinusoidal waveform, using **Eqn 2-19** the line rms current, $I_{s,rms}$, over a line period is

$$I_{s,rms} = \sqrt{\frac{1}{T_{line}} \int_0^{T_{line}} \left[I_s(t) \right]^2 dt} \qquad \textbf{Eqn 2-20}$$

The instantaneous power, $P_{in}(t)$, over a complete line cycle is not constant, $P_{in}(t)$ is zero during the $V_s(t)$ zero crossing, and maximum when $\hat{V}_s$ is reached, Figure 1-7, and is calculated by

$$P_{in}(t) = V_s(t) I_s(t) \qquad \textbf{Eqn 2-21}$$

The average input power, P_{in}, during a half line cycle can be derived

$$P_{in} = \frac{1}{T_{line}/2} \int_0^{T_{line}/2} V_s(t) I_s(t) dt \qquad \textbf{Eqn 2-22}$$

As already detailed in Section 1.2.4 and Figure 1-7, the instantaneous load power, $P_o(t)$, is not equal to the instantaneous input power, $P_{in}(t)$, a capacitive storage component is required to provide a low frequency energy storage element. Assuming a sinusoidal input, unity power factor and a lossless converter, by equating the instantaneous input and output power under steady-state converter operating conditions the capacitor voltage ripple from [126] is expressed as

$$V_B(t) = V_B \sqrt{1 - \frac{P_o}{\omega C_B V_B} \sin(2\omega t)} \qquad \textbf{Eqn 2-23}$$

where P_o is the average output power, C_B is the S^{4}PFC boost capacitor.

Assuming that average input power, P_{in}, of the S^{4}PFC, is equal to the average output power , P_o, substituting **Eqn 2-14** and **Eqn 2-19** into **Eqn 2-22** and rearranging for the duty ratio, D, gives

$$D = \sqrt{\frac{2\pi L_B f_{sw} P_o}{\hat{V}_s^2 \int_0^{T_{line}/2} \frac{\sin^2(\omega t)}{1 - \frac{\hat{V}_s}{V_B}\left|\sin(\omega t)\right|} d\omega t}} \qquad \textbf{Eqn 2-24}$$

To ensure that the boost stage of the S^4PFC stays in discontinuous current mode, then **Eqn 2-25** must be satisfied for all operating conditions.

$$D + \delta < 1 \quad \forall \omega t \qquad \textbf{Eqn 2-25}$$

Assuming an ideal operation, using **Eqn 2-23**, the voltage transfer function of the continuous conduction mode forward converter stage of the S^4PFC can be expressed by

$$V_o = DV_B(t)N_{p,s} \qquad \textbf{Eqn 2-26}$$

where $N_{p,s}$ is the primary to secondary turns ratio of the transformer. **Eqn 2-26** shows that with a constant duty cycle, D, the twice line voltage ripple of $V_B(t)$ will appear at the output of the S^4PFC, but may be attenuated by the L_o-C_o output filter of the CCM forward stage, depending upon the design values of the components.Various control approaches to reduce this low frequency ripple voltage are detailed in [127, 128], however they both require complex control strategies.

To limit the current ripple through the output capacitor, C_o, and limit the overall power losses of the forward converter stage, the output inductor, L_o, operates in continuous conduction current mode for all operating conditions. Therefore, as opposed to **Eqn 2-25**, **Eqn 2-27** must be true for all operating conditions.

$$D + \partial = 1 \quad \forall \omega t \qquad \textbf{Eqn 2-27}$$

where ∂ is the duty ratio for the falling current I_{L_o} until the the next switching cycle. The output inductor, L_o, can be expressed as

$$L_o = \hat{V}_{L_o} \frac{DT_{sw}}{\hat{I}_{L_o}} \qquad \textbf{Eqn 2-28}$$

where $\hat{V}_{L_o}$ and $\hat{I}_{L_o}$ are the peak voltage across and current through L_o.

2.1.3 Integrated Magnetic Principles of Operation

The transformer and the boost inductor are combined in the S^4PFC topology, as seen in Figure 2-1. The aim is to reduce the overall component count without a detrimental impact on the performance. The approach taken is that the magnetic components should not interact, so the magnetic flux produced by one will result in zero net effect on the operation of the other. This section details the winding arrangement, the operation, and analysis of the integrated magnetic. Figure 2-9 shows the IM core, its windings and the flux paths.

The boost inductor, L_B, is split into two equal-turn windings, wound on the two outer legs of the E-core. The coil former for the spilt inductor windings is bespoke. The flux generated by the inductor, ϕ_{L_B}, plotted in red, flows in a clockwise direction around the outer legs of the core. Any flux flowing through the centre leg due to ϕ_{L_B} cancels itself out, as they have the same magnitude but opposite polarities, the result being that the centre limb can be used for the forward converter transformer.

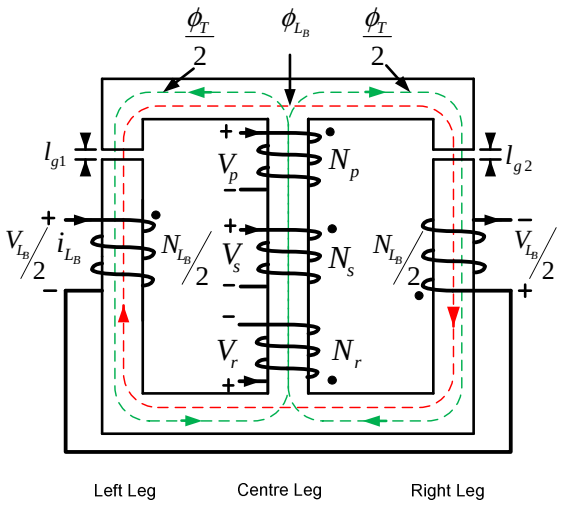


Figure 2-9 Winding arrangement of integrated magnetic E-core

Figure 2-10 shows the wave shape of flux ϕ_{L_B}, which mirrors I_{L_B}. As there is no magnetic flux in the centre limb produced by the inductor windings, any windings wound around the centre limb will not be coupled to L_B.

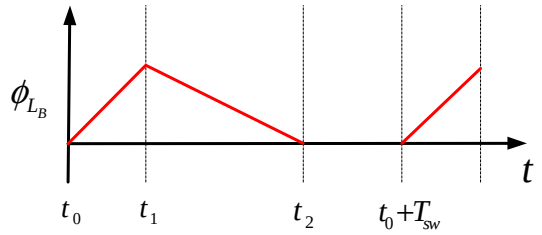


Figure 2-10 Inductor generated flux, ϕ_{L_B} in outer legs

The transformer windings, N_p, N_s, and N_r are wound around the centre leg of the E-core, which does not require a custom manufactured core or coil former. The flux generated by the transformer windings in Figure 2-9, ϕ_T, is drawn in green. Flux ϕ_T is generated in the centre leg, divides equally, assuming the outer limb air gaps are the same, and flows in opposite directions around the outer legs of the core. The magnitude and wave shape of ϕ_T in the three legs of the core are drawn in Figure 2-11.

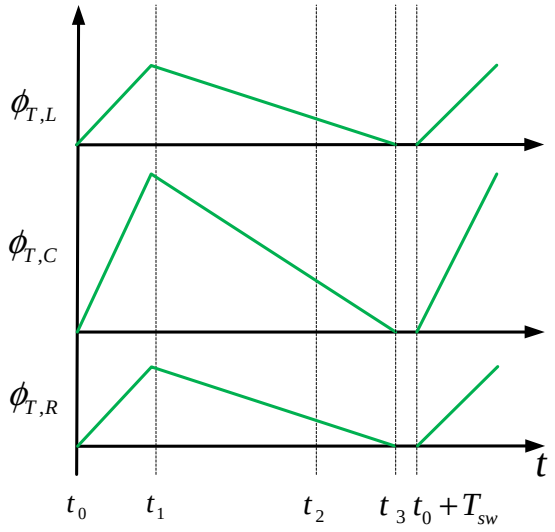


Figure 2-11 Transformer generated flux, ϕ_T **,** in all three core legs

As the two magnetic components are wound around the same core, the magnetic fluxes ϕ_T and ϕ_{L_B} interact, resulting in a modification of the total flux level ϕ_{lM}, Figure 2-12. Assuming that the magnetic material is linear and applying the superposition theorem, the instantaneous flux magnitude on the left leg of the core is determined by

$$\phi_{IM,L} = \phi_{L_B} - \phi_T \qquad \textbf{Eqn 2-29}$$

the instantaneous flux magnitude in the centre leg of the core is simply

$$\phi_{IM,C} = \phi_T \qquad \textbf{Eqn 2-30}$$

and finally, the instantaneous flux magnitude in the right leg of the core is

$$\phi_{IM,L} = \phi_{L_B} + \phi_T \qquad \textbf{Eqn 2-31}$$

In this example, from **Eqns 2-29** to **Eqns 2-31** it can be seen that there is an imbalance of flux levels. This results in a localised 'hot spot' of flux in the right leg of the magnetic core leading to an increase of localised core losses and temperature. This is unavoidable, as any other winding arrangement allows inductor flux to couple directly with the transformer windings which may adversely affect the single-stage power factor corrector operation of the converter. Alternative winding strategies are proposed in [99], which would ensure equal flux magnitudes in each limb, but were considered overly complex and likely to have an unacceptable cost penalty.

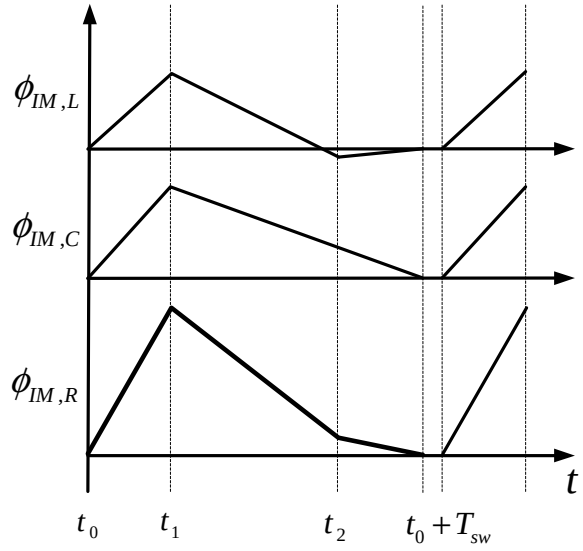


Figure 2-12 Integrated magnetic component flux, ϕ_{IM} **,** waveforms

To assist with the analysis, understanding and development of a SABER simulation model of the integrated magnetic component, a gyro-capacitor model of Figure 2-9 is shown

in Figure 2-13. This modelling approach is introduced in Section 1.2.6, and is a method that can express the non-linear effects and parasitics of a magnetic device whilst providing an insight to the core's operation [97-99]. For simplicity, flux leakage of the IM is neglected.

The magnetic core paths and permeances are represented by capacitors, where C_L is the left hand core limb, $C_{G,L}$ is the left hand core gap, C_C is the centre core limb, C_R is the right hand core limb and finally $C_{G,R}$ is the right hand core gap.

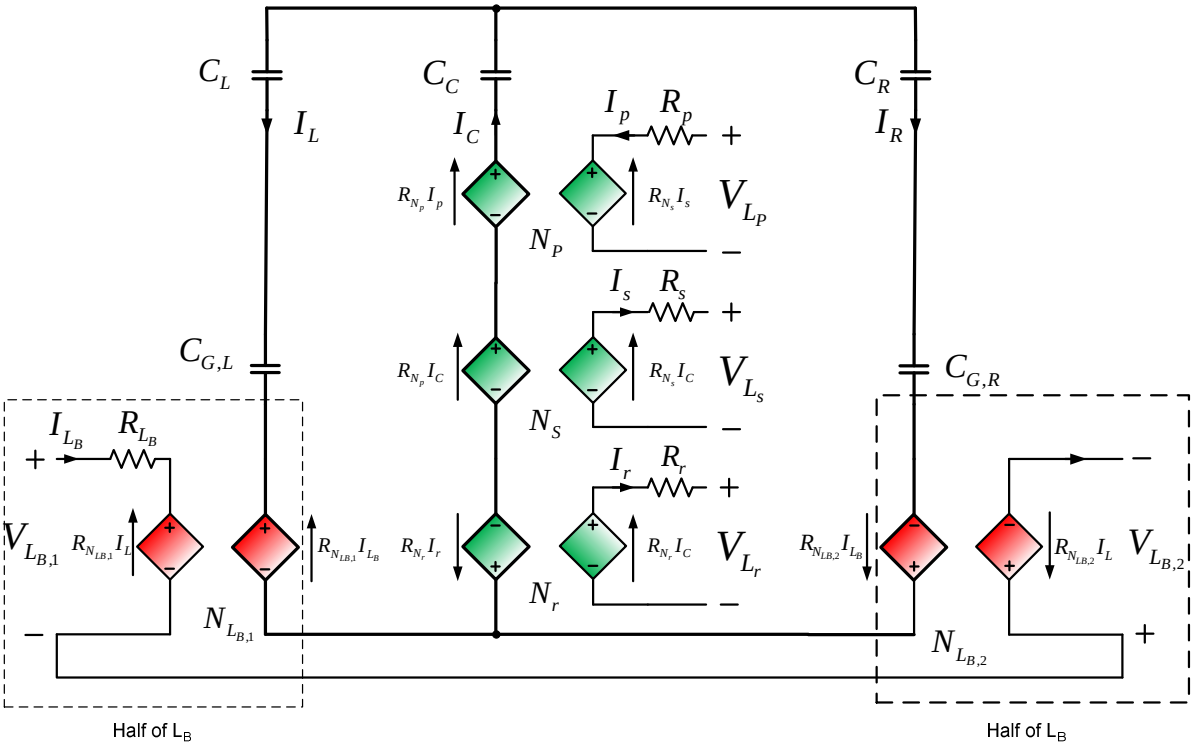


Figure 2-13 Gyro-Capacitor model of integrated magnetic component

The IM windings N_{L_B}, N_p, N_s and N_r are all represented by gyrators. The gyrator is an ideal two-port circuit element that reflects the impedance at one port as its reciprocal at the other, where R is the gyrator resistance of the respective winding, and a voltage source is reflected as a current source.

The inductor winding N_{L_B} is split equally between the two outer core legs of the IM and is represented by $R_{L_{B,1}}$ and $R_{L_{B,2}}$ respectively, with the inductor current I_{L_B} being identical through both windings.

The transformer windings N_p, N_s and N_r are modelled as gyrators R_{N_p}, R_{N_s} and R_{N_r} respectively around the IM centre limb. The voltage sources of all the gyrators appear as currents in the magnetic core path with the direction of current flow indicated.

2.2 S⁴PFC Prototype

This section details the design approach of the S⁴PFC based upon the analysis in sections 2.1.2 & 2.1.3. An iterative and practical approach is followed to determine the feasibility of the S⁴PFC with an IM component. Design variables such as maximum bus voltage, V_B, boost inductance, L_B, and $L_P/L_S/L_R$ ratios are selected whilst IM design approaches, converter power losses and cost analysis are considered. Steady-state SABER simulations are performed on the S⁴PFC and the IM to verify the theoretical analysis.

2.2.1 Single-Stage Single Switch Power Factor Correction Specification

Table 2-1 details the specification of the power stage, which were set by the sponsoring company PSU Designs. The S⁴PFC is designed to operate at a nominal 230 V_{rms} input with an output voltage of 14 V at power of 180 W. The converter must also comply with input current harmonic limitations for Class C equipment as shown in [13].

Table 2-1 S⁴PFC Converter with Integrated Magnetic Specification

Description		Value	Unit
Input Voltage	V_s	230 +10, -6%	V_{rms}
Max Input Current	I_s	0.92	A_{rms}
Output Voltage	V_o	14	V_{rms}
Output Voltage Ripple	$\tilde{V}_o$	100	mV
Output Current	I_o	12.8	A
Peak to Peak Inductor Ripple	$\tilde{I}_{L_o}$	3	A
Switching Frequency	f_{sw}	100	kHz
Line Operating Frequency	f_{line}	50	Hz
Output Power Range	P_{out}	90 - 180	W
Converter Efficiency	η_{PFC}	80 % @ 180 W	
Power Factor	PF	≥ 0.98	

2.2.2 Design Procedure

To ensure that the S[4]PFC meets the specified input current harmonic regulations detailed in section 2.2.1. The minimum $\hat{V}_s / V_B$ needs to be determined. The low frequency input current harmonics are generated due to the trailing edge boost current in each switching cycle. Assuming the line current I_s averaged over a line period, is symmetrical, the complex fourier coefficients of the input current shown in [129] are derived as

$$I_{s(n)} = \frac{1}{2\pi} \int_0^{2\pi} f(\theta) e^{-jn\theta} d\theta \qquad \textbf{Eqn 2-32}$$

where n is the harmonic number. Substituting **Eqn 2-19** into **Eqn 2-32** and plotting over a range of voltage ratios $\hat{V}_s / V_B$ using MATLAB Fast Fourier Transform simulator. The results for the dominant odd harmonics with respect to the fundamental are shown in Figure 2-14.

The line connecting the cross symbols in Figure 2-14, indicates the harmonic limits from the BS EN61000-3-2 standard Class C equipment [13]. The line marked with crosses indicates the boundary for the European applications, $V_{S\min} = 216\,V$, and the one marked with circles indicates the boundary for universal applications, $V_{S\min}$ = 90 V. From this the minimum permissible voltage ratios can be deduced, $\hat{V}_s / V_B < 0.95$ for European and $\hat{V}_s / V_B < 0.83$ for Universal applications.

It can be seen that the largest input current harmonics occur for large voltage ratios of $\hat{V}_s / V_B$ where the contribution of the trailing edge boost current, I_{L_B}, Figure 2-3, to the total input current is the highest. All input current harmonics diminish as the boost voltage, V_B, increases compared to the peak line voltage, $\hat{V}_S$. The third harmonic is the most dominant component, apart from the fundamental, well above 10 % for $\hat{V}_s / V_B$ ratios up to 0.43.

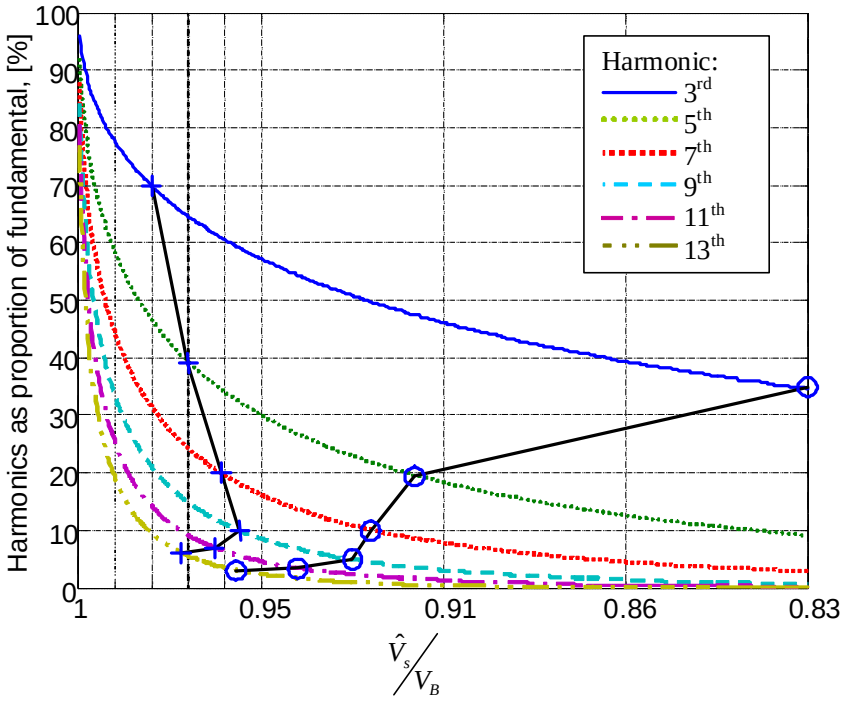


Figure 2-14 Dominant input current harmonics for a range of voltage ratios

To limit the MOSFET conduction losses, a low-voltage device is preferred. This however implies a low boost voltage and therefore a high distortion. Figure 2-14 is used to identify the minimum $\hat{V}_s / V_B$ ratio for which the input current harmonic content complies with Class C of [13].

Since the third harmonic, for practical voltage ratios ($\hat{V}_s / V_B \leq 0.91$), is much larger than the other harmonics, compliance with the standard in reference [13] for the third harmonic, usually guarantees fulfilment of the rest of the harmonics for this topology.

As well as determining the input current harmonics, the ratio $\hat{V}_s / V_B$ is required to determine the converter input power factor. PF defined by [126] and is expressed as

$$PF = \frac{P_{in}}{S_P} \qquad \textbf{Eqn 2-33}$$

where P_{in} is the real power, and S_p is apparent power. Substituting **Eqn 2-19** and **Eqn 2-22** into **Eqn 2-33** gives the form

$$PF = \frac{P_{in}}{V_{s,rms} I_{s,rms}}$$ **Eqn 2-34**

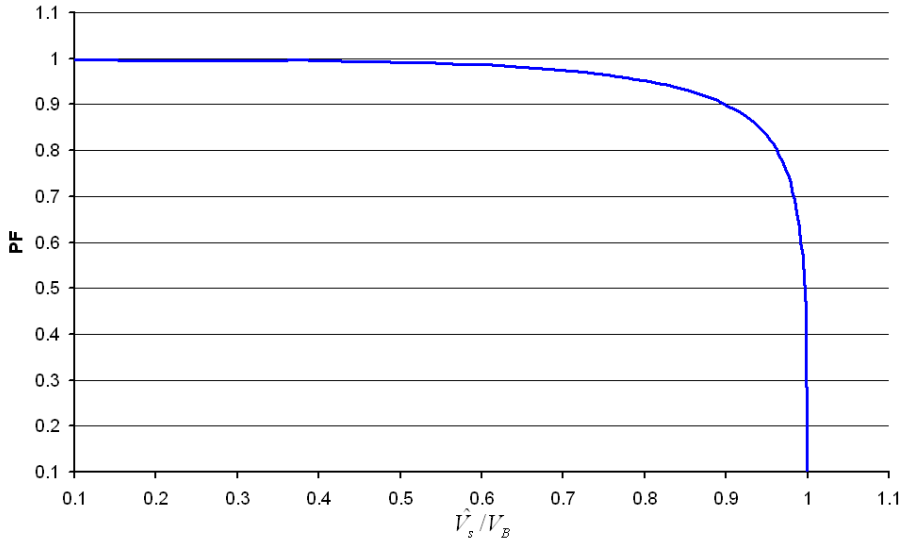


Figure 2-15 Power factor versus $\hat{V}_s / V_B$

Plotting **Eqn 2-34** over a wide range of $\hat{V}_s / V_B$ gives Figure 2-15. The BS EN 61000-3-2 standard [13] does not specifically state a minimum power factor requirement. However, a value of power factor is required in order to determine the maximum permissible third harmonic current, expressed as a percentage of the fundamental, for Class C equipment. To ensure low input current harmonics, a high power factor, whilst limiting peak semiconductor current losses a $\hat{V}_s / V_B$ ratio of 0.7 is selected, giving a PF of approximately 0.98, and a third harmonic 30 % of the fundamental frequency line current.

The boost stage inductor, L_B, not only determines the peak switching current, $\hat{I}_{L_B}$, but also peak magnetic core losses, power semiconductor conduction losses, the output boost voltage, V_B, and more critically the converter stage operating mode. **Eqn 2-25** identifies the condition that should be met in order for the PFC stage to remain in the DCM throughout the entire line cycle. During a single switching cycle, see Figure 2-3 , the boost stage inductor, L_B, volt second balance is derived as

$$|V_s| DT_{sw} = |V_s - V_B| \delta T_{sw}$$ **Eqn 2-35**

Using **Eqn 2-14** and **Eqn 2-35**, **Eqn 2-25** now becomes

$$D\left(1+\frac{\hat{V}_s \sin\omega t}{V_B-\hat{V}_s \sin\omega t}\right)\le 1 \quad (0\le \omega t\le \pi) \qquad \textbf{Eqn 2-36}$$

Eqn 2-36 shows that L_B is most susceptible to entering the CCM at the peak of the line voltage, $\hat{V}_s$. Using the MATLAB symbolic toolbox, the critical value of L_B to maintain DCM over half a line period is determined by substituting **Eqn 2-24** into **Eqn 2-36**, giving

$$L_{B,crit}=\frac{\left(1-\frac{\hat{V}_s}{\hat{V}_B}\right)^2 \hat{V}_s^{\,2}}{2P_o f_{sw}\pi}\int_0^{\pi}\frac{\sin^2\omega t}{1-\frac{\hat{V}_s}{\hat{V}_B}\sin\omega t}d\omega t \qquad \textbf{Eqn 2-37}$$

To determine the critical boost inductance, Figure 2-16 plots **Eqn 2-37** with $\hat{V}_s/V_B$ ratio of 0.7, an output power of 180 W and a switching frequency of 100 kHz, determined in Table 2-1.

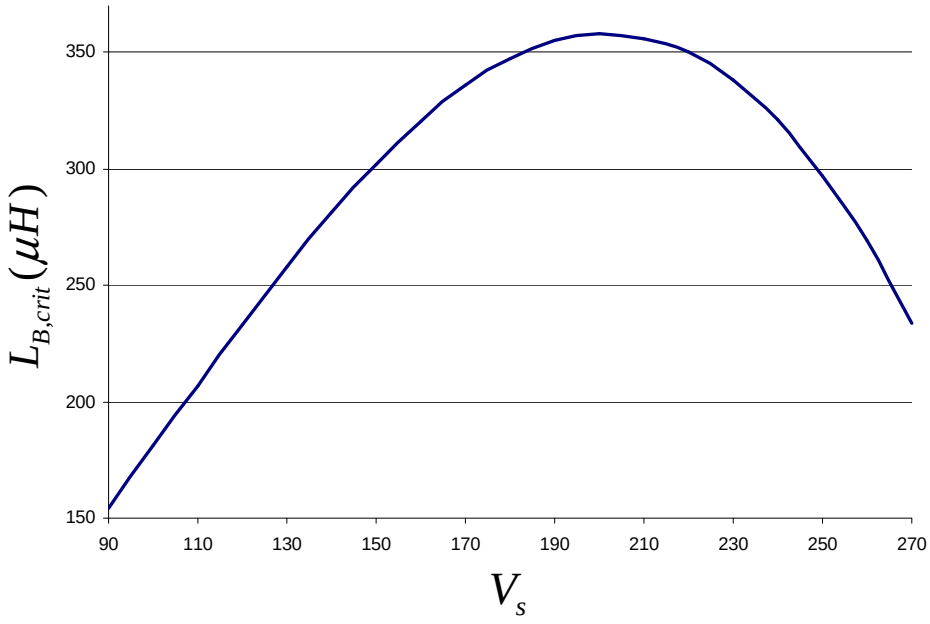


Figure 2-16 $L_{B,crit}$ over the universal line input voltage range

In order to maintain DCM for all operating conditions $L_B < L_{B,crit}$. Figure 2-16 plots **Eqn 2-37** over a universal input voltage range with an output power of 180 W. Aware of the limited winding space available on an integrated magnetic E-Core, the number of turns that can be wound round the outer limbs and the packing factor, an inductance of 111 μH is chosen for L_B. This value of L_B, guarantees that the converter PFC stage stays in DCM despite not achieving the minimum $\hat{I}_{L_B}$ possible.

The instantaneous boost stage capacitor voltage, $V_B(t)$, is given by **Eqn 2-23**. Plotting this equation for various capacitances at output powers of 90 W & 180 W, the twice line ripple frequency voltage ΔV_B is shown in Figure 2-17. Decreasing the $\hat{V}_s / V_B$ ratio would reduce ΔV_B further, however the peak voltage stresses across components would increase.

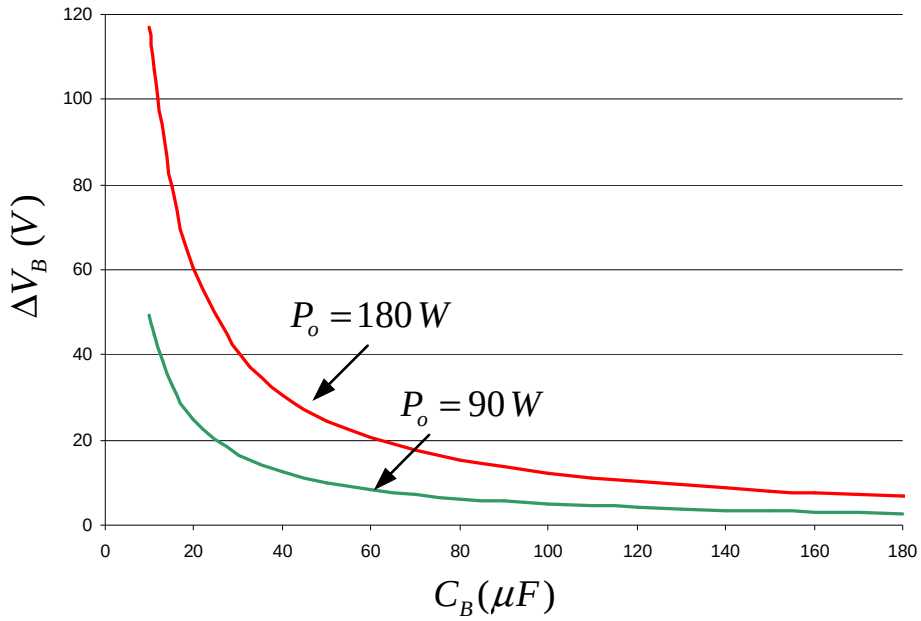


Figure 2-17 Boost capacitor stage low frequency voltage ripple at P_o= 90 W & 180 W

Table 1-2 in section 1.2.7.4 summarises the performance and specification parameters of a number of different capacitor types. Figure 2-17 shows that a capacitance of > 180 μF would provide the lowest ΔV_B. Electrolytic capacitors can both adequately withstand high voltages whilst providing sufficient capacitance for energy storage, however this capacitance is not achievable at a $\hat{V}_B$ of 570 V, unless specialised devices are used. Capacitors of the 350

V range are more readily available, therefore two 100 μF 350 V components in series are used.

Since the CCM forward converter stage utilises the same MOSFET as the DCM boost converter, the turns ratio of $N_{p,s}$ of the S^4PFC are dictated by the values chosen for the ratio of V_B/V_o and the duty cycle, unlike a standard forward converter.

As the parameters such as duty ratio, D, and boost capacitor voltage, V_B have already been determined by the requirements of a high input power factor and low input current harmonics, in order to realise the low output voltage, V_o, listed in Table 2-1, then only the primary-secondary turns ratio, $N_{p,s}$, of the IM can achieve this. Using the steady-state voltage conversion ratio of a continuous conduction mode forward converter, $N_{p,s}$ the required turns ration is calculated as

$$N_{p,s} = \frac{V_o}{DV_B} \qquad \textbf{Eqn 2-38}$$

At a nominal input line voltage and a maximum output power of 180 W, the duty ratio D= 0.16 generates V_B of 460 V, therefore using **Eqn 2-38** the turns ratio of the S^4PFC $N_{p,s}$ is 0.19.

To limit the MOSFET peak voltage, $\hat{V}_Q$ during the transistor off-time, assuming that the transformer reset time is equal to the transistor off-time, then the ratio of $N_{r,p}$ is calculated by

$$\frac{N_r}{N_p} = \frac{V_0}{\hat{V}_Q - V_B} \qquad \textbf{Eqn 2-39}$$

where N_r and N_p are the number of turns of the IM core reset and primary windings respectively. Again using the converter operating parameters that have been already defined, the reset-primary turns ratio $N_{r,p}$ is 0.13. Determining the IM primary winding inductance, L_p, is an iterative process, as if too a low value is used $\hat{I}_{L_p}$ will become large, increasing the

primary conduction losses. Also if the number of turns in the windings is too low, the core flux will be excessive, resulting in high core losses even saturation.

If L_p is too large, then the total number of turns, N_p, may not be accommodated by the IM winding window. Efficient power MOSFETs that can withstand the converter parameters thus far are detailed in section 2.3, and using **Eqn 2-2** and **Eqn 2-3**, L_p is defined as 1.1 mH. The turns ratios defined in **Eqn 2-38** and **Eqn 2-39** define L_s and L_r as 41 μH and 20 μH respectively.

To ensure that the forward converter stage of the S^{4}PFC stays in continuous conduction current mode for all operating conditions, the peak to peak current ripple of the output inductor, $\tilde{I}_{L_o}$, must be smaller than $\tilde{I}_{L_o}$ defined in Table 2-1. The output inductor L_o is expressed as

$$L_o = \frac{V_{D_4} - V_o}{\tilde{I}_{L_o}} \qquad \textbf{Eqn 2-40}$$

Using **Eqn 2-40**, L_o is chosen as 60 μH.

2.2.3 Design Summary

Table 2-2 lists a summary of the key component values derived in section 2.2.2.

Table 2-2 S^{4}PFC key component values

Parameter	Calculated	Unit
L_B	111	μH
L_p	1100	μH
L_s	41	μH
L_r	20	μH
L_o	60	μH
C_B	50	μF
C_o	1000	μF

Using the component values listed in Table 2-2, and the design approaches in section 2.1.2, Table 2-3 lists the key calculated values of the S^4PFC with a nominal input voltage of 230 V_{rms} and an output power, P_o of 180 W and 90 W.

Table 2-3 Key calculated values of S^4PFC at a P_{out} of 180 W and 90 W

Parameter	P_{out}= 180 W	P_{out}= 90 W	Unit
	Calculated	Calculated	
V_s	230	230	V_{rms}
$\hat{I}_s$	1.37	0.59	A
f_{line}	50	50	Hz
f_{sw}	100	100	kHz
D	0.16	0.13	-
$\hat{\delta}$	0.40	0.21	-
$\hat{I}_{L_B}$	4.8	3.8	A
$\hat{V}_Q$	563	663	V
$\hat{I}_Q$	7.9	5.7	A
V_B	460	566	V
$\hat{I}_{L_p}$	3.15	1.92	A
V_o	14	14	V

2.2.4 Integrated Magnetic Design

This section details the design procedure for selecting, gapping and winding the integrated magnetic component. The principles of the integrated magnetic component operation and winding arrangement are introduced in section 2.1.3, the aim of the IM is to reduce the overall component count without having a detrimental impact on the performance of the S^4PFC. A winding approach is already proposed so that the magnetic components do not interact, therefore the magnetic flux produced by one will result in zero net effect on the operation of the other, Figure 2-12. Despite there being no magnetic coupling, the two magnetic components are utilising the same core, and so the design procedure must be complementary to ensure that the magnetic core can not only achieve the desired electrical performance but also accommodate the total number of windings. Figure 2-19 shows a flow chart detailing the iterative design process followed for the integrated magnetic component.

The first stage of the integrated magnetic design is the selection of a suitable core material. Table 2-3 details the switching frequency of the S^4PFC converter, a ferrite material survey using [130], shows 3F3 to be the least lossy at this frequency range.

Selecting the E-Core size is an iterative process, as it is not yet known whether the initially selected core will suffice until the design process in Figure 2-19 is completed. After a number of iterations however the core size ETD 44 is selected. An ETD E-Core construction was chosen due to the centre limb of the core being circular in cross section, therefore increasing the winding area window and increasing the packing factor [130]. The maximum allowable peak flux density, $\hat{B}$, is determined from the magnetics ferrites core manual.

Due to the custom gapping arrangement used in the integrated magnetic, that is only the outer limbs are gapped, the gap was calculated in the following way.

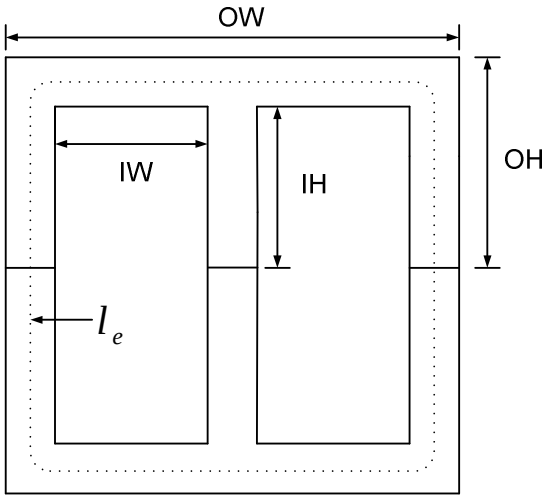


Figure 2-18 ETD core dimensions, not to scale

Using the physical core dimensions from Figure 2-18, the effective magnetic core path length, l_e, the effective core volume, v_e, and the effective cross sectional areas, A_e of each of the limbs are identified.

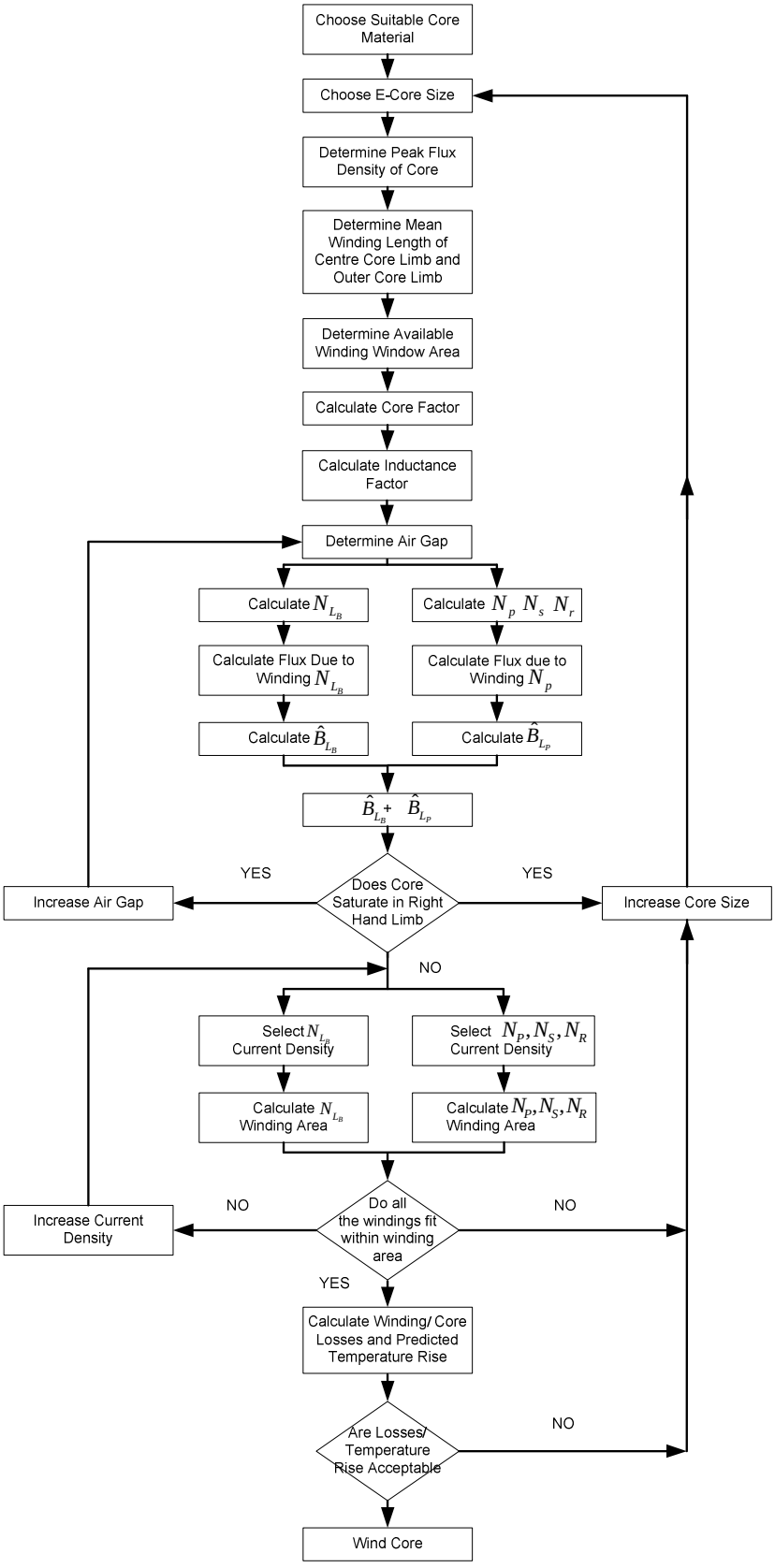


Figure 2-19 Flow chart for the design of the integrated magnetic component

Using the physical dimensions of the selected core, the effective permeability of the core, μ_e is calculated as

$$\mu_e = \frac{\mu_i}{1+\left(\frac{G\mu_i}{l_e}\right)} \qquad \textbf{Eqn 2-41}$$

where μ_i is the initial permeability of the core, [130], and G is the air gap length.

The inductance factor is determined by

$$A_L = \frac{\mu_o \mu_e}{\Sigma(l/A)} \qquad \textbf{Eqn 2-42}$$

where μ_0 is the permeability of free space, $4\pi\times10^{-7}$ Hm^{-1}, and $\Sigma(l/A)$ is the core factor, a ratio of the sum of the core limb lengths and cross sectional areas.

Using the required inductance values listed in Table 2-2, the total number of turns for N_{L_B}, N_p, N_s and N_r respectively is found using

$$N = \sqrt{\frac{L}{A_L}} \qquad \textbf{Eqn 2-43}$$

Using Faraday's law, the peak AC flux, $\hat{\phi}_N$, generated in a winding is

$$\hat{\phi}_N = \frac{V_N}{N} DT_{sw} \qquad \textbf{Eqn 2-44}$$

where V_N is the voltage across the winding. The total flux in each core limb is found using **Eqn 2-29** to **Eqn 2-31** in section 2.1.3

The peak flux density in each core limb is

$$\hat{B} = \frac{\hat{\phi}_T}{A_e} \qquad \textbf{Eqn 2-45}$$

where $\hat{B}$, $\hat{\phi}_T$ and A_e, are the peak flux density, peak flux and core cross sectional area respectively of that particular limb.

From Figure 2-17, if the peak flux density in the right hand core limb, $\hat{B}_R$, exceeds the already established maximum peak flux density of the core, then either increase the core air gap length or increase the core size. If $\hat{B}_R$ is within limits, the windings N_{L_B}, N_p, N_s and N_r can now be calculated. Selecting the current density, J, for each winding, the total cross sectional area of wire, A_{cu}, is

$$A_{cu} = \frac{I_{rms}}{J} \qquad \textbf{Eqn 2-46}$$

where I_{rms} is the respective RMS current of that particular winding. The skin depth, SK, of the current in each of the windings is calculated as

$$SK = \frac{66}{\sqrt{f_{sw}}} \quad (mm) \textbf{ [131]} \qquad \textbf{Eqn 2-47}$$

Due to the skin and proximity effects, multiple parallel wire strands are used to minimise the AC resistance of the winding.

Should $A_{cu,total}$, shown in **Eqn 2-48**, be less than the total core winding area available then the core may be wound, if not, then the winding current densities, J, must be increased.

$$A_{cu,total} = p\sum_n N_n A_{cu_n} \qquad \textbf{Eqn 2-48}$$

where $n = N_{L_B}, N_p, N_s, N_r$ and p is the packing factor which includes winding build up and insulation.

The DC wire resistance of each winding is determined by

$$R_{dc} = \rho \frac{l_{cu}}{A_{cu}} \qquad \textbf{Eqn 2-49}$$

where ρ is the resistivity of copper, and is $1.724\times10^{-6}\,\Omega cm$ at $20\,^{\circ}C$.

The AC wire resistance of each winding is determined by

$$R_{ac} = \frac{8.32\times10^{-5}\sqrt{f_{sw}}}{SK} \qquad \textbf{Eqn 2-50}$$

Table 2-4 lists the IM component parameters, including the magnetic core details, the number of turns required for each winding, the peak flux generated in each winding and finally the main integrated magnetic loss components.

Table 2-4 Integrated magnetic core parameters and operating values at 180 W

Parameter					**Unit**
Core manufacturer	Ferroxcube				-
Core type	ETD 44				-
Core material	3F3				-
Effective volume	17800				mm^3
Effective length	86				mm
Effective area	174				mm^2
Max flux density	350				mT
Initial permeability	1740				-
Effective permeability	50				-
	C_C		**$C_{L,R}$**		
Core factor	0.589		0.164		mm^{-1}
Mean turn length	77		56		mm
Inductance	**L_B**	**L_p**	**L_s**	**L_r**	
	111	1100	41	20	µH
Number of turns	32	101	20	14	-
Flux	20	7.8	-		µWeb
Flux density	111	40	-		mT
Wire length	2.77	7.8	1.51	1.05	m
Current density	3.00	3.00	3.00	3.00	A/mm^2
Wire diameter	0.82	0.68	1.42	1.03	mm^2
Skin depth	0.20	0.20	0.20	0.20	mm
DC Wire resistance	0.24	0.25	0.12	0.16	Ω
AC Wire resistance	0.35	0.95	0.91	0.33	Ω
Copper loss @ 100°C	1.46	1.42	3.76	1.41	W
Core loss @ 100°C	0.51	0.05	-		W
Total losses @ 100°C	**8.57**				W

Numerous transformer winding arrangements were investigated, but the winding arrangement seen in Figure 2-20 was found to minimise leakage between the transformer windings N_p, N_s and N_r, and minimise losses due to winding proximity effects.

The primary winding, N_p, is divided in two and sandwiched between windings N_s and N_r. This results in a transformer winding arrangement, of a layer of ½ N_p, a layer of N_r, the second layer of ½ N_p and finally a layer of windings of N_s. This transformer winding arrangement also allows for the effective cooling of N_s as it is the most lossy winding in the IM device due to the high current of the output of the converter. The boost inductor windings N_{L_B} are a single layer of turns around the two outer legs of the core.

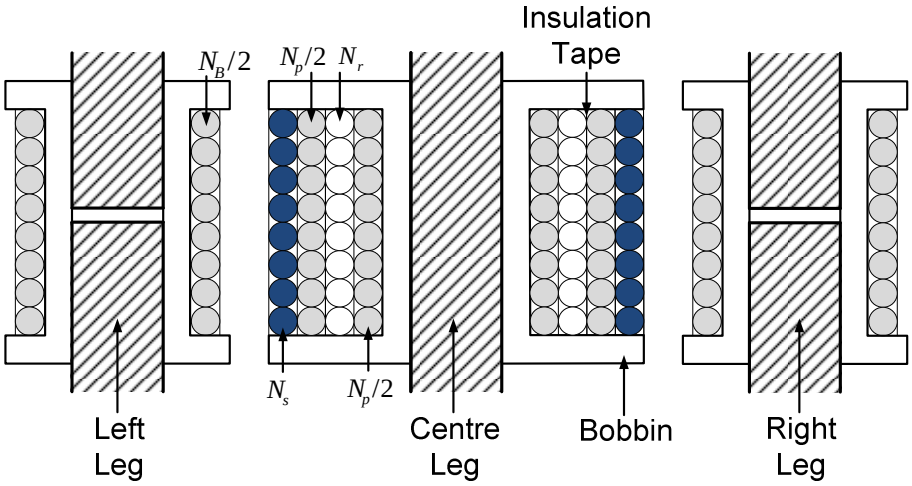


Figure 2-20 Cross section of transformer winding arrangement

The final magnetic prototype incorporating all of the windings is shown in Figure 2-21. It can be seen that all of the window area available for winding is used and is the main limiting factor for this IM design. A higher value of L_B would be ideal to reduce the $\hat{I}_{L_B}$, but with this core, the window area is insufficient.

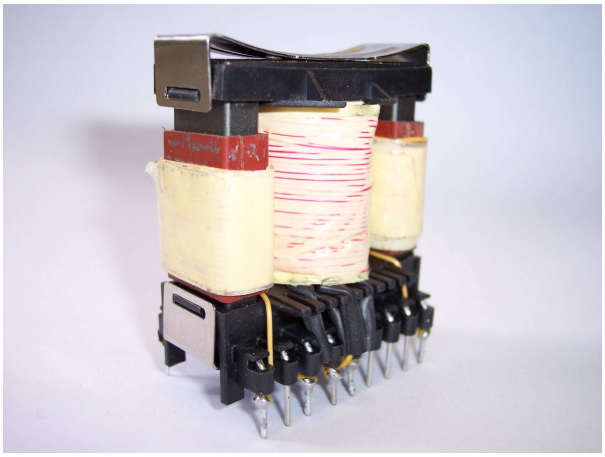


Figure 2-21 Integrated magnetic prototype

2.3 Component Selection and Loss Audit

MOSFET devices are the natural choice for this low power high frequency application. Assuming that the voltage and current waveforms at the switching instants of the MOSFETs are linear, an approximation of MOSFET losses was made using the procedure set out in Appendix A. A number of suitable MOSFETs for Q were identified and listed in Table 2-5. Despite MOSFET FQP3N80 being the cheapest, its switching losses are the highest. To strike a balance between cost and efficiency **STW10NK80** was chosen. The costs of all components in this section are single piece quotes at 2009 prices.

Table 2-5 Selection of suitable Si MOSFETs for Q

Component	Voltage Rating (V)	Continuous Current (A)	Rds_{on} Norm (Ω)	T_r (ns)	Power Loss (W)	Device Cost (£)
STW10NK80	800	9	1.6	27	8.62	2.55
FQP3N80	800	3	4.0	40	26.5	0.31
STP8NK80	800	6	1.75	14	13.6	2.96
SPA11N80C3	800	11	0.7	37	1.57	3.77

Despite silicon carbide diodes, discussed in section 1.2.7.1, having very low switching losses, they are expensive, therefore all of the diodes shortlisted in Table 2-6 to Table 2-9 are silicon devices. Table 2-6 is a shortlist of suitable diodes for D_1. Again, assuming that the voltage and current waveforms at the switching instants of the diode are linear, an approximation of diode losses was made using the procedure set out in Appendix B. Diode

BYV-29 has the lowest estimated losses, however the cost is more than twice that of diode **SF36** whose combined conduction and switching losses are comparable, therefore the **SF36** is the preferred device for D_1.

Table 2-6 Selection of suitable Si diodes for D_1

Diode	Rated Voltage (V)	Rated Current (A)	T_{rr} (ns)	Forward Voltage (V)	Power Loss (W)	Cost (£)
UF5408	1000	3	75	1.70	1.8	0.30
SF36	400	3	35	1.30	1.4	0.52
FEP14GT	400	16	50	1.30	1.5	0.90
BYV-29	400	9	60	1.03	1.1	1.7

Table 2-7 is a list of a number of diodes appropriate for D_2. As the current I_{D_2} is discontinuous, the switching losses are significantly lower. Diode FEP16GT has the lowest estimated losses. Diode UF5408 is the least expensive device but has the highest losses. **SF38** is the preferred device based upon cost despite having similar estimated losses as 31DF6.

Table 2-7 Selection of suitable Si diodes for D_2

Diode	Rated Voltage (V)	Rated Current (A)	T_{rr} (ns)	Forward Voltage (V)	Power Loss (W)	Cost (£)
UF5408	1000	3	75	1.70	2.2	0.30
SF38	600	3	35	1.70	2.0	0.52
FEP16GT	600	16	50	1.50	1.6	0.90
31DF6	600	3	35	1.70	2.4	0.86

A common cathodes dual diode package was chosen for D_3 and D_4 to reduce the overall component count. The candidate components are listed in Table 2-8, of those listed the **BYW51-200** is selected due to the lowest power loss and relative cost.

Table 2-8 Selection of suitable Si diodes for D_3 and D_4

Diode	Rated Voltage (V)	Rated Current (A)	T_{rr} (ns)	Forward Voltage (V)	Power Loss (W)		Cost (£)
					D_3	D_4	
BYW51-200	200	10	25	0.85	4.0	8.0	0.60
DSA-20	100	10	40	0.80	3.8	7.5	0.69
ON-BMRF20	100	10	30	0.85	4.1	8.0	1.28

The possible components for the transformer reset diode, D_5, are seen in Table 2-9. Due to the low forward voltage drop and low piece cost, the diode **UF5401** is the most suitable device in this case.

Table 2-9 Selection of suitable Si diodes for D_5

Diode	Rated Voltage (V)	Rated Current (A)	T_{rr} (ns)	Forward Voltage (V)	Power Loss (W)	Cost (£)
UF4004	400	1	75	1.7	4.0	0.09
UF5401	100	3	50	1.0	2.5	0.41
HERG302	100	3	50	1.0	2.5	0.57
ES3B100	100	3	30	0.62	1.5	0.69

Table 2-10 lists a number of suitable electrolytic capacitors for C_B. To achieve the necessary capacitance and voltage stresses, yet be capable of withstanding the ripple current, two 350 V capacitors need to be arranged in series. For each of these devices, calculations in Appendix C show that capacitor **EEUE2E101** generates the lowest losses and is relatively inexpensive.

Table 2-10 Selection of suitable electrolytic capacitors for C_B

Capacitor	**Rated Capacitance** (uF)	**Rating Voltage** (V)	$\mathbf{I_{rms}}$ (mA)	$\tan\delta$	**Power Loss (W)**	**Cost (£)**
EEUE2E101	100	350	2100	0.15	0.03	1.53
107LBB400-M2	100	350	1700	0.15	0.02	2.97
EEUE2V101	100	350	1600	0.20	0.03	0.57
TF10118-X25	100	350	2160	0.15	0.02	1.78

Suitable output capacitors for C_o are detailed in Table 2-11. Due to converter output voltage ripple requirements, these capacitors are electrolytic devices. As V_o is relatively low, there is no requirement to series this component, therefore capacitor **EKZE250ELL** is selected.

Table 2-11 Selection of suitable electrolytic capacitors for C_o

Capacitor	**Rated Capacitance** (uF)	**Rating Voltage** (V)	$\mathbf{I_{rms}}$ (mA)	$\tan\delta$	**Power Loss (W)**	**Cost (£)**
108KXM025	1000	25	2360	0.14	0.004	0.77
EKZE250-ELL	1000	25	2360	0.14	0.004	0.43
25YXF1000	1000	25	2360	0.14	0.004	0.67
25ZKL1000	1000	25	2250	0.16	0.005	0.90

For the selected devices Figure 2-22 shows a breakdown of the estimated power losses in the S^4PFC operating at a worst case condition of V_s= 216 V_{rms}, a maximum duty ratio of 20 % and a P_{out}= 180 W. Parasitic losses in the input filter, input rectifying diodes, PCB tracking, input/ output connectors and control circuitry are ignored and not included in this analysis. The components used were not only selected due to their electrical characteristics but also due to their cost and availability, to ensure that the overall system costs were comparable to those of a two-stage PFC/regulator approach.

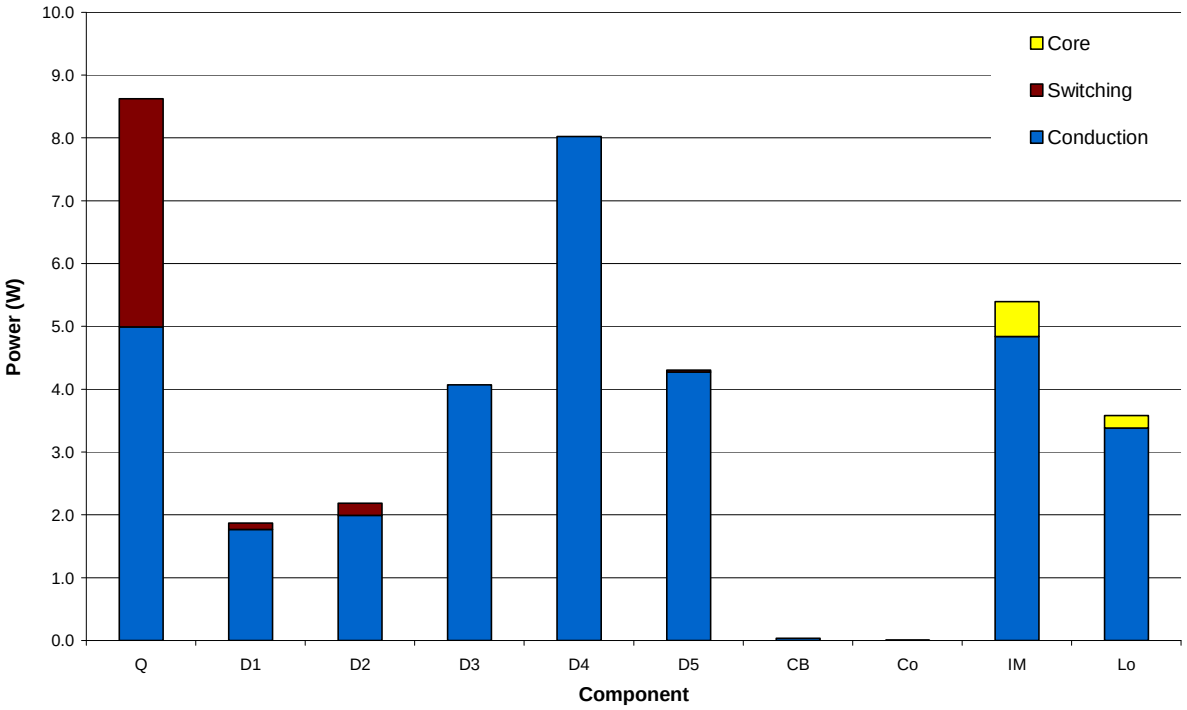


Figure 2-22 Estimated power losses in S^4PFC power devices.

The MOSFET, STW10NK80, exhibits the largest single loss of all the power devices in the S^4PFC, with 5 W of conduction loss and 3.6 W of switching losses. The MOSFET SPA11N80C would have produced a total loss of 1.57 W, but the cost is significantly higher.

Diodes D_1 and D_2 are UF5408 and have comparable losses of 1.87 W and 2.18 W. The conduction losses are the dominating loss contributor, and could be significantly reduced by using SiC diodes, but again like the MOSFET would impact the overall cost of the S^4PFC.

The forward converter stage rectifying diodes D_3 and D_4 are a single package device consisting of two diodes, BYW51-200. This package is carefully heat-sinked, as the combined power losses of the two diodes are the largest single heat source in the converter. Like D_1 and D_2, the diodes have little switching losses.

Table 2-12 A summary of the expected losses detailed in Figure 2-22

Device	Component	Loss (W)
Q	STW10NK80	8.62
D_1	SF36	1.87
D_2	SF38	2.18
D_3	BYW51-200	4.06
D_4	BYW51-200	8.02
D_5	UF4004	4.03
C_B	EEUE2E101	0.02
C_o	EKZE250ELL	0.004
IM	-	8.57
L_0	-	3.58
Total		**40.95**
Efficiency		**81.4%**

If the more efficient devices were used the estimated power loss of the S^4PFC would be 27.4 W with a system efficiency of 87 %. However the relative component cost increase would be 55 %, which would have made the converter uncompetitive for the target application.

2.4 Steady-State SABER Simulation

A SABER model was designed to confirm the predicted results detailed in Table 2-3. Figure 2-23 shows an idealised model of the S^4PFC with an IM component, a simple control block provides the duty cycle pulses to achieve the necessary output voltage. A differential mode filter and line-frequency rectifier is included for completeness.

The converter was modelled by assuming all the power stage components are ideal devices, the MOSFET is modelled as an ideal switch with zero on-state resistance and infinite off-state resistance. The power diodes are piece wise linear components with zero forward volt drop. The output capacitors are also ideal with no parasitic resistance or inductance. The integrated magnetic, comprising the boost inductor and the forward converter transformer is modelled discretely. The core legs are modelled by their respective inductance factors, A_L, derived from the core dimensions detailed in [130] and respective air gaps, section 2.2.4. The magnetic core material is ideal, with no hysteresis losses. The IM windings, are lossless, with no parasitic resistance, interwinding capacitance or leakage inductance.

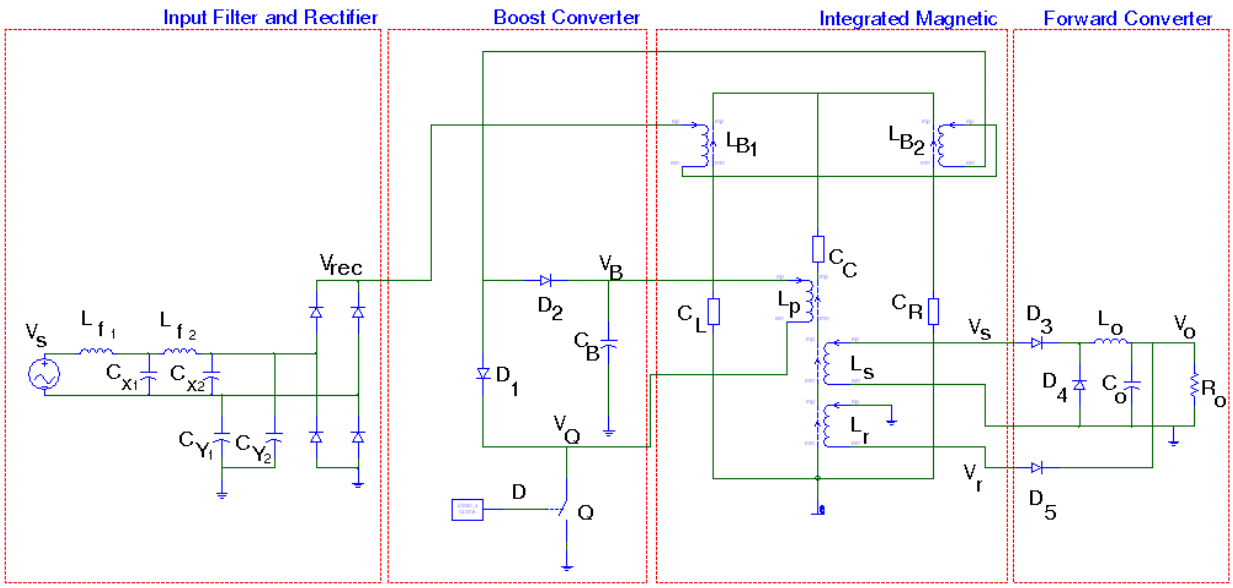


Figure 2-23 SABER schematic capture of S^{4}PFC with IM

The following simulation results demonstrate the steady-state performance of the S^{4}PFC for **V_o= 14 V, L_B= 111 µH, L_p= 1.1 mH, L_s= 41 µH, L_r= 20 µH, L_o= 60 µH, C_B= 50 µF, C_o= 1000 µF** and f_{sw} = **100 kHz**.

Figure 2-24 shows a number of key simulated waveforms for the S^{4}PFC operating over a number of switching frequency cycles at an input voltage **V_s= 230 V_{rms}** and an output power **P_{out}= 180 W**. All waveforms are captured at $\hat{V}_s$.These ideal simulated waveforms closely correspond to the theoretical waveforms seen in Figure 2-3, and to the calculated results as seen in Table 2-3. Despite using an integrated magnetic component, the winding arrangement of the two magnetic components does not impact upon the performance of the S^{4}PFC.

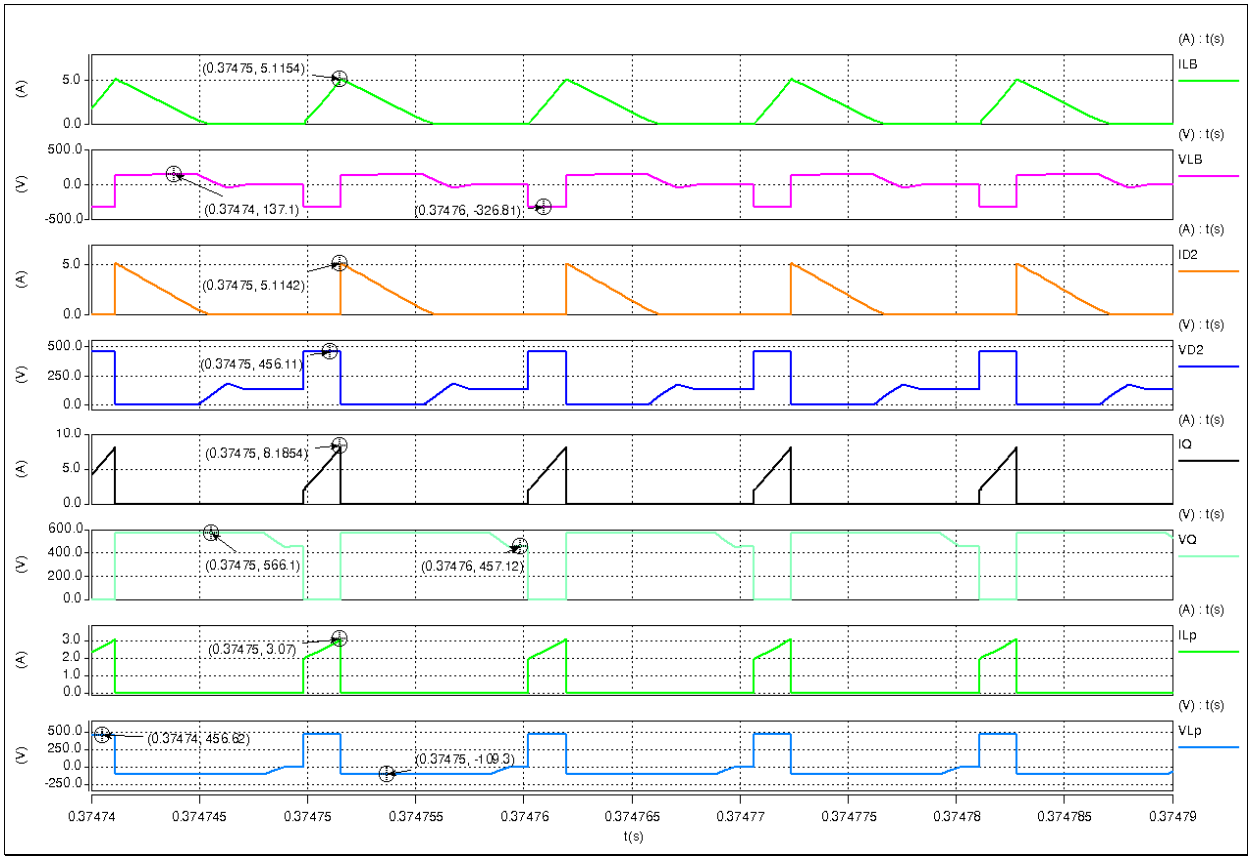


Figure 2-24 Key SABER simulated waveforms, V_s=230 Vrms, P_o=180 W

Figure 2-25 details simulation results demonstrating the steady state performance of the S^4PFC, again, for an input voltage V_s= 230 V_{rms} and V_o= 14 V**,** however the output power is P_{out}= 90 W. All other component values are as before. Once again, the steady state measurements from SABER simulations correspond closely with calculated results, as shown in Table 2-13.

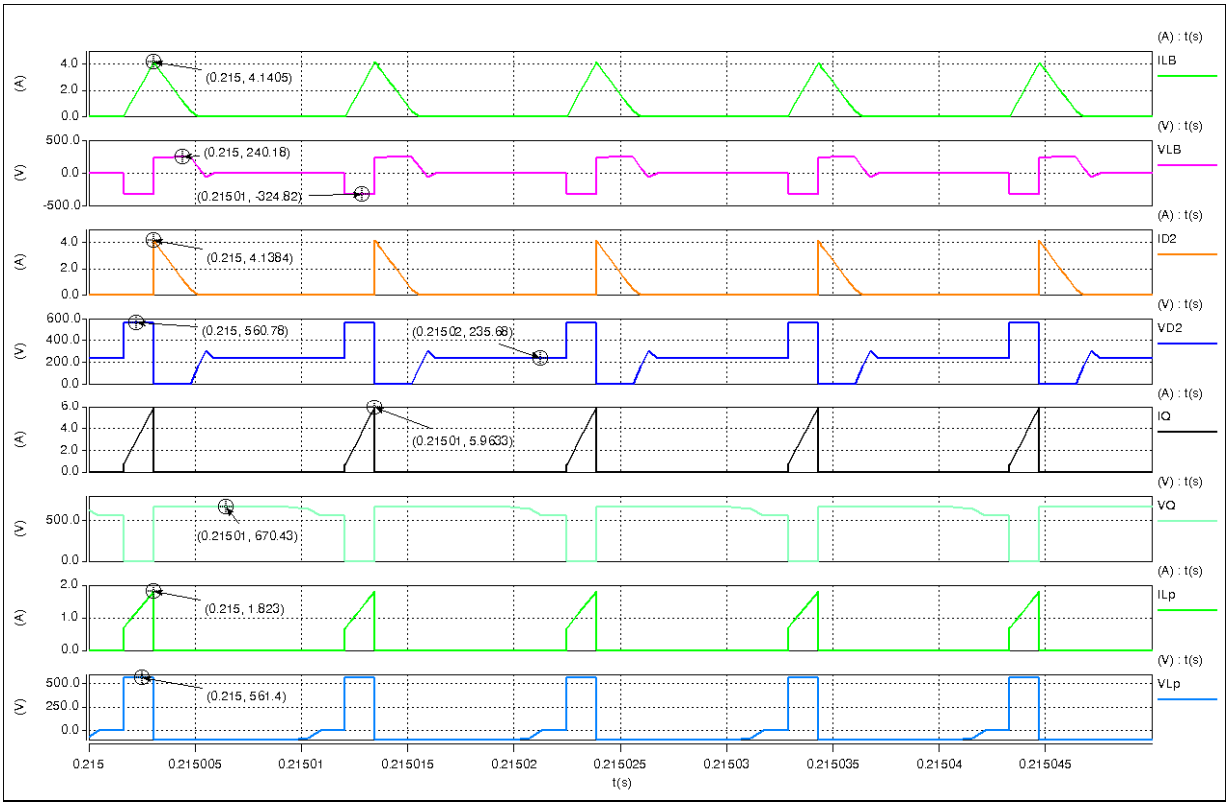


Figure 2-25 Key SABER simulated waveforms, V_s=230 Vrms, P_o=90 W

Figure 2-26 shows plots of V_s, I_s, V_B and V_o over a number of line cycles with a power output of 180 W. As the boost stage of the S^{4}PFC is operating in DCM, I_s is proportional and in phase with V_s, indicating a near unity power factor and low harmonic current content. The input current, I_s, is not purely sinusoidal however, this is due to the non-linear operation of the DCM boost converter. The twice mains frequency voltage ripple can be clearly seen in the trace of V_B. The amplitude of the AC ripple decreases with reduced load, but the DC level of V_B increases with the lighter load. The output voltage, V_o, has a small AC ripple component, due to the twice mains frequency ripple of V_B.

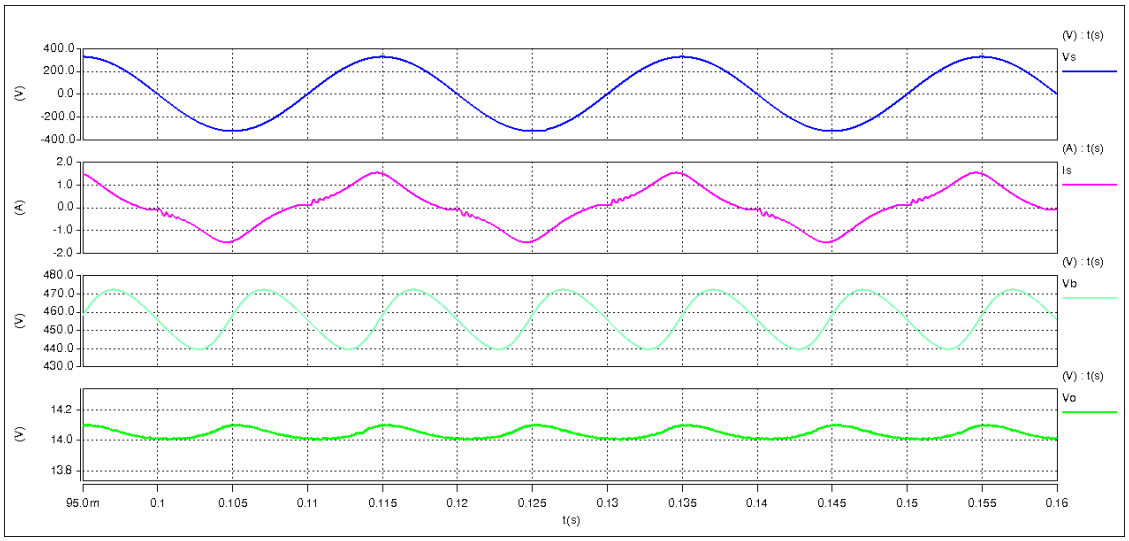


Figure 2-26 SABER simulated waveforms of V_s, I_s, V_B, and V_o at P_o=180 W

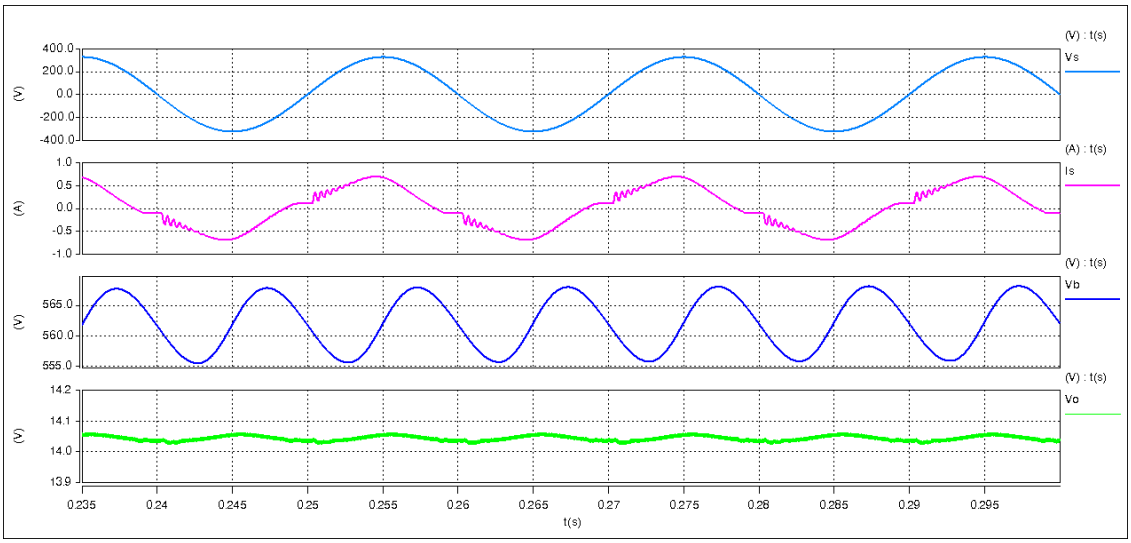


Figure 2-27 SABER simulated waveforms of V_s, I_s, V_B, and V_o at P_o=90 W

Figure 2-27 shows plots of V_s, I_s, V_B and V_o over a number of line cycles with a power output of 90 W. With a reduced load of 50 % of the nominal, the boost stage output voltage, V_B, increases as expected with DCM operation, but the voltage ripple decreases from 30 V to 12 V. The output voltage ripple, $\tilde{V}_o$, also reduces in amplitude to 38 mV.

Table 2-13 lists a comparison of calculated results in section 2.2.3 and simulated results of the S^4PFC. As expected it shows a close correlation between the two and reinforces

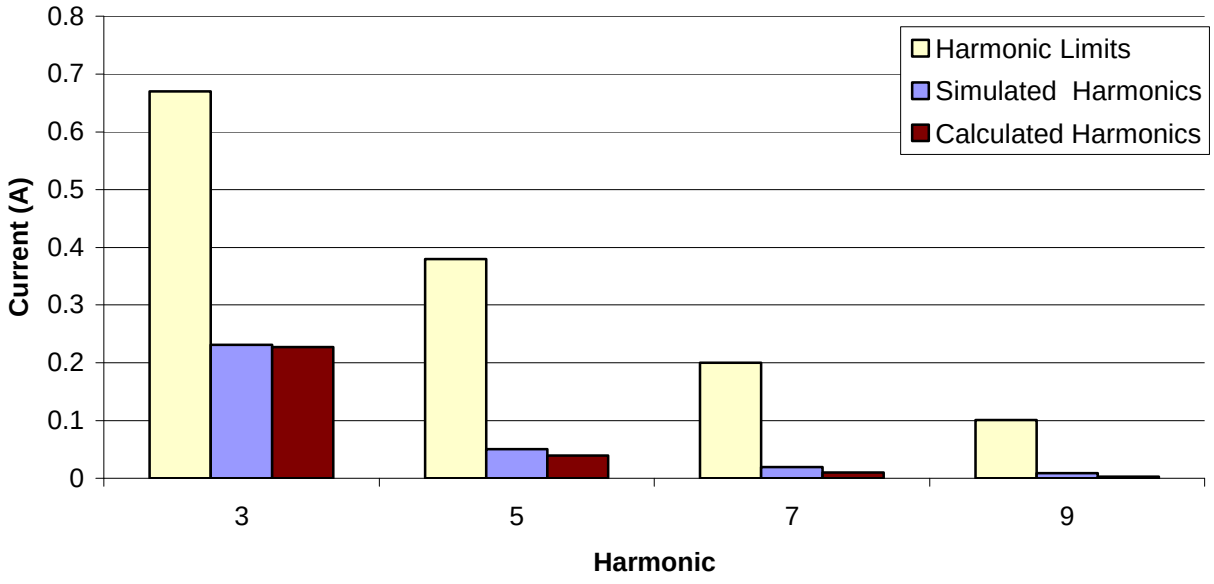
the validity of the calculations. Any disparities are due to simulation sampling rates, algorithms employed by the simulator and approximations in the analysis.

Table 2-13 Comparison of key calculated and simulated results

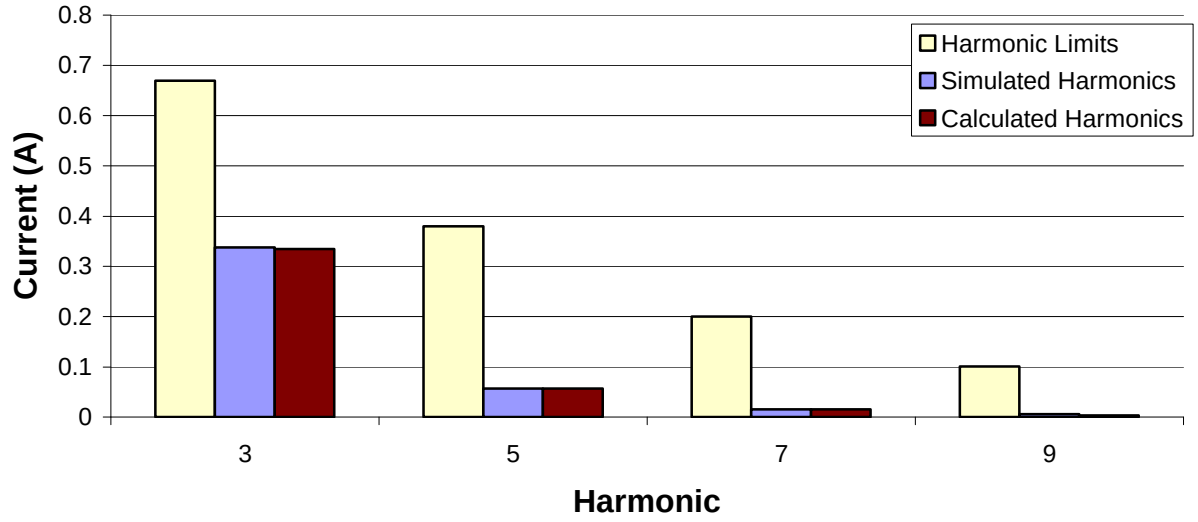
Parameter	P_{out}= 180 W		P_{out}= 90 W		Unit
	Calculated	Simulated	Calculated	Simulated	
V_s	230	230	230	230	V_{rms}
$\hat{I}_s$	1.37	1.49	0.59	0.69	A
f_{line}	50	50	50	50	Hz
f_{sw}	100	100	100	100	kHz
D	0.16	0.17	0.13	0.14	-
$\hat{I}_{L_B}$	4.8	5.1	3.8	4.1	A
$\hat{V}_Q$	563	566	663	669	V
$\hat{I}_Q$	7.9	8.1	5.7	5.9	A
V_B	460	458	566	569	V
$\hat{V}_{L_p}$	460	457	566	560	V
$\hat{I}_{L_p}$	3.15	3.07	1.92	1.80	A
V_o	14	14.04	14	14.04	V

Figure 2-28 shows simulated and calculated input current harmonics and compares them with respect to the allowable harmonic limits at an operating power of 180 W. The calculated results are accurate for the dominant harmonics, namely the 3rd, 5th and 7th, with noticeable errors for the low line conditions. The even harmonics are too small to be considered and are deemed negligible.

As expected the worst case input current harmonics occur at low line due to the higher peak currents generated by the DCM boost inductor. These results verify Figure 2-14 that a $\hat{V}_s / V_B$ ratio of 0.7 would limit input harmonic currents sufficiently to satisfy allowable limits.



(a)



(b)

Figure 2-28 Simulated and calculated input current harmonics (a) V_s = 265 V_{rms} and (b) V_s = 216 V_{rms}

Figure 2-29 plots the flux in each of the legs of the SABER simulated integrated magnetic seen in Figure 2-23. Due to the winding arrangement of the split boost inductor, N_B, and the transformer windings, N_p, N_s, N_r, there is an increased flux level in the right leg of the core, C_R, compared to the left core leg, C_L, which will result in added core losses in this leg.

This effect can be overcome by increasing the number of turns of $N_{L_{B1}}$ and reducing $N_{L_{B2}}$ but this will destroy the core symmetry.

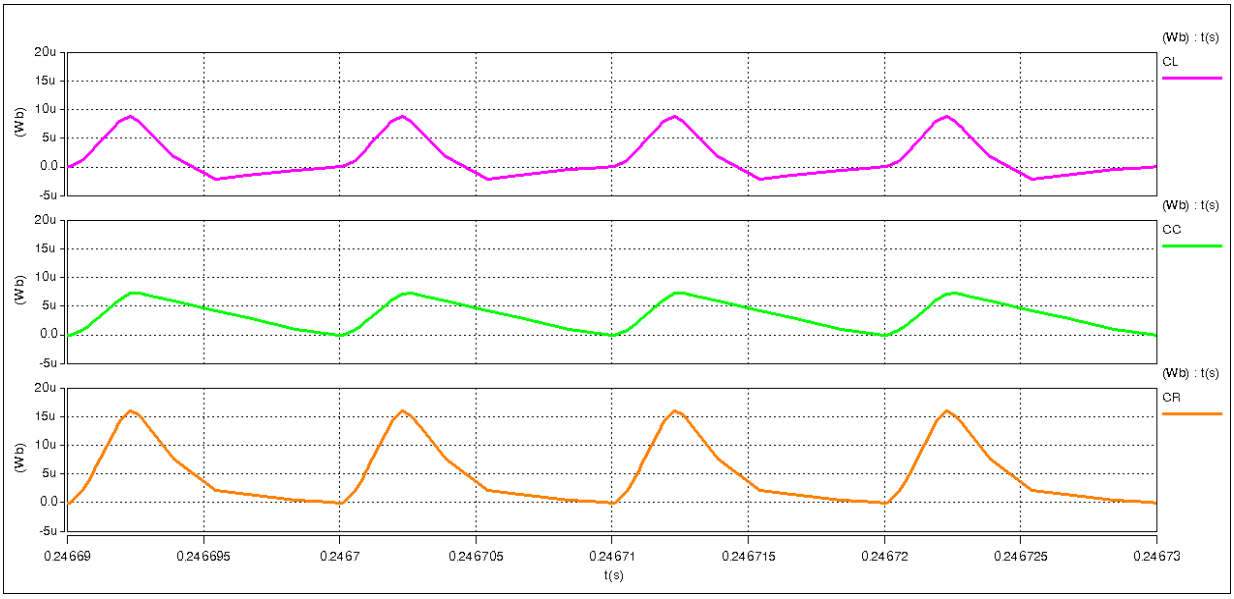


Figure 2-29 SABER simulation of integrated magnetic flux waveforms

2.5 Summary

This chapter presents a theoretical study, analysis and design of a single-stage, single-switch power factor corrector, S^4PFC, with an integrated magnetic component.

The steady-state analysis of the S^4PFC with an integrated magnetic component goes beyond any current work presented for this topology. Modes of converter operation are detailed and expected waveforms drawn. Design equations such as for $\hat{V}_s / V_B$ ratio to determine the dominant input current harmonics, and the maximum duty cycle are realised, with an understanding of the design trade offs such as cost, complexity and performance. Integrated magnetic analysis, design calculations/ process and winding approaches are realised that enable the amalgamation of two magnetic components onto a single core yet avoid electrical interaction.

MATLAB and SABER simulations verify the predicted steady-state performance of the S^4PFC as well as characterising the IM component. These results allowed for optimisation

of the power stage and provided results for the most suitable components to be selected for a prototype S^4PFC.

Part of this work formed a conference paper and poster presentation at the IEEE Power Electronics and Drives Systems Conference, November 2005, in Malaysia.

3 Single-Stage Single-Switch PFC Converter Dynamic Behaviour and Control Design

3.1 Introduction

This chapter details the dynamic behaviour of the S^4PFC with an IM and its control requirements. Small-signal models of the S^4PFC converter are realised and the requirements of a control loop discussed. A suitable control approach is identified from Chapter 1, along with an analysis of the characteristics of the controller. Using MATLAB Control Toolbox, the line-to-output, control-to-output and compensator transfer functions are realised and modelled. Design of the compensator is performed and a practical control approach that provides galvanic isolation is designed and modelled. A mixed-signal switching SABER model of the power stage and control loop is conducted that validates the predicted operation, stability and performance of the loop.

3.2 Line-to-Output

The S^4PFC converter analysed in Chapter 2 is a cascaded boost converter operating in DCM and a forward converter operating in CCM, Figure 3-1. Neglecting the input EMC filter, the line-to-output transfer function for a DCM boost converter [126] is shown in **Eqn 3-1**.

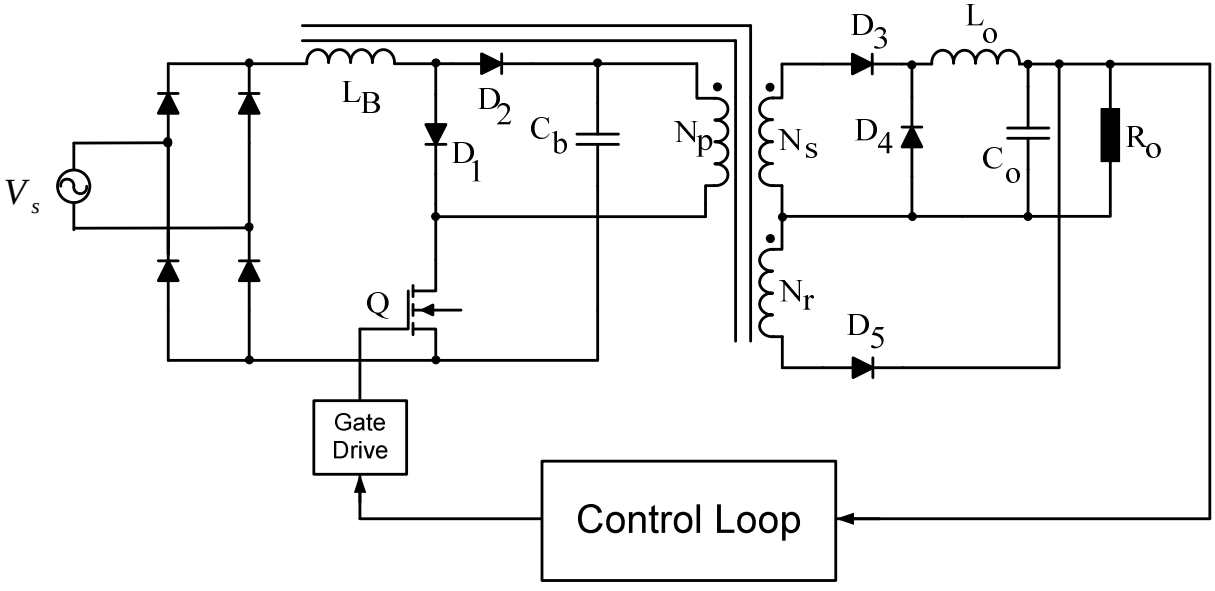


Figure 3-1 Single-stage single switch power factor corrector with simple control block

$$G_{v_s}(s) = \frac{\hat{v}_B}{\hat{v}_s}\bigg|_{\hat{d}=0} = \frac{G_B}{1+\dfrac{s}{\omega_p}} \qquad \textbf{Eqn 3-1}$$

where the ^ symbol over a lower case variable denotes a small perturbation around the steady-state operating point and

$$G_B = M = \frac{\hat{V}_s}{V_B} \qquad \textbf{Eqn 3-2}$$

and

$$\omega_p = \frac{2-M}{(1-M)R_B C_B} = 2\pi f_p \qquad \textbf{Eqn 3-3}$$

where R_B is the effective boost stage load resistance defined by $R_B = V_B^2 / P_o$ and C_B is the boost stage capacitance. The line-to-output transfer function of **Eqn 3-1** exhibits a single pole at ω_p.

Assuming the turns ratio of the forward converter $N_{p,s}$ = 1:1, the line-to-output transfer function for a CCM forward converter from [126] is

$$G_{v_B}(s) = \frac{\hat{v}_o}{\hat{v}_B}\bigg|_{\hat{d}=0} D\frac{1}{\left(1+\dfrac{s}{(Q_0\omega_0)}+\dfrac{s^2}{\omega_0^{\,2}}\right)} \qquad \textbf{Eqn 3-4}$$

where D is the duty ratio, $\omega_o = \dfrac{1}{\sqrt{L_o C_o}}$ and Q_o is defined by

$$Q_0 = \frac{\sqrt{L_o C_o}}{L_o/R_o + R_{esr}C_o} \qquad \textbf{Eqn 3-5}$$

where L_o is the forward converter output filter inductor, C_o is the output capacitance, R_o is the output load resistance and R_{esr} is the Equivalent Series Resistance, ESR, of C_o. The line-to-output transfer function of **Eqn 3-4** exhibits a double pole at ω_o and a resonant peak of Q_o.

Therefore the total line-to-output transfer function of the single-stage, single-switch power factor corrector is realised by **Eqn 3-6**

$$G_v(s) = G_{v_s} G_{v_B}(s) \qquad \textbf{Eqn 3-6}$$

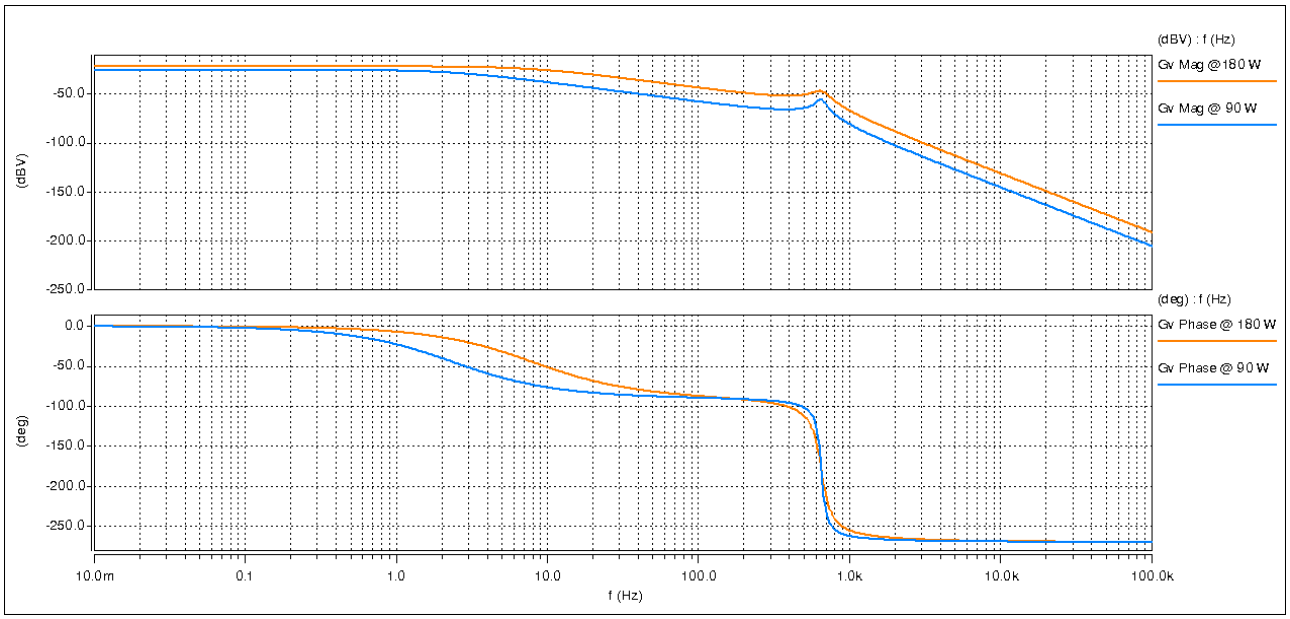


Figure 3-2 Magnitude and Phase plot of $G_v(s)$ at V_s = 230 V and P_o = 90 W and 180 W

Using the MATLAB Control Toolbox, Figure 3-2 is a plot of **Eqn 3-6** with the S^4PFC converter component values listed in Table 2-2 at V_s = 230 V and an output power of 90 W and 180 W. At P_o = 90 W the magnitude plot shows the low frequency pole of the discontinuous boost converter, f_p at 2.3 Hz, the -20 dB/dec slope above 2.3 Hz and the associated -90˚ phase shift. The high frequency complex pole, f_o, due to the continuous forward converter stage is at 650 Hz, and an additional – 180 ˚ phase shift is added to the response. Above 650 Hz the magnitude plot shows a role off -60 dB/dec slope.

At P_o = 180 W, the high frequency complex pole, f_o, does not change, apart from an increase in gain magnitude. However the low frequency pole of the discontinuous boost converter, f_p, increases to 8 Hz.

3.3 Control-to-Output

The control-to-output transfer function of the S^{4}PFC converter is that of a conventional CCM forward converter shown in **Eqn 3-7** [126].

$$G_{vd}(s) = \frac{V_B}{N} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{(Q_0\omega_0)} + \frac{s^2}{\omega_0^2}\right)} \qquad \textbf{Eqn 3-7}$$

where $\omega_o = 1/\sqrt{L_o C_o}$ and $\omega_z = 1/C_o R_{esr}$. Inserting the S^{4}PFC component parameters from Table 2-2 into **Eqn 3-7** , Figure 3-3 shows a plot of the control-to-output of the S^{4}PFC using MATLAB, traced in orange at V_s = 230 V and a maximum power output of 180 W. The resonant pole, f_o is at 650 Hz with a –40 dB/dec magnitude roll-off above this frequency. The high frequency zero, f_z, due to the parastic ESR of C_o is at 650 kHz. Reducing P_o to 90 W, does not change the frequency position of f_o or f_z, only increasing the resonant peak Q_o.

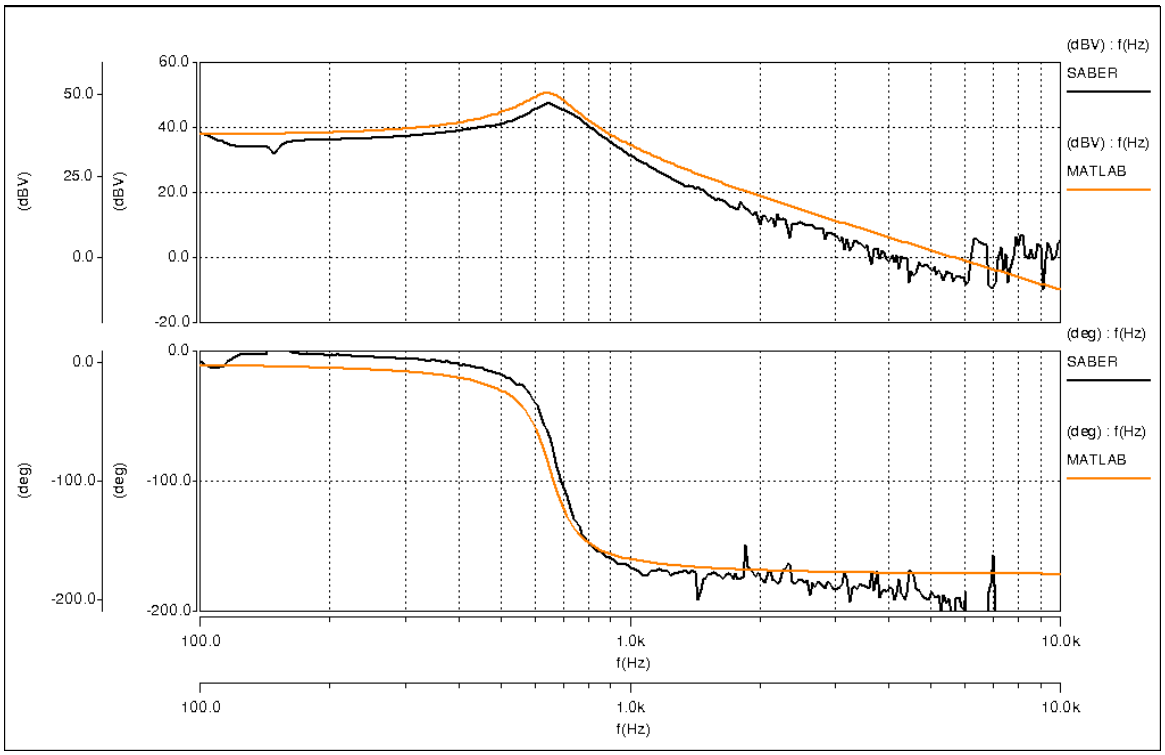


Figure 3-3 SABER and MATLAB plots of control-to-output of the S^{4}PFC

Figure 3-3 clearly shows that the small-signal behaviour of the DCM boost stage of the S^{4}PFC has no impact upon the performance of the control-to-ouput of the converter

Using the SABER simulation model shown in Figure 3-4, the results of a time domain system analyser, TDSA, is plotted on the same axis as the MATLAB simulation results in Figure 3-3. The two plots show a close correlation between the simulation approaches, any disparities that are seen is due to the sampling rate of the SABER simulation approach. The parameters for the TDSA are listed in Table 3-1. By increasing max_nper and increasing the quality factor of the input band pass filter the accuracy of the SABER plot can be improved at the expense of computational time and memory. The simulation time required to provide the results for Figure 3-3, took an average of 4 hours and 6 GB of memory.

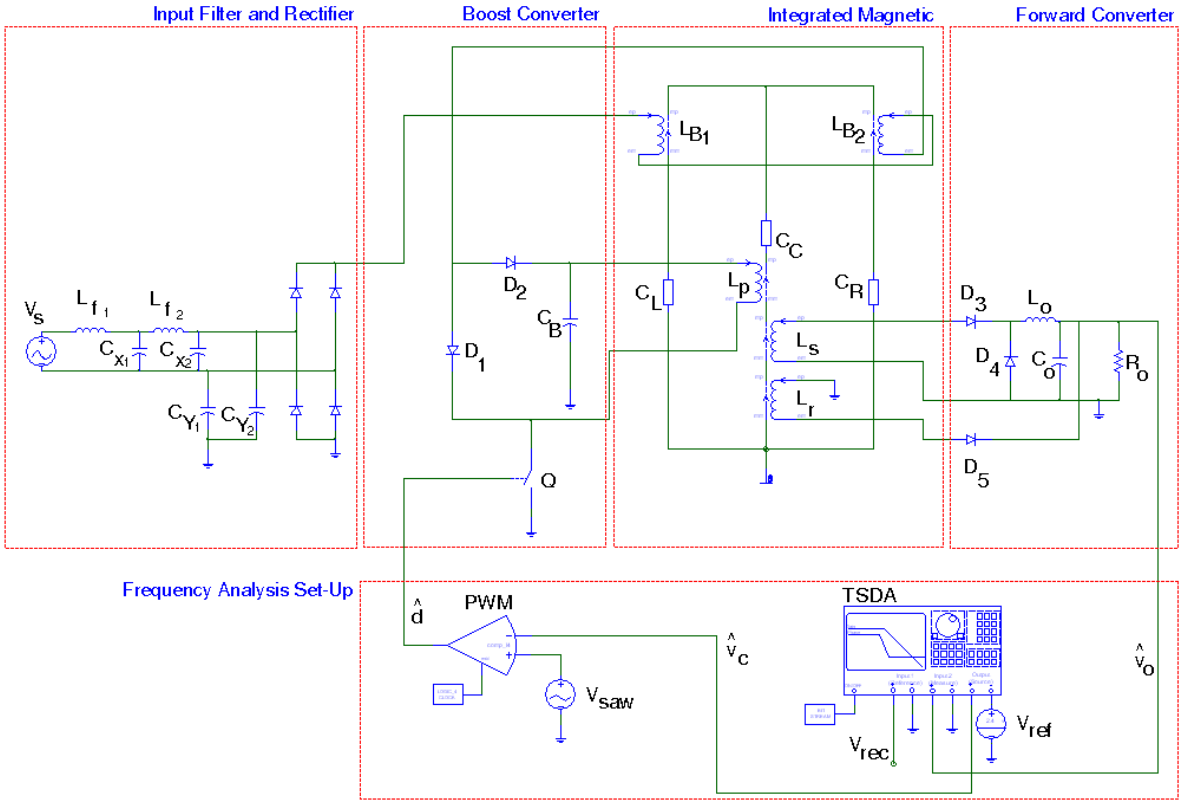


Figure 3-4 SABER simulator arrangement to determine S^{4}PFC $G_{vd}(s)$

Table 3-1 Control parameters for the TDSA component in SABER simulations

Name	Value
fbegin	50
fend	100000
ampl	0.1
Offset	0
npoints	100
Mode	logswp
Max_err	0.01
Max_nper	30
Min_nper	3
Min_tspp	40
a_o	1
q_o	10
Filter	Yes
ac	mag = 1, phase = 0

3.4 Identification of Suitable Control Approach the S^{4}PFC

This section identifies a suitable control approach from section 1.2.5 which reviews power factor correction control methods for CCM and DCM converters.

As the boost stage of the S^{4}PFC operates in discontinuous current mode, the control loop is not required to perform power factor correction, only output voltage regulation. Therefore, commonly implemented current mode approaches such as average and peak control, are not necessary unless a current or power limiting function is required. The simplest approach is a single-loop voltage-mode control, Figure 3-5, where $G_c(s)$, $G_{pwm}(s)$, $G_{vd}(s)$, and $G_{K_d}(s)$ are the transfer functions of the compensator, the PWM modulator, the S^{4}PFC control-to-output and the feedback attenuator respectively.

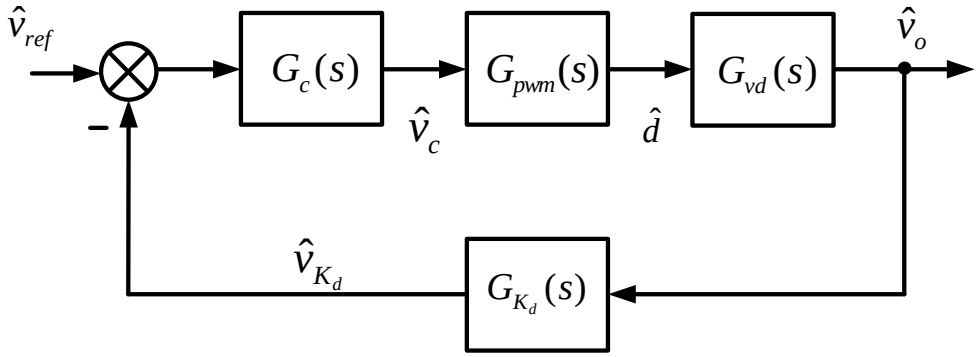


Figure 3-5 Single loop voltage mode control

The closed loop equation of the single-input, single-output control loop in Figure 3-5 is expressed as

$$H(s) = \frac{G_{vd}G_c}{1+G_{vd}G_cK_d} \qquad \textbf{Eqn 3-8}$$

Closed loop stability of a linear system is achieved if all the roots of its characteristic equation, $1+G_{vd}G_cK_d = 0$, has negative real parts [132], that is, the roots are to the left of the imaginary axis in Figure 3-6. To achieve closed loop stability and a fast transient response, a suitable control compensator G_c is required.

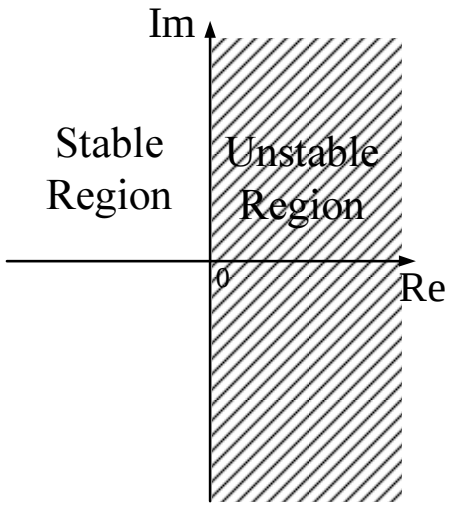


Figure 3-6 Stability regions in the complex plane for roots of the characteristic equation

The control-to-output transfer function, G_{vd}, plotted in Figure 3-3, shows the gain magnitude exhibiting a second-order response at f_p and a phase shift tending towards -180˚. To ensure system stability and fast transient response, a PID control, **Eqn 3-9**, is required to perform loop compensation [126]. This control approach can obtain both a wide frequency bandwidth and a zero steady-state error.

$$G_c(s) = \frac{\omega_g \left(1+\frac{s}{\omega_{z_1}}\right)\left(1+\frac{s}{\omega_{z_2}}\right)}{s\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \qquad \textbf{Eqn 3-9}$$

The compensator $G_c(s)$ exhibits the following characteristics, the zero at ω_{z_1} adds low frequency gain. The second zero at ω_{z_2} adds phase lead at the vicinity of the loop gain crossover frequency, f_c. Combined, ω_{z_1} and ω_{z_2} can provide a phase boost upto 180˚. The poles at ω_{p_1} and ω_{p_2} provide high frequency roll off to attenuate the high frequency switching ripple interfering with the pulse width modulator. Finally, ω_g is the gain of the compensator at f_c. Figure 3-7 shows the S^{4}PFC with a simplified block diagram of the voltage mode feedback loop.

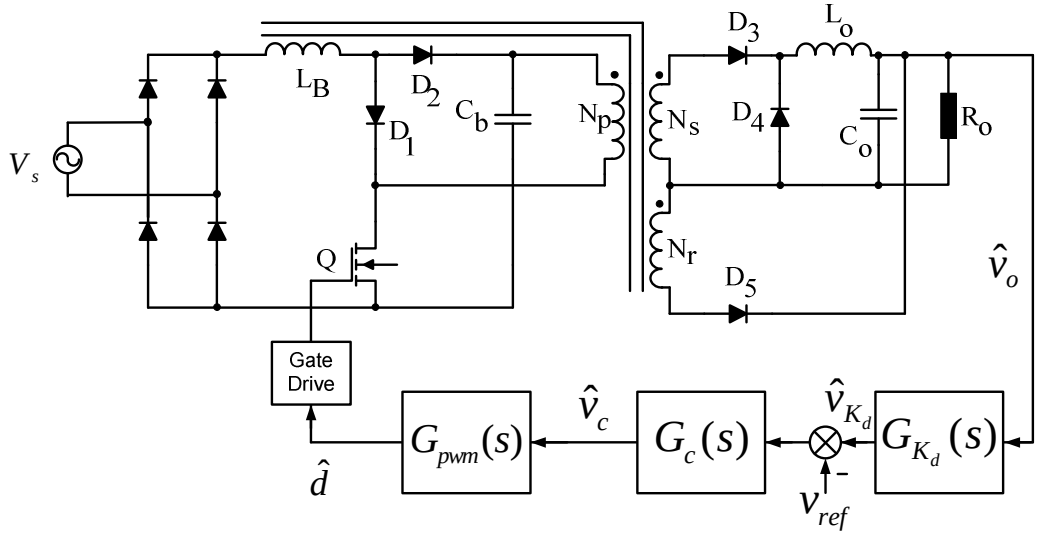


Figure 3-7 S^{4}PFC with a block diagram of the proposed voltage mode control loop

To ensure that galvanic isolation is maintained, an isolation stage is required in the feedback loop. A common approach is detailed in [133] and shown in Figure 3-8, this circuit consists of the feedback attenuator network, K_d, an error amplifier, $G_{ea}(s)$, an optocoupler, $G_{oc}(s)$ and a PWM modulator with gate drive, $G_{pwm}(s)$.

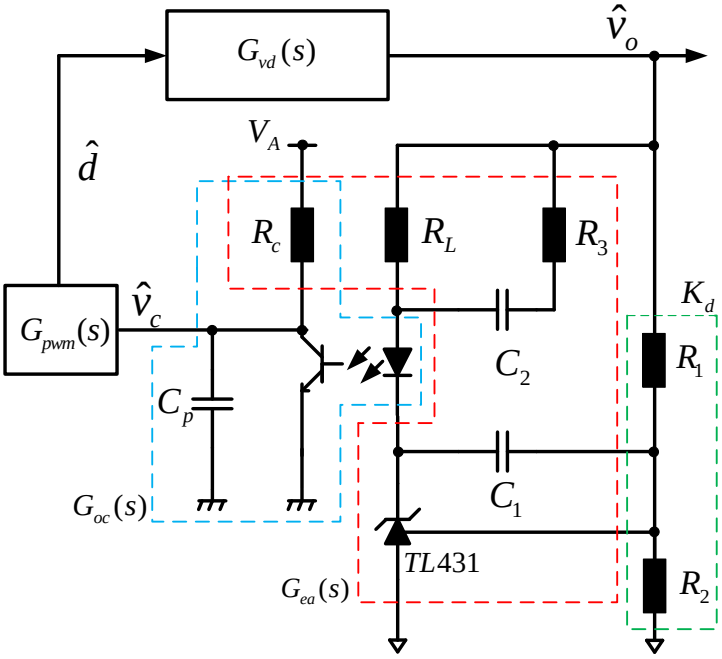


Figure 3-8 Practical implementation of isolated feed back and compensation

The attenuation resistor network, K_d, comprising the resistor network R_1 and R_2, reduces V_o to 2.5 V which is the internal precision voltage reference of the TL431 [134]. The TL431 comprises of a stable internal 2.5 V reference which is connected to an internal operational amplifier inverting input. The operation amplifier output drives an internal open collector transistor. In this approach, the TL431 is used as the error amplifier of the compensator and eliminates the need for an auxiliary power supply for the error amplifier network. The output of the TL431 is powered through the resistor R_L and the optocoupler signal diode, connected in series with the output voltage, V_o. The TL431 error amplifier now operates as a transconductance amplifier, therefore $G_c(s)$ comprises $G_{ea}(s)$ and $G_{oc}(s)$. By generating the compensation error signal, v_c, on the primary side, as opposed to transferring a proportional signal of the output voltage to the primary side, the impact of the optocoupler's

non-linearity and high gain variation is minimised. The optocoupler error signal, v_c, is compared with a set/reset latch in block, $G_{pwm}(s)$, where duty cycle, D, is generated.

For the practical control approach in Figure 3-8, the subsequent position of the zeros and poles of **Eqn 3-9** are determined by **Eqn 3-10** to **Eqn 3-14** [135].

$$\omega_{z_1} = \frac{1}{R_c C_1} \qquad \textbf{Eqn 3-10}$$

The second zero position ω_{z_2} is realised by

$$\omega_{z_2} = \frac{1}{(R_L + R_3)C_2} \qquad \textbf{Eqn 3-11}$$

The first pole position ω_{p_1} is expressed by

$$\omega_{p_1} = \frac{1}{R_3 C_2} \qquad \textbf{Eqn 3-12}$$

The second pole position ω_{p_2} is expressed by

$$\omega_{p_2} = \frac{1}{R_c C_c} \qquad \textbf{Eqn 3-13}$$

Finally ω_g is realised by

$$\omega_g = \frac{R_c}{R_L} CTR \qquad \textbf{Eqn 3-14}$$

where CTR is the current transfer ratio of the opto-coupler.

3.5 Design of Control Loop

To achieve a fast transient response whilst maintaining loop stability, the overall open loop gain, $G_{ol}(s)$, should have a unity gain cross over frequency, f_c, approximately 1/5th below the switching frequency, f_{sw}, with a slope of -20 dB/dec and the corresponding phase

margin at the unity cross-over should be approximately 45˚- 70˚to ensure a satisfactory damping ratio. The overall open-loop transfer function, $G_{ol}(s)$, is expressed as

$$G_{ol}(s) = G_{vd}G_cG_{pwm}G_{K_d}(s) \quad \textbf{Eqn 3-15}$$

Figure 3-8 shows the practical implantation of the feedback attenuator, $G_{K_d}(s)$, comprising of resistors R_1 and R_2. To ensure that the TL431 reference input is sufficiently biased, the current through R_1, I_{R_1}, should be greater than I_{bias} over the entire temperature range [134]. The attenuator network is derived by **Eqn 3-16** and **Eqn 3-17.**

$$R_2 = \frac{V_{ref}}{I_{R_2}} \quad \textbf{Eqn 3-16}$$

where V_{ref} is the internal reference of the TL431, and $I_{R_2} = I_{R_1} - I_{bias}$.

$$R_1 = \frac{V_o - V_{ref}}{I_{R_1}} \quad \textbf{Eqn 3-17}$$

From **Eqn 3-16** and **Eqn 3-17** arbitrarily choosing I_{R_1} to be 1 mA, then R_1 = 11.5 $k\Omega$ and R_2 = 2.5 $k\Omega$, therefore $G_{K_d}(s)$ is 0.17.

To ensure a stable switching frequency, f_{sw}, a pulse width modulator and efficient MOSFET gate drive, a UC2842 control IC is used [136]. Figure 3-9 shows a block diagram of the UC2842, detailing its functionality.

The S^4PFC switching frequency is set by the UC2842 internal oscillator and by the addition external components R_T and C_T and is derived by **Eqn 3-18** [136].

$$f_{sw} = \frac{1.72}{R_TC_T} \quad \textbf{Eqn 3-18}$$

The MOSFET gate driver is realised by an internal totem pole arrangement. The PWM is determined by a set-reset latch, therefore $G_{pwm}(s)$ = 1. The control IC also provides a

regulated 5 V reference, V_A. As the loop compensator, $G_c(s)$, is defined by the approach shown in Figure 3-8, the UC2842 internal operational amplifier is redundant along with the internal voltage reference. The output voltage, v_c, of the compensator $G_c(s)$ is fed directly into Pin 1 of the UC2842.

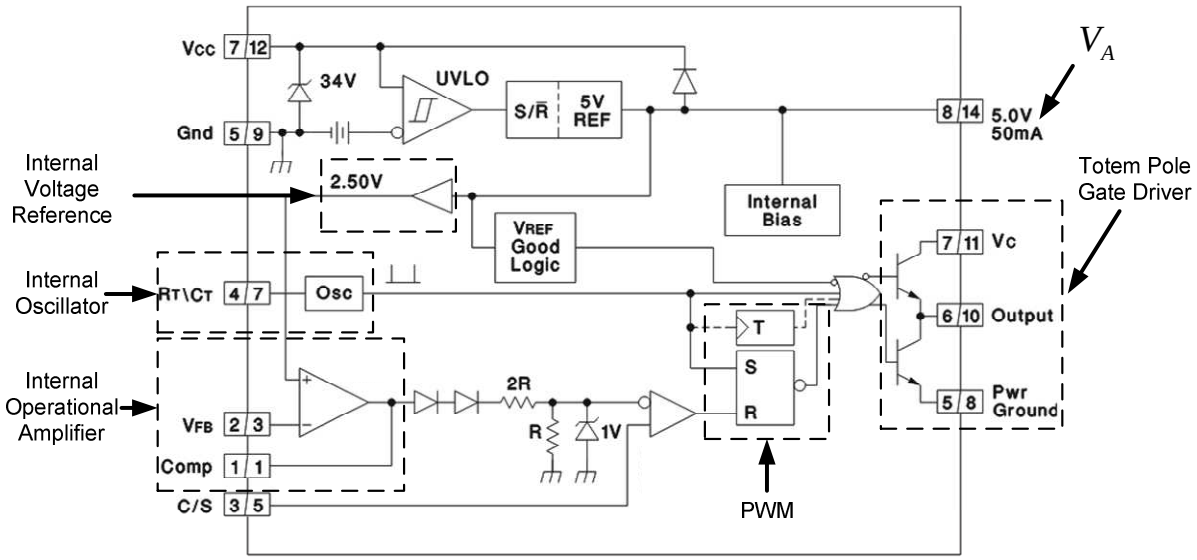


Figure 3-9 Block diagram of UC2842 control IC

Before the design of $G_c(s)$ can take place, the transfer function, $G_o(s)$ must be characterised and is expressed as

$$G_o(s) = G_{vd} G_{pwm} G_{K_d}(s) \qquad \textbf{Eqn 3-19}$$

Figure 3-10 shows a plot of **Eqn 3-19** and that at a required overall open loop transfer function, at the target frequency cross over, f_c, of 10 kHz, the gain magnitude is -25 dB with a phase shift, PS, of – 178˚. Therefore to achieve an overall open-loop transfer function, $G_{ol}(s)$, of unity gain crossover at f_c and a phase margin, PM, of 65˚, the compensator, $G_c(s)$, must provide a gain at f_c of 25 dB and a phase boost, PB, of 152˚.

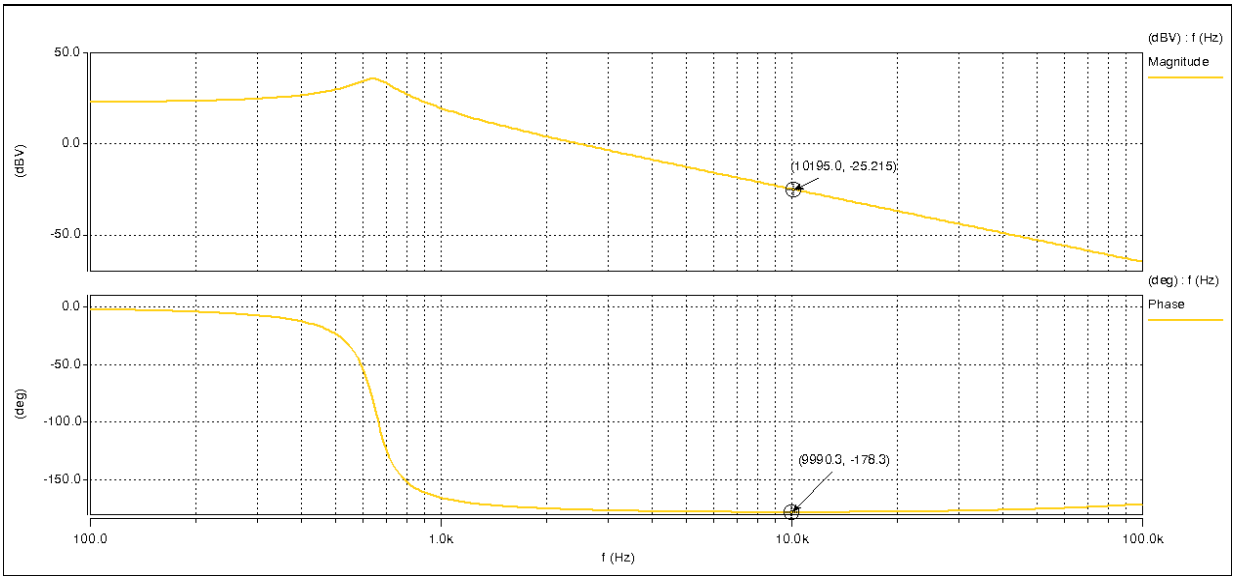


Figure 3-10 Plot of $G_o(s)$

The phase boost, PB delivered by $G_c(s)$ is defined as

$$PB = PM - PS - 90 \qquad \textbf{Eqn 3-20}$$

Placing the zeros, ω_{z_1} and ω_{z_2} of **Eqn 3-9** at 3455 rads^{-1}, and ω_{p_1} and ω_{p_2} at 3.5x10^6 rads^{-1}, to attenuate any high frequency switching noise, results in the compensator $G_c(s)$ plot in Figure 3-11. At the target f_c, 10 kHz, the gain magnitude is 25 dB with a phase boost totalling 152°.

Using **Eqn 3-10** to **Eqn 3-14**, the practical component values of Figure 3-8 to achieve the $G_c(s)$ plot in Figure 3-11, are R_1 = 11.5 $k\Omega$ and R_2 = 2.5 $k\Omega$, R_3 =54 Ω, R_L =5.6 $k\Omega$, R_p = 20 $k\Omega$, C_1 =25 nF, C_2 = 50 nF and C_p = 145 pF.

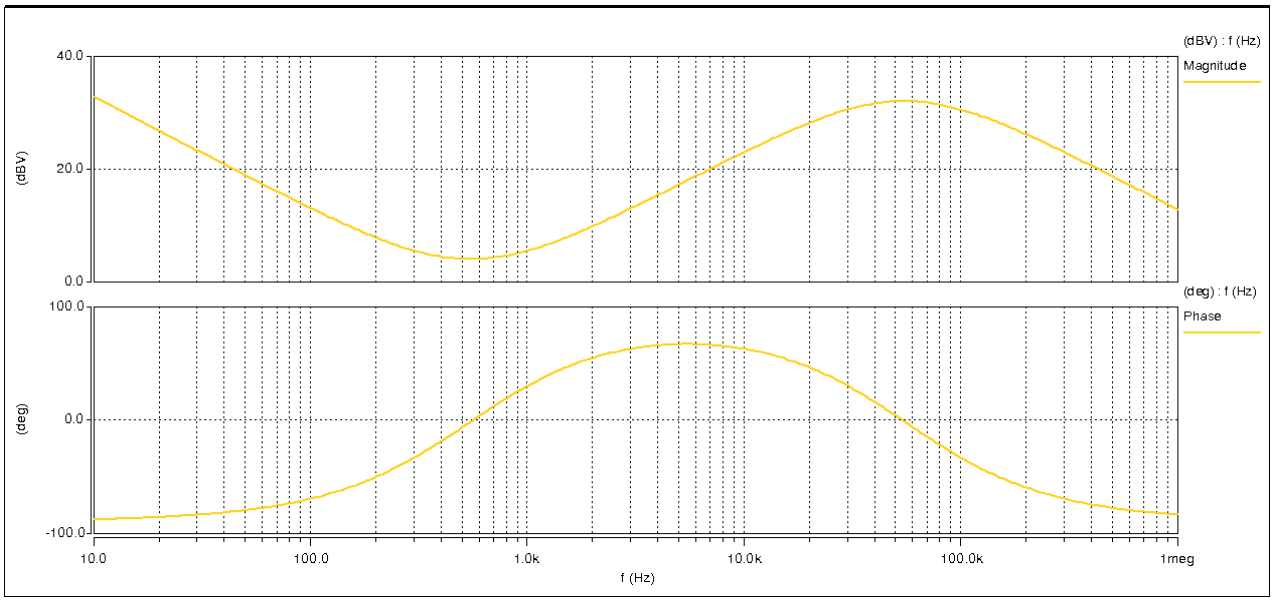


Figure 3-11 MATLAB plot of $G_c(s)$

The resulting open-loop gain $G_{ol}(s)$ is plotted in Figure 3-12. It can be seen that there is a unity gain cross over at 1/5th of the f_{sw} with a –20 dB slope. The phase margin at f_c is 65˚ as expected.

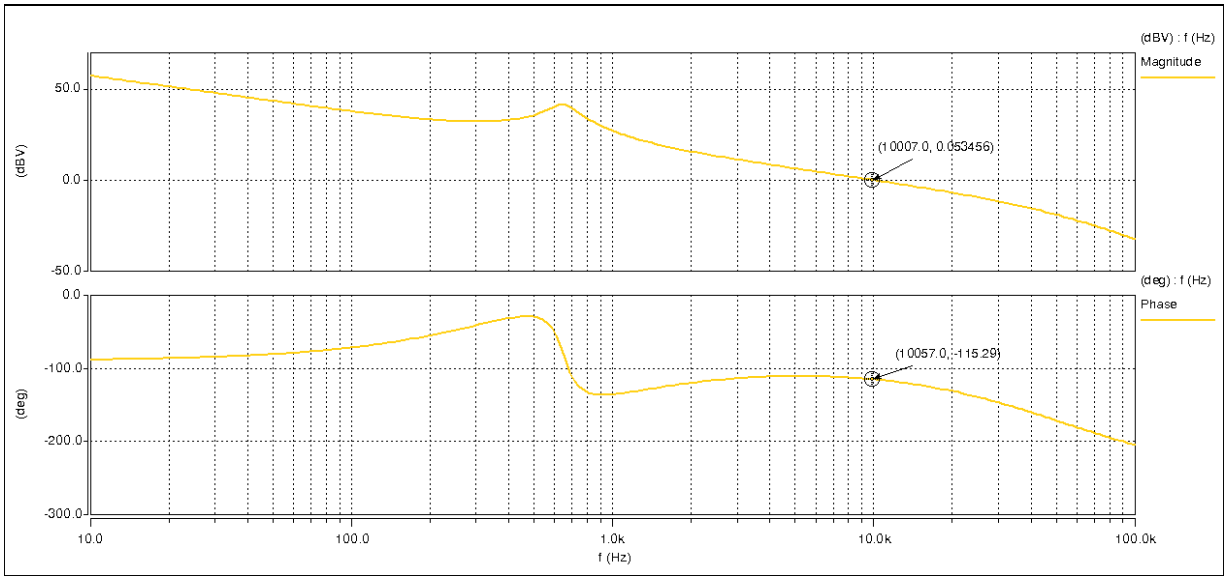


Figure 3-12 MATLAB plot of $G_{ol}(s)$

Figure 3-13 shows a normalised step response of the transfer function H(s) in **Eqn 3-8** It confirms that the loop is stable with a response typical of a system with a phase margin of 65°, settling within 2 ms of the disturbance.

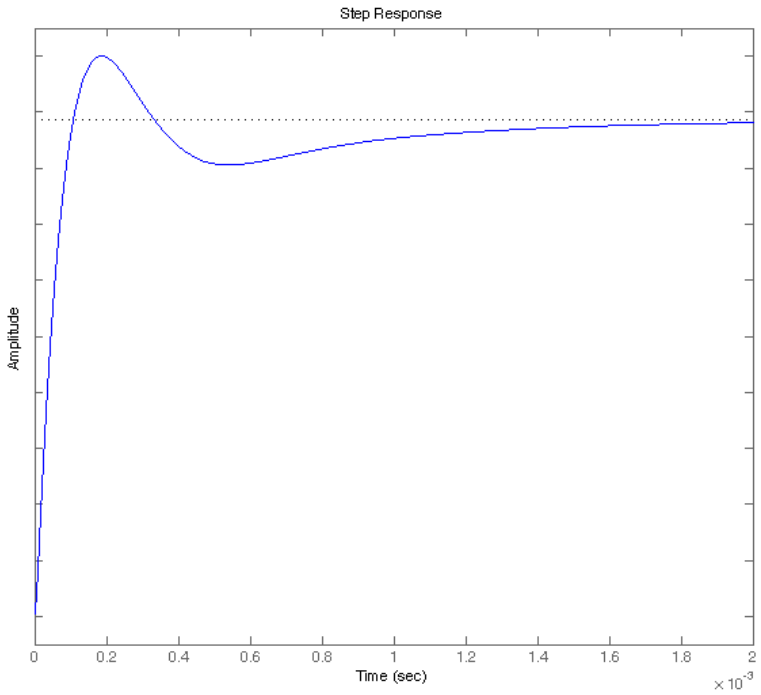


Figure 3-13 A normalised step response of closed loop system H(s)

3.6 SABER and MATLAB Simulation Verification

The results of the MATLAB control analysis in section 3.5 are verified with SABER mixed signal switching simulations. Figure 3-14 shows the SABER model of the control system $K_d(s)$, v_{ref}, $G_c(s)$, and $G_{pwm}(s)$. The control loop is simulated along side the S^4PFC SABER switching model in Figure 2-23.

The following SABER simulations demonstrate the dynamic performance of the S^4PFC converter and the proposed control approach. The results presented are all for a nominal input voltage V_s = 230 V_{rms} with the output power, P_{out}, stepping from 180 W to 90 W back to 180 W.

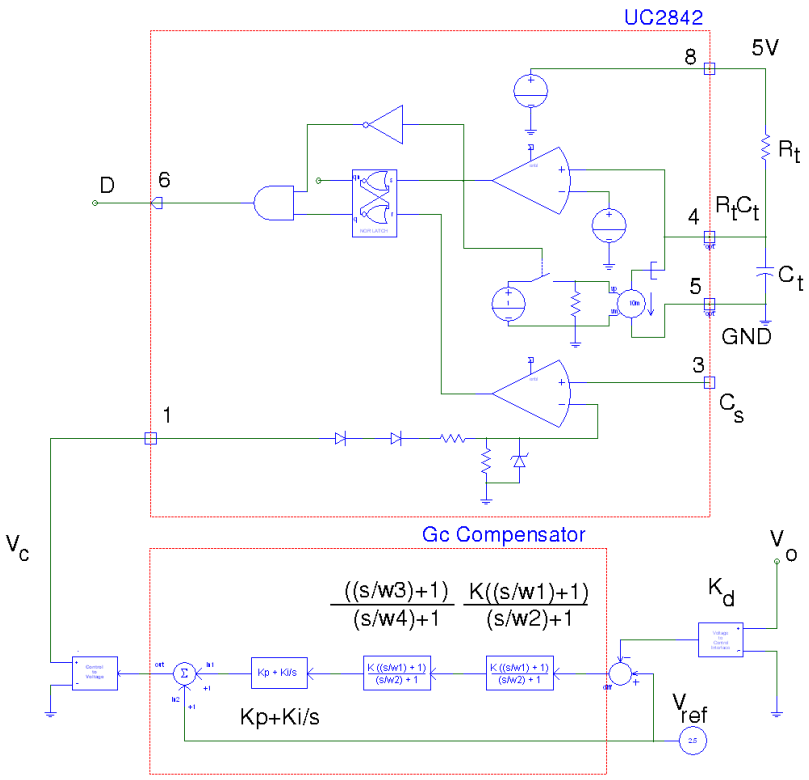


Figure 3-14 SABER simulation schematic of control loop for S[4]PFC converter

Figure 3-15 shows the response of the S[4]PFC with a step load change of 180 W to 90 W, where V_s, I_s, V_B and V_o are plotted. At time 0.14 s to 0.2 s the output power is 180 W, the input current, I_s, is in phase with the input voltage, V_s, indicating a high power factor. I_s is not purely sinusoidal, as it is distorted by the non-linear performance of the DCM boost converter. At time 0.2 s, a step load change occurs from 180 W to 90 W. The input current, I_s, remains in phase with V_s but reduces in amplitude, whilst the control loop of Figure 3-14, maintains the regulation of V_o. As V_B is not regulated there is an increase in this voltage from 460 V to 560 V. The amplitude of the ripple content of V_o also reduces with the reduced load.

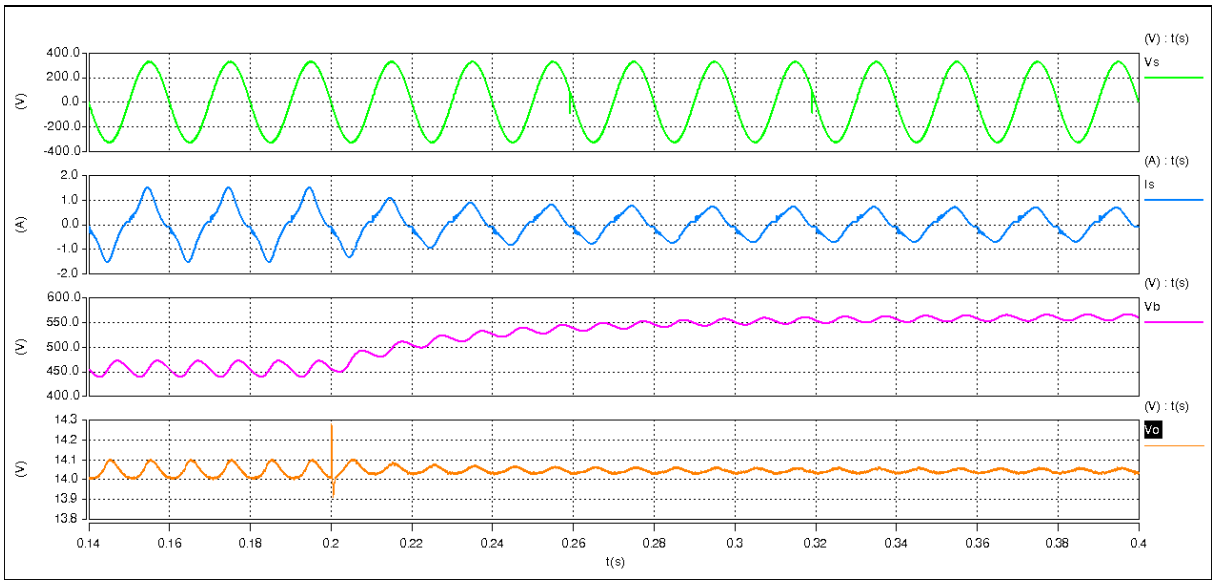


Figure 3-15 SABER simulation of V_s, I_s, V_B, and V_o in response to a step load change of 180 W - 90 W at t = 0.2 s

Figure 3-16 is a magnified image of Figure 3-15 now plotting V_o and I_o. At time 0.1992 s to 0.2 s the load is 180 W, the output voltage is closely regulated to 14 V and the output current is 12.8 A. At time 0.2 s, a step down in load to 90 W occurs. The output voltage responds by rising to 14.29 V at time 0.2001 s. The response of $G_c(s)$ overcompensates causing V_o to undershoot at 0.2005 s, however by time 0.201 s, V_o has settled to the steady-state value, exhibiting a classic second order response.

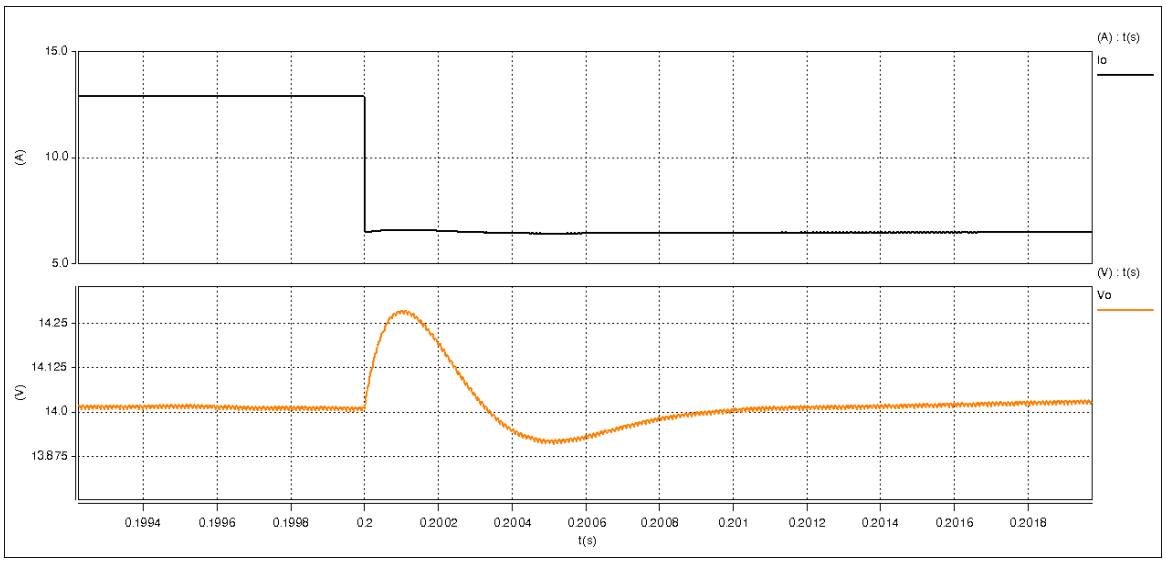


Figure 3-16 Magnified view of SABER simulation I_o and V_o response to step load of 180 W to 90W

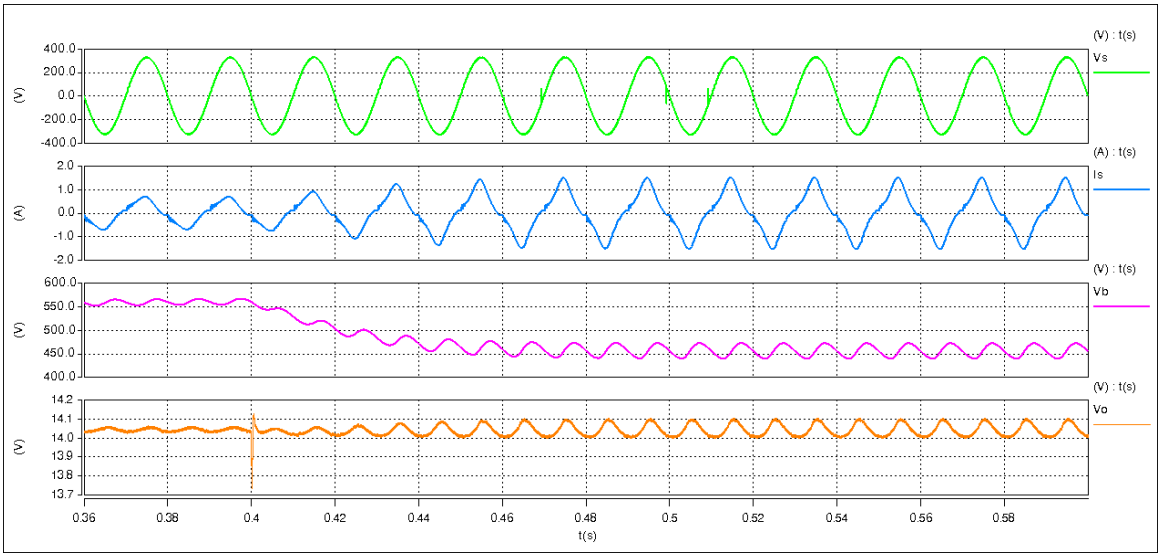


Figure 3-17 SABER simulation of V_s, I_s, V_B, and V_o in response to a step load of 90 W to 180 W at t = 0.4 s

Figure 3-17 shows the response of the S^{4}PFC to a step load change where V_s, I_s, V_B and V_o are plotted. At time 0.36 s to 0.4 s the output power is 90 W, the input current, I_s, is in phase with the input voltage, V_s, again indicating a high power factor. At time 0.4 s, a step load change occurs from 90 W to 180 W. The input current, I_s, remains in phase with V_s but increases in amplitude, whilst the control loop, Figure 3-14, maintains regulation of V_o. As V_B is not regulated there is a decrease in this voltage from 560 V to 460 V. The amplitude of the ripple in V_o also increases with the increased load.

Figure 3-18 is a magnified image of Figure 3-17 showing V_o and I_o. At time 0.3992 s to 0.4 s the load is 90 W, the output voltage is closely regulated to 14 V and the output current is 6.4 A. At time 0.4 s, the load steps to 180 W. The output voltage responds by dropping to 13.75 V at time 0.4001 s. The response of $G_c(s)$ overcompensates causing V_o to overshoot at 0.4005 s, however by time 0.4018 s, V_o has settled to the steady-state value.

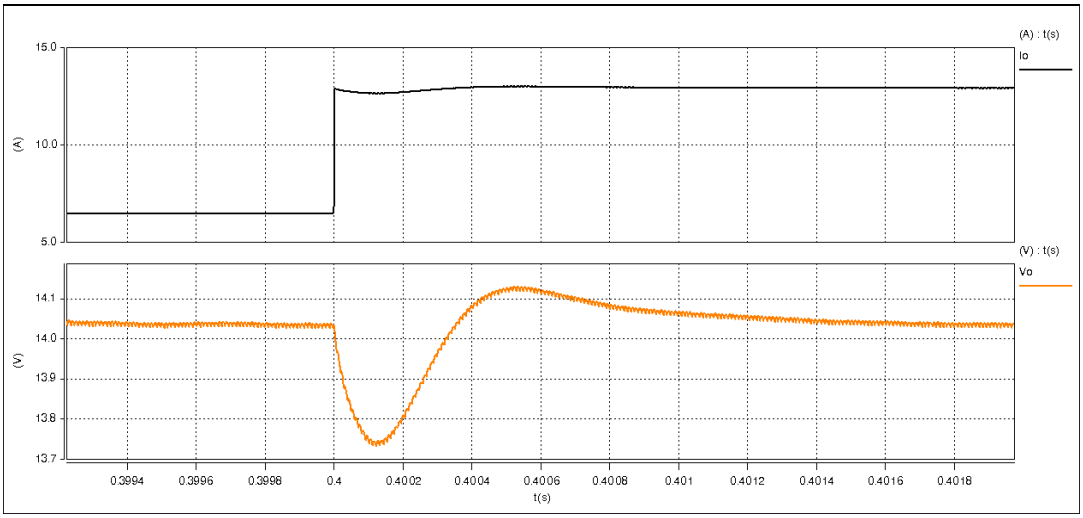


Figure 3-18 Magnified view of SABER simulation I_o and V_o response to step load 90 W to 180 W

From these simulations it can be seen that the simulated model of the power stage and its control loop are performing as expected. Neither step up or step down load changes appear to cause any sub harmonic instabilities.

3.7 Summary

This chapter details the dynamic performance and the requirements of the S^4PFC converter control loop. The dynamic analysis of the S^4PFC with an IM has not been found in any of the literature reviewed by the author. The converter line-to-output and control-to-output transfer functions, suitable control approaches are realised, as well as the necessary circuit protection measures to ensure there is no over voltage of the DCM boost stage capacitors under light load conditions.

A suitable control approach is identified from Chapter 1, and evaluated using MATLAB and SABER simulations, designed and implemented, ensuring a fast transient response to step load changes, whilst ensuring loop stability. A practical approach is developed that allows for fast dynamic response, but also provides the required galvanic isolation between the primary and secondary.

The MATLAB and SABER switching model simulations confirm the theoretical results increasing the confidence in the S^4PFC small-signal analysis and validate the identified control approach.

4 Experimental Performance of S^{4}PFC with IM

4.1 Introduction

Following the analysis and design of the S^{4}PFC with an IM device in Chapters 2 and 3, this Chapter details the development of the prototype converter. Firstly, the construction and layout approach used is shown along with the experimental laboratory set-up. Secondly, verification of the operation of the S^{4}PFC with an IM device is performed, comparing SABER simulations and experimental waveforms, validating the design. Finally, a cost analysis is discussed.

4.2 Circuit Construction and Experimental Setup

This section details the experimental laboratory setup, including the design and layout of the Printed Circuit Boards, PCBs, the equipment used for verifying the performance of the single-stage, single-switch power factor corrector. The PFC stage and the respective control components are arranged so that they occupy a small area to minimise parasitic inductance loops. The power stage and the control loop are closely arranged on a single board. The PCB is FR4 insulating fibre glass with a single sided 1oz copper layer. Full schematic drawings of the S^{4}PFC circuit diagram can be found in Appendix D.

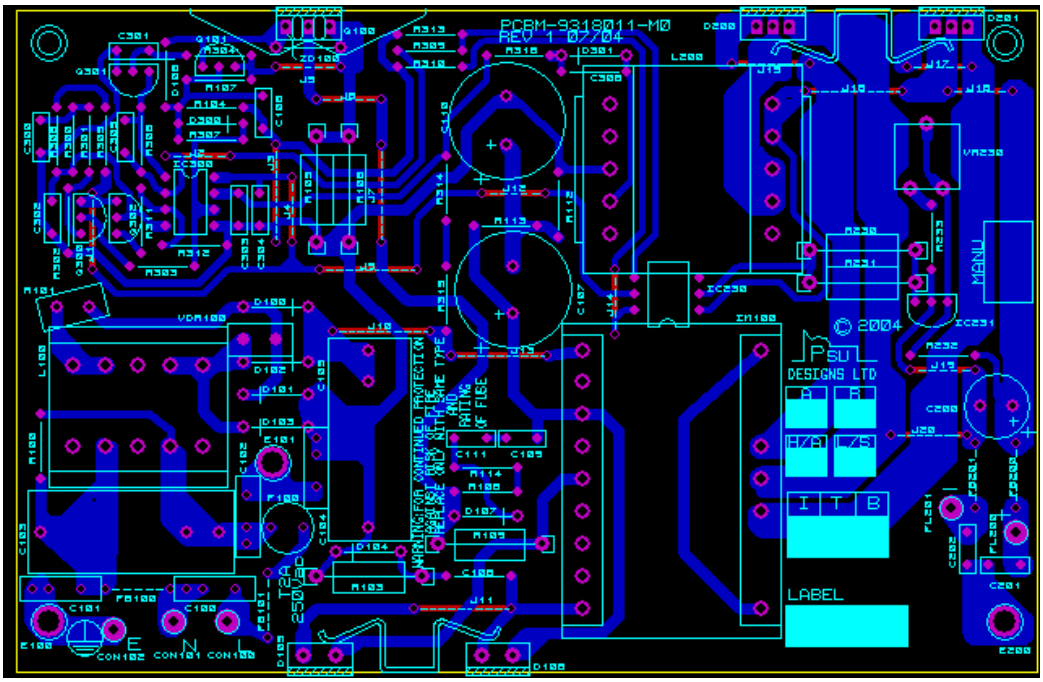


Figure 4-1 PCB capture of S^{4}PFC layout and tracking

Figure 4-1 shows the circuit layout for the S^{4}PFC converter. The input line connection, V_s, is on the bottom left hand side of the power board. This input is fused for safety and voltage surge suppression components are also added. Immediately following the fused input are the EMC components, X-capacitors C103, C104 and a common-mode inductor, L100. The network of components in the upper left corner of Figure 4-1 is the UC2842 PWM controller and supporting devices. The main switching power MOSFET, Q, is labelled Q100 in this diagram. The main boost capacitors are located in the centre of the board and are labelled C107 and C110. The integrated magnetic component is clearly seen as it is the largest single device on the PCB and is labelled IM100. L200 is the output filter inductor of the forward converter stage. Use of space was minimised to ensure compactness and efficiency. There are also numerous test points situated across the circuit board for ease of testing. The dimensions of the converter in Figure 4-2 is 250 mm x 150 mm x 100 mm.

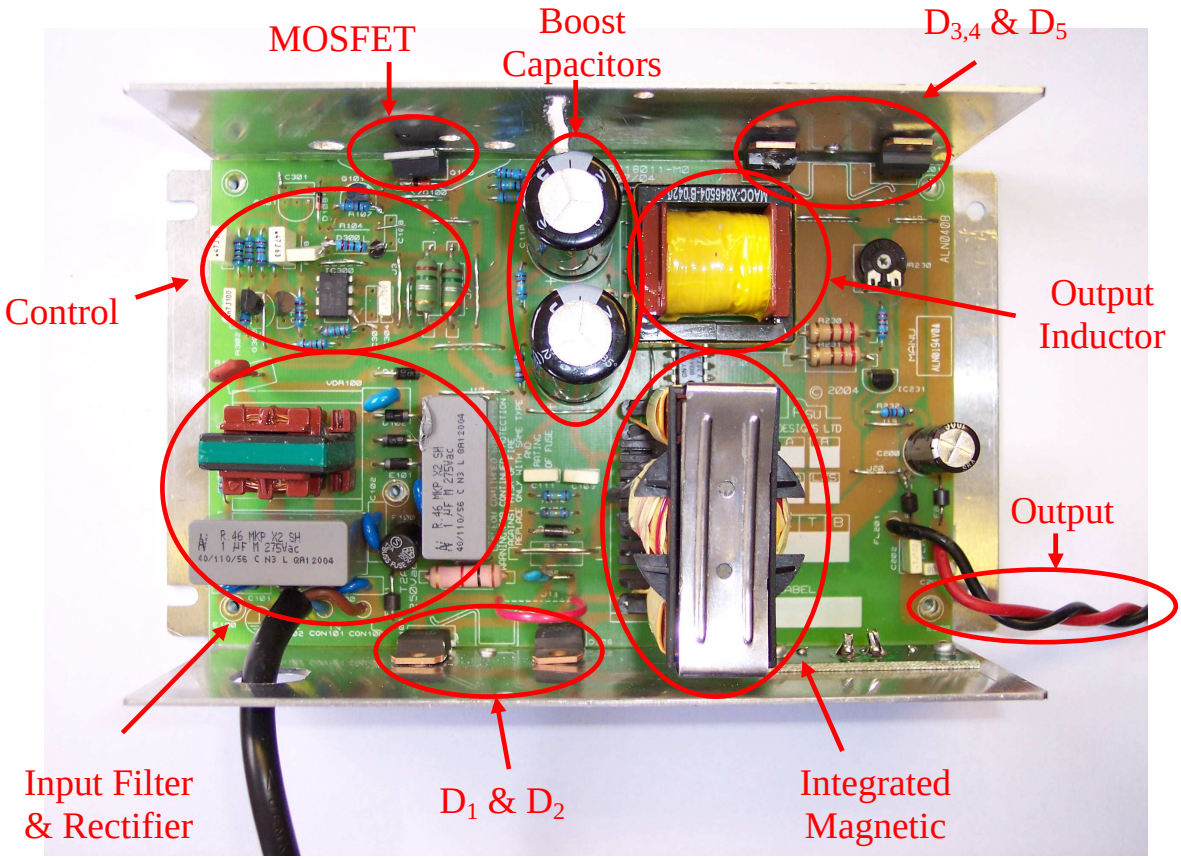


Figure 4-2 S^{4}PFC with integrated magnetic prototype

Once the PCB had been populated, detailed testing was undertaken using a artificially generated single phase AC sine voltage to ensure a good distortion free voltage waveform, a

Yokogawa WT3000 power analyser recorded and assessed the line voltage and current waveform quality and harmonic content, and a Lecroy WaveRunner oscilloscope along with a high voltage differential probe ADP305 and a AP105 current probe was used to measure converter waveforms. Figure 4-3 shows the laboratory set up used to evaluate the S^4PFC prototype.

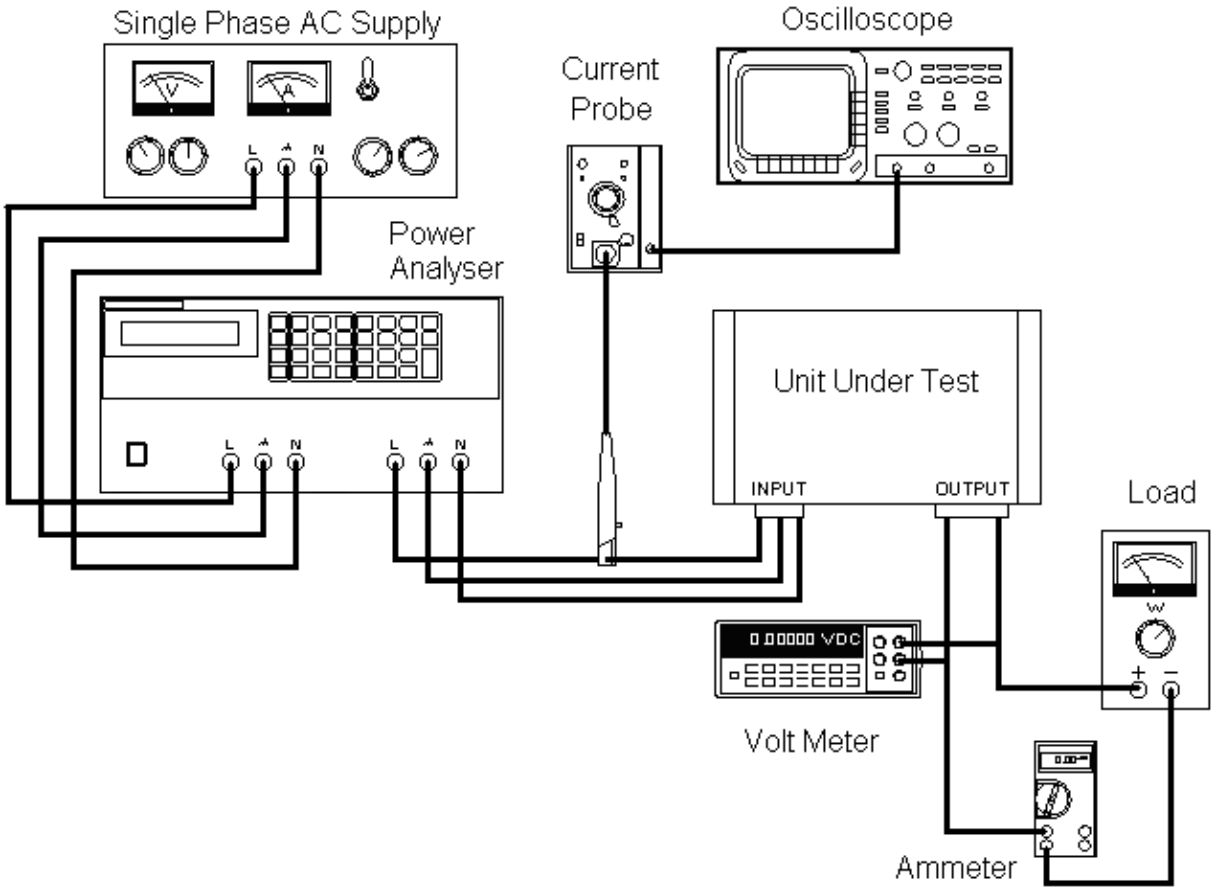


Figure 4-3 Laboratory setup

4.3 Experimental Verification and Performance Comparisons

The following sections detail the measured steady-state waveforms of the prototype S^4PFC and compare them with the theoretical predictions and SABER simulations over a number of operating conditions. Input current quality and harmonics are plotted at various line and loads states, as well as comparisons of key converter waveforms.

4.3.1 Input Current Quality and Harmonic Content

Figure 4-4 and Figure 4-5 show experimental and simulated results of the S^{4}PFC line supply voltage, V_s, and supply current, I_s, to determine wave shape quality, power factor and current harmonic content. The SABER simulations presented in this section are the result of mixed signal modelling of the steady-state S^{4}PFC schematic in Figure 2-23 with the component values listed in Table 2-2, and the control loop shown in Figure 3-14.

The simulated results are plotted in solid black lines, whilst the corresponding experimental results are plotted in colour. Figure 4-4 compares experimental and simulated V_s and I_s, where V_s = 230 V_{rms} and the converter output power is 180 W. The plots show comparable current waveforms. Despite the input current, I_s, not being purely sinusoidal due to the non-linearity of the DCM boost stage, it is in phase with V_s, indicating a high power factor and low harmonic current content.

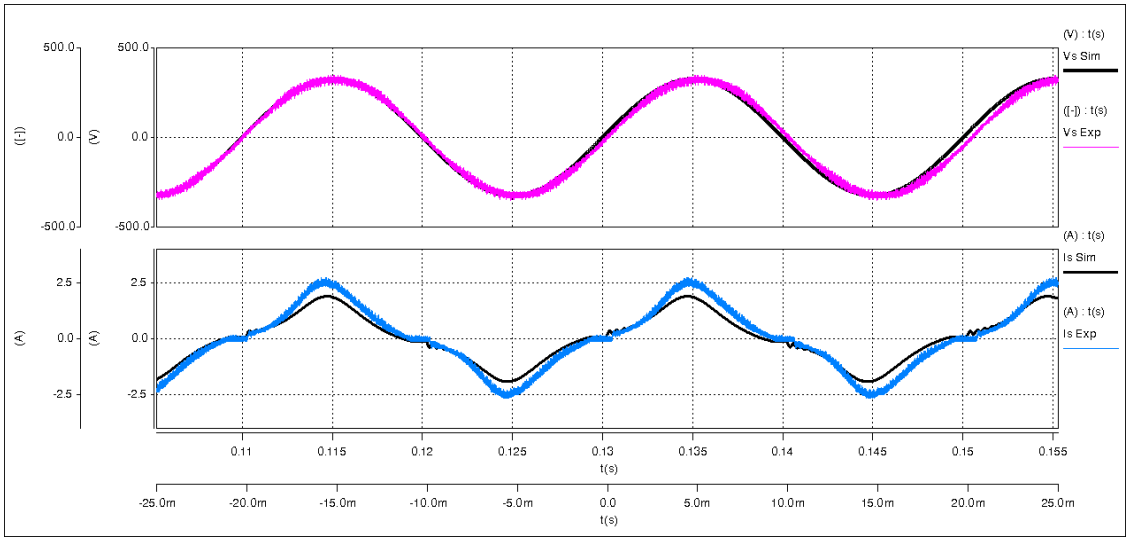


Figure 4-4 Simulated and experimental waveforms of I_s and V_s where V_s = 230 V_{rms} and P_0 =180 W

The amplitude of the experimental I_s results is larger than that of the simulated I_s results due to the S^{4}PFC parasitics and resistive losses that are not included in the SABER simulations. The small phase shift between the experimental results and the simulated results is due to slightly different line frequencies, the simulated frequency is accurately set to 50 Hz, however, in practice this is not precisely matched.

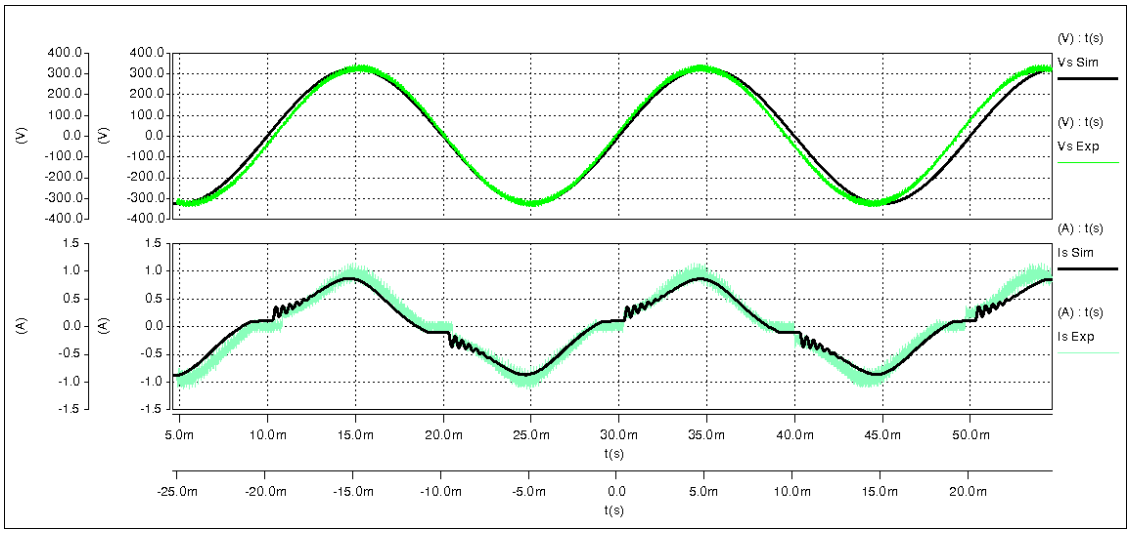


Figure 4-5 Simulated and experimental waveforms of I_s and V_s where V_s = 230 V_{rms} and P_0 =90 W

Figure 4-5 plots simulated and experimental results of I_s and V_s at an output power of 90 W. I_s is again in phase with V_s and there is a closer correspondence with the simulation data.

Table 4-1 S^4PFC input measurements over various operating conditions

V_s (V)	I_s (A)	P_s (W)	P_o (W)	S (VA)	Q (VAR)	φ (˚)	PF (%)	V_s THD (%)	I_s THD (%)
260	0.44	114	90	79	21	10.8	98	0.200	2.8
230	0.50	115	90	78	20	10.0	98	0.217	2.7
215	0.54	116	90	77	19	9.6	98	0.215	2.8
260	0.60	156	120	76	11	4.1	99	0.187	4.0
230	0.69	158	120	75	9	3.3	99	0.176	5.4
215	0.77	165	120	72	10	3.5	99	0.178	6.2
260	0.92	239	180	75	12	2.9	99	0.169	7.1
230	1.05	241	180	75	12	2.8	99	0.166	7.5
215	1.13	242	180	74	11	2.8	99	0.168	7.9

Using a Yokogawa WT3000 power analyser, Table 4-1 lists the experimental results of the input voltage and current quality at various operating conditions of th S^4PFC. Where **S** is apparent power, **Q** is reactive power, φ is the phase angle between V_s , and I_s. Power factor is labelled as **PF** and **THD** is the total harmonic distortion of V_s and I_s respectively. Since φ

is small across the operating conditions listed in Table 4-1, the subsequent power factor is near unity as expected with a boost converter operating in DCM, resulting in a low apparent power and successive reactive losses.

4.4 Steady State Waveforms

Figure 4-6 to Figure 4-8 show simulated and measured steady state waveforms of the S^4PFC with an output power of 180 W and an input line voltage of 230 V_{rms}. All of the simulations were performed with ideal components at a switching frequency of 100 kHz. The SABER simulated results are plotted in solid black lines, whilst the corresponding experimental results are plotted again in colour. Figure 4-6 plots waveforms of the discontinuous boost inductor current, I_{L_B}, and corresponding V_{L_B}. The experimental waveforms show close correlation with the simulated results in terms of wave shape and magnitude. The phase shift seen between the simulated and experimental results is due to slightly different switching frequencies and formatting discrepancies, the simulated frequency is accurately set to 100 kHz, however in practice the experimental switching frequency is 101 kHz, due to component tolerances. This applies to all figures in this section comparing simulated and experimental results.

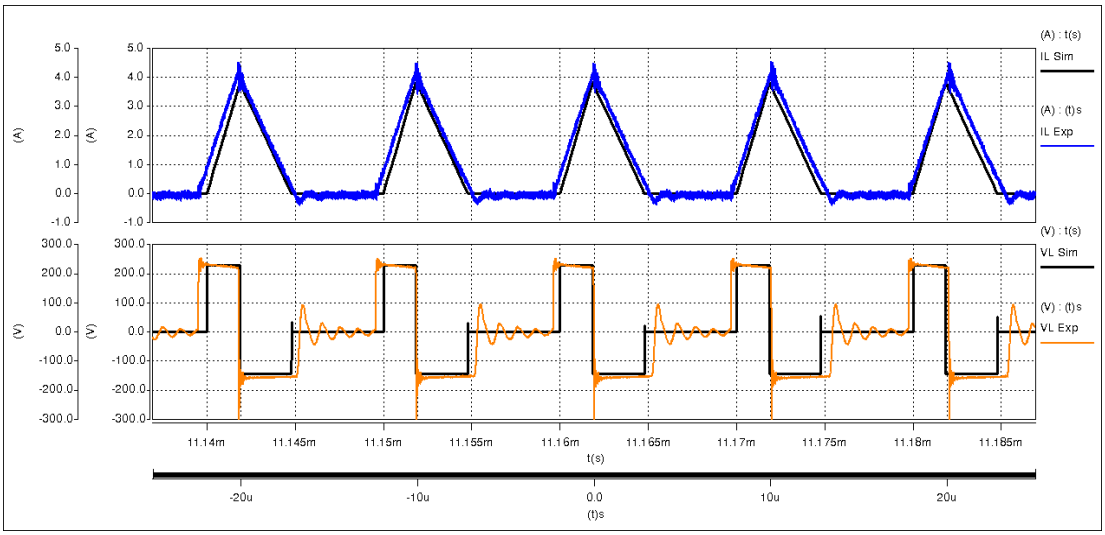


Figure 4-6 Simulated and experimental waveforms of I_{L_B} and V_{L_B} for V_s = 230 V and P_0 =180 W

The higher peak current I_{L_B} in the experimental result is attributed to PCB circuit losses, resistive winding losses and other parasitics not included in the simulation. These

parasitic effects also have an impact upon the duty ratio of the experimental results as the control loop automatically increases the duty ratio to compensate for the circuit losses and maintain the output voltage at the required level.

Despite efforts to ensure a compact and efficient circuit layout, track inductance and parasitic semiconductor capacitances also cause resonant ringing of the boost inductor voltage during the discontinuous current stage of the waveforms. This parasitic oscillation is especially evident in Figure 4-8 and Figure 4-11 and invariably adds to converter power losses. A small overshoot is also evident in the V_Q waveform at the turn-off instant which was attributed to the layout inductance and the leakage inductance of the transformer.

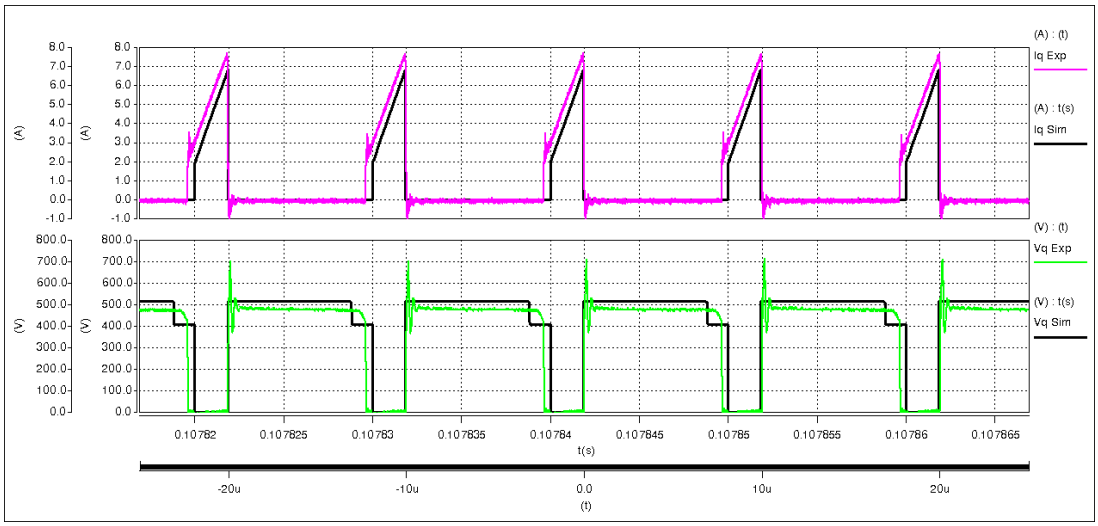


Figure 4-7 Simulated and experimental waveforms of I_Q and V_Q for V_s = 230 V and P_0 =180 W

The results in Figure 4-7 show that the experimental and simulated waveforms closely agree, however once again, unaccounted for component parasitics cause leading edge parasitic ringing in the experimental results. The experimental waveform of voltage V_Q is slightly lower than the simulated result due to a number of reasons. Higher than expected resistive and parasitic losses increase the load on the output of the boost stage**,** further, with V_B being lower than predicted, the duty ratio, D, must increase in order to achieve output voltage, V_o**,** regulation. The result of increasing D consequently reduces the time period t_3 to $t_0 + T_{sw}$ in Figure 2-3, pushing this recovery stage close the CCM as seen in the lack of step in the experimental wavform V_Q in Figure 4-7.

Figure 4-8 shows plots of simulated and experimental waveforms of I_{D_1} and V_{D_1} at an output power of 180 W. The two waveforms of I_{D_1} show close correclation, yet the experimental V_{D_1} shows significant high frequency ringing at the reverse bias voltage transition and low frequency ringing when I_{L_B} becomes discontinuous due to a less than ideal component layout, contributing to converter losses. The near continuous conduction mode operation of the transformer reset winding is also apparent in the experimental waveform of V_{D_1} as seen in the lack of step in Figure 4-8.

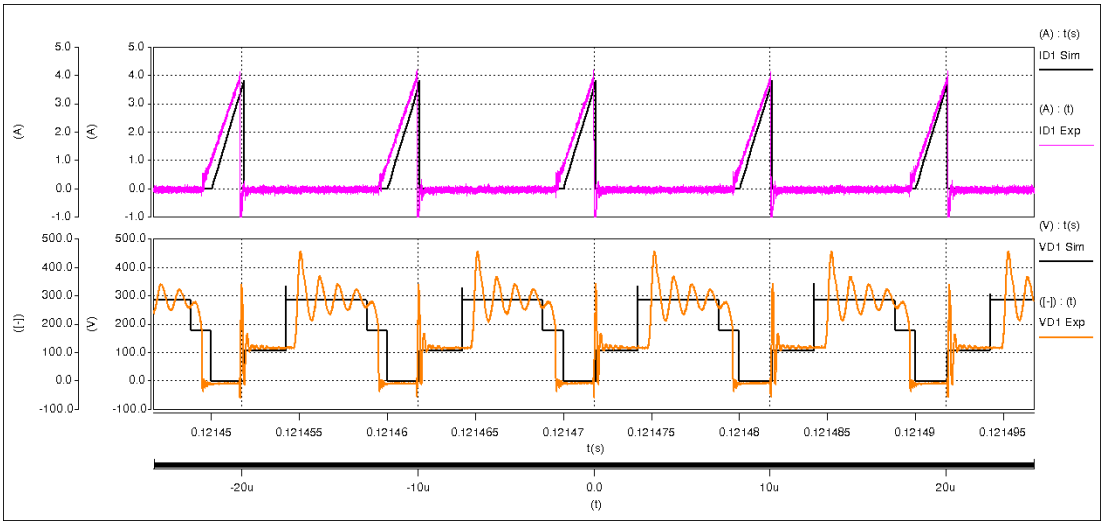


Figure 4-8 Simulated and experimental waveforms of I_{D_1} and V_{D_1} for V_s = 230 V and P_0 =180 W

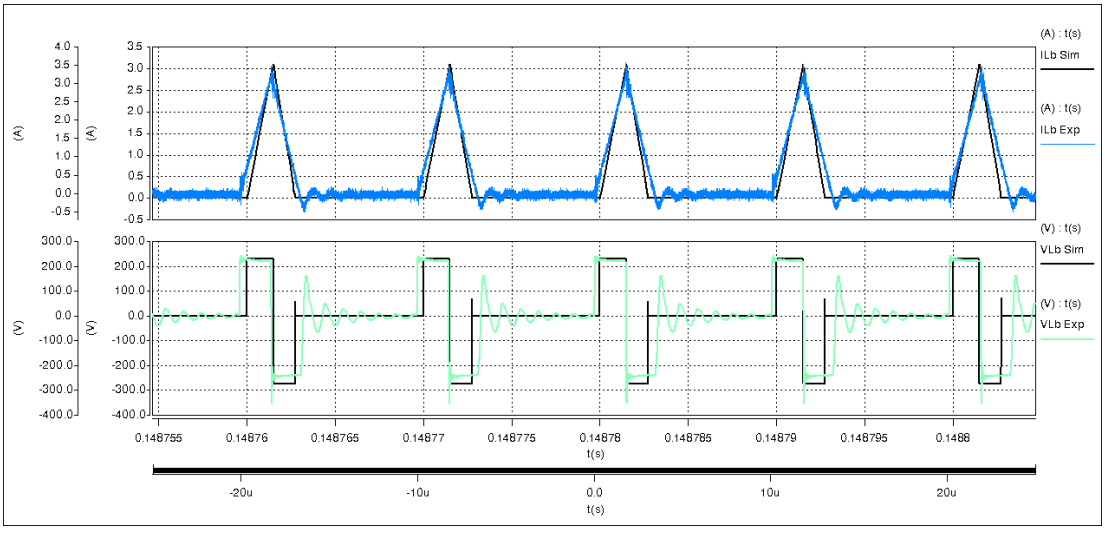


Figure 4-9 Simulated and experimental waveforms of I_{L_B} and V_{L_B} for V_s = 230 V and P_0 =90 W

Figure 4-9 to Figure 4-11 shows steady state plots of the S[4]PFC at an output power of 90 W. Again like the converter operation at 180 W the experimental results at 90 W shows close correlation to the simulated plots especially the experimental current plots of I_{L_B}, I_Q, I_{D_1} and I_{D_2}, for all of the conditions shown, confirming the expected performance and design of the integrated magnetic.

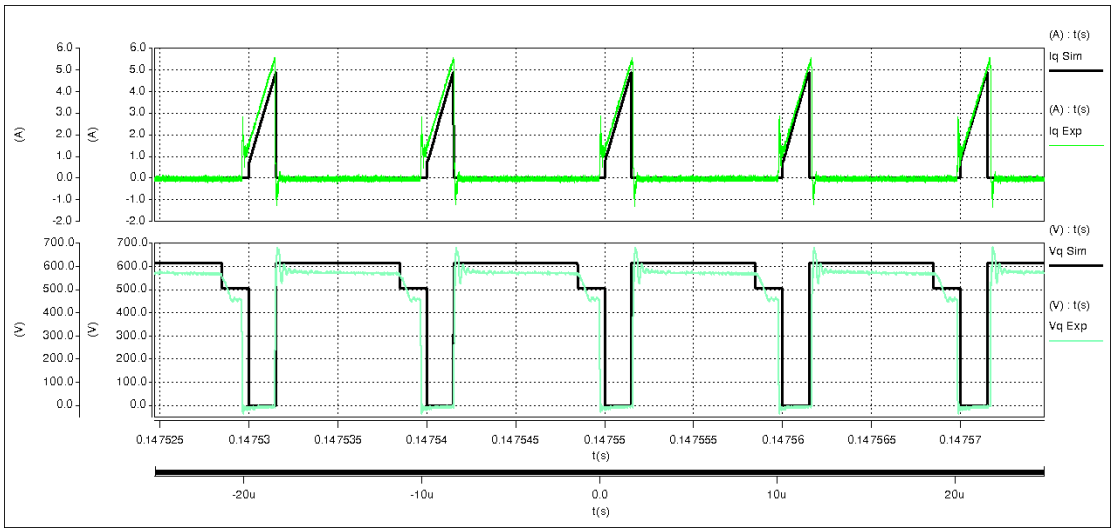


Figure 4-10 Simulated and experimental waveforms of I_Q and V_Q for V_s = 230 V and P_0 =90 W

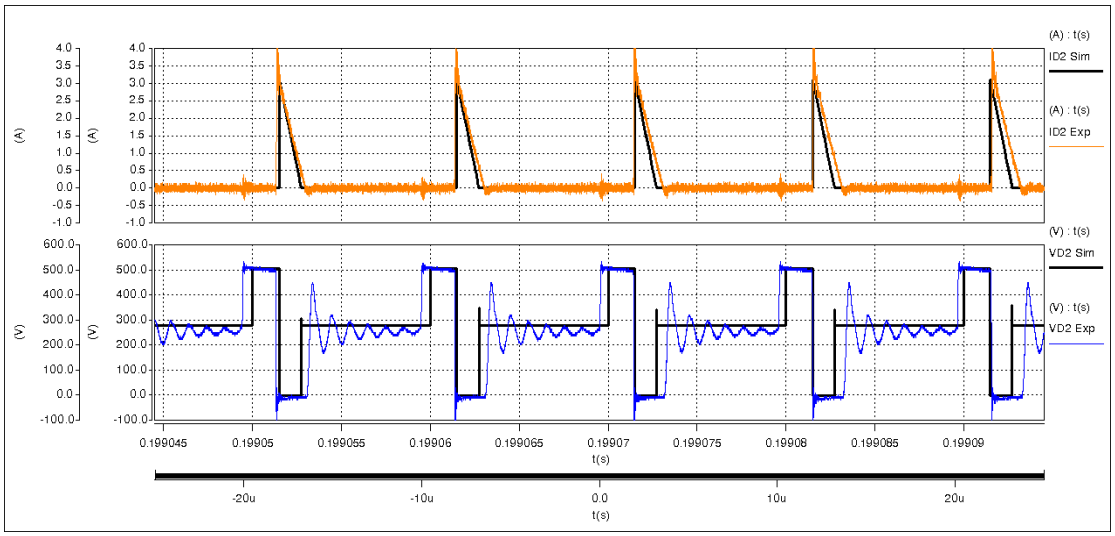


Figure 4-11 Simulated and experimental waveforms of I_{D_2} and V_{D_2} for V_s = 230 V and P_0 =90 W

Considering magnetic core utilisation, the analysis assumes that there is better core usage of the integrated magnetic approach compared to using separate magnetics. This

assumption is based upon the total core volumes involved in each case. Yet in practice, the desired core cannot always accommodate the total number of windings required, making it difficult to realise appreciable volume savings. Non-ideal elements in the converter still dominate during periods $(1\text{-}D)T_{sw}$ causing unwanted oscillations.

In conclusion to this section, the comparisons between the experimental results and the ideal SABER simulation results validate thoroughly the steady-state analysis and design performed in earlier sections, with the integrated magnetic performing as expected.

4.5 Cost Analysis

A cost evaluation of the S^4PFC is conducted in order to determine whether this single-stage single switch with an integrated magnetic approach is financially viable compared to the standard two-stage approach. In order to simplify the cost analysis and comparison of the two approaches, the S^4PFC and the two-stage prototypes are based on the same specifications.

Table 4-2 outlines the critical component analysis of the PFCs. The first column is the standard two-stage converter approach, the second details the S^4PFC with separate magnetic components. Finally, the third column shows again a S^4PFC, however this now utilizes integrated magnetics. All figures are normalized for simplicity, and the standard two-stage rectifier converter is used as a cost reference. The value of '3' for the IM is with reference to the combined cost of the boost inductor and the transformer in the two-stage converter.

Table 4-2 further shows the evident cost increase of having to utilize a high voltage and current rating for the MOSFET, **2.75**. The technology used for this device is a relatively new introduction to the commercial market and its cost therefore will fall with time.

Again, like the MOSFET, high rated parts that can withstand the voltage imposed and current ripple tend to be more costly components. So, in the S^4PFC two boost capacitors are arranged in series to withstand the stresses imposed, resulting in the high cost for this component.

The IM assembly is more expensive than that of the conventional separate magnetic components. This is again due to the technology being immature, therefore there is a high cost

associated with the tooling of non-standard bobbin formers, the complex winding and assembly of the constituent parts.

Table 4-2 Cost analysis of critical components

Component	Two-Stage	S^4PFC	S^4PFC with IM
MOSFETs	2	2.75	2.75
L_B	1	1	-
Transformer	1	1	-
IM	-	-	3
D_1	1	1.5	1.5
D_2	-	1	1
C_B	1	2.5	2.5
D_3	1	1	1
D_4	1	1	1
D_5	1	1	1
L_o	1	1	1
C_0	1	1	1
Control Circuitry	2	1	1
Relative Cost	**1**	**1.2**	**1.28**

Other major cost contributors to the total bill of materials include the PCB and the chassis. Despite the notable reduction in overall component count with the S^4PFC, the increase in the power ratings of various components, cancelled the effect for a reduced PCB area. Therefore, there was no effect on the volume and cost, of the PCB and metal work of all designs.

It can be noted however, that the manufacturing processes impeded the opportunity to reduce the overall volume of the single-stage approach significantly; single-sided, through-hole techniques were used on all converter assemblies. The use of double-sided, surface mount technologies would certainly reduce the overall volumes of the converters, but would correspondingly increase the cost of manufacture.

Further associated cost savings with the single-stage PFC that are not detailed in Table 4-2, include the costs of tracking, storing and assembling 26% fewer components than the two-stage Converter, this is mostly due to the elimination of a control loop.

This very small cost saving, compared to the high percentage savings from component reduction, is due to the manufacturing stage in which these components are inserted. Variable Centre Distance, VCD, and Axial Insert, AI, equipment was used to place all of these components automatically. Therefore, the impact of a reduction in assembly time/cost is minimal.

4.6 Summary

This chapter has described the development of the experimental prototype S^4PFC with an IM device. The detailed experimental results presented for the S^4PFC circuit show excellent correlation with earlier theoretical predictions and simulations, showing that this approach exhibits a near unity power factor with input current harmonics falling within specified limits, whilst being able to provide a regulated output voltage. An important contribution is demonstrating that this IM arrangement can be implemented within the S^4PFC topology, reducing component count and increasing core usage, whilst having little detrimental affect upon the performance of the power stage.

5 Ultra Bright White Light Emitting Diode Driver

5.1 Introduction

This chapter details the design and development of a power converter for a high power white light emitting diode street luminaire. A suitable power topology is identified for the power factor correction stage and the constant current regulator stage, and necessary modifications are made in order to fulfil the requirements specified in Chapter 1. The steady-state operation of the converter is detailed, as well as the essential design equations. MATLAB and SABER simulations characterise the steady-state performance of the converter and verify the design equations. Finally, simulated and experimental results verify the design methods and validate the approach for a HP LED street luminaire.The street light is to be used on main distributors, and is of lighting class M3a. Main distributors are routes between strategic highways such as dual carriage ways and urban centres, where speed limits are < 40 mph [123].

These issues impact on the design of the HP LED street light, leading to an unusual electrical design. Taking into account these concerns, Figure 5-1 shows the design of the concept luminaire which will adhere to the regulations, and includes both the power converter and HP LED strings.

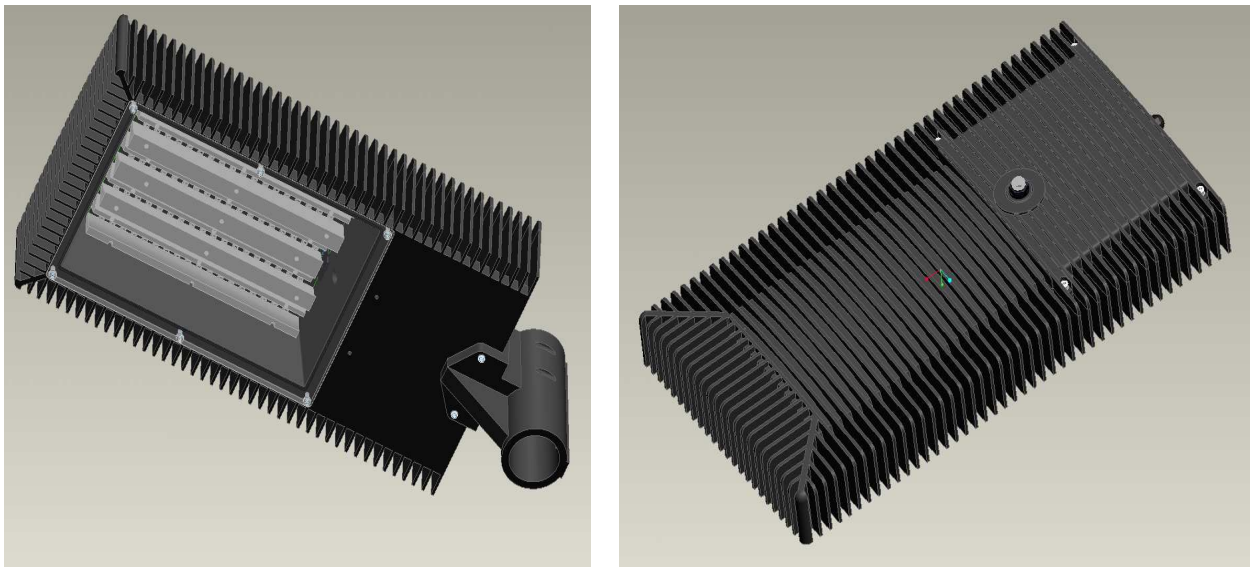


Figure 5-1 CAD drawing of proposed LED Street Light

5.2 HP LED Power Converter Requirements

As already detailed in Chapter 1, HP LEDs cannot be directly connected to the mains supply, as firstly they require reverse voltage protection, secondly, the current through the HP LEDs needs to be regulated, and finally there are harmonic limits specified for lighting equipment that is connected to the mains grid. The power factor correction stage limits line harmonic currents, minimises total harmonic distortion, and provides sufficient energy storage during the twice per cycle voltage zeros. A secondary converter is required to regulate the current through the HP LED strings.

An added difficulty is the elimination of any electrolytic capacitors, so that a long converter lifetime can be achieved, see section 1.2.7.2. as the useful operational lifetime of HP LEDs is 50,000 hours. Many commercially available PFC drivers implement the lowest cost electrolytic capacitors available for the requirement, to minimise 100 Hz ripple frequency and perform energy storage. Yet these electrolytic capacitors have an operating lifetime of typically several thousand hours [40]. If exposed to high temperature environments or high ripple currents, the lifetime of these wet electrolytic capacitors will be reduced further due to the electrolyte evaporating and venting and so the operating life of the entire system would be compromised. In order to provide continuous power flow to the load and avoid 100 Hz stroboscopic effects, a capacitor with the necessary energy storage capacity is needed. This can be realised by using a long life, > 50,000 hours, electrolytic capacitor, which is expensive and too large to fit in the luminaire, or using a non-electrolytic capacitor operating at a high voltage to provide the necessary energy storage.

Metal film capacitors are suitable for high voltage use and have long lifetimes. These capacitors are inexpensive and physically small [137] compared to long life time electrolytic capacitors [43]. Other characteristics include low ESR, low ESL, low dissipation factor and high reliability. These attributes all indicate that this capacitor type would be suitable for this application. Metal film polyester dielectric construction is preferred over a film/foil construction due to the self healing properties, smaller relative size and lower cost per microfarad, see Figure 5-2.

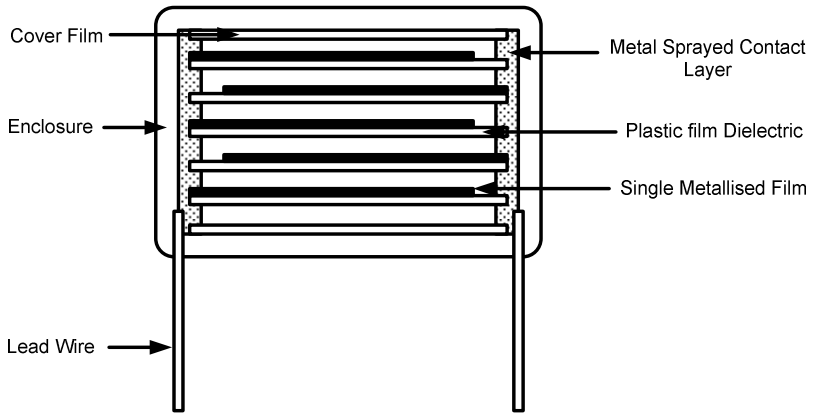


Figure 5-2 Metallised film capacitor construction

Assuming metal film capacitors are used, the only PFC converter options are those topologies that can boost the output voltage higher than the peak line voltage.

As well as being electrically efficient, durable and requiring low maintenance during its lifetime, the power converter must also meet street luminaire optical standards which govern the quality of the light output [42, 123, 138] and section 1.2.8. Of particular concern are stroboscopic effects.

To avoid these unwanted effects a secondary cascaded converter is required to produce a constant current in the LEDs. This converter must operate at switching frequencies beyond the sampling frequencies of camera equipment and human visual perception. The converter also performs a light dimming function if required.

Figure 5-3 is a block diagram of the HP LED power converter arrangement. The power factor block contains the input EMC filter, mains rectifier, energy storage, and auxiliary power supplies. The other three blocks are controlled constant current regulators which each supply a HP LED string. These regulators are independent of one another, as this approach allows for control of the street luminaires optical footprint.

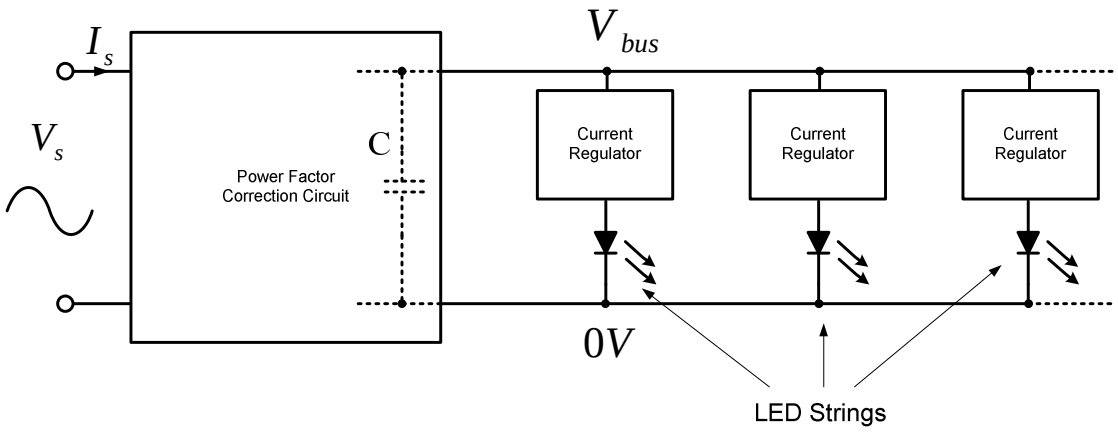


Figure 5-3 HP LED power converter block diagram

5.3 Power Factor Correction Converter Selection

Since the HP LED street light will draw more than 25 W of power from the supply, it is subject to Class C requirements of British Standard 61000-3-2:2006 [13]. This class is more stringent than other classes, as it is the only case where a limit for the 2nd harmonic input current is specified, see Table 1-1.

Referring to Figure 5-3, the capacitor, C, must store enough energy to allow it to supply the LED drivers during the twice per cycle mains voltage zeros, so that the voltage supplied to these never falls below the minimum necessary for correct operation.

This requirement precludes passive PFC approaches and the active buck switching converter topology identified in Chapter 1, since the DC link voltage must be higher than the peak line voltage, $\hat{V}_s$. Section 1.2.3 describes the power imbalance that the active PFC stage must compensate, and using **Eqn 5-1,** the output voltage, V_{bus}, of the PFC, must be higher than $\hat{V}_s$.

$$V_{bus} = \sqrt{E_{C,mean}{}^2 \pm \frac{P_o \sin(2\omega t)}{\omega}} \qquad \textbf{Eqn 5-1}$$

Therefore the remaining suitable converters are boost and buck-boost type converters. An isolated topology such as the flyback converter is not required, as galvanic isolation adds complexity to the power stage. Other converters identified for PFC include the Cuk, Sepic and

Zeta converters. The operation of these converters, Section 1.2.3, reveal that they do not have an inherent PFC ability, produce a distorted input current waveform and are not suitable for this application.

The author believes the buck-boost converter is the most suitable power topology for the role of street luminaire PFC. The converter is able to boost its output voltage to a level significantly higher than its input voltage, albeit this is a negative voltage. The negative voltage is not problematic for this application, as the load comprises constant current regulators and HP LED strings. The converter can be operated in DCM, which automatically shapes the input current to be directly proportional to the input voltage, ensuring a near unity power factor and a simpler approach to control than continuous current mode operation. This is beneficial since lighting harmonic current regulations are more stringent than for other equipment.

5.4 Principles of Operation of Power Factor Correction Stage

This section details the discontinuous operation of the power factor correction buck-boost converter, Figure 5-4. As this power stage offers no significant research interest, only brief principles of operation of the power stage are given along with simulations and a power loss audit of the regulator.

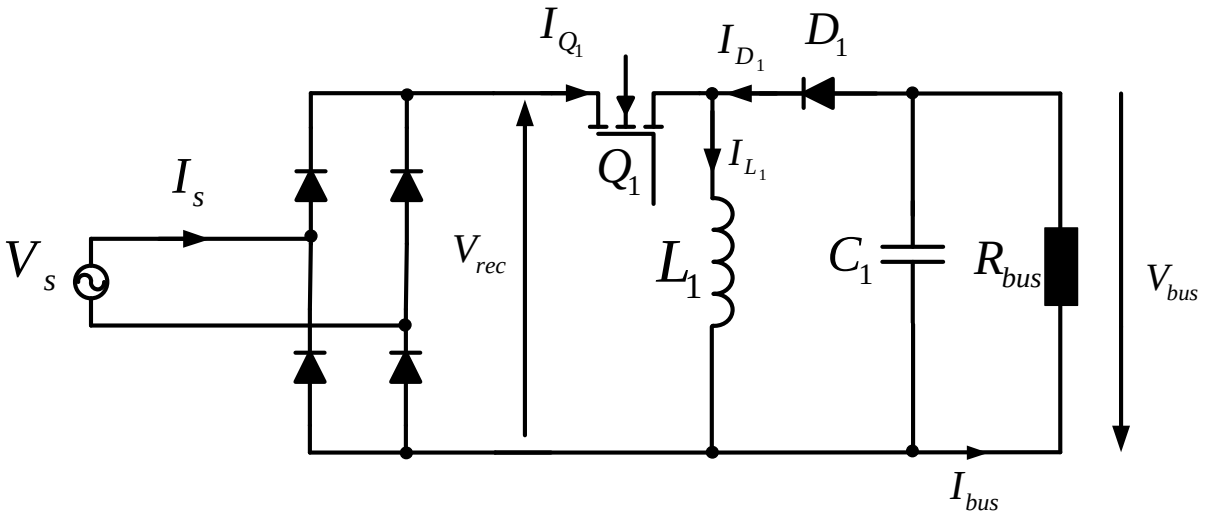


Figure 5-4 Buck-boost power factor corrector stage

Described is the state-by-state operation and key waveforms, see Figure 5-6. This section also details the analysis and predicted performance of the power factor correction circuit. With the buck-boost converter operating in DCM, the topology can eliminate the need for unnecessary complex control circuitry and requires only a small L_1 value compared to a CCM inductor. Control circuit simplification is achieved due to the inherent operation of the DCM. The current through L_1 becomes zero at some time within the off-period of Q_1, in each switching cycle, thereby ensuring the peak value of input current is proportional to voltage and in phase with it, resulting in a near resistive input impedance for the stage. With this approach, a high PF can be realised. Along with Figure 5-6, a description of the operating principles of a DCM buck-boost restifier is given.

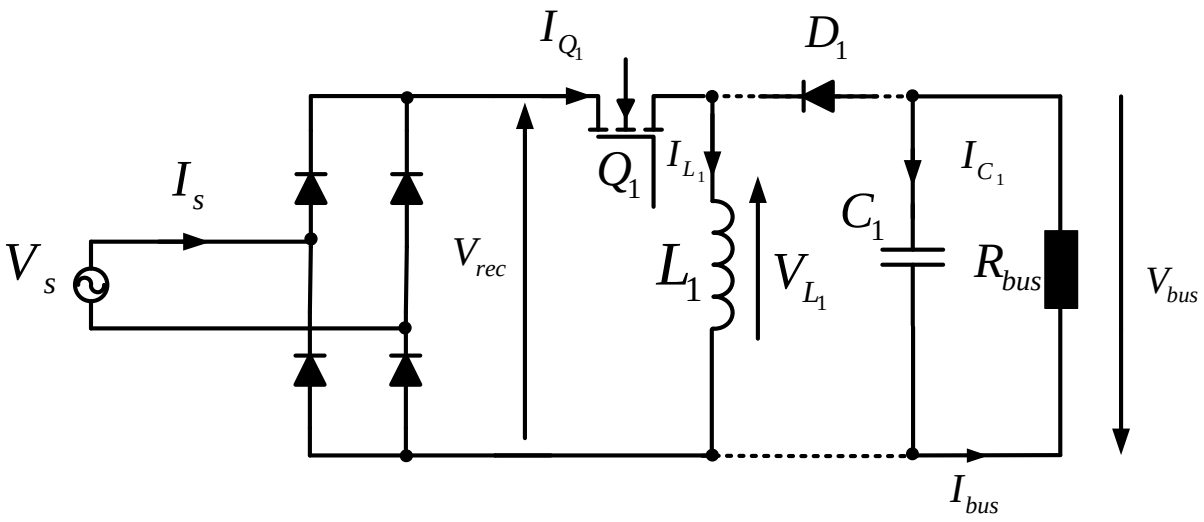


Figure 5-5 Buck-boost converter at t_0 to t_1

During period nT_{sw} to t_{n1}, the effective circuit of the buck-boost converter is shown in Figure 5-5. MOSFET Q_1 is conducting and the input voltage V_{rec} is applied to inductor L_1. The current through L_1 and Q_1 is given by

$$\frac{\hat{I}_{L_1}}{DT_{sw}} = \frac{\left|\hat{V}_s\right|}{L_1} \qquad \textbf{Eqn 5-2}$$

where D and T_{sw} are the duty cycle and switching period of the buck boost power stage respectively.

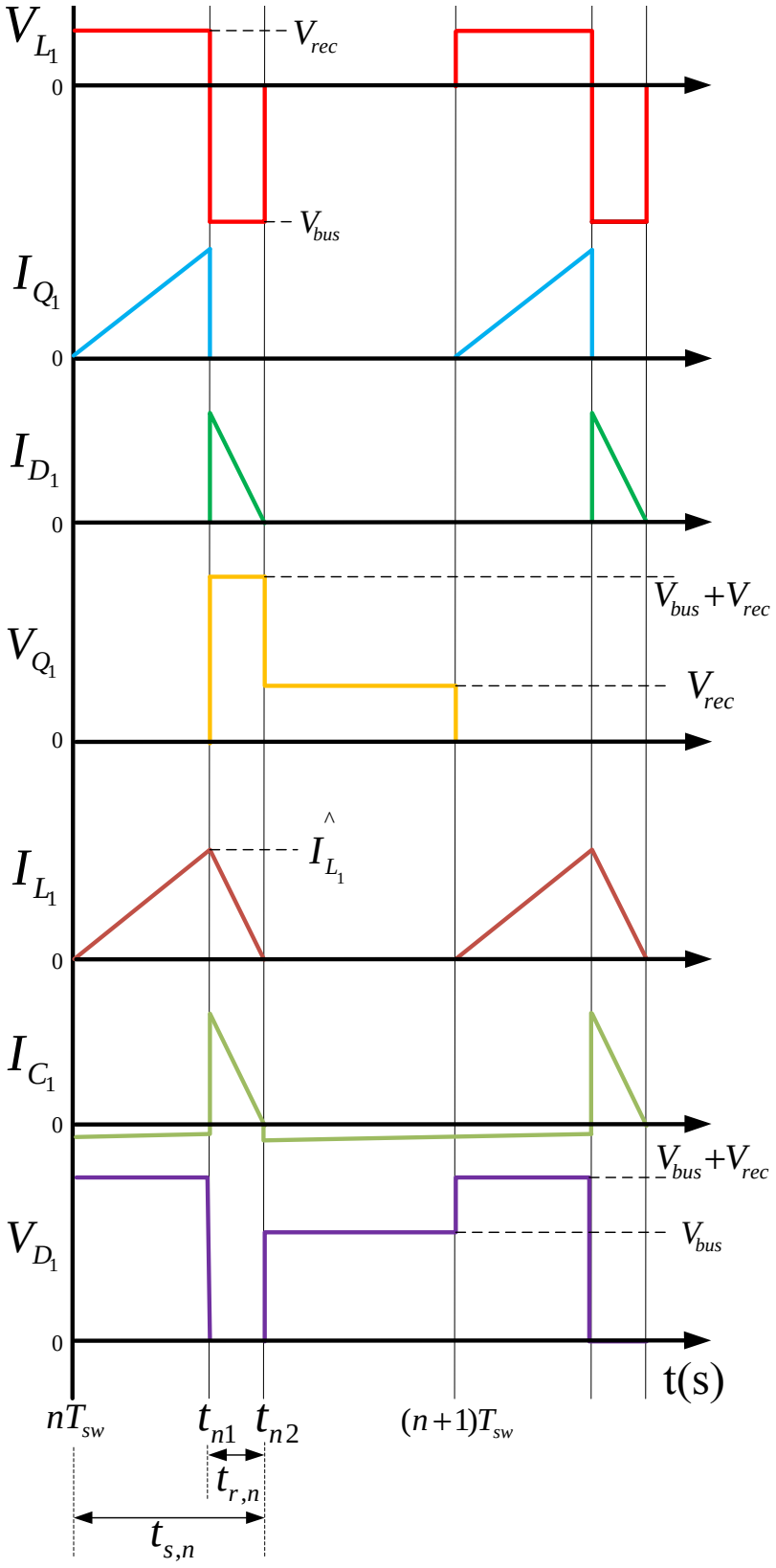


Figure 5-6 Key waveforms of DCM buck-boost converter

Diode D_1 is reversed biased and capacitor C_1 supplies the current to the output load. Thus

$$\hat{I}_{L_1} = \frac{\left|\hat{V}_s\right| DT_{sw}}{L_1} \qquad \textbf{Eqn 5-3}$$

The reverse bias voltage across diode D_1 is given by

$$V_{D_1} = V_{rec} + \left|V_{bus}\right| \qquad \textbf{Eqn 5-4}$$

During the time, t_{n1} to t_{n2}, Q_1 is off and the circuit is shown in Figure 5-7. The inductor is connected to the output load and capacitor via D_1 and the energy stored in L_1 transfers to C_1 and the output load. Q_1 voltage becomes

$$V_{Q_1} = V_{rec} + \left|V_{bus}\right| \qquad \textbf{Eqn 5-5}$$

The voltage across L_1 is now equal to V_{bus}.

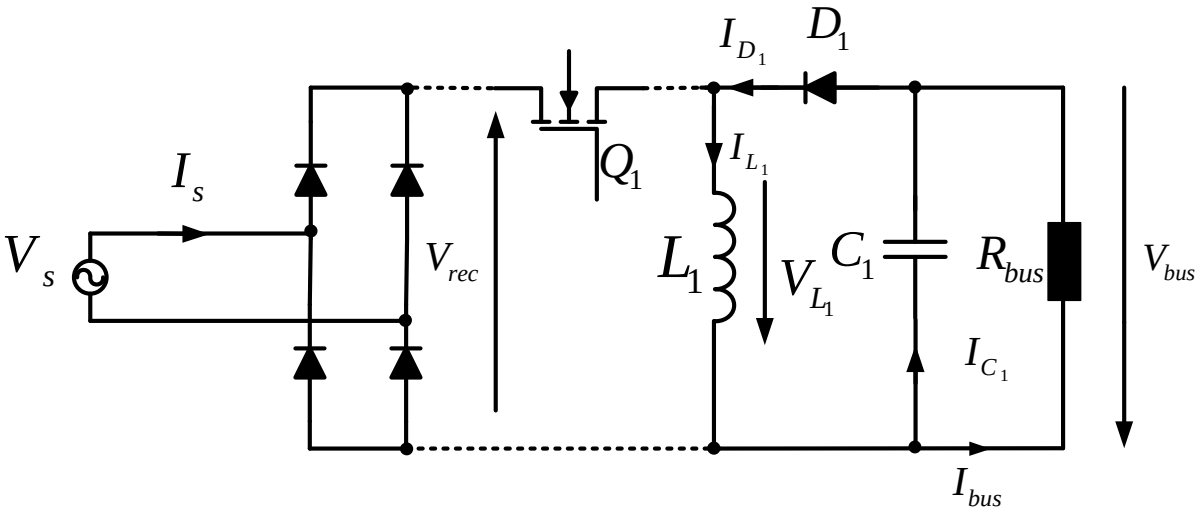


Figure 5-7 Buck boost converter during t_1 to t_2

In discontinuous current mode control, I_{L_1} falls to zero before the start of the next switching cycle. This period t_{n1} to t_{n2} is given by

$$t_{r,n} = \frac{\hat{I}_{L_1} \cdot L_1}{V_{bus}} = \frac{V_{rec} D T_{sw}}{V_{bus}} \qquad \textbf{Eqn 5-6}$$

During the remaining off period t_{n2} to $(n+1)T_{sw}$ the inductor current I_{L_1} is zero. This time period is determined as

$$(n+1)T_{sw} - t_{n2} = T_{sw}\left(DT_{sw} + \frac{V_s D}{V_{bus}} T_{sw} \right) \qquad \textbf{Eqn 5-7}$$

The output capacitor C_1 now supplies current to the load during this period.

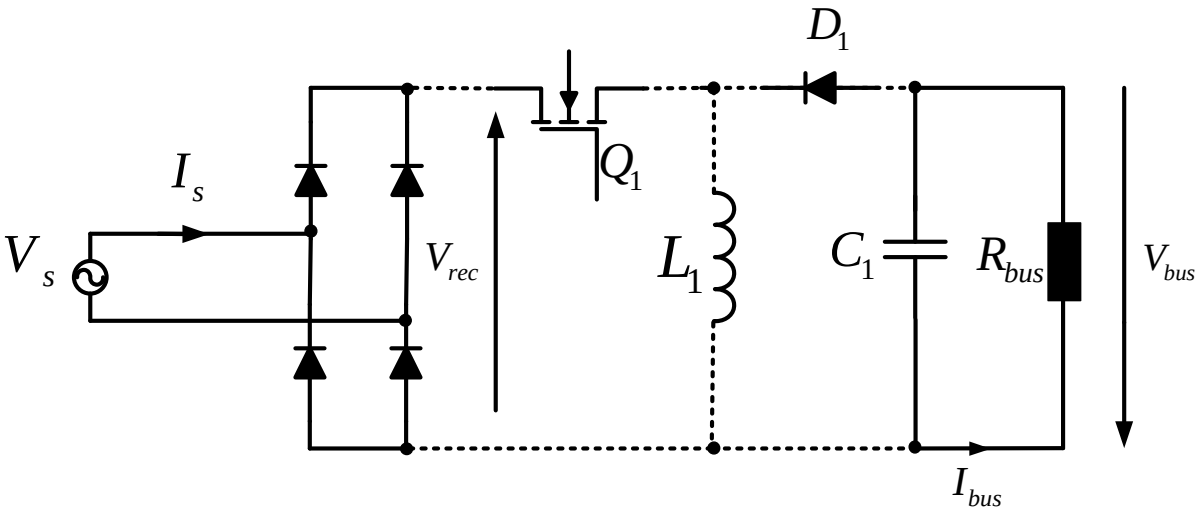


Figure 5-8 Buck boost converter during period t_{n2} to $(n+1)T_{sw}$

The high frequency output voltage ripple $\tilde{V}_{bus_{sw}}$ is

$$\tilde{V}_{bus,sw} = \frac{\hat{I}_{L_1}}{C_1}\left(t_{n1} - nT_{sw} \right) \qquad \textbf{Eqn 5-8}$$

Thus far, the analysis of the buck-boost converter has only been concerned with the steady-state DCM condition over a single switching cycle. Neglecting the effect of an input filter, over a single line period the input voltage, V_s, is time varying as described by

$$V_s(t) = \hat{V}_s \sin \omega t \qquad \textbf{Eqn 5-9}$$

where $\hat{V}_s$ is the peak line voltage, ω, is the angular frequency of the line voltage. Similarly the rectified voltage, V_{rec}, is defined as

$$V_{rec}(t) = \hat{V}_s \left|\sin \omega t\right| \qquad \textbf{Eqn 5-10}$$

With a constant duty cycle, over half a line period, the DCM buck-boost inductor current is similar to that of the DCM boost current of the S^{4}PFC shown in Figure 2-7. However, unlike the DCM boost converter the trailing edge of I_{L_1} is not seen by the input, as shown in Figure 5-9.

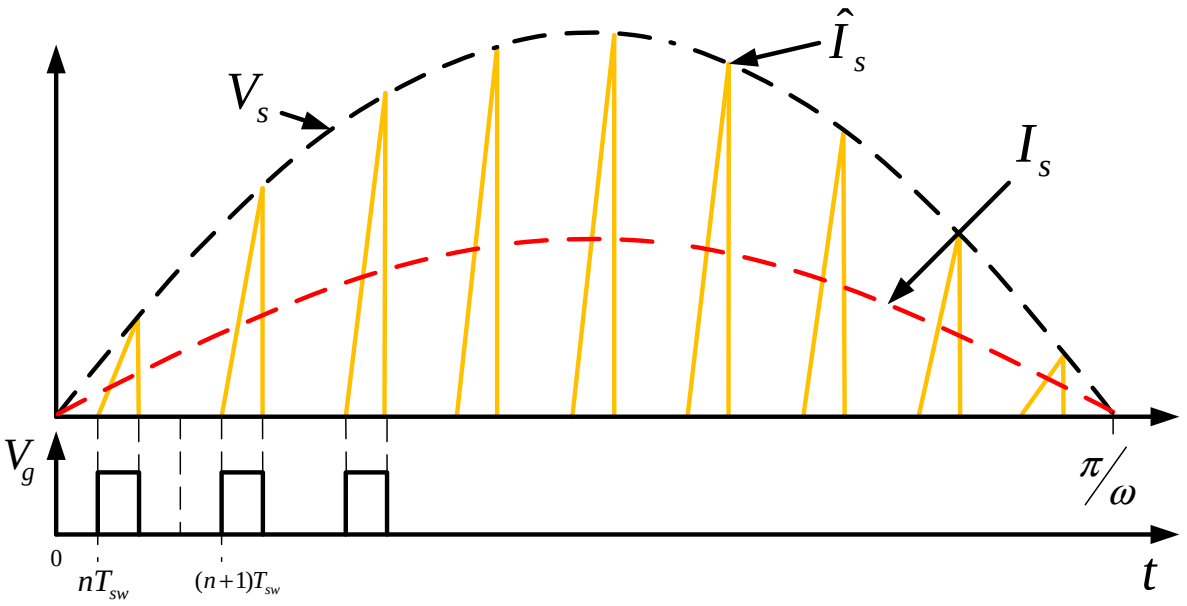


Figure 5-9 Buck boost input voltage, V_s, and current, I_s, over a half line period.

From **Eqn 5-3** and **Eqn 5-9**, the peak inductor current, I_{L_1} can be defined as

$$\hat{I}_{L_1} = \frac{\left|\hat{V}_s \sin \omega t\right|}{L_1} DT_{sw} \qquad \textbf{Eqn 5-11}$$

From Figure 5-6, the average current of I_{L_1} during nT_{sw} and $(n+1)T_{sw}$ can be found as

$$I_{L_1,n} = \frac{t_{s,n}\hat{I}_{L_1}}{2T_{sw}} \qquad \textbf{Eqn 5-12}$$

Substituting **Eqn 5-4, Eqn 5-6** and **Eqn 5-11** into **Eqn 5-12** yields

$$I_{L_1,n} = \frac{D^2 T_{sw}}{2L_1 V_{bus}} \hat{V}_s \sin \omega t_n \qquad \textbf{Eqn 5-13}$$

Therefore the average current of inductor L_1 over a half line period of 0 to π/ω is described as

$$I_{L_1} = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} \left(\frac{D^2 \hat{V}_s T_{sw}}{2L_1 V_{bus}} \sin^2 \omega t \right) dt = \frac{D^2 \hat{V}_s T_{sw}}{4L_1 V_{bus}} \qquad \textbf{Eqn 5-14}$$

Assuming no converter losses, thus $P_{in} = P_o$, from **Eqn 5-13**

$$\frac{D^2 \hat{V}_s T_{sw}}{4L_1 V_{bus}} = \frac{D^2 \hat{V}_s}{4L_1 V_{bus} f_{sw}} = \frac{V_{bus}}{R_{bus}} \qquad \textbf{Eqn 5-15}$$

From [139] the voltage gain is defined as

$$V_{bus} = \frac{D\hat{V}_s}{2\sqrt{\tau_{L_1}}} \qquad \textbf{Eqn 5-16}$$

where $\tau_{L_1} = \frac{L_1 f_{sw}}{R_{bus}}$ is the normalised inductor time constant.

To ensure that the converter remains in discontinous current mode, **Eqn 5-17** determines the boundary conduction conditions.

$$M_{BC} = \frac{V_{bus}}{\hat{V}_s} = \frac{D}{2(1-D)} \qquad \textbf{Eqn 5-17}$$

Figure 5-10 plots the duty cycle against the converter voltage gain of **Eqn 5-17**

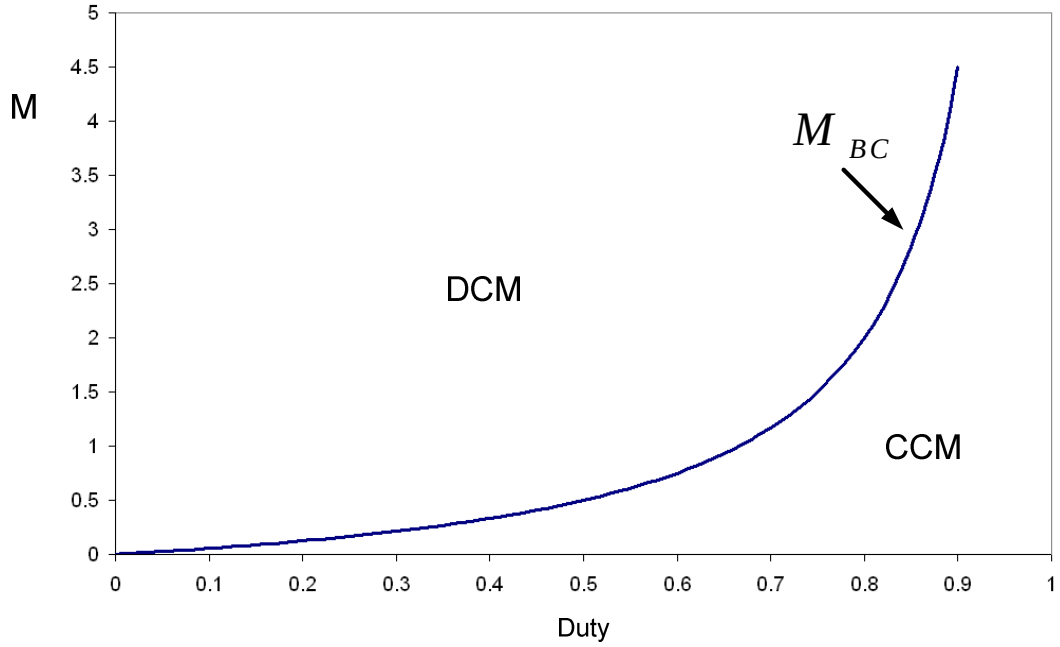


Figure 5-10 Boundary conduction of buck boost PFC coverter

Therefore to maintain discontinuous current mode the inequality of **Eqn 5-18** must be satisfied.

$$L_1 < \frac{R_{bus}}{f_{sw}} \tau_{L_1} \qquad \textbf{Eqn 5-18}$$

As C_1 will be a metal film capacitor of a few μF value, so the voltage across it, V_{bus}, will have a high component of ripple at 100 Hz as seen in Figure 5-11. The RMS current of C_1 is

$$I_{C_{1,rms}} = \sqrt{I_{D_{1,rms}}{}^2 - I_{bus_{rms}}{}^2} \qquad \textbf{Eqn 5-19}$$

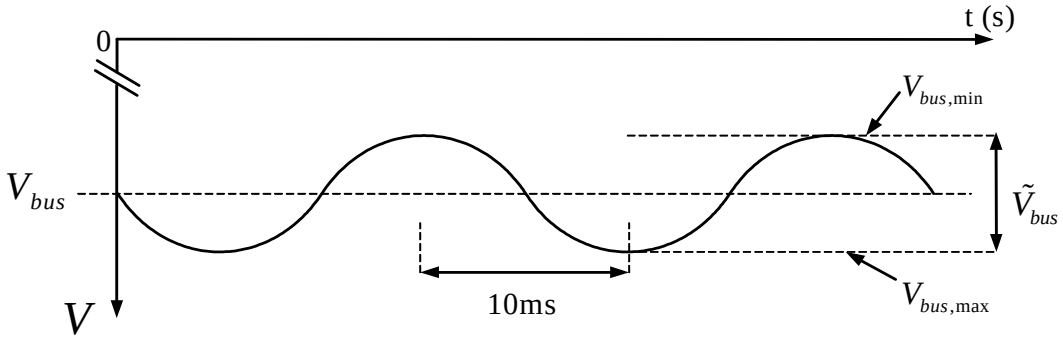


Figure 5-11 V_{bus} waveform

The 100 Hz ripple voltage can be determined by

$$\tilde{V}_{bus} = V_{bus,\min} - V_{bus,\max} \qquad \textbf{Eqn 5-20}$$

where

$$V_{bus,\min} = \sqrt{V_{bus}{}^2 - \left(\frac{P_o}{2\pi f_{line} C_1}\right)} \qquad \textbf{Eqn 5-21}$$

and

$$V_{bus,\max} = \sqrt{V_{bus}{}^2 + \left(\frac{P_o}{2\pi f_{line} C_1}\right)} \qquad \textbf{Eqn 5-22}$$

f_{line} and P_o are the line frequency and the output power of the PFC converter respectively. Note, that from **Eqn 5-20**, $\tilde{V}_{bus}$, varies with load current, this result is of interest when determining the control parameters, see Chapter 6.

5.5 Buck Boost Power Factor Correction Specification

Table 5-1 details the specification of the power stage, which were set by the sponsoring company Dialight Lumidrives. The HP LED PFC is designed to operate at a nominal 230 V_{rms} input with an output power of 180 W. The converter must also comply with input current harmonic limitations for Class D equipment as shown in [13].

Table 5-1 HP LED power factor corrector specification

Description		Value	Unit
Input Voltage	V_s	230 +10, -6%	V_{rms}
Max Input Current	I_s	1.0	A_{rms}
Line Operating Frequency	f_{line}	50	Hz
Output Power Range	P_{out}	60 - 180	W
Converter Efficiency	η_{PFC}	80 % @ 180 W	
Power Factor	PF	≥ 0.98	

5.6 Converter Optimisation and Component Selection

In order to achieve maximum performance of this power converter stage whilst obtaining long operating lifetime and converter reliability, parameters such as the switching frequency and peak component voltage stresses need to be identified. The design approach becomes an iterative process, as not only does the most optimal electrical performance need to be chosen but also the component cost and physical size needs to be evaluated and a balance found. This section details the design and selection of the key electrical power components discussing the balance to achieve maximum converter performance whilst minimising size and cost. Before the optimisation process can begin a number of parameters are defined. The operating phase voltage range is 230 V_{rms} +10 % -6 %, the output bus voltage of the PFC stage is -600 V, this value was arbitrarily chosen to ensure a high PF, provide sufficient energy storage due to the low buck-boost capacitance, and to obtain an efficient duty ratio for the current regulator stage. The output power range of the stage is 60-180 W. Therefore from **Eqn 2-17** the voltage ratio M, varies between 1.60 and 1.96.

Using the normalised inductor time constant, τ_{L_1} and inserting various values for L_1, a value of 900 μH ensures that the buck-boost PFC converter stays in discontinous current mode over all line and load conditions.

Figure 5-12 plots τ_{L_1} over low and high line, low and high output power loads showing the operating area of the PFC power stage. The plot clearly shows the converter operating in DCM with sufficient margin as to ensure no CCM boundary cross over.

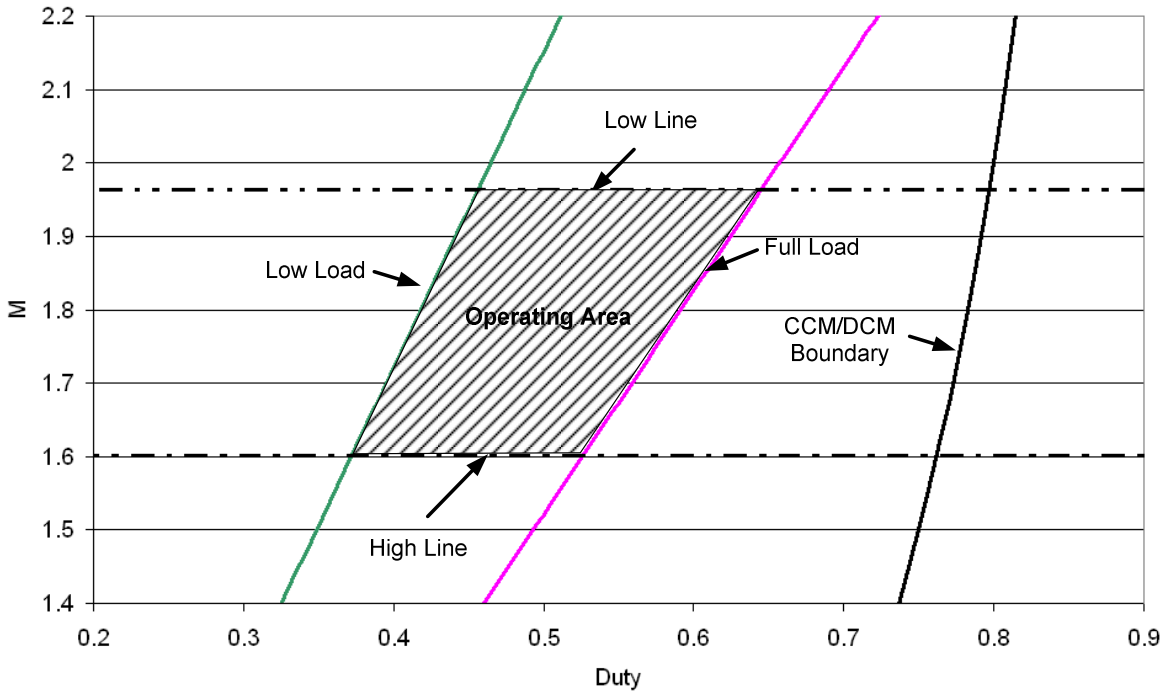


Figure 5-12 DCM buck boost PFC operating area.

As the minimum value of L_1 to maintain DCM has been identified, peak and average currents can be determined and consequently semiconductor and capacitor devices can be shortlisted.

Table 5-2 lists a number of suitable switching power MOSFETS for Q_1. These devices are all rated to withstand the peak voltage, as determined by **Eqn 5-5**, and are inexpensive and readily available.

Table 5-2 Selection of suitable Si MOSFETs for Q_1

Component	Voltage Rating (V)	Continuous Current (A)	Rds_{on} Norm (Ω)	t_{rr} (ns)	Device Cost (£)
Toshiba 2SK1120	1000	8	1.75	50	5.07
Toshiba 2SK1119	1000	4	1.9	18	3.79
ST STP5NB100	1000	5	1.75	11	4.90
ST STP8NK100Z	1000	6.3	1.75	19	3.23
IR IRFBG50	1000	6.1	1.6	35	8.79
IR IRFBG30	1000	3.1	2.0	25	1.66
Vishay IRFPG40	1000	4.3	1.75	33	3.51

The operation of the buck boost converter in DCM exposes its semiconductor components to significantly higher voltage and current stresses than that of a boost converter operating under similar conditions. The diode, D_1, is subject to high peak currents, **Eqn 5-3,** and a high reverse voltage, **Eqn 5-4**. Suitable power diodes that will withstand these stresses are listed in Table 5-3.

Table 5-3 Selection of Si ultra fast power diodes

Diode	**Rated Voltage (V)**	**Rated Current (A)**	**T_{rr} (ns)**	**Forward Voltage (V)**	**Cost (£)**
RHRP8120	1200	8	50	1.0	0.56
UF4007	1000	1	75	1.7	0.36
RHRG30120	1200	30	70	2.6	1.20
FFPF10F150S	1200	10	85	1.9	0.50
RURD10F150	1200	4	68	2.5	0.60
ISL9K301G3	1200	30	45	2.6	1.56

The diodes shown in Table 5-3 are all Si diodes. SiC diodes, see section 1.2.7.1, would be more appropriate due to their lower switching losses. However due to the commercial constraints of cost and availability, they were not considered for this application.

Table 5-4 Section of metallised film capacitors

Capacitor	**Rated Capacitance (uF)**	**Rating Voltage (V)**	**Max $\frac{dv}{dt}$ $(V/\mu s)$**	$\tan\delta$	**Cost (£)**
MMK37.5475K	4.7	1000	10	0.008	3.50
R60QW4470	4.7	1000	10	0.010	3.52
MMK37.5395K	3.9	1000	10	0.008	3.20
940C10W2K	2.0	1000	480	0.001	3.18
MMKP386	1.8	1000	350	0.001	2.98
MKP1840M	1.5	1000	195	0.002	1.89
MWA10W1K	1.0	1000	40	0.005	1.75

Table 5-4 lists a number of metallised film capacitors and their characteristics. Capacitor selection for the output filter stage of the buck boost converter is dependent upon the rated voltage, current ripple, lifetime and operating temperature for this particular

application. The capacitor is subjected to a continuous voltage of around 600V with an additional voltage ripple at twice the line frequency. Figure 5-13 shows a plot of the total power loss of the shortlisted MOSFETs in

Table 5-2 versus various L_1 values when operating at a fixed switching frequency. The power loss mechanisms of MOSFETs are detailed in Appendix A. The MOSFET type 2SK1120 has the lowest combined losses of all the devices at all operating conditions. However from

Table 5-2, it is one of the most expensive. Since cost is also a driving factor in this application, the STP8NK100Z was chosen as the preferred device as it only has an increased power dissipation of 0.5 W over the 2SK1120, and this extra power loss was considered acceptable.

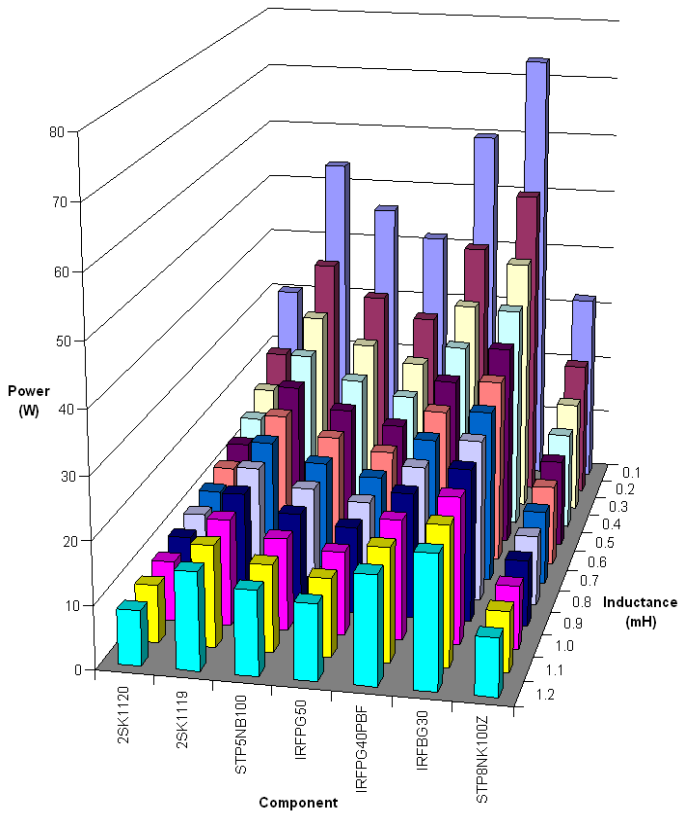


Figure 5-13 Total losses of MOSFETs versus inductance

Figure 5-14 shows the total power loss of the power diodes suitable for D_1 versus various L_1 values at fixed switching frequency. By inspection, it is seen that diode RHRP2180 is the most appropriate device, having the least total power loss, yet having an acceptable cost, see Table 5-3.

Identifying the best switching frequency, f_{sw}, is dependent upon a number of factors. The higher the switching frequency, the smaller the magnetic devices can be. However an excessively high switching frequency will cause switching losses to dominate over conduction losses, and EMC will become a greater issue. Figure 5-15 illustrates the loss of the MOSFET type STP8NK100Z at L_1=900 uH over various frequencies.

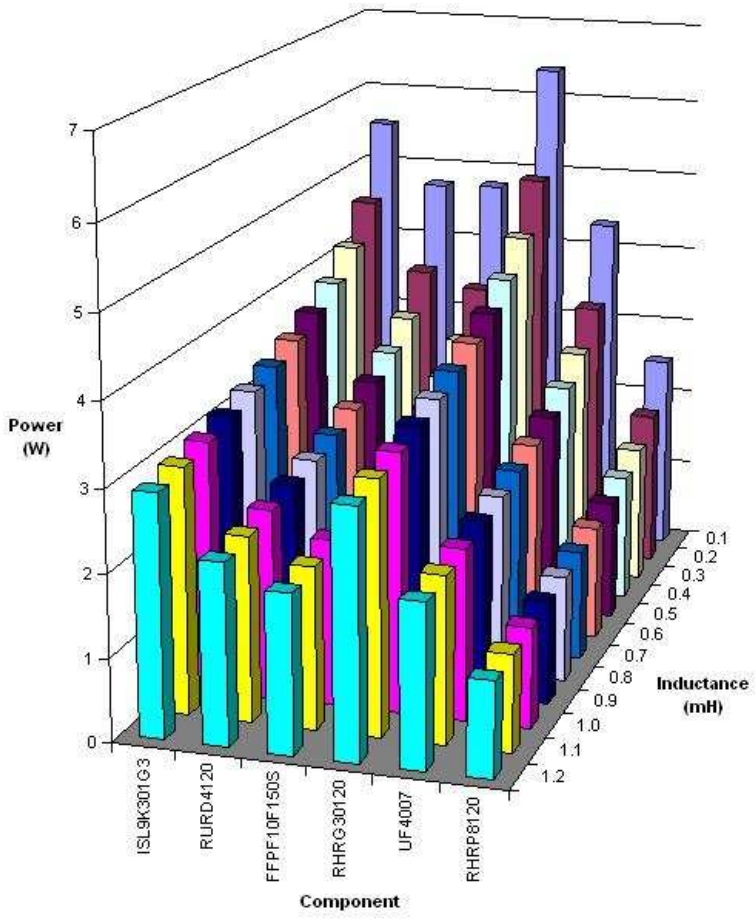


Figure 5-14 Total diode losses versus inductance

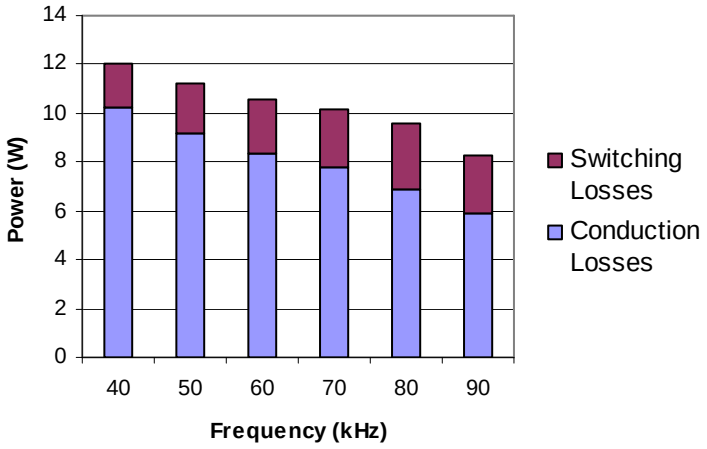


Figure 5-15 MOSFET STP8NK100Z power losses versus frequency

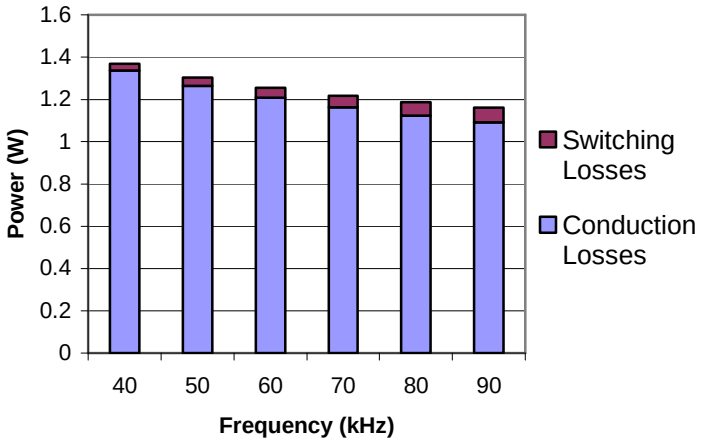


Figure 5-16 Diode RHRP8120 losses versus frequency

As the switching frequency increases, so conduction losses reduce, but losses due to switching dynamics increase. From this plot, the lowest power loss is at 90 kHz, and the same is true for the diode RHRP8120 in Figure 5-16. However at frequencies above 60 kHz, using **Eqn 5-18**, the buck boost converter tends further towards continuous conduction mode. Therefore 60 kHz is the maximum switching frequency allowable.

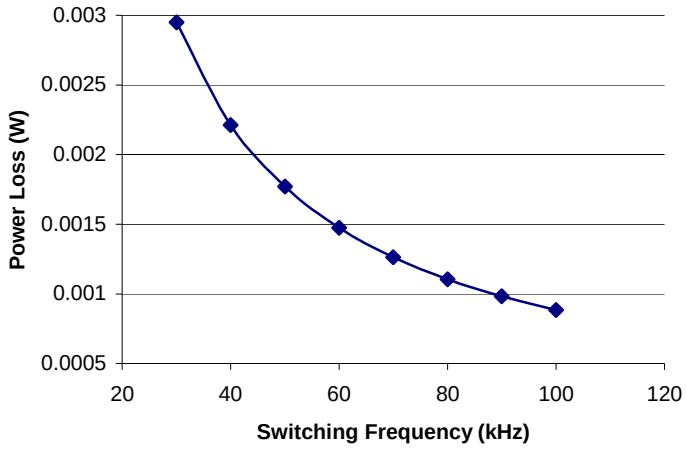


Figure 5-17 Capacitor losses against converter switching frequency

There is little to distinguish between the output filter capacitors for the PFC stage listed in

Table 5-4. The capacitor selected was the 4.7uF 1kV Evox Rifa MMK35.7 475K1000R08L4, based purely on cost and capacitance value. In order to limit the low frequency voltage ripple, $\tilde{V}_{bus}$, using **Eqn 5-20**, a total output capacitance of 14.1 uF is required. Using **Eqn 5-19,** $I_{C_{1,rms}}$, and the manufacturers specifications of $\tan\delta$, the power loss of C_1 can be determined. The power loss of this capacitor versus switching frequency is shown in Figure 5-17.

The losses associated with the metal film capacitors are negligible across the range of switching frequencies considered. Therefore C_1 does not impact upon the selection of f_{sw}. The loss mechanisms of the capacitor can be seen in Appendix C.

5.7 Selection of Magnetic Components

The choice of magnetic core subtly affects the converters operation. The magnetic core structure and winding arrangement can radiate EMC which can interfere with and disturb electrically sensitive control stage components, causing converter instability. Due to the compactness required in the luminaire, switching power electronic components and control circuit components are closely located to one another. Therefore a magnetic structure that inherently shields generated switching parasitics will be needed.

An RM type core [130] was chosen for L_1. This core is mechanically robust, has a large copper window area, and provides magnetic shielding as the windings are totally enclosed. 3F3 core material is the most suitable for the selected switching frequency, as it provides the lowest losses.

Magnetic core optimisation is an involved iterative process. A balance has to be struck between core hysteresis losses and limiting wire copper losses. Hysteresis losses are a function of the converter switching frequency and the flux swing of the core [45]. Wire losses are invariably a result of the resistance of the wire and the current through it. Figure 5-18 depicts the calculated winding and core losses incurred at 100 ºC, [46, 130]. From this graph the lowest total power loss occurs at a core gap of 1.6 mm.

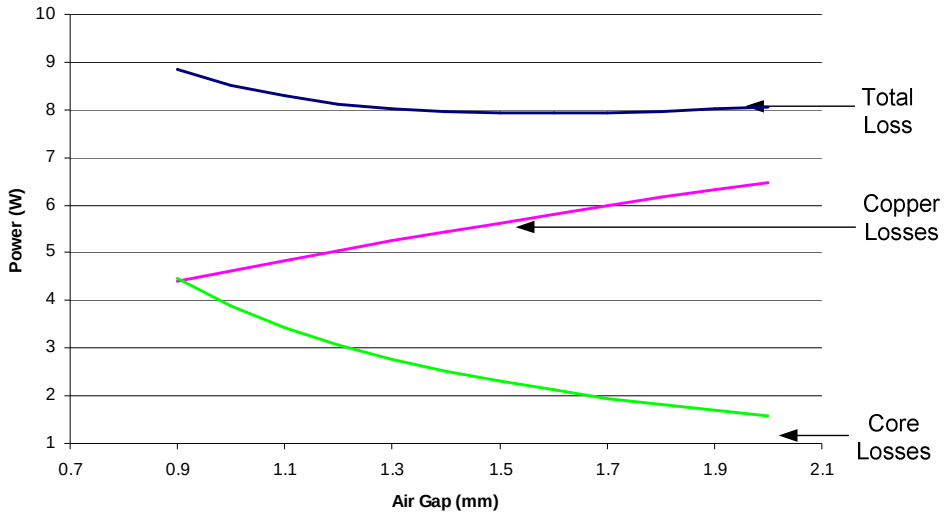


Figure 5-18 Magnetic losses at various core air gaps

Owing to the high specific resistance of ferrite materials, the eddy current losses in the frequency range of interest, 1 kHz - 2 MHz, may be practically disregarded except in the case of core shapes having a large cross-sectional area. A design summary of the discontinuous current mode buck boost inductor is given in Table 5-5.

The completed inductor was tested by an HP 4284A LCR meter. The measured inductance showed a value of 904 uH, a wire resistance of 1.01 Ω and a winding capacitance of 12 pF.

Table 5-5 Characteristics of the power factor correctors inductor

Parameter	**Calculated**	**Unit**
Core manufacturer	Ferroxcube	-
Core type	RM12	-
Core material	3C90	-
Core factor	0.38	mm^{-1}
Effective volume	8340	mm^3
Effective length (m)	55.6	mm
Effective area	146	mm^2
Max flux density (T)	380 @ 100 ºC	mT
Mean turn length	61	mm
Initial permeability	1730	-
Effective permeability	30.9	-
Air gap	1.6	mm
Inductance factor	114.7	nH
Inductance	900	uH
Number of turns	88	-
Flux	35	uW
Flux density	254	mT
Wire length	5.4	m
Current density	3.0	A/mm^2
Wire resistance @ 100 ºC	1.01	Ω
Copper loss @ 100 ºC	5.8	W
Core loss @ 100 ºC	2.11	W
Total losses @ 100 ºC	7.9	W

5.8 Loss Audit

Table 5-6 lists the significant power loss components of the PFC converter. The worst case operating condition is when P_{out} is maximum, V_s is at its minimum input. This estimation does not include the power loss due to track, connector or cabling resistance.

Table 5-6 Estimated power losses of converter components at P_{out}=180 W and $V_{s,min}$

Component	Device	Switching Loss (W)	Conduction Loss (W)	Core Loss (W)	Total Loss (W)
Q_1	STP8NK100Z	2.2	8.3	-	10.5
D_1	RHRP8120	0.04	1.2	-	1.24
L_1	RM12	-	5.8	2.1	7.90
C_1	MMK35.7 475K	-	0.015	-	0.01
Total Estimated Power Loss					**19.65**
Expected Efficiency					**90%**

Table 5-6 shows that the conduction loss of Q_1 is the largest single source of power loss in the PFC converter. This loss could have been reduced by using the IRFBG50 MOSFET from International Rectifier, however the 8 % $R_{ds,on}$ reduction does not justify the 63 % cost increase. Furthermore the switching rise and fall time of the IRFBG50 is increased by 45 %, thus increasing MOSFET switching losses.

The second largest loss component is the winding loss of L_1. To reduce this power loss would require a reduction in inductance, the consequence being an increased peak current. Litz wire could be used to reduce ac resistance loss but this wire is expensive and any decrease of power loss would be minimal [10].

Diode power losses are mostly due to the forward conduction losses of the device, switching losses are minimal, as DCM operation reduces the switching losses during turn on of any semiconductor component. Capacitor losses are negligible, due the low $\tan\delta$.

5.9 Summary of PFC Design

Table 5-7 details the key calculated parameters of the PFC buck-boost converter at the nominal input voltage, 230 V_{rms} for three output powers. The buck-boost converter is specified to operate from 180 W to 90 W, which is the specified output of the HP LED street luminaire. The power converter will never have to operate in a no load condition.

Table 5-7 Key PFC component parameters at $V_s = 230V_{rms}$ at P_{out}=60 W, 120 W and 180 W

Parameter	60 W	120W	180 W	Unit
V_s	230	230	230	V_{rms}
$I_{s,rms}$	0.26	0.52	0.78	A_{rms}
f_{line}	50	50	50	Hz
f_{sw}	60	60	60	kHz
k	0.018	0.036	0.054	-
D	0.35	0.49	0.60	-
$\hat{V}_{L_1}$	325	325	325	V
$\hat{V}_{Q_1} = \hat{V}_{D_1}$	936	947	958	V
$\hat{I}_{L_1} = \hat{I}_{Q_1} = \hat{I}_{D_1}$	2.10	2.98	3.65	A
$nT_{sw} \rightarrow t_{n1}$	5.83	8.25	10.10	μs
$t_{n1} \rightarrow t_{n2}$	3.16	4.47	5.48	μs
$t_{n2} \rightarrow (n+1)T_{sw}$	7.67	3.95	1.090	μs
V_{bus}	600	600	600	V_{rms}
$\tilde{V}_{bus}$ (at $2\times f_{line}$)	23	46	68	V
$\tilde{V}_{bus,fsw}$	0.21	0.41	0.60	V
I_{bus}	0.10	0.20	0.30	A_{rms}

5.10 PFC SABER Simulation

A SABER model was constructed to confirm the predicted results detailed in section 5.9. Figure 5-19 shows this idealised model, which consists of a simplified buck-boost power stage and its control stage.

All the power stage components are ideal devices. The MOSFET is modelled as an ideal switch with zero on state resistance and infinite off state resistance. The power diodes are piece wise linear components with zero forward volt drop. The power inductor is linear with no resistance or interwinding capacitance. The output capacitor is also ideal with no resistance or inductance. The following simulation results demonstrate the steady state performance of the DCM buck-boost converter and the proposed voltage regulation band control. The results

presented are for a voltage input $\mathbf{V_s}$**= 230** $\mathbf{V_{rms}}$ with an output power $\mathbf{P_{out}}$**= 180 W** and $\mathbf{L_1}$**= 900 µH,** $\mathbf{C_1}$**=14.7 µF,** f_{sw} **=60 kHz**.

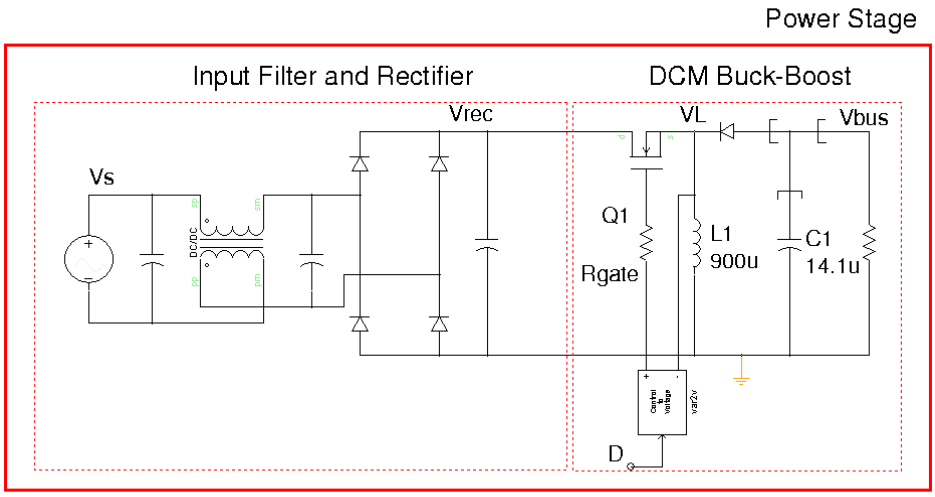


Figure 5-19 SABER schematic capture of DCM buck boost PFC stage

Figure 5-20 shows a number of key simulated waveforms for the buck boost converter operating in discontinuous current mode over a number of switching frequency cycles. These simulated waveforms closely correspond to the predicted waveforms, Figure 5-6, and calculated predictions of Table 5-7. There is one disparity in Figure 5-20, f_{sw} is not exactly 60 kHz, this is due to the resistor capacitor combination chosen for generating the oscillator signal.

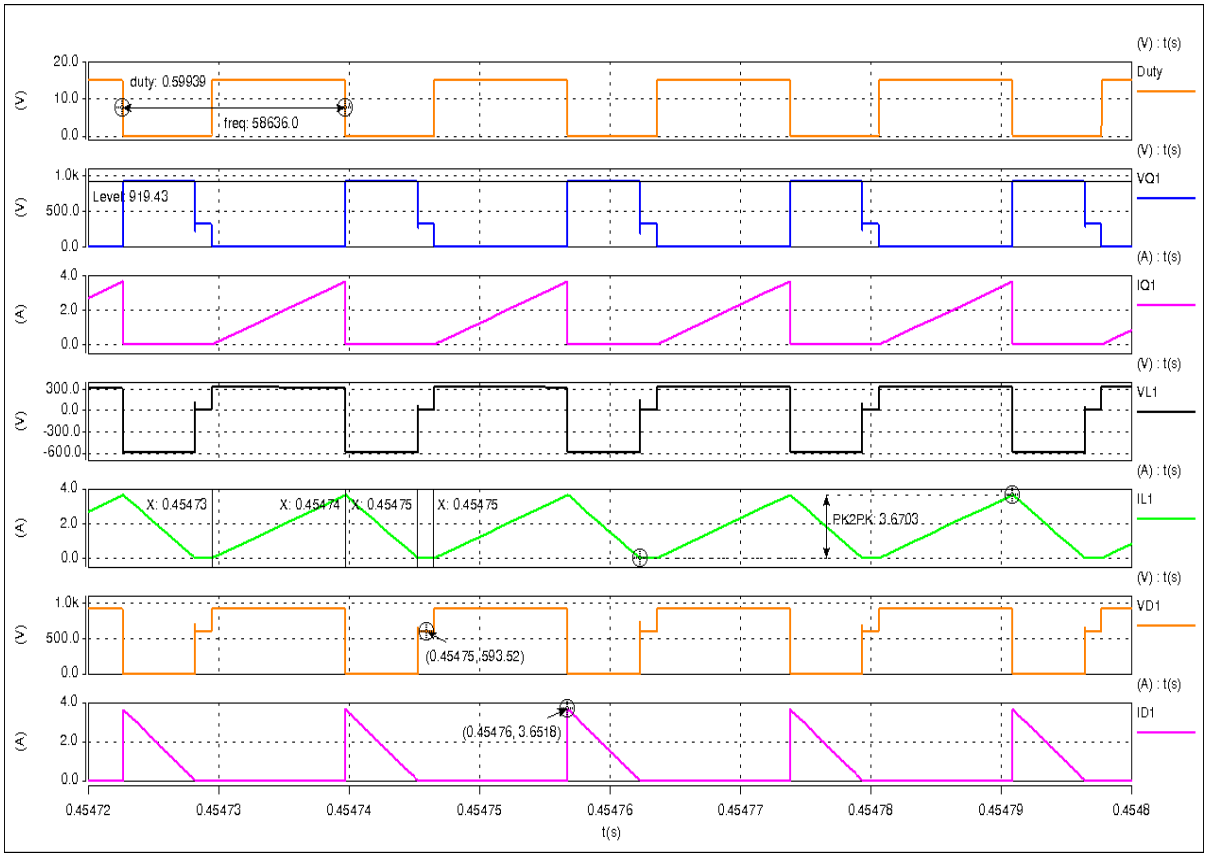


Figure 5-20 Key steady-state SABER simulated waveforms of the DCM buck boost converter

Figure 5-21 shows waveforms of V_{rec}, I_{L_1}, V_{bus} and I_{bus} over one and a half line cycles. The energy transfer imbalance between input and output of the PFC stage, results in a phase shift between $\hat{V}_{rec}$ and $\hat{V}_{bus}$. As the buck boost is operating in DCM, I_{L_1} is proportional to V_{rec} and is a clear haversine waveform, indicating near unity power factor and low harmonic current content.

Figure 5-21 also shows the twice mains frequency voltage ripple superimposed on V_{bus}. The amplitude of this ac oscillation, $\tilde{V}_{bus}$, at twice the line frequency, corresponds to the calculated results in Table 5-7. At lower power loads the amplitude of $\tilde{V}_{bus}$ decreases.

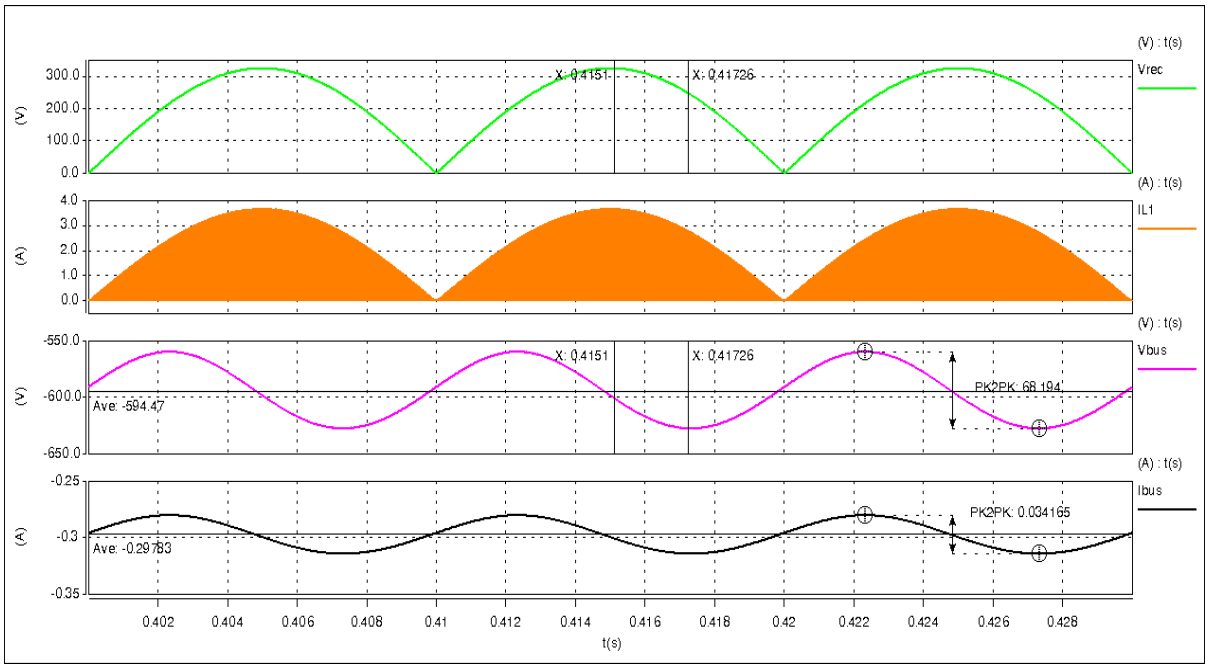


Figure 5-21 Input current and voltage SABER simulated waveforms of the DCM buck boost converter

Table 5-8 Comparison of key calculated and simulated

Parameter	Calculated	Simulated	Unit
V_s	230	230	V_{rms}
f_{line}	50	50	Hz
f_{sw}	60	58.6	kHz
D	0.60	0.59	-
$\hat{V}_{L_1}$	325	322	V
$\hat{V}_{Q_1} = \hat{V}_{D_1}$	930	930	V
$\hat{I}_{L_1} = \hat{I}_{Q_1} = \hat{I}_{D_1}$	3.65	3.65	A
$nT_{sw} \rightarrow t_{n1}$	10.10	10.17	μs
$t_{n1} \rightarrow t_{n2}$	5.48	5.36	μs
$t_{n2} \rightarrow (n+1)T_{sw}$	1.090	1.08	μs
V_{bus}	600	601	V_{rms}
$\tilde{V}_{bus}$ (at $2\times f_{line}$)	68	68.2	V
$\tilde{V}_{bus,\,fsw}$	0.60	0.58	V
I_{bus}	0.30	0.29	A_{rms}

5.11 Power Factor Correction Converter Prototype Design

This section details the prototype PFC converter design, showing the operational parameters and expected performance. Front end EMC filters are discussed, and designed.

5.11.1 Design Specifications

To summarise the previous design sections, Table 5-9 shows the specifications of the power factor correction stage, with component values of $L_1 = 900\ \mu H$ and $C_1 = 14.1\ uF$ **.**

Table 5-9 PFC converter specification

Description		Value	Unit
Input Voltage	V_s	230 +10, -6%	V_{rms}
Max Input Current	I_s	1.0	A_{rms}
Output Voltage	V_{bus}	600	V
Output Voltage Ripple	$\tilde{V}_{bus}$	0.6 at f_{sw} 69 at f_{line}	V
Output Current	I_{bus}	0.3	A
Line Operating Frequency	f_{line}	47-63	Hz
Converter Switching Frequency	f_{sw}	60	kHz
Output Power Range	P_{out}	60-180	W
Efficiency	η_{PFC}	90 % @180 W	
Inrush Current Protection	-	Varistor	
Power Factor Correction	PFC	<0.98	
Total Harmonic Distortion	THD	4 %	

5.11.2 EMC Filter

Generally all switching converters have a filter stage at the input to minimise the injection of high frequency current harmonics into the supply and protect against spurious electromagnetic interference generated by other equipment. Regulations such as [140] and [141] limit injected current amplitudes to values typically 40 – 80 dB less than peak 50 Hz current over a frequency range typically 150 kHz to 30 MHz. Approaches taken to limit EMC emissions and to limit converter susceptibility take numerous guises. Differential mode filters limit harmonics generated by the power converter topology between line and neutral. Common mode filters attenuate the currents flowing through parasitic capacitances between sources of high dv/dt and earth chassis.

EMC is well understood and the filter stage will have little impact on the performance of the control loop. Therefore the EMC filter is loosely designed to provide token EMC attenuation of high frequency current harmonics. A SABER simulation of the input EMC filter, see Figure 5-22, was conducted in order to provide an approximate value of the harmonic current attenuation. Accurate experimental verification was not performed as suitable laboratory equipment such as a Line Impedance Stabilization Network, LISN, and a Spectrum Analyser were not available to optimise the EMC filter and verify design.

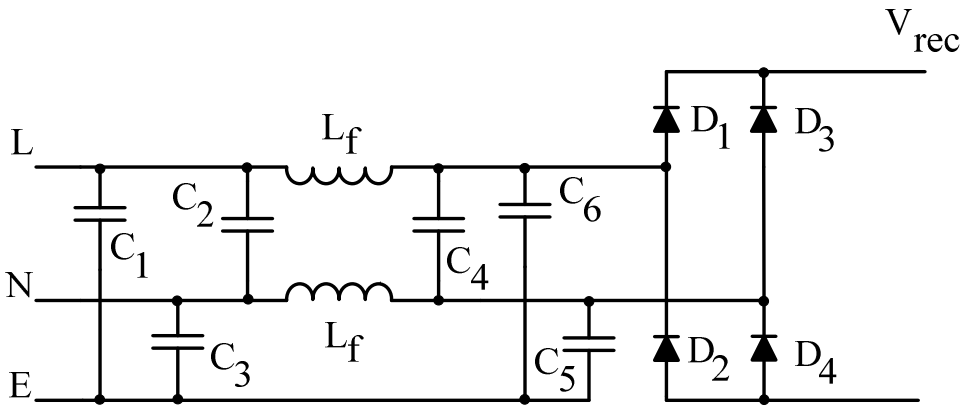


Figure 5-22 EMC filter for PFC

The π-filter consisting of 'X-type' capacitors C_2 and C_4, and inductance L_f attenuates differential mode currents. Capacitors C_1, C_3, C_5 and C_6 are all 'Y-type' capacitors and provide a path to earth for the common mode currents.

5.12 Summary

This chapter has presented the requirements and issues of developing a power factor correction converter for driving HP LEDs. With these issues clearly defined a suitable power factor correction stage is identified from the converter approaches detailed in Chapter 1, that can significantly boost the output voltage with respect to the line voltage. This requirement is due to the limited output capacitance of the metal film capacitors implemented in this PFC, as electrolytic capacitors, despite their high capacitance, lack the useful operating lifetimes needed for this application. A brief description of the operation of the steady-state performance of the PFC is characterised along with the design procedure, fundamental design equations, magnetic design and expected loss analysis of all devices.

Analysis of this approach reveals that due to the lack of any significant output capacitance of the PFC stage, a large voltage ripple appears at the converter output that has the ability to draw significant input harmonic currents from the supply if the correct converter control approach is not adopted.

Finally, SABER switching simulations are shown to validate the theoretical design.

6 HP LED Power Factor Correction Control Stage Design

6.1 Introduction

This chapter discusses the issues and control requirements of the HP LED power factor corrector converter controller. A suitable approach is identified from the methods shortlisted in Chapter 1. The principles of operation are briefly reviewed and the design of the control loop is conducted. MATLAB and SABER simulations confirm the operation, stability and predicted performance of the loop.

6.2 Identification of Control Approach

Section 1.2.5 reviews power factor correction control methods for CCM and DCM converters. As the buck-boost PFC converter is operating in DCM, commonly implemented current mode approaches, average and peak control, are not necessary to perform this task.

The simplest approach to DCM PFC control summarised in section 1.2.5, is the single loop voltage mode control. The control loop needs only to regulate the DC bus voltage and power throughput. Yet this approach makes the assumption that the output voltage ripple of the PFC is negligible. This case is not applicable here however, since the use of metal film capacitors results in a low capacitance and therefore the PFC output bus voltage has a high ripple component at the 2^{nd} harmonic of the mains supply.

To accommodate this ripple, the functionality of the buck boost DCM voltage loop controller needs to be addressed. If the voltage control loop was designed for a fast transient response, the controller would constantly attempt to correct the voltage ripple, causing 2^{nd} harmonic input current flow. Likewise, if the control compensator bandwidth was limited to reject twice mains ripple frequency, the transient response of the closed loop system would be slow, with possible loss of output voltage regulation and even converter failure under line and load condition changes.

Numerous voltage control loop methods to accommodate this ripple with varying degrees of success, are detailed in section 1.2.5. The notch filter method [86] is the most logical approach as the tuned filter would reject the twice mains ripple frequency, allowing only the high frequency components of the output voltage to be compensated. In order to

achieve good results, the filter would require a high Q_o factor with exact peak tuning, otherwise the performance of the filter would be compromised. As the mains frequency is not always at 50 Hz due to line loading conditions, frequency tracking methods would need to be employed to ensure accurate filtering. This approach requires high tolerance components and adds unnecessary expense.

Other solutions proposed are to ‘sample and hold’ the sensed output voltage [86]. Despite effectively eliminating the voltage ripple, should the converter be subject to transient load or line conditions between sampling periods, the control loop will not respond until the next sampling period, possibly subjecting converter components to high voltage or current spikes.

The most suitable approach to limiting the response is regulation band control [86, 142, 143]. This method can accommodate the voltage ripple and minimise converter instability whilst maintaining a fast transient response to line/load perturbations. Figure 6-1 shows a practical approach for this controller. Components A_1 and A_2 are comparators, A_3 and A_4 are operational amplifiers. This circuit carries out the following functions. Output voltage, V_{bus}, is attenuated by resistors R_a, R_b and R_c and sensed by comparators A_1 and A_2. The value of R_b determines the regulation band. If V_{bus} lies within the regulation band then D_a and D_b block the outputs from A_1 or A_2, and K remains unchanged. If the sensed output voltage leaves the regulation band due to line or load perturbations, then either comparator A_1 or A_2 will generate an output voltage which passes by the appropriate diode and is integrated by the compensator, comprising components A_3, R_d, R_f and C_f.

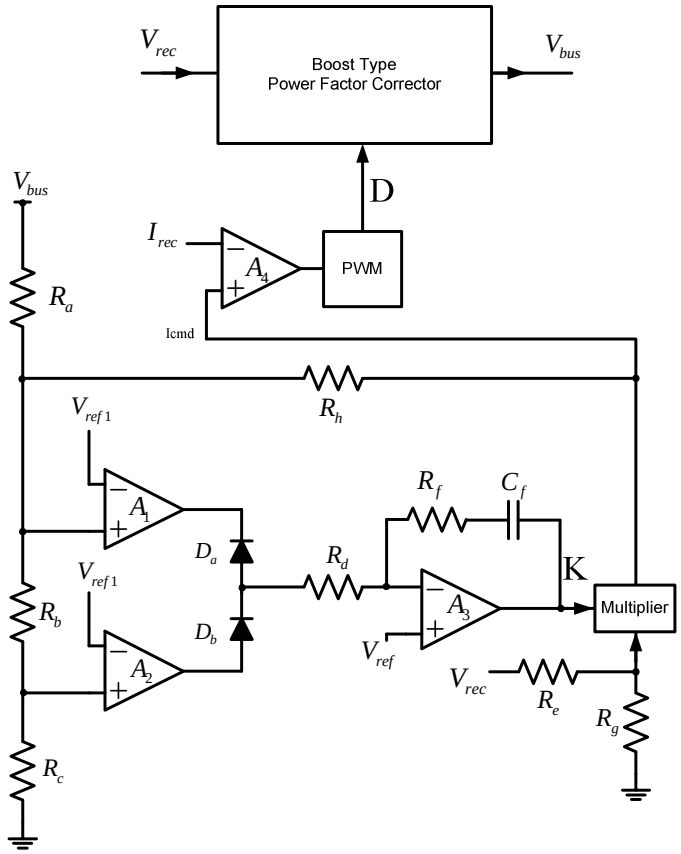


Figure 6-1 Regulation band control block diagram [86]

The output of A_3, the voltage K, is multiplied with the attenuated V_{rec} signal and the resulting output is compared with the sensed input rectified current, I_{rec}, in A_4 to produce an error voltage for the PWM stage, which in turn generates the duty ratio, D. As there is a multiplication between K and the V_{rec} signal in the feedback loop, R_h is used to optimise the transient response [143].

By implementing regulation band control with A_1 and A_2 at the input to the integrating compensator A_3, it is ensured that A_3 does not respond to voltage perturbations within the preset dead band, and a fast voltage control response can be achieved with low line current harmonics.

The stability aspects of this control approach fall into three parts; firstly the setting of the upper and lower limits of the regulation band. The band needs to be large enough to include the maximum expected V_{bus} ripple. If the regulation band is too narrow to accommodate the ripple, K will vary due to the normal output ripple, and cause distortion of

the input line current. Conversely, if the regulation band is too large, the output voltage regulation will be loosely coupled and over and under voltages may occur, compromising converter integrity.

Secondly, the response of the controller when the regulation band is exceeded by the output voltage is critical. Over or undershoot of the output bus voltage may cause the converter to operate outside its intended region of operation, possibly compromising the withstand voltages of components connected to V_{bus}. Thirdly a stable value of K is needed to maintain the output voltage within the limits during steady state.

The author has modified the proposed control method to enable it to operate in DCM with a buck-boost converter. The current sense loop is unnecessary when the power stage is operating in this mode. The author's improved controller is shown in Figure 6-2, in which the regulation band method only has to regulate V_{bus} .Thus the multiplier, V_{rec} signal, R_h and A_4 in Figure 6-1 are not required.

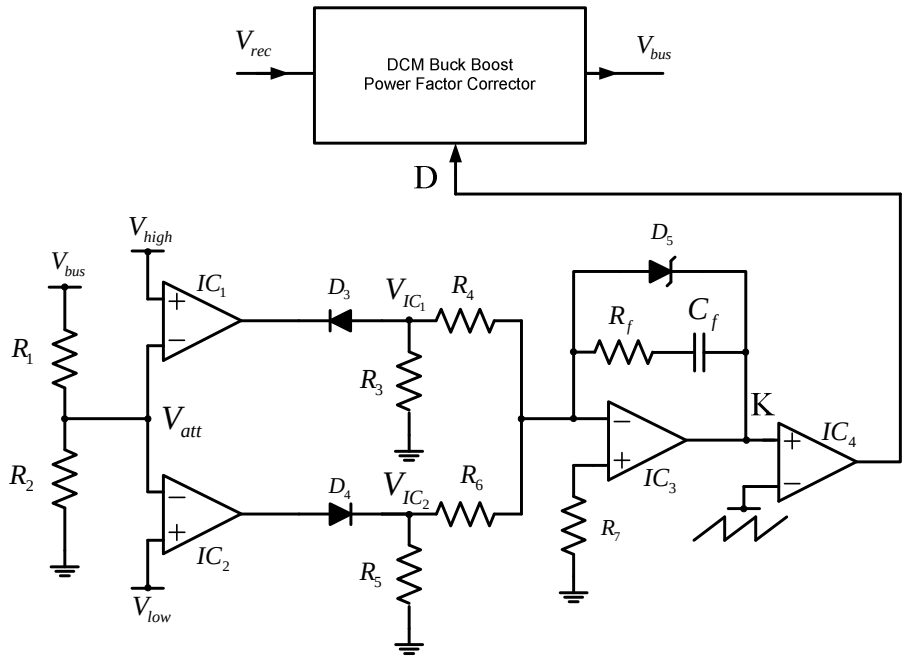


Figure 6-2 Modified regulation band control for DCM operation

6.3 Principles of Operation

Figure 6-2 shows a simplified version of the modified regulation band control for the DCM buck boost converter. Full schematic diagrams are given in Appendix E. Operation of the regulation band voltage controller is similar to the previous approach described earlier. The operation of this control loop is as follows.

The output voltage, V_{bus}, is attenuated by resistors R_1 and R_2, and the signal is sensed by the regulation band comparators IC_1 and IC_2. If the attenuated V_{bus} signal, V_{att}, is between reference voltages V_{high} and V_{low}, see Figure 6-3, then the outputs of IC_1 and IC_2 are blocked by D_3 and D_4 and K remains unaltered. During this operational state, the controller is essentially open loop, as there is no continuous feedback loop.

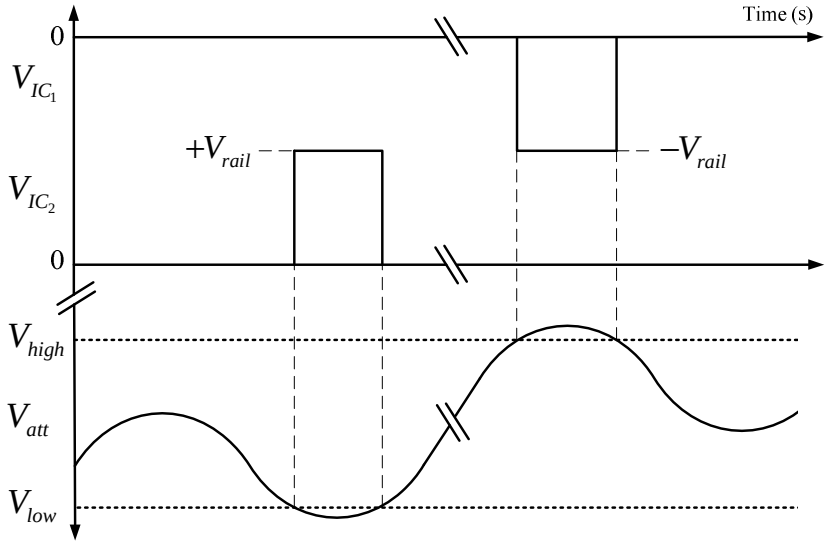


Figure 6-3 Buck boost output voltage regulation band limits

If V_{att} exceeds the limit V_{high} then IC_1 will generate a negative rail voltage which is passed by D_3 to the input of IC_3. If V_{att} goes below the limit V_{low} then IC_2 will generate a positive rail voltage which is passed by D_4 to the input of IC_3. These signals are integrated by the operational amplifier IC_3 to produce an updated value of K. The output of IC_3 is compared with a reference sawtooth voltage waveform, at switching frequency, f_{sw}, by IC_4 to produce the required duty ratio, D. The output signal, D, is now fed directly to the gate drive circuit of MOSFET Q_1 in the power factor corrector.

Zener diode, D_5, in the feedback loop of the compensator limits the maximum and minimum voltage error signal K, which in turn limits the maximum and minimum duty ratio.

6.4 Design of Voltage Regulation Band Control

A block diagram of the DCM buck boost and the regulation control loop is shown in Figure 6-4. It consists of four linear time variant blocks; the voltage compensator, $G_c(s)$, the PWM stage, $G_{pwm}(s)$, the buck-boost power stage, $G_p(s)$ and the feedback attenuator $G_{K_A}(s)$. The final block in the diagram is the static nonlinearity, a relay with dead band (R), which represents the regulation band comparators.

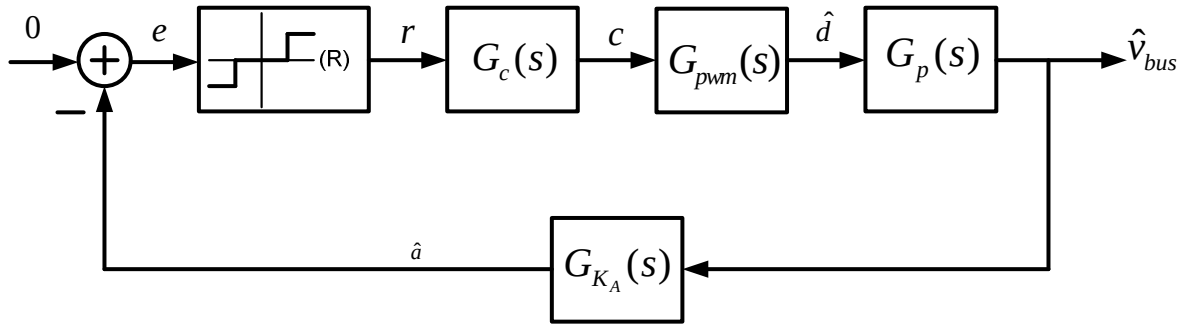


Figure 6-4 Control loop block diagram

A small signal analysis of the DCM buck boost converter conducted in [126] determines the control-to-output transfer function, $G_P(s)$ to be

$$G_P(s) = \frac{\hat{v}_{bus}}{\hat{d}}\bigg|_{\hat{v}_s=0} = \frac{G_{d0}}{1+\frac{s}{\omega_p}} \qquad \textbf{Eqn 6-1}$$

where

$$G_{d0} = \frac{V_{bus}}{D} \qquad \textbf{Eqn 6-2}$$

and

$$\omega_p = \frac{2}{R_L C_1} \qquad \textbf{Eqn 6-3}$$

where ω_p is the buck boost power stage pole, R_L is the equivalent converter load and C_1 is the output capacitance across V_{bus}. V_{bus} and D are the steady state output voltage and duty ratio respectively, and $\hat{v}_{bus}$, $\hat{d}$ and $\hat{v}_s$ are small ac perturbations about the quiescent points of V_{bus}, D and V_s.

The compensator, $G_C(s)$, in Figure 6-4 is a Proportional-Integral controller, PI. This compensator increases the low frequency gain, so that V_{bus} is well regulated and sets the open loop zero dB cross over frequency, f_c to be below the converter switching frequency, f_{sw}. The transfer function, $G_C(s)$ of this PI compensator is determined by

$$G_C(s) = G_{C\infty}\left(\frac{s+\omega_z}{s}\right) = -\frac{R_f}{R_x}\left(\frac{s+\dfrac{1}{R_f C_f}}{s}\right) \qquad \textbf{Eqn 6-4}$$

where $G_{C\infty}$ is the gain of the PI at high frequency and ω_z is the compensator zero determined by C_f and R_f in Figure 6-2. R_x is the value of the input resistor to IC_3, either R_4 or R_6 depending on whether limit V_{high} or V_{low} has been exceeded.

The PWM stage, $G_{pwm}(s)$, is considered linear, therefore the transfer function is

$$G_{pwm}(s) = \frac{1}{V_m} \qquad \textbf{Eqn 6-5}$$

where V_m is the peak to peak saw tooth voltage of the PWM comparator.

The attenuator, $G_{K_A}(s)$, transfer function is

$$G_{K_A}(s) = \frac{R_2}{R_1} \qquad \textbf{Eqn 6-6}$$

The first step of the control design is to determine the values of the voltage dead band limits V_{high} and V_{low}. Using **Eqn 5-17** the peak to peak voltage ripple of V_{bus} can be determined. Table 5-7 lists the steady state parameters of the DCM buck boost PFC operating in various modes. From this table, the worst case V_{bus} ripple is identified as $\tilde{V}_{bus}$ =68 V at 180 W output. The voltage dead band must not be smaller than the low frequency voltage ripple at full power. For practicality a 10 % margin has been added to account for component variability and drift.

The other factors determining control response require a more iterative process. Figure 6-4 can be consolidated and simplified to become Figure 6-5, by combining the transfer functions G_C, G_{pwm}, G_P and G_{K_A} to become the transfer function H(s), whilst the static nonlinearity remains as R. The transfer function of H(s) is

$$H(s) = G_C G_{pwm} G_P G_{K_A}(s) \qquad \textbf{Eqn 6-7}$$

The conventional approach of establishing a fast transient response and closed loop stability by methods of small signal modelling is detailed in [144, 145]. Unfortunately, this approach is not suitable for loops containing nonlinearities. The proposed method for achieving stability with a non linearity is based on the circle criterion [146, 147]. This approach provides a means for analysing nonlinear time-varying systems to obtain system stability.

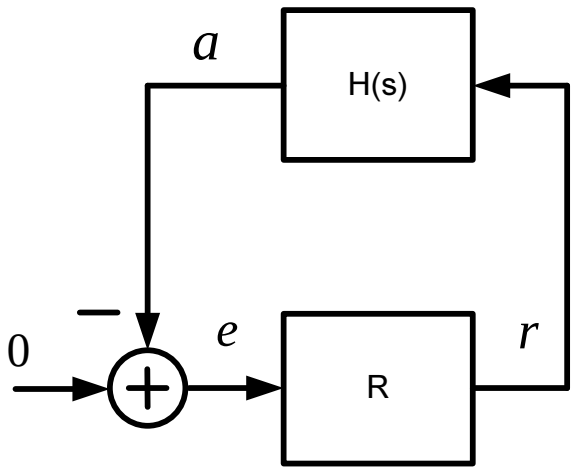


Figure 6-5 Simplified model of the buck boost and control

The conditions for stability must satisfy

$$\mathrm{Re}[1+zH(j\omega)]>0 \quad \forall\omega \qquad \textbf{Eqn 6-8}$$

where $z=\Delta r/\Delta\varepsilon$, the slope of the dead band relay seen in Figure 6-6 . The upper and lower voltage limits of the regulation zone are represented by ε and $-\varepsilon$ respectively, and the output signals of block R, are shown by r and $-r$.

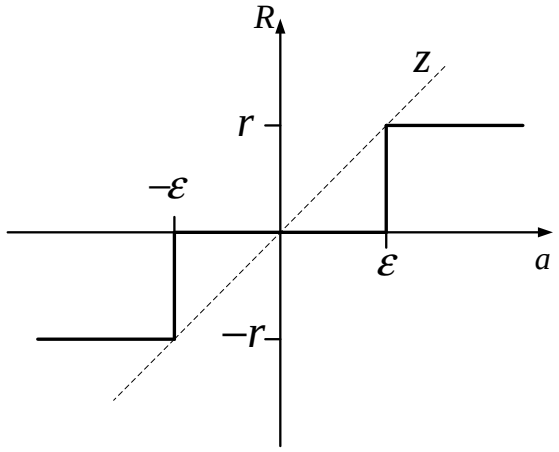


Figure 6-6 Operation of the relay with dead band

Subsequent Nyquist plots of $1+zH(j\omega)$ must remain in the positive sector of the real axis, Figure 6-7. The values r and $-r$ are determined by the output voltages of IC_1 and IC_2, and ε and $-\varepsilon$ are predetermined by the attenuator R_1 and R_2 and the reference values V_{high} and V_{low} in Figure 6-2.

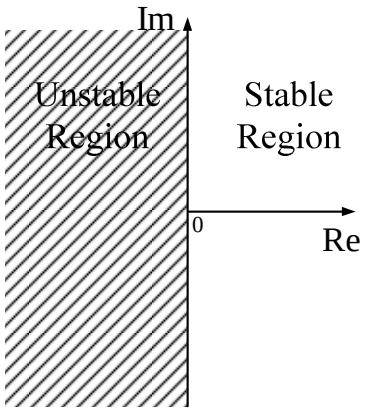
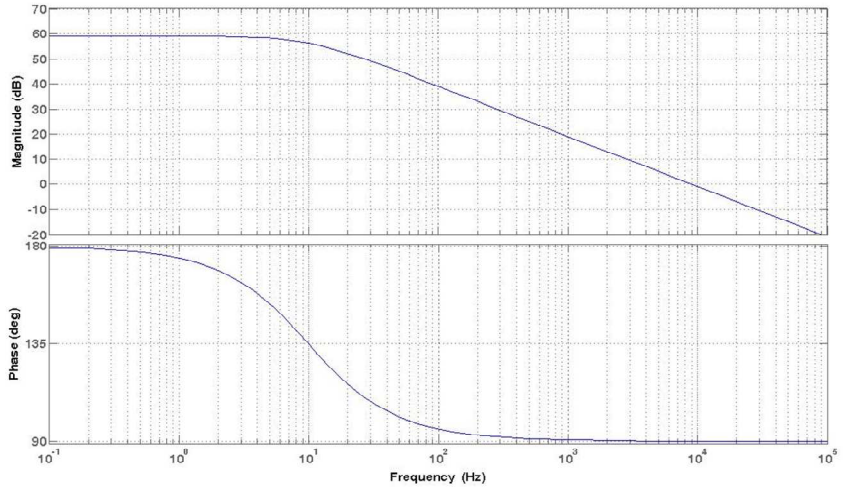


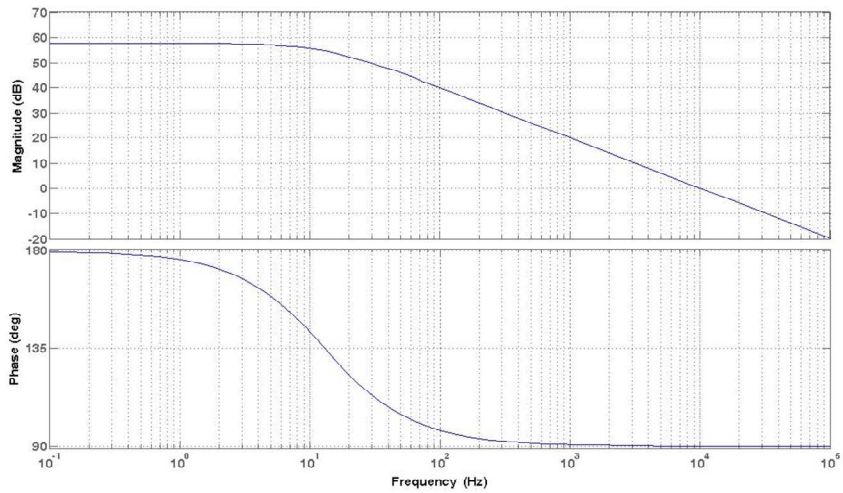
Figure 6-7 Circle criterion stability requirements

6.5 Open Loop Analysis

This section details the analysis of the open loop system of blocks **R** and $H(s)$ and analysis is conducted using MATLAB. Plots of the control to output transfer function of the DCM buck boost converter, the PWM stage, the attenuator, the gain of the voltage dead band relay and the PI voltage compensator are given. When operating in DCM, the duty ratio of the buck boost converter and therefore its bode plot is affected by the load. **Eqn 6-1** is plotted for a nominal input voltage, V_s= 230 V_{rms}, at either output voltage limit, -640 V and -560 V. The output power is varied from full power, 180 W, to minimum power, 60 W.

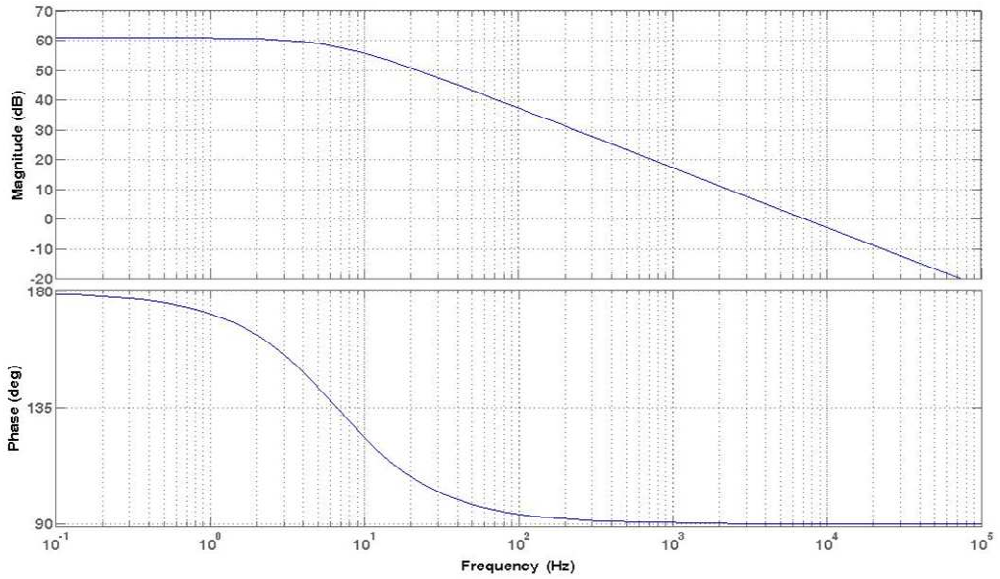


(a)

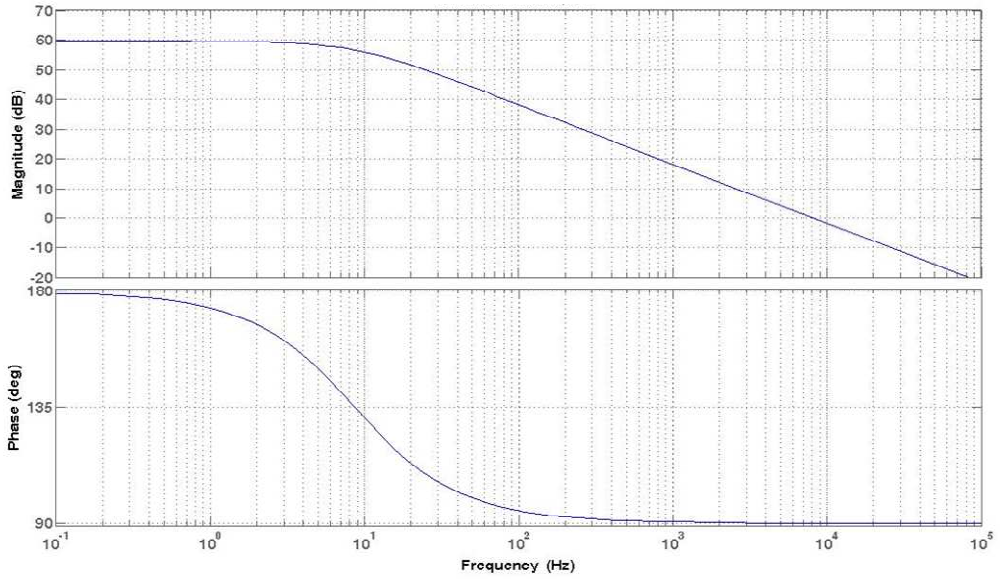


(b)

Figure 6-8 Control-to-output magnitude and phase plots of the buck-boost converter, V_s=230 V_{rms}, P_{out}=180 W, (a) V_{bus}= -640 V, (b) Vbus= -560 V

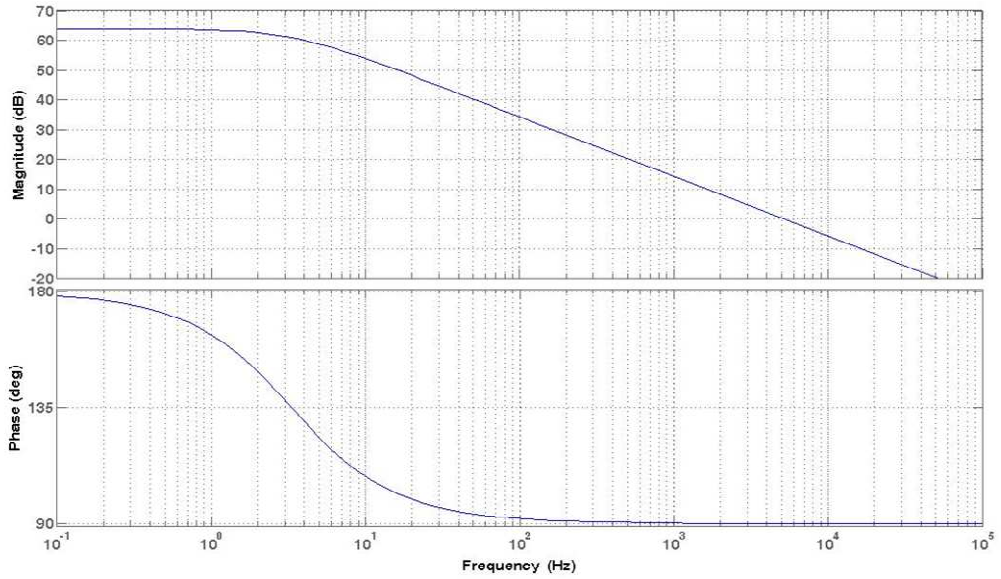


(a)

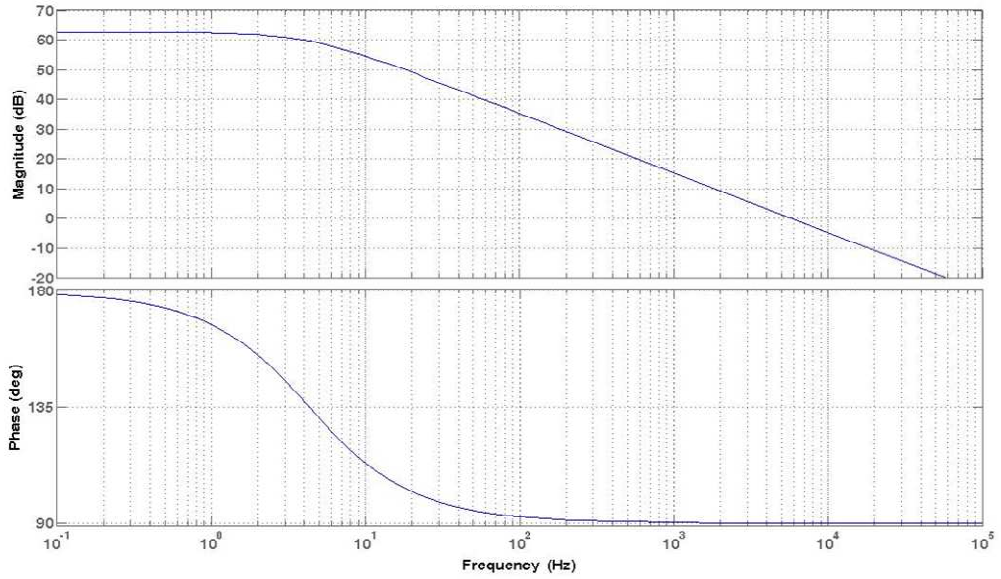


(b)

Figure 6-9 Control-to-output magnitude and phase plots of the buck boost converter, V_s=230 V_{rms}, P_{out}=120 W, (a) V_{bus}= -640 V, (b) Vbus= -560 V



(a)



(b)

Figure 6-10 Control-to-output magnitude and phase plots of the buck boost converter, V_s=230 V_{rms}, P_{out}=60 W, (a) V_{bus}= -640 V, (b) Vbus= -560 V

A summary of the key points of these plots is given in Table 6-1. With an increase of power output the low frequency gain decreases whilst the frequency of the pole and the zero dB cross over point increases. With these characteristics in mind, the frequency of the PI compensator zero is critical.

Table 6-1 Summary of control-to-output, $G_p(s)$, phase and gain bode plots at various loads

V_s (V_{rms})	V_{bus} (V)	P_{out} (W)	Gain @ low frequency (dB)	f_p (Hz)	f_c (kHz)
230	-640	180	59.1	9.92	9.03
230	-560	180	57.8	12.92	10.3
230	-640	120	60.9	6.60	6.96
230	-560	120	59.6	8.60	8.22
230	-640	60	63.9	3.30	5.77
230	-560	60	62.6	4.30	5.90

The magnitude and phase of the PWM stage, $G_{pwm}(s)$, are constant at -20 dB and zero degrees for all frequencies. The magnitude and phase of the attenuator stage, $G_{K_A}(s)$, are constant at -40 dB and zero degrees for all frequencies.

The voltage dead band relay, block R, is modelled at its maximum gain, i.e. when either limit V_{high} or V_{low} is exceeded by the attenuated V_{bus} voltage. From Figure 6-6, parameters 'r' and '-r', ± 12 V. The limits 'ε' and '$-\varepsilon$', are V_{high} and V_{low}, -5.6 V and -6.4 V. Therefore using $z = \Delta r / \Delta \varepsilon$, the magnitude and phase of the voltage dead band relay are given by 29.5 dB and zero degrees for all frequencies.

Now that transfer functions $G_p(s)$, $G_{pwm}(s)$, $G_{K_A}(s)$ and **R** have been defined, the PI compensator, $G_C(s)$, can be designed to ensure a stable closed loop system whilst achieving a fast response. The requirement for the open loop gain is that it should be high at low frequencies to minimise steady state error, the cross over frequency, f_c, should be approximately an order of magnitude below f_{sw}, and the magnitude gain plot should cross the zero dB axis with a slope of -20 dB per decade [45]. To achieve a high open loop gain cross over frequency, the gain of the PI needs to be high. The result of this is that when V_{bus} reaches V_{low}, the PI will compensate by decreasing its output, K, to momentarily stop the PWM stage switching. The input current, I_s, will be interrupted, possibly causing a current surge at the next MOSFET turn on and an increase in input current harmonics.

Using the MATLAB control toolbox SISOTOOL, the maximum gain of the compensator can be determined to ensure closed loop system stability whilst ensuring acceptable phase and gain margin of the open loop.

6.6 Proportional Integrator Compensator Design

This section shows the results of the empirical methods used to determine the position of the compensator zero and the respective gain using the MATLAB control toolbox SISOTOOL. Simulations show that placing the zero of the PI compensator at a slightly higher frequency than the pole of the buck boost power stage results in the real part of $1+zH(jw)$ crossing into the negative plane, thus not satisfying the Circle Criterion.

For Figure 6-8 to Figure 6-10, frequencies above f_p, the magnitude decays at – 20 dB/dec. In order to achieve an open loop zero dB crossover slope of -20 dB/dec, for block **R** and $H(s)$, the zero of the linear compensator needs to be situated at a lower frequency than the pole of the power stage, otherwise a -40 dB/dec slope would occur at the zero dB crossover point.

From Table 6-1, the lowest value of the control-to-output pole of the power stage is 3.3 Hz, therefore by ensuring the PI compensator zero frequency is below this value, the system stability can be assured for all operating conditions. A bode plot of the PI compensator is shown in Figure 6-11, where the zero is at 1.6 mHz, and the high frequency gain is 32 dB.

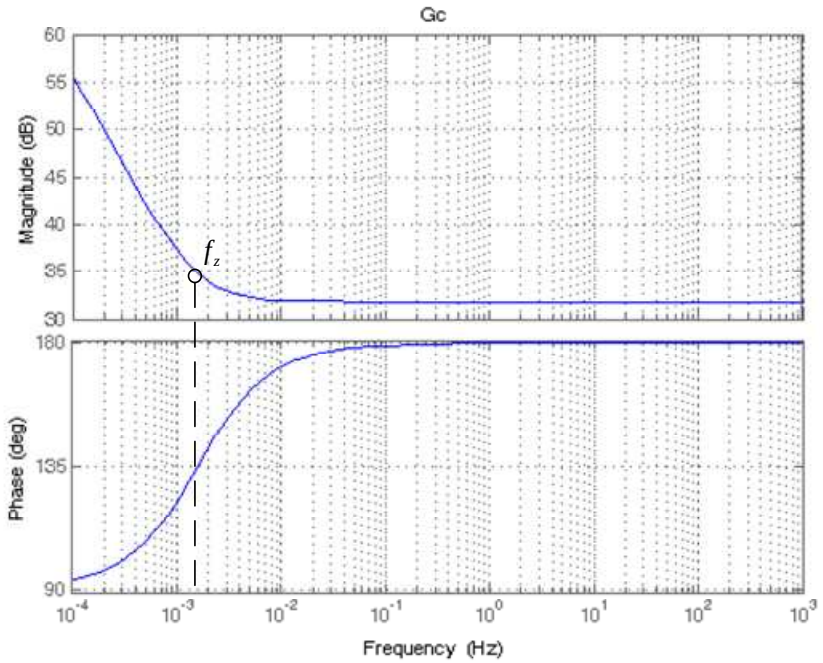


Figure 6-11 Bode plot of $G_C(s)$

The resulting transfer function of the linear compensator in Figure 6-11 is

$$G_C(s) = \frac{-39s - 0.39}{s} \qquad \textbf{Eqn 6-9}$$

6.7 Voltage Loop Response at Regulation Band Limits

As the control loop is effectively open when V_{bus} is within the voltage regulation band, the output is unregulated. Hence system stability and response is only of concern when V_{bus} exceeds the limits. Therefore the following analysis looks only at the stability occurring at these boundaries. Figure 6-12 (a) shows the magnitude and phase plots of $zH(s)$, where $z = \Delta r / \Delta \varepsilon$, at nominal V_s, an output power of 180 W and when the attenuated V_{bus} signal, V_{att}, is more negative than V_{low}. The compensator zero, f_z, is at a lower frequency than the power stage single pole, f_p, allowing for a –20 dB/dec slope at the zero dB cross over frequency, and a 90° phase lead. Figure 6-12 (b) is the Nyquist plot of $1 + zH(j\omega)$ at the same input and output conditions**.** It can be seen that the Circle Criterion is satisfied for stability, as

the entire plot remains in the positive half of the real axis. For clarity, Figure 6-12 (c) is a close up of the real axis of Figure 6-12 (b).

Figure 6-13 (a) shows the magnitude and phase plots of $zH(s)$, at nominal V_s, an output power of 180 W and when V_{att} is more positive than V_{high}. As before, the compensator zero, f_z, is below the power stage single pole, f_p, allowing for a –20 dB/dec slope at the zero dB cross over frequency, and a 90° phase lead. Figure 6-13 (b) is the Nyquist plot of $1+zH(j\omega)$ at the same input and output conditions**.** It can be seen that the Circle Criterion is satisfied for stability, as the entire plot remains in the positive portion of the real axis. For clarity, Figure 6-13 (c) is a close up of the real axis of Figure 6-13 (b).

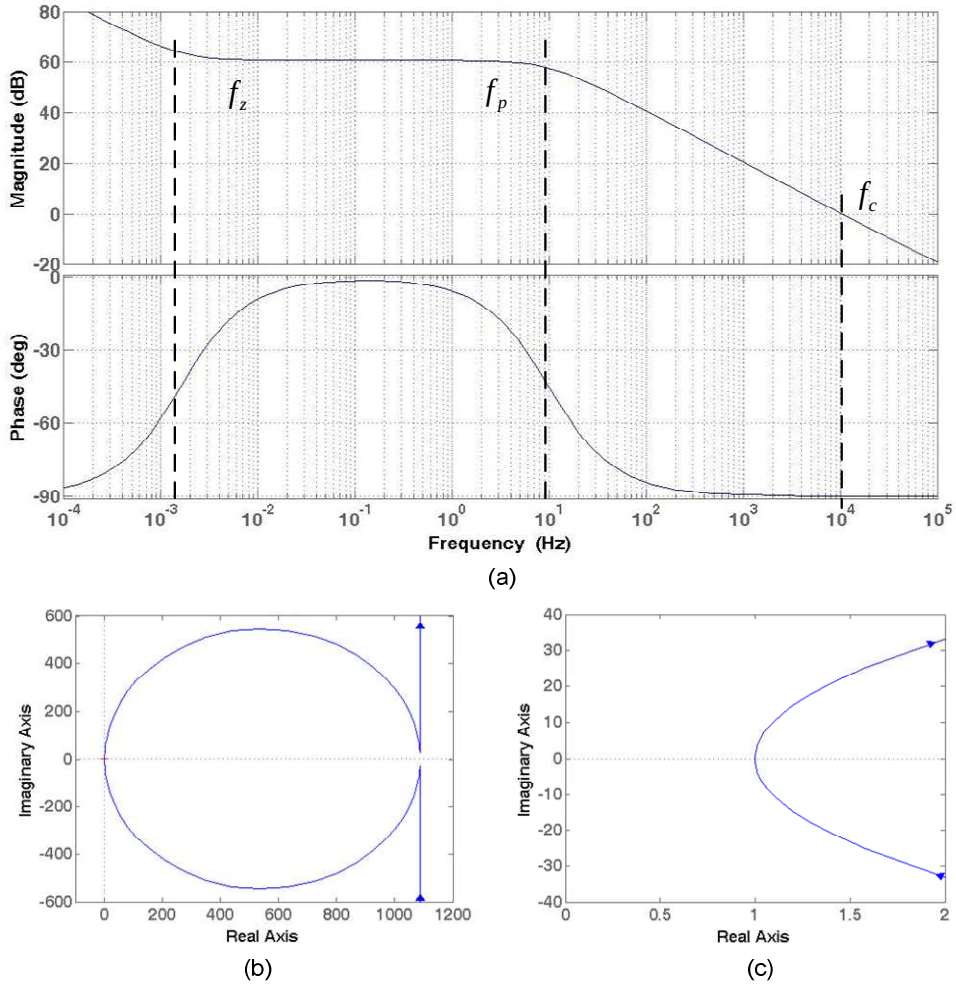


Figure 6-12 (a) Magnitude and phase of $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms},V_{bus}= -640 V and P_{out}= 180 W.

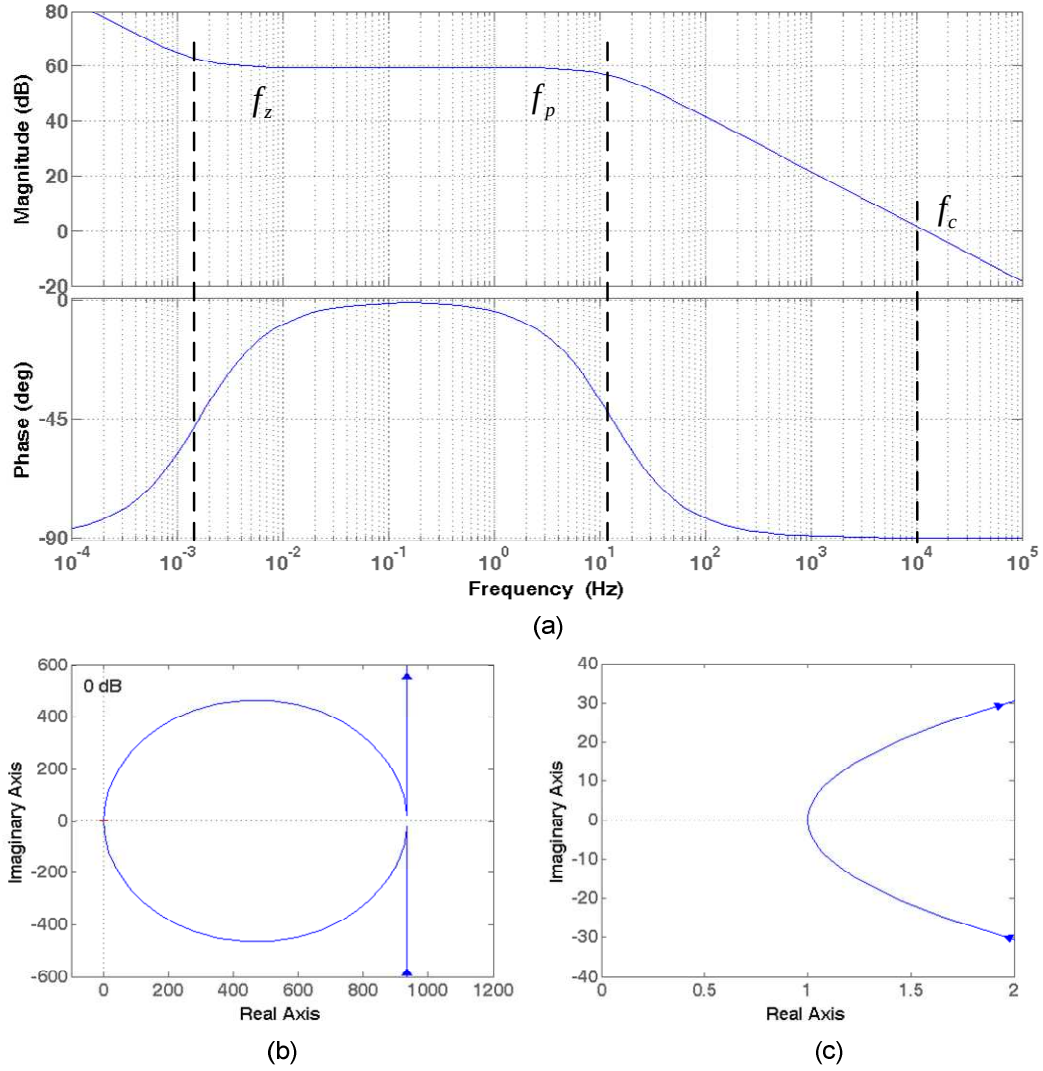


Figure 6-13 (a) Magnitude and phase of $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms}, V_{bus}= -560 V and P_{out}= 180 W

Figure 6-14 and Figure 6-15 again plot the magnitude and phase diagrams of $zH(s)$ and a Nyquist plot of $1+zH(j\omega)$ for a nominal V_s of 230 V_{rms}, an output voltage exceeding V_{high} and V_{low}, however the output power is reduced to 120 W.

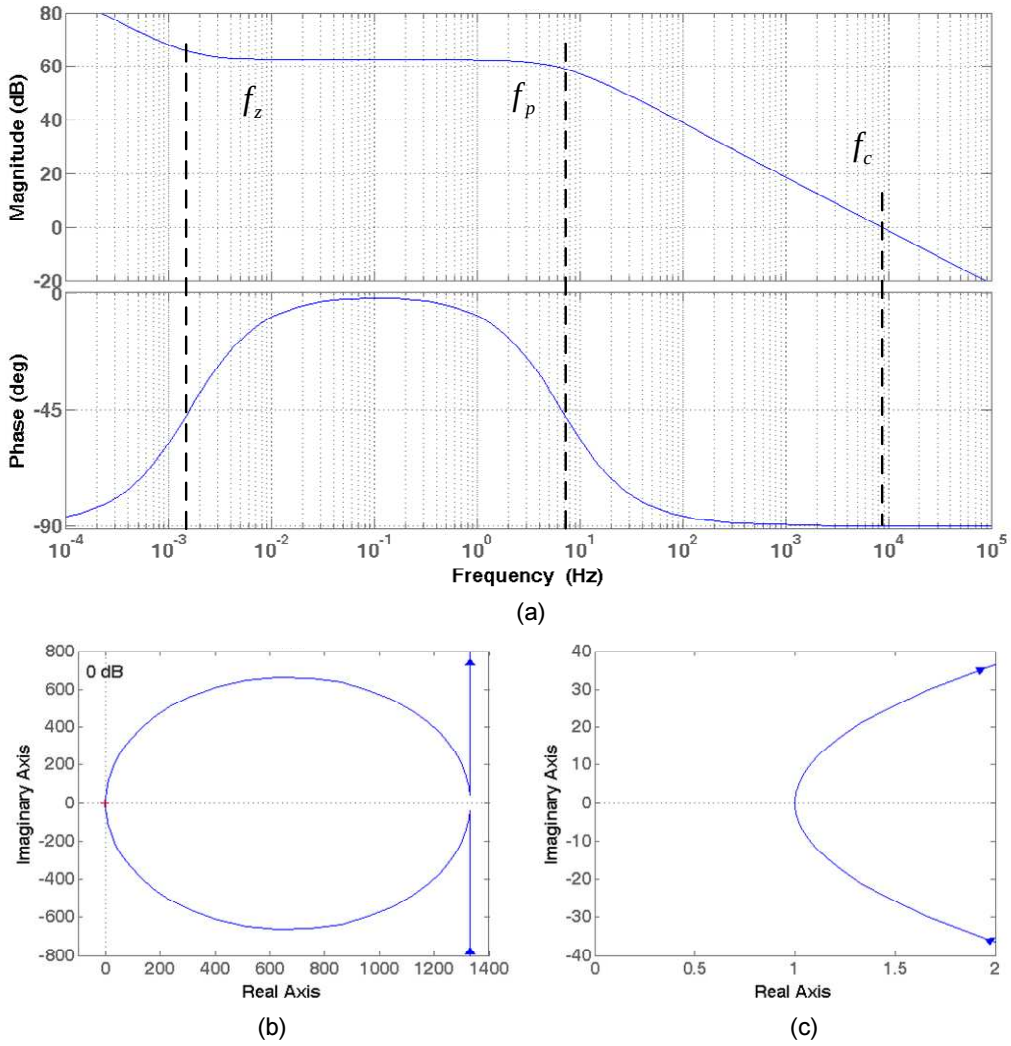


Figure 6-14 (a) Magnitude and phase of blocks $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms}, V_{bus}= -640 V and P_{out}= 120 W

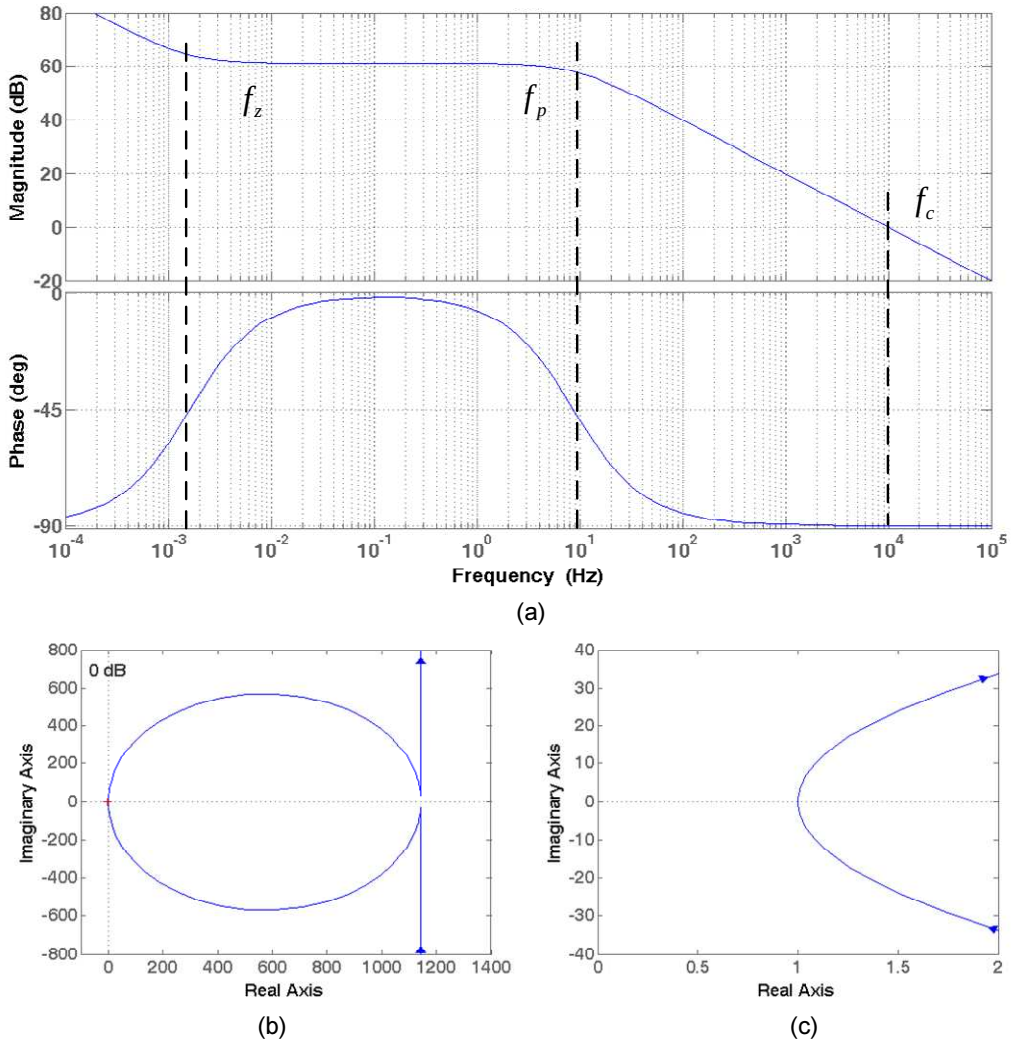


Figure 6-15 (a) Magnitude and phase of $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms}, V_{bus}= -560 V and P_{out}= 120 W

Finally Figure 6-16 and Figure 6-17 plot the magnitude and phase diagrams of $zH(s)$ and a Nyquist plot of $1+zH(j\omega)$ for a nominal V_s of 230 V_{rms}, an output voltage exceeding V_{high} and V_{low}, however the output power is reduced to 60 W.

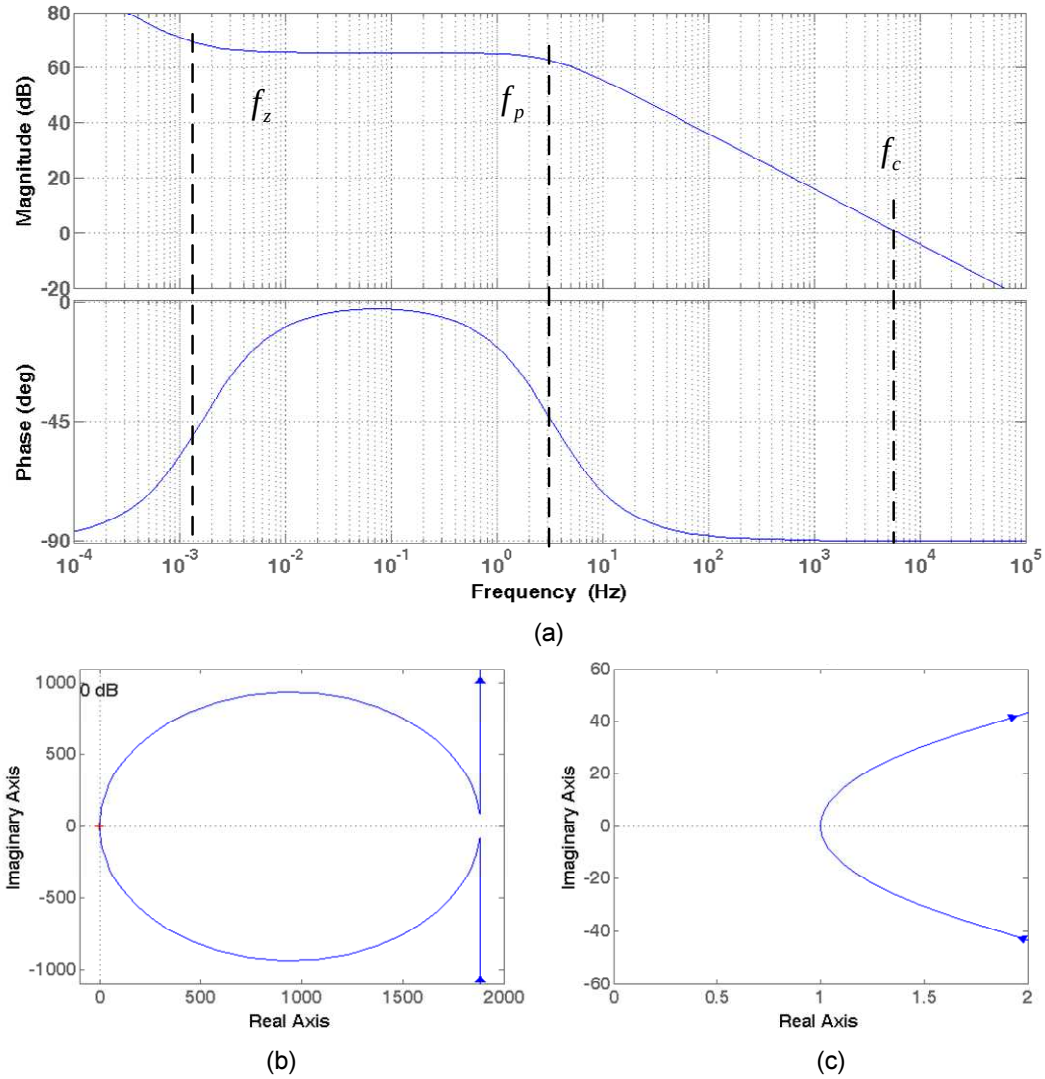


Figure 6-16 (a) Magnitude and phase of $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms}, V_{bus}= -640 V and P_{out}= 60 W

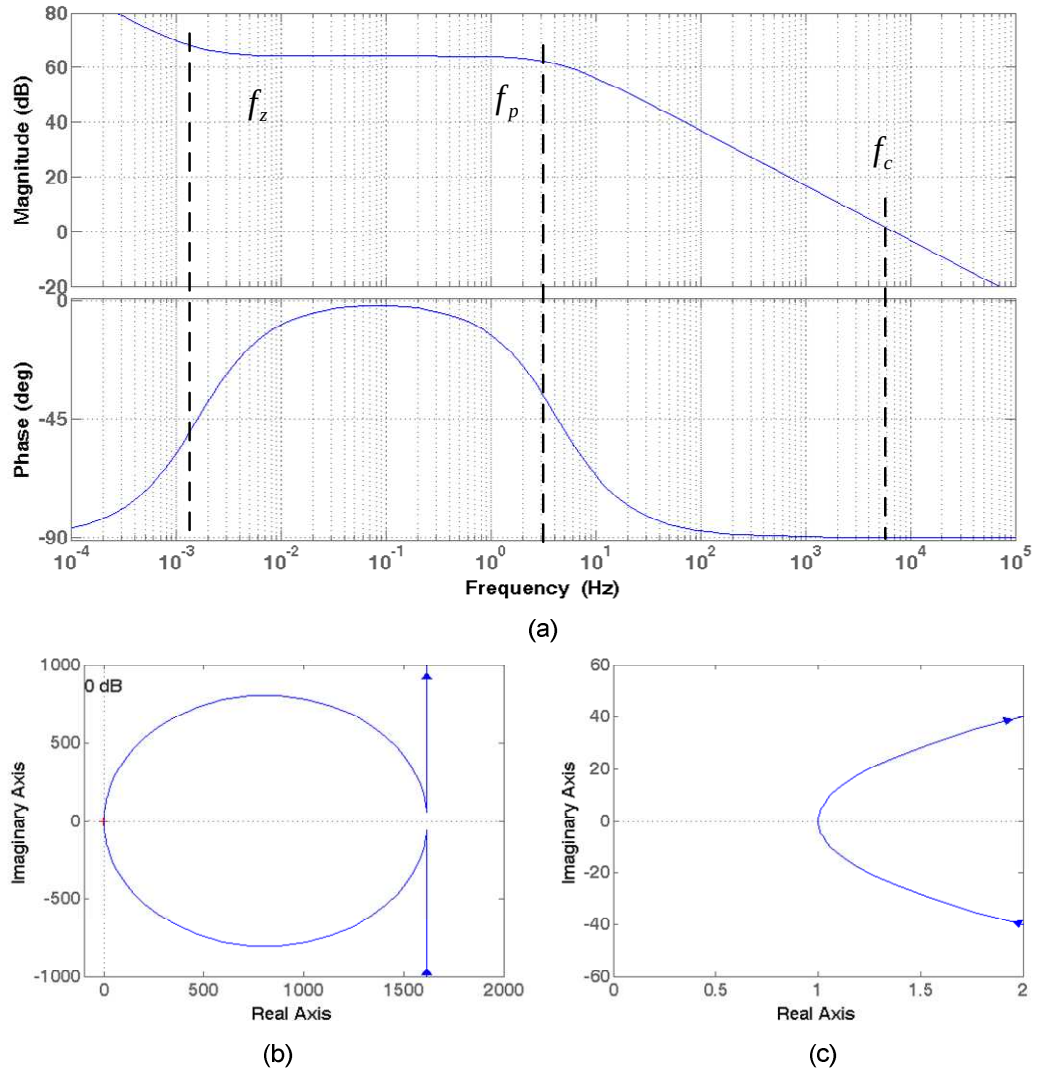


Figure 6-17 (a) Magnitude and phase of blocks $H(s)$ and **R**, (b) & (c) plots of $1+zH(j\omega)$ for V_s= 230 V_{rms}, V_{bus}= -560 V and P_{out}= 60 W

Table 6-2 summarises the frequencies of the PI compensator zero, and the power stage pole at a fixed V_s but with varying values of P_{out} and V_{bus}. It can be seen, that under the various line and load conditions, f_p, f_c and the gain change. The tables shows that the cross over frequency of $H(s)$ and **R** varies from 5.22 kHz at (V_s=230 V, V_{bus}=-640 V, P_{out}=60 W), to a maximum of 10.3 kHz at (V_s=230 V, V_{bus}= -640 V, P_{out}= 180 W).

A final point of observation to be made of Table 6-2, is the consistent phase margin of 90^o. As f_z is below f_p, the 90^o phase lag of f_p dominates the phase at f_c, thus ensuring

stability of the open loop system. Generally a phase margin of 45^o to 60^o is used in a control system for a fast response [45], however this is not achievable in this instance. From [148] a phase margin of 90^o relates to a damping ratio of 3.0. This ensures that there is no overshoot or oscillation of the open loop system to a step load or input voltage change.

Table 6-2 Summary of Figure 6-12 to Figure 6-17

V_s (V)	V_{bus} (V)	P_{out} (W)	f_z (mHz)	f_p (Hz)	f_c (kHz)	Gain (dB)	Phase Margin (^{o})
230	-640	180	1.6	9.92	10.3	60.7	90
230	-560	180	1.6	12.92	10.1	57.8	90
230	-640	120	1.6	6.60	8.67	62.5	90
230	-560	120	1.6	8.60	9.59	61.2	90
230	-640	60	1.6	3.30	5.22	63.8	90
230	-560	60	1.6	4.30	6.83	64.2	90

6.8 SABER Simulation PI Compensator Design

From the results detailed previously for the SISOTOOL simulated PI compensator, the experimental component values for compensator A_3 were found to be **R_1= 990 kΩ**, **R_2= 10 kΩ**, **$R_{3,4,5,6}$= 51 kΩ**, **R_7= 102 kΩ**, **R_f= 20 kΩ**, **C_f= 0.5 μF** and **D_5= 7.8 V** zener.

6.9 SABER Simulation Verification of Control Loop

The results of the MATLAB control analysis were verified with a SABER simulation. The control block, in Figure 6-18, consists of the converter output feedback attenuator, and an extra operational amplifier acting as a buffer to avoid loading the resistor chain, the non linear relay with voltage dead band, the PI voltage compensator, a saw tooth waveform generator, the PWM stage comparator and a gate drive interface. The feedback attenuator reduces V_{bus} by a factor of 100. Regulation dead band limits V_{high} and V_{low} are set by ideal voltage sources of -5.6 V and – 6.4 V respectively. A fixed 60 kHz saw tooth waveform is generated by an LM555 timer and fed to the PWM stage comparator to be compared with the output of the PI compensator.

The following simulations demonstrate the dynamic performance of the DCM buck-boost converter with the proposed voltage regulation band control. The results presented are

all for a nominal input voltage V_s=230 V_{rms} with the output power, P_{out}, varying in a stepped manner. Ideal operational amplifiers were used in the simulation, thus there is no offset voltage at the input of the PI compensator to introduce a positive or negative drift in K, hence making D vary and V_{bus} drift between voltage limits.

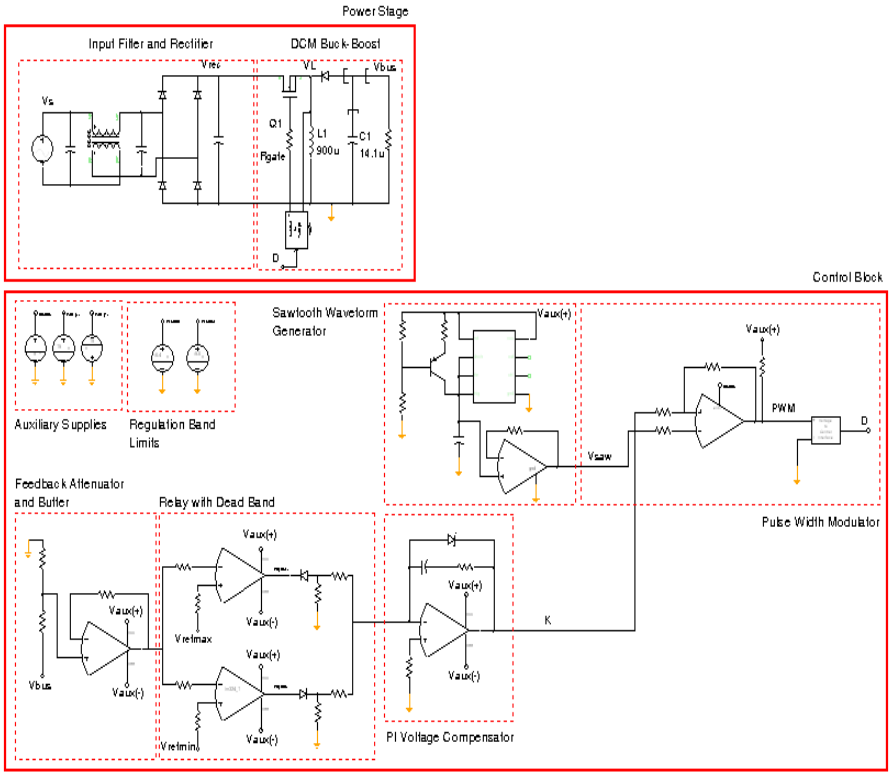


Figure 6-18 SABER simulation schematic of control loop and PFC converter

The following plots, Figure 6-19 to Figure 6-21, show the converter control loop response being subjected to a step load change of 0 W to 60 W, 0 W to 120 W and 0 W to 180 W. At 80.0 ms there is no load across the output capacitor, C_1, and K is low to prevent MOSFET switching and charging of C_1. At 0.1 s the step load occurs, causing the voltage across C_1 to reduce. The control loop does not respond until V_{bus} reaches the upper voltage limit, - 560 V. The capacitor C_1 is the only source of energy to the load before the upper voltage limit is reached. The control loop only regulates V_{bus} when the -560 V limit is exceeded, as is seen by an increase in K at around 0.11 s. The response of K in these figures is such that it does not overcompensate V_{bus}, due to the 90^o phase margin, forcing it towards the lower voltage boundary, -640 V, where the control loop again would have to correct, causing further oscillations.

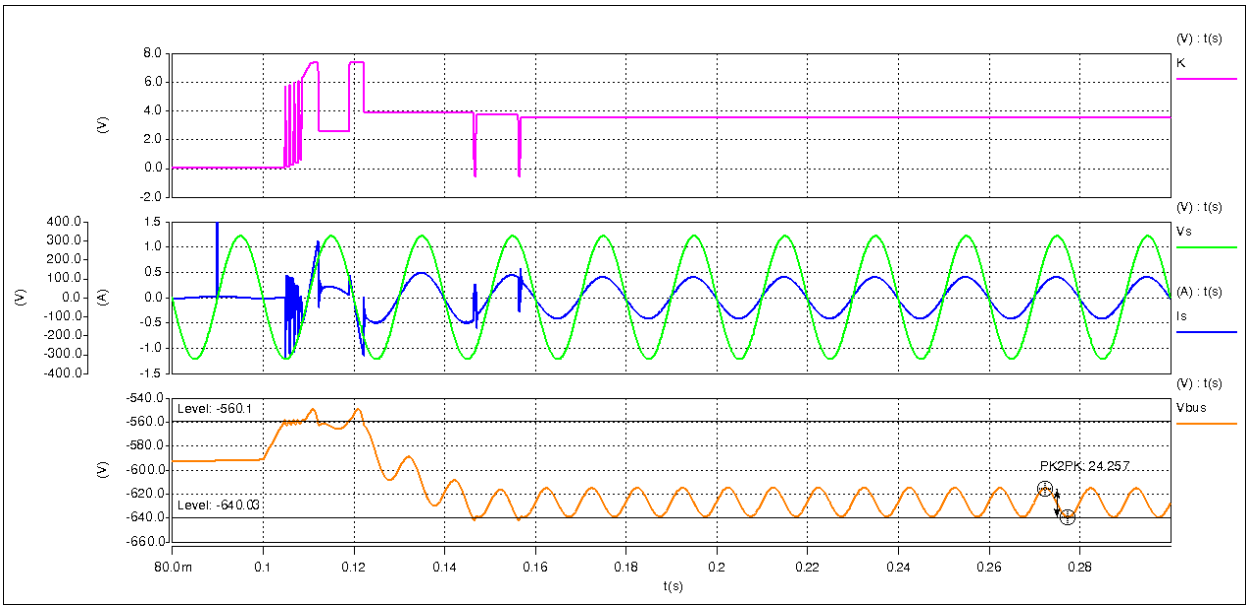


Figure 6-19 SABER V_{bus} response to step load 0 W to 60 W

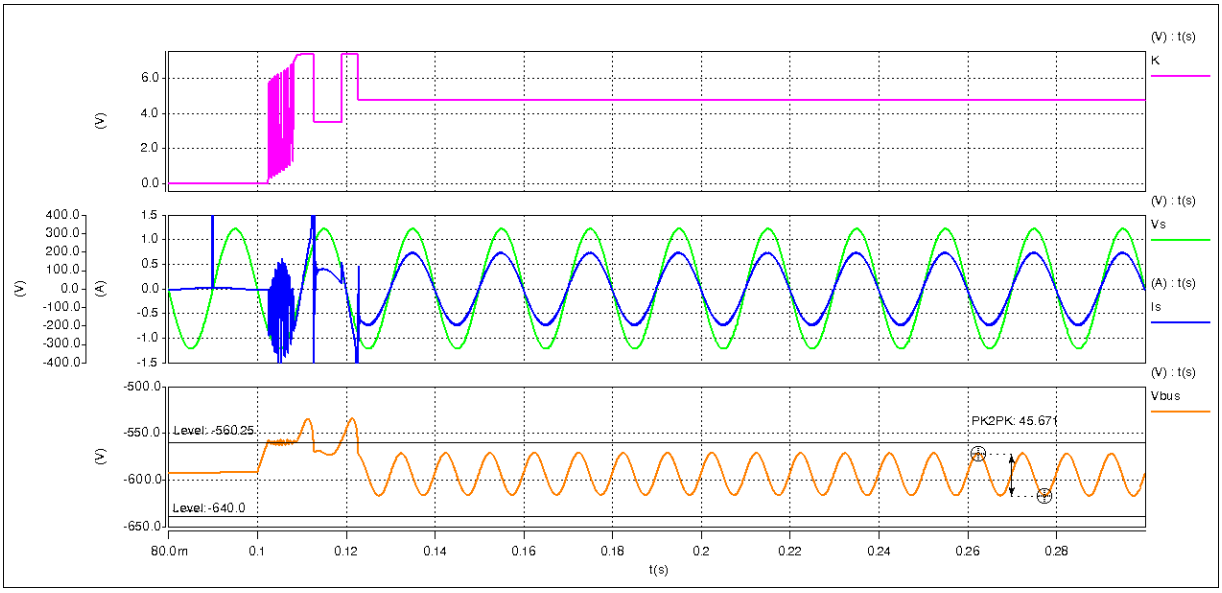


Figure 6-20 SABER V_{bus} response to step load 0 W to 120 W

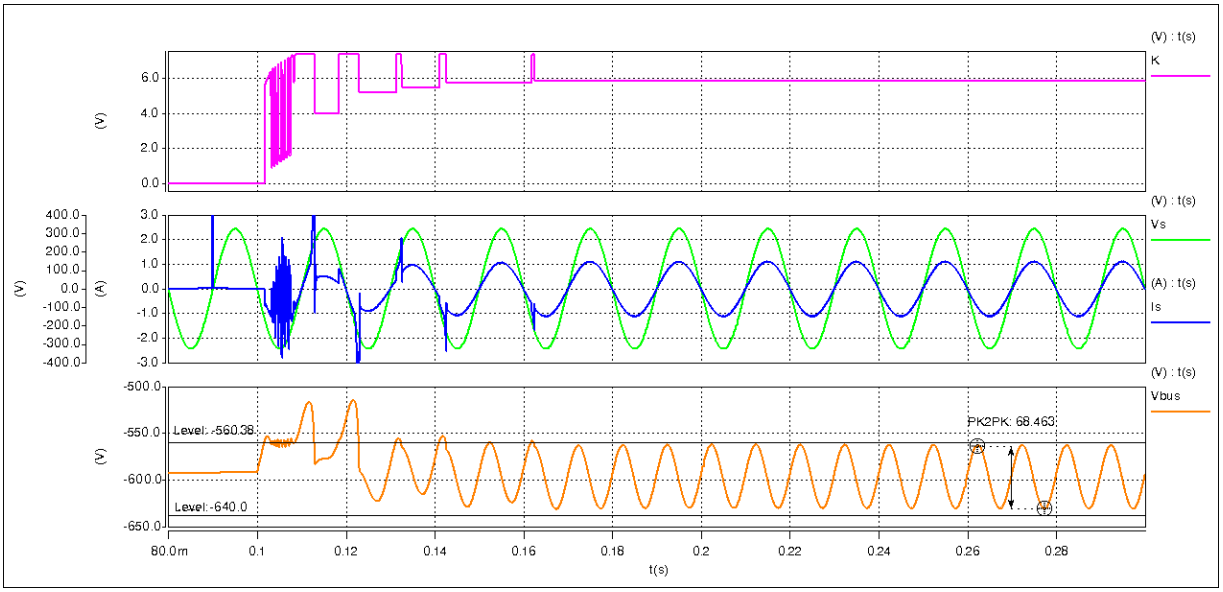


Figure 6-21 SABER V_{bus} response to step load 0 W to 180 W

During the step load change, V_{bus} repeatedly becomes more positive than limit V_{high} for a number of cycles despite the PI compensator attempting to regulate V_{bus} back within the voltage regulation band. The maximum output voltage of the compensator, K, is limited by zener diode D_5, and a high frequency oscillation can be seen during the cross over of V_{bus} at around 0.11 s as K increases and the natural 100 Hz ripple of V_{bus} attempts to pull the voltage beyond the regulation band. This high frequency oscillation can be eliminated by reducing the gain of the PI compensator, which will in turn reduce the band width of the open loop stage. However, reducing the PI compensator gain would cause V_{bus} to sag significantly during step load increases, and the subsequent constant current power stages to operate beyond their specifications.

For this application step load changes would only occur at the turn on of the LED constant current regulators. Other step load conditions to which the application may be subject are those when the LED string is required to dim or brighten. Figure 6-22 details the converter subject to a change in load from 0 W to 60 W with step load increases to 120 W and finally 180 W at 10 ms, 0.1 s and 0.3 s respectively. Figure 6-23 shows the converter subject to a change of load from 0 W to 180 W followed by step load decreases to 120 W and 60 W, at 5 ms, 0.1 s and 0.3 s.

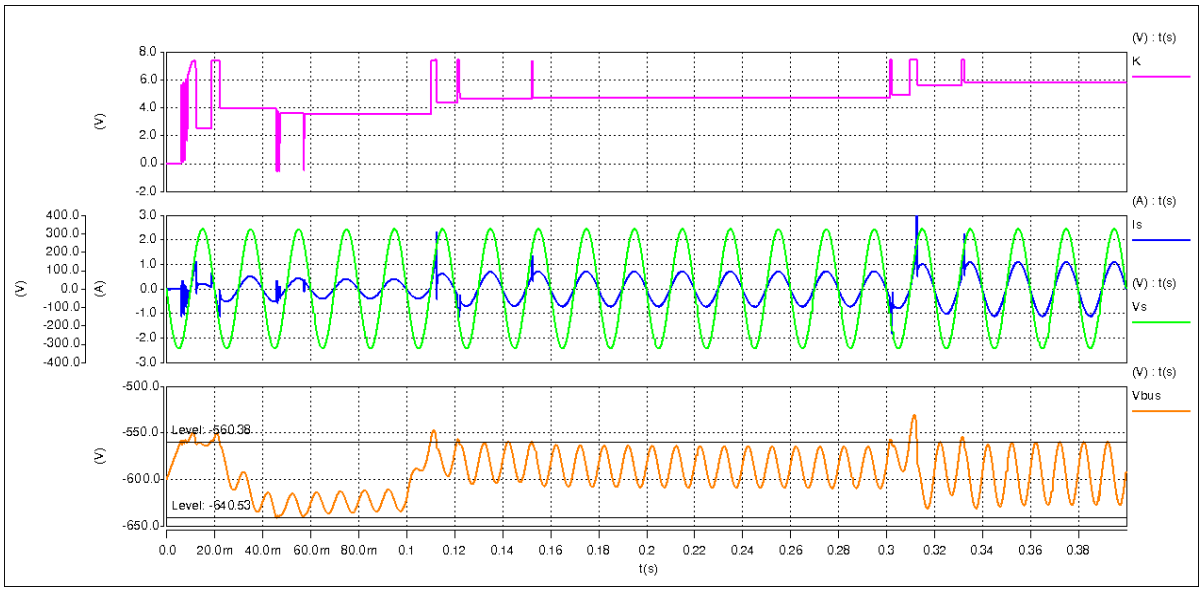


Figure 6-22 SABER V_{bus} response to step load from 0 W to 60 W to 120 W to 180 W

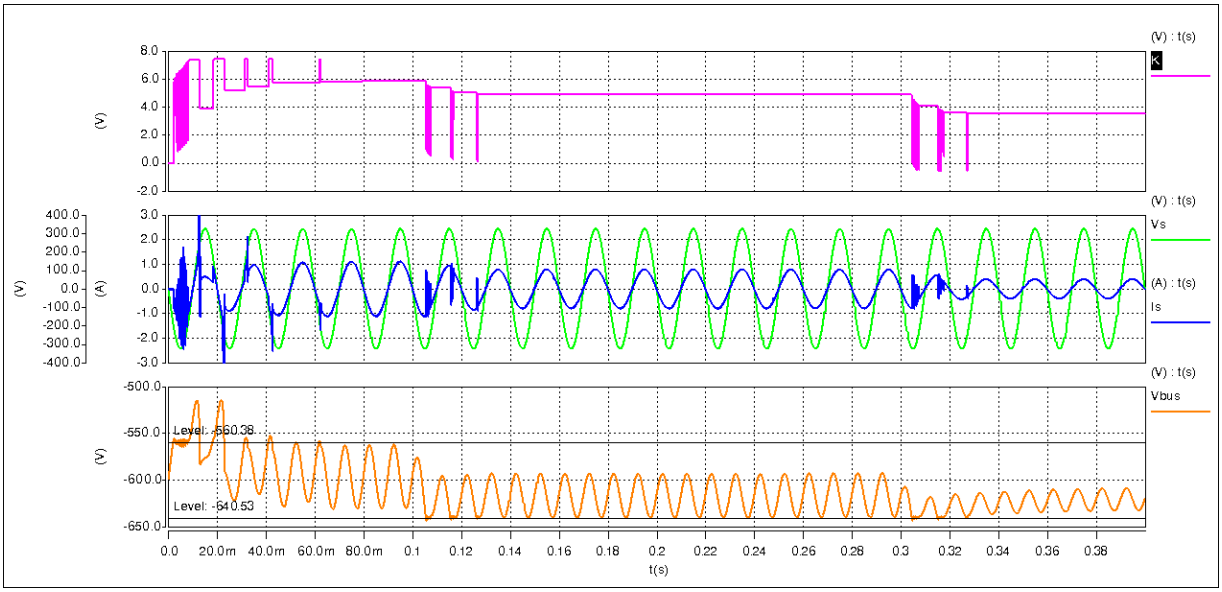


Figure 6-23 SABER V_{bus} response to step load from 0 W to 180 W to 120 W to 60 W

From these simulations it can be seen that the simulated model of the power stage and its control loop are performing as expected and are suitable for this application.

6.10 Summary

This chapter has presented a thorough analysis of a modified regulation band voltage controller for a HP LED power factor correction converter. Due to the implications of the performance characteristics of the PFC stage, a suitable control loop had to be realised that

whose operation would regulate the PFC output voltage, but would not generate any significant input current harmonics. A modified regulation band controller detailed in Chapter 1 is developed that fulfils this criterion.

A detailed description of operation of this method is discussed and the dynamics of the control loop are analysed. Due to the non linearity presented by the regulation band, Circle Criterion is applied to determine the system loop stability whilst MATLAB and SABER simulations validate the initial theoretical analysis. Finally a discrete regulation band controller is designed for implementation in a proof of concept prototype.

An important contribution of this chapter is the development, analysis and design of a control approach that has not been presented in any literature for this application. This work forms part of a conference paper and presentation at the IEEE Power Electronics, Machines and Drives, 2008, York.

7 Experimental Verification and System Performance

7.1 Introduction

This chapter details the prototype development of the HP LED driver designed in Chapters 5 and 6. After a review of the HP LED driver requirements the design of a current regulator and control approach is conducted with SABER simulations to validate the design. The development of the prototype HP LED driver, PFC and regulator stage is undertaken showing the layout and tracking of the two topologies. Finally, the prototypes experimental measurements are compared with the predicted SABER and MATLAB simulation models.

7.2 HP LED Constant Current Regulators

This section details the design of the power topology and control approach for regulating the current through each of the three LED strings introduced in section 5.2. High power LED devices need to be supplied with a regulated current. The current flow through them defines the lumens output. In order to achieve a regulated LED current, whilst minimising peak current and voltage ripple stresses, a secondary converter is required. The LED power system arrangement detailed in Figure 5-3 shows a front end PFC delivering a regulated V_{bus} and unity power factor, and three strings of high power LEDs. Each string of LEDs is independently current regulated. In order to achieve a lumen output of 8,000 lm, 144 HP LEDs are necessary, in this case arranged in three separate strings. Each LED string comprises of 48 LEDs in series. The maximum voltage across a string at 350 mA is around 180 V at T_j = 50 ˚C. As V_{bus} is -600 V, a step down converter is required to supply each LED string with a regulated constant current. Section 1.2.3 identifies the buck converter as a topology able to perform this step down conversion. To maintain simplicity, achieve high reliability and efficiency, the buck converter can operate in near Critical Current Conduction Mode, CCCM see Figure 7-1**,** to perform current regulation. By not using an output filter capacitor while in this operating mode, long operation lifetime can be realised and a simple method of converter control realised. Control methods identified in Section 1.2.5, show that simple hysteretic control would meet the regulation needs.

7.3 Principles of Operation of the Constant Current Converter

Figure 7-1 shows the schematic of the buck converter and a block diagram of the hysteretic control loop. Along with Figure 7-2, the operation of this converter stage is as follows. During t_0 to t_1, MOSFET Q_A is on, and $V_{L_A} = (V_{bus} - V_{led})$ appears across inductor L_A. I_{L_A} increases from $I_{L_{A,\min}}$ to $I_{L_{A,\max}}$. When I_{L_A} reaches $I_{L_{A,set}}$, transistor Q_A turns off. Diode D_A is reversed biased during this period.

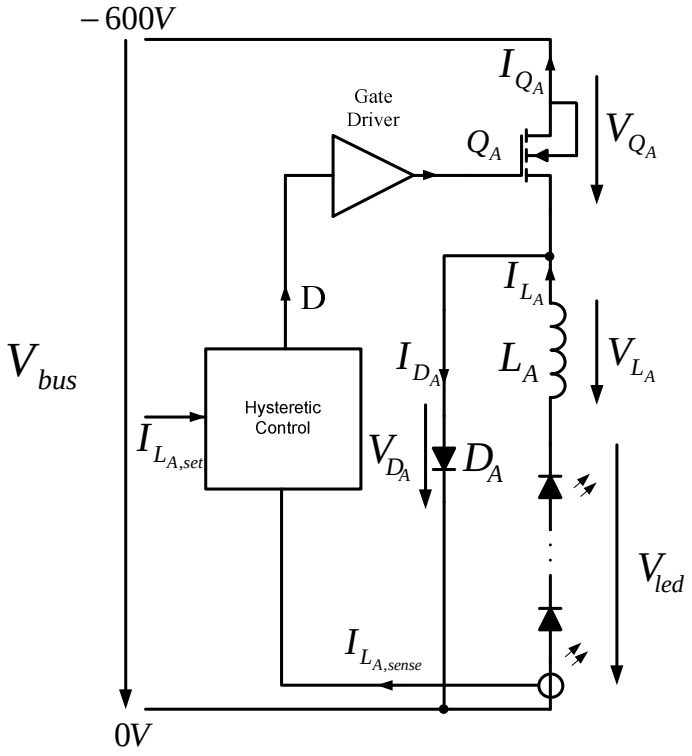


Figure 7-1 Constant current buck regulator with control

The time t_0 to t_1 is given by

$$t_1 - t_0 = \frac{L_A(I_{L_{A,\max}} - I_{L_{A,\min}})}{V_{L_A}} \qquad \textbf{Eqn 7-1}$$

During the period t_1 to $t_0 + T_{sw_A}$ the current in the inductor falls from $I_{L_{A,\max}}$ to $I_{L_{A,\min}}$, and diode D_A conducts.

$$(t_0 + T_{sw_A}) - t_1 = \frac{L_A\left(I_{L_{A,\max}} - I_{L_{A,\min}}\right)}{V_{led}} \qquad \textbf{Eqn 7-2}$$

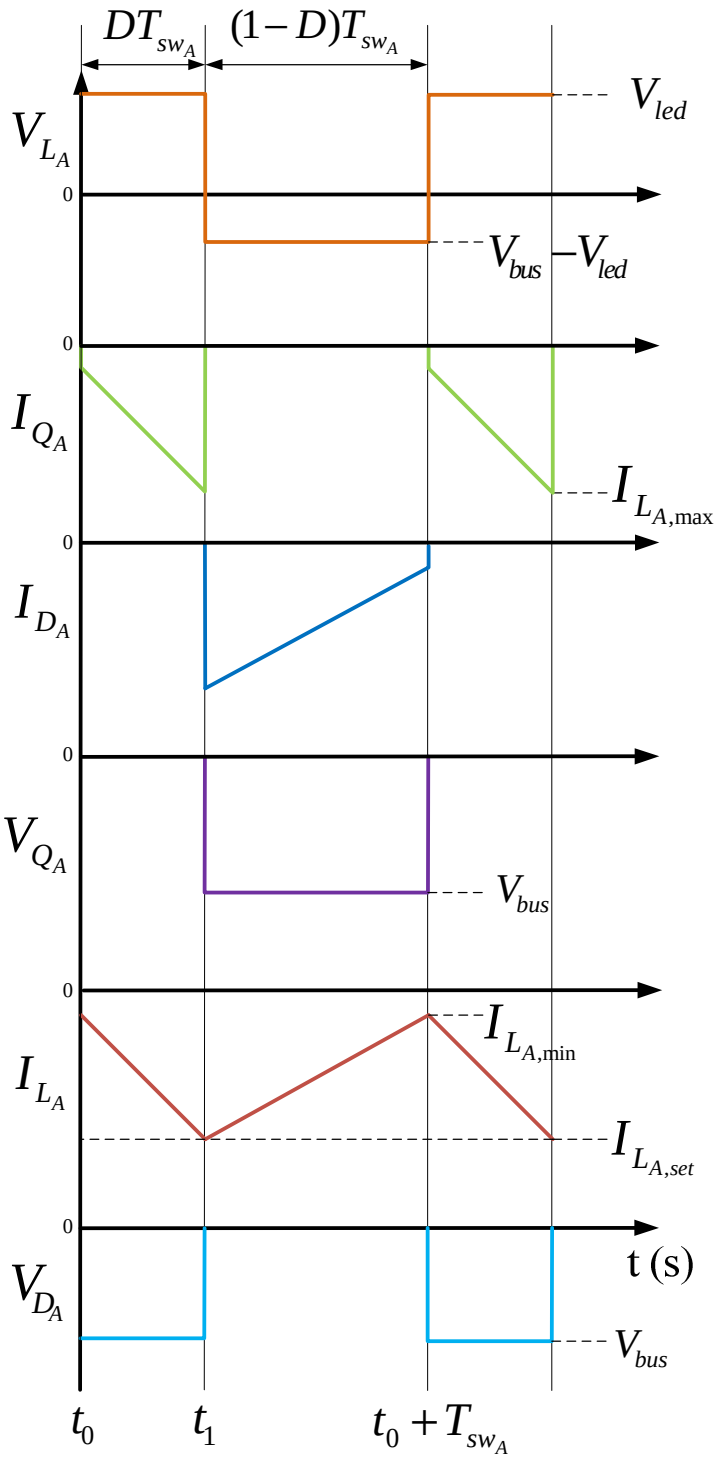


Figure 7-2 Key waveforms of buck converter

When $I_{L_{A,\min}}$ is reached, Q_A is turned on again and the cycle repeats. The average current through the HP LEDs is

$$I_{L_{A,ave}} = \frac{I_{L_{A,\max}} + I_{L_{A,\min}}}{2} \qquad \textbf{Eqn 7-3}$$

The buck converter operates close to boundary conduction current mode, i.e. $I_{L_{A,\min}}$ is nearly zero.

By using this method simple hysteretic current control is possible. Hysteretic operation eliminates the need for small-signal control loop compensation. To reduce the average current supplied to the HP LED string, $I_{L_{A,\max}}$ needs to be reduced so that the required value of $I_{L_{A,ave}}$ is reached. The value of $I_{L_{A,\max}}$ is set by the circuit to be equal to $I_{L_{A,set}}$, a control voltage input level. So $I_{L_{A,ave}}$ is adjusted by controlling $I_{L_{A,set}}$, either from a separate voltage source or via a potentiometer. There is a consequential change in switching frequency from approximately 40 kHz to 80 kHz for an average supply current to the LEDs of 350 mA to 100 mA. Switching the HP LED string at these frequencies will not cause stroboscopic effects.

7.4 Control of Buck Converter

Figure 7-3 shows a diagram of one buck converter hysteretic controller. The HP LED current flows through a sense resistor, R_{sense} creating a voltage signal which is inverted and amplified by a factor of 10 by the instrumentation amplifier, IC_{A1}. The output waveform is applied to the inverted pin of comparator, IC_{A2}. The feedback components R_{A2}, R_{A3} and D_{A1} form the Schmitt trigger. The upper and lower limits are not set by R_{A2} and R_{A3}. The lower Schmitt trigger level is determined by voltage $L_{A,\min set}$, and the upper Schmitt trigger level is set by $I_{L_{A,set}}$.

The output from IC_{A2} is a square wave, which is a function of the amplified sensed inductor current and the upper and lower voltage limits of the Schmitt trigger. This signal is applied to the gate drive circuits switching MOSFET.

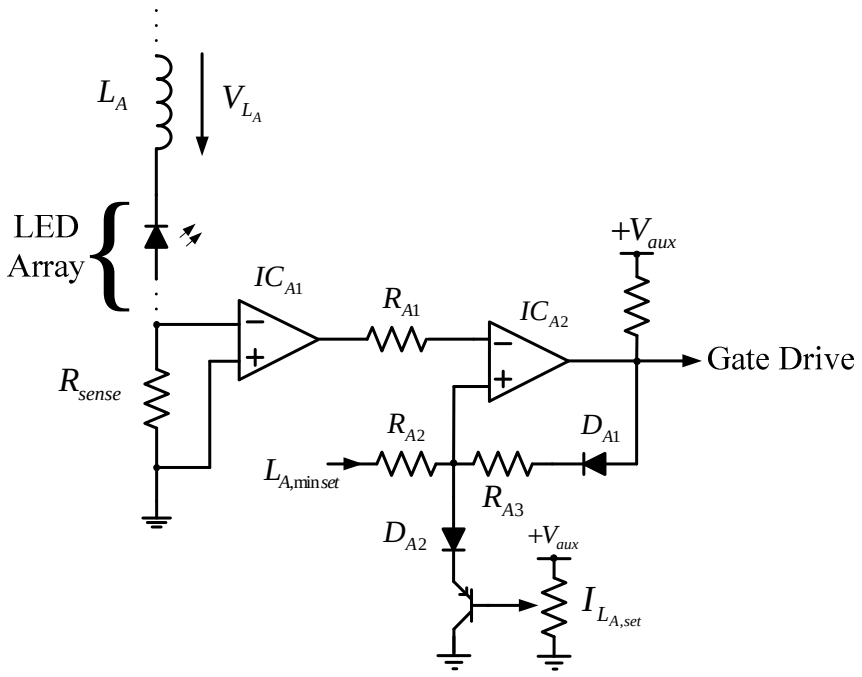


Figure 7-3 Buck Control block diagram

7.5 Constant Current Converter Optimisation

This section details the buck converter design optimisation as well as inductor design and component selection. The principles of operation in the previous section outline the key design equations to help identify the most appropriate inductance, which will in turn realise the optimum frequency operating range and power loss.

With L_A= 5 mH, Table 7-1 details the key calculated operating conditions at a constant input voltage and at minimum and maximum power.

Table 7-1 Key calculated values of constant current converter at minimum and maximum load

Parameter	**30 W**	**60 W**	**Unit**
V_{bus}	-600	-600	V
Duty	0.31	0.31	-
F_{sw}	86.4	40.0	kHz
$I_{LA,pk}$	-0.32	-0.65	A
$I_{LA,ave}$	-0.16	-0.32	A
V_{QA}=V_{DA}	-600	-600	V
$I_{QA,rms}$	0.10	0.2	A
$I_{DA,rms}$	0.15	0.3	A
V_{led}	-186	-186	V

Using the magnetic design approach in section 2.2.4, a summary of the buck magnetic component design can be found in Table 7-2. The same core material and type as the PFC inductor was used again due to its availability and performance characteristics. The relative size of the core allowed the magnetic core and conduction losses to be minimised to a minimum in order to maintain converter stage efficiency.

A power loss break down of the converter operating at full power, 60 W, is detailed in Table 7-3. The power losses of the interconnecting cables, tracks and connectors are ignored. At maximum output the total estimated power loss is 2.70 W, a theoretical converter efficiency of 95 %. A slight increased efficiency to 96.4 % (2.2 W loss) of the converter can be achieved by reducing the buck inductance. However the result of this would be a marked increase in maximum operating frequency to 205 kHz, which is near the optimum operating limit of the magnetic core material and increased EMC interference with the rest of the HP LED lighting system.

Table 7-2 Characteristics of constant current converter inductor

Parameter	**Calculated**	**Unit**
Core manufacturer	Ferroxcube	-
Core type	RM12	-
Core material	3C90	-
Core factor	0.38	mm^{-1}
Effective volume	8340	mm^3
Effective length (m)	55.6	mm
Effective area	146	mm^2
Mean turn length	61	mm
Initial permeability	1730	-
Effective permeability	30.9	-
Air gap	0.5	mm
Inductance factor	351	nH
Inductance	5.1	mH
Number of turns	119	-
Flux	26.8	uW
Flux density	189	mT
Wire length	7.30	m
Current density	3.00	A/mm^2
Wire resistance	13.5	Ω
Copper loss @ 100 °C	1.85	W
Core loss @ 100 °C	0.25	W
Total losses @ 100 °C	2.10	W

Table 7-3 Estimated power losses of converter at full load

Component	Device	Switching Loss (W)	Conduction Loss (W)	Core Loss (W)	Total Loss (W)
Q_A	STP10NK70Z	0.16	0.05	-	0.21
D_A	RHRP8120	0.08	0.311	-	0.391
L_A	RM12	-	1.85	0.25	2.10
Total Estimated Power Loss					**2.70**

7.6 Constant Current Regulator Specifications

To summarise the previous design sections, Table 7-4 details the specification of the current regulator stage.

Table 7-4 Current regulator specifications

Description		Value	Unit
Input Voltage	V_{bus}	600 ±5 %	V
Max Input Current	I_{bus}	122	mA
Output Voltage	V_{led}	180 ±2 %	V
Output Voltage Ripple	$\tilde{V}_{bus}$	5	V
Output Current	I_{Led}	350	mA
Converter Switching Frequency	f_{sw}	40-86	kHz
Output Power Range	P_{out}	30-60	W
Efficiency	η_{PFC}	95 % @ 60 W	

7.7 Constant Current SABER Simulation

The predicted design calculations of the power stage and the hysteretic control loop were verified in a SABER model. Figure 7-4 shows the simulation schematic of the HP LED constant current regulator. The MOSFET is an ideal device with negligible on-state resistance and high off-state resistance. The power diodes are all piece wise linear components with no forward volt drop. The power inductor is also a linear device with no parasitic ESR and interwinding capacitance.

The key simulated results plotted in Figure 7-5 are captured where the input voltage V_{bus} is set to -600 V with a power output delivered to the HP LEDs of 60 W. The results show a close correlation to the predicted design detailed in Table 7-1.

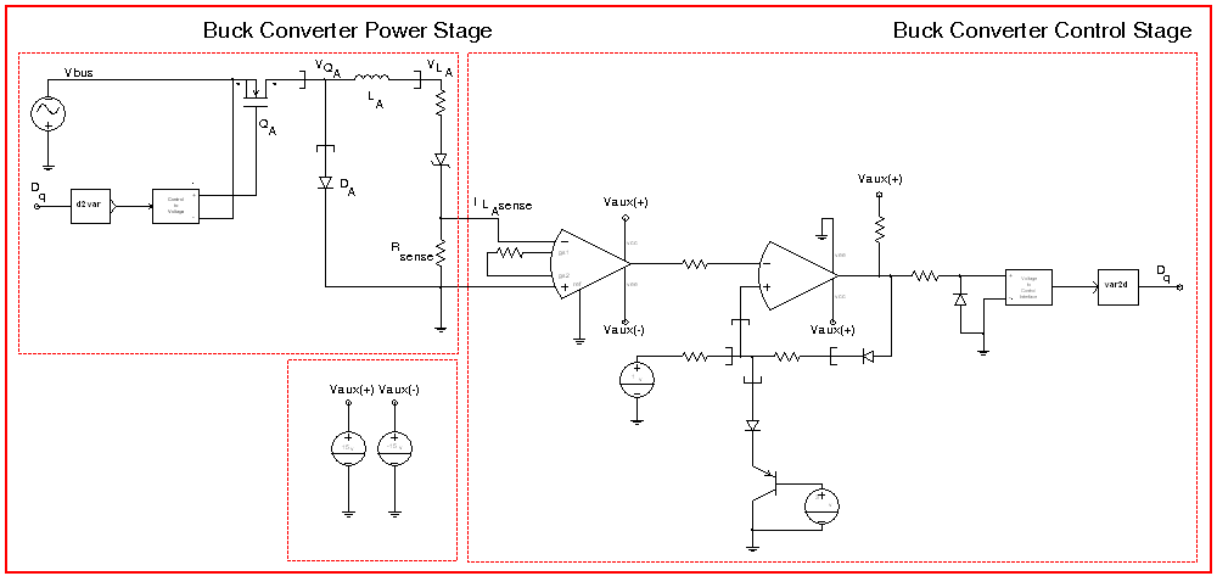


Figure 7-4 SABER simulation model of constant current HP LED regulator

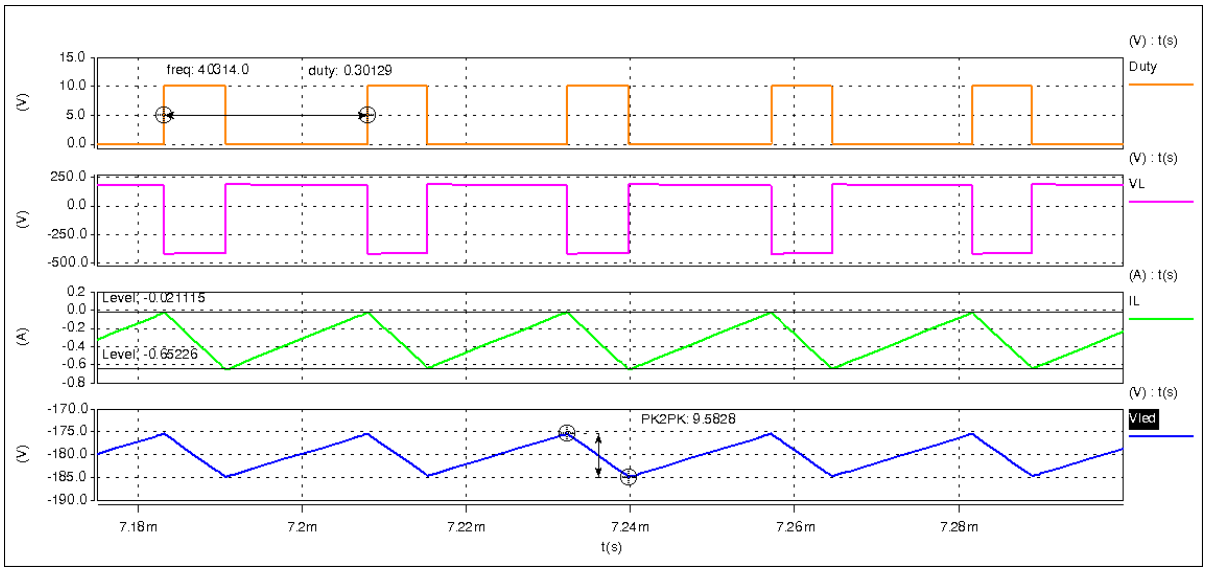


Figure 7-5 SABER simulation of key waveforms of constant current HP LED regulator

7.8 Experimental and Laboratory Setup

This section details the experimental laboratory setup, including the design and layout of the Printed Circuit Boards, PCBs, the equipment used for verifying the performance of the HP LED power converter, and finally the layout tracking of the 180 W LED string.

7.8.1 Power Factor Corrector Circuit Layout

The power factor corrector power stage and the respective control board components were arranged so that they occupied a small area to minimise parasitic inductance loops. The PFC stage comprises two circuit boards, the power stage and a separate control board. The PCBs are FR4 insulating fibre glass with a double sised 1 oz copper layer

Full schematic drawings of control and power stages can be found in Appendix E & F.

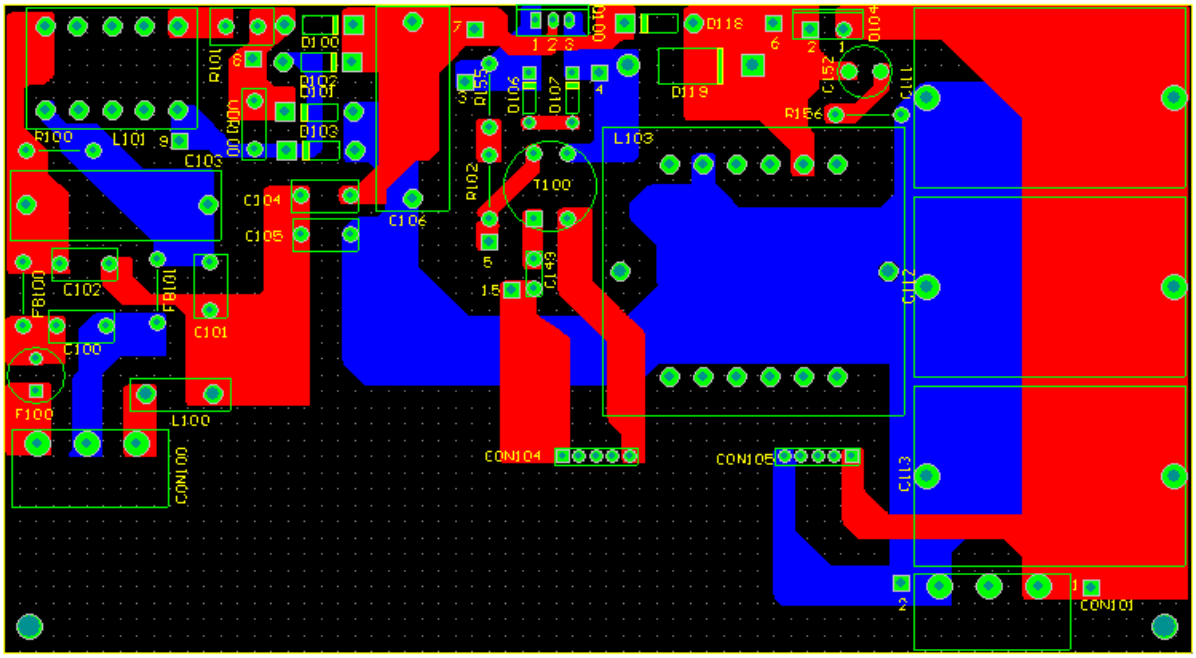


Figure 7-6 PCB capture of power board layout and tracking

Figure 7-6 shows the circuit layout for the buck boost stage. CON 100 on the bottom left hand side of the power board is the line input connector V_s. This input is fused for safety and current surge suppression components are also added. This connector input is keyed so that no connection errors can be made during testing. This also applies to the output, V_{bus}, connector CON 101, bottom right hand side. The connectors CON 104 and CON 105, centre bottom, are the power stage's interface with the control board, see Figure 7-7. CON 105 is the

V_{bus} feedback and CON 104 is the output of the gate driver. As the buck boost MOSFET Q100, is not directly referenced to ground, an isolating pulse transformer T100, is used to transfer the low side voltage gate signal from the control loop, to the high side connected MOSFET, Q100. The RM12 buck boost inductor is labelled device L103 in Figure 7-6 and the metallised film capacitors C111-C113. All inputs and outputs were capacitively decoupled to a copper earth plane, so to ensure EMC suppression.

The control board, see Figure 7-7, consists of the output voltage V_{bus} attenuator, the relay with dead band, the linear PI compensator, a sawtooth waveform generator to supply the PWM comparator, MOSFET gate drive circuitry and auxiliary ± 15 V supplies provided by onboard linear regulators. Again, use of space was minimised to ensure compactness and efficiency. There are also numerous test points situated across both circuit boards for ease of testing.

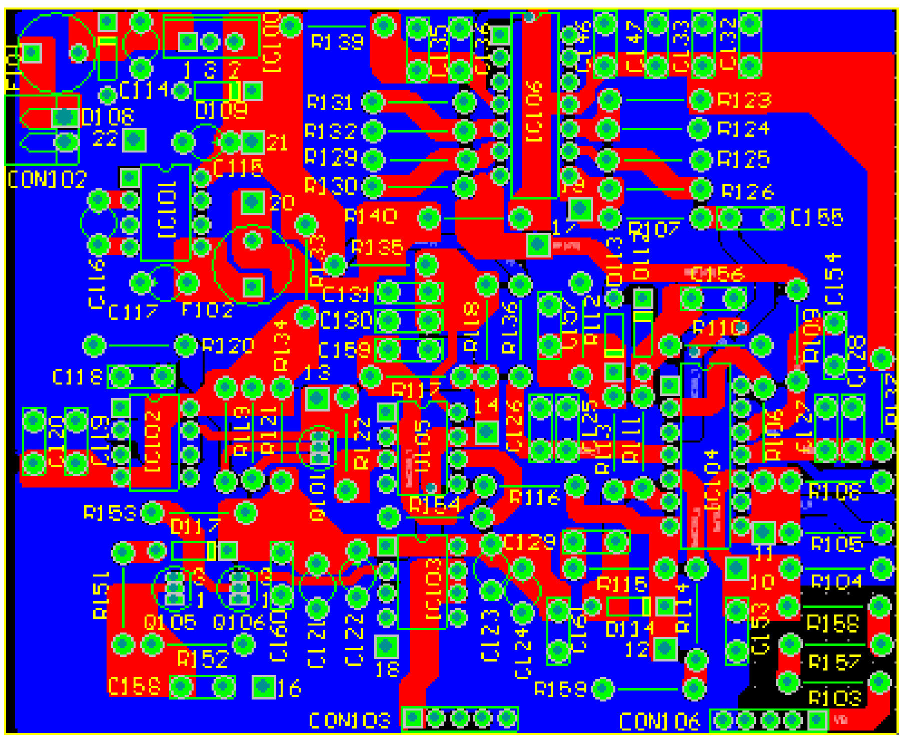


Figure 7-7 PCB capture of control circuit layout and tracking

Figure 7-8 is a picture of the DCM buck boost PFC and its associated control board.

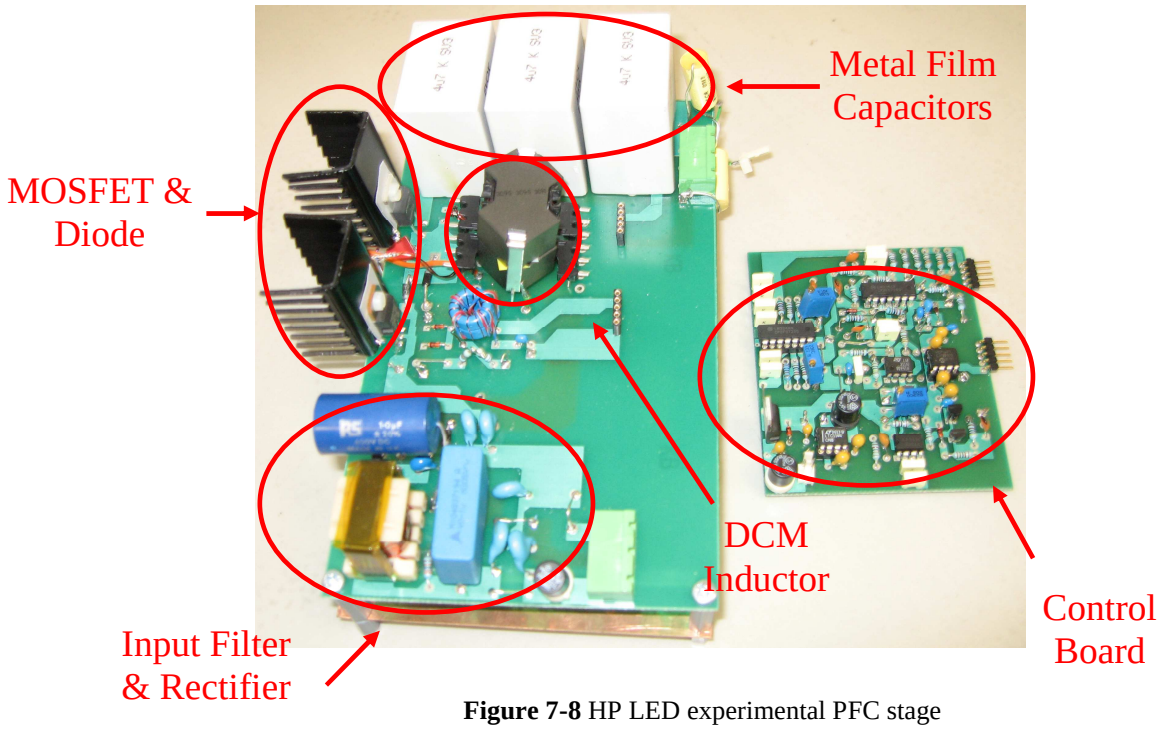


Figure 7-8 HP LED experimental PFC stage

7.9 Constant Current Regulator Circuit Layout

The HP LED current regulators comprise three identical power converters. The buck regulator is a physically compact design to minimise parasitic loops, and minimise EMC generation. The PCB is of FR4 fibre glass with a double sided 1 oz copper layer. The same principles of design and layout were applied. Power connectors were keyed and minimum voltage clearances were observed as to prevent voltage creep. The input connector, CON200, is fused to provide protection should the LED string fail to a short circuit. As the buck MOSFET Q200, source is connected to -600 V, an isolating pulse transformer T200, is used to transfer the low side voltage gate signal from the control loop, to the MOSFET. The power inductor L_A is labelled L200 in this layout, and is also a shielded RM core.

A start up oscillator that momentarily pulses a signal to the input of the comparator which provides a leading edge on which the converter can start switching. The pulse frequency is sufficiently low enough so not to interfere with steady state operation.

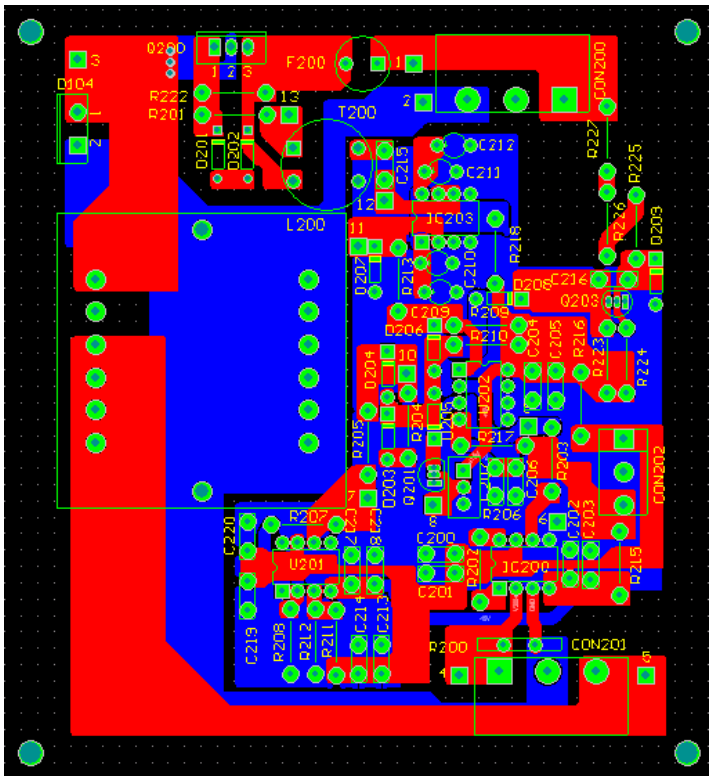


Figure 7-9 PCB layout of constant current buck regulator

Once the PCBs had been populated testing of the prototype boards used the following to acquire and record experimental data; a Lecroy WaveRunner oscilloscope along with a high voltage differential probe ADP305 and a passive AP105 current probe, were used to capture voltage and current waveforms. A Yokogawa WT3000 power analyser recorded and assessed the line voltage, current waveform quality and harmonic content. Laboratory set-up is shown in Figure 4-3.

7.10 HP LED String

In order to fully test the performance of the converter stages, and to realise whether they are suitable for this application, an LED string was constructed, see Figure 7-10, the measured outer dimensions of which are 216 mm by 520 mm. The total display consists of three individual strings of 48 ultra white Cree XLamp XR series HP LEDs. These high power devices emit a lumens output of 70 lm/w at a current throughput of 350 mA.

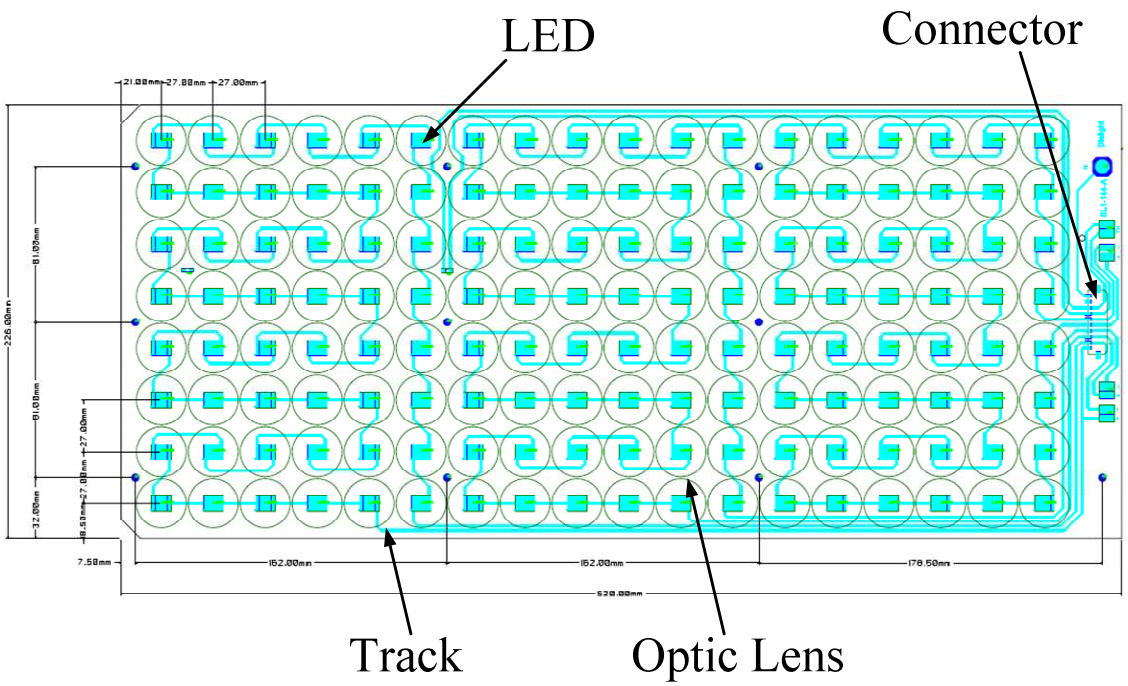


Figure 7-10 PCB layout of HP LED string

Despite the individual LEDs not dissipating their generated heat via radiation as with conventional light sources, they need to be bonded to a thermally conductive PCB and heat sink in order to prove reliable. A single sided aluminium clad laminated with a 1 oz copper PCB is used, to which the LEDs can be directly bonded. This approach not only provides an excellent thermal path but offers electrical isolation as well as a means for tracking. Finally this board was enclosed in a suitable heat sink and the lenses covered with an optically opaque film to protect the observer's vision and other laboratory users, and to reduce harmful glare, see Figure 7-11.

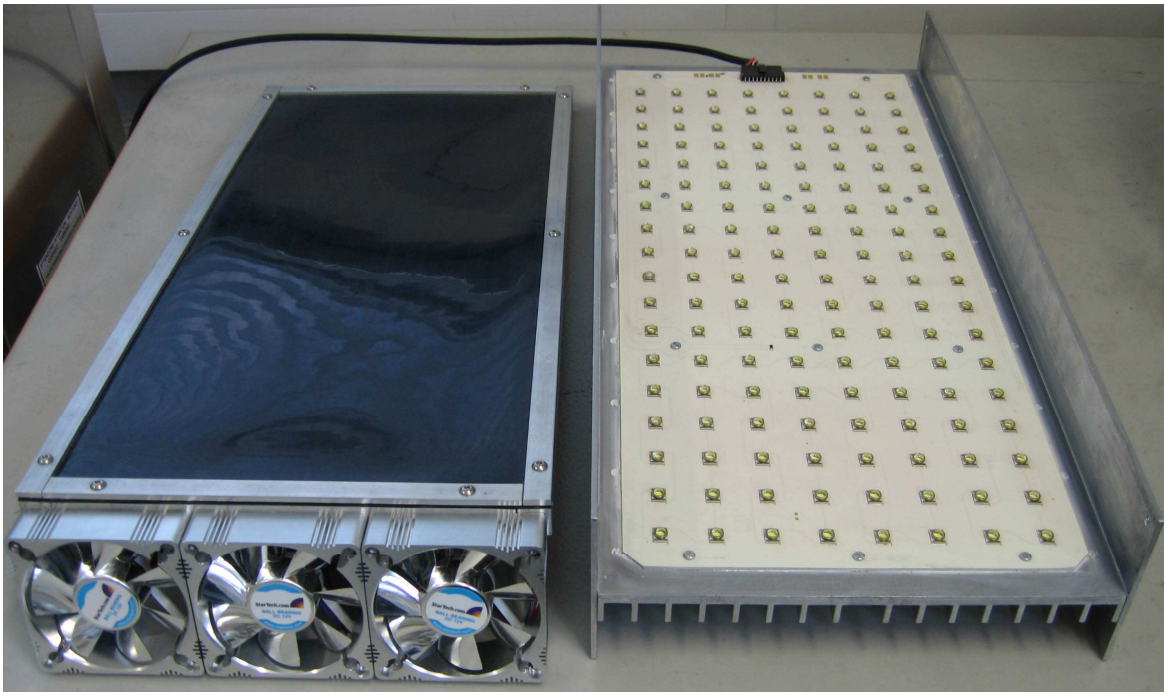


Figure 7-11 HP LED strings and protective cover

7.11 Verification and Results

This section validates the calculated design, computer simulations and experimental data of both the power factor corrector and the respective LED current regulators. Experimental results show the compatibility of the ability of the PFC to be able to meet harmonic regulations and maintain a sinusoidal input current waveform, I_s, in phase with its respective voltage V_s.

7.11.1 Power Factor Corrector

Key design equations and converter operational parameters are detailed in Section 5.9. Table 5-7 lists a number of key design figures predicting the various peak currents and voltages that the components are subject to. All figures presented make the assumption that the converter is operating under ideal conditions, i.e. no parasitic elements.

Table 1-1 in Chapter 1 details the Class C harmonic limits for all lighting equipment rated above 25 W. The first ten specified limits are plotted against the measured input current harmonics of the PFC stage. Again like Table 5-7, the input current harmonics in Figure 7-12 are taken at a nominal input voltage over three various output power loads. It can be seen that all input harmonics fall well within the specified limits, especially that of the second harmonic

that has been all but eliminated by the control approach. The measured power factor of the system was near unity at 0.99.

Table 7-5 Measured parameters of PFC

Parameter	**Test 1**	**Test 2**	**Test 3**	**Unit**
Input Voltage, V_s	216	230	265	V_{rms}
Input Current, I_s	0.94	0.86	0.74	I_{rms}
Input Power, P_{in}	203.4	200.2	198	W
Apparent Power, S_p	203.6	201	198.6	VA
Reactive Power, Q_p	8.48	8.11	9.46	VAr
Power Factor, PF	0.998	0.999	0.998	-
Phase Angle, θ	2.39	2.35	2.74	°
V_s THD	0.93	0.93	0.93	-
I_s THD	5.08	5.108	5.57	-
Output Voltage, V_{bus}	602	595	599	V_{rms}
Output Current, I_{bus}	0.29	0.30	0.30	I_{rms}
Output Power, P_{out}	179.8	180.1	180.2	W
Efficiency, η	88	90	91	%

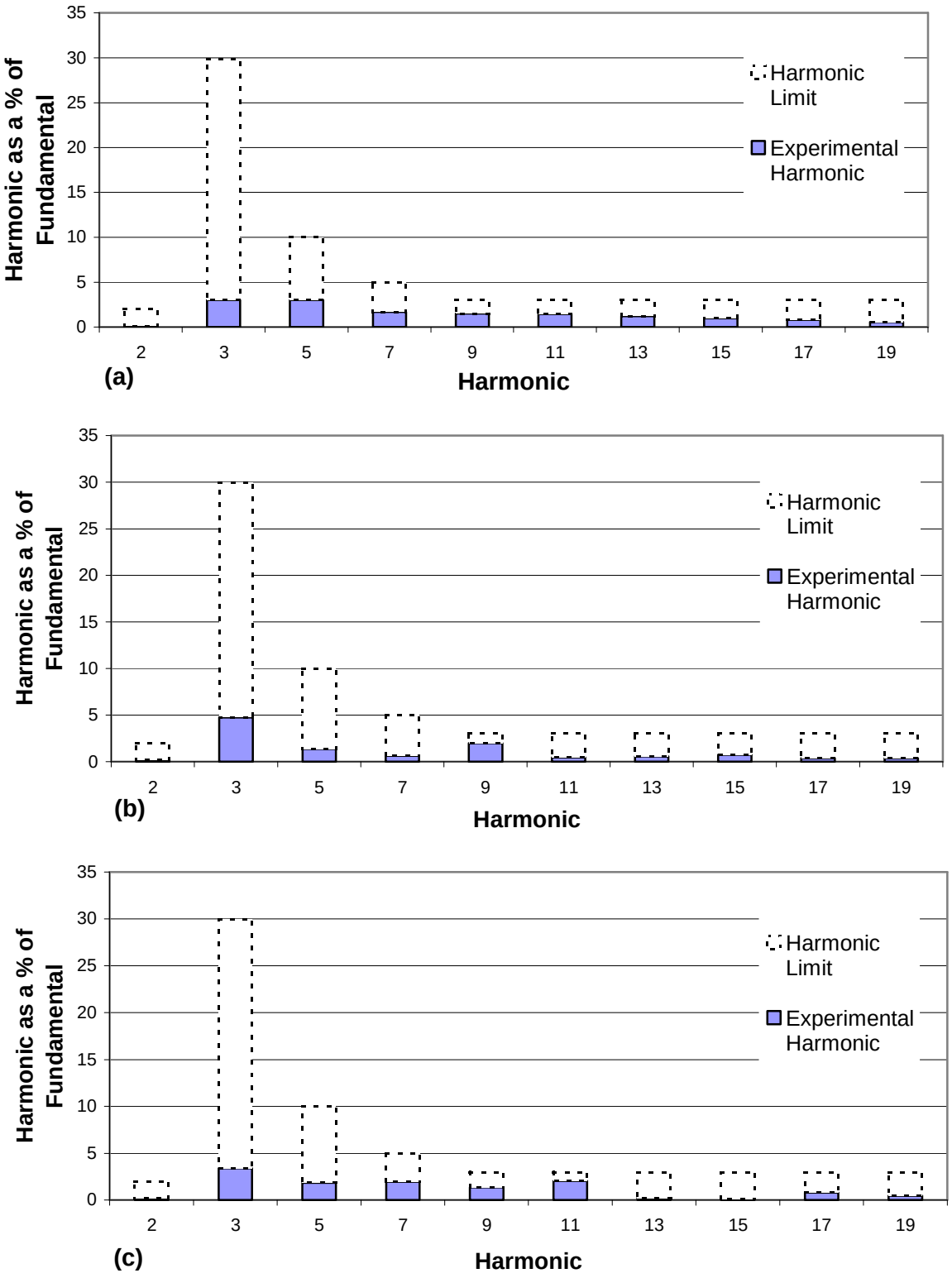


Figure 7-12 Input current harmonics at $V_s = 230\,V$ (a) 60 W, (b) 120 W, (c) 180 W output

.

7.11.2 Buck boost steady state experimental waveforms

In this section the recorded steady state experimental waveforms of the buck-boost PFC. These signals are superimposed and compared with the SABER simulated waveforms to verify the performance and operation of the prototype. The following steady state plots are captured at an input voltage of $V_{s,nom}$, at various load conditions.

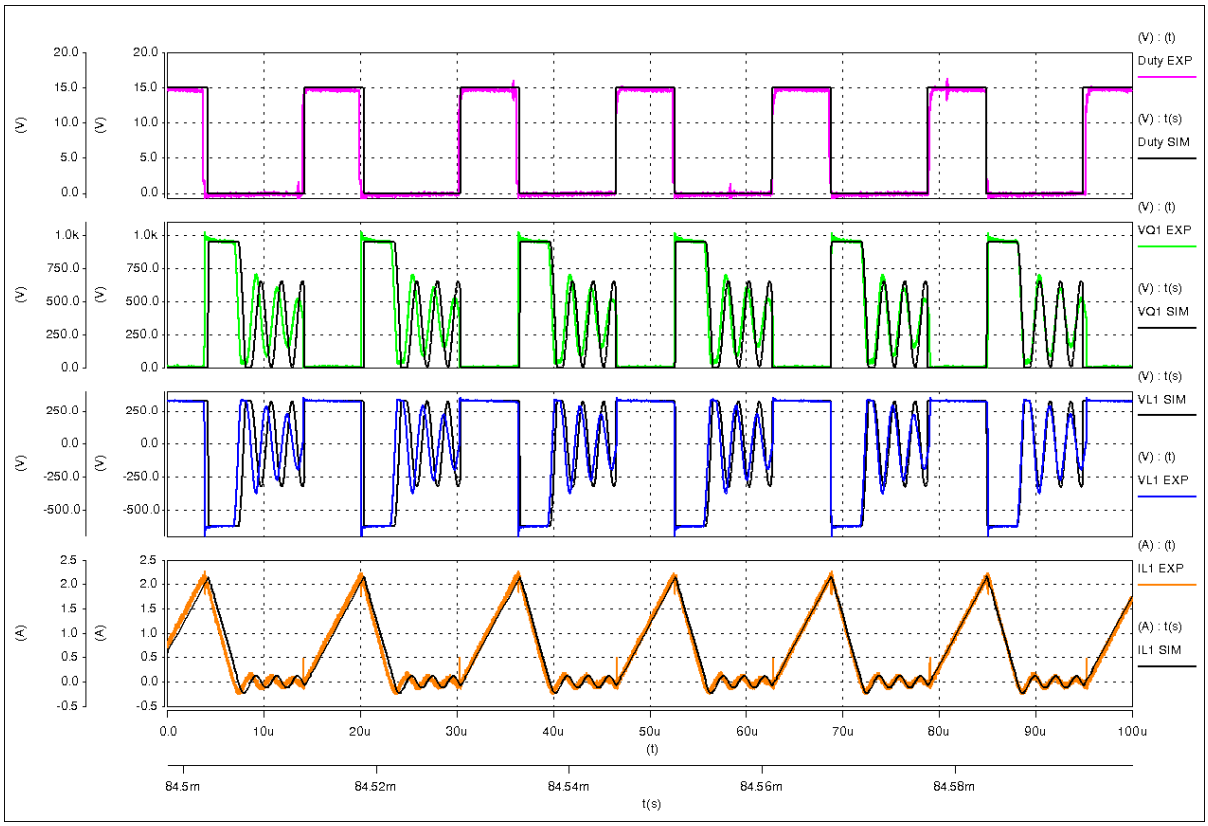


Figure 7-13 Comparison of simulation and experimental results for V_s=230 V_{rms} at P_{out}=60 W

Excellent correlation between simulated and experimental waveforms can be seen, in terms of similar wave shapes and magnitudes. Due to parasitic observations observed in Section 4.4, parasitic components are modelled, hence the high frequency oscillations occurring during the DCM in the simulated steady state waveforms. However there are some minor discrepancies that are worth noting. Again there is a slight mismatch between the switching frequency of the simulation and the prototype. This is due to prototype component tolerances in the PWM oscillator. Switching interference is observed on the experimental waveforms of the duty cycle of all figures. The frequency of this interference corresponds to the switching frequency of the cascaded buck converter. EMC suppression approaches

diminish this interference to the magnitudes seen in Figure 7-13 to Figure 7-15, and do not degrade the performance of the PFC power stage or the control loop.

Parasitic elements of the prototype were introduced to the simulation model to improve the accuracy and verify the performance. Again close relationship of the parasitic oscillations can be seen apart from the damping ratio.

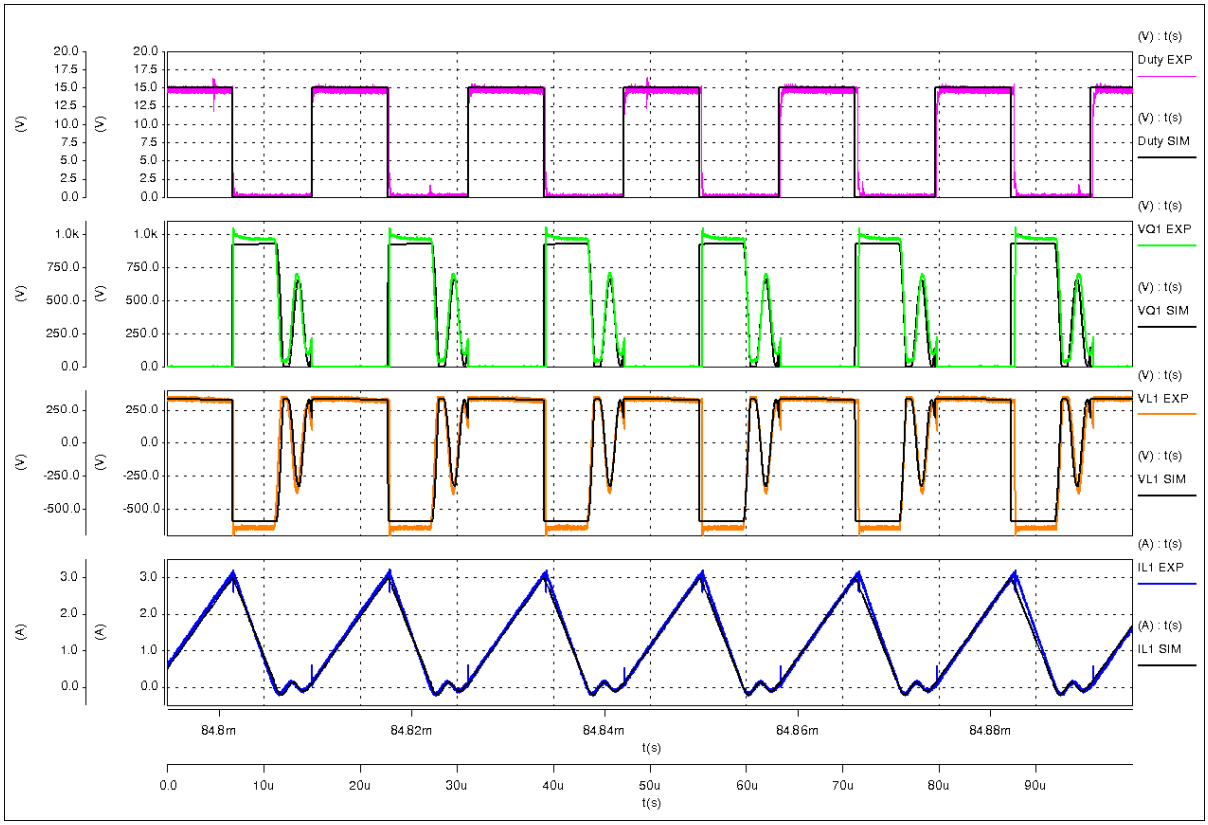


Figure 7-14 Comparison of simulation and experimental results for V_s=230V_{rms} at P_{out}=120W

Figure 7-15 shows the PFC operating at full power and with an input line voltage of 230 V_{rms}. The converter can clearly be seen to be operating close to the limit of discontinuous current mode. Parasitic oscillations are not evident in both the simulated or experimental waveforms as the dead time is near zero. The operating mode of the PFC tends to near critical current conduction mode as the input voltage approaches $V_{s,min}$. Experimental observations show that critical conduction mode is not realised unless the supply voltage exceeds its defined limits.

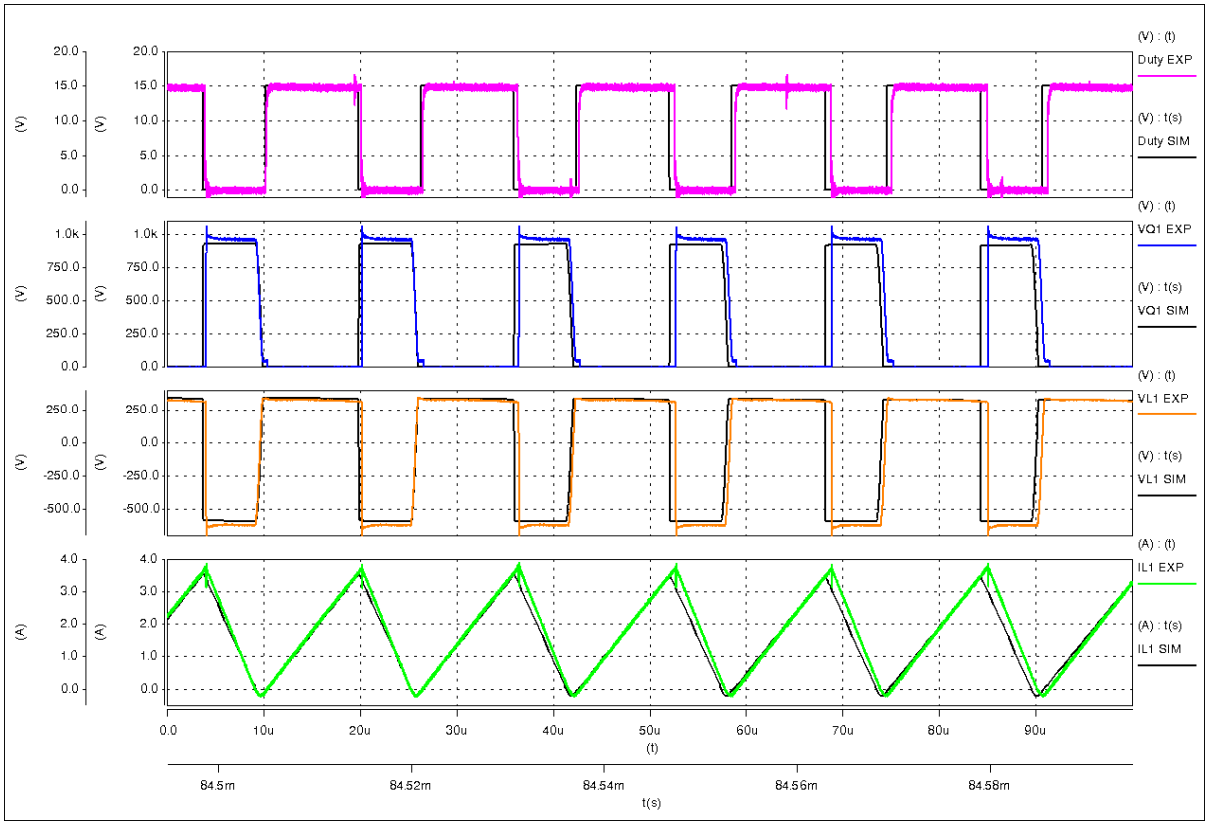


Figure 7-15 Comparison of simulation and experimental results for V_s=230V_{rms} at P_{out}=180W

Besides the parasitic elements of the switching semiconductor, of which one has no control, there is very little leading or trailing edge current or voltage spikes, owing to the careful and compact circuit layout.

7.11.3 Parasitics

Note the oscillations of the simulated SABER waveforms and that of the measured experimental waveforms during T_{off}. The oscillation observed during the period that the inductor current falls to zero is due parasitic inductances and capacitive components, most notably during low load, 60 W. Figure 7-16 details these main components such as track inductance, semiconductor capacitances, and inductor winding capacitance. Track inductance can be deemed to be negligible as the layout is compact. The semiconductor capacitances can easily be determined by referring to their respective datasheet.

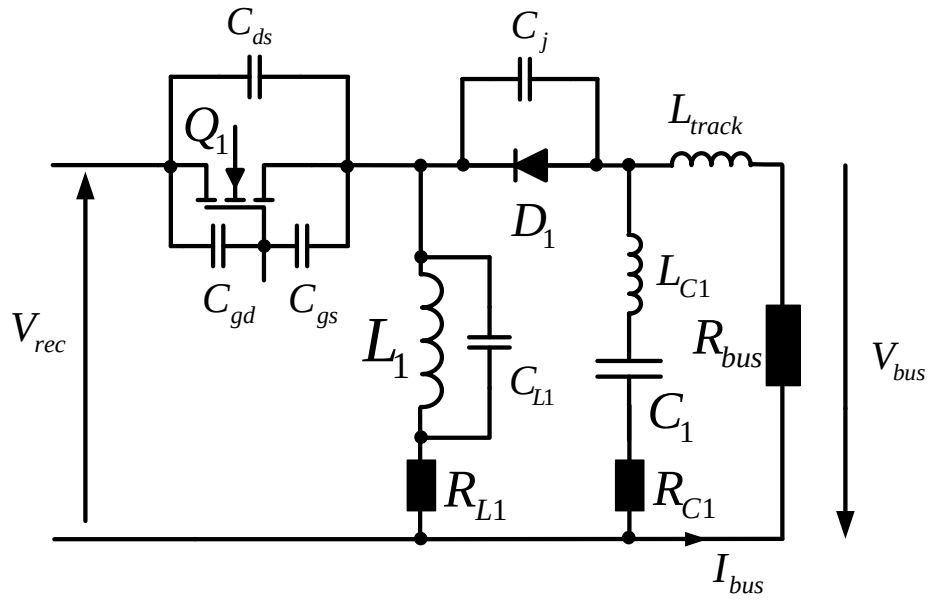


Figure 7-16 Parasitic components of buck boost

The winding capacitance of the inductor L_1 is more difficult to determine. In order to realise this parameter an HP-3577B Network Analyser was used to determine the resonant frequency. An impedance measurement over a frequency spread of 10 kHz to 5 MHz determines the resonant frequency, f_r to be approximately 1.8 MHz. Using

$$C_{L1} = \frac{1}{w_r{}^2 L_1} \qquad \textbf{Eqn 7-4}$$

where $w_r = \frac{1}{f_r}$, the winding capacitance becomes 9 pF. From Figure 7-17 the high frequency of the measured oscillation was determined to be 467 kHz. Further investigation showed the oscillation to be excited by the inductance L_1 and output capacitance C_{oss} of the MOSFET. The MOSFET output capacitance, $C_{oss} = C_{ds} + C_{gd}$, is 174 pF. These parasitic components were simulated and a comparison can also be seen in Figure 7-17. The conditions for this figure are V_s=230 V_{rms}, V_{bus}=-629 V, P_{out}=60 W, F_{sw}=58 kHz, Duty= 0.36. These oscillations are difficult to suppress with a typical resistor, capacitor, diode, RCD, combination without excessive power dissipation.

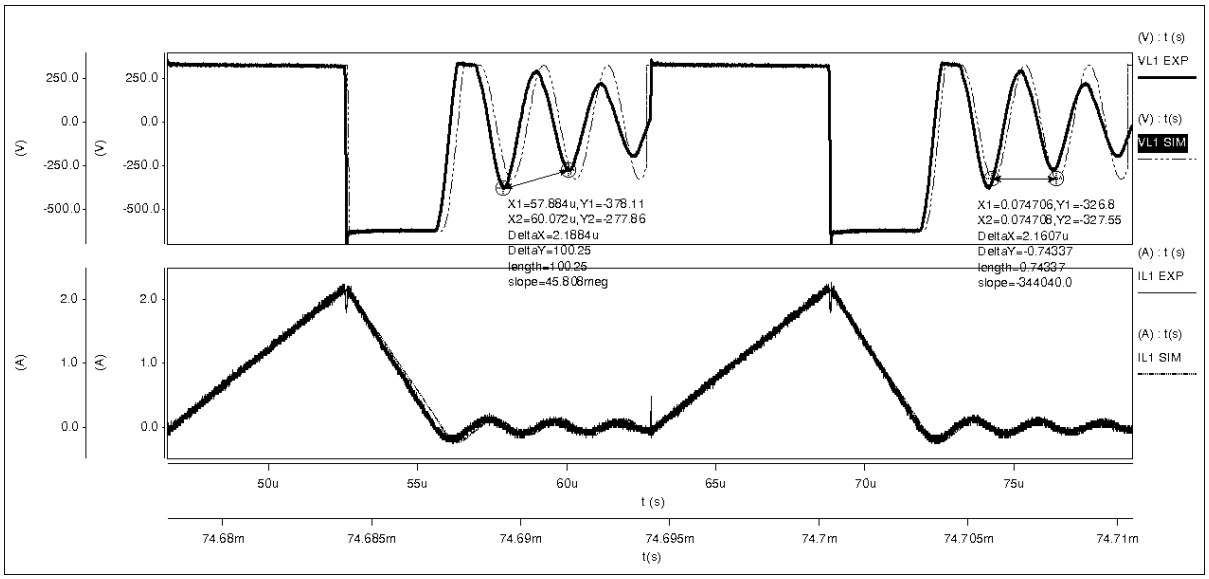


Figure 7-17 Comparison of simulated and experimental parasitic components

The resonance damping seen in the experimental measurements is due to track resistance and inductor resistance, which is difficult to estimate for a simulation. These parasitic components are now included in the simulation for all line and load conditions and the results can be seen in the next section.

7.11.4 Buck boost transient experimental waveforms

The transient response of the prototype converter is shown in this section were it undergoes step load changes. The key waveforms captured are the output power step load, P_{out}, the output signal of the PI compensator, K, the buck boost inductor current, I_{L1}, and finally the output voltage, V_{bus}.

Figure 7-18 shows the PFC being subject to a step load change of 0 to 60 W at time 18 ms. When the step load change occurs, the output capacitors are discharged and V_{bus} tends to zero. Upon exceeding the predetermined voltage bandwidth of -560 V 18 ms later, the PI controller responds by increasing K, which increases the switching duty ratio and bringing V_{bus} back within the limits. At this point K maintains its level until another transient. The calculated and simulated models are verified by the performance of the prototype. The 100 Hz output voltage ripple, $\tilde{V}_{bus}$, the peak current $\hat{I}_{L1}$ and the response time in the below figures are the same as those calculated and predicted by models.

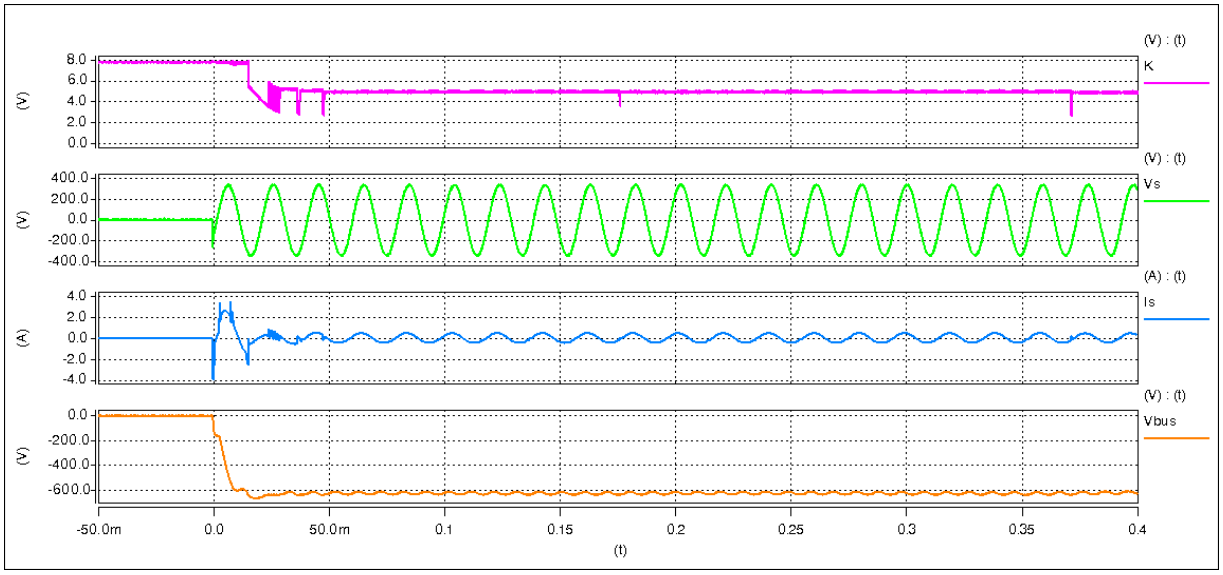


Figure 7-18 Experimental results of PFC output with a step load of 0 W to 60 W

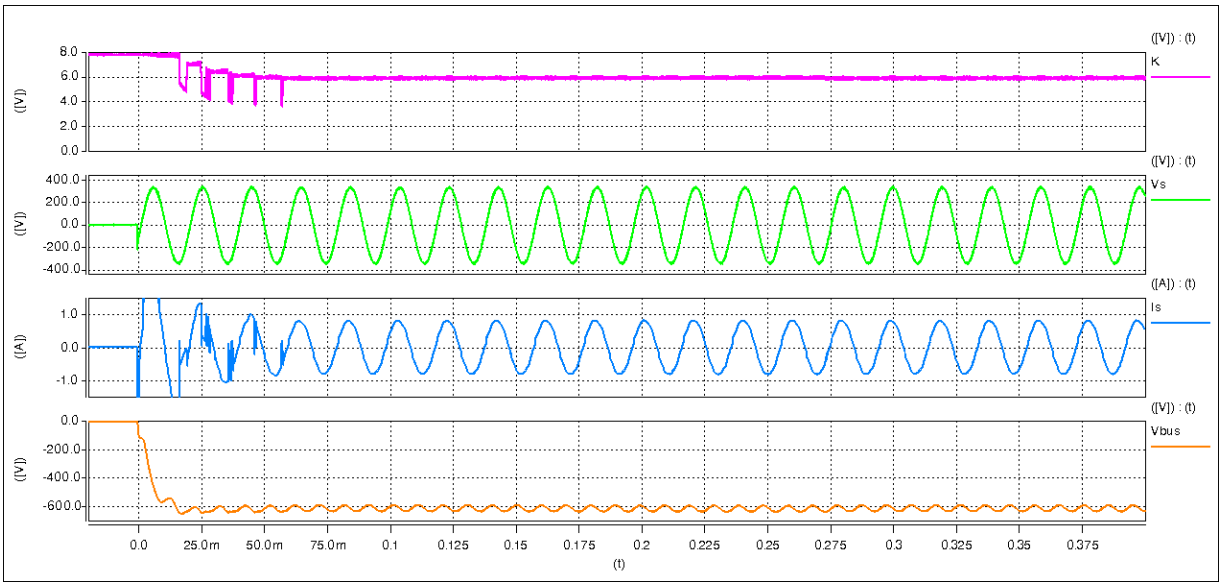


Figure 7-19 Experimental results of PFC output with a step load of 0 W to 120 W

A disparity between the simulated and experimental measurements is the DC offset of V_{bus} when it is within the voltage bandwidth. In this state the power converter is in an open loop condition therefore it is not possible to capture the same voltage level twice. The same is true for the value of signal K.

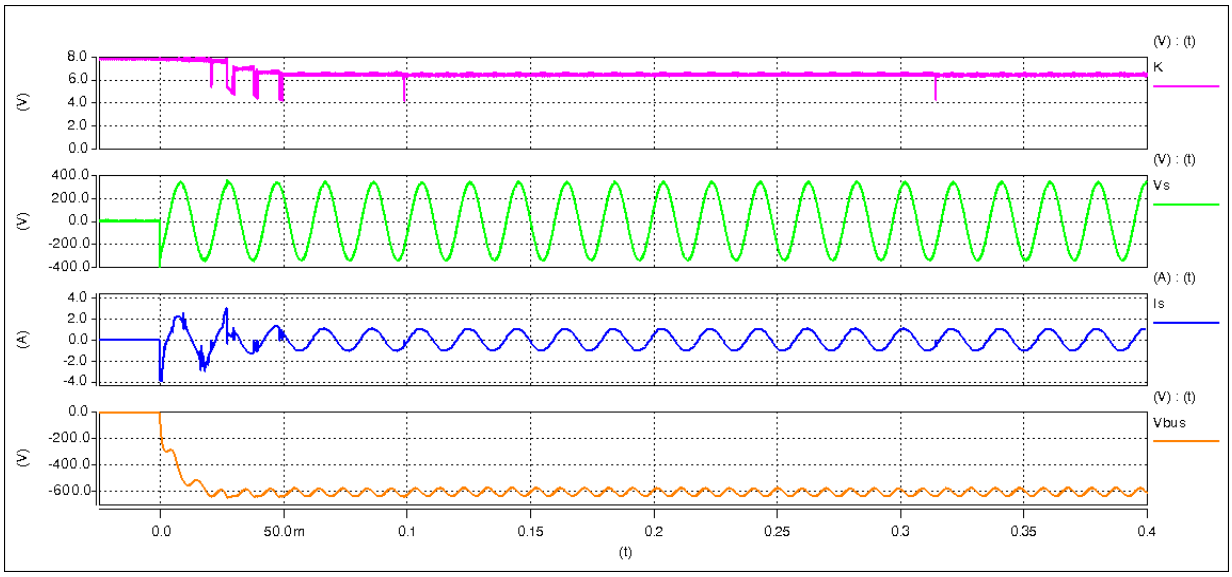


Figure 7-20 Experimental results of PFC output with a step load of 0 W to 180 W

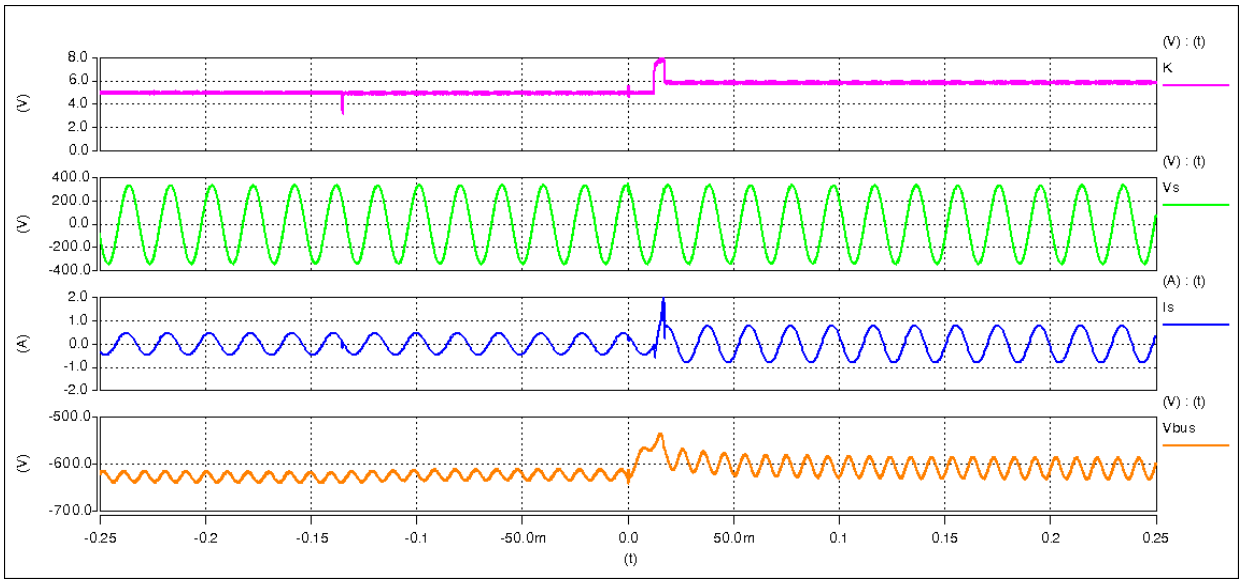


Figure 7-21 Experimental results of PFC output with a step load of 60 W to 120 W

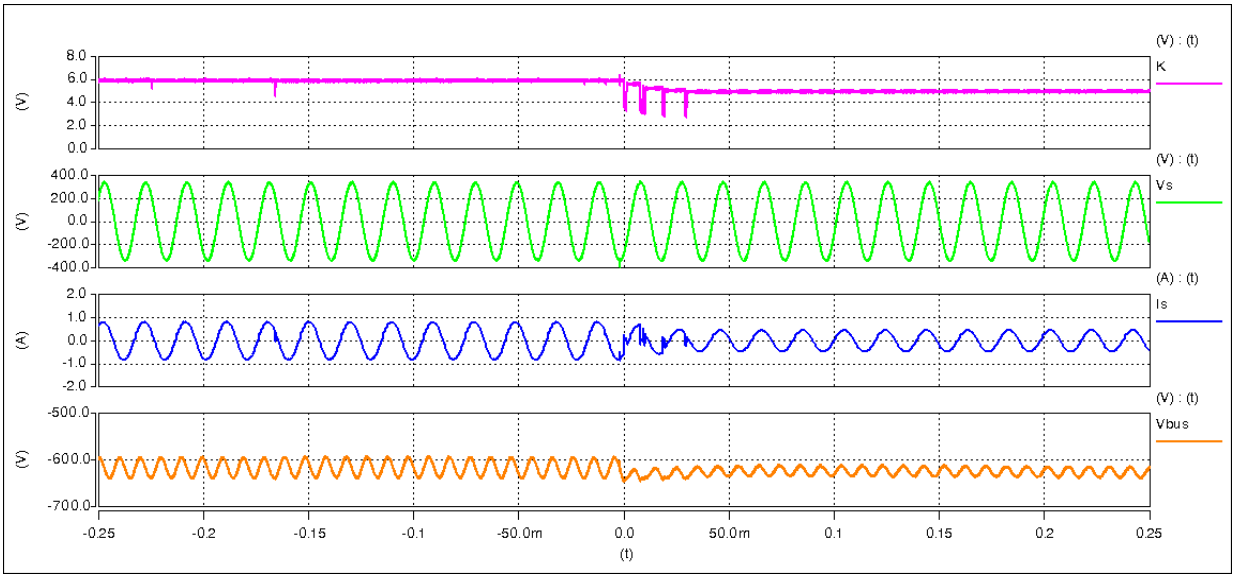


Figure 7-22 Experimental results of PFC output with a step load of 120 W to 60 W

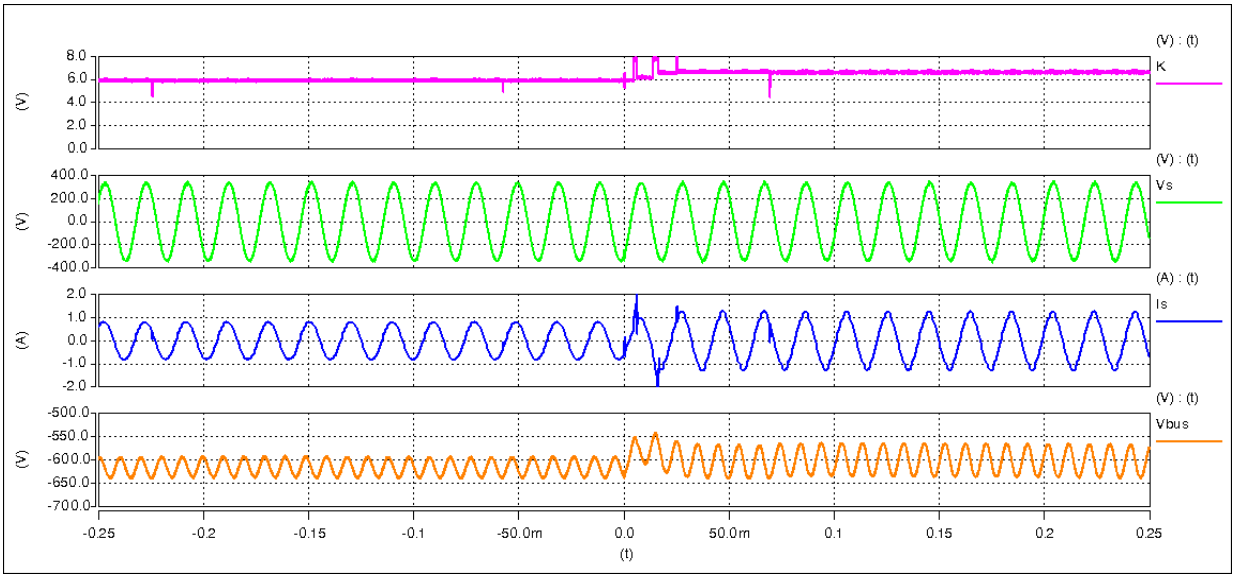


Figure 7-23 Experimental results of PFC output with a step load of 120 W to 180 W

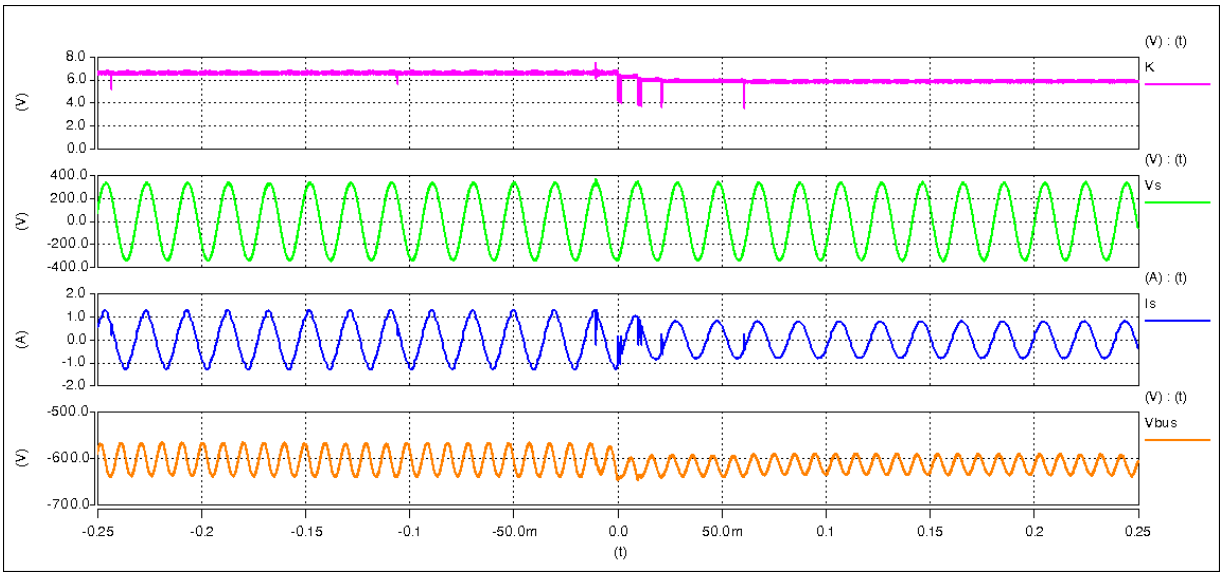


Figure 7-24 Experimental results of PFC output with a step load of 180 W to 120 W

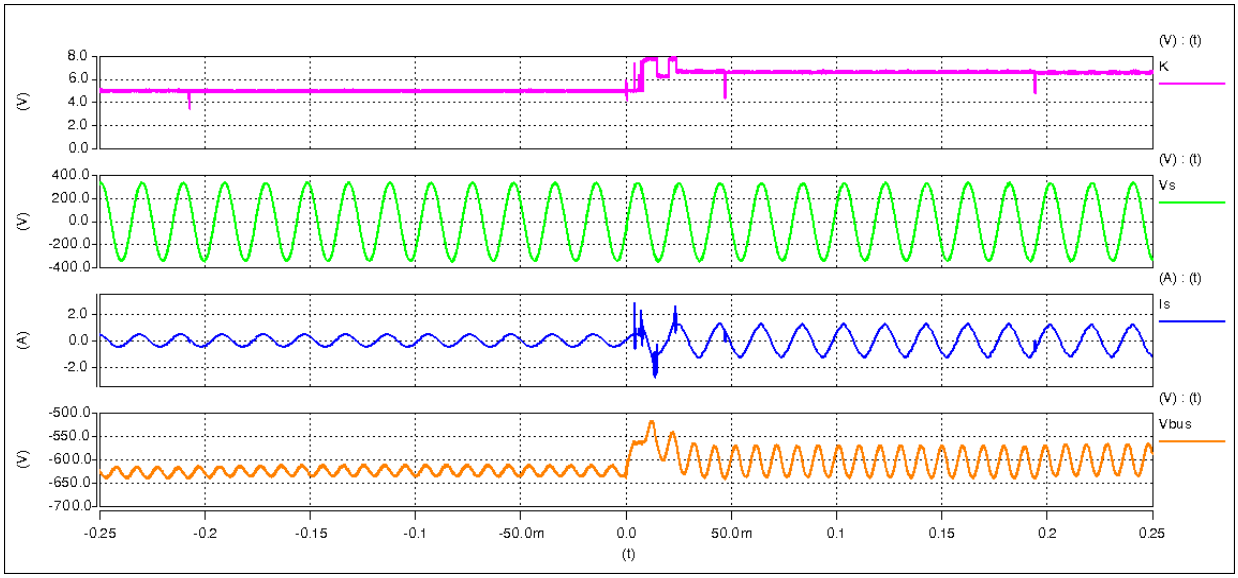


Figure 7-25 Experimental results of PFC output with a step load of 60 W to 180 W

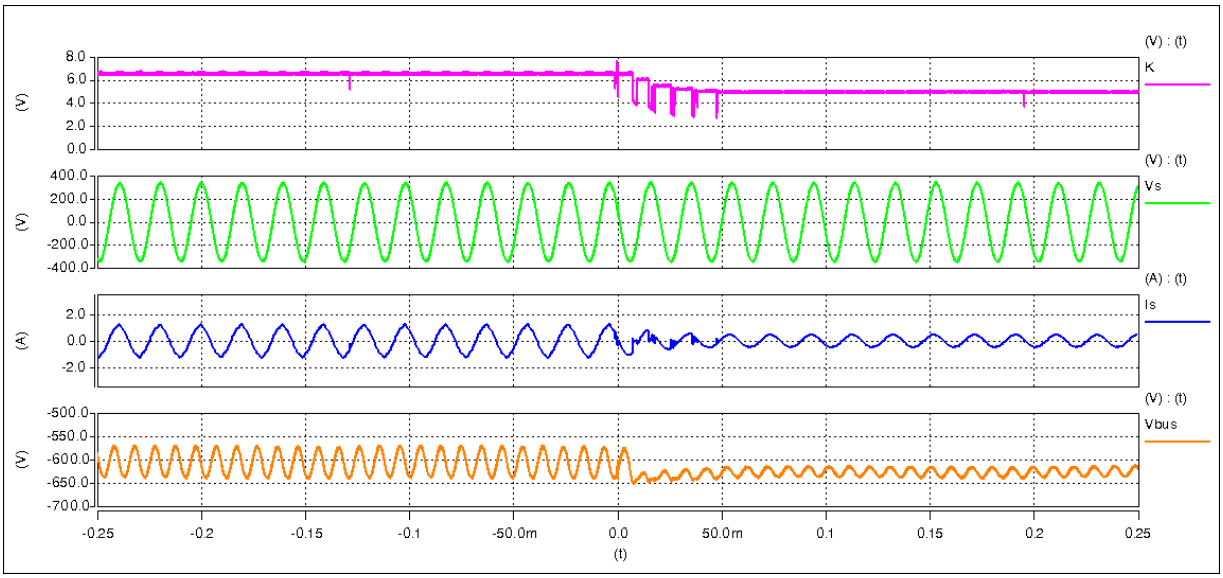


Figure 7-26 Experimental results of PFC output with a step load of 180 W to 60 W

7.12 Summary

This chapter details the design and development of a simplified critical conduction mode buck converter and its respective hysteretic controller to regulate the current through each of the HP LED strings. SABER simulations performed confirm the suitability of this approach prior to the prototype buck regulator being developed and tested.

A laboratory set up is shown for the evaluation of the performance of the HP LED power converter system and the bank of HP LEDs to achieve the 8,000 lm is tracked out and populated. The experimental results of the PFC stage are shown, revealing that the converter and the regulation band control operate as predicted. The 2nd harmonic of the input current is well within specified limits, and the regulation band control regulates the output PFC bus voltage with good transient response at the band limits and showing loop stability under steady-state conditions.

8 Conclusions and Further Work

8.1 Introduction

Power electronic development has always been driven by the advancement of new design techniques and emerging technologies. It is these innovations that have led to the recent advances in active power factor correction methods and the commercial release of high power light emitting diodes.

A comprehensive literature review identifies the main issues and requirements to successfully develop these technologies, input current harmonic limits are specified, power converter operating conditions are described, suitable power/control methods are reviewed, magnetic modelling techniques are identified and finally a discussion of the current development status of power components is included.

8.2 Summary of the Thesis

The merging of advanced power topology techniques and integrated magnetic approaches had led to the development of a single-stage, single-switch power factor corrector with an integrated magnetic component. A suitable power converter topology has been identified that can perform single-stage power factor correction and which can accommodate the integration of a complex magnetic component. This magnetic device combines the functions of a DCM boost inductor and a power transformer. Steady-state analysis of the power converter and state-by-state description of the operation provide an understanding of the complex waveforms and enabled the design and development of an integrated magnetic prototype. The construction of the IM ensured that the S^4PFC was able to operate unaffected by the IM whilst achieving optimum performance.

To confirm the operating principles and design of the converter and magnetic component, steady-state SABER switched modelling was conducted. The simulation also allowed the operating conditions of the magnetic core to be examined, in particular to check that the saturation limits were not exceeded. The simulation results correlated closely with initial design predictions and showed that the input current harmonics complied with regulations. Steady-state simulations did highlight however the limitations of the S^4PFC,

namely, under light load conditions, the boost voltage increases as it is not directly regulated by the controller.

Small-signal models of the S^4PFC were developed and the dynamic performance of the power stage was characterised by MATLAB simulations. The results showed that the control-to-output transfer function is similar to that of a non-isolated CCM buck converter, and the input-to-output transfer function, neglecting any input filtering, is similar to that of a DCM boost converter in series with a CCM buck converter. These dynamic characteristics suggest that a simple voltage-mode control can be implemented to perform output regulation. A PID control loop was designed and modelled using MATLAB and SABER which ensured that the S^4PFC was stable under transient conditions and had a fast transient response. A 180 W prototype S^4PFC with an IM was developed, and the measured results verified the theoretical and simulated steady-state operation and dynamic performance.

High power light emitting diodes offer numerous advantages over current lighting solutions in terms of light quality, efficiency and useful operating lifetimes. However one of the main factors limiting the take up of HP LEDs is the comparatively poor lifetime of many of the power electronic converters used to supply them which is due to the use of electrolytic capacitors to provide energy storage and hold-up capabilities.

In contrast metal film capacitors can operate for up to 100,000 hours, even over large temperature variations, but have significantly lower capacitance than electrolytics however they withstand much higher voltages. Therefore to realise the necessary energy storage requirements of a power factor correction stage, using long-lifetime capacitors, the output voltage of this stage must be increased.

A buck-boost topology operating in discontinuous current mode was identified as the most suitable topology for the HP LED PFC stage as it can achieve both automatic input current wave-shaping, limiting current harmonics, and provide a high output voltage. Steady-state analysis was performed to verify the approach, but indicated that due to the low PFC stage output capacitance, there was a significant twice-line-frequency voltage ripple at the output. As the input harmonic current limits are more tightly regulated for lighting equipment, a control approach was identified that would provide output regulation but would not process

the 100 Hz ripple voltage, thereby preventing the ripple voltage from propagating around the control loop and disturbing the input current.

A modified regulation band voltage mode controller was developed and designed. A SABER simulation was performed and analysis, based on the circle critereon was used to determine the stability conditions. MATLAB simulations verified this approach, and provided a basis for the design of a regulation band controller. SABER simulations of the regulation band controller and PFC stage validated the theoretical design.

To regulate the current through the HP LEDs, a secondary constant current buck regulation stage was developed and simulated. A 180 W prototype HP LED power factor corrector and constant current converter validated the theoretical and simulated predictions.

8.3 Contributions of this Research

To the best of the authors knowledge, there is no previously published work that examines an integrated magnetic component with a single-stage, single-switch power factor corrector. The analysis presented in this Thesis details the flux waveforms that occur within the core of the integrated magnetic in this topology. The solution that has been developed offers a well utilised core and optimised winding arrangement.

The dynamic analysis of the S^4PFC with an IM has not been undertaken previously. By determining the S^4PFC line-to-output and control-to-output transfer functions, suitable control approaches were identified and demonstrated.

To address the limited lifetime of current power supplies for HP LEDs, the author proposes a power topology and control solution that uses metal film capacitors instead of electrolytics for the PFC output stage, and the resulting increased output voltage ripple is regulated by adopting a modified regulation band control approach.

This controller regulates the PFC output voltage within defined limits, with a fast, stable response at these boundaries, whilst limiting the generation of the second harmonic input current. Circle criterion analysis is used to evaluate the dynamic performance of the regulation band control loop and the closed loop stability of the HP LED power system.

8.4 Future Development

Analysis and operating results of the S^4PFC indicates that due to the unregulated DCM boost output voltage and increased current though the MOSFET, this device is particularly stressed. Therefore the MOSFET that meets these requirements is invariably more expensive than that used in a two-stage PFC approach. As semiconductor technology invariably advances, then the piece cost of these devices will drop, making this approach much more attractive for future designers.

Due to the complex winding structure of the IM device for the S^4PFC, this approach may be unattractive due to cost and assembly considerations. An alternative construction approach would be to use planar magnetic structures, in which the windings are either etched on to PCBs or stamped out copper sheets. This approach overcomes the need for custom coil formers, and may also enable more rapid prototyping and automated assembly.

As HP LEDs become more widely used and as the size of HP LED strings increase, higher capacity power supplies will be required and further research is therefore needed to identify optimium solutions, for example to determine whether interleaved power factor corrector approaches can be realised using the regulation band controller. The possibility of current imbalances between the interleaved topologies must be examined, which might interfere with regulation, stability and input current harmonic content.

One possible alternative application of the HP LEDs is in communication systems where the LED string would pulse at high frequency, far beyond the range of human perception. Investigations need to be conducted as to whether the regulation band control approach is still suitable for this application.

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Appendix A

MOSFET losses are a combination of conduction losses due to on-state resistance, and switching losses. The conduction losses were realised by determining the normalised on-state drain-to-source resistance, $R_{ds_{on}}$ expressed as

$$R_{ds_{on}} = R_{ds_{on},@25^{\circ}C} \times R_{ds_{on},norm} \quad \textbf{A.1.}$$

and the RMS current flowing through the MOSFET during the on-time, DT_{sw} and $I_{Q,rms}$ is the rms current through MOSFET Q_1 and is given by

$$I_{Q,rms} = I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \quad \textbf{[126]} \quad \textbf{A.2.}$$

Figure A.1. shows and ideal plot of the transistor current.

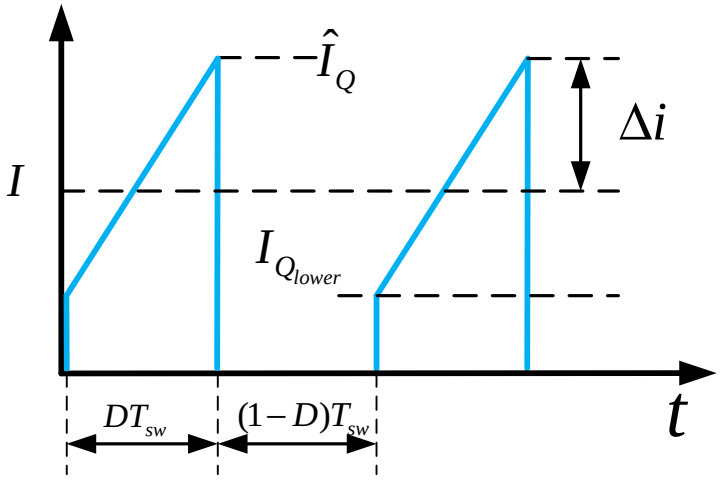


Figure A.1. Ideal transistor current, I_Q waveform

Conduction losses are now calculated using the following

$$P_{Q,cond} = I_{Q,rms}^2 R_{ds_{on}} \qquad \textbf{A.3.}$$

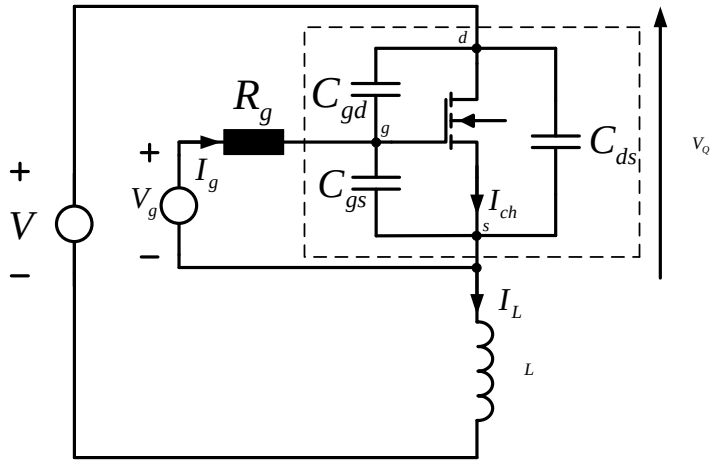


Figure A.2. Shows the parasitic elements of a typical MOSFET

The calculation of the MOSFET switching losses are more involved, as the devices parasitic elements contribute to the system, Figure A.3. shows the typical turn on/turn off current and voltage waveforms for a MOSFET operating in continuous current mode. It is this period of current and voltage crossover that determine the magnitude of MOSFET switching loss.

$$P_{Q,sw} = \frac{1}{2} I_Q V_Q (t_{off} + t_{on}) f_{sw} + \frac{1}{2} C_{oss} V_Q^2 f_{sw} \quad \textbf{[126]} \qquad \textbf{A.4.}$$

where I_Q, V_Q and f_{sw} are the MOSFET current, voltage and switching frequency respectively.

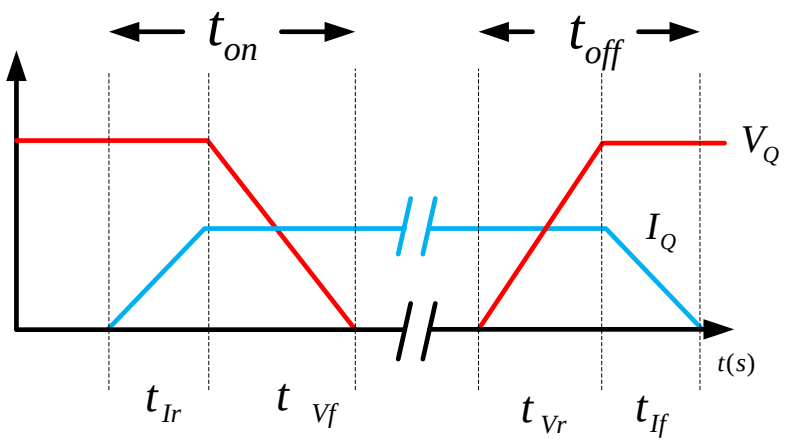


Figure A.3. Voltage and current waveforms of a MOSFET during switching transitions

The variables t_{on} and t_{off} are the turn-on and turn-off times of the MOSFET, and are estimated by

$$t_{on} = t_{off} = \frac{Q_{sw}}{I_g} \qquad \textbf{A.4.}$$

I_g is the MOSFET gate current and Q_{sw} is the gate switch charge. The output capacitance C_{oss} is defined by

$$C_{oss} = C_{gd} + C_{ds} \qquad \textbf{A.5.}$$

However, as the PFC stages are operating in DCM, the inductor current I_L has fallen to zero before the next MOSFET turn-on transient, therefore switching losses during this transition are non-existent.

As described previously the total MOSFET power loss is the combination of conducted and switching losses therefore

$$P_Q = P_{Q,cond} + P_{Q,sw} \qquad \textbf{A.6.}$$

Appendix B

The diode losses are a result of two mechanisms, forward conduction losses and switching losses. Conduction losses are defined by

$$P_{D,cond} = I_{D,rms} V_F \qquad \textbf{B.1.}$$

where V_F is the forward conducting voltage drop of the diode.

Losses as a result of the switching dynamics are more involved, but never the less a well understood process. During conduction the diode stores a minority charge of magnitude Q_s which is dependent on the forward current I_F, see Figure B.1. Before the diode can be reversed biased this charge must be removed. This charge dissipation occurs through two processes, firstly by passive recombination and secondly via active current reversal. The actively removed charge is Q_R and is defined by

$$Q_R = \frac{1}{2} t_{rr} I_{RM} \qquad \textbf{B.2.}$$

where t_{rr} is the reverse recovery time, and I_{RM} is the peak reverse recovery current defined by

$$I_{RM} = \sqrt{\frac{4}{3} Q_R \left(\frac{dI_F}{dt} \right)} = \frac{dI_F}{dt} \cdot \frac{t_{rr}}{S+1} \quad \textbf{[126]} \qquad \textbf{B.3.}$$

and S is referred to as the ‘snappiness factor’ of the diode, and is expressed as

$$S = \frac{t_b}{t_a} \qquad \textbf{B.4.}$$

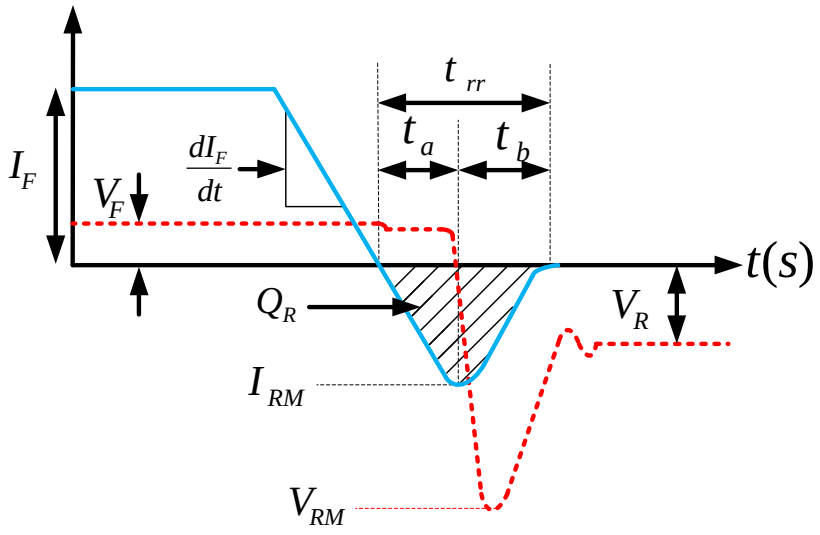


Figure B.1. Diode reverse recovery mechanisms during turn-off

During the reverse recovery time, t_{rr}, negative current flows through the diode yet the diode remains forward biased thus the instantaneous power loss is relatively high. The amount of stored charge, Q_s, that is recovered by this active process is dependent upon the rate $\frac{dI_F}{dt}$, the lower this rate enable a significant amount of the stored charge to recombine during diode turn off. Reverse recovery diode power loss can now be defined as a function of reverse recovery charge, Q_R, reverse bias voltage, V_R, and the switching frequency, f_{sw}.

$$P_{D,sw} = Q_R V_R F_{sw} \quad \textbf{[45]} \qquad \textbf{B.5.}$$

Thus total diode power loss is

$$P_D = P_{D,cond} + P_{D,sw} \qquad \textbf{B.6.}$$

Appendix C

The power dissipation for a capacitor is determined by

$$P_c = 2\pi f_{sw} C V^2 \tan\delta \qquad \text{[45]} \qquad \textbf{C.1.}$$

$\tan\delta$ is the dissipation factor of the capacitor and is determined as the ratio of the ESR to the capacitive reactance X_C, series capacitance.

$$\tan\delta = \frac{ESR}{X_C} \qquad \textbf{C.2.}$$

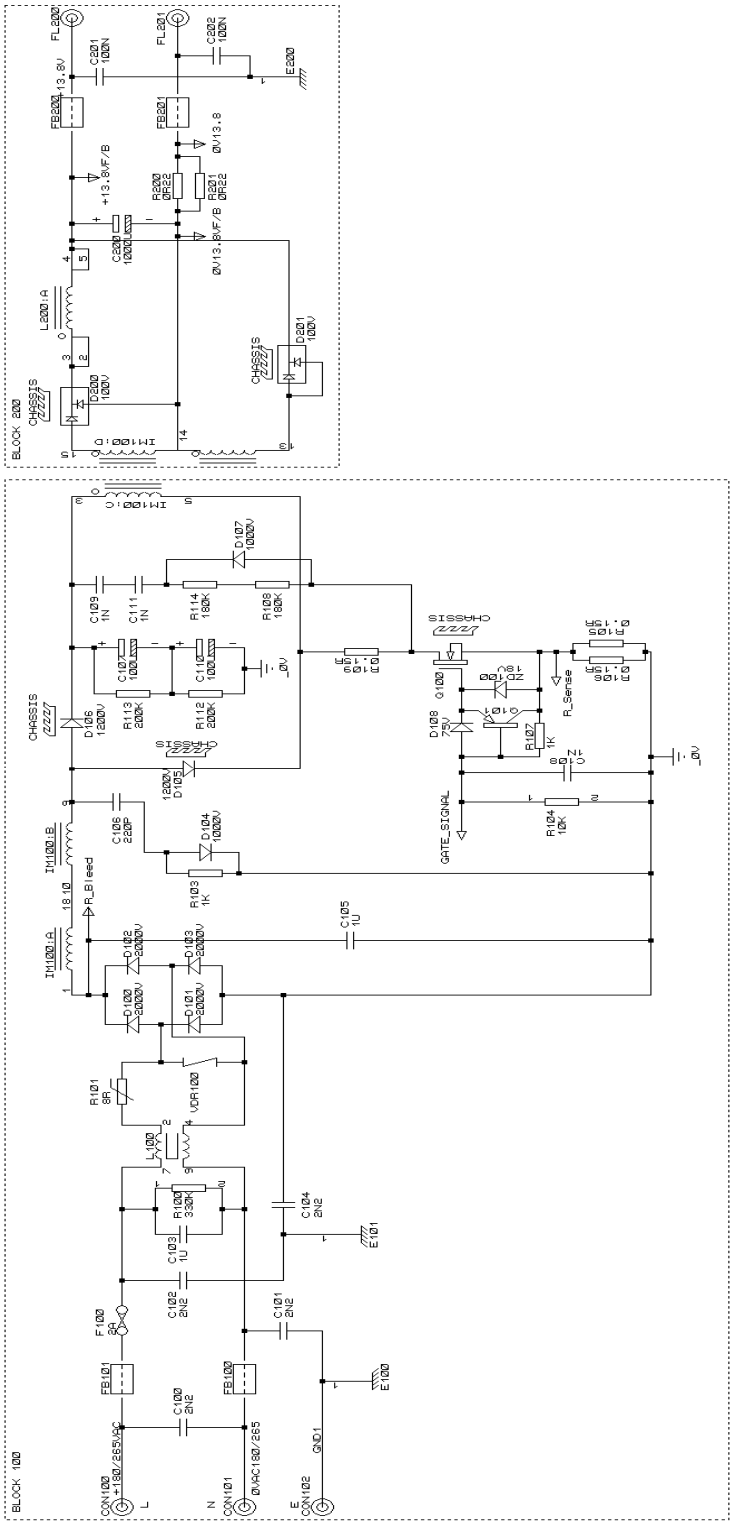
The dissipation factor reflects the polarisation losses of the dielectric film and the losses caused by the contact resistance of the terminals.

Therefore, rearranging **Eqn C.2.** for ESR:

$$ESR = \frac{\tan\delta}{2\pi f_{sw} C} \qquad \textbf{C.3.}$$

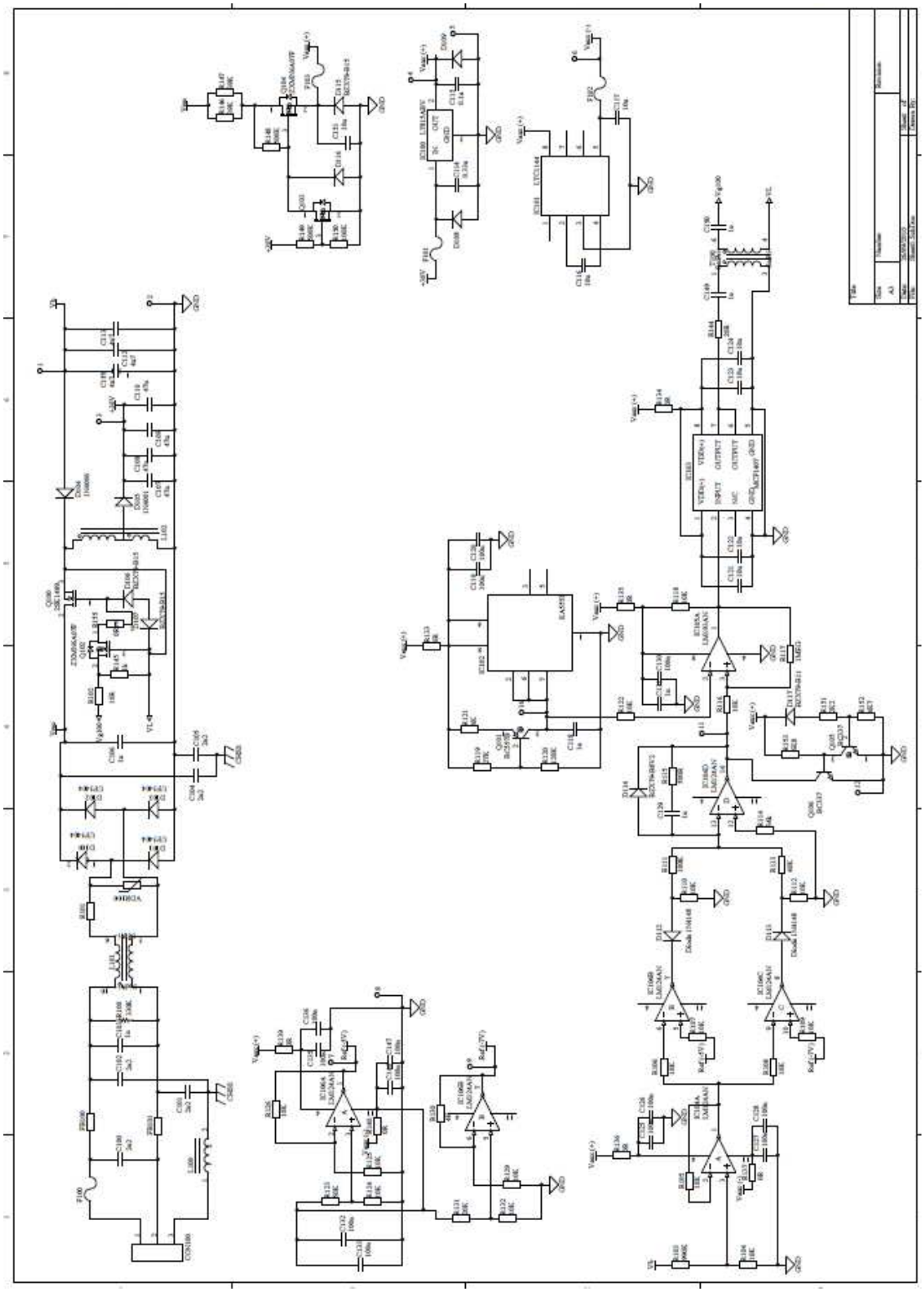
Appendix D

Single-State Single-Switch Power Factor Corrector schematic diagram



Appendix E

Power factor correction converter and control schematic diagram



Appendix F

HP LED current regulator and control schematic diagram