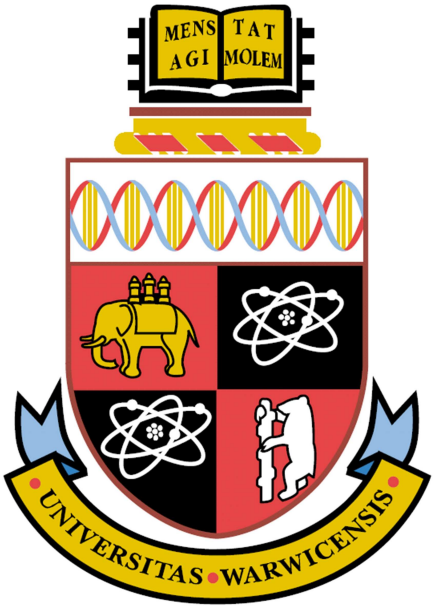
Development of SiC Heterojunction Power Devices



Peter Michael Gammon

Department of Engineering

University of Warwick

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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. Except where specifically stated, all of the work described in this thesis was carried out by the author or under his direction in the Department of Physics at the University of Warwick from September 2007 until May 2011.

P. M. Gammon
May 2011

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"The big question is this: How is the problem of high temperature going to be solved? What are the horses to put one's money on?... One approach is the logical sequence we see here: Ge, Si, SiC, C in that sequence"

William Shockley [1]

"God made the bulk; surfaces were invented by the devil."

Wolfgang Pauli [2]

"[Germanium] was a material studied only for its scientific interest; its complete uselessness fascinated and challenged me."

Gordon Teal [3]

"The only regret I have about the transistor is its use for rock and roll music"

Walter Brattain [4]

Publications

Patent

1. **P. M. Gammon**, A. Pérez-Tomás, and P. A. Mawby

   'Silicon Carbide Semiconductor Device'

   Patent No. 20110062450, Filed 15/09/2009

Journal Publications

1. **P. M. Gammon**, A. Pérez-Tomás, M. R. Jennings, O. J. Guy, N. Rimmer, J. Llobet, N. Mestres, P. Godignon, M. Placidi, M. Zabala, J. A. Covington, and P. A. Mawby

   'Integration of HfO2 on Si/SiC heterojunctions for the gate architecture of SiC power devices'

   Appl. Phys. Lett. 97, 013506 (2010)

2. **P. M. Gammon**, A. Pérez-Tomás, M. R. Jennings, V. A. Shah, S. A. Boden, .M. C. Davis, S. E. Burrows, N. R. Wilson, G. J. Roberts, J. A. Covington, and P. A. Mawby

   'Interface characteristics of n-n and p-n Ge/SiC heterojunction diodes formed by MBE deposition'

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3. **P. M. Gammon**, A. Pérez-Tomás, M. R. Jennings, G. J. Roberts, V. A. Shah, J. A. Covington, and P. A. Mawby

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2. **P. M. Gammon**, A. Pérez-Tomás, M. R. Jennings, O. J. Guy, N. Rimmer, J. Llobet, N. Mestres, P. Godignon, M. Placidi, M. Zabala, J. A. Covington, and P. A. Mawby

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4. M. R. Jennings, **P. M. Gammon**, A. Pérez-Tomás, V. A. Shah, M. C. Davis, S. E. Burrows, G. J. Roberts, P. A. Mawby

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   ISPS Prague 2008, IET Digest Vol 2008, P 69 (2008)

Abstract

Silicon carbide (SiC), with its wide bandgap, high thermal conductivity and natural oxide is a substrate that has given rise to a new generation of power devices than can operate at high temperature, high power and high frequency, though the material is not without its problems. SiC "heterojunction devices" are layers of germanium (Ge) or silicon (Si) that are deposited via molecular beam epitaxy (MBE) or wafer bonded onto the SiC surface. These narrow bandgap thin films can provide a high mobility channel region overcoming SiC's crippling channel mobility, which is most often made worse by a high density of interface states. Concentrating predominantly on Ge/SiC heterojunctions, this thesis characterises the physical and electrical nature of these structures, investigating the rectifying properties of the heterojunction interface and the ability of these layers to support a depletion region.

A physical analysis of the layers revealed that the Ge formed in an unexpectedly uniform fashion, given the large lattice mismatch involved. At a deposition temperature of 500^{o}C the Ge initially clumped into wide, shallow islands before merging, forming at best a 300 nm polycrystalline layer with a surface roughness of only 6 nm. This was in contrast to MBE deposited Si/SiC layers that formed tall islands that at 1 μm thick, still had not merged. After being formed into Ge/SiC heterojunction diodes they were electrically characterised. The layers displayed near ideal (η = 1.05) turn-on characteristics, low turn-on voltage (approximately 0.3 V less than Ni/SiC SBDs), reasonable on-resistance (12 mΩcm^2) and minimal leakage current. The devices were shown to suffer severe Fermi level pinning that defined the way the materials' bands aligned. This occurred as a result of an inhomogeneous interface that also caused fluctuations in the size of the Schottky barrier height across the interface. New characterisation techniques relating to these phenomena were applied to a heterojunction for the first time.

MBE formed Ge/SiC layers and wafer bonded Si/SiC layers were formed into MOS capacitors through the deposition of the high-K dielectric hafnium oxide (HfO_2). The increased conduction band offset between oxide and narrow bandgap semiconductor suppressed leakage problems often seen in HfO_2/SiC structures. Capacitance-voltage results showed that they could both support a depletion region, though the best results came from the MBE Ge/SiC diodes. Current-voltage results showed that the more uniform Si/SiC devices could block 3.5 MV/cm.

List of Abbreviations and Symbols

*i*Ge	Intrinsic Germanium
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BSE	Backscattered Electrons
c-AFM	Conducting Atomic Force Microscopy
C-V	Capacitance-Voltage
CMOS	Complimentary Metal Oxide Semiconductor
CTLM	Circular Transmission Line Method
CVD	Chemical Vapour Deposition
DI Water	Deionised Water
EDX	Energy Dispersive X-ray
FE	Field Emission
FIB	Focussed Ion Beam
FM	Frank-van der Merwe Growth Mode
HD	Highly Doped
HF	Hydrofluoric Acid
HIM	Helium Ion Microscopy
HVDC	High Voltage Direct Current
I-V	Current-Voltage
I-V-T	Current-Voltage-Temperature
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
M-S	Metal-Semiconductor
MBE	Molecular Beam Epitaxy
MIS	Metal-Insulator-Semiconductor
MISFET	Metal-Insulator-Semiconductor Field Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RCA	Radio Corporation of America

RHEED	Reflection High-energy Electron Diffraction
RIE	Reactive Ion Etching
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectroscopy
SK	Stranski-Krastanov Growth Mode
SOI	Silicon on Insulator
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TFE	Thermionic Field Emission
VW	Volmer-Weber Growth Mode
WB	Wafer Bonded
XRD	X–Ray Diffraction

Al	Aluminium
Al_2O_3	Aluminium Oxide
AlAs	Aluminium Arsenide
B	Boron
C	Carbon
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
HfO_2	Hafnium Oxide
Ni	Nickel
Sb	Antimony
SF_6	Sulphur Hexafluoride
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
Ti	Titanium

$\hat{U}_S$	sign ($\pm$) of U_S
$\hbar$	$h/2\pi$
A	Active Device Area (cm^2)
a	Lattice Constant $\mathring{A}$
A^{**}	Richardson Constant ($Am^{-2}K^{-2}$)
A_{eff}	Average area of a single patch of low SBH (cm^{-3})

c	Lattice Constant $\mathring{A}$
C_{Acc}	MOS Capacitance under Accumulation Biasing (F)
C_{Depl}	MOS Capacitance under Depletion Biasing (F)
C_{Inv}	MOS Capacitance under Inversion Biasing (F)
C_{Ox}	Oxide Capacitance (F)
C_{Series}	Series Capacitance of the Heterojunction Structures (F)
C_S	Semiconductor Capacitance (F)
d	CTLM: Distance between conducting pads (cm)
D_{GS}	Density of Surface States at the metal-semiconductor interface (cm^{-2})
D_{it}	Density of Interface Traps ($cm^{-2}eV^{-1}$)
E	Electric Field (V/cm)
E_0	Vacuum Energy Level (eV)
E_C	Bottom of Conduction Band (eV)
E_F	Fermi Energy Level (eV)
E_G	Semiconductor Band Gap (eV)
E_i	The Intrinsic Fermi Level (eV)
E_V	Top of Valence Band (eV)
E_{00}	Characteristic Energy (eV)
E_{CF}	Critical Field (MV/cm)
E_{CNL}	Charge Neutrality Level (eV)
h	Planck Constant (Js)
I_{leak}	Leakage Current (A)
I_r	Reverse Leakage (A)
J	Current Density (A/cm^2)
J_S	Saturation Current Density (A/cm^2)
J_{FE}	Field Emission Current Density (A/cm^2)
$J_{m\rightarrow s}$	Current Density from Metal to Semiconductor (A/cm^2)
$J_{s\rightarrow m}$	Current Density from Semiconductor to Metal (A/cm^2)
J_{TE}	Thermionic Emission Current Density (A/cm^2)
J_{TFE}	Thermionic Field Emission Current Density (A/cm^2)
k	Boltzmann Constant (1.381×10^{-23} J/K)
K_O	Dielectric Constant of an Oxide
K_S	Dielectric Constant of a Semiconductor
L_D	Debye Length (cm)
L_T	Transfer Length (cm)
m_n^*	Effective Mass of an Electron (kg)
m_p^*	Effective Mass of a Hole (kg)
N	Number low SBH patches
n	Intrinsic Free Electron Concentration (cm^{-3})
$n(x)$	Electron concentration at depth x from the surface (cm^{-3})
N_A	Acceptor (p–type) Doping Concentration (cm^{-3})

N_C	Effective Density of States in the Conduction Band (cm^{-3})
N_D	Donor (n–type) Doping Concentration (cm^{-3})
n_i	Intrinsic Carrier Concentration (cm^{-3})
N_V	Effective Density of States in the Valence Band (cm^{-3})
p	Intrinsic Free Hole Concentration (cm^{-3})
q	Electron Charge (1.602×10^{-19} C)
Q_M	Charge on a Metal (C)
Q_S	Charge on a Semiconductor (C)
Q_{GS}	Charge due to Gap States (C)
Q_{SC}	Charge within the Space Charge Region (C)
r_0	CTLM: Radius of inner conducting pad (cm)
r_1	CTLM: Radius of outer conducting pad (cm)
R_q	Surface Roughness (nm)
$R_{on,sp}$	Specific On-Resistance (Ωcm^2)
R_{sh}	Sheet Resistance ($\Omega/\square$)
R_T	Total Resistance (Ω)
S	Slope parameter verifying the Schottky-Mott principle
T	Temperature (K)
t_{on}	Time taken to switch on device (s)
U	Normalised Electrostatic Potential (eV)
U_F	Normalised Fermi Potential
U_S	Normalised Surface Potential
V_A	Applied Voltage (V)
V_B	Breakdown Voltage (V)
V_B	Breakdown Voltage (V)
V_{FB}	Flatband Voltage of a MOS Structure (V)
V_F	Voltage drop at a nominal current (V)
W	Depletion Width (cm)
W_T	Depletion Width Maximum (cm)
x	Distance from semiconductor surface (cm)
x_n	Edge of the n-type depletion region (cm)
x_o	Oxide Thickness (cm)
x_p	Edge of the p-type depletion region (cm)
$\mathrm{d}n$	The amount of SBH patches considered when extracting Φ_{eff}

β	The inverse thermal voltage: $\beta = q/kT$ (eV^{-1})
χ	Electron Affinity (V)
ΔE_C	The Heterojunction Conduction Band Offset (eV)
ΔE_V	The Heterojunction Valence Band Offset (eV)
η	Ideality Factor

γ_{lg}	Liquid-Gas Surface Tension
γ_{sg}	Solid-Gas Surface Tension
γ_{sl}	Liquid-Solid Surface Tension
μ_n	Electron Mobility (cm^2/Vs)
μ_p	Hole Mobility (cm^2/Vs)
ϕ	Electrostatic Potential within the Semiconductor of a MOS device (eV)
$\Phi^0_{B,n}$	Metal–Semiconductor Barrier Height (eV)
ϕ_F	Semiconductor Fermi Potential (eV)
Φ_M	Metal Work Function (eV)
ϕ_n	Fermi Potential measured from the conduction band ($(E_C - E_F)/q$) (eV)
ϕ_p	Fermi Potential measured from the valence band ($(E_F - E_V)/q$) (eV)
Φ_S	Semiconductor Work Function (eV)
ϕ_S	Semiconductor Surface Potential (eV)
Φ_0	The mean SBH (a statistical average) (eV)
$\Phi_{\eta=1}$	The SBH extracted at $\eta = 1$ of a η vs $\Phi^0_{B,n}$ graph (eV)
ϕ_{CNL}	Energy Difference between the E_V and E_{CNL} (eV)
Φ_{CV}	The SBH as extracted specifically by C-V analysis (eV)
Φ_{eff}	The Effective SBH (as in an I-V sweep) (eV)
Φ_{IV}	The SBH as extracted specifically by I-V analysis (eV)
Φ_{Rich}	The SBH extracted from a Richardson Plot (eV)
Ψ	Contact Angle of a Liquid on a Surface (^{o})
ψ_{bb}	Semiconductor band banding (eV)
ψ_{bi}	Built-in Potential (eV)
ρ	Charge Density (Ccm^{-3})
ρ_c	Specific Contact Resistance ($\Omega - cm^2$)
σ	The standard distribution of the SBH values about the mean SBH (eV)
ε_0	Permittivity of free space (8.854×10^{-14} F/cm)

Chapter

1 Introduction

The pace of scientific discovery in the 20th century was unrivalled by any that had proceeded it, making possible a complete transformation in the way we live our lives through the giant leaps forward in science, technology, engineering and industry. In the century's first year, a model was proposed by Planck to describe the emission of radiation from a black body [5], using his now famous packet, or quantum, of energy. This was the trigger for what was to come, first with Einstein's quantisation of light, then by Bohr who applied this theory to the atom, revolutionising our understanding of the materials world. Soon, contributions from de Broglie, Heisenburg, Schrodinger, Bloch and Pauli completed a distinctly European revolution of thought and understanding that had redefined the understanding of the physical world.

It was, however, the application of these fundamental ideas in America that led to their technological dominance, beginning with Bardeen and Brattain's first transistor [6], which was revealed at Bell Labs in 1947. Shockley's first field effect transistor [7] and Kilby's invention of the integrated circuit [8] followed, giving way to our modern information age. Now transistor based technology such as integrated circuits and computers dominate

our day to day life, enabling such exciting technologies as the internet and the smart phone, but also much more mundane things such as the washing machine, television or air conditioning. As such the semiconductor industry is massive, with sales predicted to be worth $325 billion for 2011, up 7% from the previous year [9].

As Shockley suggested back in April 1959, at the first International Conference on Silicon Carbide [1], the question of high temperature electronics requires us to look up the periodic table away from germanium (Ge) and silicon (Si) to the wide bandgap materials of Silicon Carbide (SiC) and diamond. However, these are difficult materials to work with and substrates of SiC were not commercially available until 1991 [1], whilst diamond substrates are still not readily available. Another wide bandgap material, Gallium nitride (GaN), is showing great promise for medium and high power applications [10]; however the major draw back of the material is that it is not freestanding, having to be grown on a substrate of either Si or SiC. As a result of these drawbacks with wide bandgap semiconductors, silicon still dominates the power discretes market, worth $12 billion in 2008 [11]. The only real challenge SiC places in this market is with the Schottky barrier diode, where devices are currently available [12] from 1 A/600 V up to 25 A/1700 V. However, in the future, the dominance of the Si IGBT at medium to high power might be challenged, with Cree having just released in early 2011 the first commercial 1200 V SiC MOSFET [13], while SemiSouth have a range of 1200 V and 1700 V normally-on and normally-off JFETs. As a result, the SiC market [11] was worth a comparatively tiny $23 million in 2008, chiefly through the blue L.E.D. market, though through the increased uptake of SiC power devices, this is predicted to rise to $100 million by 2015.

1.1 Motivation

The aim of this thesis is to fabricate, characterise and understand heterojunction devices that comprise a MBE formed Ge layer deposited onto a SiC substrate.

The initial motivation for what was to be a single experiment, was to compare the rectifying characteristics of MBE formed Ge/SiC heterojunctions to that of MBE formed Si/SiC heterojunctions produced previously at Warwick University [14–16]. Other Experimentation with Si/SiC heterojunctions took place at Swansea University [17] and in institutions in Japan [18–20], Germany [21–23] and the United States [24], leading to Si/SiC heterojunction rectifiers being used in Hybrid Car inverter circuits. Nissan amongst others [18], recognised that by controlling the doping of the heterojunction layer, one may adjust the turn-on voltage and reverse characteristics to suit the needs of a particular device, whilst maintaining the high power, high frequency capabilities that made SiC so popular in the first place.

A seemingly natural step following Warwick's previous experimentation with MBE formed Si/SiC, was to attempt to repeat some of these techniques using Ge as the heterojunction material on SiC. Based in the Physics department at the University, the MBE capability facilitated doped Si and Ge deposition, and hence a set of experiments were planned. The use of Ge was of particular interest due to its high mobility and its narrow band gap which, when paired with SiC's wide bandgap was expected to form a good rectifying contact. However, whilst rectification was almost guaranteed, the really tantalising prospect was that of a SiC MOSFET with a Ge-based, high-mobility channel. If successful, this could overcome two major problems with the SiC MOSFET, its poor mobility and the carrier scattering that occurs at the silicon dioxide (SiO_2) interface.

1.2 Thesis Outline

The following Chapter introduces SiC and SiC heterojunctions in the context of the major challenges that face the power electronics industry today. The power devices relevant to this work are presented before we see how SiC is extending their range into high temperature and high power operation.

Chapter 3 presents some of the concepts required to understand the results Chapters, introducing first the band alignment of heterojunctions and the flow of current over a Schottky barrier, before looking at heteroepitaxial growth and how layers form when they are being deposited onto another semiconductor surface. Similarly introductory, Chapter 4 presents the many physical and electrical characterisation techniques that are used to extract information about the heterojunction layers and diodes.

In Chapter 5, the MBE deposition onto SiC of first Si and then Ge is described, presenting the results of layers that have been formed under varying temperatures and thicknesses and with different dopants. The full physical characterisation of each layer aims to establish the surface uniformity and crystallinity through the use of high resolution TEM, AFM, helium ion microscopy and FIB/SEM images, and XRD and EDX crystallographic analyses.

Chapter 6 describes how the Ge/SiC heterojunction diodes were fabricated using clean room equipment and processes. A full electrical characterisation involves circular transmission line measurements to extract contact resistivity and current voltage analysis at room temperature and at 25 K steps from 225 K up to 450 K to extract information about the turn-on voltage, barrier height, ideality factor, reverse leakage and breakdown. C-V analysis is carried out to further assess barrier height and doping concentration but is quickly discredited in the face of surface states.

Some unusual results extracted about the Schottky barrier height in Chapter 6 require much more exploration, so Chapter 7 presents some more advanced characterisation methods adapted for the first time for heterojunction analysis. Fermi level pinning of the heterojunction interface is described, as well as fluctuations in the SBH brought about because of the inhomogeneous Ge/SiC interface. Finally, a model is proposed to describe why the doping of the Ge layers appears to make little or no difference to the devices' forward characteristics.

The final Chapter of results, Chapter 8 describes how MBE Ge/SiC and wafer bonded Si/SiC heterojunction layers were made into MOS capacitors, by the deposition of the high-K dielectric hafnium oxide. The structures are analysed using current-voltage tests, which show the leakage of the devices. Capacitance-voltage tests and the fitting of models to the data enables the extraction of interface trap densities, whilst describing how a depletion region spread across the heterojunction interface.

A summary of the results and the conclusions are presented in chapter 9. Suggestions are made for further research, which would further advance the understanding of these and other heterojunction devices.

Chapter

2 The Power Electronics Hierarchy

2.1 Introduction

In this thesis, Ge/SiC heterojunction diodes are characterised in an attempt to overcome challenges that face the wide-bandgap semiconductor SiC, a material starting to make a real impact in the power semiconductor industry. However, this is a difficult concept without a frame of reference, and therefore, this Chapter aims to frame the research presented herein by breaking down today's biggest power engineering challenges into their constituent parts, showing how materials science research at the bottom most rung might impact all the way up the chain to the wind turbines and electric cars.

Figure 2.1 shows a Power Electronics hierarchy, beginning with three of the most relevant challenges to today's industry. The requirements of these systems will be discussed, before breaking the technology down layer by layer, passing through the systems, circuitry and devices until the materials are met. At this point SiC and its many successes and challenges will be introduced before moving on to the state-of-the-art SiC heterojunction research.

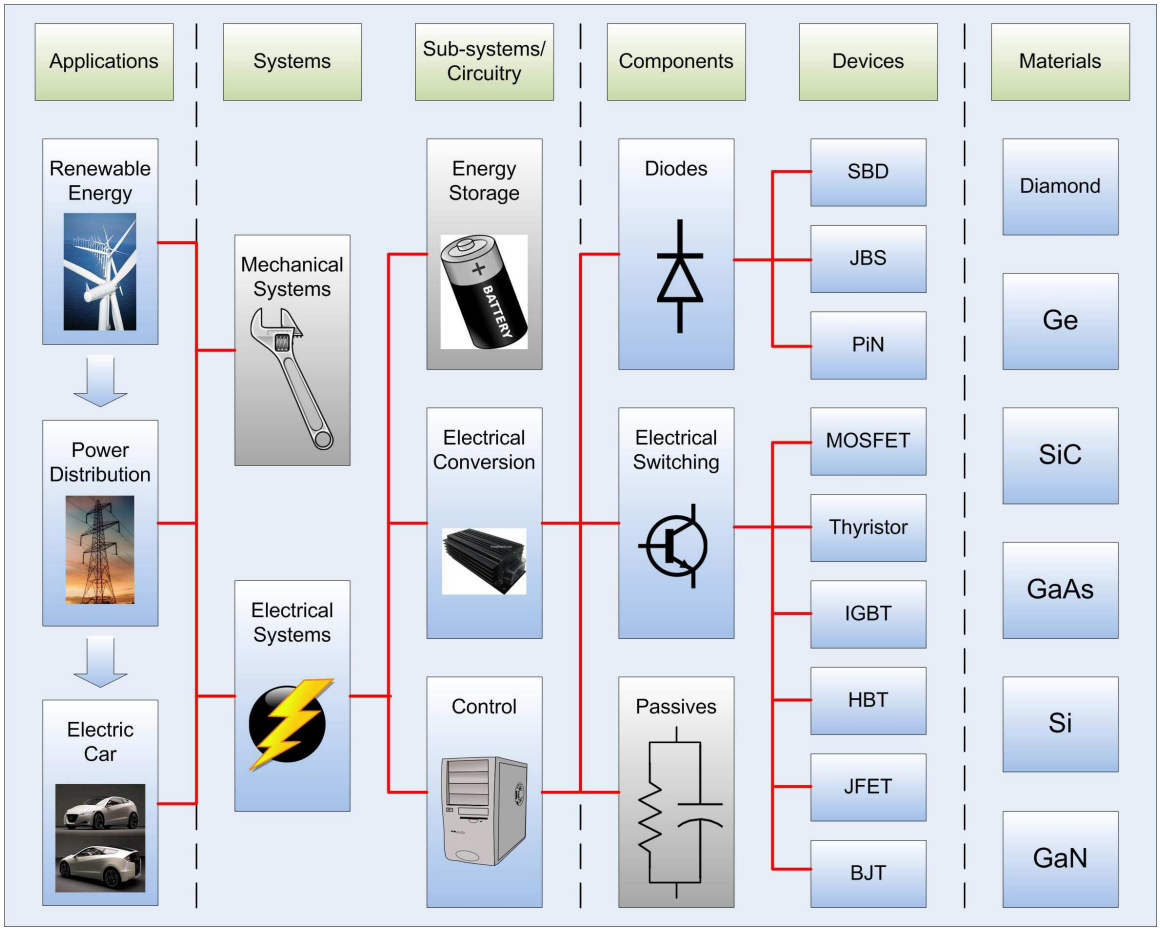


Figure 2.1: The power electronics hierarchy, from applications and systems to devices and materials.

2.2 The Systems

Renewable energy is the future of power generation and currently the only truly clean form of energy generation with Nuclear Fusion still a long way from fruition. Excluding biofuels, renewables including wind, solar, wave and hydro powers accounted for just 6 % of the global final energy consumption in 2009 [25]. Wind power accounts for a large proportion of the renewables market and at the time of writing, the UK had 3157 turbines, with a maximum output capacity of 5.2 gigawatts (GW) of power [26], some 5 %

of the national requirement. Being ideally positioned for offshore wind generation, just under 4 GW of construction projects were under way, with another 5 GW given the go ahead, and 8 GW in the planning stages [26]. These impressive figures show that this is a huge, expanding industry, and power electronics plays an important role in optimising the turbines. Beginning with the hugely variable energy supply of the wind, energy must first be transferred from mechanical, rotational power to electrical power through a gearbox and generator. This must then be transformed onto the correct AC rating to be placed on the national grid, therefore requiring efficient bi-directional DC-AC converters at the systems level of Figure 2.1.

Once onto the grid, the efficient and appropriate distribution of electrical power is the next challenge. A recent buzz-word, the smart grid is an ideology that encompasses a number of technological challenges that have a common theme of providing power in a fashion that reduces cost, saves energy and improves reliability. At the forefront of this idea is the increased use of control systems, smart meters in homes that can communicate power requirements immediately back to the national grid and to the suppliers, thus regulating output with up-to-the-minute demand. This is the popular face of the smart grid idea; however, the true "smart" network needs more. Power, like so much else, is becoming an international affair, with the national grids all over Europe connected up. However, each A.C. grid has its own requirements in terms of transmission frequencies and powers. This means that each nation's grid must be joined to the next by converting the A.C. to D.C. and back to A.C. again. Seeing that DC power is generated at the power stations and that most domestic products are D.C., one has to ask, why are we not using a D.C. grid? Significant progress has been made in the field of high voltage D.C. (HVDC) distribution and it is now the most energy efficient way to transmit power over long distances. Many international HVDC cables already exist such as those linking

Britain with France, Scotland with Northern Ireland, as well as many other connections across Europe and the globe. At the moment however, the significant cost of these systems has prevented HVDC being rolled out as a national grid. With a HVDC national grid off the cards for the foreseeable future, the use of more efficient, smaller, cheaper and lighter power conversion solutions is essential. Hence in a similar conclusion as the last paragraph, the efficiency of DC-AC, AC-DC and DC-DC converters are essential.

After the power has been generated, transmitted and distributed, we end up with it in our homes, and the role of power electronics does not end. It crops up in all our electronic equipment converting the 220 V 50 Hz A.C. supply down to the 5, 9 or 12 V DC the T.V., computer or radio requires. However looking again to the future, it is likely to be our domestic energy supply that powers our mobility, and it is the electric car in particular that has so much to be won and lost in the quality of its electronics. The biggest challenge currently facing the full electric car market is actually energy storage, as it is the absence of a small and lightweight, but high capacity battery that prevents the electric car getting further than their current 100 mile range [27]. As well as this so called "Range Anxiety", the biggest criticism of electric cars is the fact that they are only as green as the electricity supply. This neatly brings us full circle in our demand for greener energy, reiterating the previous need for investment in renewables. Currently these limitations hold us back from using full electric vehicles, but hybrids are becoming ever more popular, with several on the market already [28]. In both full electrics and hybrids we return to our recurring need for efficient power conversion as these cars require an efficient inverter to convert stored D.C. charge into the A.C supply powering the motor. Of course in reverse, as the motor is acting as a generator, the opposite is true and the A.C. needs to be rectified to D.C. for storage.

2.3 Circuitry and the need for device efficiency

The need for efficient energy conversion is clear then; the efficient switching of energy from one form to another is an issue that impacts on all the green technologies that will become so prevalent over the next 50 years. But what makes an inverter, a rectifier or a DC-DC converter efficient? Figure 2.2 shows the simplest inverter circuit, where the application of a trigger to transistors 1 and 4 allow current flow one way through the load, whilst the triggering of 2 and 3 forces it through in the opposite direction. The use of pulse width modulation and some smoothing circuitry offers the opportunity to reduce the harmonic frequencies in this circuit after smoothing, hence creating an AC signal such as the dotted line in Figure 2.2. The peak-to-peak amplitude of the resulting A.C. signal is twice the DC current, whilst the frequency is controllable by the devices' switching speed. The diodes in this circuit prevent any inductive reverse current from the load damaging the transistors. Further detail on this and more complex converters may be found in [29].

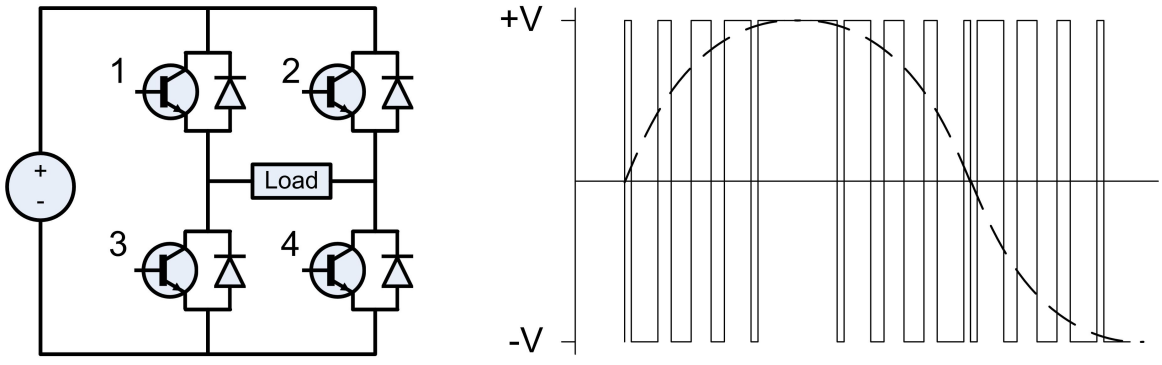


Figure 2.2: An inverter circuit and the output across the load before and after smoothing.

For efficient circuit performance, one needs efficient device performance, minimising

loss in power. When 'off', the transistors and diodes must block all current and when on, they should conduct losslessly; they would also switch between these states as quickly as possible. However, real devices have real practicalities, and the above statements often contradict each other leading to trade offs and compromise. Whilst typical inverter efficiencies will be in the high nineties of percent, every fractional increase in this value represents a significant saving in energy and money, especially when a typical supply chain contains multiple energy conversions.

2.4 Devices

To outline the following discussion, the following is a general list of requirements for a diode in this circuit:

1. The diode must be capable of blocking a voltage up to V_B.
2. Reverse leakage current must be below a value I_r at V_B.
3. Specific forward resistance must not exceed $R_{on,sp}$.
4. The forward voltage must not exceed V_F for at a nominal current e.g. 1 A.
5. The time taken to switch between V_B and V_F must not exceed t_{on}.
6. The device must work up to a temperature T.
7. Device area must not exceed A.
8. Costs including materials and processing must not exceed $£X$.

The problem with this list is that the modification of a given physical characteristic will improve one of these requirements, but often at the detriment of another. This includes the choice between unipolar or bipolar operation, device thickness, Schottky barrier height (SBH), and most specifically material, which affects all of the above. Before looking at the impact of materials in the next Section, here, three common diode devices will be

introduced showing how they satisfy the above list, before the common transistors are also featured.

2.4.1 Schottky Barrier Diodes

Unlike the bipolar devices featured later, SBDs rely on only majority carriers for their operation. This allows for a very fast operation as the switch from a conducting state to a blocking state or vice versa involves no electron-hole recombination, a relatively slow process. This unipolar behaviour also dictates that the SBD's place in the power market is at the low-medium blocking voltage end, with commercial silicon devices available capable of blocking up to 200 V, whilst commercial SiC diodes are available up to 1200 V. This is because the one-sided depletion region that forms at a metal-semiconductor interface cannot support the same electric field in a given thickness as that of a p-n junction, whilst V_F tends to soar at higher SBD blocking voltages. A large V_B in a SBD is reliant on a thick epitaxial layer of low-doped semiconductor beneath the metal. Unfortunately, the same thick layer will add a significant $R_{on,sp}$, and this is a common place trade-off as one can have a large breakdown or low resistance, but not both.

Another trade off exists in the size of the SBH. A large SBH presents a large hurdle to a reverse leakage current, and hence this is minimised. However, the larger the SBH, the larger the amount of voltage require to turn the device on. Given that the choice of metal (or indeed heterojunction layer) controls the height of the SBH, the selection of the correct metal is a matter of optimising each property for the given application.

SBDs feature heavily throughout this thesis, similar as they are to the heterojunction SBDs formed and analysed in Chapters 6 and 7. The theory behind these devices is presented in Appendix A.5.

2.4.2 PiN Diodes

A significant switch in parameters sees unipolar action swapped for bipolar action, PiN diodes exploiting a lightly doped intrinsic region between a highly doped p-n junction to support large breakdown voltages at reasonable values of V_F. The highest breakdown voltages are attainable due to the high level injection of minority carriers into the intrinsic region, which vastly reduces the $R_{on,sp}$ of the otherwise resistive low doped layer [30].

As suggested before, the weaknesses of the SBD tend to be the strengths of the PiN diode and vice versa, so the use of bipolar action is synonymous with low resistance and high breakdown, but very slow switching due to the need to extract the slow minority carriers from each layer. Commercial Si PiN diodes are available up to a V_B of 20 kV; however it is expected [30] that SiC devices will replace the Si devices for blocking voltages upwards of 2 kV thanks to their very low V_F. SiC has been shown to support voltages of up to 20 kV [31], though these still suffer from forward voltage drift [32].

2.4.3 JBS Diodes

The junction barrier Schottky (JBS) diode mixes Schottky contact regions on an N-drift region with P+ stripes or dot regions forming localised pn junctions [33]. Designed as a halfway house between the PiN and Schottky diodes, the (JBS) diode specifically exploits its bipolar features in the reverse direction where blocking and leakage is improved compared to a regular SBD, though at the cost of some speed and V_F increase. This becomes another application based balancing act, where the separation of the p-type regions have to be separated sufficiently far to allow maximum metal-drift region contact to form free of the p-type regions, minimising V_F. However, in the reverse they should be as close as possible to prevent the build up of electric field at the metal-semiconductor

interface and minimise reverse leakage [34].

2.4.4 Transistor Devices

Having a set of trade-offs very similar to that of the diode devices, the choice of transistor is often based on balancing a range of characteristics for a given application. One must again choose between unipolar and bipolar, with the former offering speed and minimal losses, whilst the latter offers huge blocking and low resistance.

The unipolar metal-oxide-semiconductor field-effect transistor (MOSFET) is the most common and well known transistor, featuring as it does in complimentary MOS (CMOS) technology. CMOS is the mainstay technology in the microchips, processors and computers that have revolutionised modern day life. The MOSFET, pictured in Figure 2.3a, is based on Shockley's field-effect [7], whereby the application of a positive voltage to the gate (the metal of a MOS structure) forms a region depleted of majority carriers at the surface of the semiconductor. The depleted region is as a high mobility, low resistance channel for electrons to pass from the n-type source through to the n-type bulk and drain. With no applied voltage to the gate, the p-n-p structure between source and drain should suffice in blocking all but the smallest leakage currents.

Its use in CMOS has made the Si MOSFET the most advanced semiconductor device, with Intel's latest chipset using channel regions just 32 nm across. As well as its success in the low power, fast switching situations, there are a number of structures that allow the MOSFET to support large blocking voltages. One of these is the vertically diffused (VD) MOSFET, pictured in Figure 2.3a, where the use of a lightly doped drift region has the same effect as it does in a SBD, providing a region that builds electric field and hence V_B at the expense of $R_{on,sp}$. This drift region can be built up laterally rather than

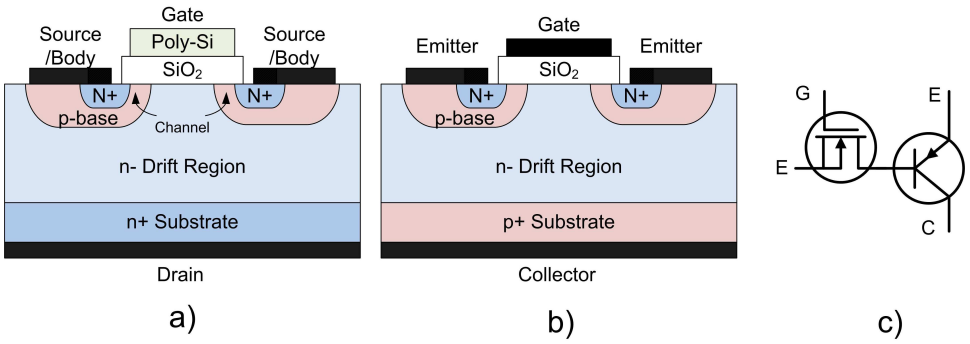


Figure 2.3: a) A standard vertically diffused n-type MOSFET, b) a symmetric IGBT and c) an IGBT equivalent circuit.

vertically, and laterally diffused (LD) MOSFETs involve a top contact drain, with the drift region situated between the drain and the channel.

For very high voltage, low frequency operation, the Si Insulated Gate Bipolar Transistor (IGBT), pictured in Figure 2.3b is the current device of choice. The structure of an IGBT is quite easily pictured as being similar to the VDMOS structure but with the n+ substrate exchanged for a p-type one. Shown in 2.3c, this creates a bipolar p-n-p transistor structure between the source and the drain, with the n-drift region acting as the base contact to this structure. Therefore, applying a positive voltage to the MOS gate and the collector causes bipolar conduction between the collector and emitter, a high level injection of holes into the n-drift region from the collector causing a low resistance bulk region.

In this thesis, the MOS gate is most relevant, featuring heavily in Chapter 8. The vast detail of transistor operation is beyond the scope of this text. Further information on the operation of the MOSFET and IGBT devices, and also Junction FETs, bipolar junction transistors and thyristors may be found in [30, 34–36] whilst their use in power circuitry may be found in [29].

2.5 The Semiconductors

The final step on the power electronics hierarchy of Figure 2.1, the materials are the focus of the majority of this thesis. Referring back to the list of requirements for a power device in Section 2.4, every requirement in this list will be affected by the material choice. The traditional semiconductor material silicon is the staple material for SBDs, PiN diodes and MOSFETs; however, the emergence of wide bandgap semiconductors such as 4H-SiC is beginning to dent Si's dominance. Already, Cree [12] offer SiC SBDs with 1200 V blocking capability, while Si languishes down at 200 V. Semisouth [37] also offer 1200 V JFETs designed to replace Si MOSFETs and IGBTs of the same rating due to the low $R_{on,sp}$, fast switching speeds and high temperature performance of SiC.

Table 2.1: The material properties of Si, Ge, 4H-SiC, 3C-SiC and GaN at 300 K.

Property	Units	**Ge**	**Si**	**3C-SiC**	**GaN**	**4H-SiC**
Physical Properties						
Crystal Structure		Diam.	Diam.	Z-B	Wurt.	Wurt.
Lattice Constant, a	$\mathring{A}$	5.658	5.431	4.360	3.189	3.073
Lattice Constant, c	$\mathring{A}$				5.186	10.053
Density	$\mathrm{gcm^{-3}}$	5.323	2.329	3.166	6.150	3.211
Thermal Conductivity	$\mathrm{Wcm^{-1}K^{-1}}$	0.58	1.3	3.6	1.3	3.7
Thermal Expansion	$\mathrm{10^{-6}K^{-1}}$	5.9	2.6	3.8	3.17	4.3
Melting Point	°C	937	1412	3103	2500	3103
Electron Eff. Mass, m_n^*	g	$0.22m_0$	$0.36m_0$	$0.35m_0$	$0.20m_0$	$0.37m_0$
Hole Eff. Mass, m_p^*	g	$0.34m_0$	$0.81m_0$	$0.60m_0$	$1.5m_0$	$1.0m_0$
Electrical Properties						
Bandgap Energy, E_G	eV	0.66	1.12	2.36	3.20	3.23
Dielectric constant, K_s		16.2	11.7	9.72	8.9	9.66
Electron Affinity, χ	eV	4.0	4.05	4.0	4.1	4.05
Electron Mobility, μ_n	$\mathrm{cm^2V^{-1}s^{-1}}$	3900	1400	800	1000	900
Hole Mobility, μ_p	$\mathrm{cm^2V^{-1}s^{-1}}$	1900	450	320	350	120
Critical Field, E_{CF}	$\mathrm{10^6Vcm^{-1}}$	0.1	0.3	2-3	5	3-4
Elec. Sat. Velocity v_{sat}	$\mathrm{10^7cm\ s^{-1}}$	0.65	1.0	2	1.5	2

Table 2.1 contains a list of semiconductor properties, both physical and electrical, for the narrow-band semiconductors, Si and Ge, and the wide-bandgap semiconductors 4H-SiC, 3C-SiC and GaN. Each material has an individual set of parameters, a band gap, mobility, critical field and thermal conductivity, that all combine to position it within the semiconductor industry.

Germanium (Ge) is a semiconductor with a very narrow band gap at only 0.66 eV. As a result, it has a very high concentration of electrons in the conduction band at room temperature making it an excellent conductor at low temperatures. Furthermore, its mobility values are very high as a result of the low carrier masses. The downside is that at raised temperatures, there are too many electrons in the conduction band and the material acts like a metal. Also, the maximum electric field that a semiconductor can withstand before breaking down is connected to the energy gap, and hence Ge, with the lowest bandgap and critical field, can only be considered a low-power material.

Silicon (Si), is probably the best balanced semiconductor for room temperature operation. With a band gap of 1.12 eV, it has reasonably low losses and sufficiently high breakdown properties. Also, its reasonable mobility and its natural oxide in silicon dioxide have resulted in its dominant position in the semiconductor market. However, it does not support the same high temperature, high power operation that SiC does due to its comparatively low critical field, hence explaining the difference in breakdown voltages achievable between Si and SiC SBDs - 200 V and 1.2 kV.

2.5.1 Silicon Carbide

SiC is hailed as the semiconductor most likely to replace Si in “high temperature, high frequency and high power applications” [38]. This statement appears at the start of the

majority of papers concerning SiC as a semiconductor. The properties that prompt this commonly used statement are listed within Table 2.1. First and foremost is its wide bandgap, which at 3.26 eV is nearly three times that of Si. This means that at any given temperature far fewer electrons can cross from the valence band to the conduction band, resulting in a low intrinsic carrier concentration (n_i) within SiC at room temperature. Si and Ge's high n_i prevents them operating at high temperature as the flood of carriers in the semiconductors promote behaviour resembling that of a metal. The onset of this problem in SiC happens at hundreds of degrees higher than that of Si - in fact, given Equation A.4 in the Appendix, the n_i experienced by Si at room temperature will not be reached until around 700^{o}C. Taking into account the material's thermal conductivity, which is nearly three times Si's, SiC is clearly a material for high temperature operation.

The high power and high frequency statements, both stem from SiC's ability to support a large electric field, as given by the material's critical electric field (E_{CF}) of 3 MV/cm, twelve times that of Si. A semiconductor will breakdown at a voltage proportional to the square of E_{CF}, hence it is has a huge capacity to support a voltage, hence its high power credibility. A weakness of SiC is its low carrier mobility which is particularly poor as a p-type material, which leads to a high resistance for a given thickness of SiC. However, the majority of a device's resistance will be dropped over its low doped epitaxial layer its drift region. As SiC can support a greater electric field per μm of epi-layer, the layer can be made much thinner for a given blocking voltage, leading to a low on-resistance. This, combined with the material's superior electron saturation velocity, results in low switching losses.

The potential of the material is clear, yet the truth remains that at the time of writing, 20 years after the first commercial 6H-SiC wafer was produced [1], only SiC SBDs are established within the power market [12], though a range of FETs are new to the market

[37]. Furthermore, in 2008 power electronics accounted for only a small portion of the SiC market lagging way behind the LED market that dominates more than 80% of the market. The slow adoption of SiC is a reflection on the challenges that SiC has had to overcome, and those it still faces. The multifarious reasons for this include substrate quality and cost, technological issues including most specifically a low carrier mobility made worse by the oxide quality and the slow adoption by companies that require extensive process qualification.

Crystal quality was the first challenge, particularly micropipe defects, which were to be found at a density of 1000 cm^{-2} in the first wafers. Formed via the convergence of several smaller screw dislocations or by contamination during the crystal growth, micropipes form as a hollow core penetrating the entire wafer along the c-axis [38]. Just one of these micropipes located within the active area of a device will ruin its operation, hence SiC device yield is reliant on the micropipe density being close to zero. It is only since 2007 that, thanks to the advance in materials processing techniques [39], Cree have been able to sell a premium range of 100 mm wafers that are guaranteed to be micropipe free [40]. Their standard SiC wafers still only guarantee a micropipe density of 15 cm^{-2}, which is still too high to produce a good yield of many of the large area, high current devices. As an example, to achieve an 80% yield of 50 A Schottky diodes, one would require a micro pipe density better than 2 cm^{-2} [38].

Compounding the raw materials issue is the SiC wafer cost. Given a like for like low current (<10 A) device, SiC is some 10-15 times more expensive than Si, a situation which can only improve with greater competition, demand and substrate size. Competition is increasing, with II-IV, Tanke Blue, Rohm and Norstel now all producing viable SiC substrates. Demand is rising, thanks largely to the success of the SiC SBD. However, demand is unlikely ever to reach Si levels, so some cost differential is always likely to be

maintained. In this sense it will be important for SiC to justify the cost difference, proving the savings that can be made in terms of energy saving in the end product, an inverter for example. Addressing the substrate size, Cree are expected to release a 150 mm wafer in the not too distant future [41], though for comparison, the Si industry are at a similar stage of development for a 450 mm technology, with 300 mm the current standard.

The technological issues are perhaps the biggest barrier that remain, as a proven SiC MOSFET would likely trigger a rise in demand and quality, and a drop in costs. However, significant hurdles remain, and the most significant of these is finding a quality oxide solution on SiC. Problems with reliability, threshold voltage drift and failures at high temperature are all significant. Furthermore, the large density of interface traps (D_{it}) at the metal-oxide interface cause a large reduction of SiC's already low channel mobility.

This flawed oxide was originally considered one of the key benefits of SiC, the materials high Si content meaning that when the surface was oxidised, SiO_2 could form. However, the presence of the carbon has become a real hinderance as it is not simply being removed via the oxidation process in the form of CO or CO_2, as one might expect [42]. Instead, it is building up at the SiO_2/SiC transition region, perhaps as immobile carbon di-interstitial clusters [43]. The C:Si ratio has been shown [44] to reach 1.2 in the SiO_2/SiC transition region, which is some 6-25 nm wide depending on the processing technique. Interestingly, the same work shows that channel mobility is inversely related to the width of this interface region, with the nitric oxide (NO) treated interface that produced an interface region of only 6 nm having a highest mobility at 29 cm^2/Vs. Over the last 15 years, various methods have been used to try and suppress the D_{it} values and raise mobility, including the post oxidation anneals in NO [44–47] and N_2O [45,48]. The greatest success purely in terms of mobility [48], saw the gate oxide grown in sintered alumina [49], producing a mobility of

150 cm^2/Vs; however this is still only 15% of the bulk value. Furthermore, the presence of sodium within the oxide caused severe device instabilities during negative gate bias stressing [49].

Further problems arise from the low dielectric constant of SiO_2, at $\varepsilon_{SiO_2} = 3.9$. Gauss' law ($\nabla \cdot \varepsilon\varepsilon_0 \overrightarrow{E}$) means that the product $\varepsilon_{SiO_2} E_{CF,SiO_2}$ should exceed $\varepsilon_{SiC} E_{CF,SiC}$ if SiC is to reach its full critical electric field. With SiC having a dielectric constant of 10, SiO_2 must be capable of withstanding 7 MV/cm to match the potential of SiC. In theory, SiO_2 has a breakdown electric field of only 0.8 MV/cm [38] and hence investigations with other oxides with large dielectric constants (High-K) have been investigated as an alternative to SiO_2. A trade-off exists however, and Figure 2.4 shows how an increase in dielectric constant results in a sacrifice of bandgap width. Popular studies have included Al_2O_3 and HfO_2 deposited onto SiC [50, 51]. Results have shown a reduction in interface trap density compared to SiO_2/SiC interfaces [51]; however large leakage currents occurred due to the the reduction in bandgap [52]. The use of a thin SiO_2 interlayer [53, 54] reduced this leakage and achieved a reported [54] channel mobility of 300 $cm^2/(Vs)$. However, the reintroduction of SiO_2 lowers the total dielectric constant value and reintroduces the SiO_2/SiC transition layer.

2.5.2 Silicon Carbide Heterojunctions

Despite its increasing popularity as a power material, the biggest share of the SiC market, accounting for some 80% is its use in a heterojunction technology, as GaN is grown on SiC substrates to produce the blue LED's with which SiC has become synonymous. A heterojunction is the unison of any two dissimilar semiconductors and other examples include, most notably, the laser which is commonly an amalgamation of AlAs and GaAs,

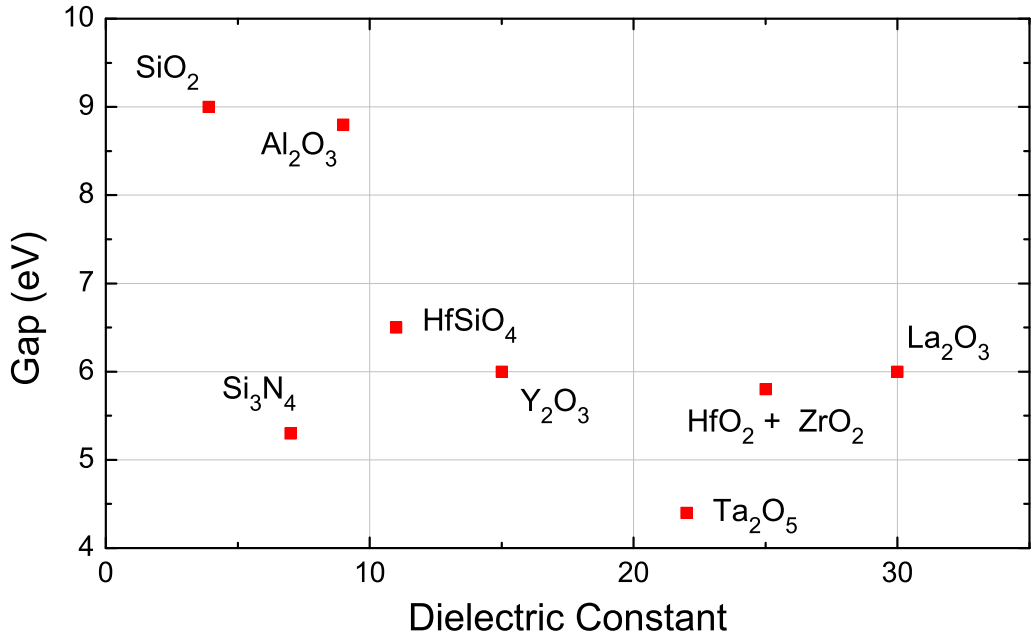


Figure 2.4: A plot of dielectric constant versus bandgap showing the trade off that exists in the choice of an oxide. Data taken from [55].

semiconductors with very similar lattice parameters allowing their unison.

Considering the list of problems that plague SiC MOS transistor technologies, another materials' solution was sought [14, 15, 19, 20, 56] that might offer some relief to the oxide and mobility problems. That solution was to try and reintegrate silicon into the channel region, it being a material that has none of the described problems. This would provide many experimental options. The entire Si layer could be oxidised returning the layers to a SiO_2/SiC MOS structure. The idea behind this is to control the oxidation time such that the Si gets complete the oxidised, but the SiC does not, though this is a processing challenge.

Alternatively one could partially oxidise the Si surface, or indeed deposit an oxide

directly onto the Si surface, either method providing a Si channel between the oxide and the SiC. This channel, if single crystal would have a high mobility and would bond well with a SiO_2 layer free of interface traps. The SiC would remain to provide a low doped drift, or blocking, region though one might expect a reduction in the breakdown voltage due to the reintegration of Si with its lower critical field.

Such a device was built by Hoshi et al [19], at the Nissan research Centre, forming a Si/4H-SiC heterojunction tunneling transistor (HETT). This device was capable of handling current densities greater than 1700 A/cm^2 with a specific on-resistance of 2.9 mΩcm^2.

Another use for the structures was presented [19,20] as the layers were used to produce Schottky-barrier-like diodes using a degenerate Si layer ($N_{A_{Si}} = 1 \times 10^{20} cm^{-3}$) that acted as a metal due to its large number of carriers. A small barrier to electrons compared to that for holes ensured the heterojunction diodes were unipolar, with turn-on characteristics exactly like SBDs. The Si/SiC diodes were shown to have a low forward voltage drop and a large blocking voltage compared to SiC SBDs, being able to block 1600 V, with an on-resistance of 1.4 mΩcm^2. The work of [14, 15, 56] produced similar p-N and n-N 4H-SiC/Si heterojunction diodes, though the electrical results were not as encouraging, most likely due to the fabrication techniques that were far simpler than the Japanese devices. However, as we will see in Chapter 5, this work represented the first attempt to form heterojunction layers on SiC via MBE techniques, which was an essential foundation upon which the work in this thesis was laid.

With quite an extensive body of research existing on Si heterojunction layers on a SiC substrate, the aim of this work is to see if Ge can emulate or even better this.

2.6 Summary

The aim of this Chapter was to show that the material and device challenges facing SiC, impact on the low-carbon, energy efficient projects that are so relevant in today's society. Wind turbine, smart grid and electric car technologies were directly linked to the efficient transformation of power from one form into another, thus placing strict energy efficiency requirements on the devices at circuitry level. SiC was introduced, showing the progress and problems of the material as it tries to leverage a stake in the silicon dominated power semiconductor market. Finally, the niche SiC heterojunction technology was introduced, presenting the ideas that might help to alleviate some of the problems that face SiC in its battle with channel mobility and interface states.

Chapter

3 Theoretical Discussion

3.1 Introduction

This Chapter serves as an introduction to concepts that will be used throughout the results Chapters. We are particularly concerned in Chapter 5 with the ways in which the atoms of one semiconductor will arrange themselves when deposited onto another semiconductor. Therefore, time is necessarily spent introducing the crystalline properties of different semiconductors in Section 3.2 and heteroepitaxial growth in Section 3.3. Once these layers have been formed, it is quite essential for the electrical characterisation of Chapters 6 and 7 that the energetic interaction of these two layers is understood and current flow. Hence, Section 3.4 describes the band alignment and barrier formation of two semiconductors. Once formed, the highly doped Ge thin film causes the heterojunction diodes to act like Schottky barriers, so Section 3.5 introduces the theory of Schottky contacts and the flow of current over them.

This Chapter, and indeed the proceeding Chapters presumes a level of understanding about basic semiconductor physics. However, included in Appendix A are some of the more basic theories of the subject. These include fundamental band structure, the alignment of like semiconductors, metal-semiconductor theory and breakdown voltage considerations.

The theory behind metal-insulator-semiconductor is left until the self contained Chapter 8.

3.2 Semiconductor Crystal Structure

Throughout this thesis, the structure of a semiconductor will be frequently referred to. It is therefore important to introduce the crystalline nature of the different semiconductors used in this work and the differences that make the Si/SiC and Ge/SiC heteroepitaxy difficult.

Solid elements and compounds form into regular crystal patterns that can be categorised by the shapes they make when split into unit cells. Si, Ge, and diamond form into a diamond pattern, whilst 3C-SiC also forms the same pattern but being made up of multiple elements, it is referred to as a zinc-blende pattern. 4H-SiC and 6H-SiC form into hexagonal structures, though the fact that these structures also contain multiple elements, this is referred to as a Wurzite structure. These can be seen in Figure 3.1, where a and c represent the lattice constants of the cells. A tetrahedral arrangement is evident in both structures, with each atom having four nearest neighbours. The bond formed between each pair of atoms comes from the attraction of electrons with opposing spin.

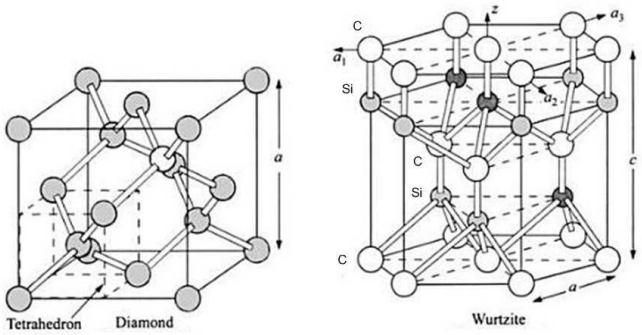


Figure 3.1: Two common crystal pattern structures in their unit cells. The Wurzite structure contains labels pertaining to a SiC structure. (From Ref [36].)

3.2.1 SiC Polytypes

The hexagonal structure of Figure 3.1 may be seen as layers of silicon and carbon and is the basis of the SiC molecule. To determine the relevant polytype of SiC, every carbon layer should be discounted and the position of the Si layers assessed. Given that any two bonds from one atom in a tetrahedral system are separated by 120 degrees, there exists three lattice positions at which a Si atom may end up. These are represented by layers A, B, and C in Figure 3.2a. The order with which these layers repeat determines the SiC polytype. Figure 3.2b shows how these layers repeat for the three most common SiC polytypes. 4H-SiC is represented by the repeating pattern $ABCB$, whilst 6H-SiC is represented by $ABCACB$. These polytypes form only in the hexagonal cell structure. 3C-SiC is the simplest of the three being a repeating ABC pattern. By tilting these hexagonal-style layers of 3C-SiC by 54.7 degrees down any of the hexagonal a-planes, the resulting atomic pattern revealed is that of the zinc-blende cell structure.

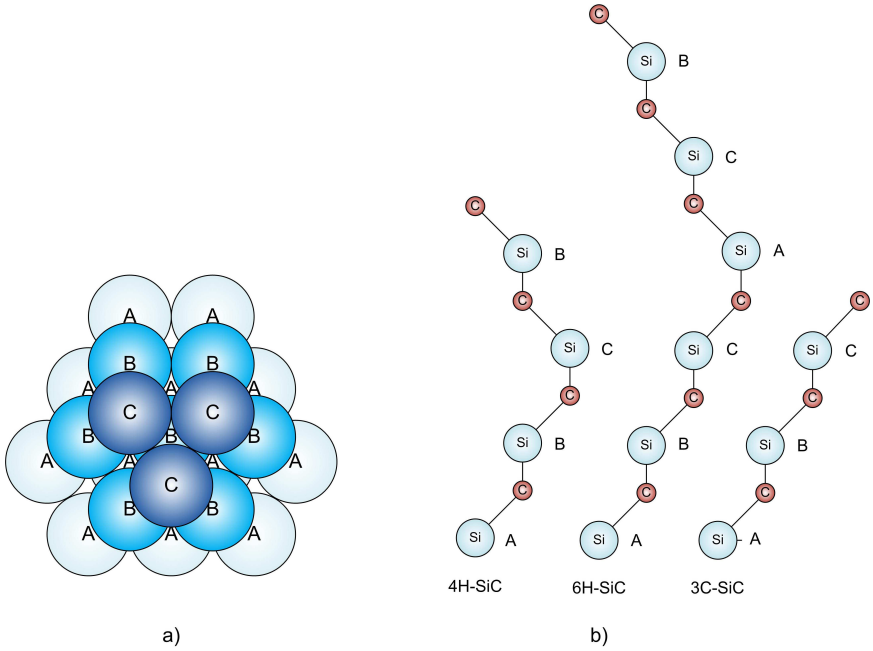


Figure 3.2: a) The location of the 3 Si atoms within a SiC stacking sequence and b) the three different stacking sequences.

3.2.2 Miller Indices

To identify the correct orientation of a crystal, the cell structures are referred to in terms of planes that dissect the axes of symmetry within each of the structures. This is known as the Miller indices and for cubic cells this is a represented by a three term vector, (hkl). h, k, and l are determined by finding respectively the intercepts of the plane in the x- y- and z-axes and taking their reciprocal values. Hence, a 1 represents the cell's lattice parameter, whereas a 0 means that the plane will be parallel to the axis, the plane never meeting the axis. A -1 or a $\hat{1}$ represents the plane crossing the negative axis, the full lattice parameter distance from the origin. Three of the most common planes are shown in Figure 3.3.

Similarly, for the hexagonal structures, the Miller indices uses the three axes of symmetry of the hexagon (a_1, a_2 and a_3) and the z-direction to form a four term vector

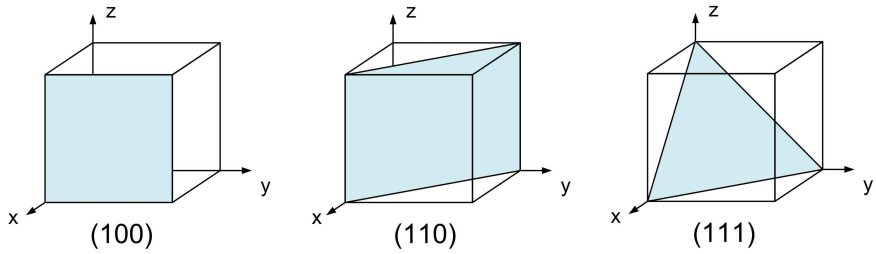


Figure 3.3: Three common crystal planes in cubic structures.

$(hklm)$. Once again, the numbers within the vector are the reciprocal of where the plane cuts the axis. Three common planes are shown in Figure 3.4.

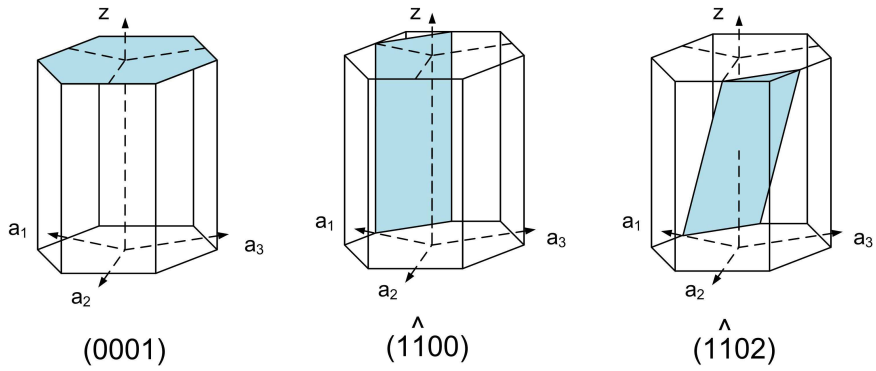


Figure 3.4: Three common crystal planes in hexagonal structures.

Returning to the example of 3C-SiC; this material is a cubic structure as pictured in Figure 3.1. However, taking a cut through the (111) plane will leave you with the (0001) plane of the hexagonal structure, where the individual layers of Si and C repeat in the ABC pattern.

3.3 Thin Film Science

In this section the theory of heteroepitaxial growth will be investigated, building up from the basics of surface science. Firstly a brief introduction will be given to surface tension and surface energy, underlining why certain materials wet a surface when others ball up, both of which we will see in the results sections. The epitaxial growth of new layers will be investigated, showing that atoms with sufficient energy can find a bonding site that minimises the dangling bonds of that atom and those around it. The idea of strained and mismatched layers will be discussed, before an idealistic Ge on SiC growth regime is presented.

3.3.1 Surface Tension and Wetting

To determine how materials interact in deposition, we must first understand how differing surface tensions between the substrate and the deposited material can affect growth. The term surface tension makes one think of liquids, waterboatmen sitting on a lake, or the balling up of water on a Teflon pan. Indeed the theory behind surface tension is most easily imagined given the analogy of a liquid upon another surface. The liquid will always tend to the most energetically favourable situation, be it to ball up like the water in the pan, or to spread out creating a very thin uniform layer, such as a teaspoon of oil spreading thinly across a lake. The difference between these two examples is the relative amounts of surface tension the two liquids have compared to the surfaces they sit upon. In the balling up example the surface tension of the liquid is very high and the minimal energy state of the liquid is when it is attached to itself rather than the surface. Of course, the opposite state sees a liquid with low surface tension spreading itself thinly due to the minimal energy state being to combine with the surface.

Quantifying these two extremes, Figure 3.5 displays an example of a liquid that has been deposited on to a solid surface, with a contact angle Ψ. The three components, the gas, liquid and solid, come together at a single point known as the triple interface. Here, the surface tensions associated with each interface must balance according to Young's equation,

$$\gamma_{sl} + \gamma_{lg} \cos \Psi = \gamma_{sg}. \tag{3.1}$$

where γ is the surface tension between the liquid (l) gas (g) or solid (s). At equilibrium, the magnitude of Ψ determines how the materials are interacting. If $\Psi > 0^\circ$ then the forces promoting the liquid to stay balled up outweigh those promoting spreading, hence,

$$\gamma_{sl} + \gamma_{lg} > \gamma_{sg}. \tag{3.2}$$

If $\Psi > 90^\circ$ then the liquid has not wet the surface at all. This situation can be viewed as it being energetically favourable for the liquid atoms to bond with themselves or the gas rather than the solid. If $0^\circ < \Psi < 90^\circ$, then the liquid partially wets the surface, as in Figure 3.5. If $\Psi = 0^\circ$ then the forces promoting spreading outweigh those promoting the liquid to stay balled up, hence,

$$\gamma_{sl} + \gamma_{lg} \leq \gamma_{sg}. \tag{3.3}$$

The two extremes of wetting and balling up described here is important when it comes to depositing solid materials heteroepitaxially. Given limitless energy, the atoms of a deposited material would ball up in exactly the same way, if the surface tension of the epitaxial material was great enough. However, in solid-solid deposition carried out at moderate temperatures, the atoms lose the energy required to break the interatomic bonds formed at bonding sites and thus there is not the fluid motion of a liquid. What

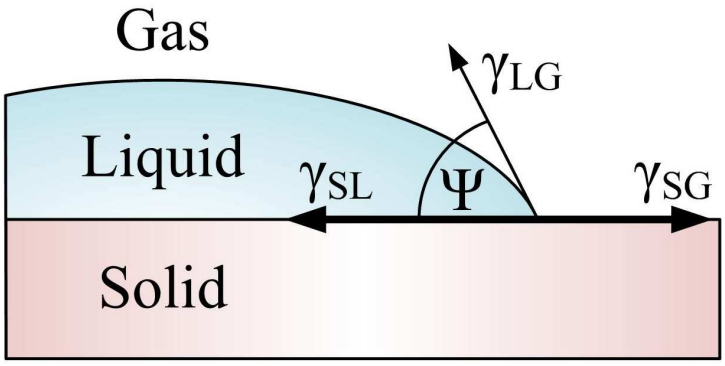


Figure 3.5: A liquid on the surface of a solid. The contact angle of the liquid gas interface, Ψ, is determined by the relative surface tension value γ at the interfaces of each material. The contact angle dictates whether the liquid wets the surface ($\Psi < 90°$) or whether the surface tension of the solid, γ_{sg}, is too large ($\Psi > 90°$) leading to the liquid 'balling up'. [57, 58]

will occur instead will be the formation of 3-dimensional islands during growth, the atoms preferentially bonding to other like atoms rather than the surface. However, at the opposite extreme, with a large substrate surface tension, the preferential bonding sites will be on the surface rather than the other like atoms, leading to layer by layer growth. These concepts will be revisited in Section 3.3.4.

3.3.2 Nucleation

The formation of an epitaxial layer begins with a cloud of the atoms above the substrate. Provided the deposition is occurring at a raised temperature, the adatoms will arrive on the surface with energy sufficient enough to move about the surface or find a nucleation site as outlined in Figure 3.6a. Whilst the atoms arrive at the surface at a given rate, there is also a lesser rate at which the atoms simply re-evaporate from the surface, rejoining the atomic gas above the substrate. Those that do not re-evaporate have the energy to move around the surface seeking a preferential bonding site, be it at a step edge, into a

cluster or binding with another adatom to provide the beginnings of another cluster.

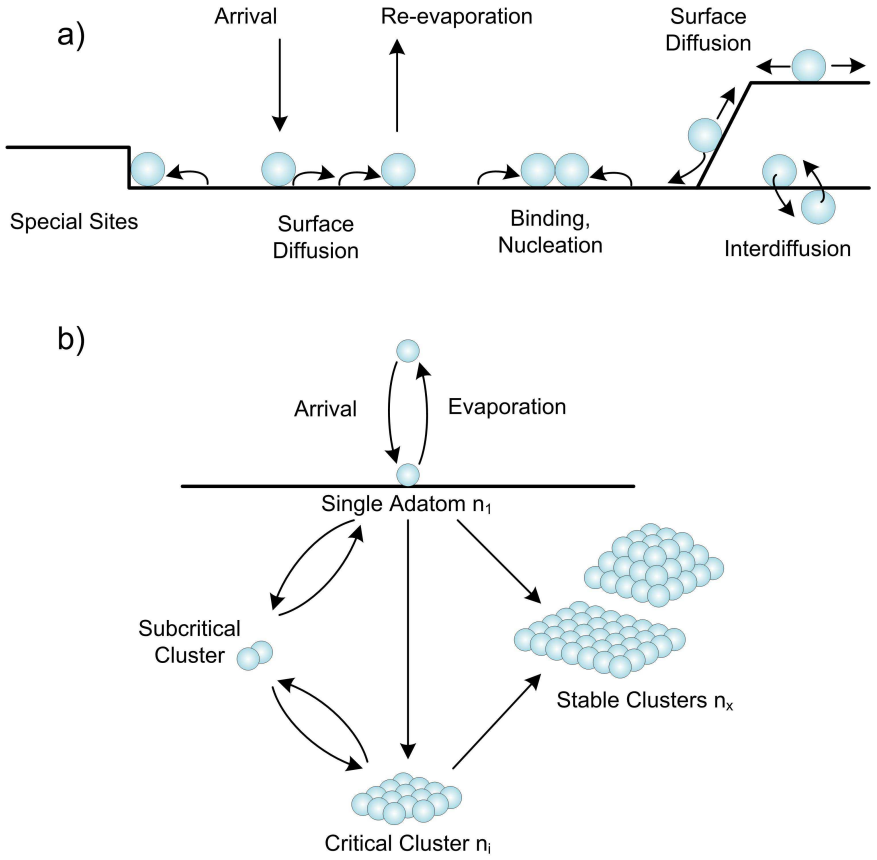


Figure 3.6: a) The behaviour of energetic adatoms on a substrate during deposition. b) The cycle of nucleation that sees the deposited adatoms form eventually into stable clusters. Both processes reproduced from [59] with permission from Elsevier.

Figure 3.6b shows the process that leads to the original adatoms forming the clusters, that in turn merge to form an epitaxial layer. Individual adatoms will seek a position on the surface that will minimise its dangling bonds and the simplest way that this happens is by joining an existing cluster. It is energetically favourable for an atom to join a large cluster, as it is reducing the total number of dangling bonds and decreasing the overall surface area within the system. Such large clusters are deemed stable, and will only grow in size, two- or three-dimensionally depending on the growth mode. However, up until

a critical size, the bonds keeping the adatoms together are weak and the combining of adatoms into the cluster is reversible. Hence, Figure 3.6b shows that the path from an individual adatom to a subcritical cluster and a critical cluster is bidirectional. [59]

3.3.3 Lattice Mismatch Induced Strain

Strain within an epitaxial layer prevents uniform, layer-by-layer growth and is brought about largely due the differing lattice properties of the materials in question. Take first the example of homoepitaxial growth, whereby Si is grown upon a Si substrate. Energetic Si adatoms deposited onto the surface of a clean, flawless Si(111) surface will have few problems forming a single crystal layer on the substrate. This is because the layer being formed and the substrate are exactly lattice-matched; the atoms forming on the surface require the same spacing as those acting as a seed layer on the substrate beneath, and hence the layer is free of stress. There are a few examples where different materials have the same lattice parameters, and hence stress-free heteroepitaxial growth is possible. The mismatch (f) between the two materials is given by [57, 60],

$$f = \frac{a_A - a_B}{a_B}, \tag{3.4}$$

where a_A and a_B are the lattice constants of the two materials. The chief example of lattice-matched layers is used in III-V laser technology, where AlAs and GaAs are mismatched by only 0.12%, which can further be reduced by employing an $Al_xGa_{1-x}As$ alloy. Similar is true of HgTe and CdTe mismatched by 0.3%, where $Hg_xCd_{1-x}Te$/CdTe is an important heterostructure used in infrared detectors and imaging arrays [61].

If the layers are mismatched by as much as 0.5% then the strain in the layer can become unmanageably large. Using an example of Si deposited on a Ge substrate, the

lattice mismatch is approximately 4.2%, with the Ge atoms having the larger separation distance. When the Si adatoms arrive on the surface they will attempt to form its usual crystal pattern whilst bonding to the substrate beneath, so minimising the number of dangling bonds. However, the Ge atoms are too far apart to allow the Si to relax into its normal lattice parameters. To minimise the dangling bonds, the Si atoms must spread beyond their usual spacing, thus inducing strain into the system. This is only possible for small mismatches and for thin epitaxial layers, as the strain in the layer quickly becomes too large. When the strain reaches a threshold, something has to give, and dislocation misfits will occur to relieve the strain at the expense of filling all the dangling bonds. Figure 3.7 shows these situations where Si is deposited onto Ge, a large mismatch, and where it is deposited onto a Si_xGe_{1-x} compound, where the Si content is high enough ($x > 0.9$) to strain the Si, without relief. As a strained layer gets thicker, the need to relieve the strain increases until a critical thickness is reached, beyond which the uniform crystalline growth no longer continues. This is the basis of Stranski-Krastanov growth and will be touched upon later. The critical thickness of Si grown directly on Ge is 1 nm, not large enough to practically use. In a Si_xGe_{1-x} compound where $x = 0.9$, the lattice mismatch is approximately 0.4%, and the critical thickness rises to approximately 20 nm. With the Si lattice stretched beyond its usual lattice parameters, mobility in the strained layer is increased due to the reduction of scattering events. This is known as strained Si and the concept is exploited in the CMOS industry to provide low resistance channel regions [62].

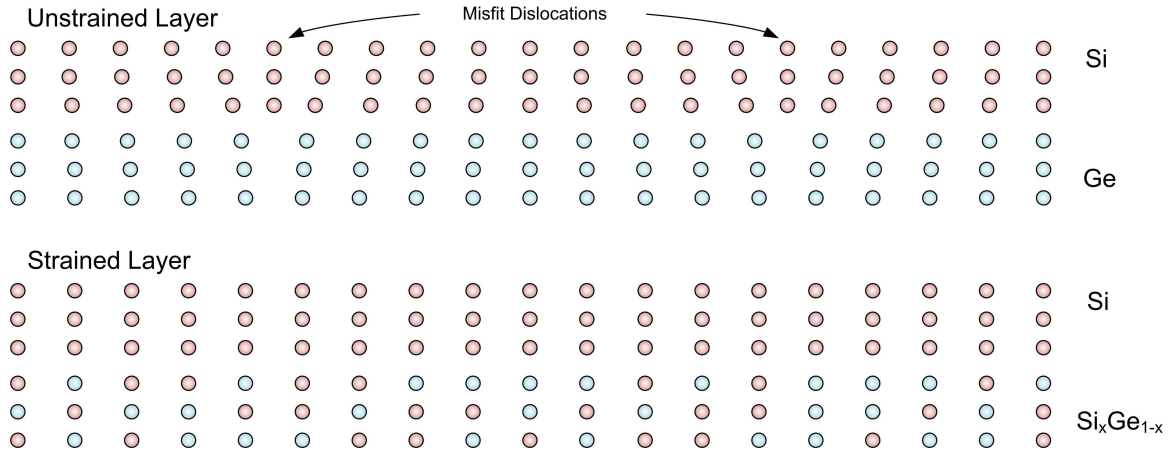


Figure 3.7: A graphical representation of Si grown on Ge and on Si_xGe_{1-x} [60].

3.3.4 Thin Film Growth Modes

In the previous sections we have seen that there is a lot to get right in order to grow perfect layers. The wrong balance of surface tensions or the mismatch of lattice parameters by the smallest of margins will affect the quality of the layers deposited. Here we describe the very precise requirements of layer-by-layer growth, and explain the alternative growth modes that occur in order to relieve strain or minimise surface energies.

Firstly, layer-by-layer deposition, otherwise known as Frank-van der Merwe (FM) growth, can be seen in Figure 3.8a and is desirable for growing single crystal layers. As mentioned in Section 3.3.3, FM growth happens most frequently in homo-epitaxial growth whereby the material being grown has a lattice structure entirely matched to the substrate beneath. The precise conditions for FM growth are as follows: Referring to Figure 3.5 and Equation 3.3,

$$\Psi = 0 \Rightarrow \gamma_{sg} \geq \gamma_{sl} + \gamma_{lg}. \tag{3.5}$$

Furthermore, the layers should be precisely lattice matched to minimise strain, or, for

layers that are slightly mismatched, the layer must not exceed the critical thickness for that mismatch.

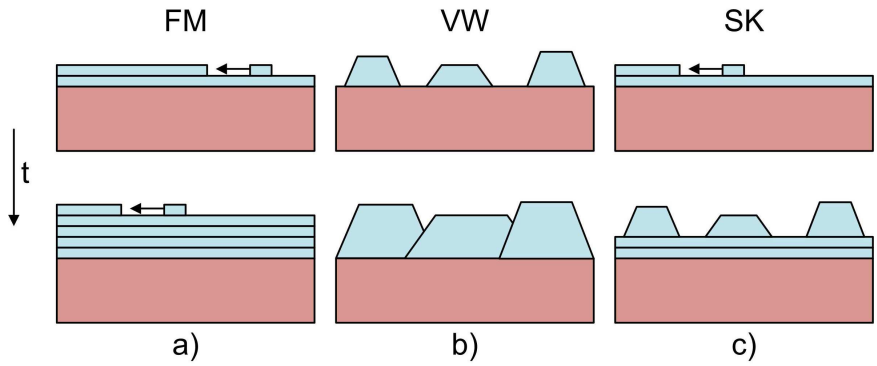


Figure 3.8: The three major growth modes of thin films; a) Frank-van der Merwe, b) Volmer-Weber and c) Stranski-Krastanov

Any lattice mismatch between the substrate and the film will prevent the preferred FM growth mode. In terms of the lattice mismatched adatoms on a surface, the adatom can either bond with the substrate forming the strained layer, or bond preferentially with other adatoms. The result of the latter is that the layers form in clumps on the surface, or islands. This is known as Volmer-Weber (VW) growth and is displayed in Figure 3.8c. Once the islands are large enough, they will begin to overlap and a solid layer will be formed, albeit with a rough surface. The overall layer will tend to be polycrystalline with many different crystal orientations. This growth mode can also occur in lattice matched systems if the balance of surface tensions are not correct. If the minimal energy state is for the deposited material to bond with itself, i.e. if,

$$\Psi > 0 \Rightarrow \gamma_{sg} < \gamma_{sl} + \gamma_{lg}, \tag{3.6}$$

then wetting will not occur and the material will ball up.

This third mode is known as Stranski-Krastanov (SK) growth and it occurs when the depositing layer wets the surface as in Equation 3.3. In contrast to FM growth however, the presence of strain from a small lattice mismatch allows the film to grow layer by layer only up to a critical thickness, at which point islanding begins, as shown in Figure 3.8b. Within an epitaxial layer that is thinner than the critical thickness, the atoms will be strained, to comply with the lattice parameters of the substrate beneath. The example of strained silicon given in Section 3.3.3 is a good example of the SK growth mode, where the amount of Ge present in the SiGe layer will dictate the thickness at which the layer by layer growth gives way to defects and islanding.

Predicting how one material will grow on another is a very difficult thing to do. Most research into epitaxial growth is done practically, analysing the results of laying one material on another given certain conditions. Of course we can attempt to pick materials that are in theory lattice matched in some orientation using, for instance, the chart in Figure 3.9 however, the proof lies in the experimental analysis. The case of Si or Ge growing on SiC is presented herein, and the growth modes can be assessed in each case. Both narrow band semiconductors can be seen in Figure 3.9 at around 5.5 $\mathring{A}$, SiC down at 3.2 $\mathring{A}$. Taking into account the difference in crystal structure as well, the prospect of anything but VW growth appears thin. Indeed, we will witness Si MBE depositions balling up, forming distinct islands in a manner that suggests that VW growth is dominant. Ge growth is not so clear cut however, with the islands that form being much more expansive, covering a much larger surface area, overlapping at a much reduced thickness compared to Si. This suggests that the surface is being wet much better in the case of Ge, and hence the SK mode is more likely.

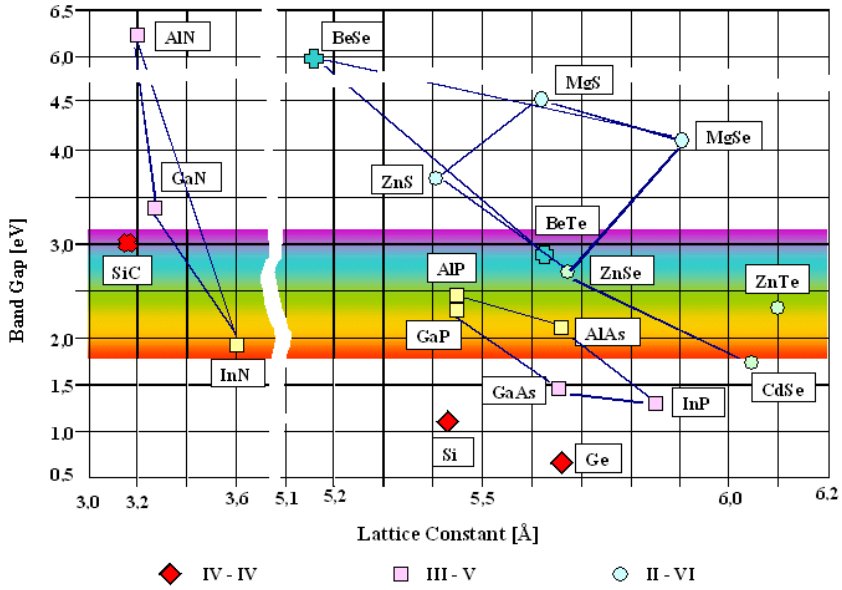


Figure 3.9: A plot of bandgap against lattice parameter for the major semiconductors [63].

3.4 Heterojunction Theory

A heterojunction is the union of dissimilar semiconductors, and heterojunctions of silicon or germanium on SiC form the backbone of the proceeding Chapters. The theory behind how these different semiconductors may coexist energetically is introduced here. However, this basic theory is grounded in how a p-n junction forms when two like semiconductors interact. Hence, in Appendix A.3.1, an introduction to homojunction theory may be found. In heterojunctions as in homojunctions, Fermi levels must align in adjacent semiconductors, however with different bandgap widths, the conduction and valence bands will not fully align.

Unlike in a p-n junction. the built in potential ψ_{bi} is not the only barrier that the electrons have to overcome as the conduction and valence bands of the different semiconductors are apart from each other. Considering the example of the p-N heterojunction of

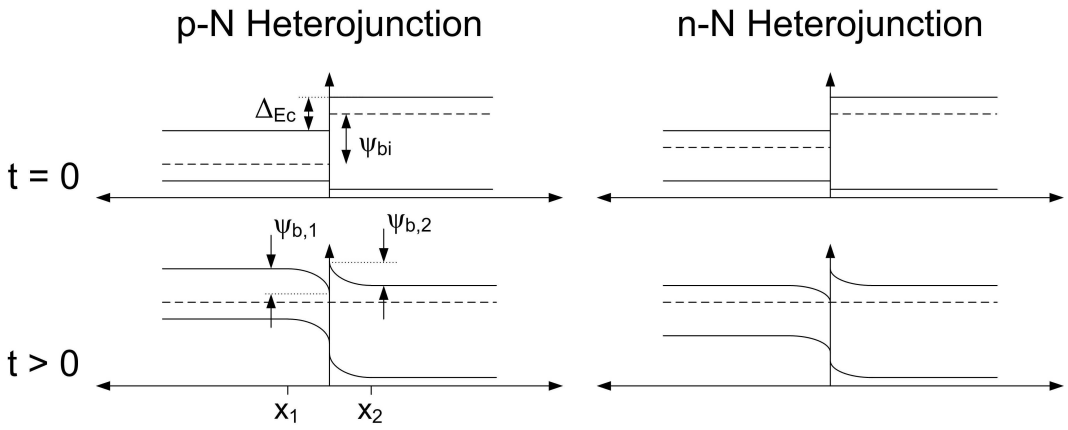


Figure 3.10: Band diagrams of a p-N and n-N heterojunction interface a) prior to settling to the steady state and b) in the steady-state.

Figure 3.10, there is a barrier to electrons to be overcome in both directions. A majority carrier electron, travelling conventionally from right to left must overcome potentials $\psi_{b,1}$ and $\psi_{b,2}$, which combine to a total of ψ_{bi}. A minority carrier electron travelling in the reverse direction, will have to overcome the abrupt barrier of ΔE_C, thus limiting electron leakage. To holes the scenario is different, the majority carriers must overcome the full ψ_{bi} in addition to ΔE_V, whereas minority carriers will have a path clear of potential barriers. This makes this example unipolar depending on the direction of the bias.

Considering the electrostatic analysis, which is shown in full in Appendix A.4.3, the depletion width edges x_1 and x_2 are found to be,

$$x_1 = \sqrt{\frac{2K_{s,1}K_{s,2}}{q}\frac{N_{D,2}}{N_{A,1}(N_{A,1}K_{s,1}+N_{D,2}K_{s,2})}\psi_{bi}} \tag{3.7a}$$

$$x_2 = \sqrt{\frac{2K_{s,1}K_{s,2}}{q}\frac{N_{A,1}}{N_{D,2}(N_{A,1}K_{s,1}+N_{D,2}K_{s,2})}\psi_{bi}} \tag{3.7b}$$

3.4.1 Degenerate Semiconductors

Another important concept is that of the degenerate semiconductor, where a semiconductor is so highly doped that the large amount of carriers causes it ro behave like a metal. The use of a degenerately doped Ge layer, allows the formation of ohmic contacts to the heterojunction devices seen later.

In a non-degenerate semiconductor, the position of the Fermi level within the a semiconductor is dictated by the occupancy of states within the conduction band. At low doping, the quantum mechanical Fermi-Dirac statistics [36] which describes this occupancy can be approximated using classical physics. Specifically, Boltzmann Statistics reduces the Fermi-Dirac integral to an exponential equation resulting in the simple formulas of Equations A.2 and A.5 that can be seen in Appendix A.2.2.2. However, as the doping increases above approximately 5×10^{18} cm^{-3}, the Boltzmann approximation breaks down, due to the interparticle distance reducing to a value below the thermal de Broglie wavelength, and causing quantum interaction between the particles. On the energy scale, the Boltzmann approximation is considered accurate until the Fermi level comes to within the thermal voltage of the conduction or valence bands, such that $E_V + kT/q < E_F < E_C - kT/q$. Outside these bounds, one approximation to the Fermi-Dirac function was published by Joyce and Dixon [64], such that Equations A.5 are replaced with,

$$\phi_n = \frac{E_C - E_F}{q} \approx \frac{kT}{q}\left[\ln\left(\frac{N_D}{N_C}\right) + \frac{1}{\sqrt{8}}\frac{N_D}{N_C} - \left(\frac{3}{16} - \frac{\sqrt{3}}{9}\right)\left(\frac{N_D}{N_C}\right)^2 + ...\right] \qquad \text{for n-type} \tag{3.8a}$$

$$\phi_p = \frac{E_V - E_F}{q} \approx \frac{kT}{q}\left[\ln\left(\frac{N_A}{N_V}\right) + \frac{1}{\sqrt{8}}\frac{N_A}{N_V} - \left(\frac{3}{16} - \frac{\sqrt{3}}{9}\right)\left(\frac{N_A}{N_V}\right)^2 + ...\right] \qquad \text{for p-type} \tag{3.8b}$$

Semiconductors outside of the bounds of the Boltzmann statistics are known as degenerate, and the onset of degeneracy occurs as the doping increases towards the effective density of states (N_C or N_V). The behaviour of a degenerate semiconductor is rather like that of a metal, and this is reflected in the make up of the band diagram when a moderately doped semiconductor meets a degenerate semiconductor. Relevant to this thesis, Figure 3.11 shows a lightly doped wide-bandgap semiconductor and a degenerate narrow bandgap semiconductor and this n-N heterojunction is presumed to have a one sided depletion region. The conduction band offset (using n-type SiC) allows us to treat the heterojunction structure as if it were a metal-semiconductor Schottky diode, the theory of which will be tackled in Section 3.5.

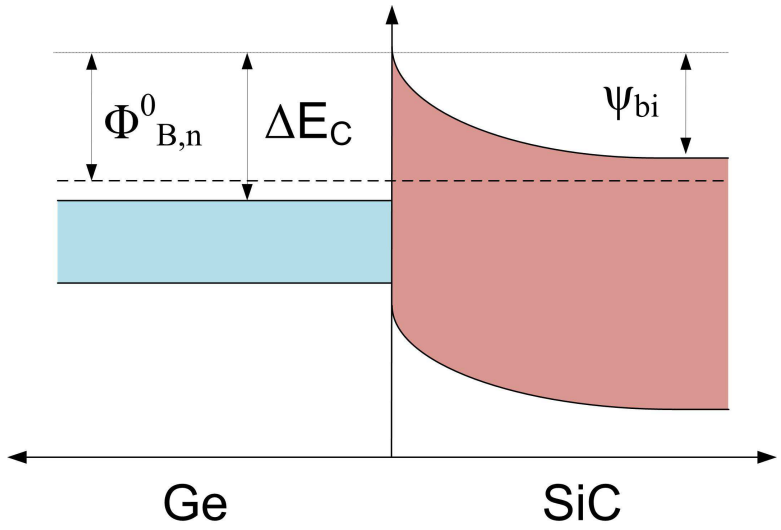


Figure 3.11: Band diagram of a n-N heterojunction, with degenerate doping of the narrow-bandgap semiconductor.

3.5 Schottky Contacts

The use of degenerate Ge or Si as a heterojunction sandwich layer between a SiC substrate and a metal contact has two distinct effects which permits their treatment as Schottky barrier diodes. First of all, the Ge or Si's degeneracy makes the heterojunction interface one sided, with the depletion region formed on the SiC side of the interface. Secondly, the degenerate layer means that the potential barrier to the metal contact is so thin that carriers tunnel through it, creating an ohmic contact. The net result is a single potential barrier at the Ge/SiC interface and the flow of carriers over this may be controlled by the voltage across it. For this reason it is synonymous with a Schottky diode structure.

The theory behind the formation of a Schottky barrier and the flow of electrons over it, or thorough it, may be found in Appendix A.5. The Schottky contacts presented in this thesis may be presumed to be dominated by the thermionic emission current transport technique alone due to the very low doped SiC. As such, the most important consideration of the theory is that the flow of current over the barrier is given by,

$$J_{s\rightarrow m} = A^{**}T^2 e^{-\beta\Phi^0_{B,n}} \left(e^{\beta V}\right) \tag{3.9}$$

where A^{**} is the Richardson's Constant and β is the inverse thermal energy ($\beta = q/kT$). J is the current density expressed as $J = I/A$, where A is the contact area. This can be shortened to,

$$J_{s\rightarrow m} = J_S e^{\beta V} \tag{3.10}$$

where J_S is the saturation current shown to be

$$J_S = A^{**}T^2 e^{-\beta\Phi^0_{B,n}}. \tag{3.11}$$

Equation 3.9 is an ideal scenario that does not consider any of the practical implications of a real Schottky contact. Here, three factors will be described that can modify this equation, specifically, other current transport mechanisms, series resistance and leakage current.

3.5.1 The Ideality Factor

Equation 3.9 represents the current flow over the Schottky barrier when thermionic emission is the only current mechanism at work. If other mechanisms are involved or if imperfections are present at the contact, then the current-voltage response can shift from this model, with the logarithmic slope of the on characteristics becoming less steep. This may be characterised by adding an ideality factor, η, into Equation 3.9, such that,

$$J = A^{**}T^2 e^{-\beta\Phi^0_{B,n}} \left(e^{\beta V/\eta} - 1\right). \tag{3.12}$$

Thus as η tends to 1, so the diode is increasingly ideal as thermionic emission facilitates the fastest device turn-on. As η increases towards 2, this suggests that some other current mechanism is beginning to dominate, often recombination within the depletion region.

3.5.2 Series Resistance

Equation 3.9 and in turn Equation 3.12 consider that the only barrier to electron flow is the Schottky barrier itself. Of course, any real device will have an associated resistance, most often proportional to the thickness of the drift region used to suppress reverse electric field. Therefore, if one is interested in modelling the turn on characteristics once series resistance kicks in, then one must include a resistance value. In the most basic of approximations [65], the applied voltage, V, in Equation 3.12, is simply replaced with

$(V - IR_S)$, thus limiting the applied voltage as the current grows. Hence Equation 3.12, would become,

$$J = A^{**}T^2 e^{-\beta\Phi^0_{B,n}} \left(e^{\beta(V-IR_S)/\eta} - 1\right). \tag{3.13}$$

This is a very basic approximation however, and this model is clearly flawed as $(V - IR_S) \rightarrow 0$, however it is a very useful first approximation, used successfully in Section 6.3.4.1. Other models exist to extract the series resistance, and these are especially useful when the resistance is particularly large, preventing normal parameter extraction. The most used of these is known as a Norde plot defined in [66].

Most often, the series resistance is not considered and modelling such as that in Section 7.2.3 ignores the series resistance, fitting only to the linear part of the plot.

3.5.3 Leakage Current

In the reverse direction, there are also practical limitations that prevent the perfect scenario. A large barrier is presented to electrons passing from a metal into the semiconductor. This appears independent of bias, and hence the current that crosses it may be obtained from Equation 3.9, setting $V = 0$,

$$J_{m\rightarrow s} = -A^{**}T^2 e^{-\beta\Phi^0_{B,n}} \tag{3.14}$$

Hence combining Equations 3.9 and 3.14, we may obtain an overall equation for the passage of thermionic emission in either direction over the Schottky Barrier,

$$J = J_{m\rightarrow s} + J_{s\rightarrow m} = A^{**}T^2 e^{-\beta\Phi^0_{B,n}} \left(e^{\beta V} - 1\right). \tag{3.15}$$

From this, we can conclude, that in the reverse direction, due to thermionic emission, the current will saturate at a leakage current of $I_{leak} = -AA^{**}T^2e^{-\beta\Phi^0_{B,n}}$. However, with increased voltage, the reverse leakage current increases beyond this threshold. This is due to Φ_B having, in practice, a small bias dependency, such that,

$$\Phi_{B,n} = \Phi^0_{B,n} - \Delta\Phi. \tag{3.16}$$

$\Delta\Phi$ arises due to an effect known as image-force lowering [36]. As an electron approaches the metal at a distance x from the interface, a hole is induced within the metal at a distance $-x$. The attraction that occurs between the two particles is known as the image-force, and this had the ability to lower the potential barrier under a high electric field. The image force lowering is defined as,

$$\Delta\Phi = \sqrt{\frac{qE_{max}}{4\pi K_s}}, \tag{3.17}$$

where E_{max} is the maximum electric field. This image-force lowering may be small compared to $\Phi^0_{B,n}$, but the lowering can be enough to significantly enhance the leakage current.

Chapter

4 Heterojunction Characterisation Techniques

4.1 Introduction

The forthcoming results Chapters rely heavily on analytical techniques that are used to extract information from the Ge/SiC or Si/SiC heterojunction layers. The first half of this Chapter introduces a range of analytical techniques that assess the physical properties of a layer. Measurable properties include surface roughness, layer crystallinity and stress, and the existence of any unwanted contaminants or oxides. The second half of this Chapter is dedicated to the electrical analysis, introducing techniques that measure, amongst others, the Schottky barrier height, breakdown characteristics, contact resistivity and doping profiles.

4.2 Physical Characterisation Techniques

The bulk of the work in this thesis concerns the heteroepitaxial growth of one semiconductor upon another. Using microscopy tools, a picture of the surface quality of the

heteroepitaxial layer, which can have an impact on channel scattering should the layer be employed in a MOS transistor. Furthermore, through FIB/SEM and TEM, any transitionary layers at the interface can be identified. Using the spectroscopy tools, we can identify the materials present within the sample locating any oxide formation or contamination by foreign elements. We can also understand the form of the crystal, be it crystalline, polycrystalline, or amorphous, whilst any stress induced in the heteroepitaxial layer can also be identified. All this knowledge can be of great use when interpreting the electrical results, helping to explain low resistance, non-ideal responses, SBH fluctuation or reverse leakage.

In this Section, a brief overview of each of the nine microscopy and spectroscopy techniques is given. As these are established techniques used widely, these techniques will only be introduced here, with their relevance to their current work highlighted. Running concurrent with this Section, Appendix B details some of the theory behind the techniques.

The AFM, TEM, RHEED and Raman measurements were all carried out by collaborators in Warwick University Physics Department, whilst the FIB/SEM and HIM images were carried out in collaboration with S. Boden at Southampton University.

4.2.1 Atomic Force Microscopy (AFM)

AFM is used to get very high resolution profiles of a surface by scanning a cantilever with a very sharp tip over the sample. AFM is employed in this work after the deposition of a heteroepitaxial layer to build up a 3-dimensional image of the surface. From this, the surface roughness of the layer is immediately available, whilst this technique also provides a first idea as to the crystalline nature of the layer.

There are three methods by which the surface profile may be constructed, details of

which may be found in Appendix B.1 and in [67]. The dynamic contact, or 'tapping' mode is used throughout this thesis because it is considered the most accurate of the methods with sub-nanometer resolutions possible [68].

The model used throughout this work is an Asylum Research MFP-3D. It has a z-range of 40 μm, with scanning in the x- and y-directions available over a range of 90 μm. It is capable of operating in the standard AFM modes including contact, tapping, and conducting AFM.

4.2.2 Focused Ion Beam (FIB) / Scanning Electron Microscopy (SEM)

The focused ion beam is used to prepare a sample for SEM or TEM analysis, using gallium ions to carve a wedge out of the surface, the shape of which may be seen in Figure 4.1. A sheer, rectangular face perpendicular to the surface is formed, and the built-in SEM in most machines is used to observe the detailed layers down from the surface. Two of these sheer faces back to back form the very thin cross-sectional sample needed for TEM analysis.

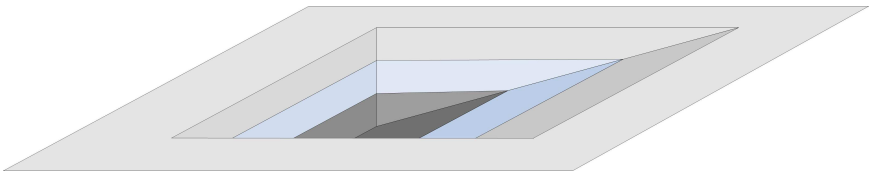


Figure 4.1: A graphical representation of the FIB 'wedge' that is formed with the rectangular face of the wedge perpendicular to the surface.

An electron gun built into the FIB system, allows SEM for imaging of the cross-sectional profile. The unique advantage of a SEM over other imaging techniques, is the huge depth of field with magnification possible, from 10x up to 500,000x. This is achieved

through the use of a very small electron beam spot size, typically down to 1 nm, which allows the very high resolution of the images. Details of SEM operation can be found in Appendix B.2.

The operation of a FIB is very similar to that of a SEM, except that ions of usually Gallium are used to bombard the specimen surface instead of electrons. However, as they are bombarded onto the sample surface, the heavy, large ions displace much more material at the surface as they have a very limited penetration depth. At low beam currents very little material is sputtered and the system can be used as an imaging tool with resolutions of 5 nm achievable. However,at high beam currents, a large amount of material is displaced and the tool is used for the required high precision milling.

The FIB/SEM employed in this work is a JEOL4500, which contains two 30 kV columns, one a vertical 30 kV electron column with a LaB6 electron gun, and the other an inclined 30 kV ion column with a Ga+ ion source. The FIB/SEM images used throughout are tilted 54^o as required to view the surface cross section from a detector outside a trench like that seen in Figure 4.1.

4.2.3 Transmission Electron Microscopy (TEM)

TEM is a very high resolution technique used in this work to observe the atomic structure of the Ge/SiC heterojunction layers, at the interface and within the bulk. Unlike the other techniques presented here, the beam of electrons fired at the sample is travelling right through it, interacting with the lattice as it goes. As such, the sample must be very thin, tens of nanometers at the most. This poses a problem with the very hard material SiC, which must be thinned using polishing pads of either SiC or diamond, or, as in this work, by using a FIB to dig two trenches back-to-back, resulting in the very thin sample

that may then be cut out.

As the beam of electrons passes through a sample, the amplitude of the beam is attenuated when it comes into contact with the the lattice. The amount of attenuation is proportional to the square of the atomic number, and hence the amplitude of the beam exiting a sample is proportional to the type of element that has crossed its path. Passing this beam over a sample, one can build up a map of the elements within that structure. The highest resolution results come with a very large signal and a very thin sample, less than 10 nm, where the lattice interactions cause a phase shift of the electron beam signal.

The TEM used is a JEOL2000fx, capable of 750,000x magnification using a beam of 0.32 nm diameter and an acceleration voltage ranging from 80 to 200 kV. The machine also has a built in EDAX facility and a reflection high-energy electron diffraction (RHEED) detector.

4.2.4 Helium Ion Microscopy (HIM)

HIM is a very new form of microscopy, based on the concept of an SEM, which can attain very high resolution images thanks to the use of helium ions that bombard the surface. Similar to the FIB, these ions are very large when compared to the electrons fired from a SEM. The short de-Broglie wavelength associated with the ions enables a sub-nanometer resolution, and a depth of field 5 times that of the SEM. HIM images in this thesis were taken in one day at Southampton University using their Carl Zeiss Orion HIM. Figure 4.2 is an example of the HIM's capability, showing the surface of a SiC wafer that has been damaged by acid. The tool is used in this thesis to look at the quality of polycrystalline and amorphous surfaces.

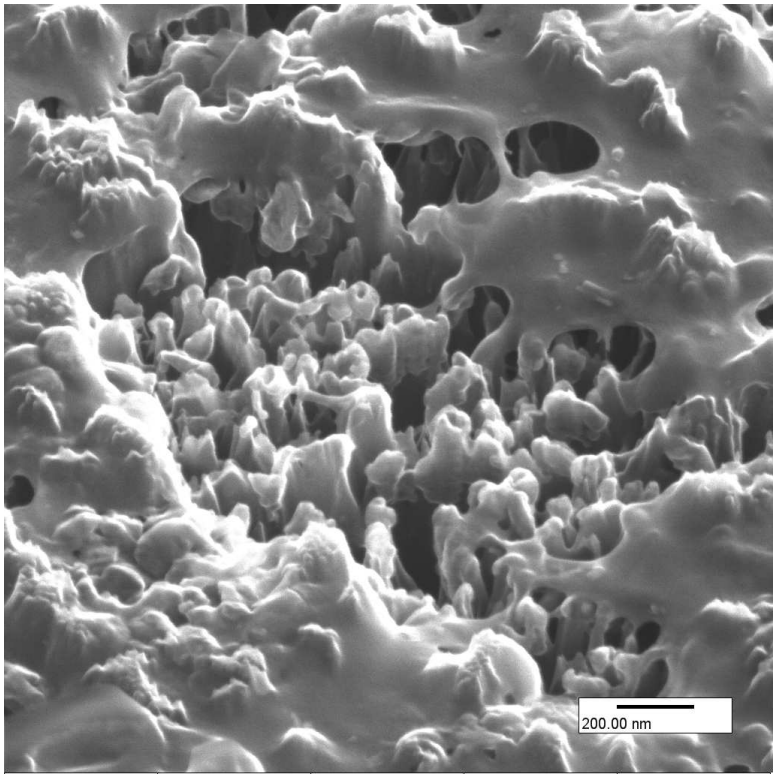


Figure 4.2: An example of the helium ion microscope: The surface of an acid damaged SiC wafer.

4.2.5 X-Ray Diffraction (XRD)

The XRD is one of the initial tests carried out on a heteroepitaxially grown layer to determine its crystallinity. X-rays, bombarding a sample, interact with the uppermost monolayers of atoms, reflecting back X-rays when a critical angle is reached. The angle at which this occurs is unique to an element in a given crystal orientation. Hence if only one of these peaks is present one knows that only a single crystal-orientation is present, and hence the it is likely to be single crystal. Conversely, multiple peaks are evidence that the layer has formed in a poly-crystalline fashion. Given no peaks, it is likely that the material is amorphous, having no single polycrystal big enough to emit a signal. Further detail of XRD operation, which is based on Bragg's law can be found in B.3.

The XRD used throughout this work is a Philips 1820 diffractometer.

4.2.6 Energy Dispersive X-Ray (EDX)

EDX is a method for determining a detailed analysis of the elements present with a sample. Electrons, which bombard a sample surface, often displace an electron from an atoms's inner shells. This electron is replaced by one of higher energy in an outer shell, with an element and shell unique amount of energy being given off as an x-ray. This element based x-ray signature is valuable in determining what materials are present in a sample, be they intentionally deposited, or unwanted trace contaminants or oxides. X-ray detectors are commonly found in most modern SEM and TEM systems, thus providing the user multiple capabilities from the one system. Further detail of an EDX can be found in B.4.

4.2.7 Reflection High-energy Electron Diffraction (RHEED)

RHEED uses the same principles as the XRD to attain a local snapshot of the crystal structure, using electrons rather than X-rays, typically within a TEM. Its similarity to XRD is shown in Figure 4.3b, with the concentric electron scattering patterns highlighted and aligned with the XRD pattern for this sample. In this work, RHEED is used to determine the crystal properties of a Ge sample undergoing TEM analysis.

4.2.8 Raman Spectroscopy

Raman spectroscopy is used within this thesis to demonstrate the amount of stress induced in epitaxial layers formed on SiC. Based on photons interacting with the lattice structure, the technique involves a laser being shone onto the sample. An individual photon will

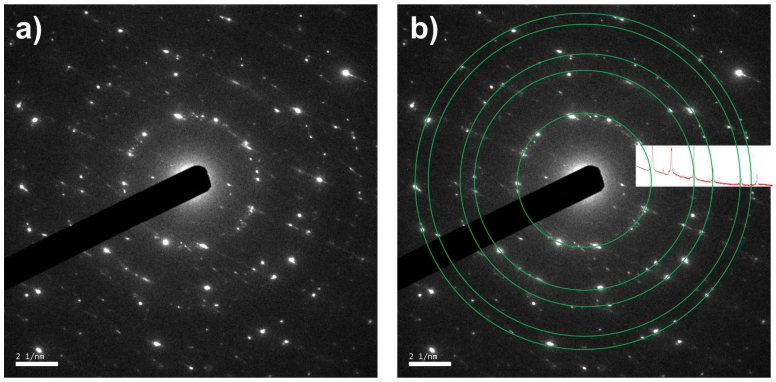


Figure 4.3: a) The RHEED profile of a Ge sample within a HfO_2/Ge/SiC stack. b) The same profile with the sample's XRD scan aligned to the highlighted concentric rings.

interact with an atom, resulting in another photon being emitted, due to a transference of energy.

The wavelength of the emitted photons from a sample are compared to those that were fired into the sample, with the difference recorded as the Raman Shift. The Raman Shift of a given element is unique, meaning the technique can be used for elemental identification, as in the EDX. However, the Raman Shift is also dependent on the stress of a layer, so by comparing the Raman Shift of a relaxed substrate with a layer heteroepitaxially grown on another semiconductor, one can determine the level of stress induced in the layer.

The Raman spectrometer used throughout this work is a Jobin-Yvon T-64000 attached to an Olympus microscope, equipped with a liquid-nitrogen-cooled CCD detector.

4.3 Electrical Characterisation Techniques

The physical characterisation can tell us only so much about how a device is going to work. Given a flat single crystal surface, one expects that the mobility will be high, and hence the resistance low. Given no unwanted oxide and few contaminants one would also

expect a good interface between the materials. However, only in the electrical analysis can we quantify these factors, discovering how the layers of materials will perform in a real device.

4.3.1 I-V analysis

The cornerstone of device analysis is the simple, yet very powerful current-voltage (I-V) measurement. I-V analysis of a simple Schottky diode, can provide the breakdown voltage (V_B) and the leakage current (I_L) when reverse biased. The forward voltage drop (V_F), ideality factor(n), Schottky Barrier Height (SBH) $\left(\Phi^0_{B,n}\right)$ and specific on-resistance ($R_{on,sp}$) can all be found under forward biased conditions.

4.3.1.1 Low Power I-V analysis

The majority of the I-V measurements described within this document were performed on a simple probe station and the low power Agilent Technologies B1500A Semiconductor Device Analyser. The probe station was setup for either lateral or vertical device measurements with four Karl-Suss probes providing two pairs of force and sense, a setup that removes probe resistances. A conducting back plate allows connections to be made to the back of a device.

To perform a simple voltage 'sweep', the analyser provides a known voltage across the device and measures the current being passed through it. The voltage is incremented in predetermined steps, for example, from -10 to 10 V at 20 mV steps is a very typical 1001 step sweep. The amount of current allowed to pass through the device is limited by the power rating of each Source Measuring Unit (SMU) used. The high power SMU is able to reach 20 V at 1 A or 200 V at 50 mA.

An example of a simple J-V plot for a heterojunction Schottky diode is presented in Fig. 4.4 to demonstrate the extraction techniques. The same data has been plotted twice, in logarithmic form, and in linear form. The logarithmic shows the very small leakage current in the reverse direction, as well as the turn on characteristics up until the point at approximately 1 V, where the current begins to become limited by the specific on-resistance. This can be seen in the linear plot where Ohms law allows for the simple extraction of the resistance.

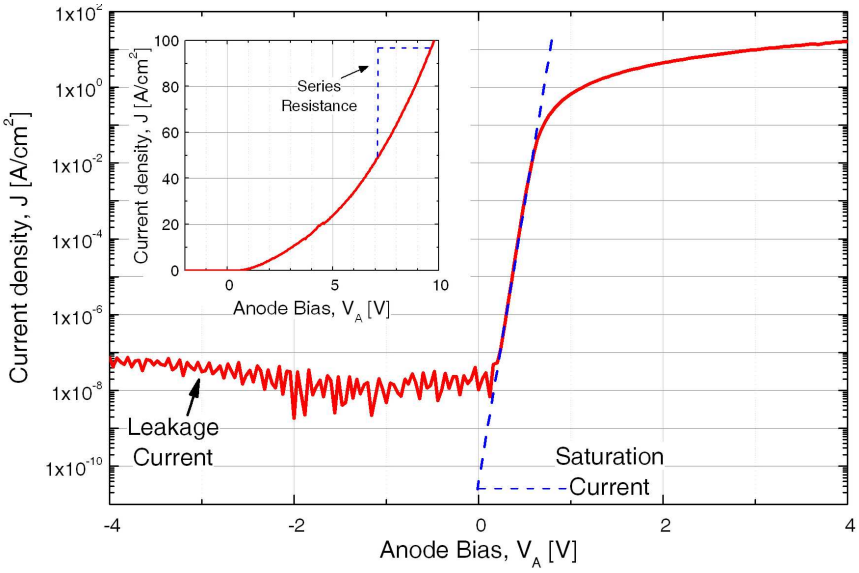


Figure 4.4: A typical current-voltage trace for a heterojunction Schottky diode with the parameter extraction techniques indicated.

Considering the logarithmic plot, the linear turn-on characteristic displayed from approximately 0.3 to 0.8 V can be used to extract $\Phi^0_{B,n}$ and the ideality factor. The linear region is dictated by the thermionic emission equation, rearranged here from Equation 3.12,

$$J = J_s \left(e^{\beta V/n} - 1 \right). \tag{4.1}$$

and where the saturation current, J_s, is defined as,

$$J_s = A^{**}T^2 e^{-\beta\Phi^0_{B,n}}. \tag{4.2}$$

J_s can be determined graphically from the logarithmic plot of Fig. 4.4 by extrapolating the linear region of the plot to $V = 0$. This enables the extraction of $\Phi^0_{B,n}$ from Eq. 4.2, given that the other values are all known constants. The ideality factor can be found by rearranging Eq. 4.1 to,

$$\ln(J) = \beta V/n + \ln(J_s) \tag{4.3}$$

which is in fact the equation for the straight line in the logarithmic plot of Fig. 4.4. Therefore the gradient of this line is equal to β/n, which then easily leads to the determination of n due to β being a constant.

The extraction of $\Phi^0_{B,n}$ and the ideality factor requires a reasonably high resolution I-V sweep, so that there are sufficient data points available within the linear turn-on region. The linear fit to this data is then carried out in Microcal Origin, a piece of software designed specifically for graphing and data-analysis. It is worth pointing out that the values of $\Phi^0_{B,n}$ and ideality factor quoted herein are estimates, and the software gives an uncertainty value as to the accuracy of these figures. All the data used in Chapter 6 was found to be within 0.25% accuracy - for example the maximum error of $\Phi^0_{B,n}$ was ± 0.0026 eV, though this was more typically lower than ± 0.0015 eV. For this reason, these values are quoted in this thesis to three decimal places with a good degree of accuracy.

4.3.1.2 I-V measurements at varying temperature

The SBH found via a single I-V measurement is a very useful first indicator; however, in reality the SBH of an interface is a complex parameter that is dependent on temperature,

whilst the quality of the interface and the build up of imperfections can lead to local SBH fluctuations. Considering the SBH against temperature is a useful way to find out more information about the parameter, and indeed the nature of the interface.

In order to extract this information, a Tenney environmental chamber is used to step the ambient temperature up in 25^{o}C intervals from -50^{o}C to 175^{o}C (225-450 K). To contact to the diodes from outside the chamber, the individual diodes are wire bonded to a PCB board, from which, heat proof wires are passed out of the chamber to the Agilent Technologies B1500A Semiconductor Device Analyser. The temperature was controlled and monitored in the chamber by a Watlow Series 942 temperature controller and verified using a Fluke 52 II Thermometer, the ends of which were placed on the PCB board.

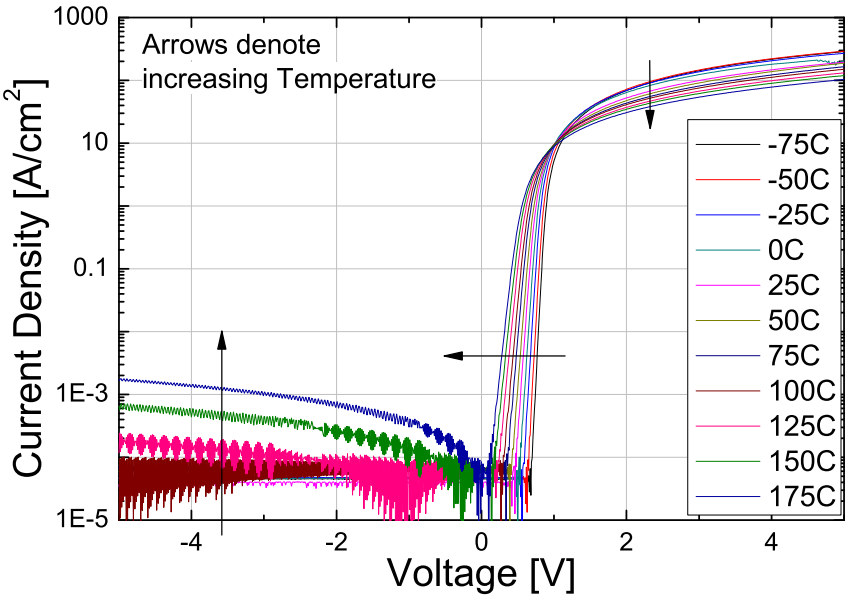


Figure 4.5: Current-voltage curves taken at ambient chamber temperatures from -75°C to 175°C

Figure 4.5 shows a temperature dependent I-V plot of a Schottky, heterojunction diode. The temperature is seen to have a direct effect on the plot due to the reliance on tem-

perature of most of a device's key parameters. Carrier mobility drops away significantly with rising temperature because increased lattice vibrations mean that there are more scattering events. This causes the rise in resistance observed above 1 volt. Furthermore, as temperature rises, thermionic emission current will increase, and the built-in potential decreases causing respectively, the variations in reverse leakage current and turn-on voltage.

Using the techniques described previously, the SBH, ideality factor and the saturation current may be extracted from each of the individual I-V plots of Figure 4.5. Though not immediately obvious, the SBH and the ideality factor both rely on temperature to a similar degree. Therefore, plotting the values against each other for a given temperature reveals a straight line. One technique suggested by Schmitsdorf et al [69] uses the extrapolation of this linearity to find an "ideal" barrier height, denoted $\Phi_{\eta=1}$, at $\eta = 1.0$.

The saturation current was defined in Equation 4.2, and this may be rearranged in order to quantify the SBH independent of temperature.

$$\ln\left(\frac{J_S}{T^2}\right) = -\frac{q\phi_{Rich}}{k}\frac{1}{T} + \ln\left(A^{**}\right). \tag{4.4}$$

Hence, plotting $\ln\left(J/T^2\right)$ against the inverse temperature will reveal a SBH value (ϕ_{Rich}) on its slope and the natural log of the Richardson constant (A^{**}) at its Y-intercept. ϕ_{Rich} represents an average value of all those extracted from the I-V-T plots. This technique is known as a Richardson plot.

The techniques used to find $\Phi_{\eta=1}$ and ϕ_{Rich} will be used in Section 7.2, where we will also look at the weaknesses of the Richardson Plot and ways to overcome this.

4.3.1.3 High Power I-V analysis

The Agilent Technologies B1500A Semiconductor Device Analyser, is perfect for low voltage, high resolution testing. However, in analysing our devices we need to consider higher voltages for breakdown and leakage tests. An ideal diode would have a very high breakdown voltage, up to which no reverse current would flow. In practice, the breakdown voltage can reach hundreds of volts, but there will always be at least some minute leakage. To facilitate the higher voltages required, breakdown tests are carried out using a Tektronix 571B Curve Tracer, a facility that can be run under high current (30 V/100 A) or high voltage (3000 V/10 mA) modes. Whilst the resolution is not as high as the Agilent, simple I-V plots can be acquired showing the point at which the reverse current has suddenly surged, indicating breakdown.

4.3.2 C-V Analysis

Capacitance-Voltage (C-V) characterisation is a technique that has long since been used to analyse metal-semiconductor contacts and MOS devices. When considering heterojunction layers, the use of a highly doped, degenerate heterojunction layer on the SiC, allows many parallels to be drawn between the extensive research carried out on M-S junctions [70] and the heterojunction diodes. Similar to a M-S interface, the space charge region can be presumed to be entirely on the lower-doped SiC side due to the huge doping differential. Hence, a variation of the voltage across the heterojunction alters the width of this space charge region, in turn impacting on the interface capacitance.

Once again, the C-V characterisation technique is carried out using the Agilent Technologies B1500A Semiconductor Device Analyser. Using fundamental capacitance equations, one can build up an equation that relates the Schottky barrier height and the bulk

doping to the inverse square of the capacitance (C^{-2}), such that

$$\frac{1}{c^2} = \frac{-2\left(\psi_{bi} + V_A + \beta\right)}{qA^2 K_s \varepsilon_0 N_D}, \tag{4.5}$$

This fundamental relationship is derived in Appendix C. After conducting a conventional C-V plot of a diode, a plot can be constructed relating the inverse square of the capacitance to the voltage, as shown in Figure 4.6. The doping of the structure is estimated from the inverse slope of the data, whilst the built-in potential (ψ_{bi}) is estimated from the x-intercept.

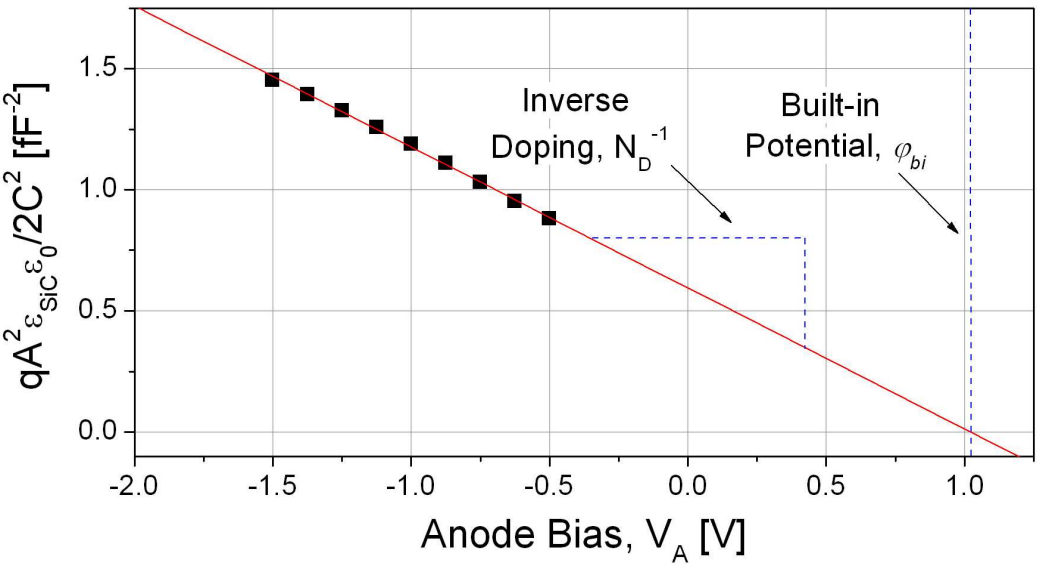


Figure 4.6: A typical C^{-2}-V trace for a heterojunction Schottky diode with the parameter extraction techniques indicated.

Despite being one of the most traditional measurement techniques available, its results are riddled with cautionary tales, and in Section 6.3.1.2, the limitations of this technique will be detailed.

4.3.2.1 C-V analysis and its use for heterojunctions

C-V analysis can be used to produce a one-dimensional doping profile of a layer from the surface downwards. For a given DC offset in a C-V sweep, the capacitance attained can be used to find the SCR width (W) and the majority carrier density $n(W)$ at this point. Both of these values are attained from simple manipulations of earlier equations. A rearrangement of Eq. C.6 gives,

$$W = \frac{K_S \varepsilon_0 A}{C}. \tag{4.6}$$

The majority carrier concentration is attained from rearranging Eq. C.9 to,

$$n(W) = \frac{2}{K_S \varepsilon_0 A^2 \left(dC^{-2}/dV_A\right)}. \tag{4.7}$$

Hence, the carrier concentration can be plotted against the SCR width for every given capacitance value. A test of this technique was carried out using a Ge/SiC diode, with 300 nm of HD-Ge ($N_D = 5 \times 10^{19}\ cm^{-3}$) upon a SiC substrate ($N_D = 1.4 \times 10^{15}\ cm^{-3}$). The result is shown in Figure 4.7.

The switch from using the doping concentration (N_D) to using the majority carrier concentration $n(W)$ is pertinent. Much discussion [65, 71–74] has concluded that this is a more accurate parameter, as the derivations used in Appendix C, assumed a perfect situation in which the space charge region ($x < W$) was completely depleted of majority carriers ($n(x) = 0$) and that the bulk ($x > W$) is in neutrality ($n(x) = N_D$). This is a very good approximation when the device is reverse biased, such as it is for determining the SBH. However under zero- or forward biased conditions, additional charge due to excess minority carriers in the quasi-neutral regions renders this approximation inaccurate.

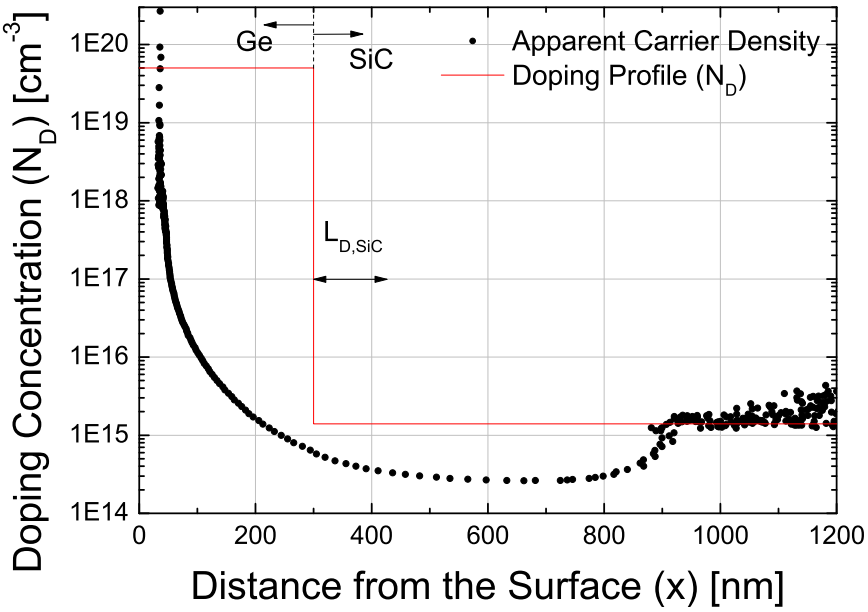


Figure 4.7: A one-dimensional doping profile of a n-type 300 nm Ge/SiC heterojunction diode.

Instead, the apparent carrier density is profiled $\hat{n}(x)$, a value that is an approximation of the majority carrier density $n(x)$. This is a good approximation until the electron concentration varies on a scale less than the Debye Length (L_D), a phenomena known as Debye smearing. L_D is defined as,

$$L_D = \sqrt{\frac{kTK_s\varepsilon_0}{q^2 n}}. \tag{4.8}$$

When $n(x)$ varies by a significant amount over a distance less than L_D, then $\hat{n}(x)$ will take an average $n(x)$ value over a distance, in the order of L_D. Hence abrupt changes in doping concentration from layer to layer will not be recorded by C-V profiling. In the examples used here, the Debye length is calculated to be 127 nm for the bulk SiC and 0.47 nm for the Ge. With an abrupt step change as from the degenerate Ge to the lightly doped SiC, the $\hat{n}(x)$ averaging witnessed in Fig. 4.7 is significant, though at a distance $5L_D$ from

the interface, $\hat{n}(x)$ and the predicted N_D appear to converge. A solution relating $\hat{n}(x)$ back to $n(x)$ over distances less than L_D [75] has been proven by simulations [72] to be an ineffective simplification.

4.3.3 CTLM Structures

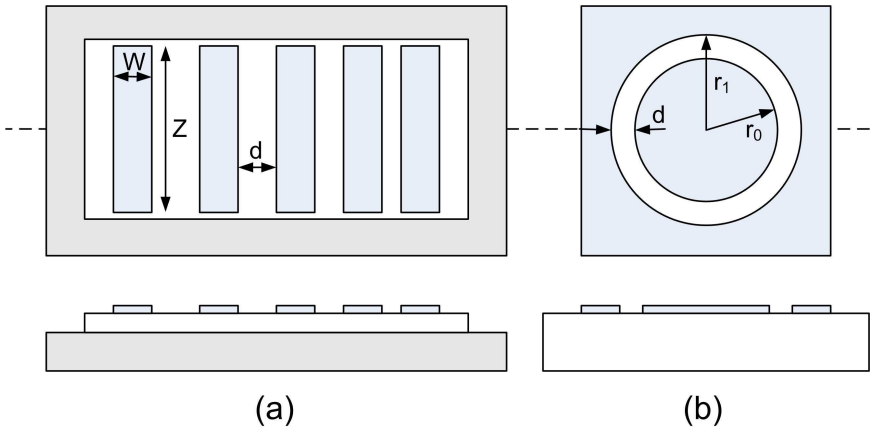


Figure 4.8: Plan- and side-views of the test patterns used for ohmic contact characterisation: (a) Rectangular TLM pattern, (b) CTLM pattern.

The Transmission Line Model (TLM) is a technique designed to extract the specific contact resistance ρ_c of the metal-semiconductor contact, a value of units $\Omega - cm^2$ that is used to compare the quality of ohmic metal-semiconductor contacts. The sheet resistance of the material (R_{sh}) directly beneath the metal contacts is also extracted, a value measured in $\Omega/\square$. TLM structures consist of three or more rectangular contacts with increasing spacing between them as seen in Figure 4.8a. By applying a constant current through adjacent pairs of contact pads a voltage drop between them can be recorded, and hence a value for the total resistance between the pads, R_T can be extracted. Plotting R_T against d, the distance between the pads, results in a straight line, the gradient of which is proportional to R_{sh}. Where this line crosses the X-axis, is a value equal to twice

the transfer length (L_T), a distance over which most of the current will pass from semiconductor to metal or vice versa [65]. This is demonstrated in Figure 4.9, where the line has been fitted to the data using a least squares routine.

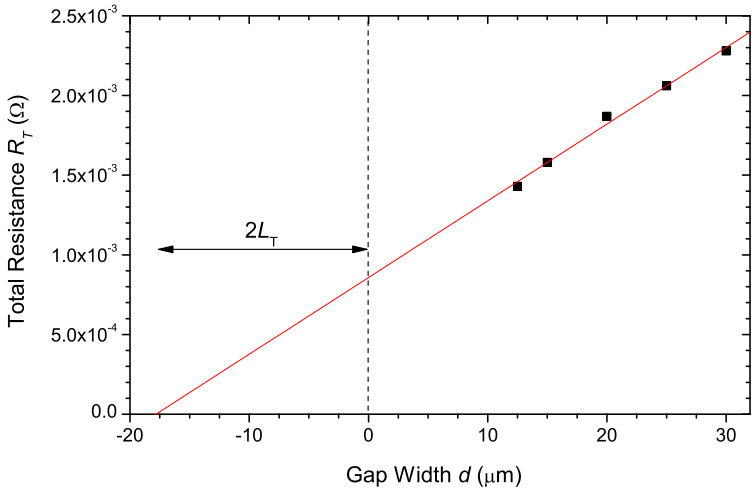


Figure 4.9: The determination of the Transfer Length parameter, L_T.

Having extracted L_T, R_{sh} can be determined using the dimensions of the TLM structure [76],

$$R_T = R_{sh}\frac{L_T}{Z}\frac{\cosh\left(X/L_T\right)}{\sinh\left(W/L_T\right)}. \tag{4.9}$$

If $W >> L_T$ then Equation 4.9 may be simplified to,

$$R_T = R_{sh}\frac{L_T}{Z}. \tag{4.10}$$

The specific contact resistance ρ_c is found using the transfer length and sheet resistance,

$$L_T = \sqrt{\left(\frac{\rho_C}{R_s h}\right)}. \tag{4.11}$$

The downside of this technique is that current can flow between the contacts in the region beyond the test structure unless a mesa etch is used to isolate the test structure such as that seen in Figure 4.8a. However, this is a potentially complicated extra processing step requiring another mask. To overcome this Reeves [77], introduced a Circular Transmission Line Model (CTLM) which was later refined by Marlow and Das [76]. In order to remove the stray current flow, a series of circular pads were employed consisting of a conducting inner region of radius r_0, a gap of width d and a conducting outer region with radius r_1 [65]. One such structure is illustrated in Figure 4.8b. Throughout this work, five such structures were used with r_0 typically 150 μm and the gap width varying between 10 and 35 μm.

The total resistance, R_T, between r_0 and r_1 is [76],

$$R_T = \frac{R_{sh}}{2\pi}\left[\ln\frac{r_1}{r_0} + \frac{L_T}{r_0}\frac{I_0\left(r_0/L_T\right)}{I_1\left(r_0/L_T\right)} + \frac{L_T}{r_1}\frac{K_0\left(r_1/L_T\right)}{K_1\left(r_1/L_T\right)}\right], \tag{4.12}$$

where L_T is found using the same graphical method described above, and I_0, I_1, K_0 and K_1 are the modified Bessel functions, given by Willis [78] as

$$K_v(t) = \left(\frac{\pi}{2t}\right)^{1/2} e^{-t}\left\{1 + \frac{(4v^2-1^2)}{1!(8t)} + \frac{(4v^2-1^2)(4v^2-3^2)}{2!(8t)^2} + ...\right\} \tag{4.13}$$

$$I_v(t) = \frac{1}{(2\pi t)^{1/2}} e^{t}\left\{1 - \frac{(4v^2-1^2)}{1!(8t)} + \frac{(4v^2-1^2)(4v^2-3^2)}{2!(8t)^2} - ...\right\} \tag{4.14}$$

ρ_c can then once again be found using Equation 4.11.

Chapter 5

Silicon Carbide Heterojunction Formation

5.1 Introduction

In this Chapter the deposition of Ge (and briefly Si) onto SiC will be studied, with the aim of producing heterojunction layers ideal for the diode and MOS devices that will be formed respectively in Chapters 6 and 8. As such, the narrow bandgap layers are required to be flat, crystalline, uniform and homogeneous to maximise channel mobility and to minimise series resistance and interface charge. This is not a simple problem, the difference in crystal structure between the cubic narrow bandgap semiconductors and the hexagonal compound of silicon carbide dictating that the two materials should not, and often will not, adhere. The Chapter concentrates on the use of Molecular Beam Epitaxy (MBE) and wafer bonding (WB), the former offering the opportunity to form better interfaces at the expense of the crystallinity and surface finish offered by WB. The state-of-the-art microscopy techniques introduced in 4.2 show Ge layers outperforming Si, as they produce shallower islands at low thickness and reasonably flat, polycrystalline layers at 300 nm and above. It shall be seen that the use of high temperature, small,

light dopants and optimal thicknesses will produce the layers with maximum crystallinity and minimum grain boundaries, requirements necessary for producing the low-resistance layers desired in future Chapters.

First however, this physical analysis will be introduced by considering to what degree these layers meet the intended goals of a heterojunction device.

5.2 Ge/SiC Heterojunction Growth: The ideal situation and the realities.

From the theory introduced in Section 3.3, an ideal situation for the formation of a heterojunction layer may here be outlined followed by a discussion on the realities that most often prevent the formation of perfect layers.

To assess the ideal situation we must first revisit the purpose of forming the layers. A Si/SiC heterojunction could overcome one of two pertinent problems that hinder SiC MOSFET development, namely the inferior oxide formation and channel mobility. Silicon dioxide grown on SiC suffers from the build up of interface traps at the semiconductor/oxide interface, due to carbon clusters that are not released in the oxidation process. This introduces scattering at the semiconductor surface, much reducing the already low channel mobility. Pure silicon has no such problem however, and hence two options present themselves when considering a Si layer on SiC. The Si layer can either be entirely sacrificed through the oxidation of the epitaxial layer, thus forming a SiC/SiO_2 interface potentially free of carbon clusters, or the SiO_2 layer can be formed on the top of the Si, forming a $SiC/Si/SiO_2$ device. Either option should dramatically reduce the concentration of traps at the interface. The further benefit of the $SiC/Si/SiO_2$ device is

that the electron mobility of Si is 50% better than SiC's whilst the hole mobility of Si is 5 times that of SiC's.

The use of Ge is attractive due to its even higher mobility, which for n- and p-type materials is respectively, 4 and 20 times bigger than SiC. The use of Ge however, rules out the sacrifice of the entire layer, as the natural oxide of Ge is unusable. Hence when considering Ge as a heterojunction solution, we must consider a High-K/Ge/SiC structure. The issues that need to be considered in creating such a device are presented in Figure 5.1. The ideal situation shown is one where a flawless transition occurs between the semiconductors, free of any inhomogeneities such as contaminants, surface roughness, or defects. As a result, the SiC face would have to be atomically flat, upon which Ge would be grown layer by layer (FM Growth) leading to an atomically flat Ge surface and hence, a MOS channel free of scattering events. A single crystal of Ge would also maximise the potential mobility that could be achieved due to the elimination of grain boundaries that amorphous or polycrystalline layers introduce.

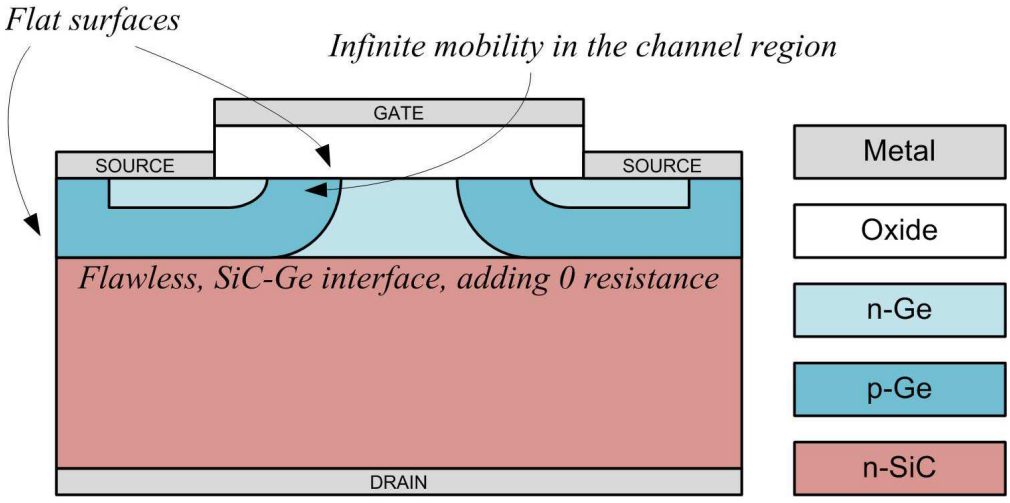


Figure 5.1: An ideal Ge/SiC heterojunction MOSFET.

5.2 Ge/SiC Heterojunction Growth: The ideal situation and the realities.

So the ideal Ge/SiC heterojunction MOSFET will be achieved if we can grow single crystal Ge on atomically flat SiC. Atomically flat SiC is a challenge but attainable. The SiC wafer bought from Cree Inc. is research grade, and AFM micrographs presented in [79] of the SiC surface reveals the surface roughness before and after a RCA clean. Prior to the clean, the rms roughness is 23 Å, reducing to 11 Å afterwards. It is possible that this could be improved through polishing of the SiC wafer prior to processing [80].

Unfortunately, the limitations of mismatched lattices, discussed throughout this Section, result in a challenging processing problem. Due to Ge being a cubic structure and SiC being hexagonal, heteroepitaxial growth on the majority of planes will be hindered by entirely misaligned bonding patterns. Having said this, the (111) crystal orientation of Ge is hexagonal, and whilst the 1:1 match of Ge to SiC atoms is not possible, we will see later that a rotation in the crystal allows for the potential alignment of every few atoms. However, the likeliest outcome when forming any Ge layers on SiC is the build up of strain and hence the formation of large polycrystals.

One way to relieve the strain between layers is to step up the lattice constant using monolayers of materials with progressively larger lattice constants layer at a time, until single crystal Ge can be grown to a reasonable width [81, 82]. However, with mismatches this large this would be a big task, and generally we must accept the usual growth mode is VW or SK, with a polycrystalline layer forming.

Polycrystal formation has an effect on two of the requirements described in Figure 5.1. Firstly, regardless of the substrate surface quality, the Ge surface will form in individual polycrystals that result in a rough surface. This could possibly be polished afterwards, though this has not been tried. Secondly, the channel mobility is diminished by the presence of grain boundaries throughout the layer. A grain boundary can be seen as a homojunction formed between two like materials of differing crystal orientation. Hence

there is a very small barrier that will need to be overcome in passing between crystals due to the differing conduction properties of different crystal orientations. Whilst the energy loss will be minimal over only one of these boundaries, with crystal sizes no bigger than 200 nm, there may be a lot of them.

Another solution exists to tackle the surface quality of the Ge; however, it comes at a price. Growing the layers at very low temperature leads to amorphous layers given that the adatoms have little energy to find a bonding site. The lack of energy means that there is no chance of the layer forming into a single crystal, due to the large amount of energy the adatoms require to seek sites to minimise their dangling bonds. Instead, the adatoms will tend to remain in the position where they are deposited, creating either an entirely amorphous layer or a polycrystalline layer with very small grain sizes. The benefit of this is that the resulting layer will be close to being as flat as the substrate beneath. However, there is a large detrimental affect on the electrical characteristics, with the number of grain boundaries having been multiplied, increasing on-resistance.

A second solution is to attempt wafer bonding, forcefully uniting the layers through the exploitation of van der Waals forces which keep the layers together. This allows for the creation of a single crystal heterojunction layer, with very high mobility and a flat surface. However, the potential problem area with this solution is the heterojunction interface, where a very inhomogeneous contact is likely to result between the SiC and the narrow bandgap wafer.

5.3 Thin Film Processing Techniques

The starting point for all of the devices is an unprocessed 4H-SiC wafer bought from Cree Inc. To develop this into the heterojunction devices, the surface must first be cleaned,

removing any residual material from the wafer surface before depositing (or wafer bonding) the silicon or germanium.

5.3.1 SiC Wafers

Cree Inc. [12] supply wafers of 4H-SiC and 6H-SiC up to a diameter of 100 mm, with optional epitaxial layers formed 0.2-50 μm thick on the substrate surface. The doping of both the substrate and the epitaxial layer can be selected independently between 9×10^{14} and 1×10^{19} cm^{-3}, n- or p-type. The quality of the wafer is determined by the density of the micropipe defects, with Cree's best being guaranteed to have less than 1 micropipe/cm^2 at elevated cost; these are their so-called "Micropipe free" range. One must also select the orientation of the crystalline structure with respect to the surface of the wafer. So called 'on-axis' wafers are available whereby the silicon and carbon layers within the crystal structure align parallel to the surface leading to an atomically flat surface. However, with the Si and C atoms forming SiC in stacked layers, the surface of on-axis wafers will always be a silicon face or a carbon face. This prevents the growth of an epitaxial layer as both the Si and C atoms will require bonding sites when they are deposited on the SiC surface. Hence, any wafers with epitaxial layers are supplied either 4 or 8 degrees off axis. These do not achieve the same atomically smooth surfaces. Other SiC substrate suppliers exist other than Cree as do companies that grow the epitaxial layers; however Cree accounts for around 80% of the market being the only company to offer both of these services at a low micropipe density.

The cost of SiC makes exhaustive research a difficult task on a budget, with 100 mm wafers typically costing between $3000 and $10000. The huge variation in cost comes mostly from the epitaxial layer, which costs approximately $100 per μm, though there is

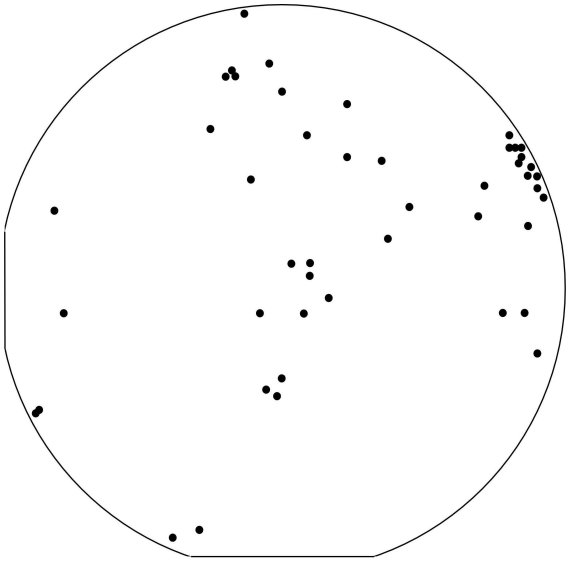


Figure 5.2: The micropipe map of the 4H-SiC wafer used in this project (with micropipes made larger for visibility).

also a wide variation in wafer quality available. For this reason the body of work carried out in this thesis was carried out on half of a SiC wafer diced into smaller 10 × 10 mm chips.

The wafer used for all the MBE work was a 100 mm diameter, 4^o off axis 4H-SiC substrate, with a bulk n-type doping of 1×10^{18} cm^{-3} and a 10 μm, lightly n-type doped ($1.4 \times 10^{15} cm^{-3}$) epitaxial layer. The wafer was a research grade wafer meaning than it had a reasonably large density of defects, defined by Cree as covering no greater than 30 % of the wafer. The micropipe density of the wafer was 31-100 per cm^2, and the "Micropipe Map" supplied with the wafer is shown in Figure 5.2. Given that this is a 100 mm diameter wafer, the density appears much better than projected. However, many hundreds of micropipes appear right at the very wafer edge, not shown here, and hence, chips from the centre of this wafer were used to develop these heterojunction devices. It was calculated that in the worst case scenario, micropipes will occur in 1 in 30 of the

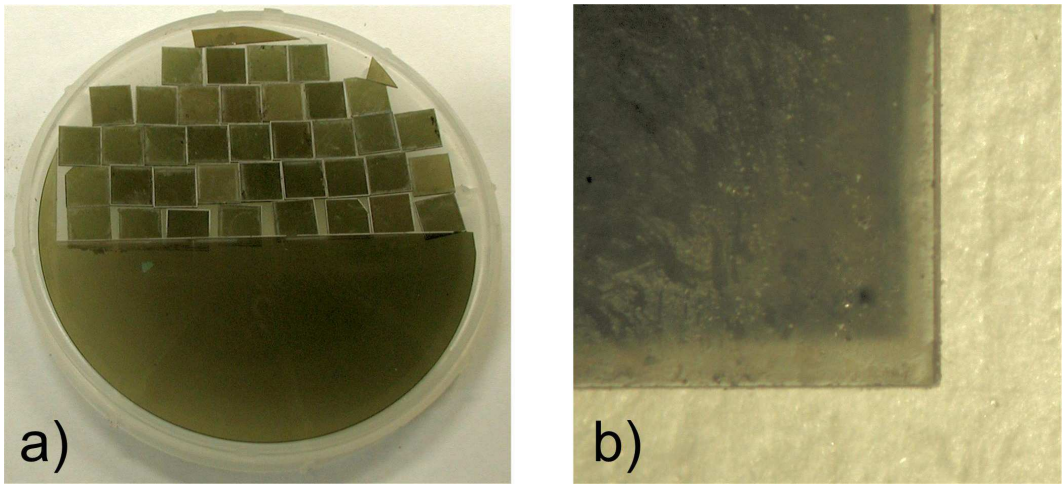


Figure 5.3: The result of the laser cutting of the 4H-SiC wafer. a) the diced wafer and the remaining half a wafer and b) a close up of the wafer surface at a chip corner.

devices made on this wafer at the most, as the eventual diodes were formed from 200 μm diameter dots.

5.3.2 SiC Wafer Dicing

Due to the aforementioned expense of the substrate material, the half-wafer was diced into 38 10×10 mm chips using a Nd:YAG micromachining laser. Figure 5.3a shows a previous SiC wafer dicing performed by a University of Warwick colleague, with the chips aligned as they were prior to dicing. 5.3b shows a close up image of the corner of a single chip. The damage at the edges appeared to be minimal though a very large quantity of dirt and dust was visibly spread over the wafer. To prevent this happening for the chips used in this work, the chips were covered in photoresist prior to laser cutting. Although the damage at the edges appears minimal here, a commonsense approach was taken when selecting diodes for electrical testing, choosing those closest to the chip centre.

Those chips right at the wafer edge were used for testing due to the high density of

micropipes, which left 25 chips for the Ge/SiC heterojunction devices.

5.3.3 SiC Pre-Processing

Before processing the chips with metal contacts or applying the thin films the trace impurities on the substrate surface must be removed as they can have a detrimental affect on the electrical performance of a device. The cleaning is achieved using a three-stage process. A solvent clean is first, consisting of acetone, isopropanol and methanol being sprayed onto the substrate surface whilst it is rotating in a spinner unit. This removes some of the organic impurities [83].

Next, the Radio Corporation of America (RCA) cleans [84] are applied. The RCA cleans work by first removing the organic matter in the RCA1 formulation, then the metals and chemisorbed ions in the RCA2 formulation. The RCA1 clean consists of a 1:1:5 solution of NH_4OH:H_2O_2:H_2O at approximately 80^oC for 10 minutes. This solution leaves a very thin ($\sim 10\mathring{A}$) SiO_2 layer on the surface, which must be removed via a quick immersion in dilute hydrofluoric acid (HF), at a ratio of 50:1 H_2O:HF, at room temperature. The RCA2 procedure then consists of a 1:1:6 solution of HCl:H_2O_2:H_2O at approximately 80^oC for 10 minutes.

Finally, a "Piranha" clean (so named due to its ferocity) is used to remove any final organic material that may remain. A 10 minute dip in 1:1 mix of H_2SO_4:H_2O_2 produces an exothermic reaction that reaches 130^oC. Once again, a quick dip in 50:1 H_2O:HF after the Piranha clean removes any built up oxide.

Whilst this procedure has developed from the silicon industry, one study [14] has suggested that a clean consisting only of an RCA2 clean produces the best results; however this would not remove any metallic impurities.

This cleaning procedure is not appropriate for use on Ge due to the HF and H_2O_2 etching the material. In Chapter 6 we will outline an alternative cleaning method specific to forming metal contacts on the Ge/SiC surface.

5.3.4 Molecular Beam Epitaxy (MBE)

The MBE is used substantially within this work to deposit layers of Ge or Si onto SiC. The MBE technique was invented in 1960 in Bell Laboratories and involves the growth of epitaxial layers through the fine control of a beam of evaporated solids. Housed in individual Knudsen Cells, or K-Cells, the elements to be deposited are heated under high pressure until they sublimate [57]. In the University of Warwick's V100S MBE system, shown in Figure 5.4 these elements are the semiconductors Si or Ge, and the dopants boron, arsenic and phosphorous. The resulting elemental gas is formed into a beam using an aperture within the K-cell. The beam of gases is controlled by a shutter in front of the aperture that can be rapidly open and shut. This allows for the deposited material to be controlled down to the monolayer scale, whilst the amount of dopants employed is also finely controlled.

The growth parameters, including temperature, pressure and growth rate can be controlled during deposition, making the MBE a useful research tool. Temperature in particular has a large effect on the resulting layer, giving the individual atoms the energy they require to find their optimal bonding site where the maximum number of dangling bonds are eliminated. However, in a system where the minimum energy positions do not coincide with smooth layer-by-layer growth, the raised temperature will initiate faceting, the growth of islands, and the result will be a very rough, polycrystalline layer.

The 10x10 mm chips were entered into the MBE on a holding wafer of prime Si. As

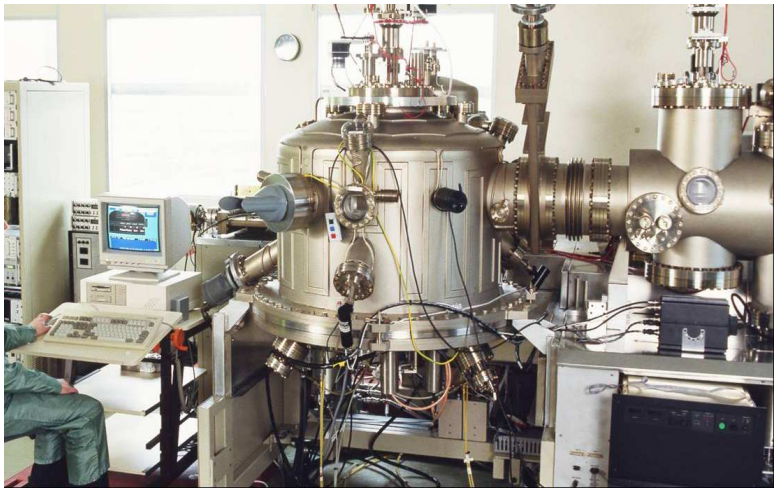


Figure 5.4: The University of Warwick's MBE Facility.

this holding wafers were covered with the same epitaxial layers, they were used as dummy substrates to perfect the fabrication processes before the SiC was used.

5.3.5 Si Wafer Bonding

Another method used within this thesis to form layers of Si on SiC, was that of wafer bonding, using the SmartCut technique. Although the technique is now commonplace within the silicon-on-insulator (SOI) industry, this is a new and somewhat experimental approach when considering SiC. The SmartCut process is shown graphically in Figure 5.5. Due to the cost and complexity of the process, it was only carried out just once, and hence the exact process is laid out here.

Wafer bonding was performed on commercial 3 inch 4H-SiC substrates from Cree Inc., USA. Two wafers, one 4^o-off axis, doped at 1.4×10^{18} cm^{-3}, the other on-axis, highly doped at 1×10^{19} cm^{-3} were used. The Smartcut process transferred a 300 nm p-type Si wafer doped at 1×10^{17} cm^{-3} employing a hydrogen-ion implant, room-temperature wafer bonding, and subsequent heat-treatment for wafer splitting. Before wafer bonding

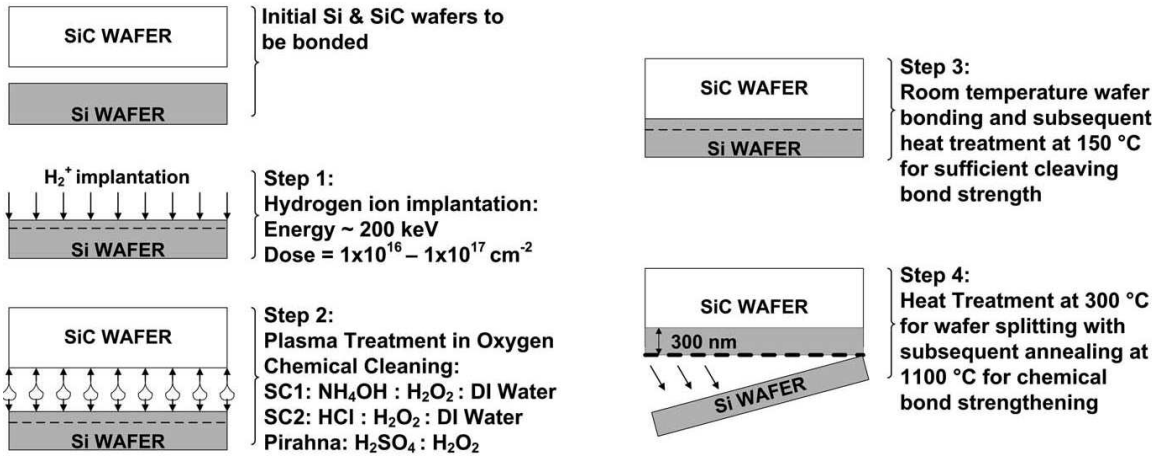


Figure 5.5: The SmartCut wafer bonding process.

was performed, the Si wafer was implanted with H_2^+ ions at an energy of ∼200 keV and a dosage in the range of $1 \times 10^{16} - 1 \times 10^{17}$ cm^{-2}. Both wafers were then cleaned using an oxygen (O_2) plasma treatment and a modified RCA1, RCA2, and piranha cleaning procedure for 20 min. Rinsing and drying of the wafers was performed before bonding. The wafers were then bonded in a vacuum at room temperature followed by a 150^{o}C anneal in order to achieve a sufficient bond strength for cleaving. Next, the wafers were cleaved at a temperature of 300^{o}C with further annealing performed at 1100^{o}C for 2 hours to further strengthen the chemical bonds.

5.4 Si/SiC Heterojunction Structures

The difficulty in achieving the perfect heterojunction layer, a single crystal with a flat surface and a defect free interface, was discussed in Section 3.3. Over the next two Sections, the two methods of layer formation, MBE and wafer bonding, introduced previously will be used to form Si/SiC and Ge/SiC heterojunctions and the resulting layers will be physically analysed using the techniques described in Section 4.2. When planning the MBE

deposition process, one is faced with an array of choices including, but not limited to, the choice of material to deposit, the temperature that it is grown at, the thickness of the layer and the choice of dopant, with the specific choice of dopant element being surprisingly relevant. All of these choices impact on both the physical and electrical characteristics of the layers and the challenges of finding the right combination is of high priority. The physical impact these deposition choices make on the layers can be monitored through microscopy techniques, AFM, HIM, TEM, FIB, and SEM and through crystal spectroscopy techniques XRD and EDX. The huge impact that these choices have on the electrical results, including the layer and contact resistivity, the Schottky barrier height manipulation, the Fermi level pinning and the interface inhomogeneity will be looked at in great detail in Chapter 6.

The idea of depositing a narrow bandgap semiconductor on SiC was reasonably novel when this project began. No papers existed on Ge/SiC, and only a limited amount of knowledge had been gathered on Si/SiC structures, much of it by a previous project at Warwick University. Therefore, to begin this project it was decided to use the tools available. The University had a wealth of expertise in using MBE to deposit Si, Ge or SiGe on Si [81, 82, 85], skills that had been utilised in a previous Engineering project to experiment with Si heterojunction layers on SiC [14, 15, 56]. Therefore, the starting point for this project was to run a new physical analysis of these existing Si/SiC samples.

The aim of the new Si/SiC analysis was to show how the MBE settings affected the Si growth. They also act later as a useful comparison, evidence as they are of how different semiconductor layers form on the SiC substrate. The samples used came from the same batch of chips processed in [14] and in [56]. The three depositions are shown in Figure 5.6.

The structures used in [14] came from single 10x10 mm SiC chips as described in

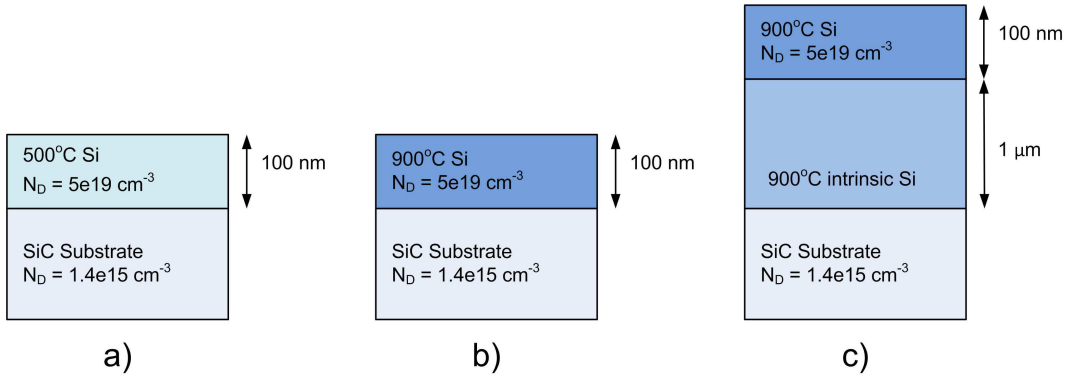


Figure 5.6: The intended structure of Si/SiC heterojunction layers. Image a) shows the amorphous 100 nm nSi layer, b) shows the polycrystalline 100 nm nSi layer and c) shows the polycrystalline 1 μm iSi layer.

Section 5.3.2, which were placed into the MBE. Figure 5.6a shows the Si/SiC layer that was expected to be amorphous, formed by depositing at 500^{o}C, highly n-doped ($N_{D,Ge} = 5 \times 10^{19}\ cm^{-3}$, antimony was the dopant) Si onto the chip. At a rate of 0.1 $\mathring{A}s^{-1}$, a deposition of 10,000 s (2 hrs, 45 mins) was expected to deposit 100 nm of Si. The second structure, shown in Figure 5.6b, was grown under identical conditions to the last layer but with a deposition temperature of 900^{o}C, it was intended to be polycrystalline. The third structure was the similar to the second but with an intrinsic Si buffer layer between the highly doped Si cap and the SiC substrate that would act as a drift region when it came to analysing these devices electrically. Furthermore, when these devices are formed into MOS devices, such low doped regions will form the channel, hence it will be imperative to understand the nature of a Si/SiC (or Ge/SiC) interface that is not degenerate on the Si (Ge) side. The buffer region was deposited at 1 $\mathring{A}s^{-1}$ for 10,000 s (2 hrs, 45 mins) and hence it was expected to be 1 μm thick.

Full justification of the MBE settings can be found elsewhere [14, 56], but they were chosen to compare the electrical and physical properties of amorphous/polycrystalline layers and the development of these properties with layer thickness. The doping was selected

so that ohmic contacts would form when metal was deposited, whilst the thicknesses were chosen to show two quite extreme examples of the thin and the thick films.

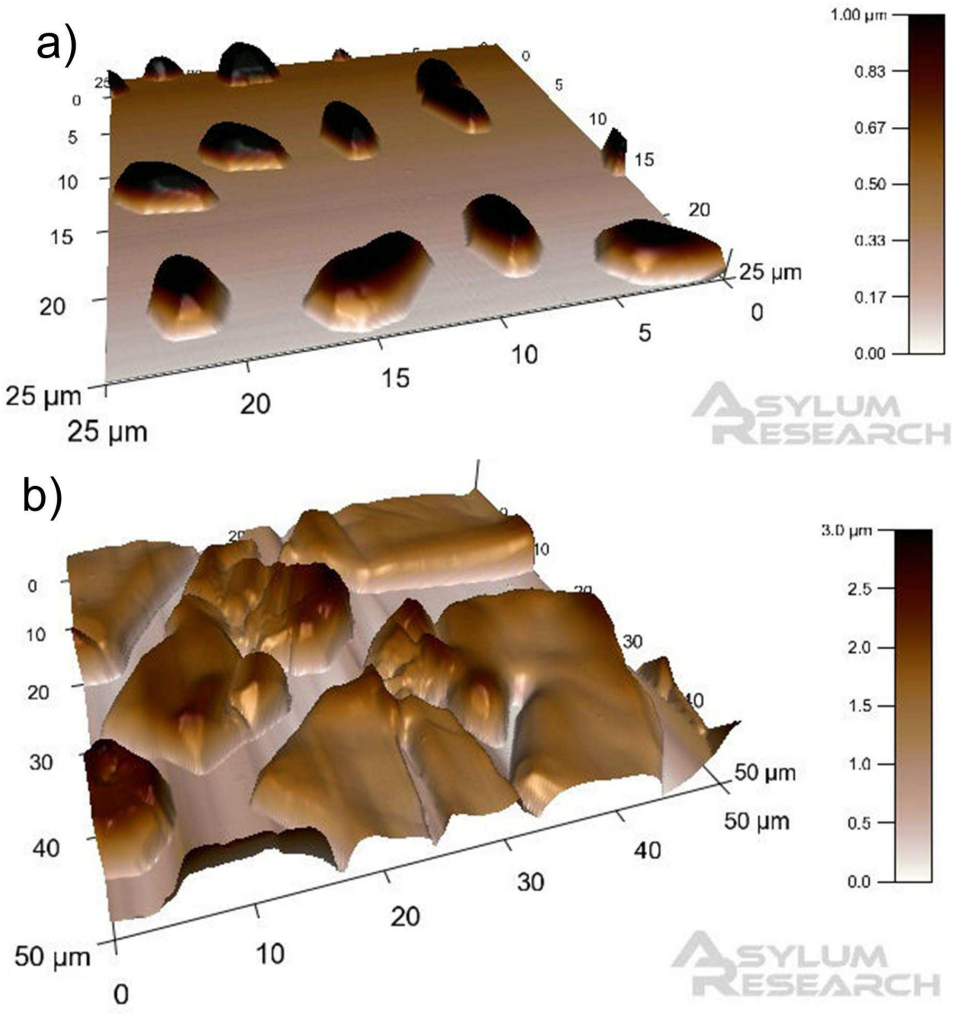


Figure 5.7: AFM images of the Si/SiC heterojunction layers. Image a) is of the high temperature n+ layer which was designed to be 100 nm thick. Image b) is the high temperature intrinsic layer that was designed to be 1 μm thick.

Considering first the high deposition temperature layers, a new physical analysis of them is shown in Figure 5.7 using AFM. Figure 5.7a shows the heavily n-doped layer that was designed to reach a uniform covering of 100 nm. However, the result was anything

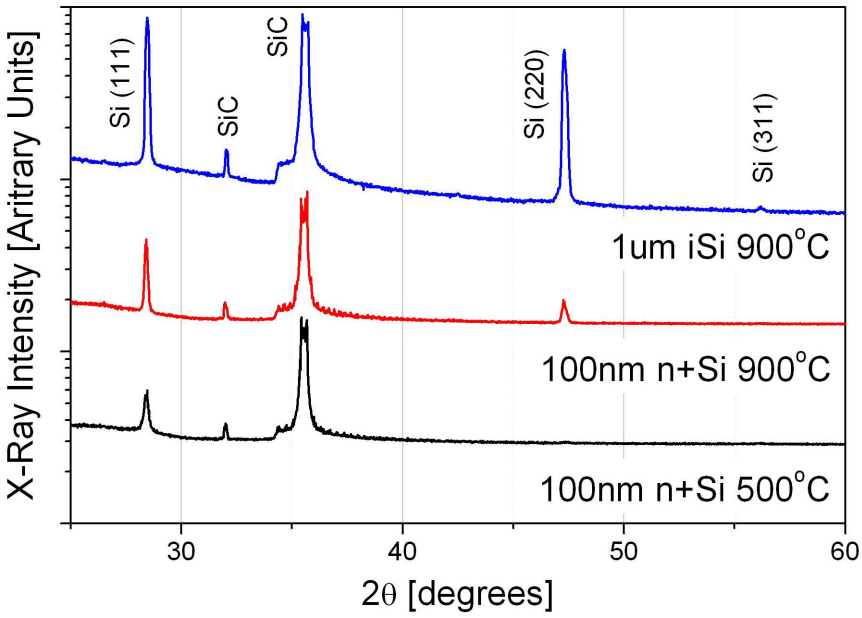


Figure 5.8: XRD results of the Si/SiC heterojunction layers.

but uniform, with the Si preferentially bonding to itself, forming quite significant islands up to 1 μm in height, with large areas between them. Figure 5.7b shows what happened to the Si when the layer thickness was increased. Some of the islands merged, but in general, they appear to have continued to grow in stacks, with large trenches between each one. The islands reached heights some 2-3 μm above the surface.

New XRD scans were performed over the entirety of the deposited layers and the results are shown in Figure 5.8. The SiC peaks are ever present in all the layers as expected. The high temperature layers show evidence of only the (111) and (220) peaks of Si, with the (111) peak significantly dominant in the 100 nm layer. This suggests that the majority of Si adatoms have sufficient energy to find a bonding site next to another Si atom, forming in the hexagonal (111) plane.

Given these results, it seems unlikely that uniform Si can be deposited on SiC at these raised temperatures as it appears to be energetically favourable for the Si to bond to itself

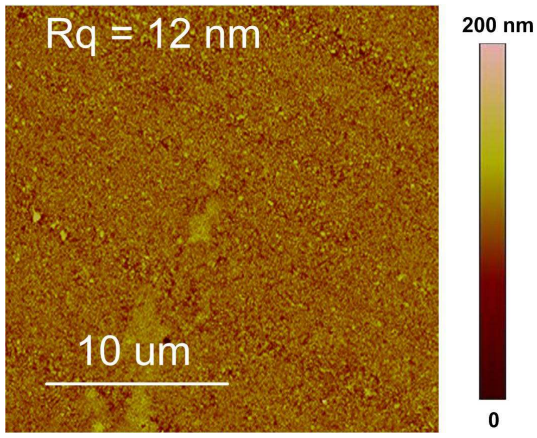


Figure 5.9: AFM image of the low temperature n+ layer which was designed to be 100 nm thick. Image reproduced with permission from [56]

than to the SiC surface. The reason for this may be that the growth temperature was too high, giving the layers too much energy as they come to the surface, thus enabling them to find other Si adatoms to bond to over the SiC surface. Alternatively, it seems more likely that the Si layers have a set of lattice parameters that are incompatible with the hexagonal SiC surface, making a FM or SK growth mode unobtainable. Appraising the poor electrical results achieved in [14, 15, 56] from these structures, it seems likely from Figure 5.7, that the devices formed patch contacts, whereby the metal layer contacted the Si and the SiC at the same time.

AFM results of the low temperature Si/SiC sample, repeated in Figure 5.9 with permission from [56], show a uniform Si covering but a very bumpy surface, the resulting roughness being 12 nm RMS over the scanned 25×25 μm area. The XRD result from this layer shows that a (111) peak is evident, despite the intention that this layer be amorphous. This suggests that this layer was in fact polycrystalline, explaining the high roughness value, whilst suggesting that the deposition temperature was not quite low enough to reach the degree of uniformity expected.

The point of relevance here is that lessons were drawn from these results that heavily affected the Ge/SiC depositions. The first point was that a high temperature deposition, 900^{o}C in this case did achieve a polycrystalline layer. Just as importantly, there is evidence that a 500^{o}C deposition is not low enough to form an amorphous layer. Because of the balling up of the Si in the high temperature layers, little can be concluded about deposition thickness. However, the intended values of 100 nm and 1 μm seem valid, allowing comparison between those layers forming and those (supposedly) fully formed. As for doping values, it is necessary that the top metal-semiconductor contact is ohmic, leaving the only rectification coming from the heterojunction region and hence the value of $N_{D,Ge} = 5 \times 10^{19}\ cm^{-3}$ seems valid as it, in theory, makes the semiconductor layer degenerate, though the validity of this will be checked in the next Chapter.

5.5 Ge/SiC Heterojunction Structures

In this Section, the development of the Ge/SiC structures will be traced, starting initially with their like-for-like comparison to the Si/SiC diodes that preceded them. Following the development of a second generation of the diodes it will then be possible to compare the Ge layers across thickness and dopant lines. Table 5.1 summarises all the layers that were produced over the two batches.

Dopant	n	n	i	i	n	n	p	p	i
Dep. Temp. (^{o}C)	300	500	300	500	200	500	200	500	500
Intended Thickness (nm)	100	100	1000	1000	300	300	300	300	500
R_q (nm)	1.8	60	6	45	2.1	6.7	3.5	30	32

Table 5.1: The deposition parameters and resulting surface roughness (R_q) of all the Ge/SiC layers formed over the two generations. The n-type dopant is antimony and the p-type dopant boron.

Off of the back of the Si/SiC analysis, the design of the Ge/SiC heterojunction diodes could begin. The most important difference between the depositions of Ge and Si is that Ge has a melting point of only 937^{o}C compared to 1420^{o}C for Si. This heavily influences the deposition temperatures required to form polycrystalline and amorphous layers. Taking first the amorphous layers, the failure of the Si layers to form smooth amorphous layers free of lumpy crystalline material, meant that the amorphous Ge layers needed to be relatively much smaller. Hence, it was decided to start the first Ge/SiC batch with a value of 300^{o}C, which could be modified up or down later if required. As for the high temperature deposition, the value of 500^{o}C was arrived at in an attempt to scale down the successful polycrystalline Si/SiC deposition that was 500^{o}C lower than its melting point. The rest of the deposition remained the same: 100 nm highly doped Ge ($N_{D,Ge} = 5 \times 10^{19} cm^{-3}$) with antimony as the dopant and 1 μm intrinsic Ge depositions. However, this time both high and low temperature depositions were carried out at the thicker layer completing a 2×2 test matrix of temperature and thickness. Each of the four depositions was carried out on one 10×10 mm SiC chip.

The first set of AFM results, shown in Figure 5.10, suggested immediately that the quality of Ge/SiC layers may be markedly better than that of the bunched, island ridden Si/SiC samples. Experimentally this set of AFM results consisted of only one 25x25 μm AFM scan per sample, though the results were typical of the layer.

Addressing first the amorphous layers. The chief problem with the Si/SiC layers was that the deposition temperature was likely too high, resulting in bumpy, somewhat polycrystalline layers. The AFM scan of Figure 5.10a shows that the layer appears very smooth, though significant diagonal marking appears. These marks can also be seen in Figure 5.10c, and are actually polishing marks from the SiC surface that have been faithfully replicated in the Ge layer. Also seen in Figure 5.10a are two vertical scratch

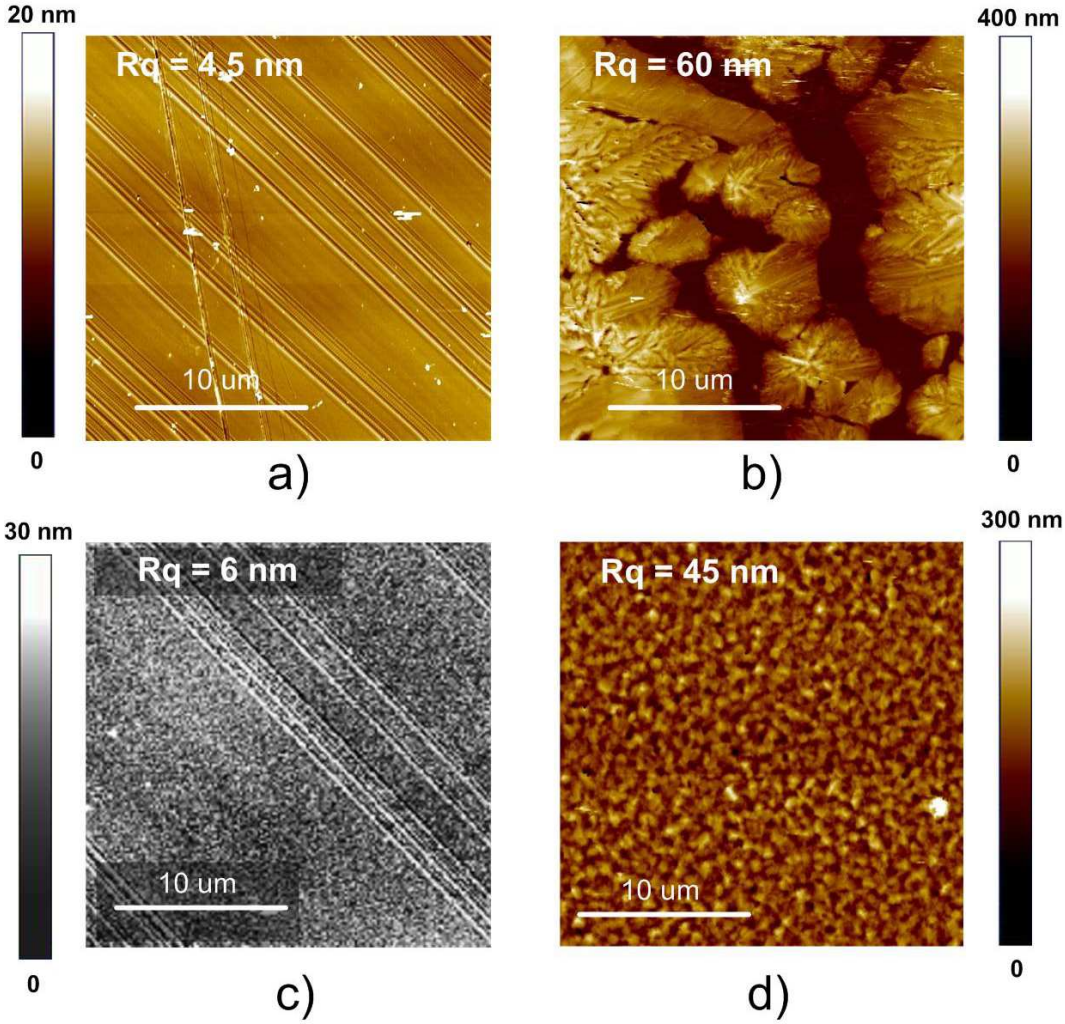


Figure 5.10: AFM Micrographs of the first Ge/SiC Heterojunction Layers with the following intended layer thicknesses and deposition temperatures: a) 100 nm, 300^{o}C b) 100 nm, 500^{o}C c) 1 μm, 300^{o}C and d) 1 μm, 500^{o}C. R_q is the surface roughness values.

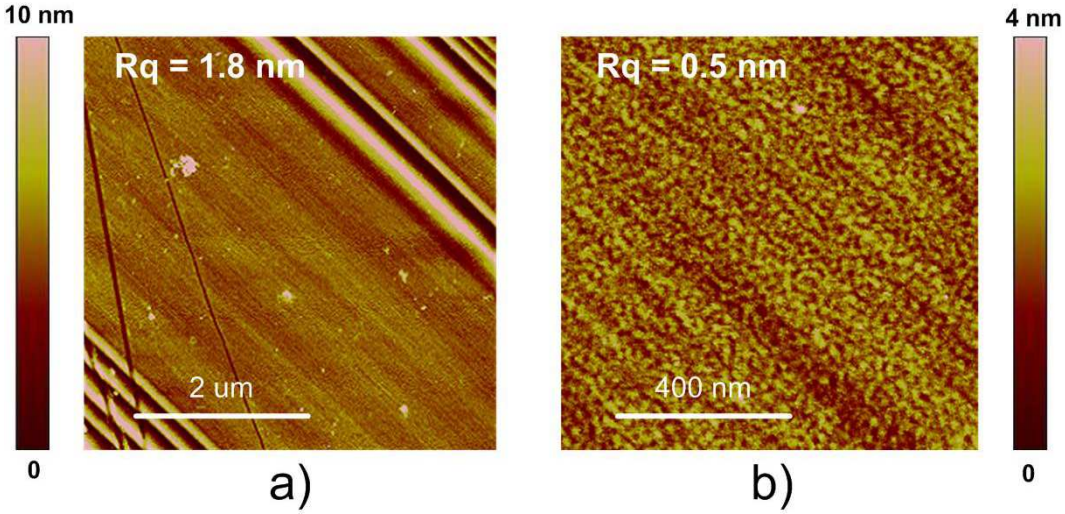


Figure 5.11: Higher resolution AFM Micrographs of the 100 nm, 300°C Ge/SiC layer with a) a 5x5 μm scan and b) a 1x1 μm scan.

marks that have come through from the SiC surface beneath. These features somewhat skew the surface roughness which was taken from the 25×25 μm AFM scan as 4.5 nm for the 100 nm Ge layer. To get a better idea of the roughness induced by the amorphous deposition, areas between the SiC defects were zoomed into, and new higher resolution 5×5 μm and 1×1 μm AFM scans were taken. These are shown in Figure 5.11, where avoiding the vertical scratches, the 5×5 μm scan revealed a roughness of 1.8 nm. In later analysis, the figure of 1.8 nm is used for this sample being the fairest comparative figure out of these, having no scratches but still considering the roughness from the SiC which is the same for all the samples. Zooming in with the AFM further and avoiding the polishing marks, the 1×1 μm scan reveals a very smooth surface with only tiny dimples that accounts for a roughness of just 0.5 nm. This suggests that given a smooth starting surface a very flat layer of Ge can be formed, something that could be achieved through SiC wafer polishing services such as NovaSiC [86].

XRD scans for all these layers are shown in Figure 5.12. The 100 nm, amorphous

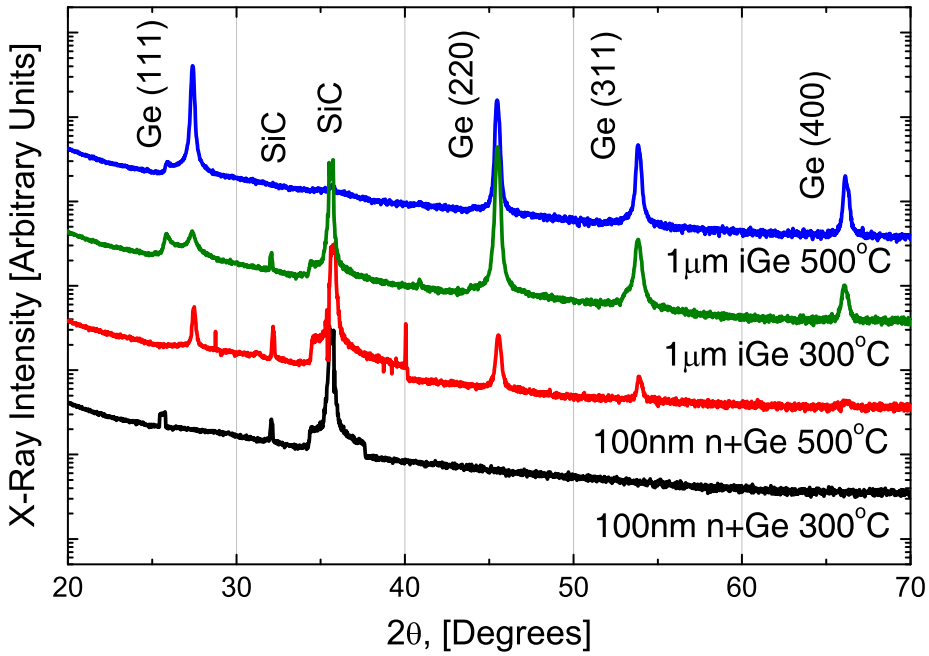


Figure 5.12: XRD θ-2θ scans of the first MBE Ge layers deposited on 4H-SiC.

layer shows no sign of any polycrystalline Ge, as expected given the AFM results. To test for amorphous Ge on the 200^{o}C, 100 nm layer, Energy Dispersive X-Ray (EDX) analysis was carried out. This technique is not reliant upon the material under scrutiny being crystalline for identification, unlike the XRD analysis. Figure 5.13 shows that distinct Ge peaks were found along with peaks of the dopant element, antimony. As part of the SiC, silicon is also highly visible; however carbon is outside the range of this particular scan.

Contrary to the 100 nm layer, the results of the XRD scan show that the 1 μm thick, low temperature layer contains significant crystalline material, particularly in the (220) and (311) orientations. This suggests that as the layer thickens, at 300^{o}C the adatoms have sufficient energy to form small polycrystals. The SiC peak can be seen to almost entirely disappear in the polycrystalline 1 μm layer due to the increasing thickness of Ge covering the substrate.

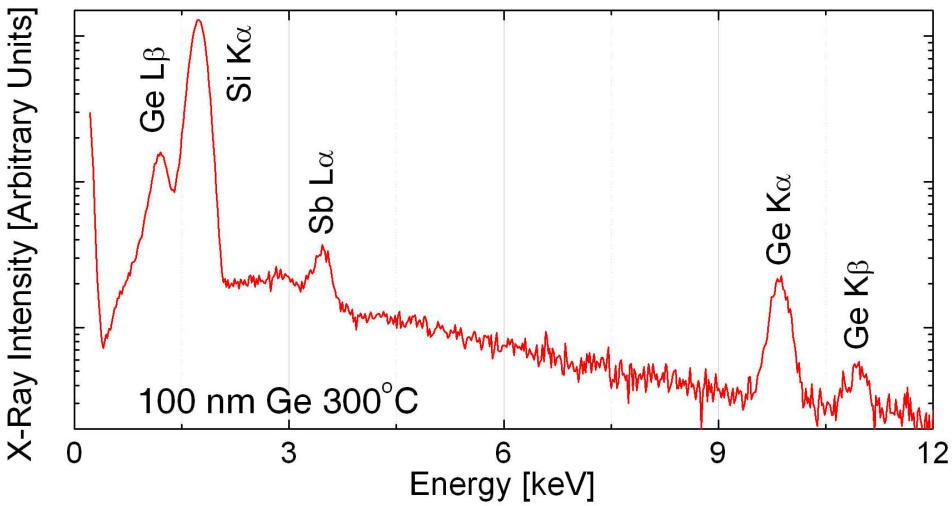


Figure 5.13: EDX scan of the 100 nm 300^{o}C Ge/SiC layer.

Considering now the polycrystalline layers, there is here a marked improvement from the Si results, Figure 5.10b showing the layer that was designed to be 100 nm thick. There is clearly a large amount of islanding with peaks as high as 300 nm. However, compared to the Si results these are very shallow and wide islands that show evidence of merging even at these reduced thicknesses. Confirmation that uniform high temperature deposition was possible came from the 1 μm thick polycrystalline layer of Figure 5.10d, which shows a consistent coverage of polycrystals. Of course this makes for a large roughness and 45 nm for this layer is particularly high. However, it proves that Ge can be deposited on SiC at high temperature and a further polishing stage could flatten this layer.

Having analysed this first generation of Ge/SiC layers, it was possible to refine the MBE process, tweaking the settings to form a more uniform set of structures. In the hope of improving on the crystalline islands of the 500^{o}C, 100 nm Ge/SiC, this deposition was repeated under exactly the same conditions but the deposition time was tripled, thus aiming for a 300 nm layer, structure b) in Figure 5.14. With the aim of comparing a new variable, the dopant type, a 500^{o}C, 300 nm layer was also formed with boron as the

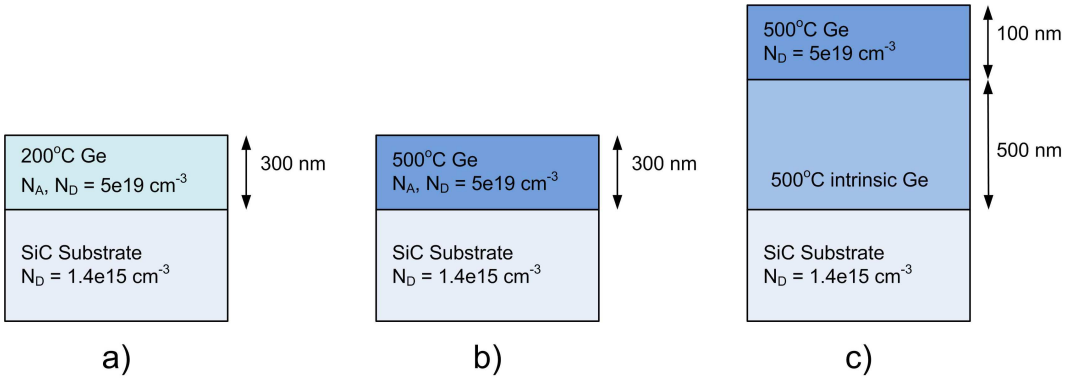


Figure 5.14: The intended structure of second generation of Ge/SiC heterojunction layers. Image a) represents the two amorphous 300 nm layers to be highly doped n-type and p-type, b) represents the two polycrystalline 300 nm layers to be highly doped n-type and p-type and c) shows the polycrystalline 200 nm *i*Ge layer.

dopant, making the layer heavily p-doped. To complete a 2×2 experimental matrix of dopant type and temperature, amorphous 300 nm layers of p-type and n-type were also formed. However, to prevent the chance of crystalline material appearing as occurred with the 1 μm thick layer, the temperature was dropped to 200^{o}C. Finally, in an attempt to reduce a serious series resistance problem with the 1 μm thick polycrystalline layer, which we will see in the next Chapter, this structure was repeated with only 500 nm of intrinsic buffer instead of 1 μm.

These were, in fact, the last Ge/SiC diodes to be made. Layers that were planned to further study the growth modes and the heterojunction interface were not completed as the unique Ge MBE deposition system at the University of Warwick was decommissioned due to various problems and its expensive running costs.

However, over the next sections the influence of first layer thickness, then dopant type will be assessed in the thin highly doped layers. Following this, the new intrinsic layer will be discussed briefly.

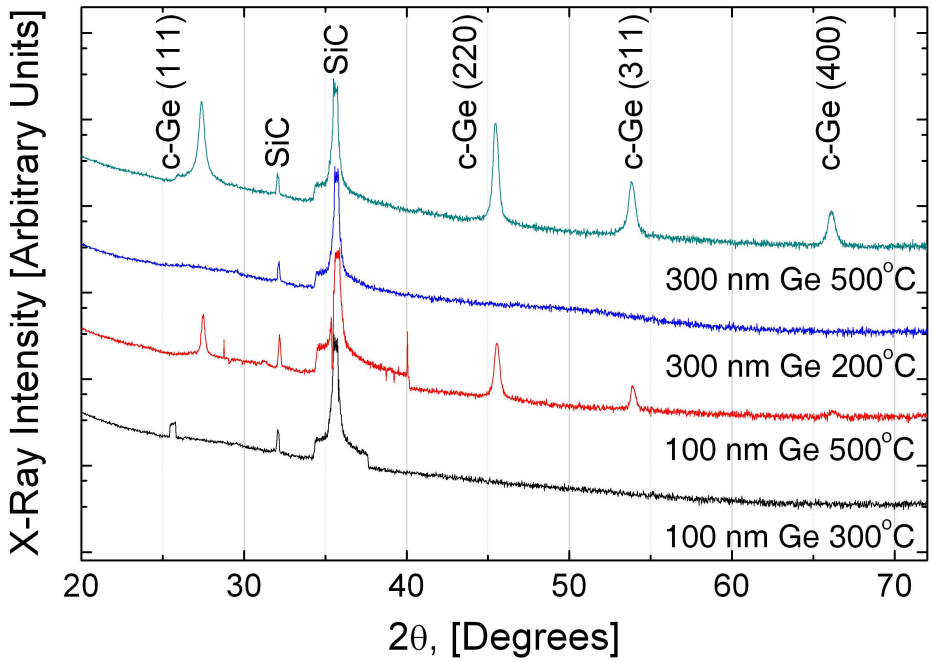


Figure 5.15: XRD θ-2θ scans comparing Ge layer thickness and deposition temperature.

5.5.1 Layer Thickness and Deposition Temperature

The 100 nm and 300 nm layers' crystallinity, and hence their conducting properties, was investigated using XRD analysis as shown in Figure 5.15, where 4H-SiC spikes are apparent for all the deposition conditions. Both samples deposited at 500^{o}C display the same four main Ge peaks, suggesting that Ge polycrystals of multiple orientations form. It appears logical that the thicker 300 nm layer displays larger, more defined peaks, due simply to the larger volume of material. The new amorphous 300 nm layer grown at 200^{o}C displays no Ge spikes, suggesting that there is no crystalline Ge in this layer.

Figure 5.16 shows the AFM images of the new 300 nm layers over a 25 $\times$ 25 μm area of each Ge layer. These images are typical of three scans taken on each wafer, whilst the roughness values quoted are average values. The 100 nm AFM results are repeated here for ease of comparison. As before, the amorphous layer of Figure 5.16c reveals only

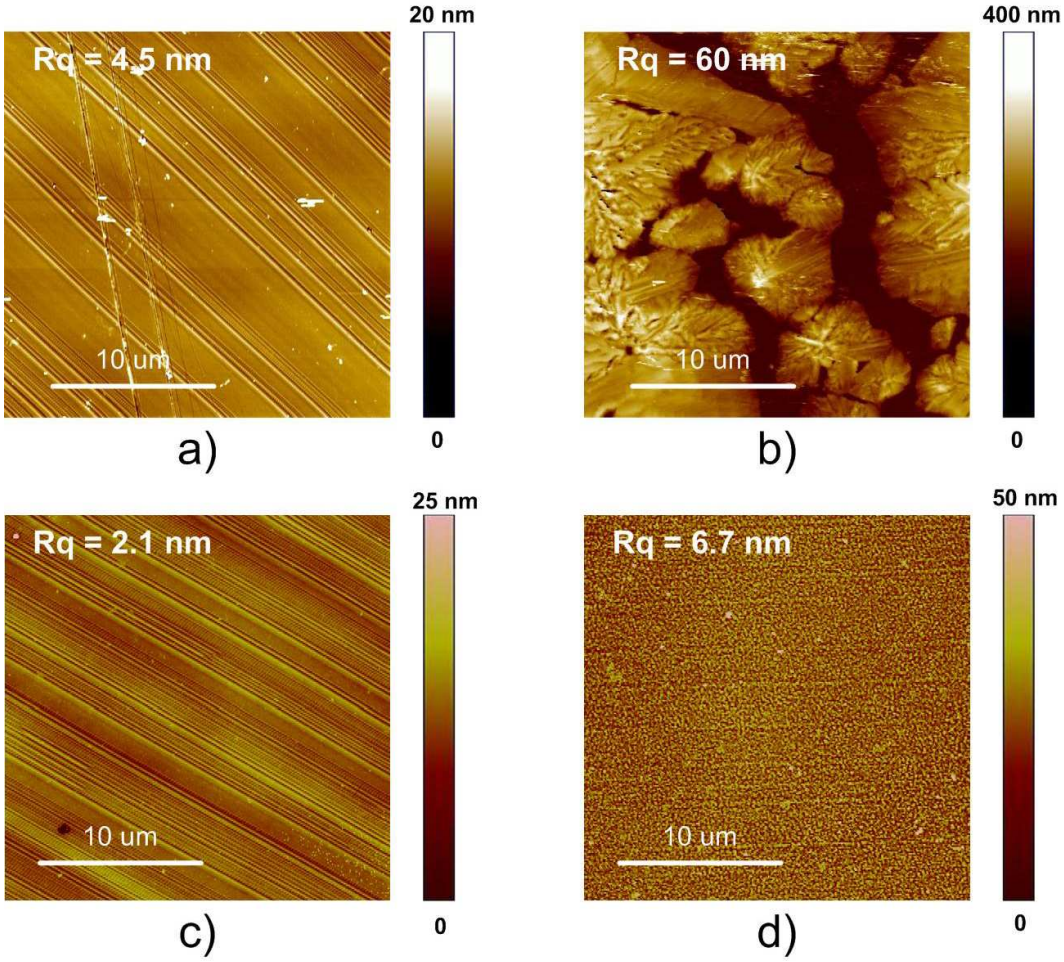


Figure 5.16: AFM Micrographs of the Ge/SiC Heterojunction Layers with the following layer thicknesses and deposition temperatures: a) 100 nm, 300^{o}C b) 100 nm, 500^{o}C c) 300 nm, 200^{o}C and d) 300 nm, 500^{o}C. R_q is the surface roughness values.

polishing marks from the SiC beneath. Its surface roughness of 2.1 ± 0.2 nm compares well with 1.8 nm roughness of the 5×5 μm 100 nm AFM result of Figure 5.11, which was the view free of scratch marks. However, there are no patches on the three AFM scans that could give a roughness as flat as the 0.5 nm roughness seen on the 1×1 μm scan of Figure 5.11, so the layer is becoming more disordered with thickness.

The AFM scan of Figure 5.16d suggests that the 300 nm polycrystalline layer is a vast improvement on the large islands that formed in the supposed 100 nm layer. With a surface roughness of 6.7 ± 0.1 nm it appears as if the large islands will have continued their S-K growth until the point at which they merged together.

The 300 nm layers were studied in greater detail using a helium ion microscope (HIM) and FIB/SEM analysis, the results of which can be seen in Figure 5.17. The HIM allowed for a greater appreciation of the deposition temperature contrast at a very high resolution, with Figure 5.17a and 5.17b showing the surface features of the low and high temperature layers respectively, at 500 nm and 1 μm fields of view. As with the AFM micrographs, the contrast between the surface roughnesses is visible, though at this magnification the difference in individual crystal size also becomes apparent. The amorphous layer shows some order with approximately 20 nm 'dimples' occurring on the surface, perhaps suggesting very small poly-crystals. Much clearer are the larger poly-crystals of the higher temperature deposition, with crystal grains appearing on the surface up to 200 nm in size.

The cross-sectional images of Figure 5.17c and 5.17d taken from the SEM within a FIB system show the three individual layers of both 300 nm layers. From the bottom up, SiC, then Ge, Ni and a protective carbon cap are clearly defined. In both cases, a double layer of Ni is evident due to the deposition of two 300 nm layers. Once again, a slightly rougher Ge surface is evident on the higher temperature deposition.

To summarise this Section, a trade off is evident in the choice of deposition temper-

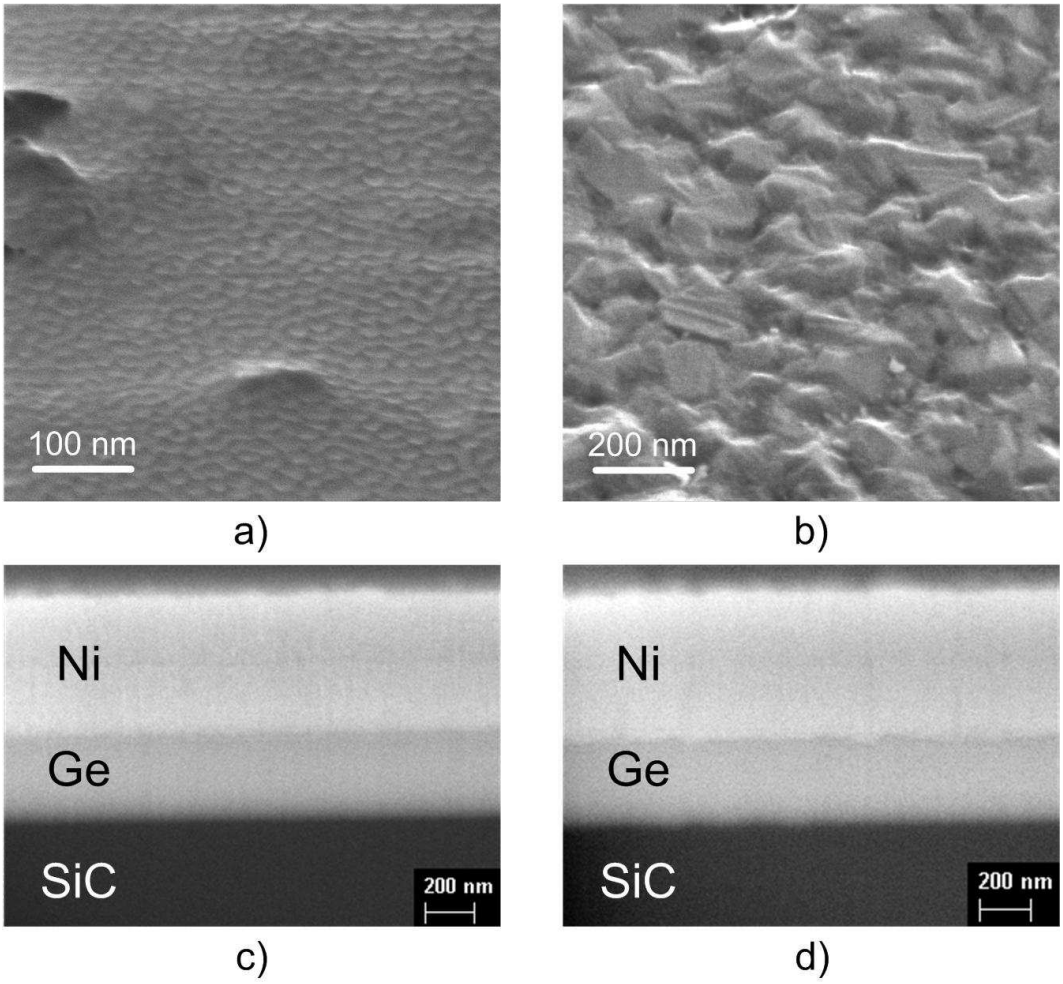


Figure 5.17: HIM (a and b) and FIB/SEM (c and d) images of the 300 nm Ge/SiC Heterojunction Layers grown at 200^{o}C (a and c) and 500^{o}C (b and d). The samples are tilted 54^o away from the detector, hence the vertical axis is not to scale.

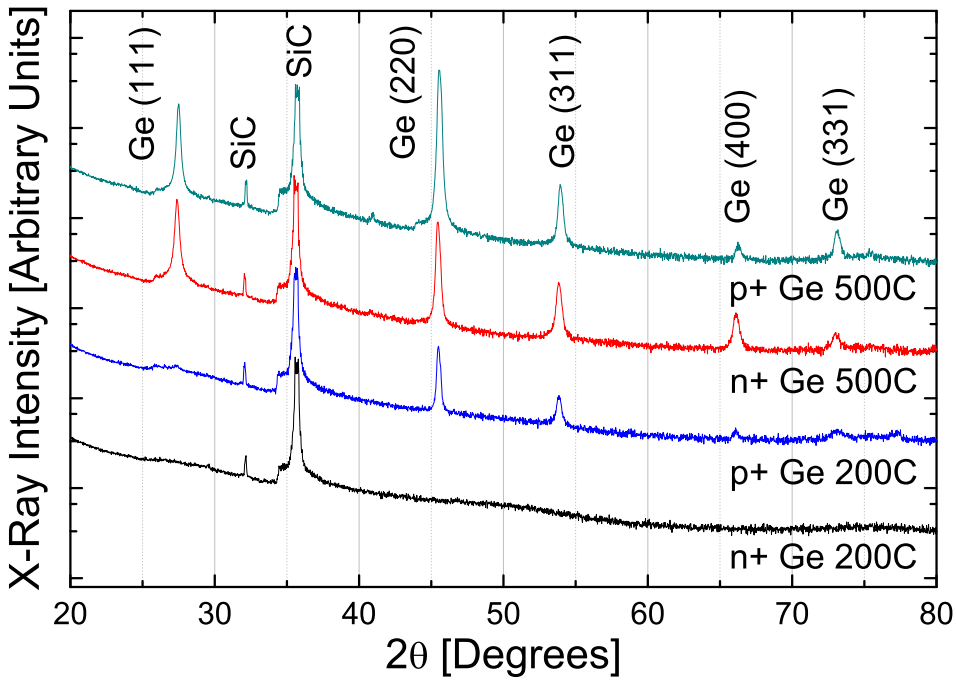


Figure 5.18: XRD θ-2θ scans of the MBE Ge layers deposited on 4H-SiC with different dopants and deposition temperatures.

ature. It is expected that the polycrystalline layers will form the best electrical contacts having the least grain boundaries within the layer. The amorphous layers have the advantage of producing a flat surface; however, this advantage could be negated if the polycrystalline layers were polished to improve the finish.

5.5.2 The Role of the Dopant

It is not immediately obvious how the selection of a dopant may impact on the physical properties of the layer. However, XRD and AFM results will here show that there is in fact a physical difference between the 300 nm layers that were doped p-type with boron (B) and those doped n-type with Antimony (Sb). High and low temperatures are again compared with the n-type layers being the 300 nm layers used in the last Section.

Figure 5.18 shows the XRD results of the p-type layers compared with the n-type layers. SiC is evident in all the samples; however, the cubic Ge content is sample specific. As witnessed previously, the layers deposited at high temperature are poly-crystalline, whilst those at low temperature are much smoother. The AFM results, which may be seen in Figure 5.19, follow the previous trends with rough high temperature surfaces and smooth low temperature surfaces. The 200^oC p-type layer seen in Figure 5.19b has a surface roughness of 3.5 ± 0.2 nm, whilst the 500^oC p-type layer of Figure 5.19d is up at 30 ± 2 nm.

Comparing across dopant lines, the p-type layers have in general, X-ray intensities greater than their n-type counterparts, suggesting greater crystallinity. This is evident in the (220) direction especially. The low temperature depositions show some contrast, with the p-type layers displaying evidence of crystallinity in the (220) and (311) orientations, the same as the 1μm iGe layers of Figure 5.12. This comes despite the lowering of the deposition temperature from 300^oC to 200^oC. Furthermore, the p-type layers have rougher surfaces, whilst the individual grains are noticeably larger in the high temperature p-layer than in its corresponding n-layer.

With all other conditions being equal, these differences are most likely due to the difference in the dopants. Given the physical nature of this analysis, the difference cannot simply be attributed to the choice of a p-type or n-type dopant, but instead to the properties of the doping element. The p-dopant B, is a light and small atom compared to Ge and the n-dopant Sb, is heavy and large in comparison. With high doping levels ($N_{D,Ge} = N_{A,Ge} = 5 \times 10^{19} cm^{-3}$), there is approximately 1 dopant atom for every 1000 Ge atoms, so the atom size will have an impact on the crystal structure. The smaller B atoms are likely to be incorporated into the Ge lattice with some ease whereas the larger Sb atoms will not perfectly fit the lattice and will displace a number of Ge atoms.

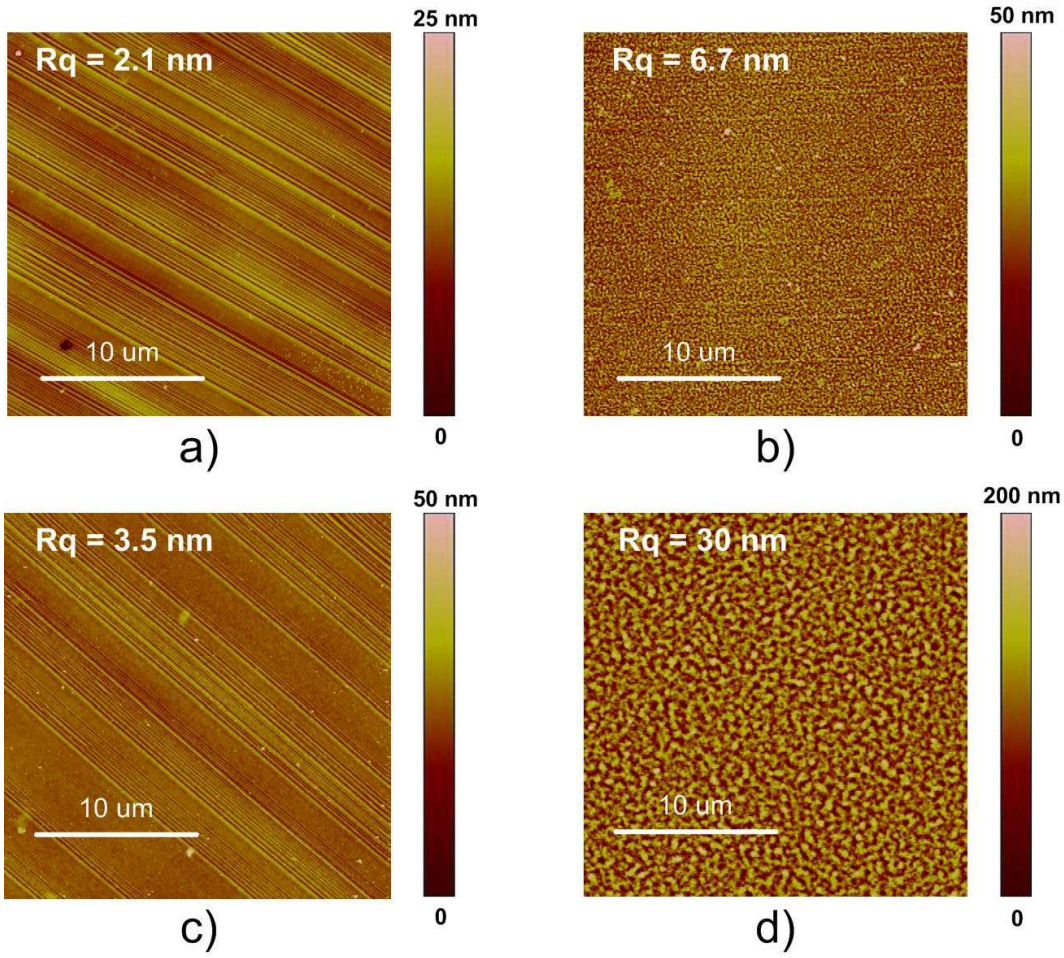


Figure 5.19: AFM Micrographs comparing Ge dopant type. The 300 nm Ge/SiC Heterojunction Layers have the following layer dopant types and deposition temperatures: a) n-type, 200^{o}C b) n-type, 500^{o}C c) p-type, 200^{o}C and d) p-type, 500^{o}C

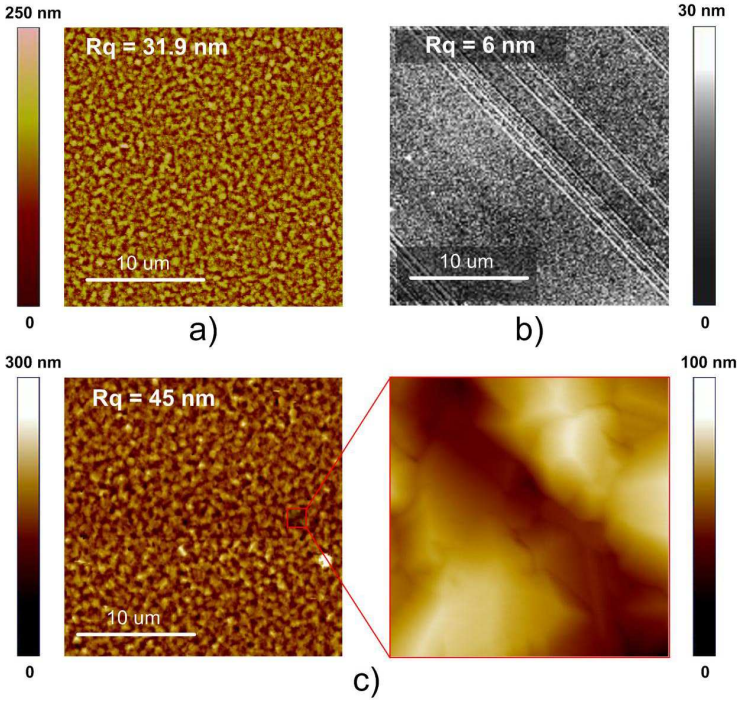


Figure 5.20: AFM Micrographs of the *i*Ge/SiC Heterojunction Layers with the following layer thicknesses and deposition temperatures: a) 500 nm, 500^{o}C b) 1 μm, 300^{o}C and c) 1 μm, 500^{o}C.

This will affect the growth of the layer, with extra strain in the lattice likely to lead to a greater number of defects and hence smaller polycrystals. Secondary to this, the difference in mass between the atoms could also be pertinent. The light Ge/B atoms may have more energy than the heavy Ge/Sb atoms to find a site that minimises its dangling bonds on the SiC surface, creating larger polycrystals.

5.5.3 Intrinsic Ge Layers

Considering again the layers with an intrinsic drift layer, the second generation of layers grown included a new layer deposited at 500^{o}C that used a 500 nm intrinsic region, halved from the original 1 μm in a hope to reduce series resistance. This provided an opportunity

to examine a high temperature layer grown to another intermediate thickness. The AFM results from all the intrinsic layers are presented in Figure 5.20. The surface roughness of the high temperature layers appears to increase quite consistently with layer thickness, the new 500 nm layer having a roughness of 31.9±0.3 nm, two thirds that of the 1 μm layer. Similarly, the size of the polycrystals also appear to increase with thickness, most likely due to the releasing of the strain that the SiC lattice induces. In Figure 5.20c, the AFM is used to concentrate on the polycrystals from a 1×1 μm area on the high temperature 1 μm *i*Ge layer. One can see the polycrystals, which reach half a micron in diameter, with valleys up to 150 nm deep between the crystal peaks. The low temperature layer is relatively smooth, though its roughness at a thickness of 1 μm is three times what it was at 300 nm.

5.5.4 Ge Layer Growth Summary

Over the two generations of diodes, a total of nine different Ge layers were deposited on SiC, at varying deposition temperature, dopant type and thickness. A summary of the results is presented in Figure 5.21, where deposition temperature and layer thickness is compared in turn to the resulting surface roughnesses. Over the last Sections it has been evident that surface roughness is proportional to the degree of crystallinity extracted from XRD scans, hence it is fair to say that the results of Figure 5.21 would look little different if surface roughness were replaced by relative XRD X-ray intensity.

Despite being a small sample set, patterns are evident that may well be illustrative of the larger picture. The Temperature-Roughness plot gives the clearest evidence of the trade-off between crystallinity and roughness, with every pair of diodes with like dopant types and layer thickness, showing the improvement in roughness at lower temperature.

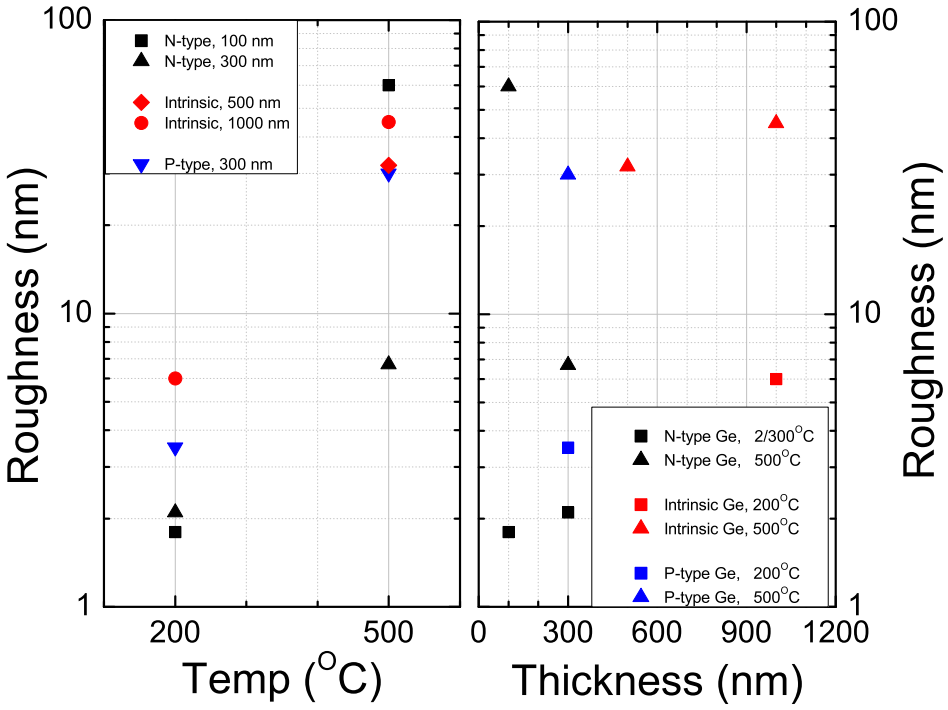


Figure 5.21: An overview of the different Ge layers, comparing surface roughness to temperature (left) and thickness (right).

The Thickness-Roughness plot shows a reasonably linear proportional relationship between the two in the amorphous results. Less clear, but implied from the Thickness-Roughness plot is the idea that, for the high temperature layers, there is an optimal thickness at which roughness is at a minimum, potentially around 300 nm. This idea may be described qualitatively. Large, shallow islands were formed at 100 nm, as seen in Figure 5.16b. At 300 nm in thickness the gaps between these islands have filled in leaving a fairly smooth layer in the case of the n-type layer of Figure 5.16d. Increasing the thickness further, reduces the impact of the strain induced from the SiC surface and, as seen in the intrinsic results, the layers becoming rougher and the polycrystals grow in size. Across both graphs in Figure 5.21it appears that the p-type layers are rougher than their n-type contemporaries. As described in Section 5.5.1, this is likely due to the size and mass of the dopants.

This is not an exhaustive data set unfortunately due to problems with the MBE equipment midway through the proposed set of layers. Had this not occurred, the ideas proposed above may have had more concrete evidence backing it up. However, for now, the layers that are missing must now go down as future work.

5.5.5 The Ge/SiC Interface

Perhaps some of the most revealing physical results come from the TEM analysis of a HfO_2/Ge/SiC sample that was being used for the MOS experimentations of Section 8.5.1. The Ge layer involved was a 300 nm, intrinsic Ge layer similar to the highly doped layer analysed in Sections 5.5 and 5.5.1. Figure 5.22 shows the various TEM images, zooming in from image 5.22a, a cross section that reveals all the layers, to image 5.22c, which reveals the individual monolayers of Ge at the interface.

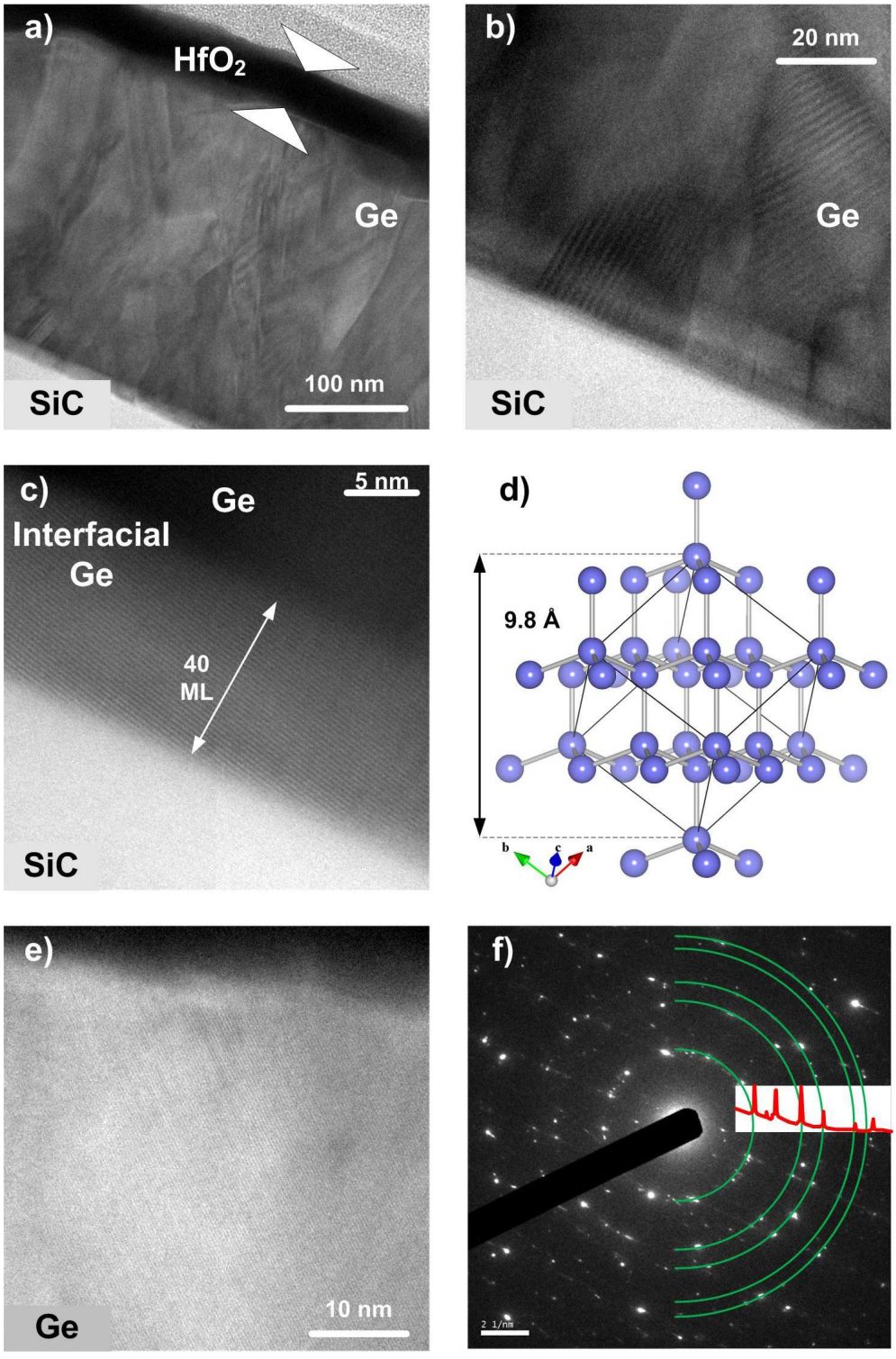


Figure 5.22: TEM images of the 300 nm Ge/SiC heterojunction layers with a HfO_2 oxide layer

Image 5.22a shows very clearly the individual layers and the polycrystalline patterns within the Ge layer, with the difference in contrast between the layers resulting from the ability of the electrons to pass through them. The most detail appears in the Ge layer, where defects between the polycrystals appear as diagonal lines. Zooming in on the interface in image 5.22b, the boundary of multiple polycrystals may be seen in much greater detail. Each individual polycrystal may be identified by the differing contrasts or by the angle of the lattice features. Zooming in further, image 5.22c shows the interface between the SiC and a single large Ge crystal which is greater than 50 nm wide. At this magnification (800,000x), the individual monolayers of Ge can be seen thanks to the huge resolution of the TEM. These monolayers are clearest within the first 10 nm of the interface, where approximately 40 monolayers were counted. Closer inspection reveals the distance between monolayer edges is approximately 3.1 angstroms. This corresponds with the spacing of monolayers within the (111) plane of a Ge unit cell, as shown in image 5.22d, which was formed using the crystallography freeware program VESTA (standing for Visualization for Electrical and STructural Analysis, this tool is downloadable from [87]). The two atoms highlighted, at opposing corners of the unit cell, are exactly three monolayers apart and perpendicular to the (111) plane. Measuring their separation in VESTA, they are 9.8 angstroms apart, leading to a monolayer separation of 3.27 angstroms. This implies that in image 5.22c, (111) Ge is forming on the SiC surface. One peculiarity here though is that the Ge is angled some 12 degrees from the interface, which means that the Ge layer is not aligning perfectly with the (0001) SiC plane, as that is only 4 degrees off axis. This is however a hugely positive result as it shows that the Ge is forming on the SiC surface in a distinctly layer by layer, monocrystalline fashion.

Beyond the first 10 nm of Ge in image 5.22c, the monolayers can be seen to continue, though they eventually fade into the darker contrast. The reason for this may be down

to the formation of other polytypes at this thickness, which in turn could be due to the release of strain within the Ge layer at this thickness (more of which in Section 5.5.5.1), by the formation of dislocations. As we progress further into the Ge bulk, big polycrystals continue to form and image 5.22e shows one near the HfO_2 interface. It is a single individual Ge polycrystal that appears to have a diameter of about 50 nm. Monolayers again appear at an angle of about 60° from the surface. Image 5.22f shows a diffraction pattern image taken from the bulk of the Ge layer using the built in reflection high-energy electron diffraction (RHEED) apparatus within the TEM. The regular concentric circles imply that the sample is indeed polycrystalline. The spacing of the circles agree exactly with the Ge peaks of the sample's XRD response in Figure 5.15, confirming that crystals of (111), (220), (311), (440) and (331) orientation are all located within this sample.

5.5.5.1 The possibility of strained Ge

The discovery that Ge forms in a uniform, potentially layer by layer fashion on SiC, leaves one very obvious question; why? In Section 5.4, AFM evidence suggested that Si forms on SiC in the Volmer-Webber mode, forming distinct islands that do not merge even at 2-3 microns of deposition. So why is it that Ge can produce such uniform layers? Is it possible that there is a lattice match?

Figure 5.22c shows that (111) Ge is growing on SiC and hence VESTA is used to compare the hexagonal faces of (0001) 4H-SiC, and (111) Ge. The individual (0001) Si face of SiC can never align atom for atom with the (111) Ge face due to different lattice constants; however, there is a single geometry that aligns approximately 1 in 7 Ge atoms with 1 in 12 of the SiC's Si atoms. This alignment can be seen in Figure 5.23, where the lattice parameters involved are 1.0644 nm in the SiC and 1.0585 nm in Ge.

If this alignment was indeed possible, the 0.5% mismatch between the layers would

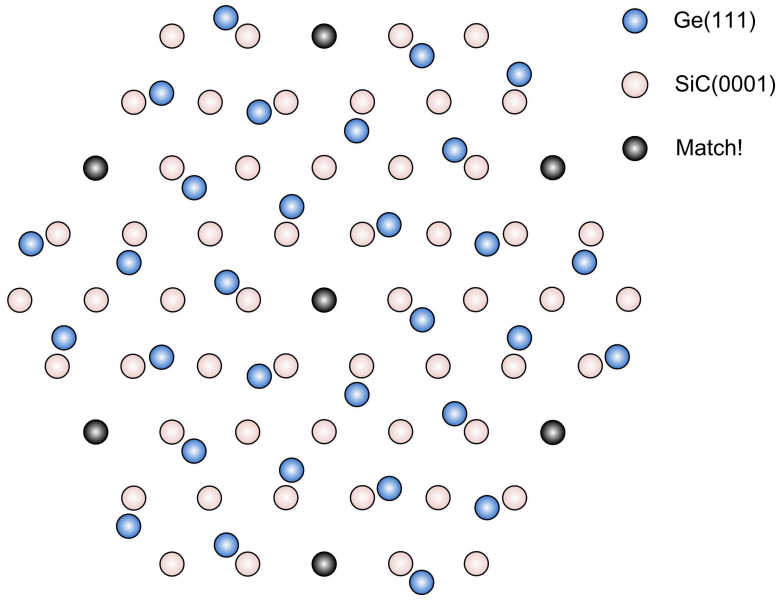


Figure 5.23: A potential lattice match between the (0001) Si face of SiC and the (111) plane of Ge.

place the Ge under tensile strain; the individual Ge atoms being forced further apart than they ordinarily would be. Similar to strained Si, this "strained Ge" may well have a mobility greater than bulk Ge due to the increased lattice spacing, which results in less scattering events for a given carrier. This opens the door to a potential new device, a lateral high-mobility Ge MOSFET that is developed on a SiC heat sink.

5.5.6 Si Wafer Bonded Results

Finally in this Chapter, the physical results of the Si/SiC wafer bonding technique will be introduced paving the way for the MOS analysis carried out on these structures in Chapter 8.

The wafer bonded structures that were described in Section 5.3.5 were analysed physically using AFM and XRD. First though, Figure 5.24 shows the results of the bonding

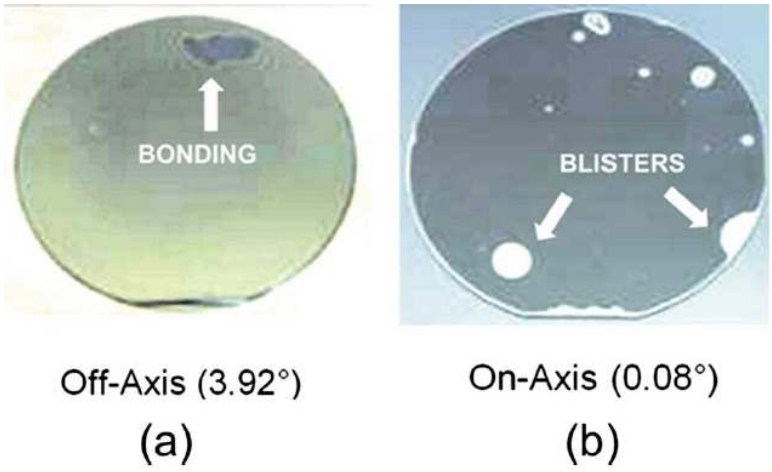


Figure 5.24: The areas of wafer bonding achieved, comparing off- and on-axis SiC substrates.

process, where image a) shows the off axis wafer and b) shows the more successful on-axis wafer. The dark regions on each wafer represent the bonded areas of which there is very little on the off-axis wafer. This can be explained by AFM measurements which were conducted on both SiC wafers prior to the bonding process. The RMS roughness of the off-axis material was 1.5 nm, most likely due to the 4^o-off step bunch. The on-axis 4H-SiC material yielded a low RMS value of 0.6 nm, which approaches the limit for SiC wafer bonding - it is assumed that SiC requires a RMS roughness of ~ 0.5 nm or less for successful room-temperature bonding. The Si/SiC bonding coverage is much better on on-axis material because of its low surface roughness value, and in the case of an off-axis wafer, only a few atoms are indeed contacting the Si layer. Improved polishing techniques and the optimisation of the cleaning procedure may improve the yield of both wafer types.

Discarding the off-axis wafer due to its lack of cohesion, Figure 5.25 shows the AFM scans taken from an on-axis WB sample. The first image is one of a defect free area, where the surface is not smooth, undulating fairly consistently to a level 20 nm above or below the normal. This leads to an RMS roughness of 5.8 nm for the non-blistered regions.

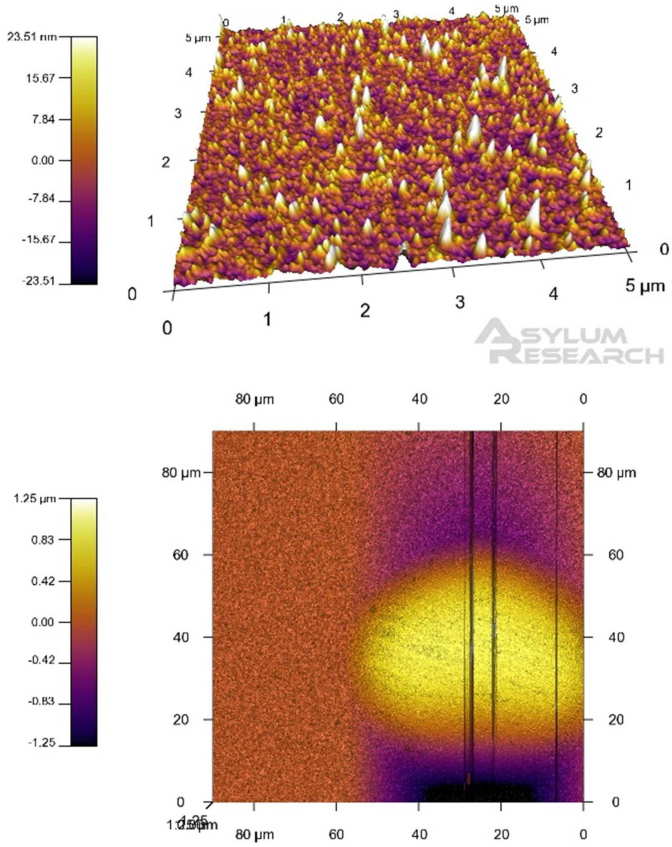


Figure 5.25: AFM images of two WB Si/SiC regions; left, a detailed picture of a defect free area and right a more macroscopic, birds eye view of a single blister.

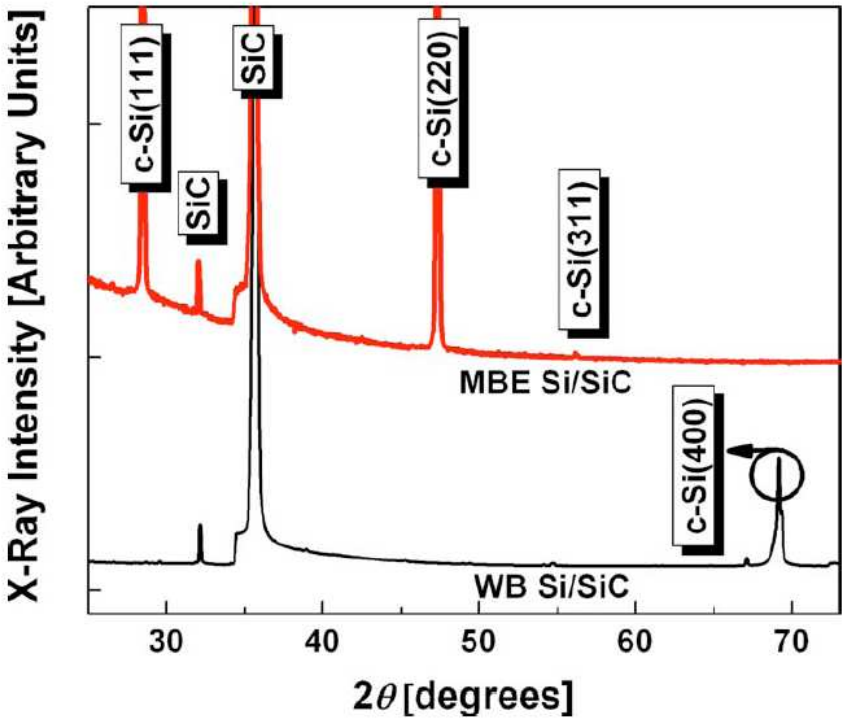


Figure 5.26: A comparison of the XRD scans taken from the two different Si/SiC wafers. Above is the MBE layer and below, the wafer bonded layer.

Another polishing stage post-bonding could reduce this value. The second image clearly show a very large blister some 50 μm in diameter. The blister itself rises approximately 1 μm above the surface, creating a valley of a similar depth next to it.

XRD scans of the WB Si layer are presented in Figure 5.26 in comparison to the intrinsic MBE layer that was designed to have a 1 μm thick layer, which was presented initially in Figure 5.8. Reassuringly, only one Si peak was present over the entire layer, evidence that the Si wafer maintained its crystallinity during the WB process.

5.6 Summary

The formation of narrow bandgap - wide bandgap heterostructures was attempted, with Ge and Si both being deposited via MBE onto the surface of a 4^o off axis, lightly n-type doped 4H-SiC epitaxial layer. The impact of these physical results will be felt in the preceding electrical analyses, the layers that appear most crystalline offering the lowest resistance, whilst those with the flattest surface finish being most suited to MOS channel production.

Beginning as just a comparison between the narrow bandgap semiconductors, the MBE Ge deposition proved rather successful, mitigating the problems of the seemingly incoherent lattice parameters much better than the Si/SiC layers. At the intended deposition width of 100 nm, both semiconductors formed large island structures when the material was deposited at high temperature. However, the Ge islands were very shallow, reaching heights no greater than 400 nm and covering nearly the entire SiC surface as they had begun to merge. The Si islands by comparison were tall tower blocks reaching 1 μm thick and covering very little area. At thicker layers the trend continued; the Ge layer merged completely forming a uniform layer, which at best had a 6 nm roughness at a thickness of 300 nm. This value could be improved even further through the use of a pre- and post-deposition polishes. The Si islands on the other hand did not merge, and even at a intended thickness of 1 μm, large gaps remained between the ugly sprawling blobs of crystalline material. With little hope remaining for poly-Si uniformity, the focus shifted entirely to Ge MBE layers.

Progressively increasing the thickness of the polycrystalline Ge layer to 500 nm and 1 μm allowed the relaxed (non-strained) polycrystals to grow larger with thickness, creating bigger polycrystals and very rough layers with valleys between the crystals. Lowering

the deposition temperature bore layers that were almost entirely uniform, but at the cost of crystallinity, the layers being entirely amorphous. At best, a roughness of 0.5 nm was achieved by measuring between the polishing marks that had emanated through from the SiC surface. Changing the dopant in the layers also seemed to affect the physical morphology, with larger, heavier n-dopant atoms causing greater stress in the individual polycrystals. This in turn, caused defects to occur at a smaller polycrystal size, and hence a flatter layer was produced by more polycrystals.

Wafer bonding provided an alternative method for forming a heterojunction and 600 nm of a Si wafer was bonded to a SiC wafer. Vastly more successful from a physical standpoint than Si MBE, the resulting Si layer appears flat, with an RMS roughness of 5.8 nm in all the non-blistered regions.

5.7 Conclusions

1. For a given set of conditions, a more homogeneous, crystalline and flat layer will be produced via the deposition of Ge, rather than Si onto 4^o off-axis 4H-SiC.

2. The best layers formed from MBE deposition are achieved at high temperature, using physically small dopants. Roughness increases with thickness; however, it is possible to achieve the smoothest layers by depositing layers too thick and polishing them back to the desired thickness.

3. It is likely that a high temperature post deposition anneal would improve interface homogeneity and layer crystallinity; perhaps increasing the volume of deposited material that forms into a single preferential crystal orientation.

4. Wafer bonding of Si or Ge to on-axis 4H-SiC leads to fully crystalline layers, that

are reasonably smooth without polishing. However, this comes at the expense of a highly resistive, inhomogeneous interface, a cost that appears prohibitive.

Chapter 6

Characterisation of Silicon Carbide Heterojunction Diodes

6.1 Introduction

In the last chapter, heterojunction layers were produced for diode and MOS devices, with layers of minimal grain boundaries and surface roughness. In this chapter, the rectifying properties of the layers are tested using the electrical analysis tools of Section 4.3 to investigate the heterojunction interface. Ohmic contacts with low contact resistivity are formed on the Ge front and SiC back, meaning that as current flows through the device, the rectifying heterojunction interface will be the only barrier that the carriers have to overcome. Furthermore, being unipolar rectifiers, the devices may be characterised as a regular Schottky Barrier Diode, and I-V analysis shows that the diodes produced have very low ideality factors and remarkably consistent barrier heights. Series resistance is very variable however, and those layers that were shown to form in the last Chapter with a minimum of grain boundaries, produce the layers of least resistance.

This Chapter naturally splits into two Sections. In the first, the procedures used to form heterojunction diodes, will be introduced. Following this, the results of the diode

characterisation will be discussed in the second Section.

6.2 Heterojunction Diode Production Procedure

The transformation of two layers of semiconductor into a heterojunction diode is a reasonably simple processing problem, requiring only a single photolithography step and the use of a small number of clean room machines. The basic process is shown in Figure 6.1, whilst a SolidWorks representation of the final structures is shown in Figure 6.2. Firstly, Ni front contacts are patterned forming the dots and circular transmission line measurement (CTLM) structures that will be used to test the device. Using the Ni features as a mask, each device is then isolated by etching the Ge from between the metal contacts. As seen in Figure 6.2, half of the chip is protected from this final step to maintain the functionality of the CTLM structures. Having processed the front, a simple back contact may be formed.

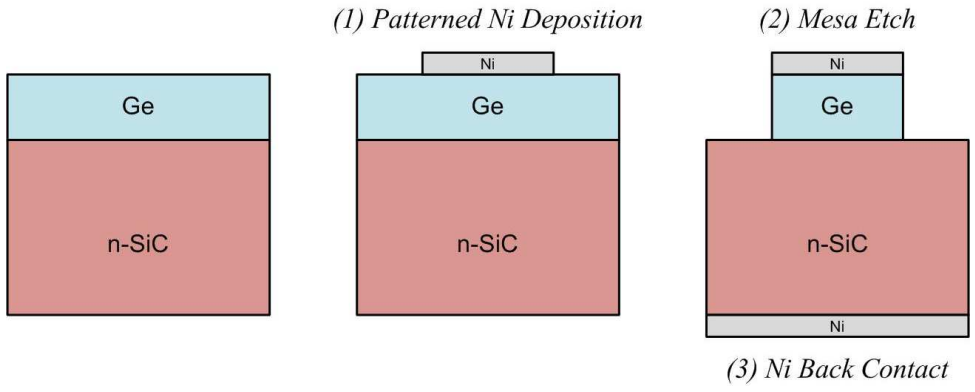


Figure 6.1: The basic process for forming the semiconductor layers into heterojunction diodes, involving the fabrication of the metal front contacts, the etch that forms the mesa isolation and the forming of the back contact.

The dots and CTLM structures formed on the top of these devices can be achieved

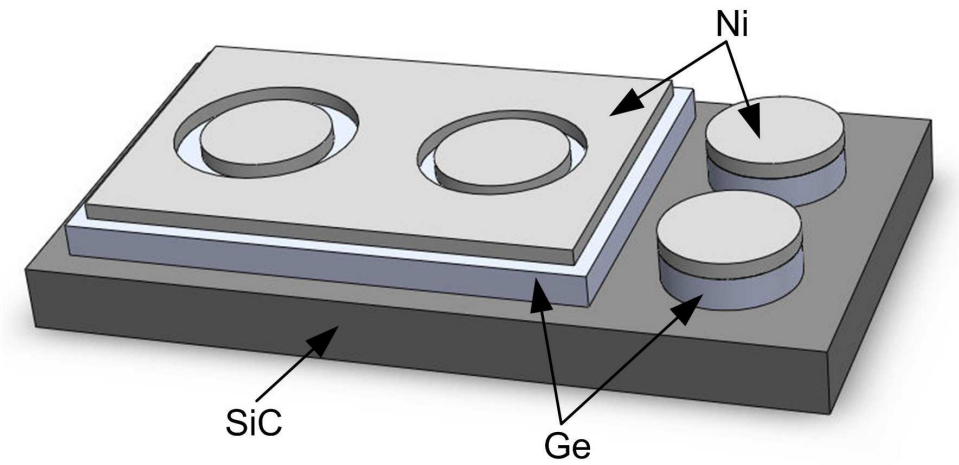


Figure 6.2: The layout of the Ni/Ge/SiC mesa diodes and CTLM Structures (not to scale).

via one of two processes, the lift-off technique or the metal-etch. Figure 6.3 outlines both of these methods. The lift-off technique involves coating the sample with photoresist in all the places to be protected prior to metal deposition using a positive photolithographic mask. After a layer of the metal has been sputtered onto the entire sample, a dip in acetone causes all the photoresist and unwanted metal to "lift-off".

In the metal-etch process, the whole sample is covered in the required metal. A negative photolithographic mask then allows the deposition of photoresist covering all the wanted metal. A wet etch such is then used to remove the unwanted metal. In the case of nickel, which is used on all the Ge/SiC samples, aqua regia (HNO_3:HCl, 1:5) is used as the etchant.

Further details of both techniques may be found in [88]. Both featured in prototype runs, carried out to form Ni contacts on stock Si wafers; this allowed the fabrication process to be refined. The wet etch required in the metal-etch process was a particularly difficult process, requiring the immersion of Ni samples in the vicious aqua regia etch for just the right amount of time, typically 5 seconds. The results were variable, sometimes

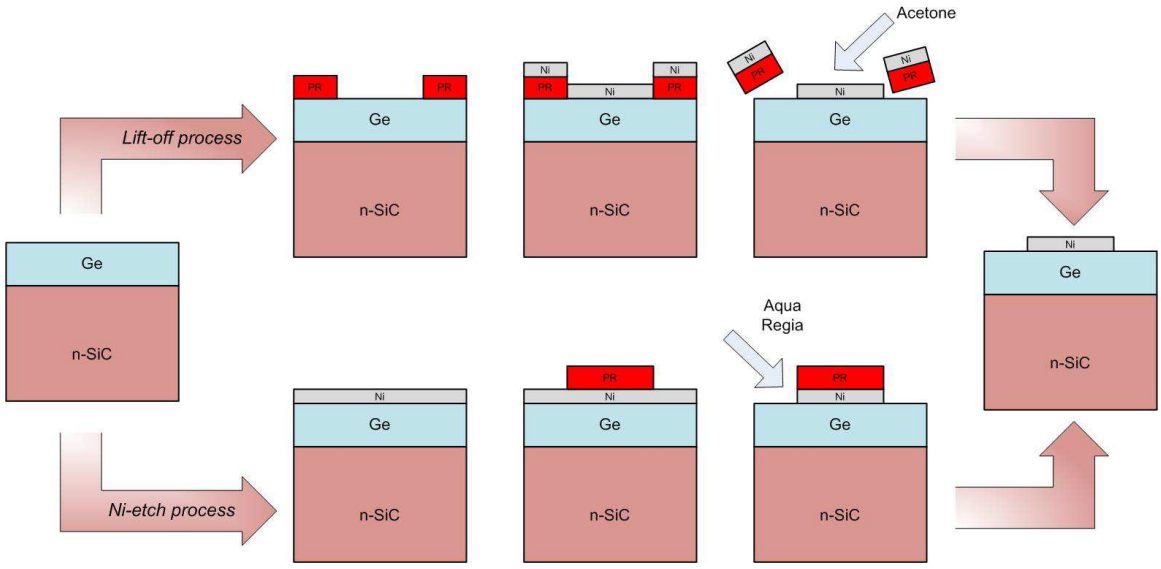


Figure 6.3: The lift off (above) and metal etch (below) processes used to form patterned metal on a semiconductor.

etching too much other times not enough, and the etch also attacks the semiconductor surface, leaving it unusable if you did need to continue to process it. However, given many practice iterations, the process can be refined resulting in very well defined metal contacts. Furthermore, this processing step was followed by an etch to remove all the semiconductor between the metal contacts, so this problem was negated.

Preferably, one would always use the lift-off technique, as it does not require the etch, and the semiconductor surface is well protected. However, practically, the metal definition just did not compare, with features often appearing jagged around the edges where the photoresist had ripped the metal off the surface. As such, the metal etch technique was used for all these devices. The difficulty with this technique is controlling the very fast acting etch, that will seriously undercut the photoresist mask if left a few seconds too long. Hence, with improved facilities, work and a lot of process refining, the lift-off technique would be worth mastering as it is a much more repeatable and consistent process.

The detailed processes that were used in the metal etch process are laid out below.

6.2.1 Thin Film Surface Clean

Prior to depositing the metal, the surfaces must be cleaned as the earlier physical characterisation was not performed under clean room conditions and hence foreign particles will have accrued on the surface. When cleaning the heterojunction layers, the type of clean used depends on the materials in question. Having been designed specially for silicon, the RCA1/RCA2/Piranha cleans described in Section 5.3.3 are appropriate for any Si/SiC devices. However, the common factor between all these cleans is hydrogen peroxide, an acid that etches Ge very quickly. At the concentrations it is used in the common cleans, 100 nm of Ge will be stripped in under 40 seconds.

There are a few papers which suggest alternative cleans. Used in the processing of all the 300 nm Ge layers, a 1996 paper [89] suggested an aqueous ammonia (28% NH_4OH:DI, Water 1:4) treatment at room temperature for 30 seconds to remove residual metals, followed by a diluted sulphuric acid dip (H_2SO_4:DI Water, 1:7) for 2 minutes to remove hydrocarbon-related contamination. A more comprehensive paper was published in 2008 by IMEC [90]. This work lists the Ge etching rates of some 50 chemical recipes, concluding that the most appropriate clean is a 0.5% concentration of hydrofluoric acid in DI water for 5 minutes at room temperature. This removed all the metals tested in their work, doing so at a suitably slow etch rate.

In this work, the clean in aqueous ammonia followed by diluted sulphuric acid dip was used.

6.2.2 Metal Deposition

The deposition of metals is carried out in the University of Warwick clean room using a PC controlled CVC deposition tool, or 'sputterer'. This can process 4" wafers or the smaller samples considered here, utilising 4 inch targets of aluminium, nickel and titanium. The sputtering process employs a plasma under a high vacuum, with the sample surface facing the metal target. With a bias applied to the target, the ions within the plasma bombard the metal surface dislodging individual atoms. These metallic atoms then coat the surface of the sample, forming the amorphous metal layer.

Nickel was the chosen metal for the heterojunction diodes due to its large work function of 5.15 eV, which forms a SBH sufficiently large to SiC that the largest blocking voltages and minimum leakage voltages are achieved [91–94]. Whilst the Ni/Ge contact should be ohmic due to the large amount of doping in the layers ($N_{D,Ge} = N_{A,Ge} = 5 \times 10^{19} cm^{-3}$), the large work function of the Ni will influence the amount of band bending in the SiC.

1 μm of Ni was deposited onto the Ge/SiC surface using an argon plasma that was maintained at a flow rate of 20 sccm, a pressure of 2 mTorr, and an RF power of 500 W. Though 1 μm of Ni is quite a thick layer, this helped in the processing, allowing for more controllability on the Ni etch time.

6.2.3 Photolithography

A standard photolithography routine [95] was used to pattern the Ni/Ge/SiC structures. Photoresist was deposited over the entire chip using a Headway spinner machine. Shipley 1818 photoresist was applied to the chip using a pipette as the sample was spun at 4000 RPM, resulting in a photoresist thickness of 1 μm. The photoresist was selectively softened by exposure to 350 W of UV light for 30 seconds using a Karl Suss MJB21 mask

aligner and the mask shown in Figure 6.4. To protect the Ni dots and CTLM structures from the aqua regia etch, the light field half of the mask was employed. Once softened, the unwanted photoresist was removed by dipping the samples into a beaker of 319 Developer for 30 seconds. A DI water dip removed the remaining 319 developer.

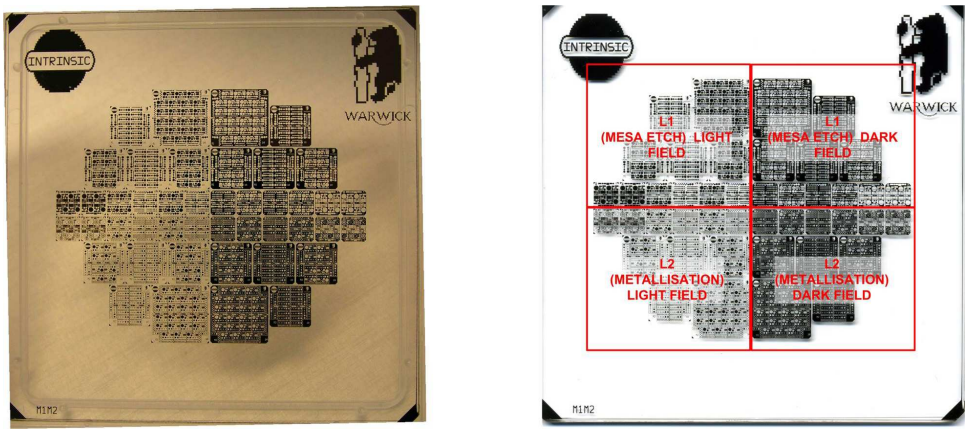


Figure 6.4: A photo and a diagrammatic view of the mask used to create the heterojunction diodes.

6.2.4 Device Isolation and Materials Etching

Full device isolation prevents the build up of an electric field at the abrupt edge of a contact, so that the highest possible breakdown can be achieved for the devices in question. A full treatment of state of the art techniques, such as guard rings and field plates is given in A.6. Here, due to the ease of processing, device isolation was achieved through a mesa etch using the existing metal contacts as the mask. This was carried out on half of each chip so that the CTLM structures on the protected half could be used to determine the contact resistivity at the Ni/Ge interface. The etch was achieved using a BOC-Edwards Plasma System RIE Machine, removing up to 1 μm of Ge with a 20:80 SF_6/Argon plasma for five minutes at a power of 10 W.

6.2.5 Contact Annealing

The final step in the fabrication process is an optional anneal. Annealing improves the interface between metal and semiconductor, creating more cohesion between the layers and hence improving ohmicity. At annealing temperatures ranging from 200 to 800^{o}C, nickel and Si form transitional silicide layers such as NiSi, Ni_2Si and $NiSi_2$, lowering the barrier height between the semiconductor and metal as they form [36]. Titanium and nickel silicides also form at a SiC interface [93, 96].

As will be seen in the proceeding Sections, a lot of the scientific interest in the Ge/SiC structures lay in the difference between Ge grown at low temperature and high temperature. It was imperative that the devices remained with their structural differences in tact after processing. Hence, the metal contacts, which had to be formed after Ge deposition to stop MBE contamination, were not annealed. This meant that experimental interest was retained at the expense of a higher contact resistance.

6.2.6 Resulting Structure

The finished Ni/Ge/SiC heterojunction processing may be seen in Figure 6.5, complete with dots and CTLM structures. This was the half of the wafer that had been etched, the other half having been protected from the etch for the CTLM testing. The cross section of these devices was shown in Figure 6.2.

6.3 Electrical Analysis of Heterojunction Layers

This Section describes the electrical analysis carried out on the heterojunction diodes. The progression of this Section is concurrent with Section 5.5, describing the electrical

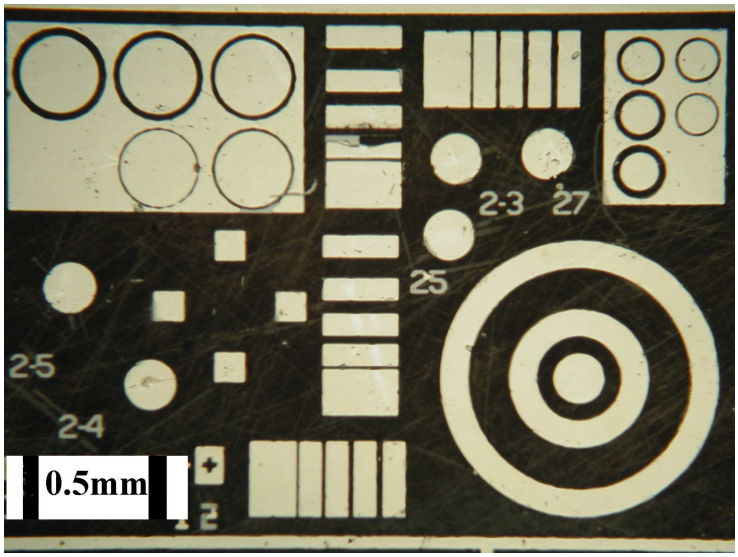


Figure 6.5: The result of all the processing: CTLM and TLM structures, and dots all ready for testing.

behaviour of the same thin films, comparing the different samples along lines layer thickness, deposition temperature, dopant type and deposition technique (MBE or WB). All the layers that were described in Section 5.5 underwent the processing described in the last Section, producing heterojunction diodes, and CTLM structures. The performance of the rectifiers will be analysed using I-V, C-V, IVT and CTLM analyses. A detailed description of these techniques can be found in Section 4.3.

6.3.1 The thickness and deposition temperature of MBE layers

Section 5.5 showed how the 100 nm and 300 nm n-type layers suffered from the same temperature deposition trade off, with the higher temperature layers forming the polycrystalline layers, whilst the low temperature layers were amorphous. The poor surface quality of the 100 nm layers improved as the thickness increased to 300 nm, the gaps between islands filling in to form a complete surface though this was still a way from

being perfectly smooth. In this Section the performance of these layers as heterojunction rectifiers will be assessed using I-V and C-V analysis. With the MBE layers of Ge highly doped, the heterojunction barrier should behave as a Schottky barrier as described in Section 3.4.

6.3.1.1 I-V Analysis

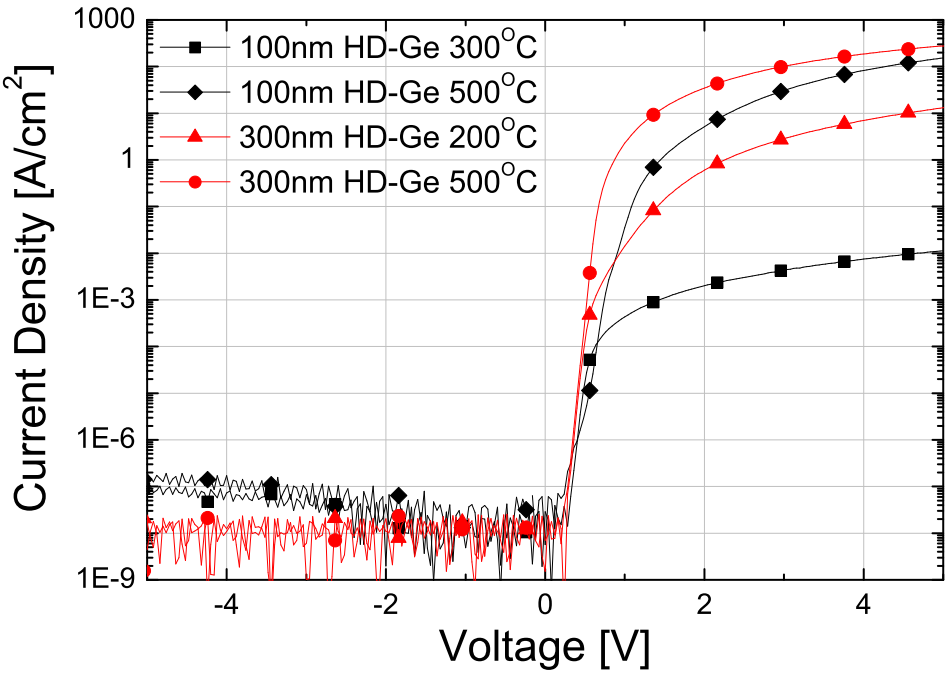


Figure 6.6: I-V results for the n-type 100 nm and 300 nm Ge/SiC heterojunction diodes.

Current-Voltage results for the 100 nm and 300 nm n-type diodes are shown in Figure 6.6. These results are typical of the ten contacts that were tested for each diode and were taken at room temperature (approximately 24^{o}C) using the probe station and Agilent Parameter Analyser as described in Section 4.3.1.1. Using the techniques described in Section 4.3 a lot of information may be extracted about these diodes. First of all though, visual inspection alone shows a great deal. The 300 nm, 500^{o}C diode has the highest

forward current, and hence, the lowest resistance, of any of the diodes. With the 100 nm and low temperature layers having a much larger resistance we can see immediately the straightforward correlation between the physical results and the electrical ones. In Section 5.5, the 300 nm, 500^{o}C layer was the only layer to be polycrystalline and free from patch contacts. What is more, this layer produced the smoothest surface of any polycrystalline layer produced. Comparing this layer to the amorphous, 300 nm, 200^{o}C layer, at 5 volts we can see that the polycrystalline layer has a current approximately 200 times greater than its otherwise equal, amorphous counterpart. Therefore, the multitude of grain boundaries within the amorphous layer has a significant effect on the electrons passing through the layer. Comparison between the 500^{o}C layers shows that the 100 nm layer has only a slightly higher resistance but a visibly poor turn on characteristic, most likely due to the poor patch contact. Further visual inspection of Figure 6.6 shows a split along layer thickness lines in the reverse direction. The leakage current is below the threshold of the measuring equipment for the thicker layers, whilst the thinner layers are experiencing leakage in the realm of 0.1 mA/cm^2 at only -5 V, values that will lead to unacceptable reverse leakage currents.

One curiosity of the Ge/SiC diodes is their low forward voltage drop. All the diodes begin to turn on very early, at approximately 0.3 V which is earlier than regular Ni/SiC Schottky barrier diodes [91–94]. This alone is an energy saving achievement, as minimal voltages are required to reach good current values. This is compounded somewhat by the high forward resistance of even the best diodes on display here, but if this resistance could be reduced by improving the Ge/SiC interface, then a markable power saving could be made. The reason for this early turn-on is that the Schottky barrier height at the Ge/SiC interface is likely to be smaller than that of a Ni/SiC interface. This is illustrated in Figure 6.7.

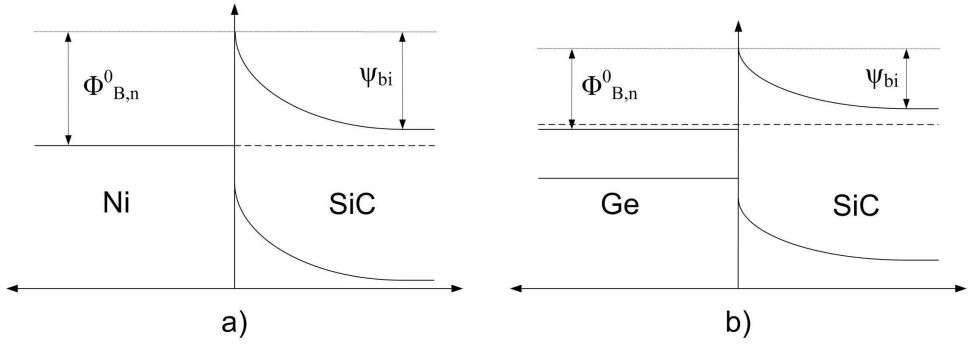


Figure 6.7: The band diagrams of a) Ni/SiC and b) Ge/SiC, showing the larger SBH in the metal-semiconductor.

Carrying out some more detailed analysis of the data that makes up Figure 6.6, the ideality factor (η) may be calculated, a value that gives some indication as to how well a device replicates the ideal diode equation of Equation 3.12. Close correlation, as $\eta \rightarrow 1$, indicates that thermionic emission current dominates and the diode will turn on efficiently and quickly. With η nearing 2, or more, then recombination current dominates. The 300 nm heterojunction diodes had ideality factors of 1.03 and 1.01 for the low- and high-temperature layers respectively. The 100 nm diodes produced ideality factors of 1.12 and 2.23 for the low- and high-temperature layers respectively. Hence, with the exception of only one layer the diodes demonstrate a quality Ge/SiC interface dominated by thermionic emission. The reason for the poor result in the 100 nm, 500^{o}C diode is understandable when one considers the AFM micrograph of this layer from Figure 5.16b. When the Ni is deposited on this surface, it contacts both the Ge islands and the SiC between the islands. Hence, as the device is turning on, there are multiple paths that electrons may follow, some more energetically favourable than others, explaining the visibly poor turn on characteristic.

The Schottky barrier height (SBH) may also be extracted. The SBH is the amount of energy that electrons must gain to pass from metal to semiconductor or indeed between

semiconductors at a heterojunction interface. As previously discussed, it is found by estimating the saturation current from the data and entering this into the ideal diode equation of Equation 3.15. The SBHs of the 100 nm diodes were 1.015 eV and 1.013 eV for the low- and high-temperature layers respectively. The 300 nm heterojunction diodes had SBHs of 1.085 eV and 1.094 eV for the low- and high-temperature layers respectively. The difference between these values is quite negligible and inconclusive. The absolute values themselves are very interesting, as they all concur that the SBH at a Ge/SiC interface is approximately 1.1 eV. When considering how the semiconductors align and form a band offset, it is clear that this value is too large to support a theory based on the classic Schottky-Mott principal [97, 98], which states that the vacuum levels will align, leaving the electron affinities to dictate the offset. With both semiconductors having electron affinities of approximately 4 eV, the Ge-SiC offset should be no more than 0.2-0.3 eV under this principal. Hence, in Section 7.3, Fermi level pinning will be discussed and used to explain these large offsets.

6.3.1.2 C-V Analysis

Capacitance-Voltage (C-V) measurements of these devices are shown in Figure 6.8. They were taken at room temperature using the low power Agilent Technologies B1500A Semiconductor Device Analyser, as described in Section 4.3.2. A frequency of 1 MHz was used and Figure 6.8 is typical of three runs that were taken on each of ten diodes. The doping concentration of the SiC and the built-in potential (ψ_{bi}) was extracted, from which the SBH was estimated. Cree suggested that the epitaxial layer was doped n-type at a concentration of 1.4×10^{15} atoms per cubic cm. Calculating the inverse slope (dx/dy) of each of the diodes in the Figure 6.8 produces doping concentrations of 6.3×10^{15} cm^{-3} and 2.4×10^{15} cm^{-3} for the 100 nm, low- and high-temperature layers respectively, and

1.6×10^{15} cm^{-3} and 1.7×10^{15} cm^{-3} for the 300 nm, low- and high-temperature layers respectively. All of these represent reasonable experimental error from the doping levels promised by Cree.

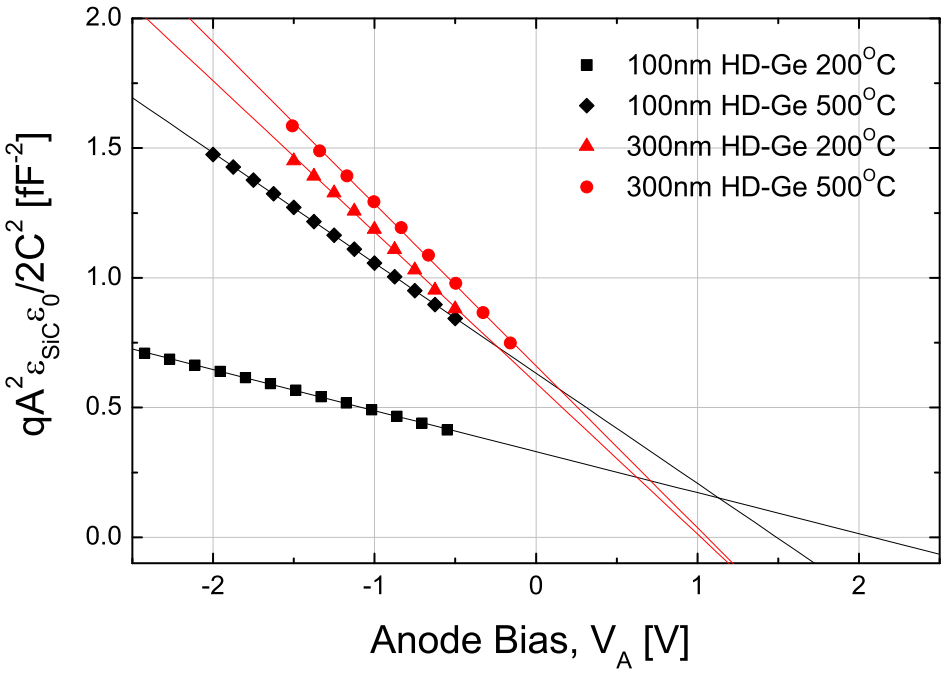


Figure 6.8: 1 MHz C-V results for the n-type 100 nm and 300 nm heterojunction diodes.

The built-in potential values, read from where the C-V data crosses the x-axis, can also be taken from Figure 6.8. The low- and high-temperature 100 nm diodes yielded values of $\psi_{bi} = 2.0$ and 1.5 eV respectively. Both 300 nm layers produced values of $\psi_{bi} = 1.1$ eV. The built-in potential is related to the SBH as,

$$\Phi_{CV} = \psi_{bi} + \phi_{n,SiC} - \phi_{n,Ge}, \tag{6.1}$$

where $\phi_{n,SiC}$ and $\phi_{n,Ge}$ are the fermi potentials as measured from the conduction band in SiC and Ge respectively, defined in Equation A.5 for a non-degenerate semiconductor,

and in 3.8 for a degenerate semiconductor. Using the calculated values of ϕ_n results in SBH values for the 100 nm layers of approximately 2.3 eV and 1.8 eV for the low- and high-temperature layers respectively, and of 1.4 eV for both 300 nm layers.

There is clearly a large discrepancy between the CV results and the SBH values taken from the I-V data (0.29 eV for the high temperature, 300 nm diode). This could be explained by the method in which the two techniques estimate barrier height. The C-V technique presumes that one is dealing with a homogeneous, uniform layer, where the SBH will be of one value at any one given point across the interface. However, most interfacial systems are far from being this perfect. Inhomogeneities at the surface cause a two-dimensional fluctuation in the SBH; the source of the inhomogeneities being from surface roughness, non-uniform doping or imperfect surface preparation leading to an unclean surface or an interfacial oxide. This is quantified and explained in detail in Section 7.2. Thus, a very commonly reported [70, 99–104] phenomena occurs where the C-V attained SBH value exceeds that attained from I-V methods. This occurs because by using I-V analysis, the majority of current passing through the layer will do so over only the lowest barriers, this being the path of least resistance. Values from C-V analysis are an average across the entire interface.

However, it seems likely that a discrepancy of nearly 0.3 eV is too high to be explained away this easily, and by consulting the M-S SBH theory [70] and performing further analysis, a secondary explanation was found for the large discrepancy. Figure 6.9 shows a 10 kHz $C^{-2} - V$ plot of the high temperature, 300 nm diode. A linear fit to the full data set has been plotted to satisfy Eq. 4.5 and the extraction of the built in potential. This results in a ψ_{bi} of over 2 eV, grossly over estimating the ψ_{bi} of 0.855 eV, that was extracted from I-V analysis (considering a SBH of 1.1 eV). This value drops by 0.5 eV if the data set is reduced to the data closest to the x-axis as was done previously for the 1 MHz data

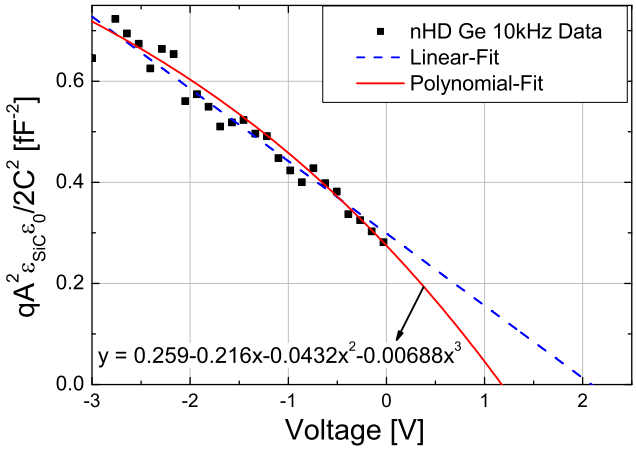


Figure 6.9: A $1/C^2 - V$ plot taken at 10 kHz for a polycrystalline n-type layer, with linear and polynomial fits to the experimental data.

in Figure 6.8; however this is an act that sits most uncomfortably. The accuracy of the linear fit to the experimental data can be brought into question by visual inspection alone, with the data scattered either side of the fit. However, attempting many non-linear fits of different order, a third order polynomial was found to produce the tightest fit to the data having a coefficient of determination (R^2) of 0.943. This fit can also be seen in Fig. 6.9. The ψ_{bi} extracted from this method results in a SBH much closer to that provided by the I-V analysis; however, ψ_{bi} is largely dependent on the frequency of the C-V measurement, varying from 1.25 eV at 1 kHz to 1.45 eV at 100 kHz. With a non-linear fit, the extraction of the doping could only be estimated by differentiating this curve at various points along its arc, a situation that produces doping levels ranging from 3.2×10^{15} cm^{-3}, closest to x-axis, to 1.0×10^{16} cm^{-3} nearest the y-axis, with the manufacturer stating a bulk SiC value of 1.4×10^{15} cm^{-3}.

The reason for the non-linearity originates form the way that the way that the $C^{-2} - V$ relationship is derived, as repeated in Appendix C. It is presumed that the only charge from the semiconductor is that from the space charge region, such that $Q_S = Q_{SC}$.

This statement can only be true when the Fermi level and charge neutrality level of a semiconductor are in alignment, under homogeneous and intrinsic conditions. In reality, the total charge should consider also charge at the interface (Q_{GS}), brought about by the inhomogeneous interface, thus making Eq. C.1

$$C = \frac{d\left(Q_{SC} + Q_{GS}\right)}{dV}. \tag{6.2}$$

The addition of this extra charge has a distinct impact on the parameters extracted from C-V analysis as seen in Figure 6.9. Various models exist attempting to include Q_{GS} in CV analyses, though the exact nature of the interface is still uncertain. Unique relationships exist between the interface parameters and the capacitance dependent on whether the metal and/or the semiconductor contribute charge to the interface, whether the charge on either side of the interface can follow the AC signal, and any combination of the above [105]. This is further complicated by the knowledge that these models presume that some interfacial layer has formed between the metal and the semiconductor due to processing defects. The validity of such a model has been brought in to question [70], due to its reliance on the original Schottky-Mott equation when the materials come in direct contact.

Realistically, these results are only useful in proving that interface states are prominent at the heterojunction interface. This will be further investigated in Section 7.3.

6.3.1.3 Thickness Conclusion

The results over this Section have consistently shown that the polycrystalline heteroepitaxial layers form the better contacts as suggested by their near ideal turn on and lower on-resistance. The thicker, 300 nm layers also outperform the 100 nm layers, achieving

good forward characteristics, and a low leakage current across their more uniform Ge/SiC interface. Encouragingly, all the devices produce near ideal I-V results, and a 0.3 V turn-on voltage. However, the forward resistance is high, potentially due to the lack of annealing of the contacts.

6.3.2 The Role of the Dopant

The layers of Ge considered in Section 5.5.1, consisting of p- and n-type dopants grown at low and high temperatures, are here electrically analysed after they were formed into mesa Schottky diodes. The physical analysis revealed that boron-doped p-type layers have greater x-ray intensities compared to the antimony-doped n-type layers, whilst the polycrystals of the p-type layers also appear bigger and leave a rougher surface. All this is evidence that the small, light boron dopants induce less stress than the big, heavy antimony dopants when they are incorporated into the SiC lattice. Hence, during growth, the crystals can grow to a large size before misfit dislocations and other stress-induced lattice faults prevent the crystals growing any bigger.

First of all, CTLM analysis was used to verify the ohmicity of the front and back contacts and to compare the conductivity of the Ge layers. Using I-V analysis the effect of the dopant on the layers was then analysed electrically.

It is worth repeating that the layers used here are all 300 nm layers, with the layers varying only in dopant type and growth temperature an a 2×2 matrix of parameters. The 300 nm n-type devices are those that were compared to the 100 nm n-type layers in the Section 6.3.1.

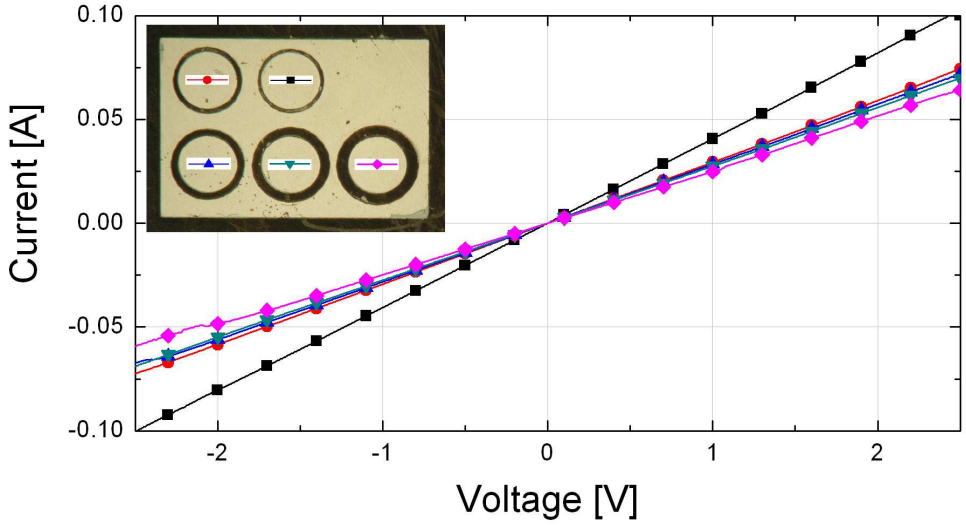


Figure 6.10: The CTLM I-V responses from the p-type Ge/SiC sample grown at 500^{o}C. Inset: Microscope images of the corresponding CTLM structures

6.3.2.1 CTLM Analysis

The ohmicity of the Ni-Ge layers can be verified using the techniques described in Section 4.3.3, confirming that the only rectifying action within the devices occurs at the Ge/SiC interface. The contact resistivity (ρ_c) and the sheet resistance (R_{sh}) can both be extracted from the CTLM measurements, of which a typical set is shown in Figure 6.10, taken at room temperature using the Agilent B1500A parameter analyser. ρ_c can be used to calculate the resistance of the Ni-Ge interface, whilst R_{sh} denotes the resistance of the Ge layer. These values may be extracted from I-V measurements taken from each of the CTLM structures using a spreadsheet to handle the extraction of the transfer length and the complex mathematics of Equation 4.12 with its associated Bessel Functions.

The contact and sheet resistance of all the Ni-Ge contact layers considered here are displayed in Table 6.1 and shown graphically in Fig. 6.11. The results clearly divide along crystallinity lines with the high temperature, polycrystalline layers forming the

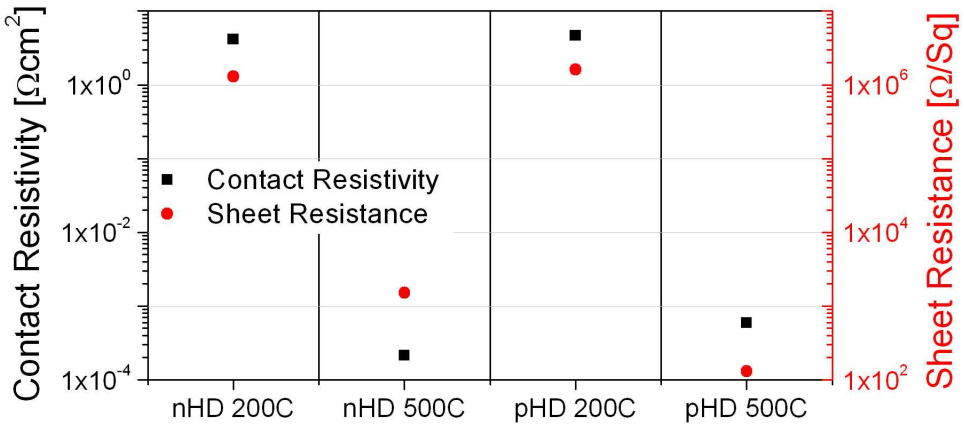


Figure 6.11: The contact resistivity and sheet resistances of four Ni/Ge layers as extracted using CTLM structures.

interfaces with the lowest resistance. All the contacts were proven to be ohmic, with the high temperature layers' contact resistivity of the order of 1×10^{-3} Ωcm^2. The sheet resistance of the p-type layer is over 25 times less than that of the n-type layer. This is most likely due to the greater incorporation of the dopant within the lattice that leads to large polycrystals and few grain boundaries.

The contact resistivities presented here are reasonably high, and will undoubtedly contribute to the series resistance of the I-V characteristics. The large values are due to the relatively low temperature anneal carried out. A higher temperature anneal (900-1000^{o}C) could reduce the contact resistivity of the Ni/SiC interface to a value as low as 1×10^{-6} Ωcm^2 [106]. However, a higher temperature anneal would affect the physical characteristics of the Ge layers, reducing the effects of the MBE deposition temperature, which we are trying to observe.

Diode	$n200$	$n500$	$p200$	$p500$
R_q (nm)	2.1	6.7	3.5	30
ρ_c (Ωcm^2)	2.8	4.93e-4	5.8	1.37e-3
R_{sh} ($\Omega/\square$)	2.1M	1262	1.8M	48.8
η	1.103	1.039	1.071	1.047
$\Phi_{B,n}$ (eV)	1.085	1.094	1.119	1.127
$R_{on,sp}$ ($m\Omega cm^2$)	474	18.3	26.6	17.3
V_B (V)	150	250	150	250

Table 6.1: The electrical properties of the 300 nm Ge/SiC heterojunction diodes, as well as the surface roughness (R_q) from the Section 5.5.1 for reference. The diode names refer to the doping type (n or p) and the deposition temperature (200^{o}C or 500^{o}C).

6.3.2.2 I-V Analysis

Typical current-voltage (I-V) results, taken from the Ge/SiC heterojunction diodes at 25^{o}C, are shown in Figure 6.12. From this data the ideality factors and Schottky barrier heights have been extracted using the techniques described in Section 4.3, and summarised in Table 6.1. The specific forward resistance was extracted from the graph in the inset of Figure 6.12 by taking the gradient (dV/dJ) at the linear region of each curve. All the heterojunction diodes approach perfect ideality factors, 1.1 being the highest value, with both the polycrystalline diodes having values under 1.05. The barrier heights ($\Phi_{B,n}$) were all between 1.05 and 1.15 eV, and the specific forward resistance ($R_{on,sp}$) of the polycrystalline diodes was below 20 $m\Omega cm^2$. These results compare well with the state of the art Ni/SiC diodes, which will be shown in Section 6.3.4.1. The breakdown voltage (V_B) of the polycrystalline diodes was over 250 V, with this expected to vastly improve with the addition of passivation and proper junction termination.

Fig. 6.12, displays the strongest argument for opting for the polycrystalline layers formed from the higher deposition temperature of 500^{o}C. The amorphous layers have a

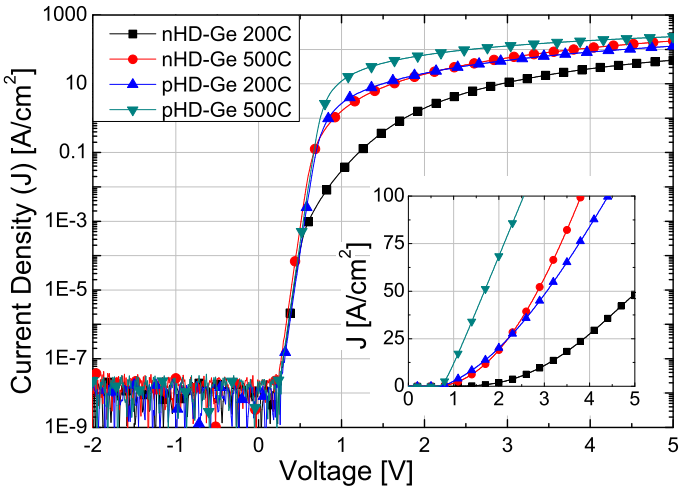


Figure 6.12: I-V analysis comparing dopant type and deposition temperature. The logarithmic and linear (inset) responses are plotted.

much larger specific forward resistance due to the large number of grain boundaries that slow the progress of an electron through the material. A better solution for overcoming the surface roughness seems to lie in post deposition polishing, such as has been carried out on SiC surfaces [80].

In comparing the dopant types, it is not surprising that the p-type layers have a lower specific on resistance than the n-type layers, considering the difference in poly-crystal grain size already discussed. What is more interesting about the differing dopant types is the complete lack of differences between the two, especially in the high temperature layers. They both turn on in a near ideal fashion, with only about some 40 mV gap between the two in a distinctly unipolar, Schottky manor. What is more, the SBHs extracted are only 33 meV apart.

The unipolar action in the p-N devices deserves an explanation, as one might expect some bipolar action. This can be attributed to a high barrier to holes, similar to that reported in Si/SiC heterojunction devices [19,20]. This is further demonstrated in Figure

6.13, where the band diagrams of the p-N Ge/SiC structures are shown before and after the bands align. Given the vast 3.25 eV bandgap of SiC, and a SBH of 1.1 eV taken from the experimentation, there is already another 2.15 eV between the Ge Fermi level and the SiC valence band before the layers enter equilibrium. This gets larger as the SiC bands bend downwards to align the Fermi levels, and hence there is an even greater barrier to electrons.

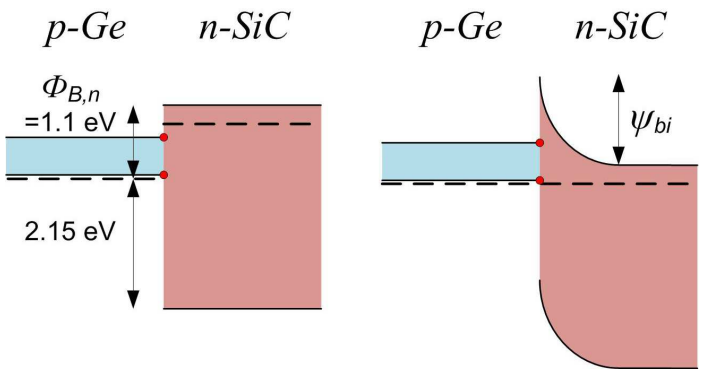


Figure 6.13: The band diagrams for p-N Ge/SiC heterojunction before and after alignment.

The near identical turn-on and SBH values across the p-N and n-N barriers has significant implications, suggesting that the Ge is pinned within the SiC bandgap such that the doping has no effect on the characteristics. In Section 6.3.1.2 the evidence of surface states at the interface are a further indicator that Fermi level pinning may be occurring. Whilst interesting, Fermi level pinning is quite an in-depth subject that is an aside from the comparison of layer types presented in this Chapter, hence it will be addressed fully in Section 7.3.

6.3.3 Intrinsic Ge Diodes

The final MBE structures analysed in this Chapter are thick layers of intrinsic Ge (iGe). Layers 500 nm and 1 μm thick were deposited without any intentional doping. The thicker layers were grown at high and low temperature, while the single thinner layer was grown at high temperature. All the layers were topped with a high temperature, 100 nm highly n-doped layer (5×10^{19} cm^{-3}) in order to form an ohmic contact with the metal. C-V analysis will first be used to assess how 'intrinsic' these structures turned out to be, given that it is a virtual impossibility to reduce unintended doping to zero. Secondly the I-V results of the structures will be compared.

6.3.3.1 Intrinsic or lightly doped?

One caveat to the term intrinsic used here, is that MBE deposition is a somewhat dirty process, and stray, unintentional dopants are likely to have contaminated the layers to a degree. Two ways to check the doping of the layers involve the C-V techniques introduced in Section 4.3.2. Although significant doubt has been cast upon the use of $1/C^2$-V analysis in the previous Sections, taking a tangent to the sloping profiles should still be adequate to give a 'ballpark' indication of the doping. An example of this, taken at room temperature and 100 kHz, from the 1 μm high temperature iGe diode, is shown in the inset of Figure 6.14, where both n-type and p-type dopants contribute capacitance slopes either side of zero volts. Extracting the doping from these slopes, furthest away from zero, results in a doping in the region of 4×10^{17} cm^{-3}. The presence of both dopant types in equal measure suggests that the most likely source of this doping is contamination from the MBE. The absolute value of this does seem high; however.

A second technique was used to assess the doping profile of the 500 nm high tem-

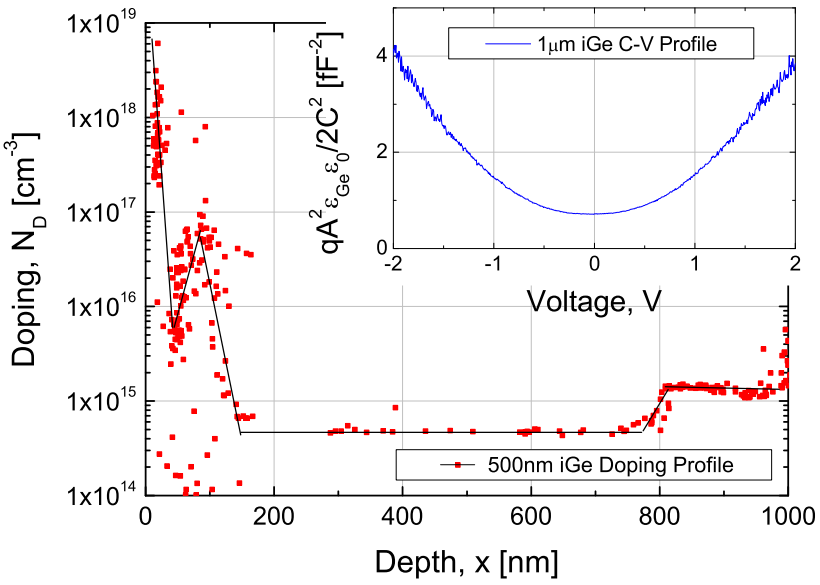


Figure 6.14: Capacitance-voltage results of a 1 μm thick, high temperature intrinsic Ni/Ge/SiC diode prepared in a $1/C^2$-V plot. Inset: The doping profile of the 500 nm thick, high temperature intrinsic Ni/Ge/SiC diode as extracted from a C-V sweep.

perature *i*Ge diode, a sample from which the C-V results were inconclusive. Originating from [65], and introduced in Section 4.3.2.1, this technique gives an effective doping profile, which is approximately the sum of the two dopant types at that point, though this is approximately equal to the majority carrier profile when $n >> p$ or vice versa. This means that one cannot differentiate the dopant types and hence the MBE contaminating species using this method. The doping profile of the diode is shown in Figure 6.14 shows a region of high doping 100-150 nm from the surface, as expected with the 100 nm highly doped cap layer forming an ohmic contact to the metal. This then drops away to a value of approximately 5×10^{14} cm^{-3} for 500-600 nm, before raising again to a value just above 1×10^{15} cm^{-3}, approximately that expected from the SiC. This is the profile that would be expected from this structure, and therefore it may suggest that the doping figure taken from the $1/C^2$-V technique is just an average over the top few hundred nanometers of Ge.

However, given the evidence of p-type dopants to a similar level as n-dopants, the value of 5×10^{14} cm^{-3} for the Ge bulk is likely the product of both dopant types.

6.3.3.2 I-V Results

The current-voltage plots for the three intrinsic Ge diodes are shown in Figure 6.15 along with that of the high temperature 300 nm Ge/SiC diodes from the last Section for comparison. The Figure shows that like the highly doped layers, the intrinsic layers are all turn on at around 0.3 V, though there is clearly quite a difference in performance between the best 500 nm *i*Ge diode and the 1 μm *i*Ge diodes. The properties extracted from these diodes are listed in Table 6.2. The 500 nm diode produced an ideality factor of only 1.026, with a series resistance of 12.2 $m\Omega cm^2$, which represents the best performance of any of the diodes so far. The 1 μm diodes appear to be plagued by high resistance and ideality factors that exceed most of the other diodes.

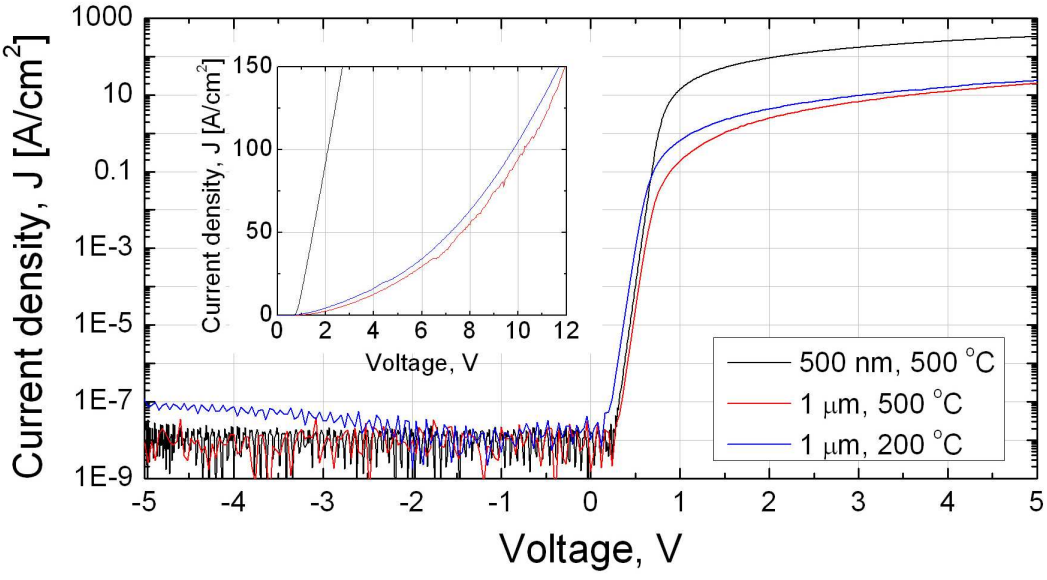


Figure 6.15: Current-voltage results of the intrinsic Ni/Ge/SiC diodes in both log-linear and linear (inset) format.

The previous Chapter revealed the difference in grain size and surface roughness between the thin and thick high temperature intrinsic diodes, the 500 nm *i*Ge layer having an rms roughness of 30 nm, compared to 45 nm rms for the 1 μm *i*Ge layer. The inset of Figure 6.15 now shows the vast difference in series resistance between the layers, which could be explained by the impact of a less homogeneous Ni/Ge interface with increased surface roughness. Alternatively, it could well be that the threshold was reached, whereby increasing the thickness of the Ge layer stops benefitting the overall system due to the Ge forming into larger crystals, and begins simply adding more resistance and grain boundaries. However, it seems most likely that the biggest single influence on the poor 1 μm *i*Ge diodes will have been the immaturity of the processing, as the 500 nm diodes were produced a long time later, with a much more refined and elegant fabrication process.

Dopant	*n*	*n*	*p*	*p*	*i*	*i*	*i*
Dep. Temp. (^{o}C)	200	500	200	500	500	300	500
Thickness (nm)	300	300	300	300	500	1000	1000
R_q (nm)	2.1	6.7	3.5	30	32	6	45
η	1.103	1.039	1.071	1.047	1.026	1.120	1.082
$\Phi_{B,n}$ (eV)	1.085	1.094	1.119	1.127	1.086	1.040	1.153
$R_{on,sp}$ ($m\Omega cm^2$)	474	18.3	26.6	17.3	12.2	36.9	35.3

Table 6.2: The electrical properties of the intrinsic Ge/SiC heterojunction diodes, compared to the 300 nm *n*- and *p*-type Ge diodes. The surface roughness (R_q) from the Section 5.5.1 is included for reference. η is the ideality factor, $\Phi_{B,n}$ the SBH and $R_{on,sp}$ the specific on-resistance.

Comparing now the best *i*Ge layer to the best highly doped layers, the series resistance of the intrinsic layer is evidently a little lower. The reason for this is most likely the reverse argument of the previous paragraph, whereby the thicker 500 nm layer is allows the Ge more space to relax and form into bigger crystals, or, that the huge reduction in dopant

concentration is allowing the Ge adatoms a more stress free environment in which to develop. Given the reasonably small decrease in the resistance from the p-type layer to the n-type layer, an increase in surface roughness by 2 nm appears to back up this hypothesis.

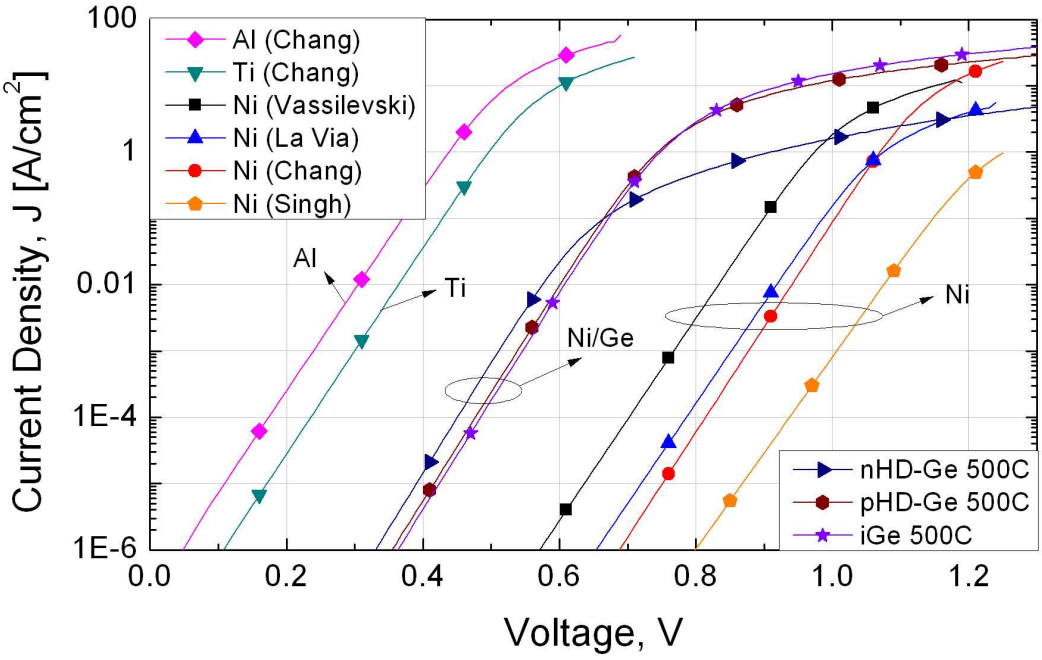
6.3.4 Benchmarking to SiC SBDs

The best MBE Ge/SiC diodes considered within this Chapter in terms of forward resistance, blocking voltage, leakage current and ideality factor were those grown to a thickness of between 300 and 500 nm, at the higher temperature of 500^{o}C. In this Section, these high temperature Ge/SiC diodes, which were formed from intrinsic, p-type and n-type Ge, will be compared to SiC metal/semiconductor Schottky Barrier Diode results taken from the literature.

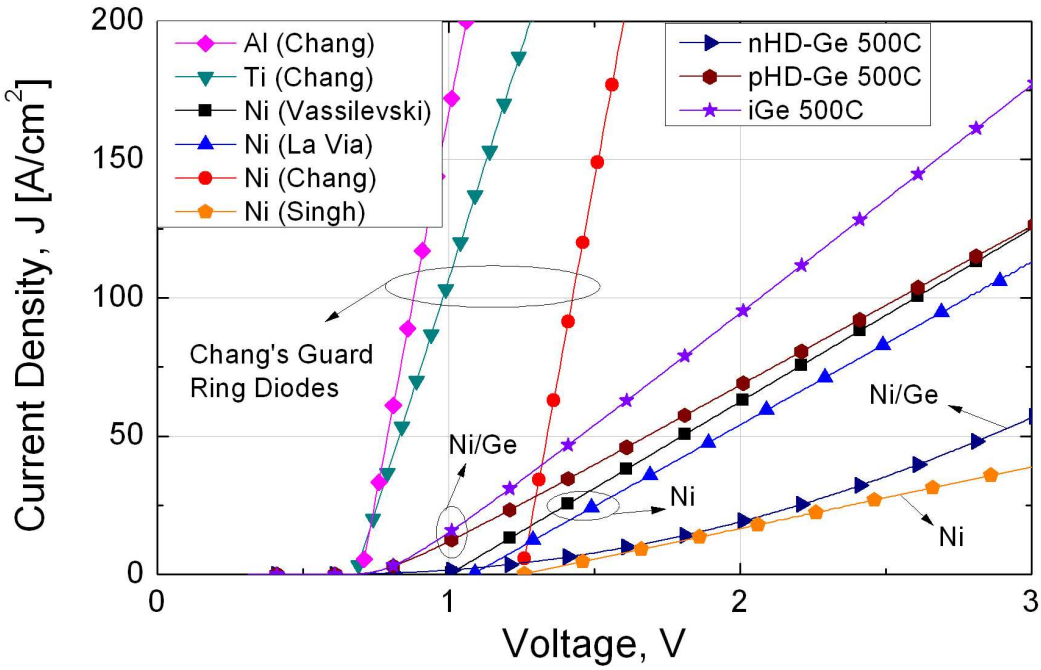
6.3.4.1 The Model Diodes

The diodes considered here [91–94] originate from four different groups and feature devices designed for high voltage blocking and those rated at a lower voltage but with a much lower specific-on resistance. The results are showed in Figure 6.16.

As suggested in Section 2.4 and Appendix A.6, a trade off exists between blocking voltage and series resistance due to the thickness of the epi-layer. This is shown in its extreme when, 10 years ago, the then brand new material, SiC, was being pushed to its limits. Singh et al [94]produced a 5 kV SBD, formed from a 50 μm epitaxial SiC layer doped at 5×10^{14} cm^{-3}. The authors of this work claimed a specific on-resistance of 17 mΩcm^2; however, a simple fit to their data using the ideal diode equation suggests that a figure of 45 mΩcm^2, may be more accurate. Made using a Ni contact, this is one of the reference diodes displayed in Figure 6.16. Another more extreme example [107],



(a) Ideality Factor and SBH Profiles.



(b) Resistance Comparisons.

Figure 6.16: A comparison between the Ni/Ge/SiC diodes and SiC diodes found in the literature [91–94].

not shown here, was a 10 kV device produced from a massive 115 μm epitaxial SiC layer doped at 5×10^{14} cm^{-3}. The price paid for this was the specific on-resistance, which was up at 97.5 mΩcm^2.

At the other end of this trade-off is the work by Chang et al [92], who used a 10 μm epitaxial SiC layer doped at 3×10^{14} cm^{-3}, - very similar substrates to those used to produce the Ge/SiC heterojunction diodes. Conducting a study that optimised the use of floating metal rings to distribute the electric field at the SiC surface, they achieved a breakdown close to 1 kV for a Ni/SiC diode at a specific on-resistance estimated to be as low as 1.75 mΩcm^2. Similarly impressive on-resistance values were achieved for titanium and aluminium contacts, and these are also shown in the Figures.

Two other SBDs are presented in Figure 6.16, the details of which are listed in 6.3. Vassilevski et al [91] produced a 3.4 kV SBD from a 20 μm epi-layer at 16 mΩcm^2. Finally, for a comparison across polytypes, a 6H-SiC SBD produced by La Via et al is also included. Their 4 μm epi-layer produced an on-resistance of 17 mΩcm^2, but breakdown is not stated.

Diode	nGe	pGe	iGe	Ni [94]	Ni [91]	Ni [93]	Ni [92]	Ti [92]	Al [92]
Epi (μm)	10	10	10	50	20	4	10	10	10
Epi N_D (cm^{-3})	1.4e15	1.4e15	1.4e15	7e14	3e15	2.8e15	3.5e15	3.5e15	3.5e15
V_B (V)	250	250	–	5k	3.4k	–	900	850	600
$R_{on,sp}$ (mΩcm^2)	18.3	17.3	12.2	17/45*	16*	17*	1.75*	3*	1.8*
η	1.039	1.047	1.026	1.1	1.1*	1.07	1.163	1.094	1.176
$\Phi_{B,n}$ (eV)	1.094	1.127	1.086	1.41	1.4	1.30	1.38	0.99	0.77
ρ_c (Ωcm^2)	5e-4	1.e-3	–	–	–	4e-5	–	–	–

Table 6.3: The best Ge/SiC heterojunction diodes compared to Ni/SiC SBDs taken from the literature as follows: a) Singh [94], b) Vassilevski [91] c) La Via [93] d) Chang [92]. V_B is the breakdown voltage, $R_{on,sp}$ the specific on-resistance, η the ideality factor, $\Phi_{B,n}$ the SBH and ρ_c the contact resistivity. Parameters with the * are estimated from fitting parameters.

Considering the very experimental nature of the Ni/Ge/SiC structures, these devices

do not look out of place amongst these metal-semiconductor devices. All three Ni/Ge/SiC structures produce an ideality factor below 1.05, lower than all the diodes taken from the literature. This indicates that thermionic emission dominates the transport of carriers over the heterojunction interface, as predicted by the diode equation of Equation 3.12. The best heterojunction diode has an on resistance of just 12.2 mΩcm^2, which compares favourably with La Via [93] and Singh's [94] diodes, though they fall behind the other diodes employing a 10 μm epi layer. This is however in light of a number of imperfections such as grain boundaries and poor contact resistivity, the improvement of which will lower this resistance further. Considering the ohmicity of the contacts, the p- and n-type Ge/SiC devices are respectively 2 and 1 orders of magnitude higher than that reported by La Via et al [93]. Having proven that high temperature layers produce good diodes, experimentation with post MBE anneals is a future project that will produce better Ni/SiC back contacts and Ni/Ge front contacts.

However, the heterojunction diodes simply cannot compete in terms of breakdown voltage. Proven in extensive studies on oxide/poly-Si [108–110], such rough surfaces and the large number of grain boundaries promote the build up of an electric field at the surface, diminishing breakdown and causing leakage through the oxide layer. The Ge/SiC structures also suffer from their very simple structure. For ease of fabrication, these devices were formed from very simple mesa-etched dots that required just one photolithographic mask level to produce. The devices from [91, 92, 94] in Table 6.3 involve the use of edge termination, whilst [91] also employs surface passivation. Boron implants in [91, 94] are used to form their junction termination extensions (JTE) adding complexity, mask levels and cost. The lack of such an edge termination in the Ge/SiC devices explains the low breakdown values as the spreading of the electric field across the surface is unabated and the devices are allowed to breakdown at the weakest point, the contact edge. A potential

device structure including JTEs is shown in Figure 6.17. The potential is clear in these structures to block a significant voltage, as 250 V is not insignificant. What is also greatly encouraging, is the results of Si/SiC heterojunction diodes [19,20], that managed to block 1600 V using the same 10 μm SiC epitaxial layers but with JTEs and field plates. It seems likely that Ge could reach very similar levels given these more advanced processing techniques.

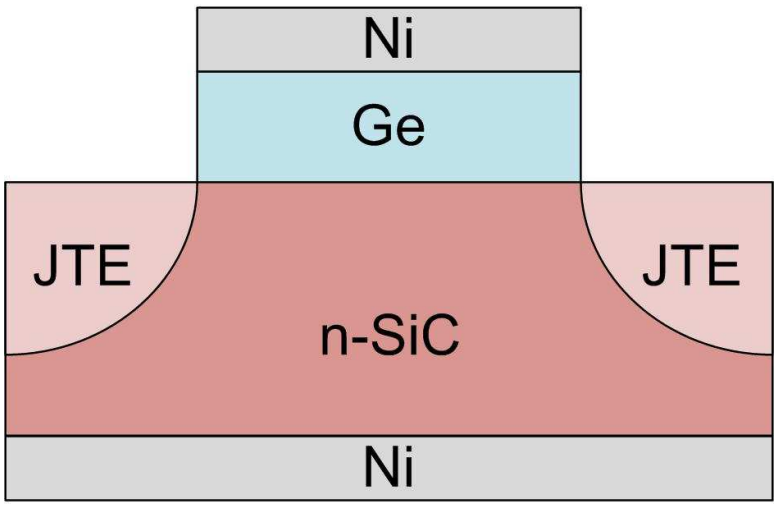


Figure 6.17: A heterojunction SBD with Junction termination extensions.

There are two further mitigating points for the breakdown results. The barrier height for these devices is around 75 % that of a Ni/SiC Schottky diode and the effect that this has can be witnessed in Table 6.3. Chang et al's aluminium and titanium diodes with barrier heights of 0.77 and 0.99 eV respectively give rise to breakdown voltages of 600 and 800 V. Given a barrier height of 1.1 eV, the 800 V figure should be a minimum figure achievable by the Ge/SiC diodes. However, the final mitigating point is that the use of Ge most likely has an impact on the breakdown values as well, being that it has a critical field only one tenth that of SiC.

Of course, with funding, facilities and time, exploration into the use of post deposition polishing and edge termination techniques ought to be explored to maximise the breakdown values of these devices. However, one reasonably cheap way to achieve such a result will be to employ the floating metal ring edge termination, which features in Chang et al's work [92]. Claiming an increase in breakdown voltage of 142 %, their very simple design looks possible to implement in only one mask layer.

6.3.5 Si/SiC Results

Figure 6.18 shows the I-V results of the wafer bonded Si/SiC diodes compared to MBE Si/SiC diodes taken from [14, 15]. The metal contact to these layers was formed using a mercury probe, therefore the results do not stand up in comparison to the Ge/SiC diodes. Taking first the wafer bonded samples, the results indicate a huge series resistance and a meagre reverse characteristic. However, given the experimental nature of these structures, that they were formed via wafer bonding it is quite an achievement to see that they produce a Schottky-like response. It even produces a reasonable turn on characteristic, free of the bumps that plague the MBE formed layers. With an ideality factor of 2, recombination dominates in these structures.

In Section 5.4, high temperature layers were shown to form non-uniform layers with large islands at thicknesses up to 3 μm. This means that any metal placed on the substrate surface will be contacting both Si and SiC at the same time. This accounts for the turn-on characteristics of the MBE high-temperature (900^{o}C) Si/SiC diode, where the many bumps that appear in the I-V response as the device is turning-on represent the differing Ni/Si/SiC and Ni/SiC SBHs. Also, the low temperature Si/SiC diode has a large leakage current.

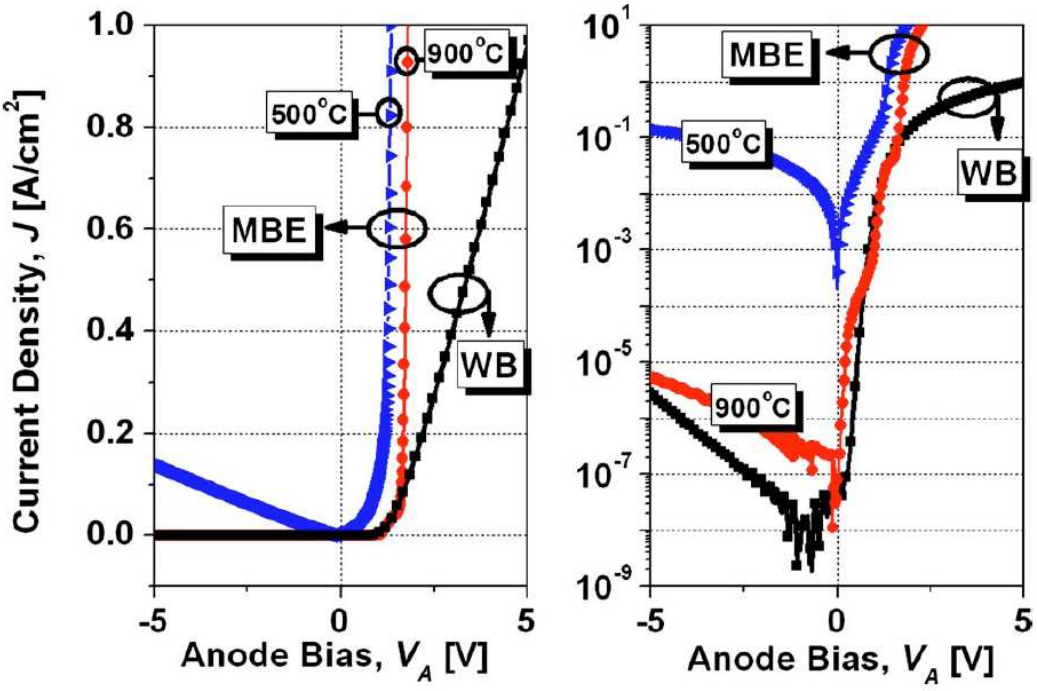


Figure 6.18: A comparison between the wafer bonded Si/SiC diodes and MBE Si/SiC diodes found in the literature [14, 15]. In this log-linear format, the ideality factors and the SBH dictated turn-on voltage can be compared.

Undoubtedly these results would improve with full processing using Ni front and back contacts. The series resistance would drop and a more homogeneous metal-semiconductor interface may prevail. However, it is highly doubtful that they would match the the Ge/SiC results due to the non-uniformity and poor coverage achieved by the MBE device and the inhomogeneous heterojunction interface of all the Si/SiC layers.

6.4 Summary

Central to this thesis, the work in this Chapter has seen the heterojunction layers of MBE Ge/SiC and wafer bonded Si/SiC formed into heterojunction diodes through the implementation of ohmic front and back contacts and a mesa etch. The MBE diodes performed

well, producing devices that compared very favourably with SBDs found in the literature. The intrinsic and p-type diodes in particular gave a low specific on-resistance and an exceptional ideality factor indicating that thermionic emission dominates the transport of carriers over the heterojunction interface. A barrier height of approximately 1.1 eV for all the diodes mean that they require less voltage to turn on in comparison to a standard Ni/SiC SBD. This is likely to come at a cost and there is likely to be an impact on leakage current and maximum achievable breakdown.

Comparing between Ge layer types, the influence of deposition temperature, layer thickness and dopant type became evident and parallels nicely with the results from the physical section. The general trend appears to be that the layers formed from the fewest and largest polycrystals tend to form the best layers, most likely due to the reduced number of grain boundaries and the better interaction with the SiC surface. Evidence for this was seen in this Chapter as polycrystalline layers significantly outperformed amorphous ones and as the rougher intrinsic and p-type layers out-performed their n-type counterparts, most likely due to the physical size of the dopant atoms in the Ge lattice. The one caveat to the "bigger is better" crystal theory seems to come in the layer thickness. The biggest single crystals were evident in the thinnest, 100 nm layers; however, the fact that these had not at this thickness merged to form a uniform layer, meant that a patch contact was formed and the results were poor. Also there appeared to be an optimum thickness, somewhere between 300 and 500 nm, where it seems the increasing thickness only adds resistance despite the increasing surface roughness and crystal size.

6.5 Conclusions

1. Ge/SiC layers formed via MBE produce very ideal turn-on characteristics with a

consistent barrier height of 1.1 eV. The lowest on-resistance is produced by the layers with the least grain boundaries, grown at high temperature and with physically small (or even without) dopants.

2. The rough surfaces and the lack of edge termination, passivation or other techniques promote the build up of an electric field, and hence the low breakdown values.

3. The use of C-V techniques in heterojunction analysis was seemingly discredited as the presence of interface states between the semiconductors added non linearities to the $1/C^2$ - V plots.

Chapter 7

Inhomogeneities, Surface States and their Impact on the Heterojunction Interface

7.1 Introduction

Heterojunctions are prevalent throughout the semiconductor industry, occurring in applications including lasers, solar cells and many modern transistors such as HEMTs and those employing strained Si. Therefore, some of the issues raised in the last Chapter, such as SBH discrepancies and Fermi level pinning have a much wider impact than being refined to just these SiC devices. Therefore, with this in mind, the focus of this PhD thesis shifts from the production of power devices to the explanation of the device physics - an attempt to solve the materials science problems that impact the wider semiconductor community.

It must be pointed out that Ge/SiC is an extreme example in most senses, especially when compared to more common heterojunction structures such as Si/SiGe and GaAs/AlGaAs. The large lattice mismatch leads to polycrystalline lumps of Ge covering the SiC surface, hence the defects and the roughness of the layers produce countless inhomogeneities at the interface. Furthermore, the conduction band offset and hence the SBH

between the layers, is also huge, the SBH regularly being measured via I-V techniques at 1.1 eV. However, it is in this extreme example with its large SBH and inhomogeneous nature that techniques have been refined to quantify both.

This whole Chapter sets out to answer the lingering questions from the last Chapter by analysing in great detail the interface between the layers. Firstly, the I-V/C-V discrepancy is revisited using detailed analysis techniques to quantify a large distribution of SBH values at the interface. Next, in Section 7.3, Fermi Level pinning of the SiC layer is cited as the reason why the SBHs extracted are so large, when the Schottky Mott principle states it should be so much lower. In Section 7.4, the question is raised of why the p-type and n-type Ge layers produce such consistent SBH values. A Pinning Model is proposed that explains the behaviour of these seemingly inseparable layers, showing that they can indeed be separated when one looks at their reverse bias characteristics.

Of course, many of these questions have already been answered in the far more familiar setting of the metal-semiconductor interface. Many studies over the last 50 years have quantified the Fermi level pinning of these Schottky barrier devices [70, 111–113] and likewise Tung's papers on SBH fluctuations at these interfaces [70, 100–102], are seminal works. Here, this existing work is built upon, changing the boundaries by considering two semiconductors in contact, each with their inhomogeneities, surface states and surface band bending, and consider how they interact in intimate contact.

Throughout this Chapter the 300 nm, p-type Ge layer grown at 500 ^{o}C on n-type 4H-SiC will remain the benchmark sample, on which all the proceeding theory is tested. The techniques have been verified on the other heterojunction diodes, and their results shall also be reported.

7.2 Ge/SiC SBH Fluctuation

In Chapter 6 a number of discrepancies arose, chief amongst these being that a SBH extracted from C-V analysis always exceeded one taken via I-V analysis. The reason for this can be partially explained by the non-linearities within the C-V plot, which discredits the accuracy of this technique. However, in devices that are not inhomogeneous to this degree, this SBH discrepancy still arises. Indeed, a polynomial line of best fit to any of the C-V results in Section 6.3.1.2 still produce C-V SBH results that are greater than the I-V results.

The reason for the discrepancy can be very easily explained: Quite simply, there is no one SBH at an inhomogeneous interface and instead one should consider the interface as an array of patches of varying SBH. Without actually passing current through the device, C-V techniques look at this entire interface and produce an average value. I-V techniques involve a significant current passing over the interface, and as such, the carriers find the path of least resistance, i.e. the lowest barriers. This situation naturally leads to some questions, namely: Which is correct? Can the fluctuations be quantified? What impact does this have on our devices? In this Section, these questions are answered using various techniques to quantify the fluctuations, resulting in an array of information about the interface.

I-V/C-V discrepancies and SBH fluctuation is not uncommon in SBH extraction, with this phenomena having been explained at length in several metal-semiconductor studies over the last two decades [100–104, 114–117], with inhomogeneities at the interface always being cited as the cause for the error. Despite the comprehensive treatment of this subject, it was obvious that this had never before been reported for heterojunction structures, and hence a novel opportunity arose to adapt this technique for use in heterojunction devices.

7.2.1 Inhomogeneities and their Impact on the Interface

Inhomogeneities are imperfections at the interface between two intimate materials. They are borne from the surface not being atomically flat due to grain boundaries, multiple phases, facets and defects [116]. Other sources of inhomogeneity include non-uniformity within the doping profile [103] and residual materials left over from processing [104] creating interfacial states between the surfaces.

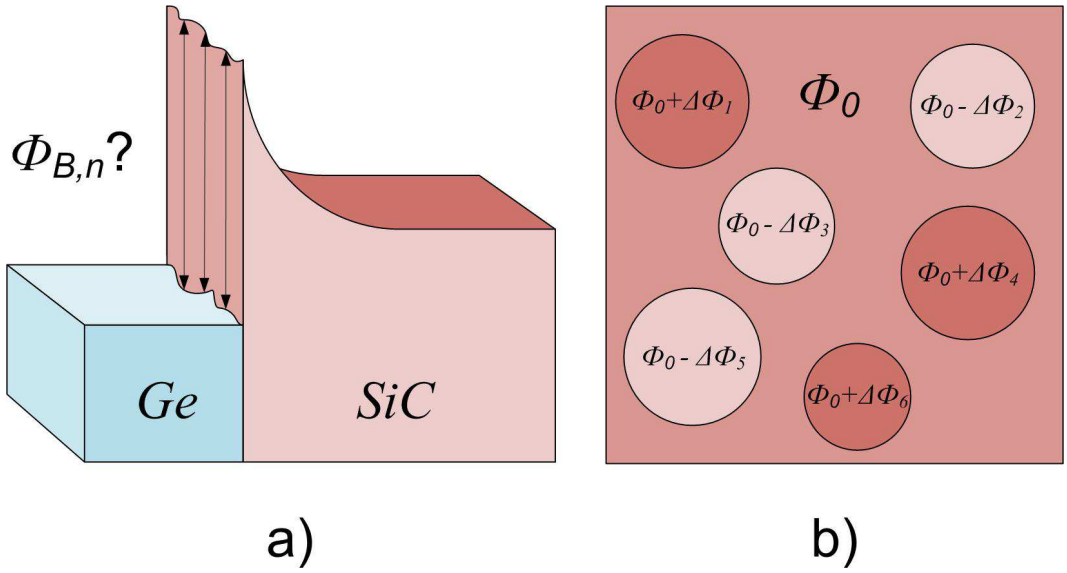


Figure 7.1: a) The band diagram of an inhomogeneous Ge/SiC heterojunction extended into three dimensions, showing the potential fluctuation in the SBH. b) The interface as it is perceived here, with patches of varying SBH sitting in a background mean SBH value.

Inhomogeneity at the interface of two materials causes spatial fluctuations in the SBH to occur. Figure 7.1a, represents this by extending the band diagram into three dimensions to effectively include a 1-dimensional profile of the SBH variation. Extending this idea further, one may imagine the heterojunction interface as in Figure 7.1b. Against a background, mean SBH value (Φ_0), patches of varying SBH are present [100–102], the

physical size of which are considered to be small compared to the depletion width of the semiconductor [117]. Over an entire contact, the SBH is assumed to have a Gaussian distribution with a standard distribution (σ) about Φ_0 [101–103, 114, 116]. Given this, many patches exist with a SBH significantly lower than the mean value, which explains the I-V and C-V analysis discrepancy. When finding a path through the interface of the two materials, the carriers choose the path with the lowest barrier to overcome, the result being that the I-V analysis yields a lower than average barrier height. C-V analysis considers an average value over the whole interface, therefore this value is very likely to be closer to Φ_0 [103, 114]. Ballistic electron emission microscopy on Pd/6H-SiC barriers, has recently confirmed the presence of a nanometer scale distribution of SBH [118], whilst conductive atomic force microscopy has also been used to map inhomogeneities on Au/4H-SiC samples [119].

The origins of inhomogeneous Schottky barrier research dates back to the 1960's when non-linearities within the classic Richardson plot (a technique introduced in Section 4.3.1.2) hindered the extraction of the correct SBH and Richardson constant (A^{**}) [120]. This became known as the T_0 effect whereby it was found that adding a temperature constant into the thermionic emission equation the plot would linearise and aid in the extraction of the SBH. It is now known that at an inhomogeneous Schottky Barrier, the SBH will rise and the ideality factor drop as the temperature is lowered due to the junction current becoming dominated by fewer low SBH patches [100–102]. This SBH temperature dependence is what causes the non-linear Richardson Plots. Many solutions were suggested to return linearity to the plots [120–122] before the link with inhomogeneities was made [101, 103, 114, 123].

Two techniques exist to modify the classic Richardson plot to information about the barrier height, taking into account the inhomogeneous patches of low SBH that dominate

the I-V extraction. The first involves the presumption that the majority of current flows over the few smallest barriers, and hence the experimental I-V-T data is simulated using lower SBH values and smaller areas. The second technique uses Gaussian statistics to extract a distribution of barrier heights surrounding a mean SBH value (Φ_0), which is considered close to that extracted by C-V analysis [103, 114].

In Sections 7.2.3 and 7.2.4, these techniques will be explained in greater detail and used on the Ge/SiC diodes to attain the relevant SBH values. First however, the classic techniques introduced in Section 4.3.1.2, including the unmodified Richardson plot, will be applied to our test sample to produce more information on it.

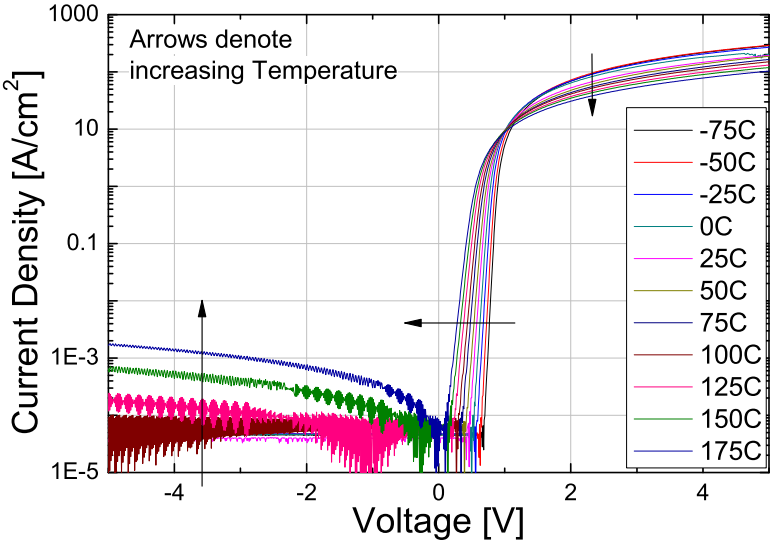
7.2.2 The Extraction of the SBH via Classic Techniques

The two techniques introduced in Section 4.3.1.2 allow us to exploit the temperature dependence of the diode equation parameters to produce further information about the 300 nm, n-type Ge layer grown at 500 ^{o}C on n-type SiC. The starting point for all the analysis is the extraction of information from I-V-T plots of the sample. Figure 7.2 shows the I-V plots and the SBH and ideality factor values extracted from it, plotted against the relevant temperature.

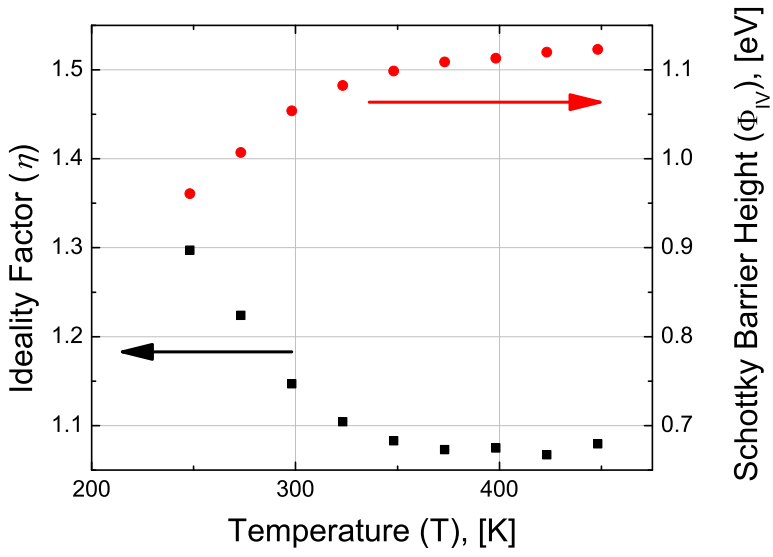
The diode equation of Equation 3.12 is repeated here for ease.

$$I = AA^{**}T^2 e^{-\beta\Phi^0_{B,n}} \left(e^{\frac{\beta V}{\eta}} - 1 \right). \tag{7.1}$$

The values of A, A^{**}, T and β ($\beta = q/kT$) are all known prior to any testing, making them fixed. $\Phi^0_{B,n}$ and η can both be determined from a single I-V plot; however, the temperature dependence of both dictate that the value extracted will only be accurate at the temperature of measurement. This dependency is evident when analysing the SBH



(a)



(b)

Figure 7.2: a) the I-V-T plots of the 300 nm, n-type Ge layer grown at 500 ^{o}C on n-type SiC (Repeated from Figure 4.5) and b) the extracted ideality factors and SBH values plotted against temperature.

and ideality factor values of Figure 7.2(b), where η decreases and $\Phi^0_{B,n}$ increases with increasing temperature over the range tested. At 25^{o}C, the ideality factor of this device was 1.145 proving that it is a contact of good quality. Φ_{IV} at 25^{o}C is 1.056 eV.

Plotting the barrier heights against their respective ideality factors as shown in Figure 7.3 displays the linear correlation between the two. Extrapolating a linear fit of the data to $\eta = 1$ reveals the theoretical barrier height of an ideal diode, $\Phi_{\eta=1}$. As such this should represent a maximum SBH in the region of Φ_0, representing an ideal interface with no SBH fluctuation. Indeed, when Schmitsdorf et al [69] first reported this relationship, they referred to the ideal barrier height as the homogeneous barrier height. Extrapolation to $\eta = 1$ in Figure 7.3 provides an ideal barrier height of $\Phi_{\eta=1} = 1.163$ eV. Analysing the data in Figure 7.3, the technique appears to break down when the temperature rises above 100^{o}C and the diodes appear to reach an ideality factor minimum and a SBH maximum.

Introduced in Section 4.3.1.2, another technique used to extract information about the barrier height is the Richardson plot, with $\ln(J_s/T^2)$ plotted against the inverse temperature, where $J_s = I_s/A$. Figure 7.4 shows the Richardson plot for the Ge/SiC heterojunction diode where ϕ_{Rich} was found to be 1.069 eV. Unfortunately, this SBH represents little more than average of the individual SBH values extracted from Figure 7.2(b) as this technique does not consider the temperature dependence of the SBH. The weakness of this technique is further revealed when one considers that the Richardson constant A^{**} extracted from the Y-intercept of Figure 7.4 was 50.368 $Acm^{-2}K^{-2}$. This is approximately one third that of the calculated figure [124] of 146 $Acm^{-2}K^{-2}$, though the method for calculating this value has been disputed [125].

Whilst seemingly meaningless now, the Richardson plot does have a role to play. However, it must be modified to remove the non-linearity. It is therefore necessary to

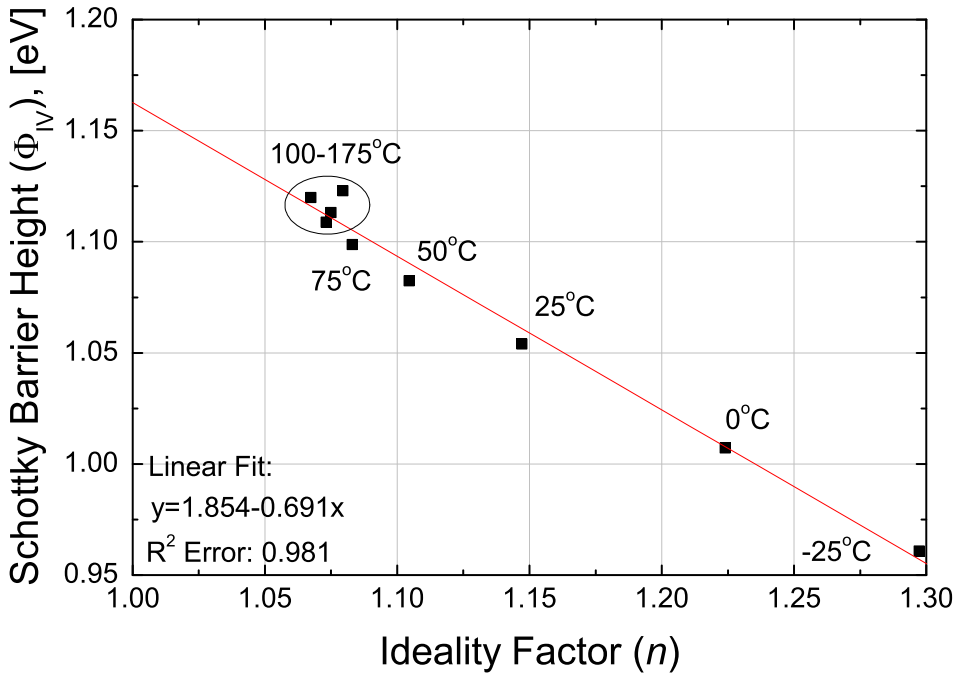


Figure 7.3: With the barrier height plotted against the ideality factor, the extrapolation to $\eta = 1$ via a linear fit gave the ideal barrier height $\Phi_{\eta=1} = 1.163$.

use the techniques presented in Sections 7.2.3 and 7.2.4 to facilitate the extraction of temperature independent values, taking into account the patches of low SBH hidden amongst the mean values.

7.2.3 The Extraction of the Effective Barrier Height

This method of extracting the SBH presumes that within an inhomogeneous contact, the distribution of low SBH patches that contribute to I-V analysis can be represented by one common SBH, Φ_{eff}, and that all the current passing through the device does so only over these patches. The value Φ_{eff} is representative of the SBH whenever the diode is being used in any practical situation.

Considering the interface represented in Figure 7.1b, a Gaussian distribution of SBH

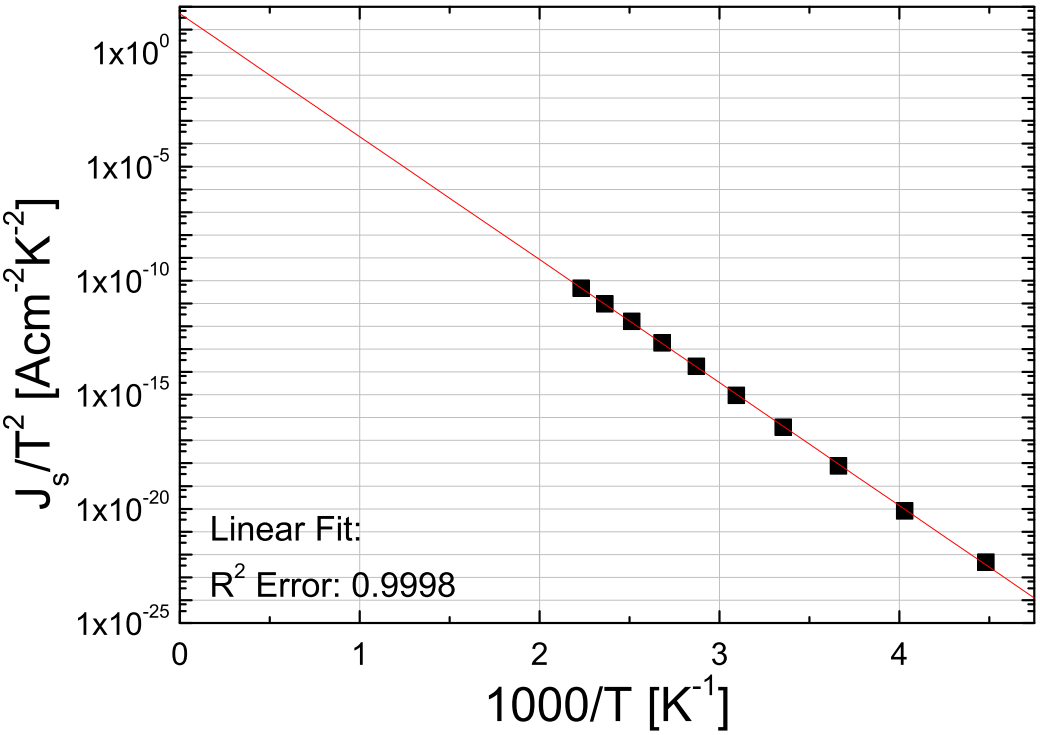


Figure 7.4: An unmodified Richardson plot, $\ln(J_s/T^2)$ vs $1000/T$. A SBH, ϕ_{Rich}, of 1.069 eV was extracted from the slope of the linear fit, which also produced a Richardson constant of 50.368 $Acm^{-2}K^{-2}$ from the Y-intercept.

values around Φ_0 will mean that there are a lot of patches with a SBH approximately equal to Φ_0, many with a little lower SBH and very few with much lower SBHs. As carriers pass over this interface, they are naturally seeking the path of least resistance and hence the patches with the lowest barriers are used preferentially. Using this logic, a simulation technique was designed that involves replacing A and $\Phi_{b,n}$ in the thermionic emission equation with modelling parameters, NA_{eff} and Φ_{eff}, such that Equation 7.1 becomes,

$$I = NA_{eff}A^{**}T^2e^{-\beta\Phi_{eff}}\left(e^{\beta V/n}-1\right). \tag{7.2}$$

Here, A_{eff} represents the average area of a patch of low SBH, and N is the number of

them in an area A. The product NA_{eff} can be represented as a percentage of the original area A, a value typically 1-5%. Φ_{eff} is an effective SBH, a value that is lower than Φ_0, but remains an average value of the lowest SBH values that are relevant to I-V analysis. These parameters, shown graphically in Figure 7.5, are refined until they produce an accurate fit to the experimental data. After a good fit is achieved, a Richardson Plot based on Equation 7.2 is used to further refine the Φ_{eff}. Using this technique, the Richardson plot becomes linear as only one temperature independent SBH value was used, which leads to the extraction of an accurate value of A^{**}. This technique is based on work by Roccaforte et al [104], which in turn is based on Tung's model [100–102].

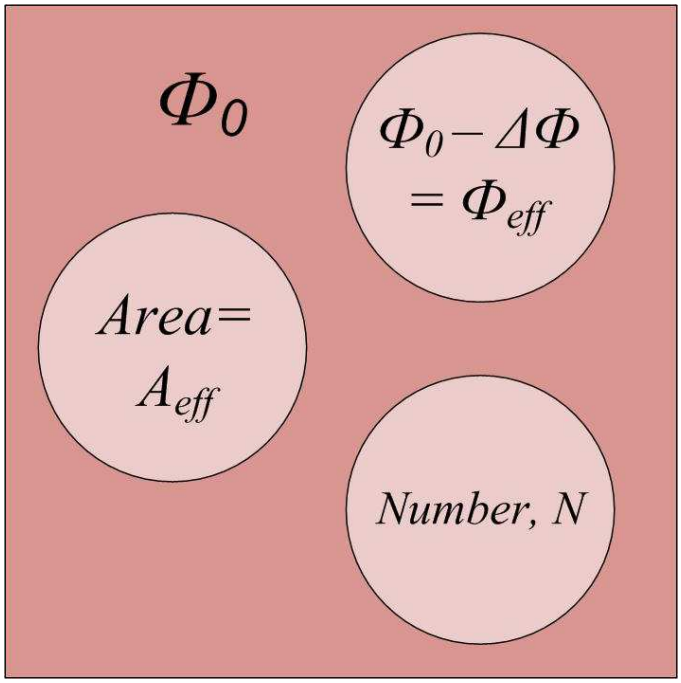


Figure 7.5: The interface as it is modelled, employing a number (N) of patches with average area A_{eff} and average barrier height Φ_{eff}.

According to Tung [100, 101], the parameter A_{eff} is determinable knowing value of

Φ_{eff}, being defined as

$$A_{eff} = \frac{4\pi\gamma}{9\beta\psi_{bb}} \left(\Phi_B^0 - \Phi_{eff}\right) \tag{7.3}$$

where ψ_{bb} refers to the total band bending brought about by the built-in potential (ψ_{bi}) and the applied voltage V_A and $\gamma = K_s/qN_D$.

With A_{eff} joining the ranks of constants from Equation 7.2, three parameters remain that can be used to manipulate a theoretical fit of the IVT data, namely N, Φ_{eff} and η. Figure 7.6 shows graphically how altering each of these variables affects these plots. Increasing the number of low SBH patches, N, allows more current to pass through the device for the same voltage and hence the fits move upwards. Increasing the SBH, Φ_{eff}, causes a reduction in the current flowing over the barrier, hence a vertical drop in the fits; however, being an exponential term, all the temperature fits also spread out away from each other. Increasing the ideality factor, η, causes the resistance of the device to increase, thus decreasing the gradient of the slope.

Figure 7.6 shows that selecting the correct balance of the variables N, Φ_{eff} and η, provides a very good approximation to the linear fits of the experimental data. The values of η used were those extracted from each individual I-V plot, as was illustrated in Figure 7.2. Once the fit is close to being correct the values of Φ_{eff} and N are used within a modified Richardson Plot, which further refines these values producing a tighter fit. The modified Richardson plot is achieved by rearranging Equation 7.2 to,

$$\ln\left(\frac{J_s}{T^2 N A_{eff}}\right) = \ln\left(A^{**}\right) - \frac{q\Phi_{eff}}{kT}. \tag{7.4}$$

The combination of the fitting process and the modified Richardson Plot facilitates a closed loop system that hones in on a value of N and Φ_{eff}, that produces both a very tight fit to the experimental data, and a linear Richardson plot that produces an accurate

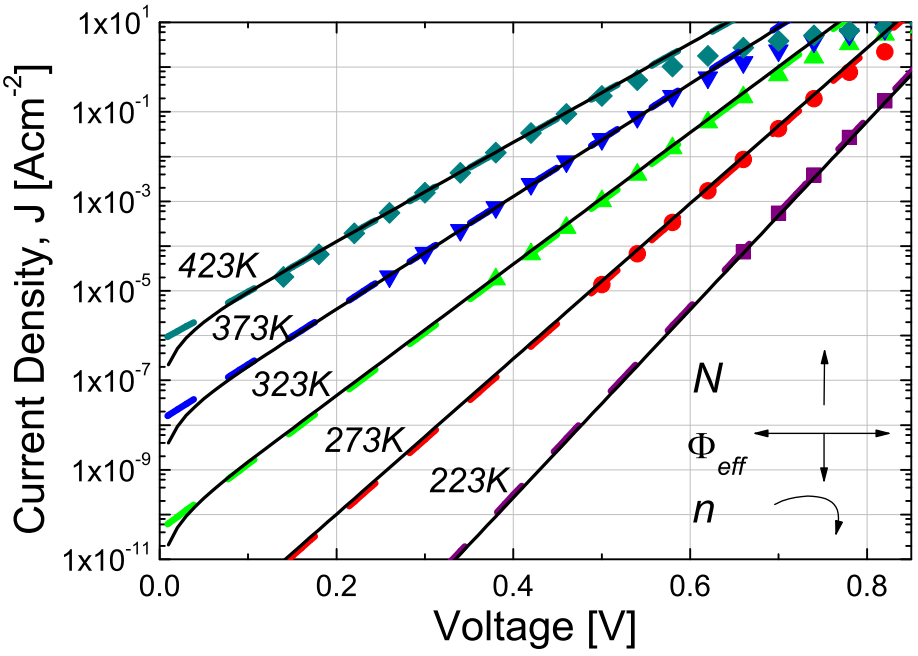


Figure 7.6: A graphical indication of how a theoretical model based on Equation 7.2 can be used to simulate experimental data. The scattered shapes are experimental data extracted from IVT measurements. The dashed lines are linear fits of the experimental data extrapolated to Y=0. The solid black lines are the theoretical fits from Equation 7.2. The effect of altering the parameters N, Φ_{eff} and η in Equation 7.2 are also shown.

value of $A**$.

Using this method on the p-type, 500^{o}C Ge/SiC diode, Φ_{eff} was found to be 1.028 eV and N was 1.1×10^7. As a result, at 25^{o}C, A_{eff} was found to be 2.9×10^{-9} cm^2 and the product NA_{eff} represented 3.2% of the total area A. The resulting modified Richardson Plot can be seen in Figure 7.7. The Richardson constant extracted was 142.3 $Acm^{-2}K^{-2}$.

The list of fitting parameters and results for all the diodes may be found in Table 7.1; however η and A_{eff} are not included as they were temperature dependent values. The ideality factors, though described as a variable above, were fixed to their experimentally

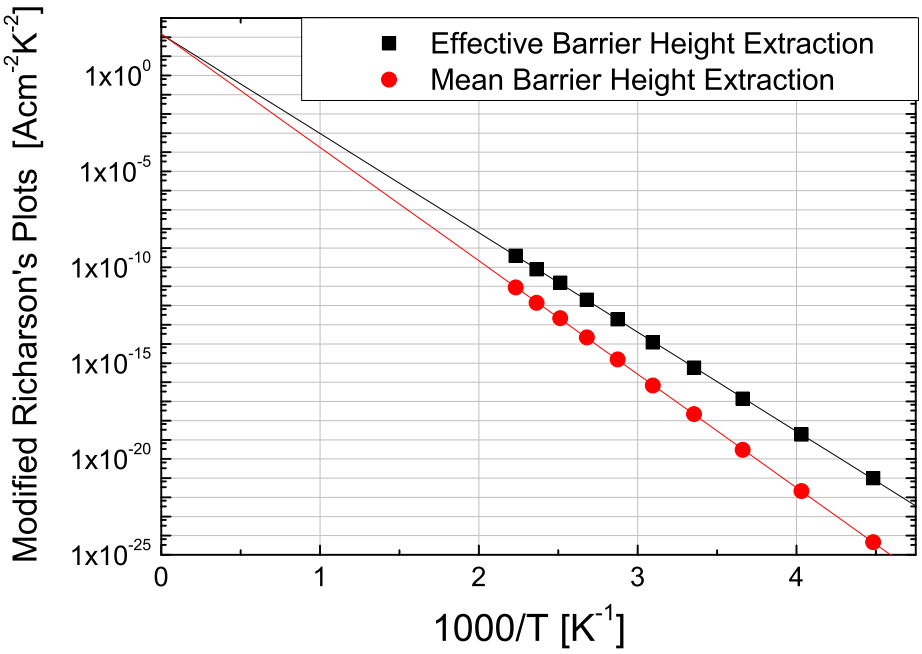


Figure 7.7: The modified Richardson plots for the extraction of the effective SBH, Φ_{eff}, and the Mean SBH, Φ_0. The y-axis represents respectively, $\ln\left(J_s/T^2NA_{eff}\right)$ and $\ln\left(J_s/T^2\right) - 0.5\beta^2\sigma^2$ vs $1000/T$. An effective barrier height of 1.028 eV and a mean barrier height of 1.174 eV were extracted.

extracted values. A_{eff} for each diode and temperature can be calculated from Equation 7.3. The technique was only carried out on those diodes with very ideal behaviour because the equations, such as Equation 7.2, are based on the diode equation, which holds true only for thermionic emission. At η >1.15, fitting via this technique became inaccurate.

The diodes tested all produced good fits, resulting in Φ_{eff} values lower than the experimental results over a fraction of the area. The verification of the values came in the form of the Richardson Constant, all of which produced values within experimental error of the 146 $\mathrm{Acm^{-2}K^{-2}}$

Dopant	n	p	p	i
Dep. Temp. (^{o}C)	500	200	500	500
Thickness (nm)	300	300	300	500
Φ_{IV} (eV) @ 25^{o}C	**1.099**	**1.056**	**1.118**	**1.069**
N	5.1e7	5.7e6	1.1e7	4.0e6
A^{**} (Acm^{-2}K^{-2})	140.8	148.4	142.3	144.6
A/NA_{eff} @ 25^{o}C	8%	1.3%	3.2%	1.4%
Φ_{eff} (eV)	**1.033**	**1.012**	**1.028**	**0.928**
A^{**} (Acm^{-2}K^{-2})	142.8	130.1	147.2	150.5
σ (eV)	0.0385	0.0846	0.0534	0.0649
Φ_0 (eV)	**1.126**	**1.254**	**1.174**	**1.121**

Table 7.1: Properties of the Ge/SiC heterojunction diodes extracted via basic I-V analysis (Φ_{IV}), the graphical fitting method (Φ_{eff}) and the statistical fitting method (Φ_0).

7.2.4 The extraction of the mean barrier height

This technique uses Gaussian statistics to relate experimental values of SBH extracted from I-V analysis, back to a mean SBH, Φ_0. A value for the standard deviation of the SBH over the entire interface is extracted from the experimental data before this is used to modify the Richardson plot. Φ_0 is analogous to the SBH extracted from C-V analysis [103, 114], that is, an average of the barrier heights over the entire contact, with no SBH of any size contributing any more than any other. This is a method first described in the paper by Song et al [114] and further built on by Werner and Güttler [103].

The amount of patches ($\mathrm{d}n$) that will have SBH values falling between Φ_0, and the value of SBH measured from the individual I-V curves $\Phi_{B,n}$, has a Gaussian distribution given by [103, 114],

$$\mathrm{d}n = \frac{N}{\sigma\sqrt{2\pi}} \exp\left[-\frac{\left(\Phi_0 - \Phi_{IV}\right)^2}{2\sigma^2}\right] \mathrm{d}\Phi_0. \tag{7.5}$$

where σ is the standard deviation of the distribution and N the total number of patches in the area A. Song et al [114] show that the total forward current can be given by merging Equations 7.1 and 7.5, and integrating, giving

$$I = AA^{**}T^2 e^{-\beta\Phi_{IV}+0.5\beta^2\sigma^2}\left(e^{\beta V/n}-1\right). \tag{7.6}$$

The thermionic emission equation for current over the a barrier of mean SBH Φ_0 is

$$I = AA^{**}T^2 e^{-\beta\Phi_0}\left(e^{\beta V/n}-1\right). \tag{7.7}$$

Combining Equations 7.6 and 7.7 and rearranging leaves

$$\Phi_{IV} = \Phi_0 - \frac{\beta\sigma^2}{2}. \tag{7.8}$$

This allows the values of SBH measured from the I-V analysis to be plotted against the inverse thermal energy, to extract σ and Φ_0. This is shown in Figure 7.8 where the p-type, 500^{o}C Ge/SiC diode was found to have a σ of 0.0534 eV. The value of Φ_0 extracted was 1.176 eV. Verification of this value can be carried out using a Richardson plot after Equation 7.6 has been rearranged to

$$\ln\left(\frac{J_s}{T^2}\right) - \left(\frac{\beta^2\sigma^2}{2}\right) = \ln\left(A^{**}\right) - \frac{q\Phi_0}{kT}. \tag{7.9}$$

Figure 7.7 shows the resulting Richardson Plot where Φ_0 was found to be 1.174 eV and A^{**} was 147.2 $Acm^{-2}K^{-2}$.

The results from this statistical technique are summarised in Table 7.1 along with the other techniques. All the values were found to have Φ_0 greater than the experimental val-

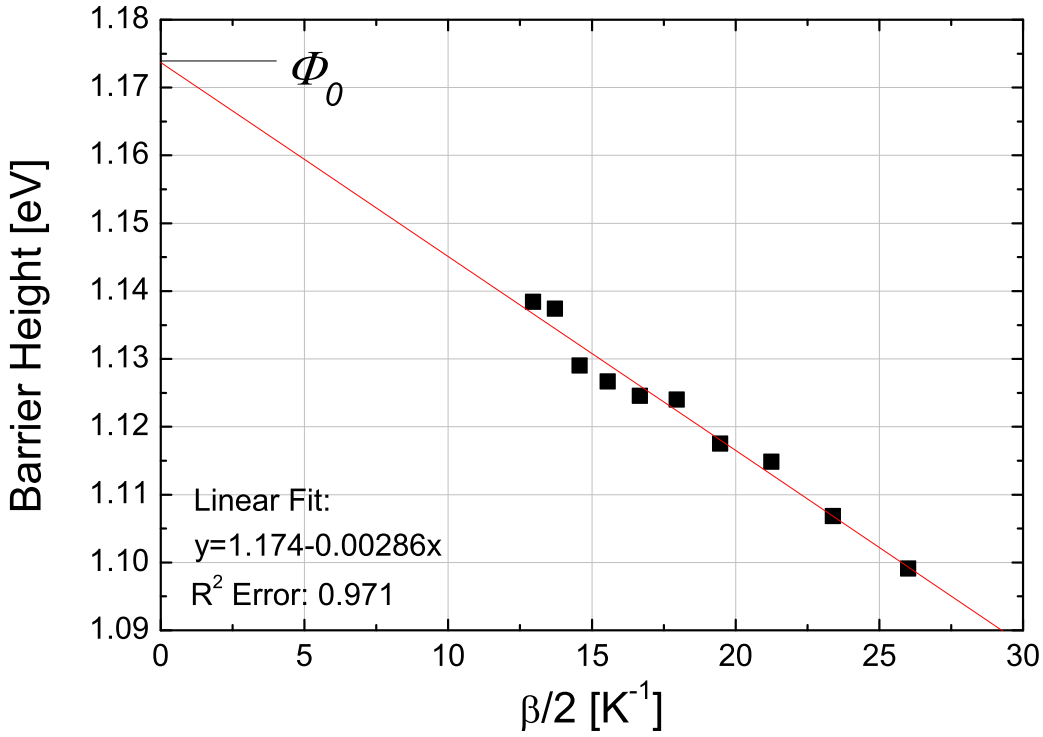


Figure 7.8: The barrier heights extracted from I-V analysis plotted against the inverse thermal energy. Φ_0 is 1.147 eV and σ is 0.0534 eV.

ues, as expected. Interestingly, the one low temperature diode tested produces the greatest standard deviation suggesting its interface, which will have the greatest number of grain boundaries, might also have the greatest array of SBH values. As before, the Richardson Constants produced were within close proximity to SiC's reported 146 $Acm^{-2}K^{-2}$ value.

7.2.5 A comparison of the results

The various analysis techniques have produced an array of data that was summarised in Table 7.1. The results for the p-type, 500^{o}C Ge/SiC diode have been further analysed graphically in Figure 7.9, where the effective area relevant to the two featured techniques is plotted against the SBH. As well as the two SBH values from the techniques above,

included in this plot are the experimental I-V and C-V values, Φ_{IV} and Φ_{CV}, and the ideal barrier height $\Phi_{\eta=1}$. This final value is representative of a SBH from an ideal ($\eta = 1$), homogeneous diode [69] and as such, one would expect a uniform barrier height over the interface, with no patches of low, or high SBH. As such, the value of $\Phi_{\eta=1}$ should be close to the mean background SBH and also represent a theoretical SBH maximum for the diode in question. Reassuringly, the value of Φ_0 extracted from the Gaussian technique is very close to $\Phi_{\eta=1}$, somewhat validating the technique. With the exception of the consistently erroneous Φ_{CV}, all the SBH values fall beneath $\Phi_{\eta=1}$. As expected, the effective barrier height, Φ_{eff} a product of only 3% of the total contact area produces the lowest SBH at 1.033 eV due to the current transport over only the lowest barriers. Φ_{eff} can be considered the most relevant of the SBH values as it demonstrates what happens when the diode is being used in its day-to-day application. This was demonstrated in Figure 7.6, where Φ_{eff} was employed to produce an accurate fit to the experimental IVT data.

The theory [103,114] indicates that the values of Φ_{CV} and Φ_0 values should be very as the statistical measures employed in calculating the mean SBH should compensate for the patches of low SBH. However, the SBH extracted from C-V analysis was 1.38 eV, a value much higher than the relatively consistent values of Φ_0 and $\Phi_{\eta=1}$. This does not help corroborate this analysis but is in itself a reflection on the weakness of the C-V analysis as it was described in Section 6.3.1.2.

Having presented all the techniques, a single obvious question remains: Which technique is right?! Quite simply they all are (perhaps with the exception of Φ_{CV}), and one needs to consider very carefully the reason they need the value and the mechanisms in use. If building a current voltage model Φ_{IV} is perfectly valid, provided that it is not used at any other temperature than the one it was extracted. If temperature is to be used in

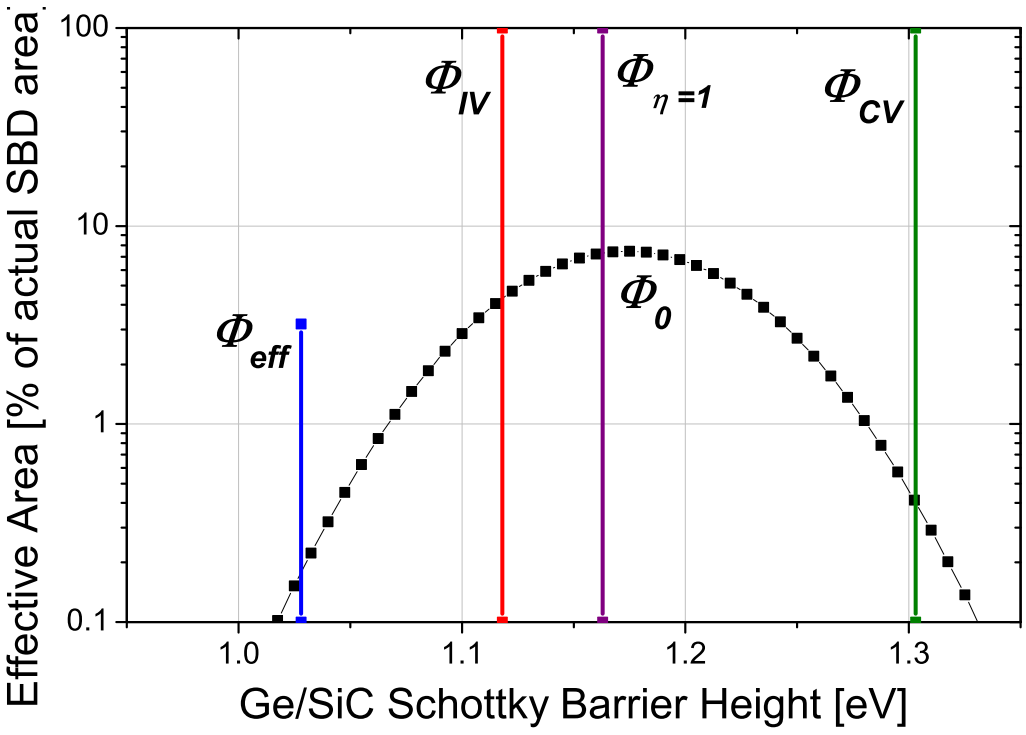


Figure 7.9: A comparison of the SBH extraction techniques, showing the effective area percentage that each barrier height occupies within the total area A.

the model then it should be altered to use Φ_{eff} and NA_{eff}, ensuring that the diodes in question are ideal. If they aren't ideal, then a similar modification as the one presented in Section 7.2.3 would need to be carried out on the current transport mechanism in question, be it from TFE, FE, or recombination/generation. Of course for a model not concerned with the direct transport of current over the boundary, then Φ_0 is the most relevant. This is the only one that gives a realistic picture of the interface due to its statistical distribution, above and below the mean value; however it has little relevance to the practical situation most diodes are used in.

One interesting experiment which must go down as future work will be to confirm the variation of the barrier height at the Ge/SiC interface through the use of conducting-AFM, which could give a 2-dimensional map of barrier heights across the surface. Similar was done to confirm fluctuations at the Au/SiC interface [119].

7.3 Fermi Level Pinning

Fermi level pinning is a subject that has attracted a lot of research in the determination of M-S SBH behaviour [70,111–113]. Here, the same techniques are applied to the degenerate Ge/SiC interface. The presence of interface traps at the surface was suggested by the non-linear nature of the C-V data in Section 6.3.1.2. Further evidence that the Fermi levels were pinned originated in the I-V analysis of the heterojunction diodes, in Section 6.3.2.2, where one peculiarity was the absolute size of the SBHs (approximately 1.1 eV). This value is clearly too large to support a theory based on the classic Schottky-Mott principal [97, 98], which states that the vacuum levels will align, leaving the electron affinities to dictate the offset. With n-type doping in both semiconductors, and nearly equal electron affinities, the Ge-SiC offset would be closer to 0.1 eV under this principal.

Hence, this Section details the idea that the Fermi level has been pinned at the surface of the SiC.

Within the Appendix, Sections A.3 and A.5 introduce the basics of semiconductor-semiconductor and metal-semiconductor interfaces, including a review of the Schottky-Mott principle. This states that the vacuum levels of different materials will align, with the conduction and valence bands bending from their bulk positions to align the Fermi levels. As a result, for any given semiconductor $S_\phi = 1$, given that the slope parameter is given by

$$S_\phi = \frac{d\Phi^0_{B,n}}{d\Phi_M}. \tag{7.10}$$

However, in tests carried out in 1939, Schweikert showed that $S_\phi = 0.08$ for Selenium Schottky contacts, having characterised many different metals [112]. Eight years later, Bardeen [126] proposed that surface states with an energy inside the bandgap of the semiconductor were responsible for this very weak correlation.

In practice, the Schottky-Mott principle only holds true only under very specific and ideal conditions due to the presence of the semiconductor surface that does not behave in the same fashion as the bulk. This affects the alignment of the bands prior to Fermi level alignment and hence affects the Schottky barrier height.

The surface of a semiconductor can be seen as an abrupt end to the uniform bulk crystal lattice structure, giving way to the atmosphere or another material, be it insulating or conducting. As such, electronic states unique to the semiconductor surface exist originating from the rearrangement of surface atoms that minimise dangling bonds. Other sources of surface states include inhomogeneities, surface imperfections such as surface roughness, non-uniform doping or imperfect surface preparation leading to an unclean surface or an interfacial oxide. Surface states can exist at any given energy including

within the bandgap of the semiconductor and here they will be treated as uniform across the entire bandgap surface. To maintain the balance of the charge within the surface and the space charge region, surface band bending occurs, effectively pinning the semiconductor Fermi level to an energetically neutral point at the surface.

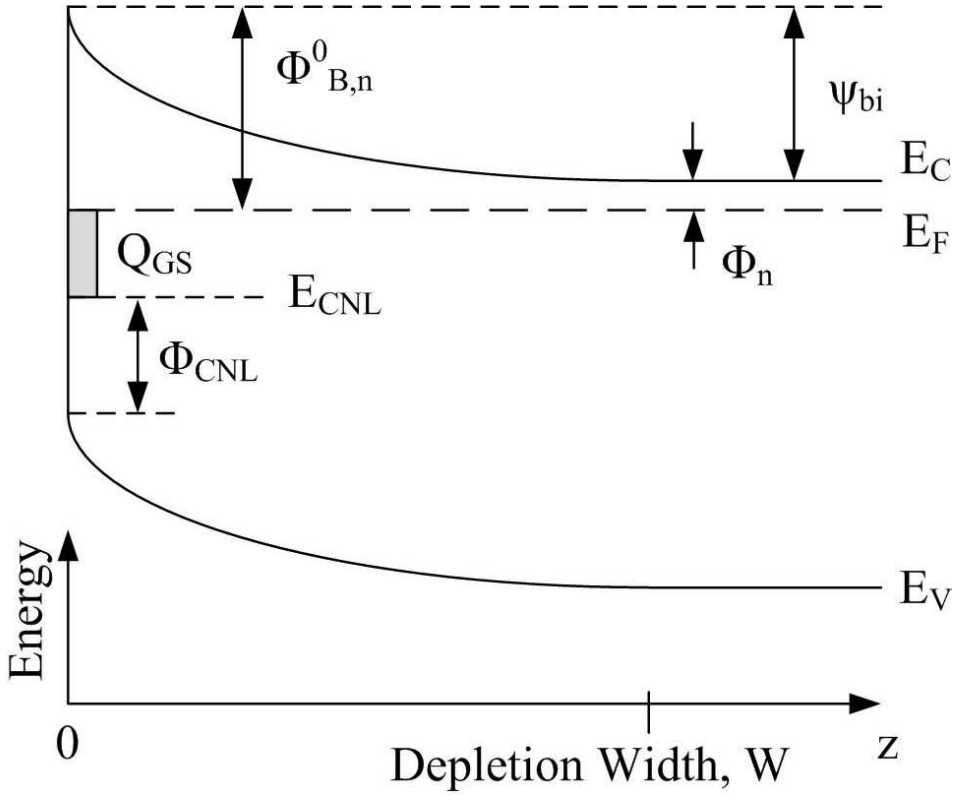


Figure 7.10: A band diagram of a semiconductor experiencing Fermi level pinning due to the existence of surface states. Reproduced from [70]

Charge neutrality occurs when the conduction band is devoid of charge and the valence band filled. Any state (be it interfacial, surface or defect) that exists within the bandgap will add to the overall charge by being there [111]. By occupying a state in the bandgap close to the valence band, a very small negative charge is added. If it is not filled it contributes a large positive charge. The opposite is true near the conduction band. The

charge neutrality level (E_{CNL}), an intrinsic property of the semiconductor in question, indicates the point at which the influence on that charge from valence and conduction bands is equal, where occupation of the state would contribute the same negative charge as positive charge from it being empty.

The bulk Fermi level (E_F) should not be confused with E_{CNL}. E_F indicates the point within the bandgap where filled surface states give way to empty ones - the point at which there is a 50% chance of occupancy. If E_F does not coincide with E_{CNL} then a net charge will exist at the semiconductor surface. If E_F is closer to the conduction band than E_{CNL} then there will be an excess of electrons and a net negative charge; this is the case in Fig. 7.10. If the Fermi level is closer to the valence band then a net positive charge will exist. This net charge (Q_{GS}) can be defined as [70],

$$Q_{GS} = qD_{GS}\left(\Phi^0_{B,n} + \phi_{CNL} - E_G\right) \tag{7.11}$$

where D_{GS} is the density of surface states, $\Phi^0_{B,n}$ is the SBH, E_G is the bandgap energy and ϕ_{CNL} is the energy difference between the valence band and E_{CNL}. ϕ_{CNL} (also known as the branch point energy) of SiC and Ge are reported [112, 113] as 1.44 and -0.28 eV respectively. At the surface, the Fermi level will align with E_{CNL}, if there is no charge from within the space-charge region (Q_{SC}) that requires neutralising. The charge in the space-charge region is given as [70],

$$Q_{SC} = \sqrt{2\varepsilon_s N_D q\left(\Phi^0_{B,n} - \Phi_n\right)} \tag{7.12}$$

where $\Phi_n = E_C - E_F$. In practically all real semiconductors, $Q_{SC} \neq 0$ and there will necessarily be some deviation of the surface Fermi level from the CNL to maintain charge

neutrality. This interdependency leads to the combination of Eq. 7.11 and 7.12,

$$Q_{SC} + Q_{GS} = qD_{GS}\left(\Phi^0_{B,n} + \phi_{CNL} - E_G\right) + \sqrt{2\varepsilon_s N_D q\left(\Phi^0_{B,n} - \Phi_n\right)} = 0. \tag{7.13}$$

A rearrangement of Equation 7.13 allows D_{GS} to be plotted against $\Phi^0_{B,n}$, which can be simply modelled in Matlab. Figure 7.11 is an example of this for moderately n-doped SiC and degenerately n-doped Ge. The Figure shows us that the Fermi level at the surface of the semiconductor will be pinned at the CNL when D_{GS} is large, resulting in the situation seen in Figure 7.10. As D_{GS} tends to 0, the surface Fermi levels return to the their bulk positions, and the Schottky-Mott principle will once more prevail.

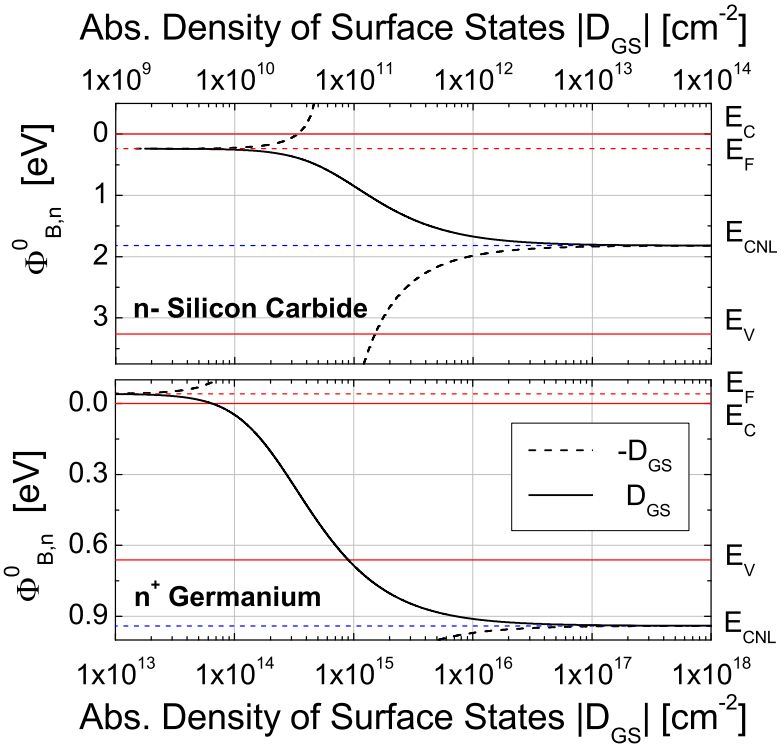


Figure 7.11: A plot of D_{GS} against $\Phi^0_{B,n}$, as extracted from Equation 7.13 for moderately n-doped SiC and degenerately n-doped Ge. This shows how a metal may be pinned to the CNL rather than the Fermi level.

Despite evidence in the literature [127] of Ge being pinned by Ni and other metals, the doping of the Ge ($N_{A,Ge} = 5 \times 10^{19} cm^{-3}$) is so great that the amount of surface states ($|D_{GS}| > 1e14$ cm^{-2}) required to move the Fermi level from its bulk position are greater than the amount required to completely pin the SiC Fermi level at E_{CNL}. Therefore, it is here presumed that the Ge remains unpinned at its bulk position, helping to justify the assumption that the degenerate Ge acts as a metal in these devices.

Of course in light of the last Section, it is difficult to say what the precise SBH of any one contact is, making the precise determination of D_{GS} and $\Phi^0_{B,n}$ from this technique impossible. However, taking the effective SBH of the polycrystalline diodes, 1.028 eV, and assuming that the Ge acts as a metal, then reading from Figure 7.11, this equates to a surface state density of $D_{GS,SiC} = 2.3 \times 10^{11}\ cm^{-2}$.

Figure 7.11 and the above calculations can be used to explain the size of the SBH of the heterojunction interfaces. Undoubtedly, the charge neutrality level is causing the Ge to be pinned to a point within the SiC bandgap. However, the absolute values attained must be treated only as estimates due to the assumptions made. The value of $\phi_{CNL} = 1.44\ eV$ for the bulk material of SiC is essential to determining where the Fermi level is pinned. The source of this figure [112, 113] seems somewhat hazy, with the specific SiC polytype on which this is based not mentioned.

Fermi level pinning affects the surface of most semiconductors and explains many experimental irregularities. As regards the validity of the Schottky-Mott principle, a first approximation of how materials will energetically align is essential. For this purpose, and for initial device design, it must continue to be used due to the complexity of predicting the affects of the surface states. In practice however, the only way to attain a valid idea of the SBH between materials, is via experimental and analytical means.

7.4 Fermi Pinning and the Experimental Results

A final mystery may be addressed in light of the Fermi level pinning discussions. In Section 6.3.2.2, the lack of difference between n-type and p-type layers was discussed, with both layers having a SBH extracted by conventional I-V characterisation of 1.1 eV, an ideality factor < 1.05, and their turn-on voltages were separated by just 40 meV. The amount of voltage require to turn on a device is determined by the height of the built-in potential (ψ_{bi}), therefore, given this evidence $\psi_{bi,pN}$ must be very similar to $\psi_{bi,nN}$. In light of all this it appears that the doping has of the Ge has no effect, but that just cannot be the case. The potential shift of the Ge Fermi level from one doping extreme to the other must impact on a device as no physical model can allow the conduction and valence bands, and the Fermi levels from the Ge to remain in the same position in the SiC bandgap regardless of doping. The implications of these results will be discussed here in light of the Fermi pinning models built up in this Chapter. Given a full understanding of the results, and by revisiting the experimental results a thorough picture is built up of how the Ge/SiC interface forms and behaves.

7.4.1 Defining the heterojunction SBH

Until now, the heterojunction diodes have been treated exactly as metal-semiconductor diodes and as a result, the exact relevance of the SBH has been missed. To understand the formation of the heterojunction interface one must define the SBH in energetic terms and disassociate it from the conduction band offset when referring to heterojunction devices.

Having painstakingly defined the exact value and nature of the SBH in this Chapter, it does appear backwards to only now be defining its meaning within a heterojunction. However, it is only now that its exact relevance is seen. In a metal-semiconductor contact

the very obvious definition of the SBH is the potential between the metal work function and the semiconductor's conduction band. Electrons sitting in an energy state equal to the metal Fermi level must gain so many eV of energy before it can pass into the SiC. When transposing this to the semiconductor-semiconductor contact, it is easy to assume that the SBH is equal to the conduction band offset because we most often consider free electrons, those that already occupy an energy equal to that of the conduction band already. However, the conduction band electrons are not the 'average' electrons, most often these are the exception rather than the rule (though not in our degenerate n-type case). Therefore, the SBH can be described as the amount of energy that the *average* electron requires to be promoted from the narrow-bandgap semiconductor into the wide-bandgap semiconductor. We can therefore define the heterojunction SBH as follows:

$$\Phi^0_{B,n} = E_{C,WB} - E_{F,NB}, \tag{7.14}$$

where $E_{C,WB}$ is the conduction band energy of the wide bandgap material prior to equilibrium, the SiC in our case. $E_{F,NB}$ is the Fermi level of the narrow-bandgap material, our Ge. This definition is shown in Figure 7.12c and d, distinguishing it from the conduction band offset (ΔE_C) and the built-in potential (ψ_{bi}).

7.4.2 The Pinning Model

A model referred to here as the "Pinning Model" is proposed to explain the experimental results seen in Section 6.3.2.2, using the Fermi pinning theory introduced in Section 7.3 and the rigorous SBH definition.

Given the low doping of the SiC and the presence of surface states it is likely that the SiC surface is pinned prior to alignment as in Figure 7.10. Due to its degenerate doping,

Figure 7.11 suggested that the Ge would not be pinned unless the density of surface states was extremely high, hence the first presumption of the Pinning Model is that the SiC is pinned to a point in its bandgap prior to intimate contact, whilst the Ge is not. This is shown in Figure 7.12a and b.

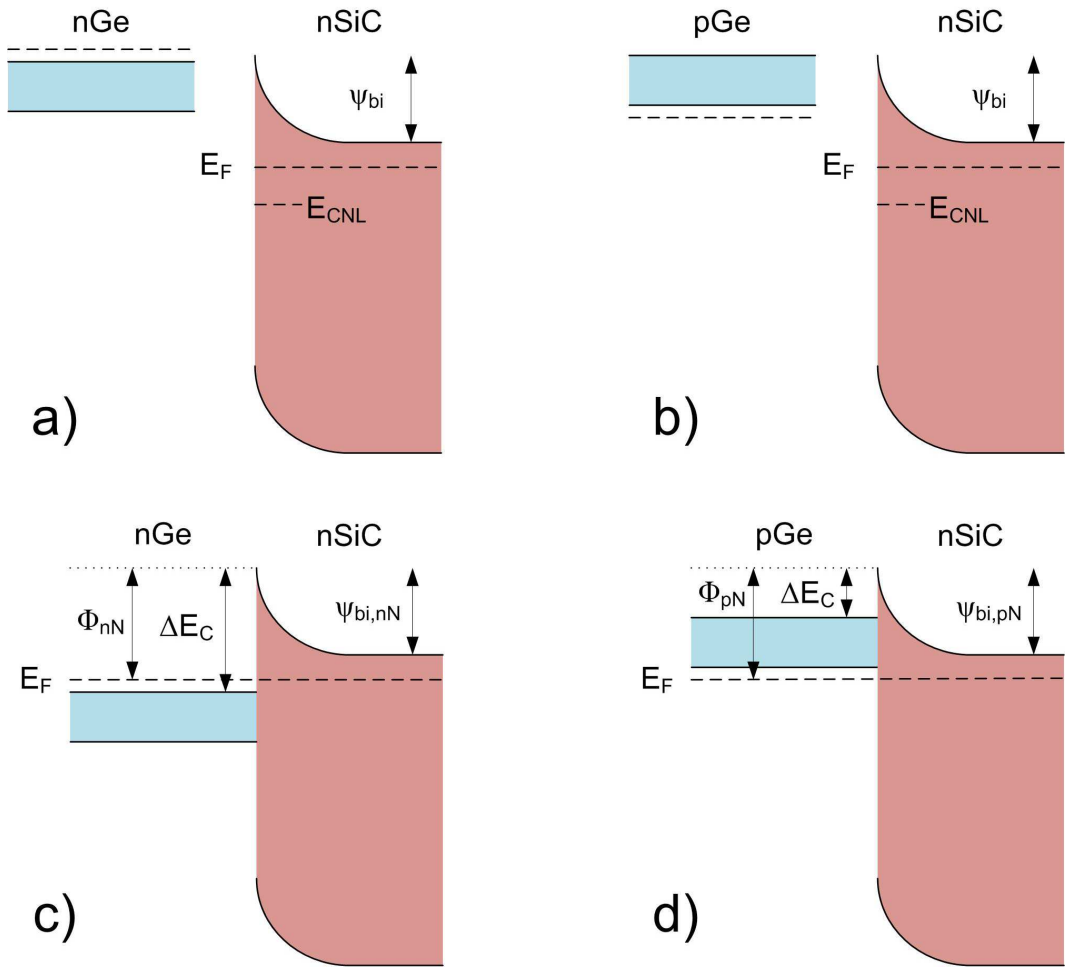


Figure 7.12: Band diagrams representing the n-type and p-type Ge layers prior to (a) and c)) and after (b) and d)) alignment with the Fermi pinned SiC.

Disregarding the Schottky-Mott principle of band alignment due to the overwhelming evidence of surface states at the interface, the second presumption in this Model is that the Ge and SiC Fermi levels will line up, as shown in Figure 7.12c and d, such that the Ge

valence and conduction bands can be in such vastly different positions. This is something of a leap of faith as one naturally thinks the reverse to be true, that the huge degenerate doping of the Ge should render its position fixed, leaving the lightly doped SiC to move its bands into alignment with the Ge. However, that traditional model does not work for these diodes, leading to vast mismatches in the built-in potential. No statement is made here about whether the Ge bands bend to get into this energetic position within the SiC bandgap, as this does not effect the model - if Ge band bending does occur, then the huge doping will render the barriers invisible to the carriers as they are easily tunneled through.

The result of the Pinning Model is shown in Figure 7.12c and d labelled with all the important characteristics. The Fermi level of each Ge structure aligns at the same point in the SiC bandgap, which leads to identical SBHs and ψ_{bi}s, explaining their near identical forward characteristics. However, it would be impossible for all the parameters to remain the same, and it is clear from Figure 7.12 that the one parameter in the Pinning Model that alters is the conduction band offset (δE_C). δE_C is the barrier that controls leakage current, so an opportunity arises to prove whether this model holds true, by comparing the n-N and p-N diode leakage currents.

Figure 7.13 provides the evidence needed. The current-voltage-temperature (IVT) tests used of Figure 7.2 were carried out on the 500^{o}C p-type and n-type Ge/SiC heterojunction diodes, and the reverse leakage results are presented in Figure 7.13. For any one temperature the leakage from the p-type diode was approximately double that of the n-type diode. Given the exact situation in Figure 7.12c and d, δE_C could be expected to be approximately 1.1 eV in the n-N case and 0.35 eV in the p-N case.

The leakage results of Figure 7.13 are an encouraging result backing up the Pinning Model theory, which can now be use to explain three of the defining characteristics of the

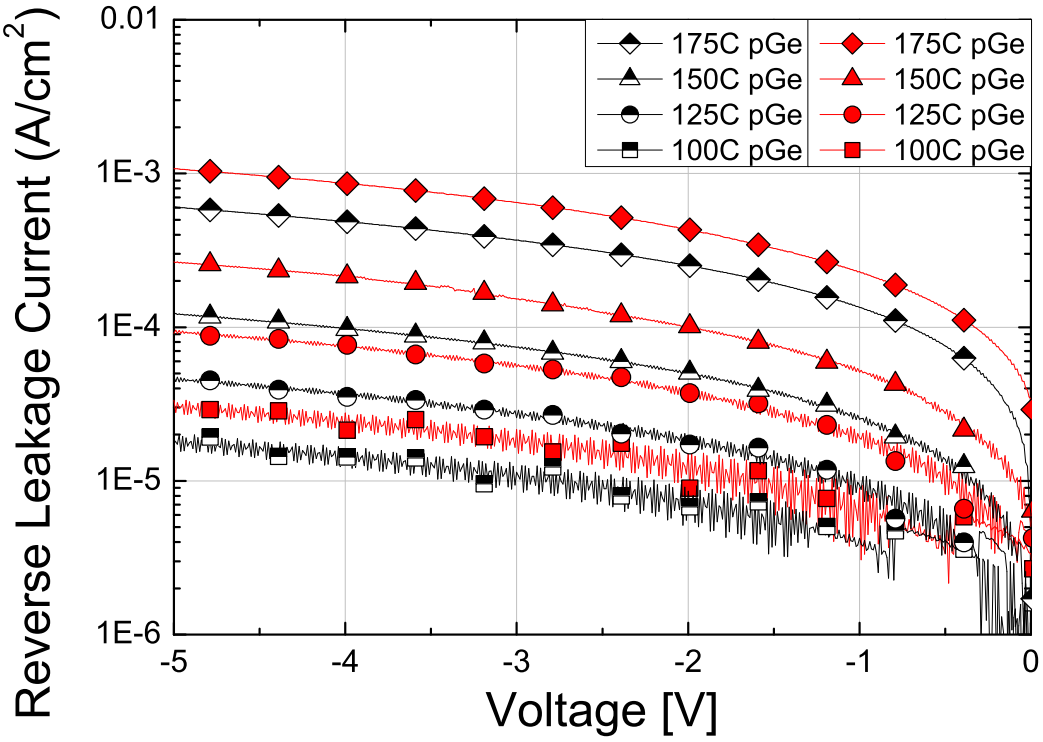


Figure 7.13: I-V-T reverse leakage results for the 500°C p-type and n-type Ge/SiC heterojunction diodes.

contacts, the SBH, the ψ_{bi} and the leakage.

7.5 Summary

This Chapter represents a fundamental overview of the heterojunction interface; introducing new characterisation methods for heterojunction diodes that culminate in a better understanding of the nature of these structures. This work was essential, providing an explanation for the first time as to why semiconductors align as they do and further explaining discrepancies in the experimental results. The common link running through this Chapter, linking SBH fluctuation analysis and Fermi Pinning is inhomogeneity at the interface, which causes surface states to occur between the semiconductors. Reduction of

these could produce smaller standard deviation distributions of the SBH and effective and experimental SBH's that are much closer to the average value. Surface state reduction may also reduce Fermi level pinning, thus allowing the semiconductors to align in a way more similar to the Schottky-Mott principle. This would accentuate the differences between p-type and n-type layers, creating dopant dependent turn-on voltages, but reducing the difference in the reverse direction. Cleaner processing, pre- and post-deposition polishing steps and even alternative deposition methods such as CVD might help to achieve this greater uniformity and homogeneity.

7.6 Conclusions

1. The variation in Ge/SiC Schottky barrier heights between measurement methods suggested that the inhomogeneous interface had a large distribution of barriers. In a direct I-V regime, the majority of carriers take the path of least resistance over the lowest (approximately 3%) of barriers. In a C-V measurement, this distribution of barriers is simply averaged.

2. Fermi level pinning explains why the barrier height is consistently 1.1 eV, much higher than the Schottky-Mott theory would predict. Prior to alignment with the Ge, the Fermi level of the lightly doped SiC layer is pinned mid bandgap at its surface, thanks to a large number of surface states.

3. The consistent Ge/SiC barrier height of 1.1 eV across dopant types suggests an unusual alignment of the Ge to the SiC, one where the conduction band offset between the two materials appears variable, an idea seemingly confirmed by experimental leakage results.

Chapter 8

Silicon Carbide Heterojunction MOS Characterisation

8.1 Introduction

Over the past three Chapters, the novel Ge/SiC and Si/SiC heterojunctions have been introduced, with much emphasis on understanding their complex interfaces and their physical and electrical characteristics. The use of these structures as heterojunction diodes has been proposed and the initial results were promising, with good turn-on characteristics and a forward resistance that could rival most diodes with improved processing techniques. Using this body of knowledge as a basis, this Chapter is an exploration into the feasibility of forming more advanced devices, specifically MOS transistors. The production of full heterojunction transistors is an iterative process that would require a PhD thesis and more to itself. However, the success of such a device depends largely on the quality of its oxide-semiconductor interface and specifically, the quality of the channel that forms in the region nanometers from this interface. The formation of the channel, known more formally as the depletion region due to the exodus of majority carriers from the interface, is characterised using the powerful capacitance-voltage (C-V) technique. When combined

with some parameter extraction and simulation techniques, parameters such as the density of interface traps (D_{it}), depletion region doping and voltage offset become apparent. As we will see in Section 8.5.1, these parameters become interesting when the depletion region expands beyond the heterojunction interface, into the second semiconductor. At this point, the shape of the C-V curves deviate from the conventional, leading to a scenario in which some novel and exploratory modelling is used to qualify the results.

The use of a heterojunction beneath an oxide is unusual and we will see in this Chapter that it enables the use of high-K dielectrics on SiC, by adding a layer that boosts the otherwise meagre conduction band offset between the layers. Layers of Ge and Si are used as the heterojunction material here, deposited respectively by MBE and wafer bonding. The crystallinity and smoothness of a wafer bonded layer will be shown to produce an excellent blocking capability, whilst the MBE formed layers will show a superior accumulation/depletion transition.

However, in the proceeding Section, the theory behind the MOS structure and its progression from accumulation to depletion and inversion will be introduced. Following this, Section 8.3 will describe the MOS C-V technique and the simulation processes.

8.2 Metal-Insulator-Semiconductor Theory

The metal-oxide-semiconductor (MOS) interface is the key element of a lot of power switches, particularly the MOSFET and the IGBT. To simplify matters, we are here only interested in the MOS capacitor, the semiconductor and metal sandwiching the insulator. Such a structure is pictured in Figure 8.1, with the band structure of each material. As in the metal-semiconductor and semiconductor-semiconductor interfaces seen in Chapter 3, the Fermi level of each material will align when they are in intimate contact and under

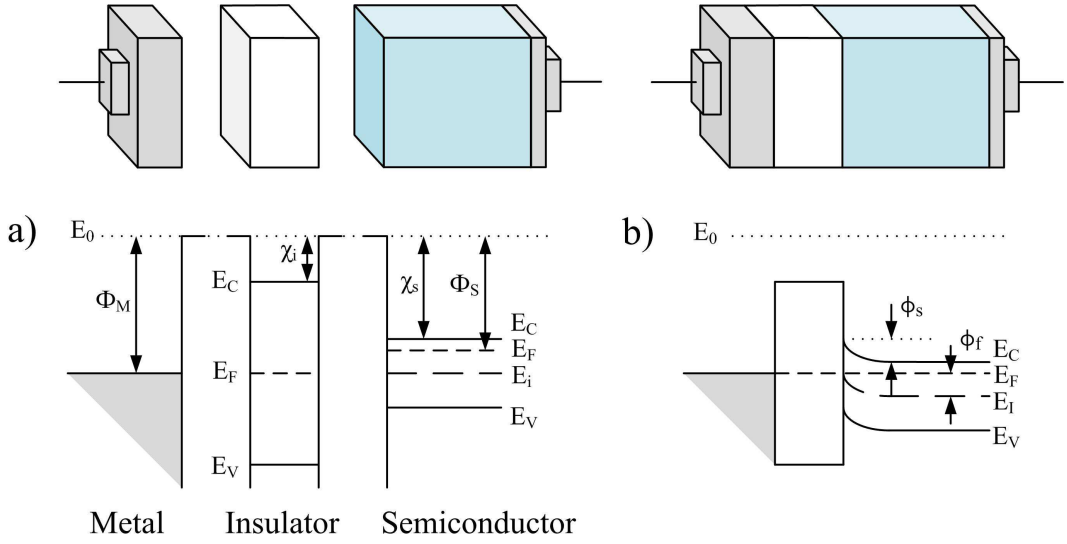


Figure 8.1: MIS structures with the band diagrams of the component parts in a) separation, and b) intimate contact.

equilibrium conditions. Any insulator used within the MOS structure will have a band structure with an associated bandgap, similar to an undoped semiconductor. The only difference is the size of the bandgap, for example 8.9 eV for SiO_2. This is the reason that these materials prevent current flow, as the barrier that forms is too large for the majority of carriers to mount. Similarly, the leakage current through the oxide is determined by the amount of carriers that manage to overcome the large barrier.

Two potentials are marked in Figure 8.1. The Fermi potential (ϕ_F) represents the energetic difference between the Fermi level and the Intrinsic Fermi level, and is attained by rearranging Equations A.2. $\phi(x)$ represents the potential between any given depth x from the surface and the bulk level as represented by the band bending. At $x = 0$, the potential represents the entire potential difference between the semiconductor surface and its bulk. This is known as the surface potential, and is represented by ϕ_S, though this is synonymous with $\phi(0)$.

The application of bias to a MOS device forces the semiconductor bands to bend

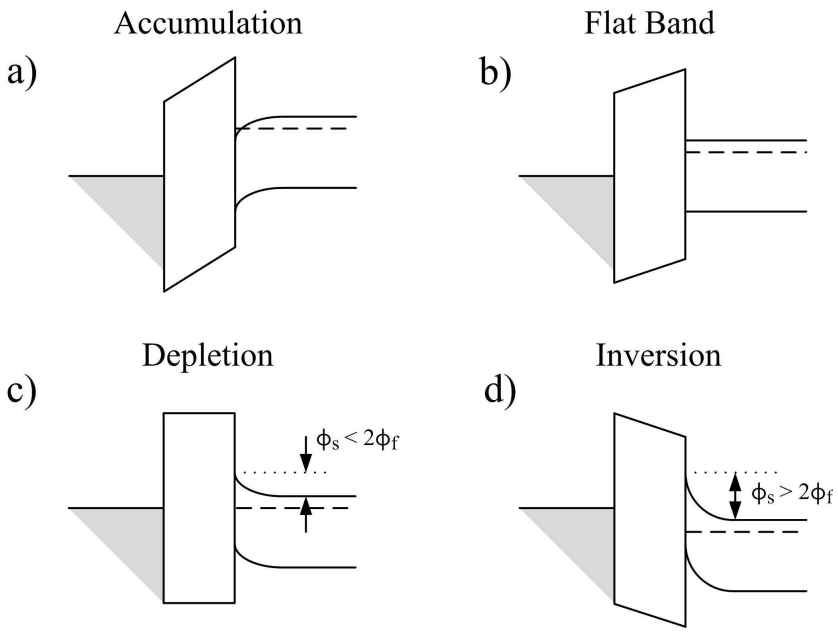


Figure 8.2: The band diagrams of a n-type MOS device under different biasing conditions.

into one of four distinct states, namely accumulation, flat band, depletion and inversion. The energy band diagrams of each of these are depicted in Figure 8.2. The example that follows relates each of these states to an applied voltage referring specifically to the example already seen in Figure 8.1b, where the semiconductor is n-type and where, in equilibrium, the bands have shifted into depletion. Beginning with Figure 8.2a, the application of a large positive voltage to the gate (the metal, in MOSFET terminology) causes the electron majority carriers within the semiconductor to accumulate at the oxide interface. This accumulation state, is used in MOSFET terms to turn the device hard off, as the channel, located beneath this oxide will be flooded with majority carriers.

Reducing the voltage leads to the flat band voltage of Figure 8.2b, whereby the potential is sufficient to overcome the intrinsic band bending of this structure. In this state, neither majority nor minority carriers are compelled towards the oxide, and the surface

of the semiconductor is in its neutral, bulk state.

This structure's unbiased state is in depletion, though this would often be the result of the application of a small negative voltage. The negative potential depletes the surface states of their majority carriers whilst beginning to attract minority carriers. Whilst $\phi_S < \phi_F$, the number of minority carriers attracted is very small, less than the intrinsic carrier concentration (n_i). Similarly, the number of minority carriers does not exceed the intentionally doped majority carriers until $\phi_S = 2\phi_F$, known as the depletion/inversion transition. As the negative voltage increases and ϕ_S exceeds $2\phi_F$, the number of minority carriers exceeds the majority carriers and the semiconductor surface could be said to have been inverted, having switched from n-type to p-type.

8.2.1 Electrostatics

Each of the states of Figure 8.2 has its own electrostatic situation that determines the profile of carriers and potential over the materials. Building up a model of these distributions allows an understanding of the application of a bias to the MOS structure for any given semiconductor/insulator combination. Such a model is the basis of another that will be used in Section 8.3 to build up an ideal capacitance-voltage plot of a MOS structure. This in turn is used as a benchmark to extract the density of interface traps at the semiconductor/insulator interface, a value that influences how much Coulomb scattering will occur in the channel of a MOS based device. Coulomb scattering is one of four mechanisms with an associated mobility that can cause the degradation of device performance. The other major mechanisms are bulk mobility, surface roughness, and phonon (or lattice) scattering; and the lowest dominates.

To simplify the process of extracting the potential distribution, the normalised poten-

tials, U U_S and U_F are employed, whereby

$$U(x) = \frac{\phi(x)}{kT/q}, \tag{8.1}$$

$$U_S = \frac{\phi_S}{kT/q}. \tag{8.2}$$

and

$$U_F = \frac{\phi_F}{kT/q}. \tag{8.3}$$

These potentials are then related to their semiconductor depth using the following equation, the derivation of which may be found in Appendix B of Pierret's Semiconductor Device Fundamentals [35]:

$$\hat{U}_S \int_U^{U_S} \frac{dU'}{F(U', U_F)} = \frac{x}{L_D}, \tag{8.4}$$

where,

$$\hat{U}_S = +1 \qquad \text{if} \quad U_S > 0 \tag{8.5a}$$

$$\hat{U}_S = -1 \qquad \text{if} \quad U_S < 0 \tag{8.5b}$$

$$F(U, U_F) = \left[e^{U_F}\left(e^{-U} + U - 1\right) + e^{-U_F}\left(e^{U} - U - 1\right)\right]^{1/2} \tag{8.6}$$

and

$$L_D = \sqrt{\frac{K_S e_0 kT}{2q^2 n_i}}. \tag{8.7}$$

L_D is the Debye Length, the distance over which carriers screen out electric fields. Implementing Equation 8.4 in Matlab allows the potential distribution extraction for a full range of surface potentials, as can be seen in Figure 8.3(c). Having established a $U(x)$

distribution, the electric field and charge density profile may be found using respectively,

$$E(x) = \hat{U}_S \frac{kT}{q} \frac{F(U(x), U_F)}{L_D} \tag{8.8}$$

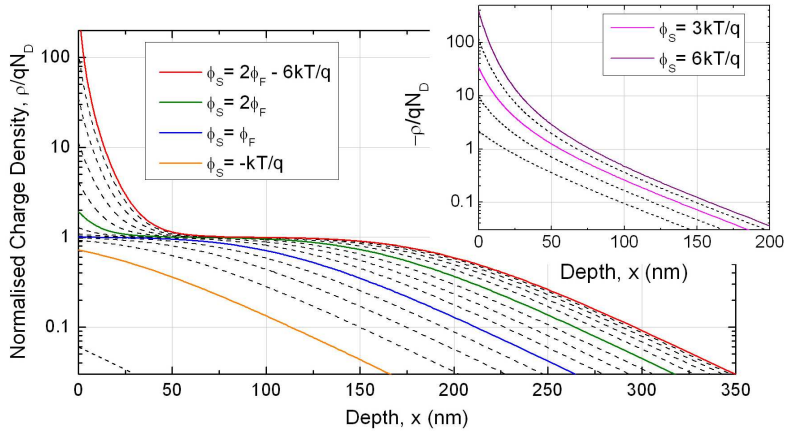
and

$$\rho(x) = qn_i \left(e^{U_F - U(x)} - e^{U(x) - U_F} + e^{-U_F} - e^{U_F} \right). \tag{8.9}$$

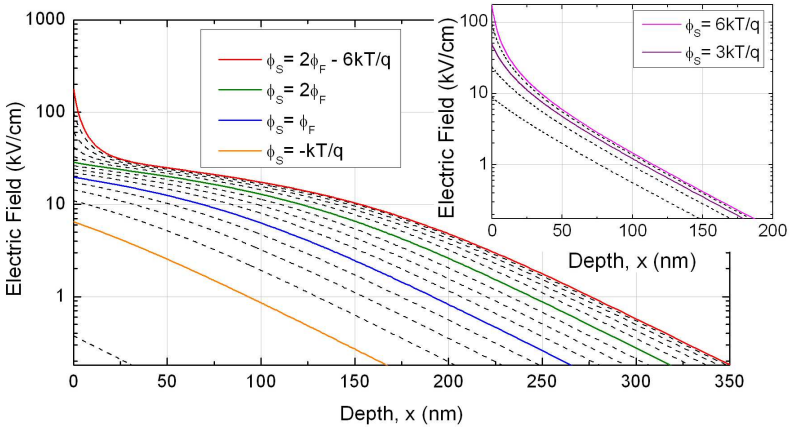
Again, these equations have been implemented in Matlab for a range of surface potentials can be seen in Figure 8.3.

The profiles of Figure 8.3 demonstrate the effects of biasing on a MOS device. This profile was based on a Ge/HfO_2 interface that will be physically tested in Section 8.5.1. The doping of the semiconductor was low at 5×10^{15} cm^{-3} and an insulator thickness of 50 nm. Presuming an intrinsic flatband scenario, where the bands remain unbent with no applied voltage, the application of even a very small positive voltage sent the semiconductor into accumulation. Under these conditions, the bands bend, trapping the majority carriers, electrons, right at the semiconductor surface. This can be seen in the inset to Figure 8.3(a), where a very narrow depletion region is formed with little spreading from the surface.

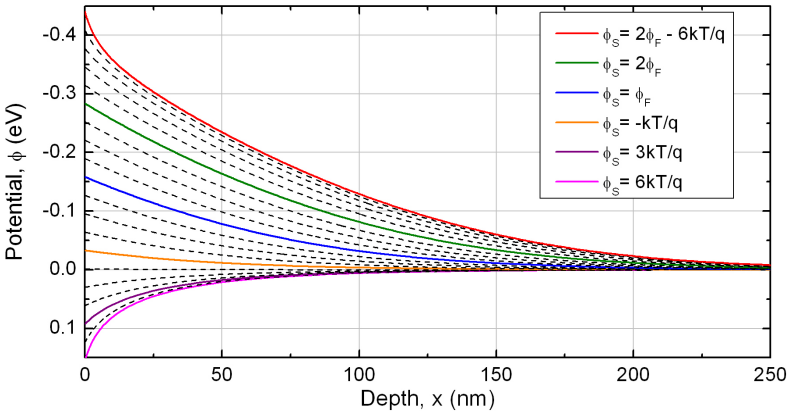
The application of a small negative voltage begins the depletion of the majority carriers, and the start of a depletion region that extends well into the semiconductor. It may be seen that the minority charge density distributions for $\phi_S < 2\phi_F$, the minority charge density profiles get no larger than the equivalent n-doping, spreading deeper into the semiconductor rather than building up at the interface. Beyond this critical value, the depletion width stops expanding and the minority carriers form as the majority carriers did in accumulation, at the interface, thus justifying the name inversion. This happens due to the large band-bending at the semiconductor surface, that effectively turns the



(a) Charge density profile.



(b) Electric field profile.



(c) Potential profile.

Figure 8.3: The charge density, electric field and potential profiles of a moderately n-doped Ge semiconductor, having a 50 nm HfO_2 insulator. The surface potentials are varied from accumulation ($\phi_S = 6kTq$), through the central depletion region ($\phi_S = \phi_F$) and the depletion/inversion transition ($\phi_S = 2\phi_F$) to inversion ($\phi_S = 2\phi_F - 6kTq$).

n-type material p-type, due to the shifting of the Fermi level to the opposite half of the bandgap.

Figure 8.3(a) shows how far the depletion region extends into the semiconductor from the surface. Under moderate negative bias, $\phi_S > \phi_F$ the semiconductor is completely depleted of carriers until around 150 nm from the surface, and bulk conditions have not been re-established 300 nm from the surface.

8.3 C-V Measurements

The C-V technique was introduced in Section 4.3.2 as a tool for extracting barrier height and doping from a Schottky interface. The downfall of this technique, as explained in Section 6.3.1.2, was that the standard equation did not take into account trapped charge at the interface. Quite on the contrary, the MOS C-V technique can be used to approximate the amount of trapped charge at the semiconductor-oxide interface, as will be revealed in Section 8.3.2. However, to begin this Section, the C-V technique pertaining specifically to MOS structures will be introduced, building up a picture of the capacitance in such a structure as the semiconductor passes from accumulation through to inversion. As before, capacitance measurements are taken using the Agilent Technologies B1500A Semiconductor Device Analyser, using the full range of its frequencies, from 1 kHz to 1 MHz. This time however, the analyser is used in conjunction with a mercury probe, preventing us from needing to process metal contacts upon the oxide surface. Instead, a vacuum formed at the oxide surface allows an 819 μm diameter dot of mercury to form. Being a liquid at room temperature, mercury forms a reasonable contact with the oxide, forming the metal in the MOS setup.

A MOS structure may be perceived as two capacitances in series. The first, the oxide

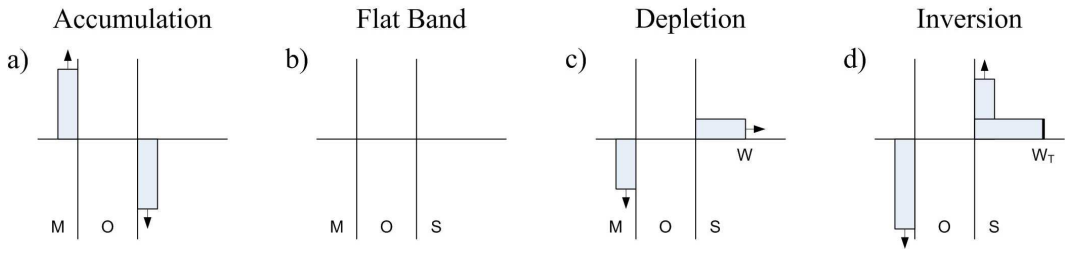


Figure 8.4: The charge distribution of a n-type MOS device under different biasing conditions

capacitance, is defined by its thickness (x_o) and dielectric constant (K_O) as follows:

$$C_{Ox} = \frac{K_O \varepsilon_0 A}{x_o}, \tag{8.10}$$

This is is an ever-present capacitance which does not vary with applied voltage. The second capacitance; however, is formed in the semiconductor region directly beneath the oxide and is determined by the width of the depletion region (W) such that,

$$C_S = \frac{K_S \varepsilon_0 A}{W}. \tag{8.11}$$

The depletion region is devoid of majority carriers, leaving only ionised dopants and hence the dielectric of this second capacitor, is the dielectric constant (K_S) of the semiconductor. The width of the depletion region, and hence its capacitance is determined by the amount of bias applied to the gate. This can be described qualitatively by considering the build up of charge each side of the oxide as shown in Figure 8.4, where the four biasing conditions correspond accordingly with the four band diagrams of Figure 8.2. It is worth reiterating here that the C-V technique comprises of a D.C. sweep through the required voltage range, onto which is imposed a small A.C. signal that slightly alters the charge balance each side of the capacitor. The arrows in Figure 8.2 show the impact of this charge variation at the

different biases.

Under strong accumulation conditions, where a positive voltage is placed upon the gate, the majority carriers (electrons in this case) gather at the oxide-semiconductor interface, resulting in no depletion region capacitance, hence,

$$C_{Acc} = C_{Ox}. \tag{8.12}$$

Applying an increasingly negative bias begins the formation of a depletion region, where the ionised donors spreading through the semiconductor balance the negative charge on the gate. Hence, under negative bias the two capacitances exist and are in series, meaning,

$$C_{Depl} = \frac{C_{Ox}C_S}{C_{Ox} + C_S}. \tag{8.13}$$

At small biases the capacitance of C_S is very large and hence $C_{Depl} \rightarrow C_{Ox}$. As the depletion width expands, the capacitance of C_S decreases, gradually reducing C_{Depl}. This may be seen in Figure 8.5, where a Si substrate with 200 nm of SiO_2 is used to demonstrate the total capacitance as a proportion of C_{Ox}. Increasing the reverse bias further pushes the semiconductor interface into inversion, with the build up of a large amount of minority carriers. Figure 8.4d shows that in inversion the depletion width stops expanding at its maximum width W_T, whilst any further bias increase adds only to the minority carrier build up.

In inversion, the depletion region has reached its maximum at W_T and it can expand no further, hence the charge must build up elsewhere. Figure 8.4d, shows two frequency dependent situations. At lower frequencies (1 kHz), the time varying signal is approximately a succession of D.C. states and there is sufficient time to generate or annihilate

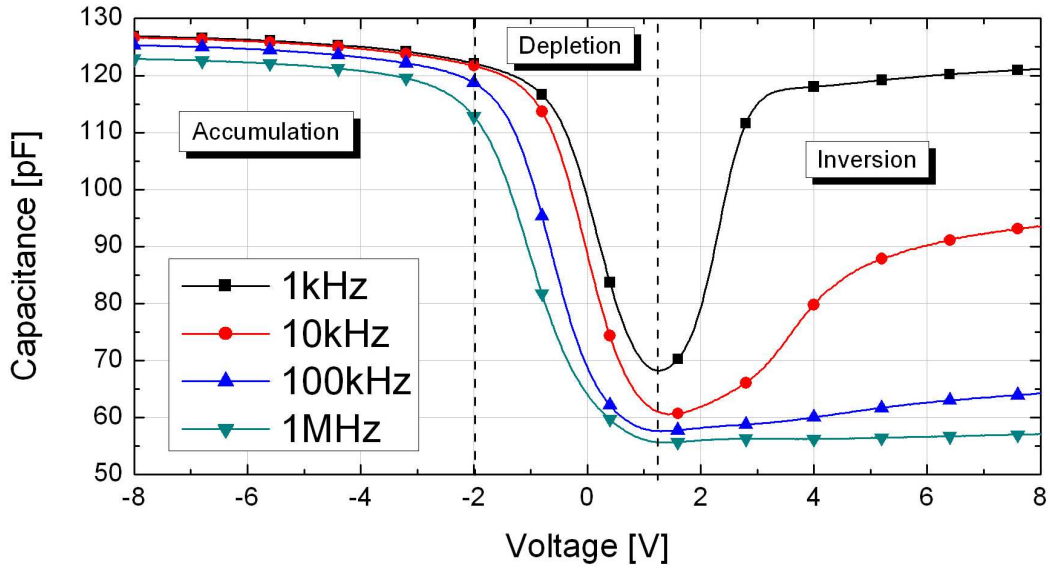


Figure 8.5: The C-V response of a p-type Si substrate with 200 nm of SiO_2, taken using a mercury probe connected to the Agilent B1500A. The small signal frequency varies from 1 kHz to 1 MHz.

minority carriers [35]. Hence, the increase in charge occurs within the inversion region next to the oxide interface, with minority carriers building up then dissipating with the alternating frequency. This greatly increases the capacitance within this layer, meaning that the capacitance once more tends to C_{Ox}. This capacitance increase is shown in Figure 8.5. At higher frequencies, there is not enough time for the recombination/generation process to occur, and hence the charge fluctuations occur around the depletion width maxima, W_T. With W_T at its limit, and the charge in the inversion region unable to respond to the C-V signal, the capacitance appears fixed at its minimum value. Hence, it follows that [35],

$$C_{Inv} \simeq C_{Ox} \quad \text{for } \omega \to 0 \tag{8.14a}$$

$$C_{Inv} = \frac{C_{Ox}C_S}{C_{Ox}+C_S} = \frac{C_{Ox}}{1+\dfrac{K_O W_T}{K_S x_o}} \quad \text{for } \omega \to \infty \tag{8.14b}$$

Another practical effect of frequency is seen in Figure 8.5, where, at high frequencies, the resistance of the semiconductor bulk comes into play, reducing the observed capacitance [35].

8.3.1 C-V Modelling

A theoretical C-V plot may be modelled using a set of equations that follow on from the derivation of the electrostatics in Section 8.2.1, using the same normalised potentials U_S and U_F to develop an associated gate voltage and capacitance. Further details of the technique and a full derivation appears in [35, 65, 128].

The total capacitance of a MOS structure was given in Equation 8.14b, where the total capacitance in a layer is determined by the depletion width W_T. From the discussions of Section 8.3, we know that this is a complex quantity, the whole nature of which changes depending on measurement frequency. For low frequency measurements, regardless of whether the semiconductor is depleted or in accumulation,

$$W_{eff} = \hat{U}_S L_D \left[\frac{2F(U_S, U_F)}{e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right)} \right] \tag{8.15}$$

This Equation holds true for high frequency measurements also, whilst the semiconductor is in accumulation. However, when it is depleted,

$$W_{eff} = \hat{U}_S L_D \left[\frac{2F(U_S, U_F)}{e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right)/\left(1 + \Delta\right)} \right] \tag{8.16}$$

where,

$$\Delta = \frac{\left(e^{U_S} - U_S - 1\right)/F(U_S, U_F)}{\displaystyle\int_{0^+}^{U_S} \frac{e^{U_F}\left(1 - e^{U}\right)\left(e^{U} - U - 1\right)}{2F^3(U, U_F)} dU} \tag{8.17}$$

The gate voltage, V_G is also calculated as a product of the surface potential, as given by,

$$V_G = \frac{kT}{q}\left[U_S + \hat{U}_S \frac{K_S x_o}{K_O L_D} F(U_S, U_F)\right]. \tag{8.18}$$

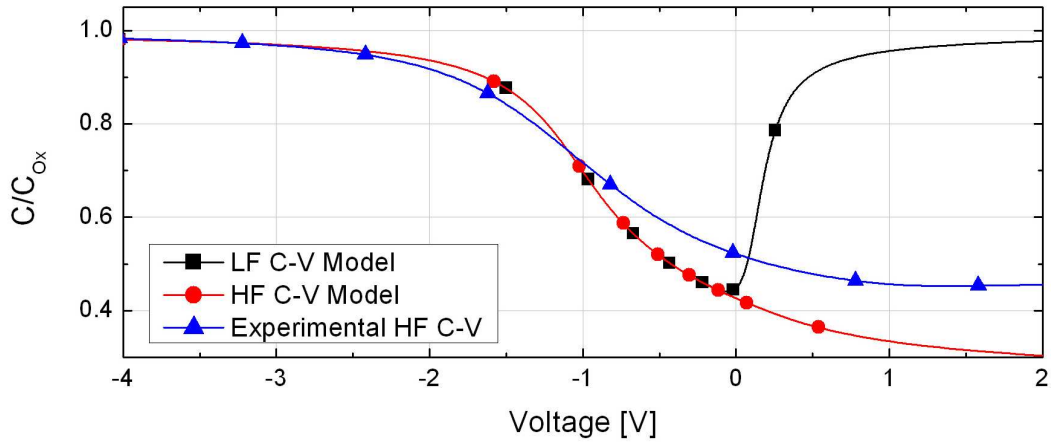


Figure 8.6: The theoretical and experimental curves for a Si/SiO_2 MOS interface, showing the spreading that occurs in the practical situation due to interface traps.

Implementing Equations 8.15 8.16 and 8.18 in MatLab produce the two theoretical C-V_G curves of Figure 8.6, where the low frequency curve can be seen characteristically returning to the oxide capacitance C_{Ox}, whilst the high frequency curve continues to diminish. The MOS structure modelled was the Si/SiO_2 layer, the experimental results of which were previously shown in Figure 8.5. This high frequency experimental curve is also shown in this plot, and the fit is not encouraging. However, the reason for the discrepancy is not down to the accuracy of the model. As we will see in the following Section, the influence of interface states must still be taken into account.

8.3.2 Trapped Charge and the Modelling of Real MOS devices

The scenario described above to build up the electrostatic picture and the C-V curves may be viewed as the ideal scenario, with the only charge contributing to the MOS capacitance coming at either side of the oxide, exclusively due to the application of a potential across the structure. In reality there exists at least three charge centres within the oxide region that can have an effect on the conventional C-V curves. Mobile ions, fixed charges and interface traps will be expanded on below and Figure 8.7 shows their location within an oxide-semiconductor interface.

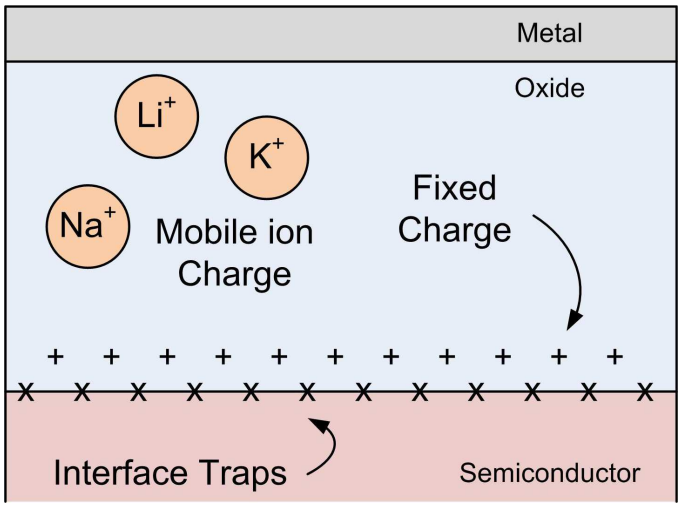


Figure 8.7: A MOS interface with three charge centres depicted.

Mobile ions caught within the oxide layer can cause havoc with the capacitance in a MOS structure, causing apparently random shifts in the D.C. offset of a C-V curve with temperature and biasing. Normally consisting of positive ions of sodium, lithium or potassium, these unwanted contaminants left over from processing are free to move within the oxide layer, building up at either the metal-oxide or the oxide-semiconductor interface depending on the bias and temperature. The distribution of the ions within the

oxide affects the amount of voltage shift that will occur, the effect being more pronounced when the charge is situated at the oxide-semiconductor interface [65]. The mobility of the ions is proportional to temperature and hence density of these charges is measured by comparing the flat band shift after the device has been left under the extremes of biasing for 5-10 minutes at temperatures above 150^oC (in Si/SiO_2 technologies). Mobile charge densities are minimised by introducing into the oxide chemicals such as calcium of phosphorous that neutralise the mobile charge. A mobile charge concentration in the range of $5 \times 10^9 - 10^{10}$ cm^{-2} is considered acceptable in integrated circuits [65].

Fixed charges are a more predictable, and repeatable cause of voltage shift that were revealed after scientists in the 1960's managed to isolate and eliminate mobile ions from their processing [35]. Situated at the oxide-semiconductor interface, these charges produce a voltage shift that is repeatable for a given material, irrespective of fabrication conditions, oxide thickness, or the type or concentration of doping. These experimentally conceived facts suggest that the origin of this fixed charge must be right at the oxide-semiconductor interface, and indeed tests on Si/SiO_2 have shown that a monolayer of SiO_x, where $x < 2$, exists at the interface [35]. This represents a layer that was left in limbo, being the next Si monolayer that would have been formed into oxide when the process was halted. The amount of fixed charge is minimised through annealing the oxide in an inert atmosphere and via the use of the semiconductor faces that produce the least charges.

Interfacial traps (a.k.a. surface states) are the most troublesome of the charge centres, degrading channel mobility and stretching out the accumulation/depletion C-V curve, meaning that a greater voltage is required to turn a MOS-based device hard-on or hard-off. We have already introduced the source of these traps in Section 7.3, where the same "Surface States" were causing the semiconductor surface to become pinned at the material's Charge Neutrality Level. The list of inhomogeneities that cause these unwanted

states, or traps, included poor surface preparation leaving a rough or unclean finish and a non-uniform doping profile. At the MOS interface, another source of inhomogeneity is dangling bonds, where the oxide molecule does not bond with every semiconductor atom, leaving charge centres at the interface.

The density of interface traps (D_{it}) is a value that may be estimated using a number of different methods, based on the C-V techniques and the ability of charge centres to respond to a quickly fluctuating A.C. signal. The effect of interface states on a C-V curve is shown in Figure 8.6, where an experimental Si/SiO_2 C-V response is compared to a theoretical version of the same structure. One can see the spreading of the practical C-V response as a result of the charge centres at the interface that will make result in a bigger voltage range between device turn on and turn off.

The larger problem concerned with a large D_{it}, is the effect that this has on the channel region directly beneath it. The charge centres sitting directly at the oxide-semiconductor interface cause a significant decrease in the channel mobility, as they obstruct the path of the passing electrons or holes. This scattering is the major region why Si/SiO_2 channels must be reduced to the $10^9 - 10^{10}$ $cm^{-2}eV^{-1}$ range, a feat achieved through a post-deposition anneal in hydrogen, which terminates some of the unsatisfied dangling bonds at the interface. This problem is not so easily solved in SiC however. The presence of the carbon and Si at the interface means that there is a more complicated structure that is required than in the Si/SiO_2 example, where Si atoms could simply give way to its natural oxide. The result in the SiC/SiO_2 example, is one where many dangling carbon bonds remain unsatisfied, and novel nitric oxide or nitrous oxide anneals fail to bring the D_{it} below the state-of-the-art $10^{11} - 10^{12}$ $cm^{-2}eV^{-1}$ range [129].

For this reason, alternatives have been sought to overcome the SiC/SiO_2 problem, and this is one of the large motivating factors behind the Ge/SiC and especially the Si/SiC

heterojunction work. If a good transition from single crystal Si to SiC could be realised, then established Si/SiO_2 techniques could be used to create a low, high mobility D_{it} Si channel, with a SiC blocking region.

8.3.3 D_{it} Modelling

Three methods exist that estimate D_{it} using C-V methods. The low-frequency method and the combined high-low frequency capacitance methods are not used in this work. This is due to the dependence of these techniques on a measurement frequency low enough that minority carriers and interface traps respond immediately. This involves a measurement frequency lower than was possible using the Agilent 1500A, whilst experimentation with quasi-static techniques that estimate capacitance using an I-V sweep, proved unsuccessful. Information on these techniques may be found in [35, 36, 65, 130].

Instead, the Terman, or high frequency, method uses only a high frequency A.C. signal, though a large amount of simulation is required. As mentioned previously, the experimental C-V response is stretched out when compared to an ideal curve due to the presence of the interface traps. Hence the high-frequency method compares the gradient of the responses as they pass from accumulation to depletion. The most thorough explanation of this technique is located in [130]; however, a brief summary of the method is provided here.

When measured at high frequency, the total capacitance in a MOS layer is modelled, regardless of bias, by the series combination of C_{Ox} and C_S, as given by Equations 8.13 and 8.14b. C_S is a product of the depletion width length and hence by the amount of band bending, ϕ_S. The stretching out of the C-V curves in the presence of interface traps occurs, because the larger the D_{it}, the more gate voltage is required to achieve the same

ϕ_S, given that [65],

$$V_G = V_{FB} + \phi_S + V_{Ox} = V_{FB} + \phi_S + Q_G/C_{Ox} \tag{8.19}$$

where the gate charge, Q_G, is given by

$$Q_G = -\left(Q_b + Q_n + Q_{it}\right) \tag{8.20}$$

where Q_b, Q_n and Q_{it} is respectively the bulk, electron and interface state charge density.

It is therefore through the variation of the experimental ϕ_S from the ideal that provides the information required to extract D_{it}. Hence, for a given experimental C-V curve, a ϕ_S-V_G plot is constructed, using the ideal curves of Equations 8.14b and 8.16 to extract a value of ϕ_S, for every experimental C-V plot. The gradient of the ϕ_S-V_G plot is proportional to the density of interface traps given that [130],

$$D_{it} = \frac{C_{Ox}}{q}\left[\frac{dV_G}{d\phi_S} - 1\right] - \frac{C_S}{q}. \tag{8.21}$$

8.4 Oxide Deposition

The oxides in this thesis were formed via three different techniques, using either a low-pressure chemical vapour deposition (LPCVD) oxide furnace or a standard thermal oxide technique to produce SiO_2 and an atomic layer deposition (ALD) furnace to produce HfO_2.

The Tetreon Thermco 2410 LPCVD furnace uses tetraethyl orthosilicate (TEOS, $Si(OC_2H_5)_4$) as a volatile precursor, which reacts with the substrate surface, forming SiO_2 and the waste products ethylene (C_2H_4) and water. This reaction takes place at a

temperature between 650 and 750^{o}C forming a deposited oxide at a rate of 6.5 nm/minute. When comparing oxides grown on Si substrates, deposited oxides such as this are of reduced quality when compared to thermally produced oxides, as they contain a greater quantity of fixed and interfacial charge.

However, thermal techniques do not 'deposit' SiO_2, they sacrifice existing Si. Using standard furnaces at a temperature of around 1100^{o}C, pure oxygen or water vapour (dry or wet oxidation) passes over the wafer, reacting to form SiO_2. When SiC is involved this reaction also involves the large amount of carbon in the structure. As this process begins, the reaction is simple, for example, $SiC + 2O_2 \rightarrow SiO_2 + CO_2$. However, as the oxide grows thicker it becomes harder to extract the CO_2 through the existing oxide, hence large amounts of trapped charge build up [131, 132].

The Savannah-200 ALD system from Cambridge NanoTech Inc. was used to form layers of HfO_2. An ALD system works in a very similar fashion to a CVD system, except that the surface is exposed to two precursors sequentially, one after the other in two half-reactions. The use of the two precursors, kept separate within the system, allows for precise control of the layer thickness down to sub-atomic ($< 0.1\mathring{A}$) thicknesses. In the formation of HfO_2, the oxygen precursor is deionised water or ozone (O_3), and the Hafnium, precursor is tetrakis (dimethylamido)-hafnium. A nitrogen purge between precursors keeps them separate.

8.5 Analysis of Heterojunction MOS Layers

Having introduced the theory behind MOS structures and the techniques used to characterise and analyse them, presented here are the results of two heterojunction MOS devices. High and low temperature Ge MBE depositions in a HfO_2/Ge/SiC structure

are compared, whilst a wafer bonded HfO_2/Si/SiC structure is compared to HfO_2/Si, HfO_2/SiC and a HfO_2/SiO_2/SiC structure. The thickness of the HfO_2 was 40 nm in each case, formed using ALD system described previously. 12-15 nm thick SiO_2/SiC structures were formed using the standard cleans presented in Section 6.2.1, before thermal oxidation of the surface was carried out through a standard wet oxidation process lasting 2 hours at 1100 ^{o}C. The SiO_2/Si structures used as examples throughout this Chapter were formed using the LPCVD furnace.

8.5.1 MBE HfO_2/Ge/SiC MOS Device

Chapter 6 revealed the rectifying properties of the Ge/SiC layers, whilst in Chapter 7 the interfacial properties of the layers were formed. Here, the possibility of forming a MOS device using these layers as a substrate will be analysed through the addition of an oxide layer. 40 nm of the high-K dielectric HfO_2 was deposited onto the 300 nm thick amorphous and polycrystalline Ge layers. HfO_2 was chosen because of its compatibility with Ge, a semiconductor whose native oxide GeO is soluble in water, though much recent progress [133] has been made with GeO_2, with D_{it} values down around 10^{11} cm^{-2}eV^{-1}. Recent papers had shown very promising accumulation/depletion curves using HfO_2 on Si, with the oxide able to sustain up to 4 MV/cm [134, 135], though one study had claimed that the combination of HfO_2 on Ge could withstand up to 15 MV/cm with nitridation [136]. One negative of HfO_2 is its ability to sustain large peaks on voltage, as it might under surge conditions. Recent work [137] has suggested that sandwiching a thin SiO_2 layer between the SiC and the HfO_2 may improve its ability to block these voltages.

C-V and I-V analysis has been used to test whether the heterojunction structures can produce good accumulation/depletion curves and to what extent they can sustain an

electric field. The C-V and I-V results of this Section were attained using a mercury probe to form the metal-oxide contact. The C-V results were taken at a frequency of 10 kHz to minimise series resistance when extracting D_{it}.

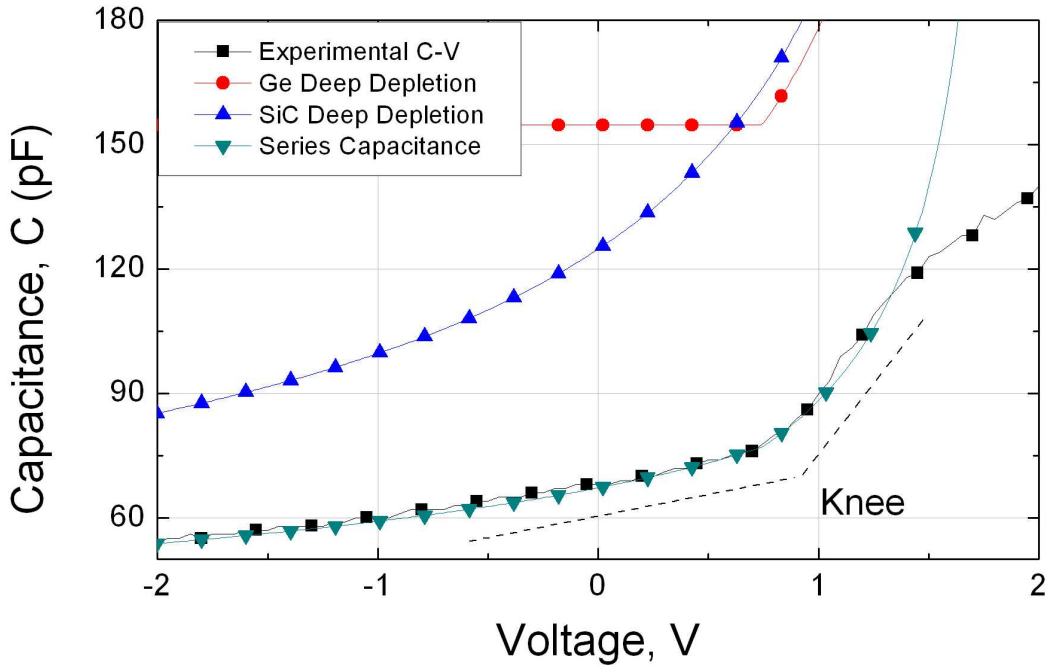


Figure 8.8: C-V results and simulations of the HfO_2/Ge/SiC MOS device containing the amorphous Ge layer.

Figure 8.8 shows the C-V results of the amorphous Ge MOS structure. The experimental data (black squares) contain a very pronounced 'knee' - a sudden change in the gradient - at 0.75 V, where one would usually expect a smooth continuous transition from depletion to inversion. A model was put together in Matlab to try and simulate this behaviour. A conventional MOS structure, as seen previously, is the series combination of the oxide capacitance and the semiconductor's depletion region capacitance. However, with two n-type semiconductors, both in close proximity to the oxide, it was predicted that the n-N heterojunction structure might be modelled by three capacitances in series,

adding the SiC depletion width capacitance (C_{SiC}) to that of the Ge layer (C_{Ge}) and the oxide, such that,

$$\frac{1}{C_{Series}} = \frac{1}{C_{Ox}} + \frac{1}{C_{Ge}} + \frac{1}{C_{SiC}}. \tag{8.22}$$

Furthermore, the Ge capacitance will clearly by limited by the thickness of the layer, meaning C_S in Equation 8.11 will be limited by a maximum depletion width, W, of 300 nm. This lead to the simulation of C_{Ge} (red circles) in Figure 8.8, created using the equations of Section 8.3.1 but with a minima of approximately 155 pF. C_{SiC} (blue triangles) was a slightly easier modelling parameter, having the full substrate thickness with which to expand, and hence its contribution is the conventional C-V curve in depletion/inversion. The contribution of C_{ox}, a constant capacitance of approximately 2.5 nF was included in the simulation but is not shown in Figure 8.8.

Using a trial and error approach to fitting the variables (doping, voltage shift, exact layer thickness in the case of the Ge), the model produced a series depletion curve (C_{Series}, green triangles) that fits rather tightly with the depletion region of the experimental results, explaining the knee in these results. A doping of 1×10^{16} cm^{-3} for the Ge layer and 1.8×10^{16} cm^{-3} for the SiC provides a very accurate fit to the data. The manufacturer stated that the SiC epitaxial layer was doped to 1.4×10^{15} cm^{-3}, and hence there is a discrepancy here, though given the simplicity of the model, and the many approximations it uses, including the constant Ge doping and the flat homogeneous interface, it seems fair to attribute this discrepancy to experimental error. A voltage shift of +1.85 V in the model suggests that the experimental layers are depleted prior to any bias being applied.

Figure 8.9 shows the C-V results of the HfO_2/Ge/SiC structures formed by high temperature deposition. Again, the Equations of Section 8.3.1, provided the tools needed to model the slope and extract information. However, the shape of the experimental

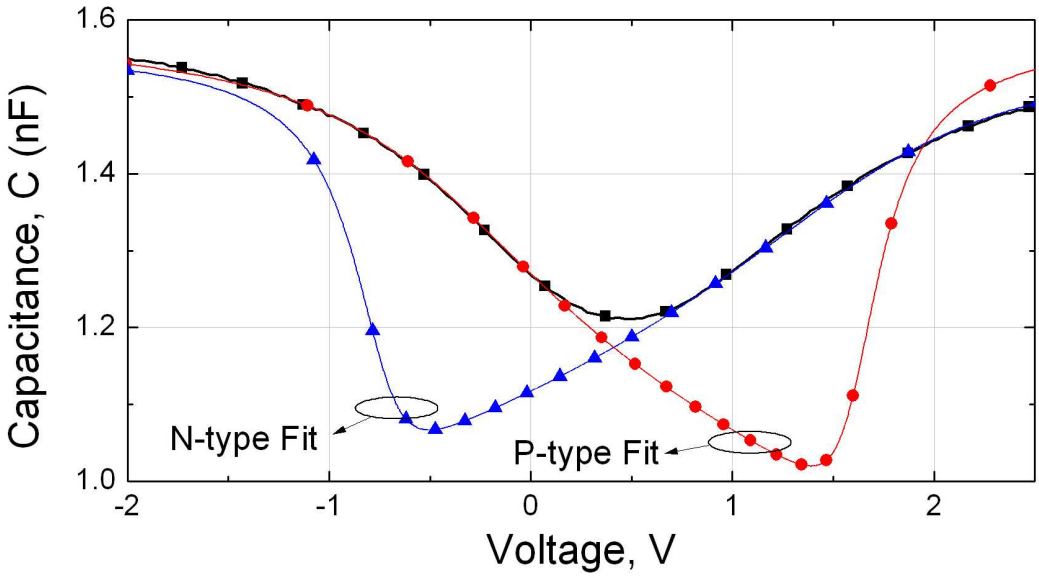


Figure 8.9: The C-V results and simulation of the HfO_2/Ge/SiC MOS device containing the polycrystalline Ge layer.

curve within Figure 8.9, is out of the ordinary, appearing as two mirrored accumulation/depletion curves with no deep depletion/inversion element. Indeed, treating the two halves of the curve as individual accumulation/depletion curves allows for p-type and n-type modelling, as shown in the Figure. Two excellent fits result, both employing a Ge doping in the region of 1×10^{18} cm^{-3}. With doping this high, the depletion region remains entirely within the Ge layer, never encroaching on the SiC. This is a strange result, consisting of an unusually high concentration of two dopant species. This may be explained by the MBE process which was notoriously leaky at the intended low doping levels. Furthermore, compared to the 200^{o}C results, the dopants in these layers may have been better incorporated and activated due to the higher deposition temperature.

The Terman, high frequency method of interface trap extraction introduced in Section 8.3.3, was used to compare each half of Figure 8.9 in turn with ideal C-V plots to estimate the D_{it}. The results of this process are shown in Figure 8.10, where for each dopant type,

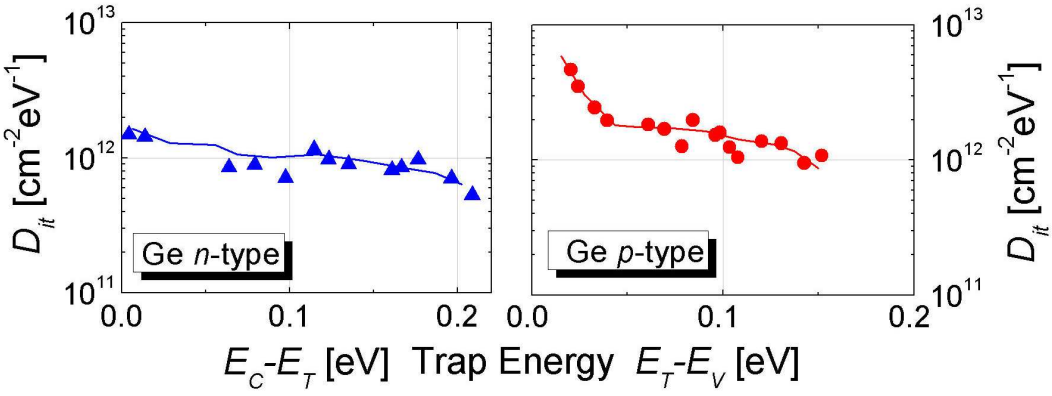


Figure 8.10: The interface trap density extracted from the polycrystalline HfO_2/Ge/SiC MOS device via the Terman method.

a D_{it} was extracted of the order of 10^{12} cm^{-2}eV^{-1}. This is a value only slightly above that of studies of HfO_2 grown on pure Ge [138], despite some obvious flaws with our approach: compared to a Ge single crystal substrate, the polycrystalline structure is very rough and contains multiple grain boundaries, whilst the processing was far from perfect, having being carried out in an MBE system. Hence with process refinement, including CVD deposition and post-deposition polishing, the D_{it} figure would likely improve.

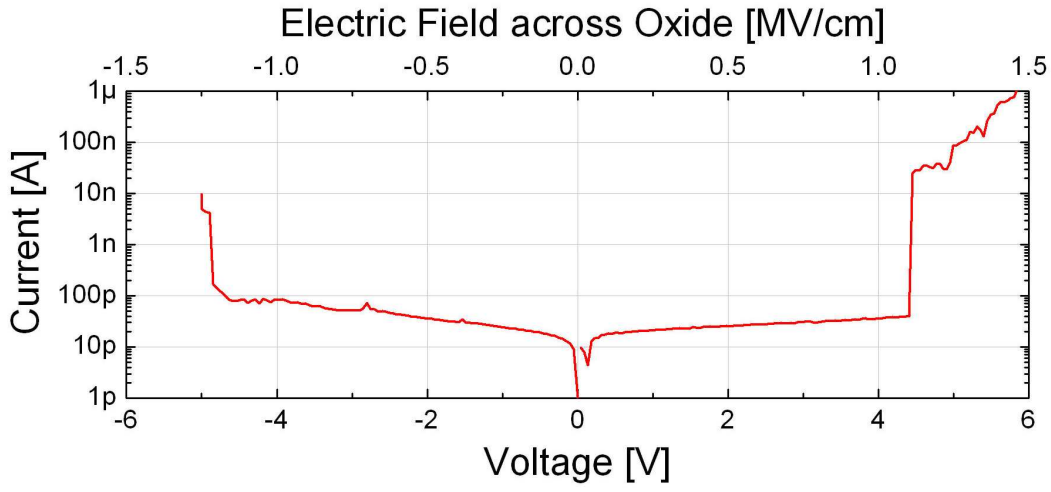


Figure 8.11: I-V results of the HfO_2/amorphous-Ge/SiC MOS device.

Typical I-V results for the HfO_2/Ge/SiC capacitors are presented in Figure 8.11, where the results for the amorphous layer are shown. The leakage current, most likely due to tunneling through the oxide, is quite low (< 1 nA) suggesting that the HfO_2/Ge conduction band-offset is relatively high. The breakdown of the oxide occurs at ± 4.5 V. Using these results in conjunction with the C-V results, a picture of how the layers operate under different biasing can be painted. In accumulation, a build up of majority electrons at the Ge surface means that the vast majority of the voltage is dropped over the oxide, breaking it down when it reaches a critical field. Similar occurs in inversion with the build up of minority carriers at the interface. This is after the depletion region has expanded through the Ge region and into the SiC before reaching its maximum width as witnessed in the C-V results. The critical field, 1.25 MV/cm if the applied voltage is dropped entirely over the oxide, is low compared to the 3-4MV/cm found regularly in HfO_2/Ge literature [134, 135]. This is not surprising considering the surface roughness and the presence of a large number of grain boundaries in each deposition type.

Significantly, the C-V and I-V results display a margin for gate control, in which a potential channel could be operated form accumulation through to inversion. Thicker, more homogeneous Ge layers would likely increase the breakdown values.

8.5.2 Wafer bonded HfO_2/Si/SiC MOS Device

In Sections 5.5.6 and 6.3.5, the wafer bonding of Si to SiC was introduced. Now, this heterojunction substrate is formed into a MOS capacitor through the deposition of HfO_2 on the Si surface, forming a HfO_2/Si/SiC MOS capacitor. This will be compared with three other standard SiC MOS structures found throughout the literature, all of which have been suggested as possible replacements for the SiO_2/SiC MOS device. The first of these

was the simple replacement of SiO_2 with HfO_2. However, the development of HfO_2/SiC capacitors has been hindered by an inadequate conduction band offset of approximately 0.7 eV between the materials [139] causing a large leakage current and an inadequate breakdown. To counteract the leakage, the second structure is a HfO_2/SiO_2/SiC MOS capacitor, which sees the reintroduction of a thermal oxide [53, 140], adding a thin barrier to the oxide stack that reduces leakage due to thermionic emission. Of course this is something of a backwards solution, as it reintroduces all the existing problems with SiO_2, decreasing the effective dielectric constant, and leaving carbon-based traps in the channel. The final structure compared here to the heterojunction structure is the HfO_2/Si MOS capacitor. Hafnium-based oxides have had some significant commercial success, replacing SiO_2/Si in many commercial CMOS processes including in Intel's new 45 nm technology [141]. The switch comes as SiO_2 was having to be scaled to such thin dimensions that leakage due to tunneling and early breakdown becomes too great a problem. The beauty of the high-K solution is that it allows for thicker oxide layers, whilst retaining the same capacitance, as K_O and x_o balance out in equation 8.10. Of course this comes at a price and the barrier height of HfO_2 is two thirds that of SiO_2, resulting in greater leakage due to thermionic emission. Furthermore, the processing, so well defined for silicon's natural oxide, is immature and much more complicated in comparison.

Here, the HfO_2/Si/SiC MOS capacitor is compared to the HfO_2/Si, HfO_2/SiC, and HfO_2/SiO_2/SiC MOS capacitors. The motivation, as in the last Section, is to assess how well the heterojunction devices might perform as MOS structures - whether wafer bonded Si/SiC devices will operate as well as the MBE Ge/SiC samples did.

The blocking characteristics of all the structures are displayed in Figure 8.12a. A large leakage current and a breakdown of less than 1 MV/cm can be seen for the HfO_2/SiC structures, in line with their meagre band offsets. The HfO_2/SiO_2/SiC capacitor performed

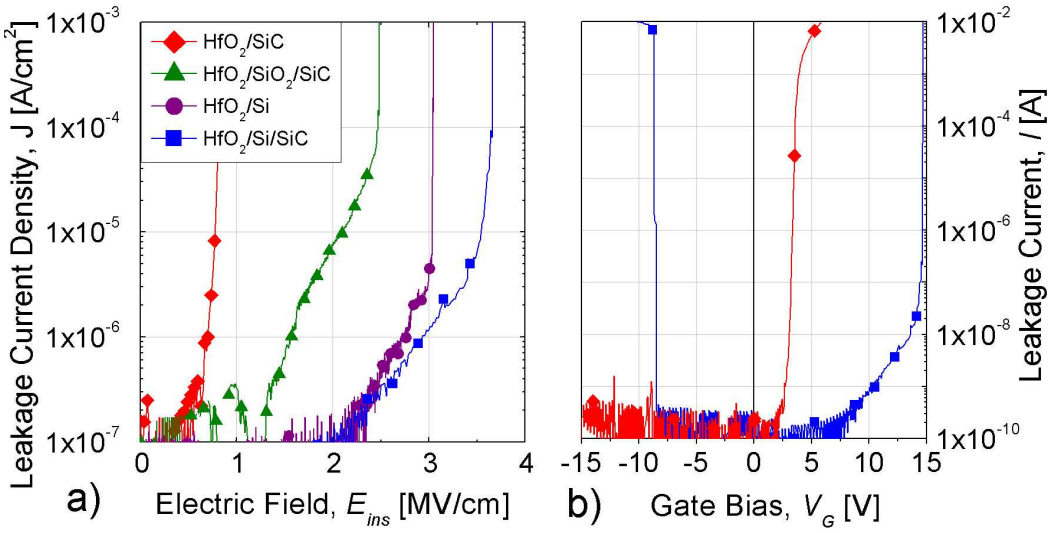


Figure 8.12: a) Leakage and breakdown characteristic taken using I-V analysis. b) The forward and reverse breakdown of the HfO_2/Si/SiC structure compared to the HfO_2/SiC structure.

better, the structure breaking down at 2.5 MV/cm, consistent with other studies [140,142]. However, with its large band offset, the wafer bonded HfO_2/Si/SiC capacitor exceeded both of these at 3.5 MV/cm, with a leakage current consistent with the other structures. This result is similar to that achieved by the HfO_2/Si structure and much closer to the values found in the literature for the upper limit of HfO_2 [134, 135]. This is a result that exceeds the MBE formed HfO_2/Ge/SiC samples, which perhaps validates the previous assertions that a flat, homogeneous surface is the most crucial aspect in forming these capacitors, something much more easily achieved by wafer bonding than by MBE when considering these highly lattice mismatched semiconductors.

In Figure 8.12b, the HfO_2/Si/SiC structure is further compared with the HfO_2/SiC structure. As the SiC is n-type, the HfO_2/SiC capacitor can withstand a very large negative voltage but breaks down with the application of a very small positive (accumulation) voltage. The HfO_2/Si/SiC capacitor suffers breakdown in both directions most likely due

to the p-n heterojunction beneath the oxide, and the limited, 400 nm thick, region of Si. Given a positive voltage the p-N heterojunction is forward biased, and there should be no obstruction to electron flow. Hence, the voltage is entirely dropped over the oxide, now effectively a Si/HfO_2 structure, perhaps explaining their very similar breakdown values. In the reverse direction, the bands of the p-n junction bend the other way and a large depletion region is formed. This is then effectively two capacitors in series, reducing the overall capacitance of the structure. This acts as a potential divider for the total voltage dropped over the structure and may also explain the reduced breakdown voltage in the reverse direction.

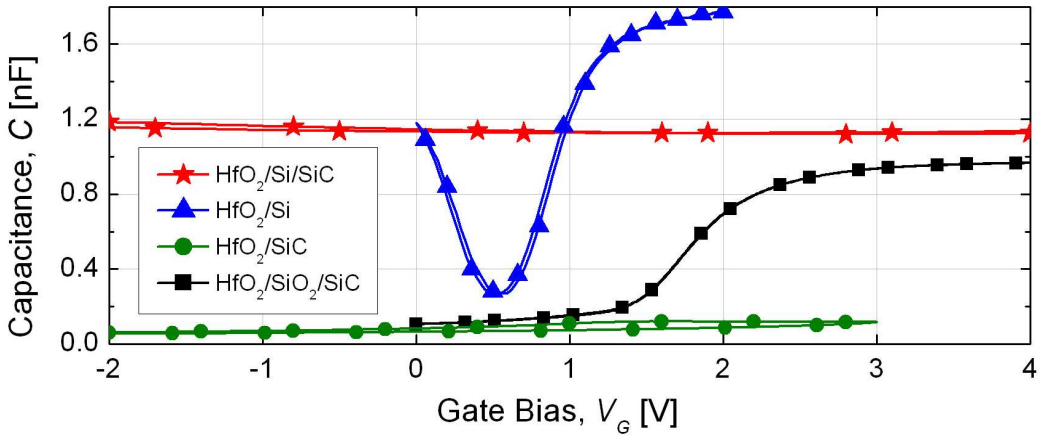


Figure 8.13: C-V results from the High-K MOS structures.

High frequency (100 kHz) C-V analysis was carried out on the four HfO_2 samples and the results are presented in Fig. 8.13. The leakage current of the HfO_2/SiC capacitor is the likely reason for the very low, almost immeasurable accumulation/depletion curve seen in the Figure. The HfO_2/SiO_2/SiC prevents a large leakage current and the structures can be seen to produce good C-V inversion-accumulation characteristics, though the stretching out of the curve suggests that there may be a large amount of trapped charge. The

HfO_2/Si layer, with a conduction band offset [52] of approximately 1.5 eV, can be observed transitioning from depletion to inversion, as one would expect. If the wafer bonded layer was thick enough and homogeneous enough, this is the type of behaviour one would also expect from this structure.

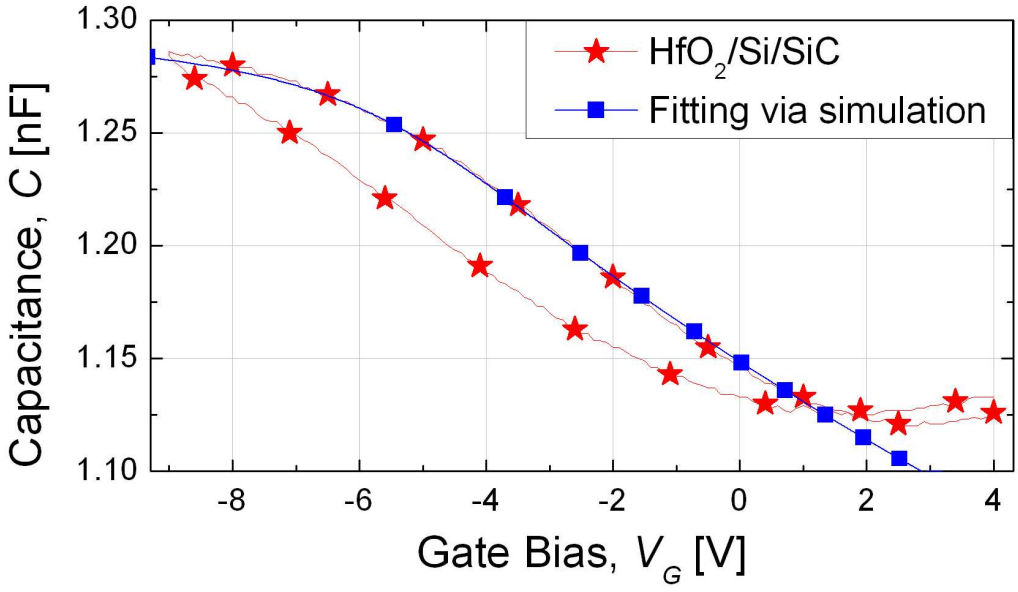


Figure 8.14: C-V results from the HfO_2/Si/SiC MOS structure, with fitting.

The HfO_2/Si/SiC structure by comparison appears to show little variation in its capacitance, compared to the other devices tested. This is unexpected, as simulations suggest that the capacitance of these structures should vary over a similar scale, given the Si doping ($N_A = 1 \times 10^{17}$ cm^{-3}) and an oxide identical to the others. Despite this, Figure 8.14 shows a close up the HfO_2/Si/SiC result, with a Si MOS capacitance model that fits this structure. The zoomed in view of this structure shows that some degree of gate control is attainable on a similar capacitance scale to that seen in Figure 8.9 for the polycrystalline Ge device. Unlike these results, and as one would expect, the C-V result of Figure 8.14 is one sided, with only one dopant type having contributed to this curve. However, to

produce the simulation that fit the gradient of one side of the hysteresis affected curve, the simulated parameters included a doping that was nearly 3 orders of magnitude greater ($N_A = 9 \times 10^{19}$ cm^{-3}) than the actual doping in the wafer bonded Si. If the Si layer were this highly doped it would explain the difference between the structures in Figure 8.13; however it is highly unlikely that a wafer would vary to this degree from the manufacturers specification, whilst no processing steps carried out will have altered the doping to this degree. Therefore, other factors must have affected these results.

Comparing these wafer bonded HfO_2/Si/SiC structures to the MBE formed HfO_2/Ge/SiC, the first obvious difference is the change of material and doping, from n-N Ge/SiC heterojunction structures to p-N Si/SiC heterojunctions. The change of material should make little difference - the conduction band offset should still suffice between Si and SiC, as demonstrated by the I-V results, and the difference in dielectric constant will make minimal difference. However, the change of dopant affects the SiC layer as it will no longer be depleting as the heterojunction layer does. In fact, as the Si depletion width is expanding with increasingly positive voltage, the p-N junction will become increasingly forward biased, reducing its depletion width. This can be visualised in Figure 8.15, where it is predicted that with enough positive voltage, the whole Si layer would deplete (invert) and begin to overcome the p-N depletion region. With a negative bias, the p-N junction depletion region will be expanding as the Si heterojunction region is in accumulation. The dynamics of the three capacitors in series are therefore very complicated and are most likely the reason for the results of Figure 8.14. The apparent high doping may well be a red herring, the slope being a result of the complex series capacitances, rather than the doping of one layer alone.

One further point of note in comparing the structures. The MBE method, though dirty and unreliable with regards to dopant concentration, will produce a very homogeneous

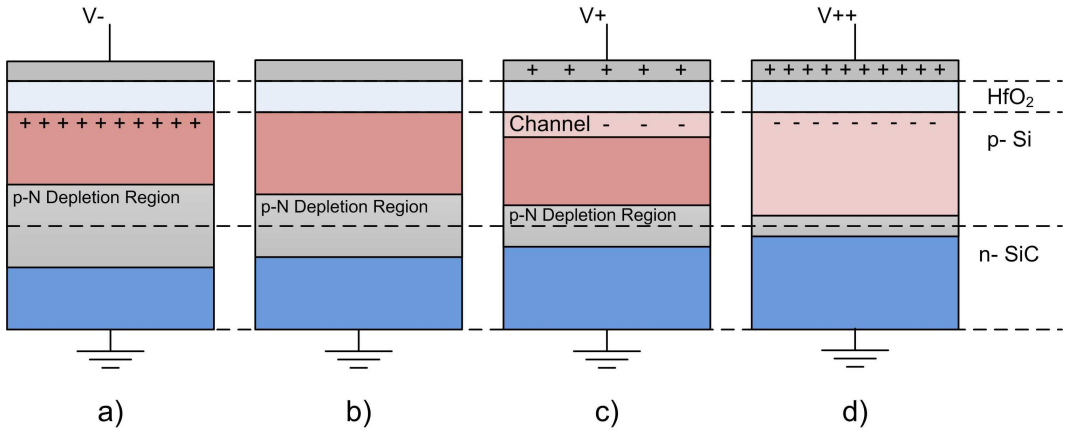


Figure 8.15: A prediction of how the Si and p-N depletion regions interact, as the Si region passes from a) accumulation to b) flat band, c) depletion and d) deep depletion/inversion.

contact, laying down the Ge layer atom by atom on the SiC surface. On the other hand the wafer bonding is very unreliable, producing an interface that has thousands of blisters caused by trapped air or contaminants. Even between the blisters, the homogeneity of the contact is doubtful, as only those surface atoms in intimate contact with the other semiconductor will have formed bonds between the materials. This is another potential source of stray capacitance that could be contributing to the C-V results, though like the speculation above about the complex capacitances, it would be very difficult to quantify the impact of this without much more exhaustive testing.

8.6 Summary

This Chapter has been dedicated to proving the feasibility of MOS devices formed from SiC heterojunction devices. MOS structures were formed on two different SiC heterojunction structures deposited via two different methods. The MOS capacitors were analysed via C-V and I-V techniques. The results from C-V analysis showed that MBE deposited

layers have the ability to form very good depletion/inversion curves, signifying a degree of control over the channel. The technique threw up some problems with depositing layers however, as layers that were intended to be lightly doped appearing to be contaminated with a large quantity of p-type and n-type dopants. Furthermore, given dopants with a low deposition temperature, the likelihood is that the intended dopants will not become activated in the amorphous structure. For the bonded wafers, the C-V results displayed some transition from accumulation to depletion, though models attempting to predict the nature of these results proved inconclusive due to the complex nature of these structures, with multiple sources of capacitance. I-V results showed the ability of the MOS devices to block a voltage. It was of little surprise to see here the flatter, monocrystalline wafer bonded structures out-performing the rough deposited layers, with their multiple grain boundaries. The wafer bonded layers managed to block an electric field of 3.5 MV/cm, a value that is as large as the best HfO_2 layers formed on pure Si or Ge substrates [134,135]. However, the deposited Ge layers managed only one third this value.

Future heterojunction MOS devices could improve on what has been learnt here. Experimentation with CVD deposition instead of MBE, should remove cleanliness and accidental doping as a consideration, whilst a variety of post deposition anneals could be considered to better the semiconductor-semiconductor and semiconductor-oxide interfaces. In both cases, experimentation with a post-processing polish, would improve the homogeneity of the semiconductor-oxide interface.

8.7 Conclusions

1. The use of a narrow bandgap semiconductor between HfO_2 and SiC offers increased band offsets that block significant current. Results also show that significant gate

control is possible using these structures.

2. A wafer bonding/MBE trade off exists whereby layers with the best blocking ability appear to come from the crystalline, flat wafer bonded layers. However, the MBE layers produce the more robust C-V results, showing a smooth transition from depletion to accumulation.

Chapter

9 Conclusions and Further Work

9.1 Summary

The work that has been described at length in this thesis, all originated from one experiment to compare the growth of Ge on SiC to that of Si to SiC. Having available a flexible MBE tool capable of fine controlling the growth parameters of Si and Ge layers, it was a natural step to build upon the large amount of existing Si/SiC research [14, 15, 19, 20] and see if Ge would interact in the same way with the SiC substrate. A like for like comparison between Si/SiC and Ge/SiC was designed, creating new Ge/SiC layers such that they would match existing Si/SiC layers. Therefore the intended thickness, dopant type and quantity, and relative growth temperatures of the first Ge layers all matched the Si experiments that preceded it. On beginning the physical analysis, it soon became apparent that the Ge was not behaving in the same way, seemingly defying its huge lattice mismatch to SiC to produce a degree of uniformity unobtainable in the Si depositions via the same methods. When they were formed into heterojunction diodes and electrically characterised, the layers displayed near ideal turn-on characteristics, low turn-on voltage

and minimal leakage. Series resistance was a problem that improved with a second generation of diodes that refined the Ge growth conditions, vastly improving layer uniformity. However, the devices' breakdown voltage could never be improved beyond 250 V, a by product of the poor edge termination and device isolation techniques available.

Experimentation with the many different MBE deposition parameters suggested that the layers with the biggest polycrystals tended to produce the diodes with the lowest on-resistance. Layers grown at high temperature, with physically small and light dopants produced the lowest resistance layers, with the optimum thickness being somewhere between 300 and 500 nm.

Several questions began to mount up about the way the potential barrier formed between the two semiconductors. Repeatedly, the same culprit came to the fore in the shape of inhomogeneities and the charge they cause to be trapped at the interface. SBH values appeared too large as a result of Fermi level pinning, the trapped charge causing band bending at the surface. This further explained why the extracted SBH and the built-in potential values were nearly identical from Ge layers doped degenerate p-type, degenerate n-type and those unintentionally doped. The impact of the inhomogeneous interface was further cited to explain why the ideality factor and SBH values extracted from I-V analysis were temperature dependant, whilst surface states caused the erroneously large SBH values extracted from C-V analysis. Parameter modelling methods and analysis techniques were adapted from the metal-semiconductor literature to justify and explain all these phenomena, resulting in a sound understanding of the heterojunction interface.

A final test of the heterojunction structures was to see if a good depletion region could be formed in the epitaxial wafer bonded Si layers or the MBE formed Ge layers. This would enable a range of different field effect devices to be considered; heterojunction transistors with narrow bandgap channel regions and wide bandgap blocking regions, or

ultra fast, high mobility Ge FETs supported by the SiC substrate with its high thermal conductivity. The results were promising, showing that using HfO_2 as the dielectric, the WB wafer bonded Si layers could support a decent electric field, managing to block 3.5 MV/cm, a value as large HfO_2 layers formed Si or Ge wafers [134, 135]. Furthermore, the MBE Ge/SiC layers displayed the huge potential to form a depletion region in these layers.

9.2 Conclusions

With the Summary in mind, the general conclusions of this work are listed here.

Polycrystalline germanium, deposited onto a SiC substrate via MBE has been shown to form a more uniform coverage of the SiC substrate than silicon, for which it is more energetically favourable to ball up into tall narrow islands. At an intended deposition thicknesses of 100 nm the Ge also forms islands on the SiC, though these by contrast are much shallower with little bare SiC between the islands. By 300 nm intended thickness, the gaps have filled in and the layers are reasonably uniform. This difference between the narrow bandgap materials is most likely thanks to a lattice parameter in the (111) orientation that is mismatched from a single (0001) SiC parameter by only 0.5 %, though this is far from a 1:1 match of the different atoms, matching at best 1 in 7 Ge atoms with 1 in 12 of the SiC's Si atoms. Furthermore, high resolution TEM images of the interface showed that ordered (111) Ge had formed locally on the SiC substrate in crystals up to 50 nm in diameter.

The key to forming the diodes with the lowest on-resistance was to form layers with the largest polycrystals, and hence the least number of grain boundaries. The polycrystalline nature of the Ge, meant that this requirement was in direct conflict with another, that

the layer should be as flat as possible. In attempting to optimise the layers, a large matrix of variables were controllable, though a balance was not found that could satisfy both requirements. High temperature deposition provided the Ge adatoms the energy they required to find a preferential bonding site, most often next to another Ge adatom minimising the dangling bonds. Therefore, islanding occurred in the thinnest films and large polycrystals (up to 200 nm diameter) formed in the thicker layers, both leading to relatively bumpy surfaces, though a roughness of just 6 nm rms was achieved for a 300 nm n-doped layer deposited at 500^{o}C. Those layers grown at low temperature clearly had little energy to form into crystalline layers and the result, at any intended deposition thickness was very flat, smooth layers, showing minimal crystallinity, though helium ion microscopy images did show some order in the shape of small (¡20 nm) 'dimples' on one surface. Electrical results soon showed that the performance of the low temperature layers was unacceptable, with the surface quality unable to mitigate for the extreme on-resistance and less than ideal turn-on characteristics.

The correlation between surface roughness and on-resistance continued when the difference between dopant types was observed. 300 nm p-type layers that employed the relatively light and small dopant of boron produced a roughness of 30 nm rms and an on-resistance lower than the heavily n-doped layer that employed antimony as its dopant, which is the heavy and large compared to Ge. It seems likely that the antimony caused extra strain within the layer, resulting in small polycrystals and a roughness of only 6 nm rms. The thickness of the layer also had an influence, with on-resistance dropping up to a thickness of 500 nm but then rising beyond this. This was a small data set but the result is not surprising. Up to a given thickness the separate islands are merging and then the polycrystals appear to be under reduced strain and able to grow in size. However, a thickness will be reached where the resistance gain from the increased polycrystal size

is outweighed by the increased number of grain boundaries that the carriers will have to navigate through.

Given all these considerations it seems that the optimum layer would be deposited at high temperature (500^{o}C) to a thickness beyond that required, so that a post-deposition polish could reduce the thick bumpy layer, back to a smooth layer of optimal thickness, somewhere between 300 and 500 nm. An anneal prior to the polish is likely to increase the volume of the deposited layer that forms into a single preferential crystal orientation. The best dopant would be light and small so an upgrade from antimony to nitrogen or phosphorous would likely facilitate larger n-type polycrystals. A pre-deposition polish of the SiC substrate would likely improve uniformity, and would be essential in reducing the inhomogeneities found at the interface.

The electrical performance of the best diodes compared well to conventional Ni/SiC diodes. None of the high temperature Ge/SiC layers had an ideality factor that exceeded 1.1 and the on-resistance was similar to those Ni/SiC diodes with the same 10 μ thick epitaxial layer, between 10 and 20 mΩcm^2 for the best diodes. The SBH of 1.1 eV led to a built-in potential low enough that the diodes' turn-on voltage was approximately 0.3 V lower than their Ni/SiC counterparts. Under reverse bias, leakage was low for the n-type layers; however the biggest problem with the diodes was their inadequate breakdown which never exceeded 250 V. This is a somewhat irrelevant statistic however, as this was achieved without proper isolation, passivation or edge termination, so the true blocking capabilities of these layers will remain uncertain until these more complicated and expensive procedures are carried out, though the literature suggests that very similar Si/SiC devices blocked 1600 V [19, 20].

In attempting to explain the behaviour of the diodes, questions about the Schottky barrier height were continually raised. The barrier behaved unusually; seemingly too

large at 1.1 eV, unusually immovable (along with the built-in potential) in the face of vast dopant changes and yet inconsistent when subjected to temperature change and different analysis techniques. Explaining these phenomena became the new focus of the thesis.

The discrepancy between C-V and I-V techniques was the first to be explained, being similar to that which occurs in a metal-semiconductor regime [70]. It was shown that the C-V technique of SBH extraction was inconsistent, the results being non-linear and varying with frequency in the presence of surface states. This adequately explained the excessive C-V SBH values attained, but despite this, parameters extracted via I-V techniques were also inconsistent, as the ideality factor and the SBH were shown to be temperature dependent, whilst the Richardson constant extracted at any temperature was always at least an order of magnitude lowerthan the calculated value [124] for SiC of 146 $Acm^{-2}K^{-2}$. The reason for this was found by considering two-dimensional fluctuations of the SBH across the heterojunction interface. The variation in the SBH size over the interface leads to the idea that carriers approaching that interface will preferentially find the routes of least resistance - with far more electrons having the energy to cross the lower barriers.

Two techniques were adapted for use on heterojunctions to quantify the fluctuations in SBH. The first treated the device contact area as a variable some fraction the size of the total area, thus representing the small patches across which the majority of current passes. Using this new variable in conjunction with the SBH and the ideality factor, it was possible to extract a single SBH that was approximately 90% the size of the mean SBH found later. Entering this into the diode equation to the experimental results at any temperature, produced much more realistic Richardson constant values. The second technique involved a statistical analysis of the interface, building up a mean SBH value

and a standard deviation value to characterise the distribution of SBH values across the interface.

The surface states that gathered at the heterojunction interface as a result of these distinctly inhomogeneous contacts, were responsible for the fundamental way in which the bands aligned. It was shown to be highly likely that the the Fermi level of the SiC was pinned at its surface to an energy close to the material's charge neutrality level. Ge on the other hand, was hugely unlikely to be pinned due to the huge degenerate doping, which caused it to behave like a metal. This Fermi level pinning was used to show why the SBH was so large, when other methodologies predicted it should be very small, the band bending at the SiC surface influencing where the Ge lined up in its bandgap. It was also used to justify why the size of the SBH and built-in potential appeared to be independent of doping type, the Fermi level of the Ge having to align exactly with the Fermi pinned SiC surface. This 'Pinning Model' predicted that the leakage of a p-type device would be greatly increased over that of an n-type device, something that was proven correct by previous experimental data.

The final proof of concept was to see if a good depletion region could be formed in the SiC heterojunction devices. Firstly, two MOS capacitors were tested employing hafnium oxide as the gate oxide on MBE formed Ge/SiC structures substrates formed using unintentionally doped 300 nm layers, one of which was deposited at low temperature, the other at high temperature. C-V curves extracted from both structures showed that some gate control was possible. The low temperature layer appeared to show a kink in the depletion/accumulation curve, which was shown to be likely the result of the Ge depletion region stretching out to its full 300 nm thickness, whilst the SiC was free to expand unprohibited. This situation was modelled in Matlab and fitted to the experimental data using a doping of 1×10^{16} cm^{-3} in the Ge layer. The high temperature layers produced

the best depletion/accumulation curves; however, there was evidence that the "intrinsic" layers had indeed been unintentionally doped both p-type and n-type by the MBE process. Values extracted from the symmetrical p-type and n-type depletion/accumulation curves suggested that both dopants were present to a level of 1×10^{18} cm^{-3}, higher than the low temperature depositions likely due to the better dopant incorporation and activation. I-V results showed that these layers were unable to block more than 1 MV/cm; however, this was predictable given the uneven surfaces and large number of grain boundaries, which will cause spikes in the electric field.

In contrast to the MBE results, MOS capacitors formed using HfO_2 on wafer bonded Si/SiC, performed well in I-V tests and poorly in C-V testing. The I-V analysis showed that leakage was low and that they could block an electric field of 3.5 MV/cm, larger than HfO_2/SiC and HfO_2/SiO_2/SiC structures and equivalent to the best HfO_2/Si and HfO_2/Ge layers in the literature. The C-V curves extracted showed that some gate control was manageable, though the nature of the curves, specifically the perceived excessive doping was explained by the p-N Si/SiC heterojunction interface, that would form a complex combination of three capacitors in series, each of which was acting in conflict with the other.

9.3 Future Work

This work was the first study on the deposition of Ge onto SiC and as such there are many avenues that future research shall take, especially in the refinement of the deposition technique and the development of new devices, whilst the analysis techniques developed should be applied to other heterojunction layers.

9.3.1 Deposition

The biggest disappointment of this project was that the unique MBE facilities were closed two years into the project, a lack of funding for the equipment leading the University's Nano-Silicon group to focus instead on Chemical vapour deposition (CVD) techniques. At this stage, there was a third generation of diodes planned that would have answered some of the remaining questions, and no doubt, many new experiments would have followed in fourth and fifth generations. CVD was considered as an alternative but the ultra clean vacuum systems required entirely clean substrates, something that could not be guaranteed from the laser cut, air exposed SiC chips used in this project.

The following is a comprehensive list of experiments that would help to definitively characterise the deposition method.

1. This project involved a range of deposition thicknesses but the comparisons are not always fair, involving a range of different dopants. A comprehensive test is suggested to show the different stages of growth, i.e. high temperature intrinsic layers grown at 20 nm intervals up to 200 nm, then at 50 nm intervals up to 600 nm. It appears likely that in the initial stages the formation of the sprawling islands would be evident. These should gradually merge and become more uniform, the individual polycrystals then increasing in size with layer thickness. As well as the materials' interest to this test, the real practical gain will be in knowing at what thickness the on-resistance of the layers reaches its minimum. From the preceding results this is predicted to be around 400 nm.

2. 500^{o}C has been the high temperature growth of choice in this project. However, its original selection was somewhat arbitrary, its relative success meaning that other more interesting parameters took precedence. Again, a fair matrix is required that

will observe the relative pros and cons of a range of growth temperatures, i.e. all other parameters remaining equal, varying the growth temperature at 25^{o}C steps from 400 to 600^{o}C.

3. We observed in this thesis the difference in layer morphology between antimony and boron as a dopant, everything else in the layers being equal. Antimony was heavy and large compared to Ge, boron small and light. Completing this matrix would also be interesting to observe if the differences can be confirmed as large vs, small dopant, or somehow p-type vs. n-type. Hence, joining antimony and boron should be a range of other dopants. Nitrogen would be difficult to include as the Warwick MBE took only solid source dopants, but could be used in those with a gas line. Indium would be the equivalent p-dopant to antimony, whilst the pairs of gallium and arsenic or aluminium and phosphorous could also be considered.

4. A final useful comparison will be the deposition of equivalent layers via MBE, CVD and any other technique to compare the differences. It is expected that CVD would provide a cleaner environment in which to deposit the layers helping to diminish unwanted doping and improve homogeneity.

9.3.2 Fabrication

It is almost too obvious to say that the quality of the diodes are going to be linked to the quality of the technology used, the cleanliness of the environment and the knowledge of the operators using the equipment. Therefore, this Section is a little like saying "If we have a blank cheque...". The best way of achieving state of the art fabrication would be a collaboration with industry leaders and under these conditions, the quality of the diodes would leap up. However, closer to home, there are a couple of ways the fabrication can

be improved without going to huge expense.

5. The use of pre- and post-deposition polishes would most likely have been included in the third generation of diodes. NovaSiC can polish SiC at an affordable rate [86], while they have confirmed in conversation that Ge polishing is also possible. This would vastly improve the quality of both top interfaces, reducing inhomogeneities and hence likely relieving some of the Fermi level pinning and SBH fluctuations.

6. A range of experimentation needs to be carried out on the quality of the layers with anneal temperature. All the layers considered here were not annealed to maintain high/low-temperature differences within the Ge layers. However, now that low temperature layers have been somewhat discredited as an option, a range of anneals on samples from 200^{o}C up to around 800^{o}C, would likely improve the ohmicity of the front Ni/Ge contact, and maybe the SiC/Ge interface; however anneals closer to 1000^{o}C are usually used on SiC, though this is above the melting point of Ge.

7. Some experimentation with techniques that will push up the breakdown voltage is essential, and the techniques described in Appendix A.6 could all be sought at varying degrees of complication. Passivation layers, or field plates, could be achieved reasonably simply with a new two mask process. JTEs and field rings provide extra expense and complication because of the need for an implantation process.

9.3.3 Heterojunction Devices

The work presented in this thesis has been something of a proof of concept for the rectifying properties of Ge/SiC heterojunction diodes and the SiC heterojunction MOS capacitors. This work can be extended as far as resources allow.

8. The basic FET operation could be proven by showing that structures such as the MOS capacitors already established are capable of moderating a channel current. This could be performed relatively simply with minimal processing. A more complicated heterojunction MOSFET is also feasible but would require significant funding, device modelling and process refinement to perfect the multiple mask layer process including implantation.

9.3.4 Materials

A lot of what has been learnt and developed in this project could be applied to other materials including those established heterojunctions and other new semiconductors.

9. It would be a fascinating study to apply the techniques developed in Chapter 7 to other established heterojunction interfaces. A good example is strained silicon where the use of epitaxial strain is exploited to boost carrier mobility. It is therefore of great interest to know if the strain affects interface homogeneity, promoting either Fermi level pinning or quantifiable SBH fluctuations. Increasing the content of Ge in a Si/SiGe layer, the strain is released through the presence of dislocations. Again, these are likely a cause of surface charge and inhomogeneity, so their increase with Ge content may well also show an increase in the spread of SBH values at the interface, measurable by the standard deviation in Section 7.2.4. This same technique could be applied to other combinations for example, Ge/GaAs or AlAs/GaAs.

10. Another very simple recommendation is that epitaxial layers of Si or Ge be grown upon other high power, high temperature, wide-bandgap semiconductors such as GaN and diamond. These other combinations may produce other good structures upon which heterojunction diodes or transistors could be formed. GaN with Si is

well established, the difference being however, that the Si is commonly a supporting substrate for the non-freestanding GaN material.

9.3.5 Analysis Techniques

There are two other analysis techniques that would shed more light onto the nature of the layers.

11. Secondary Ion Mass Spectroscopy (SIMS). SIMS could be used to give a detailed dopant profile through the heterojunction layer potentially showing how well the dopant has integrated. This is of interest because non-uniformity of the dopant is another source of interface inhomogeneity, especially if the dopant has a tendency towards the interface, or indeed grain boundaries.

12. Conductive AFM (C-AFM). Performed on an unprocessed Ge/SiC layer, this technique could be used to perform localised I-V sweeps on the nanometer scale as another method that might shed light on the localised fluctuations of the SBH.

9.3.6 And Finally...

The development of the heterojunction diodes and MOS capacitors in this thesis were the result of three years of research. Some of the ideas presented here could encompass two or three more PhD or post-doctoral positions. However, at the time of writing work had already begun on proving some FET capability, not yet successfully. The idea in point 9 of extending the heterojunction analysis techniques beyond Ge/SiC into Si/SiGe has also begun, through a collaboration with Warwick University's Nano-Silicon group.

Appendix

A Supporting Background Theory

A.1 Introduction

Presented in this Section are some of the fundamental concepts which were taken as presumed knowledge within the bulk of the thesis. This begins by building up the band diagram from basic principles before the interaction of like semiconductors is introduced. Electrostatics are used to build up some of the key equations, before we move on to the most relevant topic, metal semiconductor interaction. This being synonymous with degenerate heterojunction behaviour, band alignment, current transport and the diode equations are introduced. Ohmic contacts are then mentioned, before moving to the more advanced topic of breakdown voltage and the prevention of electric field bunching.

A.2 Band Diagram Theory

This Section introduces the fundamental energy diagram that has become so familiar to the semiconductor world. Starting the discussion with the makeup of the fundamental

elements, we build up the idea of doping and introduce the semiconductor before discussing the band diagram itself including the Fermi level.

A.2.1 The Periodic Table and the Structure of an Atom

The periodic table of elements lists all the elements that are known to man. If we exclude the transitional and rare earth elements, then the classification of the elements in the periodic table is rather simple. From the top of the table down, every row represents a new outer shell that surrounds an atom's nucleus. Each element will have a number of negatively charged electrons in their shells, balancing the number of protons within the nucleus. The atom's horizontal position is determined by the number of electrons that are orbiting in the outer shell, known as valence electrons. The number of the group, I through to VIII, represents the number of valence electrons orbiting the outer shell of the atom.

The first, innermost shell may contain only two electrons. Hence the first row of the periodic table is made up of only two elements, hydrogen with only one valence electron and helium with two. Despite the atom's natural state, it is energetically favourable for all the elements to complete their outer shells. Hence, helium is considered very stable, as there is no benefit in it altering its natural state. Hydrogen, on the other hand is found naturally in its H_2 form, whereby two hydrogen atoms share their electrons, completing the outer shell of both. Having only one electron, hydrogen is the lightest element and also the most abundant in the universe.

The next six shells that can surround an atom's nucleus may hold up to eight electrons. Again, the eight valence electrons found in argon and neon make them very stable elements. The other elements will attempt to complete their outer shells by sharing their

electrons with like and dissimilar elements. In doing so, they form the crystal structure that is the basis of all solid materials. The group IV elements are the simplest example of this, with carbon, silicon and germanium all forming very stable semiconductor materials by bonding to their like elements, though SiGe and SiC are both compounds formed between different group IV elements. Bonding between groups produces stable compounds, with gallium nitride (GaN) and gallium arsenide (GaAs), aluminium nitride (AlN) and aluminium arsenide (AlAs) all popular III-V compound semiconductors, whilst magnesium sulphide (MgS) and zinc oxide (ZnO) are examples of II-VI semiconductor compounds. These compound materials form regular, repeatable crystal structures, the same as Si or diamond. Group I and VII contains the most volatile of the elements as they react with most other elements attempting to lose or gain an electron.

A.2.2 Building the Energy Diagram

In 1926 Erwin Schrödinger gave birth to the equation that bears his name. This described how the properties (e.g. energy, momentum, position) of a particle (e.g. an electron) may be obtained by treating it as a wave function, Ψ. In a level of complexity beyond this text, Felix Bloch translated this theory to the realms of an electron travelling through a unit cell, such as those in Figure 3.1. He revealed that the momentum-energy picture is dependent on the orientation of the electron within the cell. Hence, he was able to derive a set of allowed energy states for an electron within a given lattice, defining for the first time the band structures that have become so fundamental to modern semiconductor physics.

The band diagram may be seen as a map of energy states, representing on a macroscopic scale, the energies of electrons in a material. Given a simple band diagram, such

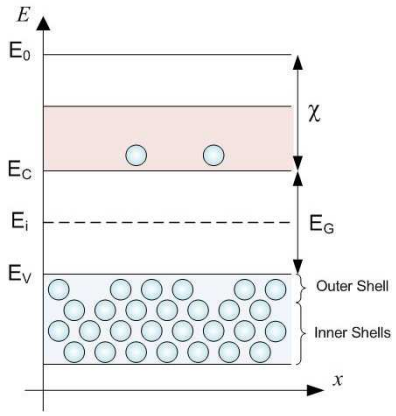


Figure A.1: The band diagram of a generic, undoped (intrinsic) semiconductor.

as that in Figure A.1 which happens to be that of a semiconductor, the vertical scale represents the energy levels of electrons in a lattice. These can be broadly divided into two states, those that are associated with an atom, and those that are free, or conducting. The electrons that are free have much more energy than those within a rigid lattice, and hence they are represented higher up the diagram. In explaining the layout of the band diagram in Figure A.1, we will start right at the bottom. The electrons with the least energy are those that reside in the inner shells. Above these, energetically, are the valence electrons, residing in the outer shell. Having a greater potential energy, it takes much less effort to remove these electrons from the lattice. Hence they are closer to what is known as the valence band edge, E_V, the maximum energy an electron may have whilst maintaining a bond to the atom. The conduction band edge, E_C, represents the lowest possible energy that a free electron may have and is an energy E_G, above the valence band. The intrinsic energy level, E_i, represents a point half way between the bands. This is usually used to denote that the semiconductor is undoped, and hence at 0 K there will be no excess of holes or electrons in the lattice. Once over the energy gap, free electrons may exist at energy levels anywhere within the conduction band. Given a large amount

of energy, electrons may escape the material. This energy level is represented by the vacuum level, E_0, which is the highest point on a band diagram, though often excluded. The vacuum level is an energy, χ, above the conduction band edge, known as the electron affinity.

A.2.2.1 Semiconductors

The energy gap between the conduction and valence bands represents the amount of energy that is required to free an electron from its lattice. The size of the gaps tells us how good a conductor the material is. In an insulator such as that in Figure A.2a, the gap is prohibitive, and no electron given reasonable stimulus can be excited to the conduction band. In a metal, seen in Figure A.2c, the conduction and valence bands actually overlap and there is no gap. This means that there will be a large quantity of free electrons, even at 0 K, and hence they are the best conductors. Between these two extremes are semiconductors, seen in Figure A.2b. Because of the size of their band gap, semiconductors will act as insulators at 0 K and conductors at high temperature. At 0 K, no thermal energy exists to break the bonds holding the electrons to the lattice and hence, the conduction band will be devoid of electrons. At room temperature, the thermal energy is great enough that a proportion of the valence electrons will have broken away, crossing the energy gap to the conduction region.

A.2.2.2 Doping, the Energy Diagram and the Fermi Level.

Figure A.3a shows a simplified example of a group IV material, Si for example. The valence electrons are depicted here as orbiting the nucleus as a planet would the sun; however, the real scenario is of course three dimensional, allowing atoms to form in a crystalline lattice. The uniform nature of this Si material can be easily disturbed by introducing

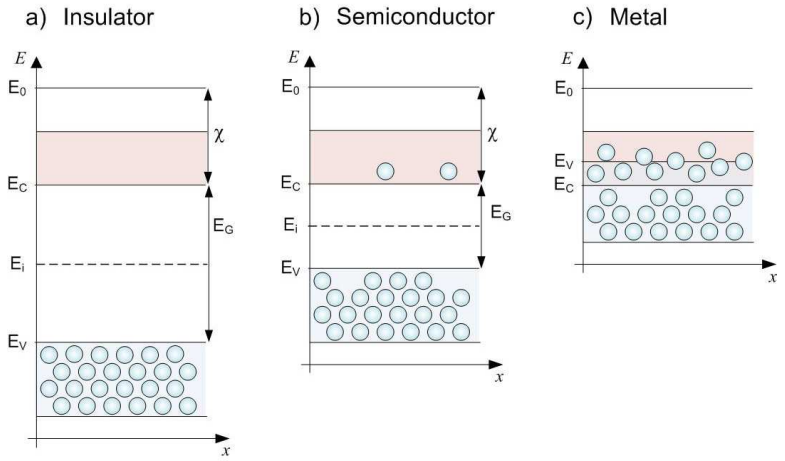


Figure A.2: The band diagrams of an insulator, a semiconductor and a metal.

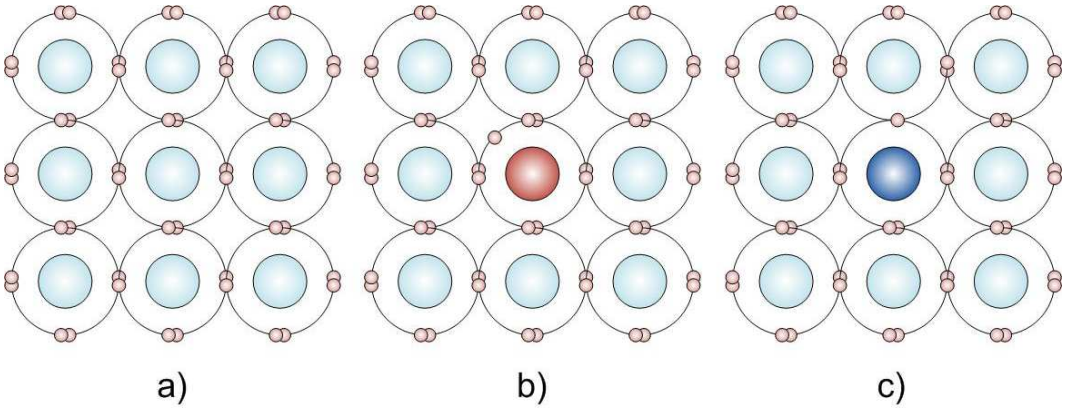


Figure A.3: Three doping types for a group IV elemental material: a) Undoped, or Intrinsic, b) n-type doped with a group V element containing an extra electron, c) p-type doped with a group III element containing one electron less.

elements from different groups into the lattice. Figure A.3b shows the scenario where a single atom of a group V element, phosphorous for example, has been introduced amongst the Si lattice. The addition of this single atom means that only four of its electrons can bond to its neighbours, leaving one spare electron. The electron being a negative particle, this is known as n-type doping. It follows that p-type doping is the opposite of this. Figure A.3c shows a group III element such as aluminium having been introduced into the Si. With one negative electron less than usual, the lattice is said to have gained a 'hole' and is p-type.

The extra electron in n-type doping and conversely, the hole in p-type doping, have only a very weak association with their host atom. Hence, in the n-type case only a small amount of energy will be required to remove a dopant electron from the lattice to the conduction band. The energy required to achieve this has been quantified for Si dopants, with the electrons in the n-dopant phosphorous requiring only 0.045 eV to free themselves into the conduction band [35]. This is approximately 25 times less energy than is required to excite an electron across the 1.12 eV Si bandgap. For this reason, we may visualise the n-type dopants as sitting just below the conduction band in the energy spectrum as laid out in Figure A.4a. At absolute zero, the electrons within the material have no energy, and all the dopant atoms sit in their lattice position at an energy just below the conduction band. As the temperature begins to rise, the electrons begin to jump into the conduction band. At room temperature, all the dopants will have passed into the conduction band.

Though harder to perceive, the opposite case is true for holes. Holes are also fluid given that with energy, electrons from the next complete atom may move into the gap left by the dopant atom. This takes more energy than the freeing of an extra electron, and hence the macroscopic movement, or mobility, of holes through a p-type material

is slower than the movement of electrons through n-type material. The p-dopants sit, energetically, in the semiconductor bandgap just above the valence band as seen in Figure A.4b. Electrons within the valence band require 0.067 eV to jump into holes introduced by the p-dopant aluminium, the reliance on temperature being the same as it was for the n-dopants.

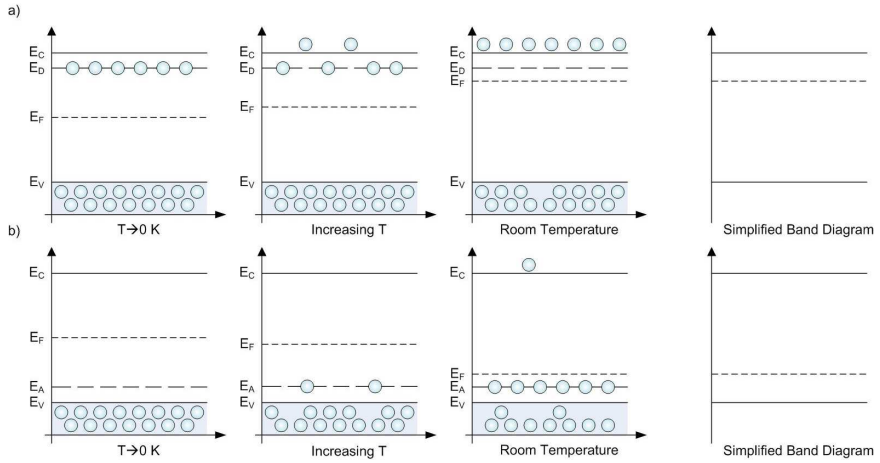


Figure A.4: The effects of dopants on the energy diagram, with the introduction of a) n-type dopants and b) p-type dopants. [35]

In Figure A.4, the Fermi level (E_F) was introduced. Used generally as an indicator of a semiconductor's doping, the Fermi level indicates the energy level at which 50% of the states will be filled with electrons. The number of states in the conduction band (N_C) and the valence band (N_V) are intrinsic properties proportional to the effective mass of an electron (m_n^*) and a hole (m_p^*), respectively, within that material, such that,

$$N_C = 2\left[\frac{m_n^* kT}{2\pi\hbar^2}\right]^{3/2} \tag{A.1a}$$

$$N_V = 2\left[\frac{m_p^* kT}{2\pi\hbar^2}\right]^{3/2} \tag{A.1b}$$

Given that these two values will be very similar, it is only a minor approximation to say that in an intrinsic semiconductor, such as that in Figure A.1, the Fermi level will be halfway between the conduction and valence bands, very close to E_i. In fact, the exact position of the Fermi level in a moderately doped (non-degenerate) semiconductor is very precise, taking into account the excitation of carriers across the bandgap due to temperature and the difference in the effective masses of the carriers. E_F is defined for the non-degenerate case as [35],

$$E_F = E_i + \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \qquad \ldots N_D \gg N_A, \quad N_D \gg n_i \tag{A.2a}$$

$$E_F = E_i - \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad \ldots N_A \gg N_D, \quad N_A \gg n_i \tag{A.2b}$$

where,

$$E_i = \frac{E_C + E_V}{2} + \frac{3}{4}\frac{kT}{q} \ln\left(\frac{m_p^*}{m_n^*}\right) \tag{A.3}$$

and n_i is the intrinsic carrier concentration of a material given by

$$n_i = \sqrt{N_C N_V} \exp -E_G/2kT. \tag{A.4}$$

For moderately doped semiconductors, Boltzmann statistics relate the concentration of carriers to the Fermi level's offset from the conduction or valence bands, known as ϕ_n and ϕ_p respectively, such that

$$\phi_n = \frac{E_C - E_F}{q} = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right) \qquad \text{for n-type} \tag{A.5a}$$

$$\phi_p = \frac{E_F - E_V}{q} = \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right) \qquad \text{for p-type} \tag{A.5b}$$

The final images in Figure A.4 depict the simplified band diagrams, which represent

the most common way of presenting semiconductors energetically. The vacuum, dopant and intrinsic Fermi levels are ignored along with the areas that made up the conduction and valence bands. Instead only the conduction and valence band edges remain outlining the bandgap, whilst the Fermi level represents the quantities of holes and electrons that make up the doping levels.

A.3 Semiconductor-Semiconductor Theory

Having built up the band diagram of a semiconductor, we can now consider what happens when semiconductors are brought into intimate contact, and what happens when we apply a voltage to these structures. Section A.3.1 explores the homojunction, two like semiconductors that are brought in to intimate contact. The case where the semiconductors are of opposite doping, the *p*-*n* junction, is first examined, followed by the isotype junction, where both semiconductors are of the same doping. The degenerate semiconductor will also be examined showing the effect of a large differential in doping between semiconductors.

A.3.1 Homojunction Theory

A homojunction is the union of two like semiconductors. The connection may be made by various means including epitaxial growth and bonding, or simply by doping one region of a semiconductor differently to the bulk. To start we will give the semiconductors opposite doping, forming a *p*-*n* junction. This is one of two basic diode forms along with the metal-semiconductor Schottky diode which will be seen in Section 3.5.

Depicted in Figure A.5 are the two semiconductors of opposite doping being brought into intimate contact. In Figure A.5b, the semiconductors are in intimate contact at $t = 0$.

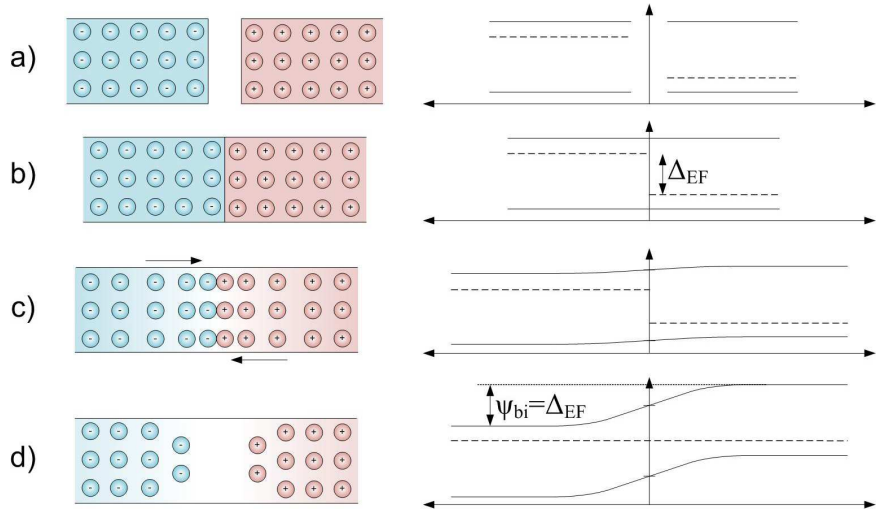


Figure A.5: The flow of majority carriers and the energy situation as two like semiconductors of opposite doping come into intimate contact.

With charge carriers of opposite polarity now in intimate contact, this is an unstable state and the recombination of those charges near the interface is inevitable.

Until now we have only really considered the vertical axis of the energy diagram. The horizontal axis represents the depth into the semiconductor, starting from the surface at a point 0. As more or less carriers gather at the surface or within the bulk, so the energy is able to change along the X-axis. We see this beginning to occur in Figure A.5c and fully in d). The instant after the two semiconductors have been brought into contact, the free electrons of the n-type material are drawn towards the holes of the p-type material and vice versa, thus forming a neutral layer at the interface where the carriers have recombined. This is an area depleted of carriers and hence known as the depletion layer. There is evidence of these depleted carriers in the energy band diagram of Figure A.5d (the stable state) where, at the interface the semiconductor appears intrinsic, having a centred Fermi level. The Fermi levels of the two semiconductors may be seen to have aligned, and this is the golden rule of the energy diagram; that in a steady state with no applied bias,

the Fermi levels of materials in intimate contact will align. This holds true across dopant types forming the basis of p-n junction theory; between different semiconductors, the basis for heterojunction theory; and even between metals, semiconductors and insulators, the basis for Schottky and Ohmic contacts as well as MOS structures.

The potential difference between the conduction bands, ΔE_C (and indeed the valence bands ΔE_V in a homojunction) is known as the built-in potential (ψ_{bi}) under steady state conditions. This value quantifies the amount of bias that must be applied to a p-n interface before 'flat band' conditions are achieved, and electrons can flow unhindered between the semiconductors. The built-in potential between two like semiconductors is simply equal to the potential difference of the Fermi levels ΔE_F prior to intimacy, as seen in Figure A.5b. Hence, subtracting Equation A.2b from A.2a and rearranging, one obtains the built-in potential for a non-degenerate p-n junction,

$$\psi_{bi,pn} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right). \tag{A.6}$$

Considering Equation A.6, the intrinsic carrier concentration n_i at the given temperature will determine the potential barrier to be overcome. Considering again Equation A.4, we may see how much of an influence the bandgap of the semiconductor has on a device. Comparing silicon and silicon carbide, the former with its bandgap of only 1.12 eV has a moderate 8×10^9 cm^{-3} free carriers at room temperature. This leads to built-in potential of 1 Volt given a p- and n-type semiconductor of doping 2×10^{18} cm^{-3} each. For SiC, there are only 9×10^{-9} cm^{-3} free carriers at room temperature. Given the same p- and n-doping, the built-in potential is 3.1 Volts, and hence much more energy is required to turn on this diode.

Whilst much reduced in comparison, the 1 V value for ψ_{bi} is still rather large for a

diode, as a lot of energy will be wasted turning the device on. For this reason bipolar diodes tend to be reserved for applications where large breakdown voltages (> 2 kV) are required.

A.3.1.1 The Application of a Bias

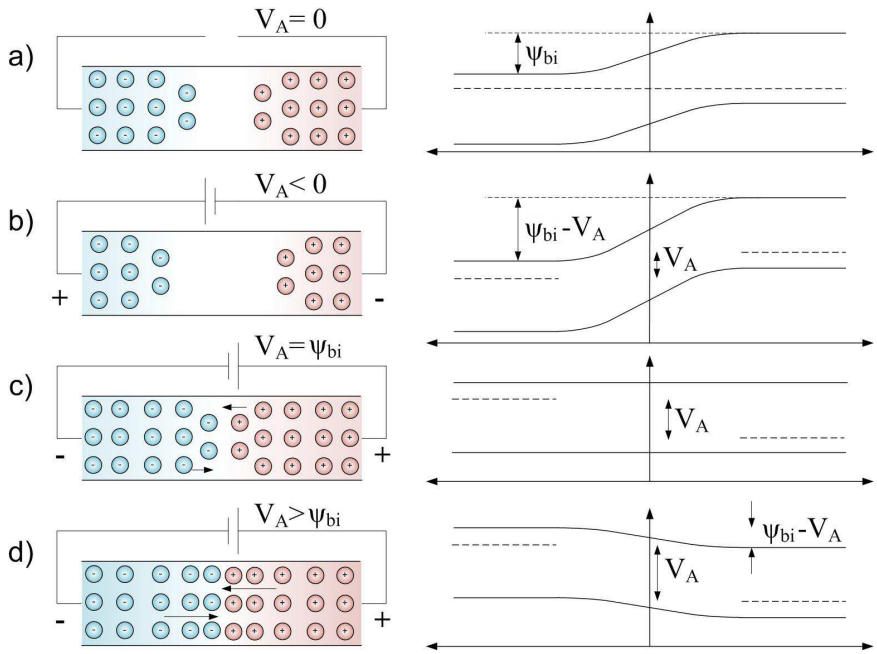


Figure A.6: The flow of majority carriers and the energy situation as a bias is applied to a p-n junction of like semiconductors.

Considering the stable *p-n* junction of Figure A.5d, we can now see how it is used as a diode and assess what happens when a voltage is applied, as shown in Figure A.6. Firstly, in Figure A.6a, the structure lies in its steady state, with no bias applied. With the application of a reverse bias, the depletion region at a p-n interface will widen, the majority carriers on each side being drawn back from the interface. As such, the potential barrier will widen, and

$$\Delta E_C = \psi_{bi} - V_A, \tag{A.7}$$

where the applied voltage, V_A, is a negative value. With the application of the reverse bias, the only electrical conduction through the structure will be down to minority carriers, with a barrier too large to surmount for majority carriers. With the application of a forward bias, this barrier begins to reduce, until a point in Figure A.6c where, with an applied voltage equal to that of ψ_{bi}, the bands flatten. There is now no barrier for carriers to surmount, and current begins to flow in earnest. Increasing V_A so that it is bigger than ψ_{bi}, as in A.6d, causes the bands to bend the opposite way from their origin, further increasing current flow.

Hence, the actions of a bipolar diode have been explained. A reverse bias causing little but leakage current, the small potential barrier causing a small turn-on voltage and the device turning fully on when the applied voltage exceeds the built-in potential. Given a very large reverse bias the structure will breakdown, causing a large flow of current.

A.4 Electrostatic Relationships

Electrostatic analysis allows us to build up a picture of the electric field, E, and the electrostatic potential, V, at a p-n junction interface from the starting point of knowing only the doping and the dielectric constant of the semiconductors. By defining equations for V we can take this further, defining the edges of the depletion region, x_p and x_n, and thus finding the full depletion width W.

A.4.1 The p-n Junction

We use throughout the example of a p-n junction, where both sides of the interface are moderately doped, but where N_A on the p side is three times that of N_D on the n side. In the bulk of these materials charge neutrality prevails [35], as the charge of the free

carrier is balanced by the ionized dopant atom it came from. Within the depletion region (also known as the space-charge region) at a p-n junction, the free electrons and holes have recombined leaving the static ionized dopants, and hence an overall charge density of opposite polarity each side of the interface. The charge density in these regions, ρ, is fully defined by considering all the charge within a semiconductor,

$$\rho = q\left(p - n + N_D - N_A\right), \tag{A.8}$$

where n and p are the intrinsic concentrations of electrons and holes respectively. However, this can be approximated by considering only the intentional doping, reducing Equation A.8 to

$$\rho = q\left(N_D - N_A\right). \tag{A.9}$$

This is known as the Depletion Approximation, and its characteristically square profile can be seen in Figure 8.2.1a. The true profile tails off slightly at the depletion region edges.

Poisson's equation is used to relate the charge density of the space charge region to the electric field across the same region. The three dimensional form is defined as

$$\nabla E = \frac{\rho}{\varepsilon_s}. \tag{A.10}$$

where ε_s is the semiconductor permittivity given by $\varepsilon_s = \varepsilon_0 K_S$. However, in one dimensional problems Equation A.10 simplifies to,

$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon_s}. \tag{A.11}$$

Combining Equations A.11 and A.9, we come to the differential equations that can be used to solve for the electric field.

$$\frac{dE}{dx} = -\frac{qN_A}{\varepsilon_s} \qquad \ldots -x_p \leq x \leq 0 \tag{A.12a}$$

$$\frac{dE}{dx} = \frac{qN_D}{\varepsilon_s} \qquad \ldots 0 \leq x \leq x_n \tag{A.12b}$$

$$\frac{dE}{dx} = 0 \qquad \ldots x \leq x_p \text{ and } x \geq x_n \tag{A.12c}$$

Hence, integrating these equations with the interface and the edges of the depletion region gives the electric field, thus,

$$E(x) = -\frac{qN_A}{\varepsilon_s}(x_p + x) \qquad \ldots -x_p \leq x \leq 0 \tag{A.13a}$$

$$E(x) = -\frac{qN_D}{\varepsilon_s}(x_n - x) \qquad \ldots 0 \leq x \leq x_n \tag{A.13b}$$

The electric field within the depletion region of our example semiconductors is shown in Figure 8.2.1b. The electric field is always negative within the depletion region reaching its strongest point at the interface. Considering the electric field at the interface, where $x = 0$, the two halves of Equation A.13 may be equated, leaving

$$N_A x_p = N_D x_n. \tag{A.14}$$

This explains the correlation between the doping and the depletion width each side of the interface.

The electrostatic potential is the integral of the electric field, given by

$$\frac{dV}{dx} = -E. \tag{A.15}$$

Hence, substituting Equations A.13 into A.15 leaves the differential equations that can be solved to reveal the electrostatic potential. The limits are again between the interface and the depletion width edges, and between 0 volts and the maximum voltage V_{bi}, leaving

$$V(x) = \frac{qN_A}{2\varepsilon_s}(x_p + x)^2 \qquad \ldots - x_p \leq x \leq 0 \tag{A.16a}$$

$$V(x) = V_{bi} - \frac{qN_D}{2\varepsilon_s}(x_n - x)^2 \qquad \ldots 0 \leq x \leq x_n \tag{A.16b}$$

V is seen in Figure 8.2.1c, showing the quadratic curve commonly seen within band diagrams. Again the two parts of Equation A.16 can be equated at the interface, giving

$$\frac{qN_A}{2\varepsilon_s}x_p^2 = V_{bi} - \frac{qN_D}{2\varepsilon_s}x_n^2. \tag{A.17}$$

We have now built the electrostatic picture within the space charge region of the p-n junction; however all this has been done without defining the width of this region. x_p can now be found by rearranging Equation A.17, and eliminating x_n by substituting in Equation A.14. This can be repeated for finding x_n leaving,

$$x_p = \sqrt{\frac{2\varepsilon_s}{q}\frac{N_D}{N_A(N_D + N_A)}V_{bi}} \tag{A.18a}$$

$$x_n = \sqrt{\frac{2\varepsilon_s}{q}\frac{N_A}{N_D(N_D + N_A)}V_{bi}} \tag{A.18b}$$

Hence the full depletion width is given by adding these two depletion edges,

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\frac{N_A + N_D}{N_A N_D}V_{bi}} \tag{A.19}$$

A.4.2 Isotype Homojunctions

The previous electrostatic analysis can be equally applied to an isotype junction with only a change in the nomenclature. The n-n homojunction of Figure A.7, is considered, where one side has the greater doping, and hence a Fermi level offset exists, equal as before to V_{bi}. However, being a unipolar system, the interface between the two layers acts slightly differently. On the instant of contact between the materials an imbalance exists, with the higher doped semiconductor having more free electrons than the other semiconductor. Hence, as time progresses, the two sides balance out, with the electrons diffusing to the side of least carriers. As in the case of the p-n homojunction, the highly n-doped semiconductor is depleted of its carriers, and hence its bands bend up at the interface. Contrary to this, the lighter doped semiconductor is now in accumulation, having more electrons than donor sites, hence the bands bend down at the interface. As you move further from the interface into the bulk of each semiconductor, the bands return to their pre-contact levels.

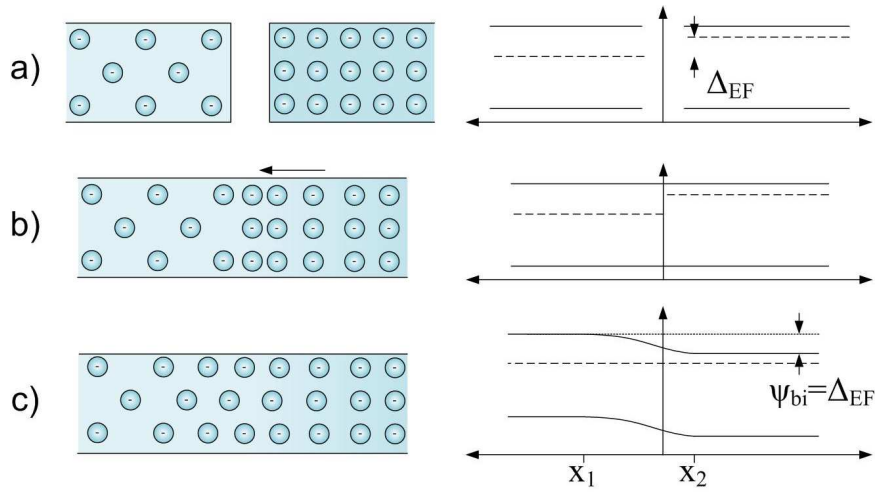


Figure A.7: An isotype homojunction a) prior to intimate contact, b) at the the instant of contact, c) after it has reached its steady state.

From an electrostatic viewpoint, this scenario plays out in a fashion very similar to that of the *p*-*n* homojunction. As the highly n-doped semiconductor is depleted, the charge density is still dictated by Equation A.9. On the other hand, the lightly n-doped layer is in accumulation and hence the charge density is approximated by $\rho = -qN_{D,1}$, leaving the electric field analysis as,

$$\frac{dE}{dx} = -\frac{qN_{D,1}}{\varepsilon_s} \quad \ldots -x_1 \leq x \leq 0 \tag{A.20a}$$

$$\frac{dE}{dx} = \frac{qN_{D,2}}{\varepsilon_s} \quad \ldots 0 \leq x \leq x_2 \tag{A.20b}$$

$$\frac{dE}{dx} = 0 \quad \ldots x \leq x_1 \text{ and } x \geq x_2 \tag{A.20c}$$

It follows then that Equations A.13 to A.19 follow exactly as before, with only a change of nomenclature, $N_{D,1}$ replacing N_A, $N_{D,2}$ replacing N_D, x_1 replacing x_p and x_2 replacing x_n.

A.4.3 Heterojunctions

In considering a *p*-*n* heterojunction, one must consider the differing dielectric constants of the unlike semiconductors. Equations A.13 and A.16 derived for the electric field and the electrostatic potential still hold true. Equation A.14, equating the electric field at the interface, still holds true as $\varepsilon_{s,1}E_1 = \varepsilon_{s,2}E_2$. However, the use of the different dielectrics (ε_1 and ε_2) means that Equation A.17, equating the electrostatic potential at the interface, now becomes,

$$\frac{qN_{A,1}}{2\varepsilon_{s,1}}x_1^2 = \psi_{bi} - \frac{qN_{D,2}}{2\varepsilon_{s,2}}x_2^2. \tag{A.21}$$

Using Equation A.14 to nullify x_2 and x_1 respectively in A.21, x_1 and x_2 at the p-n heterojunction may be found as

$$x_1 = \sqrt{\frac{2\varepsilon_{s,1}\varepsilon_{s,2}}{q}\frac{N_{D,2}}{N_{A,1}(N_{A,1}\varepsilon_{s,1} + N_{D,2}\varepsilon_{s,2})}\psi_{bi}} \tag{A.22a}$$

$$x_2 = \sqrt{\frac{2\varepsilon_{s,1}\varepsilon_{s,2}}{q}\frac{N_{A,1}}{N_{D,2}(N_{A,1}\varepsilon_{s,1} + N_{D,2}\varepsilon_{s,2})}\psi_{bi}} \tag{A.22b}$$

A.5 Metal-Semiconductor Theory

From a circuitry point of view, we take for granted that our transistors and diodes, with their metal contacts, will slot together with other devices in a predictably ohmic, low-resistance fashion. We need to know no information about how one metal contact may interact with another, we simply presume that they will conduct almost losslessly. To facilitate this level of ease, we must ensure that all our devices begin and end with metal contacts. It is therefore imperative that we understand the interaction between metal and semiconductor.

The band diagrams of the two contact types, the Schottky and Ohmic contact, are very similar in appearance. They both involve a potential hill, or Schottky barrier, that majority carriers have to overcome, though they achieve this in quite different ways. To understand these concepts, three significant current transport techniques must first be understood. We will then discuss the rectifying Schottky contact, the key to the Schottky Barrier Diode, followed by the Ohmic contact, which ideally is a lossless transition between the materials.

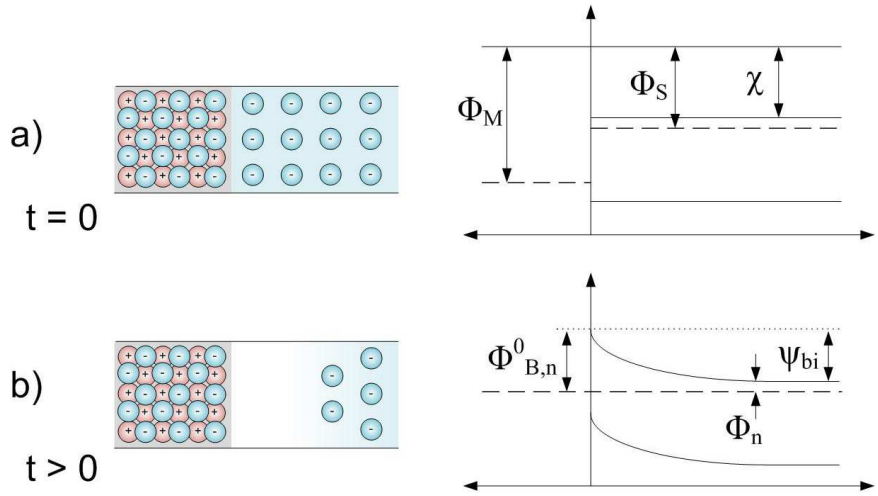


Figure A.8: A Schottky metal-semiconductor interface a) prior to settling to the steady state and b) in the steady-state.

A.5.1 The Schottky Barrier

The potential barrier that occurs at the M-S interface is known as a Schottky Barrier after the German Physicist, Walter H. Schottky who first developed the now common mathematics surrounding the idea [97]. A simple M-S interface involving a moderately n-doped semiconductor ($N_D < 1 \times 10^{15}$ cm^{-3}) may be seen in Figure A.8. The large quantity of free carriers within the metal means that a one-sided depletion region forms synonymous with that of a degenerate p-n junction. One can gather the vital equations up by visually inspecting the pre- and post-connection band diagrams of Figure A.8. The built-in potential, ψ_{bi}, is clearly the difference between the semiconductor and metal Fermi-levels prior to contact. The Schottky-Mott principle [97,98] states that the vacuum levels will align, leaving the electron affinities to dictate the offset. Under these conditions, the built-in potential is simply,

$$\psi_{bi} = E_{F,S} - E_{F,M} = \Phi_M - \Phi_S, \tag{A.23}$$

where Φ_M and Φ_S are the respective energy differences between the metal and semiconductor's Fermi levels and the vacuum level. The next logical step, is defining the height of the Schottky Barrier, Φ_B, over (or, as we will see, through) which electrons must pass when travelling from the metal to the semiconductor. To clarify the nomenclature, Φ_B, refers throughout to any M-S offset. The subscript p or n narrows this down to the hole or electron barrier whilst $\Phi^0_{B,n}$ refers specifically to the theoretical maximum M-S barrier formed before any real-world effects are considered, such as image-force barrier lowering or tunneling. From Figure A.8 and Equation A.23, it follows that

$$\Phi^0_{B,n} = E_{C,S} - E_{F,M} = \Phi_M - \chi, \tag{A.24}$$

where χ is the semiconductor electron affinity, the potential difference between the semiconductor's conduction band and the vacuum level equal to $\Phi_S - \Phi_n$ and where Φ_n is the difference between the conduction and Fermi levels. Given this it follows, that the Schottky barrier height is also defined as

$$\Phi^0_{B,n} = \psi_{bi} + \Phi_n. \tag{A.25}$$

A.5.2 Current Transport Processes

Unlike the p-n junctions discussed in Section A.3.1, metal-semiconductor contacts are mainly unipolar, with the majority carriers responsible for the majority of current flow. Figure A.9 shows five of the transport processes that occur under forward bias. Either thermionic emission (TE), thermionic field emission (TFE), and field emission (FE) will dominate the current transport process dependent on the level of doping within the semiconductor, and we will analyse these techniques in detail. Diffusion is the process by

which particles move from areas of high concentration to areas of low concentration. In this case, electrons travel from the bulk to take the place of those others that have been induced over (or through) the barrier. Also some minority carrier injection takes place at high forward bias with holes diffusing from the metal towards the bulk. The recombination (or generation) of carriers occurs in the depletion region of a contact whenever the thermal equilibrium of a semiconductor is disturbed, i.e. when $pn > n_i^2$ (or $pn < n_i^2$). The amount of minority carriers that diffuse into the depletion region within these contacts is very small due to the large potential barrier, thus the recombination current is insignificant compared to that induced by thermionic or field emission. In a full analysis, the minority injection and recombination currents cannot be ignored, and further details of them can be found elsewhere [36].

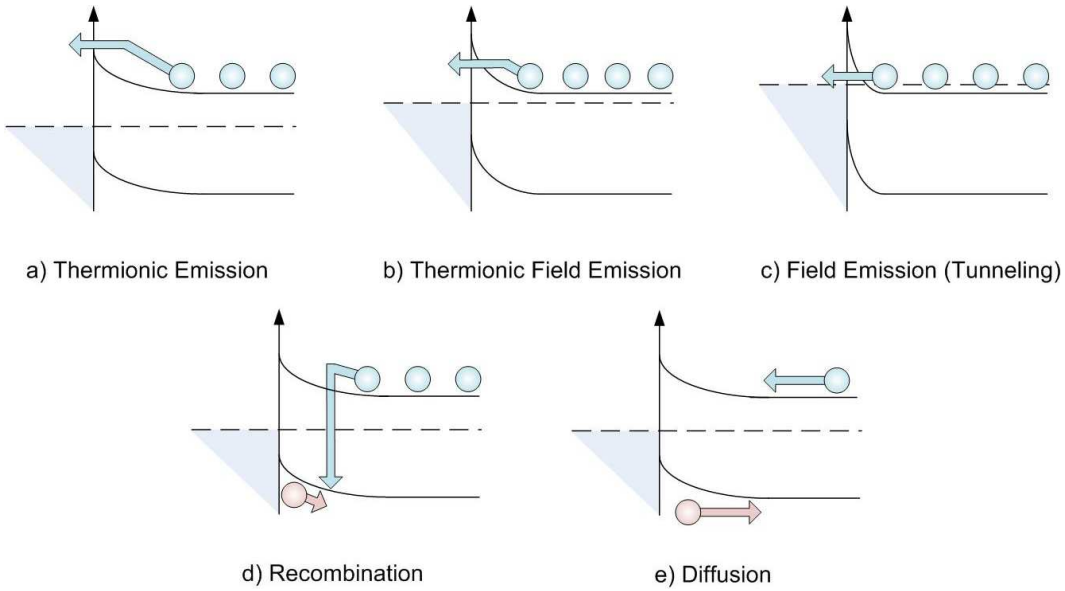


Figure A.9: Band diagrams depicting the three current transport mechanisms and their relationships to semiconductor doping.

The way in which carriers overcome the Schottky barrier depends on the width of the depletion region, W, which in turn is dependent on the doping of the semiconductor.

Figures A.9a-c, relate the semiconductor doping and the current transport mechanisms, from low doping and thermionic emission at one extreme, to high doping and field emission at the other.

Thermionic emission is the dominant mechanism in Schottky contacts, and is the most simplistic process to understand. Presented with the barrier seen in Figure A.9a (or in Figure A.8), the carriers within the semiconductor bulk need to gain enough energy to mount the Schottky barrier. Though some diffusion may take place over the barrier, the driving force to current flow is drift following the application of a bias that decreases the barrier height and raises the energy of the individual carriers to a higher level. However, in reversing the bias, the barrier that is presented to a majority carrier at the M-S interface is too great to overcome, blocking current flow from all except the minority carrier leakage. Under forward bias, the current that flows from the semiconductor to the metal is dominated by the combination of thermionic emission and majority carrier diffusion, and is expressed as [36, 65],

$$J_{s\rightarrow m} = A^{**}T^2 e^{-\beta\Phi^0_{B,n}}\left(e^{\beta V}\right) \tag{A.26}$$

where A^{**} is the Richardson's Constant and β is the inverse thermal energy ($\beta = q/kT$). J is the current density expressed as $J = I/A$, where A is the contact area. This can be shortened to,

$$J_{s\rightarrow m} = J_S e^{\beta V} \tag{A.27}$$

where J_S is the saturation current defined as

$$J_S = A^{**}T^2 e^{-\beta\Phi^0_{B,n}}. \tag{A.28}$$

The other extreme is in Figure A.9c, and is the mechanism used most commonly in Ohmic contacts. With a highly doped semiconductor, the band bending takes place over a very thin region less than 3 nm thick. This barrier appears invisible to the carriers and they can quantum mechanically tunnel through the barrier in an effect known as field emission. In between the two extremes lie thermionic-field emission, whereby the moderate to high doping means that tunneling may occur once the carriers have reached a certain energy level above the bulk. In actuality, some tunneling will occur in all contacts, though deep within the thermionic emission regions, the energy at which this is possible may be only fractions of milli-electron-volts from the top of the barrier.

We can apply some quantitative analysis to expand the metal-semiconductor model already built up, classing a given contact into one of the conduction methods. The effective thermionic barrier height (E_m) can then be found, the point at which tunneling will occur. Here we use as an example the Ni/Ge interface, which we will use in later chapters as an Ohmic contact to the heterojunction diodes, though this works equally with any metal/semiconductor combination.

To determine the conduction method, the characteristic tunneling energy E_{00} of the semiconductor can be calculated and compared with the thermal energy kT. E_{00} is given by Padovani & Stratton [143] as follows:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_d}{m_T^*\epsilon_s}}, \tag{A.29}$$

where $\hbar$ is the reduced Planck's constant and m_T^* is the tunneling effective mass. m_T^* is given [144] for n-type Ge as $0.12m_0$. FE is said to dominate [65] if $E_{00} \geq 5kT$ while TE will dominate at $E_{00} \leq 0.5kT$, and between these margins TFE will dominate. In Figure A.10, we can see the result of Equation A.29 plotted for a Ni/Ge contact with a range of

Ge doping values, with the aforementioned boundaries marked.

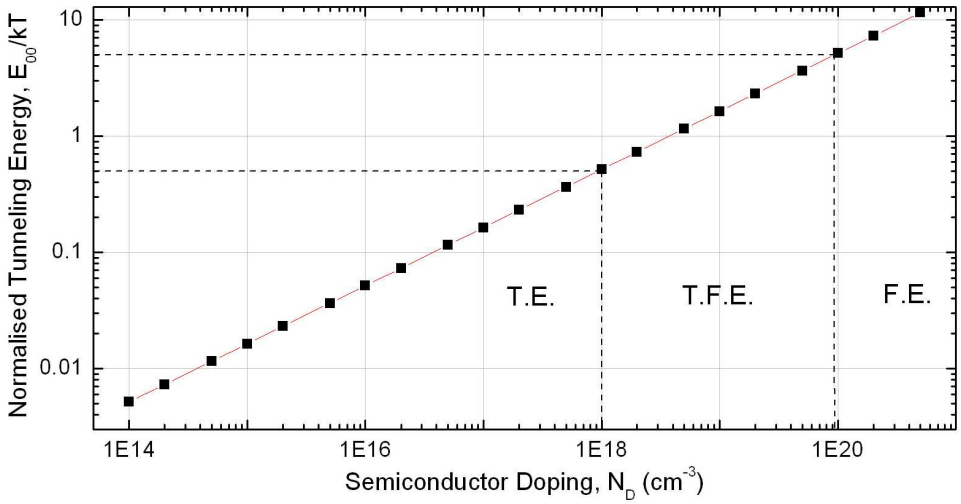


Figure A.10: The boundaries of the conduction methods for a Ni/Ge contact as laid out by Padovani & Stratton [143].

From Figure A.10, we can see that any doping above 1×10^{20} cm^{-}3 is firmly in the Ohmic field emission region, whilst below 1×10^{18} cm^{-}3, thermionic emission dominates. The effective barrier height (E_m) at which tunneling occurs is given by [36, 143]

$$E_m = \frac{q\left(\Phi^0_{B,n} - V_N - V_A\right)}{\cosh^2\left(E_{00}/kT\right)} \tag{A.30}$$

In Figure A.11, E_m is plotted as a function of the doping, with the boundaries of the conduction methods marked. It can be seen that within the thermionic emission region, the barrier height rises as V_n decreases. At a critical point at a doping of around 1×10^{17} cm^{-}3, the depletion width becomes thin enough to allow significant tunneling and the curve begins to dip, entering the thermionic-field emission region. As the depletion width gets thinner, the barrier height tends to zero, entering the field emission region.

To complete the picture, the current due to field emission under forward bias, is given

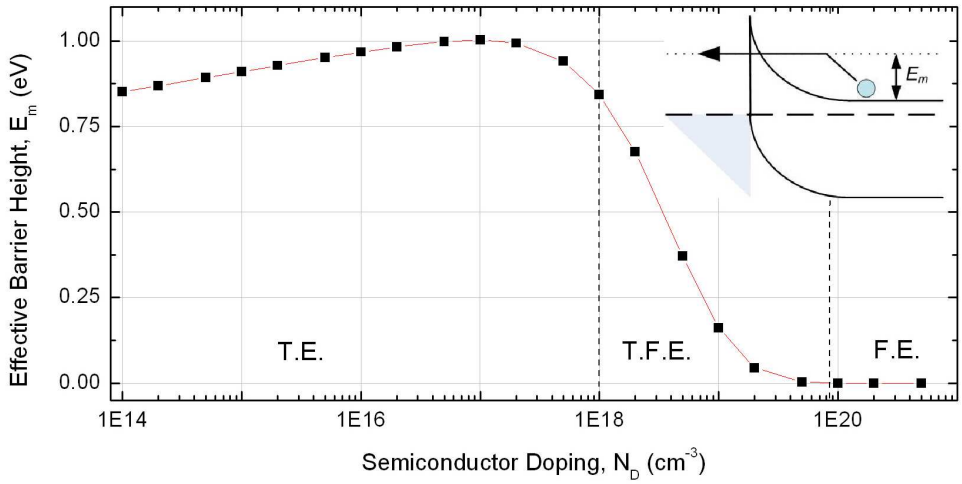


Figure A.11: The effective barrier height as a function of the Ge doping within a Ni/Ge contact. Inset: E_m from an energy perspective. In both, $V_A = 0$.

by [36],

$$J_{FE} = \frac{A^{**}T\pi \exp\left[-q\left(\phi^0_{B,n} - V_A\right)/E_{00}\right]}{c_1 k \sin\left(\pi c_1 kT\right)}\left[1 - \exp\left(-c_1 q V_A\right)\right], \tag{A.31}$$

where,

$$c_1 = \frac{1}{2E_{00}} \log\left[\frac{4\left(\phi^0_{B,n} - V_A\right)}{-\Phi_n}\right]. \tag{A.32}$$

The current due to thermionic field emission is expressed as [36],

$$J_{TFE} = \frac{A^{**}T\sqrt{\pi E_{00} q\left(\phi^0_{B,n} - \Phi_n - V_A\right)}}{k\cosh\left(E_{00}/kT\right)} \exp\left[-\beta\Phi_n - \frac{q\left(\phi^0_{B,n} - \Phi_n\right)}{E_0}\right] \exp\left[\frac{qV_A}{E_0}\right] \tag{A.33}$$

where,

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \tag{A.34}$$

A.5.3 Ohmic Contacts

Similar to the Schottky contact, the Ohmic contact is a very simple contact made by depositing a metal on a semiconductor. These contacts are used to connect the semiconductor from the outside world with minimal impedance. As the name suggest the best Ohmic contacts will not be rectifying and will be purely resistive, though with very low contact resistivities down in the order of 1×10^{-7} Ω cm^2 for the best contacts, the resulting contact resistances will be small, though not entirely negligible. In theory, two methods can be employed to form an Ohmic contact, though the most common is that already described in the previous Section.

The simplest ohmic contact conceptually, is formed from a metal with a work function of a similar energy to the semiconductor's conduction or valence band, depending on whether the semiconductor is n- or p-type doped. Hence, any barrier that forms will be minimal to the majority carriers. In practice this is particularly difficult to do. The semiconductors Si, Ge, and SiC all have electron affinities of approximately 4 eV. Hence to form an Ohmic n-type contact, a metal is needed with a similar work function. Aluminium has one of the lowest at 4.28 eV, so whilst only a very small barrier will exist, without high doping, some rectifying action will be present. Furthermore, as we will see in Section 7.3, there are sufficient doubts over the validity of the Schottky-Mott principle, which mean that the materials may not align exactly as their work functions suggest they will.

More reliable is the Schottky barrier that uses high doping and field emission to form the Ohmic contact as described in the previous Section. With this form of the contact, the offset of the work functions makes little difference as the band bending over a very small depletion region helps to form contacts that are easily quantum mechanically tunneled through. An example of this is shown in Figure A.12, where the doping of the

semiconductor will typically be 5×10^{18} cm^{-3} or greater, and as discussed previously, degenerate. In the example of a degenerate semiconductor in contact with another non-degenerate semiconductor, all the band bending was presumed to occur in the lower doped semiconductor. Here, up against the immovable metal, all the band bending occurs in the degenerate semiconductor over a very narrow distance.

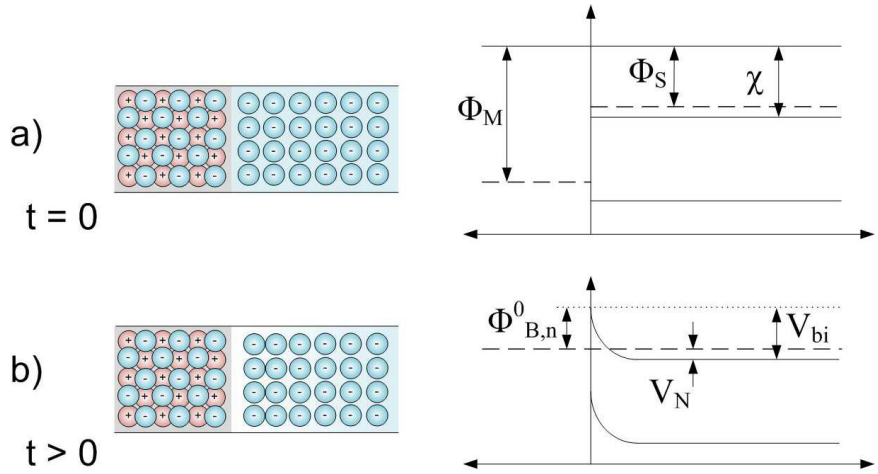


Figure A.12: An Ohmic metal-degenerate semiconductor interface a) prior to settling to the steady state and b) in the steady-state.

Whilst quantum mechanical tunneling is the key to Ohmic contact operation, the low resistances come from the annealing process. Exposing the structures to high temperatures enables interdiffusion of the atoms between the layers, forming metal-semiconductor compounds such as nickel-silicides or aluminium-germanides. These layers enable the smooth transition from metal to semiconductor, filling the gaps that may be caused by surface defects and resulting in a clean planar contact.

A.6 Breakdown Voltage

At a moderate reverse bias, minority carriers will be accelerated across the depletion region causing a small leakage current. As this carrier crosses the depletion region, its path is interrupted by collisions with the lattice, that lose the particle energy and slows it down. As the reverse voltage increases further, there becomes a great energetic gap between the fermi levels on each side of the depletion region, and the carrier undergoes a greater acceleration between collisions. When this acceleration increase is great enough, the impact of the carrier on the lattice becomes significant enough to ionise another semiconductor atom, inducing an electron to be freed from the valence band. The newly created electron and hole along with the original particle are immediately accelerated again, each freeing more carriers on their next collision. This process is known as impact ionisation and leads to an avalanche current that in turn leads to the device's reverse breakdown. On the lead up to the breakdown, the impact of the impact ionisation is simply to increase the leakage current. However, at a critical bias, known as the breakdown voltage, V_{BR}, the acceleration of this process is too great, and the current runs away.

The amount of voltage a Schottky barrier can support depends largely on the thickness of a low-doped epitaxial bulk region which supports a significant electric field. Baliga [30] relates the doping to breakdown voltage and the maximum depletion width, relationships which for Si and SiC are reproduced in Figure A.13a and A.13b. Given that dopant concentration is inversely proportional to resistance, the introduction of a very thick low-doped region will add a large amount of series resistance to the device. Hence, Figure A.13c shows the minimum possible resistance for a given breakdown voltage. Therefore, at the most fundamental level, a trade-off exists, and the device designer must choose between resistivity and blocking voltage. Of course, there are other considerations here

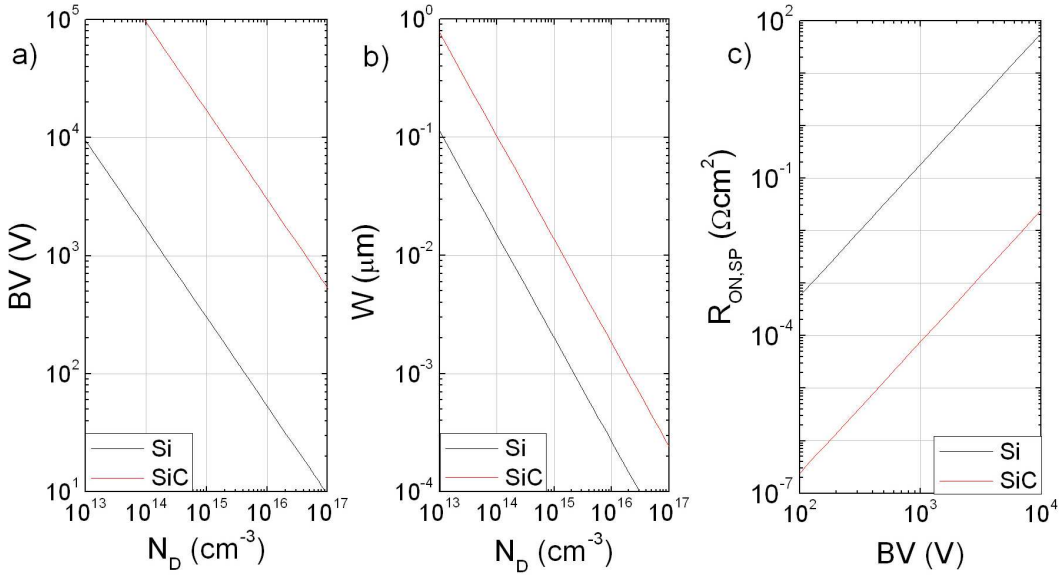


Figure A.13: Relationships between doping concentration (N_D), breakdown voltage (BV), maximum depletion width (W) and specific on-resistance $R_{ON,SP}$ are shown, reproduced from [30].

which influence this; epitaxial layers are expensive with their cost usually being a per μm value. This means there is even more reason to deal with layers as thin as possible, and so other techniques are used to maximise the breakdown voltage so that the thinnest possible epi-layer can be used.

One such technique is the use of appropriate edge termination. Figure A.14 shows the situation that occurs in unterminated situations where a metal-semiconductor region is subject to a reverse bias that forms a depletion region around the contact. Evident is the situation at the edge of the contacts where the electric field is bunching, providing an electric field spike at the contact edge. This spike causes the critical electric field (E_{CF}) to be breached at a voltage much lower than the theoretical breakdown voltage and hence the full potential of the materials are not being met. Various methods exist to reduce the spikes at the contact edges, the simplest of which is mesa etching as shown in

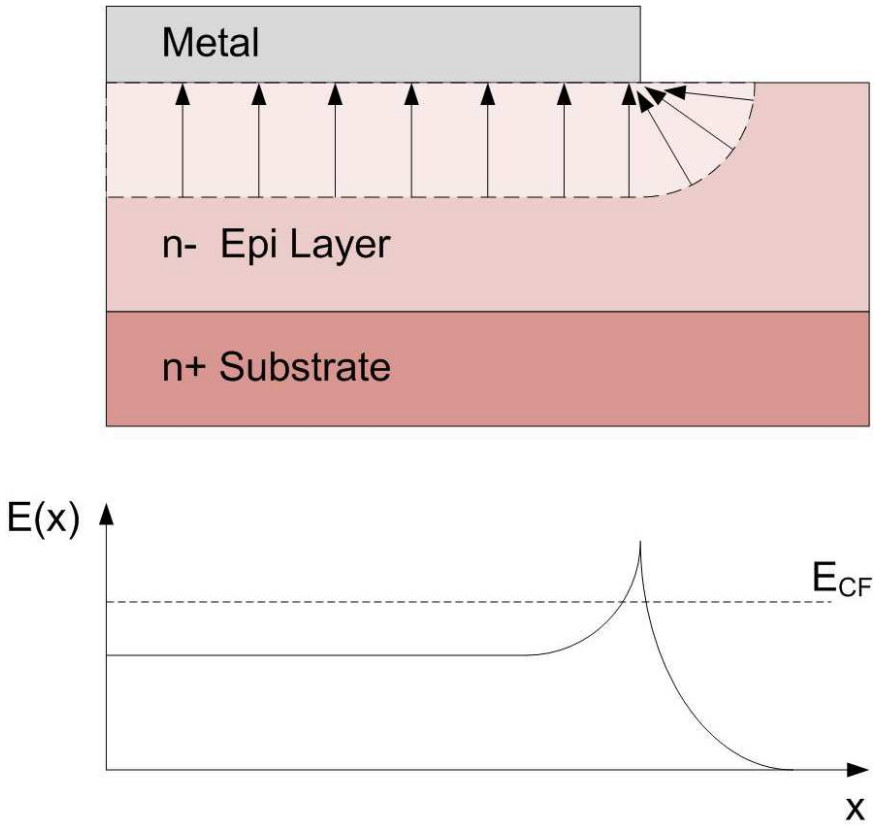


Figure A.14: A reverse biased metal-semiconductor region with no edge termination, showing the build-up of electric field at the junction edges. Reproduced from [145].

Figure A.15a. This allows a significant drift region to form under the contact where the electric field will be uniformly spread, before it reaches the main substrate. At this point bunching will again occur, but the electric field at this depth will be much less that it is at the surface directly beneath the contact.

Many techniques attempt to spread out the lines of bunched up electric field at the contact edges. Floating field rings are a popular technique, most commonly implanted p-type layers [145,146] (in an n-type substrate), though also floating metal rings [92]. These floating rings are designed to spread the electric field beyond the edges of the contact as shown in Figure A.15b. They prevent the large build up of electric field at any one point,

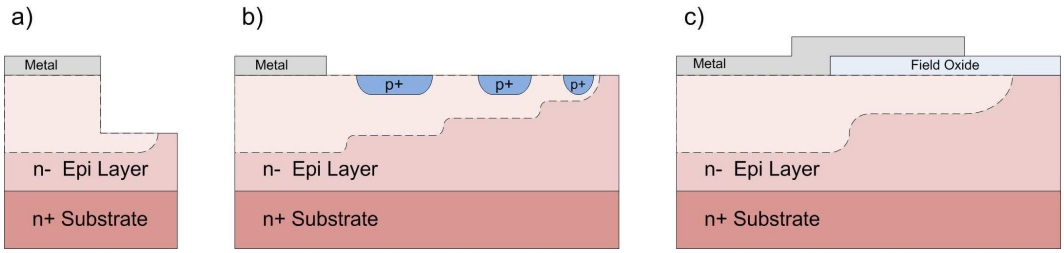


Figure A.15: The use of various techniques to reduce electric field spikes.

allowing the breakdown voltage to approach its theoretical value. Another method of achieving this is through the use of a field plate as shown in Figure A.15c, where the continuation of the contact over a field oxide causes the spread of the depletion region beyond the edges of the contact. Other methods including junction terminal extensions (JTE) and bevelled edges are used in transistor devices to achieve the same uniform spreading.

A final technique used to optimise the breakdown electric field and reduce leakage is the use of passivation, an oxide layer deposited onto the semiconductor surface wherever it would otherwise be exposed to the elements. This prevents the build up of unwanted charge due to surface recombination or an inhomogeneous surface, whilst also protecting the surface from any chemical interaction with the air surrounding it.

Appendix

B Extended Physical Analysis Theory

The theory behind many of the physical analysis techniques is presented here, providing some of the detail behind Section 4.2.

B.1 Atomic Force Microscopy (AFM)

The concept behind AFM is quite a simple one. A cantilever with a very sharp tip is used to probe the surface of the semiconductor one position at a time. The deflection of the cantilever as it makes contact with the surface is used to control the height of the sample under test, recording a z-direction value for each 2-dimensional co-ordinate. A SEM image of an AFM cantilever and tip is shown in Figure B.1. As this was a used tip, it is rather blunt; the radius of curvature of a new tip is in the order of nanometers. The deflection of the cantilever is typically measured by using a fixed laser angled onto the reverse of the cantilever, with an array of photodetectors measuring the reflection angle, which is dependent on the cantilever's deflection.

There are three methods by which the surface profile may be built [67]. The static

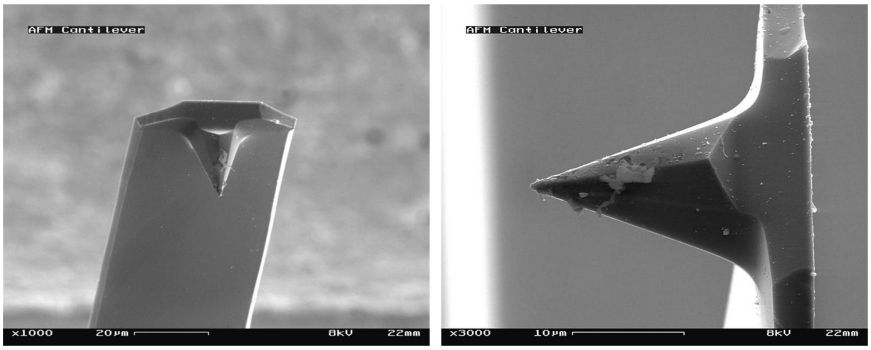


Figure B.1: SEM images of a used AFM cantilever and tip [147].

contact mode involves the tip being in constant contact with the surface, at a constant force. The height of the sample is controlled to maintain a constant force on the tip, and hence a constant laser deflection angle. For every position in an x by y scan, a z-direction value may be ascertained from the sample height that maintains the correct deflection angle. The problem with this method is that the attractive forces can damage soft samples, and that the tip will degrade relatively quickly.

The dynamic non-contact mode involves the cantilever being oscillated at its resonant frequency just above the surface of the sample. As the tip comes to the bottom of its oscillation within 1-10 nm of the sample surface, the van der Waals forces are at their strongest and act to reduce the frequency of oscillation. The AFM software can therefore build up the z-profile for every x-y position by altering the sample height, maintaining a constant amplitude or frequency of oscillation without the tip having come in contact with the surface. This overcomes the tip and surface degradation problems of the contact mode. However, the disadvantage is that this mode will not discriminate between the solid sample surface and any adsorbed fluid on the surface, presenting a potential source of inaccuracy. Furthermore, the tip can become stuck to the sample surface.

The dynamic contact, or 'tapping' mode is very similar to the non contact mode;

however the amplitude of the oscillations are much larger, typically 100-200 nm, with the tip allowed to touch the surface at the bottom of its oscillation, once more having a knock on affect on the amplitude and frequency of oscillation. The maintenance of a constant amplitude again facilitates the construction of the 3-dimensional image. The tapping mode is considered the most accurate of the methods with very high resolutions, whilst the tip and sample damage is minimised due to the gentle tapping [67]. This is the technique predominantly used throughout this work.

One variation on the standard AFM technique is to pass a small electrical current from the tip into the sample, known as conductive AFM or c-AFM. This technique combines physical and electrical characterisation techniques, allowing fluctuations in current density or SBH to be mapped at the same time as gaining the surface profile.

B.2 Scanning Electron Microscopy (SEM)

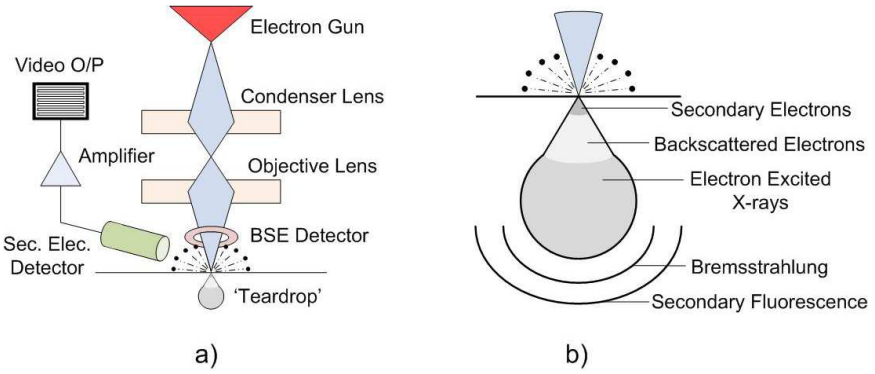


Figure B.2: a) The basic configuration of the SEM and b) a diagram showing the teardrop particle excitation area. Diagrams reproduced from [148].

Figure B.2a shows how the SEM works. The electron beam is generated from an electron gun and focussed using a condenser lens and an objective lens to form a small

spot on the sample surface [148]. As the beam impacts the sample surface, the electrons lose energy through various scattering events and absorbtion, that radiate in a teardrop fashion into the sample from the impact site. The particles that are emitted from the sample depends on the depth of the interactions and Figure B.2b shows the source of the particles from within the teardrop distribution. Right at the top of the teardrop to a depth of only nanometers, electrons collide with, and ionise atoms, losing all their energy in the process. This 'inelastic scattering' frees secondary electrons from the k-orbitals of the sample's atoms and these are emitted in all directions including towards a secondary electron detector. Known as an Everhart-Thornley detector, the secondary electrons are first attracted into the detector via a +400 V grid. A +2000 V bias accelerates the electrons towards a scintillator whereby the energy generated through the electrons impact causes the scintillator to emit flashes of light. These are amplified via a photomultiplier and displayed on an analogue video display, or converted for digital storage. The intensity of the signal is determined by the amount of electrons that reach the scintillator. SEM images appear three dimensional as the angle of incidence of the electron beam to the surface is proportional to the number of secondary electrons that are emitted. Hence, flat perpendicular surfaces appear dull, whilst steeper angles appear bright.

Further into the teardrop, the electrons that have evaded the surface atoms collide with deeper atoms and are rebounded or deflected out of the sample. The intensity of these 'backscattered electrons' (BSE) is determined by the atoms from which they are scattered, with heavy atoms generating the greater intensity signals. The BSE are collected by a BSE detector where the raster scan is again used to create an image, though the information gathered this time is about the elements present in the sample.

Amongst the other particles excited by the electron bombardment, the emission of light, or cathodoluminescence, can be monitored and displayed, whilst X-rays are readily

collected by those SEM fitted with energy dispersive X-ray (EDX) or wavelength dispersive x-ray detectors. These will be described further in Section 4.2.6.

B.3 X-Ray Diffraction (XRD)

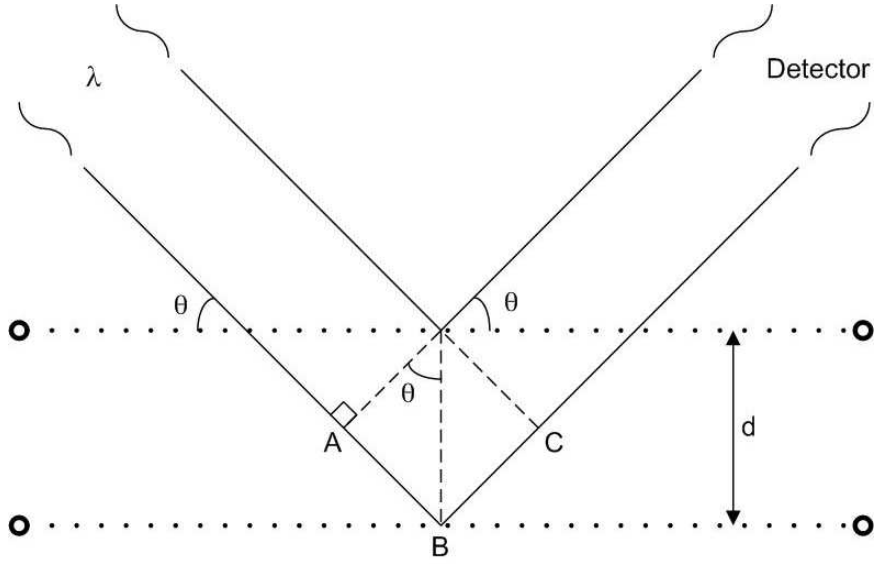


Figure B.3: Bragg's Law.

X-ray diffraction is based on Bragg's law, which is best imagined as two parallel beams of X-rays, approaching a crystalline surface at an angle θ from the horizontal, as in Figure B.3. The top beam deflects off the top layer of the lattice, the bottom beam carrying on to the second layer, a material-specific distance d from the first. It can be seen from Figure B.3 that the bottom beam will have to travel from points A to C on top of what the top beam travels, a distance that is equivalent to $2AB$. AB can be seen to be derived from simple trigonometry as

$$AB = d \sin \theta. \tag{B.1}$$

From this it follows that X-rays with a wavelength λ will be in phase when the following is satisfied,

$$n\lambda = 2d \sin\theta. \tag{B.2}$$

where n is any integer.

In the practical XRD machine, the sample is mounted beneath a beam of X-rays on a tilting platform such that the angle of diffraction for every crystal plane will be satisfied. The diffracted X-ray intensity is then measured and plotted against the angle of incidence. The results can then be compared against known crystal plane responses for the purposes of identification. The intensity of the X-ray diffraction pattern can be used to determine relatively how much of each crystal type there is.

B.4 Energy Dispersive X-Ray (EDX)

When a particle such as an electron from an SEM system is fired at an atom, it will often displace an otherwise stable, unexcited electron from its place of rest in the atom's inner shells. Figure B.4a and B.4b shows an inner most electron being displaced by an external particle, though an electron from any of the other rings could equally have been displaced. This leaves a hole where the electron was and Figure B.4c shows how electrons of higher energy in the outer shells will always come down in energy to fill the gap. In the process an X-ray is expelled equal in energy to that lost by the demoted electron. Figure B.4c shows that for three shells electrons can be demoted in one of three ways, giving off an X-ray of a unique energy, $K\alpha$, $K\beta$, or $L\alpha$, depending on whether the electron has come from the middle or outer shell and if the latter, whether it has jumped one or two shells. The final result for the atom is shown in Figure B.4d, where it ends up with an electron hole in the outer shell.

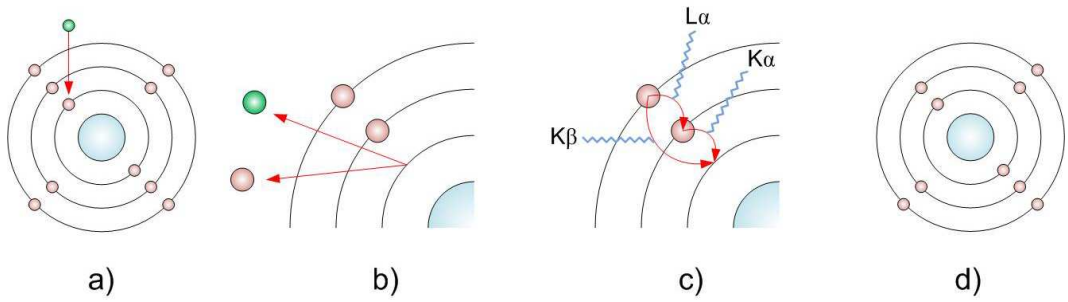


Figure B.4: The stages by which an electron is displaced by an external particle, and electrons of higher energy are demoted to take their place, giving off an x-ray in the process.

Considering again the macroscopic scale, the bombardment of electrons onto a sample leads to the emission of many X-rays, each having an energy relating to an electron demotion event. The EDX spectrometer gathers in the X-rays and maps their quantity against their energy. Hence, using the known codes that relate to an elements $K\alpha$, $K\beta$, or $L\alpha$ energies, one can determine the elements present within a sample.

Appendix

C Derivation of the Capacitance-Voltage Equations

The original theory of the C-V technique [65, 149] states that, for an abrupt junction, a linear relationship will exist between an applied voltage and the inverse square of the capacitance. Here this relationship will be derived.

A small AC signal, approximately 10 mV in amplitude and at a frequency between 10 kHz and 1 MHz, is imposed upon a DC voltage increasing from some reverse bias towards a positive voltage, typically -3 to 2 V. This varies the amount of charge on the on the metal (Q_M) semiconductor (Q_S) sides of the capacitor, which must be equal and opposite, and hence,

$$C = -\frac{dQ_M}{dV_A} = \frac{dQ_S}{d\psi_{bb}}, \tag{C.1}$$

where ψ_{bb} refers to the total band bending brought about by the built-in potential (ψ_{bi}) and the applied voltage V_A. An incremental increase of the reverse potential over a metal-semiconductor junction, will have a knock-on increase in the size of the space charge region width (W), and hence the charge in this region (Q_{SC}). The impact on Q_{SC} may be written

as,

$$Q_{SC} = qA \int_0^W (N_D - N_A + p - n)\, dx \approx qA \int_0^W N_D dx \tag{C.2}$$

presuming that $N_D \gg N_A, p, n$. Presuming that N_D is constant over the space charge region then Eq. C.2 may be rewritten as,

$$Q_{SC} = qAN_D dW. \tag{C.3}$$

Here we presume that $Q_S = Q_{SC}$; a presumption that we have to further explore later. However, we may now combine Eq's. C.1 and C.3 to produce,

$$C = qAN_D \frac{dW}{d\psi_{bb}}. \tag{C.4}$$

The AC signal constantly changes the width of the depletion region (W) given that,

$$W = \sqrt{\frac{2K_S\varepsilon_0\psi_{bb}}{qN_D}}. \tag{C.5}$$

As W varies, so too does the capacitance, given that the capacitance in the space charge region is analogous to that across the parallel plates of a capacitor,

$$C = \frac{\varepsilon A}{d} = \frac{K_S\varepsilon_0 A}{W}, \tag{C.6}$$

though the width of the semiconductor region (W) replaces the distance between the plates (d) and the semiconductor permittivity ($K_S\varepsilon_0$) replaces the permittivity of the dielectric (ε). Differentiating Eq. C.6 with respect to voltage and rearranging gives,

$$\frac{dW}{d\psi_{bb}} = \frac{dCK_S\varepsilon_0 A}{C^2 d\psi_{bb}}. \tag{C.7}$$

Substituting Eq. C.7 into Eq. C.4 and rearranging gives,

$$-\frac{2}{N_D K_S \varepsilon_0 A^2} = -2C^{-3}\frac{dC}{d\psi_{bb}}. \tag{C.8}$$

Integrating $-2C^{-3}dC/d\psi_{bb}$ leaves $dC^{-2}/d\psi_{bb}$, and this can be substituted into Eq. C.8 and rearranged to give,

$$\frac{dC^{-2}}{d\psi_{bb}} = -\frac{2}{K_S \varepsilon_0 A^2 N_D}. \tag{C.9}$$

This result shows how the gradient of a $C^{-2} - V$ plot may theoretically be used to extract the doping of a semiconductor. The above derivation may be worked through for p-type material also, the result of which being a

$$\frac{dC^{-2}}{d\psi_{bb}} = \frac{2}{K_S \varepsilon_0 A^2 N_A}. \tag{C.10}$$

Hence, considering C.9 and C.10 an overall expression for the C-V technique may be arrived at, given that $\psi_{bb,n} = -(\psi_{bi} + V_A) - \beta$, $\psi_{bi,n} < 0$, $\psi_{bb,p} = \psi_{bi} + V_A - \beta$, and $\psi_{bi,p} > 0$:

$$\frac{C}{A} = \sqrt{\frac{\pm q K_s \varepsilon_0 \left(N_A - N_D\right)}{2\left(\pm\psi_{bi} \pm V_A - \beta\right)}}, \tag{C.11}$$

where the pluses are used given $N_A > N_D$, and the minuses if $N_D > N_A$. The C^{-2} against V_A plots should be linear when a reverse voltage is applied to the diodes. Hence, doping values may be found from the slope of the plot, and the built-in potential may be found by extrapolating the data points down to where they meet the x-axis, given that this will be where $\psi_{bi} - V_A \Rightarrow 0$. This may be seen as the point where the conduction or valence bands have flattened, eradicating the space charge region, and hence C tends to infinity.

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