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Design and characterization of GaAs multilayer CPW components and circuits for advanced MMICs

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Abstract

With the demand of modern wireless communications, monolithic microwave integrated circuit (MMIC) has become a very promising technique as it is mass-productive, low loss and highly integrated. Microstrip and Coplanar Waveguide (CPW) are both widely used in MMIC. Particularly, CPW has seen a rapid increase on research works recent years due to its unique capability including having less parasitic contribution to the circuit.

In this thesis, a novel 3-D multilayer CPW technique is presented. Semi-insulating (S.I.) GaAs substrate, polyimide dielectric layers and Titanium/Gold metal layers are employed in this five-layer structure. The active devices are based on GaAs pHEMTs technology provided by Filtronic Compound Semiconductor Ltd. The fabricated components are simulated and characterized by Agilent Advanced Design System (ADS) and Momentum E.M simulator. A novel Open-short-through de-embedding technique is developed and applied to the passive circuits in order to reduce the impact of pads on probing.

A new library of components and circuits are built in this work. Various structures of 3-D CPW transmission lines are designed and characterized to demonstrate the low-loss and highly compact characters. Meanwhile, the influence of various combinations of metal and dielectric layers is studied in order to provide designers with great flexibility for the realization of novel compact transmission lines for 3D MMICs. The effect of temperature on the performance of the transmission lines has also been investigated. Moreover, a set of compact capacitors are designed and proven to have high capacitance density with low parasitics. Finally, based on the extraction of pHEMT parameters from circuit characterization and analysis program (IC-CAP), RF switch and active filter MMICs have been designed and simulated to provide references for further development of 3-D multilayer CPW circuits.

Declaration

I declare that no portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

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List of Publications From This Work

[1] **J.Lu,** A. A. Rezazadeh, 'Characterization of CPW multilayer MIM capacitors for MMICs', in preparation.

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[3] J. Yuan, A. A. Rezazadeh, **J. Lu**, Q. Sun and V. T. Vo, 'Design and temperature Dependent Analysis of GaAs Multilayer Transmission Lines,' Proceedings of European Microwave Integrated Circuit (EuMIC) Conference, Amsterdam, October 2008, pp. 378-381. (This paper was awarded PhD Student Fellowship by The GAAS® Association at this conference)

[4] J. Yuan, A. A. Rezazadeh and **J. Lu**, 'Microwave and Thermal Analysis of 3D Transmission Lines in Multilayer MMICs,' Submitted to IEEE Transaction on Advanced Packaging.

[5] Q. Sun, J. Yuan, **J. Lu**, A. A. Rezazadeh, L. Krishnamurthy, V. T. Vo, 'Compact Multilayer CPW MMIC Spiral Directional Couplers and Bandpass Filters', accepted as oral paper to be presented at European Microwave Conference Week, Paris, September, 2010.

Chapter 1 Introduction

1.1 Introduction

Wireless communication is playing a very important role in modern electronics industry. With the ever increasing demand of higher data rate, compact device size and better power efficiency, Monolithic Microwave Integrated Circuits (MMICs) have earned more attention. Such wireless services include wireless local area network (WLAN), point-to-point digital radio links, broadband wireless access systems, video streaming, satellite communication systems and intelligent transportation systems. For the systems evolving in the mm-wave spectrum (over 30 GHz), the inherent capabilities of MMICs make them the only realistic choice. The hybrid microwave integrated circuits (MICs), where different circuit components are integrated together by wire bonding, limits its application in high frequency range. Meanwhile, MMIC is a circuit in which the passive and active components are fabricated on the same semiconductor substrate.

Due to the absent of bonding and soldering, the parasitic associated with MMICs is significantly reduced comparing with hybrid MICs. One of the main advantages of MMICs over other technology is the cheap cost of fabrication in large quantities. It is especially suitable for some complicated and dedicated circuits, proven to be more economical to hybrid MICs. Also, due to the nature of photolithographic masks and fabrication steps of MMICs processing, the reproducibility is fairly good for MMICs. Furthermore, the MMICs are more reliable as circuit integration is not achieved with soldered wires. In other words, it suffers less thermal and mechanical stress than hybrid MICs.

MMIC technology utilizes various semiconductor substrates such as Silicon, GaAs, InP. Silicon technology is still so far the most mature one; it provides a rich library of active and passive components. Nowadays, MMICs predominantly use GaAs as the semi-insulating material due to higher saturated electron velocity and higher electron mobility than silicon, shown in Table 1.1. This allows transistors made from this semiconductor to function at frequencies in excess of 250 GHz. These properties recommend GaAs circuitry in mobile phones, satellite communications, microwave point-to-point links, and some radar systems. Because of the wide bandgap, pure GaAs is highly resistive. Combined with the high dielectric constant, this property makes GaAs a very good electrical substrate and unlike Si provides natural isolation between devices and circuits. This is especially advantageous for MMICs as the active and passive components can be readily produced on a single slice of GaAs.

However, several concerns are raised when applying this semiconductor. GaAs, in contrast with Si which has a nearly perfect lattice, has a very high impurity density, which makes it difficult to build ICs with small structures. So the 500 nm process is a common process for GaAs while 32 nm for Si. Also, GaAs has problems of stochiometric imbalance and thermal unmixing and Silicon doesn't. Furthermore, GaAs is simply more expensive than Silicon.

Properties	Si	GaAs
Intrinsic Electron Mobility at 300 K, $cm^2V^{-1}s^{-1}$	1500	8500
Electron Saturation velocity, cms^{-1}	9×10^6	1.3×10^7
Intrinsic Hole Mobility at 300 K, $cm^2V^{-1}s^{-1}$	450	400
Thermal conductivity at 300 K, $Wcm^{-1}K^{-1}$	1.5	0.46
Dielectric constant	11.9	12.9
Substrate (intrinsic) resistivity at 300 K, Ω x cm	10^3	3.7×10^8
Band gap at 300 K, eV	1.12	1.424

Table 1.1 Electronic and physical properties of Silicon and GaAs [2-4].

Slot-line, Coplanar strip, Microstrip (MS) and Coplanar Waveguide (CPW) are the techniques which been predominantly utilised in the MMICs. Each of these has their own advantages and disadvantages. Microstrip and CPW are the most popular ones in realising MMICs.

Coplanar Waveguide (CPW) invented by Cheng P. Wen [1] in 1969 is a type of planar transmission line used in MICs and MMICs [5]-[8]. The appealing feature of CPW is that all the conductors are on the same side of the substrate, which is uniplanar in construction. This allows fast and inexpensive for mass-production and unparallel performance compared with conventional microstrip designs.

CPWs have received considerable attention due to several advantages offered [9]-[14]: First, it simplifies fabrication; second, it facilitates easy shunt as well as series surface mounting of active and passive devices; it also eliminates the need for wraparound and via holes, and fourth, it reduces radiation loss. Furthermore a ground plane exists between any two adjacent lines; hence cross talk effects between adjacent lines are very weak. As a result, CPW circuits can apply a thicker substrate than conventional microstrip circuits. Also, the characteristic impedance is determined by the ratio of central conductor width and gap between central conductor and ground, so size reduction is possible without limit, the only penalty is that CPW may have higher losses [15].

The integrated level of current GaAs based MMICs is fairly low. This will increase the cost of MMICs as the natural complex process technique and high risks involved. The development turn-around-time is longer for MMICs as the semiconductor fabrication process takes several weeks. The three-dimensional (3D) MMIC technology developed by the University of Manchester has provided a strong foundation towards resolving these issues to some levels. The state-of-art 3D MMIC technology offers a semi-custom MMIC and reduces the development time of

multifunctional MMICs. A great amount of research activity is being carried out at various prestigious research institutes in order to increase the overall packaging density. This technology translates passive components from horizontal to vertical plane of the circuits to create a 3D structure wafer allowing the circuits size to be minimised and subsequently significantly reducing the fabrication cost per circuit.

Comparing with microstrip and conventional CPW designs, by far multilayer CPW technologies still require systematically studies. In this thesis, we present multilayer CPW transmission lines, capacitors, switches and active filters MMICs. Their design, fabrication and analysis are discussed in detail. The combined strength of the CPW and multilayer MMIC technology provides an attractive field for the design of compact low cost MMICs for affordable wireless communications. The 3D designs not only allow cost-effective MMICs but also enable designers to realize innovative circuit architectures. Also, it helps in reducing the total chip area, losses and parasitic associated with the passive components. For example, the well known current crowding problem in transmission lines has been significantly reduced using multilayer technique. The current density in multilayer components is uniformly distributed, thus not accumulating at the edge of the conductor. Therefore the resistive loss in the conducting strip significantly reduced. The multilayer CPW passive and active components are designed, fabricated and characterized to demonstrate the advantages of this technology.

Figure 1.1 shows a cross-sectional view of a multilayer CPW MMIC concept employed in this work. Three conductor layers separated by two dielectric layers are stacked on a semi-insulating GaAs substrate. Metal layers are connected vertically through dielectric windows. Thin film resistors, capacitors, inductors, interconnections and other passive components were designed and realized at the University of Manchester. Active pHEMT devices, protected by a thin Si_3N_4 layer used for integration were prefabricated by Filtronic Ltd.

In this work, all the components designed and analysed are thoroughly simulated using both EM and circuit simulators and an in-depth comparison between measured and simulated results has been carried out. We have used Momentum, ADS and IC-CAP from Agilent, HFSS from Ansoft and Microwave office from AWR. On-wafer measurement is also carried out using Cascade on-wafer probe stations and HP8510 Vector Network Analyzer. The measured S-parameters are then properly calibrated and de-embedded.

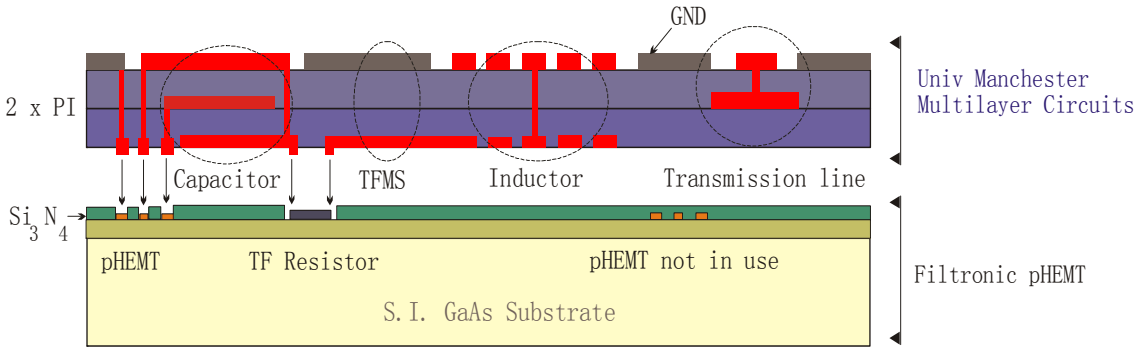


Figure 1.1: Integration of passive and active components in multilayer CPW technology.

1.2 Key objects

The main aims involved in this research work are listed below:

- To carry out review of published theoretical and experimental papers, journal and reports and establish a solid foundation for the development of 3D MMICs.

- To investigate and establish an accurate E.M. simulation knowledge and skills for the development of 3D MMICs using available commercial RF CAD software tools.

- To develop novel simulation techniques to improve the accuracy of the results obtained and compare the results with those data already published and demonstrate the advantages of 3D MMICs.

- To develop a good understanding of different types of calibration techniques available and choose the suitable calibration method for this work.

- To attain in-depth knowledge on different characterization techniques of the involved multilayer CPW components. Identifying solutions to involve these techniques in characterising the components and circuits studied in this work.

- To analyse and establish optimisation techniques for the multilayer components and exploit the flexibility available in multilayer technology in achieving low cost components with reduced area.

- To investigate the thermal behaviour of the multilayer components including understanding of physical background behind any variations observed and the effects that the incorporation of the variations in the circuit parameters.

1.3 Overview of the thesis

This thesis has five chapters.

In chapter 1 presents a general overview of the research work. Motivation and key factors of the related technologies of this PhD work are also included.

Chapter 2 presents the in-depth literature survey on different CPW based passive

components and the current models available for them. Background theories as well as appropriate formulas are introduced and discussed. In particular, components such as transmission lines, capacitors, switches and active filters need thorough understanding of their functionality and modelling techniques. Analytical formulas required in designing the CPW based passive components have been discussed in detail.

In Chapter 3 experimental techniques and tools used in designing the multilayer MMICs have been presented. Sophisticated software simulation tools, both EM and circuit simulators are studied and their advantages and disadvantages are discussed in detail. Accurate RF measurement always needs a perfect calibration to remove all probe parasitics involved and give accurate results. Different types of calibrations techniques and ambient temperature control system have been studied discussed in this chapter. The de-embedding scheme employed in this work has been presented and discussed.

Chapter 4 discusses both DC and RF, measured and simulated results of the multilayer CPW passive and active components. Section 4.1 presents the design and layout of the multilayer CPW transmission lines with various characteristic impedance. It is shown that one can take advantage of multilayer structure to provide low dissipation loss by reducing current crowding effect at conductor edges of the conventional CPW transmission lines. For matching networks, transmission lines with varied characteristic impedance (lower or higher than 50 Ω) are needed. The multilayer transmission lines can be designed to have specified characteristic impedance within a wide range. The designed and fabricated multilayer CPW transmission lines are then measured and characterised at various ambient temperatures to obtain the temperature dependence of their parameters. Their conductor losses and dielectric losses are analyzed. Moreover, the effect of alternative conductor positions within different layers is discussed. Eye diagram is also used to discuss the behaviour of 3D

transmission lines.

In section 4.2, multilayer MIM capacitors are investigated. Folded designs are proven to be have higher capacitance density per unit area than the conventional MIM capacitors. The designed capacitors are then modelled using five lumped elements. Series resistance, Q factors, resonant frequency and other parameters are used to characterize the designed capacitors. A novel concept of parallel capacitors is studied in this section to provide flexibility of designing multilayer capacitors.

In order to demonstrate the integration of proposed compact multilayer CPW passive components designed and fabricated in the University of Manchester with double channel pHEMT prefabricated on S.I GaAs substrate manufactured by Filtronic, switches and active filter applying multilayer CPW technology are designed and studied.

In Chapter 5, the key objectives achieved in this project are presented. Some potential future work are also identified and discussed.

Chapter 2 Literature review

2.1 Introduction of MMIC technology

2.1.1 Brief history of MMICs

The concept of integrated circuits was first presented by Kilby [16] in 1959 in Texas Instruments. In early 1960s initiated by Moll [17] follow with several publications [18-20] started the rapid growth of integrated circuits applications. The first Silicon based monolithic microwave integrated circuit was introduced by Ruegg [21] in 1964. The device was an analogue FET switch but with a very poor switching speed due to the low mobility of the Silicon substrate as shown in Figure 2.1. Microstip lines, reported by Wheeler [22-26] in mid 1960s, have been an important development to the technology. Among these publications, [25-26] are recognised as the origin of GaAs based MMIC technology which feature a simple Schottky diode circuit (Figure 2.2)

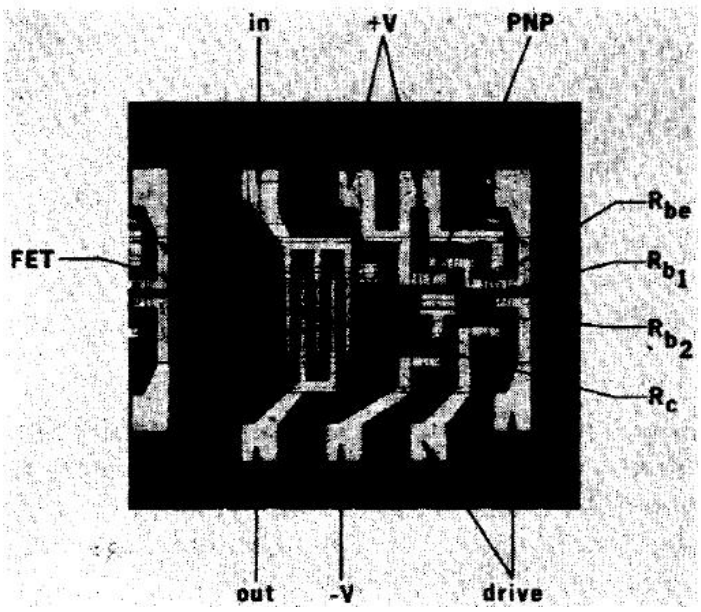


Figure 2.1: The analogue FET switch based on Silicon MMIC technology [21].

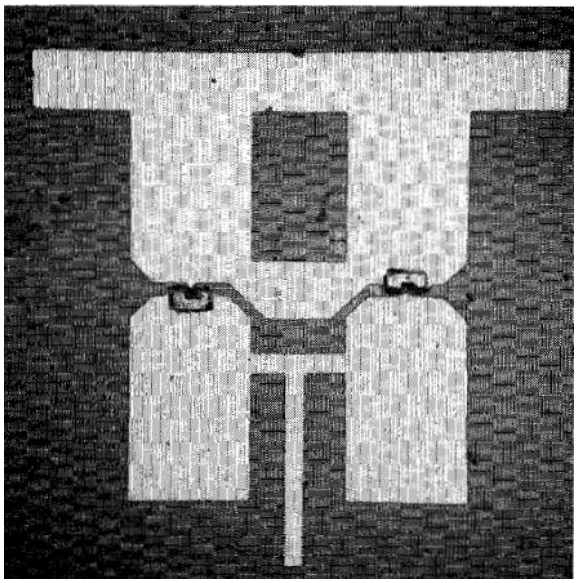


Figure 2.2: Monolithic balanced mixer circuit [26].

In 1976, Pengelly and Turner [27], who were acknowledged as the inventor of MMICs reported a GaAs FET amplifier which known as the first practical MMIC. This single-stage amplifier is shown in Figure 2.3 and provided 5 dB of gain at X-band using 1 μm optically-written gates. The lumped element matching network of the amplifier was designed by computer optimisation and no DC block was applied in the work.

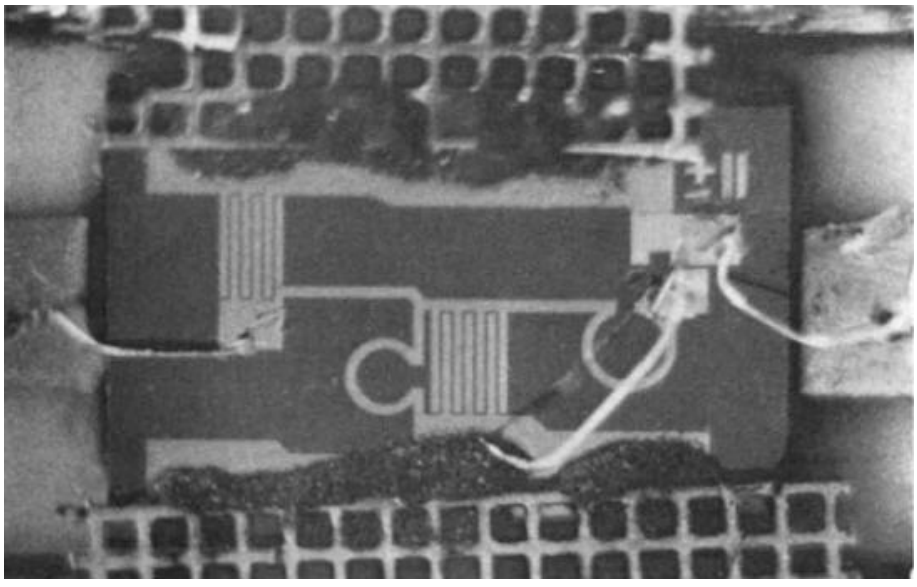


Figure 2.3: Realisation of monolithic FET amplifier chip [27].

2.1.2 Advantages and disadvantages of MMICs

In hybrid MICs, solder or conductive epoxy are used to bond on-chip and off-chip components on a common substrate. It suffers from existence of large parasitic, as various parts of the MIC circuit need to be connected as part of the assembly.

The purpose of using MMIC technology instead of hybrid MIC technology is to remove the need for any kind of gluing, soldering, wire bonding and so on, and hence there are no extra parasitic surrounding the components, ensuring better broadband performance and higher operation frequencies.

	MMIC	**Hybrid MIC**
Cost	Cheap in large quantities Cheap for complicated circuits with large number of components	Cheap for simple circuits and with automated assembly
Choice of components	Limited choice of components	Vast selection of components
Parasitics	Less unwanted parasitic Can be controlled	More unwanted parasitic from bond pads/bond wires Cannot be controlled
Performance	Good broadband performance	Limited bandwidth performance
Frequency of operation	Good performances to well over 100 GHz	Very hard to realize above 30 GHz
Assembly work	Minimal	Can be difficult and time-consuming to assemble
Reproducibility	Very good	Poor
Reliability	Very good	Adequate
Size, weight and layout area	Very small and light in general Must miniaturise area as much as possible to stay commercially competitive	Larger and heavier than MMICs Less pressure to miniaturise layout as substrate is low cost
Turnaround and post-fabrication modifications	Typically 3-6 months Cannot make any changes to the design after fabrication	Typically a few days Possible to tune after fabrication
Investment required	Very expensive to start up	Little investment required to start up

Table 2.1: Advantages and disadvantages of MMICs and hybrid MICs [28].

Chip size(mm^2)	Yields (%)	Working circuits per 3 inch wafer	Cost of single chip at $4000 per wafer ($)
1 x 1	80	3600	1.1
2 x 2	70	800	5
5 x 5	45	80	50
7 x 7	30	25	160
10 x 10	20	9	440

Table 2.2: Effect of chip size on fabrication cost in 1995 [28].

Table 2.1 lists the advantages and disadvantages of MMICs comparing with hybrid MICs and Table 2.2 shows the approximate chip fabrication cost in 1995 against chip size for a high yield MESFET process using ion-implantation.

2.1.3 Multilayer implementation

A conventional CPW on a dielectric substrate consists of a centre strip conductor with semi-infinite ground planes on either side as shown in Figure 2.4. This structure supports a quasi-TEM mode of propagation, so there will be no low frequency cut-off [1]. Other advantages for coplanar waveguide application in MMICs are described in [30].

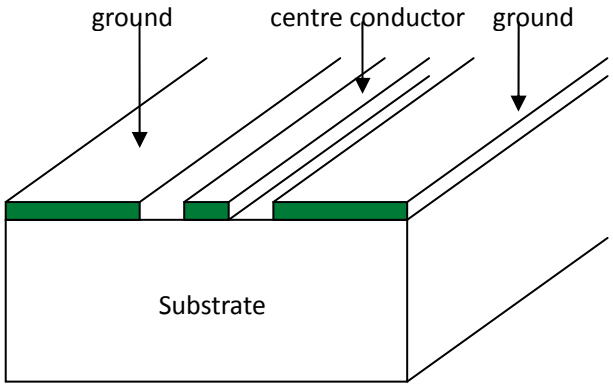


Figure 2.4: Structure of coplanar waveguide.

At millimetre-wave band, it is essential to employ huge amount of passive components in order to achieve different functions such as matching, biasing, phase shifting, coupling and filtering. As a result, the passive devices on chip often take up far more space than the active ones. This will significantly degrade the chip cost-effectiveness.

One of the low-loss, efficient, highly integrated single-chip solution is that the three-dimensional multilayer CPW design. Miniature transmission lines and structure stacking effectively reduces the circuit area. The design has less parasitics loss because of the narrow strip conductor width and the thin polyimide film thickness. Meanwhile the distance between adjacent line segments is wide enough to practically eliminate the undesired coupling effect [31].

It is desirable to use high-impedance lines for applications such as reduced-size couplers and nonlinear transmission lines. On the other hand, ultra-low impedance transmission lines are needed in matching networks where low-impedance devices such as power field-effect transistors (FETs) or photodiodes are used. The range of the characteristic impedance of conventional CPWs is limited. The maximum value is limited by the practical size of the slot and the width of the centre line, while a

practical low limit is imposed by fabrication of the very narrow slot, and the high losses resulting from current crowding at the conductors edges [29]. In multilayer structures, one can simply lift the centre conductor to get higher impedance without narrowing the width. For realization of very low impedance, the centre conductor can be extended under the ground metal, resulting in very high capacitance per unit length. Meanwhile, the conductor gap width limitation and high current crowding can also be overcome by employing a V-shaped centre conductor [32].

One problem associated with the CPW is that the ground must be on either side of the signal lines, which increases the complexity of the circuit designs. A potential solution to this is to utilize a multilayer technique in which several metal layers are sandwiched by insulators. This provides microwave engineers the flexibility in designing multilayer structures with improved circuit performance.

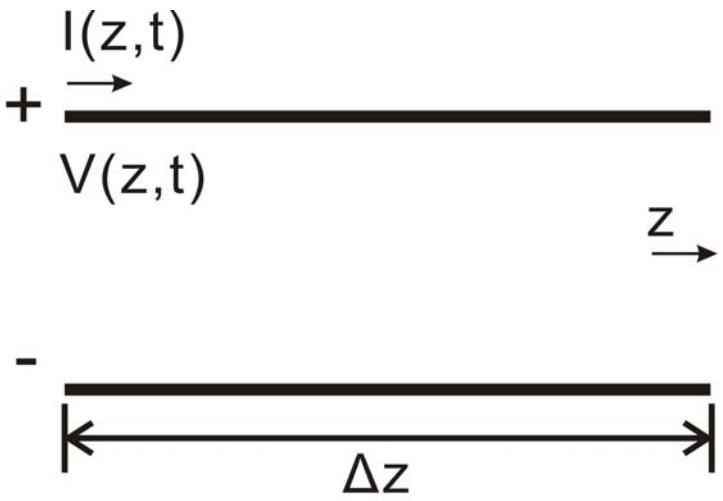
Recent interest in highly integrated monolithic microwave integrated circuit (MMIC) for wireless application has been driven by the expansion of the market for wireless communications and sensors. The thin-film multilayer technology demonstrates that it can be very effective in realization of miniaturization and high-level integration, which results in reduction of chip size and, thus, low cost [33], [34]. The design carried out in [29] had proved to reduce the size of devices by approximately 75%, and significantly improves electrical performance while reducing cost. This technology also offers an effective separation of the application circuit process from the semiconductor active device process, resulting in a much shorter turnaround time.

2.2 CPW transmission lines

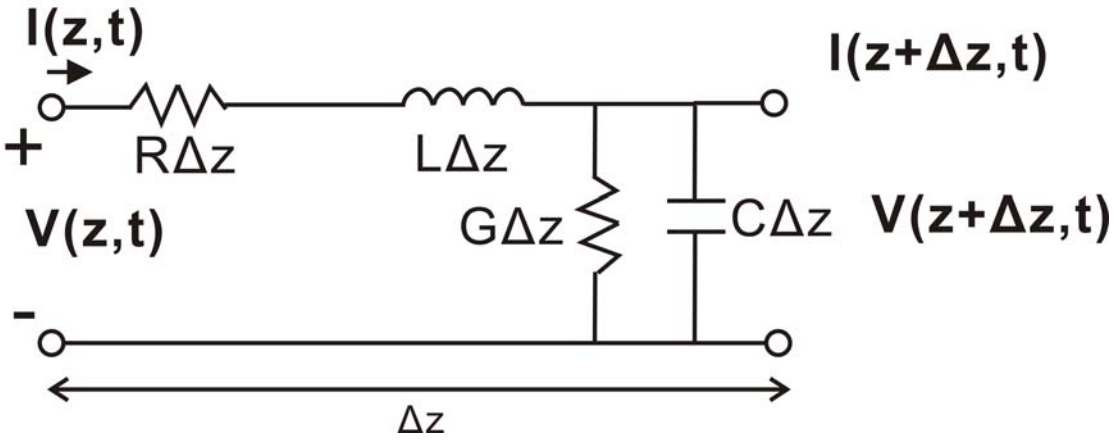
2.2.1 Modelling and characterizing of transmission lines

2.2.1.1 The telegraph model

Transmission line in its simplest form; is a two-wire line structure. Thus a transmission line can be represented by a distributed parameter network, where voltages and currents can vary in magnitude and phase over its length. For efficient transmission of electrical signals, coaxial lines and rectangular waveguides are used at microwave frequencies but these lines can not be used with planar integrated circuits. Therefore in microwave integrated circuits microstrip lines, slot lines, coplanar waveguides and coplanar strips are the most common type of planar transmission lines used. For efficient transmission, coaxial lines and rectangular waveguides are usually employed. Low-loss coax is used mostly at frequencies below 5GHz, while rectangular guide is the popular choice at the higher frequencies.



(a)



(b)

Figure 2.5 Voltage and current definitions and equivalent circuit for a transmission line of length Δz: Voltage and current definition (a) and Lumped-element equivalent circuit (b).

Signal propagation in a single line interconnect is modelled by the Telegrapher's equation [35]. Transmission lines can be represented or modelled by taking an infinitesimal length Δz of wire piece as a lumped-element circuit. The model is shown in Figure 2.5 (a) and (b), where **R**, **L**, **G**, **C** define the following:

R is series resistance per unit length, for both conductors, in Ω/m

L is series inductance per unit length, for both conductors, in H/m

G is shunt conductance per unit length, in S/m

C is shunt capacitance per unit length, in F/m

The series inductance represents the self-inductance of the conductor; and the shunt capacitance is due to the close proximity of the two conductors. The series resistance represents the finite conductivity of the conductor; the shunt conductance is the dielectric loss or leakage due to the non conducting material between the two conductors. Hence the series resistance and the shunt conductance represent the loss in a transmission line. Applying Kirchhoff's voltage and current laws to the circuit shown in Figure 2.5 (b), one can obtain [35]:

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \quad (2.1)$$

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta t,t)}{\partial t} - i(z+\Delta z,t) = 0 \quad (2.2)$$

Dividing Equations (2.1) and (2.2) by Δz and taking limit as Δz → 0 gives the following differential equations.

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \quad (2.3)$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \quad (2.4)$$

These equations are known as Telegrapher's equations and when a sinusoidal wave is applied to these lines, Equations (2.3) and (2.4) are simplified to

$$\frac{dV(z)}{dz} = -(R + jwL)I(z) \quad (2.5)$$

$$\frac{dI(z)}{dz} = -(G + jwC)V(z) \quad (2.6)$$

Solving Equation (2.5) and (2.6) simultaneously:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \quad (2.7)$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \quad (2.8)$$

Where, $\gamma = \alpha + j\beta$ or $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$ (2.9)

And α= attenuation coefficient, in nepers per meter

β= phase-change coefficient, in degrees, or radians, per meter

Also from Equation (2.9), one can see that the propagation constant is frequency dependent and hence the travelling wave solution for transmission line is given as:

$$\begin{cases} V = V_0^+ e^{-\gamma x} + V_0^- e^{\gamma x} \\ I = \dfrac{1}{Z}(V_0^+ e^{-\gamma x} - V_0^- e^{\gamma x}) \end{cases} \quad (2.10)$$

Where, $e^{-\gamma z}$ represents wave travelling in +z direction (forward) and $e^{\gamma z}$ represents the wave travelling in the –z direction (reserve).

2.2.1.2 Characteristic impedance

The characteristic impedance of a transmission line is the ratio of voltage to current waves travelling on the transmission line in the absence of reflections:

$$Z_0 = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-} \quad (2.11)$$

Applying Equation (2.5) and (2.10), it gives:

$$I(z) = \frac{\gamma}{R + j\omega L}(V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}) \quad (2.12)$$

Comparing Equation (2.10) with Equation (2.12), we can derive:

$$Z_0 = \frac{R + j\omega L}{\gamma} \quad (2.13)$$

Applying Equation (2.9) to the equation above:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.14)$$

For a lossless line, R and G in Equation (2.14) are considered as zero so that the characteristic impedance reduces to:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.15}$$

Characteristic impedance, in its Cartesian form, is expressed as Z = R + jX. Resistance R is the real part of impedance; a device with a purely resistive impedance exhibits no phase shift between the voltage and current. Reactance X is the imaginary part of the impedance; a component with a finite reactance induces a phase shift θ between the voltage across it and the current through it. Resistance and reactance together determine the magnitude and phase of the impedance.

2.2.1.3 Wave propagation constant

From Equation (2.9) ($\gamma = \alpha + j\beta$), we can easily write the following form:

$$e^{-\gamma z} = e^{-\alpha z} e^{-j\beta z} \tag{2.16}$$

In the time domain this can be given in the form:

$$e^{-\gamma z} = e^{-\alpha z} \cos(\omega t - \beta z) \tag{2.17}$$

The above equation represents a wave travelling in the +z direction. The rate of signal attenuation of the travelling wave with distance is given by α and the phase variation with distance is given by β. Therefore α and β are defined as the attenuation constant and phase constant respectively [35].

In the time domain, Equation (2.10) can be represented as:

$$V(z,t) = \left|V_0^+\right| \cos(\omega t - \beta z) e^{-\alpha z} + \left|V_0^-\right| \cos(\omega t + \beta z) e^{\alpha z} \tag{2.18}$$

The term V_0^- represents a forward travelling wave and V_0^+ is the reverse wave. The wavelength, λ is defined as the distance between two successive wave peaks. From

Equation (2.18), when z = λ gives out $\beta\lambda = 2\pi$, which leads to

$$\lambda = \frac{2\pi}{\beta} \tag{2.19}$$

Consider the first term in Equation (2.18), to maintain a fixed point on the wave, one meet the condition $\omega t - \beta z = x$, where x is a constant. The phase velocity, v_p in transmission line theory is defined as the speed at which a point of fixed phase propagates, thus we can derive:

$$v_p = \frac{dz}{dt} = \frac{d}{dt}\left(\frac{\omega t - x}{\beta}\right) = \frac{\omega}{\beta} \tag{2.20}$$

Apply Equation (2.19) to (2.20), the phase velocity can be expressed as:

$$v_p = \frac{\omega\lambda}{2\pi} = \lambda . f \tag{2.21}$$

Where f is the signal frequency and λ is the wavelength in transmission line.

2.2.1.4 Effective dielectric constant

Dielectric constant ε_r is used to show how a material slows electromagnetic signal, also known as relative permittivity. The dielectric constant is the ratio of the permittivity of a substance, ε to the permittivity of free space, ε_0 and can be written as:

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0} \tag{2.22}$$

The dielectric constant of a material can be used to quantify how much a material slows an electromagnetic signal. The phase velocity for electromagnetic wave travelling in a lossless dielectric material can be found as:

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{c}{\sqrt{\mu_r \varepsilon_r}} \tag{2.23}$$

Where μ is the absolute permeability and ε is the permittivity the medium. For the free space the phase velocity is the speed of light and can be written as:

$$c = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} \tag{2.24}$$

Applying Equation (2.24) into (2.23) will give:

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{1}{\sqrt{\mu_0 \varepsilon_0 \varepsilon_r}} = \frac{c}{\sqrt{\varepsilon_r}} \tag{2.25}$$

For CPW transmission lines, most of the electric field travels within substrate or dielectric layer while small part of it is constrained in air. Therefore, the concept of effective dielectric constant, $\varepsilon_{r,eff}$ is introduced to reflect the effect of both dielectric material and the air.

Thus, Equation (2.25) can be modified to:

$$v_p = \frac{c}{\sqrt{\varepsilon_{r,eff}}} \tag{2.26}$$

Applying Equation (2.20) to (2.26), the equation of effective dielectric constant is:

$$\varepsilon_{r,eff} = \left(\frac{c}{v_p}\right)^2 = \left(\frac{\beta c}{\omega}\right)^2 \tag{2.27}$$

2.2.1.5 Losses in transmission lines

From Equation (2.9), one can learn the propagation constant consists of 'attenuation constant α' and 'phase constant β'. Due to the attenuation constant, forward travelling voltage waves experiences a reduction in their amplitudes. There are mainly three

types of loss factors, namely dielectric loss, conductor loss and radiation loss, associated with the transmission lines [35].

Radiation losses can also become noticeable with CPW, but this is much lower than with microstrip. It is significant to be able to characterize CPW in terms of these losses because usually their minimization is important. Dielectric loss and conductor loss occur continuously along the length of the transmission structure.

Dielectric loss, α_d, is caused by dielectric absorbing energy. The transferred electric wave penetrates into dielectric, and part of it is absorbed by dielectric. Such absorbed energy results dielectric loss. It is given as a function of the transmission medium filling factor (q), the relative permittivity (ε_r) and loss tangent (tan δ) of the substrate, the effective permittivity and also the wavelength for transmission along the coplanar waveguide as [35]:

$$\alpha_D = \frac{q\varepsilon_r \tan\delta}{\varepsilon_{eff}\lambda_g} \qquad (N_p/m) \tag{2.28}$$

Dielectric loss is dominated by the loss tangent of the substrate material and this tends to be around 0.001 or lower for most substrates. The filling factor and the permittivity are not significant influences upon dielectric loss. Therefore, α_d is relatively low in most transmission lines.

Conductor loss, α_c, dominates the dissipation losses in CPW. It is due to electric energy transforms to heat while electromagnetic wave travels in transmission lines because of metal resistivity. The metal conductor resistivity, skin effect and the influence of surface roughness are important parameters influencing conductor loss. The conductor resistance:

$$R = \rho\frac{L}{Wt} \tag{2.29}$$

where ρ is the metal conductivity; L, W and t is the length, width, and thickness of

conductor strip respectively.

At high frequency, skin effect that currents are concentrated in a small region closed to surface leads to resistance increasing.

$$E = I^2 R \tag{2.30}$$

E is the lost energy due to conductor loss.

Thus the value of R in Equation (2.30) should be minimized to keep a low conductor loss.

In a practical way, dissipation loss is introduced to characterize the loss property of transmission lines. It is defined as the power loss of transmitting signals travelling in a microwave network and can be expressed as the ratio of its output power to its input power.

$$DissipationLoss = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2}{V_{in}^2} \tag{2.31}$$

If we only consider the signal in forward direction, the previous equation can be written as:

$$DissipationLoss = \frac{V_{out}^2}{V_{in}^2} = \frac{V(0)^2}{V(-l)^2} = \frac{\left|V_0^+ e^0\right|^2}{\left|V_0^+ e^{\gamma l}\right|^2} = e^{-2\alpha l} \tag{2.32}$$

where l is the length of the transmission line.

Then the dissipation loss in dB scale can be presented as:

$$\text{Dissipation loss (dB)} = 10 \log e^{-2\alpha l} = 20 \log e^{-\alpha l} \tag{2.33}$$

2.2.2 Types of transmission lines

There are four main types of planar transmission line structures used in MMICs. Microstrip requires a ground plane on the bottom side of the substrate. It is developed by Grieg and Engelmann at ITT laboratories [36]. It has been developed for many years [37-49] and is the most popular transmission line configuration for MMIC applications due to several reasons: Firstly, passive and active elements are easily inserted in series in microstrip structure; also, the metalized ground plane on the back of the substrate can be used both as the mounting surface and the heat sink for heat generated by active devices on the surface; moreover, a large amount of theoretical and experimental data has been developed for microstrip applications and most of the EM software packages are designed for this type of structure. However, we can not deny the difficulty of connecting elements in shunt to ground due to the non-coplanar geometry as well as the thinned substrate for making via holes which is fragile and increases fabrication cost. Furthermore, the parasitic inductance associated with the via holes would degrade the performance at high frequency.

Strip line was invented by R. Barrett [50] in 1955. Strip line is a TEM transmission line media, which means that it is non-dispersive and has very high cut-off frequency [35]. It offers better isolation between adjacent traces than the microstrip simply because of the upper ground plane prevents the electric fields to expand to wide area [51]. The disadvantage of strip line is that the fabrication is more complicated and expensive. Lumped elements either have to be buried between the ground planes or be transferred to microstrip structure to get the components onto the top of the substrate. Moreover, because of the existence of the second ground plane, the strip width of a strip line is much narrower for a given impedance and dielectric thickness than that of microstrip [51].

Slot line was first introduced by Cohn in 1968 [52, 53] as an alternative transmission

line for integrated circuits. Due to its property of radiation, it is normally used in broadband antenna. Slot line is able to obtain a characteristic impedance of 50 Ω with a similar geometry size as those of microstrip line. It also has the advantage in achieving higher theoretical impedance levels than with microstrip for the same dielectric substrate [54]. However, slot line support non-TEM mode of propagation and therefore is quite dispersive and lossy [51]. They also have difficulties to connect devices in series therefore do not allow a great deal of versatility in the circuit layout [55].

As mentioned in Chapter 1.1, CPW has a coplanar geometry with a central conductive strip and two adjacent ground planes on the same surface of the substrate. The effective dielectric constant and characteristic impedance are determined by the dimensions of the centre strip width, the gap, the thickness and permittivity of the dielectric substrate. For CPW, devices and components can be grounded without via-holes, which means it is not necessary to thin down the substrate and the fabrication cost can be reduced. It also suffers much less dispersion loss than microstrip line. Packing density can be increased because the ground lines provide shielding between adjacent signal lines. Last but not least, CPW has the advantage of small radiation at discontinuities.

Low characteristic impedance of conventional CPW lines is achieved by increasing the central strip width and decreasing the slot width. This will cause the dimension size inconvenient for fabrication and any small variation of geometries would lead to unpredictable behaviour. Another disadvantage of CPW transmission line is that because of the ground conductors are on each side of the signal line with small separation distances and this will result in most of the electric field concentrated on the edge of the signal line causing the current crowding phenomenon [56, 57]. The crowded current on the edge of the transmission line will not only increase the dissipation loss but also produce more heat which may damage the surrounding active

devices.

Property	Microstrip	Strip Line	Slot Line	CPW
Attenuation loss	Low	Low	High	Medium
Dispersion	Low	Low	High	Medium
Z_0 range	15-110	20-150	50-300	25-125
Connect shunt elements	Difficult	Difficult	Easy	Easy
Connect series elements	Easy	Difficult	Difficult	Easy

Table 2.3: Comparison of four transmission line configurations [51].

The feature of these four transmission line realizations are summarized in Table 2.3. Considering the fabrication cost and the difficulty of integration, strip lines and slot lines are not suitable for compact MMICs. Meanwhile, CPW offers the most balanced performance among the four configurations and is more compact than microstrip lines.

2.2.3 The proposed 3-D CPW transmission lines

Semi-insulating (SI) GaAs is utilized for substrate in this multilayer structure and polyimide layers can be sandwiched between Au layers. The thickness of Au layer is approximately 0.8 μm. And the isolating polyimide layer is 2.5 μm thick. As one of the advantage that CPW structures have, one can apply a SI GaAs substrate of thickness of 600 μm. All the transmission lines being studied in this work are designed to work at about 10 GHz.

In realizing these multilayer structures, several processing aspects should been

involved including polyimide spin, curing, etching and metal contact formation. In the fabrication of these structures, different layers need to be interconnected properly through the etched windows of the polyimide insulating layers.

The polyimide interconnection windows were formed by oxygen plasma reactive ion etching (RIE) through a photo-resist protecting layer patterned using the lithography process. In order to optimize the polyimide etching process, different polyimide etching conditions had been tried including varying plasma power, chamber pressure and gas flow rate.

A conventional CPW transmission line is shown in Figure 2.6 (a1). The 20 μm centre metal width and 15 μm gap width between centre metal and ground metal are designed to have a characteristic impedance of 50 Ω.

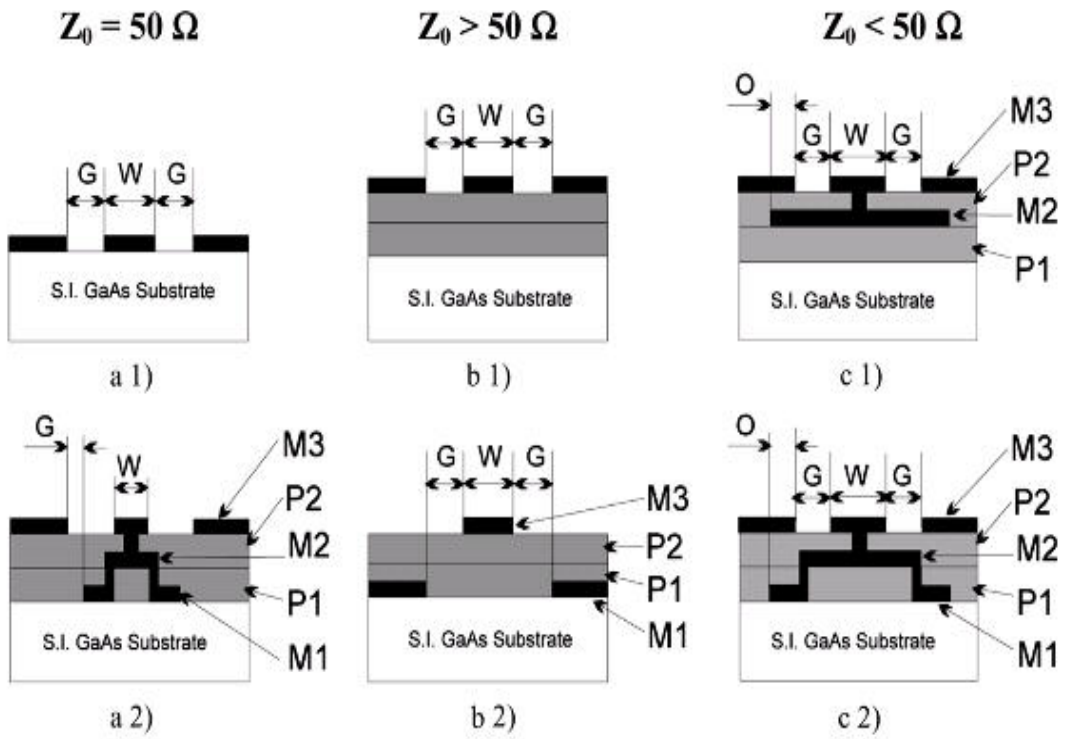


Figure 2.6: Cross-sectional view of multilayer CPW transmission lines with various characteristic impedance.

Another design with 50 Ω characteristic impedance is indicated in Figure 2.6 (a2). In this structure centre metal extend to M2 and M3 layers and meanwhile the same W/G ratio is maintained for 50 Ω characteristic impedance. As the shape of the conductor looks like an upside down "V", it is called V-shape multilayer structure. It will be proved in Chapter 4 to be less lossy as the current crowding effect is eliminated and more electric flux lines "appear" in the low permittivity polyimide layers.

There are mainly two ways to have higher impedance than 50 Ω in multilayer structures. In Figure 2.6 (b1), all the metal is lifted to two layers of polyimide and in Figure 2.6 (b2), the centre metal is lifted to the top. We know that at high frequency,

$$Z_0 \propto \sqrt{\frac{L}{C}} \tag{2.34}$$

Both of the designs can be used to increase the characteristic impedance as the reduction of their capacitance to the ground.

In some application of low-impedance transmission lines, Figure 2.6 (c1) and (c2) can be considered. In (c1), overlap is implemented on M2 layer and in (c2) overlap is employed on M1 layer. The rise of Z_0 is achieved by high capacitance due to overlapped structure. Current density becomes very high at the overlapped section, and loss would degrade the performance. The latter one (c2) can dissipate more heat and resulting in relatively low loss.

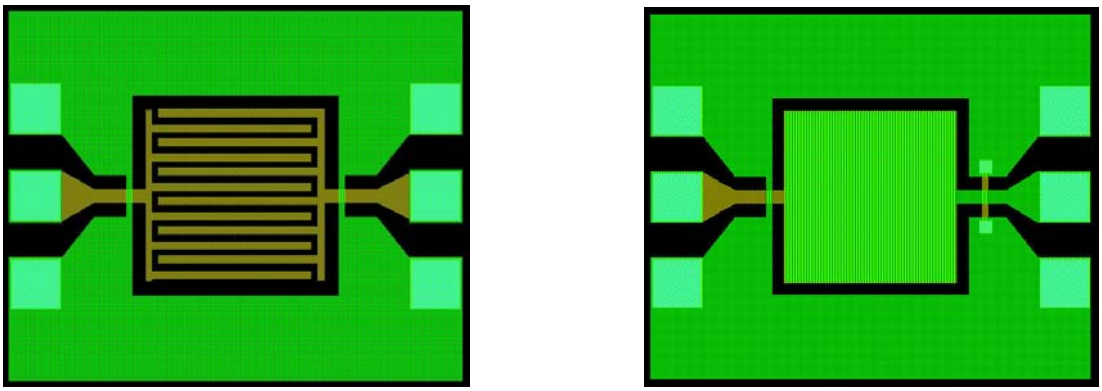
In this study, conventional CPW transmission line (a1), planar on two layers of polyimide (b1), 50 ohm V-shape line (a2) and overlapped (c1) transmission lines are featured in the Chapter 4. Their characterization will be based on scattering parameters measurement on a vector network analyzer (Chapter 3).

2.3 CPW capacitors

Capacitor is one of the key passive components used for building MMIC products. They are often been used for DC coupling, biasing and matching. Today's process technology offer a wide variety of capacitors to designers: metal-oxide-semiconductor (MOS) capacitors, poly-insulator-poly (PIP) capacitors, metal-insulator-metal (MIM) capacitors, junction capacitors, gate capacitors, metal plate capacitors, and metal finger (interdigital) capacitors.

When designing an analogue RF circuit, a designer has to choose between these available capacitors based on their desired properties such as linearity, quality factor, breakdown voltage, area, and sensitivity to process variation, temperature coefficient, matching, cost and performance. The desirable characteristics of an integrated capacitor are low cost, small process variation, low temperature coefficient, low voltage coefficient, low leakage, low noise, low hysteresis, low parasitic ground capacitance, high capacitance density, good matching, high reliability and high yield. For RF circuits, the additional requirements are high self-resonance frequency, high quality factor, high break-down voltage and constant capacitance over the usage frequency range.

Interdigital and MIM capacitors are commonly used in RF MMIC because of their high capacitance density, good voltage linearity, low series resistance and low parasitic capacitance.



(a) (b)

Figure 2.7: Layout of CPW multilayer interdigital (a) and MIM (b) capacitor (Green colour indicates M3 layer and yellow indicates M2 layer).

For the interdigital capacitor design [Figure 2.7 (a)], capacitance arise from capacitive coupling between adjacent metal fingers aided by the dielectric layers. In Figure 2.7 (b), the layout of metal-insulator-metal capacitor is shown. The capacitance of MIM structure is generated by the coupling from two metal layers with the aid of dielectric layer between.

It is obvious that MIM capacitors have less process variation compared to the metal fingers. Hence, manufacturing tolerance of the MIM capacitors can be much tighter [58]. The MIM capacitance is determined by the thickness and the dielectric constant of the insulator between the two plates. Most of the capacitance in the finger capacitors comes from the sidewall (fringing) capacitance between the metal lines, so the metal line space is the dominant factor. It is shown in [58] that the percentage of line width variation for the finger capacitors is much larger than the layer thickness variation of the MIM capacitor; so metal finger capacitors have a much larger tolerance window.

An interdigital capacitor is simulated and compared with an MIM capacitor with the same area (0.16 μm^2). The capacitance can reach 2.1 pF for the MIM structure and only 0.17 pF for the interdigital one. Conventionally, interdigital capacitors have good

application for objective capacitance below 1 pF. From literature [59], we also know that MIM capacitors have better linearity, higher Q factor and smaller temperature variations.

As a passive device, it is desirable in MMICs that capacitors should be kept as small as possible. Meanwhile, small physical dimension means small series inductance. Thus, average AC current path is shorter and self-resonance frequency will be higher. Secondly, capacitors of small size always result in a small series resistance because of short metal length. Therefore, a higher Q factor will be expected.

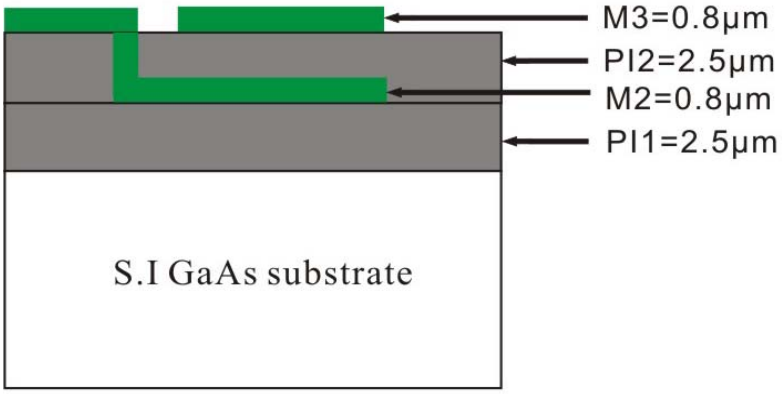
The quality factor, Q is an import figure of merit for the capacitor at high frequencies. This parameter can be defined as the ratio of energy stored to the energy dissipated and is given by [60]:

$$Q = \frac{Power \quad stored}{Power \quad dissipated} \tag{2.35}$$

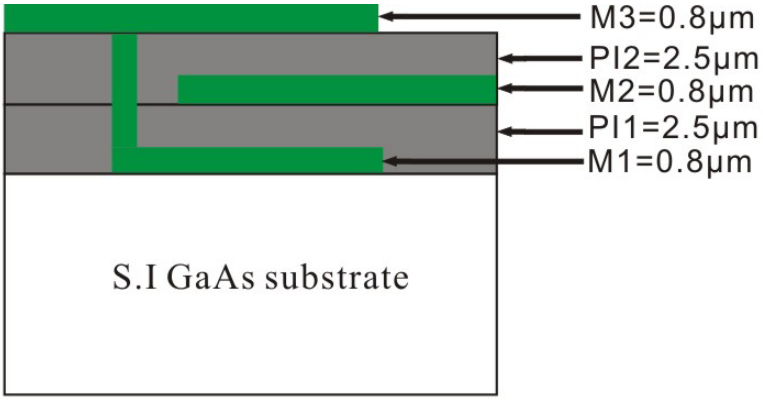
For an ideal capacitor, the Q factor should be infinite, but in reality the series resistance and parasitic capacitance reduce the Q. Improved Q factor can be obtained by increasing the metal thickness, reducing parasitic capacitances and using multilayer dielectric medium [61]. High values of Q are needed to improve the microwave circuit performance such as insertion loss, gain, noise and power-added efficiency.

Multilayer capacitors are advantageous on high capacitance and overall good electrical performances, including low leakage current and high breakdown voltage. In previous work [62], a group of compact 3D MIM capacitors are designed and fabricated. Conventional capacitor (Figure 2.8(a)) is realized by two metal layers and a polyimide layer between them. We placed metal on the top layer (M3) and the next metal layer (M2) in order to minimize the parasitic capacitance from the bottom metal

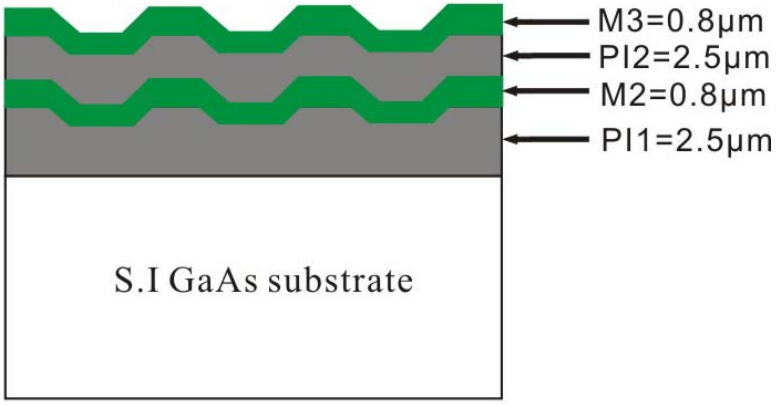
plate to substrate.



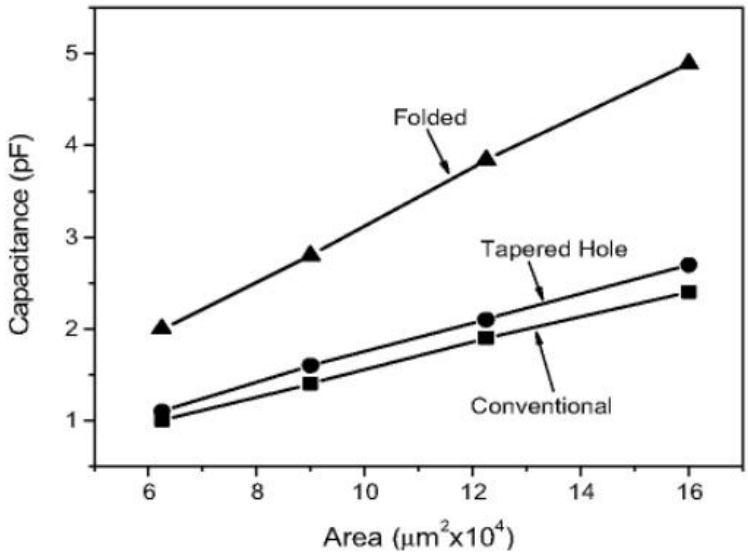
(a) Conventional MIM capacitor



(b) Folded MIM capacitor



(c) Tapered holes MIM capacitor



(d)

Figure 2.8: Cross-sectional view of three different CPW capacitors (a) – (c) and variation of their capacitance with area (d) [62].

Folded capacitor [Figure 2.8(b), also known as MIMIM capacitor] is designed in order to increase the capacitance density. M1 layer is connected with M3 and M2 layer is coupled with both of them so that the effective area is almost doubled compare with the conventional design [Figure 2.8(a)].

For tapered holes design [Figure 2.8(c)], large amount of vias are used to increase the resultant effective area of coupling. It is shown in Figure 2.8(d) that the capacitance density is increased by 20% comparing with the conventional design. One can explain this according to

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{2.36}$$

where ε_0 is the permittivity of vacuum; ε_r is the relative permittivity of the dielectric material, which is the polyimide; A is the area of the capacitor plates and d is the distance between the plates or the thickness of the dielectric material between the plates.

Moreover, it is reported in [63] that resistance could be lowered dramatically by using this “sea of vias” design and thus Q factor is increased at high frequency compared with the conventional design.

In this work, a four-element lumped model is developed for 3-D CPW MIM capacitors up to 10 GHz. Q-factor and cut-off frequency for these multilayer designs are extracted and reported for the first time. Considerations of designing multilayer capacitors are also discussed.

2.4 GaAs based FETs

2.4.1 Introduction to transistors

Transistors are semiconductor devices commonly used to amplify or switch electronic signals. A transistor is normally made of a solid piece of semiconductor material with three terminals. The voltage or current applied to one of the terminals controls the current flowing through other two terminals. Because the controlled power can be much larger than the controlling power, the transistor therefore provides ‘amplification’ to input signals.

Transistors can be divided into two families, bipolar transistors and field effect transistors (FET). The difference between a bipolar transistor and a field effect transistor is the current transport mechanism of the device. For a bipolar transistor, such as bipolar junction transistor (BJT), heterojunction bipolar transistor (HBT), the current flow involves both of the majority and minority carriers. For a field effect transistor, only majority carriers contribute to the current transport. Another difference between the two types of transistors is that the field effect transistors have significant

higher input impedances than the bipolar transistors [64].

Field effect transistors can be fabricated either using Silicon or GaAs. As described in previous section, GaAs based active devices perform much faster than Silicon devices and make them more suitable for microwave and millimetre wave applications. The first field effect transistor was invented by a physicist named Julius Edgar Lilienfeld in 1925, but the practical FETs were made much later and started to be used in microwave circuits from mid 1960s [65-67]. Field effect transistors can be further divided into several categories, i.e. metal semiconductor field effect transistor (MESFET), high electron mobility transistor (HEMT) and pseudomorphic high electron mobility transistor (pHEMT), as shown in Figure 2.9.

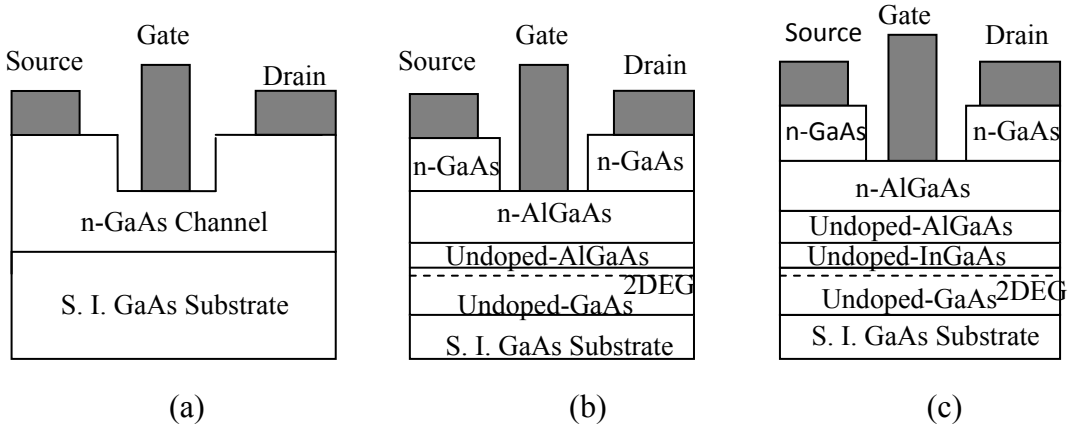


Figure 2.9: Structures of three types of FETs: (a) MESFET, (b) HEMT and (c) pHEMT.

MESFET is a simple field effect transistor that uses the same material for semi-insulate substrate and the active layer. A GaAs MESFET with an n-type GaAs channel is shown in Figure 2.9(a). Although the construction of MESFETs is very simple, they have the problem of high channel resistance. Normally in a field effect transistor, active semiconductor layers need to be doped with impurities to generate mobile electrons. However, the impurities from doping will collide with the moving electrons and increase the effective channel resistance [68].

Unlike MESFETs, HEMTs use the junction between two materials with different band gaps (heterojunction) as the channel instead of a single doped active layer. A GaAs HEMT is shown in Figure 2.9(b), the heterojunction consists of a highly-doped n-type AlGaAs layer as the donor-supply layer and an undoped GaAs channel layer with a very thin undoped AlGaAs layer in the middle. The heterojunction materials form a deep canyon in the bandgap structure, which was referring as the quantum well, limits the electrons from escaping to the n-type AlGaAs layer. Therefore the electrons can only move quickly in the undoped GaAs layer without colliding with any impurities. This phenomenon creates a very thin layer of highly mobile conducting electrons with very high concentration, giving the channel very low resistivity. This layer is called a two dimensional electron gas (2DEG) [68].

A new development made to improve the performances of HEMTs are introduced in 1990s [69-71] and named as pseudomorphic HEMTs (pHEMTs). An extremely thin layer of heterojunction material with different lattice constant, normally is InGaAs, is sandwiched between AlGaAs and GaAs, as shown in Figure 2.9(c). This type of structure enhances the 2DEG and gives pHEMTs better performance than HEMTs.

2.4.2 FETs in switches

FETs are very popular switching elements due to its flexibility of integrating with MMICs. When used in switching applications, FETs can be switched to On-state by reducing the depletion region to open the drain-source channel and to OFF-state by simply shutting down the channel.

However, the requirements for a switch FET are quite different than those of an amplifier FET. Since switch does not involve gain from the device, thus the gate terminal resistance is not important any more. Furthermore, instead of trying to match

the gate terminal to the system characteristic impedance, the gate of a switch FET use the highest practical impedance to prevent RF energy from leaking to the bias network. The most significant difference is the drain-source voltage, V_{ds} of a switch FET is always set to zero, corresponds to the low V_{ds} part of the output characteristics. This configuration helps the switch to achieve low channel resistance and reduce the insertion loss for switches.

2.4.3 pHEMT in this work

GaAs MESFETs, have shown to be capable of excellent microwave performance. However, higher maximum frequency of oscillation (f_{max}) and transition frequency (f_T) can be obtained with a conventional HEMT of the same geometry. On the other hand due to high doping concentration HEMTs suffer from lower breakdown voltage levels than MESFETs [68], which limits their use in high power applications. MESFETs have lower electron mobility and effective saturated velocity is lower compared to HEMTs. On the other hand the current level and gate to drain reverse breakdown voltage in HEMTs need to be increased before the full advantage of a hetero structure for power applications can be obtained. These short comes are overcome in pHEMTs, where multiple interfaces are used achieving better electron transport characteristics. In this work pHEMTs with two fingers prefabricated by Filtronic compound semiconductor Ltd on a 6 inch semiconductor wafer are used. Gate length of a device is 0.5 μm with 100 and 60 μm gate widths are used with later device giving higher f_T and f_{max}. The pHEMTs gates are mushroom structures, thereby reducing gate metal resistance that would result from narrower gate base area [73]. The Schottky contact to the semiconductor is made through standard Pt/ Ti/ Au layered structure. Drain and source contacts are alloyed AuGe/ Ni/ Au and this type of structure has been established as a very stable and robust contact structure. All the discrete pHEMTs are passivated with Silicon Nitride (Si_3N_4), which doubles as scratch protection.

2.5 MMIC switches

2.5.1 Types of switches

Switches are one type of components that can interrupt the power transmission or divert it from one conductor to another. Switches can have multiple poles and multiple throws and an N-poles-N-throws switch is illustrated in Figure 2.10. The switch is able to shut down the power transmission at all branches if the throws are lifted up and continue the transmission by reset the throw conductors back to contact. Microwave switches are commonly used in wireless transmitters and receivers to allocate signals to different processing channels.

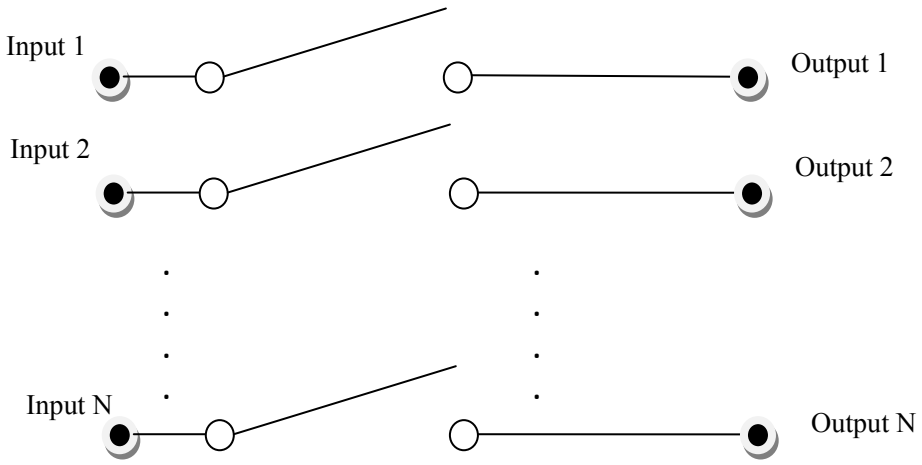


Figure 2.10: A demonstration of a NPNT switch.

Microwave switches can be made of either PIN diodes or FETs. PIN diode switches were developed since mid 1960s and have the advantage of low loss and very good isolation [74-81]. The isolation of PIN diode switch is realized by its low off-state capacitance, of which also makes the PIN diode be able to work at very high frequency. The PIN diode switches have another advantage of the high current handling ability and can be designed to suit many power applications [81-83].

However, the PIN diode has the significant problem in integrating with other components and circuits in microwave circuits. Very few foundries offer PIN diodes on MMICs, and this limits the designing flexibility.

For this reason, switches employing FETs are more popular in MMIC designs and started to develop since late 1970s [84-86]. FET switches can be made of MESFET, HEMT or pHEMT and easily integrated with any MMIC devices, offers great flexibilities to MMIC designers. However, the capacitances introduced by the depletion region of FETs are significant higher than those of PIN diodes, causing the isolation or insertion loss of FET switches to be relatively poor. Also the power handling ability of FETs is lower than the PIN diodes. The comparison of the characteristics of FETs and Pin diodes used as switching elements are listed in Table 2.4.

	1μm MESFET	**GaAs PIN Diode**
Typical ON-resistance	1.5 Ω/mm	1.7Ω
Typical OFF-capacitance	0.40 pF/mm	0.05pF
Breakdown voltage	15 V	30 V
Integration Complexity	Low	High

Table 2.4: Comparison of the characteristics of FETs and PIN diodes for switching [86].

Due to the high depletion region capacitance of FETs, several papers reported circuit optimising techniques for high isolation FET switches [87-89], but the fundamental way to improve the switch performances is to utilizing the FET structure to achieve a relatively low depletion region capacitance [90]. The FET depletion region capacitance is determined by the length and width of the gate contact.

When increase the gate length, the channel resistance of FETs will increase and the

depletion region capacitance will decrease. For the gate width, the channel resistance will be minimised if the gate width is long enough. However, the drawback of increasing the gate width is that it will also increase the depletion region capacitance. Therefore, compromise need to be made for optimum design of switches.

2.5.2 Characterization of switches

The performance of a switch is measured by its return loss, insertion loss and the isolation. A simple illustration of a single pole double throw switch is shown in Figure 2.11, where input port is port 1, output ports are port 2 and port 3. The switching is achieved by moving the throw to either port 2 or port 3.

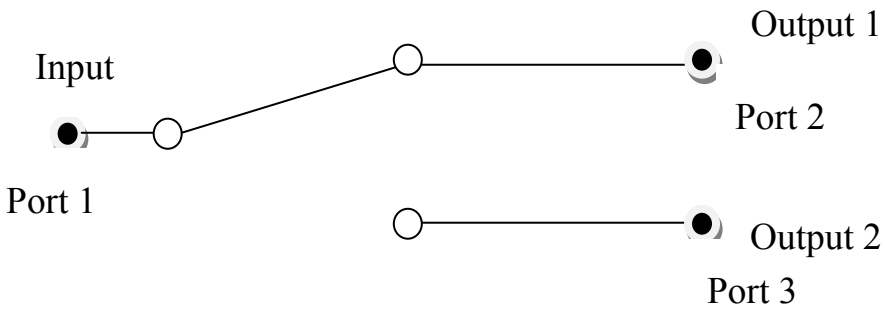


Figure 2.11: Illustration of a SPDT switch.

When the throw is connected to the upper branch of the switch, the power transmits through to port 2 and the lower branch is switched off. Then the reflection loss is defined as the ratio of reflected power to the input power and can be expressed in dB as:

$$\text{Reflection loss} = 10\log\frac{P_{ref}}{P_{in}} = 10\log|S_{11}|^2 = 20\log|S_{11}| \qquad (2.37)$$

The insertion loss is defined as the ratio of the power going through to port 2 to the input power, which can be written as:

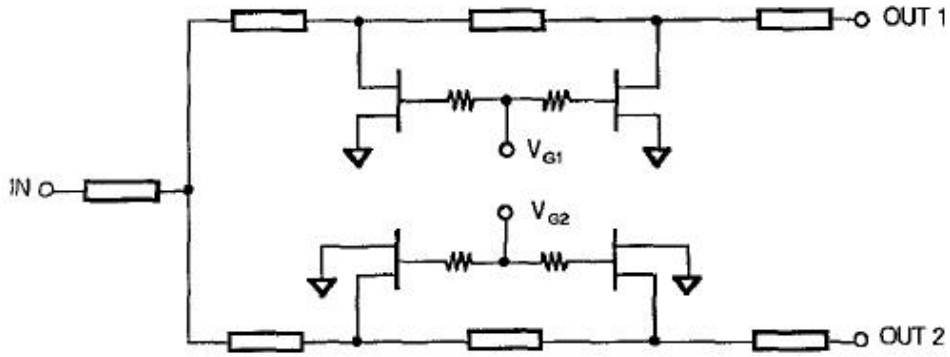
$$InsertionLoss(dB) = 10\log\frac{P_{op1}}{P_{in}} = 10\log|S_{21}|^2 = 20\log|S_{21}| \quad (2.38)$$

The isolation is defined as the ratio of the power leaked to the port 3 to the input power:

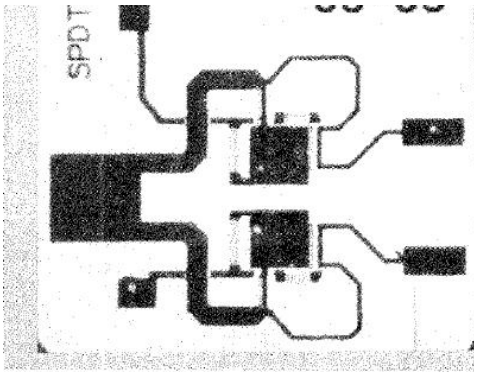
$$Isolation(dB) = 10\log\frac{P_{op2}}{P_{in}} = 10\log|S_{31}|^2 = 20\log|S_{31}| \quad (2.39)$$

2.5.3 Device modelling

A practical microwave switch employs active devices to replace the poles and throws in a concept switch. The schematic and photograph of a DC-40 GHz single pole double throw (SPDT) FET switch is illustrated in Figure 2.12. It uses two transistors as a throw for each branch, the input port corresponds to port 1 of a concept switch in Figure 2.11, output ports 1 and 2 are port 2 and 3 in Figure 2.11. V_{G1} and V_{G2} are the controlling voltage to switch each branch to ON or OFF states. When certain V_{G1} and V_{G2} are applied, the FET 1 and FET 2 are changed to the state of blocking the power transmission and FET 3 and FET 4 to the state of conducting microwave power, and then the signal from input port will flow through to output 1 and no power will go to output 2. This approach is equally the same as connecting the throw of the switch to the upper branch as shown in Figure 2.11.



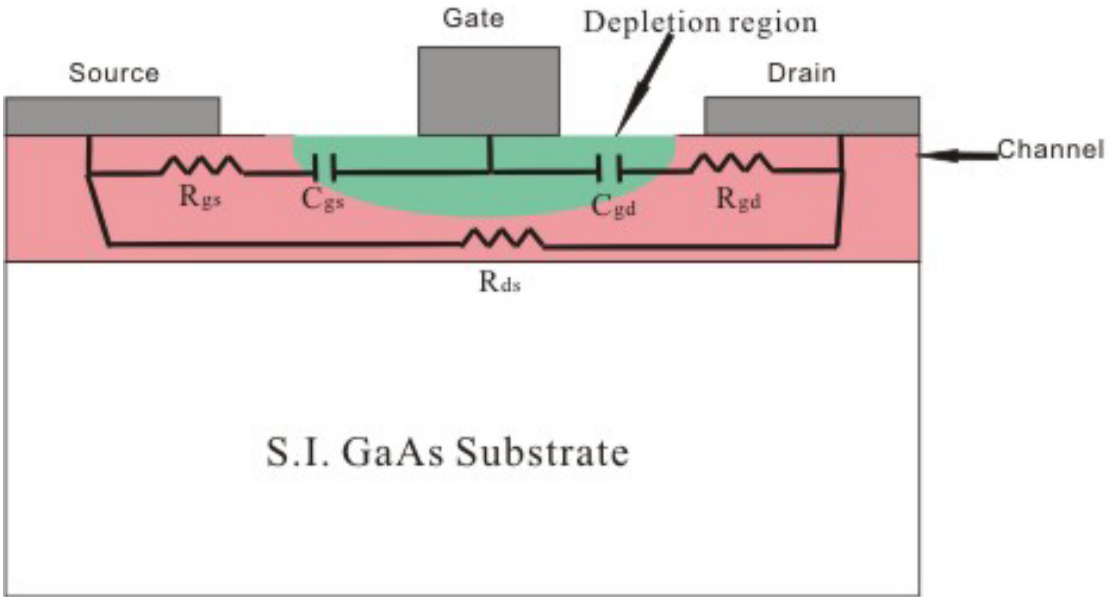
(a)



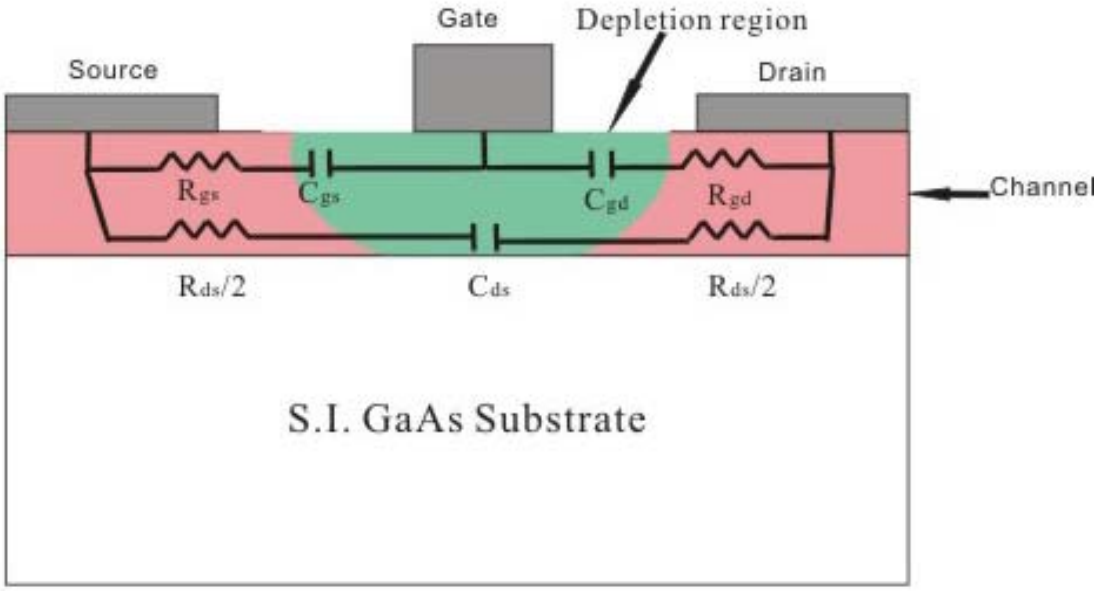
(b)

Figure 2.12: Schematic (a) and photograph (b) of 20 - 40 GHz SPDT FET switch [91].

The way of using FETs in switches is quite different from those of in amplifier applications, even though they may have the same structure. The drain-source voltage, V_{ds} of a switch FET is always set to zero, so the channel is not biased and can not be used to amplify a signal. Moreover, amplifier FETs are commonly grounded at the source but switch FETs may not be RF grounded at all, in the case of a series switch FET. Therefore, the small signal models of common FETs when used as amplifier elements are not suitable for switch design.



(a)



(b)

Figure 2.13 Cross sectional views of the FET switch intrinsic equivalent circuit for the On state (a) and Off state (b) [92].

Compare to the small signal models of amplifier FETs, the model for switch FETs are relatively simple and easier to extract. Simplified cross-sectional views of a GaAs FET in On and Off states and their corresponding equivalent circuits are shown in Figure 2.13.

2.6 MMIC active filters

For fully integrated microwave transceivers, there is considerable interest in filter design for MMIC realization. Unfortunately, at microwave frequencies, the Q factor of the on-chip inductors is typically low and, hence, passive MMIC filters usually exhibit high-insertion loss and poor selectivity.

Active MMIC filters have gained interest due to the attractive features potentially offered by them, such as selectivity and agility realized on chip. Such filters could be used to realize more compact and less complex receiver architectures, thus making more cost effective microwave systems for radar and wireless communications possible in the future.

The advantages of active filters are their small size, high selectivity, and their easy integration with amplifiers, mixers, and oscillators. In addition there is scope for electronic tuning to be used for channel agility. Selectivity requirements derive both from the need to isolate system functions being performed simultaneously in separate frequency bands, and from the necessity to limit external signal interference through control of receiver bandwidth. Size constraints are dictated, in part, by phased-array system concepts being developed, which restrict filter geometries to dimensions commensurate with the close spacing of array antenna elements. Miniature high-performance microwave filters find use in other applications as well, such as in mobile communication equipments and frequency-synthesized signal generators [93].

However drawbacks associated with active techniques are their poor noise figure, limited power handling, and the need for DC power. In addition, whilst very high selectivity filters can be demonstrated in the research lab, in practice these filters are limited by their sensitivity to fabrication tolerances and their environmental sensitivity [94]. A few papers had been published to discuss the noise issue in microwave active

filters [95-97].

In this session, a variety of microwave active filters in different realization will be investigated and discussed.

2.6.1 Active filters based on coupled negative resistance

In 1990, a new coupled negative resistance method to build a microwave active band-pass filter is introduced [98]. Based on this method, four microstrip line end-coupled filters are built.

The coupled-resonator bandpass filter is the most popular structure used at microwave frequencies. It consists of tanks and coupling structures between adjacent tanks. The coupling structures function as impedance or admittance transformers. Usually, these transformers are called J (for admittance transformer) or K (for impedance transformer) inverters. In the case of a lossy tank, the equivalent circuit of the tank circuit contains a dissipating resistor, R_p. This R_p determines the unloaded Q of the tank circuit. Figure 2.14 shows how the coupled negative resistance method works. In this figure, the tank is coupled to an outside negative resistor, R_n. By properly adjusting the negative resistance and coupling value, the dissipating resistor, R_p, can be cancelled out; therefore, a lossless tank may be obtained. In contrast to the active tank described above [99-101], the tank itself consists of only passive elements, and the active device is placed in the outside coupling structure. This concept is realizable in microstrip circuit form. Figure 2.14(c) shows the microstrip active tank circuit using the coupled negative resistance method. The equivalent circuit of this structure is shown in Figure 2.14(b). The half-wavelength microstrip tank is equivalent to a shunt circuit parallel LC tank [102]. All of the losses, such as conductor loss,

dielectric loss, and radiation loss, are represented by a tank dissipating resistor, R_p. The microstrip active tanks are coupled via J inverters to construct an active filter.

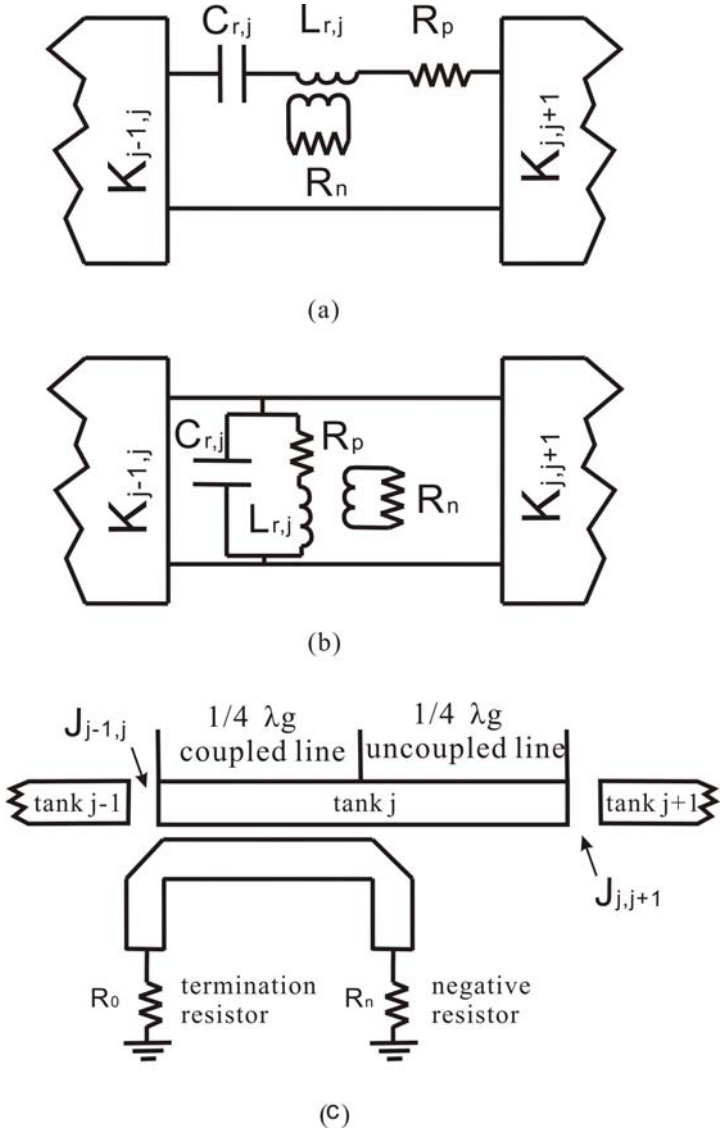


Figure 2.14: The active tank circuit using coupled negative resistance method: series tank with K inverters (a); shunt tank with J inverters (b); active tank (c) realized in microstrip circuit form [98].

The basic structure of an end-coupled active band-pass filter is shown in Figure 2.15. The filter uses the simplest coupling structure, namely the microstrip gap, between adjacent tanks. By varying the gap width, the J inverters may be realized. After these steps the active circuit part is inserted into each tank circuit as shown in Figure 2.15.

The end-coupled filter discussed here is narrowband because of the weak gap coupling.

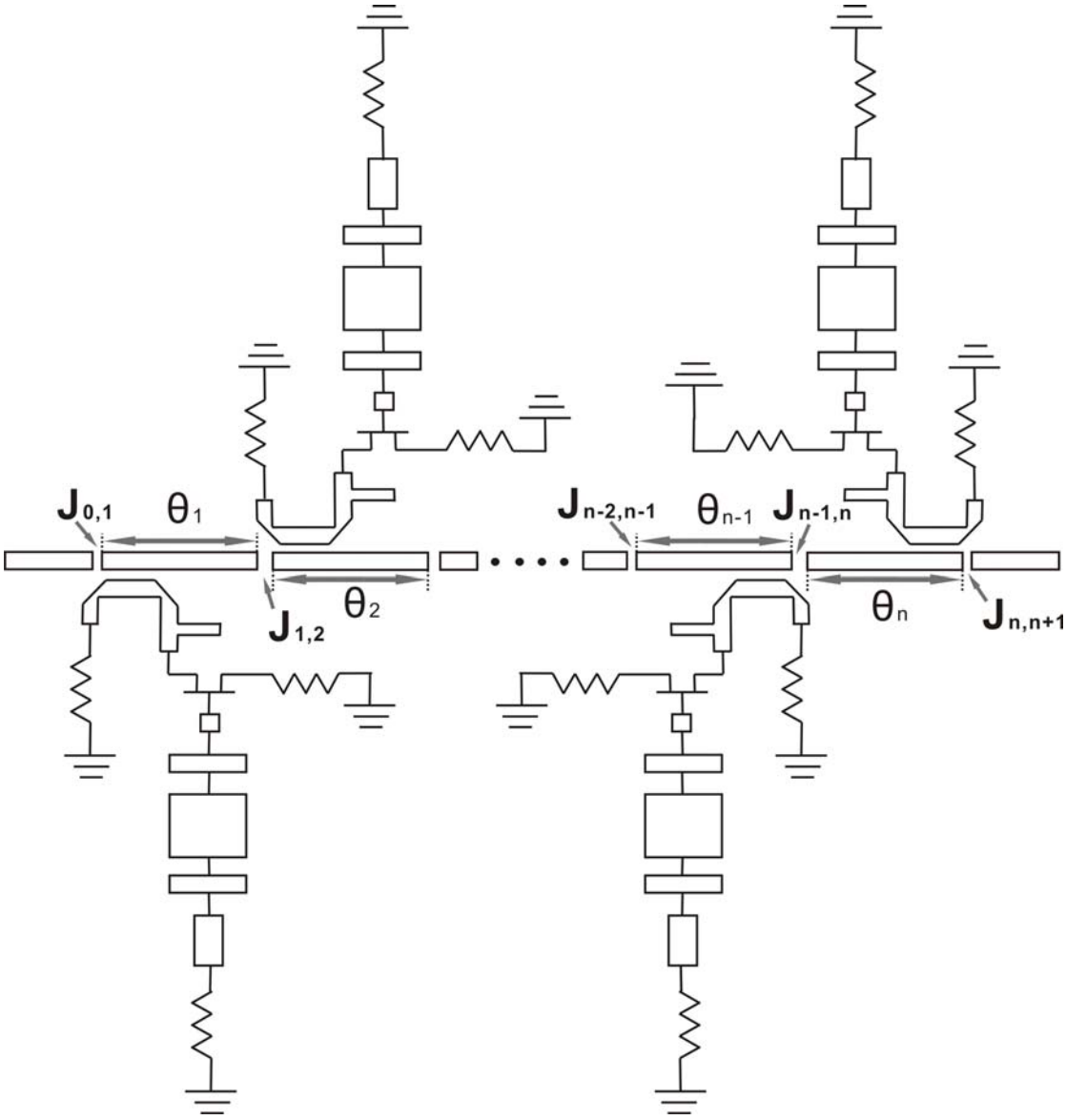


Figure 2.15: The end-coupled active filter [98].

In Figure 2.15, the MESFET's are in series feedback configuration. A low-pass filter is connected to the gate of the MESFET, which makes the MESFET produce negative resistance at a frequency higher than the cut-off frequency of the low-pass filter. The low-pass filter also bypasses the low-frequency signal and therefore prevents low-frequency instability. The source inductor is used to enhance the negative

resistance value.

A systematic study of the in-band noise behaviour of negative resistance compensated bandpass filters has been presented in [97]. A general analytical expression governing the overall noise figure of the filter as a function of circuit and device parameters has also been developed in [98]. This formula suggested that further improvement of noise performance may be achieved by compromising linearity [103].

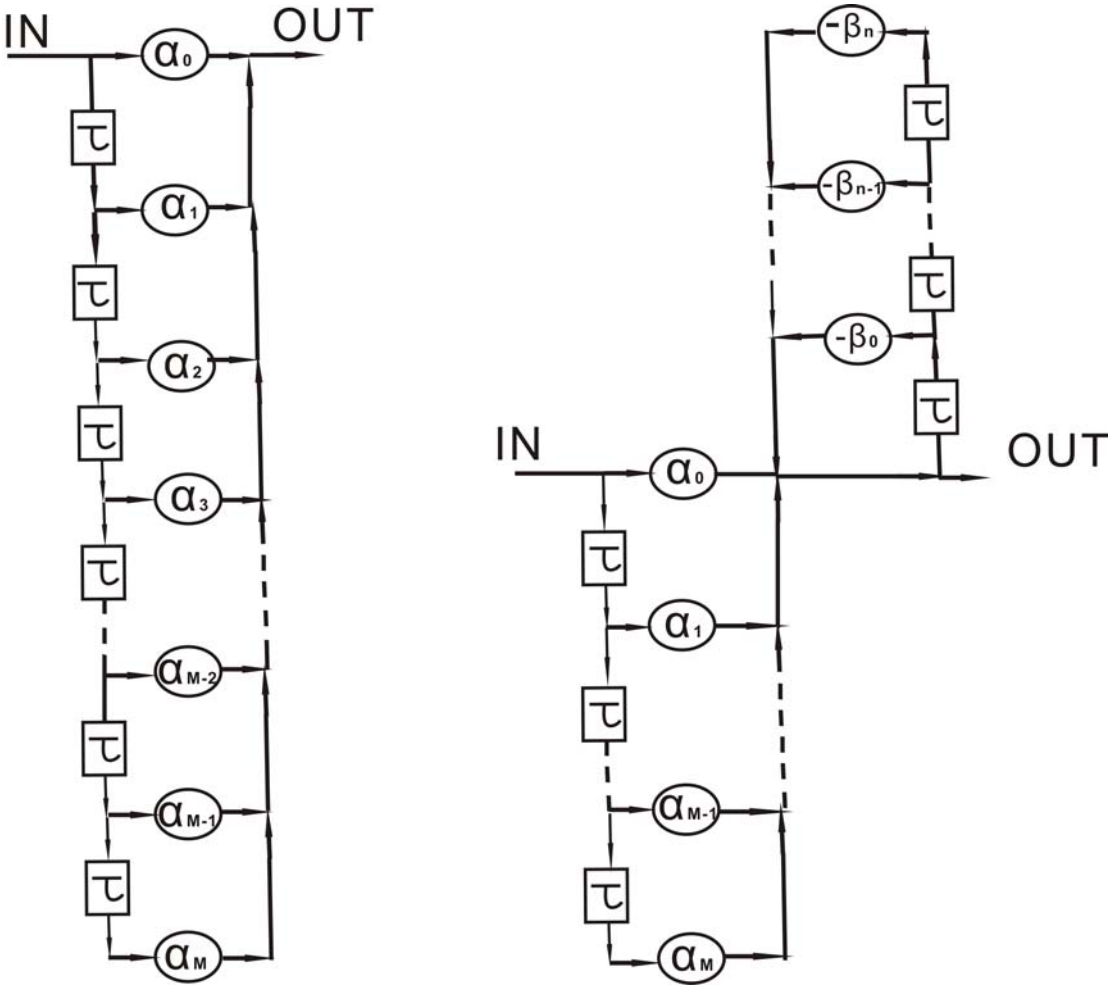
2.6.2 Active filters based on transversal and recursive principles

Transversal and recursive filter concepts, normally associated with discrete-time applications, are adapted for implementation in the microwave frequency range [104]. Principal focus is on microwave active filter designs that permit realization of wide bandwidths, with microwave transistors used as active elements. The study focuses on distributed active filter concepts. Although these concepts are normally associated with applications in the digital domain, they can also be adapted to address analogue filter needs. They are of particular interest in the present context because of their potential for more easily coping with active device constraints relative to gain and time delay at microwave frequencies. The distributed filter structures to be considered are divided into two basic categories.

The first category comprises circuits of the transversal type which, aside from parasitic feedback effects, employ feed forward techniques exclusively.

A flow graph representation of such a filter is shown in Figure 2.16 (a). The underlying design concept displays certain similarities with familiar microwave distributed amplifiers. The fundamental distinction between the two kinds of circuits

is that, in the amplifier case, individual signal components are all combined in-phase, whereas, in the filter case, the frequency selective overall response is derived by combining signal components with different amplitudes and frequency dependent phase delays.



(a) (b)

Figure 2.16: Flow graph examples of distributed filters: transversal filter (a) and recursive filter (b) [104].

The second category in this type of filter is the recursive type. As the name indicates, these filters are based on the use of feedback, generally involving transversal principles simultaneously. Filter responses are again derived through interaction between signal components with appropriate amplitude and phase relationships. The flow graph example in Figure 2.16 (b) depicts one of the numerous ways of

representing such a filter. The additional design freedom offered by the presence of feedback generally translates into more compact circuit realizations. Although the recursive structures give the appearance of being potentially more susceptible to instability than transversal-type circuits, parasitic feedback within typical microwave active two-port devices tend to disallow a meaningful distinction in practical design situations.

Unlike the approaches just outlined, microwave active filters based on transversal principles are neither subject to time-delay-related frequency range limitations, nor are they burdened by stability concerns. This follows from transversal filters establishing frequency selectivity through interference among signal components that derive from the input signal and propagate only in forward direction, rather than through reliance on circuit elements with high Q-factors or dependence on active-circuit feedback schemes.

Transversal based approaches possess one main drawback in that they require large amounts of space to realize filter structures with highly selective, narrowband response characteristics. Size has remained a fundamental concern, despite notable advances in the generalized application of transversal principles [105].

2.6.3 Microwave channelized active filters

The new class of microwave active filters being presented in [105] offers a convenient way to realize miniature filter circuits with sharp passband-to-stopband transitions. The approach, which lends itself to a broad range of narrowband and wideband filtering applications, involves parallel connections of frequency selective, unilateral network branches that contain both passive and active subcircuits. Highly selective filtering action derives from controlled interferences among branch signal components.

Attributes of the new technique include unconditional circuit stability, tolerance for large passive-circuit-element losses, practicability of narrowband lumped-element configurations, graceful performance degradation with active element parameter changes, and the advantage of module-based procedures for design and implementation.

The composite active filter topology that emerges is a parallel connected array of frequency-selective unilateral branches, as schematically shown in Figure 2.17. Aside from passive filter sub-networks, branches also contain means of amplification to establish desired unidirectionality among signal components and adjust relative signal strengths.

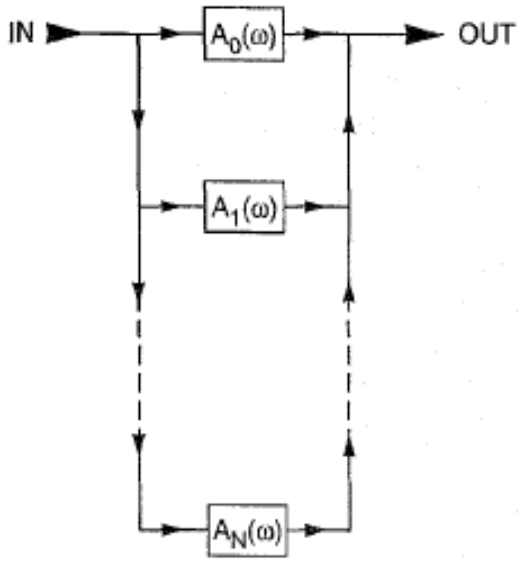


Figure 2.17: Signal flow diagram of a microwave channelized active filter [105].

Among the simplest channelized filters are those designed to produce sharp signal rejection spikes at designated notch frequencies. All that is required to implement a transmission notch is to split an incident signal into two separate components, adjust their responses to be of equal amplitude and out-of-phase at the desired frequency, and recombine the components to form a notched output signal.

With reference to the conceptual block diagram given in Figure 2.18, this can be accomplished with a channelized structure that involves two unilateral branches, one of which being a straight-through channel with no deliberate amplitude frequency dependence, and the other exhibiting bandpass behaviour.

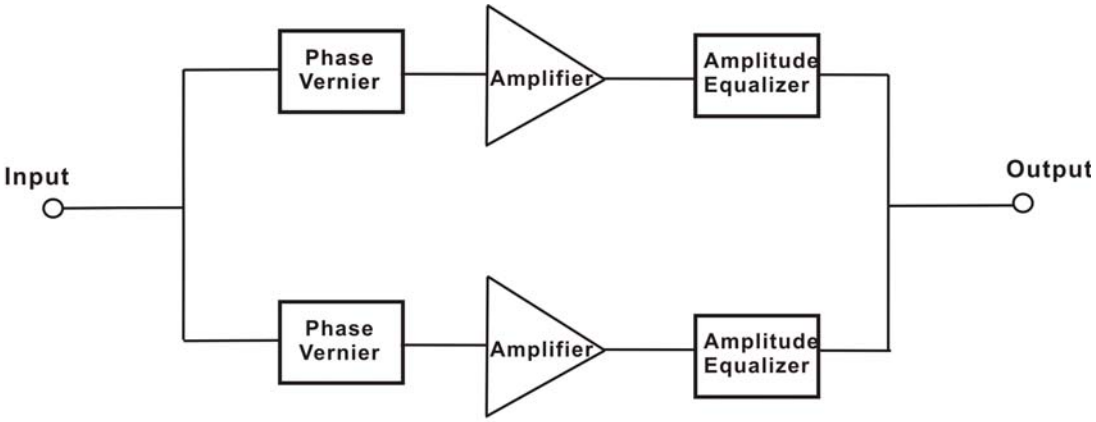


Figure 2.18: Conceptual block diagram of a channelized notch filter [105].

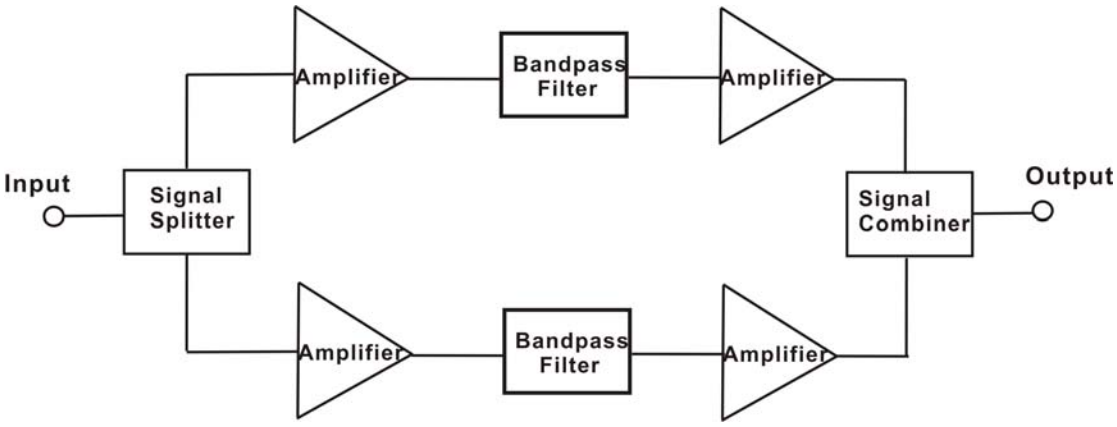


Figure 2.19: Schematic block diagram of a two-branch microwave channelized bandpass filter employing an in-phase power splitter at the input and a power combiner at the output [105].

Another simple way [106] to implement a two-channel bandpass filter is with the help of an in-phase power splitter that divides the incident signal between the two branches, and an in-phase power combiner that merges the two branch signals back into one at the output after passing through respective channel networks. Each channel network

may be configured as a cascade assembly of amplifiers and bandpass filter sections, with a typical arrangement depicted in Figure 2.19. This arrangement is easy to realize, based on the fact that it is made up entirely of 50 Ω referenced building blocks. With the noted toleration for passive-element losses, circuits can be made very compact through reliance on integrated lumped-element technology for signal splitters and combiners, filter sections, and amplifiers.

A potential drawback of this particular implementation lies with its susceptibility to interference from out-of-band signals, as the input amplifiers are not preceded by a means of frequency preselection. Another potential concern is the fact that the two channels do not fully utilize their allocated shares of the input signal, as signal content that falls outside each channel's ascribed frequency response is discarded. The partial sacrifice of signal power is akin to adding attenuation at the input, which, in turn, affects minimum achievable noise-figure values. It should be noted, however, that the two-branch configuration still holds, in this regard, a significant 1.8-dB advantage over a comparable three-branch realization, as confirmed by computer simulations for cases where signal power is distributed equally among channels [105].

Noise is a common concern in microwave active filters. The concern relates especially to the passband edges, where attempts to sharpen them by selectively boosting signal transmission can lead to increased noise.

In channelized filters, there are seldom surprises, though, due to the absence of regenerative feedback. With each channel composed of a simple cascade of amplifiers and passive filter sections, noise performance can be easily assessed. Computer-generated estimates confirm that the input amplifiers and input power splitter are the main contributors to the overall noise figure, whereas channel filter losses and the output amplifiers account for only a few tenths of a decibel each. Due to the amount of incorporated channel amplification, noise generated by the output

power combiner itself becomes negligible.

Sensitivity to parameter changes is of special relevance when insuring against potential circuit instability. Channelized active filters are not prone to instability, due to their general reliance on feed forward-only signal flow. The amplifiers used to direct signal flow are never completely unilateral, though, allowing small amounts of unavoidable parasitic feedback to occur. Possible concerns can be easily countered by employing unconditionally stable gain stages and securing sufficient isolation between channels.

Chapter 3 Experimental details

In this chapter, the technical details of the measurement and simulation environment are introduced. Vector Network Analyser is used to carry out the on-wafer S-parameter measurement and ADS Momentum is employed for schematic and layout simulations. Calibration and de-embedding methods are also discussed.

3.1 S-parameter measurement

The S-parameters for a two-port network are defined using the reflected or emanating waves, b_1 and b_2, as the dependent variables; and the incident waves, a_1 and a_2, as the independent variables. The general equations for these waves as a function of the S-parameters are also shown in Figure 3.1.

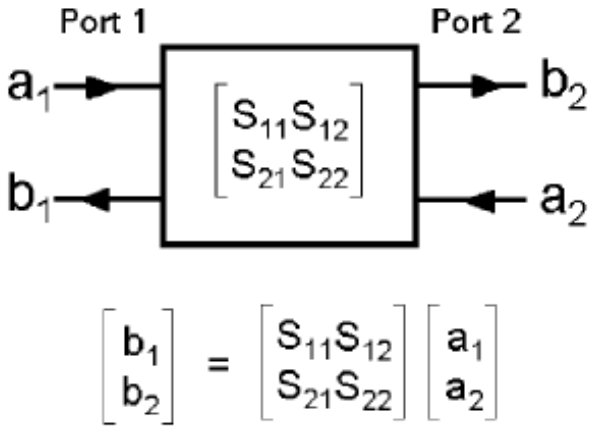


Figure 3.1: Definition of a two-port S-parameter network [127].

Using these equations, the individual S-parameters can be determined by taking the ratio of the reflected or transmitted wave to the incident wave with a perfect termination placed at the output (S_{11}, S_{12}, S_{21}, S_{22}). These four S-parameters completely define the two-port network characteristics.

RF and microwave networks are often characterized using S-parameters. The S-parameters of a network provide a clear physical interpretation of the transmission and reflection performance of the device. On-wafer measurement provides the designers a useful platform to perform fast, repeatable and accurate frequency domain measurements without packaging the devices.

The Vector Network Analyzer (VNA) has become the workhorse of most network measurements above 1 GHz. A VNA measures vector ratios of reflected or transmitted energy to energy incident upon the device-under-test (DUT) [107]. As a stimulus-response measurement, a VNA measurement determines the properties of device rather than the properties of signals. On-wafer S-parameter measurements were carried out on all types of CPW multilayer components, including transmission lines, capacitors from 45 MHz to 40 GHz using HP 8510B VNA (Figure 3.2).

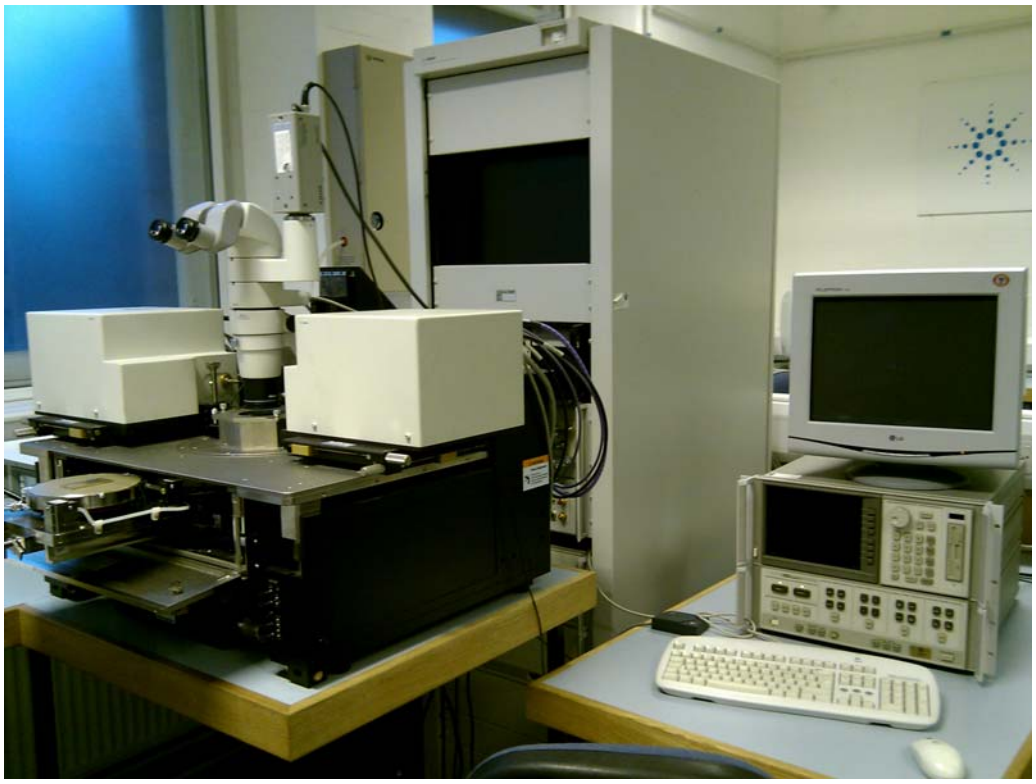
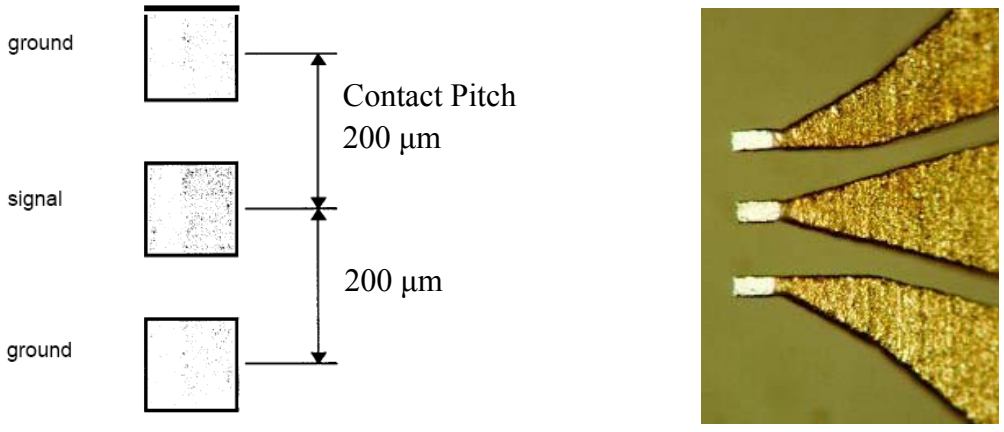


Figure 3.2: On-wafer S-parameter measurement facilities.

A Cascade Microtech on-wafer probe station is used in the equipment set. A key feature of this probe station is that the probe heads are held very rigidly in place so that cable forces from coaxial cables connected to the probe heads do not move the probe heads significantly with respect to the wafer [108].

The requirements for a microwave wafer probe are first that it has reasonably low reflections. If there is a return loss of better than 10 dB, typically a corrected VNA can then read through these reflections and get pretty clean data. Secondly, it should have reasonably low insertion loss so that the network analyzer doesn't have to correct through a large loss between it and the probe tips. Thirdly, the probe's S-parameters should be very repeatable. A typical vector difference on a Smith Chart should be less than 0.01 [108]. For the multilayer CPW transmission line designs in this project, we use the 50 Ω Ground-Signal-Ground (GSG) probe for contacting the pads on the transmission lines (Figure 3.3).

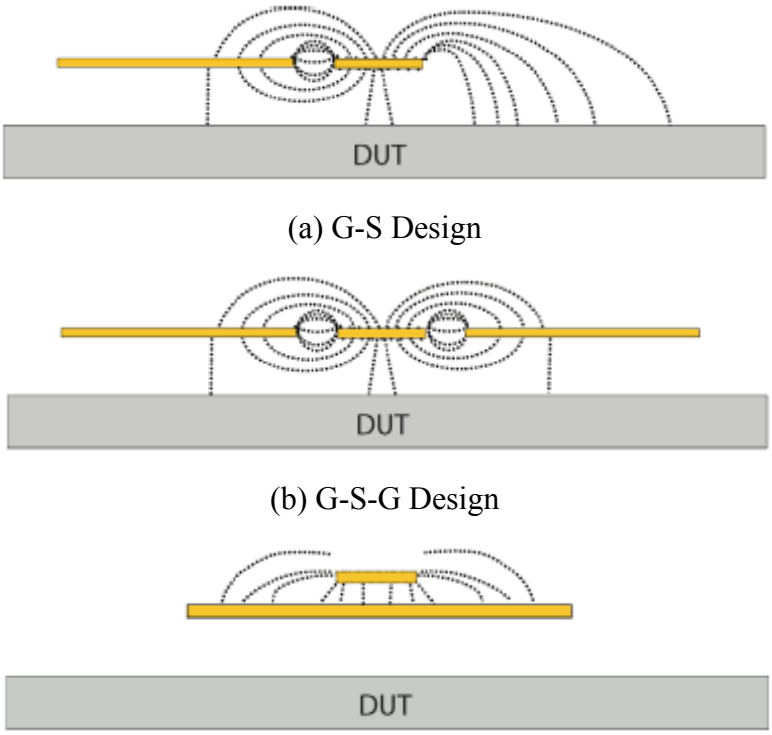


(a) Pads on the DUT. (b) The probe employed in the measurement.

Figure 3.3: The layout of the G-S-G pad with contact pitch of 200 µm.

The advantages of G-S-G design pads can be seen from the comparison with the G-S and microstrip pads (Figure 3.4). In Figure 3.3(a), G-S pad has fringes to the ground plane and it is not suitable for measurements above 10 GHz. For the microstrip design [Figure 3.3(c)], DUT is shielded, thus, resulting in reduced coupling to DUT and

reduced crosstalk.



(a) G-S Design

(b) G-S-G Design

(c) Microstrip Design

Figure 3.4: RF probe tip configurations [109].

GaAs has relatively poor thermal conductivity comparing with Silicon (see Table 1.1). If the substrate is ultra thick, the situation can go worse. Thus, it is necessary to carry out thermal characterization investigation on selected multilayer components.

Temptronic TP03200A Thermo Chuck is employed and fitted with the Cascade Microtech probe station in order to control the ambient temperature when performing on-wafer measurement, shown in Figure 3.5. The system adjusts the ambient temperature by holding the wafer on the thermal chuck and keeping it at a specified temperature throughout the whole measuring procedure. The accuracy of the temperature control is about ±2 ºC. To assure accurate temperature environment of the chunk, the wafers are hold for about one hour before measurement.

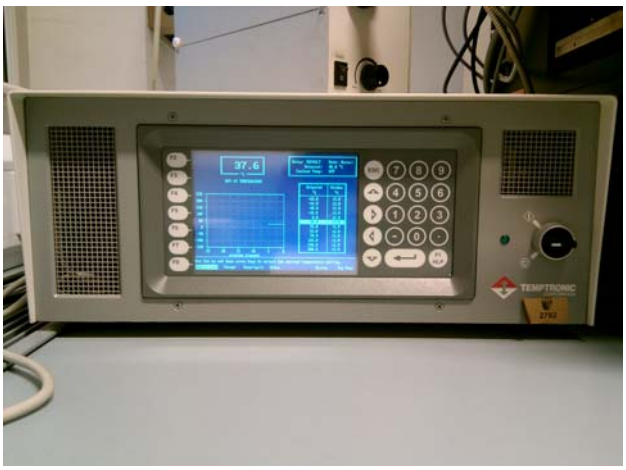


Figure 3.5: The temperature control facility.

3.2 On-wafer calibration

3.2.1 Systematic errors of S-parameter measurement

A significant challenge in stimulus-response measurements is defining exactly where the measurement system ends and the DUT begins. In on-wafer VNA measurements this boundary is known as the ‘reference plane’ of the measurement and will often be located at the probe tips.

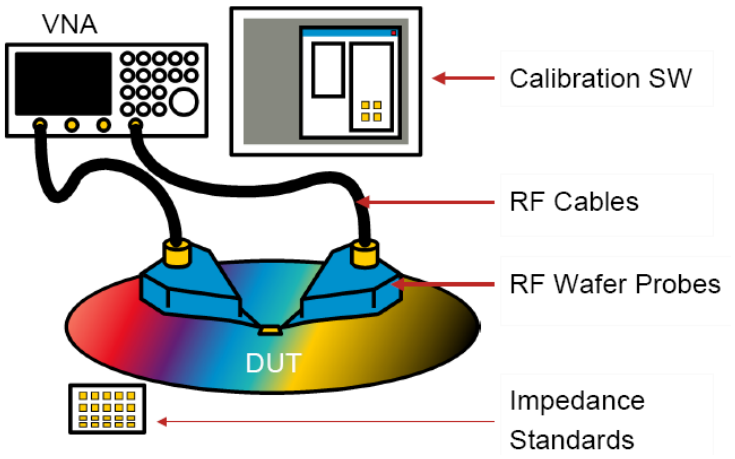


Figure 3.6: A typical RF measurement set-up at wafer level [109].

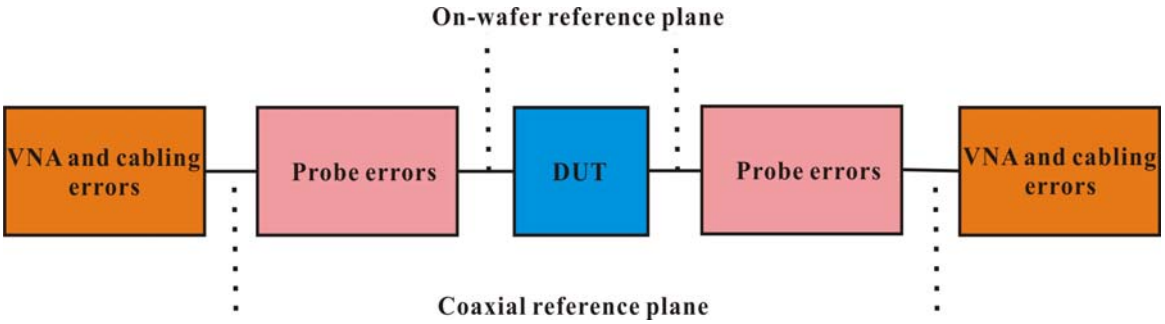


Figure 3.7: A schematic showing the different reference planes [110].

A typical measurement setting is shown in Figure 3.6 and the location of different reference planes are shown in Figure 3.7. The calibration we discuss here is to move measurement results to the on-wafer reference plane, thus, VNA cabling and probe tips errors will be removed.

The data read by HP 8510b VNA is usually raw and seldom be used directly. The reason can be outlined by the famous “12-term error corrections” (Figure 3.8) [111].

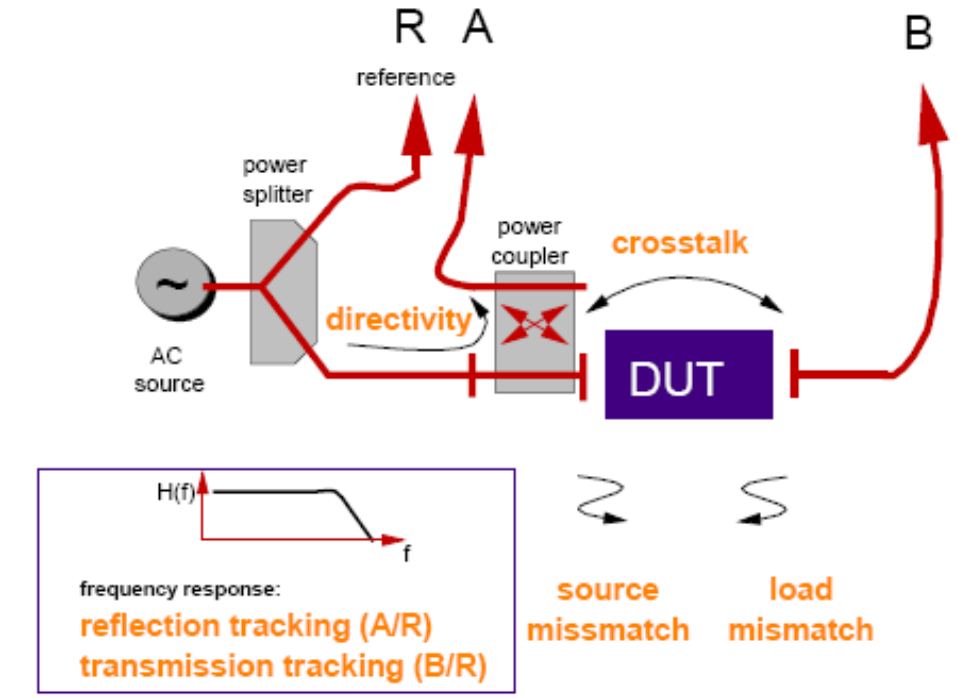


Figure 3.8: The 12 error contributions for S-parameter measurements with a VNA.

As can be seen in Figure 3.8, the following significant system errors, inherent in VNA, are found when the incident, reflected and transmitted signals are measured:

(1) Directivity: cross-talk of the power coupler; the lack of separation between the incident and reflected signals.

(2) Crosstalk: system leakages; cross-talk inside the S-parameter test set, overlying the DUT.

(3) Source mismatch: multiple reflections due to non-Z_0 input and output.

(4) Load mismatch: the same for the opposite port.

(5) Reflection tracking A/R: frequency dependence of signal path R to A; variations in the system response to the reflected signal.

(6) Transmission tracking A/R: same for signal path R to B; variations in system response to the forward propagating reverse signal.

The six significant errors are identified in both the forward and reverse directions giving the full twelve terms. The VNA is able to identify system errors by measuring

known devices and comparing the measured results to the expected results. The calibration procedure then removes the extraneous error signals and provides the corrected measurements.

3.2.2 Generalized calibration method

The VNA usefulness is enhanced by calibrating the system at the DUTs interface. As it is developed in the 1960's and 1970's, the calibration was based on reflective 1-port standards [112], [113]. The process involved first calibrating the individual test ports and then using these calibrated test ports to calibrate the system for 2-port DUTs. However, this method requires at least three, exactly known electrical standards.

In the late 1970's, new methods of calibration were developed based on transmission lines as the primary standard. First, the Thru-Short-Delay [114] (TSD) and then Thru-Reflect-Line [115] (TRL) techniques were developed. They require fewer standards and are less restrictive about actual standard characteristics than previous techniques. However, TSD and TRL are not easily applied to all measurement situations. Further development [116], [117] of the TRL calibration concepts has lead to a more generalized technique that overcomes the major limitations of TRL. The first step is to separate the system into a perfect reflectometer followed by a 4-port error adaptor (Figure 3.9) [118].

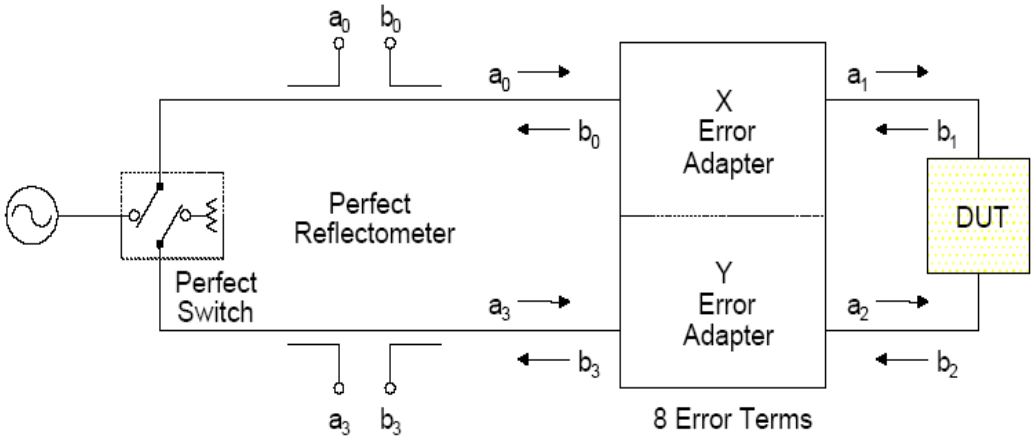


Figure 3.9: The circuit of VNA S-parameter measurement system.

The error adapter in Figure 3.9 represents all the errors in the system that can be corrected by the calibration procedures. The whole adapter is split into two 2-port error adapters, X (at port 1) and Y (at port 2). X and Y are 2-ports it would appear eight unknowns to find, however since all measurements of the made as ratios of b_i's and a_i's, there are actually only 7 error terms to find. T Parameters are then used instead of S-parameters since it allows one to represent the overall measurement. It is also shown in [119] that how the complete error model can be derived by the use of three 2-port standards where 7 of the 12 possible parameters were given. There are a number of different combination of standards that fit those requirements. In choosing appropriate standards, one standard needs to be Z_0 based, one needs to present a high mismatch reflection, another needs to provide information on the measurement reference plane and all three standards be to sufficiently different as to be three independent measurements [120].

There are a wide range of generalized solutions of choosing the standards. The use of a zero length 'thru' is an oblivious selection but a non-zero length 'thru' is also acceptable if its length is known [121] or the desired reference plane is in the centre of the non-zero length thru.

A second standard needs to be a Z_0 reference. A line of nominally ¼ wavelength can be as choice. In this generalized solution, only the impedance needs to be of concern. The S_{21} and S_{12} of this standard can be any value and does not need to be known in fact they will be found during the calibration process. This opens up the choices to a wide range of 2-port components, such as pair of matched loads or an attenuator. These are devices that can present a resistive Z_0 and work with fixed wafer probes.

For the final standard only one piece of information is needed. This could be a known reflection value or symmetrical reflections. Since the other standards have been well matched, this standard must be a high mismatch. S-parameters of this device don't

need to be known. A pair of ‘open’s or ‘short’s or any symmetrical network is a candidate.

Here is a partial list of possible calibration configurations with an appropriate three letter acronym [120].

Standard 1: Thru		Standard 2: Z_0			Standard 3: Reflect	Name
Zero Length	Non Zero Length	Line	Match	Atten.	$\Gamma_1 = \Gamma_2$	
√		√			√	TRL
	√	√			√	LRL
√			√		√	TRM
	√		√		√	LRM
√				√	√	TRA
	√			√	√	LRA
√		√			Γ=-1	TSD

Table 3.1: List of some familiar combinations of calibration standard.

The TRM/LRM family of calibration techniques addresses many of the calibration issues found in fixture and wafer probing station that occurred with previous techniques: high quality calibration over a broad frequency operation with a minimum of standards, choice of resistive or transmission line based Z_0 and applicable to fixed spacing fixtures [120].

LRRM (line-reflect-reflect-match) is developed in [121], which is a variation of LRM with several possible advantages. This method uses a line, two unknown reflects (undefined ‘short’s and undefined ‘open’s), and a ‘match’ (Figure 3.10). The LRM method can be viewed as being the special case of the LRRM method for which the

match is chosen as one of the reflect standards.

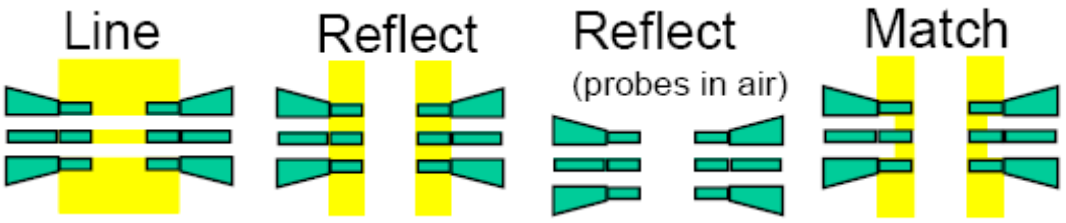


Figure 3.10: The standards used in Line-Reflect-Reflect-Match (LRRM) calibration.

LRRM had been verified by the National Institute of Standards and Technology (NIST) to be the best for probe calibration. Other two popular methods (SOLT / LRM) had growing errors with the frequency and possible reference plane error [122].

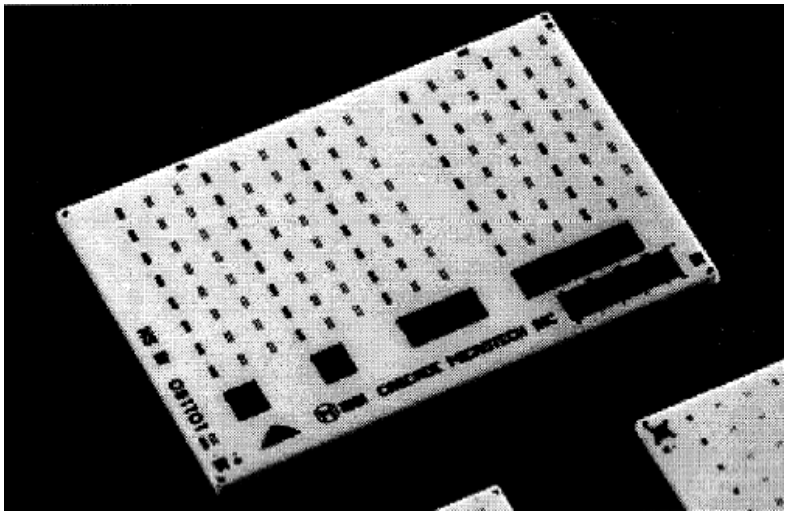


Figure 3.11: The Impedance Standard Substrate.

Cascade's alumina-based impedance standard substrate (ISS) (Figure 3.11) is used for the semi-automatic on-wafer calibration in this study. And the calibration accuracy and repeatability have been shown to be quite good for use in measuring CPW structures on GaAs substrates [123] [124].

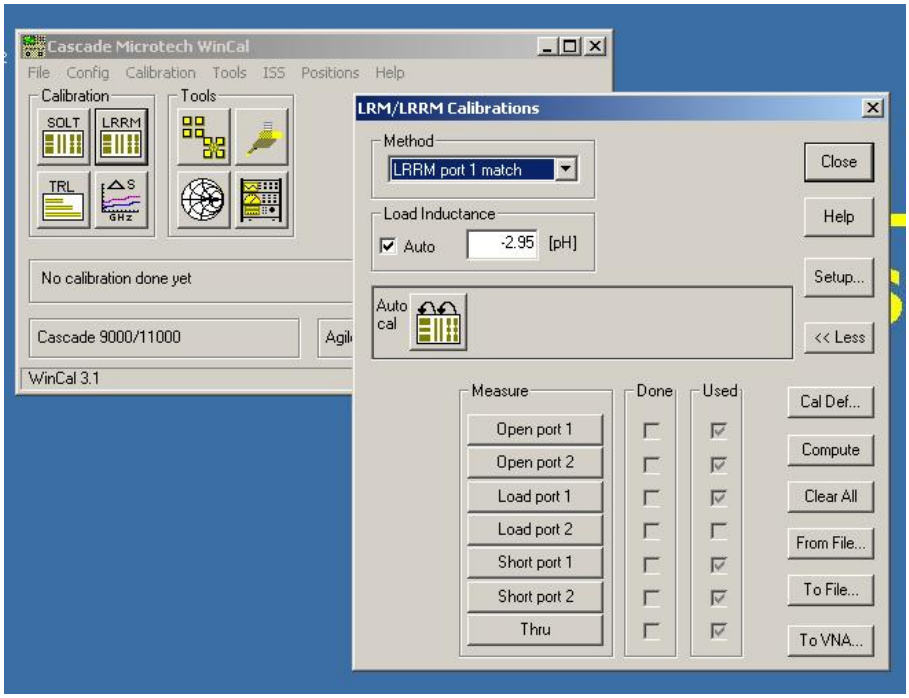


Figure 3.12: Snapshot of the user's surface of Microtech's WinCal.

The LRRM calibration algorithm is available in Cascade Microtech's WinCal VNA calibration software running on a PC. The WinCal software allows highly repeatable, fully automated VNA calibrations initiated with a single mouse click (Figure 3.12).

3.3 CAD software

3.3.1 Schematic simulation tools

Agilent Advanced Design System (ADS) is used to carry out the circuit level simulations in this work. ADS can easily and effectively communicate with other Agilent EM simulators such as Momentum and IC-CAP. The package helps to accelerate the process of designing, measuring, optimizing and validating the RF circuits.

ADS provides a vast array of simulation modes and models for microwave applications and high speed digital circuits. It also has powerful optimization and tuning functions that can lower the circuit design complexity. ADS contains a large number of simulators that enable you to simulate circuits and RF systems designed for specific objectives. Table 3.2 shows brief descriptions of the simulation types that employed in this work.

Simulator	Description
DC	Fundamental to all simulations, it performs a topology check and an analysis of the DC operating point of a circuit.
AC	Obtains small-signal transfer parameters, such as voltage gain, current gain, and linear noise voltage and currents. This simulator is useful in designing passive circuits and small-signal active circuits such as low-noise amplifiers (LNAs).
S-parameter	Provides linear S-parameters, linear noise parameters, transimpedance (Y_{ij}), by linearizing the circuit about the DC operating point and performing a linear small-signal analysis that treats the circuit as a multiport. Each port is turned on sequentially. S-parameters can be converted to Y and Z parameters.

Table 3.2: Descriptions of ADS simulation types [128].

The DC simulation calculates the DC operating characteristics of a design. The simulator computes the response of a circuit to a particular stimulus by formulating a system of circuit equations and then solving them numerically. The AC simulation performs a small-signal, linear AC analysis and enables you to obtain small-signal transfer parameters, such as voltage gain, current gain, transimpedance, transadmittance, and linear noise. The S-parameter simulation helps the users to obtain the scattering parameters of a component, circuit, or subnetwork and convert those parameters to Y or Z-parameters.

A basic circuit simulation procedure in ADS can be described as:

- Creat the schematic, then add current probes and wire/pin labels to identify the nodes from which to collect data.
- Select a simulation method, specifying parameters as necessary.
- Run the simulation.
- View DC data by annotating the schematic with DC solutions and by viewing brief or detailed device operating point data.
- Display additional results using the Data Display.
- Optimize and tune a design.

Figure 3.13 depicts the user interface of ADS schematic simulator.

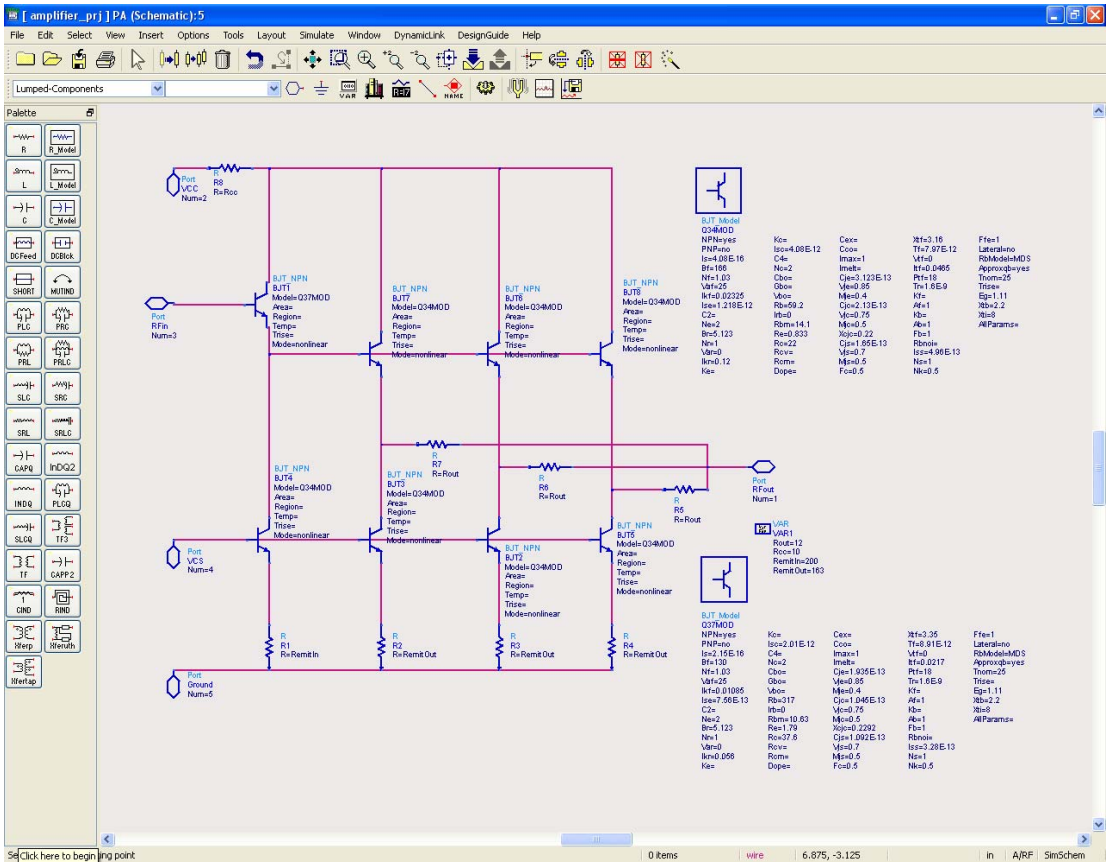


Figure 3.13: ADS schematic simulator user interface.

3.3.2 EM simulation tools

MMICs have the benefits of high performances and low cost in large quantities. However, the small physical structure, multi conductor and dielectric layers, and isolation passivating layer of MMIC circuits cause the post-fabrication tuning to be extremely difficult. Therefore, accurate EM simulation is highly demanded to predict the electrical behavior of monolithic components and circuits. In this work, ADS Momentum is applied to carry out the EM simulations.

Momentum is part of the ADS, as shown in Figure 3.14. It is an electromagnetic simulator that computes S-parameters for general planar circuits, including microstrip, slotline, stripline, coplanar waveguide and other topologies. It uses the Method of Moments (MoM) based on 2D component layouts and provides users a 3-dimensional perspective of current flow in conductors or slots and far-field radiation patterns. Therefore it is called 2.5D simulator. Momentum is completely integrated into ADS, and this allows users to have a common interface for both EM and circuit analysis.

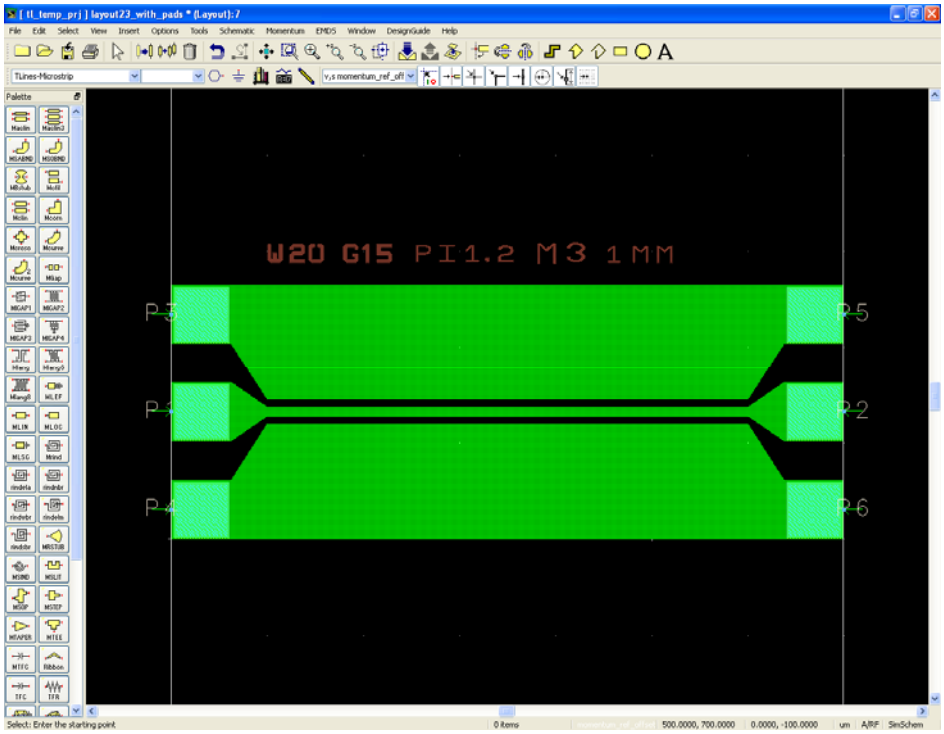


Figure 3.14: ADS Momentum user interface.

The advantage of using Method of Moments is that it consumes much less time to simulate microwave components compare to full 3-D simulators. The planar metallization patterns defined in ADS layout are meshed with rectangular and triangular cells in the microwave simulation mode as shown in Figure 3.3. Each cell corresponds to an equivalent circuit built by capacitors and inductors while all capacitors and inductors in the network are complex frequency dependent, and mutually coupled. The MoM interaction matrix equation follows from applying the Kirchoff voltage laws in the equivalent network. Once the currents are know, the field problem is solved because all physical quantities can be expressed in terms of the currents.

3.3.3 Device modelling tool

Active device modelling is always a difficult task and it takes a lot of time to optimize and validate the data. Integrated Circuit Characterization and Analysis Program (IC-CAP) is a device modelling program that provides powerful characterization and analysis capabilities. It offers a full set of tools including instrument control, data acquisition, graphical analysis, simulation, optimization, and statistical analysis. The general procedure for characterizing a device in IC-CAP is shown in Figure 3.15.

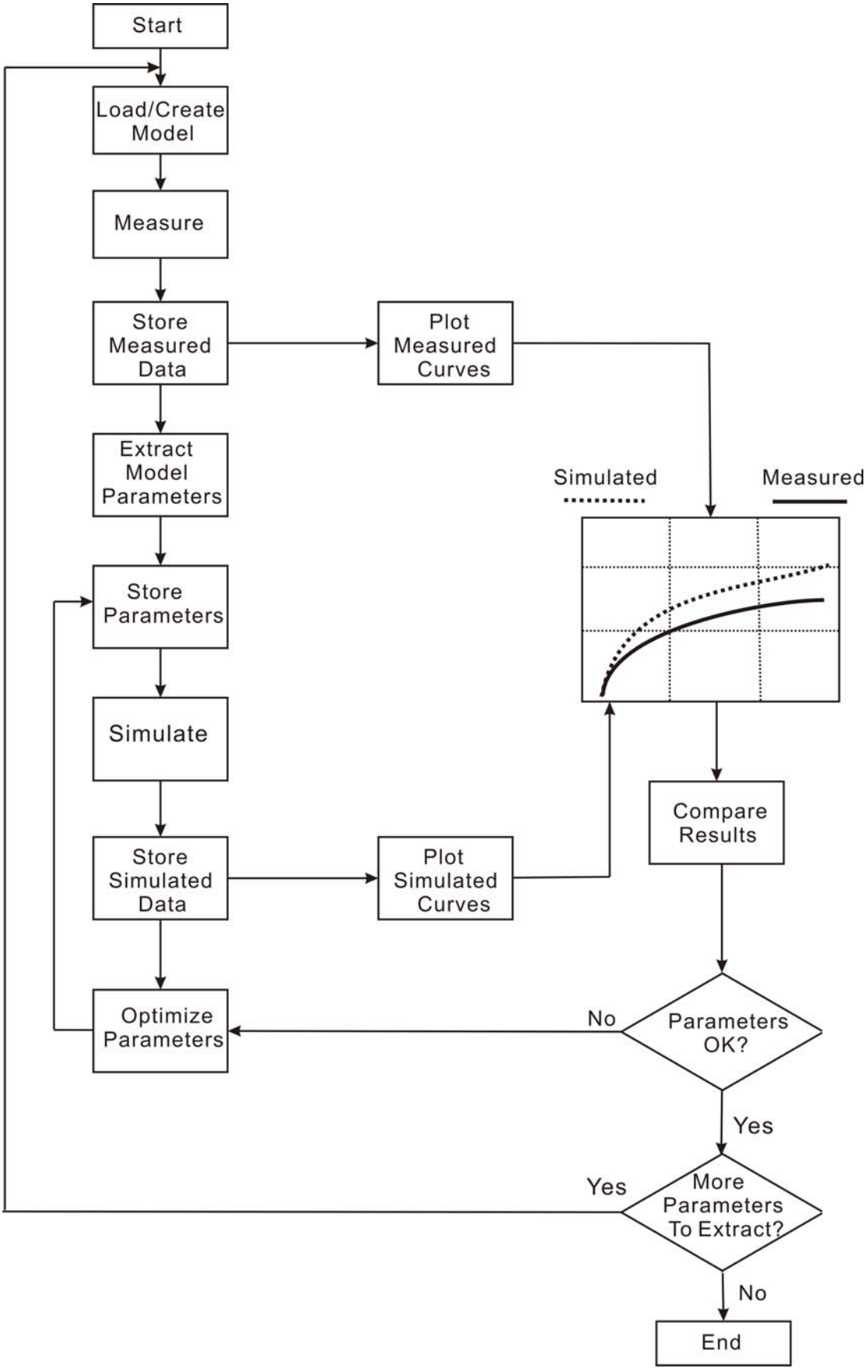


Figure 3.15: The general procedure for characterizing a device in IC-CAP [128].

Compare with the manual modelling procedure using software like MATLAB, IC-CAP has the advantage of all-in-one working environment. The whole modelling stages including measurement, model extraction, simulation, optimization and validation can all be done within the single software. This feature accelerates the whole procedure of active device modelling and helps the designers save a great deal of time.

3.3.4 The six-port simulation

Normally to simulate a CPW transmission line following setup is used, where the centre conducting strip is connected to the signal port and the conductors on the either side are grounded. The simulation set up shown in Figure 3.16 is used during the RF measurements.

Figure 3.16: Conventional setup used in the measurement and simulation of a CPW line, with a length of 1.4mm.

Since Momentum does not account for the higher order modes in the calibration process, care should be taken when selecting the type of port or port definition used. There are different types of port definitions that could be used in the EM simulations in Momentum. Some of them are single, internal, differential, etc. Single is the default port type, which is external to the structure and calibrated. The port is excited using a calibration method, which removes any undesired reactive effects of the port

excitations at the port boundary. This type of calibration process is same as any other standard calibration like LRM or LRRM used in the normal RF on-wafer measurements. Hence in Momentum using a 'single' type port eliminates the effect of parasitic on the transmission line's simulated S-parameters. Therefore the result of calibration process includes the elimination of the lower-order mode mismatch, higher order modes and removal of all port excitation parasitics. Also the simulation tool will not understand when a conductor has been connected with two ground ports on either end of the same conductor. Also when two ports of different potential are placed next to each other, energy couples between them hence leading higher order mode signals. Therefore, to eliminate the higher order modes all the ports are defined as 'single' type of ports. The set-up is shown in Figure 3.17.

Figure 3.17: Simulation setup using single port definition used in eliminating higher order modes in EM simulations.

Now with this setup the simulation becomes a six port simulation and the S-parameters obtained will be in 's6p' format. These S-parameters are exported using the 'visualization' tool in ADS Momentum. Later these S-parameters are simulated in the schematic environment of the ADS. In the schematic environment only the centre conducting strip port terminals are terminated with the excitation or single ports and all the unwanted terminals (ground planes) are terminated with the ground port terminations.

3.4 Eye diagram measurement set-up

For the eye diagram measurement, the setup used has been shown in Figure 3.18. The frequency of operation is varied between 500 MHz and 10 GHz. The device is given a small signal AC signal through the LA 19-01-03 pulse pattern generator through an attenuator which is used to set a desired input voltage from the PRBS.

The pattern generator used has the capability to generate signals up to 3 Gbps with a fixed magnitude of 2 V_{pp}. To maintain the device to operate in small signal condition a small input voltage of 25mVpp was applied and this was regulated by the use of an attenuator.

The PRBS generator used in this experiment can set to operate in two modes of number of bits, 27 and 214. However it was observed that between the two the output performance was not affected since number of bits in both cases is high. However to rule out even slight inconsistency of any manner, the number of bits was set to generate 27 bits throughout the experiment.

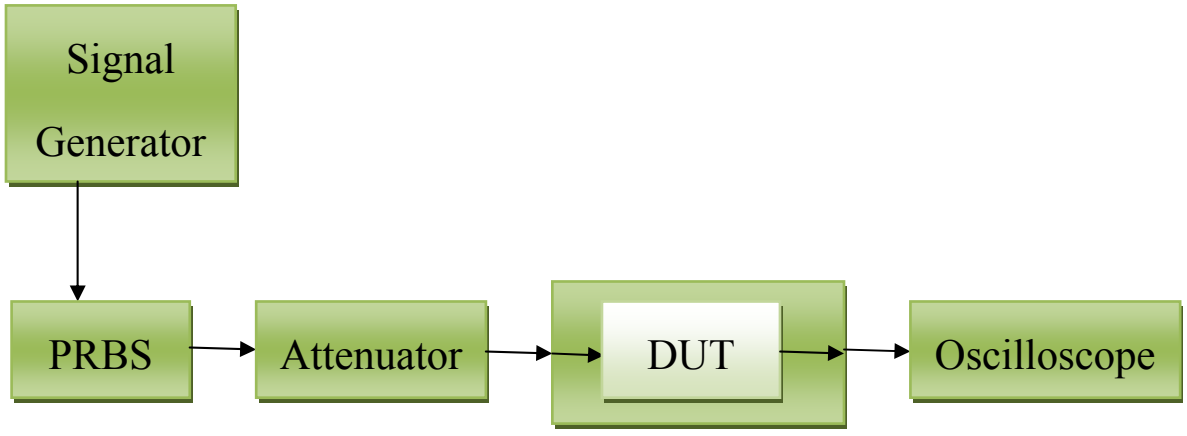


Figure 3.18: Eye diagram measurement setup.

The output signal through the device is observed on the DCA 86100A Infiniium oscilloscope which provides full real-time bandwidth of up to 50 GHz. The different eye parameters were measured and all the eye parameters were recorded over the entire range.

During measurements it was observed that the device may continue to appear functional under all frequency conditions but some critical parameters do deteriorate as is clearly visible from the eye diagram plots of different frequencies.

The definition of some main eye parameters is described in Figure 3.19:

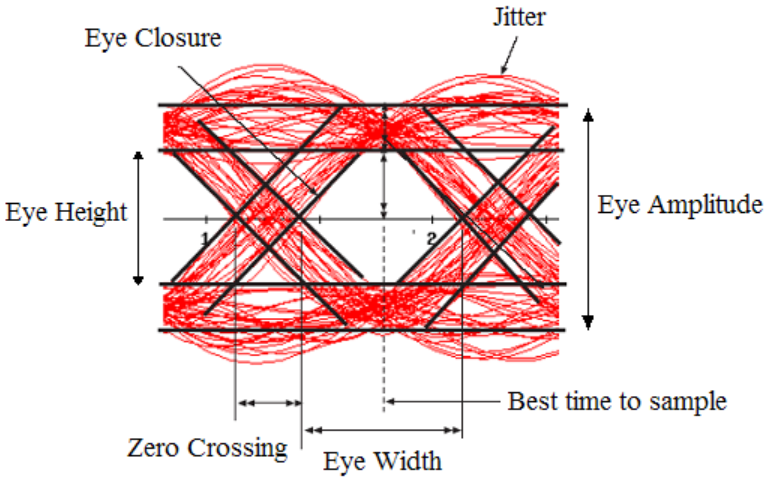


Figure 3.19: Interpretation of the Eye Diagram [125].

3.5 Pads parasitic de-embedding

3.5.1 Description of the method employed

Precise and reliable models are of significant importance for RF/microwave circuit design. The library of CPW multilayer components need to be characterized. With the

increasing of operation frequency, the influence of probing pads and interconnect parasitic on device performance has become more and more important.

In this study, a number of CPW multilayer structures had been measured at the frequency range of 0.045 – 20GHz. The parasitic effect of pads had been gradually visible after several gigahertz.

Generally speaking, de-embedding is the process of mathematically subtracting networks from the measured results. De-embedding of pads can be done by manual evaluation and optimization. The problems of this method will include inaccuracy and unreasonable results. The following de-embedding scheme is based on matrix transformation so as to meet the requirement of large number of circuits. Meanwhile it is suitable for any microwave circuits which have pads and interconnects on each side.

The preparation includes the S-parameters of 'DUT', 'open', 'short' and 'thru' dummies (Figure 3.20). L in the first figure indicates the total length of the intrinsic device and the two interconnects. L_1 and L_2 are the symmetrical short interconnects between pads and intrinsic devices [126].

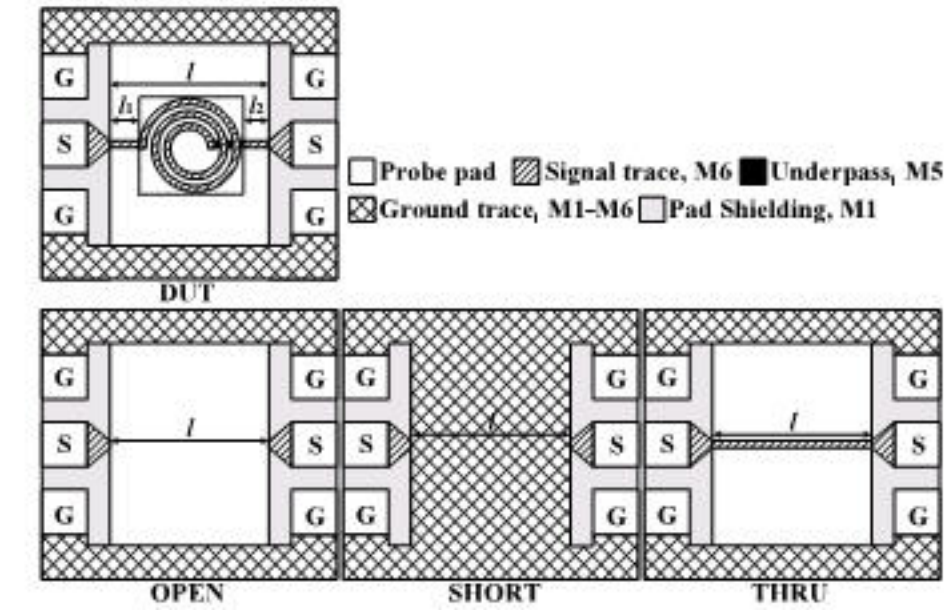


Figure 3.20: The preparation of de-embedding [126].

The theory behind is to model the pads as a combination of impedance and admittance, interconnects as short transmission lines (Figure 3.21). And then subtract them mathematically from the microwave device. Flow chart of this scheme is shown in Figure 3.22.

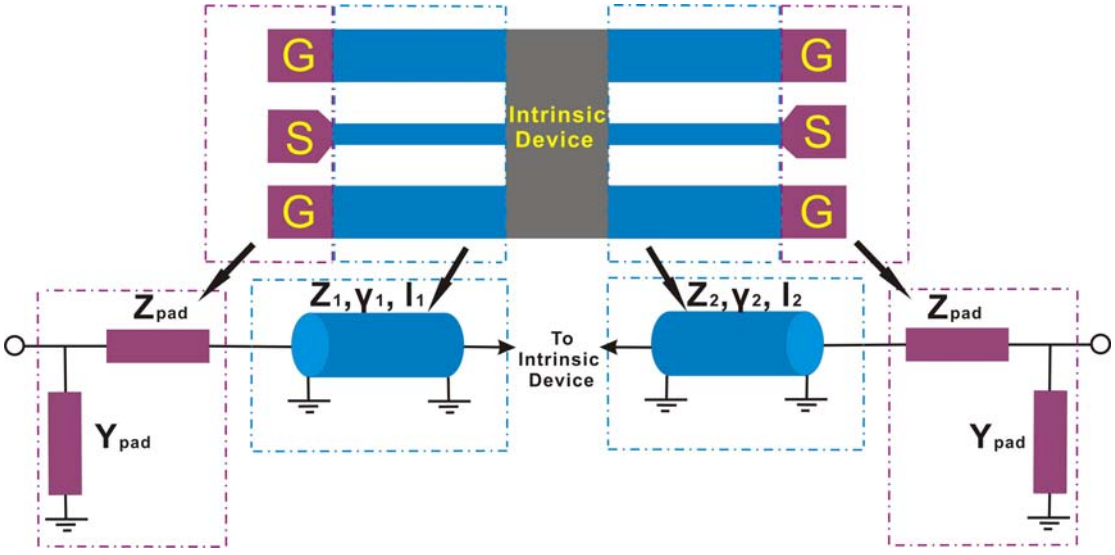
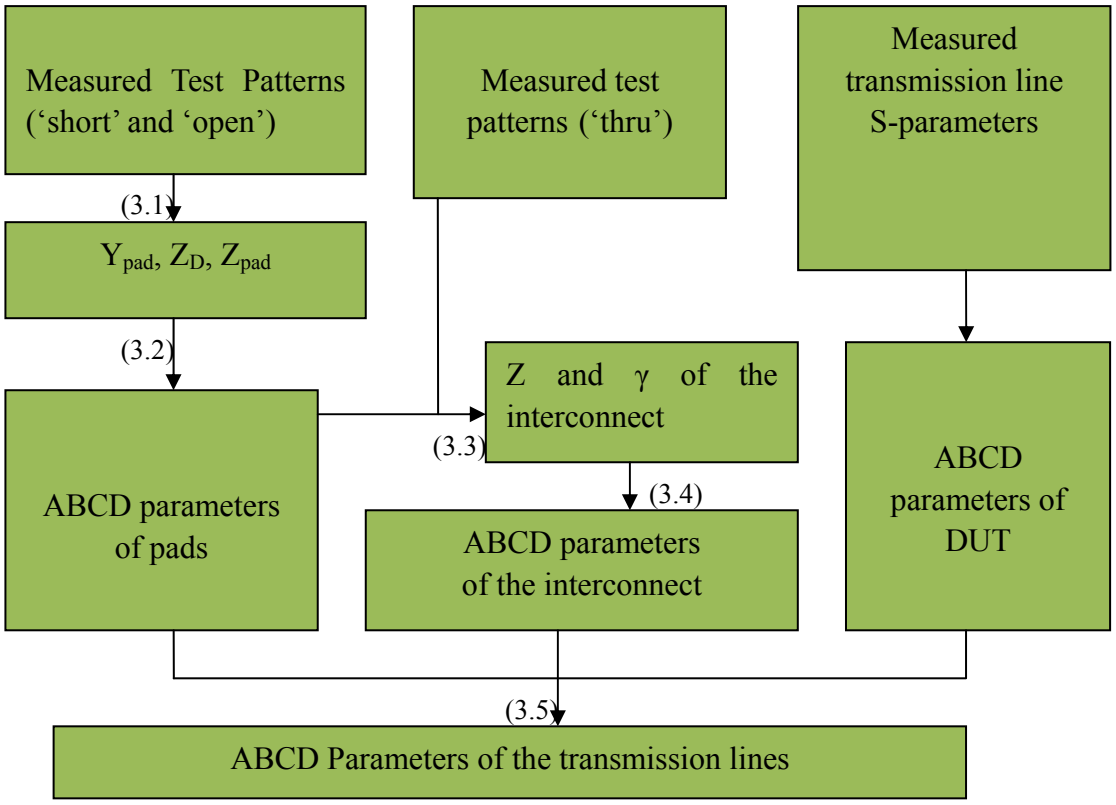


Figure 3.21: Comprehensive parasitic model of the device [127].



(3.1)

$$Y_{PAD} = Y_{11}^{OPEN} + Y_{12}^{OPEN}$$

$$Z_D = Y^{SHORT} - Y^{OPEN}$$

$$Z_{PAD} = Z_{11}^{D} - Z_{12}^{D}$$

(3.2)

$$\left[A^{PAD1}\right] = \begin{bmatrix} 1 & Z_{PAD} \\ Y_{PAD} & 1 + Z_{PAD}Y_{PAD} \end{bmatrix}$$

$$\left[A^{PAD2}\right] = \begin{bmatrix} 1 + Z_{PAD}Y_{PAD} & Z_{PAD} \\ Y_{PAD} & 1 \end{bmatrix}$$

(3.3)

$$\left[A^{INT}\right] = \left[A^{PAD1}\right]^{-1} * \left[A^{THRU}\right] * \left[A^{PAD2}\right]^{-1}$$

(3.4)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma l & Z_c \sinh \gamma l \\ \frac{1}{Z_c} \sinh \gamma l & \cosh \gamma l \end{bmatrix}$$

(3.5)

$$\left[A^{D}\right] = \left[A^{IN}\right]^{-1} \left[A^{DUT}\right] \left[A^{OUT}\right]^{-1}$$

Figure 3.22: Flow chart and the equation explanation of the de-embedding scheme.

Traditionally, we use ‘open’ pattern to subtract the capacitive and conductive parasitics of pads. The advantage of this method is resistive and inductive effects are also taken into account. Thus higher accuracy will be achieved.

In this study, most of our components don’t have short interconnects at the input and output sides. Only ‘short’ and ‘open’ dummies (Figure 3.23) are used to generate the ABCD parameter of pads. “W20 G15” in the Figure indicates that the width of the center conductor is 20 μm and the gap width between center and ground conductor is 15 μm, which are the same as the transmission line geometry.

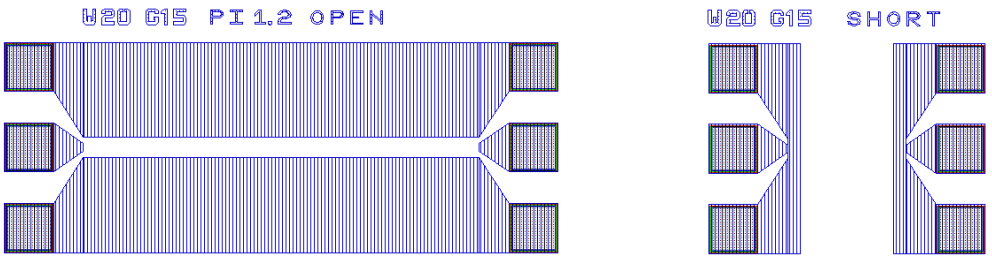


Figure 3.23: Layouts of the ‘open’ and ‘short’ test patterns used in this study.

3.5.2 Effects of de-embedding

Here is a plot of S_{21} before and after de-embedding for a conventional CPW transmission line (Figure 3.24).

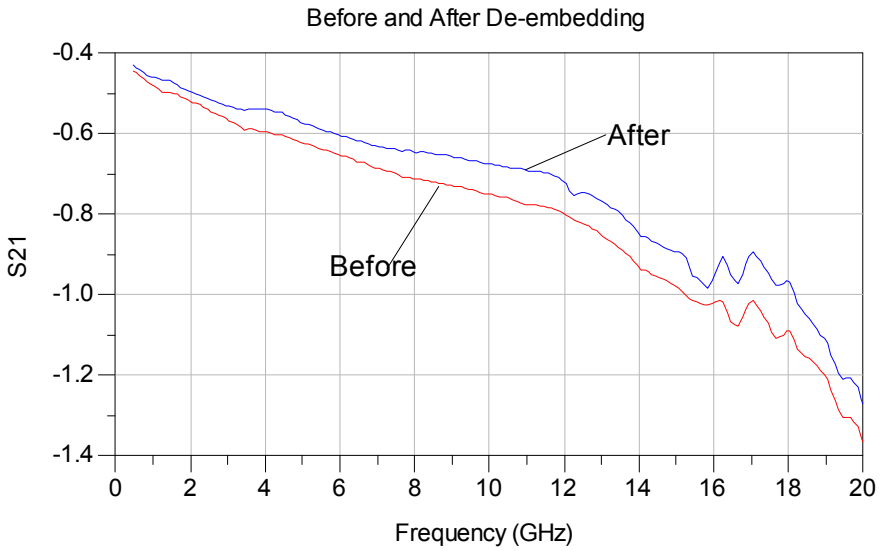


Figure 3.24: S_{21} of conventional CPW transmission lines before and after de-embedding.

It is indicated in Figure 3.24 that how the two pads had influence on the RF performance of transmission lines. As frequency increases from 2 GHz to 10 GHz the two curves experience a gradually depart from each other. This is due to the resistance of pads increases with frequency, resulting in higher insertion loss. After 10 GHz the difference becomes unchanged because of the current crowding effect for transmission line itself thus the effect of pads gets smaller.

Figure 3.25 is a plot of calculated dissipation loss of the conventional CPW transmission line applying Equation (3.6). A reduction of 10% loss is shown after removing the parasitic of pads.

$$DL = 10\log\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right) \tag{3.6}$$

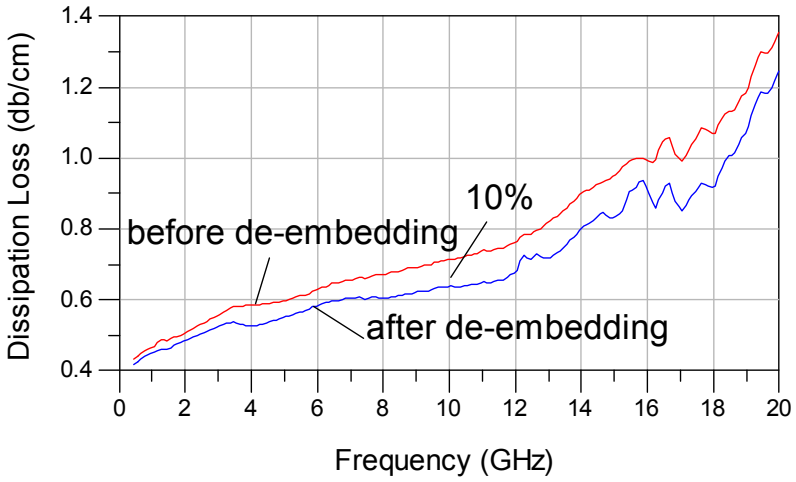


Figure 3.25: Dissipation loss of conventional CPW transmission line before and after de-embedding.

Chapter 4: Results and discussions

4.1 CPW multilayer transmission lines

In this section, several characteristics of CPW multilayer transmission lines on S.I. GaAs substrate are studied. First, a set of multilayer transmission lines realizing a wide range of characteristic impedance is designed and measured. These data are valuable for the design and optimization of future 3D MMICs. Next, thermal characterization of these transmission lines is performed for the 3D MMICs optimum design, followed by an illustration of 3D structure optimisation techniques.

4.1.1 Transmission line parameters extraction

Characterization of RF components using S-parameters is proven to be very effective comparing with other techniques. As described in Session 3.1, S-parameters are measured by HP 8510b VNA and then pads are de-embedded from the two-port S-parameters so that intrinsic parameters of transmission lines can be evaluated.

In this work, characteristic impedance, effective dielectric constant, dissipation loss and other parameters are extracted from the measured and simulated S-parameters of the transmission lines. Equations to calculate various parameters of transmission lines can be found in [129]. The magnitude of characteristic impedance (Z_0) is studied in this work. Z_0, together with the complex propagation constant, γ are giving by equations (4.1) and (4.2):

$$Z_0 = Z_{sys}\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{4.1}$$

$$e^{-\gamma l} = \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} + \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \tag{4.2}$$

where Z_{sys} is the measuring system impedance, l is the physical length of the transmission line and γ is the complex propagation constant and this is given in (4.3).

$$\gamma = \alpha + j\beta \tag{4.3}$$

Where α and β are the real and imaginary part of the complex propagation constant.

The real part of the complex propagation constant, α indicates the loss and the imaginary part gives the phase velocity, β. Using β one can deduce the effective dielectric constant, $\varepsilon_{r,eff}$ of the line using (4.4). Thus, one can easily derive the equation for the effective dielectric constant, $\varepsilon_{r,eff}$:

$$\varepsilon_{r,eff} = \left(\frac{c}{v_p}\right)^2 = \left(\frac{\beta c}{\omega}\right)^2 \tag{4.4}$$

Where c is the speed of light, ω is the angular frequency and v_p is the phase velocity.

Dissipation loss (DL) of the transmission lines can be expressed by S-parameters directly:

$$DL = 10\log\left(\frac{1 - |S_{11}|^2}{|S_{21}|^2}\right) \tag{4.5}$$

4.1.2 Transmission lines with wide range of characteristic impedance

In order to apply transmission lines in various circuits such as amplifiers and other matching networks, the availability of low loss transmission lines with wide range of characteristic impedance is vital. To demonstrate the merits of multilayer techniques, we provide some realizations of transmission line (as indicated in Figure 4.1) with various impedances. These designs are then simulated, fabricated and characterized.

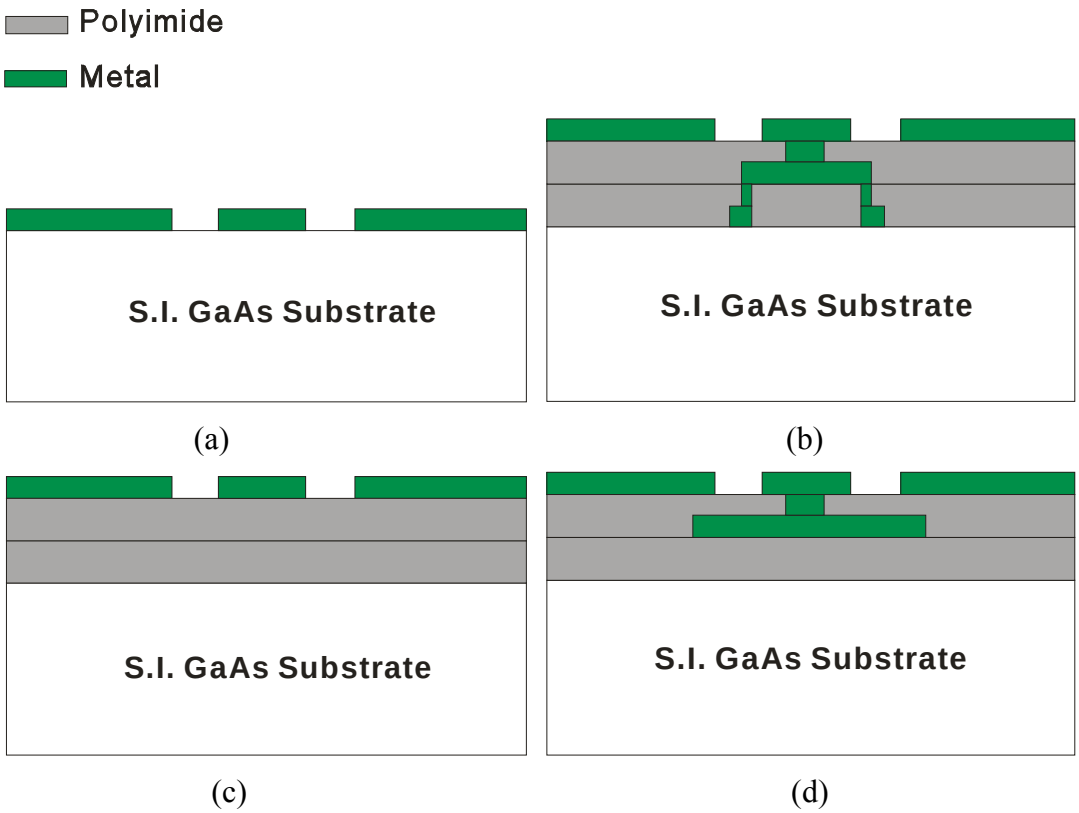


Figure 4.1: Cross-sectional view of various multilayer CPW transmission line designs: conventional 50 Ω (a); V-shape 50 Ω (b); planar on 2PI layers (c); overlapped (d).

The fabricated designs illustrated in Figure 4.1 employed a 600 μm semi-insulating GaAs substrate. In Figure 4.1, the grey colour indicates the 2.5 μm polyimide layers and the green ones are 0.8 μm titanium/gold metal layers. Gold is fabricated on the thin 100 Å titanium layer for adhesion onto the dielectrics (GaAs or Polyimide). For all designs, the gap between top centre metal and ground metal is 20 μm, the width of centre metal is 15 μm, the intrinsic length (without considering the length of the bonding pads at the two ends) of the transmission line is 2mm.

4.1.2.1 50 Ω characteristic impedance transmission line designs

50 Ω transmission lines are widely used in MMICs for interconnection in the circuits.

It can be realized by adjusting the gap (G) and centre metal width (W) of a conventional CPW transmission line (Figure 4.2). In multilayer structure, it can be realized by employing three metal layers and meanwhile optimising the ratio of effective W and G, known as V-shape structure. The concept of effective width is illustrated in Figure 4.3. In our conventional CPW design, W = 20 μm and G = 15 μm. The fabricated V-shape design has an effective centre metal width of 26 μm and the gap between centre metal and ground is 10 μm. This ratio is tuned to give a characteristic impedance of around 50 Ω.

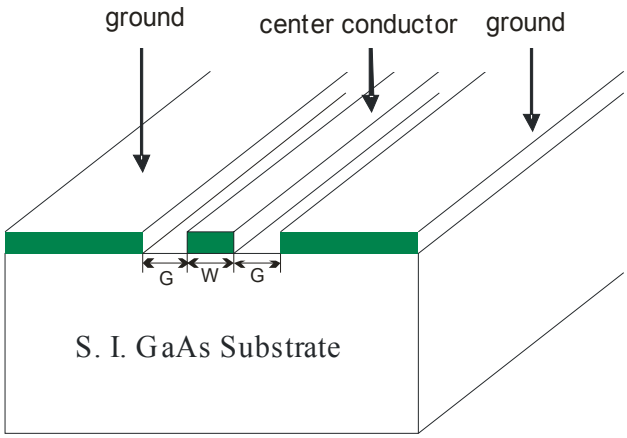


Figure 4.2: Cross-sectional view of the conventional CPW transmission line.

It has been shown [143, 144] that the ε_{eff} of a CPW increases with frequency. This type of performance is usually attributed to the increased concentration of the field (field confinement) in the dielectric at higher frequencies. On the other hand, it has been observed [145, 146] that at low frequencies for a CPW with narrow signal strip (centre metal width < 25 μm) ε_{eff} decreases with increasing frequency. This type of performance is attributed to the frequency dependence (dispersion) of the line inductance due to the skin effect [147], which has been confirmed by theoretical analysis [146, 148].

This issue can also be explained as follows: using quasi-static analysis, effective dielectric constant can be expressed as [129]: $\varepsilon_{eff} = C / C^{a}$, whereas C is the total

capacitance of the transmission line and C_a is the capacitance of the transmission line when 'air' is assumed as the dielectric material. It is indicated in [127] that substrate capacitance decrease with frequency. This will lead to decrease of total capacitance of the transmission line from low frequency to high frequency. Meanwhile, the term C_a remains relatively constant throughout the frequency. According to $\varepsilon_{eff} = C / C^a$, we can conclude that ε_{eff} decreases with frequency. Similar data are also found in [140,141,142].

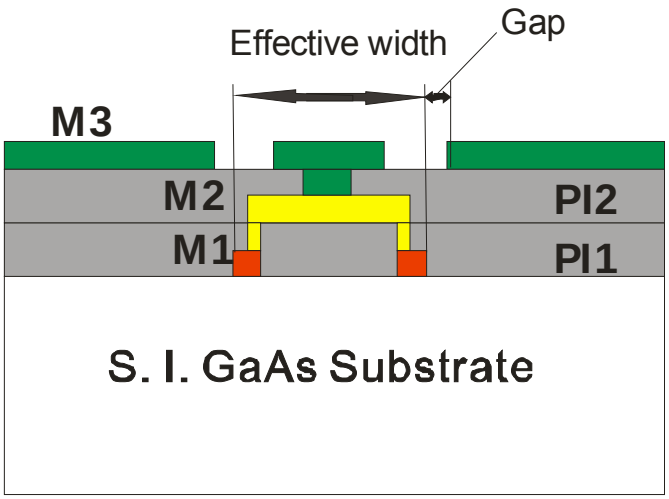
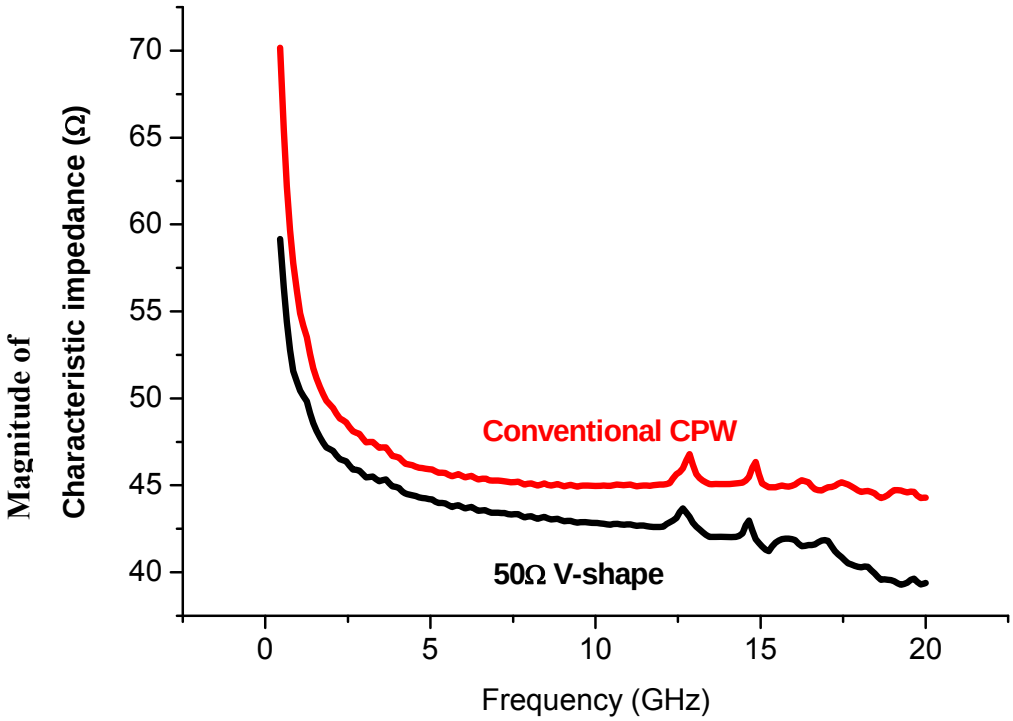


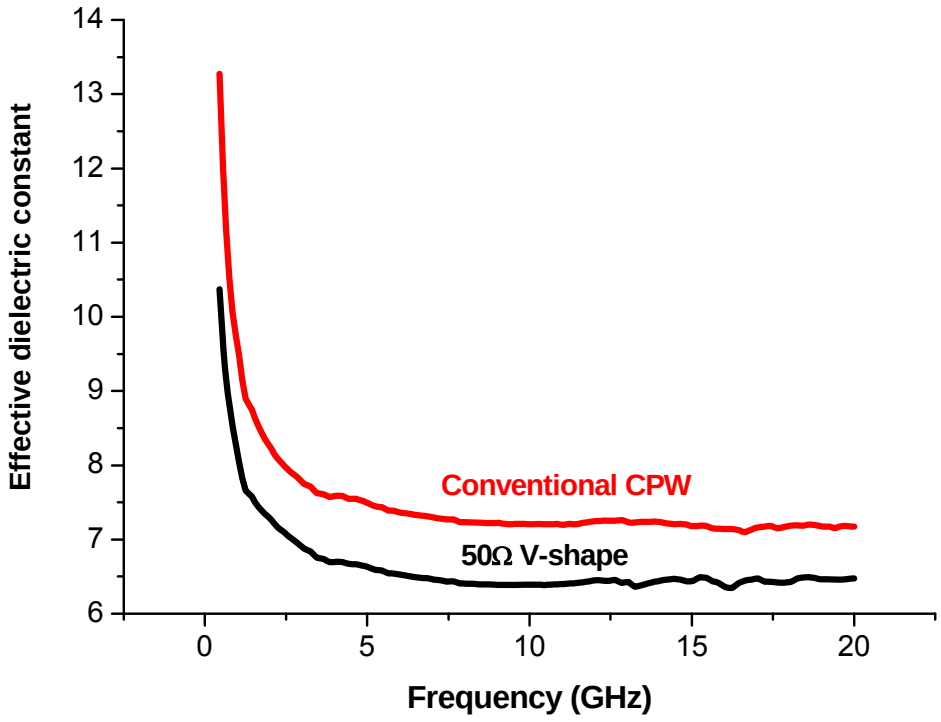
Figure 4.3: Cross-section view of the 50 Ω V-shape transmission line (effective width of the metal is 26 μm and the gap is 10 μm).

The transmission line is measured and then various transmission line parameters are extracted for the designs shown in Figure 4.1 (a) (b). Characteristic impedance is shown in Figure 4.4(a)). Measured results show that the characteristic impedance of the fabricated transmission lines is about 45 Ω. The 50 Ω V-shape has an effective dielectric constant of 6.4 at 10 GHz, comparing with 7.3 for the conventional CPW structure at the same frequency. This is due to the fact that, in V-shape structure, part of the metal strip buried in polyimide layer, which has a lower dielectric constant. We know that for conventional CPW transmission lines, the high current density at the edge of the metal strip would cause the famous current crowding effect. As in multilayer structure, cross-sectional area is greater than the conventional style; this will help to eliminate the current crowding effect. In Figure 4.4(c), we can see that the

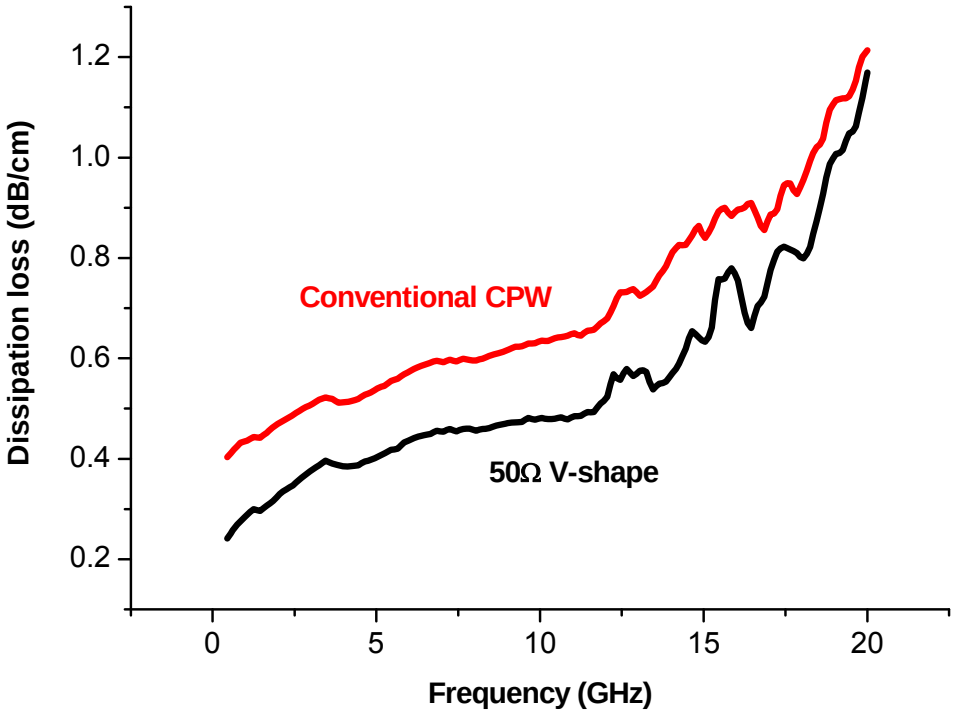
dissipation loss of V-shape design is reduced by 25% comparing with conventional CPW structure at 10 GHz.



(a)



(b)



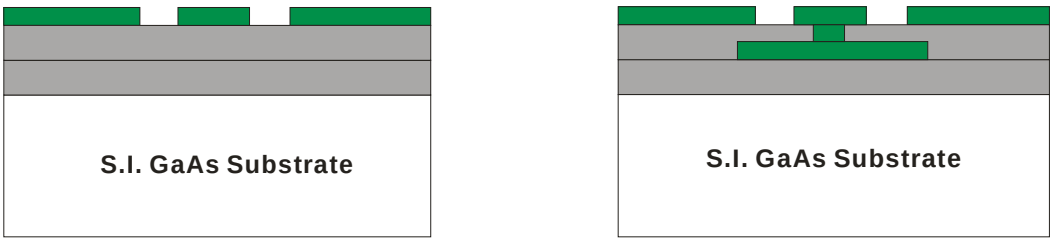
(c)

Figure 4.4: Characteristic impedance, effective dielectric constant and dissipation losses extracted from the measured S-parameters of 50 Ω conventional and V-shape CPW transmission line designs.

4.1.2.2 Transmission line designs of higher and lower characteristic impedances

In MMICs, it is desirable to design transmission lines with characteristic impedance higher or lower than 50 Ω. For example, in applications like broadband bias network and sub-picosecond sampling circuits, CPW transmission lines with characteristic impedance greater than 50 Ω is needed. In conventional designs, higher impedance of CPW transmission lines can be achieved by reducing the centre metal width or raising the gap between centre and ground metal. However, this will either make the conductor loss higher or the circuit become less compact. The similar problem exists when designing CPW transmission lines with lower impedance.

Here we present the following two multilayer designs, partly solving the problem mentioned above. In Figure 4.5(a), the metal strips are lifted onto the low permittivity polyimide layers, thus increasing the characteristic impedance. This solution avoids changing the spacing between metal strips and metal strip width. The gap between centre and ground metal is 15μm; the width of centre metal strip is 20μm. Also, in Figure 4.5(b), we make the metal on M2 layer overlapped with ground metal, therefore decreasing the characteristic impedance. This overlapped design really depicts the advantages that multilayer technique can offer. The overlapping part from fabricated transmission line is 10μm.

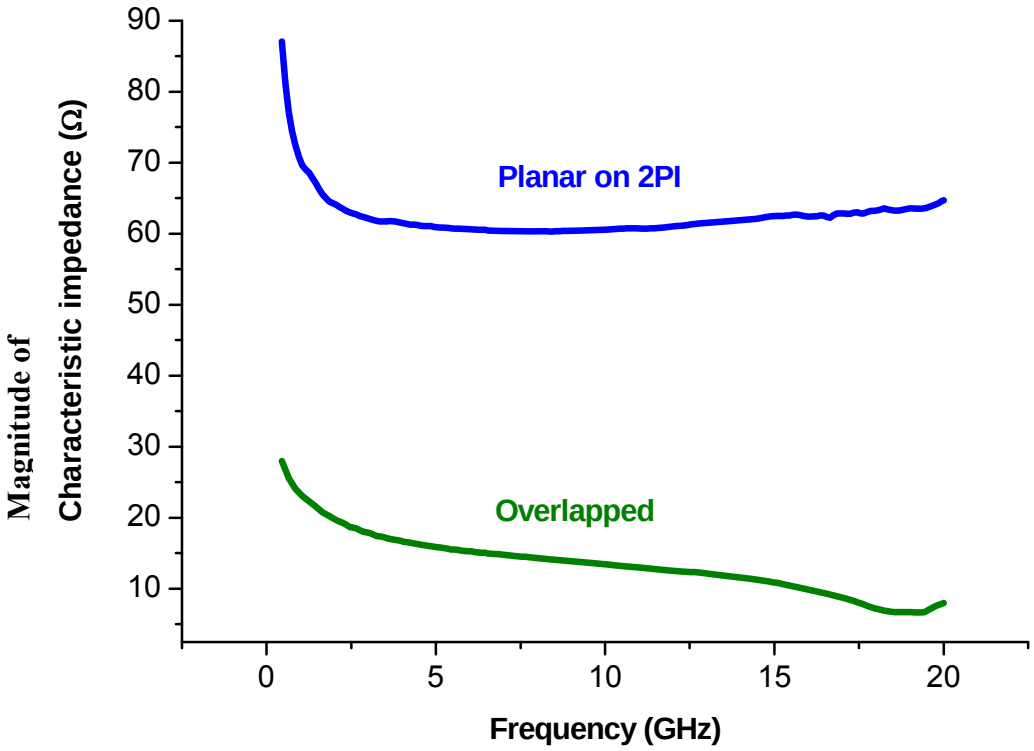


(a) (b)

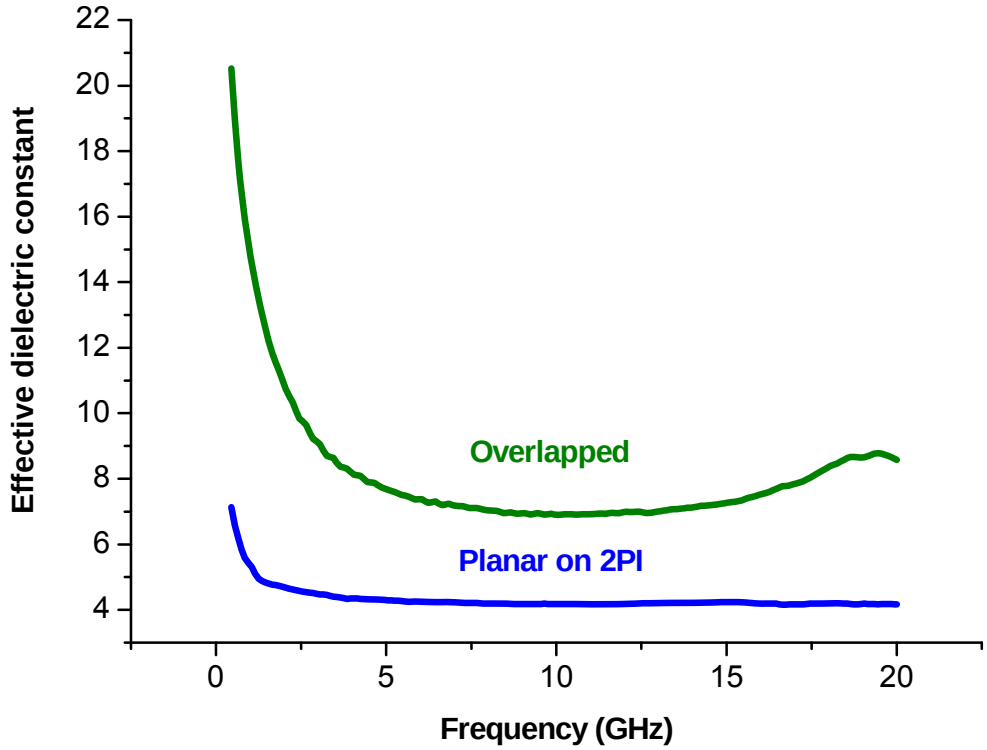
Figure 4.5: Cross-section view of planar on two PI layers (a) and overlapped (b) transmission line designs.

From Figure 4.6(a), we see that the impedance of the transmission line can increase to 65Ω or it can be reduced to as low as 15 Ω. One important feature of multilayer technology is that it offers great flexibility in realizing different characteristic impedances by adjusting the thickness of the layers. As expected, the effective dielectric constant of planar on two PI structure is much lower (about 4 at 10GHz), see Figure 4.6 (b). This is because the polyimide layer has a low dielectric constant of 3.7 as compared with the 12.9 for GaAs. Since the value of effective dielectric constant obtained is close to that of the polyimide (3.7), this means that most of the electric flux happens in polyimide layer instead of GaAs substrate. Also, additional polyimide layer will decrease the losses due to the leakage into the GaAs substrate. In figure 4.6(c), we can see that the dissipation loss is relatively constant with frequency,

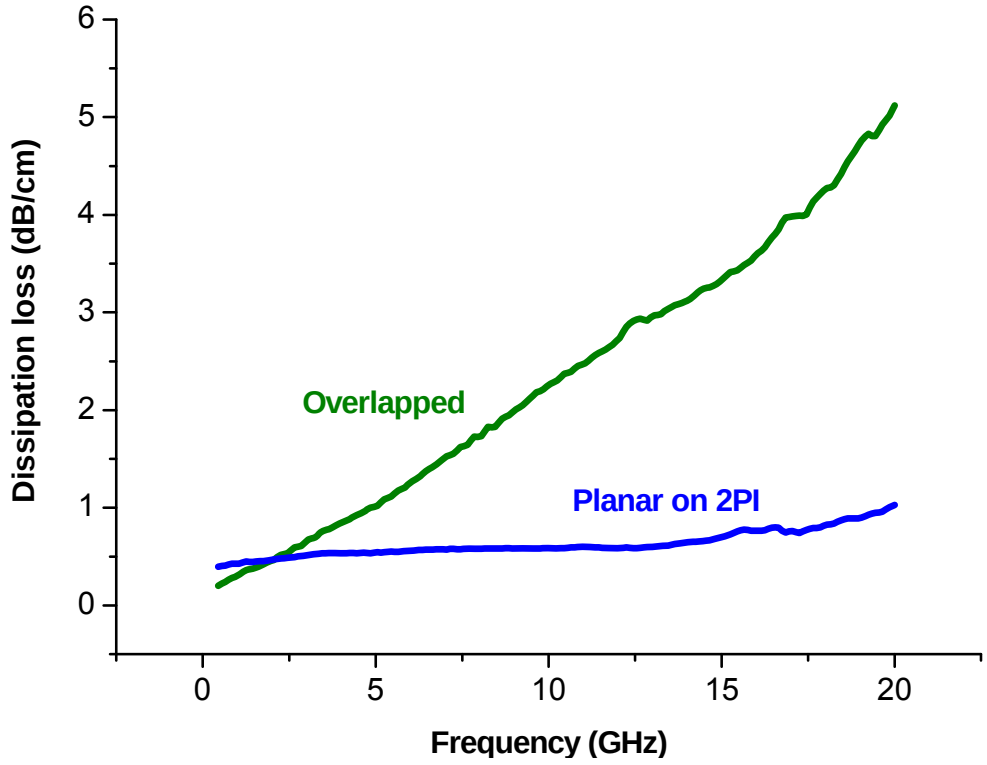
which is better than other designs. The overlapped structure has a high dissipation loss due to the overlapping introduces high current density.



(a)



(b)



(c)

Figure 4.6: Characteristic impedance, effective dielectric constant and dissipation losses extracted from the measured S-parameters of planar on 2PI and overlapped transmission line designs.

4.1.2.3 RLGC modelling

As the S-parameter of the transmission lines without pads are achieved, we can model them as RLGC model using the following equations [Equations (4.6)-(4.9)] [129]:

$$R = \mathrm{Re}\{\gamma Z\} \tag{4.6}$$

$$L = \mathrm{Im}\{\gamma Z\}/\omega \tag{4.7}$$

$$G = \mathrm{Re}\{\gamma / Z\} \tag{4.8}$$

$$C = \mathrm{Im}\{\gamma / Z\}/\omega \tag{4.9}$$

The 'G' component is ignorable at frequency no more than 10GHz, thus we model the

transmission line designs using the RLC modelling. In Table 4.1, the RLC model of four types of CPW transmission lines are shown:

@10 GHz	Conventional	Planar on 2 PI	V-shape (50Ω)	Overlapped
R (Ω/cm)	40.2	33.5	27.5	30.9
L (nH/cm)	4.05	4.05	3.56	0.728
C (pF/cm)	2.00	1.04	1.96	6.72

Table 4.1: Extracted RLC model for various transmission lines.

In Table 4.1, we can see that conventional CPW transmission line has the highest series resistance (40.2 Ω/cm), the other three have lower values due to multilayer technology employed (Figure 4.1). And series resistance directly contributes to the conductor loss of the transmission lines [132]. The ratio of L over C approximately explains the characteristic impedance at high frequency. The V-shape design has similar (50 Ω) characteristic impedance as conventional one with reduced loss. Planar on two polyimide structure shows its advantage in providing higher characteristic impedance. The capacitance of this line (1.04 pF/cm) is reduced as the metal is lifted onto two polyimide layers which have a lower dielectric constant. Overlapped structure is good in achieving low impedance. Its inductance (0.728 nH/cm) is low due to the larger effective metal width. Higher capacitance (6.72 pF/cm) is a result of overlapping effect.

4.1.3 Temperature dependence study of the multilayer transmission lines

4.1.3.1 DC resistance characterization

It is essential to know the DC characteristics of the transmission lines at various temperatures. The DC measurement helps to understand the loss at non-RF environment and the skin-depth issue at high frequencies.

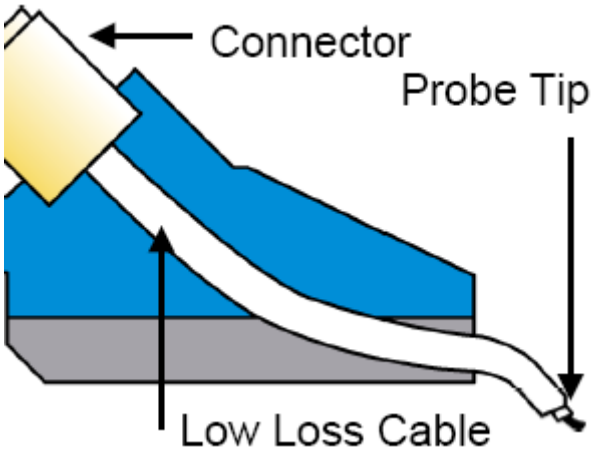


Figure 4.7: The existence of cable resistance and contact resistance in the measurement circuit.

In this work, we use IC-CAP and a DC supply to measure the resistance of transmission lines at various temperatures. Due to the existence of contact resistance of probe tip and cable resistance in the circuit (Figure 4.7), one needs to measure a 'Thru' pattern (Figure 4.8) which is fabricated on the same sample wafer. This needs to be done at each temperature point. And then, subtract the measured 'Thru' resistance from the transmission line resistance data. This step is to remove the extra resistance of pads, cables and contact resistance.

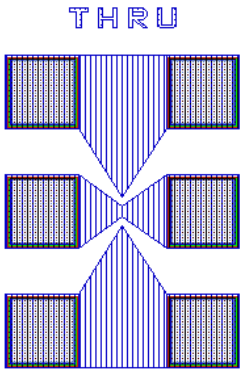
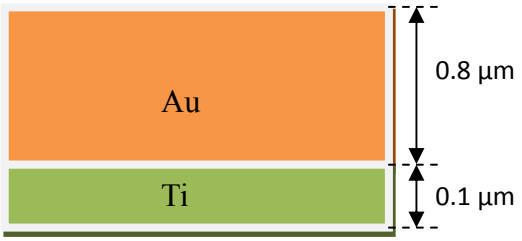
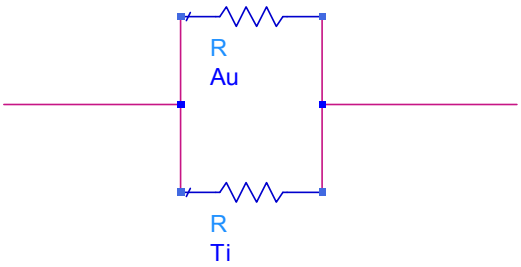


Figure 4.8: Layout of the 'Thru' pattern.

For easier adhesion onto the dielectrics (GaAs or Polyimide), a thin layer of titanium (100 Å) is fabricated on the surface of GaAs prior to the deposition of Au (Figure 4.9(a)). The equivalent circuit can be considered as two resistors in parallel (Figure 4.9(b)). Here, one can verify that the conductor loss is dominated by gold layer.



(a)



(b)

Figure 4.9: Cross-sectional view (a) and the equivalent lumped circuit (b) of the multi-metal structure.

The resistance of metal at DC condition can be given by [130]:

$$R = \frac{l}{\sigma w t} \tag{4.10}$$

where l, σ, w and t are the length, conductivity, width and thickness of the metal respectively.

Meanwhile, $\sigma_{Au} = 4.521 \times 10^7 / \Omega \cdot m$, $\sigma_{Ti} = 2.341 \times 10^6 / \Omega \cdot m$ and the gold layer is eight times thicker than the titanium one. Applying Equation 4.10, it can be derived

that $R_{Ti} = 160R_{Au}$ approximately. Thus, in the paralleled circuit above, current goes through R_{Ti} is extremely small, which can be neglected.

In RF environment of CPW designs, it is mainly the top surface which carries the RF current. The resistance of conductor at RF is controlled by skin depth effect [131]. Current density decays exponentially from its depth. δ_s is defined as the distance the wave travel in order to decay by an amount equal to e^{-1}=8.686 dB. For engineering consideration, it is assumed to be zero current distribution at a 3δs depth from the surface, which is about 0.8 μm in this design. Therefore we can conclude that in our multi-metal stack-up structure [Figure 4.9(a)], it is the gold layer in which the EM wave propagates.

Here is a summary of the DC resistances of the featured transmission lines at various temperatures.

Temperature (°C)	Conventional (Ω/cm)	Planar on 2PI (Ω/cm)	50Ω V-Shape (Ω/cm)	Overlapped (Ω/cm)
-25	19.56	18.1	10.4	6.38
0	21.08	19.68	11.37	6.88
25	22.54	21.16	12.08	7.32
40	23.6	22.22	12.72	7.78
55	24.62	23.22	13.26	8.1
70	25.54	24.14	13.72	8.365
125	28.78	27.3	15.42	9.34

Table 4.2: Measured DC resistance of 3-D transmission lines at various temperatures.

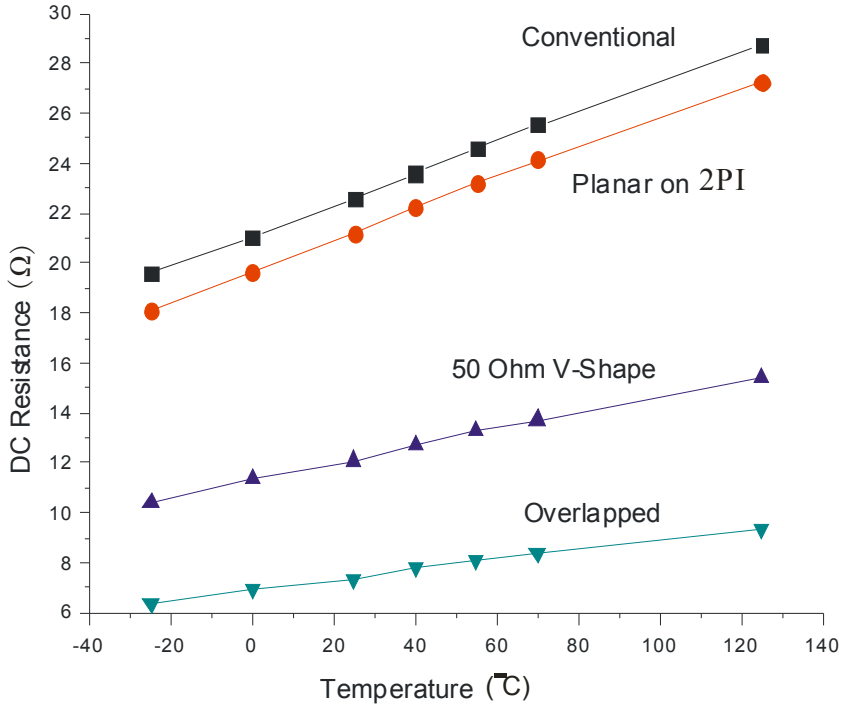


Figure 4.10: DC resistance versus temperature for various 3D transmission lines.

In Figure 4.10, one can see that at DC condition, the conventional CPW transmission line has the largest resistance. This is mainly due to the thin gold metal used in this structure. In the V-shape and overlapped structures, more than one gold layers are employed. The total thickness (t) and the equivalent width (w) of the metal can be increased and according to Equation 4.10, the resistance can be reduced substantially. The resistivity of any metal is temperature dependent and it increases with temperature. The resistivity of a metal is given [132].

$$\rho = \frac{(3K_B mT)^{\frac{1}{2}}}{n\lambda e^2} \tag{4.11}$$

where, K_B = Boltzmann constant, m = mass of the electron, T = absolute temperature, n = density of the electrons, λ = electron mean free path, e = unit charge.

The plot shown in Figure 4.11 is an overview of the increase of measured resistance

along the temperature. All the results are normalized to percentage with respect to the resistances at room temperature.

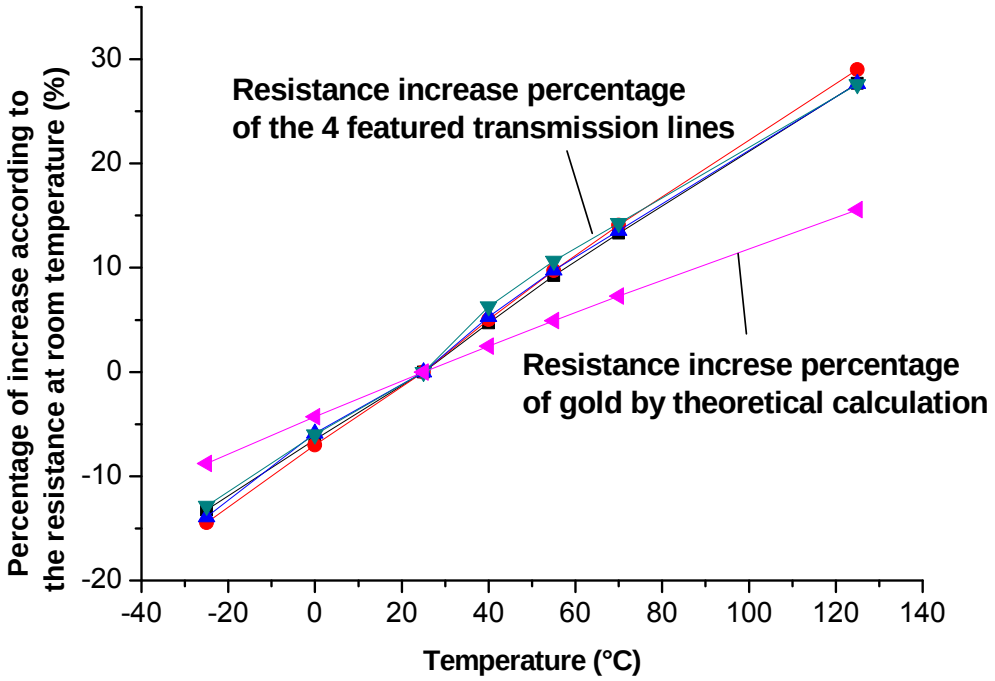


Figure 4.11: Percentage (with respect to room temperature) of resistance increase with temperature.

The pink line in Figure 4.11 is calculated by applying Equation 4.11, assuming all the other parameters unchanged with frequency except T. One can observe that the other four lines in the data of Figure 4.11 match very well. Thus it can be concluded that the temperature dependent performance is mainly related to the metal employed, it has nothing to do with either the structure of design or the dimension of the transmission lines. Another interesting point we can see from Figure 4.11 is that in real circuits the resistance increases and decreases with temperature much sharper than the values from theoretical results.

4.1.3.2 RF characterization

Each Z_0 shown in the Figure 4.12 is an average value of two sets of measured data

ensuring higher accuracy. As our transmission lines are aim to work at about 10GHz due to the length (2mm), the values taken in the Figure 4.12 are at 10GHz.

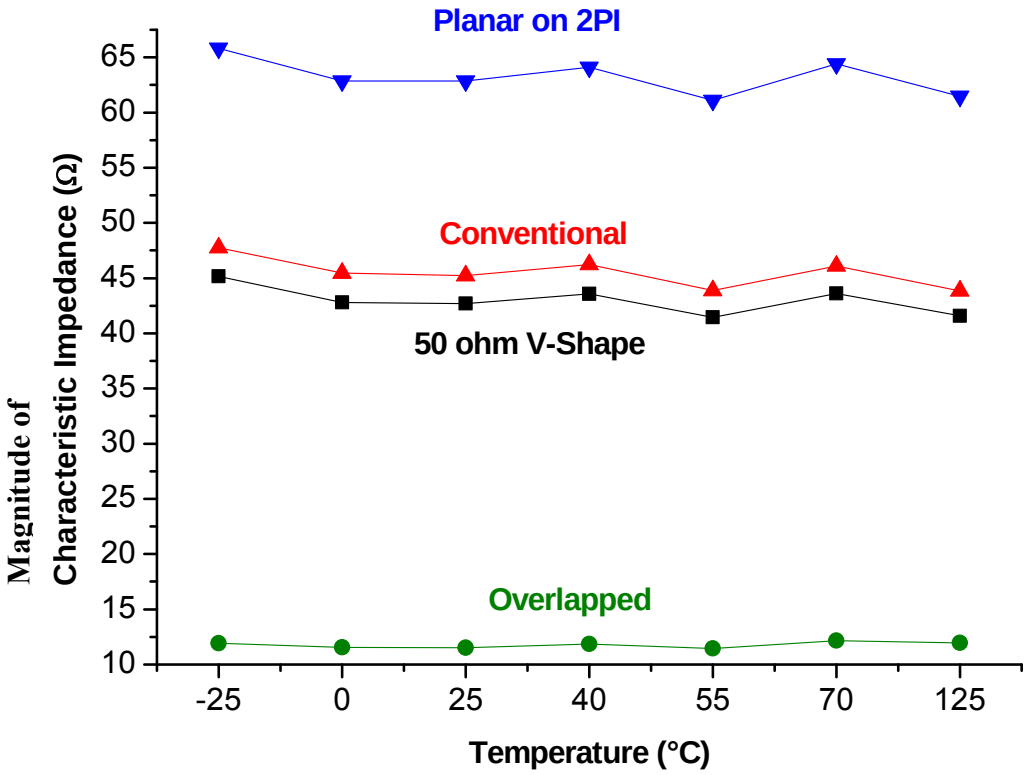


Figure 4.12: Characteristic impedance of four featured designs versus temperature at 10 GHz.

The variation of characteristic impedance versus temperature data of Figure 4.12 can be described mainly by the change of resistance of the metal and conductance of the dielectric layers. As Equation (4.10) shows, when the frequency increases (10 GHz in this experiment), the characteristic impedance becomes dominated by the ratio of total inductance to capacitance of the transmission line. Thus, we can expect a small variation in characteristic impedance as temperature changes.

Another parameter that we have considered in the study of transmission lines is the effective dielectric constant and its variation with temperatures as shown in the extracted data given in Figure 4.13. As explained, both inductance and capacitance don't change largely along the temperature. Therefore, we can predict that effective

dielectric constant can be regarded as relatively constant with temperature changes.

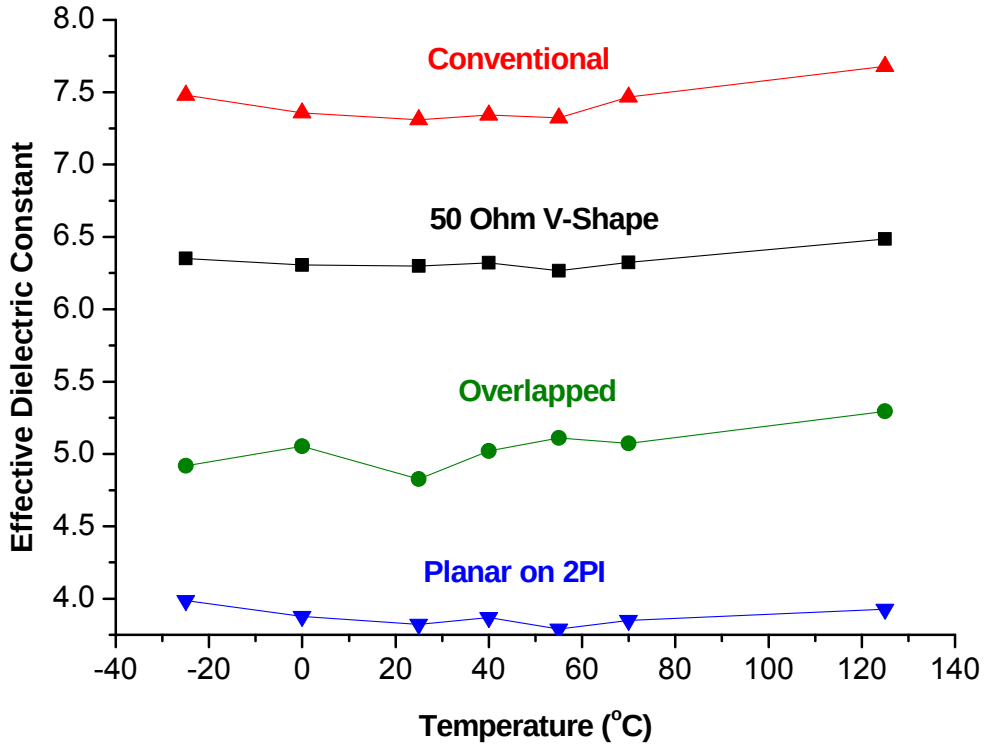


Figure 4.13: Effective dielectric constant of four featured designs versus temperature at 10 GHz.

The total loss in transmission lines is the sum of DC series resistance loss and AC resistance loss. It is described in [132] that important mechanisms that absorb energy from the signal must be taken into account when predicting the behaviour of interconnects: series resistance of the signal and the shunt leakage through the dielectric material. The series resistance of the signal and the return-path conductors increase with the square root of frequency because of the skin-depth effects. At higher frequencies, the series resistance increases, as does resistive heating. Figure 4.14 is a plot of extracted series resistance from measured results of a conventional CPW transmission line as a function of frequency at various temperatures.

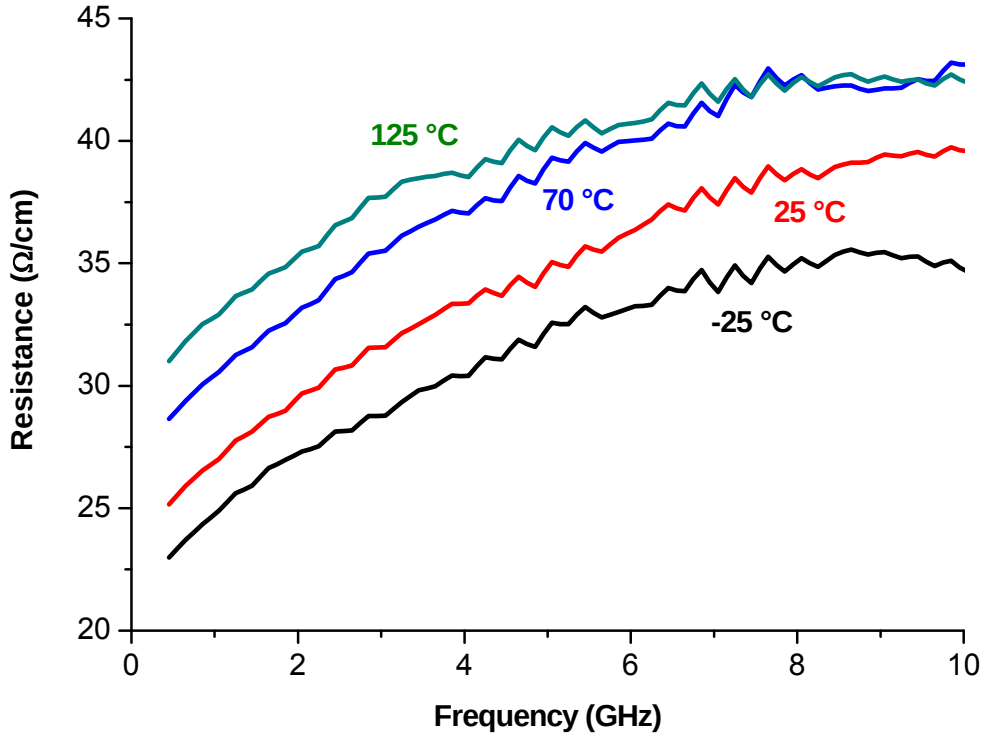


Figure 4.14: Extracted series resistance versus frequency for the conventional CPW transmission line at various temperatures.

It is depicted in the figure above that the higher the temperature environment, the higher series resistance will be. For all the data in Figure 4.14, the trends become flat when it approaches 10 GHz. There is a similar trend we can find in the plot of skin depth of the Au metal with frequency as shown in Figure 4.15.

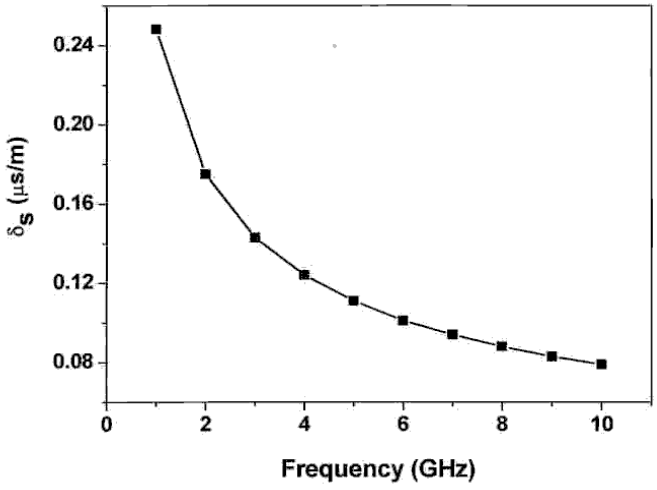


Figure 4.15: Skin depth of the Au metal with frequency.

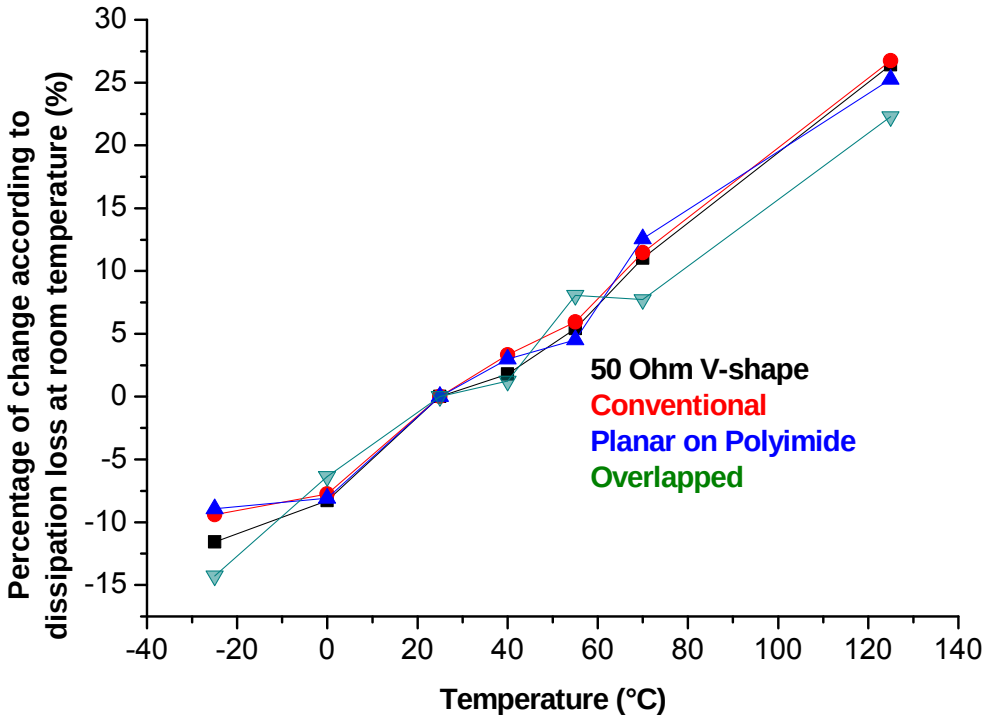


Figure 4.16: Percentage of dissipation loss change according to the dissipation loss at room temperature.

In Figure 4.16, the changes of the dissipation loss with temperature for all the four featured transmission lines are presented. Although the dissipation loss of overlapped structure is much higher than other structures (shown in Chapter 4.1.2.2), the changing rate still matches with other three designs. Thus, the temperature dependence of dissipation loss is not related to the different designs. In other word, the various multilayer structures don't have negative effect for circuits working under different temperatures conditions.

In Figure 4.17, one can make an average trend of change in dissipation loss for all structures, plotted with the average changing rate of DC resistance shown in Chapter 4.1.3.1. The two curves match quite well, shown a deviation of no more than 4%.

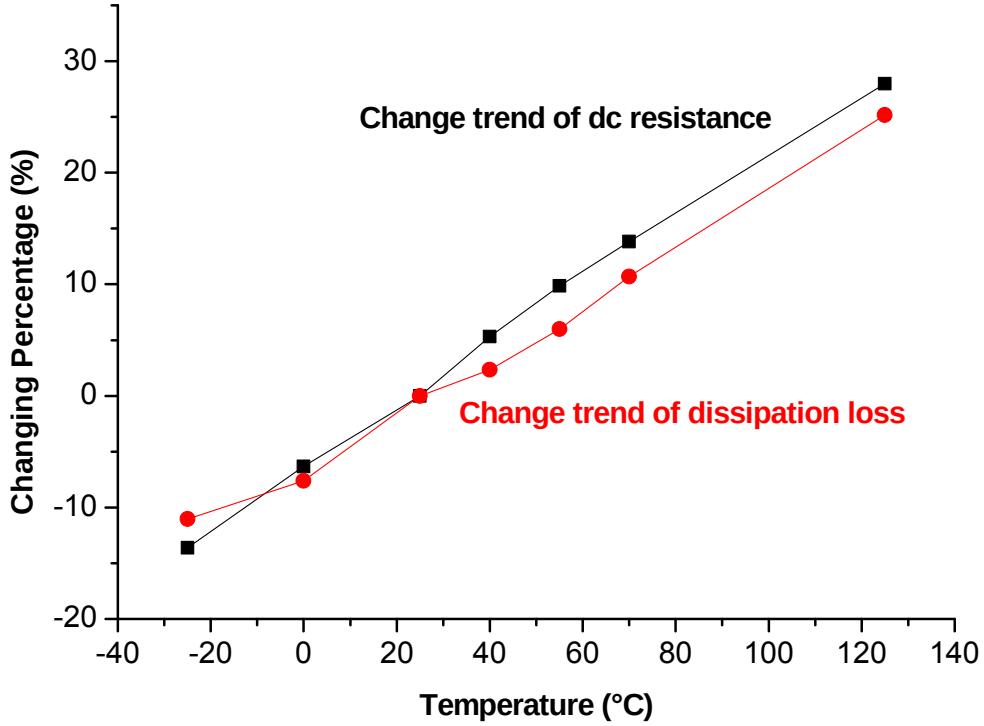


Figure 4.17: Relationship between DC resistance and dissipation loss for the featured transmission line.

4.1.4 Investigation on alternative transmission line designs with various centre and ground metal position

In multilayer MMIC circuit designs, one could face choosing from different realizations of transmission lines for matching or connecting purposes. Or due to restrictions of other components around, we may be forced to use one specific design of transmission line. Such question would come up: is the transmission line suitable for the circuit, or simply will it degrade the overall performance of the circuit? On the other hand, CPW multilayer technology introduces flexibility of designing MMIC components. Due to the nature of multilayer structure, variation of ground and

centre metal combination needs to be investigated before applying any new design. Thus it is necessary to study the effect of various ground and centre metal positions in the transmission line designs. In order to investigate on the issue, we developed nine different combinations of centre and ground metal positions (Figure 4.18). These transmission lines are all designed with a centre metal width of 20 µm, a gap between centre and ground metal of 15 µm. The length of the transmission lines are all 2 mm.

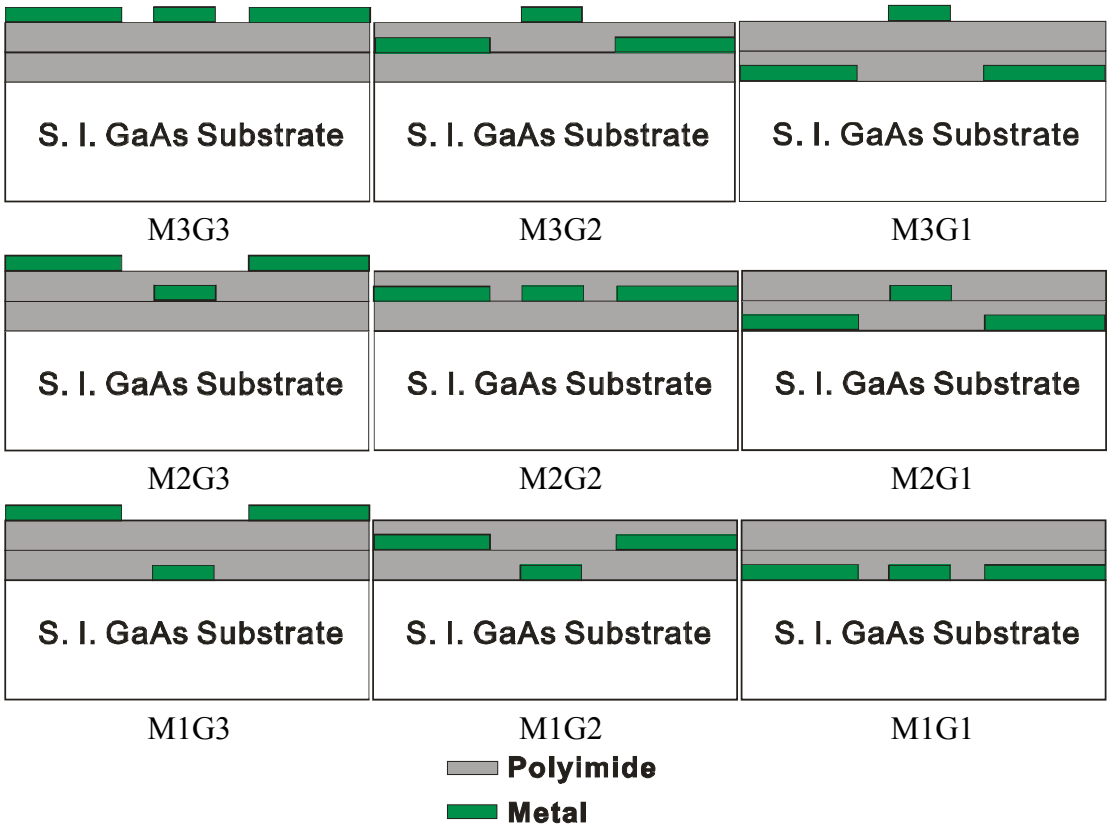


Figure 4.18: Cross-sectional view of nine 2 mm transmission line structures.

The nine structures presented in Figure 4.18 are simulated in ADS momentum. S-parameters are used to calculate effective dielectric constant, indicated in Figure 4.19. It is clear that the effective dielectric constant is dependent on the material that wave propagates in. In this case, for the transmission lines, the wave mostly propagates in the air (ε_r = 1), the polyimide layer (ε_r = 3,7) and the GaAs substrate

(ε_r = 12.9). These three dielectric constants will contribute to the effective dielectric constant. Among the nine combinations we investigate, for metal placed on the layer 1 (M1GX), those dielectric constant will be much higher than those metal placed on layer3 (M3GX). For M1GX, half of the electric flux will be inside the high permittivity substrate. On the other side, once the centre metal has been lifted, low permittivity polyimide will lower the effective dielectric constant. The position of ground metal can also make changes in effective dielectric constant, but not as much as centre metal. If we extract the effective dielectric constant at 10GHz for each transmission lines, and plot this with various metal positions, the data are shown in Figure 4.20. From this figure it can be concluded that the centre metal positions have more influence than the ground metal positions on the magnitude of dielectric constant.

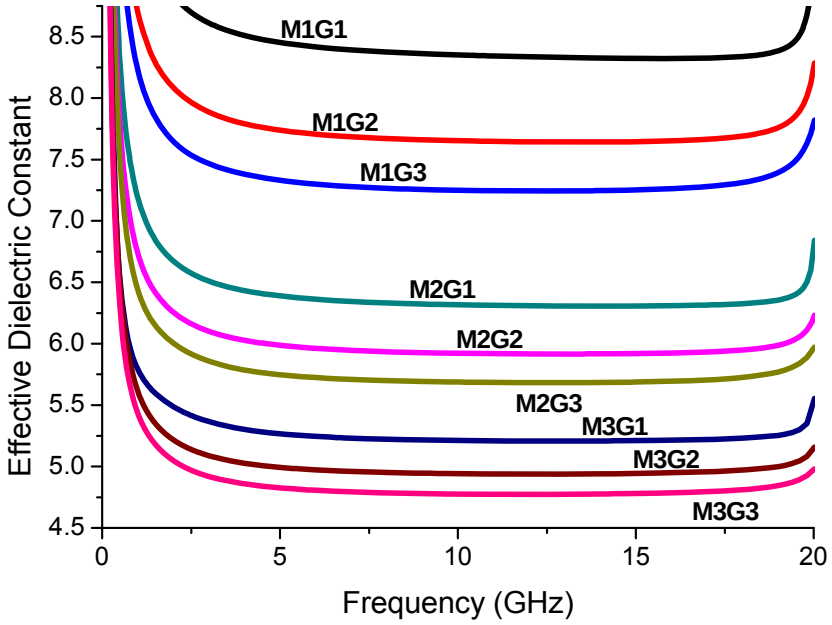
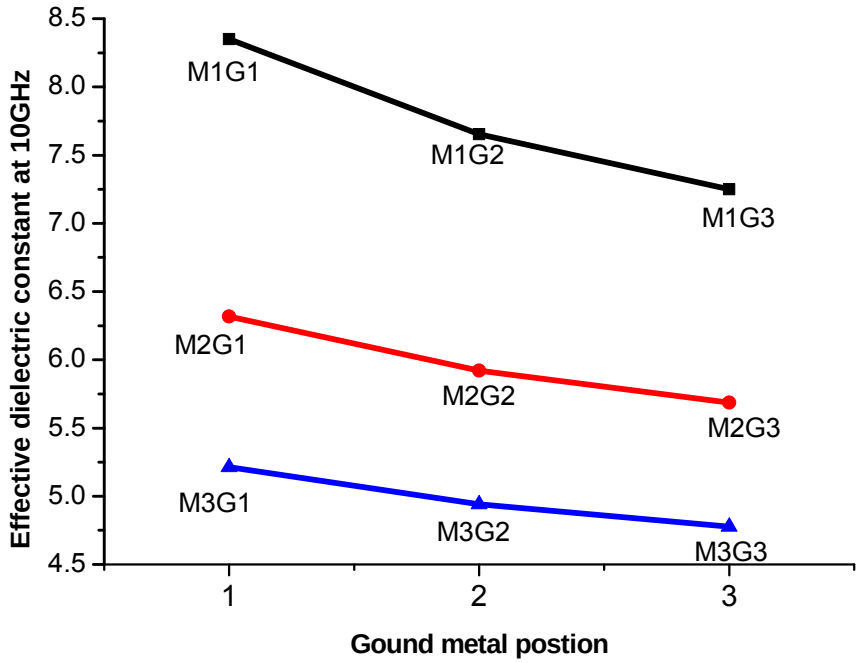
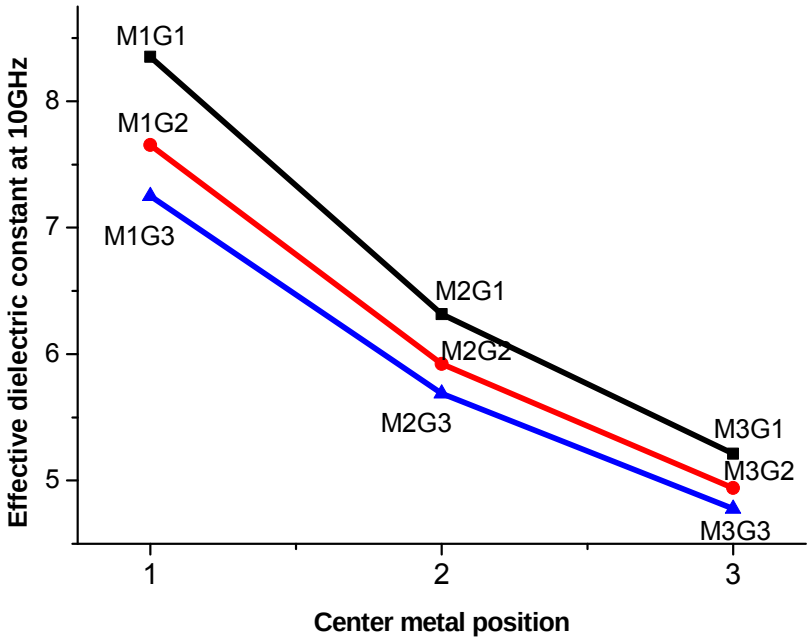


Figure 4.19: Extracted effective dielectric constant of the nine transmission lines from simulated S-parameters.



(a)



(b)

Figure 4.20: Comparison of various metal positions [ground metal position (a), centre metal position (b)] with their effective dielectric constants at 10GHz.

Characteristic impedance is also calculated ($Z = Zsys\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}$), and the data are shown in Figure 4.21. From this data it is noticed that the nine data graphs can be

divided into three groups. Transmission lines that centre metal located on layer three have higher characteristic impedance, than the ones that centre metal on layer two or layer one. It is also obvious that for the same group (centre metal on the same layer), those ground metal on higher layers have a larger impedance.

The impedance $Z \propto \sqrt{\frac{L}{C}}$, for the transmission lines with the same width, the inductance would stay constant for a given frequency. However $C = \frac{\varepsilon_0 \varepsilon_r A}{d}$, and it changes as each combination of centre and ground metal, this is proved in previous section. From this equation, it is easy to know that Z is related to $\sqrt{\varepsilon_r}$. The results shown in Figure 4.21 actually match with the ones in Figure 4.19.

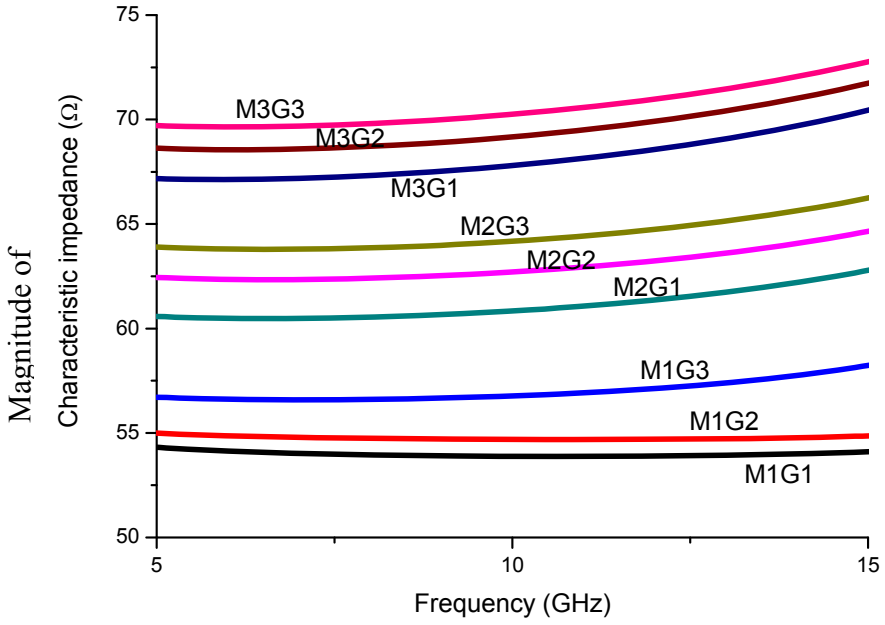


Figure 4.21: Extracted characteristic impedance of the nine transmission lines from simulated S-parameters.

Dissipation loss in transmission lines can be analysed by considering four issues: loss due to metal conductivity, loss due to dielectric loss tangent, loss due to conductivity of dielectric and loss due to radiation. Loss due to substrate conductivity can be

ignored as this is a GaAs substrate, loss due to radiation can also be neglected as it is too small comparing with other factors. In Figure 4.22, dissipation loss (DL) of nine structures are calculated using equation $DL(dB) = 10\log\frac{(1-|S_{11}|)^2}{|S_{21}|^2}$. We noticed that generally dissipation loss doesn't change much in these nine structures especially for frequency below 10 GHz. The exceptional is that the M1G1 curve is far depart from other data. This phenomenon is still to be studied in more detail. Although it doesn't show much difference from structure to structure, we still see that those M3 designs have better performance than M1 ones. This is mainly due to the increase of dielectric loss in those M1 structures as $\alpha_D = \tan(\delta)\frac{\omega C Z_0}{2}$. C is the capacitive equivalent component of the transmission line and from previous discussions we know that this parameter increases as the metal approaches substrate.

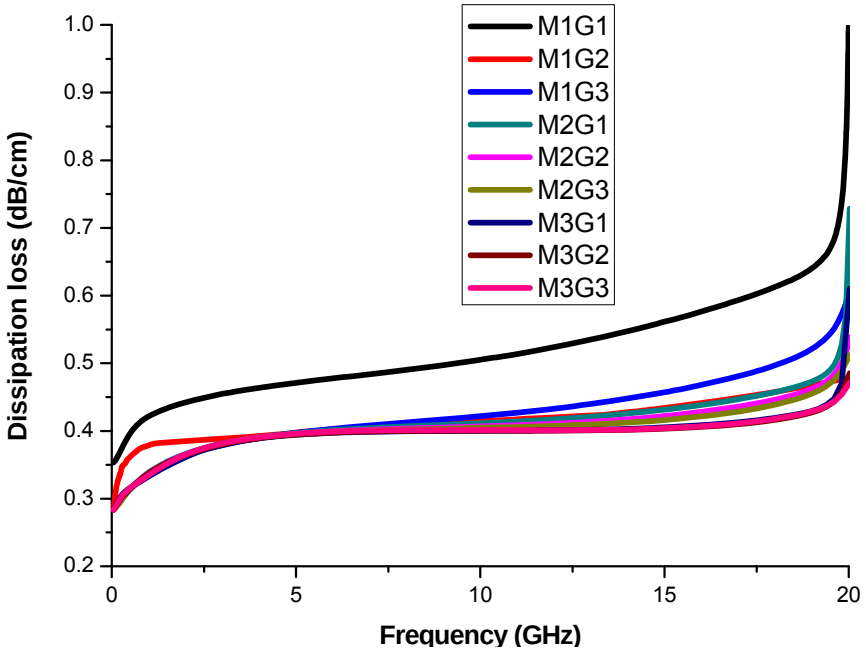


Figure 4.22: Extracted dissipation loss of the nine transmission lines from simulated S-parameters.

4.1.5 Study of transmission lines using eye diagram

From Chapter 4.1.1 to 4.1.4, we use S-parameters to characterize 3D transmission line designs. It is also interesting to know how these designs give respond to '1's and '0's. Thus, in the following session, we will employ eye diagram to study the 3D transmission lines.

During the measurement of eye diagram, the equipments are calibrated to match 50 Ω impedances. This will cause the effect of mismatch on some of the 'non-50Ω' structures such as 'overlapped' designs.

Eye amplitude indicates the power in the eye diagram that actually carries information and does not account for the noise that may exist in the signal. It is defined as the difference between the one and zero levels histogram mean.

The eye amplitude of the conventional, planar on 2 polyimide layers and overlapped designs have been extracted from their measured eye diagram and these are shown in Figure 4.23. The structure with two polyimide layers shows larger eye amplitude comparing with the conventional one. Overlapped design has much smaller eye amplitude at about 10 GHz; this is due to the high current density between the overlapped metal as well as the mismatch problem mentioned above.

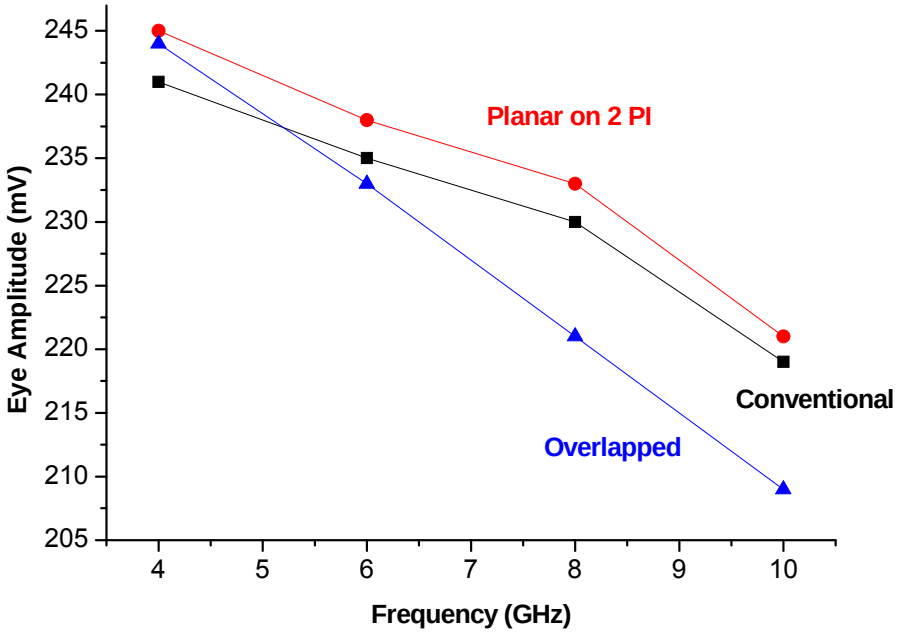


Figure 4.23: Eye amplitude of three transmission line designs.

In Figure 4.24, two groups of transmission lines are measured. One group (labelled using circles) is the transmission lines with a centre conductor of 40 μm width. The second group (labelled squares) has a centre conductor of 20 μm width. Each group has three designs including conventional design, planar on one polyimide layer and planar on two polyimide layers. All the transmission lines studied in Figure 4.24 have been optimised to have characteristic impedance of 50Ω. The data in Figure 4.24 show, to some extent, the influence of employing polyimide layers although the differences are rather small. Increasing the width of centre conductor by 50% (from 20 μm to 40 μm) will reduce the resistivity of the transmission line, and resulting in slightly better eye amplitude (3% in average). Therefore, this observation may indicate that the transmission lines with 20 μm width is a good compromise between compactness and performance. Another point can be seen that the transmission lines with polyimide layers have generally larger eye amplitude than those with conventional design, but there is not much differences between the data for the one or two polyimide layers.

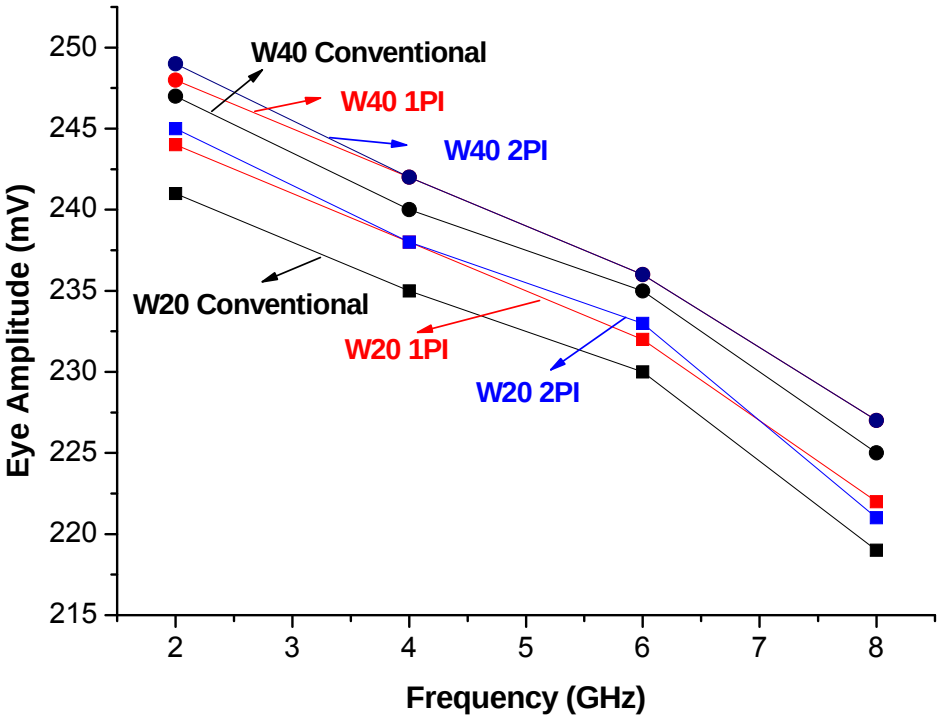


Figure 4.24: Eye amplitude of six designs showing the effect on existence of polyimide layers.

Another parameter of eye pattern to consider is eye height. This parameter depicts the clear part of the signal which is free of any losses (both timing and voltage losses). It gives the vertical opening of the eye diagram. The point of largest eye height appears in the eye diagram usually be chosen as the sampling time. The difference between eye height and eye amplitude can be seen as the distortion at sampling time. So it is desirable to have the minimum deviant from eye amplitude and eye height. The height of the eye opening in most passive components is more dependent on the noise or any other distortion in the data signal.

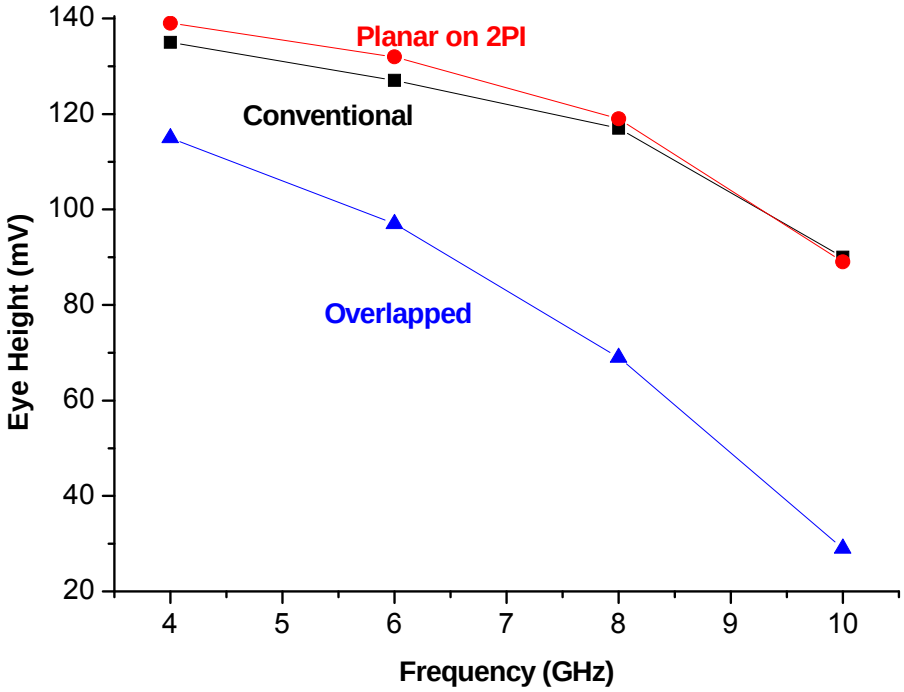


Figure 4.25: Eye height of three featured designs.

Figure 4.25 is the plots of the eye heights for the three transmission line designs. From this data it is seen that the planar on polyimide structure shows good eye height characteristic and this data is slightly better than those for the conventional design. At about 10GHz, the data approaches the conventional one. The overlapped design shows significant eye height degradation. This is interesting since this design also showed rather poor dissipation loss at high frequency (Figure 4.6(c)). The large depart from the other two designs may partly due to the mismatch issue in calibration.

One advantage of the time domain characterization is that the noise level in the system can be specified by Signal to noise ratio. Signal to noise ratio (S/N or SNR) is a measure of the signal strength relative to background noise. It is usually measured in decibels (dB). It is given by:

$$SNR = 20\lg\left(\frac{A_{signal}}{A_{noise}}\right) \tag{4.12}$$

where A is the rms amplitude of signal and noise level measured at the same or equivalent points in a system.

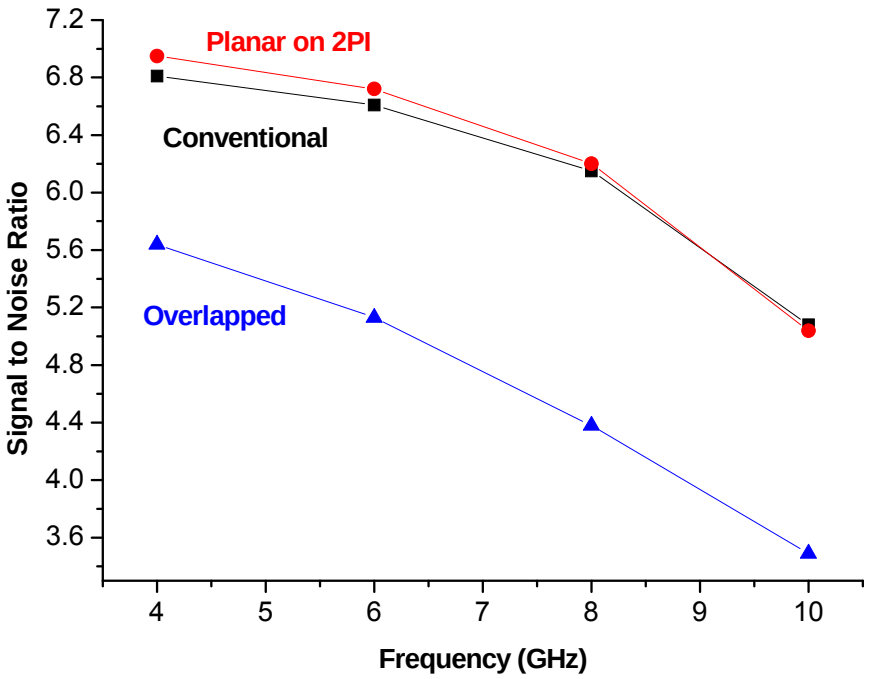


Figure 4.26: SNR of three featured transmission line designs.

	Transmission line designs	@ 4GHz	@ 10 GHz	Percentage of degradation
Eye Height (mV)	Conventional	135	90	33
	Planar on Polyimide	139	89	36
	Overlapped	115	29	75
SNR	Conventional	6.81	5.08	28
	Planar on Polyimide	6.95	5.04	27
	Overlapped	5.64	3.49	38

Table 4.3: Percentage of degradation in eye height and SNR for various transmission lines.

From the data in Figure 4.25 and 4.26, it is shown that the eye height and SNR are related together since both the conventional and planar on polyimide have better eye characteristics than the design with the overlap. As we consider the difference between 'Conventional' and 'Planar on 2PI' in Figure 4.26, it is expected that the 'Overlapped' would still perform a lower SNR comparing with other structure even if the mismatching effect has been removed. Table 4.3 is a summary of the degradation in eye height and SNR from 4 GHz to 10 GHz for the devices studied. From the data in Table 4.3 it is seen that both eye height and SNR are highly dependent on the noise level in the data signal.

It is also of interest to study the eye parameters of the overlap transmission line with having various overlap values. For this reason Figure 4.27 shows the eye height and eye amplitude with the overlaps of 1, 10 and 20 μm values. Generally, we can conclude that the larger overlapped value, the greater degradation with frequency will be. It is also seen that a larger fall of eye height with increase of frequency than the eye amplitude, which is due to more distortion introduced at the sampling time.

The percentage of decrease in the eye amplitude and eye height is shown in Figure 4.28. As the three samples have almost the same characteristic impedance of around 10 Ω, the mismatch problem can be ignored when studying the behaviour between them. This data indicates that a larger overlapped length would result in a larger fall of eye amplitude with frequency. One can interpret this when on considers the fact that the design with larger overlapped can produce, the higher current density and subsequently higher dissipation loss.

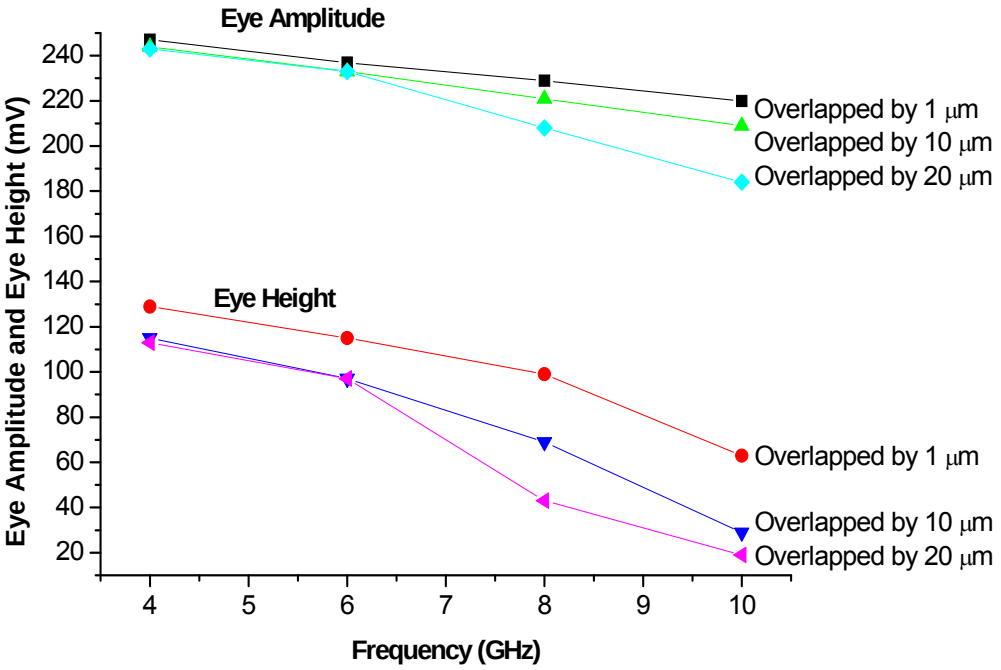


Figure 4.27: Eye amplitude and eye height of different overlapped dimension transmission lines.

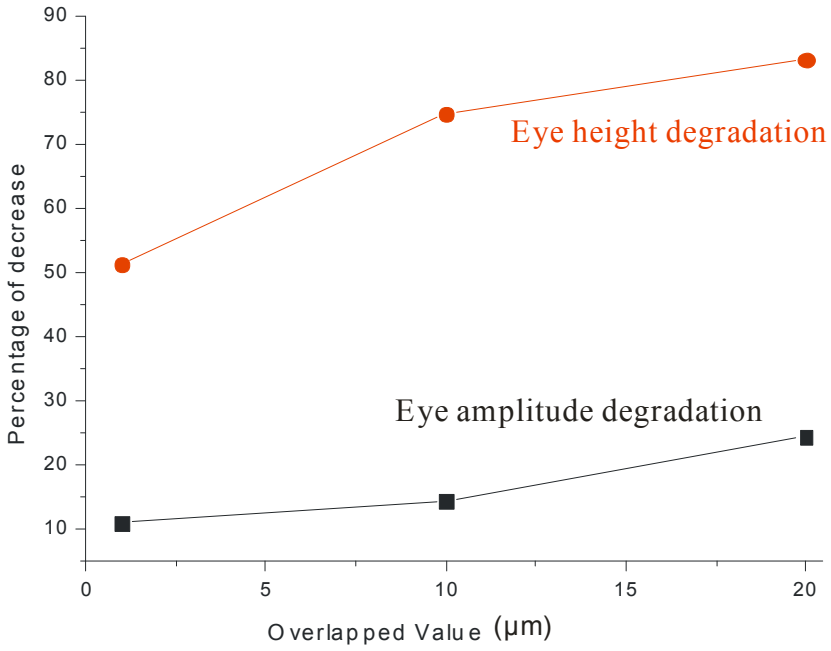


Figure 4.28: The effect of overlap length of the transmission lines on eye amplitude and eye height.

The next eye parameter to be investigated is the eye jitter. The width of the crossover represents the amount of jitter present in the signal. At high frequency, the jitter can no longer be neglected. Thus the jitter should be measured to characterise reliability of the transmission system. It is a measure of the combined effect of skews, reflections, pattern-dependent interference, propagation delays and noise that degrade the signal quality. Time delay and skew are affected by the insulation material and twisting of conductors and also mainly by the variance in the dielectric constant. Usually jitter will be taken into consideration for the timing budgets [133].

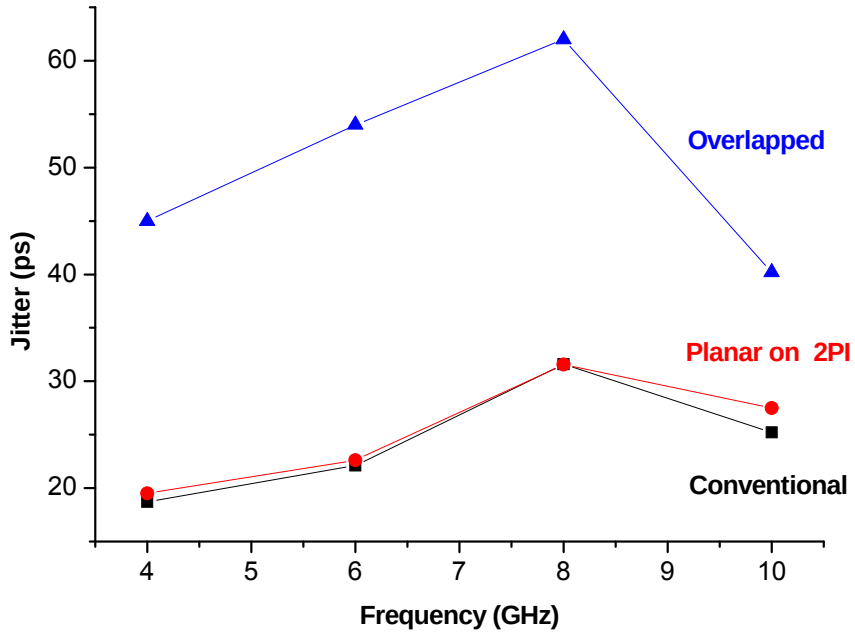


Figure 4.29: Variation of jitter versus frequency for the three featured transmission line designs.

It is depicted in Figure 4.29 that jitter increase with frequency generally. This parameter increased by 50% with the frequency range between 4 GHz and 8 GHz. As it reaches the operation frequency of 10 GHz, jitter is reduced with 33%. It is because another major jitter ingredients results from signal reflections that radiates back and forth on a transmission line due to termination impedance mismatches. Both 'Overlapped' and 'Planar on 2PI' have non-50Ω characteristic impedance, jitter of

'Planar on 2PI' is close to conventional design while jitter of 'Overlapped' is much higher than the other two designs. This indicates that mismatch in calibration doesn't play a major role here.

Another parameter of the eye pattern to consider is the rise time which is a measure of the mean transition time of the data on the upward slope of an eye diagram. The data crosses through the following three thresholds: the lower, middle and upper thresholds, as well as through the eye crossing point. A histogram is first constructed to find the mean location of the crossing points relative to level 1 and level 0 positions. Histograms are then constructed at each of the three threshold levels (e.g. the 20%, 50% and 80% points on the transition). The histogram mean at which the data crosses the separate threshold level is determined. The time difference between the 80% and 20% crossing point determine the rise time performance [133].

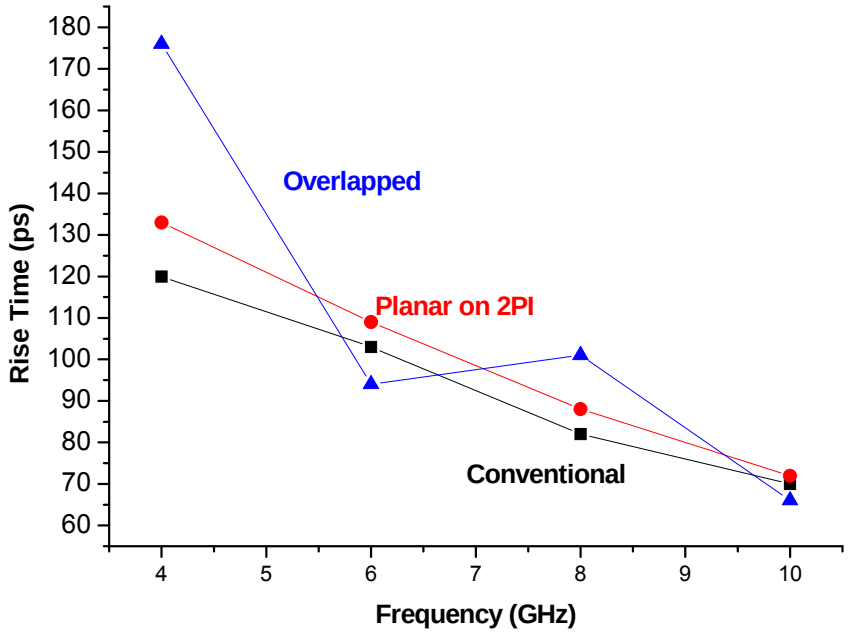


Figure 4.30: Variation of rise time with frequency for the three featured transmission line designs.

As defined above, the rise time determines the slope of the eye, which is also related

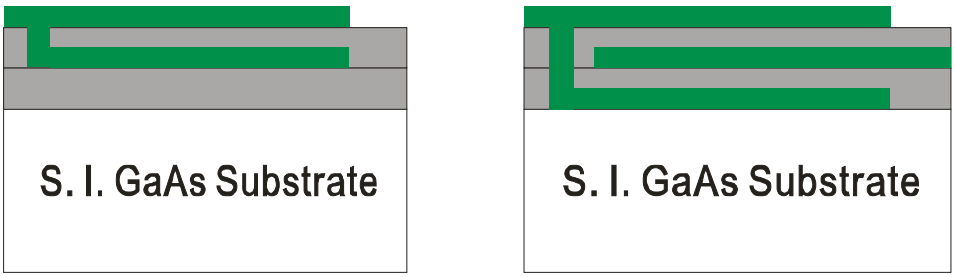
to the sensitivity of the timing error. The dominant problem that transmission line loss creates is the degraded rise time. The degradation (Table 4.4) becomes a serious problem when the degraded rise time is comparable to the signal's bit period. Then, the received waveform's precise shape depends on the previous bit pattern, causing inter symbol interference (ISI). The bit rate in this experiment is 27, which means the transmission lines can be working at 10 GHz without ISI. Figure 4.30 shows the variation of rise time with frequency.

Structure	@ 4 GHz (ps)	@ 10 GHz (ps)	Percentage of degradation
Conventional	120	70	42
Planar on Polyimide	133	72	46
Overlapped	176	66	63

Table 4.4: Percentage of rise time degradation of three transmission line designs.

4.2 CPW multilayer MIM capacitors

In MMICs, it is the passive devices that occupy most space on the chip. Thus, for compact chip designs, it is always desirable to minimize the passive components. Size of capacitors can be greatly reduced in multilayer technology due to the fact that more than 2 metal layers can be employed in this technology. The designs of conventional and folded MIM capacitors are shown in Figure 4.31.



(a) (b)

Figure 4.31: Cross-sectional view of conventional (a) and folded (b) multilayer MIM capacitors.

4.2.1 Multilayer MIM capacitor modelling

Some equivalent circuits have been studied to achieve a good first-pass design success. Most of these capacitors are based on lumped components. R. Kulke presented an equivalent circuit of ten elements for MIM coplanar capacitors on GaAs in [134]. The evaluations had been made up to 67 GHz. Another nine-element lumped model for the MIM capacitor is then introduced in 2006 by Kalavathi Subramaniam [135]. Later, a six-element equivalent circuit is carried out by Noel Segura and is applied for 3D MIM capacitors in BICMOS technology [136].

In the multilayer CPW structures studied in this project, there is less parasitic and substrate loss is very small, thus some components could be ignored. Figure 4.32(a) is a complete seven-lumped-element equivalent circuit for a multilayer CPW MIM capacitor. In which, C_{pad} and L_{pad} are the parasitics of the probing pads, L_s is the inductive behaviour of the short interconnects, R_s is the series resistance of the interconnects and metal plates, C_g is made of the capacitance from two metal plates to the substrate, R_p is the parallel resistance between two metal plates to prevent leakage and C_p is functional capacitor.

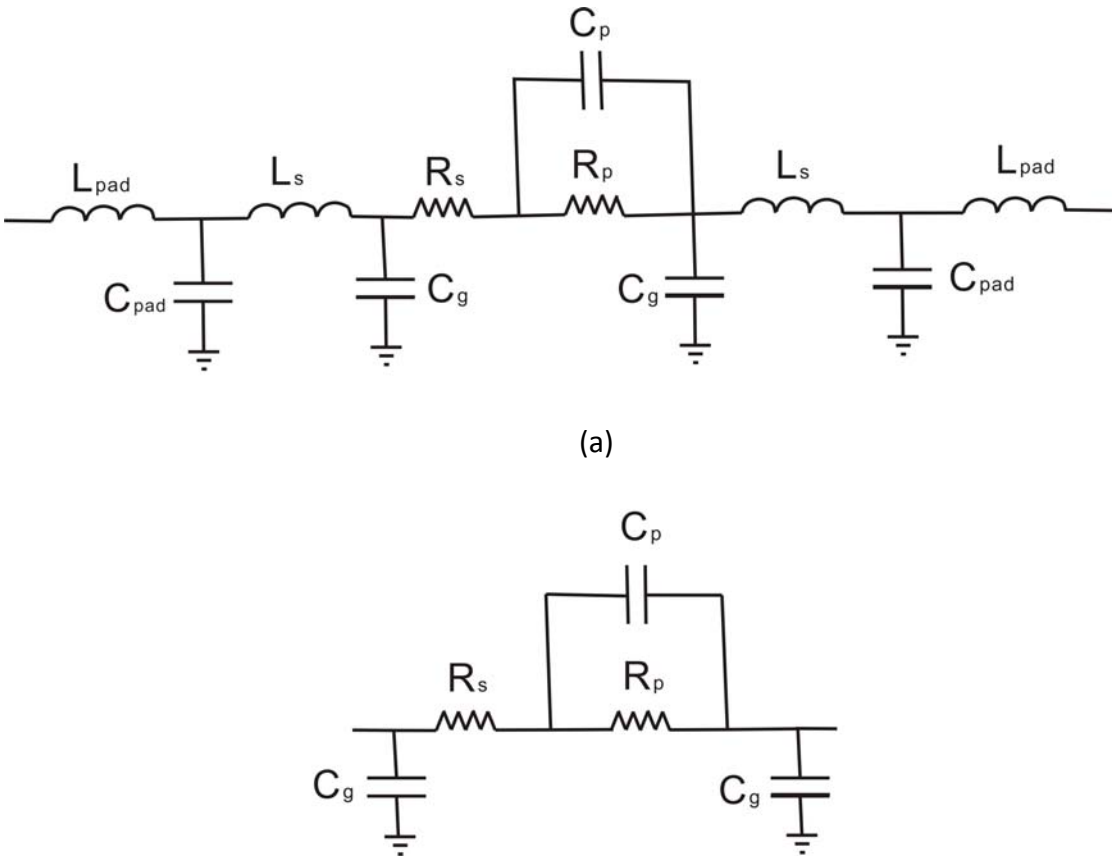
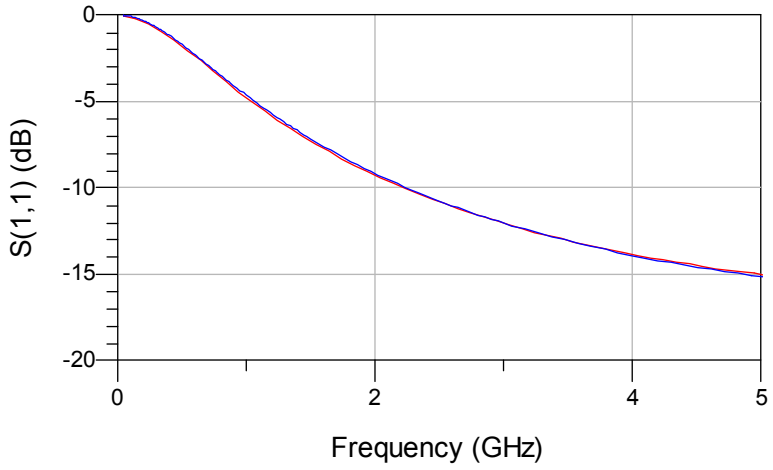
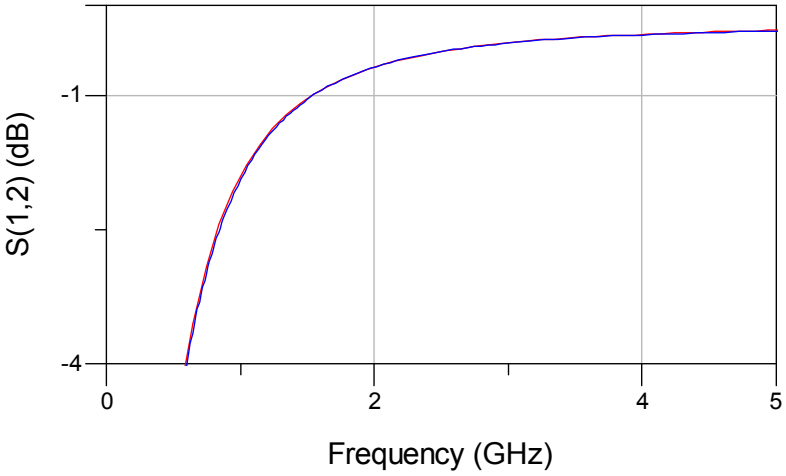


Figure 4.32: The complete seven-element model (a) and the simplified four-element model (b).

Simplification for the circuit is performed to make the model easier. As described in Chapter 3.5, pads are already de-embedded from the S-parameter; L_{pad} and C_{pad} can be removed to simplify the model. Moreover, due to the length of interconnect between capacitor and pads are short, the inductance can also be ignored. Finally, a four-element model is shown in Figure 4.32(b).



(a)



(b)

Figure 4.33: Simulated (blue) and modelled (red) S-parameters of a 0.16 μm^2 conventional MIM capacitor.

ADS is used to optimize and followed by tuning. The results of this optimization are shown in Figure 4.33 which indicate very good agreement between simulated and modelled S-parameters.

4.2.2 Q Factor and cut-off frequency of the multilayer MIM capacitors

Q factor compares the frequency at which a system oscillates to the rate at which it dissipates its energy. A higher *Q* indicates a lower rate of energy dissipation relative to the oscillation frequency. It is defined as

$$Q = \frac{Power \quad stored}{Power \quad dissipated} \tag{4.13}$$

At high frequency, the equation above can be written as:

$$Q = \frac{\frac{1}{j\omega C}}{R} \tag{4.14}$$

In our study, Equation 4.14 is used to calculate Q factor from the measured or simulated S-parameters.

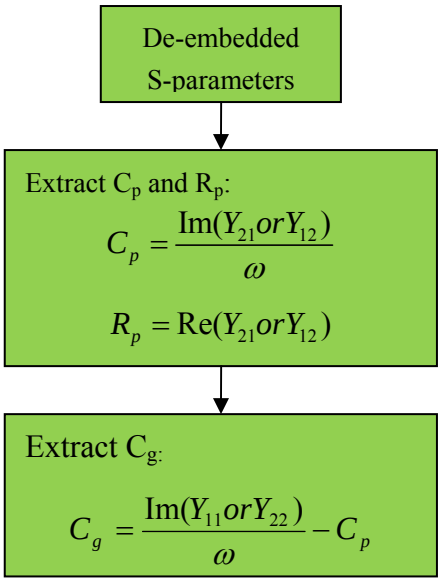


Figure 4.34: Flow diagram of parameters extraction scheme for the MIM capacitor according to the four-element modeling.

In order to see parasitics of the multilayer MIM designs, we employ schematic optimizations in ADS to get the modeled S-parameters match with the measured ones. As R_s is fairly small comparing with R_p, it is assumed to be zero in the extraction scheme (Figure 4.34). C_g, C_p and R_p are pre-estimated using equations in the scheme. S-parameter curves' fitting is then carried out to extract R_s, C_g and C_p.

High Q factor is desirable for capacitors working at RF, although it is usually poor and reduces to zero at about self-resonance frequency (Figure 4.35). This is mainly due to the resistive losses in the plates and interconnects. Also, the parasitic capacitance to the ground is another factor that degrades Q factor. We can see a relatively good match of Q factor between simulated and measured results at 2-4GHz, which is the frequency range that the capacitor works.

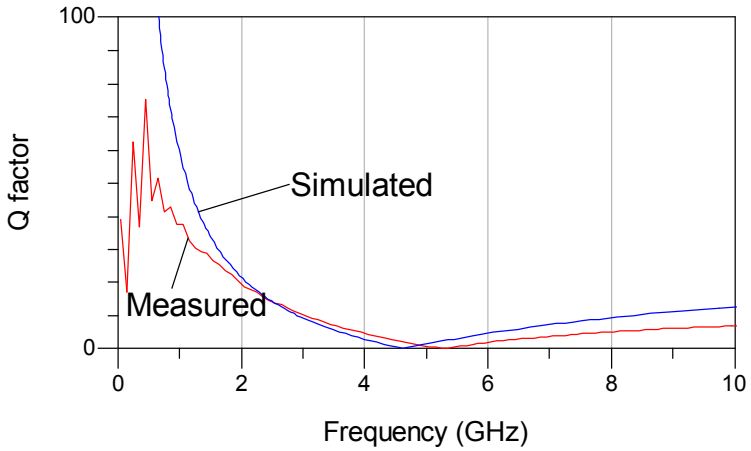


Figure 4.35: Measured and simulated Q factor of a 0.16 μm^2 conventional MIM capacitor.

In order to study the difference between the measured and simulated Q factor of conventional and folded designs with different sizes, in Figure 4.36 we capture the Q factor of various designs at 2GHz, at which the Q factor value is good enough to be compared (neither too small nor too large).

The data in Figure 4.36 indicate that the measured Q factors of conventional designs are smaller than those of simulated. The reason could be explained by examining the data give in Figure 4.37. It is clear that the resistance loss and parasitic capacitance are the two main reasons that degrade Q factor at high frequency. As shown in Figure 4.37 the extracted series resistance (R_s) and capacitance to the ground (C_g) from measurements are both higher than the simulated ones and this results in obtaining a lower Q factor as compared to simulated data. On the other hand, larger difference in the Q can be seen for small area capacitors (Figure 4.37) for the measured and simulated data. This is most likely due to the fact that small dimensions will result in larger fractional variations from the measured data.

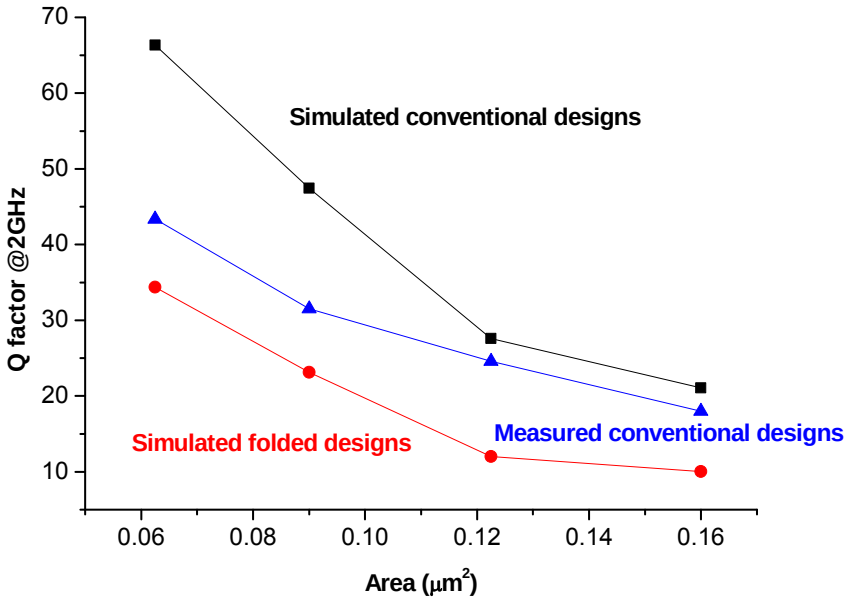


Figure 4.36: Simulated and measured Q factors of two capacitors designs with their sizes.

In Figure 4.36, we can also see that the folded designs have smaller Q factor than the conventional ones for the same area. This can be explained since there is an increase of capacitance density and multiple metal plates in the folded capacitor. From Equation 4.14, it is seen that these will result in the degradation of Q factor.

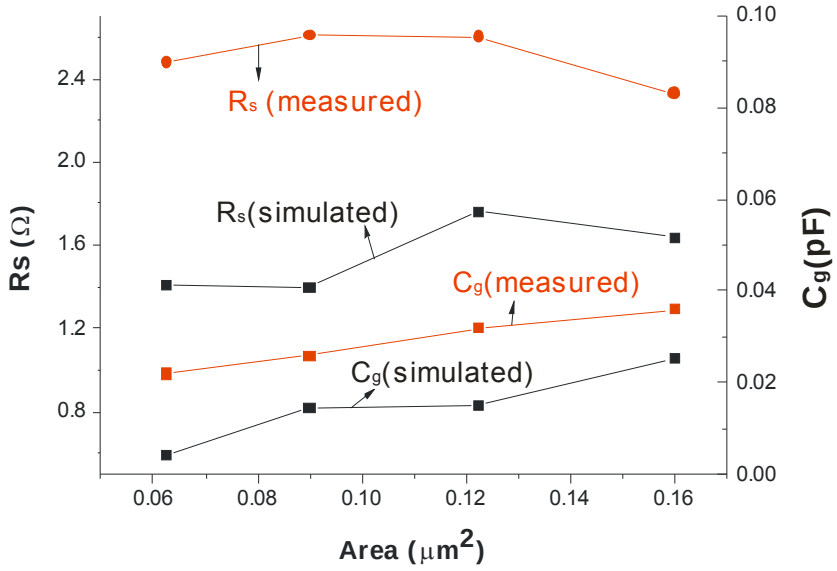


Figure 4.37: Extracted R_s and C_g versus area from measurement and simulation of conventional capacitors.

From the discussion in the beginning of this section, we note that the parasitic capacitance to the ground is also a factor that causes the Q factor to degrade. In order to know how this influences on capacitor and also to achieve design rules, we vary the distance between centre conductor and the ground metal in five values (15 µm, 20 µm, 28 µm, 36 µm and 44 µm) while keeping the other parameters unchanged. As Figure 4.38 shows, the capacitance to the ground decreases as the gap is widened. The figure indicates a gap value around 30 µm would be good choice between good performance and compactness. It is also interesting that we found out that Q values stay constant as the gap distance increases. Therefore, it can be generally concluded that in the multilayer capacitor designs studied, capacitance to the ground does not play a major role in Q factor degradations.

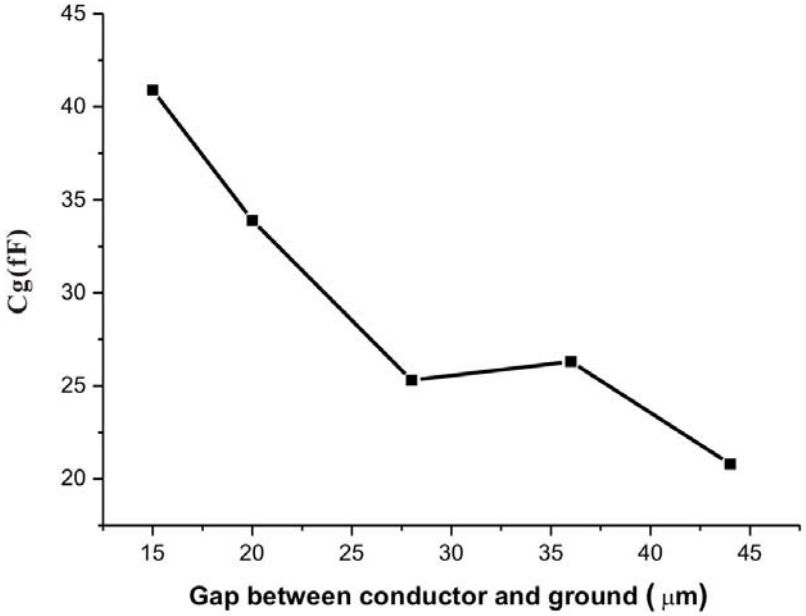


Figure 4.38: Capacitance to the ground with various gap distances between centre and ground conductor for the conventional capacitor design.

Another important parameter in RF capacitor is the cut-off frequency. This is defined as the frequency where the circuits turn from capacitive to inductive. Phase of simulated and measured Z_s of a 0.16 μm^2 conventional MIM capacitor is plotted in Figure 4.39. Z_s is defined as the complex impedance:

$$Z_s = Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{21}S_{12}}{2S_{21}} \tag{4.15}$$

In Figure 4.39, it is shown that the measured cut-off frequency of a conventional MIM capacitor is about 5.2 GHz.

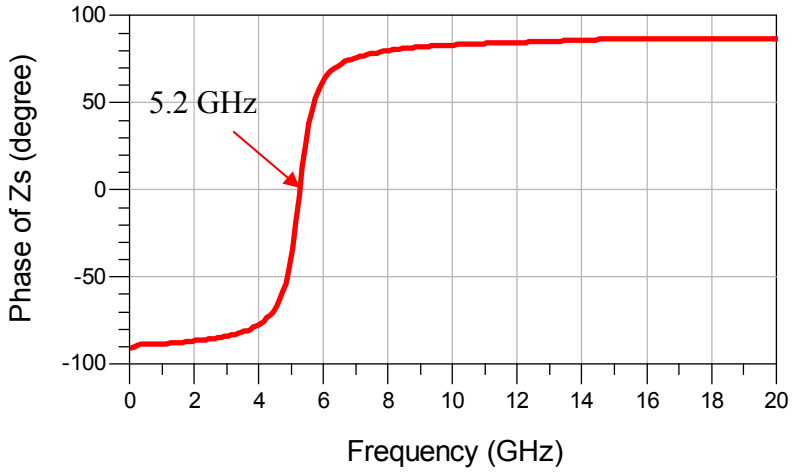


Figure 4.39: Measured phase of Z_s of a 0.16 μm^2 conventional MIM capacitor.

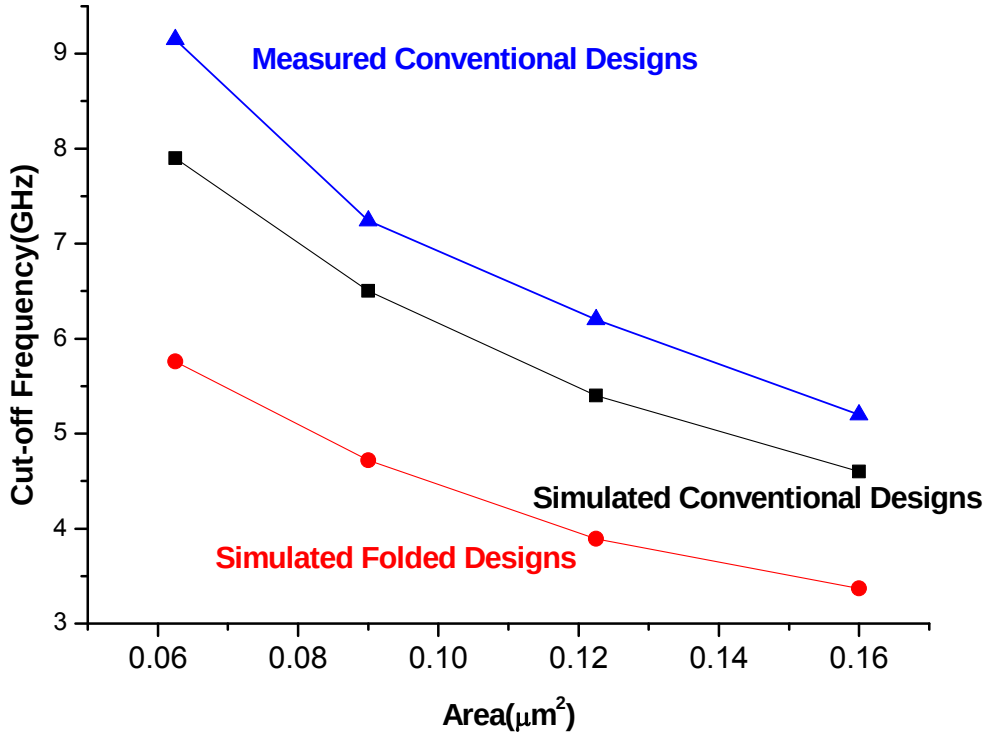


Figure 4.40: Simulated and measured cut-off frequency versus capacitor area for two MIM capacitor designs.

Figure 4.40 depicts the plots of cut-off frequency from simulated and measured results of two designs. We can see that cut-off frequency of measurement data is higher than

the simulated ones. The reason for this is that the measured functional capacitances (or global capacitance) are smaller than the simulated ones (Figure 4.41). Also due to higher capacitance in the folded structure, lower cut-off frequency can be expected (Figure 4.40).

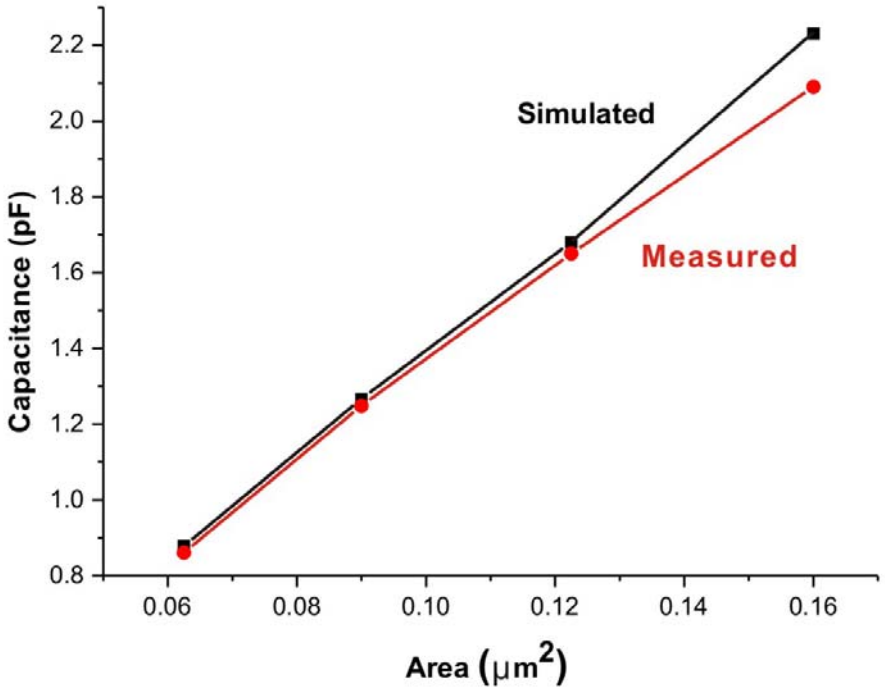


Figure 4.41: Comparison of simulated and measured capacitance of conventional designs.

In order to investigate how the shape of the capacitors has impact on their performances, four capacitors with same area (0.16 μm^2) but with different shapes (square and rectangular) are simulated and their extracted parameters are displayed in Table 4.5.

From this data it can be seen that different capacitor shapes (square or rectangular) have very similar parameters, although there is a slight variation on R_s (series resistance). This result indicates allows the designers to have full flexibility in integrating capacitors of the same quality with different shapes.

Dimension (μm)	Cut-off frequency(GHz)	Q factor	Capacitance (pF)	Rs (Ω)
400 x 400	4.6	21.1	2.23	1.64
350 x 458	4.6	23.1	2.22	1.56
300 x 534	4.6	21.1	2.21	1.63
250 x 640	4.6	21.3	2.22	1.58

Table 4.5: Extracted parameters for multilayer capacitors with various dimensions.

4.2.3 Optimization of multilayer capacitors – the effects of metal and dielectric layer thickness

The conventional CPW multilayer capacitor studied above has two 0.8 μm gold layers, sandwiched by a 2.5 μm polyimide layer fabricated on the 600 μm S.I. GaAs substrate.

In this work, 400 x 400 μm^2 capacitors with various metal thicknesses and various dielectric thicknesses are simulated. The results are shown in Tables 4.6 and 4.7.

Metal thickness (μm)	0.8	1.2	1.6
C_p (pF)	2.23	2.23	2.23
C_g (fF)	25	32	32
R_s (Ω)	1.64	1.07	0.53
Q (@2GHz)	21	50	64
Cut-off (GHz)	4.6	4.7	4.7

Table 4.6: Parameter extracted for conventional 400 x 400 μm^2 capacitors with various metal thicknesses and fixed polyimide thickness (2.5 μm) from simulated S-parameters.

Polyimide thickness (μm)	2.5	3.0	3.5	4.0
C_p (pF)	2.23	1.88	1.60	1.41
C_g (fF)	25	24	18	17
R_s (Ω)	1.64	1.55	1.44	1.43
Q (@2GHz)	21	30	36	44
Cut-off (GHz)	4.6	5.1	5.5	6.0

Table 4.7: Parameter extracted for conventional 400 x 400 μm^2 capacitors with various polyimide thicknesses and fixed metal thickness (0.8 μm) from simulated S-parameters.

In Table 4.6, one can also note that Q factor see a major increase when the metal thickness increases from 0.8 to 1.2 μm , as one would expect series resistance reduced significantly by the increase in the metal thickness (Table 4.6). This is because 0.8 μm is approximately calculated as the skin depth thickness at the operating frequency. The skin depth effect is well solved when the metal thickness is about 1.2 μm. Moreover, when the thickness increases to 1.6 μm, Q factor only slightly improved.

From the R_s and C_g values in Table 4.7, we find that both the two parameters decrease with the increase of polyimide thickness. It is due to widen of space between metal layers, the E.M wave density has been reduced.

From the data given in the table of 4.6 and 4.7 it can be seen that the capacitance doesn't change with the metal thickness since the increase in metal thickness doesn't change the coupling between the metal plates. However, with the raise of polyimide thicknesses (Table 4.7), C_p decreases. This is because the coupling becomes weaker as the distance between the two metal plates increased. Figure 4.42 shows how C_p changes with the polyimide thickness.

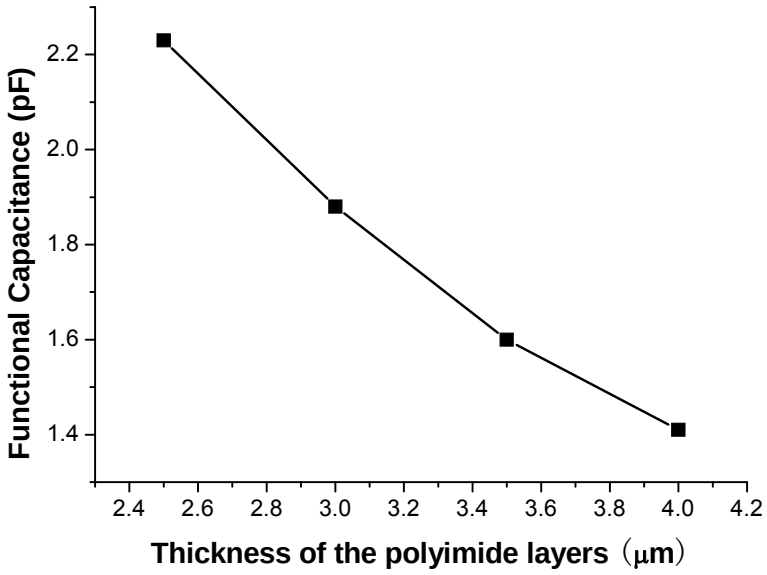


Figure 4.42: Extracted functional capacitance with various dielectric thicknesses for the conventional 400 x 400 μm^2 capacitors.

From the discussion above one can see that generally the capacitor tends to have better performance when the thickness of polyimide layer increases. For parameters such as C_g, R_s, Q and cut-off frequency, big advantages can be seen when using thicker polyimide layers. The only concern will be the value of functional capacitance.

4.2.4 Parallel multilayer capacitors

4.2.4.1 Two capacitors in parallel

The parallel structure of multilayer capacitor is realized by connecting two multilayer capacitors by a short interconnect in the middle (Figure 4.43). This structure is useful when designer intend to integrate a capacitor with large capacitance values.

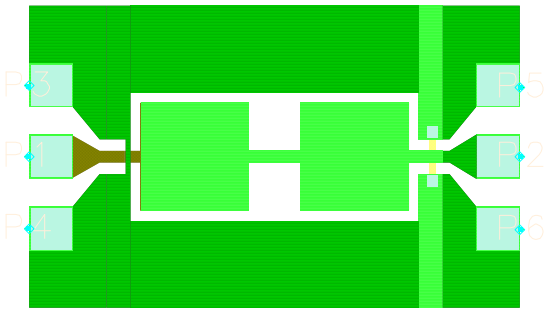


Figure 4.43: Layout of two paralleled multilayer capacitor.

Dimensions (µm)	Single 300 x 300 μm^2	parallel 300 x 300 μm^2 G=200 µm	parallel 300 x 300 μm^2 G=150 µm	parallel 300 x 300 μm^2 G=100 µm	parallel 300 x 300 μm^2 G=50 µm
C_p (pF)	1.25	2.53	2.53	2.53	2.53
C_g (fF)	11	16	19	24	28
R_s (Ω)	1.26	1.9	1.7	1.63	1.6
Q (@2GHz)	47	18	20	22	24
Cut-off (GHz)	6.5	3.7	3.8	3.9	4.1

Table 4.8: Simulation of capacitors' parameters from the single and parallel 300 x 300 μm^2 multilayer capacitors.

Dimensions	single 400 x 400 μm^2	parallel 400 x 400 μm^2 G=200 µm	parallel 400 x 400 μm^2 G=150 µm	parallel 400 x 400 μm^2 G=100 µm	parallel 400 x 400 μm^2 G=50 µm
C_p (pF)	2.23	4.45	4.45	4.45	4.45
C_g (fF)	25	25	44	48	52
R_s (Ω)	1.28	1.84	1.64	1.6	1.6
Q (@2GHz)	21	7	7	8	8
Cut-off (GHz)	4.6	2.9	2.9	2.9	3.0

Table 4.9: Simulation of capacitors' parameters from the single and parallel 400 x 400 μm^2 multilayer capacitors.

In our ADS Momentum simulation, the new structure is implemented by using the same square size as conventional MIM capacitors used in previous designs. The length of short interconnect between the two capacitor is varied in order to study the effect of any parasitic capacitances which may be produced from metal distance. The simulation results are shown in Tables 4.8 and 4.9. From these data, the capacitance of all parallel capacitors is increased to twice as the single one. This is reasonable as effective coupling area of the parallel ones are doubled when the two single capacitors are connected.

One of the important parameters in characterizing the performance of the multilayer CPW capacitor is the parasitic capacitance. It is known that with the decrease in the gap between the centre and the ground metals, capacitance to the ground will increase and thus degrades the performance of the capacitor. Figure 4.44 shows a graphical data taken from the extracted parasitic capacitance given in Table 4.8 with various gaps sizes between the two capacitors (from 50 µm to 200 µm). From this figure it can

be seen that the parasitic capacitance to the ground decreases linearly with the increase of gap distance.

The series resistance given in both Tables 4.8 and 4.9 indicates that the parallel capacitors have naturally high parasitic resistance due to the existence of the short interconnections. Meanwhile, we can also find that the series resistance decreases with the increase of gap distance between the two connected capacitors.

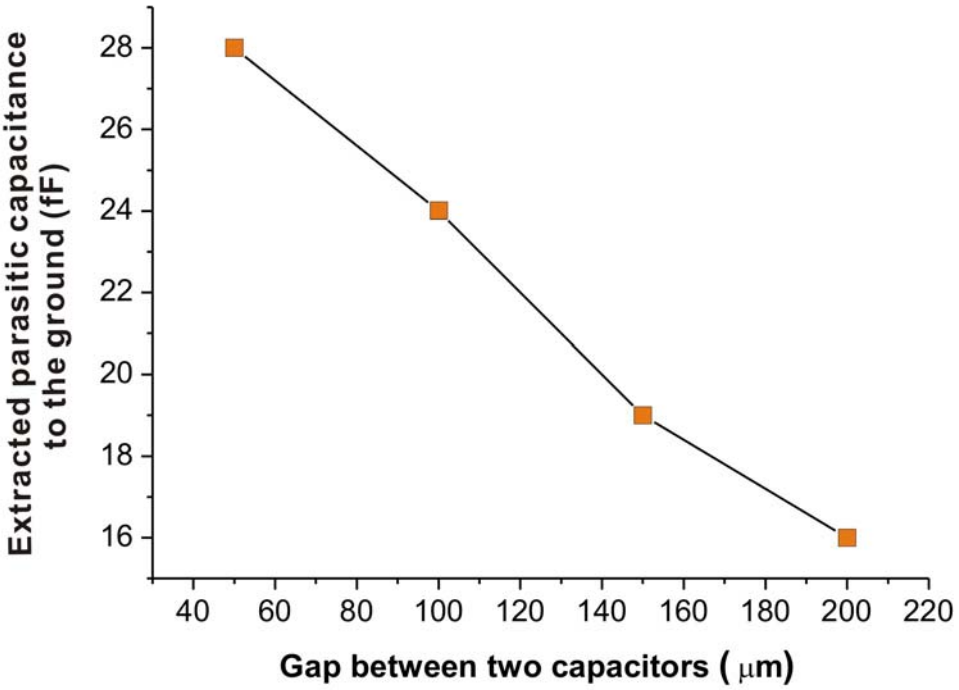
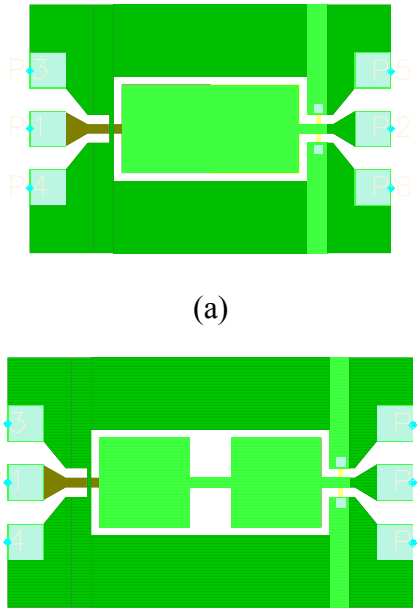


Figure 4.44: Extracted parasitic capacitance to the ground with various gap sizes between the two capacitors.

The data given in Table 4.8 and 4.9 also show that the Q factor and cut-off frequency behaviour are becoming poorer than the single capacitors. This is mainly because parallel capacitors have higher functional capacitance resulting in lower Q factor and cut-off frequency. Decreasing the gap size from 200 μm to 50 μm will help to enhance the behaviour of the capacitor slightly.

In order to study the differences between the single and parallel capacitors, we simulate a single conventional capacitor having a dimension of 300 x 600 μm^2 and a parallel 300 x 300 μm^2 capacitor with the gap of 50 µm (Figure 4.45). These two structures have the same effective area of 0.18 mm^2.



(a)

(b)

Figure 4.45: The layout of conventional (a) and parallel (b) capacitors with the same effective coupling area of 300 x 600 μm^2.

Dimensions	Parallel capacitor 300 x 300 μm^2 Gap = 50 µm	Conventional capacitor 300 x 600 μm^2
C_p (pF)	2.53	2.42
C_g (fF)	28	32
R_s (Ω)	1.26	1.00
Q (@2GHz)	24	27
Cut-off (GHz)	4.1	4.3

Table 4.10: Comparison between parallel and conventional capacitors with the same effective coupling area of 300 x 600 μm^2.

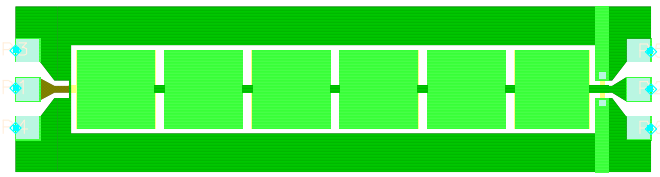
As seen in Table 4.10, the parallel capacitor has slightly better performance in the C_p value and C_g. As already shown in previous simulation (see Figure 4.44), the capacitance to the ground generally increases with the reduction of gap distance. Thus, one would expect that the 300 x 600 μm^2 conventional design will have a higher parasitic capacitance comparing with the parallel one. On the other side, both Q factor and cut-off frequency are higher in the conventional design.

4.2.4.2 Multi-capacitors in parallel

From theoretical consideration of capacitors it can be noted that for realizing large capacitance capacitor in lumped element, it is necessary to make the dimension smaller than 1/10 of a wavelength at the maximum frequency of its usage. For obtaining large capacitors it is useful to investigate parallel structure designs see if there are advantages.

The following four conventional designs are simulated: 400 x 1800 μm^2, 400 x 2400 μm^2, 400 x 3000 μm^2 and 400 x 3600 μm^2. Another set of parallel structures (Figure 4.46), but with the same total coupling area, are also considered. These two sets could be compared as the expected functional capacitances (C_p in Figure 4.32) are equal in effective coupling area. R_s, C_g are extracted from the modelling. The results are shown in Table 4.11.

(a)



(b)

Figure 4.46: Layouts of conventional (a) and parallel (b) capacitors with same effective coupling area.

Designs (μm^2)	C_p (pF)	C_g (pF)	R_s (Ω)
Conventional 1800 x 400	9.7	0.11	1.9
Parallel 2000 x 400	10.1	0.07	2.4
Conventional 2400 x 400	12.5	0.16	1.7
Parallel 2630 x 400	13.0	0.11	2.6
Conventional 3000 x 400	15.8	0.20	1.7
Parallel 3280 x 400	16.5	0.13	2.6
Conventional 3600 x 400	19.4	0.24	1.7
Parallel 3950 x 400	19.9	0.15	2.9

Table 4.11: Extracted parameters from simulation of various designs of capacitors.

Along with the previous simulated conventional CPW capacitors (Chapter 4.2.1), we plot capacitance values achieved as a function of the effective coupling area (Figure 4.47). The plot shows that capacitance reasonably linear with the coupling area, which indicated in the following function:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \qquad (4.16)$$

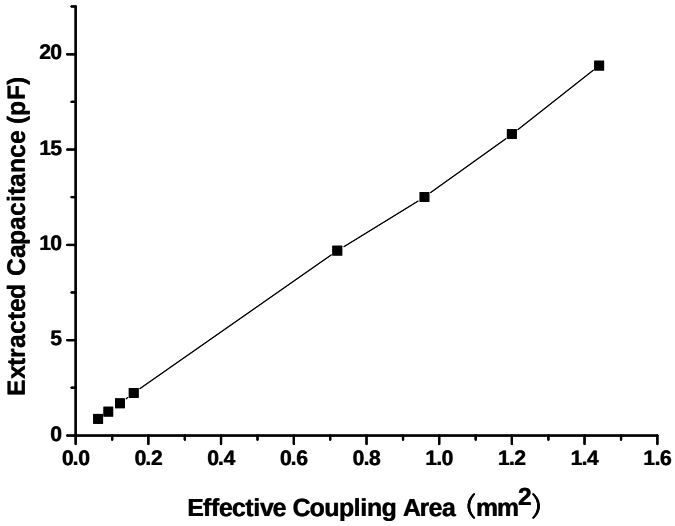
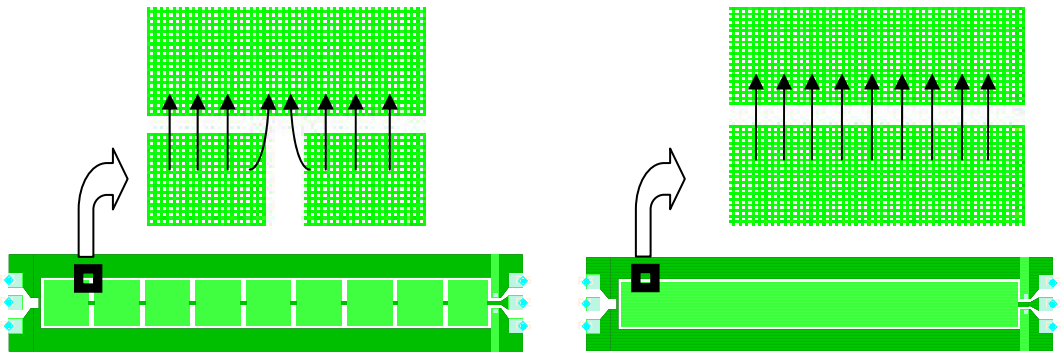


Figure 4.47: Extracted capacitance in the function of effective coupling area of the capacitors.



(a) (b)

Figure 4.48: Field distribution for the parallel (a) and conventional (b) multilayer capacitors.

It is depicted in Table 4.11 that C_g for the parallel designs are smaller than those from the conventional designs. The reason for this is shown in Figure 4.48. From parallel designs, one can see that there are discontinuities at the connection of square metal plates. These discontinuities will naturally result in low current distribution, thus will cause low electric field density. Therefore, the fringing capacitance (C_g) is lower comparing with the conventional structures. Generally, C_g also increases with the rise

of total dimension of the capacitor. Figure 4.49 illustrates the value of extracted parasitic capacitor (C_g) as a function of total coupling length of the parasitic capacitor. We approximate the total coupling length as double value of the metal plate length: 3600µm, 4800µm, 6000µm and 7200µm.

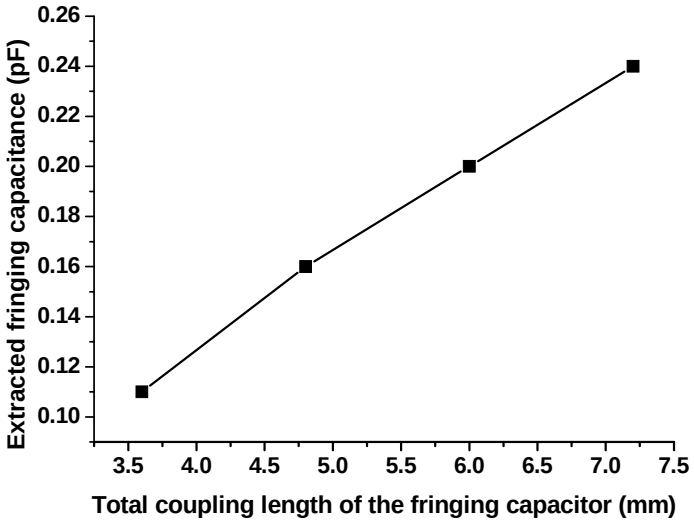


Figure 4.49: Extracted fringing capacitance (C_g) with total coupling length.

From Table 4.11, one can also note that the equivalent series resistance (R_s) is increased when parallel structures are applied. This is because the current flows more smoothly in the single metal plate than those with connections. Those short interconnects will lead to high current density, thus result in high resistive loss in those areas. With conventional designs, R_s is not sensitive with the dimensions. On the other hand, R_s from parallel designs climb as the total dimension rises. This can be explained by more short interconnects introduced for large dimension designs. An optimisation of suitable width of the short interconnect is needed.

As these high capacitance designs have really low cut-off frequency, Q factors are sampled at 500 MHz (Table 4.12). One can note from these data that with a similar functional capacitance, Q factor is much lower than the conventional ones. This could be the dominance of equivalent series resistance (R_s) value in Q factor behaviour.

Figure 4.49 shows how Q factors degrade with achieved total capacitance at various frequencies (0.5 GHz, 1 GHz, 1.5 GHz and 2 GHz). If we transform Equation 4.16 to the following:

$$Q = \frac{1}{j\omega CR} \tag{4.17}$$

In which, C is the total capacitance and R is the equivalent series resistance (ESR).

Designs (μm^2)	C_p (pF)	Q factor (@500MHz)
Conventional 1800 x 400	9.7	25.2
Parallel 2000 x 400	10.1	17.5
Conventional 2400 x 400	12.5	19.5
Parallel 2630 x 400	13.0	10
Conventional 3000 x 400	15.8	13
Parallel 3280 x 400	16.5	8.4
Conventional 3600 x 400	19.4	8.7
Parallel 3950 x 400	19.9	3.9

Table 4.12: Functional capacitance and Q factor of various conventional and parallel capacitor designs.

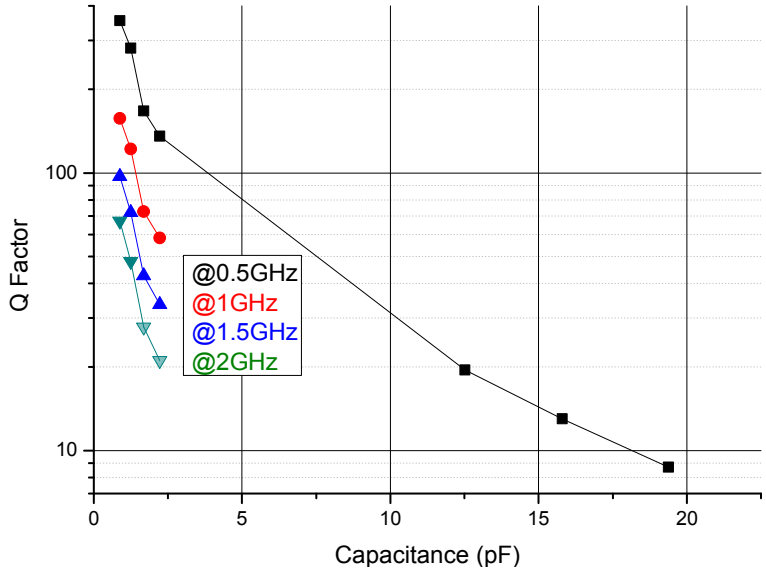


Figure 4.50: Q factors of conventional capacitor designs versus capacitance magnitude at various frequencies.

4.3 CPW multilayer switches

4.3.1 pHEMT modelling

AlGaAs/InGaAs/GaAs pHEMT manufactured by Filtronic is applied in these CPW multilayer switches. The cross-sectional view of the pHEMT is shown in Figure 4.51.

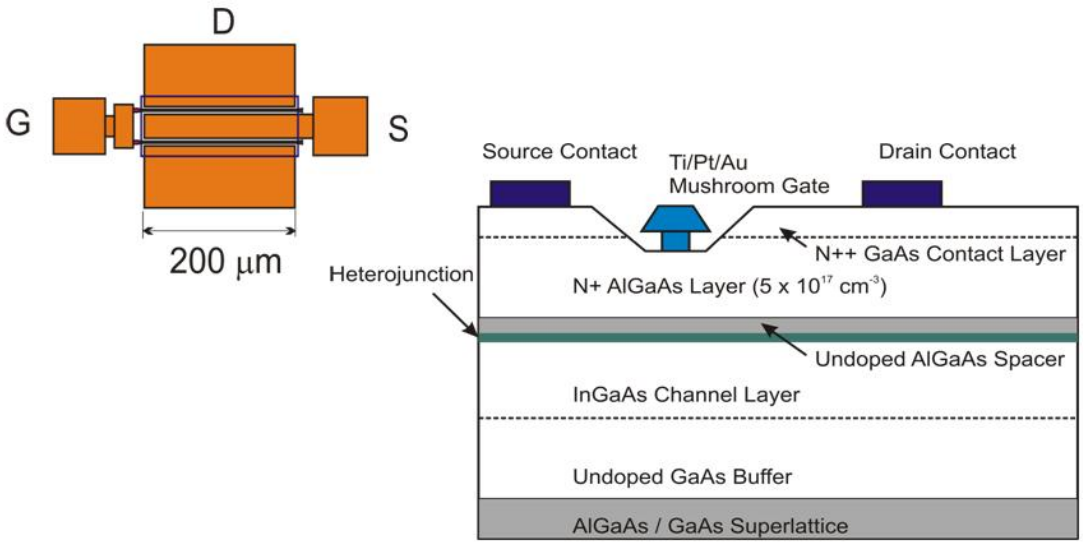
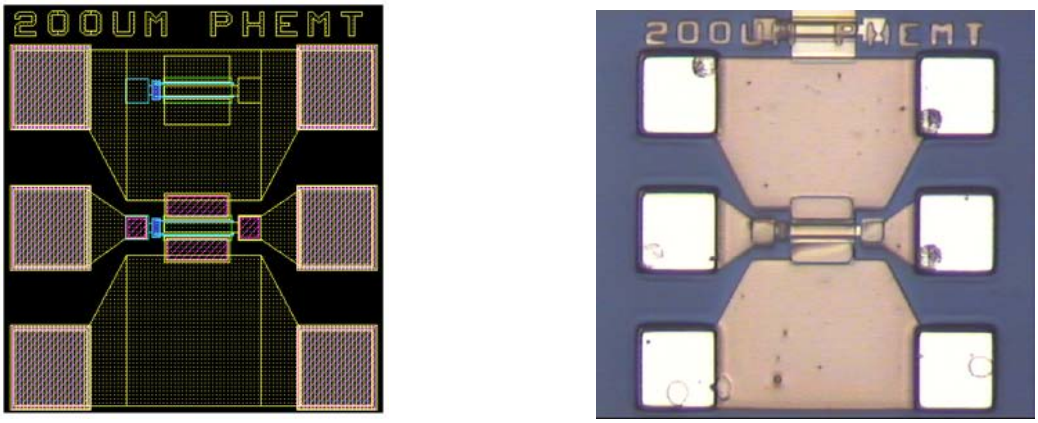


Figure 4.51: Top and cross-sectional views of the pHEMT structure.



(a) (b)

Figure 4.52: Layout design (a) and the fabricated micrograph (b) of the multilayer 0.5 x 200 μm^2 pHEMT.

The pHEMT shown in Figure 4.52 has a gate finger length of 0.5μm and two gate width of dimension 2 x 100μm^2. It is fabricated on a 0.6mm thick semi-insulating GaAs substrate. These devices are fabricated on the wafer where there are other uncommitted pHEMTs were present (see Figure 4.53). So only some of the pHEMTs were chosen for the multilayer MMICs. In Figure 4.52b one can see two pHEMTs: a pre-fabricated device which is not being used (with no bonding pads) while the lower device has the bonding pads fabricated during the multilayer process.

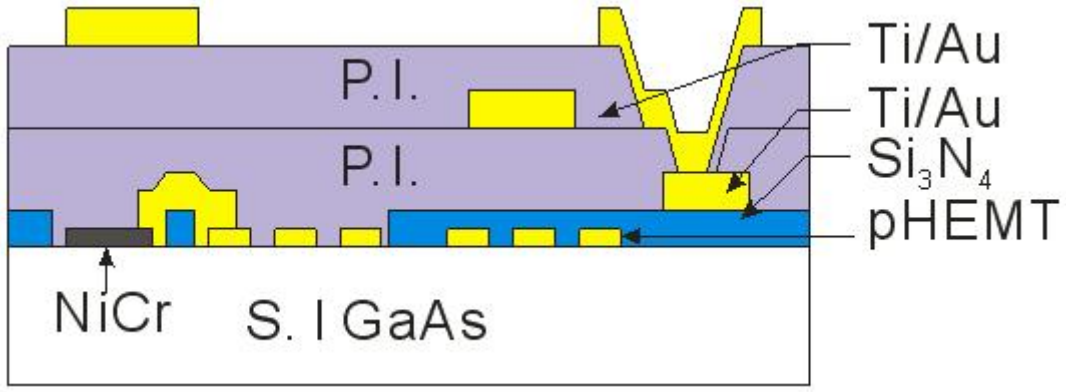


Figure 4.53: Cross-sectional view of MMIC showing the location of pHEMTs.

In switch applications, the pHEMT can be either in On-state or Off-state. During On-state, the drain-source channel is opened by reducing the depletion region, while for Off-state; the channel is completely shut down. The drain is not biased in the low V_{ds} region as Figure 4.54 shows. When the gate voltage, V_{gs} is greater than 0.6 V, the drain to source current, I_{ds} changes with V_{ds} in the low V_{ds} region, which means the drain-to-source channel is open. It is also obvious that I_{ds} changes linearly with V_{ds} at low value of V_{ds} so the pHEMT acts as a small value resistor when it's at On-state. When V_{gs} lower than -1.4 V, Ids is about zero around low V_{ds} region, which means pinched off (used as Off-state).

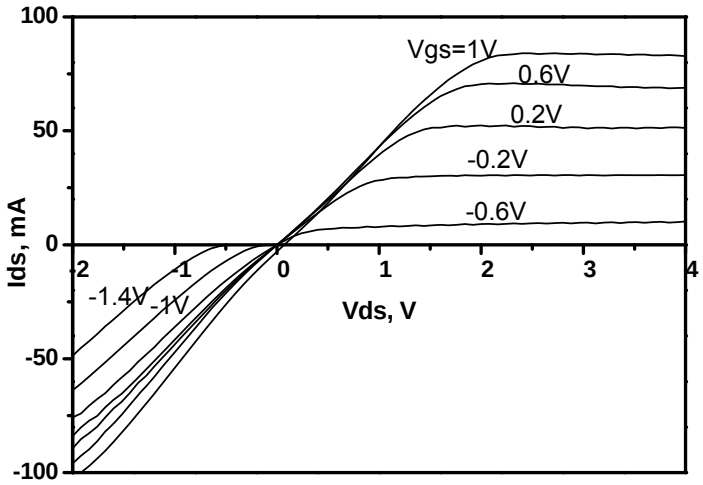


Figure 4.54: DC output characteristic of a pHEMT.

Therefore, in the switch designs, considered in this work, the pHEMT is modelled as On-state when V_{gs} is 0.6 V. As mentioned above, the pHEMT acts as a resistor at On-state, R_{on}. For Off-state, V_{gs} should be lower than -1.4 V. At this time, the depletion region under the gate finger shuts down the drain-to-source channel. Thus the pHEMT can be modelled as a capacitor, C_{off} with its series resistor R_{off}, as shown in Figure 4.55 [137].

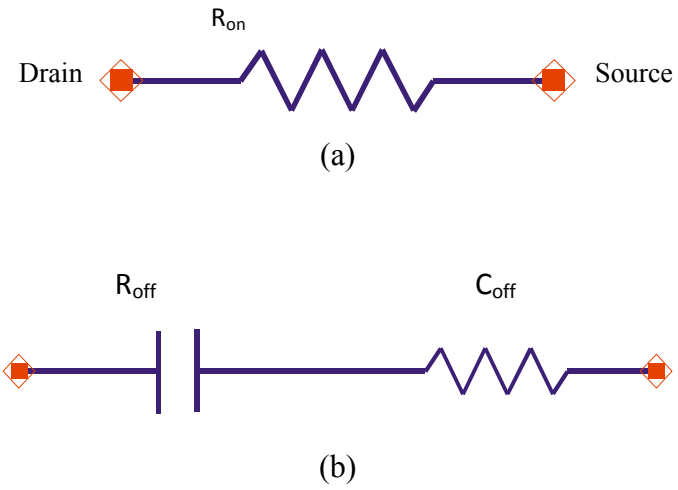


Figure 4.55: Small signal equivalent model for On (a) and Off (b) states of pHEMT.

In order to achieve accurate modelling, the parameters R_{on}, R_{off} and C_{off} are extracted from measured S-parameters of the pHEMT.

The on-state resistance, R_{on} is defined as the dynamic resistance ie the ratio of the drain-to-source voltage, V_{ds} and the channel current, I_{ds} when V_{ds} is at small signal mode and can be expressed as:

$$R_{on} = \frac{\Delta V_{ds}}{\Delta I_{ds}} | V_{ds} \approx 0 \qquad (4.18)$$

Thus R_{on} can be easily deduced from the pHEMT DC output characteristic. Figure 4.56 shows the I_{ds} as a function of V_{ds} where the gate voltage, V_{gs} is set to 0.6 V to leave the channel wide open. The slope is then used to represent R_{on} and the calculated result is approximately 20 Ω.

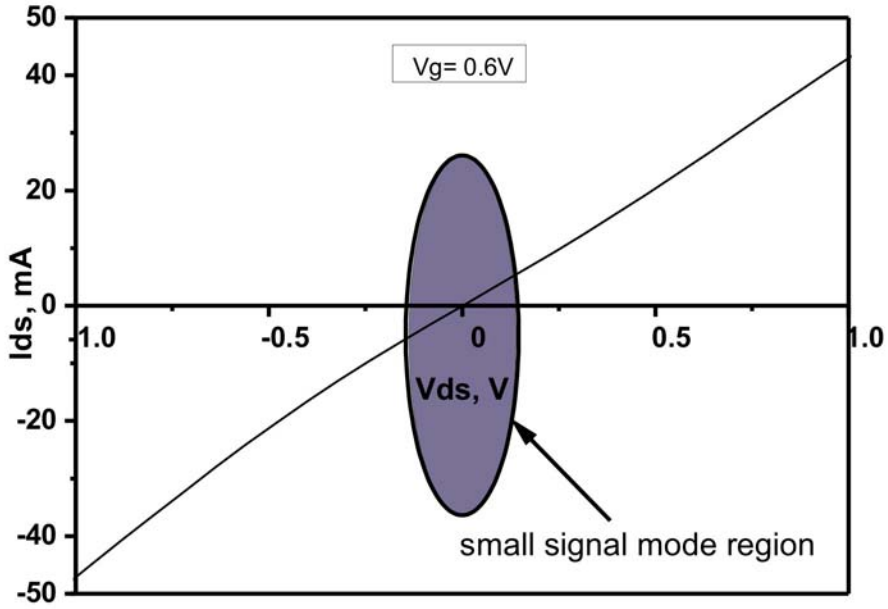


Figure 4.56: pHEMT DC output characteristic.

A π equivalent circuit model biased in common source configuration is adopted as the small-signal model for the pHEMT and shown in Figure 4.57. The equivalent circuit can be categorised as the intrinsic and the extrinsic parts [138]. The intrinsic elements are intrinsic transconductance, g_m, output resistance, g_d (R_{ds}), gate-source capacitance, C_{gs}, gate-drain capacitance, C_{gd}, drain-source capacitance, C_{ds}, input resistance, R_i and signal delay, τ are bias dependent elements. The extrinsic elements are gate parasitic inductance L_g, gate parasitic resistance, R_g, gate parasitic capacitance, C_{pg}, source parasitic inductance L_s, source parasitic resistance, R_s, drain parasitic resistance, R_d, drain parasitic capacitance C_{pd} and drain parasitic inductance, L_d is independent of the biasing.

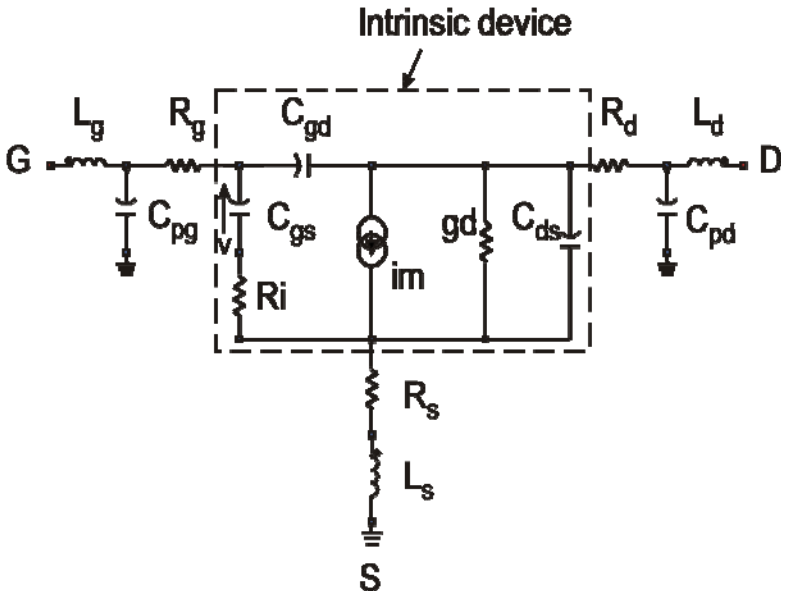


Figure 4.57: The small signal equivalent circuit of a field effect transistor in common source configuration.

When the pHEMT is under the strong pinch off bias condition ie V_{ds} = 0V and V_g lower than pinch off voltage, its equivalent circuit is represented in Figure 4.58. The intrinsic parameters are simplified to the fringing capacitance, C_b, which is due to the depletion region extension at each side of the gate. C_{pg} is mainly the capacitance between gate probing pad and ground; C_{pd} represents the drain probing pad to ground

capacitance together with capacitance between the drain and source metal contact; R_g and L_g, R_d and L_d, R_s and L_s are the parasitic resistance and inductance at gate, drain and source respectively.

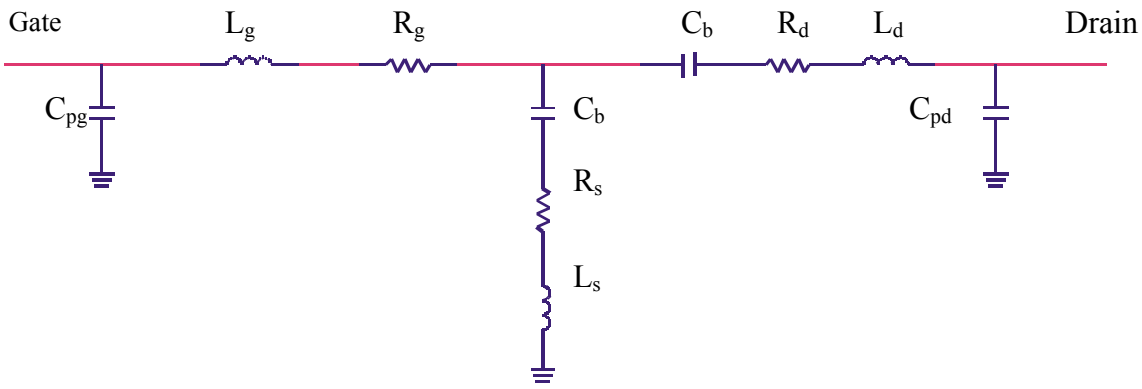


Figure 4.58 Small-signal equivalent circuit of a pHEMT at strong pinch-off mode ie V_{ds} = 0V and gate voltage lower than the pinch off voltage.

Two different operating conditions are needed to extract the extrinsic parameter shown in Figure 4.58, which are off (V_{ds} = 0 and V_g = 0) and strong pinch off (V_{ds} = 0 and V_g much lower than pinch off voltage V_{po}) bias condition. The flow chart in Figure 4.59 indicates the steps to be followed to extract the corresponding extrinsic parameters.

To extract the extrinsic parasitic inductances and resistances, S-parameters measurements are firstly carried out at off state with V_{ds} = 0 and V_g = 0 using on-wafer measurement. The measured S-parameters, [S] are then converted to Z-parameters, [Z]. The expressions for the Z-parameters at off state are given as [138]:

$$Z_{11} = R_s + R_g + 0.33R_{ch} + j\omega(L_s + L_g) \tag{4.19}$$

$$Z_{12} = Z_{21} = R_S + 0.5R_{ch} + j\omega L_s \tag{4.20}$$

$$Z_{22} = R_d + R_S + R_{ch} + j\omega(L_S + L_d) \quad (4.21)$$

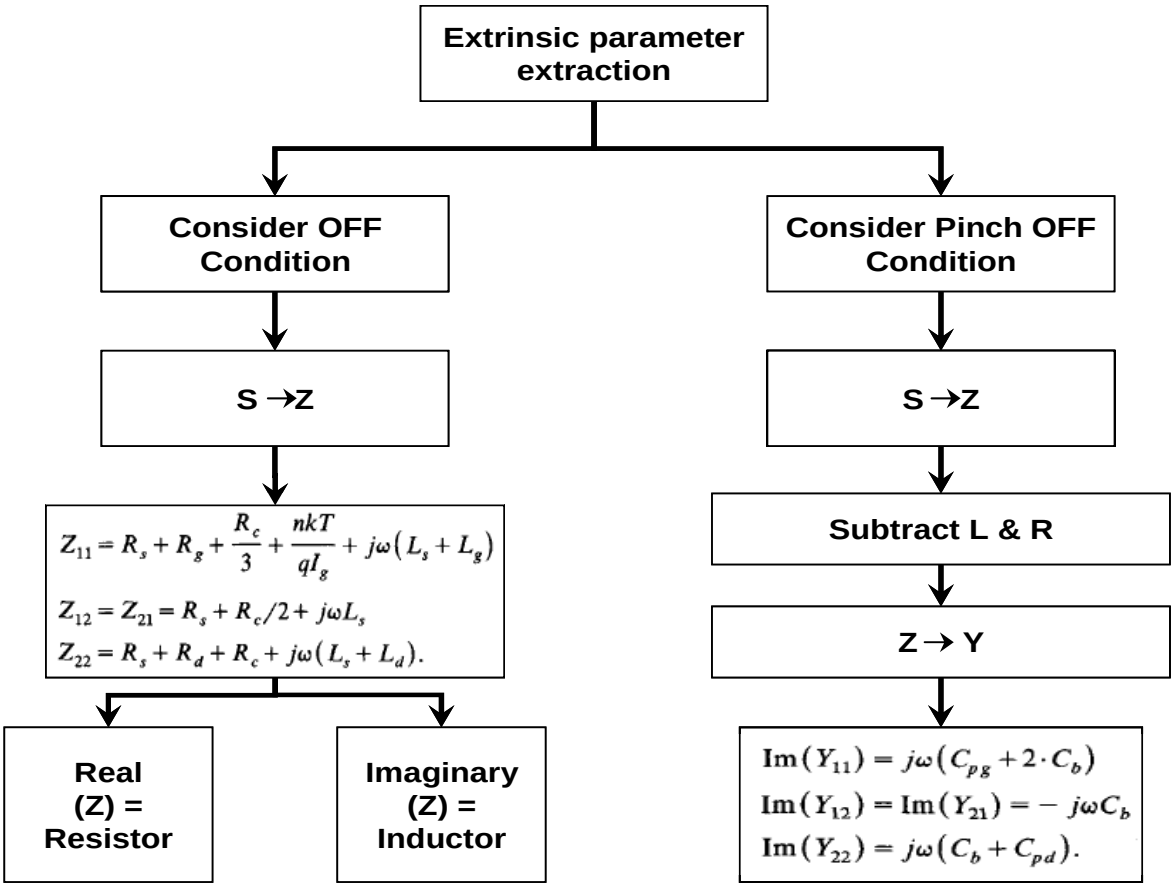


Figure 4.59: The flow chart of extracted extrinsic parameters of the pHEMT.

Where R_{ch} is the channel resistance under the gate when $V_g = 0$ V and $V_{ds} = 0$ V [138]. As we can see, the parasitic inductances L_s, L_d and L_g can be computed by using the imaginary parts of Equations (4.19), (4.20) and (4.21).

$$\mathrm{Im}(Z_{12}) = \mathrm{j}\omega L_s \Rightarrow L_s = \frac{\mathrm{Im}(Z_{12})}{\omega} \tag{4.22}$$

$$\mathrm{Im}(Z_{22}) = \mathrm{j}\omega(L_s + L_d) \Rightarrow L_d = \frac{\mathrm{Im}(Z_{22})}{\omega} - L_s \tag{4.23}$$

$$\mathrm{Im}(Z_{11}) = \mathrm{j}\omega(L_s + L_g) \Rightarrow L_g = \frac{\mathrm{Im}(Z_{11})}{\omega} - L_s \tag{4.24}$$

Similarly, the parasitic resistances R_s, R_d, R_g can be extracted from the real parts of Equations (4.19), (4.20) and (4.21). However, an additional expression is needed as there are four unknowns with only three equations. By biasing the pHEMT under strong pinch-off condition (V_{ds} = 0 and V_g much lower than pinch off voltage V_{po}) and measuring the S-parameters, then convert the measured S-parameters $[S]_{Vpo}$ to Z-parameters $[Z]_{Vpo}$, the fourth equation is given as [138]:

$$\mathrm{Re}[Z_{11(V_{po})}] = R_s + R_g \tag{4.25}$$

Thus, the parasitic resistances can be extracted using Equations (4.19), (4.20), (4.21) and (4.25):

$$\begin{aligned} &\mathrm{Re}[Z_{11(V_{po})}] = R_s + R_g \ \textit{and}\ \mathrm{Re}[Z_{11}] = R_s + R_g + 0.33R_{ch} \\ &\Rightarrow R_{ch} = 3 \times \left\{ \mathrm{Re}[Z_{11}] - \mathrm{Re}\left[Z_{11(V_{po})}\right] \right\} \end{aligned} \tag{4.26}$$

$$\mathrm{Re}[Z_{12}] = 0.5R_{ch} + R_s \Rightarrow R_s = \mathrm{Re}[Z_{12}] - 0.5R_{ch} \tag{4.27}$$

$$R_g = \mathrm{Re}[Z_{11}] - R_s - 0.33R_{ch} \tag{4.28}$$

$$R_d = \mathrm{Re}[Z_{22}] - R_s - R_{ch} \tag{4.29}$$

For the parasitic capacitances C_{pg}, C_{pd} and C_b, the measured S-parameters of pHEMT under strong pinch off condition are converted to the respective Z-parameters and then, according to the topology of the equivalent circuit model, the inductances and

the resistances computed in the previous section are subtracted to eliminate their effect:

$$Z_{11} - R_s - R_g - j\omega(L_s + L_g) \tag{4.30}$$

$$Z_{12} - R_s - j\omega L_s \text{ or } Z_{21} - R_s - j\omega L_s \tag{4.31}$$

$$Z_{22} - R_d - R_s - j\omega(L_s + L_g) \tag{4.32}$$

After the calculation, the resultant Z-parameters are transformed to the respective Y-parameters and can be expressed as:

$$Y_{11} = j\omega(2C_b + C_{pg}) \tag{4.33}$$

$$Y_{12} = Y_{21} = j\omega C_b \tag{4.34}$$

$$Y_{22} = j\omega(C_b + C_{pd}) \tag{4.35}$$

The capacitances can then be extracted using Equations (4.33), (4.34) and (4.35) as:

$$C_b = \frac{\mathrm{Im}(Y_{12})}{\omega} \tag{4.36}$$

$$C_{pg} = \frac{\mathrm{Im}(Y_{11})}{\omega} - 2C_b \tag{4.37}$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{22})}{\omega} - C_b \tag{4.38}$$

Use the above equations, the extrinsic parameters of a pHEMT can be calculated and the results are listed in Table 4.13.

Extrinsic small signal parameters	Values
C_{pg}, fF	44
L_g, pH	140
R_g, Ω	1.0
C_{pd}, fF	87
L_d, pH	72
R_d, Ω	9
L_s, pH	1.0
R_s, Ω	3
C_b, pF	0.11

Table 4.13: Extracted small signal model for the pHEMT at strong pinch off biasing condition.

The extracted small signal model of the pHEMT at strong pinch off biasing condition is then employed to characterise its off-state capacitance for switch application. Firstly the small signal model is modified to fit the pHEMT configuration in switch application by redefining the RF ports at drain and source instead of gate and drain. Secondly, because of the source is no longer configured as common ground and probing pads is removed in switch application, the gate parasitic capacitance, C_{pg} needs to be neglected since it represents the gate probing pad to ground (source) capacitance. Drain parasitic capacitance, C_{pd} also needs to be reduced by the value of C_{pg} for the similar reason since it represents not only the drain-to-source metal contact capacitance but also the drain probing pad to ground (source) capacitance. Finally the off-state capacitance, C_{off} and resistance, R_{off} of the pHEMT model for switch application in Figure 4.55b are deduced by optimizing the simulated S-parameters to fit the simulated results of the model in Figure 4.60. The matched S-parameters are

shown in Figure 4.61 and the optimized off-state capacitance C_{off} and resistance, R_{off} is 0.09 pF and 10 Ω respectively.

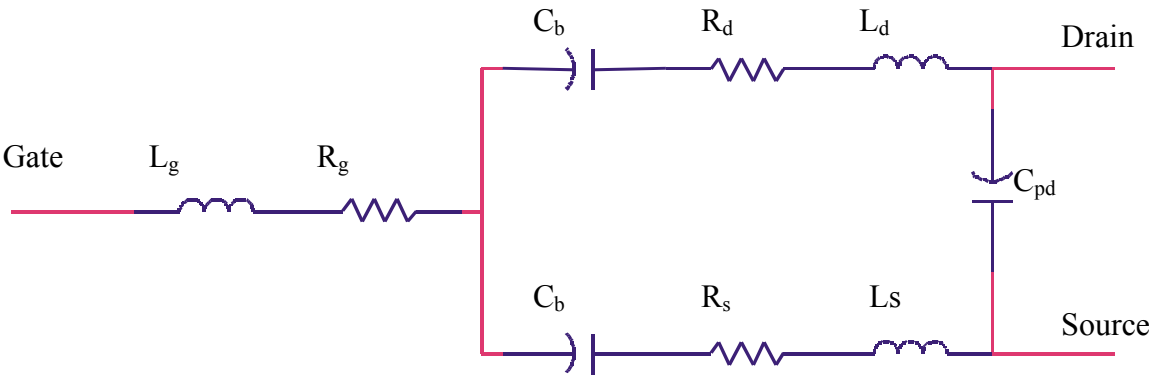


Figure 4.60: Modified equivalent circuit at strong pinch off gate voltage of the pHEMT without probing conductor for switch application.

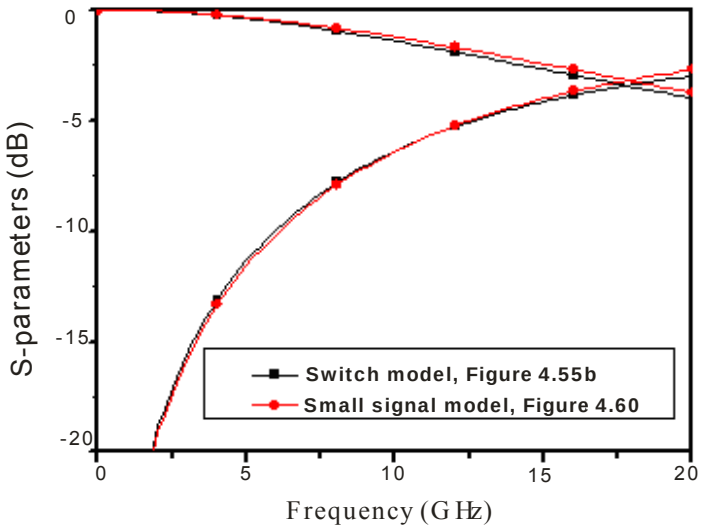


Figure 4.61: Procedure of using ADS optimising to extract C_{off} and R_{off}.

4.3.2 Shunted pHEMT switch designs

The shunt configuration has a better tolerance to high on-state resistance and is suitable to be used in a low loss switch design. Also, as no power flow through the

active devices when the branch is On, the power handling ability of the shunt configuration would be better [139]. For the shunted configuration (Figure 4.62), when the pHEMT is switched to on-state, where the drain-to-source channel is fully open, the pHEMT is ideally a short circuit conductor and the input impedance at port 1 of the switching branch is infinite. Thus the branch is shut down to OFF and no signals will pass through. On the other hand, when the pHEMT is switched to off-state, where the drain-to-source channel is completely shut down, ideally the pHEMT will have the impedance of infinity (open circuit). Hence the input impedance at port 1 of the branch is 50Ω and allows the signal to transmit through without any reflection. This state for the switching branch is then called the ON state.

As the On-state resistance is about 20Ω, one then try to use paralleled pHEMTs to reduce the total resistance of the On-state switch.

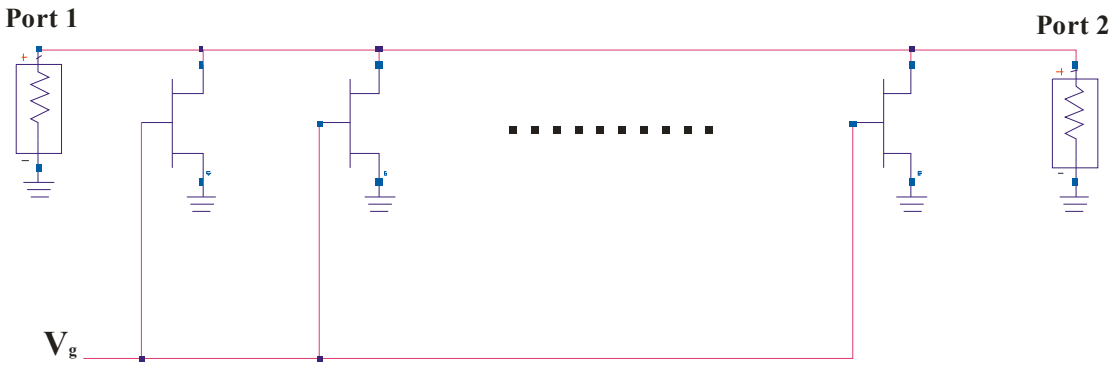
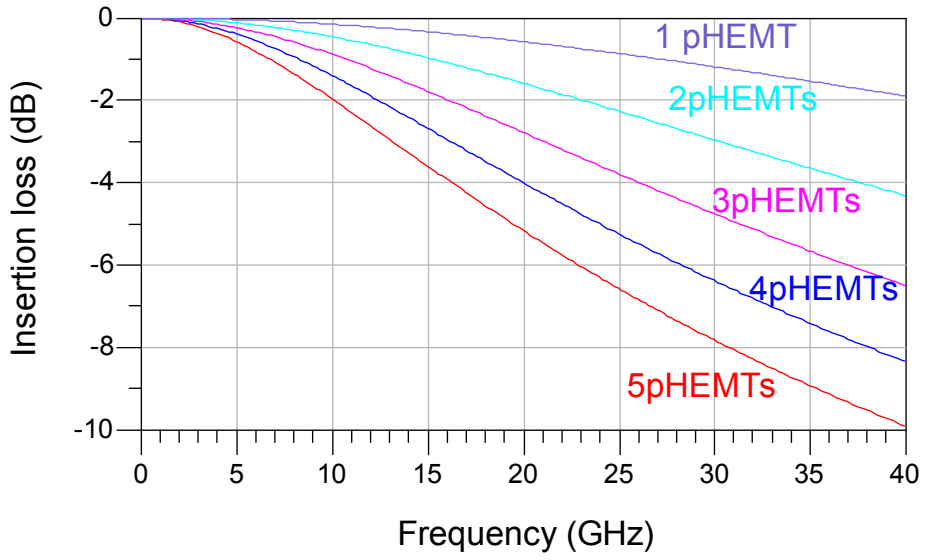
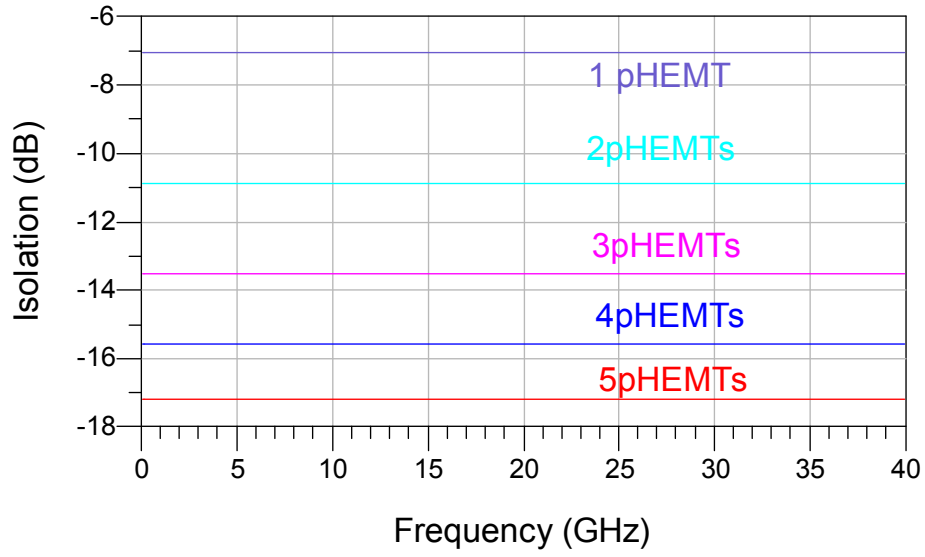


Figure 4.62: The basic configuration of shunted pHEMT switches.



(a)



(b)

Figure 4.63: Simulated insertion loss (a) and isolation (b) of the shunted configuration switches with various pHEMTs.

From Figure 4.63, one can note that when the number of pHEMTs increases, one can achieve better isolation but with poorer insertion loss. This problem can be partly solved if we combine the series configuration and shunt configuration. In the following we propose a design of SPST four-pHEMT switch.

In Figure 4.64, the parallel pHEMTs have common ground configuration to provide

better isolation at off state. V_{g1} is the control voltage for the series pHEMT; and V_{g2} is the control voltage for the parallel ones. The switch is on when the series pHEMT is on, the other three pHEMTs would be working under off state. And the switch is off when the series pHEMT is off, the other three would be on to provide good isolation.

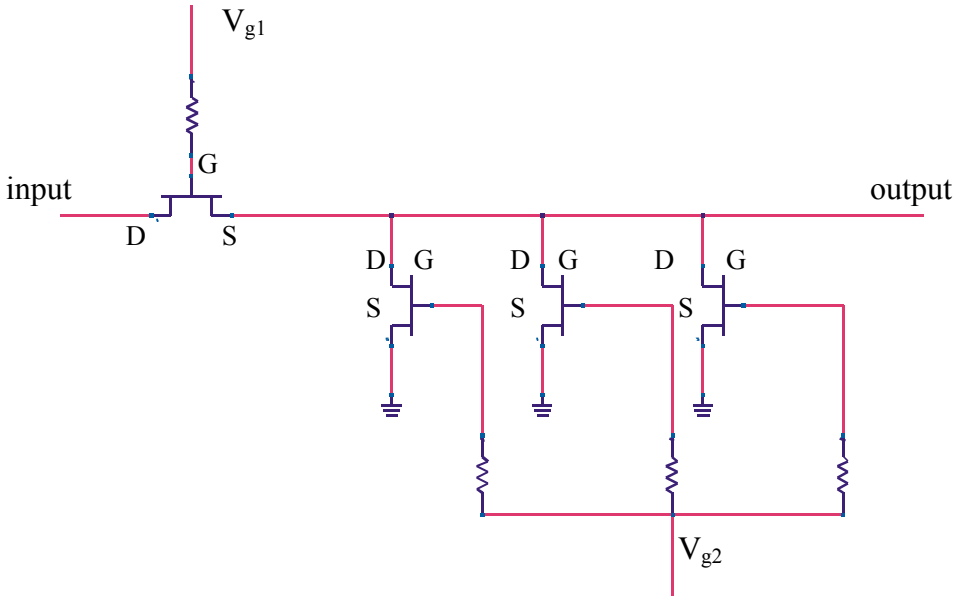


Figure 4.64: The proposed switch design using four pHEMTs.

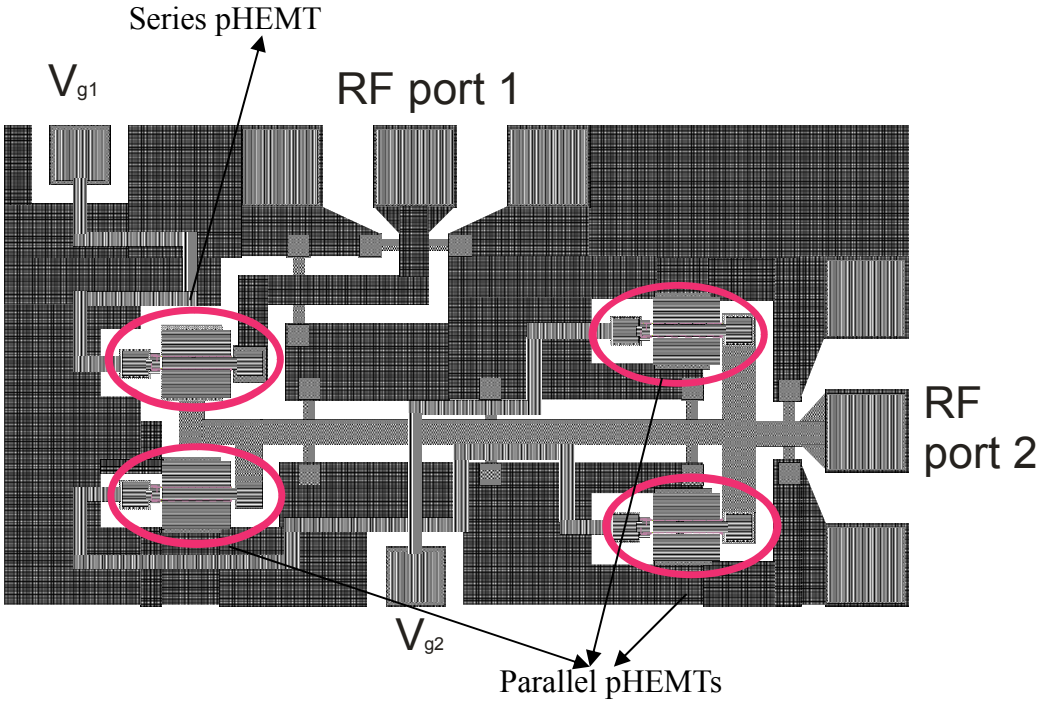
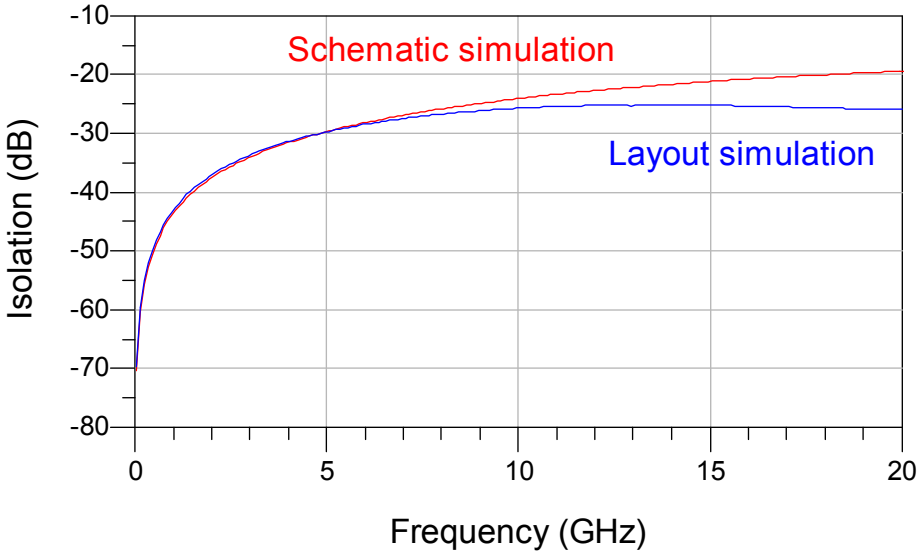
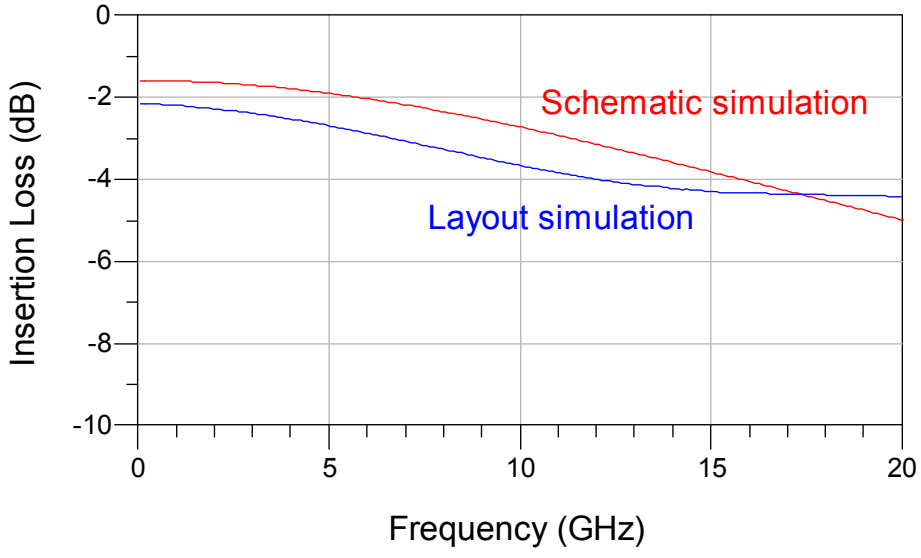


Figure 4.65: Layout of the switch design using four pHEMTs.

Figure 4.65 shows the layout of the designed switch applying multilayer CPW components. The size of the layout is measured as 1400 x 750 μm^2. The switch is simulated in ADS momentum using the modelled pHEMTs schematics, as well as using layout shown above (Figure 4.66).



(a)



(b)

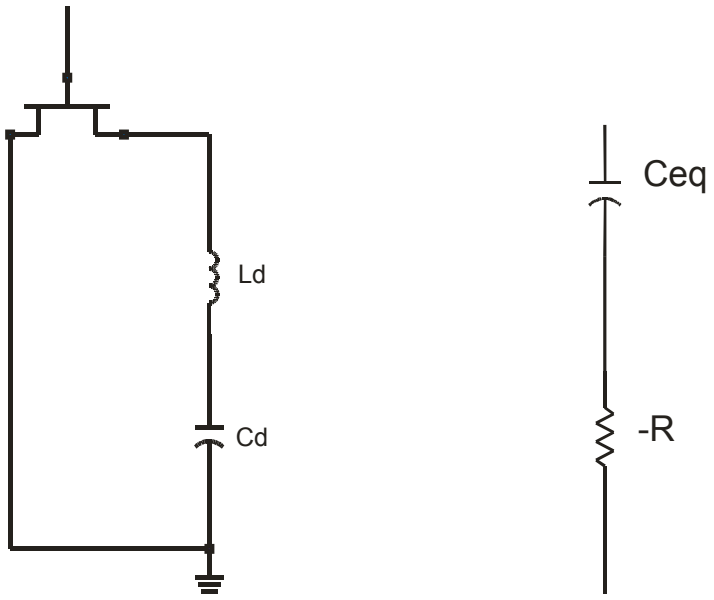
Figure 4.66: Isolation (a) and insertion loss (b) of the switch design using schematic and layout simulation.

The simulation data shown suggest that the proposed design is suitable for microwave and millimetre wave applications with reasonable performance. Good agreement between layout and schematic simulation also imply that the multilayer passive components applied in the circuit have reliable performances.

4.4 Multilayer active filter

Main types of MMIC active filters are reviewed in Chapter 2.5. With considerations of compactness and performance, negative resistance topology is chosen for our multilayer CPW technology.

In the conventional topologies, the negative resistance topology composed of common-source or common-gate series feedback structure. This feedback structure usually is used for oscillator design. Therefore, the noise performance of transistor is increased by series feedback structure. The proposed topology is common-source, and common-drain inductive and capacitive series feedback structure. Figure 4.67 shows the structure and the equivalent circuit of this topology. It is different from the conventional type by the oscillator design method. This topology doesn't use the common-source or common-gate series feedback structure with a major noise performance increment cause. Therefore, the noise performance can be improved by the proposed topology. The active capacitor made of pHEMT exhibits a negative resistance property as well as capacitive property. This topology is simple in structure and could be conveniently applied to the narrowband filter design [72].



(a) (b)

Figure 4.67: Proposed negative resistance circuit (a) and its simple equivalent circuit (b).

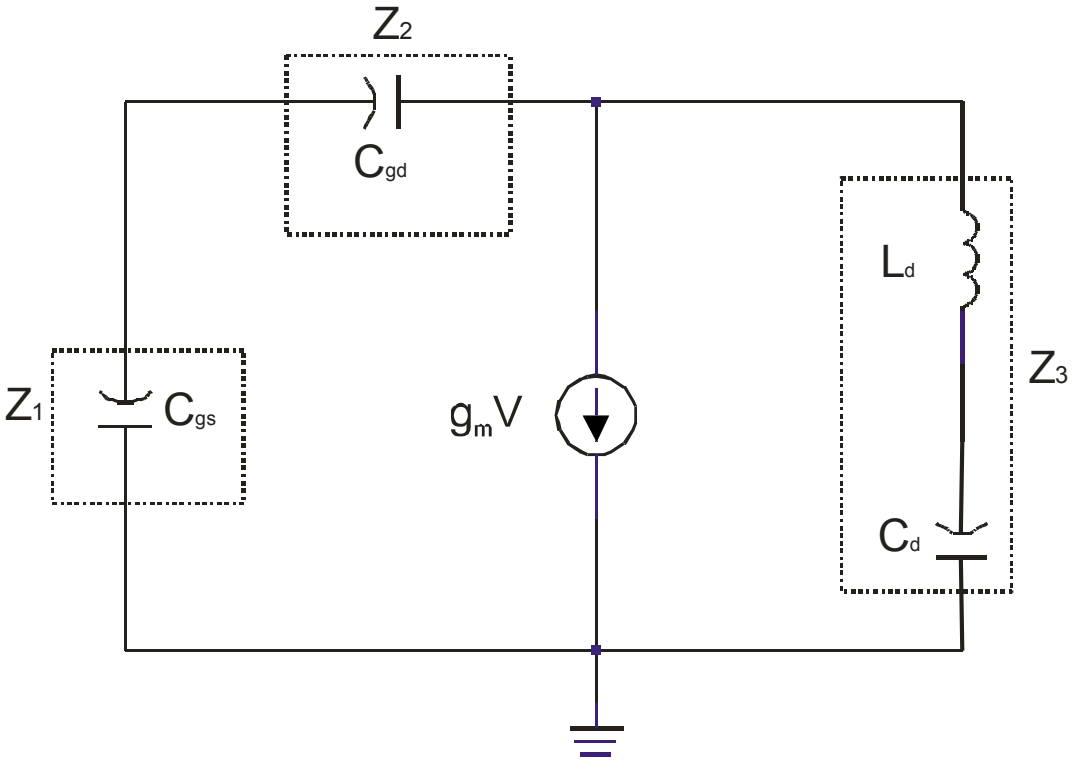


Figure 4.68: The complete equivalent circuit of the negative resistance circuit.

Figure 4.68 illustrates the complete equivalent circuit, where C_{gd}, C_{gs} and g_mV come from the active component, pHEMT, in our proposed circuit. According to the extracted result, the integrated pHEMT has: C_{gd} = 19 pF, C_{gs} = 380 pF and g_m = 70 ms.

The input impedance can be written [72]:

$$Z_{in} = \frac{Z_1(Z_2 + Z_3)}{Z_1 + Z_2 + Z_3 + g_m Z_1 Z_3} \tag{4.39}$$

Where, the parameters are

$$Z_1 = \frac{1}{jwC_{gs}} = -jX_1$$

$$Z_2 = \frac{1}{jwC_{gd}} = -jX_2$$

$$Z_3 = j(wL_d - \frac{1}{wC}) = jX_3$$

And $X_1, X_2, X_3 > 0$.

The expression 4.39 is

$$Z_{in} = \frac{g_m X_1^2 (X_3^2 - X_2 X_3)}{(g_m X_1 X_3)^2 + (X_3 - X_2)^2} - j\frac{X_1(X_3 - X_2)(X_3 - X_2 - X_1)}{(g_m X_1 X_3)^2 + (X_3 - X_2)^2}$$
$$= R_{neg} + \frac{1}{jwC_{eq}} \tag{4.40}$$

Therefore, the condition of negative resistance is

$$\frac{1}{\sqrt{L_d C_d}} < \omega < \sqrt{\frac{1}{L_d(\frac{C_d C_{gd}}{C_d + C_{gd}})}} \tag{4.41}$$

The proposed topology can be made negative resistance by the feedback L_d, C_d and gate to drain capacitor C_{gd}. The connecting by shunt inductor L_r at the proposed negative resistance circuit can make the resonator. The resonance frequency is

$$\omega_0 = \frac{1}{\sqrt{L_r C_{eq}}} \tag{4.42}$$

From the above analysis, it can be possible to design a new RF active bandpass filter. The resonance structure is composed of a feedback capacitor C_d, inductor L_d at drain, an external shunt inductor L_r, and series capacitor C_g, at gate. The parallel resonance circuit can be made by using the proposed negative resistance topology. Figure 4.69 shows the parallel resonator circuit. The capacitance of resonator is $C_g//C_{eq}$,. The resonance frequency is

$$\omega_0 = \frac{1}{\sqrt{L_r C_{eq} C_g}} \tag{4.43}$$

The quality factor Q of inductor is controlled by negative resistance, therefore, the losses of the resonator can be compensated for. Also, in the structure of the resonator, it can be connected by parallel capacitor in order to increase capacitance of the resonator. Here, R_d has no need of use in the circuit. The reason is that it is used for fine controlling of negative resistance.

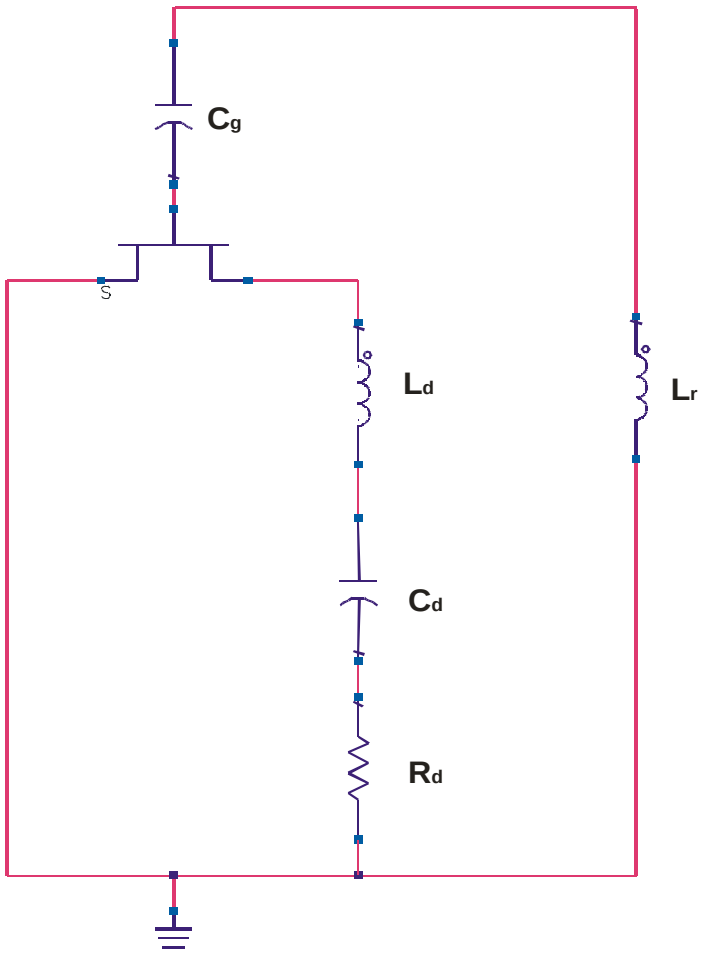


Figure 4.69: The second-order active filter circuit.

In Figure 4.70, a coupled second-order active filter is shown. C_{01}, C_{12} and C_{23} are acting as J-inverters.

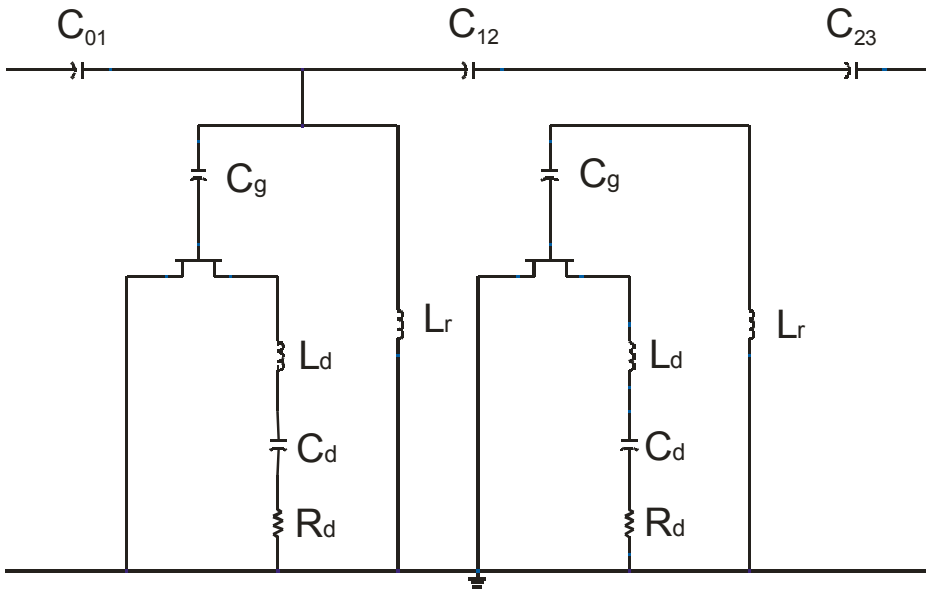
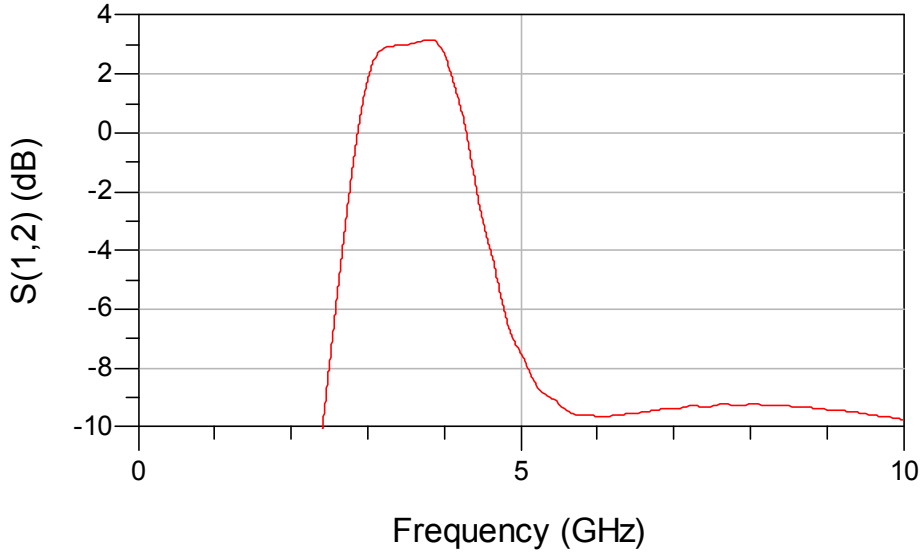
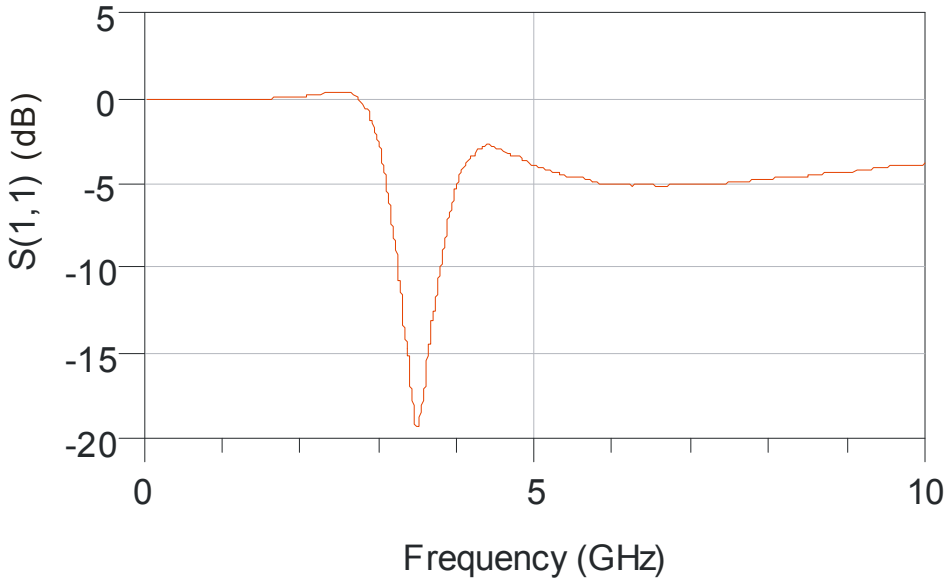


Figure 4.70: A coupled second-order active filter [72].

The circuit is built in ADS and then simulated. The active filter is centred at 3.5GHz. Figure 4.71 shows the 3 dB bandwidth of the filter is about 1.4 GHz. The gain of the filter within passband is about 3 dB. The bandwidth can be tuned to become smaller but with loss of gain. Also, S(1,1) in Figure 4.71 indicates there is quite good return loss at the centre frequency (-19dB). A layout design of this active filter is shown in Figure 4.72, which has an area of 3600 x 2200 μm^2.



(a)



(b)

Figure 4.71: Simulated S parameters of the proposed active filter circuit.

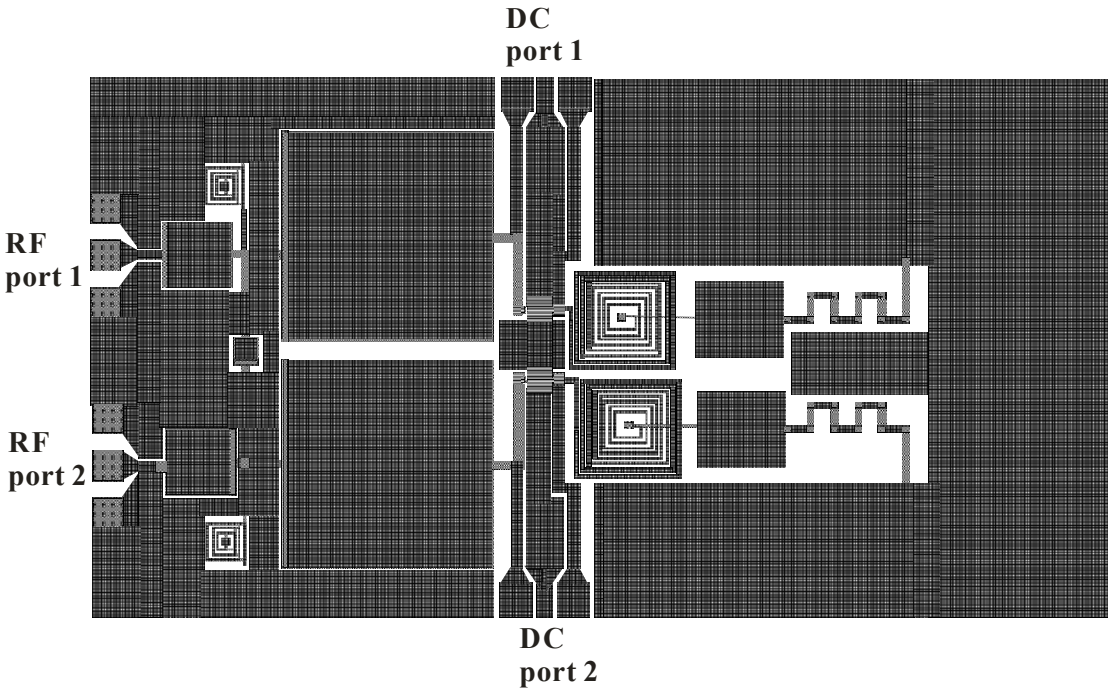


Figure 4.72: Layout design of the proposed active filter.

Chapter 5
Conclusions and future works

5.1 Conclusions

Multilayer CPW technology has been developed in this project. Multilayer transmission lines, MIM capacitors, switches and active filters have been designed, simulated, fabricated, measured and analysed. Thermal characterization of multilayer components from -25 to 125 ^{o}C has been carried out. Cutting-edge electromagnetic and circuit simulators were employed in the process of designing advanced MMICs. HP8251C Vector Network Analyser has been used to carry out RF measurements. Temptronics temperature controlling chamber is used to control and monitor the temperature. Various types of calibration methods have been studied and analysed. LRRM calibration and Open-Short-Thru de-embedding scheme are used to remove the systematic error occur in measurement and pads parasitics in the circuit. The CPW multilayer components reported in this work were fabricated at the Electromagnetic Centre, the University of Manchester. The multilayer technology employs the sandwiched structure consists of three metal conductor layers and two dielectric layers on a 0.6 mm thick semi-insulator GaAs substrate with prefabricated pHEMTs. Gold is used for metal conductor and polyimide is used for dielectric layers. The pHEMTs are used as active devices for integration with multilayer CPW passive components on a single substrate to demonstrate the possibility of forming ultra compact microwave on-chip circuits.

CPW multilayer transmission lines are designed, measured and characterized. The four featured transmission lines are characterized using effective dielectric constant

and dissipation loss. These transmission lines have been proven to provide wide range of characteristic impedance (approx. 10-75 Ω). Low impedance lines are realised using multilayer transmission lines with overlap. Reduced dissipation losses by using V-shaped and multilayer lines have successfully been achieved. Transmission lines with high impedance can be realised with elevated metal conductor layers. It is shown that by employing the multilayer structure, the dissipation loss of V-shape design is reduced by 25% comparing with conventional CPW structure at 10 GHz. RLC lumped element model is extracted to understand the transmission lines behaviour with the increase of frequency. Then, multilayer transmission lines are characterized within a temperature range of -25 ºC to 125 ºC, which is reported for the first time. Both DC and AC measurement are done and results are discussed. It is indicated that the conductor losses of the transmission lines increase with increasing ambient temperature causing the dissipation losses increase with ambient temperature. The data also show that the dissipation losses of the transmission lines are less sensitive to temperature at high frequency than at lower frequency due to the temperature dependent of the skin depth. We managed to show that 3-D technology has no negative effect on the circuits working under various temperature conditions. Meanwhile, the DC resistance degradation with temperature is shown to dominate the change of dissipation loss under different temperature circumstances. And then, eye diagram is used in a time domain characterization and some main eye parameters are extracted. Data extracted have further verified the findings in S-parameter characterizations. From the investigation of variation of ground and centre metal combination, it is shown that centre metal positions have more influence than the ground metal positions. This position optimization is carried out for the first time.

The design and modelling of several multilayer CPW capacitors, such as conventional and folded types, are carried out. It is observed that with the folded type of multilayer capacitor almost twice the capacitance is obtained when compared to the conventional type of capacitors having the same area. The four-element (namely the functional

capacitor, the capacitor to the ground, the series resistor and the parallel resistor) model is verified to be effective up to 10 GHz and good agreement has been achieved between the modelled and measured S-parameters. The approaches to extract Q factor and cut-off frequency are presented. Evaluation of Q factor and cut-off frequency is scaled with the area of MIM capacitors. The differences between the measurement and simulation, conventional and folded, are depicted and analyzed. Q factors, cut-off frequency, along with the extracted series resistance and parasitic capacitance are used to characterize the designed capacitors. Some design rules of CPW multilayer capacitors are achieved: with various distance of centre conductor and ground metal, the parasitic capacitance is studied; meanwhile, capacitors with different dimensions but with the same area are simulated to have very close performance on most parameters. This provides great flexibility of designing integrating multilayer capacitors. The feasibility of parallel capacitors is investigated. This provides an approach to design capacitor with large capacitance values. The potential problems are addressed and studied.

Multilayer CPW technology enables the manufacturer to fabricate various choice of miniature components on a single substrate with active devices, such as MESFET, pHEMT, HBT etc. to form a commercial competitive microwave circuit. In order to demonstrate this, switches and active filters are designed in this work. A four-pHEMT switch and an active-capacitor topology active filter are designed and simulated. The simulated result shows reasonable behaviour while the multilayer technology naturally makes them more compact than conventional CPW designs.

5.2 Future works

In Chapter 4.1, we chose four transmission lines to represent some typical multilayer designs in this project. But the designs with varied dimension, material and other alternative structures are not included. For example, elevated structure is another good choice for low-loss transmission lines with higher characteristic impedance than 50 Ω. Furthermore, it would be interesting to know how other dielectric materials, such as BCB and Silicon Nitride, collaborate with multilayer technology. This will certainly be helpful to establish a good library of 3-D CPW components.

The temperature dependence of the transmission line parameters provides a good aspect of studying the loss and material properties. This study still needs to be carried out on more complicated passive components such as power dividers, couplers and baluns. Also for circuits with active components, as the pHEMTs are buried under multiple layers of dielectric material, the junction temperatures of these active devices can typically reach about 150 to 200^{o}C. The heat generated must be dissipated properly, otherwise will result in the performance deviation of the integrated circuits. Therefore, it is essential to well address the issue.

As described in the Chapter 3.4 and 4.1.5, eye diagram measurement in this experiment is still not accurate enough as cable loss and system delay become serious after several gigahertz. It is reported in some published papers that the loss by system may reach about 30 %. Therefore it must be removed for higher level of eye diagram application. Meanwhile, impedance mismatch, another factor that will cause inaccuracy, should be improved in future work.

Some newly reported MIM capacitor structures need to be implemented into CPW multilayer structure for smaller size and better Q factor. This includes a comb structure and some designs using lateral field components.

Switches and active filter need to be fabricated and tested. With the measurement results, noise performance and power handling issue need to be studied. Meanwhile, other topology of switches and active filters need to be implemented into 3-D CPW technology to provide a wide range of selection for MMIC applications.

References

[1] Cheng P. Wen, “Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications”, IEEE Transactions on microwave theory and techniques, Vol. MTT-17, No.12, pp. 110-115, December 1969,

[2] Y. S. Yung, “A tutorial on GaAs vs Silicon”, in ASIC Conference and Exhibit, Proceedings of Fifth Annual IEEE International, pp. 281-287, 1992.

[3] J. Mun, “GaAs integrated circuits”, London: BSP Professional, 1988.

[4] D. Haigh and J. Everard, “GaAs technology and its impact on circuits and systems”, in IEE circuits and systems series; 1 London: Peregrines on behalf of the Institution of Electrical Engineers, 1989.

[5] J. L. B. Walker, “A Survey of European Activity on Coplanar Waveguide”, IEEE MTT-S Int. Microwave Symp. Dig., Vol.2, pp.693-696, Atlanta, Georgia, June 1993.

[6] A. K. Sharma and T. Itoh (Editors), “Special Issue on Modelling and Design of Coplanar Monolithic Microwave and Millimeter-Wave Integrated Circuits”, IEEE Trans. Microwave Theory Tech., Vol.41, No.9, Sept. 1993.

[7] T. Sporkmann, “The Evolution of Coplanar MMICs over the past 30 Years”, Microwave Journal, Vol.41, No.7, pp. 96-111, July 1998.

[8] T. Sporkmann, “The Current State of the Art in Coplanar MMICs”, Microwave Journal, Vol. 41, No. 8, pp. 60-74, Aug. 1998.

[9] J. Browne, “Broadband Amps Sport coplanar Waveguide”, Microwaves RF, Vol. 26, No. 2, pp. 131-134, Feb. 1987.

[10] “Technology Close-Up”, Microwaves RF, Vol. 27, No. 4, pp. 79, April 1988.

[11] J. Browne, “Coplanar Waveguide Supports Integrated Multiplier Systems”, Microwaves RF, Vol. 28, No. 3, pp. 137-138, March 1989.

[12] J. Browne, “Coplanar Circuits Arm Limiting Amp with 100-dB Gain”, Microwaves RF, Vol. 29, No. 4, pp. 213-220, April 1990.

[13] J. Browne, “Broadband Amp Drops through Noise Floor”, Microwaves RF, Vol.31, No. 2, pp. 141-144, Feb. 1992.

[14] J. Browne, “Coplanar MIC Amplifier Bridges 0.5 To 18.0 GHz”, Microwaves RF, Vol. 26, No. 6, pp. 194-195, June 1987.

[15] R. E. Stegens and D. N. Alliss, “Coplanar Microwave Integrated Circuit for Integrated Subsystems”, Microwave Sys. News Comm. Tech., Vol. 17, No. 11, pp. 84-96, Oct. 1987.

[16] J.S. Kilby and E. Keonjian, “Design of a semiconductor-solid-circuit adder”, in Electron Devices Meeting, 1959 International, pp. 76-78, 1959.

[17] J. L. Moll, “Integrated Circuits and Microminiaturization Education”, IRE Transactions on, vol. 3, pp. 141-144, 1960.

[18] H. K. Dicken and D. Bailey, “Integrated devices for hybrid circuits”, in Electron Devices Meeting, 1962 International, pp. 34, 1962.

[19] D. S. King, W. Corrigan, and G. Madland, “Methods of isolation of active elements in integrated circuits”, in Electron Devices Meeting, 1962 International, pp. 36, 1962.

[20] R. Kraus, “Vacuum Deposition Techniques in an Engineering Laboratory Facility for Producing Thin Film Integrated Circuits”, Product Engineering and Production, IEEE Transactions on, vol. 7, pp. 40-47, 1963.

[21] H. W. Ruegg, “An integrated FET analog switch”, Proceedings of the IEEE, vol. 52, pp. 1572-1575, 1964.

[22] H. A. Wheeler, “Transmission-Line Properties of Parallel Wide Strips by a Conformal-Mapping Approximation”, Microwave Theory and Techniques, IEEE Transactions on, vol. 12, pp. 280-289, 1964.

[23] H. A. Wheeler, “Transmission-Line Properties of Parallel Strips Separated by a Dielectric Sheet”, Microwave Theory and Techniques, IEEE Transactions on, vol. 13, pp. 172-185, 1965.

[24] H. A. Wheeler, “Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane”, Microwave Theory and Techniques, IEEE Transactions on, vol. 25, pp. 631-647, 1977.

[25] S. Mao, S. Jones, and G. D. Vendelin, “Millimeter-Wave Integrated Circuits”, Microwave Theory and Techniques, IEEE Transactions on, vol. 16, pp. 4550461, 1968.

[26] E. Mehal and R. Wacker, “GaAs Integrated Microwave Circuits”, Microwave Theory and Techniques, IEEE Transactions on, vol. 16, pp. 451-454, 1968.

[27] R. S. Pengelly and J. A. Turner, “Monolithic broadband GaAs FET amplifiers”, Electronics Letters, vol. 12, pp. 251-252, 1976.

[28] I. D. Robertson, “MMIC Design”, in IEE circuits and systems series; 7 London: Institution of Electrical Engineers, 1995.

[29] Van Tuyen Vo, Lokesh Krishnamurthy, Qing Sun, Ali A. Rezazadeh, “3-D Low-Loss Coplanar Waveguide Transmission Lines in Multilayer MMICs”, IEEE Trans. Microwave Theory and Techniques, Vol. 54, No. 6, pp. 2864-2871, June 2006.

[30] T. C. Edwards and M. B. Steer, “Foundations of Interconnect and Microstrip Design”, Third Edition, Chapter Six, 2002.

[31] Kenjiro Nishikawa and Ichihiko Toyoda, “Recent Progress in 3D/Multilayer MMIC Technology”, pp. 1-4.

[32] D. Budimir, Q. H. Wang, A. A. Rezazadeh, and I. D. Robertson, “V-shape CPW transmission lines for multilayer MMICs”, Electron. Letters, Vol. 31, pp. 1928-1929, Oct. 1995.

[33] H. Ogawa, T. Hasegawa, S. Banba, and H. Nakamoto, “MMIC transmission lines for multi-layered MMICs”, in IEEE MTT-S Int. Microwave Symp. Dig., pp. 1067-1069, 1991.

[34] C. Warns, W. Menzel, and H. Schumacher, “Transmission lines and passive elements for multilayer coplanar circuits on silicon”, IEEE Trans. Microwave Theory Tech., Vol. 46, No. 5, pp. 616-622, May 1998.

[35] D. M. Pozar, “Microwave Engineering”, 3rd ed. New York; Wiley, 2005.

[36] D. D. Grieg and H. F. Engelmann, “Microstrip-A new transmission technique for the Klilomegacycle range”, Proceedings of the IRE, vol. 40, pp. 1644-1650, 1952.

[37] H. R. Kaupp, “Characteristics of Microstrip Transmission Lines”, Electronic Computers IEEE Transactions on, vol. EC-16, pp. 185-193, 1967.

[38] E. Yamashita, “Variational Method for the Analysis of Microstrip-Like Transmission lines”, Microwave Theory and Techniques, IEEE Transactions on, vol. 16, pp. 529-535, 1968.

[39] G. I. Zysman and D. Varon, “Wave Propagation in Microstrip Transmission Lines”, in Microwave Symposium Digest, G-MTT International, pp. 3-9, 1969.

[40] M. Maeda, “An analysis of Gap in Microstrip Transmission Lines”, Microwave Theory and Techniques, IEEE Transactions on, vol. 20, pp. 390-396, 1972.

[41] M. V. Schneider, “Microstip dispersion”, Proceedings of the IEEE, vol. 60, pp. 144-146, 1972.

[42] B. E. Spielman, “Dissipation Loss Effects in Isolated and Coupled Transmission Lines”, Microwave Theory and Techniques, IEEE Transactions on, vol.25, pp. 648-656, 1977.

[43] C. M. Krowne, “Network analysis of microwave oscillators using microstrip transmission lines”, Electronics Letters, vol. 13, pp. 115-117, 1977.

[44] M. Kuma, “Coupling between two microstrip lines through apertures”, Electronics Letters, vol. 14, pp. 415-416, 1978.

[45] E. Van Lil and A. Van De Capelle, “Transmission line model for mutual coupling between microstrip antennas”, Antennas and Propagation, IEEE Transactions on, vol. 32, pp. 816-821, 1984.

[46] J. Svacina, “Alternative computation of attenuation in microstrip”, Electronics Letters, vol. 27, pp. 847-848, 1991.

[47] D. K. Paul, P. Gardner, and B. Y. Prasetyo, “Broadband branchline coupler for S-band”, Electronics Letters, vol. 27, pp. 1318-1319, 1991.

[48] H. Ogawa, T. Hasegawa, S. Banba, and H. Nakamoto, “MMIC transmission lines for multi-layered MMICs”, in Microwave Symposium Digest, 1991., IEEE MTT-S International, vol. 3, pp. 1067-1070, 1991.

[49] M. Kobayashi and N. Sawada, “Analysis and synthesis of tapered microstip transmission lines”, Microwave Theory and Techniques, IEEE Transactions on, vol.40, pp. 1642-1646, 1992.

[50] R. M. Barrett, “Microwave Printed Circuits – A Historical Survey”, Microwave Theory and Techniques, IRE Transactions on, vol. 3, pp. 1-9, 1955.

[51] C. A. Harper, “High Performance Printed Circuit Boards”, New York: McGraw Hill, 2000.

[52] S. B Cohn, “Slot-line: An Alternative Transmission Medium for Integrated Circuits”, Microwave Symposium Digest, G-MTT International, pp. 104-109, 1968.

[53] S. B. Cohn, “Slot Line on a Dielectric Substrate”, Microwave Theory and Techniques, IEEE Transactions on, vol. 17, pp. 768-778, 1969.

[54] E. A. Mariani, C. P. Heinzman, J. P. Agrios, and S. B. Cohn, “Slot Line Characteristics”, Microwave Theory and Techniques, IEEE Transactions on, vol. 17, pp. 1091-1096, 1969.

[55] A. Skalare, E. Kollberg, and J. Johansson, “Slot Line Components For Millimeter Wave and Sub-Millimeter Wave Integrated Circuits”, in European Microwave Conference, 18th, pp. 665-668, 1988.

[56] D. Budimir, I. D. Robertson, A. H. Khalid and A. A. Rezazadeh, “Low loss multilayer coplanar waveguide transmission lines on silicon substrate for MMICs”, in European Microwave Conference, 26th, pp. 697-700, 1996.

[57] D. Sriram Kumar, A. Srinivas and G. Ratnakar, “Simulation and analysis of coplanar waveguide (CPW) discontinuities”, in Recent Advances in Microwave Theory and Applications, 200, Microwave 2008 International Conference on, pp. 784-786, 2008.

[58] Queennie S. I. Lim, Albert V. Kordesch and Richard A. Keating, “Performance comparison of MIM capacitors and metal finger capacitors for analog and RF applications”, 2004 RF and Microwave Conference, pp. 85-89, Malaysia, 2004.

[59] Roberto Aparicio and Ali Hajimiri, “Capacity limits and matching properties of integrated capacitors”, IEEE Journal of solid-state circuits, Vol. 37, No. 3, pp.384-393, March 2002.

[60] Yue, C. P. and S. S. Wong, “Physical modelling of spiral inductors on silicon”, IEEE Transactions on Electron Devices, Vol. 47, No. 3, pp. 560-568, March 2000.

[61] Bahl, I. J., “Improved quality factor spiral inductors on GaAs substrates”, IEEE

Microwave and Guided Wave Letters, Vol. 9, No. 10, pp. 398-400, October 1999.

[62] L. Krishnamurthy, V. T. Vo and A. A. Rezazadeh, “Thermal Characterization of Compact Inductors and Capacitors for 3D MMICs”, Proceedings of the 36th European Microwave Conference, pp. 52-55, 2006.

[63] Magdalene W. C. Goh and etc. “Design of Radio Frequency Metal-Insulator-Metal (MIM) Capacitors”, Solid-State and Integrated Circuits Technology, Proceedings, 7th International Conference on, pp.209 – 212, vol.1, 2004.

[64] O. Leistiko and D. Hilbiber, ‘The FET tetrode: A High-performance, small-signal amplifier,’ in Electron Devices Meeting, 1964 International, pp. 60, 1964.

[65] K. E. Lyon, “FETs in Communication Circuit Applications”, Broadcast and Television Receivers, IEEE Transactions on, vol. 11, pp. 79-83, 1965.

[66] K. F. Smith and J. E. Cline, “A Low-noise Charge Sensitive Preamplifier for Semiconductor Detectors Using Paralleled Field-Effect-Transistors”, Nuclear Science, IEEE Transactions on, vol. 13, pp. 468-476, 1966.

[67] M. Maeda and Y. Minai, “Microwave Variable-Gain Amplifier with Dual-Gate GaAs FET”, Microwave Theory and Techniques, IEEE Transactions on, vol. 22, pp. 1226-1230.

[68] P. H. Ladbrooke, “MMIC design: GaAs FETs and HEMTs”, Boston, Mass.; London: Artech House, 1989.

[69] S. J. J. Teng, C S. Wu, L. D. Hou, and D. C. Wang, “Implant isolation of InGaAs/GaAs pseudomorphic high-electron mobility transistor structure using boron”,

Electronics Letters, vol. 30, pp. 1539-1540, 1994.

[70] C. S. Wu, F. Ren, S. J. Pearton, M. Hu, C. K. Pao, and R. F. Wang, “High efficiency microwave power Al GaAs/In GaAs PHEMTs fabricated by dry etch single gate recess”, Electron Devices, IEEE Transactions on, vol. 42, pp. 1419-1424, 1995.

[71] N. X. Nguyen, W. N. Jiang, K. A. Baumann, and U. K. Mishra, “High breakdown AlGaAs/InGaAs/GaAs PHEMT with tellurium doping”, Electronics Letters, vol. 31, pp. 586-588, 1995.

[72] Jae-Ryong Lee, Young-Hoon Chun and Sang-Won Yun, “A Novel Bandpass Filter Using Active Capacitance”, Microwave Symposium Digest, 2003 IEEE MTT-S International, Vol.3, pp. 1747-1750, 2003.

[73] Filtronic application note, “Discrete FET/pHEMT Devices”, Revision A, August 1996.

[74] R. N Assaly, “Some Designs of X Band Diode Switches”, Microwave Theory and Techniques, IEEE Transactions on, vol. 14, pp. 553-563, 1966.

[75] W. C. Jakes, “Analysis of coupling loops in waveguide and application to the design of a diode switch”, Microwave Theory and Techniques, IEEE Transactions on, vol. 14, pp. 189-200, 1966.

[76] H. Mott and D. N. McQuiddy, “The Harmonics Produced by a PIN Diode in a Microwave Switching Application”, Microwave Theory and Techniques, IEEE Transactionss on, vol 15, pp. 180-181, 1967.

[77] K. E. Mortenson, J. F. White, A. Armstrong, and J. Borrego, “Bulk

Semiconductor Switches and Phase Shifters", in Microwave Symposium Digest, G-MTT International, pp. 190-196, 1968.

[78] W. O. Schlosser, J. P. Beccone, and R. S. Riggs, "A Pin Diode for mm-Wave Digital Modulation", in Microwave Symposium Digest, G-MTT International, pp. 114-117, 1970.

[79] R. H. Pflieger, "Spaceborne Hybrid MIC PIN Diode Radiometer Switch", in Microwave Symposium Digest, GMTT International, pp. 8-10, 1972.

[80] R. Tayrani and R. W. Glew, "Ultra fast GaAs microwave PIN diode", Electronics Letters, vol. 19, pp. 479-480, 1983.

[81] C. Barratt, A. Christou, N. Jansen, R. E. Neidert, Jr., M. L. Ruess, and C. W. Young, "New GaAs PIN Diodes with Lower Dissipation Loss, Faster Switching Speed at Lower Drive Power", in Microwave Symposium Digest, MTT-S International, pp. 507-509, 1983.

[82] D. Leenov, "The silicon Pin diode as a microwave radar protector at megawatt levels", Electron Devices, IEEE Transactions on, vol. 11, pp. 53-61, 1964.

[83] H. R. Malone, M. L. Matson, and P. D. Kennedy, "High Power PIN Diode Switch Matrix", in Microwave Symposium Digest, 1974 S-MTT International, pp. 173-175, 1974.

[84] C. J. Georgopoulos, "High Power Pin Diode Switching Circuitry With Built-In Short Circuit Protection", Industrial Electronics and Control Instrumentation, IEEE Transactions on, vol. IECI-23, pp. 302-307, 1976.

[85] W. C. Tsai, S. F. Paik, and B. S. Hewitt, “Switching & Frequency Conversion using Dual-Gate FETs”, European Microwave Conference 9th, pp. 311-315, 1979.

[86] W. V. McLevige and V. Sokolov, “Microwave switching with parallel-resonated GaAs FETs”, Electron Device Letters, IEEE, vol. 1, pp. 156-158, 1980.

[87] M. Hieda, K. Nakahara, K. Miyaguchi, H. Kurusu, Y. Iyama, T. Takagi and S. Urasaki, “High-isolation series shunt FET SPDT switch with a capacitor cancelling FET parasitic inductance”, Microwave Theory and Techniques, IEEE Transactions on, vol. 49, pp. 2453-2458, 2001.

[88] D. A. Blackwell, D. E. Dawson, and D. C. Buck, “X-band MMIC switch with 70 dB isolation and 0.5 dB insertion loss”, in Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1995. Digest of Papers, pp. 97-100, 1995.

[89] N. Imai, A. Minakawa, and H. Okazaki, “Novel high isolation FET switches”, Microwave Theory and Techniques, IEEE Transactions on, vol. 44, pp. 685-891, 1996.

[90] JaeKyoung Mun, HongGu Ji, Hyokyun Ahn, Haecheon Kim and C. O. Park, “Design and fabrication of pHEMT MMIC switches for IEEE 802.11.a/b/g WLAN applications”, Semiconductor Science Technology, vol. 20, pp. 677-684, 2005.

[91] M. J. Schindler and A. Morris, “DC-40GHz and 20-40 GHz MMIC SPDT Switches”, Microwave Theory and Techniques, IEEE Transactions on, vol. 35, pp. 1486-1493, 1987.

[92] A. Gopinath and J. B. Rankin, “GaAs FET RF switches”, Electron Devices, IEEE Transactions on, vol. 32, pp. 1272-1278, 1985.

[93] Christen Rauscher, “Two-Branch Microwave Channelized Active Bandpass Filters”, IEEE Transactions on microwave theory and techniques, Vol. 48, No. 3, pp.437-444, March 2000.

[94] U. Karacaoglu, S. Lucyszyn, I.D. Robertson and M. Guglielmi, “GaAs MMIC Active filters for L-band mobile systems”, printed and published by the IEE, Savoy Place, London WC2R 0BL, UK, 1994.

[95] E. C. Krantz and G. R. Branner, “Active microwave filters with noise performance considerations”, IEEE Trans. Microwave Theory Tech., vol. 42, pp.1368-1378, July 1994.

[96] H. Ezzedine, L. Billonnet, B. Jarry, and P. Guillon, “Optimization of noise performance for various topologies of planar microwave active filters using noise wave techniques”, IEEE Trans. Microwave Theory Tech., vol. 46, pp. 2484-2492, Dec. 1998.

[97] Kwok-Keung M. Cheng and Hil-Yee Chan, “Noise performance of negative-resistance compensated microwave bandpass filters- theory and experiments”, IEEE Transactions on microwave theory and techniques, Vol. 49, No. 5, pp.924-927, May 2001.

[98] Chi-yang Chang and Tatsuo Itoh, “Microwave Active filters based on coupled negative resistance method”, IEEE Transactions on Microwave theory and techniques, Vol. MTT-33, No. 12, pp.1879-1884, December 1985.

[99] K. D. Adams and R. Y. C. Ho, “Active filters for UHF and microwave frequencies,” IEEE Trans. Microwave Theory Tech., Vol. MTT-17, pp. 662-670, Sept. 1969.

[100] R. V. Snyder and D. L. Bozarth, “Analysis and design of a microwave transistor active filter”, IEEE Trans. Microwave Theory Tech., vol. MTT-1R, pp. 2-9, Jan. 1970.

[101] A. Presser, “Varactor-tunable, high-Q microwave filter,” RCA Rei, vol. 42, pp. 691-705, Dec. 1981.

[102] R. E. Collin, “Foundations for microwave Engineering”, New York: McGraw-Hill, 1972, CH. 7.

[103] K. K. M. Cheng and S. C. Chan, “Reduction of intermodulation distortion in microwave active bandpass filters: Theory and experiments”, IEEE Trans. Microwave Theory Tech., vol. 48, pp.221-225, Feb. 2000.

[104] Christen Rauscher, “Microwave active filters based on transversal and recursive principles”, IEEE Transactions on microwave theory and techniques, Vol. 38, No. 12, pp.1350-1360, December 1990.

[105] Christen Rauscher, “Microwave Channelized Active Filter: A new modular Approach to Achieving Compactness and High Selectivity”, IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 1, pp. 122-132, January 1996.

[106] Christen Rauscher, “Two branch microwave channelized active bandpass filters”, IEEE Transactions on microwave theory and techniques, Vol. 48, No. 3, pp.437-444, March 2000.

[107] Cascade Microtech, “Application Note: On-Wafer Vector Network Analyzer Calibration and Measurements”.

[108] Eric Strid, “On-Wafer Measurements with the HP 8510 Network Analyzer and

Cascade Microtech Wafer Probes", RF & Microwave Measurement Symposium and Exhibition.

[109] Larry Dangremond, "Wafer-Level RF Measurement Basics", Cascade Microtech, July 2006.

[110] Anthony Lord, "Comparing the Accuracy and Repeatability of On-Wafer Calibration Techniques to 110 GHz", Cascade Microtech, Oxfordshire, UK.

[111] Franz Sischka, "Characterization Handbook", Chapter 3.3.2.1, April 2002.

[112] R. A. Hackborn, "An Automatic Network Analyzer System", Microwave Journal, pp45-52, May 1968.

[113] S. Rehnmark, "On the Calibration Process of Automatic Network Analyzer Systems", IEEE Trans. on Microwave Theory and Techniques, pp. 457-458, April 1974.

[114] N. R. Franzen, R. A. Speciale, "A New Procedure for System Calibration and Error Removal in Automated S-parameter Measurements", Proc. 5th European Microwave Conf., pp. 69-73, 1975.

[115] G. F. Engen, C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual 6-Port Automatic Network Analyzer", IEEE Trans. on Microwave Theroy and Techniques, MTT 27-12, pp. 987-983, Dec. 1979.

[116] H. J. Eul, B. Schiek, "Thru-Match-Reflect: One Result of A Rigorous Theory For De-embedding and Network Analyzer Calibration", Proc. 18th European Microwave Conf., pp. 909-914, Sept. 1988.

[117] R. A. Soares et al, "A Unified Mathematical Approach to Two-Port Calibration

Techniques and Some Applications", IEEE Trans. on Microwave Theory and Techniques, MTT 37-11, pp. 1669-1674, November 1989.

[118] D. K. Rytting, "Advances in Microwave Error Correction Techniques", Hewlett-Packard RF & Microwave Symposium, June 1987.

[119] John T. Barr et al, "A Generalized Vector Network Analyzer Calibration Technique", Hewlett Packard, Network Measurements Div. Santa Rosa, CA.

[120] C. A. Hoer, G. F. Engen, "Calibrating a Dual Six-Port or Four-Port For Measuring Two Ports With Any Connectors", 1986 IEEE MTT-S International Microwave Symposium Digest, pp. 665-668, June 1986.

[121] Andrew Davidson, Keith Jones, Eric Strid, "LRM and LRRM Calibrations with Automatic Determination of Load Inductance", Cascade Microtech, Inc.

[122] Anthony Lord, "Optimising On-wafer Measurement Performance for Device Characterization and Modelling", Cascade Microtech, May 2004.

[123] J. E. Pence, "Verification of LRRM Calibrations with Load Inductance Compensation for CPW Measurements on GaAs Substrates", Cascade Microtech, Beaverton.

[124] Anthony Lord, "Comparing the Accuracy and Repeatability of On-Wafer Calibration Techniques to 110 GHz", Cascade Microtech, Oxfordshire, UK.

[125] www.complextoreal.com

[126] Ming-Hsiang Cho, Guo-Wei Huang, Chia-Sung Chiu, Kun-Ming Chen, An-Sam Peng and Yu-Min Teng, "A Cascade Open-Short-Thru (COST) De-Embedding

Method for Microwave On-wafer Characterization and Automatic Measurement", IEICE Trans. Electron., Vol. E88-C, pp. 5, May 2005.

[127] W. R. Eisenstadt and Y.Eo, "S-parameter-based IC interconnect transmission line characterization," IEEE Trans. Comp. Hybrids, Manuf. Technol., vol. 15, no. 5, Aug.1992.

[128] Agilent Technologies, Manual – ADS Circuit Simulation.

[129] Gupta, K. C, "Microstrip lines and slotlines", 2nd ed. Artech House, 1996.

[130] Mike Golio, "The RF and Microwave handbook", CRC Press, 2001.

[131] Yungseon Eo and William R. Eisenstadt, "High-Speed VLSI Interconnect Modelling Based on S-parameter Measurements", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 5, August 1993.

[132] Eric Bogatin, "What you lose from a lossy line", Synergetix Inc, and Gene Garat, Mentor Graphic.

[133] Sanjeev Gupta and Gunner Boe, "Optimizing Interconnect Performance With Eye Diagrams", Agilent Technologies EEsof EDA division, August 2006.

[134] R. Kulke, P. Pogatzki, D. Kother, T. Sporkmann, I. Wolff, "Enhancement of coplanar capacitor models and verification up to 67GHz for MMIC circuit design", European Microwave Conference, 1994. 24th, Volume 1, pp. 258 – 262, Oct 1994.

[135] Kalavathi Subramaniam, Albert Victor Kordesch, Mazlina Esa, "Nine-Element

lumped metal-insulator-metal (MIM) capacitor model for RF Application", International Electronic Manufacturing Technology, Putrajaya, Malaysia, 2006.

[136] Noel Segura and etc., "A predictive analytical model of 3D MIM capacitors for RC IC", IEDM 2007. IEEE International, pp. 553 – 556, 10-12 Dec. 2007.

[137] M. Schindler and A. Morris, "DC-40GHz and 20-40GHz MMIC SPDT Switches", Microwave Theory and Techniques, IEEE Trans., vol. 35, pp. 1486-1493, 1987.

[138] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit", Microwave Theory and Techniques, IEEE Transactions on, vol. 36, pp. 1151-1159, 1988.

[139] Y. Tasukahara, H. Amasuga, S. Goto, T. Oku, and T. Ishikawa, "60GHz High Isolation SPDT MMIC switches using shunt pHEMT resonator", in Microwave Symposium Digest, 2008 IEEE MTT-S international, pp. 1541-1544, 2008.

[140] K. K. Samanta & I. D. Robertson, "Experimental study of ground plane width effect in multilayer MCM CPW lines", Proceedings of the 3rd European Microwave Integrated Circuits Conference, Amsterdam, Oct 2008.

[141] S. Gevorgian and etc., "Simple and accurate dispersion expression for the effective dielectric constant of coplanar waveguides", IEE Proc.-Microwave Antennas Propagation, Vol. 144, No. 2, April 1997.

[142] K. K. Samanta & I. D. Robertson, "The effect of dielectric height and ground plane width on multilayer MCM FGCPW lumped elements", Proceedings of the 38th European Microwave Conference, Amsterdam, Oct 2008.

[143] Frenkel, M. Y., Gupta, S., Valdmanis, J.A., and Mourou, G.A.: 'Terahertz attenuation and dispersion characteristics of coplanar transmission lines', IEEE Trans. Microwave Theory Tech., 1991, 39, pp. 910-916.

[144] Eufinger, B., and Feldle, H. P.: 'Coplan: CAD program for calculating numerous coplanar line types with consideration of frequency dependency'. Proc. 21 EuMC, 1991, pp. 1527- 1532.

[145] Haydle, W.H., Braunstein, J., Kitawaza, T., Schlechtweg, M., Tasker, P., and Eastman, L.F.: 'Attenuation of millimeterwave coplanar lines on gallium arsenide and indium phosphide over the range 1-60 GHz', IEEE MTT-S Int. Microw. Symp. Dig., 1992, pp. 349–352.

[146] Heinrich, W.: 'Conductor loss on transmission lines in monolithic microwave and millimeter-wave integrated circuits', Int. J. Microw. Millim.-Wave Computer Aided Eng., 1992, 2, pp. 155–167.

[147] Heinrich, W.: 'Quasi-TEM description of MMIC coplanar lines including conductor-loss effects', IEEE Trans. Microw. Theory Tech., 1993, 41, pp. 45–52.

[148] Ke, J.-Y., and Chen, C.H.: 'Dispersion and attenuation characteristics of coplanar waveguides with finite metallization thickness and conductivity', IEEE Trans. Microw. Theory Tech., 1995, 43, pp. 1128–1135.