Strained Si Heterojunction Bipolar Transistors

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Abstract

This dissertation addresses the world's first demonstration of strained Si Heterojunction Bipolar Transistors (sSi HBTs). The conventional SiGe Heterojunction Bipolar Transistor (SiGe HBT), which was introduced as a commercial product in 1999 (after its first demonstration in 1988), has become an established device for high-speed applications. This is due to its excellent RF performance and compatibility with CMOS processing. It has enabled silicon-based technology to penetrate the rapidly growing market for wide bandwidth and wireless telecommunications once reserved for more expensive III–V technologies. SiGe HBTs is realised by the pseudomorphic growth of SiGe on a Si substrate, which allows engineering of the base region to improve performance. In this way the base has a smaller energy band gap than the emitter, which increases the gain. The energy band gap of SiGe reduces with increasing Ge composition, but the maximum Ge composition is limited by the amount of strain that can be accommodated within a given base layer thickness. Therefore, a new innovation is necessary to overcome this limitation and meet the continuous demand for high speed devices. Growing the SiGe base layer over a relaxed SiGe layer (Strain Relaxed Buffer) can increase the amount of Ge that can be incorporated in the base, hence, increasing the device performance. In this thesis, experimental data is presented to demonstrate the realisation of sSi HBTs. The performance of this novel device has been also investigated and explained using TCAD tool.

Symbols

A	**Cross-section of the junction**
A*	**Richardson's constant**
a_{Si}	**Lattice constant of Si**
a_{SiGe}	**Lattice constant of $Si_{1-x}Ge_x$**
a_{Ge}	**Lattice constant of Ge**
E_a	**Activation energy**
BV_{CEO}	**Collector-emitter breakdown voltage at open base**
BV_{CB0}	**Collector-base breakdown voltage at open base**
β	**Current gain**
C	**Capacitance**
C_i	**Impurity concentration**
C_{jc}	**Base-collector depletion capacitance**
D_0	**Diffusion coefficient**
D_n	**Electron diffusivity**
D_p	**Hole diffusivity**
D_{nb}	**Electron diffusivity in the base**
D_{pe}	**Hole diffusivity in the emitter**
D1	**Distance to the collector**
D2	**Distance to the base**
ΔE_{gB}	**Reduction of the ban-gap of the base due to the presence of Ge**
ΔE_G	**Band-gap difference**

$\Delta E_{G,H}$	**Band -gap narrowing caused by doping**
ΔE_C	**Conduction band discontinuity**
ΔE_V	**Valence band discontinuity**
δ	**Tunnelling coefficient**
E_F	**Fermi level**
E_{Fn}	**Electron quasi Fermi level**
E_{Fp}	**Hole quasi Fermi level**
E_g	**Band-gap**
E_i	**Intrinsic Fermi level**
E_n	**Electric field vectors**
E_p	**Electric field vectors**
E_W	**Emitter window width**
ε	**Electric field**
f	**Frequency**
f_C	**Corner frequency**
f_T	**Cut-off frequency**
f_{max}	**Maximum oscillation of frequency**
$\hbar$	**Reduced Planck's constant**
I_B	**Base current**
I_C	**Collector current**
I_n	**Electron diffusion current**
I_p	**Hole diffusion current**
I_{R-G}	**Thermal generation current**
J	**Net flux of the impurity material**

J_C	**Collector current density**
Jn	**Electrons current density**
Jp	**Holes electron dnsity**
k	**Boltzmann's constant**
K	**Constant**
χ	**Electron affinity**
L	**Length**
L_P	**Hole diffusion length**
λ	**Thermal conductivity**
m	**Ideality factor**
m_e	**Electron mass**
μ_n	**Electron mobility**
μ_p	**Hole mobility**
τ_E	**Emitter transit time**
N region	**Region that is doped with donors impurity**
N_a	**Acceptor concentration in the base**
N_a^-	**Uncompensated acceptors**
N_d^+	**Uncompensated donor ions**
N_{ab}	**Base doping**
N_{CB}	**Density of state in the conduction band in the base layer**
N_{VB}	**Density of state in the valence band in the base layer**
N_E	**Emitter doping concentration**
n_i	**Intrinsic carrier concentration**
n_{iB}	**Intrinsic carrier concentration in the base region**

n_{iE}	Intrinsic carrier concentration in the emitter region.
n_p	Electron concentration in the P region
n_{ie}	Intrinsic carrier concentration at high doping level
n	Electron concentration
N_{deff}	Effective doping concentration in the emitter
p	Hole concentration
P region	Region that is doped with acceptor impurity
p_n	Hole concentration in the N region
p_p	Hole concentration in the P region
P_S	Power consumption
q	Electronic charge
R	Resistance
r_B	Base resistance
r_{be}	Base-emitter resistance
R_{th}	Thermal resistance
S_{IB}	spectral power density of the base current noise source
S_{IC}	spectral noise density of the collector current noise source
S_{ϕ}	Phase noise
T	Temperature
T_O	Ambient temperature
τ	Characteristic time constant of Lorentzian spectrum $1/f^2$
τ_n	Electron life time
τ_p	Hole life time
τ_B	Base transit time

$\mathbf{U_{Auger}}$	**Auger recombination rate**
$\mathbf{U_{SRH}}$	**Shockley-Read-Hall recombination rate**
$\mathbf{U_n}$	**Electron recombination rates**
$\mathbf{U_p}$	**Hole recombination rates**
V	**Voltage**
$\mathbf{V_{BE}}$	**Base–emitter voltage**
$\mathbf{v_{eff}}$	**Saturation velocity**
$\mathbf{\nu_n}$	**Mean electron thermal velocity**
$\mathbf{\nu_p}$	**Mean hole thermal velocity**
$\mathbf{W_p}$	**Width of the P region**
$\mathbf{W_n}$	**Width of the N region**
W	**Depletion layer width**
$\mathbf{W_E}$	**Emitter width region**
$\mathbf{W_B}$	**Base width region**
$\mathbf{W_M}$	**Mesa length**

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Chapter 1. Introduction

1.1 Introduction

The transistor was probably the most important invention of the 20th Century. It is the key element of any integrated circuit. This device can operate as switch or amplify a signal. The transistor is considered as a perfect alternative to the vacuum tube, since it is small and consumes low energy compared to the vacuum tube. Since the first fabrication of the transistor, there have been an enormous number of developments in the design and the fabrication techniques.

Given the recent development and need in the communication market, the bipolar transistor, which is Si based, may not be able to meet the increasing demand for high speed devices. This has opened the door widely to the integration of the SiGe into bipolar technology, leading to the fabrication of Silicon Germanium (SiGe) heterojunction bipolar transistors (HBTs). This device exhibits high performance compared to Si bipolar junction transistors (BJTs). However, a continuous improvement of the SiGe HBT’s performance required an increase of the Ge content in the base. This is not possible, since the amount of the Ge that can be used in SiGe HBTs is limited by the magnitude of the strain that can be accommodated within the base region. Using a Strain Relaxed Buffer (relaxed SiGe) as a virtual substrate (in place of Si) can allow more Ge to be introduced in the base layer.

1.2 History and development of Si bipolar junction transistor

The transistor is a three terminal, solid state electronic device. In a three terminal device we can control electric current or voltage between two of the terminals by applying an electric current or voltage to the third terminal. The transistor was not the first three terminal device. The vacuum tube triode preceded the transistor by nearly 50 years. They played an important role in the emergence of home electronics and in the scientific discoveries and technical innovations which are the foundation for our modern electronic technology. The vacuum tube triode also helped push the development of computers. They were used in several different computer designs in the late 1940's and early 1950's (In the late 1940's, big computers were built with over 10,000 vacuum tubes and occupied over 93 square meters

of space). But the limits of these tubes were soon reached. As the electric circuits became more complicated, one needed more and more triodes. Engineers packed several triodes into one vacuum tube to make the tube circuits more efficient. The vacuum tubes tended to leak, and the metal that emitted electrons in the vacuum tubes burned out. The tubes also required so much power that big and complicated circuits were too large and the energy consumption rate was high. The problems with vacuum tubes lead scientists and engineers to think of other ways to make three terminal devices. Instead of using electrons in vacuum, scientists began to consider how one might control electrons in solid materials, like metals and semiconductors.

In 1947, scientists working at Bell Telephone Laboratories were trying to understand the nature of electrons at the interface between a metal and a semiconductor (Germanium). They realized that by making two point contacts very close to one another, they could make a three terminal device - the first "point contact" transistor [1]. Although the first fabricated transistor was made using Ge, we actually live in silicon world. Greater than 95% of the semiconductor market uses the semiconductor Silicon (Si). This profound market dominance of Si rests on a number of surprisingly practical advantages that Si has over the other numerous semiconductors, including [2]:

- An extremely high quality dielectric (SiO_2) can be grown on Si and used for isolation, passivation, or as an active layer (e.g., gate oxide).
- Si can be grown in very large, low defect single crystals, yielding many (low-cost) IC's per wafer.
- Si has good thermal properties allowing for the efficient removal of dissipated heat.
- Si can be controllably doped with both N and P type impurities.
- Si has excellent mechanical strength, facilitating ease of handling and fabrication.
- It is easy to make very low-resistance ohmic contacts to Si, thus minimizing device parasitic.
- Si is extremely abundant and easily purified.

Since the fabrication of the first Si bipolar junction transistor, there have a large number of innovations and break-throughs. Bipolar junction transistors were typically formed as follows (assuming an NPN device). A patterned N subcollector is first formed on a P-type

silicon wafer by diffusion. An N-type epitaxy layer is then grown on top. A P-type pocket for the base region is then formed by diffusion. This is followed by the formation of an N-type emitter. The P-type region directly underneath the emitter forms the intrinsic base, while the remainder of the P-type pocket forms the extrinsic base as shown in Figure 1.

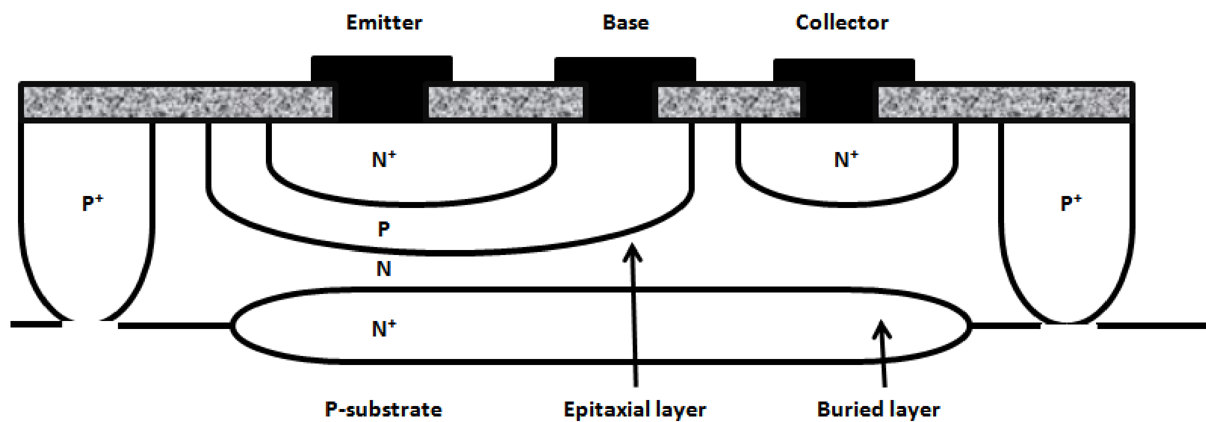

Figure 1: Cross-sectional view of a basic planar bipolar transistor

Typical emitter junction depth is about 500 nm, and typical intrinsic base width is about 250 nm [3]. The emitter and base region that are formed by the diffusion technique tend to be very wide, which slows down the device. However, the ion-implantation technique has allowed the production of narrow base and emitter regions [4]. Another development is the ability to grow a thin, heavily doped Si crystal epitaxially. High doping level means introducing more carriers which reduce of the base resistance and also the collector series resistance. The electrical isolation of the bipolar has also been subjected to some development. In the early stage, the device was junction-isolated using a P-type region. This region tends to be very large because the impurity diffuses laterally. For the isolation to be effective, the P-type region must completely surround the device. In addition, the isolation junction must be reversed biased by connecting the P-substrate to the most negative voltage in the circuit. Instead of using this method, which results in large isolation area, designers nowadays tend to use deep trench isolation. This method reduces the isolation area. The deep trenches are formed by first etching silicon trenches which are filled the trenches with oxide or a combination of oxide and polysilicon, followed by planarization using chemical-mechanical polishing [5].

The next stage of the evolution of Si bipolar transistor was the integration of the polysilicon emitter. The early experiments treated the heavily doped N-polysilicon as a metal. Perhaps the most exciting finding of these experiments was that the N polysilicon contacts to Si did not behave like ohmic contacts at all. Minority holes injected from the base into the shallow N type emitter, instead of recombining at the polysilicon-silicon interface, as expected for an ohmic contact, recombine primarily inside the N polysilicon layer, leading to significant increase in current gain [6]. The use of polysilicon was not limited to the emitter; P-type polysilicon is also used between the intrinsic base and the base contact. This actually reduces the extrinsic base area, therefore reducing the parasitic capacitance. However, this may cause an increase of the base resistance [7].

1.3 Impact of SiGe material on semiconductor technology

While silicon dominates in mainstream integrated circuit microelectronics, there are areas of analogue electronics, especially in high frequency applications, that have allowed GaAs, InP and other materials to dominate smaller niche markets such as radio frequency and power amplifiers [2]. If the performance of Si transistors or circuits could be improved by the addition of another semiconductor material then numerous new applications could be opened up. Silicon Germanium (SiGe) is one such material which may be epitaxially grown on silicon wafers and allows engineering of the bandgap, energy band structure, effective masses, density of state and mobilities while fabricating circuits using conventional Si processing tools [1]. SiGe has moved from being a research material to an important material that is used in the manufacturing of different semiconductor devices. A thin SiGe layer grown as the base of a bipolar transistor on a Si wafer leads to the fabrication of devices known as SiGe HBTs. The performance can be greatly improved over a normal Si bipolar junction transistor because the base can be doped to larger densities which reduces the resistivity of the base and hence the RC time constant for switching. The reduced base resistance is also important for reducing noise in the transistors, an important parameter in analogue and RF applications [8]. It is also important to mention that grading the Ge content in the base then builds an electric field into the device, which accelerates the carriers across the base and therefore increases the speed of the transistor [9]. The reduced bandgap of the base also leads to an increase in the gain of the transistor, as the minority carrier concentration is inversely proportional to the band gap.

The use of SiGe is widespread in CMOS technology. The continuous development of CMOS technology was achieved by shrinking the device dimensions. However this approach has also turned out to be increasingly difficult. Therefore considering other techniques, such as improving the carrier mobility becomes important. On any CMOS chip with both P and N type transistors, the major limitation in the performance is the PMOSFETs. The mobility and effective mass of holes is much worse than the mobility and effective mass of electrons in Si. To balance the current drive in CMOS circuit design, the N and P transistors have to be sized and this greatly reduces the circuit performance. The limitation caused by the low mobility of the holes in the Si can be mitigated using SiGe in the source and drain to compress the silicon channel [10]. Since The hole mobility in this latter is known to be high compared to unstrained Si. Tensile strained silicon improves electron mobility and is used in NMOSFETs. Strained Si is considered as one of the leading techniques for improving the mobility of carriers and therefore enhancing the performance of MOSFETs.

1.4 Project motivation

Bipolar technology has been subjected to a large number of innovations in recent decades. One of the most significant break throughs, which has allowed a continuous improvement of the bipolar transistor, is the implantation and epitaxial techniques that allow the fabrication of a thin base layer. Another development is the implementation of the polysilicon emitter, which blocks the diffusion of minority carriers in the emitter, therefore increasing the current gain. However, these successive achievements may not be sufficient to meet the continuous demand of high speed devices.

The recent improvement of epitaxial growth techniques has lead to the fabrication of SiGe HBTs. This device is formed using a thin SiGe layer in the base region instead of Si, which is found in Si bipolar transistors. The small band-gap of SiGe results in an exponential increase of the minority carrier concentration in the base and therefore the collector current. The profile of the Ge concentration in the base can be constant. However it is also possible to be linear, leading to the formation of triangular or trapezoidal profiles. These profiles give rise to a drift field in the base region which aids the minority carrier transport through the base, therefore increasing the speed of the device. Many papers report that the performance of the SiGe HBT is proportional to the Ge content in the base; however increasing the amount

of the Ge is not an endless process. The grown layer of SiGe on Si substrate is under strain. An increase of the Ge content raises the amount of strain in the SiGe. The final result would be the formation of defects and relaxation of the SiGe layer. If these defects are in the active region of the wafer where the transistors are fabricated, they will often lead to a device failure. This is a clear barrier toward the improvement of SiGe HBTs.

In order to improve the performance of SiGe HBTs, it is important to increase the Ge content in the base, while keeping the strain below a certain critical level. This can be achieved using a SiGe Strain Relaxed Buffer as a virtual substrate. In this case, the difference of the lattice constant between the base and collector is small which reduces the strain in the base. Therefore, the structure of the new device is as follows: relaxed SiGe in the collector compressed SiGe in the base and strained Si in the emitter. This device is called a strained Si HBT (sSi HBTs), Figure 2.

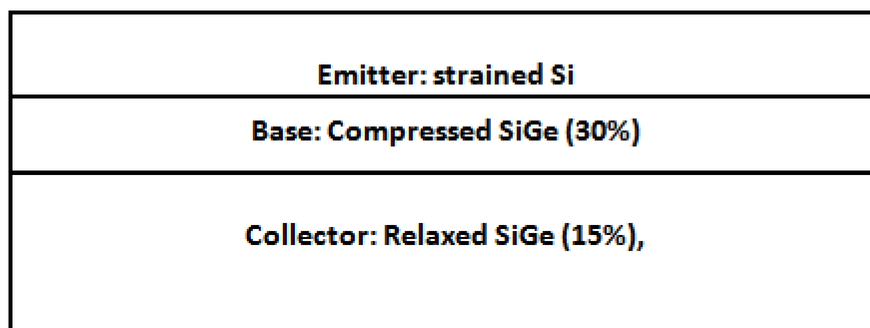

Figure 2: different layer forming sSi HBTs, The Ge composition values given here are indicative for a typical device.

The Strain Relaxed Buffer (SRB) has also been used in the fabrication of strained Si MOSFETs[11]. Current BiCMOS technology consists of the integration of SiGe HBTs and conventional MOSFETs. Using relaxed SiGe virtual substrates in the fabrication of sSi HBTs has raised the possibility of the integration of strained Si MOSFETs and sSi HBTs in one chip.

The dissertation is broken up into four sections:

- The basic equations that govern the operation of Si BJTs are developed. The impact of the implementation of SiGe into bipolar technology is also presented along with the properties of SiGe material.
- Several experimental data (SIMS, TEM image, EELS and the Raman spectroscopy) are presented to confirm the fabrication of sSi HBTs. The Si BJTs, SiGe HBTs and sSi HBTs

are compared in term of current gain. This comparison shows that this novel device exhibits a maximum current gain of 3700 compared with 334 for co-processed SiGe HBTs and 135 for Si BJTs. The common emitter characteristic has also shown that sSi HBTs suffers from the self heating.

- 2D simulation of Si BJTs, SiGe HBTs and sSi HBTs is presented. MEDICI from Synopsys is used due its ability to consider the impact of the Ge content on the material properties and therefore on the device performance. An agreement between the experimental data and the simulation results is reported. This confirms that the band gap of the base layer is the main factor that causes the high performance of sSi HBTs. An investigation of the performance of HBTs based on Ge and GaAs is also reported showing that this device might have a good current gain. However the band discontinuity and more precisely the valence band discontinuity blocks this device from reaching its full potential.
- The first comparison study of low frequency noise between sSi HBTs, SiGe HBTs, and Si BJTs is presented. This has shown that sSi HBTs exhibit higher low-frequency noise compared to control devices at fixed base current. The presence of a high concentration of defects that are caused by the strain-relaxed buffer is responsible for the low-noise performance of sSi HBTs. However, it is shown that this novel device demonstrates the lowest noise level (better noise performance) for the same collector current compared with the other control bipolar devices. The noise level in a circuit can therefore be reduced by using sSi HBTs as compared with either Si BJTs or SiGe HBTs. This results the high current gain of these devices. A relationship between low frequency noise and defects is shown by material characterization.

1.5 Conclusion

This chapter presents a summary of the development of bipolar technology. The performance of Si BJTs has improved significantly as a consequence of using novel designs and fabrication methods such as implantation and epitaxy. This chapter has also discussed the impact of SiGe on the bipolar transistor and also on CMOS technology. The limited amount of strain that can be accommodated in the SiGe base layer is seen as a real barrier to enhance the performance of HBTs. The SRB that is used as a substrate in the fabrication of strained Si MOSFETs is seen as a possible solution to the limitation of SiGe HBTs.

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Chapter 2. Background

2.1 Introduction

Most semiconductor devices contain at least one PN junction. This junction is fundamental to the performance of functions such as rectification, amplification, switching and other operations in electronic circuits. Two physical phenomena are responsible for the flow of the current in the PN junction, drift and diffusion. Determining the basic equation that governs this junction is the first step to understand the operation of bipolar transistors.

The current gain and the cut-off frequency are the main parameters used to characterise the bipolar transistor. While the first parameter is viewed as the factor that reflects the DC performance of the device, the second characterises the speed of the device. The doping level in the emitter, base and collector in addition to the width of these regions represent the parameter design space that is used to enhance the device performance. However, increasing both the DC and AC performance leads to a conflict of parameter design space requirement. For instance, low base doping increases the current gain, however this results in a reduction of the base resistance and by consequence the cut-off frequency. This means that Si BJTs may not able to meet the continuous demand of high speed devices for the communication market. This has opened the door to the use new innovation methods to improve the performance of Si BJTs. The incorporation of SiGe in the fabrication of the bipolar transistor has lead to a new device known as the SiGe heterojunction bipolar transistors. This latter device has shown high DC and AC performance over Si BJTs. The impact of SiGe is not restricted to bipolar transistors. Indeed it improves the performance of MOSFETs and BiCMOS technology as well.

2.2 PN junction

A bipolar transistor is simply two back-to-back PN junctions. Hence it is important to study the electrical characteristic of this junction. One useful feature of the PN junction is that the current can only flow quite freely from the P to N direction when the P region has a relatively positive external voltage relative to N. This asymmetry of the current flow makes the PN junction very useful as a rectifier. When N and P region are brought together to

form the PN junction, diffusion of carriers takes place because of large carrier concentration gradients at the junction. Thus holes diffuse from the P side into the N side, and electrons from the N side into the P side as seen in Figure 2.1.

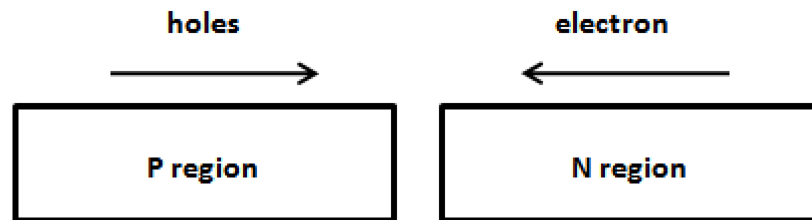

Figure 2.1: Separate P and N region and the direction of hole and electron diffusion current.

The resulting diffusion current cannot build up indefinitely, however, because an opposing electric field is created at the junction. Consider that electrons diffusing from N to P leave behind uncompensated donor ions N_d^+ in the N material, and holes leaving the P region leave behind uncompensated acceptors N_a^-, it is easy to visualise the development of a region of positive space charge near the N side of the junction and negative charge in the P side. The resulting electric field ε is directed from the positive charge toward the negative charge. Thus ε is in the direction opposite to that of diffusion current for each type of carrier. Therefore, the field creates a drift component of current from N to P, opposing the diffusion current. Figure 2.2 illustrates a PN junction with the neutral regions of P type and N type material and also the depletion region (space charge).

The equilibrium state of the PN junction can be disturbed when applying an external voltage to it. There are two distinctive biasing conditions: one is the forward bias and the other is the reverse bias. In the first case the minority carriers are injected into P and N region. The injected carriers are supplied by the reservoir of the majority carriers, which in turn are supplied by the external voltage source. In the reverse biased case, the minority carriers are extracted from P and N region due to the enhanced electric field, leading to a small current. This current is reduces as the reverse biased is increases.

However, a very small reverse current does flow. This reverse saturation current depends only on the thermal generation of holes and electrons near the junction. This reverse saturation current is quite small but it increases with increasing temperature.

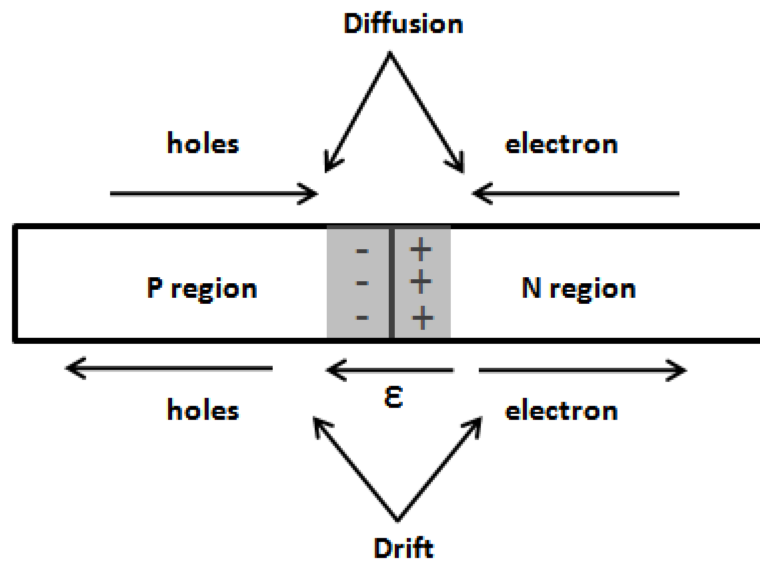

Figure 2.2: PN junction, direction of the hole and electron current (drift and diffusion)

The density of charge carriers is characterised by the Fermi level E_F. A change of the Fermi level, e.g. towards the conduction band, causes electron density to increase and hole density to decrease. Equation (2.1) and (2.2) represents the electron and hole density, respectively.

$$n = n_i \exp\left[\frac{(E_{Fn} - E_i)}{kT}\right] \quad (2.1)$$

$$p = n_i \exp\left[\frac{(E_i - E_{Fp})}{kT}\right] \quad (2.2)$$

Where n_i is the intrinsic carrier concentration, E_i is the intrinsic Fermi level, E_{Fn} and E_{Fp} is the electron and hole quasi Fermi level, respectively. Figure 2.3 illustrate the band structure of P and N-type doped semiconductor.

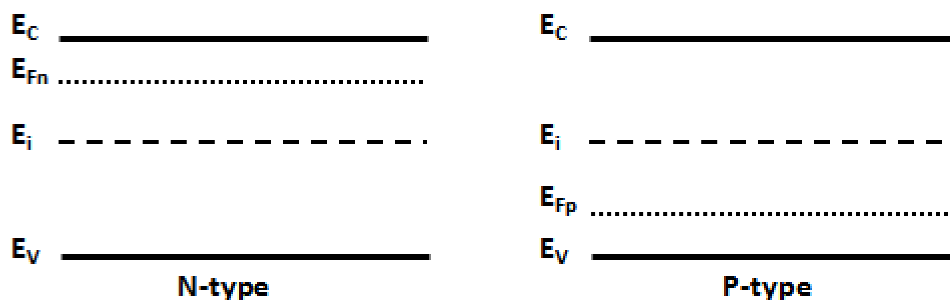

Figure 2.3: Band structure of P and N-type doped semiconductor.

The product of equation (2.1) and (2.2) equation leads to equation (2.3) of the product pn

$$pn = n_i^2 \exp\left[\frac{(E_{Fn} - E_{Fp})}{kT}\right] \tag{2.3}$$

Applying this product to the edges of the depletion region (at the position X_n and X_p) leads to the following equations.

$$p_n(X_n)n_n(X_n) = p_p(X_p)n_p(X_p) = n_i^2 \exp\left(\frac{qV}{kT}\right) \tag{2.4}$$

Where V is the voltage across the PN junction, q is the electronic charge, p_n and n_n are the hole and electron concentration in the N region, respectively. While n_p, p_p are the electron concentration in the P region, respectively. It is important to mention that this product increases at forward. Figure 2.4 illustrates minority carrier distributions on the two sides of the PN junction for forward bias.

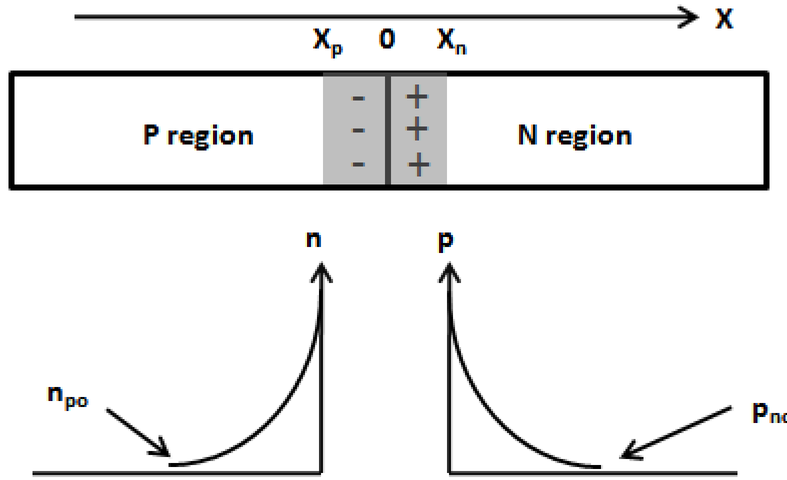

Figure 2.4: Distribution of the minority carrier under forward bias

The minority carrier concentration at the edge of the depletion region is higher than at equilibrium. For low injection of minority carries we can neglect changes in the majority carrier concentrations. Therefore it is possible to write:

$$n_n(X_n) = n_{no} \tag{2.5}$$

where, n_{no} is the electron concentration in the N region (at equilibrium). Similarly:

$$p_p(X_p) = p_{po} \tag{2.6}$$

Where, p_{po} in the hole concentration in the P region (at equilibrium).

At equilibrium (No external voltage), equation (2.4) can be written as follow

$$p_{no}n_{no} = p_{po}n_{po} = n_i^2 \tag{2.7}$$

Where, p_{no} is the hole and electron concentration in the N region (at equilibrium) and n_{po} is the electron concentration in the P region (at equilibrium).

By considering equation (2.4), (2.5) and (2.7), it is possible to develop an equation for the electron concentration in the P region at the position X_p as follows:

$$n_p(X_p) = n_{po} \exp\left(\frac{qV}{kT}\right) \tag{2.8}$$

Similarly, using equation (2.4), (2.6) and (2.7) the hole concentration in the N region at the position X_n is given by the following equation.

$$p_n(X_n) = p_{no} \exp\left(\frac{qV}{kT}\right) \tag{2.9}$$

It is important to mention that equation (2.8) and (2.9) are developed under certain assumptions. The externally applied voltage appears totally across the immediate junction, therefore all parasitic resistances and associated voltage drops due to the current flow were assumed to be negligible. Moreover, the generation recombination phenomenon is considered negligible.

The majority carrier current from one side of the PN junction is the minority carrier current on the other side of the junction. The total current flow can therefore be found by simply adding the two minority diffusion currents:

$$I = I_n + I_p \tag{2.10}$$

Where I_n is the electron diffusion current and I_p is the hole diffusion current. Since the current is caused by the diffusion of the carriers, therefore the total current can be written as follow.

$$I = -qAD_p \frac{dp_n}{dx} + qAD_n \frac{dn_p}{dx} \tag{2.11}$$

Where q is the electronic charge, A is the cross-section of the junction, D_p and D_n are the hole and electron diffusivity, respectively. Taking in consideration the gradients from Figure 2.4 and substituting equation (2.8) and (2.9) into equation (2.11) gives the current voltage relationship of the PN junction.

$$I = qAD_p \frac{p_{no}}{W_n}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] + qAD_n \frac{n_{po}}{W_p}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2.12}$$

Where W_p and W_n are the width of the P and N region, respectively.

The above equation can be rearranged in a simple form

$$I = qA[D_p \frac{p_{no}}{W_n} + D_n \frac{n_{po}}{W_p}][\exp(\frac{qV}{kT}) - 1] \quad (2.13)$$

If the N region width W_n is large compared to the hole diffusion length L_P and the P region width W_p is large compared to the electron diffusion length L_n. Then W_n should be replaced by L_p and W_p by L_n. According to this, the equation (2.13) can be rewritten as follows:

$$I = qA[D_p \frac{p_{no}}{L_p} + D_n \frac{n_{po}}{L_n}][\exp(\frac{qV}{kT}) - 1] \quad (2.14)$$

The thermal voltage at room temperature (300 K) is 0.0259 V. In practice the applied voltage in the forward mode is higher than 0.7 V, therefore the term -1 is very small compared to exp (qV/kT) and it is reasonable to eliminate it (2.15).

$$I = qA[D_p \frac{p_{no}}{W_n} + D_n \frac{n_{po}}{W_p}][\exp(\frac{qV}{kT})] \quad (2.15)$$

In the reverse mode the term exp (qV/kT) becomes very small compared to -1, therefore equation (2.13) can be simplified to equation (2.16).

$$I = -qA[D_p \frac{p_{no}}{W_n} + D_n \frac{n_{po}}{W_p}] \quad (2.16)$$

The above equation was derived assuming no generation of carriers in the depletion layer. In an actual device, the thermal generation of carriers in the depletion layer should be taken into consideration. The current due to thermal generation ($I_{R\text{-}G}$) increases with the width of the depletion layer W, which increases with the applied reverse bias. So, an $I_{R\text{-}G}$ increase as reverse voltage is increased. Equation Figure 2.19 illustrates the thermal generation current.

$$I_{R-G} = -\frac{qAn_iW}{2\tau_o} \quad (2.17)$$

Where

$$\tau_o = \frac{\tau_p + \tau_n}{2} \quad (2.18)$$

τ_p and τ_n are the hole and electron life time.

High current will pass through the diode when the applied voltage is equal (or higher than) the break down voltage of the PN junction. The current-voltage equation (2.16) does not obviously reflect this behaviour, because the break down phenomenon was not taken into consideration when developing this equation.

Figure 2.5 represents the current voltage relationship for PN junction.

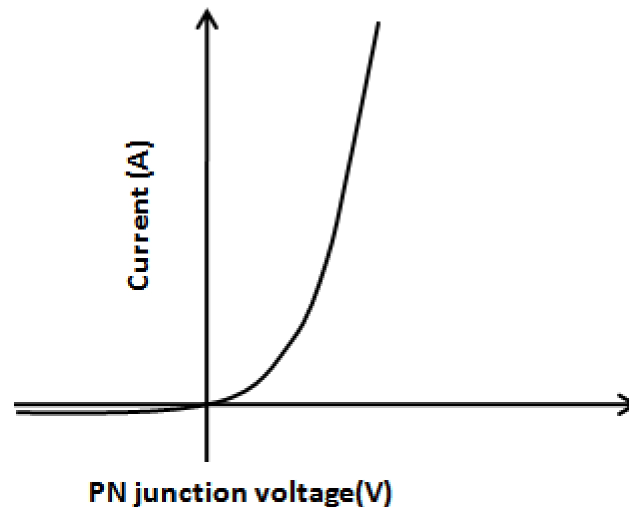

Figure 2.5: Current-voltage characteristic for PN junction

2.3 Basic operation of the Si BJTs

In order to use a bipolar transistor in a practical circuit, external bias must be applied to the emitter-base junction and collector-base junction. These two junctions provide four possible bias configurations. The forward active mode (The emitter-base junction is forward biased while the collector base is reversed biased) is the most useful arrangement. This is because in this configuration the gain of the transistor can be exploited to produce current amplification [1].

In the forward biased emitter-base junction, holes are injected into the N region (emitter) which form a minority (hole) carrier gradient. This causes a diffusion of holes and gives rise to the main component of base current. Meanwhile electrons are injected into the P base region. Some injected electrons recombine with holes in the base, but the majority diffuse through the base. Since the base-collector junction is reversed biased, these electrons are extracted from the base to the collector region forming the collector current. To have a good n-p-n transistor, it is preferable that almost all the electrons injected by the emitter into the base should be collected, thus the P type region should be narrow, and the hole life time should be long [2].

Figure 2.6 illustrates the minority carrier distribution, this figure shows that the diffusion of holes in the emitter is the source of the base current, while the diffusion of the electrons in

the base gives rise to the collector current. Consequently, it is possible to use equation (2.15) to write the base and collector current equations as follows:

$$I_C = -I_n = \frac{qAD_{nb}n_{iB}^2}{N_a W_B} \exp\left(\frac{qV_{BE}}{kT}\right) \tag{2.19}$$

Where $D_{nb}$the electron diffusivity in the base is, n_{iB} is the intrinsic carrier concentration in the base region.

$$I_B = -I_p = \frac{qAD_{pe}n_{iE}^2}{N_E W_E} \exp\left(\frac{qV_{BE}}{kT}\right) \tag{2.20}$$

Where $D_{pe}$the electron diffusivity in the emitter is, n_{iE} is the intrinsic carrier concentration in the emitter region.

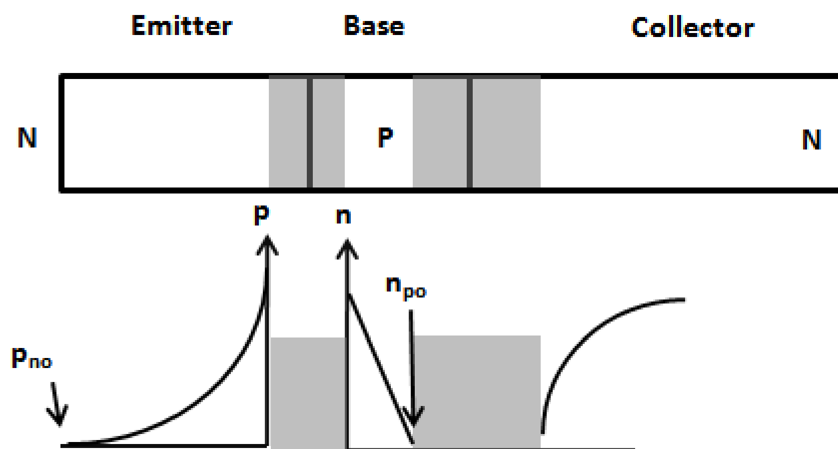

Figure 2.6: minority carrier distribution in the emitter and base region (the base-emitter region is forward biased).

In practice however, the collector and base currents do not follow equation (2.19) and (2.20) at low and high base emitter voltage. Figure 2.7 represents the theoretical and the experimental Gummel plot (collector and base current).

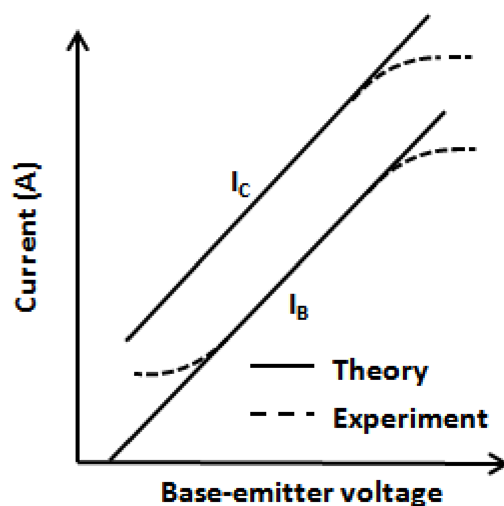

Figure 2.7: comparison between the experimental and theoretical Gummel plot.

The first information to emerge from this comparison is the base current is usually higher than in the theoritical case at low base-emitter voltage. Moreover, both base and collector currents show a reduction at high voltage. The behaviour of the base current at low voltage, which exhibits an exp (qV/mkT), where $1<m\leq2$ dependence is caused by the recombination current in the depletion region as well as the extrinsic base. The parameter m is known as the ideality factor and it is equal to 1 in the case of pure diffusion current. The amount of deviation of the base current from the ideal behaviour depends strongly on the transistor structure, device structure and fabrication process. This parameter actually determines the physical properties of defects such as their position in the band gap, the concentration and the position in the device. This behaviour is widely known, not only in BJTs but also in HBTs using different material i.e. [Si/SiGe], [AlGaAs/GaAs] and [InGaP/GaAs] [3, 4].

Figure 2.8 represents a schematic diagram illustrating the series resistance in a bipolar transistor.

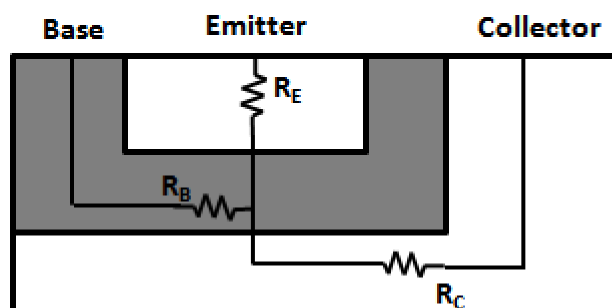

Figure 2.8: Schematic illustrating the series resistance in bipolar transistor.

The modelling study that has been carried out earlier has ignored the impact of the series resistance, and it assumed that all external voltage actually appears across the PN junction [5]. This can be a good approximation only at low voltage. The influence of the series resistances on the transistor currents can be understood from the circuit diagram in Figure 2.9. The external connections to the transistor are the terminals C, B, and E, whereas the internal terminals of the ideal transistor that we have been discussing so far are the terminals C', B' and E'.

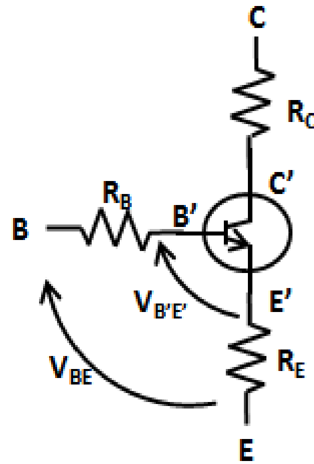

Figure 2.9: Circuit diagram showing internal collector, base and emitter series resistance

The relationship between the internal and external base-emitter voltage can be derived using Kirchoff's law:

$$V_{B'E'} = V_{BE} - I_B R_B - I_E R_E \tag{2.21}$$

$$V_{B'E'} = V_{BE} - I_B R_B - (I_C + I_B) R_E \tag{2.22}$$

$$V_{B'E'} = V_{BE} - I_B R_B - I_B R_E (1 + \beta) \tag{2.23}$$

Equation (2.23) shows that the voltage across the emitter-base junction $V_{B'E'}$ is actually smaller than the external base–emitter voltage V_{BE}. Considering this result, the base and collector current can be written as follow:

$$I_C = \frac{qAD_{nb}n_i^2}{N_a W_B} \exp\left[\frac{q\left(V_{BE} - I_B R_B - I_B R_E(1+\beta)\right)}{kT}\right] \tag{2.24}$$

$$I_B = \frac{qAD_{pe}n_i^2}{N_E W_E} \exp\left[\frac{q\left(V_{BE} - I_B R_B - I_B R_E(1+\beta)\right)}{kT}\right] \quad (2.25)$$

Considering the series resistance, the base and collector current given by equation (2.24) and (2.25) are smaller that the given by equation (2.19) and (2.20).

2.4 Current gain

The current gain represents an important parameter to characterise the DC performance of a bipolar transistor. It is given by the ratio of the collector current to the base current. Using equation (2.19) and (2.20) the current gain is

$$\beta = \frac{I_C}{I_B} = \frac{D_{nb} W_E N_d}{D_{pe} W_B N_a} \quad (2.26)$$

According to the equation above, the current gain is independent of the applied voltage. However, this is not the case in practice where the current gain is lower at low and high voltage. This is because of the behaviour of the base current and also of the collector and base current at high voltage. The behaviour of the current gain at low voltage can be predicted using the equations of the base and collector current. As was mentioned earlier, the ideality factor of the base current at low base-emitter voltage is generally higher than 1. Therefore it is acceptable to rearrange equation (2.20) to form the following equation:

$$I_B \propto \exp\left(\frac{qV_{BE}}{mkT}\right) \quad (2.27)$$

Where m is the ideality factor. In this case, the current gain is not independent of the voltage as shown by the following equation.

$$\beta = \frac{I_C}{I_B} \propto \frac{\exp\left(\frac{qV_{BE}}{kT}\right)}{\exp\left(\frac{qV_{BE}}{mkT}\right)} \quad (2.28)$$

The above equation can be simplified.

$$\beta = \frac{I_C}{I_B} \propto \exp\left[\left(\frac{qV_{BE}}{kT}\right)\left(1 - \frac{1}{m}\right)\right] = I_C^{\left(1-\frac{1}{m}\right)} \quad (2.29)$$

Figure 2.10 represents a comparison between the experimental and theoretical current gain, which shows that the current is lower at low and high voltage.

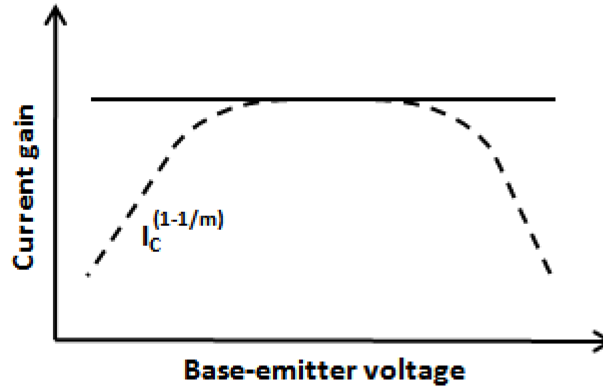

Figure 2.10: comparison between the experimental and theoretical current gain.

The low current gain at the high base emitter voltage is caused by the deviation of the base and collector current from the ideal behaviour in this region.

Equation (2.26) illustrates the main design requirement of a bipolar transistor. In particular, the ratio N_d/N_a is of great importance. In order to increase the current gain, the emitter doping should be as high as possible. Meanwhile the base doping should be as low as possible. However both strategies have drawbacks. In the case of emitter doping, high doping will cause the band gap narrowing phenomenon. High doping concentration can perturb the perfect periodicity of the semiconductor and reduce its band gap. The intrinsic carrier concentration in this case is subjected to some changes as suggested by the following equation

$$n_{ie}^2 = n_i^2 \exp\left({}^{\Delta E_{G,H}}/_{2kT}\right) \qquad (2.30)$$

where n_i is the intrinsic carrier concentration at low doping levels, n_{ie} is the intrinsic carrier concentration at high doping level and $\Delta E_{G,H}$ is the band gap narrowing caused by doping. A simple way of modelling the band gap narrowing in the emitter is through an effective doping concentration in the emitter N_{deff} as reported by Kumar et al [6].

$$N_{deff} = N_d \frac{n_i^2}{n_{ie}^2} = N_d \exp\left({}^{-\Delta E_{G,H}}/_{2kT}\right) \qquad (2.31)$$

The above equation clearly indicates that the band gap narrowing has the effect of reducing the current gain.

The resistance of a semiconductor bar with length L and cross-section A is given by the following equations:

$$R = \frac{1}{q(\mu_n n + \mu_p p)} \frac{L}{A} \tag{2.32}$$

Where μ_n is the electron mobility, μ_p is the hole mobility, n is the electron concentration and p is the hole concentration. Equation (2.32) shows that a reduction of the doping will decrease the hole or the electron concentration, which will lead to an increase of the resistance. Therefore, reducing the base doping to raise the current gain will cause an increase of the base resistance. This drop of the base resistance reduces the switching speed of the bipolar transistor. The base resistance combined with parasitic capacitance form an RC time constant which slow down the device. This impact can be seen clearly in equation (2.33).

$$f_{max} = \sqrt{\frac{f_t}{8\pi C_{jc} R_B}} \tag{2.33}$$

Where f_{max} is the maximum oscillation frequency, f_t is the cut-off frequency, C_{jc} is the base-collector depletion capacitance and R_B is the base resistance. So there is a clear conflict between the requirements for high speed and high current gain.

Another strategy that can be used to boost the current gain, is increasing the emitter depth and reducing the base width. The first option will lead to an increase of the emitter transit time as suggested by equation (2.34). This is extremely important parameter since it affects the speed of the device.

$$\tau_E = \frac{W_E W_B}{2D_{nb}} \tag{2.34}$$

Therefore, when designing a high speed bipolar transistor it is necessary to have a small emitter depth. The second option, which is reducing the base width, poses two issues. From the fabrication point of view it is difficult to fabricate a very thin base layer. This is because of the boron out-diffusion issue. The punch-through is an issue that may occur when having a very thin base layer. In the common emitter configuration, the emitter-base junction is forward biased. When the base-collector junction is reversed biased, this will increase the width of the depletion region of this junction. In the limit, this depletion region (collector-base) could extend across the whole width of the base and join up with the emitter-base depletion region [7]. In this case, the emitter and collector are connected together by a

single depletion region as illustrated in Figure 2.11. A large current will flow between the emitter and the collector which causes the device to fail.

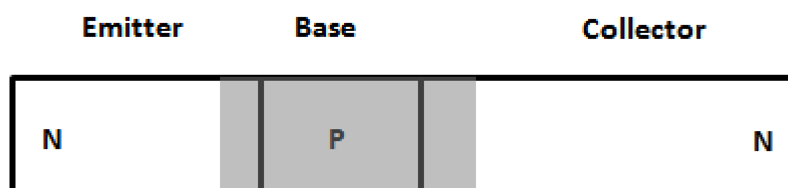

Figure 2.11: Schematic illustration of a bipolar transistor operating in punch through.

The above discussion about the current gain has shown that there is a conflict in design requirements between high current gain and high speed devices. In order to boost both DC and AC performance of the device, a new approach needs to be applied.

2.5 Epitaxial growth of silicon-germanium material

The possibility to combine the low cost advantages of the Si-technology with the high performance nature of III-V or II-VI heterostructures is believed to improve silicon-based heterostructures devices [8]. The lattice mismatch between the lattice constant of Ge and Si which is 4.17 % has allowed the possibility to epitaxially grow strained SiGe layers on Si [9]. For many applications of lattice mismatched materials the use of Vegard's law is practical. This law expresses the linear interpolation of the lattice constant of alloys as a function of parameter x defining the chemical composition of the alloy (compound). For a binary compound $Si_{1-x}Ge_x$ Vegard's law has the form

$$a_{SiGe} = a_{Si}(1 - x) + a_{Ge}x \quad (2.35)$$

Where a_{Si}, a_{Ge} and a_{SiGe} are the lattice constant of Si, Ge and $Si_{1-x}Ge_x$, respectively. However, frequently a deviation from Vegard's law has to be considered for more exact analysis [10]. A systematic investigation of $Si_{1-x}Ge_x$ thin film lattice properties as a function of the Ge content shows that the SiGe lattice constant can be fit by a parabolic relationship of the form [11]

$$a_{SiGe} = 0.002733\,x^2 + 0.01992\,x + 0.5431 \quad (2.36)$$

where the lattice constants are expressed in nm

when the SiGe is deposited on a Si substrate, the mismatch may be accommodated in one of two ways [12]:

- The lattice mismatch strain can be accommodated by a tetragonal distortion of the unit cell in the epitaxial layer. So that SiGe lattice constant fits to the Si lattice constant as illustrated in Figure 2.12 (A). In this case the SiGe layer is under compressive stress. This growth is perfect for the fabrication of the SiGe HBTs.
- Another mechanism for strain relaxation in thicker epitaxial layers is the introduction of misfit dislocations, which allows the epitaxial layer to relax toward its free lattice parameter trough the formation of misfit dislocation as illustrated in Figure 2.12 (B). This latter are basically where there is a missing or dangling bond in the lattice between two layers.

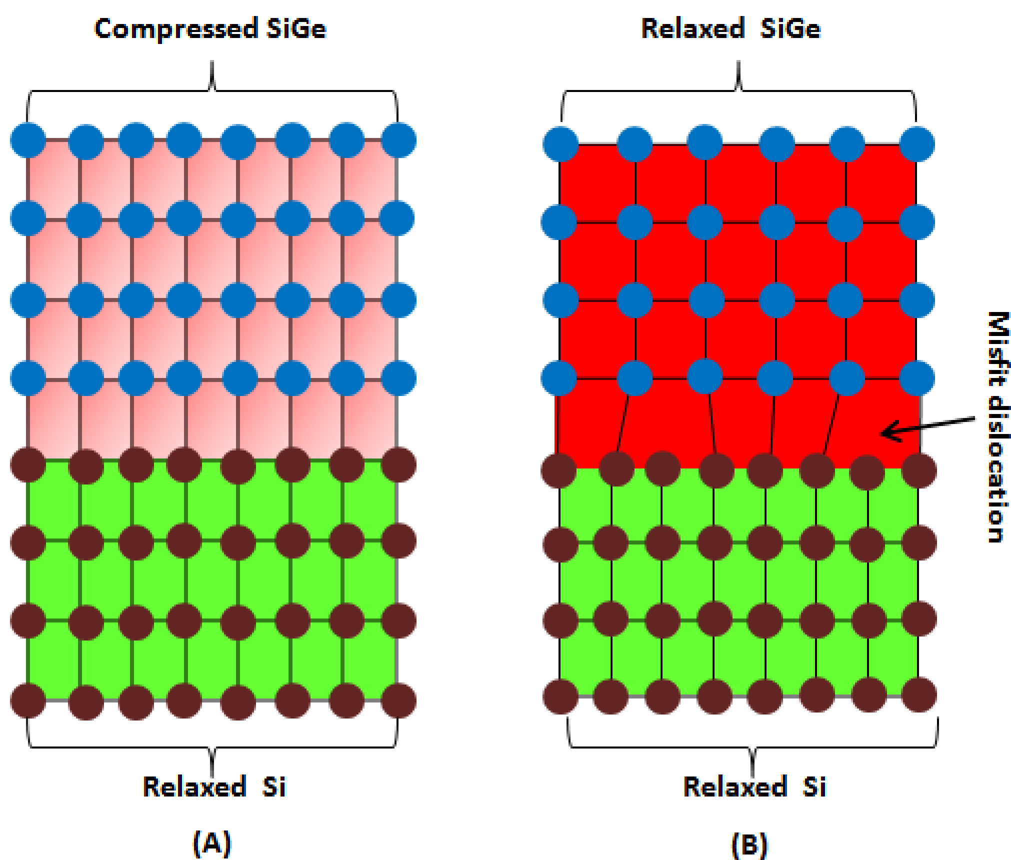

Figure 2.12: Schematic illustration of compressed (A) and relaxed SiGe (B).

The misfit dislocation can thread to the surface and lead to the threading dislocations as shown in the Figure 2.13.The grown SiGe in this case is relaxed, it is known as strain relaxed buffer (or virtual substrate). It is used to grow strained Si to enhance the mobility for MOSFETs technology. This work presents the first implication of strained relaxed buffer in bipolar technology. The existence of the misfit dislocations and threading dislocation represent the main problem with this system [13, 14]. The relaxation of the grown SiGe

layer take place only when its thickness is higher than specific thickness called the critical thickness.

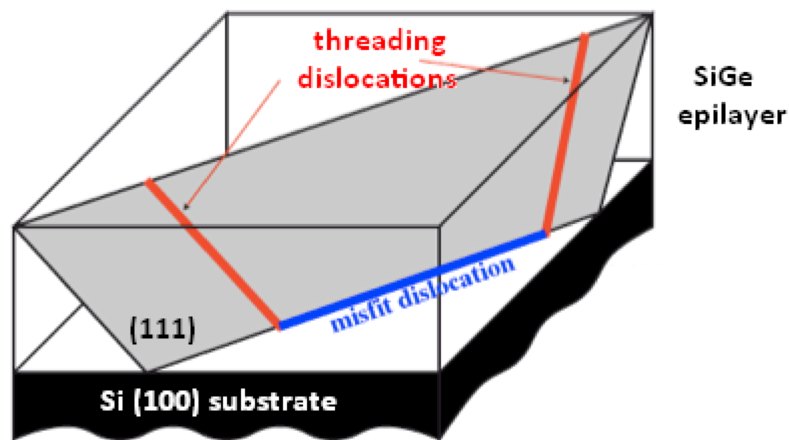

Figure 2.13: Misfit and threading dislocation in Si/SiGe heterostructure [15].

There has been much debate on the determination of the value of the critical thickness. Van der Merwe introduced the concept of critical thickness based on equilibrium theory. He defined critical thickness as the film thickness below which it was energetically favourable to contain the misfit by elastic energy stored in the distorted crystal [12]. Figure 2.1 illustrates the critical thickness.

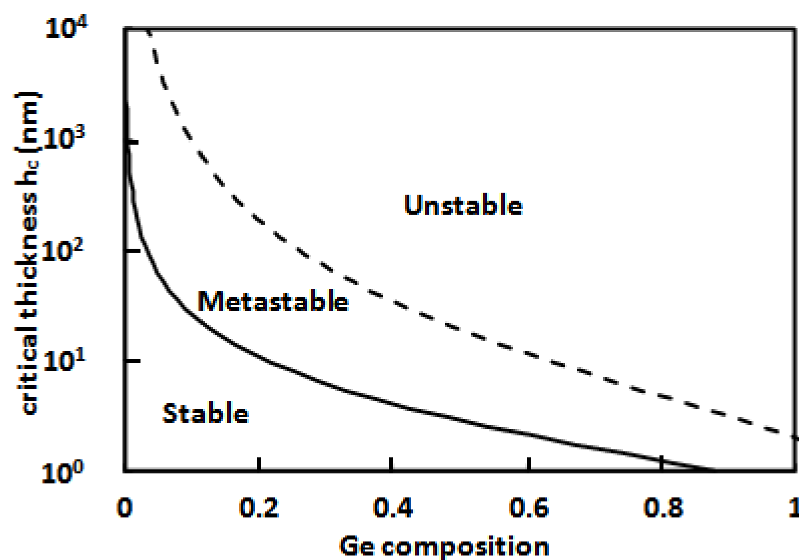

Figure 2.14: Critical thickness of the SiGe layer [12].

The most important information to emerge from this data is that the critical thickness decreases with the increase of the Ge content. This is because the increase of the Ge content raises the lattice constant and therefore reduces the lattice mismatch between the

Si substrate and the SiGe. The final result is that the strain increases within the SiGe layer. It is important to keep the thickness of the SiGe leyer well under the critical thickness when designing a device based on SiGe herostructures. This is because the relaxation of the SiGe means the formation defects. If these defects are in the active region of the wafer where the transistors are fabricated, they will often lead to a device failure. These failures can be caused directly by the electronic states associated with the defects which leads to excessive leakage. Failure may also be less direct. During processing, the defects may trap other impurities in the wafer that contribute to these electronic states. This might also lead to excessive impurity diffusion during the processing which can change the physical structure of the transistor [16].

2.6 Band gap structure of the Si/SiGe structure

The 4.17% lattice mismatch between Si and Ge has been exploited in a variety of pseudomorphic Si/SiGe heterostructure. Either Si or SiGe, is strained to match the lattice constant (parallel to the interface plane) to that of the unstrained substrate material, SiGe or Si respectively. The lattice constant perpendicular to the interface also changes to compensate for this lateral strain in the active material. There are two main configurations of Si/SiGe heterostructure as illustrated in Figure 2.15. For the SiGe HBTs the configuration (A) is the important [17].

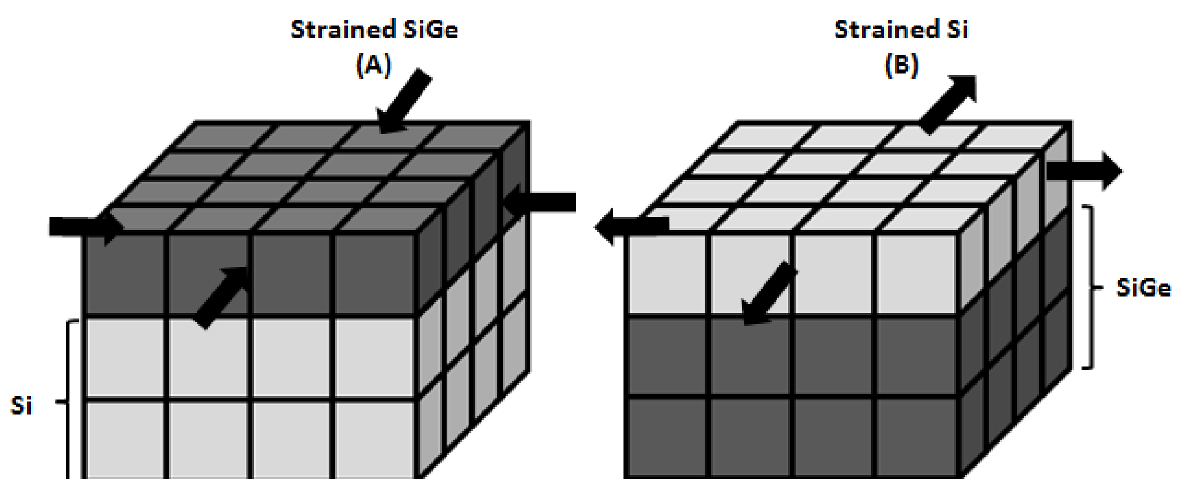

Figure 2.15: Schematic of the Si/SiGe heterostructure. Configuartion (A): strained SiGe on Si, Configuartion (B): strained Si on SiGe.

Since Ge has a significantly smaller bandgap than Si (primarily due to its larger lattice constant), it is not surprising that the bandgap of SiGe will be smaller than that of Si. The

strain in a pseudomorphic SiGe alloy, however, also plays an important role in shaping the final band alignment [11]. Figure 2.16 illustrates the band gap of strained and relaxed SiGe versus the Ge content.

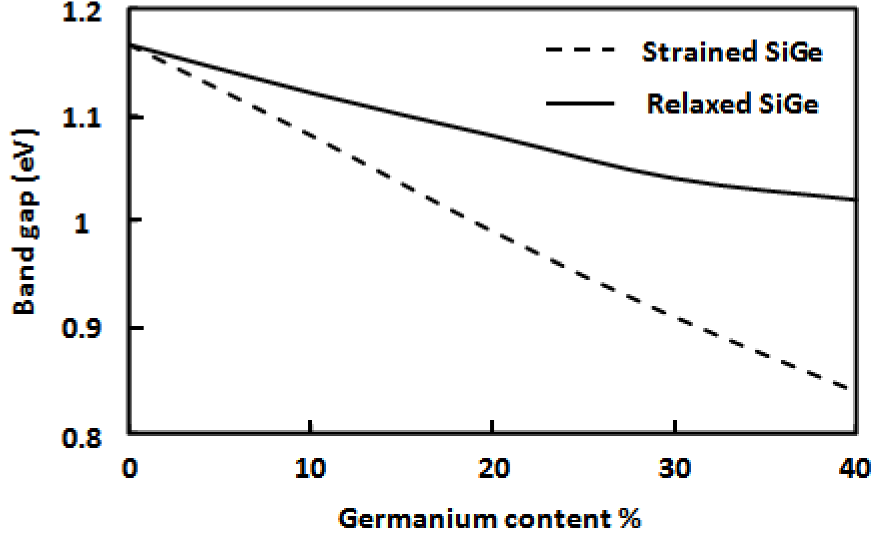

Figure 2.16: Band gap as function of relaxed and strained SiGe.

It can be seen that in addition to the Ge content, the strain has a dramatic effect on the band-gap of SiGe. The variation of the band-gap of SiGe (at low temperature 4.2 K) with the Ge content can be described by the following empirical equation developed by Weber et. Al [18].

$$E_g(x, 4.2K) = 1.155 - 0.43\,x + 0.206\,x^2 \qquad (x < 0.85) \tag{2.37}$$

To estimate the $Si_{1-x}Ge_x$ band gap at higher temperatures, the relationship of temperature with the band gap of Si as shown below [17]:

$$E_g(x, T) = E_g(x, 0K) - \frac{4.73 \times T^2 \times 10^{-4}}{T + 636} \qquad (x < 0.85) \tag{2.38}$$

This reduction of the band-gap is clearly key to the importance of SiGe in the design of SiGe HBTs. The equation (2.39) represents the widely accepted expression of the collector current for SiGe HBTs. This equation shows that a reduction of the band gap corresponds with an exponential increase of the collector current.

$$I_C = qA\exp\frac{qV_{BE}}{KT}\left[\frac{D_{nb}N_{CB}N_{VB}}{W_B N_a}\right]\exp\left[\frac{-E_g}{KT}\right] \tag{2.39}$$

Where q is the electronic charge, A is the device area, D_{nb} is the diffusion coefficient of electron in the base (SiGe layer), W_B is the base width, N_{ab} is the base doping, V_{BE} is the

base-emitter voltage, k is Boltzmann's constant, N_{CB} and N_{VB} are the density of state in the conduction band and the density of state in the valence in the base layer, respectively and E_g is the band gap of the base layer. This equation also shows that the determination of the band gap plays a crucial role in the determination of the performance of the device.

There have been many investigations into the bandgap of pseudomorphically grown strained SiGe on a relaxed Si substrate, based on the performance of SiGe HBTs [19]. To extract the bandgap of the strained SiGe and doped SiGe three ways may be used. The first possibility is to measure I_C at room temperature and to make reasonable assumptions for D_{nb}, N_C and N_V in strained SiGe. With the help of a proper knowledge of the base width and doping density, which can be extracted using SIMS data, it is then possible to calculate the bandgap Eg [19]. This is the first way to determine Eg over the Ge content. The second way [19] is to make use of the temperature dependence of I_C. For this, it is necessary to know the temperature dependence of D_{nb} in P type SiGe at the same doping concentration used in the transistor. Using this method one has to assume similar temperature dependences of the densities of states and Eg in SiGe as in Si. The advantage is that no knowledge about the base doping and thickness, the SiGe density of states and the absolute value of the diffusion coefficient of electron D_{nb} are needed [19]. The third possibility is to fabricate a similar all Si transistor [19]. By comparing the collector current of the Si transistor to that of the SiGe HBTs one can extract a Eg (SiGe) to Eg (Si) from the temperature dependence of the ratio of I_C in the two devices. The drawback of this method is that one has to assume the same temperature dependence of D_{nb} in Si and SiGe, which is improbable because of the additional effect of alloy scattering even at similar doping levels. Moreover it is technologically difficult to get an all-Si transistor with similar base doping. So usually N_{ab} (base doping) of the Si transistor is much less than in the SiGe HBT which introduces an additional error. This explains the scattering of the value of the band gap of the strained SiGe that has been reported in many literatures.

Another parameter of SiGe that is affected by the Ge content is the value of N_{CB} and N_{VB} (the density of states of the conduction and valence band). For Ge content approximately equal to 15 %, the value is of N_{CB} dropps to 2/3 of that of relaxed Si [20]. This is followed a by slight increase of its value (N_{CB}) with the increase in Ge content. The value of N_{VB} dramatically decreases for Ge content less that 20 % as shown in Figure 2.17. This is

disadvantageous for SiGe HBTs, since this reduction of N_{VB} and N_{CB} will lead to a decrease of the intrinsic carrier concentration (in the SiGe base layer) and then of the collector current [17]. However, the impact of the density of states is considered to be minor compared to that of the band-gap.

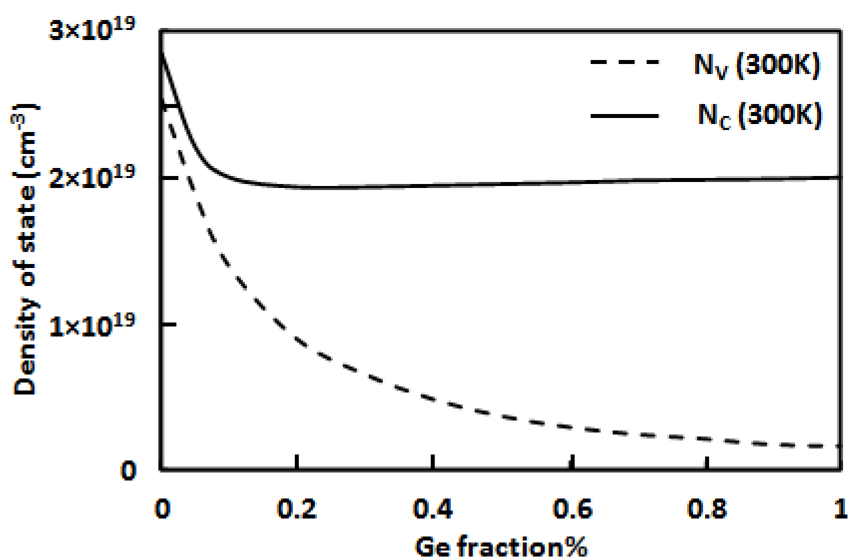

Figure 2.17: Conduction and valance band density of state in SiGe [20].

The amazing advancements achieved in recent years in Si CMOS technology have come primarily from scaling, i.e. from reducing the critical dimensions of the transistors. This has been accomplished by advances in photolithography as well as innovations in the fabrication processes and the use of new materials and novel high dielectric constant materials for the gate insulator. Because it has become increasingly difficult to further reduce critical dimensions such as the gate oxide thickness, alternative ways of improving transistor performance are also being employed. One important approach is to increase the charge carrier mobility using strained Si [21].

An important benefit of compressed SiGe is that can be used to boost the performance of PMOS devices. On any CMOS chip, the major limitation in performance is the PMOS. The mobility and effective masses of holes are smaller than those of electrons in Si. To balance the current drive in CMOS circuit design, the NMOS and PMOS have to be scaled [22]. The changes in the band-gap of the strained SiGe effectively modifies the hole transport properties in the layer, giving chances to improve the performances of PMOS [23]. Leonardo et. al. report 2.5 × hole enhancement in SiGe over Si [24].

The epitaxial growth of Si on relaxed SiGe leads to the formation of tensile strained Si. This is because the lattice constant of Si is smaller than that of SiGe. The electron carrier mobility is known to be high in tensile strained Si compared to relaxed Si, hence, the importance of this material in the fabrication of N channel MOSFETs. This has been shown in many experimental reports [25].

Several groups have reported theoretical and experimental values of the strained Si band gap on SiGe substrates as a function of the Ge content of the relaxed SiGe substrates using different calculation methods that account for conduction band and valence band shifts. According to this literature, a strained Si band gap shrinkage is expected as the Ge composition is increased in the SiGe substrate i.e., as strain is increased [26]. Equation (2.40) illustrates the band gap of strained Si versus the Ge content at 300 K [17].

$$E_g(x) = 1.11 - 0.6\,x \qquad (2.40)$$

This change in the band gap leads to a reduction of the carrier effective mass and band scattering rates, and therefore an increase of the carrier mobility (electron and hole) [27]. This mobility increases with an increase in strain which is determined by the Ge content of a SiGe layer underneath strained-Si films [28].Figure 2.18 shows also that N_V and N_C are smaller in strained Silicon compared to relaxed Si.

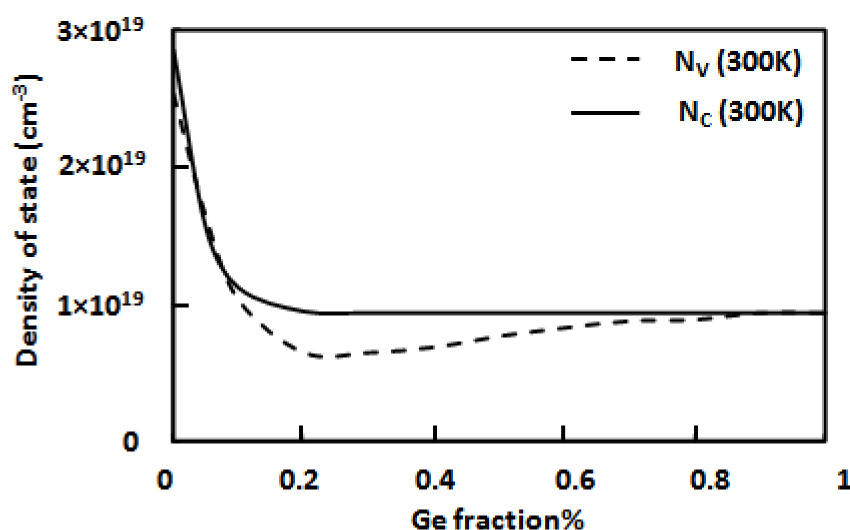

Figure 2.18: Conduction and valence band density of state in strained Si [20].

2.7 Dopant diffusion in SiGe

Every semiconductor device technology relies on the ability to fabricate well-controlled, locally doped regions of the wafer. The chemical impurities must first be introduced into some sections of the wafer. They must be active so they can contribute the desired carrier concentration. After the impurities are introduced they may redistribute in the wafer. This may be intentional or it may be a consequence of some other thermal process. In either event, it must be controlled and monitored. The motion of the impurity in the wafer occurs primarily by diffusion: any impurity that is free to move will experience a net distribution in response to a concentration gradient. The source of this movement is the random motion in the material. Since a high concentration region has more impurty atoms, there is a net movement of impurities away from the concentration maximum. This effect is not limited to impurities in semiconductors [16]. Fick's first law of diffusion given by equation (2.41) can also be used to describe heat transfer, the motion of electrons and gaseous impurities such as air pollution.

The basic equation that describes diffusion is Fick's first law [16]:

$$J = -D\frac{\partial C(x,t)_i}{\partial x} \tag{2.41}$$

Where C_i is the impurity concentration, D is the coefficient of diffusion and J is the net flux of the impurity material. The negative sign express the fact that there is net movement in the direction of decreasing concentration.

Diffusion in semiconductors can be visualised as atomic movement of the impurity in the crystal lattice by vacancies or interstitials. Figure 2.19 shows two basic atomic diffusion models in a solid. The open circles represent the host atoms occupying the equilibrium lattice positions. The solid dots represent impurity atoms. At elevated temperatures, the lattice atoms vibrate around the equilibrium lattice sites. There is a finite probability that a host atom acquires sufficient energy to leave the lattice site and to become an interstitial atom, thereby creating a vacancy. When a neighbouring impurity atom migrates to the vacancy site, as illustrated in Figure 2.19 (a) the mechanism is called vacancy diffusion. If an interstitial atom moves from one place to another without occupying a lattice site Figure 2.19 (b), the mechanism is interstitial diffusion. An atom which is smaller than the host atom

often moves interstitially [29]. The boron is known to diffuse on silicon using interstitial mechanism.

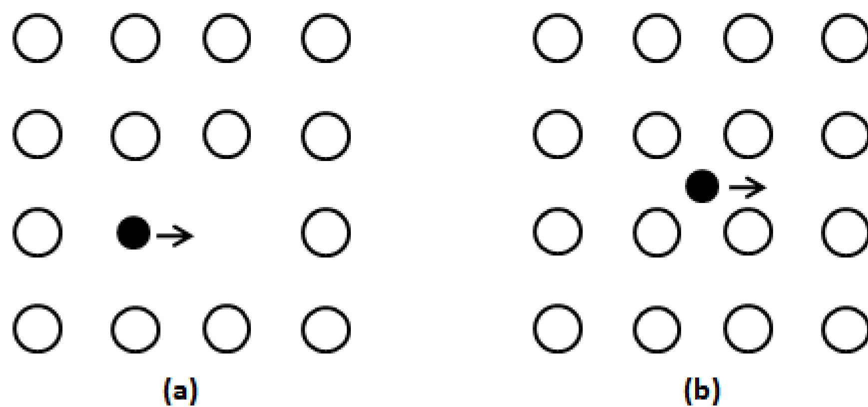

Figure 2.19: Atomic diffusion mechanisms for a two dimensional lattice. (a) Vacancy mechanism; (b) interstitial mechanism.

The logarithm of the diffusion coefficient for Si plotted against the reciprocal of the absolute temperature is known to give a straight line in most cases. This implies that over temperature range, the diffusion coefficient can be expressed as

$$D = D_0 \exp\left(\frac{-E_a}{kT}\right) \quad \textbf{(2.42)}$$

Where D_0 is the diffusion coefficient in cm^2/s and E_a is the activation energy in eV.

For the interstitial diffusion model, E_a is related to the energy required to move dopant atoms from one interstitial site to another. The value of E_a is found to between 0.5 and 2 eV in Si. For the vacancy diffusion model, E_a is related to both the energy of motion and the energy of formation of vacancies. Thus E_a for vacancy diffusion is larger than that for interstitial diffusion which is usually between 3 and 5 eV [29].

Understanding the dopant diffusion in SiGe, allows an accurate prediction of the doping profile after thermal annealing to be performed [30].

The nature of a Si/SiGe heterostructure introduces several complications to a dopant diffusion model as compared to diffusion in bulk Si. First, there is a so-called ‘‘chemical effect’’ caused by the introduction of Ge atoms [31]. The equilibrium concentration of self-interstitials and vacancies are closely related to the bonding energies of atoms. In covalent crystals, the heat of sublimation is equivalent to the energy needed for the rupture of half of the atomic bonds. The heat of sublimation values of pure Ge and Si crystals are, respectively,

equal to 374.5 and 455.6 kJ mol^{-1}. Thus, the atomic bonding energy in relaxed SiGe is lowered by the presence of Ge atoms and it is expected that both interstitial and vacancy concentrations will increase [32]. Secondly, SiGe has a larger lattice parameter, so when it is grown epitaxially on a Si substrate, the SiGe layer will be biaxially strained in order to comply with the smaller lattice parameter of the Si substrate. This macroscopic strain may influence the diffusion process as well [31].

Moriya et al. [33] have found that the boron diffusion is retarded in strained SiGe. This is advantageous for SiGe HBT design, since it facilitate the design of a device with a very thin base layer which therefore decreases both the base resistance and transit time. This results in an increase of device speed. The retardation of the boron in SiGe helps also to prevent the formation of parasitic energy barriers. This occurs when the boron penetrates outside the SiGe layer [34]. In the extreme case, depletion regions (emitter/base and base/collector) are formed in the Si region and hence the Si band gap is obtained at this depletion region. On moving into SiGe layer, a decrease of the band gap is obtained, which lead to the formation of parasitic barriers as illustrated in Figure 2.20. Even a small amount of out diffusion is reported to degrade the collector current and therefore the current gain [34].

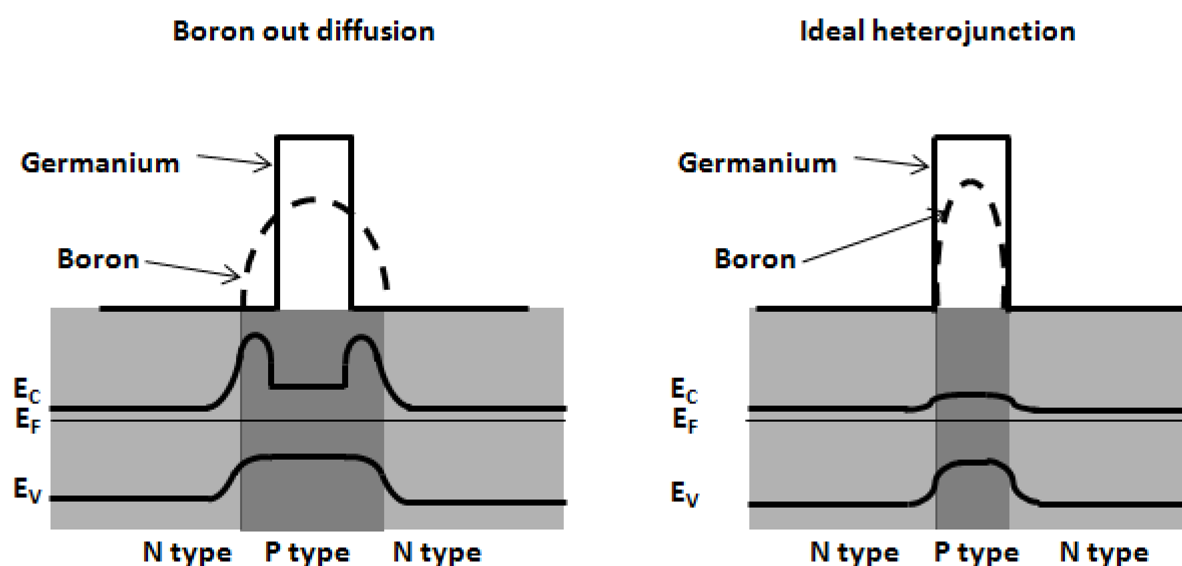

Figure 2.20: Parasitic barriers in SiGe HBTs.

Figure 2.21 illustrates the impact of Ge content on boron diffusion over a wide range of temperature. This figure shows that the presence of Ge leads to a reduction of boron diffusion.

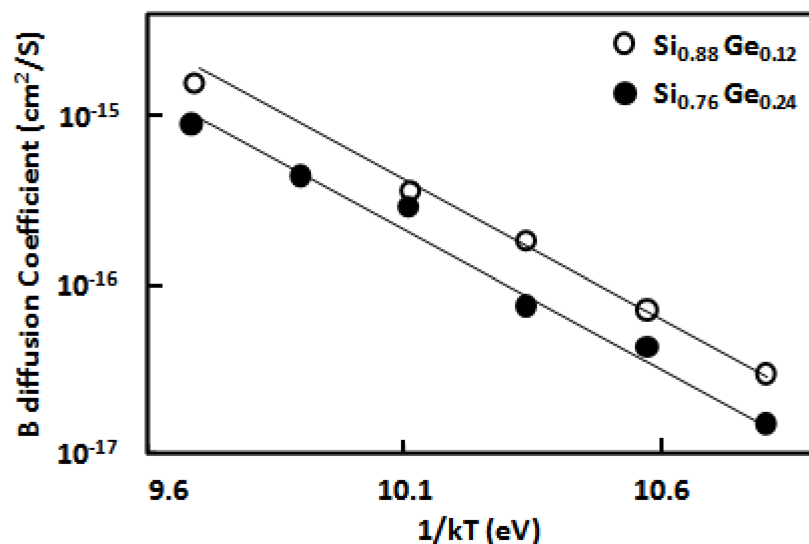

Figure 2.21: Boron diffusion in SiGe with different Ge content [35].

The work presented by Moriya et al. [33] did not separate the chemical influence and the strain influence on the boron diffusion, however this was done by Kuo et al. [36].

The strain dependence can be determined directly by measuring the diffusion in a SiGe layer grown pseudomorphically on a relaxed SiGe template. Varying the Ge content in the relaxed SiGe will allow a change in the amount of strain and also the type of the strain (compressive or tensile) in the pseudomorphic SiGe layer. Figure 2.22 represents the influence of the strain on boron diffusion at 800 °C. This data shows that the strain has a small impact on boron diffusion.

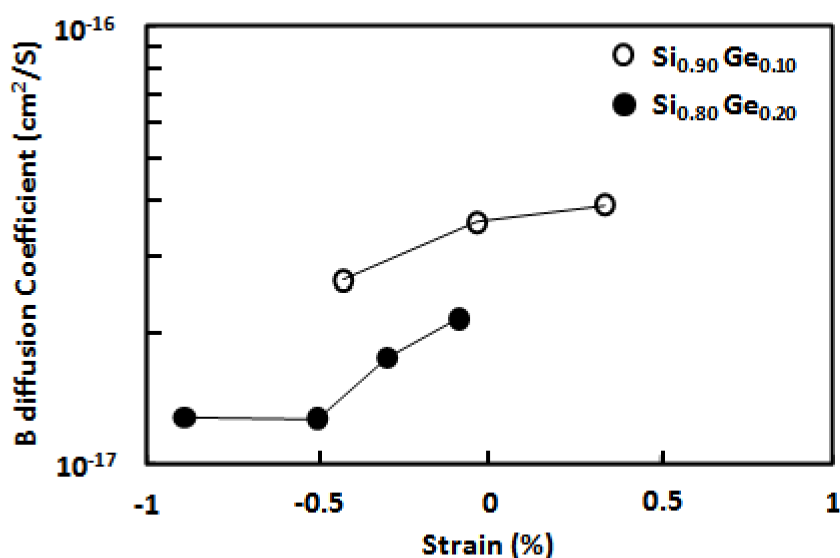

Figure 2.22: Influence of the strain on boron diffusion [36].

The impact of the Ge is not the same for all dopant species. Figure 2.23 shows that phosphorus diffusion is enhanced in SiGe relative compared to that in Si and the enhancement increases with increasing Ge content [31].

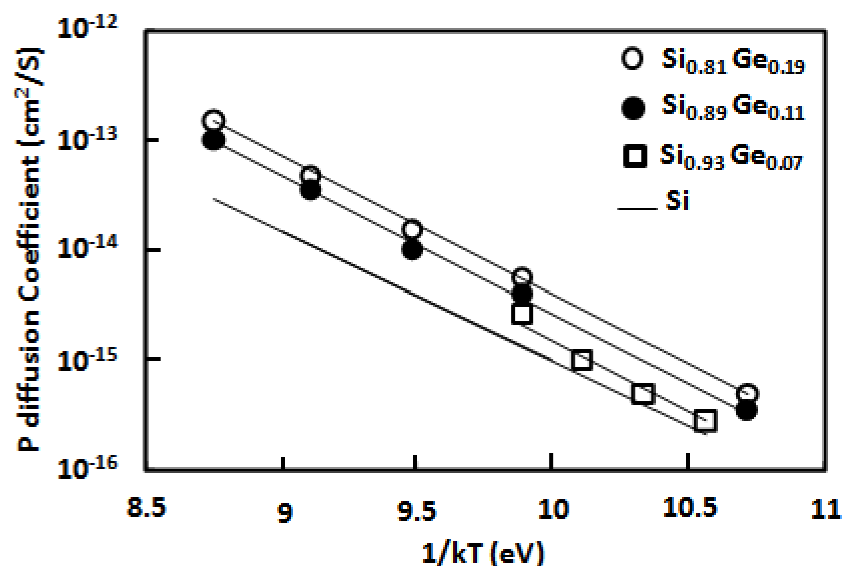

Figure 2.23: Phosphorus diffusion in SiGe [31].

2.8 Performance of SiGe HBTs

The performance of semiconductor devices tends to improve as the dimensions shrink. This simple principle of scaling has been the key to the spectacular success of the semiconductor industry over the past half-century. It has worked for virtually all types of transistors, including the Si-based bipolar transistor [37].

Historically, scaling has run into difficulties many times in the course of bipolar technology evolution, which have been successfully overcome with help from material and structural innovations, such as the self-aligned base, poly emitter, and most recently, the SiGe base.

There has been tremendous progress in the ability to grow device quality SiGe films. The initial growth technique used was Si MBE [38], but this was replaced by high quality CVD techniques such as UHV/CVD . The ability to in situ dope SiGe films with B and P and incorporate C (to reduce the boron diffusivity) in the film has greatly extended the performance levels achieved [39]. The ability to grow high quality SiGe has lead to a successful fabrication of SiGe HBTs. This device consists of having a thin SiGe layer as base instead of Si for Si BJTs.

Bandgap engineering with the incorporation of Ge in the base of silicon bipolar transistors results in improved performance of these devices with only a modest increase in process complexity. The Ge content has tipically, one of three possible profiles as shown in Figure 2.24. The first one is the Box profile: the Ge content is constant throughout the base. The second is the triangular profile, where the Ge content changes linearly with depth. The third one is the trapezoidal, which is a combination of the triangular and box profile. The small band gap of the SiGe layer increases the amount of minority carriers injected into the base exponentially, thus causing an increase in the collector current for the same forward bias. In addition, the band gap grading gives rise to a drift field which aids the minority carrier transport through the base. The incorporation of a small amount of Ge into the Si in the base layer therefore greatly enhances the performance of the transistor [40]. Figure 2.24 illustrates the three possible profiles.

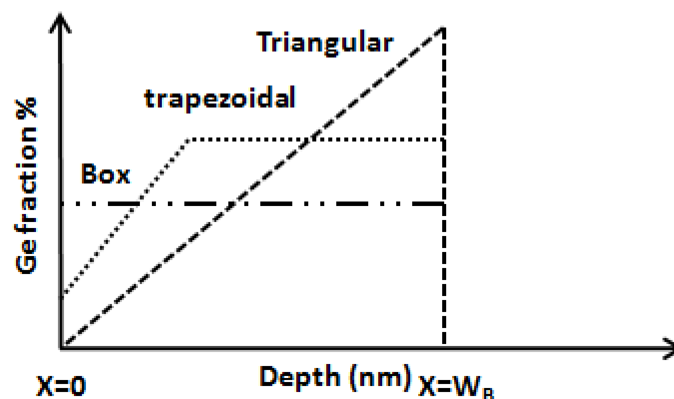

Figure 2.24: Different type of Ge profile (Box, Trapezoidal and Triangular) that can be used in bipolar technology.

Generally, the use of Ge enhances both DC (current gain) and AC (cut-off frequency) performance of SiGe HBTs. However, triangular profile increases more the speed of the device while the box profile has great impact on the current gain of the device. Figure 2.25 shows the current gain ratio for SiGe HBTs and Si BJTs. This ratio decrease when moving from box profile to triangular profile. Figure 2.26 illustrates the cut off frequency of two SiGe HBTs with different profiles. While the speed of both devices increase with increase of Ge content in the base, it obvious that the use of a triangular profile leads to the highest cut- off frequency.

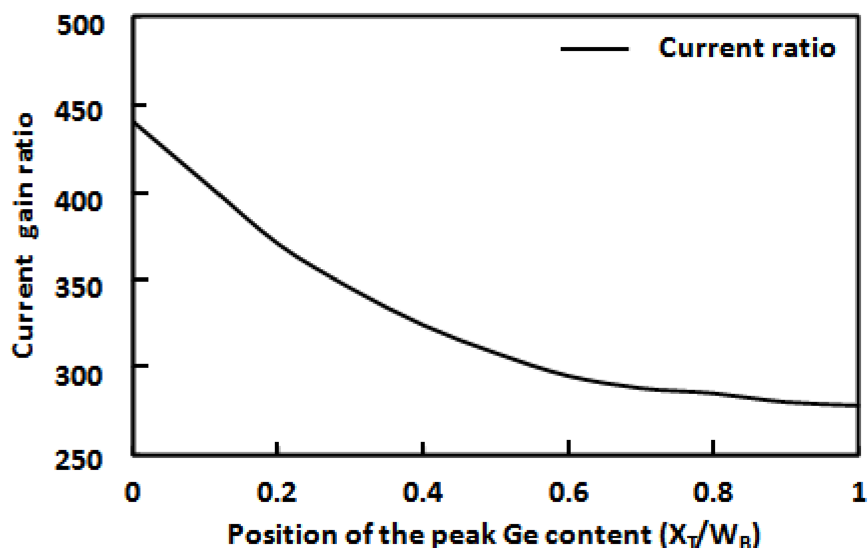

Figure 2.25: Plot of current gain ratio vs. position w, (that is, XT/WB) of the peak Ge content at the base of the SiGe HBT (w =0 for the box profile, w =1 for the triangular profile, trapezoidal otherwise) [41].

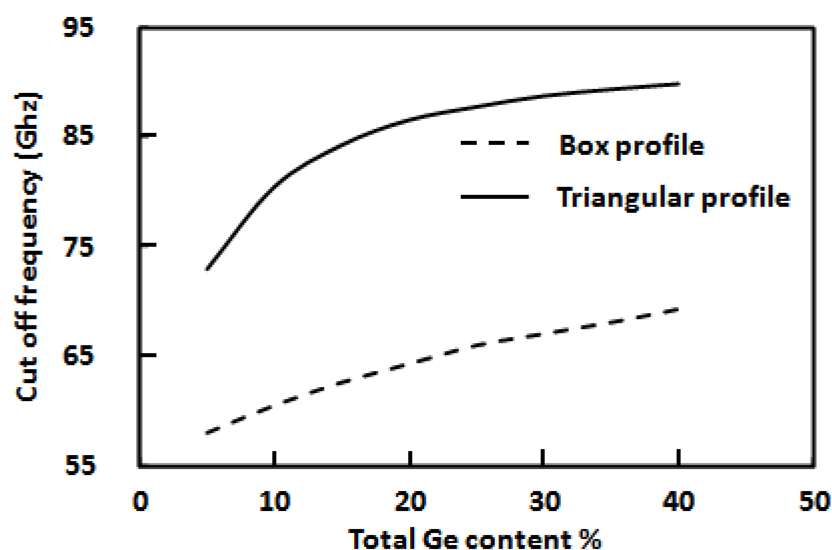

Figure 2.26: Cut off frequency versus Ge content for both Box and triangular profile [41].

2.9 BiCMOS technology using VS HBT

Silicon integrated circuits presently dominate the semiconductor industry. The two most important devices used in Si technology are field effect and bipolar transistors. For digital circuit applications, complementary metal oxide semiconductor (CMOS) technology dominates because of its low power dissipation and high density of integration However, MOS transistors have a number of disadvantages, foremost among which are limited drive

capability and limited high frequency performance. CMOS has been the work horse for microprocessors and static random access memories. Bipolar transistors with their high speed and high transconductance (therefore high current drive) have mostly been used in analogue applications. The main drawback in bipolar digital circuits is the high power consumption. To improve single chip functionality, bipolar complementary metal oxide semiconductor (BiCMOS) has been developed to combine the advantages of CMOS and bipolar devices.

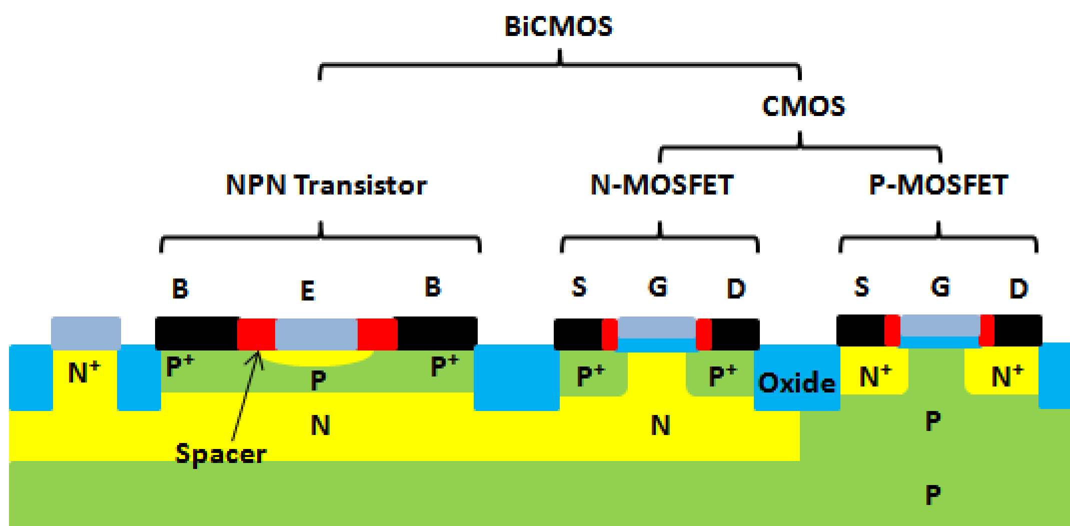

Figure 2.27: Structure of BiCMOS chip [1].

The BiCMOS process is also ideal for analogue and mixed-signal applications because the best features of MOS and bipolar transistor can be combined to deliver the best system performance. With analogue BiCMOS, a wide variety of different analogue and digital building blocks can be integrated into a single chip. This system integration approach enables digital functions, such as processors and memories, to be freely integrated with analogue functions, such as A-D converters, amplifiers and filters. In this way a powerful and universal technology is created, which makes possible the integration of all types of electronic system.

The main drawback of BiCMOS technology is the higher costs due to the added process complexity. Impurity profiles have to be optimized for both NPN, PNP and CMOS issues. This greater process complexity results in a 1.25 to 1.4 cost increase compared to conventional CMOS technology [42].

In the early BiCMOS processes, considerable effort was applied to minimising the total number of the processing steps by merging the processing steps of MOS and bipolar transistor wherever possible. For example, the P^+ source /drain implant can be used for the extrinsic base of the bipolar transistor, the N^+ source/drain implant for the collector contact and CMOS polysilicon gate for the polysilicon emitter of the bipolar transistor. In more recent BiCMOS technology, the trend is not to merge the process steps for the MOS and bipolar transistor, but rather to add the bipolar transistor with minimum distraction to the CMOS process. The reason for this change is partially due to the large effort required to develop a deep sub-micron CMOS process, and partly due to importance of time to market [1].

Analogue BiCMOS requires additional components such as resistors, capacitors, diodes and PNP bipolar transistors. RF BiCMOS requires, in addition, inductors. While some of these components can be fabricated without any additional process steps others require extra processing. Resistors can be easily produced without any additional processing by using the series resistance of the various layers that comprise the bipolar and the MOS transistors. Capacitors can be easily produced by using a thin silicon dioxide as dielectric and t therefore producing a parallel plate capacitor. Inductors are generally fabricated by realizing a metal spiral in the top level of metallization, as shown in Figure 2.28. The contact to the centre of the spiral is made to a lower level of metal through a via [1].

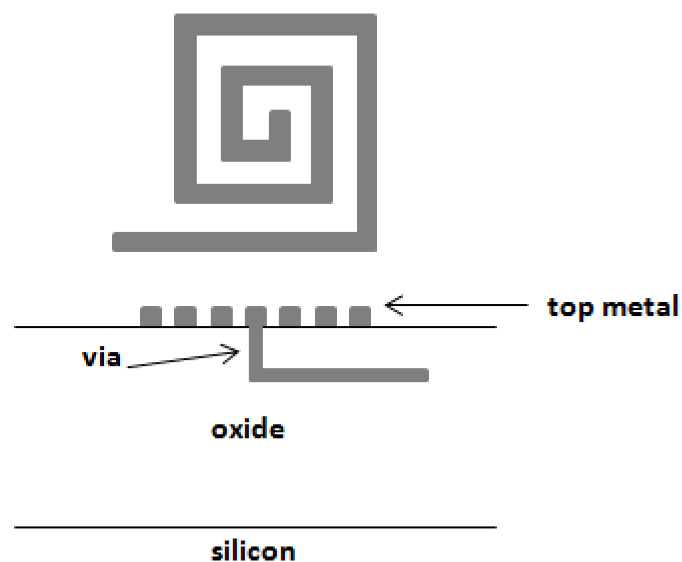

Figure 2.28: Plan and cross-views of an integrated circuit inductor.

The introduction of SiGe material into Si-based technology has remarkably enhanced the drive current and the speed of bipolar devices, leading to the fabrication of SiGe HBTs. BiCMOS technology has also benefited from this achievement, since SiGe HBTs have been successfully integrated with CMOS devices. This has resulted in even higher BiCMOS chip performance. However, up to now, there has been no integration of strained MOSFETs devices with bipolar devices.

2.10 Conclusion

This chapter presents a review of the basic equations that govern the current in the PN junction. This was an important task, since this junction is the basic element of bipolar transistor and all types of transistor. This was followed by statement of the equation of the collector and base current and therefore the current gain. Different strategies to improve the performance of the device have been discussed. The drawbacks of these methods have been also reported. The study has shown that it is difficult to improve both the DC and AC performance of bipolar transistor without adding a new aspect to this device. This aspect is the ability to engineer the band gap of the base region. Using SiGe in the base region was the method to accomplish this task, which has lead to the fabrication of SiGe HBTs. This device has proved his hog performance compared to Si BJTs. This chapter has also report the impact of the SiGe and strained Si on CMOS technology.

The profile of the Ge in the SiGe base layer can have two main shapes; the triangular and box profile. The triangular profile is known to increase the speed of the device while the box profile enhances the current gain. The improvement of the performance that has been shown by the SiGe HBTs is also linked to the total amount of the Ge in the base, more Ge simply mean increase in the performance. However, increasing the Ge percentage in the SiGe layer cannot be infinitely. This is because the lattice constant of the SiGe is higher than of the Si and having high Ge content may cause the production of defects.

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Chapter 3. Electrical & material characterisation of sSi HBTs

3.1 Introduction

The market for analogue RF ICs for mobile communication has been growing rapidly. This trend has pushed the need for new processing technologies that can achieve higher operating frequencies, lower power consumption and more compact system integration.

The conventional SiGe HBTs, which consists of a SiGe layer in the base, was introduced as a commercial product in 1999 after its first demonstration in 1988 [1]. The introduction of the Ge in the base is known to be the factor behind the outperformance of the SiGe HBTs over Si BJTs. However, if the Ge content is above a certain level, the magnitude of the strain becomes larger which results in the formation of dislocations. Advanced epitaxial growth of strained and relaxed SiGe layers enhances the amount of Ge that can be incorporated in the base. This is accomplished using a Strained Relaxed Buffer (SRB) in the collector which reduces the strain magnitude in the base.

The current BiCMOS chip consists of the integration of the SiGe HBTs and conventional MOSFET. Using SRB in the fabrication of sSi HBTs has raised the possibility of integration of strained Si MOSFET and sSi HBTs in one chip.

This chapter presents the first experimental demonstration of NPN sSi HBTs, which consist of Strained Si (emitter), compressed SiGe (base) and SiGe strain-relaxed buffer (collector). The design requirement for each layer (i.e. collector, base and emitter) in order to have best performing devices are discussed. The fabrication process steps and also doping levels, Ge content and thickness of each layer are provided. Material characterisation of sSi HBTs is presented and compared with co-processed NPN SiGe HBTs and NPN Si BJTs. A comparison of important figures of merit e.g. current gain, ideality factor, breakdown voltage and Early voltage is made between all devices. The result of this comparison is discussed and linked to material proprieties of each device.

Any effort in life is rarely one person's individual accomplishment but is rather completed through a collective support network and the work presented in this chapter is no exception. During the preparation of this work, the main focus has been on data analysis with less effort on performing electrical characterisation and masks design.

3.2 Collector layer design

A relatively low collector doping at the depletion edge of the collector-base junction is an important requirement for a small collector-base capacitance. This is an essential requirement for a high speed device [2]. However, low collector doping can also introduce high series resistance [3]. An approach which has been used in early bipolar processes is the introduction of an n+ buried layer (subcollector) which will provide a low resistive path to the collector contact. The buried layer is fabricated by implanting arsenic or antimony and heating at high temperature to diffuse the dopant. This step is followed by growing a low doped epitaxial layer which serves as a collector. Auto doping of the epitaxial (collector) layer which occurs through diffusion of the dopant from the buried layer may increase the collector doping; this is a issue for high speed devices where the collector layer is thin [4]. An alternative method, which is known as selective implant collector (SIC), is performed after the fabrication of the base layer and emitter window opening, the energy of the SIC implant is chosen to have low doping at the depletion edge on the collector side [4, 5]. For Si BJTs and SiGe HBTs presented in this work, the subcollector was grown epitaxially on (100) Si wafer at 1080 °C. However the collector was grown at only 750 °C to reduce the diffusion of the P toward the base. The epitaxy was performed in an ASM Epsilon 2000E RP-CVD reactor using in-situ doping. The subcollector and collector were doped to $3{\cdot}10^{19}$ cm^{-3} and $5{\cdot}10^{17}$ cm^{-3} respectively, and have thicknesses of 0.4 µm and 1 µm respectively. The out diffusion of the dopant from the subcollector, which can increase the doping level at the collector base depletion region, is prevented by the thickness of the collector. For the sSi HBTs, the subcollector and collector are formed from relaxed SiGe. This was grown at 850 °C using terrace grading with an average rate of 10%-Ge μm^{-1}, topped with a 1.2 µm thick $Si_{0.85}Ge_{0.15}$ layer. This relaxed SiGe layer is called Strain Relaxed Buffer layer (SRB).

3.3 Base layer design

The challenge in the fabrication of the base layer for bipolar transistors is the fabrication of a thin base layer. However, this challenge is even more serious for SiGe HBTs and sSi HBTs, where the boron profile should be retained within the SiGe layer during the post-epitaxial processing [6]. A thin base layer reduces the base transit time which improves the cut-off frequency [7], however it also raises the base resistance. In order to deal with this trade off between the cut-off frequency and base resistance, the base layer should be thin and highly doped. A low base resistance improves the maximum frequency of oscillation f_{max} [8].

The diffusion of the boron during the device processing toward the collector and emitter is called boron out-diffusion. This leads to the formation of parasitic energy barriers at the emitter base and base collector junctions [9]. These barriers suppress the transport of electrons from the emitter to the collector which result in reduced collector current [10]. To avoid the formation of these barriers, several approaches have been implemented. Introduction of a small amount of carbon (0.2–0.5%) in the SiGe layer reduces the boron diffusivity. This, in fact, decreases the boron out-diffusion and creates the possibility of extending the thermal budget of the fabrication process [11]. In this work another option has been used, which is implementing 5 nm of undoped SiGe layer on both sides of the p-type SiGe layer to allow for out diffusion, while keeping the heterojunction located in the n-type adjacent layers. This necessitates estimating the amount of out-diffusion accurately since the presence of undoped layers will contribute to poorer device performance. The Si base layer of Si BJTs was grown epitaxially at 750 ºC, while the SiGe base layer was grown at 650 ºC having Ge compositions of 30% and 15% for sSi HBTs and SiGe HBTs, respectively. The Ge profile is designed to be constant through the base layer for both devices. Emitter layer design

3.4 Emitter layer design

The emitter is required to be highly conductive for electrons and designed to provide a sufficient barrier for holes injected from the base. Therefore, the highest doping level of the emitter is required.

An emitter layer with a thickness of 30 nm was epitaxially grown at 750 ºC for all devices (i.e. Si BJTs, SiGe HBTs and sSi HBTs). It was doped at $5{\cdot}10^{17}$ cm^{-3}. This was followed by a

deposition of heavily doped poly-silicon (P, $5\cdot10^{19}$ cm^{-3}). The polysilicon improves the ability to have a shallow emitter base junction [12]; also it is reported that the interfacial oxide between the emitter and the polysilicon suppress the minority carrier transport, leading to an enhancement in the current gain [13]. It is also stated that the base current decreases significantly with only a slight increase of the interfacial oxide thickness [14]. Prior to the deposition of the polysilicon an RCA cleaning was performed. This particular method decreases the base current compared to HF [15]. The layer thicknesses, doping level and Ge content for the three devices are summarised in Table 3.1.

Layer	t (nm)	Doping (cm^{-3})	Ge (%)		
			Si BJTs	SiGe HBTs	sSi HBTs
Emitter	30	$1\cdot10^{18}$	0	0	0
Spacer	5	0	0	15	30
Base	12.5	$2\cdot10^{19}$	0	15	30
Spacer	5	0	0	15	30
Collector	1000	$5\cdot10^{17}$	0	0	15
Subcollector	400	$5\cdot10^{19}$	0	0	15

Table 3.1. The layer thicknesses, doping level and Ge content for Si BJTs, SiGe HBTs and sSi HBTs.

3.5 Strain-relaxed buffer

The high performance of SiGe HBTs over Si BJTs is due to the use of Ge content in the base layer [16]. However, the amount of Ge content that can be incorporated is limited by the magnitude of strain that can be accommodated in the base. For a given SiGe layer thickness there is a maximum Ge content that can be used; exceeding this value will lead to the relaxation of the SiGe layer through the formation of misfit dislocation defects [17], these defects are known to degrade the device performance through the recombination mechanism. To enhance the amount of Ge that can be used in the base, the strain should be kept to a certain value. This can be accomplished using a Strain Relaxed Buffer (SRB). This consists of growing a thick SiGe layer, in which the Ge concentration is increased from 0% to 15% in smooth way (10%-Ge μm^{-1}). This layer is topped with a SiGe layer with fixed Ge content. This technique has a critical problem. The SiGe layer, which becomes very large to

reduce the threading dislocation defect, causes a self-heating effect [18]. This problem can be overcome by using thin SRB. It can be produced by incorporating C into SiGe SRB during the early growth stages, this results in a final SRB relaxation level of 90% after annealing [19]. Another way to produce a thin SRB is to subject the SiGe buffer to ion implantation to form defects that work as a dislocation source for strain relaxation [20]. These methods lead to the fabrication of thin SRB on the order of 200-400nm. Moreover Bauer et al reported SRB as thin as 70 nm [21].

3.6 Fabrication process steps

The starting point was the growth of the subcollector, collector, base and emitter layer epitaxially as shown in figure 1(a), which was performed at Warwick university. This was followed by etching of the material surrounding the emitter, down to the collector to form mesa isolation, so the emitter could be isolated from the base and collector contacts, as shown in figure 1(b). An N-type collector link was implanted using P at a dose of $5\cdot10^{15}$ cm^{-2} and energy of 20 keV and an extrinsic base region was subsequently implanted using BF_2 at a dose of $1\cdot10^{15}$ cm^{-2} and an energy of 35 keV as illustrated in figure 1(c). The next step was low thermal oxide (LTO) deposition (400 nm) to isolate the structure and define the collector and emitter window, as shown in figure 1(d). Heavily doped n^+ polysilicon (P, $5\cdot10^{19}$ cm^{-3}) was deposited for both contacts, figure 1(e), followed by RTA step, which was 900 °C for 10s. Etching the polysilicon was necessary to isolate the emitter poly from the collector poly, see figure 1(f). LTO deposition (400nm) was performed to define the emitter, base and collector window contacts, as illustrated in figure 1(g). The process was concluded with the deposition of the Al base, emitter and collector contacts with a TiW barrier layer and a forming gas anneal. The final transistor structure is shown schematically in figure 1(h). The fabrication process for all devices was performed at KTH in Sweden, while the design was carried out at Newcastle University.

In order to explore the impact of parameter design space on the current gain, devices were fabricated with different values of E_W emitter window width, L_E emitter window length, D1 distance to the collector and D2 distance to the base. Figure 3.2 shows a schematic diagram of a bipolar device and the parameter design space.

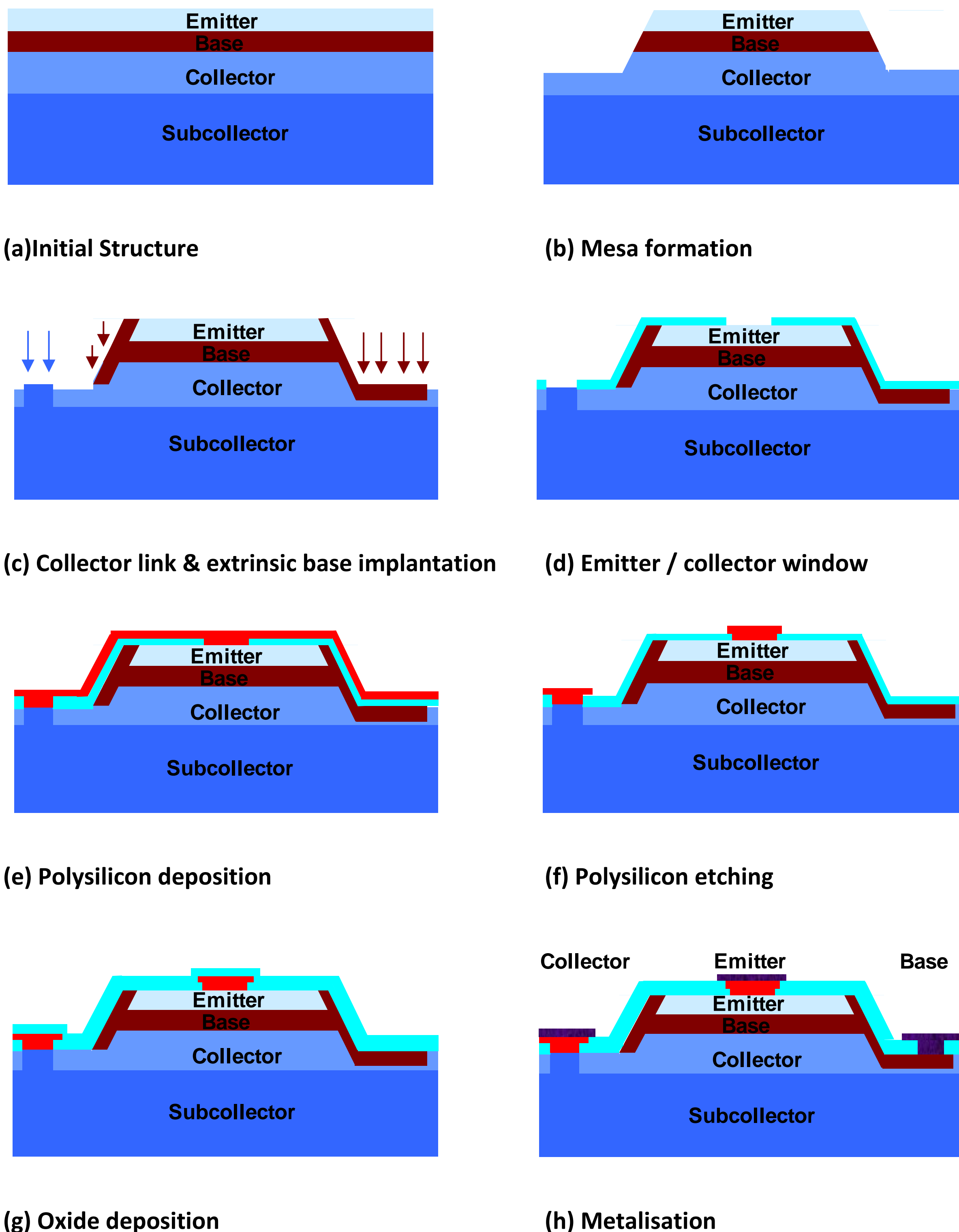

Figure 3.1. Simplified process flow, Si BJTs, SiGe HBTs and sSi HBTs were fabricated using the same process flow.

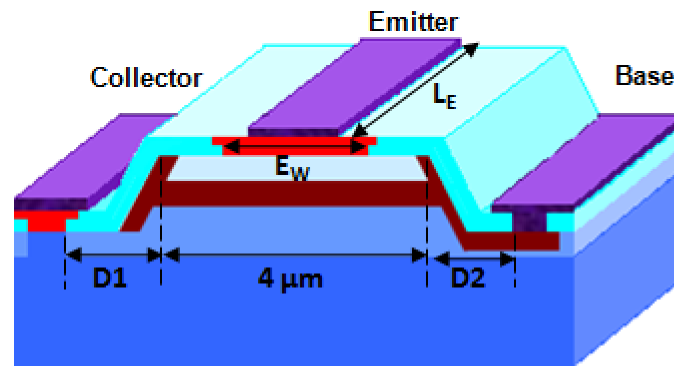

Figure 3.2: Schematic diagram illustrating different parameters design space.

3.7 Material characterisation

Material characterisation of sSi HBTs was carried out and compared with results from co-processed SiGe HBTs and Si BJTs. Transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and electron energy loss spectroscopy (EELS) were used to analyse material properties.

Figure 3.3, Figure 3.4 and Figure 3.5 illustrate the SIMS data for sSi HBTs, SiGe HBTs and Si BJTs respectively. In Figure 3.4, the Ge profile is "box like" for SiGe HBTs with a maximum value of 15%. This is in a good agreement with the target value. For the sSi HBTs, the Ge profile in the base is slightly higher than the target value; it is also slightly higher towards the collector end of the base than the emitter end. Figure 3.6 shows a comparison of the boron profile for all devices. The boron profile for the sSi HBTs is sharper compared with that of the other devices; also the boron profile for the SiGe HBTs is sharper compared with Si BJTs. This is due to reduced boron diffusion caused by the presence of the Ge [22]. A sharper boron profile is favourable for the fabrication of the thin base devices because it reduces the base transit time, hence improving the AC performance [23].

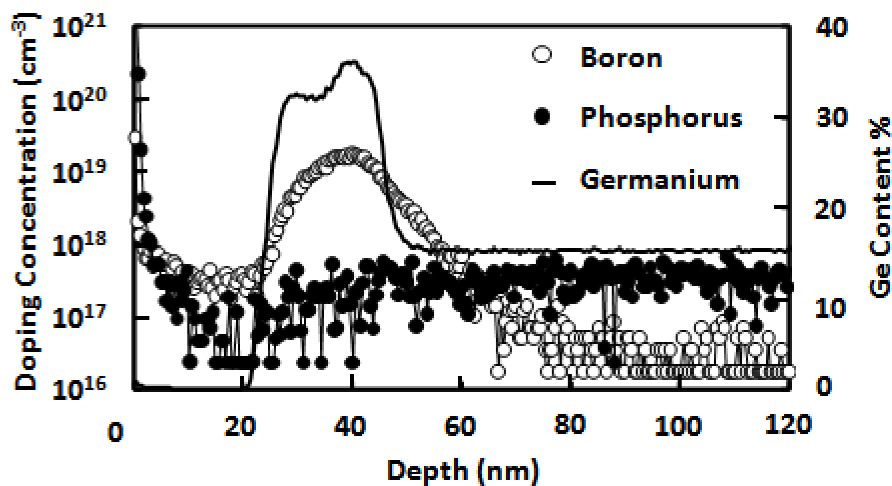

Figure 3.3: Phosphorus, boron and Ge profile for sSi HBTs.

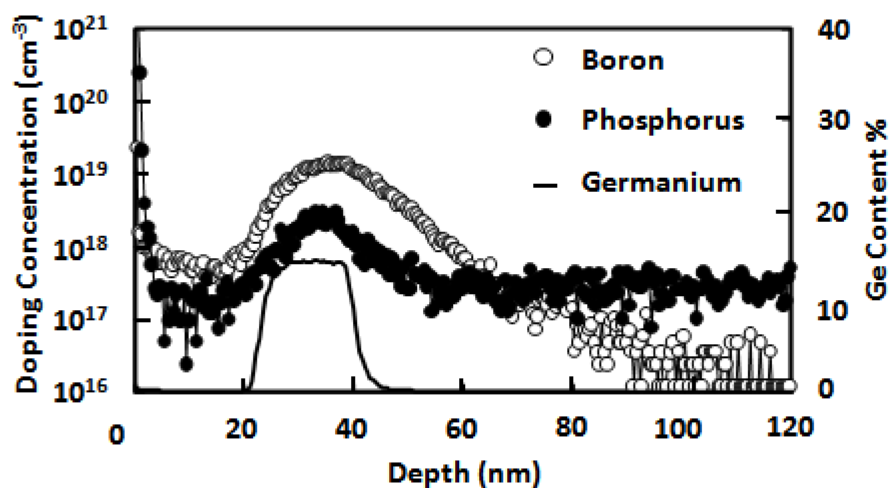

Figure 3.4: Phosphorus, Boron and Ge Box profile for SiGe HBTs.

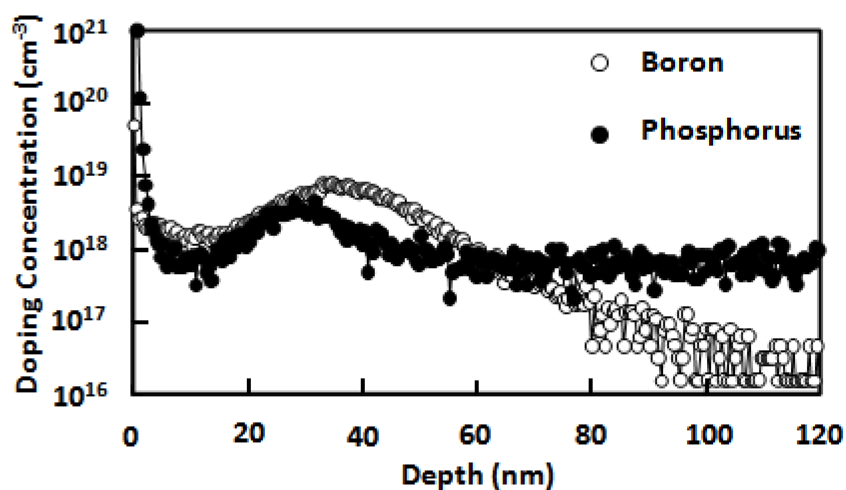

Figure 3.5: Phosphorus and Boron profile for Si BJTs.

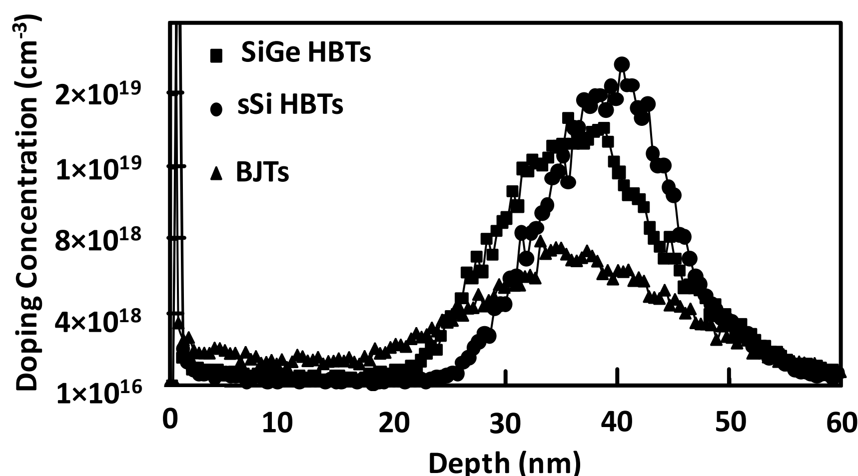

Figure 3.6: Comparison of the Boron profile in Si BJTs, SiGe HBTs and sSi HBTs.

Raman spectroscopy confirmed that strain in the emitter of the sSi HBTs was fully maintained following processing. The peak position in the Raman spectrum shown in Figure 3.7 confirms that the SRB ($Si_{0.85}Ge_{0.15}$) is fully relaxed and that the tensile strain in the emitter of the sSi HBTs was maintained after processing [24]. The base layer is too thin to be seen in these Raman spectra.

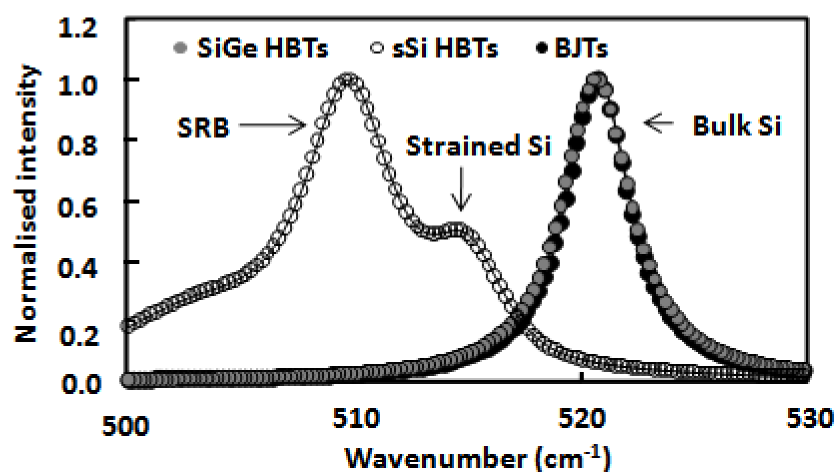

Figure 3.7: Raman spectra from strained sSi HBTs, SiGe HBTs and Si BJTs.

The TEM image for sSi HBT in Figure 3.8 shows well defined collector, base and emitter layers, with an abrupt transition between layers. Also it can be shown that the base layer is formed from two regions (Base 1, Base 2) with different Ge content (different degree of grey colour); this is consistent with the SIMS data which shows that the Ge content in the base is slightly higher towards the collector end of the base than the emitter end. Figure 3.9 is the TEM image for the SiGe HBTs, where the SiGe base layer is well defined. Figure 3.10

shows the TEM image of the Si BJTs; the image shows only one region because the emitter, base and collector layers are Si-based only.

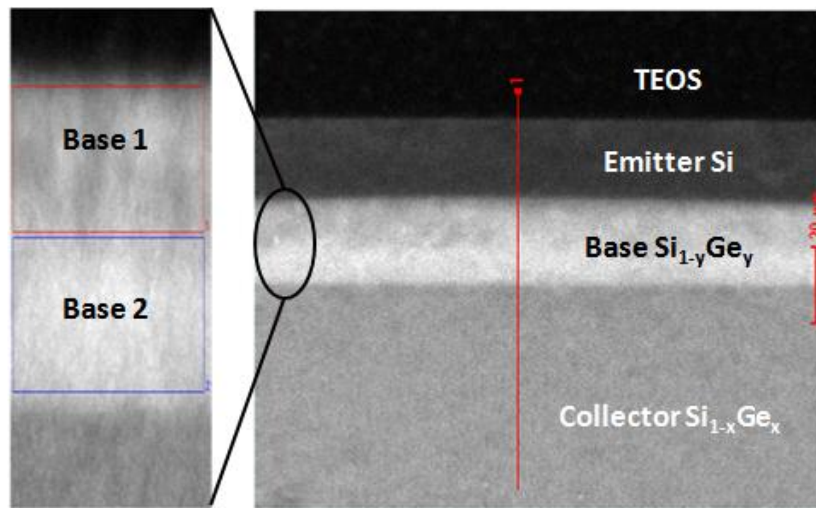

Figure 3.8: TLM image for sSi HBTs.

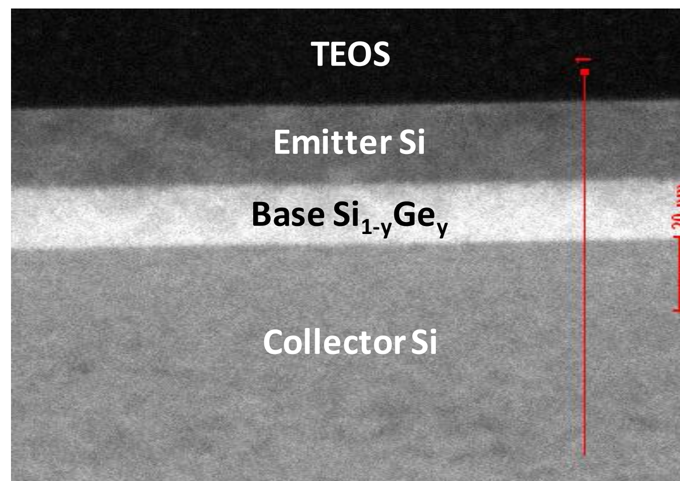

Figure 3.9: TLM image for SiGe HBTs.

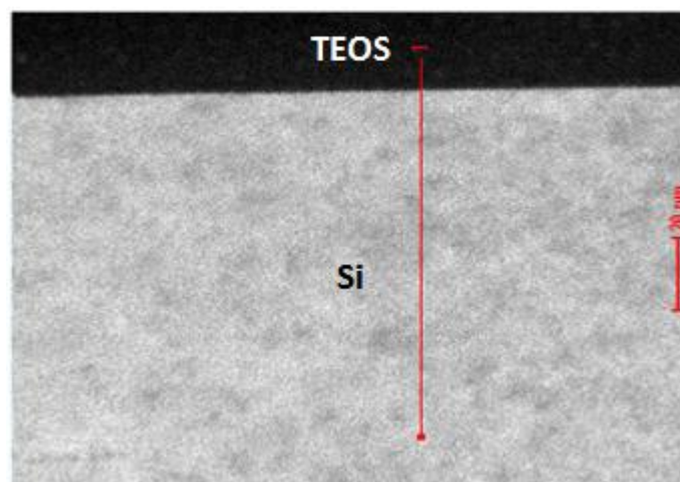

Figure 3.10: TLM image for Si BJTs.

Electron energy-loss spectroscopy (EELS) is an analytical technique that measures the change in kinetic energy of electrons after they have interacted with a specimen. When carried out in a modern transmission electron microscope, EELS is capable of giving structural and chemical information about a solid, with a spatial resolution down to the atomic level [25].

Figure 3.11 shows the Ge profile measured by EELS for the sSi HBTs. Although the Ge profile is noisy, it is still possible to conclude that the Ge content in the collector is constant. In the base, the Ge content is slightly higher towards the collector end of the base than the emitter end. This is can be only seen by ignoring the noise in the data. This is consistent with the SIMS results in Figure 3.3. Figure 3.12 shows the EELS data for the SiGe HBTs. The data shows a high level of noise. However the box-like profile is still visible. This is consistent with the SIMS results in Figure 3.4. Figure 3.13 illustrates the EELS results for Si BJTs, which shows no evidence of the presence of Ge.

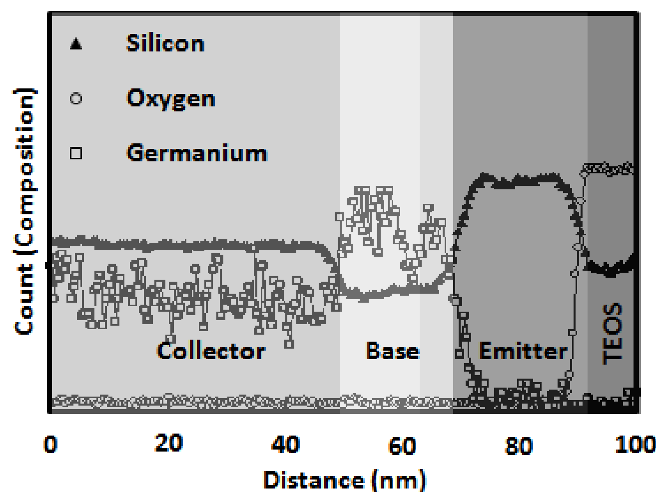

Figure 3.11: EELS data for sSi HBTs.

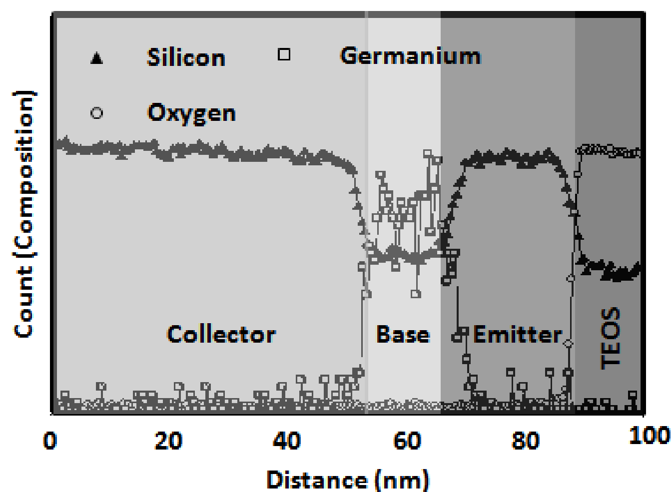

Figure 3.12: EELS data for SiGe HBTs.

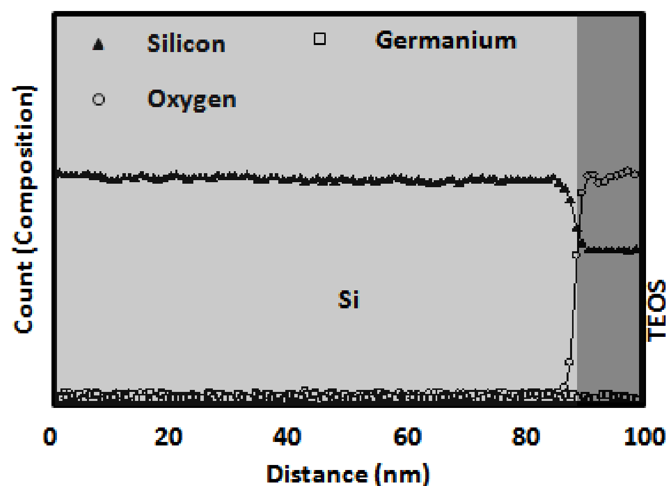

Figure 3.13: EELS data for SiGe HBTs.

3.8 Characterization methods

A typical starting point for device characterization is taking DC measurements to determine the current gain β. The current gain is obtained by measuring the collector current I_C and base current I_B as a function of the forward base-emitter voltage V_{BE}. Figure 3.14 illustrates the measurement set-up used to determine this figure of merit. The base terminal was grounded as well as the collector terminal while the emitter terminal was swept by a bias ranging from 0 V to -1 V. The measurements were performed in a Cascade probe station using Agilent 4155c parameter analyser which is controlled by Easy express software. The Gummel plot, i.e. the plot of I_C and I_B versus V_{BE} with the currents plotted on a log scale, is an exceptionally useful tool in bipolar device characterisation. First, the current gain is

defined as the ratio of the collector and the base current. Second, it allows measuring the ideality factor which reflects the quality of the emitter base depletion region [26].

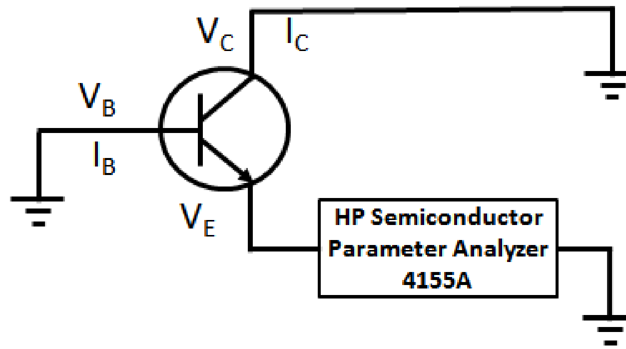

Figure 3.14: Measurement set up used to extract the Gummel plot. The collector and base contacts were grounded and the emitter contact was swept from 0 V to -1 V.

3.9 Gummel plot

Figure 3.15 shows a comparison of the collector current for sSi HBTs, SiGe HBTs and Si BJTs. The SiGe HBTs exhibits a higher collector current compared with Si BJTs, as has been reported by others [27, 28]. However, the collector current in the sSi HBTs is increased considerably compared to both devices. The equation (3.1) represents the collector current.

$$I_C = \frac{qAD_{nb}n_{iB}^2}{W_B N_a} \exp\frac{qV_{BE}}{kT} \tag{3.1}$$

Where q is the electronic charge, A is the device area, D_{nb} is the diffusion coefficient of electron in the base, W_B is the base width, N_a is the acceptor concentration in the base, V_{BE} is the base-emitter voltage, k is Boltzmann's constant and n_{iB}^2 is the intrinsic carrier concentrations in the base and it is given by the equation (3.2).

$$n_{iB}^2 = N_{CB} N_{VB} \exp\frac{-E_{gB}}{kT} \tag{3.2}$$

Where, N_{CB} and N_{VB} are the density of states in the conduction and valence bands in the base layer, respectively. $E_{gB}$is the band gap of the base layer. Inserting the equation (3.2) into (3.1) leads to equation (3.3).

$$I_C = qA\exp\frac{qV_{BE}}{KT}\left[\frac{D_{nb}N_{CB}N_{VB}}{W_B N_a}\right]\exp\left[\frac{-E_{gB}}{KT}\right] \tag{3.3}$$

The equation (3.1) shows that the collector current depends on the material properties of the base layer. The product $N_{CB}N_{CV}$ is slightly smaller for the sSi HBTs and SiGe HBTs compared with Si BJTs, this suggests a reduction of the collector current by factor of about 3 for sSi HBTs and SiGe HBTs [29]; however, there are other important parameters which are responsible for the enhancement of the collector current. The most important factor is the band gap. The band gap of the base layer decreased from 1.17 eV for the Si BJTs to 1.04 eV for the SiGe HBTs and 0.94 eV for the sSi HBTs [30]. Moreover, according to the SIMS data, the Boron profile in the sSi HBTs base layer is sharper compared to SiGe HBTs, this results in a small WB for sSi HBTs compared to other devices, similarly WB for SiGe HBTs is small compared to Si BJTs. A smaller WB further enhances the IC. The local small peak in the Ge concentration close to the collector shown in Figure 3.3 acts as an accelerating field that increases IC for sSi HBTs. The conduction band in both the SiGe HBTs and the sSi HBTs exhibits a discontinuity at the base-collector junction; this discontinuity causes a reduction in IC. The conduction band discontinuity is slightly smaller for the sSi HBTs compared to SiGe HBTs. In conclusion, the exponential dependence of the collector current on the band gap, together with the smaller band gap of the base layer for the sSi HBTs, suggests that the band gap is the important factor which results in a high I_C.

Figure 3.16 shows that the base current for the SiGe HBTs and the Si BJTs is the same. However, the sSi HBTs exhibits a slightly higher base current. The equations (3.4) and (3.5) describe the base current and the intrinsic carriers, respectively.

$$I_B = \frac{qAD_{pe}n_{iE}^2}{W_E N_E}\exp\frac{qV_{BE}}{kT} \tag{3.4}$$

Where q is the electronic charge, A is the device area, D_{pe} is the diffusion coefficient of holes in the emitter, W_E is the emitter width, N_E is the donor concentration in the emitter, V_{BE} is the base-emitter voltage, k is Boltzmann's constant and n_{iE}^2 is the intrinsic carrier concentrations in the emitter and it is given by the equation (3.5).

$$n_{iE}^2 = N_{CE}N_{VE}\exp\frac{-E_{gE}}{kT} \tag{3.5}$$

Where, N_{CE} and N_{VE} are the density of state in the conduction and valence bands in the emitter layer, respectively. $E_{gE}$is the band gap of the emitter layer. Inserting (3.5) into (3.4) leads to equation (3.6).

$$I_B = qA \exp\frac{qV_{BE}}{kT}\left[\frac{D_{PE}N_{CE}N_{VE}}{W_E N_{dE}}\right]\exp\left[\frac{-E_{gE}}{KT}\right] \tag{3.6}$$

According to the equation (3.6), the base current is inversely proportional to the band gap of the emitter layer E_{gE}. The sSi HBT is formed from a relaxed SiGe (collector), a compressed SiGe (base) and a tensile strained Si, which serves as the emitter. The strained Si has a smaller band gap compared with relaxed Si which increases the intrinsic carrier concentration [31, 32]. This results in the sSi HBTs having a higher base current compared with the other devices. The emitters in both the Si BJTs and the SiGe HBTs are formed from relaxed Si.

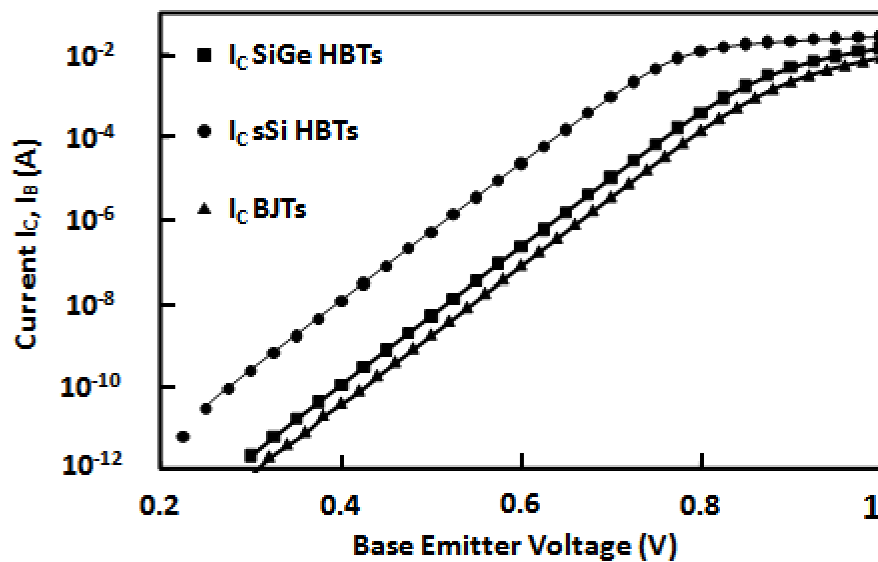

Figure 3.15: Collector current for sSi HBTs, SiGe HBTs and Si BJTs @ V_{BC} =0 V. W_E=1 μm and L_E=10 μm.

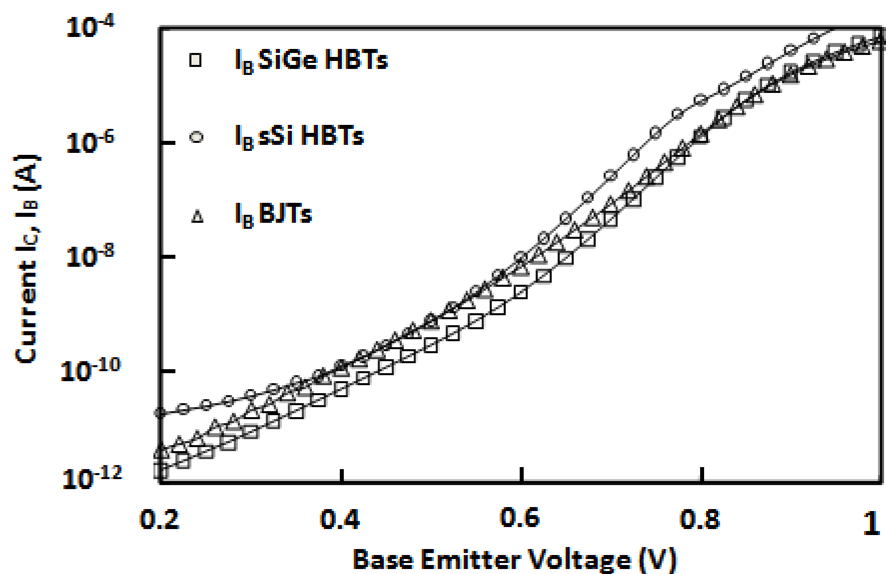

Figure 3.16: Base current for sSi HBTs, SiGe HBTs and Si BJTs @ V_{BC} =0 V. W_E=1 µm and L_E=10 µm.

3.10 Current gain

The current gain is calculated from the ratio of the collector current and the base current. Figure 3.17 shows a plot of current gain β as a function of base-emitter voltage V_{BE} at V_{CB}=0. It is plotted on a logarithmic scale and shows that the maximum value of β is 3700, 334 and 135 for the strained Si HBTs, SiGe HBTs and Si BJTs respectively. This represents an improvement in the gain of the sSi HBTs by 11x compared with the conventional SiGe HBTs and an improvement of 27x compared with the conventional Si BJTs. Figure 3.17 also shows that the maximum current gain is achieved at lower V_{BE} for the sSi HBTs. In other words the amplitude of the input signal needed for the sSi HBTs in order to operate (at maximum β) is low compared to the other devices. This advantage makes sSi HBTs ideal for amplifier circuits.

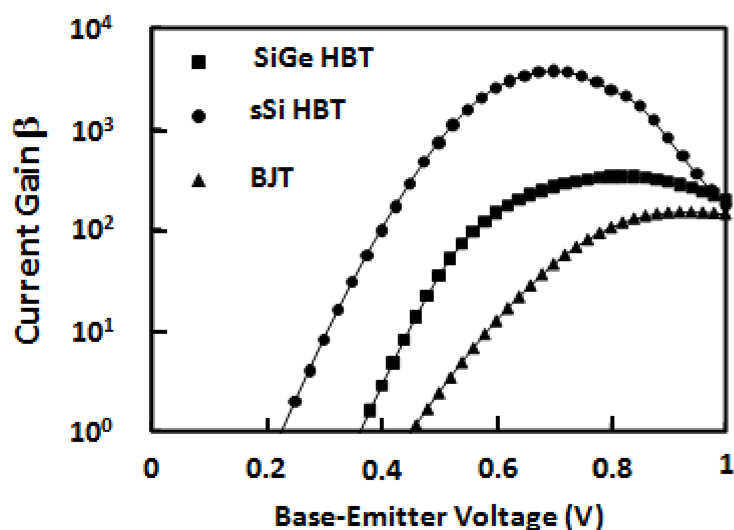

Figure 3.17: Current gain vs. V_{BE} for sSi HBTs, SiGe HBTs and Si BJTs.

3.11 Ideality Factor

The ideality factor is an important parameter that reflects the mechanisms behind the collector and base currents. Figure 3.18 shows the flow of electrons and holes in a bipolar transistor in the common-emitter configuration. As the electron leave the emitter some inevitably recombine with holes in the emitter-base junction (A), remaining electrons diffuse toward the collector, however small amount of the electrons recombine before reaching the collector-base depletion region (B). Negligible recombination can occur in this region because the high electric field. For the base current, the holes are injected from the base to the emitter, part of these holes recombines in the emitter- base junction (C). The remaining holes diffuse to the polysilicon emitter. In ideal operation, the drift and diffusion mechanisms should be predominating and therefore the ideality factor is equal to 1. The ideality factor of the collector current is found to be equal to 1 for all devices, demonstrating that the diffusion mechanism is causing the collector current. The ideality factor for the base current is 1.4 for the strained Si HBTs, 1.2 for the SiGe HBTs, and 1.4 for the Si BJTs. It is almost very difficult to achieve base current with ideality factor of 1; this is because the imperfection and impurities in the bulk and at the interfaces [33].

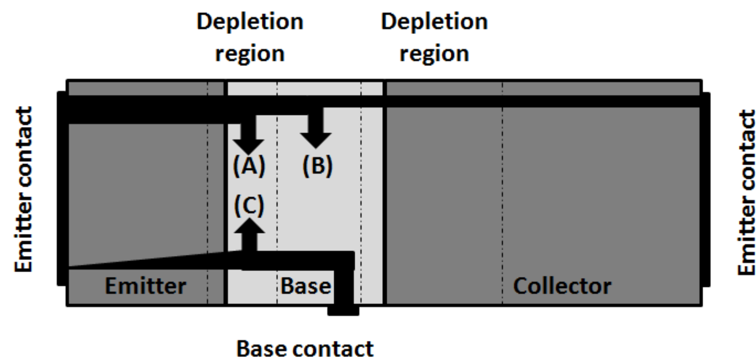

Figure 3.18: Current component in an NPN bipolar transistor operating in the common-emitter mode.

3.12 Emitter-base diode

Figure 3.20 presents the emitter-base characteristic. In the forward bias regime, three regions can be observed. In the first region (A), the current is higher than expected; this is caused by a recombination of the carriers which particularly occurs in the depletion region. Since this contribution to the current is small it can be seen only at low current. In the region (B) the current is mainly caused by the diffusion of the minority carriers. The third region (C) shows current saturation; this saturation is caused by the series resistance [34]. The emitter-base diode associated with the sSi HBTs device exhibits a high current compared with the emitter-base diodes of the other devices; also the diode associated with the SiGe HBTs shows a high current compared with a Si-based diode (Si BJTs). This increase of the current is due to incorporation of the Ge in the anode (base layer) which causes an enhancement in the intrinsic carrier concentration [35].

When the electric field across a reverse-biased p-n junction approaches 10^6 Vcm^{-1}, the n-side conduction band appears opposite to the p-side valence band as shown in the Figure 3.19. This is lead to a significant current flow caused by tunnelling of electrons from the valence band of the p-type region into the conduction band of n-type region. The tunnelling current density is given by equation (3.7) [36].

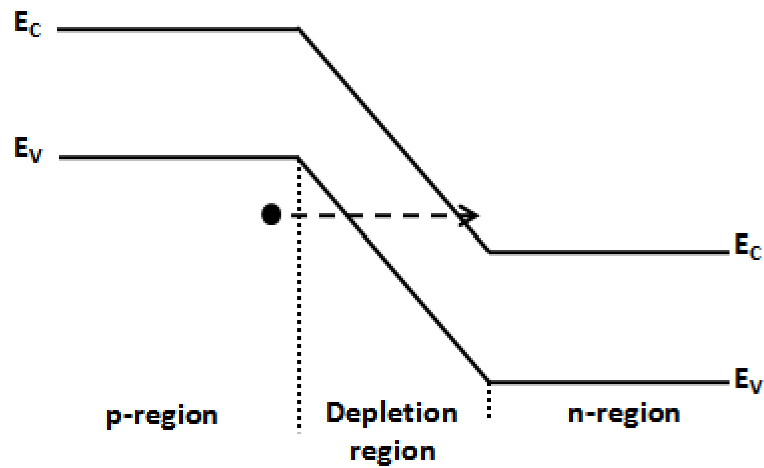

Figure 3.19: Schematic illustration band-to-band tunnelling in p-n junction under reverse bias.

$$G_{BTBT} = \frac{q^2 m_e^{0.5} \varepsilon^2}{18\pi\hbar^2 E_g^{0.5}} \exp\left(-\frac{\pi m^{0.5} E_g^{1.5}}{2\hbar q \varepsilon}\right)^{2/3} \tag{3.7}$$

Where q the electronic charge, m_e is is the electron mass, ε is the electric field, E_g is the band-gap and $\hbar$ is the reduced Planck's constant.

This equation suggests that reduction of the band-gap should lead to an increase in the tunnelling current. This is consistent with Figure 3.20, which shows that the base-collector diode associated with the sSi HBTs exhibits the highest current since the band gap of the SiGe reduces with the increase of the Ge content [37].

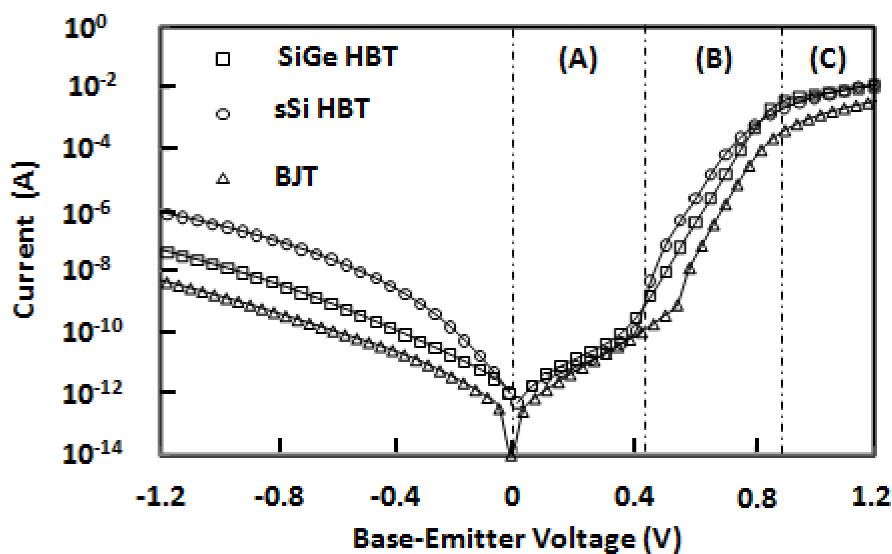

Figure 3.20: Emitter base diode characteristic.

3.13 Collector base diode

Figure 3.21 illustrates the base-collector diode characteristic for all devices. The base-collector diode associated with the Si BJTs and SiGe HBTs exhibit similar characteristics except at high voltage (over 0.8 V), where the base-collector diode associated with the SiGe HBTs is higher. For the sSi HBTs base-collector diode, the high forward current is due to the high intrinsic carriers concentration associated with the SiGe layer. The ideality factor is highest for the sSi HBTs base-collector diode and lowest for Si BJTs base-collector diode. This is most likely due to the larger number of defects in the strained Si HBTs, associated with the SRB [38]. Under reverse bias the sSi HBTs base-collector diode shows a high tunnelling current; this is due to the low band gap of the SiGe layer.

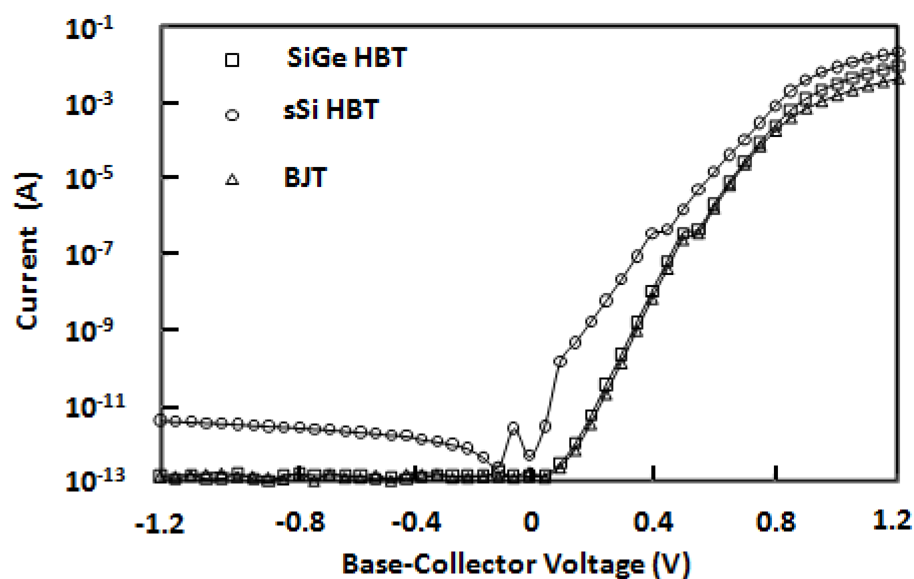

Figure 3.21: Collector-base diode characteristic.

3.14 Common emitter characteristic

The sSi HBTs exhibit a high collector current which results in high power dissipation. This power is translated into heat, mainly in the base collector depletion region, where the current and the electrical field are high [39]. The thermal conductivity of the SiGe layer is known to be small compared to Si [40]. The high power dissipation and the low thermal conductivity of SiGe in the SRB result in an excessive increase of the temperature. The high temperature causes a strong lattice vibration which decreases the electron/hole mobility leading to a reduction in the collector current as shown in Figure 3.22 [41]. This effect is recognized as being due to self-heating. The strained Si MOSFET on SRB is also known to

exhibit this phenomenon [42, 43]. However, self-heating can be reduced using thin instead of thick SRB [44].

A comparison of the common-emitter characteristics for sSi HBTs, SiGe HBTs and Si BJTs at I_B= 3µA is shown in Figure 3.23. The collector current in the sSi HBTs is 7x larger than in the SiGe HBTs and 22x larger than in the BJTs at a collector-emitter voltage of V_{CE} = 1 V. Clearly, Si BJTs and SiGe HBTs do not exhibit self-heating. If the self-heating in the sSi HBTs were to be reduced, then the enhancements in I_C would be even larger. Figure 3.24 and Figure *3.25* represent the common characteristics for SiGe HBTs and Si BJTs. No effect of self-heating was observed. The extracted Early voltage (V_A) for the Si BJTs and SiGe HBTs were 6.0 V and 1.6 V, respectively. The reduced V_A is due to the base modulation.

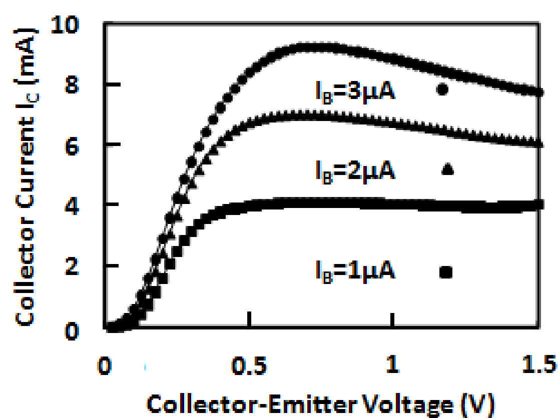

Figure 3.22: Collector current I_C vs. V_{CE} (transfer characteristics) for the sSi HBTs.

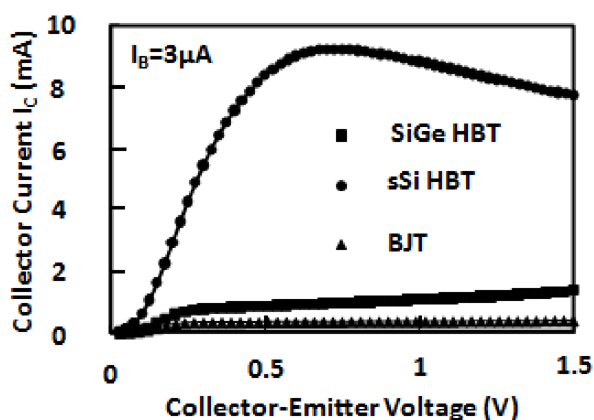

Figure 3.23: Comparison of the collector current I_C VS. V_{CE} for sSI HBTs, SiGe HBTs and Si BJTs.

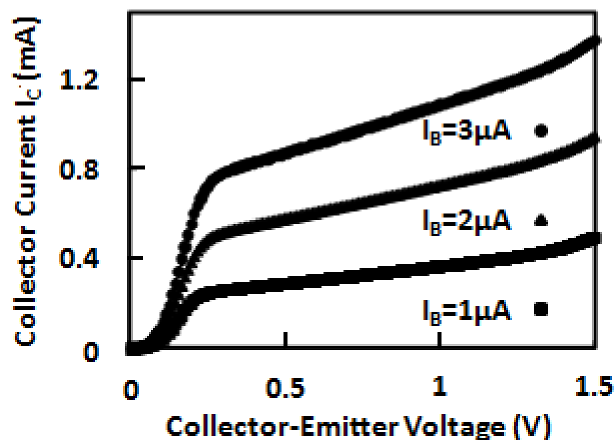

Figure 3.24: Collector current I_C vs. V_{CE} (transfer characteristics) for the SiGe HBTs.

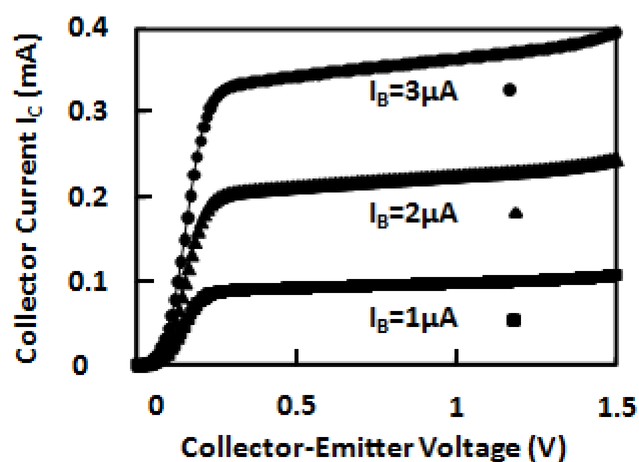

Figure 3.25: Collector current IC vs. VCE (transfer characteristics) for the Si BJTs.

3.15 Break down voltage

The breakdown mechanisms (Avalanche & Tunnelling) of a bipolar transistor are similar to that of a PN junction. Since the base-collector junction is reversed biased, it is this junction where breakdown typically occurs. Just like for a PN junction, the breakdown mechanism can be due to either avalanche multiplication or tunnelling. Since the doping of the collector in these devices does not exceed 10^{18} cm^{-3}, the breakdown phenomenon is dominated by avalanche multiplication. The electric field in the space-charge region of the collector base junction is large. Electrons injected from the emitter drift to the collector through the collector base space-charge region. For a sufficiently high electric field, electrons can gain enough energy from the electric field to create an electron-hole pair upon impact with the lattice. This carrier generation process is known as “impact ionization”. Electrons and holes generated by impact ionization can subsequently acquire energy from the strong electric

field, and create additional electron-hole pairs by further impact ionization [45]. This process of multiplicative impact ionization is known as "avalanche multiplication". This breakdown is not destructive. However, the high voltage and rapidly increasing current do cause large heat dissipation in the device, which can cause permanent damage to the semiconductor. The Figure 3.27 (a) illustrates the circuit used to measure the BV_{CB0}, the base-collector junction is reversed biased while the emitter is open circuit.

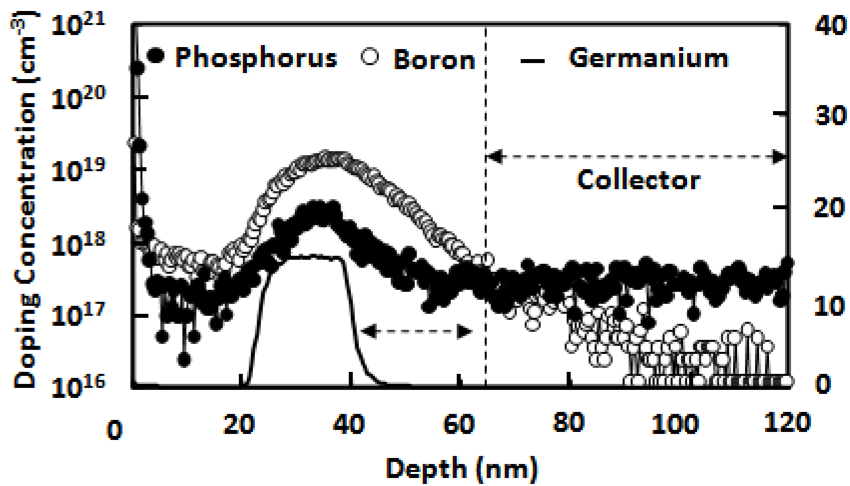

Figure 3.26: Phosphorus, Boron and Ge Box profile for SiGe HBTs. The collector-base junction is located deep in the Si Collector layer.

The Figure 3.26 shows the SIMS profile for SiGe HBTs. The collector-base junction is located deep in the Si collector layer and even at high reversed biased collector-base junction; the depletion region will still be allocated at the Si layer. Thus impact ionization occurs mostly in the Si region, resulting in the BV_{CB0} being equal for Si BJTs and SiGe HBTs (6.6 V), as shown in Figure 3.28. However, the breakdown voltage BV_{CB0} is 7.2 V for sSi HBTs, which is higher than both SiGe HBTs and Si BJTs.

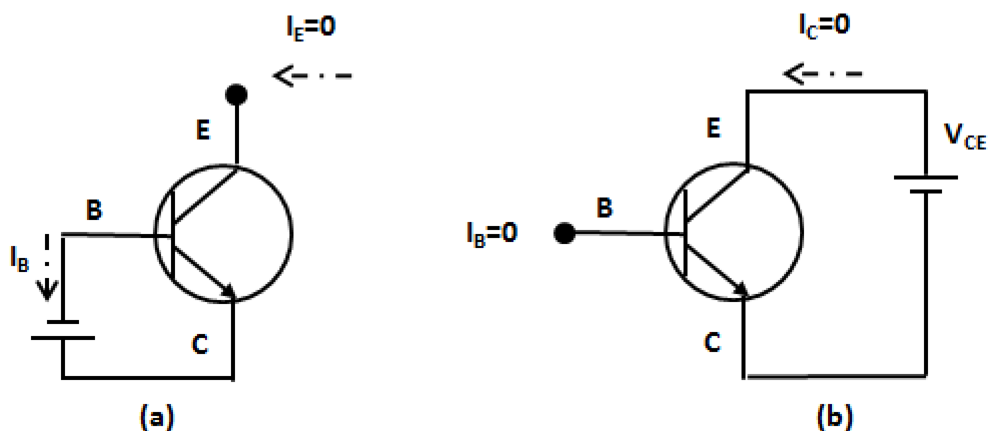

Figure 3.27: Circuit used for measuring BV_{CB0} (a) and BV_{CEO} (b)

The $BV_{CEO,}$ measured at base open (Figure 3.27 (b)), were found to be 2.5, 2.7 and 4.5 V for sSi HBTs, SiGe HBTs and Si BJTs, as illustrated in Figure 3.29. In this case the avalanche breakdown of the base-collector junction is further influenced by transistor action in the common-emitter mode of operation, since the holes generated by impact ionization are pulled back into the base region which results in an additional component of base current. This additional base current causes an even larger flow of electrons through the base and into the collector due to the current gain of the device. This current is larger for sSi HBTs, since it exhibits the highest current gain, compared to Si BJTs and SiGe HBTs. This larger flow of electrons in the base collector junction causes an even larger generation of electron-hole pairs which causes the sSi HBTs to have a small BV_{CEO}. The breakdown mechanism prove the relationship between the current gain and BV_{CEO} [46]. According to the experimental values for the breakdown, the BV_{CB0} is higher than BV_{CEO}, as reported by others [47]and is consistent with equation (3.8) [48].

$$BV_{CEO} = \frac{BV_{CBO}}{(\beta + 1)^{1/m}} \tag{3.8}$$

The figure of merit $\beta \cdot BV_{CEO}$ describes the ability to offer simultaneously high β and high BV_{CEO} for given device.[49]. The sSi HBTs exhibited a much higher $\beta \cdot BV_{CEO}$ (9250 V) than both the SiGe HBTs (900 V) and the Si BJTs (600 V). The $\beta \cdot BV_{CEO}$ for sSi HBTs is 15x that of Si BJTs, which confirms that sSi HBTs is a good platform for high performance HBTs.

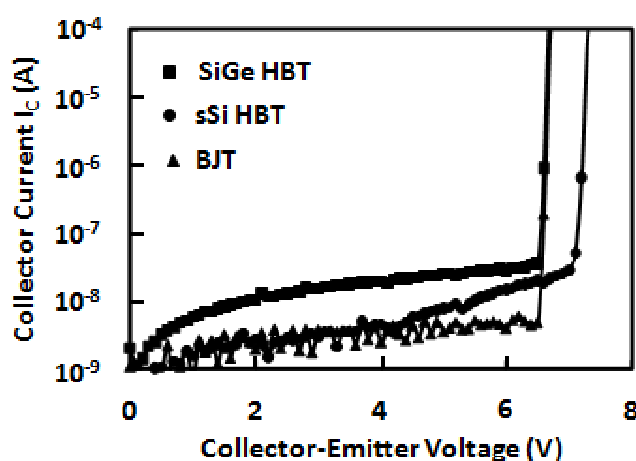

Figure 3.28: Collector-base breakdown voltage with the emitter open circuit BV_{CBO}.

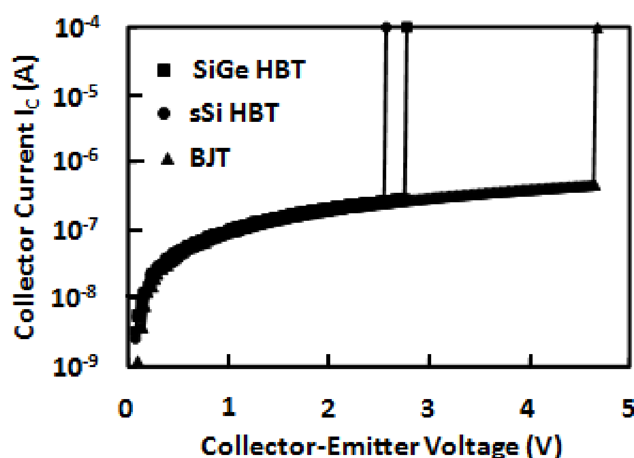

Figure 3.29: Collector-emitter breakdown voltage with the emitter open circuit BV_{CEO}.

3.16 Impact of parameter design space

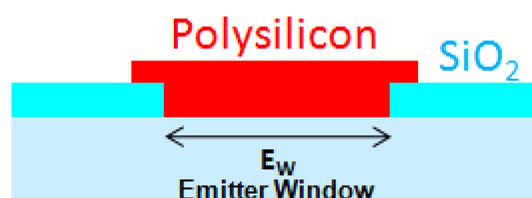

Figure 3.30: Schematic diagram showing the Polysilicon emitter and the emitter window.

Figure 3.30 shows the polysilicon emitter region. The low-doped emitter layer was epitaxially grown ($5{\cdot}10^{17}$ cm^{-3}). The thickness of the grown layer is 30nm. LTO deposition (400nm) followed by etching is used to define the emitter window E_W. A polysilicon doped by in-situ doping was then deposited. During the RTA step the N type dopant diffuses from the polysilicon to form the heavy doped emitter region. The emitter window should be cleverly designed since a large E_W risks having a direct contact between the N^+ emitter region and the P^+ extrinsic base. This will cause the emitter-base junction capacitance to be high [50]. Devices with 0.5 µm, 1 µm, 2 µm and 3 µm have been fabricated to assess the impact of E_W on the collector and base current of the devices. Figure 3.31 illustrates the variation of I_C and I_B versus E_W for all devices at V_{BE}=0.7 V. It is plotted on a logarithmic scale and shows that I_C and I_B increase with increasing E_W. Equations (3.1) and (3.4) represent I_C and I_B respectively. The only parameter that appears in both equations is the area A; an increase of this parameter leads to an increase of both currents. This suggests that the effective area of the device is controlled by E_W and not W_M the mesa length. For further investigation of this finding, two devices with different E_W (0.5 µm and 3 µm) were simulated in Taurus-Medici.

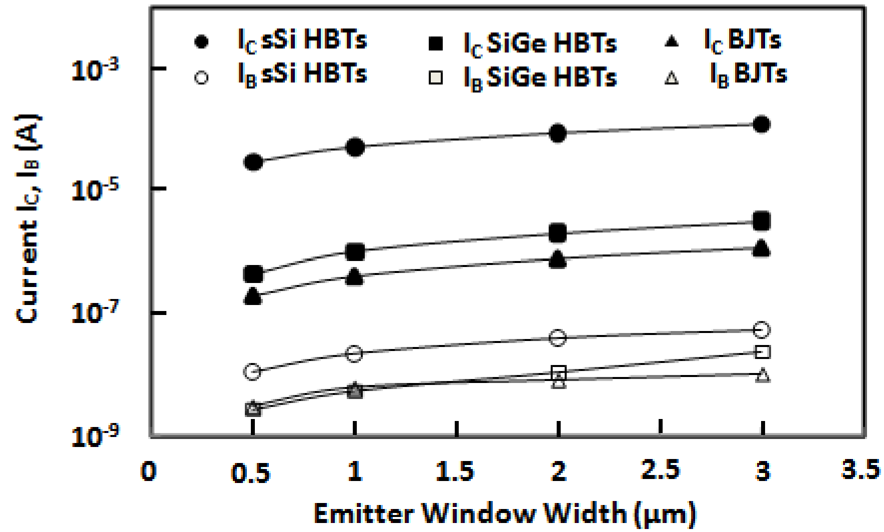

Figure 3.31: Collector and base current for sSi HBTs, SiGe HBTs and Si BJTs vs. E_W (L_E=1)

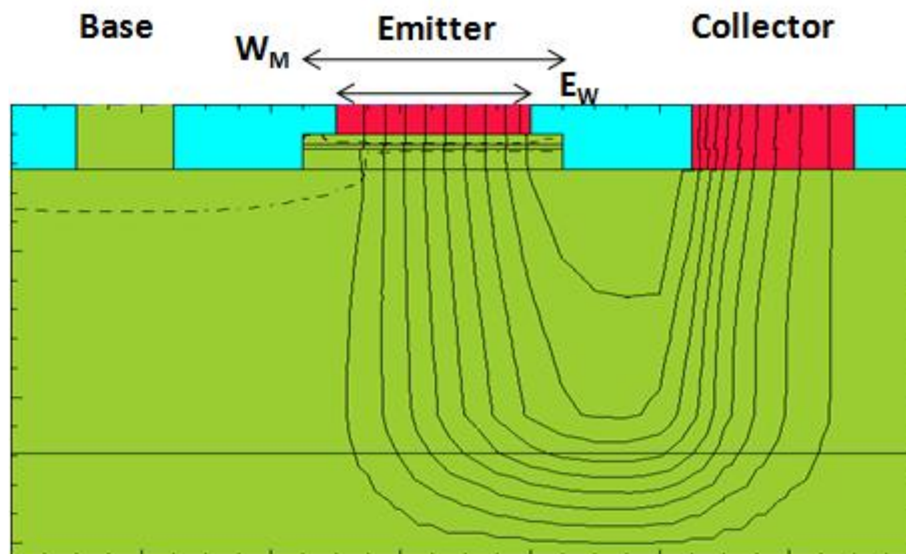

Figure 3.32: Current flow line using Taurus-Medici, W_E=0.5 μm.

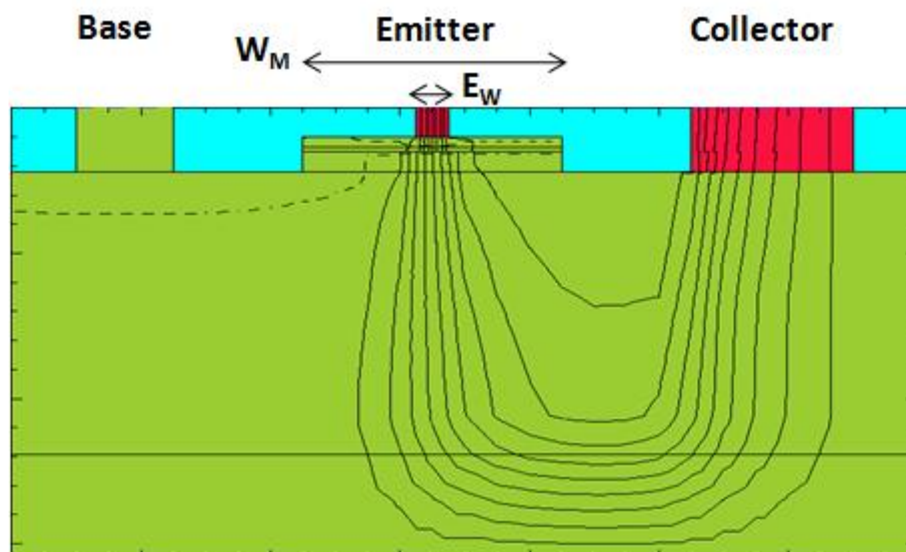

Figure 3.33: Current flow line using Taurus-Medici, E_W=0.5 µm.

Figure 3.32 and Figure 3.33 represent the current flow line at V_{BE}=0.8 V and V_{BC}=0 V for two devices with 0.5 µm and 3 µm emitter width respectively and the same value of W_M. the current flow line shows that the actual width of the intrinsic part of the device depends on E_W; it is slightly bigger than E_W. This demonstrates that the intrisic area of the device is proportional to W_E. This explains the electrical results presented by Figure 3.31, which shows both I_C and I_B increasing with the increase of E_W.

In order to invistigate the impact of emitter window length L_E (perpondiculaire on Figure 3.34) on the performance, Devices were fabricated with different value of L_E. Figure 3.36 illustrates this effect on the performance of all devices. The collector and base current raises with the increase of the emitter window length. This indicates that the length of the intrinsic area of the device is proportional to the emitter window length. To conclude, the intrinsic area of the device is determined by mainly the area of the emitter window.

While L_E and E_W were found to have an impact on the devices performance, D1, distance to the collector and D2 (Figure 3.35), distance to the base show no clear effect on the collector and base current. However these parameters will probably have an impact on the speed of the device, since the exitrince capacitance will be affect by the value of D1 and D2.

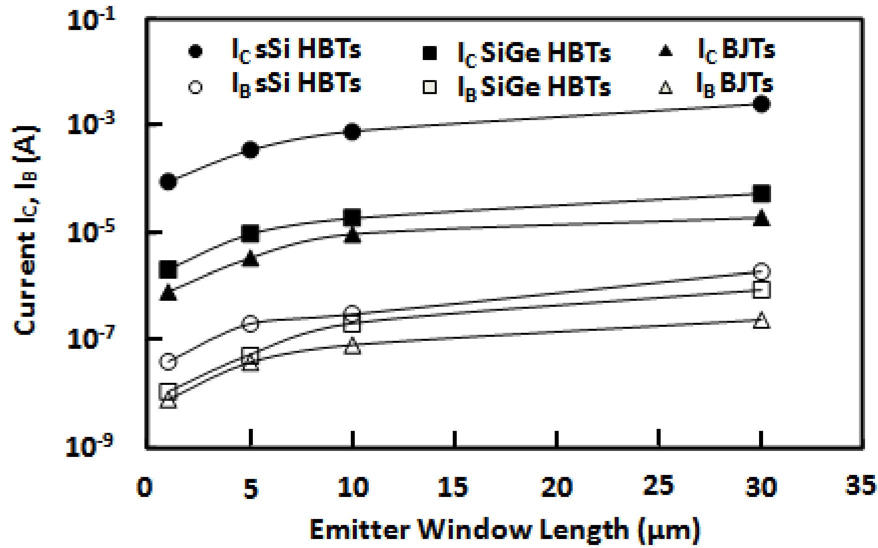

Figure 3.36: Collector and base current for sSi HBTs, SiGe HBTs and Si BJTs vs. L_E (E_W =2 µm)

3.17 Benefit of sSi HBT structure

The trade-off between the current gain and the maximum frequency of oscillation is an important issue in the design of Si BJTs. The current gain is known to be inversely proportional to the base doping, as shown in the equation (3.9) [51]; however, a low base doping leads to a high base resistance which causes a decrease in the maximum frequency of oscillation [52]. The sSi HBTs provides the flexibility to trade off its current gain to enhance the maximum frequency of oscillation.

$$\frac{D_{nb} W_E N_E}{D_{pe} W_B N_a} \tag{3.9}$$

Where D_{nB} is the diffusion coefficient of electron in the base, W_E is the emitter width, N_E is the donor concentration in the emitter, D_{pe} is the diffusion coefficient of holes in the emitter, W_B is the base width and N_a is the acceptor concentration in the base.

The compatibility of SiGe HBTs with conventional CMOS fabrication enables high levels of integration that make SiGe BiCMOS technology a cost effective solution for many applications [53]. However, the integration of SiGe HBTs with the current strained Si/SiGe MOSFETS is not possible. Recent theoretical and experimental studies reveal that strained Si/SiGe MOSFETs outperform their conventional Si-based counterparts, owing to enhanced carrier transport through strained channel layers [54]. Using SRB in the fabrication of sSi

HBTs and strained Si/SiGe MOSFET offers the possibility of integrating both devices, leading to new improvements in BiCMOS technology.

3.18 Deviation in the electric performance

As Semiconductor devices shrink to nanometer design rules, each process margin for manufacturing devices becomes tighter and tighter. With the wafer area getting larger (300mm wafers), radially dependent process variation is becoming a more serious issue. It is well-known how important it is to control and optimize the uniformity during process steps such as CMP, photolithography, and etching. It is routinely observed that a lot of process variation is radially distributed across a wafer in single wafer manufacturing equipment, often resulting in serious device parameter variation and or yield loss near the edge [55].

The cross-wafer variation in performance (maximum β) was mapped in order to identify whether there was a region of the wafer causing lower performance and also to determine the impact of RTA on the current gain. The maximum current gain was measured using an Agilent 4155c parameter analyser. The devices were located in the same position (i.e. the same size) on the die for all wafers.

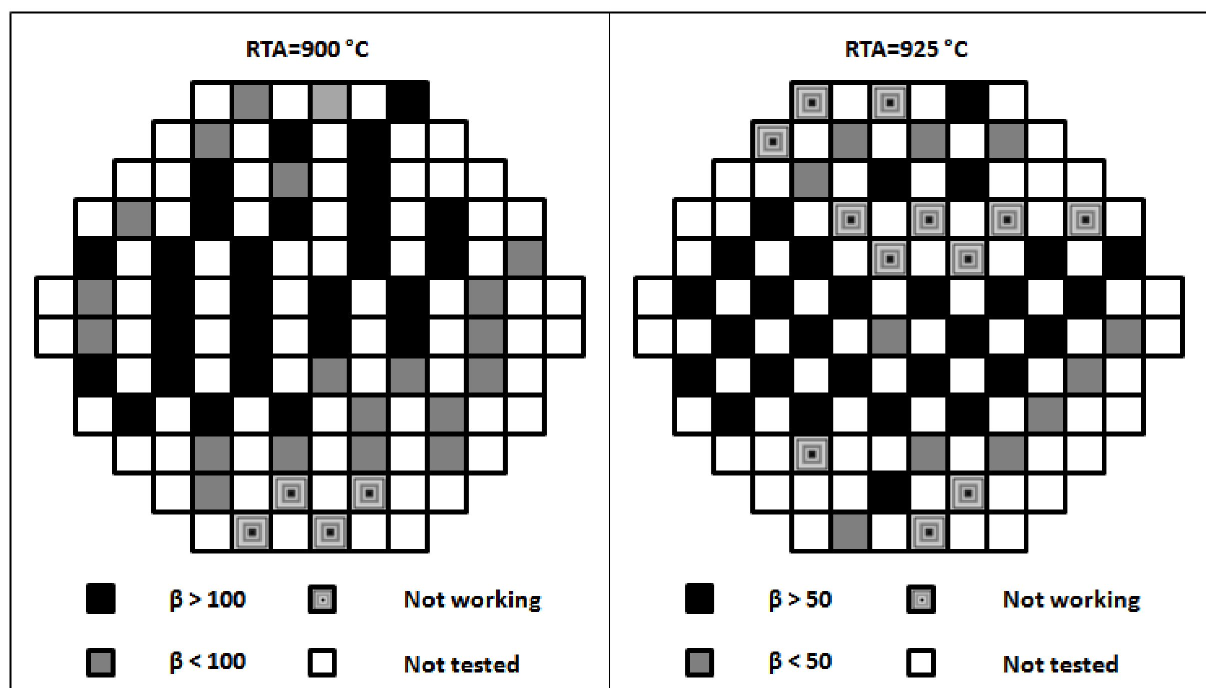

Figure 3.37: Wafer map indicating the location of the best performing (highest current gain) Si BJTs annealed at 900°C and 925 °C.

By mapping the position of the best performing devices (highest current gain), it was found that those devices are located at the wafer centre while the poorer performing ones are situated on the edge of the wafer. In order to optimise the doping drive-in from the poly to the emitter, a batch split was included, with either the 900 °C or a 925 °C anneal for 10s. A maximum current gain which is higher than 100 is the criteria used to determine the best performing devices among the devices annealed at 900 °C for 10 s. This was not the case for devices annealed at 925 °C for 10 s, where the best performing devices are considered to exhibit a maximum current gain which is higher than 50. This difference was driven by the dissimilarity in the performance between devices annealed at 900 °C and 925 °C. Only 5 devices were found to exhibit a maximum current gain over 100 among the devices annealed at 925 °C. In addition the figure Figure 3.37 shows that the number of failed devices is higher in this batch compared to the batch where that RTA was 900 °C. This difference in the performance shows the importance of choosing the optimum annealing temperature. Rapid thermal-annealing is used to activate the dopant and remove the implant damage. This processing step causes redistribution of the dopant, which is undesirable.

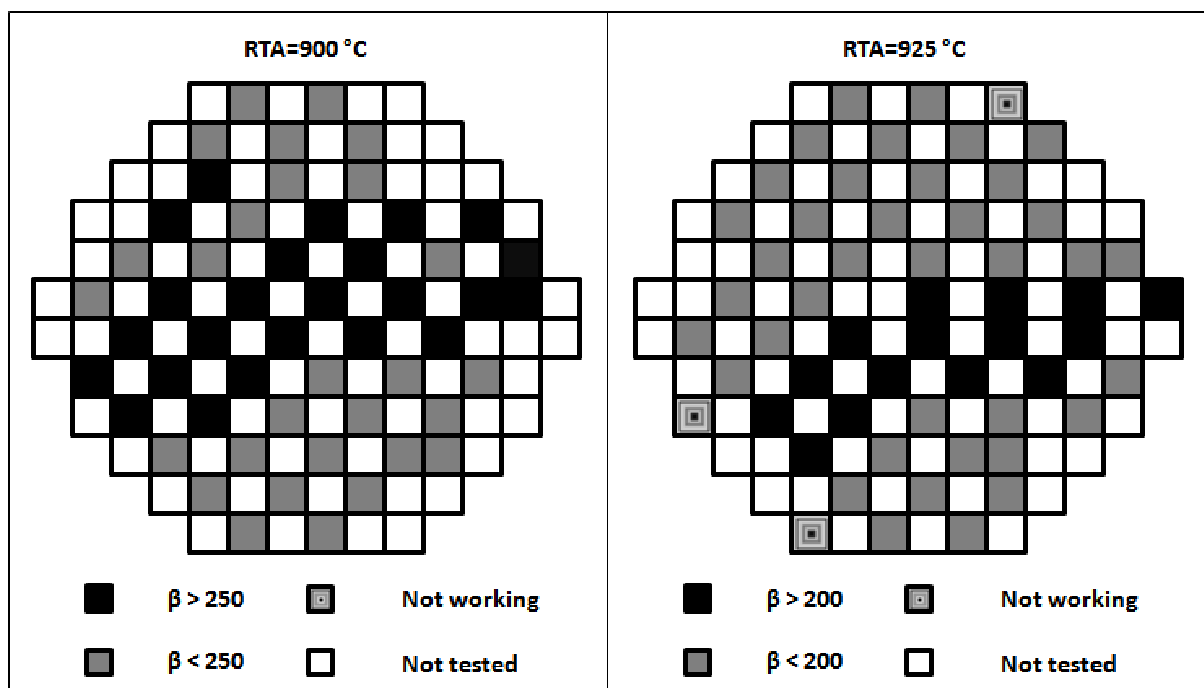

Figure 3.38: Wafer map indicating the location of the best performing SiGe HBTs annealed at 900°C and 925 °C.

Figure 3.38 shows the cross-wafer variation for SiGe HBTs annealed at 900 °C and 925 °C. The best performing devices for the batch annealed at 900 °C are located in the centre of the wafer, while the poorer performing ones are situated at the edge. For the batch annealed at 925 °C, the best performing devices are mostly situated in the bottom part of the wafer. This suggests that the origin of the degraded performance is likely to be a result of processing error since uniform processing tends to result in the best devices located in the wafer centre. Also fewer devices are reported to be not working; these devices are located in the edge of the wafer. In addition, the figureFigure 3.38 shows that the SiGe HBT devices annealed at 900 °C exhibit higher maximum current gain compared to the SiGe HBT devices annealed at 925 °C.

The sSi HBT wafer map in the figureFigure 3.39 shows that the best performing devices in the batch annealed at 900 °C were located randomly across the wafer, in contrast, the best sSi HBTs devices in the batch annealed at 925 °C are located in the centre. Also, annealing the sSi HBTs at 900 °C results in much lower current gain, and a higher number of failed devices compared to sSi HBTs devices annealed at 925 °C. This shows that 925 °C is the optimum annealing temperature for sSi HBT devices.

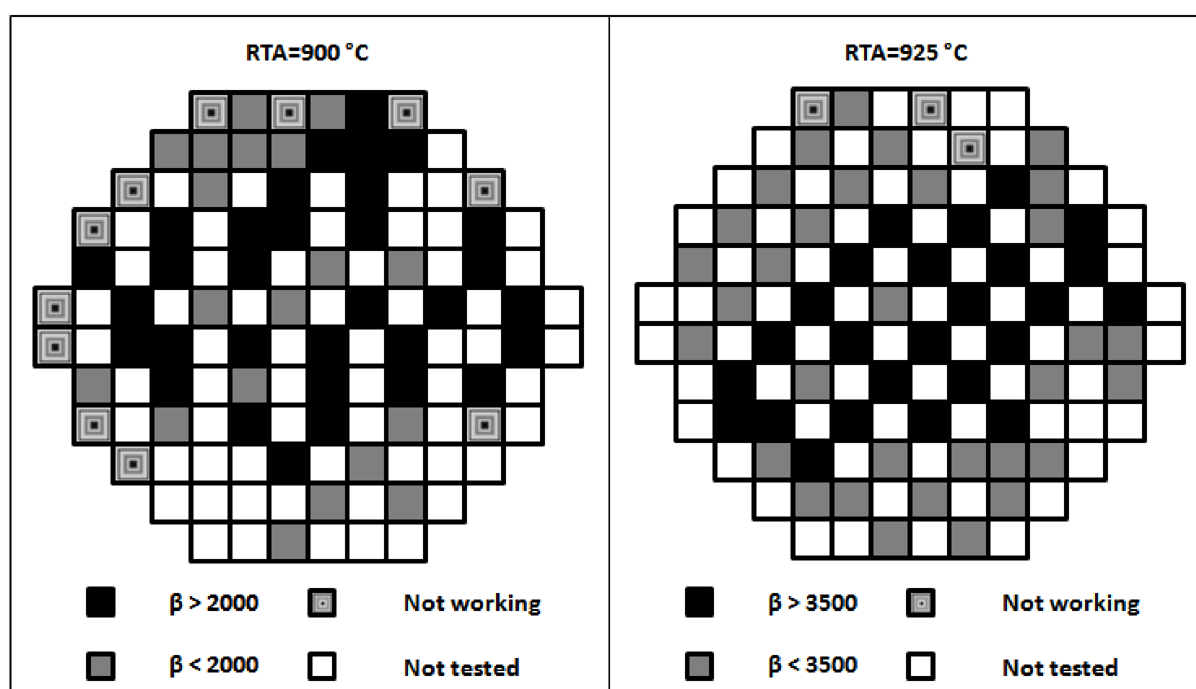

Figure 3.39: Wafer map indicating the location of the best performing sSi HBTs annealed at 900°C and 925 °C.

A histogram of the maximum current gain of all devices (i.e. Si BJTs, SiGe HBTs and sSi HBTs) annealed at 900 °C and 925 °C is shown in the figure Figure 3.40. The cross-wafer uniformity is reasonable even for the sSi HBTs devices. The 900 °C split exhibited better cross-wafer uniformity.

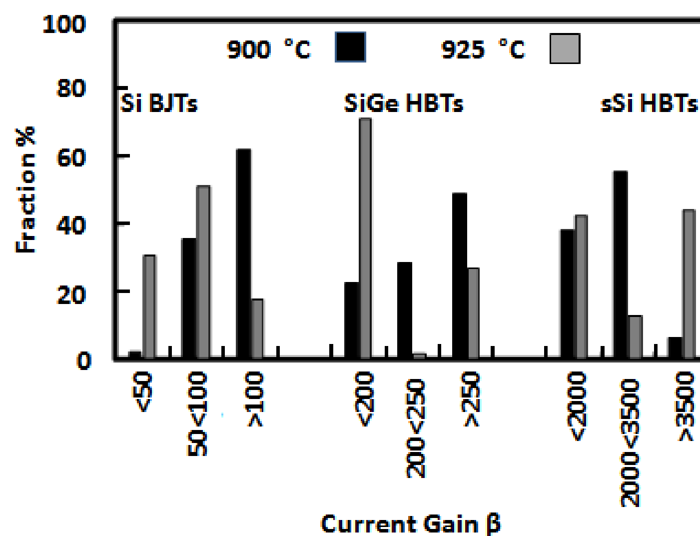

Figure 3.40: Histogram of the current gain for Si BJTs, SiGe HBTs and sSi HBTs annealed at 900 °C and 925 °C.

However, the 925 °C split shows higher maximum current gain for sSi HBTs. The histogram in the figureFigure 3.41 shows that for the 925 °C split, over 40 % of the measured sSi HBTs devices exhibit a maximum current of over 3500 , this percentage is as small as 0.06 % for the sSi HBTs annealed at 900 °C. For Si BJTs, over 60 % of the devices annealed at 900 °C show a maximum current gain which is higher than 100, this percentage has decreased to 17 % for Si BJTs devices annealed at 925 °C.

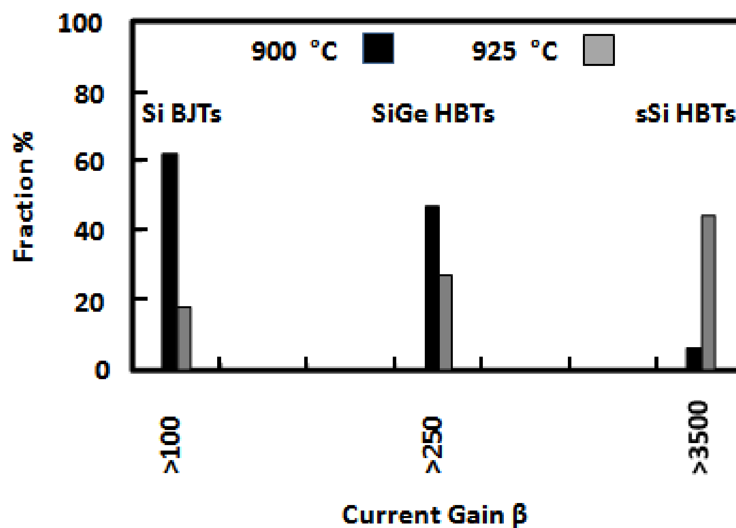

Figure 3.41: Histogram of the current gain for Si BJTs, SiGe HBTs and sSi HBTs annealed at 900 °C and 925 °C.

3.19 Conclusion

This chapter has focused on the material and electrical characterisation of sSi HBTs and compared the results with the co-processed SiGe HBTs and Si BJTs. Using a strain-relaxed buffer to grow strained-Si in the channel has lead to significant improvement in the performance of the bipolar transistor. This is the first time that a strained-relaxed buffer has been used to improve SiGe heterojunction bipolar transistor, through the increase of the amount of Ge incorporated in the base. The target doping level and Ge content were confirmed using different characterisation methods, leading to the first experimental demonstration of sSi HBTs. The Raman spectroscopy method has been used to examine the strain in different layers of all devices. An important outcome is confirmation that the strain in the emitter of the sSi HBTs was fully maintained following processing. The sSi HBT has improved the possibility of integrating strained Si CMOS and sSi HBTs in one chip. This was not possible using SiGe HBTs.

In addition to the advantages of the structure of sSi HBTs. The electrical characterisation shows that this novel device exhibit a maximum current gain of 3700 compared with 334 for co-processed SiGe HBTs and 135 for the Si BJTs. Moreover, the maximum current gain is achieved at lower V_{BE} for the sSi HBTs, which demonstrates high performance with low power consumption of this device. This advantage makes the sSi HBTs ideal for portable communications devices since it results in greater battery lifetimes.

The low base resistance is an important factor to improve the f_{max}, also the BV_{CEO} is a vital parameter to assess the capability of the device to operate at high voltage. Since there is a trade-off between these two factors and the current gain, it is possible to decrease the current gain to increase both R_b and BV_{CEO} while maintaining sufficient current gain.

This chapter has demonstrated good DC performance of the sSi HBTs compared with the Si BJTs and the SiGe HBTs. This is the first step towards the fabrication of sSi HBTs optimised for RF performance.

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Chapter 4. 2D simulation study of sSi HBTs

4.1 Introduction

The use of TCAD software has experienced a major shift in the last decade. Tools such as semiconductor device and process simulators are no longer viewed as research tools available only to university scientists and industrial researchers. As powerful workstations are easily accessible, device and process simulations have become a routine exercise for engineers to conduct the process integration, device analysis, circuit characterization and yield optimization. The proliferation of TCAD tools has a significant economical impact on the semiconductor industry. First, the shortening of the design-to-manufacture time for new products mandates a rapid design cycle for bringing up new technologies. An effective use of TCAD tools saves much experimental time for calibrating process and device parameters and minimizes the number of the trial-and-error iterations. Second, the skyrocketing cost of modern IC fabrication facilities forces engineers to re-evaluate the methodology for new technology development. Advanced simulation capability greatly reduces the cost by detecting design flaws in the early design stage and achieving optimal solutions through parameter calibration. Currently, process and device simulation has established itself as an indispensable tool for developing and optimising device and microelectronic process technologies in the R&D phase.

The main outcome of the last chapter is that sSi HBTs exhibit high performance compared to SiGe HBTs and Si BJTs. The outperformance of sSi HBTs has been linked to the Ge content in the base, which has enhanced the intrinsic carrier concentration and therefore the collector current. In order to validate this explanation, 2D simulations have been performed using MEDICI (now available from Synopsys). This tool was chosen because of its capability to simulate the changes in physical parameters that occur in the SiGe system i.e. band-gap, density of states, electron affinity. The most important part of the simulation is to include the right models for the simulated device. In this simulation study, several models have been included such as band-gap narrowing, concentration dependent mobility, thermionic field emission. A discussion of the important of these models is also presented.

4.2 Physical model

Numerical analysis based on the fundamental equations governing semiconductors has become necessary in IC technology development, and is often referred to as "device simulation”. MEDICI is part of a technology computer-aided-design (TCAD) package, which includes process simulation, device simulation, and parameter extraction programs[1]. The use of a device simulator or TCAD tools in general, requires substantially more knowledge of the internal workings of the simulator than the use of, say, a circuit simulator such as SPICE. For instance, users must choose which mobility model to use, which statistics (Fermi-Dirac or Boltzmann) to use. The default physical models are usually the simplest ones, and often give inaccurate results, particularly for advanced device technologies such as SiGe.

As was mentioned earlier, choosing the right model in the simulation is fundamental in the calibration process. Each device has its own mobility model that is suitable to its operation method. Mobility is a measure of the time interval between collisions for a carrier moving through a semiconductor lattice. The two most important collision mechanisms in bipolar transistors are lattice and impurity scattering, and the total mobility is given by the sum of the probabilities of collision due to these individual mechanisms. Lattice scattering is caused by collision between carriers and the atoms of the semiconductor lattice. These lattice atoms are displaced from their lattice site by thermal vibration, since thermal motion increases with temperature, the mobility decreases with temperature. However, as the doping concentration increases beyond 10^{15} cm^{-3} - 10^{16} cm^{-3}, which is the case in bipolar transistors, the lattice scattering mechanism becomes less important and impurity scattering becomes the major factor in defining the carrier mobility.

The impurity scattering is caused by collisions between carriers and impurity atoms in the semiconductor lattice. An increase of doping will increase the number of collision which will lead to further decrease in the mobility. This impact has been confirmed by experiment and was reported for different semiconductors such as Si, Ge and GaAs [2, 3]. Therefore, it is important to choose the mobility model that reflects the impact of the impurity (doping) on the mobility. The model chosen was the Concentration Dependent Mobility model and it has been added to the simulation by adding the term CONMOB to the model statement.

In lightly doped semiconductors, the dopant atoms are sufficiently widely spaced in the semiconductor lattice, therefore it is reasonable to assume that the dopant atoms have little effect on the perfect periodicity of the semiconductor lattice and therofore on the edge of the valence and conduction bands. However this is not true at heavy doping, where the dopant can perturb the perfect periodicity of the semiconductor and reduce its band-gap. This effect is known as band-gap narrowing. The important effect on the operation of bipolar transistors is that it affects the intrinsic carrier concentration as illustrated by the following equation [4]:

$$n_{ie} = n_i \exp\left({}^{\Delta E_{G,H}}/_{2kT}\right) \tag{4.1}$$

where n_i is the intrinsic carrier concentration at low doping levels, n_{ie} is the intrinsic carrier concentration at high doping level and $\Delta E_{G,H}$ is the band-gap narrowing caused by the doping. Various band-gap narrowing models have been developed for use in bipolar transistor simulation. However, the Slotboom BGN model is the most widely used band-gap narrowing model. This model has been implemented in nearly every major commercial device simulator, including MEDICI [5]. The following equation represents Slotboom model:

$$\Delta E_{G,H} = \Delta E_{G,L} \times \left[\ln\frac{N}{N_0} + \sqrt{\left[\ln\frac{N}{N_0}\right]^2 + C}\right] \tag{4.2}$$

With $\Delta E_{G,L}$=6.92 meV, 1.3×10^{17} cm^{-3} and C=0.5 and N is the doping level.

It is important to mention that based on the above equation the band-gap narrowing in Silicon will occur at doping levels which are higher than about 1.3×10^{17} cm^{-3}. Since the doping level in the device is higher than this value, then it is important to include this effect for an accurate simulation [6].

It is obvious that the incorporation of Ge into Si bipolar transistors, to produce SiGe HBTs and sSi HBTs, has improved the performance of bipolar technology. However, it leads to more defects present in the device. These defects cause energy states to be introduced into the forbidden gap. These energy states act as a stepping stones for the generation and recombination (G-R) of electrons and holes. As was reported in chapter 3, the ideality factor of the base current at low voltage (V_{BE} <0.4 V) is higher than 1. This increase of the ideality factor is caused by the generation recombination phenomenon. Therefore, the AUGER and

CONSRH models have been used to account for the generation–recombination processes, which are only important for the base current at low base voltages (V_{BE} < 0.4 V).

Generally, drift and (or) diffusion mechanism are responsible for the transport of electrons and holes in semiconductor. However, this is true only in continuous media (in the absence of band discontinuity). The energy bands in both the SiGe HBTs and the strained Si HBTs exhibit a discontinuity at the base-collector junction. The electrons must pass this discontinuity through thermionic-field emission or tunnel phenomenon. Therefore, including these phenomena in the simulation is necessary.

4.3 Impact of band-gap discontinuity

The use of energy-gap variation beside electric field to control the force acting on electrons and holes results in greater design freedom. This leads to higher heterostructure performance for microwave and high-speed circuit applications. For abrupt heterojunction bipolar transistors (HBTs), the carrier transport across the heterojunction is controlled by thermionic emission and tunnelling, unlike transport in continuous media, which is governed by drift and diffusion mechanism. Using compositional grading when moving from one side of the junction to other, leads to a reduction of the discontinuity in the energy band. This reduction results in an improvement of the current gain [7].

The band-gap of SiGe is known to be inversely proportional to the amount of the Ge. However, there are other factors that can also lead to this reduction such as strain and high impurity concentration.

As was mentioned earlier, the difference in the band-gap of the material results in the creation of a band-gap discontinuity. The conduction band in both the SiGe HBTs and the sSi HBTs exhibits a discontinuity at the base-collector junction as shown in Figure 4.1.

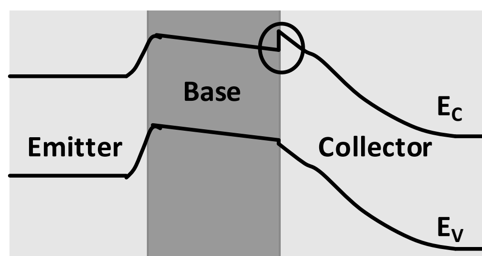

Figure 4.1. Conduction band discontinuity at the collector-base junction

The conduction band discontinuity causes a potential barrier which electrons must overcome through thermionic-field emission (TFE) and tunnelling. This barrier dramatically reduces the effective saturation velocity (v_{eff}) of the carriers at the base-collector interface [8]. In the presence of such a discontinuity in the conduction band, the saturation velocity can be expressed as follow [9].

$$v_{eff} \approx \frac{A^{*}T}{q\sqrt{N_C N_V}} \exp\left(-\frac{r\Delta E_C}{KT}\right) \tag{4.3}$$

where A* is the Richardson's constant and r is a fitting parameter (r < 1), ΔE_C is the conduction band discontinuity, N_C is the conduction band effective density of states and N_V is the valence band effective density of sates. The degradation of the current gain β due to this barrier can be minimised by grading the germanium concentration at the base-collector junction [10]. The impact of the discontinuity on the collector current can be seen in the equation (4.4).

$$I_C = q\frac{\exp\left(\frac{qV_{BE}}{mkT}\right) - 1}{\int_0^{W_B} \frac{N_a\,dx}{D_{nB} n_{iB}^2} + \frac{N_a(W_B)dx}{n_{iB}^2 v_{eff}}} \tag{4.4}$$

where N_a is the doping variation through the base, n_{iB} is the intrinsic carrier concentration in the base, D_{nB} is the electron diffusion coefficient in the base, W_B is the base width. It can be seen from equation (4.4) that the impact of the conduction band edge discontinuity is to reduce the collector current I_C by reducing v_{eff}.

Although, the difference in the band-gap is the source of the conduction and the valence band discontinuity, there are different models which predict the value of these discontinuities based on the difference in the band-gap. The most basic model which used by MEDICI, is given by the following equations:

$$\Delta E_C = \Delta\chi \tag{4.5}$$

Where ΔE_C is the conduction band discontinuity and Δχ is the difference in the electron affinity of the two layers forming the heterojunction.

The valence band discontinuity is calculated using the following equation

$$\Delta E_V = \Delta E_G - \Delta E_C \tag{4.6}$$

where ΔE_V is the valence band discontinuity.

The conduction and valence band discontinuities used in the simulation were found in Ref [11, 12][11, 12][11, 12][11, 12][11, 12][11, 12]. The corresponding heterojunction band alignments were adjusted by the electron affinities χ, taking the affinity of the relaxed SiGe collector layer as a reference for sSi HBTs and the relaxed Si layer as reference for SiGe HBTs. Figure 4.2 and Figure 4.3 illustrate the importance of including this model into consideration. The important information to emerge from these figures is that neglecting the conduction band discontinuity leads to an overestimation of the collector current.

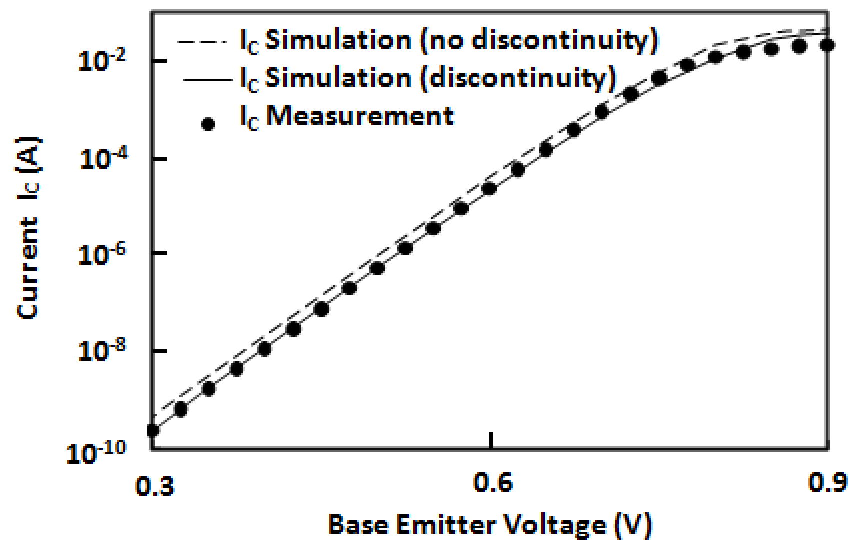

Figure 4.2: Comparison of simulated I_C–V_{BE} characteristics when the conduction band discontinuity is included and not included for sSi HBTs. When it is not included, there is an over-estimation in the collector current.

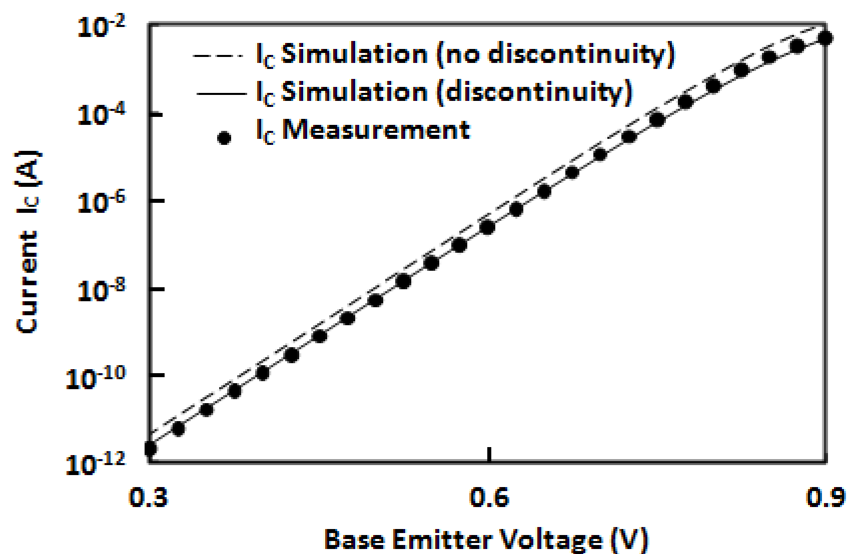

Figure 4.3: Comparison of simulated I_C–V_{BE} characteristics when the conduction band discontinuity is included and not included for SiGe HBTs. There is an overestimation in the collector current, when it is not included.

4.4 Impact of the Polysilicon emitter

Bipolar transistors with a very low intrinsic base resistance are desirable for analogue applications [13]. Increasing the base doping can be used to reduce the intrinsic base resistance; however such a solution will lead to a reduction in the current gain. The polysilicon emitter is known to increase the current gain (by reducing the base current), so it is possible to reduce the base resistance while having high current gain.

A number of previous studies have reported that, compared to conventional bipolar transistors, improvements in the current gain that ranged between factors 3 and 30 were obtained [14]. The enhancement of the current gain depends on the surface treatment being used before the deposition of the polysilicon. The wet chemical clean (which has been used in the fabrication of these devices) was reported to increase the current gain five times higher than that of the HF treatment (dip etching in hydrofluoric acid prior to polysilicon deposition) [Analytical Model and Current Gain Enhancement of Polysilicon-Emitter Contact Bipolar Transistors].

The physical mechanisms that control the base current have been extensively investigated []. It has been established that the injection of minority carriers into a polysilicon emitter is controlled by a number of complex processes: hole transport and recombination in the monocrystalline region (emitter), hole transport across the polysilicon/silicon interface and

hole transport/recombination in the polycrystalline region. The transport across the interface has actually been more thoroughly studied, and different models have been developed. This is in part due to the fact that the physical structure of the interface is very sensitive to process condition. These mechanisms have been summarized in four basic models that have different predictions with respect to a decrease in the base current and an increase in the current gain. The first is termed the "oxide tunnelling model" and explains the improved current gain by tunnelling through a thin interfacial oxide layer. This layer suppresses minority carrier hole injection from the base into the emitter [15] . The second is termed the "grain boundary mobility model" and explains the improved current gain by reduced mobility at the grain boundaries in the polysilicon and at the pseudograin boundary at the polysilicon/silicon interface. The third is termed the "segregation model" and explains the improved current gain by the presence of a potential barrier at the polysilicon/Silicon interface due to dopant atom segregation. The fourth is called the "heteroemitter-like model". This latter considers the polysilicon/silicon interface as a wide-bandgap material which can limit minority carrier transport from silicon to polysilicon, therefore increasing the current gain [14]. In conclusion, all these models report that the concentration of holes injected from the emitter to the polysilicon is reduced therefore the concentration of holes which reachs the emitter contact is small when using the polysilicon. Figure 4.4 illustrates the hole distribution in a polysilicon emitter with an interfacial layer, and for comparison the hole distribution in a single crystal emitter.

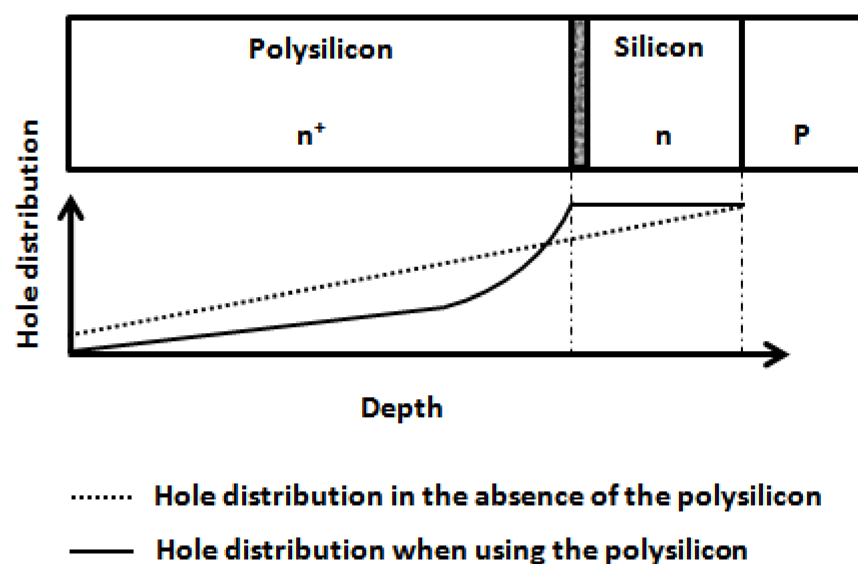

Figure 4.4: The hole distribution in the polysilicon and silicon crystalline.

The challenge when using MEDICI to simulate polysilicon bipolar transistors with a polysilicon region is that the simulator treats the polysilicon as single crystal silicon, in terms of material properties). Therefore it is not possible to include the polysilicon effect in the simulation result. In order to take account of the impact of the polysilicon, the hole mobility and life time have been reduced in this region. The base current has been simulated for different value of the hole mobility in the polysilicon region (Mobility 1 (50 $m^2/(V.s)$) < Mobility 2 (30 $m^2/(V.s)$ < Mobility 3 (10 $m^2/(V.s)$). Figure 4.5 shows that a reduction of the hole mobility in the polysilicon region leads to a decrease in the base current. This can be explained using Einstein relation between the mobility and diffusivity and also the base current equation.

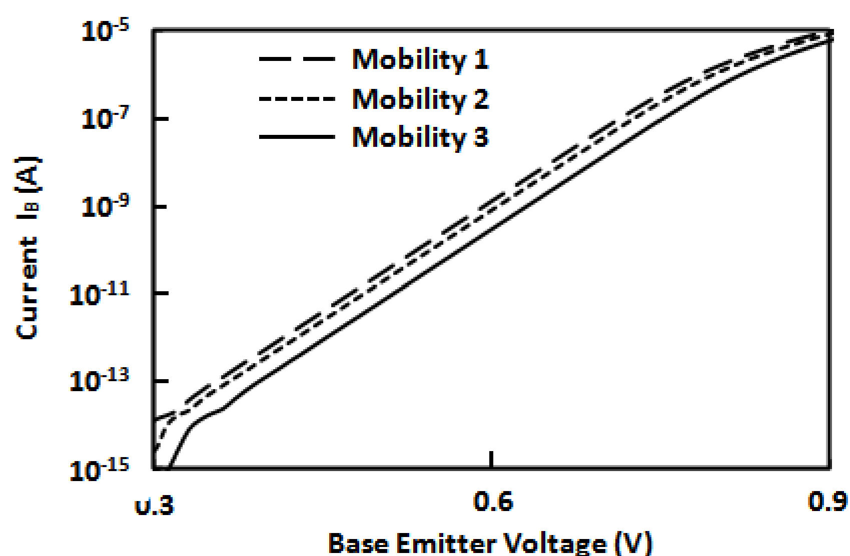

Figure 4.5: Impact of the hole mobility in the polysilicon region on the base current.

4.5 Impact of Recombination

The base current is determined by the diffusion of the holes in the emitter region and for this reason is termed diffusion current. It is well known that the value of the ideality factor for diffusion current is 1 [16]. In reality, the base current results from diffusion and recombination process. This latter process occurs in the intrinsic and extrinsic part of the device. The base current which results from the recombination in the intrinsic device (the bulk and the space charge) is usually proportional to the device area. However, the base current; which is due to recombination in the extrinsic region, depends on the device layout. HBTs designed for high speed applications have a smaller size to improve the RF performance. Thus, the extrinsic base current becomes significant for those devices [17].

The current which results from recombination (in the depletion region) is known to have an ideality factor which is higher than 1. This is illustrated in figure 3.17 in chapter 3 which shows the base current for all devices (i.e. Si BJTs, SiGe HBTs and sSi HBTs) is high at low base-emitter voltage. In the calibration process, it important to include the recombination model, so that the simulation and experimental results agree. Figure 4.6 illustrates the impact of the recombination model on the base current. This figure shows that in the case where the recombination models are included, the base current has an ideality factor which is higher than 1. In the absence of these models the base current has an ideality factor of 1

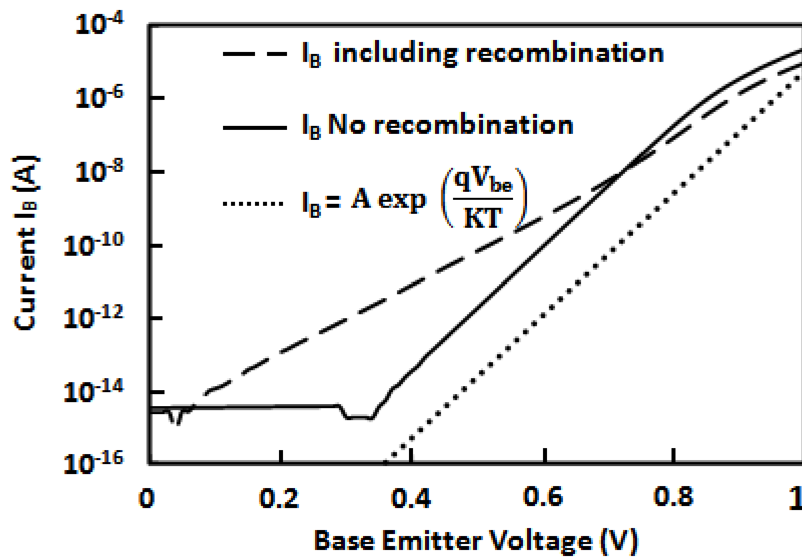

Figure 4.6: Impact of the recombination phenomenon on the base current.

In this simulation study, two recombination models have been used; AUGER and CONSRH.

The AUGER recombination is a process that is involves three particles: an electron and a hole, which recombine and give off the resulting energy to another electron or hole. This process is described by the following equation

$$U_{Auger} = \left(nC_{Auger.n} + pC_{Auger.p}\right)\left(pn - n_{ie}^{2}\right) \tag{4.7}$$

Where

$$C_{Auger.n} = AUGN\left(\frac{T}{300}\right)^{DN.AUGER} \tag{4.8}$$

and $$C_{Auger.p} = AUGP(\frac{T}{300})^{DP.AUGER} \tag{4.9}$$

where p is the local hole concentration, n is the local electron concentration, n_{ie} is the intrinsic carrier concentration, T is the temperature and AUGN, DN.AUGER, AUGP, and DP.AUGER are constants, The CONSRH recombination is described by

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p \left[n + n_{ie}\exp\left(\frac{ETRAP}{KT}\right)\right] + \tau_n \left[p + n_{ie}\exp\left(\frac{-ETRAP}{KT}\right)\right]} \tag{4.10}$$

Where ETRAP represents the difference between the trap energy level and the intrinsic Fermi energy, τ_p is the hole lifetime and τ_n is the electron lifetime. τ_n is given by

$$\frac{TAUN0}{\tau_n} = AN + BN\left(\frac{N_{total}}{NSRHN}\right) + CN\left(\frac{N_{total}}{NSRHN}\right)^{EN} \tag{4.11}$$

And τ_p is given by

$$\frac{TAUP0}{\tau_p} = AP + BP\left(\frac{N_{total}}{NSRHN}\right) + CN\left(\frac{N_{total}}{NSRHP}\right)^{EP} \tag{4.12}$$

Where N_{total} is the total doping concentration and AN, BN, CN, NRSHN, EN, AP, BP, CP, NRSHP, and EP are constants. The total recombination rate is

$$U = U_{SRH} + U_{AUGER} \tag{4.13}$$

The comparison between experimental and simulated results for the Si BJT, SiGe HBTs and sSi HBTs are shown in Figure 4.7, Figure 4.8 and Figure 4.9, respectively.

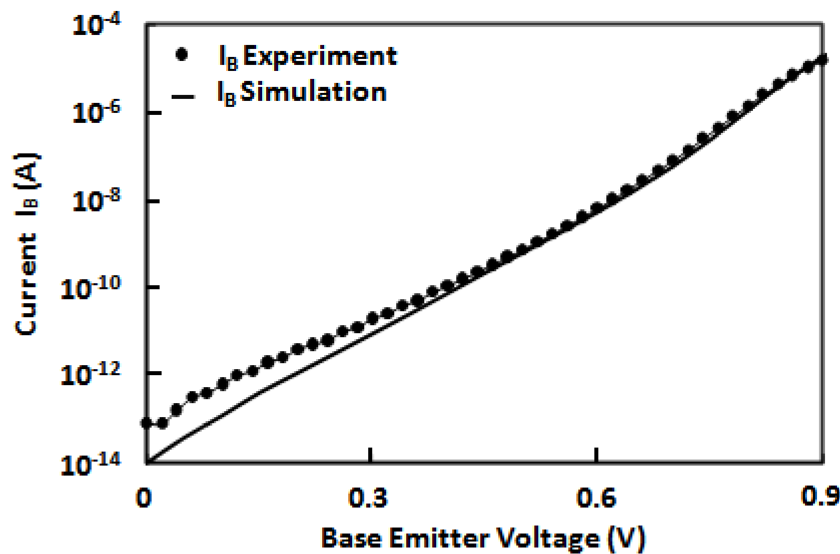

Figure 4.7. Comparison between the simulation and experiment for base current (Si BJTs).

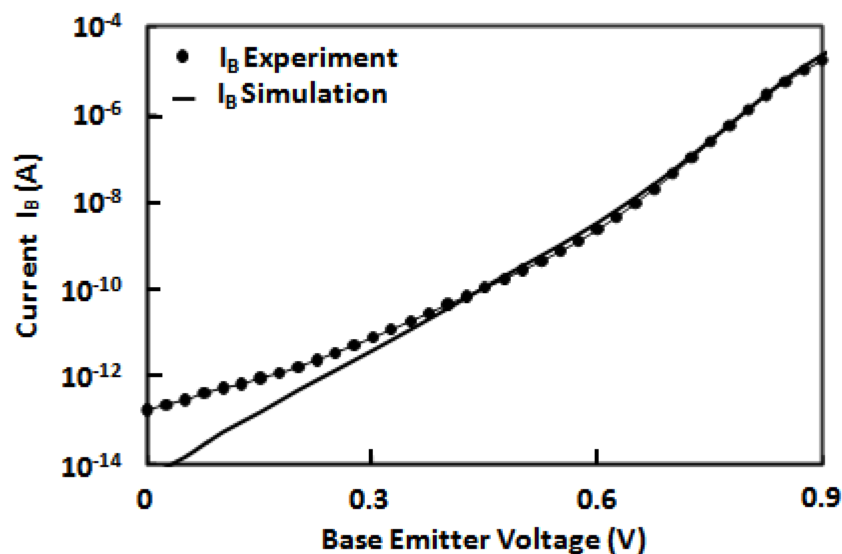

Figure 4.8. Comparison between the simulation and experiment for base current (SiGe HBTs).

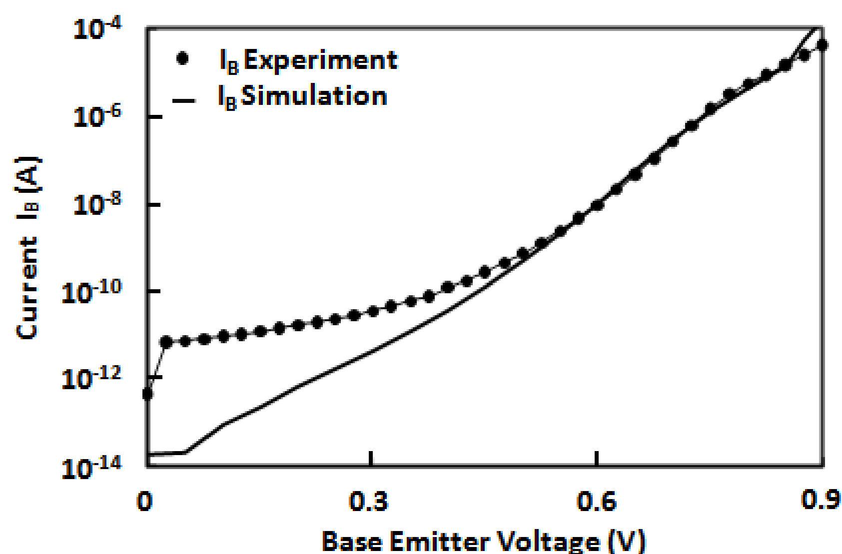

Figure 4.9. Comparison between the simulation and experiment for base current (sSi HBTs).

It is clear that there is a difference between the simulation and the experimental result at low base-emitter voltage, this difference is high in sSi HBTs compared to SiGe HBTs and the Si BJT. Achieving exact agreement between simulation and experiment at low emitter-base voltage is difficult. The circuit designer tends to use the devices in the linear region where the diffusion is the dominant mechanism. It is extremely difficult to achieve a total agreement between the simulation and experiment results at low emitter-base voltage because the defects that are responsible for the generation-recombination current can be

located in different part of the device (, SiO_2 surface, depletion region etc.) and more importantly they are situated in different energy level.

4.6 Ge Profile and SIMS profile

In recent years, the most exciting development beyond the double polysilicon bipolar transistors is perhaps the SiGe heterojunction bipolar transistor. The first successful SiGe base transistor was made using an MBE process to form the SiGe layer [18]. The band-gap engineering by the introduction of Ge in the base of silicon bipolar transistors results in an improved performance of these devices with only a modest increase in process complexity. The smaller band-gap of the SiGe HBTs exponentially increases the amount of minority carriers in base, thus causing an increase in the collector current for the same forward bias. [19]. Equation (4.14) illustrates the exponential dependence of the intrinsic carrier density in the SiGe base layer on the band-gap.

$$n_{iB}^2(\mathrm{Si}) = N_{CB}N_{VB}\exp\frac{-E_{gB}}{kT} \qquad \textbf{(4.14)}$$

Where N_{CB} in the conduction band effective density of state, N_{CV} is the valence band effective density of state and E_{gB} is the band-gap of the base layer.

Equation (4.15) presents a comparison between the intrinsic carrier concentration in the Si and SiGe.

$$n_{iB}^2(\mathrm{SiGe}) = \gamma\, n_{iB}^2(\mathrm{Si})\exp\frac{\Delta E_{gB}}{kT} \qquad \textbf{(4.15)}$$

Where

$$\gamma = \frac{(N_{CE}N_{VE})_{\mathrm{SiGe}}}{(N_{CE}N_{VE})_{\mathrm{Si}}} \qquad \textbf{(4.16)}$$

And $\triangle E_{gB}$ is the reduction of the band-gap caused by the Ge. While the factor $\exp\frac{\Delta E_{gB}}{KT}$ is equal 151 for SiGe HBT, it is over 10^3 for sSi HBTs. This shows that the reduction in the band-gap is the primary factor behind the enhancement of the current gain; therefore great care must be taken when defining the Ge profile for calibration purposes. In reality, the equation

which shows the density of the intrinsic carriers is valid in the case of a Ge box like profile which is the Ge profile used in the SiGe HBTs. However the Ge profile for the sSi HBTs is more complex. Figure 4.10 presents different Ge profiles that are used in SiGe HBTs devices.

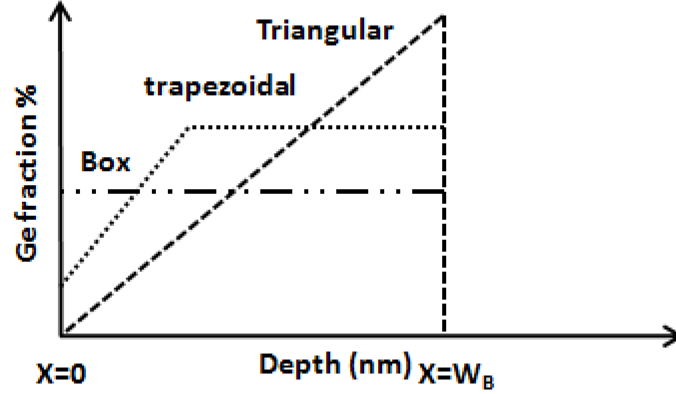

Figure 4.10: Different type of Ge profile (Box, Trapezoidal and Triangular) that can be used in bipolar technology.

Equation (4.17) represents the intrinsic carrier density, this equation can be used for any Ge profile i.e. box, triangular and trapezoidal.

$$n_{iB}^2(\mathrm{SiGe}) = \gamma\, n_{iB}^2(\mathrm{Si}) \exp\left[\frac{\Delta E_{gB}(\mathrm{grad})}{kT}\frac{X}{W_B}\right] \exp\frac{\Delta E_{gB}(0)}{kT} \qquad \textbf{(4.17)}$$

$$\Delta E_{gB}(\mathrm{grad}) = E_{gB}(X = W_B) - E_{gB}(0) \qquad \textbf{(4.18)}$$

The parameter ΔE_{gB} ($X = W_B$) and ΔE_{gB} (0) correspond to the reduction in the band-gap of the base layer due to the Ge content present in the base region at the base-collector junction and the emitter-base junction, respectively. The parameter X represents the position of the peak of the Ge profile in the base. The triangular profile is represented by $X=W_B$, while X=0 corresponds to a box profile. The box profile introduces a high intrinsic carriers and therefore high current gain compared to the triangular profile. This latter introduce an electric field in the base, which greatly speeds up the transport of carriers across the base region [20].

The discussion above shows the base intrinsic carrier density is strongly influenced by the profile of Ge. This highlights the importance of the Ge profile in the calibration process and

proves that it (Ge profile) should be identical (as much as possible) to the actual Ge profile obtained from SIMS data.

Figure 4.11 presents a comparison of the experimental Ge profile and the Ge profile used in the simulation. The Ge profile is formed by two trapezoidal profiles. Each one can be modelled as a box and a triangular profile. It is clear that the Ge profile used in the simulation is close to the Ge profile extracted from the SIMS data. This will result in having an accurate intrinsic carrier density in the base and also take the internal electric field (caused by the triangular profile) into consideration.

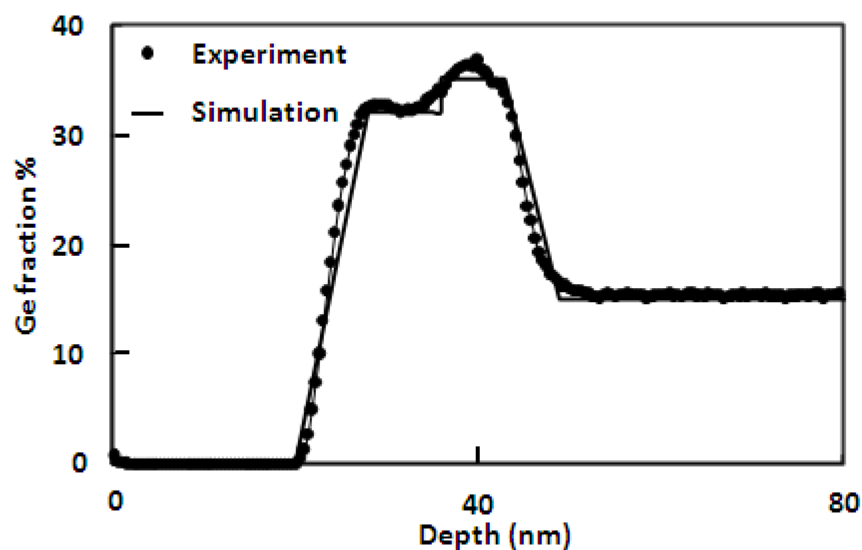

Figure 4.11. Comparison between the SIMS and the simulation Ge profile.

The Ge profile was divided into different regions where the band-gap of each region was set to a specific value based on the Ge content and profile. The values of the band-gap were extracted from the work presented in [11]. The development of a Ge profile which nearly the same as the experimental profile comes with a cost; which is the use of very dense mesh in the base region, which therefore minimises the number of nodes available for the rest of the device simulation. In order to deal with this requirement, a very dense mesh was used only in the most important part of the device.

The band-gap has a fundamental impact on the collector current. However, there are also less important factors that should be included for accurate simulation. The conduction and the valence band-density of states are smaller for SiGe compared to Si. This leads to a small intrinsic carrier density and therefore reduction of the collector current for both SiGe HBTs

and sSi HBTs. however the impact of the conduction and the valence band density of states is small compared to the impact of the band-gap. In order to perform an accurate simulation the values of the conduction and the valence band density of states for SiGe layer were taken in consideration [12].

Another important parameter in the simulation is the doping profile. Since the base layer of all devices has a different amount of Ge, therefore it is expected that the boron profile will not be the same for all devices. This is because the Ge reduces boron diffusion [21]. The SIMS data was considered to develop the doping profile for the simulation of all devices.

4.7 Self-heating

The sSi HBTs exhibits high collector current density, which results in high power dissipation as illustrated by the following equation.

$$P_S = J_C V_{CE} A \tag{4.19}$$

Where P_S is the power consumption, J_C is the collector current density, V_{CE} is the collector-emitter voltage and A is the device area. This power is translated into heat which can lead to an excessive increase of the temperature of the device. The difference between the device temperature and the ambient temperature is given by the equation

$$\Delta T = T - T_O = P_S R_{th} \tag{4.20}$$

Where R_{th} is the thermal resistance, T_O is the ambient temperature (300K) and T is device temperature. Since the thermal conductivity of the SiGe layer is known to be small compared to Si, then the temperature of sSi HBTs will be high compared to Si BJTs and SiGe HBTs. The high temperature of sSi HBTs causes a decrease of the collector current. This phenomenon is called self-heating. It also occurs in AlGaAs/GaAs HBTs due to low thermal conductivity of the GaAs substrate [22]. Alatise et al reported the same phenomenon in strained Si MOSFETs on SRB (virtual substrate) [23].

Electro-thermal simulation with full coupling between the electrical and thermal equation is essential in order to accurately describe the self-heating phenomenon in sSi HBTs. The "lattice temperature advanced application" module in MEDICI was invoked, in this simulation. This application can describe the self-heating behaviour of sSi HBTs by solving the electron and hole energy balance equations consistently with other device equations,

the continuity equations for electrons and holes, as well as the electron and hole current density equations.

Equations (4.21) and (4.22) represent the continuity equations for electrons and holes, respectively.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . J_n - U_n \tag{4.21}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla . J_p - U_p \tag{4.22}$$

Where n and p are the electron and hole concentration, respectively. U_n and U_p are the electron and hole recombination rates.

When the temperature is not taken in consideration, the electron and hole current density equations have only two terms, the first one represents the drift phenomena, while the second correspond to diffusion. However, this is not enough to model the self-heating. Equation (4.23) and (4.24) present the electron and hole current density equation that include the impact of the temperature.

$$J_n = qn\mu_n E_n + k\mu_n (T\nabla n + n\nabla T) \tag{4.23}$$

$$J_p = qn\mu_p E_p + k\mu_p (T\nabla p + p\nabla T) \tag{4.24}$$

Where μ_n and μ_p are the electron and hole mobility, respectively. E_n and E_p are the electric field vectors.

In this case, the temperature is considered as the variable T (not a constant). The heat generation in the semiconductor is modelled using the following equation;

$$H = J_n E_n + J_p E_p + H_U \tag{4.25}$$

The first and second terms are the Joule heating caused by the flow of electrons and holes in the device. Recombination of carriers also releases energy and gives rise to the third term. This latter is not important in majority carrier devices such as MOSFETs, since there is little carrier recombination. However, it is important in minority carrier devices such as bipolar transistors and P-N diodes. The low thermal conductivity of Ge, and therefore of the SiGe is known to be the cause of the self-heating phenomenon. In MEDICI, the thermal conductivity, which is known to be proportional to the temperature, is given by the following equation [24].

$$\lambda = [A + B\ T + C\ T^2 + D\ T^E]^{-1} \tag{4.26}$$

Since a model which describes the thermal conductivity of compound materials (SiGe) is not available in MEDICI, the parameters have been changed to define the thermal conductivity of SiGe. This thermal conductivity is known to be inversely proportional to the Ge content as shown in Figure 4.12 [25]

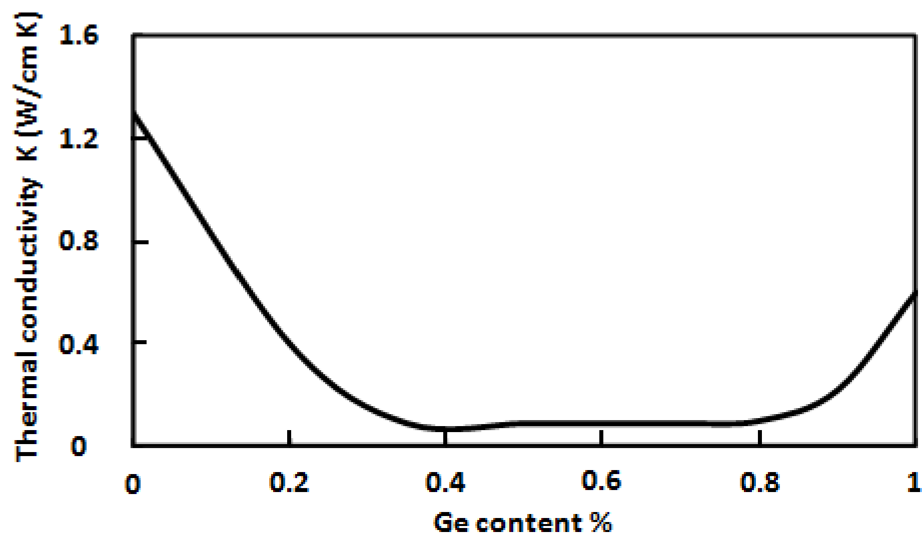

Figure 4.12: Simulation and experiment data for common-emitter characteristic.

Figure 4.13 shows both the simulation and the experimental data for a common emitter characteristic for sSi HBTs. Good agreement between the experimental and the simulation result has been achieved at I_B=3 uA. Figure 4.14 and Figure 4.15 presents the common-emitter characteristic for Si BJTs and SiGe HBTs. These figures shows that no self-heating has been observed in either device also there is a good agreement between the simulation and the experimental result.

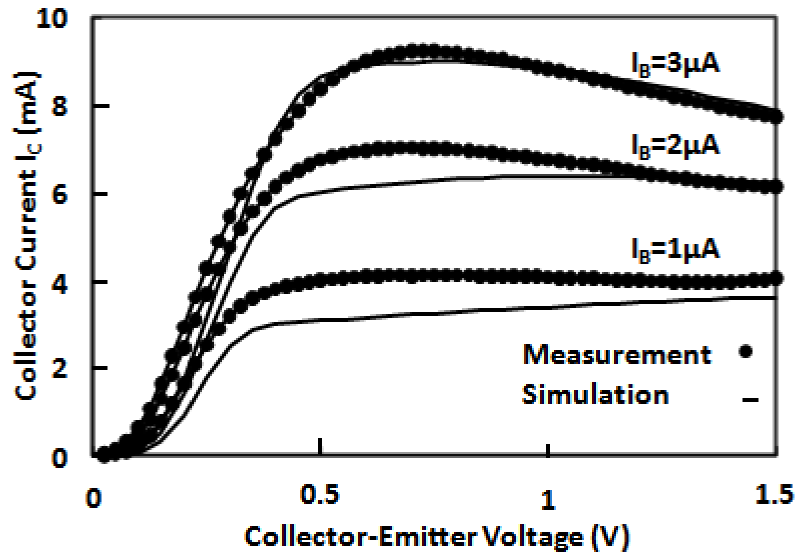

Figure 4.13: Simulation and experiment data for common emitter characteristic.

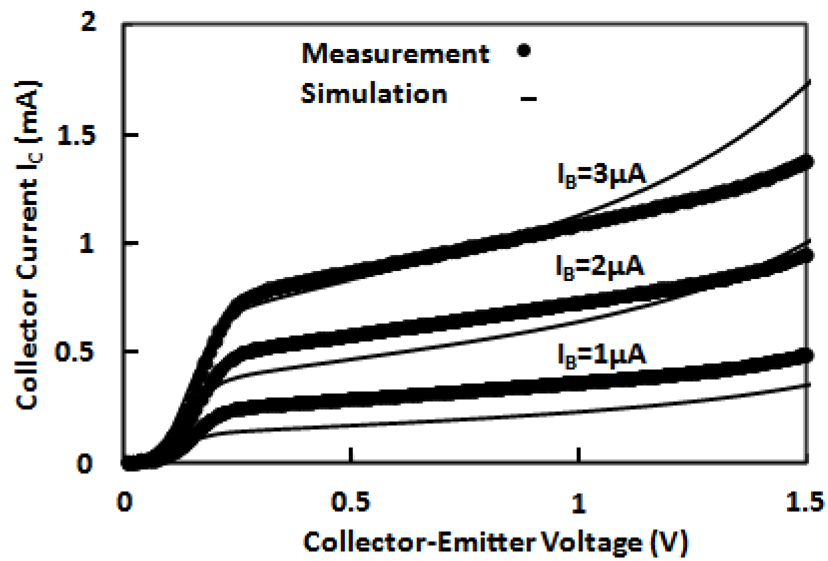

Figure 4.14: Simulation and experiment data for common emitter characteristic.

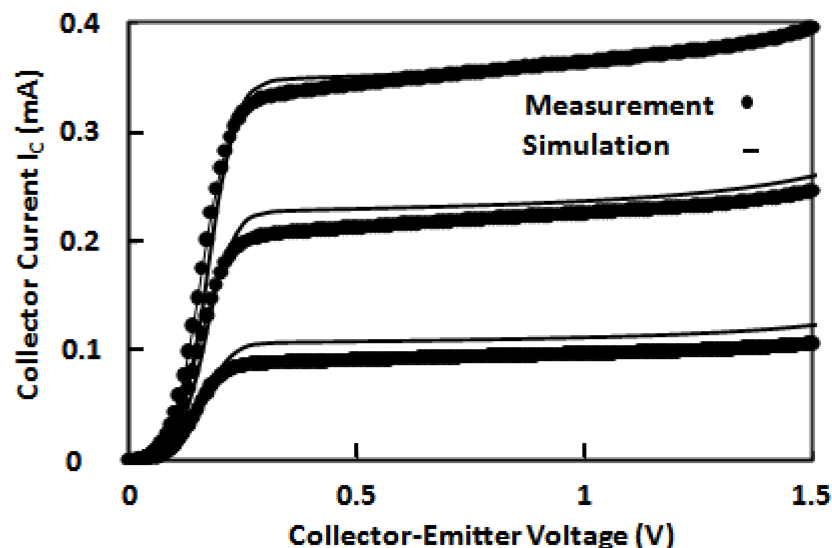

Figure 4.15: Simulation and experiment data for common emitter characteristic.

4.8 Limitation of the Si/SiGe system

Strained Si is considered as one of the leading techniques for improving the mobility of the inversion layer and therefore enhancing the performance of MOSFETs. Mainly, there are two methods to introduce strained Si into MOSFETs channel; process induced strain (local strain) and Substrate-induced strain (global strain). This latter is considered as the most effective way to introduce high tensile strain to the channel. It is based on epitaxial growth of strained silicon on a relaxed SiGe layer. Because of the lattice mismatch between Si and SiGe, the lattice of the Si layer is stretched (strained) in the plane of the interface. This deformation breaks the symmetry of the energy band structure and results in band splitting. The reduced inter-band/inter-valley scattering and effective masses result in enhanced carrier transport in the strained silicon layer that is used as the channel in MOSFETs [26]. However, using relaxed SiGe in the fabrication of the strained Si MOSFETs has lead to some issues. The self-heating is one of these problems; it is caused by the low thermal conductivity of SiGe. More over SiGe usually induces defects, which are known to decrease the performance of the device. Looking to the issues caused by SiGe which has been used to enhance the mobility, new materials with high mobility are considered to extend the performance of the MOSFETs. Material such as GaAs and Ge are studied with immense interest in the fabrication of MOSFETs due to their much higher electron and hole mobility compared to the Si. Ming et. al report the fabrication of P-MOSFETs on Ge/ GaAs heterostructure. The Ge layer was epitaxially grown on the GaAs by high vacuum chemical

vapor deposition. The resultant transistor shows an excellent sub threshold characteristic, high I_{ON}/I_{OFF} ratio and nearly 1.7 times enhancement of hole mobility over the universal mobility curve of Si [27].

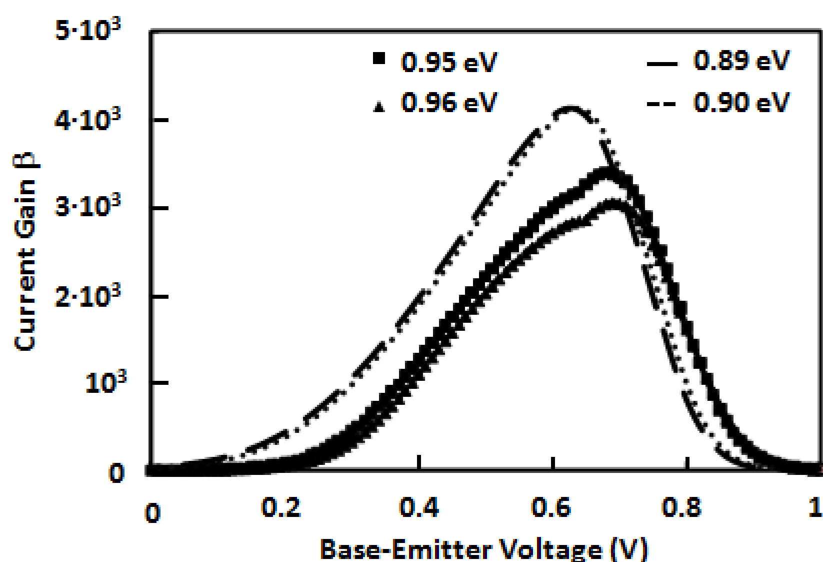

Figure 4.16: Impact of the band gap of the base on the current gain of sSi HBTs.

Figure 4.16 shows that sSi HBTs will continue to offer high current gain as long as the band gap of the base is reduced. This prediction is a result of simulation study that has been performed using MEDICI. Although this result looks promising, there are two main observations that need to be reported. Adding Ge to the base to enhance the collector current and therefore the current gain is not an endless process. More Ge leads to an increase of the lattice constant of the SiGe that forms the base. This increase will lead to more stress to be introduced in the base since the lattice constant of the SiGe (base) has to follow the lattice constant of the SiGe that forms the collector. When the stress in the base reaches a certain level, the structure becomes instable and this will lead to the formation of misfit dislocation which has a destructive impact (base current with ideality factor over 1 even at V_{BE}>0.4 V) on the device performance (full relaxation of the SiGe base layer) [28]. The second issue is the increase of the conduction band discontinuity at the collector base junction. Adding more Ge to the base cause a reduction of its band-gap, this obviously raised the conduction band discontinuity as illustrated in Figure 4.17. The impact of the continuous decrease of the band-gap of the base and the increase of the conduction band discontinuity is illustrated in Figure 4.16. While the current gain is increased with the decrease of the base band-gap, the magnitude of this increase is reduced.

Normally, this magnitude should increase exponentially when considering the reduction of the base band-gap only, it is important to mention that the increase of the current gain in Figure 4.17 correspond to a reduction of the band-gap by a value of 0.1 eV. It is clear that the conduction band-gap discontinuity becomes more and more important when the band-gap of the base reaches certain value.

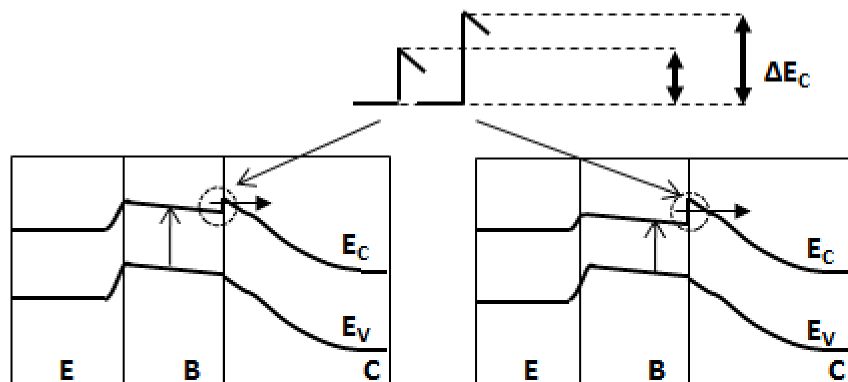

Figure 4.17: Evolution of the conduction band discontinuity at the collector-base junction with a reduction of the band-gap of the base.

4.9 Ge/GaAs heterostructure system

The current silicon based semiconductor-oxide devices are approaching their physical and technological limits because of aggressive scaling. In the search for material solutions alternative to silicon, germanium is gaining considerable interest. Germanium potentially offers several advantages with respect to silicon, such as higher electron and hole mobilities, lower operating voltages [29]. Droopad reports the fabrication of Ge p-channel MOSFETs. This device exhibits excellent sub-threshold swing of 86 mV/dec and I_{on}/I_{off} ratio greater than four orders. Additionally, 1.7 times hole mobility enhancement over the universal curve of Si was achieved. GaAs material has been also used in the fabrication of the n-channel MOSFETs, the resultant device shows high performance compared to all prior n-channel MOSFETs [30, 31].

The electron mobility in GaAs is 8500 $cm^2\ V^{-1}s^{-1}$ compared to 3900 $cm^2\ V^{-1}s^{-1}$ in Ge, this is the reason behind the fabrication of n-channel MOSFETs based on GaAs channel. Meanwhile, Ge has been used in the fabrication of the p-channel MOSFETs due to its (Ge) high hole mobility 1900 $cm^2\ V^{-1}s^{-1}$ compared to GaAs (400 $cm^2\ V^{-1}s^{-1}$) [3].

It is clear that high mobility is the driving force toward the implementation of Ge and GaAs in MOSFET technology. However, these materials can be also used in the fabrication of HBTs because of their different band-gap, more over the resultant HBTs could operate at high speed due to the high mobility of the Ge and GaAs. Additionally, this will allow the integration of Ge/GaAs CMOS and Ge/GaAs HBTs in one chip.

The band-gap of Ge is known to be equal to 0.66 eV, while it is 1.4 eV for GaAs [2]. It is clear that there is a huge band-gap difference between the Ge and GaAs; this will be reflected in the intrinsic carrier density in both semiconductors. Figure 4.18 and Figure 4.19 illustrates the I-V characteristic of Ge diode and GaAs diode, respectively. Ge diode exhibits high current because of the high intrinsic carriers that are available in the Ge material compared to GaAs.

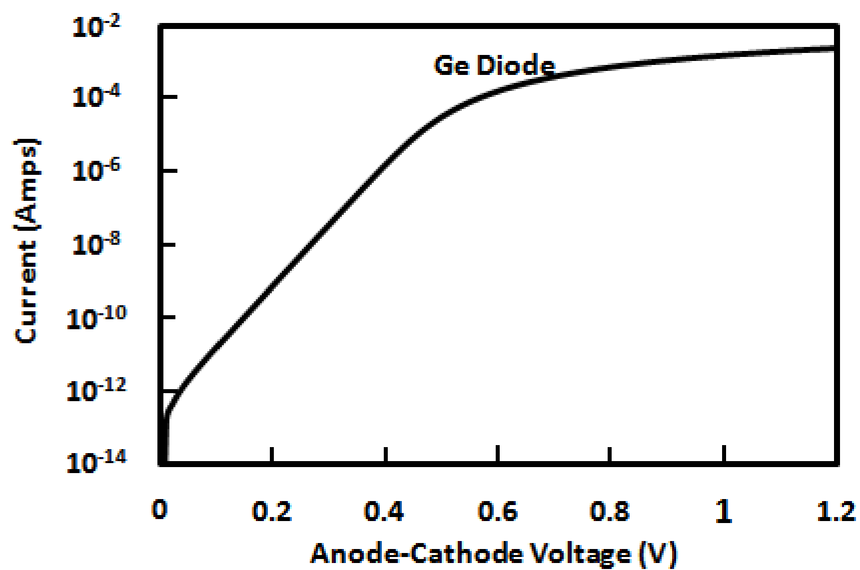

Figure 4.18: Current flowing through Ge diode VS Anode-Cathode voltage.

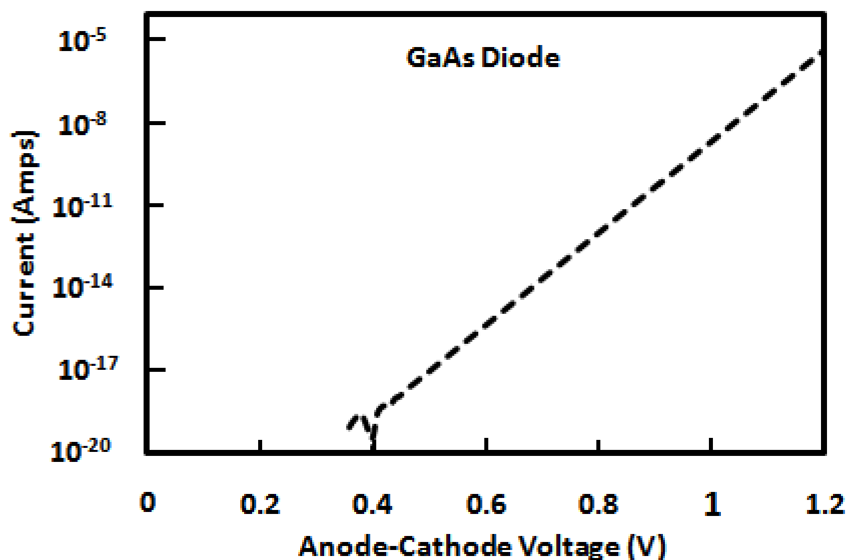

Figure 4.19: Current flowing through GaAs diode VS Anode-Cathode voltage.

Having GaAs in the emitter region and Ge in the base and collector region will result in high current gain. However there is another issue which prevent this device from reaching its full potential which is the band-gap discontinuities.

When semiconductors with different band-gap and electron affinities are brought together (Ge and GaAs in this case) to form a junction, we expect discontinuities in the energy bands as the Fermi levels line up at equilibrium. These discontinuities in the conduction and the valence band accommodate the difference in the band-gap between the two semiconductors. In an ideal case the conduction band discontinuity is a result of the difference in the electron affinity as presented by equation (4.5). Meanwhile the valence band discontinuity would be found from the difference between the band-gap and the conduction band discontinuity as presented in equation (4.6).

Figure 4.20 shows spatial variations of the conduction band E_C and the valence band E_V at equilibrium for an NPN Ge/GaAs HBTs. It is clear that the difference between the band-gap of Ge and GaAs results in a large valence band-gap offset. This agrees with the theory since the affinity of Ge is 4.13 eV and 4.07 eV of the GaAs. Therefore $\triangle E_C$ is equal 0.06 eV and the valence band discontinuity is given by the following equation.

$$\begin{aligned}\Delta E_V &= \Delta E_G - \Delta E_C \\ &= 1.43 - 0.66 - 0.06 \\ &= 0.77 \text{ eV}\end{aligned} \quad \textbf{(4.27)}$$

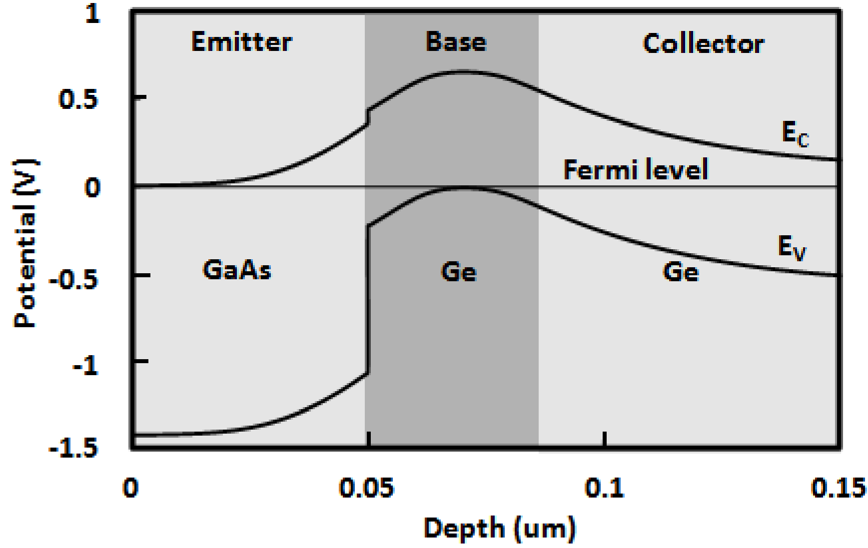

Figure 4.20: Energy band diagram for npn GaAs/Ge Profile.

Carrier transport across band-gap discontinuities is governed by thermionic emission and tunnelling, unlike transport in continuous media, which is governed by drift and diffusion mechanism. Based on the thermionic emission concept, the electron current density at the heterojunction interface can be described as the difference of the two opposing electron flux as shown by equation (4.28) [24].

$$J_n = -q\frac{\nu_n}{4}\left[n\left(x_j^-\right) - n\left(x_j^+\right)\exp\left(-\frac{\Delta E_C}{KT}\right)\right](1+\delta_n) \quad \textbf{(4.28)}$$

Where $n\left(x_j^-\right)$ and $n\left(x_j^+\right)$ is the electron density at both sides of the heterojunction, ν_n is the mean electron thermal velocity, q is the electronic charge and ΔE_C is the conduction band discontinuity and δ_n is the tunnelling coefficient.

Considering the above equation, it is also possible to develop an equation for the collector.

$$J_C = \frac{q\nu_n N_E \exp\left(-{}^{qV_{B1}}/_{kT}\right)}{1 + (W_B/D_n)\nu_n\delta_n \exp\left[{}^{q\,(V_{B2} - \Delta E_C)}/_{kT}\right]} \quad \textbf{(4.29)}$$

Where J_C is the collector current density, N_E is the emitter doping, V_{B1} and V_{B2} are the built in potential at both side of the heterojunction, W_B is the base width and D_n is the electron diffusion in the base.

Equation (4.29) shows that an increase of the conduction band-gap discontinuity will reduce the collector current density. Similarly, it is possible to write the equation of the base current density:

$$J_b = \frac{q\nu_p N_B \exp\left(-{}^{qV_{B2}}/_{kT}\right)}{1 + (W_E/D_p)\nu_p\delta_p \exp\left[{}^{q\,(V_{B1} - \Delta E_V)}/_{kT}\right]} \qquad \textbf{(4.30)}$$

Where J_b is the base current density, ν_p is the is the mean hole thermal velocity, δ_p is the tunnelling coefficient, W_E is the emitter width, ΔE_V conduction band discontinuity and D_p is the electron diffusion in the base. Equation (4.30) shows that the valence band discontinuity will reduce the base current density.

As was previously stated, MEDICI uses the value of the affinity to calculate the conduction band discontinuity, and then use this latter to calculate the valance band discontinuity ΔE_V. Therefore by changing the affinity of one of the materials, it possible to tune the conduction band discontinuity and therefore the valence band discontinuity.

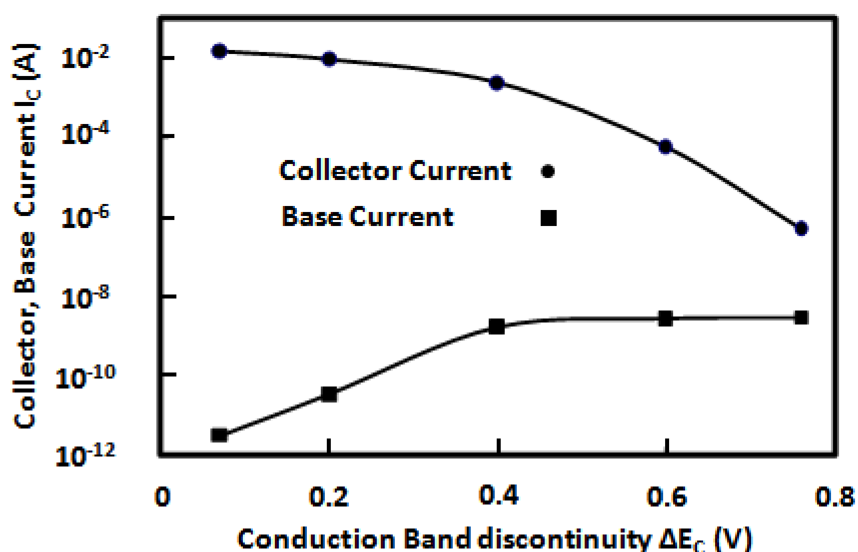

Figure 4.21: Impact of band-gap discontinuity on collector and base current.

Figure 4.21 shows the collector and the base current at V_{BE} =1 V for different value of ΔE_C. At ΔE_C=0.06 V (ΔE_V=0.77 V), which is the default value (the first data point from the left), the

base current is just over 10^{-12} uA/um. This is very small amount of current for a HBTs operating at V_{BE} =1 V. This current is believed to be a result of leakage mechanism and not diffusion. It is known that the base current depends on the minority carrier concentration gradient in the emitter as well as the valence band discontinuity. In this case, the hole current is subjected to valence band discontinuity, in addition to a low minority carrier concentration in the emitter (GaAs). These two reasons explain the small value of the base current. Another important result that emerges from this figure is that, the base current increases with the increase of ΔE_C (decrease ΔE_V), this is because the potential barrier (valence band discontinuity) that holes have to cross is getting smaller. Meantime, the collector current is getting smaller because the potential barrier for the electron is increasing (ΔE_C increase). The above analysis reflects the importance of band discontinuity in the operation of HBTs.

In practice, the band discontinuities are found experimentally for particular semiconductor pairs. For example, in the commonly used system GaAs/AlGaAs, the band gap difference between the wider band-gap AlGaAs and narrow band-gap GaAs is apportioned approximately 2/3 in the conduction band and 1/3 in the valence band for the heterojunction For GaAs/Ge system. There are mainly two types of methods that can be used to experimentally extract the band offsets; optical and transport method. Since the performance of the heterojunction device is governed by the band offsets then the current voltage characteristic can be used to calculate these band offsets. The band offsets values that are obtained by the transport method are viewed to be unreliable. This is because the I-V measurements are not governed by band offsets only but also they are affected by intentional doping, quality of the contact, recombination, tunnelling and leakage current. This explains the wide scatter in results obtained using this technique for the same system [32].

Internal photoemission measurement is considered as one of the best optical methods used to determine the band offsets. This method can be understood as a process of optically induced transitions of mobile charge carriers, electron or hole, from one side to the other of a PN junction. When light with photon energy hν (h is Planck's constant and ν is the frequency of the photon), is greater than the barrier height, a photocurrent is generated by

photoelectrons excited from one side of the PN junction to the other as illustrated in Figure 4.22 [33].

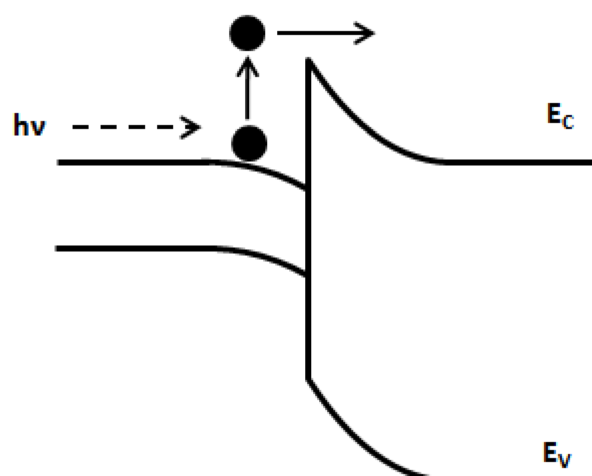

Figure 4.22: Photo emission of an electron from one side of the heterojunction to the other side. The product hv should be higher than the barrier high, so that the transition can take place.

Table 4.1 summarises some reported values of the valence band discontinuity (GaAs/Ge system) and also the extraction methods that have been used to determine these values. It is clear that there is a huge difference in the reported values. This is because the band-gap discontinuity is affected by the fabrication process of the heterojunction (i.e. temperature, quality and method of the epitaxial growth etc.) and also by the extraction method.

Growth Temperature (°C)	Extraction method	ΔE_V (V)
500	I-V	0.72+-0.01
500	I-V	0.5+-0.1
500	IPE	0.45+-0.04

Table 4.1: Different value of the valence band discontinuity in Ge/GaAs system [34].

Since the development of the heterojunction devices, there has been a lot of work to control the band offsets so an improvement of the performance of these devices can be achieved. One of the methods that is used to artificially control these band offsets consists of the incorporation of an ultrathin ionized donor or acceptor sheets at the heterojunction interface. The electrostatic potential of this "doping interface dipole" is added to or subtracted from the potential of the discontinuity. Since the separation between the charge sheets is on the order of the carrier de Broglie wavelength, electrons crossing the interface "see" a new band discontinuity (ΔE_C - eV), where V is the potential of the double layer

(Figure 4.23). Using this technique, Capasso et al. demonstrated an artificial reduction of the conduction band discontinuity of the order of 0.1 eV in an $Al_{0.25}$ $Ga_{0.75}As$/GaAs heterojunction. The other approach is compositional grading of the emitter base junction to smooth out a large part of the band-gap discontinuities [7]. This method proves great deal of importance, since it proves its ability to improve the performance of different HBTs devices such as [Si, SiGe] and [GaAs, AlGAs]. In order to apply this approach to GaAs/Ge HBTs, there is a need to pseudomorphically grow $GaAs_{1-X}Ge_X$ alloy.

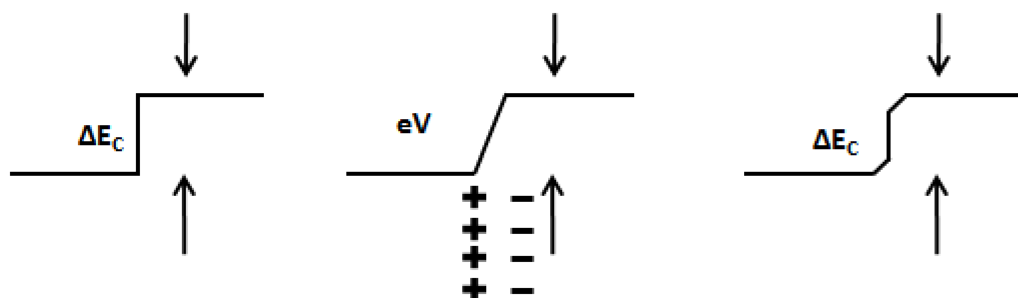

Figure 4.23. Impact of the doping interface dipole on the conduction band discontinuity.

4.10 Conclusion

A 2D simulation study of sSi HBTs has been reported for the first time. For an accurate simulation, it was necessary to include different models. High doping levels are known to reduce the band-gap of the semiconductor, therefore it is important to include a band-gap narrowing model in the simulation. The literature shows that the hole and electron mobility decreases with the increase of the doping level. This is a good reason to include concentration dependant mobility in this study. The defect characterisation that has been presented in the previous chapter has shown the existence of defects in all devices, but with different level of concentration. The sSi HBTs have the highest defect concentrations compared to SiGe HBTs and Si BJTs. These defects are known to cause generation/recombination phenomena, therefore it was important to include generation recombination models in this simulation. The conduction band discontinuity at the collector base junction has an impact on the performance of both SiGe HBTs and sSi HBTs. The thermionic emission field was considered in this work. This is because the carrier transport across the band-gap discontinuities is governed by thermionic emission, unlike transport in continuous media, which is governed by drift and diffusion mechanism. The Gummel plot and also common emitter data that have been obtained by the simulation have shown good

agreement with the experimental data. It has been proven also that band-gap engineering is the main factor behind the performance of sSi HBTs. MEDICI has been also used to predict the impact of reducing the band-gap of the base layer beyond 0.94 eV. The study has shown that sSi HBTs will carry on delivering an increase in high current gain. However, this increase is not as high as it should be. The analysis has shown that when the band-gap of the base reaches certain value, the collector base junction becomes more and more important. The new improvements that have been achieved in the fabrication of MOSFETs based on high mobility material such as Ge and GaAs have shown the importance of these materials in the future of the bipolar semiconductor technology. MEDICI simulator has been used to investigate the potential of the HBT based on Ge and GaAs. The results show that such devices might have good current gain, however the band discontinuity and more precisely the valence band discontinuity is blocking this device from reaching its full potential.

4.11 Reference

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Chapter 5. Low Frequency Noise in sSi HBTs

5.1 Introduction

The intent of manufacturers is to propose low cost RF devices for communication systems. An important parameter of bipolar transistor RF performance is low-frequency noise [1].Even though the noise is at low frequencies, it can affect the high frequency performance of bipolar circuits, for example, the phase noise in oscillators is related to low frequency noise of individual devices [2].

Oscillators are electronic circuits that produce a repetitive electronic signal, often a sine wave or a square wave. The low frequency noise of bipolar devices can be upconverted to undesired phase noise in the oscillator. The phase noise is a short-term random frequency fluctuation of a signal, it is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1 Hz bandwidth at a given offset from the desired signal. The phase noise in oscillators can limit the channel frequency spacing in communication systems [3] and the ultimate Signal-to-Noise ratio (SNR) which can be achieved when listening to a frequency modulated (FM) or phase modulated (PM) signal. In addition, the phase noise affects the Bit Error Rate (BER) performance of a digital transmission system. The low frequency noise is known to affect the performance of the mixers since it sets a fundamental limit on the minimum discernible signal level that can be received [4].

The low noise amplifier (LNA) is one of the key components in a typical wireless receiver. As the first block in the receiver chain, placed directly after the antenna, it needs to amplify received weak signals without adding much noise and distortion. If the internal noise of the LNA is high, then the wanted signal will be surrounded by noise which makes the detection of the signal difficult [5].

In addition, low frequency noise is considered as a very powerful monitoring tool for technological process characterisation and device reliability diagnostics. In effect, the 1/f noise is a very sensitive indicator of the device quality [6]. Noise measurements have been used to characterize deep-level defects and impurities, as well as surface states and hot-

electron phenomena. Moreover, phenomena such as electron migration in interconnections and point contact effects have been characterized using noise measurements [7]. Moreover noise has been linked to the time to failure of the sample [8].

This chapter presents the first noise analysis for sSi HBTs. The measurement set-up used in this work is presented and the importance of each element is discussed. The different noise mechanisms that exist in the bipolar transistor was presented and linked to its physical source. A comparison of the noise performance of sSi HBTs with co-processed SiGe HBTs and Si BJTs at fixed base current and collector current is presented. The impact of the low frequency noise on phase noise is also discussed. The impact of fabrication is known to have a fundamental effect on the noise performance [9], hence the importance to discuss the impact of rapid thermal annealing on the noise performance of the device.

5.2 Measurement set-up

When measuring low frequency noise, the challenge is to be able to measure the noise introduced by the Device under Test (DUT) without the contribution of the rest of the system (bias sources, amplifiers etc.). Historically, there have been several approaches on how to effectively measure the 1/f noise, based on the use of either a voltage amplifier [10] or transimpedance amplifier. The first one is based on the measurement of noise voltage drops induced in a resistor and amplified by a low noise voltage amplifier. The second one directly converts noise currents into noise voltages through a transimpedance amplifier [6]. Such methods enable the determination of the equivalent current noise sources at the access of the device (base contact). Figure 5.1 shows a schematic diagram of the measurement set-up, which consists of a HP 4155A semiconductor parameter analyser, low pass filter, SR570 low noise amplifier (LNA), and Agilent 35670A dynamic signal analyzer (DSA).

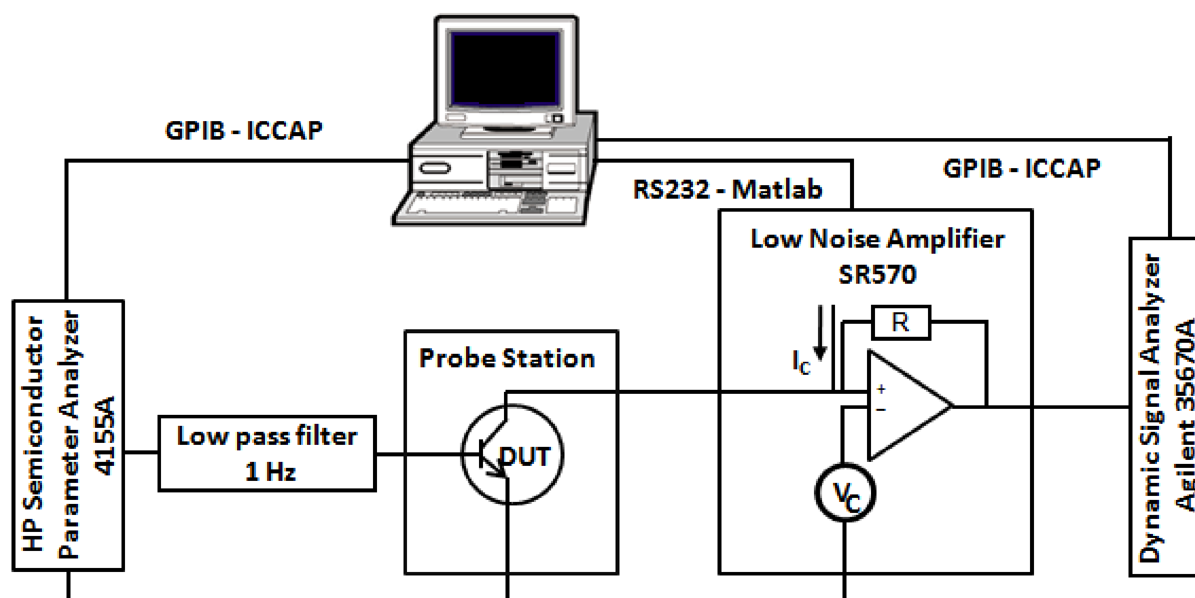

Figure 5.1: Schematic diagram of the measurement set up

The input bias is accomplished by using the HP 4155A semiconductor parameter analyser. When performing noise measurements, great care must be taken to prevent external noise from being introduced into the DUT. This is especially important because any noise from the bias source will be increased by the gain of the DUT. For this reason a high quality filter is used to minimise noise (within the frequency band of interest, above 1 Hz) to flow into the DUT from the HP 4155A semiconductor parameter [11].

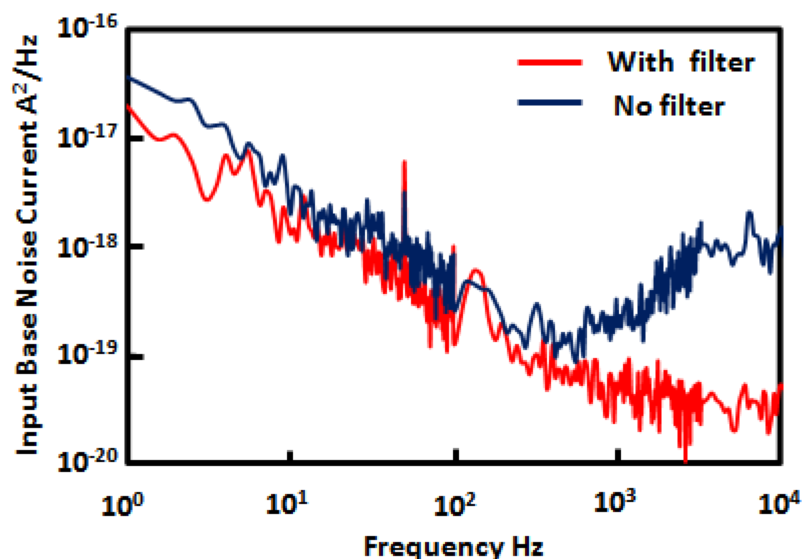

Figure 5.2: S_{IB} curves illustrating the impact of the filter.

Figure 5.2 represents the impact of the filter on the spectral noise density S_{IB}. In the absence of the filter, the measured noise level is slightly higher compared to the noise level

measured with the use of the filter, especially at frequencies over 300 Hz where very high noise has been detected (not ∝ to 1/f). The capacitors (of the filter) are able to eliminate this excess noise since they behave as a short circuit for high frequency signals. The filter is built using metal film resistors, for lowest possible 1/f noise and good quality capacitors, for minimum leakage. In the case of a bipolar transistor, 1/f noise is generated in the emitter-base region. Thus the resistance of the filter should be higher than the base-emitter resistance in all bias level otherwise it will be shorted by the filter capacitors [12]. This necessity can be explained more by modelling the noise in the transistor using a current source in parallel with r_{be}. Figure 5.3 presents the equivalent circuit of the filter and DUT.

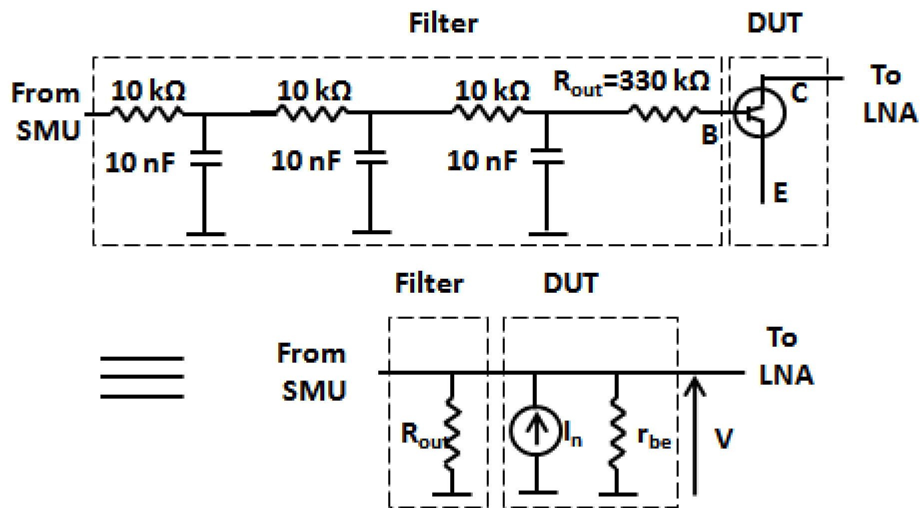

Figure 5.3: equivalent circuit for the filter and DUT

$$V = \frac{R_{out} r_{be}}{R_{out} + r_{be}} I_n \quad (5.1)$$

If $$R_{out} \ll r_{be} \quad (5.2)$$

then $$V = R_{out} I_n \quad (5.3)$$

Equation (5.3) shows that the current I_n will flow through R_{out}, which means that the noise measured at the output of the DUT will be lower than the actual value. This conclusion is illustrated in Figure 5.4, which shows that the measured S_{IB} is small when using 50 Ω as output resistance. Also, it is difficult to see 1/f dependence in this measurement (in case of 50 Ω).

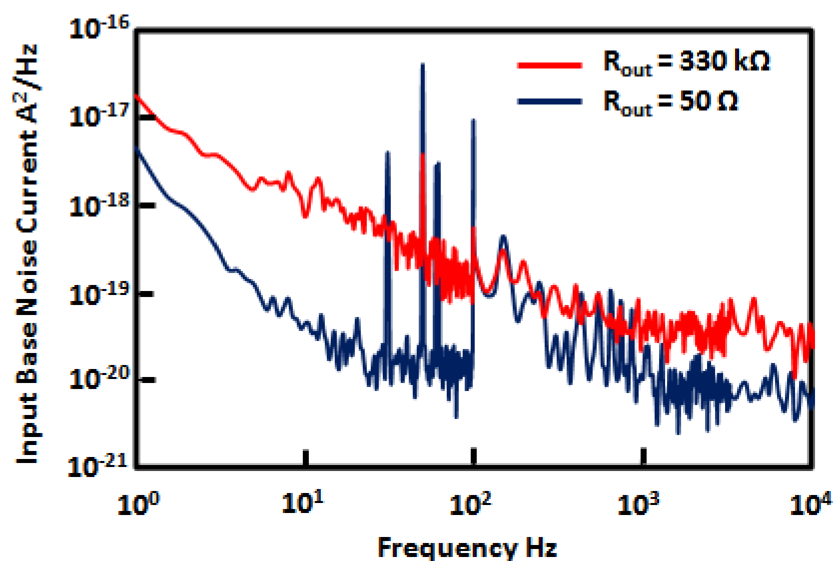

Figure 5.4: S_{IB} curves illustrating the impact of the output resistance of the filter R_{out} on the noise measurement.

The device output is directly connected to the SR570 LNA, which is battery powered for low intrinsic noise. Besides amplifying the output noise, the amplifier provides a current and a voltage supply which are used to bias the device output. The voltage supply allows the setting of the collector bias while the current source provides an offset current as not to drive the LNA into saturation. The SR570 LNA can supply an output voltage of up to 5 V and a maximum current compensation of 5 mA. The gain (expressed in terms of sensitivity A/V) can be varied between 10^{-3} to 10^{-12} A/V. Proper operation of the SR570 LNA requires that the sensitivity (gain setting resistor) has a higher (lower) value than the transconductance (output resistance) of the device [13], However, care must be exercised since too high sensitivity increases the SR570 noise contribution. The amplifier is also equipped with a comprehensive set of programmable low pass and high pass filters. In this application, they are typically set to pass the frequency range of interest, namely 1 Hz to 100 kHz.

The device spectral noise density S_{IB} is amplified and measured by the 35670A dynamic signal analyzer. This instrument is ideal for analyzing signals with a low frequency power spectrum (such as 1/f noise) as opposed to a spectrum analyzer which is used at higher frequency bands.

An verification of the system performance consists of measuring the noise of a 50 Ω resistors. This is can be accomplished by connecting the resistor to the input of the 35670

Dynamic Signal Analyzer. The noise value was found to be equal 10^{-14} A^2/Hz. This value is higher than the theoritical thermal noise of a 50 Ω resistor ($33 \cdot 10^{-26}$ A^2/Hz). This noise is related to the thermal oscillation of electrons in a resistor, it is frequency independent and bias (current)-independent. The thermal noise is given by the following equation [14]:

$$S_I = \frac{4kT}{R} \tag{5.4}$$

Where k is Boltzmann constant, T is temperature in Kelvin and R is the value of the resistance.

The above comparison between the thermal noise and the measured noise suggests that the value 10^{-14} A^2/Hz, is the intrinsic noise of the Dynamic Signal Analyzer (DSA). The question which arises is how this DSA can measure a noise which is lower than its intrinsic noise. This can be accomplished by the LNA, which amplifies the transistor noise well above 10^{-14} so that the DSA intrinsic noise does not contribute to the noise measurement. Figure 5.5 illustrates the measured intrinsic noise of the DSA, the amplified transistor noise and the actual noise of the transistor. It is clear that the transistor noise is sufficiently amplified so that the intrinsic noise of the DSA does not contribute to the total noise.

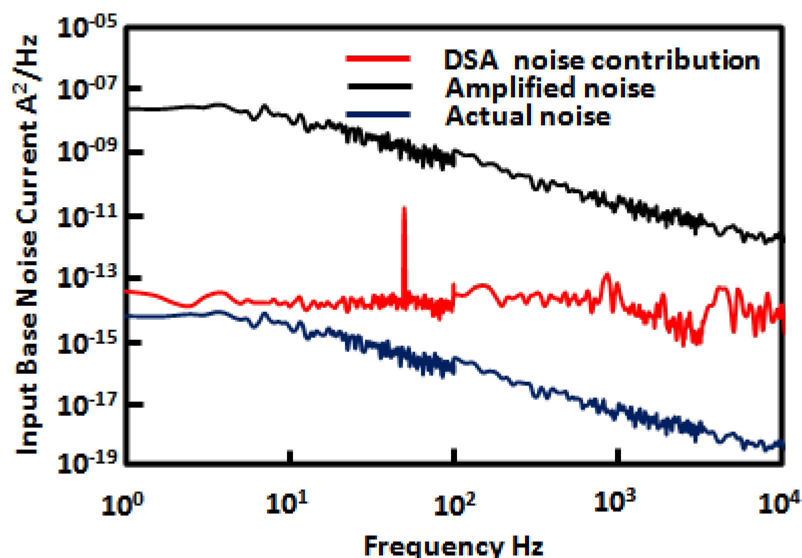

Figure 5.5: intrinsic noise of DSA, the amplified and the actual noise of the DUT

These noise measurements are performed using a Cascade probe station, which reduces the risk of having DUT oscillations and also offers the possibility of using 3-level shielding. This is definitely a good asset in performing sensitive noise measurements.

The measurement is semi-automatically controlled by Integrated Circuit Characterization and Analysis Program (ICCAP). This is a device modeling program that provides characterization and analysis capabilities for a broad range of semiconductor modeling processes.

The starting step for performing noise measurement is the DC characterisation; the DC current gain and output transconductance is obtained at this stage. The second step is running the noise program, which provides the collector voltage, current offset and the sensitivity. These values should be used to manually set the LNA configuration. In this work a RS232 port along with Matlab code has been used to configure the LNA. Then the dynamic signal analyzer starts performing the noise measurement. The spectral noise density S_{IC} is given by

$$S_{IC}(f) = (N_{meas} . S_{SR570})^2 \quad (5.5)$$

where N_{meas} is the noise measured by the analyzer expressed in $V/\ Hz$ and $S_{SR570}$is the sensitivity of the amplifier, while the actual spectral power density S_{IB} of the base current noise source is given by:

$$S_{IB}(f) = S_{IC}(f)/\beta^2 \quad (5.6)$$

The measurement set up used in this work measures the noise in an indirect way through the collector current. However it is possible to measure low frequency noise directly at the base using a current amplifier connected in series with the base biasing network, as shown in Figure 5.6.

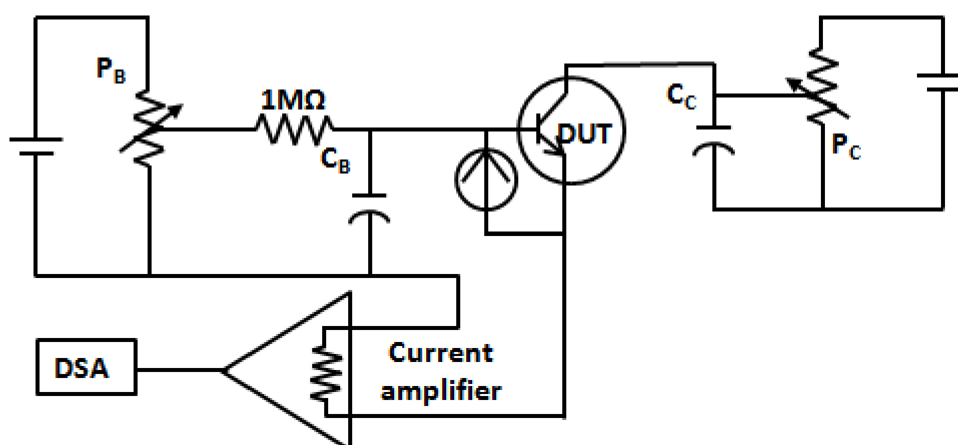

Figure 5.6: Circuit used to directly measure low frequency noise using a current amplifier connected in series with the base biasing network.

A large bypass capacitance C_B short-circuits the noise from the base biasing network, and creates a low impedance path for the spectral noise density S_{IB}. As long as the input impedance of the current amplifier is much lower than the transistor input impedance, the entire base current noise spectrum S_{IB} flows into the current amplifier. The spectral density of the current amplifier output voltage is proportional to the base noise current [15].

5.3 The base current dependence of low frequency noise

In bipolar transistors there are different types of noise: Shot noise, thermal noise and low frequency noise (1/f). The current through the P-N junction of a diode is composed of many individual current impulses, due to the transport of individual charge carriers. This individual current impulse is random and leads to the so called shot noise. For bipolar transistor, two shot noise components should be considered. The first one is related to for the base-emitter junction, and the second is associated with the base-collector junction. Thermal noise is caused by the random thermally exited vibration of a charge carrier in a conductor [16]. In bipolar transistors, three resistances can be identified, base, collector and emitter resistance. Each one of these resistances produces a thermal noise. The low noise frequency is linked to the presence of the defect in the base-emitter region [17]. This is the most important noise mechanism in the bipolar transistor, not only because of its magnitude, but also because its impact on the performance of the electronic circuit. Figure 5.7 presents the conventional hybrid-π model of a bipolar transistor with the dominant noise sources [1].

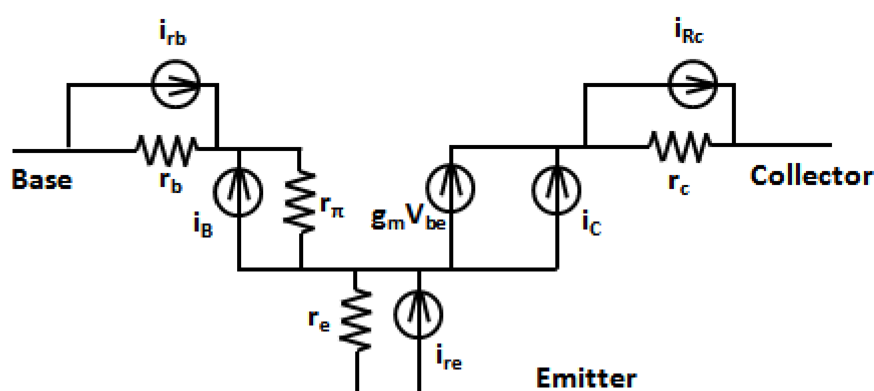

Figure 5.7: Equivalent circuit of the transistor illustrating the noise sources in bipolar transistor.

I_{rb}: thermal noise associated with the base resistance.

I_{rc}: thermal noise associated with the collector resistance.

I_{re}: thermal noise associated with the emitter resistance.

i_C: shot noise associated with the base-collector junction.

i_B: spectral noise density (1/f and shot noise associated with the emitter-base junction).

flicker noise, also called 1/f noise, is a signal with a frequency spectrum such that the power spectral density is proportional to the reciprocal of the frequency [18]. Previous studies of low-frequency noise in various semiconductor devices showed that there are two possible origins for flicker noise. The bulk mobility fluctuation model states that the normalized current noise power spectral density $S_I(f)$ for flicker noise is given by the following universal equation

$$\frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} = \frac{\alpha_H}{fN} \tag{5.7}$$

where N is the total number of carriers in the device and f is the frequency. It is assumed that the bulk mobility fluctuation arises from lattice scattering and the Hooge parameter α_H, which varies as $(\mu/\mu_1)^2$, where μ is the carrier mobility and μ_1 is the mobility due to lattice scattering alone. Later on, Hooge found that α_H can vary between 10^{-7} and 10^{-2}, which indicates that the value of α_H is very sensitive to material quality and the relative noise level of material and devices [19].

On the other hand, the trap model (carrier number fluctuation model) stipulates that 1/f noise arises from the capture and emission of carriers by localized states within the material [20, 21].

To date most publications show that the main 1/f noise sources are located at the emitter-base region in the intrinsic emitter-base junction [22] and also, it is associated with the base current. The low noise frequency is found to be usually proportional to the square of the base current, that is $S_{IB} \sim I_B^2$, However there are also a few publications which report S_{IB} proportional to I_B and I_B^3 [23]. The 1/f noise is given by equation (5.10)

$$S_{IB} = K \times \frac{I_B^2}{f^\alpha} \tag{5.8}$$

where K is a constant, I_B is base current, f is frequency, α is a constant. The constant K is known to be inversely proportional to the device area; therefore scaling down the device to improve the speed of the device results in higher 1/f noise [24, 25].

Figure 5.8, Figure 5.9 and Figure 5.10 show the spectral noise density S_{IB}, for Si BJTs, SiGe HBTs and sSi HBTs respectively. The S_{IB} exhibits 1/f dependence, which also rises with the increase of the base current. This shows that it can be modelled by equation (5.10).

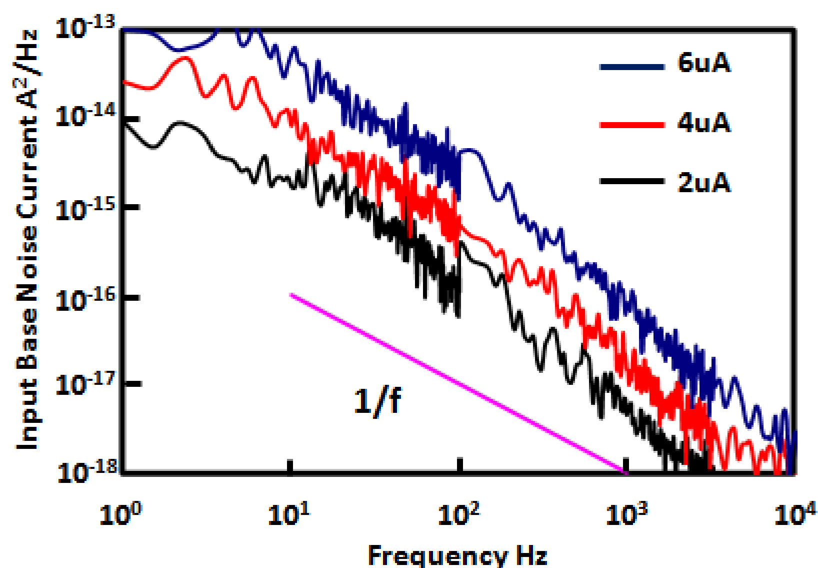

Figure 5.8: SIB curves as function of the frequency for three values of IB at VCE= 1V.

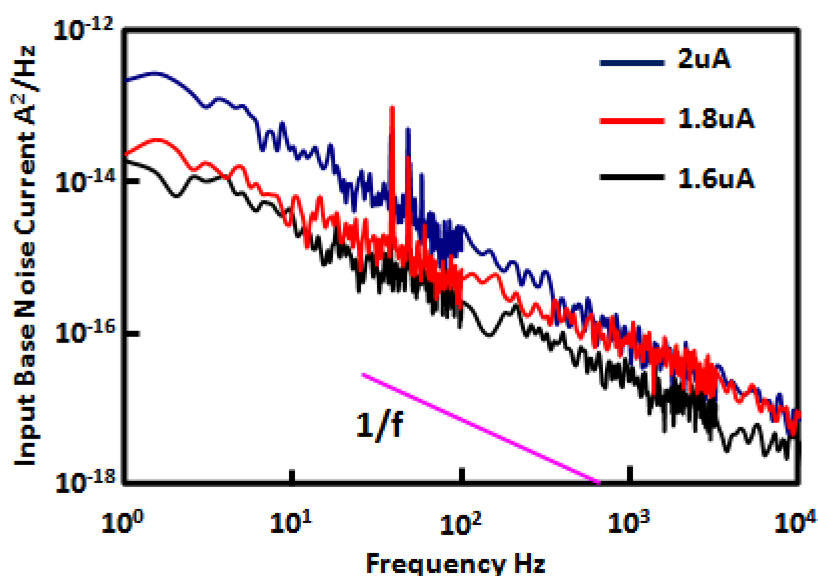

Figure 5.9: SIB curves as function of the frequency for three values of IB at VCE= 1V.

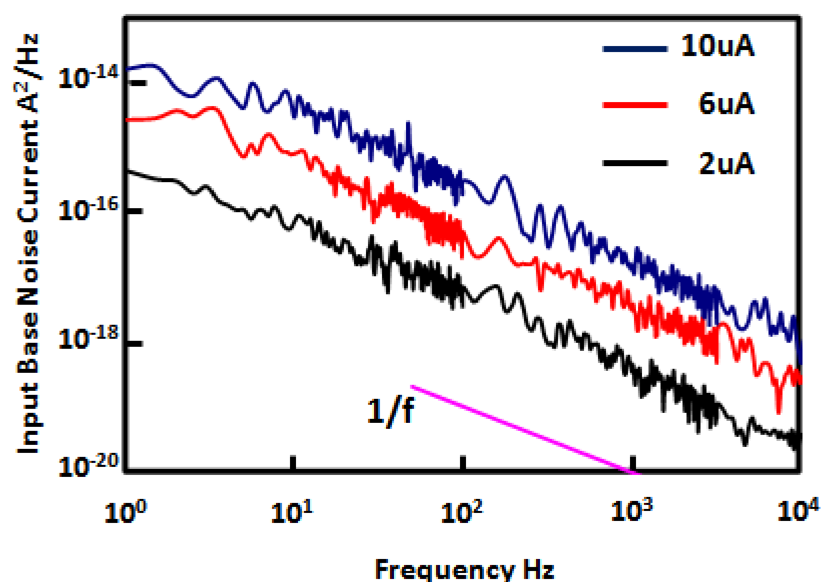

Figure 5.10: S_{IB} curves as function of the frequency for three values of I_B at V_{CE}= 1V.

α is found to be equal to 1.2, 1.6, and 1.3 for Si BJTs, SiGe HBTs and sSi HBTs, respectively. Several publications report that α is in the range of 0.8 to 1.2. However there are reports of α larger than 1.4 [26]. These measurements were performed while the devices are operating in the common-emitter configuration. The V_{CE} was set to 1V, which is smaller than the V_{CEO} for all devices to prevent any impact of avalanche multiplication on the noise measurements [27].

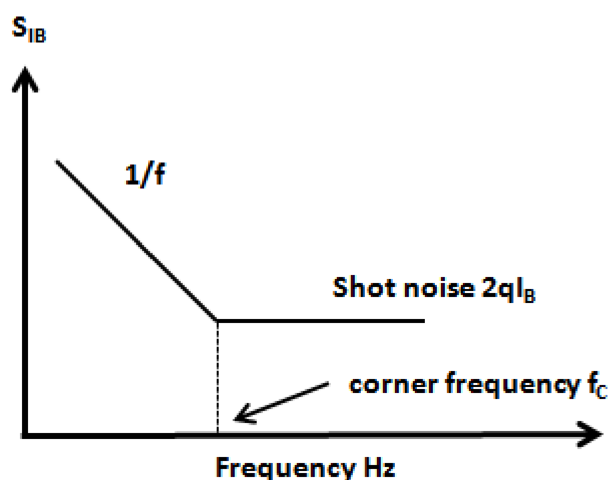

Figure 5.11: Low frequency noise and shot noise intersect at corner frequency f_C

The corner frequency f_C, defined as the frequency where the low frequency noise and the base current shot noise intersect in the frequency domain as shown in Figure 5.11. For

frequency higher than f_C, low frequency noise becomes too small and therefore the base current shot noise is the dominant noise mechanism in the device. This noise, called also shot noise, is not shown in these measurements because 1/f is high and cannot be seen in this frequency range. In the case where the shot noise is visible in the measurement, equation (5.8) is not valid anymore and the term representing the shot noise needs to be added, as shown in the equation (5.9).

$$S_{IB} = K \times \frac{I_B^2}{f^{\alpha}} + 2qI_B \tag{5.9}$$

Although f_C is not shown in the measurements shown earlier, it is possible to calculate it, since at this frequency the low frequency noise is equal to the base current shot noise.

$$S_{IB} = \frac{k\,I_B^2}{f_C} = 2qI_B \tag{5.10}$$

Therefore

$$f_C = \frac{k\,I_B}{2q} \tag{5.11}$$

Equation (5.11) shows that f_C is proportional to I_B and K, however if low frequency noise is proportional to the I_B (and not to I_B^2), f_C would be constant for any base current value as illustrated in the equation (5.12).

$$f_C = \frac{k}{2q} \tag{5.12}$$

The corner frequency f_C can be used as a parameter to compare the noise performance for different devices. A high value of f_C corresponds to poor noise performance. The corner frequency f_C is found to be equal to $1.8{\cdot}10^9$ Hz, $5{\cdot}10^{10}$ Hz and $5{\cdot}10^{11}$ Hz for Si BJTs, SiGe HBTs and sSi HBTs, respectively. This means that the sSi HBTs should exhibit higher 1/f noise compared with the other two device types. Similarly SiGe HBTs should exhibit poor noise performance (high noise) compared to Si BJTs.

Figure 5.12 shows a comparison of the spectral noise density S_{IB} for Si BJTs, SiGe HBTs and sSi HBTs. The latter exhibits a higher noise level as compared to both Si BJTs and SiGe HBTs devices whereas the noise level in SiGe HBTs is higher than in Si BJTs.

The degradation of the noise performance in sSi HBTs is proposed to be caused by high Ge content in the strained-relaxed buffer (SRB), which causes larger density of defects and

dislocations [27, 28]. These defects can be propagated from the substrate and base region all the way to the emitter region which leads to a high noise level. A comparison between the noise performance of SiGe HBTs having 22% Ge content in the base and SiGe HBTs having 35 % Ge content shows that the latter exhibits a higher noise level (two decades at 100Hz), this suggest that it is difficult to increase the Ge content in the base without introduction of dislocations [29].The correlation between the presence of Ge and low frequency noise performance has been also reported for strained Si MOSFETs, where an increase of noise level was related to the increase of the Ge content in the SRB [30].

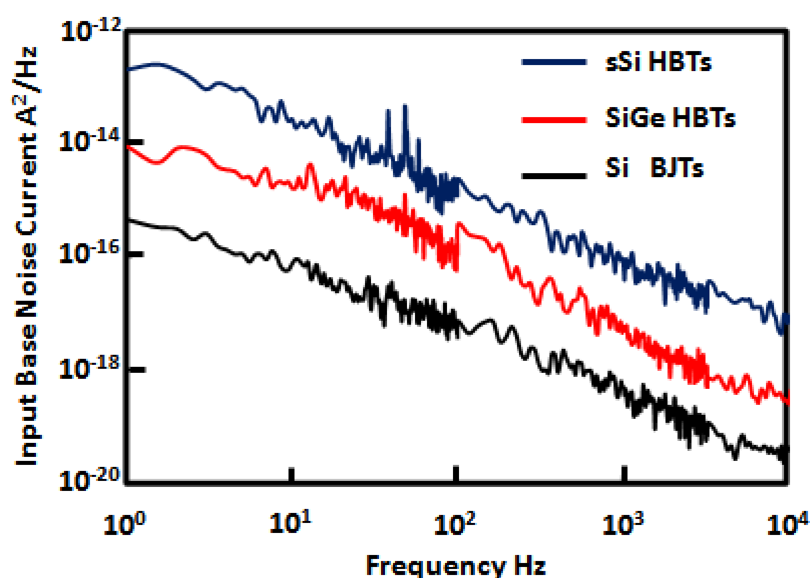

Figure 5.12: Comparison of S_{IB} as function of the frequency for the three types of devices at I_B= 2uA, V_{CE}= 1V.

The dependence of the spectral noise density S_{IB} versus the base current at a given frequency (10Hz, 100Hz) for Si BJTs, SiGe and sSi HBTs is illustrated in Figure 5.13, Figure 5.14 and Figure 5.15 respectively, which show that S_{IB} is proportional to the square of the base current. This quadratic dependence agrees with carrier number fluctuation theory, but does not agree with the mobility fluctuation theory which predicts a linear current dependence [18, 26]. Similarly, Kuo et al [31] report that the increase of the noise spectral density for MOSFETs S_{id} with I_d^2 indicates that a carrier number fluctuation is the cause of 1/f noise.

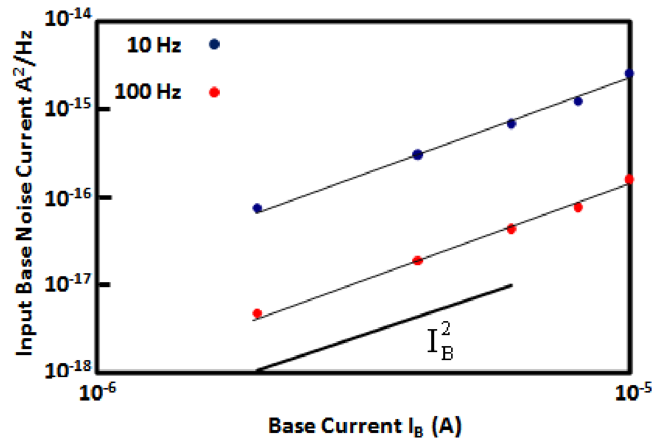

Figure 5.13: S_{IB} curves as function of the base current at fixed frequency (10, 100 Hz) for Si BJTs.

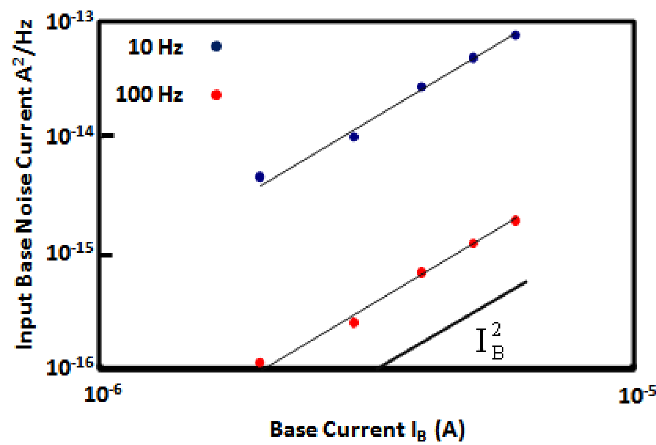

Figure 5.14: S_{IB} curves as function of the base current at fixed frequency (10, 100 Hz) for SiGe HBTs.

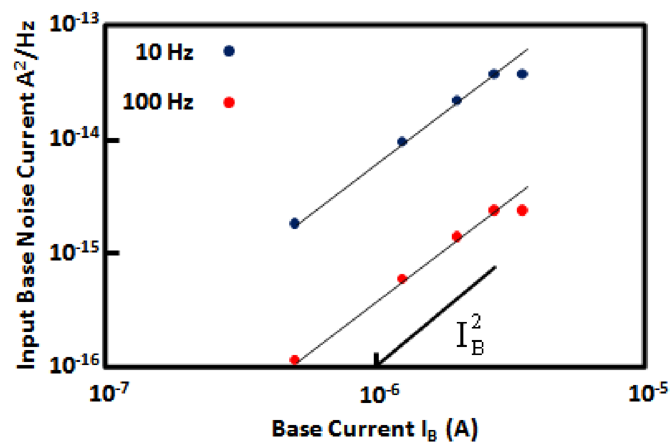

Figure 5.15: S_{IB} curves as function of the base current at fixed frequency (10, 100 Hz) for sSi HBTs.

5.4 Implication for circuit applications

From a device physics point of view, a comparison of the noise at constant I_B makes better sense, because it provides information on the rate of mobility or carrier number fluctuation. However, from an RF circuit point of view, a comparison at constant I_C often provides more insight for circuit applications e.g., oscillators, since the amplitude of oscillators depend on I_C. Furthermore many RF-figures of merit fundamentally depend on I_C instead of I_B e.g; f_T and f_{max}. Even NF_{min}, though dependent on I_B, is often compared at the same I_C as well [32, 33].

Figure 5.16 shows S_{IB} as a function of frequency for Si BJTs, SiGe HBTs, and sSi HBTs for a constant collector current (I_C=1mA).

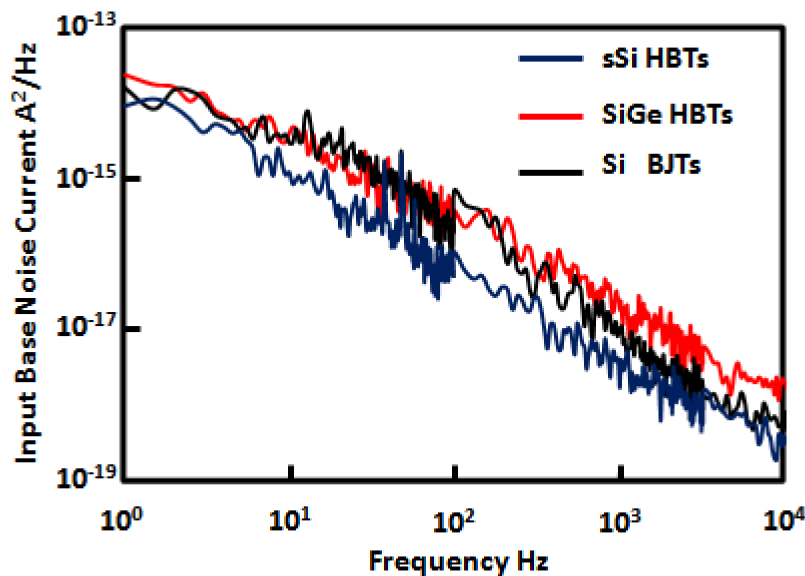

Figure 5.16: Comparison of S_{IB} as function of the frequency for the three types of devices at I_C= 1mA.

Presented in this way, the S_{IB} of SiGe HBTs is approximately as the same as that of Si BJTs. However, the S_{IB} of sSi HBTs is lower than S_{IB} of Si BJTs and SiGe HBTs. This result can be explained by considering the high current gain of sSi HBTs, which lead to a lower DC base current for a given magnitude of collector current, thus low current noise. This can be explained further by considering the equation (5.13)

$$S_{IB} = K \times \frac{I_B^2}{f^{\alpha}} \tag{5.13}$$

Since

$$I_B = \frac{I_C}{\beta} \tag{5.14}$$

Then

$$S_{IB} = K \times \frac{1}{f^{\alpha}} \times \left(\frac{I_C}{\beta}\right)^2 \tag{5.15}$$

Equation (5.15) shows that S_{IB} is proportional to I_C and inversely proportional to β. For the same collector current, the current gain is very high for sSi HBTs compared to other devices, thus lower noise (better performance).

A similar conclusion was reported by Bary et al [27, 34] for SiGe HBTs compared to Si BJTs. A comparison between two SiGe HBTs devices, with different Ge content in the base (14 %and 18 %) was performed. It was found that SiGe HBTs (18 %) have a lower S_{IB} at constant I_C compared to SiGe HBTs which have 14 % Ge content in the base. This is because the devices featuring higher Ge exhibit a lower DC base current for the same collector current and thus a lower current noise magnitude.

As was discussed earlier, at frequencies higher than f_C, the base current shot noise dominates. This noise results from the flow of current in the EB junction. This current is composed of many individual current pulses which are random. For the same collector current, the sSi HBTs needs a small base current compared to SiGe HBTs and Si BJTs. This is because of the inherently high current gain of sSi HBTs. Given the equation of the base shot noise it is possible to calculate its value which corresponds to I_C= 1mA.

$$S_{IB} = 2qI_B = 2q\left(\frac{I_C}{\beta}\right) \tag{5.16}$$

The base shot noise is found to be equal to $6{\cdot}10^{-20}$ (A^2/Hz), $4{\cdot}10^{-19}$ (A^2/Hz) and $2{\cdot}10^{-18}$ (A^2/Hz), for sSi HBTs, SiGe HBTs and Si BJTs respectively. It is clear that the sSi HBTs exhibit the lowest base current shot noise.

An important issue for integrated transceiver design is to minimize voltage-controlled oscillator (VCO) phase noise. Ideally, a purely sinusoidal output is required, the spectrum of which is a perfect delta function in the frequency domain. In reality, transistor noise causes random variations of both amplitude and phase. The amplitude noise is suppressed by the oscillator built-in amplitude limiting mechanisms and is negligible. The phase noise, however, shows up as a random variation in oscillation period or deviation of the zero crossings from

their ideal positions along the time axis. The exact mechanism of phase noise is complicated and is still an active area of research. However it is possible to understand the basic behaviour of up-conversion of physical transistor noise to phase noise S_{ϕ} by considering the equation.

$$S_{\phi} \propto \frac{S_{IB}}{(2\pi f)^2} \tag{5.17}$$

This demonstrates that the phase noise is proportional to the S_{IB} noise and inversely proportional to f^2. For noise with frequency independent also known as shot noise (white noise), S_{IB} is frequency independent and thus S_{ϕ} is proportional to $1/f^2$. For 1/f noise S_{IB} is proportional to 1/f, therefore S_{ϕ} is proportional to$1/f^3$. If this simple theory is applied to the transistor base current noise, the phase noise will look similar to the dependencies shown in Figure 5.17 [27].

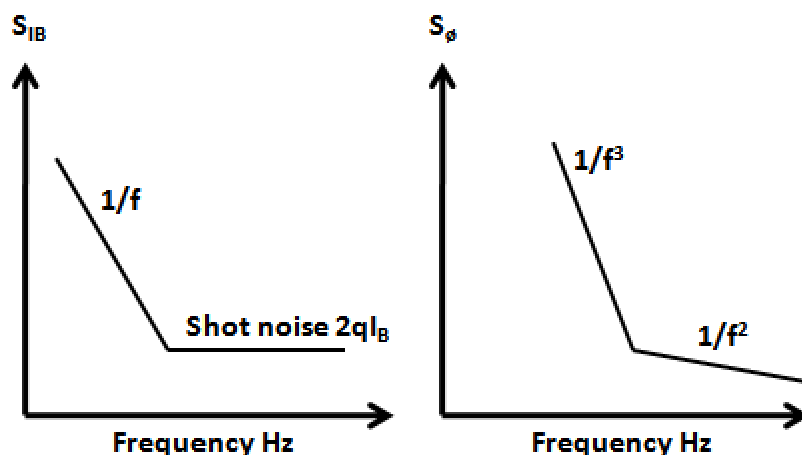

Figure 5.17: Simplified time domain model for upconversion of transistor physical noise to oscillator phase noise.

Considering a phase noise comparison for all devices at fixed collector current, it can be concluded that sSi HBTs will exhibit lower phase noise compared to SiGe HBTs and Si BJTs, and this is for two reasons. Figure 5.16 shows that sSi HBTs exhibit lower S_{IB} at I_C=1mA, which will be reflected in the phase noise, since the latter is proportional to S_{IB}. Similarly, the sSi HBTs exhibit a low base current shot noise at given collector current, which will also affect the phase noise directly, resulting in lower phase noise for sSi HBTs. Considering the explanation above the phase noise of all devices can be predicted. The aim of this prediction

is not to give exact values of the phase noise, it is rather a comparative study. This comparison is illustrated in Figure 5.18.

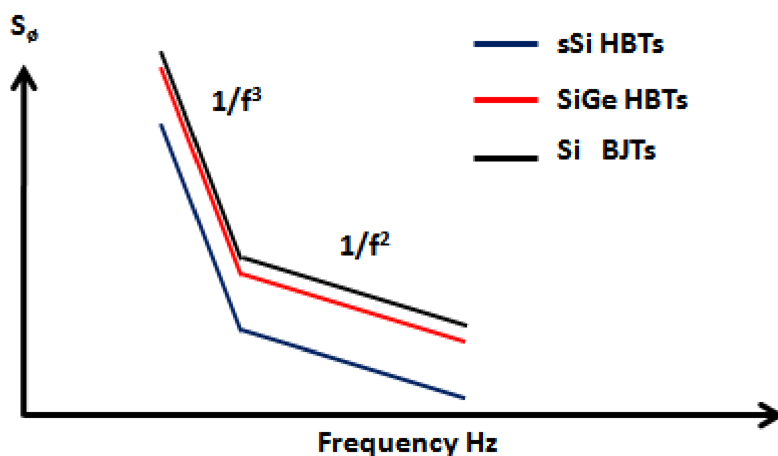

Figure 5.18: Comparison of the phase noise between Si BJTs, SiGe HBTs and sSi HBTs.

A similar methodology was used by Niu at al [33], where a comparison of 1/f noise for Si BJTs and different SiGe HBTs was conducted. This was followed by the simulation of phase noise of a single-transistor amplifier. A calibrated vertical bipolar inter-company model was used. The VBIC model is known fpr its capability to include different types of noise: shot noise, thermal noise and low frequency noise. The model parameters were extracted from the measured dc data, S-parameters, and low frequency noise data. Higher-order effects including self-heating and avalanche multiplication were taken into account in the VBIC model. The simulation shows that the device with lower S_{IB} at given collector current, also exhibits a low phase noise for fixed collector current.

5.5 Defect characterisation

The key idea in the fabrication of the sSi HBTs has been the usage of the strain-relaxed buffer (SRB) to boost the amount of the Ge content in the base [35]. The strain-relaxed buffer, often referred to as virtual substrate (VS), consists of growing a thick SiGe layer, in which the Ge concentration is increased from 0% to 15% in smooth way (10%-Ge µm-1). This layer is topped with a SiGe layer with fixed Ge content. Relaxation in the SiGe layer can be induced by promoting the formation of misfit dislocations during early stages of the growth, these defects are known to degrade the device performance and act as noise generators.

In order to investigate the impact of the strain-relaxed buffer in terms of defect density on the degradation of the noise performance, defect characterization was performed on blanket material grown simultaneously with the processed wafers. A modified Schimmel etch [36] was used to reveal defects. The impact of strain-relaxed buffer on strained Si MOSFETs noise performance is reported in many publications. Hua et al [37] presents a comparison between the Si MOSFETs and strained Si MOSFETs devices. This study shows that strained Si MOSFETs exhibit high noise magnitude compared to Si control devices. This degradation in the noise performance was linked to the presence of high defect density in strained Si MOSFETs caused by strain-relaxed buffer.

Similar study was reported in [30, 38], which compares the noise performance of strained Si MOSFETs with different Ge content in strained-relaxed buffer (15%, 20% and 28 %). This work confirms a clear trend in noise magnitude with respect to Ge concentration in the virtual substrate: the higher the Ge concentration, the higher the level of the low frequency noise. The increase of the noise as a function of increased Ge concentration in the strained-relaxed buffer is associated with an increase in trap density in the gate oxide.

Using the strain-relaxed buffer in MOSFET technology leads to global biaxial strained Si and in the channel region in particular. However it is possible to use uniaxial strained Si, which uses process induced stress locally to enhance the device performance. Kuo et al [31]report that Uniaxial Strained PMOSFETs show similar noise performance compared to a Si MOSFETs control, The number of occupied traps were extracted by the charge pumping method which shows that the trap density are only 9% larger than its control counterpart.

A study was reported by Van Haaren et al showing that SiGe HBTs having 22% Ge content exhibit lower noise magnitude (better noise performance) compared to SiGe HBTs having 35% Ge content (tow decade at 100Hz). This suggests that it is difficult to increase the Ge content to improve the current gain without introducing defects and therefore degrading the noise performance [29].

Figure 5.19 shows an optical image of the sSi HBTs material following Schimmel etching. The solid lines correspond to the misfit dislocations and the dots correspond to threading dislocations. This figure shows the defects in both interfaces: strained Si / SiGe interface and the SiGe / strain-relaxed buffer interface. This is because the lattice constant is different in

the SiGe and strained-relaxed buffer (due to the different Ge content 15 %, 30%), similarly the lattice constants of strained Si and SiGe are different which leads to the presence of defects. Figure 5.20 shows an optical image of the SiGe HBTs material following the same Schimmel etch treatment. This image is for Si (Collector) / SiGe interface. In contrast with the strained Si HBTs, the SiGe HBTs exhibits a much lower threading dislocation density (TDD) and no misfit dislocations. It is also important to note that no defects are expected in the SiGe (base) / Si (emitter) interface, because the SiGe (base) is compressed and therefore it has the same lattice constant as Si.

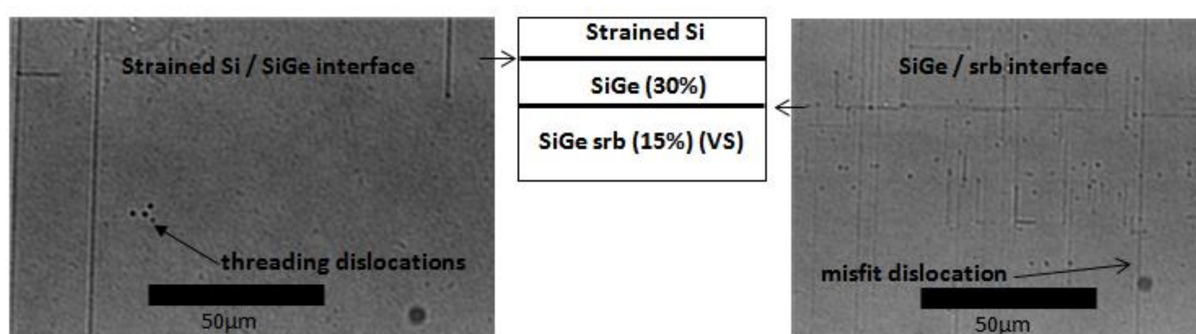

Figure 5.19: Surface morphology at the strained Si/SiGe interface and SiGe / SRB interface. The black points are the threading dislocations and the black lines are misfit dislocation.

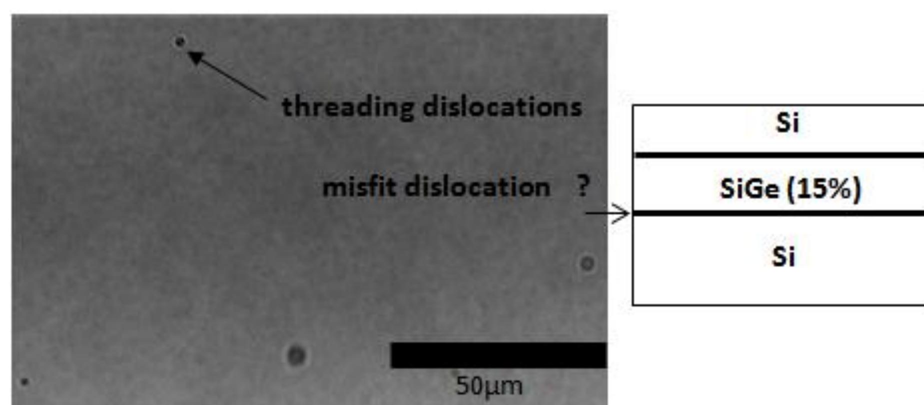

Figure 5.20: Surface morphology at the strained Si / SiGe interface (SiGe HBT).The black points are the threading dislocations.

Table 5.1 and Table 5.2 summarize the TDD and misfit dislocation density (MDD) values found in both HBT materials. They show that there is a moderate MDD at the strained Si / strained SiGe interface but much higher at the strained SiGe / SRB (virtual substrate) interface in sSi HBTs. In contrast no misfit dislocations were observed in Si / strained SiGe interface in SiGe HBTs. TDD is nearly two orders of magnitude higher in strained Si HBTs

compared with SiGe HBTs. TDD (1.7×10^{6} cm^{-2}) in the sSi HBTs is considered to high compared to the value reported by Hartmann et al which is $1.06\pm0.36\times10^{5}$ cm^{-2} [39].This high density of defects explains the degradation of the noise performance in sSi HBTs compared with SiGe HBTs.

Misfit Dislocation Density		
Strained Silicon HBTs		**SiGe HBTs**
Strained Si/ Strained SiGe interface	**Strained SiGe/SRB interface**	**Si/ Strained SiGe interface**
190 cm^{-1}	800 cm^{-1}	0 cm^{-1}

Table 5.1: Density of misfit dislocation.

Threading Dislocation Density	
Strained Silicon HBTs	**SiGe HBTs**
1.7×10^{6} cm^{-2}	3.5×10^{4} cm^{-2}

Table 5.2: Density of threading dislocation

5.6 Generation-recombination noise

Many defects that exist in semiconductor devices are unintentional. Elements such as carbon, oxygen and various metals may be introduced to the wafer during fabrication, and then become carrier trap centres that affect device performance and produce generation–recombination (g-r) noise. This noise is due to random fluctuations in the trapping and detrapping rates in the defect trap centres in the forbidden energy band gap. This in turn causes the current, or the voltage, to fluctuate as well [28, 40].

A deviation from the $1/f^{\alpha}$ spectrum with $\alpha=1$ to a spectrum with $\alpha<1$ followed by a change to an $1/f^{2}$ dependence and then back to 1/f, is characteristic of g-r noise [41], as shown in Figure 5.21.

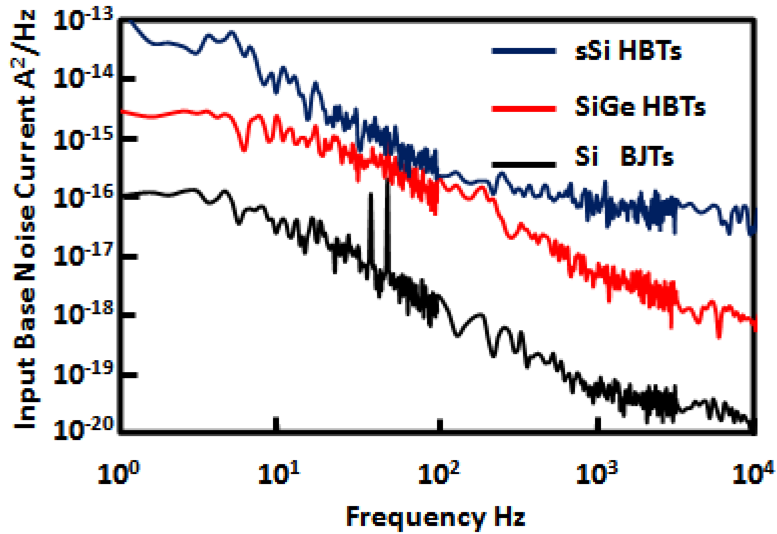

Figure 5.21: Generation-recombination noise.

This noise has been reported in other semiconductor devices e.g. MOSFET [42]. Generation recombination noise is found to exhibits a Lorentzian spectrum $1/f^2$, and the noise spectrum can be expressed as [42]

$$S_{I_B} = \alpha_r \times \frac{\tau}{1 + (2\pi f\tau)^2} \tag{5.18}$$

Where α_r is the amplitude and τ is the characteristic time constant. The noise spectrum is flat at low frequency and decrease as $1/f^2$ at high frequency, as illustrated in Figure 5.22. The superposition of a large number of Lorentzian spectra with $1/\tau$ distribution results in 1/f noise.

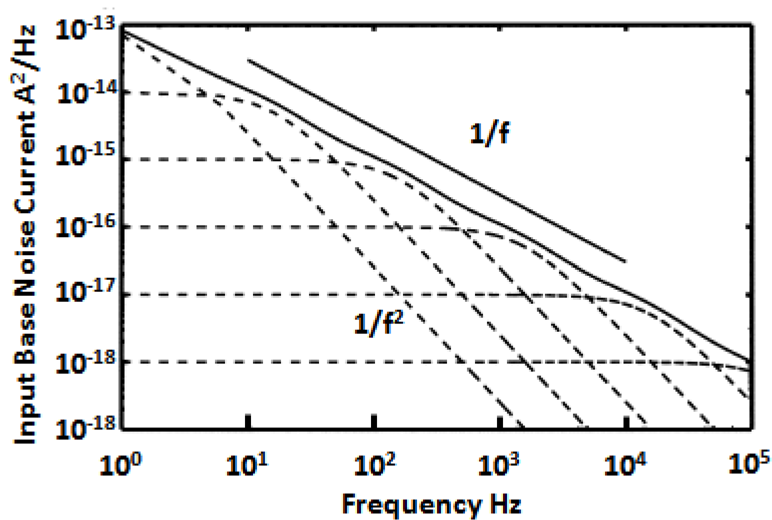

Figure 5.22: 1/f noise as a superposition of Lorentzians.

5.7 Impact of processing on low frequency noise

Low frequency noise is known to be very sensitive to the fabrication process. Epitaxial growth is now one of the necessary steps in semiconductor fabrication, especially for devices where different materials with similar lattice constant are used (heterostructure devices) e.g. [Si/SiGe], [AlGaAs/GaAs]. However, care must be taken in growing material so not to introduce defects, which will have a destructive impact on the device performance. Implantation is also an important process which is used in the doping of semiconductors. This process is preferred by designers since it is more controllable than doping using diffusion techniques. Implantation is known to introduce defects (damage), which are expected to be removed after annealing. However a low temperature and short time thermal treatment is needed to maintain the junction depth after ion implantation, which may not be sufficient to remove the implantation-induced defects. These defects cannot be a source of leakage current only but also of low noise frequency [43]. Another source of defects which is linked very well to the low frequency noise is the oxide in the polysilicon-silicon interface in the emitter region. The oxide is reported to increase the current gain in bipolar devices by presenting a barrier to the diffusion of holes in the emitter [44]. However, it is responsible for the presence of defects.

Siabi-Shahrivar et al [45, 46] have studied the effects of processing on the noise characteristics of polysilicon emitter Si BJTs. It was found that the surface treatment of the emitter has a fundamental impact on the noise level as well as the DC performance of the devices. Since the introduction of the polysilicon in bipolar technology, there have been many surface treatment methods:

- HF etch: this method consists of using hydrofluoric acid to treat the emitter surface prior to the deposition of the polysilicon. This method results in a thin nonuniform interfacial oxide with 0.4 nm thickness. The thickness can vary from 0 to 0.8 nm.
- RCA clean. This is a popular wet chemical clean which results in a 1-1.4 nm thick interfacial oxide that is relatively uniform.
- High-temperature anneal (1000°C) after the polysilicon deposition but before emitter implantation results in 'balling' of the oxide layer in which the diameter of the sphere is approximately 8nm.

- For sufficiently high temperatures (1050°C), there is epitaxial regrowth of the polysilicon layer.

These surface treatments have a significant impact on the current gain as well as the noise level in the device. A summary of the noise voltage and the current gain as well as the cleaning procedure is presented in Table 5.3. The first striking result to emerge from these data is that the surface treatment method which gives low noise level also results in high current gain. This proves the correlation between the oxide and low frequency noise as well as between the oxide and the current gain. It is also important to mention that the RCA cleaning method, which results in high current gain and low noise performance, is the method used in the fabrication process for all devices presented in this work. Therefore, it is possible to optimize the fabrication process of the sSi HBTs for RF application by trading off the high current gain (of sSi HBTs) to the noise performance. This is can be accomplished using a different surface treatment.

	RCA clean	**RCA fluorinated**	**HF clean**	**Balled oxide**	**Epitaxial alignment**
S_V (nV / Hz)	50	16	14	8.5	7
Current gain	1300	1100	75	45	20

Table 5.3: Comparison of noise voltage at 10 Hz and current gain in polysilicon emitter BJTs with different surface treatment.

Deen et al [47] present the effect of rapid thermal annealing on the noise. RTA is a technique commonly used to activate implanted species and remove the damage. This annealing is accomplished with little redistribution of the dopant atoms when compared to conventional thermal annealing procedures which are much longer, and RTA is therefore essential for devices of very small dimensions.

The impact of the thermal budget is summarized in Figure 5.23, which shows that increasing the temperature or the time (or both) improve the noise performance of the device. This proves that a high temperature (on the order of 1000 ºC) can anneal defects.

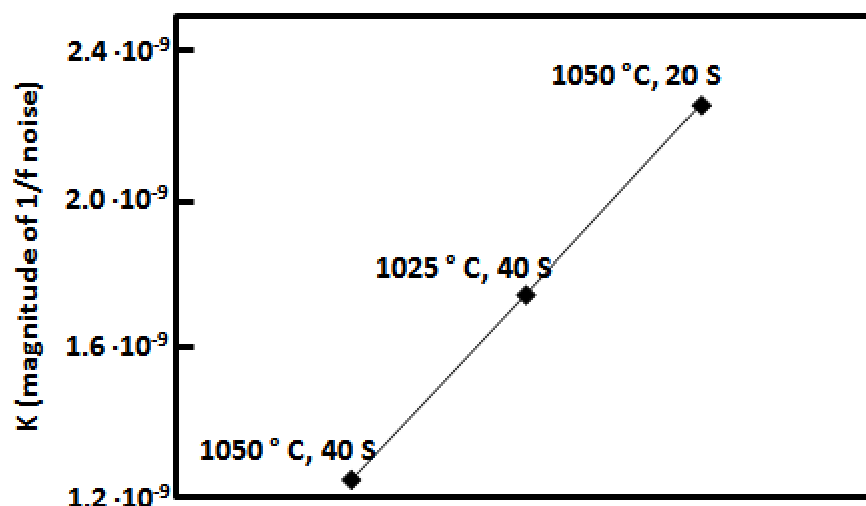

Figure 5.23: impact of time and temperature on low frequency noise

As was stated in chapter 3, a batch split was included, with either 900 ºC or 925 ºC anneal for 10 s. This step was considered to optimize the fabrication process of sSi HBTs. It was found that 925 ºC is more suitable for sSi HBTs, however this is not the case for Si BJTs which show higher current when annealed at 900 ºC. Similarly, low frequency noise measurements were performed for all devices annealed at 925 ºC and compared to those annealed at 900 ºC. The results are shown in Figure 5.24, Figure 5.25 and Figure 5.26. According to these data, rapid thermal annealing (RTA) has no clear impact on spectral noise density S_{IB}, suggesting that the increase of the temperature from 900 ºC to 925 ºC does not reduce the defect in the bulk material and also in the thin interfacial oxide in the polysilicon/silicon interface. This suggests also that low temperature and short time thermal treatment cannot reduce defects. The result reported in Figure 5.23, where a high temperature has been used in the thermal treatment (1050 ºC) concerns Si BJTs with very large base width. This is a very important observation, since it is difficult to use high temperature in the fabrication process for small feature devices, because high temperature will cause more dopant diffusion. This difficulty is even more serious for Si/SiGe heterostructure devices. Due to the metastable property of strained SiGe/Si heterostructure, SiGe layers can only grow commensurately to a critical thickness on Si substrates (for SiGe HBTs, the same thing apply to sSi HBTs). A high temperature anneal can create further dislocations if critical thickness is exceeded [48]. This means that for small sSi HBTs, increasing the thermal budget to reduce the defect density and improves the noise

performance is not valid method. However using the right surface treatment and improving the epitaxy is a better solution.

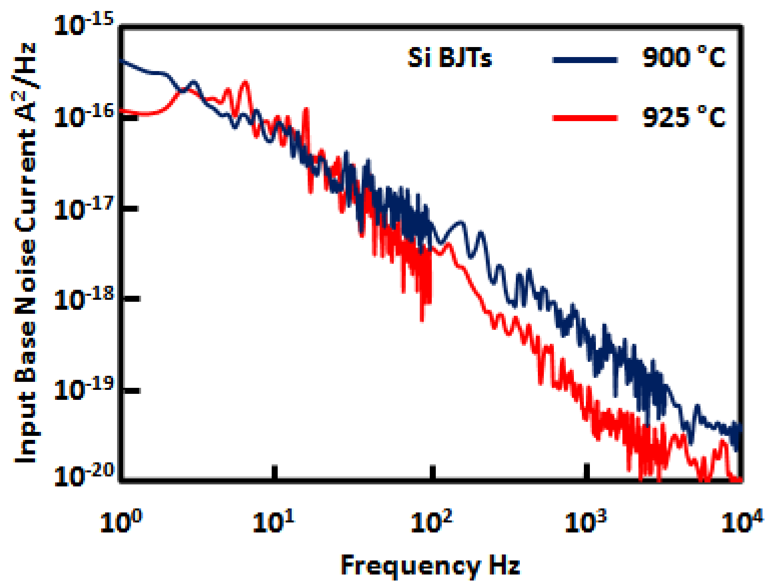

Figure 5.24: Impact of RTA on low frequency noise in Si BJTs.

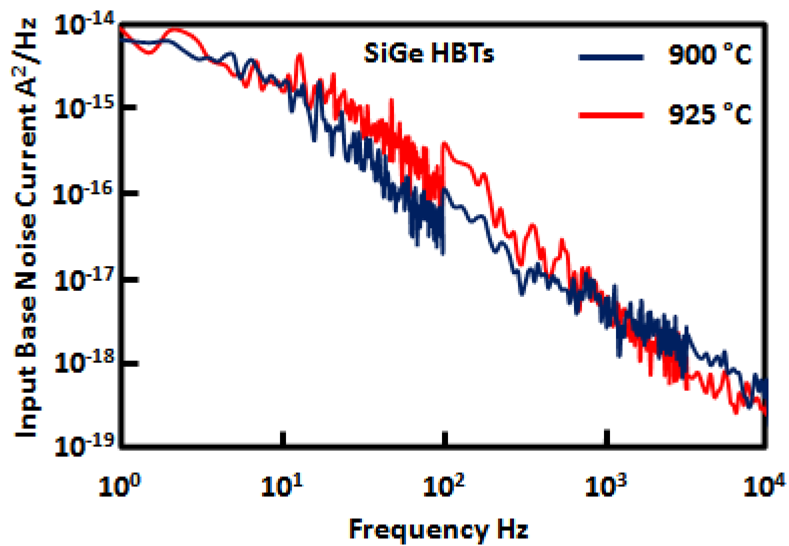

Figure 5.25: Impact of RTA on low frequency noise in SiGe HBTs.

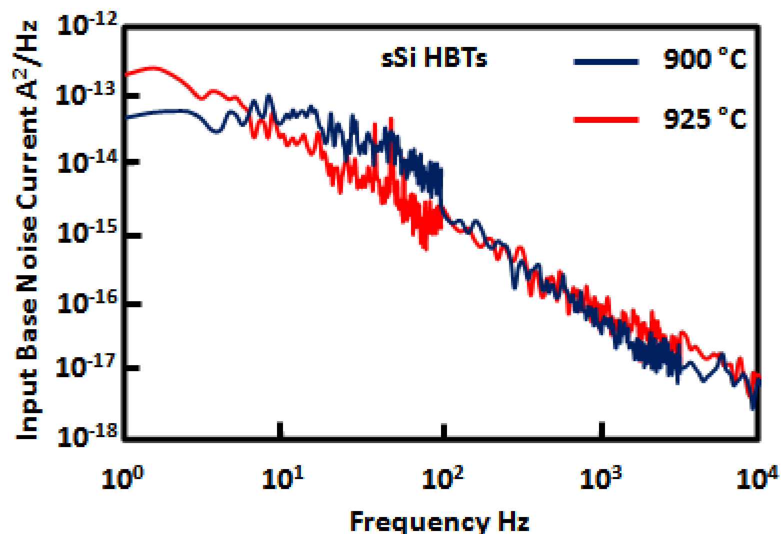

Figure 5.26: Impact of RTA on low frequency noise in sSi HBTs.

5.8 Conclusion

This chapter reports the first study of the noise performance of sSi HBTs. The strained-relaxed buffer, which has been used to increase the Ge content in the base, improves the current gain of devices. However, it results in high levels of defects in sSi HBTs devices. This results in degradation of the noise performance for constant base current. A defect characterisation was performed to prove the correlation between defect density and the noise level in the devices, showing that high defect density results in high noise level.

The strained Si HBTs exhibit a higher current gain compared to control devices. If the noise comparison is performed at a fixed collector current, the sSi HBTs offers lower noise levels than either co-processed SiGe HBTs or Si BJTs. The low noise level in sSi HBTs (at fixed collector current) will result in low phase noise in circuit application. This result is of great importance for circuit designers.

The fabrication process has a fundamental impact on the noise level in the devices. Optimizing the fabrication process of the sSi HBTs will enhance their capability to be used in RF circuits. Improving the epitaxy to prevent defects from moving from the SRB to the intrinsic device would have a great impact on the noise performance of the device, but more importantly, the surface treatment of the emitter prior to the polysilicon deposition should be optimal. Literatures show that the surface treatment which gives highest current

gain results in low noise performance. It is possible therefore to trade-off the high current gain (of sSi HBTs) against the noise performance.

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Chapter 6. Summary & Future work

6.1 Summary

This project presents the first experimental demonstration of sSi HBTs. The electrical characterisation shows that this novel device exhibits a high current gain compared to co-processed SiGe HBTs and Si BJTs. A simulation study showed that the high Ge content in the base is the key factor that has lead to this enhancement. Another important outcome is that it is possible to model the performance of this novel device using the same tools that is used for Si BJTs and SiGe HBTs. The new improvements that have been achieved in the fabrication of MOSFETs based on high mobility material such as Ge and GaAs have shown the importance of these materials in the future of the bipolar semiconductor technology. MEDICI simulator was used to investigate the potential of the bipolar based on Ge and GaAs. The results show that such devices might have good current gain, however the band discontinuity and more precisely the valence band discontinuity is a key factor in limiting this device from reaching its full potential.

The bipolar technology is known to be the first choice in the RF market due to its high noise performance and high speed. This work has shown that sSi HBTs exhibits high noise level compared with the co-processed SiGe HBTs and Si BJTs. This was linked to the high defects density in ssi HBTs that is caused by the implementation of the Strain Relaxed Buffer. This result was confirmed using defect characterisation. The sSi HBTs exhibits a higher current gain compared to other devices. Therefore, the base current can be reduced in a circuit while maintaining the collector current constant. If the noise comparison is performed at a fixed collector current, the sSi HBT offers lower noise levels than either co-processed SiGe HBTs or Si BJTs. The low noise level in sSi HBTs (at fixed collector current) will result in low phase noise in circuit application. This result is of great importance for circuit designers.

Using a strain-relaxed buffer to grow strained Si in the channel has led to significant improvement of the performance of MOSFET technology. However this is the first time that a SRB has been used to improve the bipolar technology. This is has opened the door widely to the possibility to integrate the novel sSi HBTs with strained Si MOSFETs in one ship. The

material characterisation of sSi HBTs has actually favourite this possibility, since the Raman spectroscopy has shown that that the strain in the emitter of the sSi HBTs was fully maintained following processing.

6.2 Future work

The integration of strain-relaxed buffer in bipolar technology has lead to the fabrication of the first sSi HBTs. This device offers very high current gain compared with both Si BJTs and SiGe HBTs. However, this project has highlighted the need for more work to improve and explore the potential of this novel device. Self-heating is one of the major problems that cause a degradation of the performance of this device. The MOSFETs devices that use SRB to produce biaxial strain also suffer from the self heating. The low thermal conductivity of SiGe that forms the strain relaxed buffer is the source of this problem. With the recent development in material growth, it has been possible to use a thin SRB in the fabrication of strained Si MOSFETs to reduce the self heating phenomena. Therefore, it is possible to apply this solution in the fabrication of sSi HBTs.

The bipolar devices have mostly used in analogue application. This is mostly because of their high speed and high noise performance. The latter is directly linked to the defect density in the device. The defect characterisation that has been done in this work has proved the existence of high defects density in the sSi HBTs compared to Si BJTs and SiGe HBTs. The SRB, which has been used to increase the Ge content in the base, improves the current gain of devices. However, it results in high levels of defects to be introduced in sSi HBTs devices. This results in degradation of the noise performance for constant base current. Therefore, improving the epitaxy growth of the SRB to prevent defects from moving to the intrinsic devices would have a great impact on the noise performance of the device. Another aspect to improve the noise performance is to focus on the surface treatment of the emitter prior to the polysilicon deposition that offers better noise performance.

Since the fabrication of the first bipolar transistor, there have been many improvements of the design of this device. In many cases the device is designed in particular way depending on the application. The fabricated sSi HBTs devices are actually large area. Therefore, it is not possible to use them to assess the speed of this device. In the current world, there is always a need of faster device, hence the importance to fabricate a new sSi HBTs that is

suitable for RF application. The Mesa structure that is used in the current device form a large extrinsic parasitic element, which limits the device speed. Therefore, it is important to use planner design.

The new improvements that have been achieved in the fabrication of MOSFETs based on high mobility material such as Ge and GaAs have shown the importance of these materials in the future of the bipolar semiconductor technology. Based on this study, a bipolar transistor based on these high mobility materials looks promising. However, the band discontinuity and more precisely the valence band discontinuity is blocking this device from reaching its full potential.

Appendix

Densities of state and band-gap values for different layer

Layer	Density of state N_C (cm^{-3})	Density of state N_V (cm^{-3})	Band-gap (eV)
Si	N_C=2.83E19	N_V=2.5E19	1.17
Strained Si	N_C=1.05E19	N_V=0.8E19	1.10
$Si_{0.85}Ge_{0.15}$	N_C=1.9E19	N_V=1.1E19	1.04
$Si_{0.7}Ge_{0.3}$	N_C=1.9E19	N_V=1.1E19	0.94

Recombination constants

AUGN	The Auger coefficient for electrons. cm6/s	2.8e-31
AUGP	The Auger coefficient for holes. cm6/s	9.9e-32
DN.AUGER	The exponent of temperature for the Auger coefficient for electrons.	0
DP.AUGER	The exponent of temperature for the Auger coefficient for holes.	0
AN	The constant term in the concentration-dependent expression for electron lifetime.	1
BN	The linear term coefficient in the concentration-dependent expression for electron lifetime.	1
CN	The exponential term coefficient in the concentration-dependent expression for electron lifetime.	0
NRSHN	The Shockley-Read-Hall concentration parameter for electrons.	5e16 cm^{-3}
EN	The exponent in the concentration-dependent expression for electron lifetime.	2
AP	The constant term in the concentration-dependent expression for hole lifetime.	1
BP	The linear term coefficient in the concentration-dependent expression for hole lifetime.	1
CP	The exponential term coefficient in the concentration-dependent expression for hole lifetime.	0
NRSHP	The Shockley-Read-Hall concentration parameter for holes.	5e16 cm^{-3}
EP	The exponent in the concentration-dependent expression for hole lifetime.	2
ETRAP	The trap level (E_t - E_i) used in determining the Shockley-Read-Hall recombination rate.	0 eV
TAUP0	The Shockley-Read-Hall hole lifetime.	1e-7 s
TAUN0	The Shockley-Read-Hall electron lifetime.	1e-7 s