CRANFIELD UNIVERSITY

Charalampos Fragkiadakis

# Integration of sol-gel frequency agile materials for tunable RF devices

School of Applied Sciences

Nanotechnology Group

PhD Thesis

CRANFIELD UNIVERSITY
School of Applied Sciences, Department of Materials
Nanotechnology Group

PhD Thesis
Academic Year 2011–2012

Charalampos Fragkiadakis

# Integration of sol-gel frequency agile materials for tunable RF devices

Paul B Kirby
Supervisor

January 2012

This thesis is submitted in partial fulfilment
of the requiremetns for the degree
of Doctor of Philosophy

To my parents and dear partner Giota for their love and support

# Abstract

This thesis focuses on the use of high permittivity tunable dielectrics and more specifically sol-gel ferroelectric thin films for low cost, high performance tunable devices such as varactors and filters at RF and microwave frequencies. The topics covered include measurement techniques for the characterization of tunable dielectrics at low and microwave frequencies, fabrication processes, electrical and acoustic modeling of thin film ferroelectric varactors, performance optimization using conductive electrodes, realization of tunable microwave circuits and integration of tunable dielectrics with conventional bulk acoustic wave resonators (FBAR).

A lead strontium titanate (PST) sol-gel ferroelectric varactor is designed, electrically and acoustically modeled and fabricated, displaying dielectric tunability of $\sim$75%. A two port automatic extraction technique using MATLAB allowing the de-embedding of parasitic connecting transmission lines, as well as parasitic pads has been developed and presented, yielding accurate dielectric permittivity values in good agreement with literature. The potential factors that may compromise the electrical performance of the ferroelectric tunable varactor are analyzed and a novel Au/$TiO_2$ bottom electrode stack process is proposed and shown to improve the RF performance of the tunable varactor lowering the overall metalization resistance and improving performance, compared to the commonly used Pt electrodes. To establish the possibility of tunable microwave systems integrating sol-gel ferroelectric tunable varactors the following novel microwave devices are designed, modeled and fabricated:

A ferroelectric varactor-based RF resonant switch, integrating a thin film sol-gel PST ferroelectric varactor with a high Q micro-machined inductor is fabricated. An insertion loss of ∼1.5 dB and isolation of ∼18 dB have been achieved for a single 7 GHz resonant switch with a device area of 0.6 mm × 1 mm. The intrinsic performance limitations of this type of device due to the ferroelectric thin film are discussed and the implementation of cascaded switches and state-of-the-art ferroelectric materials for further improvement of performance of this device, have been considered and simulated.

Tunable band-stop resonators and notch filters using sol-gel PST ferroelectric varactors in a coplanar waveguide (CPW) defected ground structure are fabricated and measured. The PST varactors tune single resonators and 3-pole band-stop filters, operating at the center frequency of 4 and 8 GHz, having a maximum rejection of more than 13.8 dB at the stop band, while the insertion loss at the pass band is less than 3 dB. Full-wave analysis is performed to identify the critical points, where PST varactors are implemented to adjust the resonance frequency of the devices. An optimized fabrication process allows for fabrication of a 3-stage filter with a maximum rejection of 28 dB, albeit with a reduced tuning range, possibly due to DC bias path leakage.

Finally, a fabrication approach where a ferroelectric varactor is integrated with a conventional zinc oxide (ZnO) acoustic wave resonator is presented. The approach avoids the piezoelectric thin film degradation due to the ferroelectric annealing by first fabricating the ferroelectric varactor and superimposing the conventional FBAR on top of it. The tuning of the series resonant frequency of a conventional ZnO FBAR with a ferroelectric varactor is demonstrated. Field induced deformation limits the maximum shift of the resonance to 0.45% at 1.5 GHz, for 41% tunability of the ferroelectric varactor, suggesting a big scope for possible improvements in performance by improving the design and fabrication.

# Acknowledgements

I would like to express my gratitude to Dr. P.B. Kirby for offering me the opportunity to pursue this postgraduate study at Cranfield University under his supervision. I would also like to thank Mr. R.V. Wright for his input, support and insightful discussions on almost every scientific aspect related to this research.

During the years of my thesis research and those when I worked as a Research Assistant, I have worked and established collaboration with people from many universities and institutions, for who I would like to express my appreciation. I would like to thank Dr. Peng Bao, Dr. Timothy J. Jackson and Prof. Michael J. Lancaster from the Electronic, Electrical and Computer Engineering department in Birmingham university, as well as Dr. Young-Hoon Chun and Prof. Hong Jia-Sheng from Herriot-Watt University for our collaboration in the Frequency Agile Materials project. Furthermore, I would like to thank Dr. Andrew Laister and Prof. Bob Miles from the Electrical and Electronic Engineering department in the University of Leeds for their collaboration in the Flagship project and assisting in high frequency measurements. Finally, I would like to thank Mr. Liam Floyd and Prof. Roger W. Whatmore in Tyndall Institute, Cork, Ireland.

I do feel grateful to many people from the Nanotechnology group in Cranfield University, especially my dear friends and co- patriots Dr. Petros Gkotsis, who has also been a great flat-mate and Dr. George Skoufias. Of course a lot of people from the group have been very supportive and helpful like Dr. Glenn Leighton, Dr. Debabrata Bhattacharyya, Dr. Ghazal Hakemi, Dr. David Derbyshire, Dr. Arne Luker, Mr. Matthew Taunt, Mr. Andrew Stallard and Dr. Chris Shaw. I

thank you all and wish you family happiness and success in your careers.

Finally I would like to thank my parents for their support and encouragement and of course my beloved and caring partner Giota.

# Contents

# List of Figures

# List of Tables

# Glossary

| | |
|---|---|
| AFM | Atomic force microscopy, 58 |
| AlN | Aluminum nitride, 112 |
| BST | Barium strontium titanate, 3 |
| BTO | Barium titanate, 13 |
| CAD | Computer-aided design, 78 |
| CMOS | Complementary Metal Oxide Semiconductor, 113 |
| CMOS | Complementary metaloxidesemiconductor, 29 |
| CR | Cognitive Radio, 1 |
| CSD | Chemical solution deposition, 15 |
| DC | Direct current, 3 |
| DGS | Defected ground structures, 93 |
| DRIE | Deep Reactive Ion Etching, 82 |
| DVB-H | Digital Video Broadcasting - Handheld, 1 |
| EM | Electromagnetic, 95, 112 |
| FBAR | Film Bulk Acoustic Wave Resonator, 1 |
| FEM | Front End Module, 1 |

FeRAM Ferroelecric Random Access Memory, 10
FET Field effect transistors, 77
FWHM Full width half maximum, 61

GaAs Gallium-Arsenide, 17
GPS Global Positioning System, 1
GSG Ground-Signal-Ground, 129
GSM Global System for Mobile Communications, 1

HCl Hydrofluoric acid, 31
HF Hydrofluoric acid, 31

IC Integrated Circuits, 113
IDC Interdigitated capacitor, 21
IF Intermediate Frequency, 1

LPF Low pass filters, 94
LRRM Line-Reflect-Reflect-Match, 44

MBVD Modified Butterworth-Van Dyke, 123
MEMS Micro Electro Mechanical systems, 1
MgO Magnesium oxide, 5
MIM Metal-Insulator-Metal, 3
MOCVD Metal-organic chemical vapor deposition, 5
MOSD Metal-organic solution deposition, 3

PBG Photonic Bandgap, 93

| | |
|---|---|
| PE | Polarization versus Electric field, 9 |
| PLD | Pulsed laser deposition, 3 |
| PST | Lead strontium titanate, 3 |
| PZT | Lead Zirconium Titanate, 30 |
| Q | quality factor, 112 |
| RF | Radio Frequency, 1 |
| RTA | Rapid thermal annealing, 57 |
| SAW | Surface Acoustic Wave, 111 |
| SDR | Software Defined Radio, 1 |
| SEM | Scanning electron microscopy, 30 |
| SiGe | Silicon-Germanium, 17 |
| SiP | System-in-a-Package, 1 |
| SMR | Solidly Mounted Resonator, 114 |
| SoC | System-on-Chip, 1 |
| SOLT | Short-Open-Line-Through, 82 |
| STO | Strontium titanate, 13 |
| $T_C$ | Curie temperature, 10 |
| TCF | Temperature coefficient, 121 |
| TE | Transverse Electric, 28 |
| TL | Transmission Line, 23 |
| TM | Transverse Magnetic, 28 |
| UMTS | Universal Mobile Telecom. System, 1 |

UWB Ultra-Wideband, 1

VNA Vector Network Analyzer, 19

W-CDMA Wideband Code Division Multiple Access, 111

XRD X-Ray diffraction, 30

ZnO Zinc oxide, 7

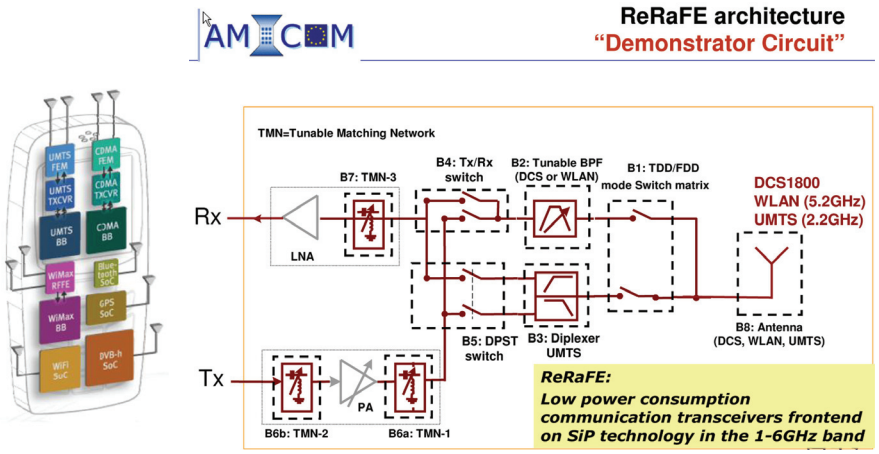
Chapter 1

# Introduction

## 1.1 Multi-standard wireless communications

Wireless communications is the fastest growing consumer electronics sector and there is an on-going demand for higher bandwidths and capacities, greater mobility and lower costs. These desired properties require electronics to achieve greater efficiencies, less power consumption and significant reductions in real-estate. This is especially true in the case of modern mobile handsets, where a multitude of wireless standards, including GSM (900/1800 MHz), UMTS (850/900/1700/1900/2100 MHz), Bluetooth (2.4 GHz), GPS (1.575 GHz and 1.228 GHz), Wi-fi (2.4/5 GHz) and DVB-H (470-862 MHz), must be supported and are presently considered essential in state-of-the-art mobile phones.

One of the most commonly used designs for wireless transceivers is the superheterodyne architecture [125], which employs frequency mixing to convert a radio frequency (RF) received signal to a fixed intermediate frequency (IF) . This baseband frequency can be more conveniently processed than the original radio carrier frequency. This is accomplished by an RF front-end module (FEM), which consists of an impedance matching network, a band-pass filter, a low-noise amplifier and a




(a) (b)

**Figure 1.1:** Different approaches to multi-standard architecture: (a) using discrete front ends, (b) using reconfigurable front end (ReRaFE).

frequency mixer. A conventional multi-band and multi-standard handset - shown in figure 1.1a - involves switching several different radios, each with its unique antennas, RF front-end module and baseband processing unit, albeit some modules can be monolithically integrated as system-on-chip (SoC) . Whereas this design principle is straightforward, this usually results in increased complexity, size and cost for the handset. Following the continuing miniaturization trend in wireless communications, research towards system-in-a-package (SiP) and multi-standard reconfigurable radio architectures including software defined radio (SDR) and cognitive radio (CR) [59], [13] has been reported. Furthermore, these architectures can utilize Micro Electro Mechanical Systems (MEMS) [130], [91] to realize reconfigurable radio front-ends [163], combined with smart antennas including varactor tunable antenna [94], switchable matrix antenna [71] and ultra-wideband (UWB) designs. Figure 1.1b, presents a reconfigurable radio front end design of a demonstrator circuit realized as part of AMICOM project 'ReRaFE' in which Cranfield

was a member and collaborator. The main goal of the project was the realization of a totally MEMS-based single radio front-end as an RF-SiP module supporting three standards: DCS1800, WLAN 5.2 GHz and UMTS W-CDMA 2.1GHz and Cranfield was to manufacture a UMTS duplexer using Film Bulk Acoustic wave Resonator (FBAR) technology. In the last quarter of 2011, the new 'Samsung Focus Flash Windows' smartphone was shown to include a RF MEMS based antenna tuning module, marking the first known use of RF MEMS in a volume commercial product. For similar RF applications, frequency agile materials have been of interest for the realization of smart and tunable devices.

## 1.2 Frequency agile materials

Reconfigurable systems such as smart transmitters and receivers, require tunable microwave components and in this connection, there has over the past decade been significant interest in thin film tunable dielectrics and more specifically ferroelectrics. The feature of interest in these materials is the large variation in dielectric constant with applied electric field - seen in figure 1.2b, which makes them ideal candidates for passive components with potentially high tunability and low loss at microwave frequencies [6]. The permittivity change of these materials when a direct current (DC) field is applied, is due to the saturation of dielectric polarization [101] and the permittivity decreases with an increased electric field. Parallel plate ferroelectric tunable capacitors in a Metal-Insulator-Metal (MIM) topology - shown in figure 1.2a, have low fringing fields, a high capacitance density and a low tuning voltage [162]. Furthermore, owing to their high permittivity, they are ideal for miniaturization purposes.

Thin-film ferroelectrics like barium strontium titanate (BST) [170] and lead strontium titanate (PST) [36] have been studied for the realization of electric field

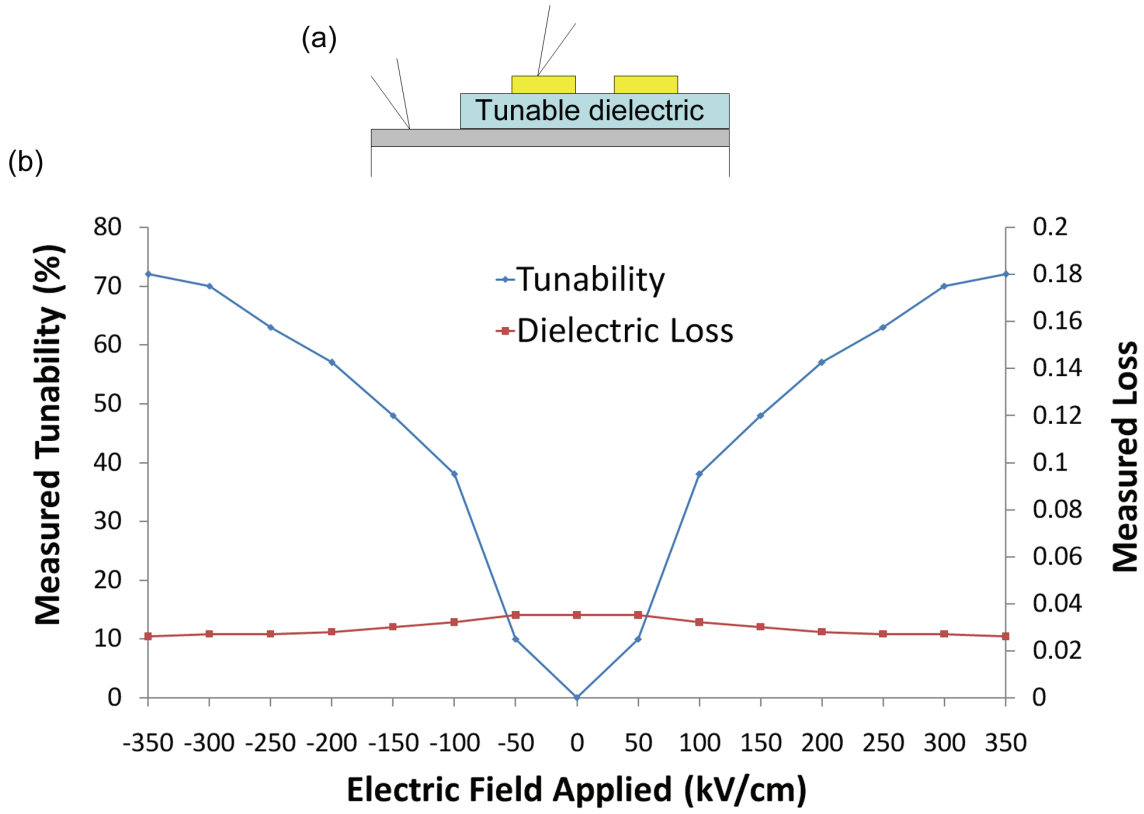



**Figure 1.2:** (a) Cross-section schematic of ferroelectric varactor and (b) example of dielectric constant tunability and dielectric loss with applied electric field.

tunable ferroelectric varactors and dielectric constant tunabilities up to 92.7% using RF sputtering [121] and dielectric losses as low as $7\times10^{-3}$ using metal-organic solution deposition (MOSD) [21] and pulsed laser deposition (PLD) [170] have been reported for BST. Tunable microwave devices and systems based on ferroelectric varactors have been realized, including tunable phase shifters [3], tunable filters [106], [164], switches [151] and tunable impedance matching networks [142]. Although the performance of some of these devices are away from practical microwave requirements, there is scope for device performance enhancement by

improving the tunable dielectric properties.

## 1.3 Motivation and research objectives

The motivation for this thesis arises from the appeal of integrating sol-gel ferroelectrics for device manufacture, as it is low cost compared to other material deposition techniques and can be deposited over large areas on well-known substrates, such as Si, glass, magnesium oxide (MgO) and sapphire. The PST system is being researched as a promising candidate for thin-film tunable microwave applications, since Somiya [147] reported dielectric loss values of less than 0.1% in PST ceramics. Although, thin-film PST deposited by RF sputtering [17], PLD [84] and MOCVD [27] have been reported , fewer studies have been targeted to sol-gel PST on Si substrates [56]. Furthermore, little effort has been targeted in directly measuring the microwave performance of PST films [27], in fabricating PST sol-gel ferroelectric tunable RF devices and in modeling the electrostrictive and acoustic behavior of PST thin films. The following research objectives reflect the above considerations.

- Development and characterization of PST thin films, suitable for RF tunable devices
  - Design, electrical modeling and fabrication of a MIM PST sol-gel ferroelectric tunable varactor as the fundamental block for tunable microwave devices.
  - Development of software, measurement techniques and CPW MIM test structures to be used in accurate high frequency dielectric properties extraction techniques.
  - Acoustic wave modeling for PST ferroelectric varactors.

- Identify critical links between varactor design, fabrication process and electrical performance (e.g. influence of bottom electrode resistance on the quality factor of the varactor). Investigate and achieve optimization of the electrical performance of the ferroelectric varactor.

- Design, model and fabricate novel RF tunable devices integrating thin film PST ferroelectric varactors (e.g. high frequency resonators and filters)
  - Develop designs and fabrication processes for integration of ferroelectric varactors in original structures (e.g. free-standing PST MIM stack, integration with bulk micromachined inductors and integration in CPW defected ground structures).

- Develop a fabrication process suitable for integration of ferroelectric thin films with conventional bulk acoustic wave technology. Design, model and fabricate a tunable FBAR with a ferroelectric varactor as the tuning element.

## 1.4 Contribution to knowledge

An original contribution to knowledge has been achieved through the analysis and development of this research. Experimental evidence is presented in sections 2 to 6 of this thesis and parts of the work have been published or are pending publication.

- A two port automatic extraction technique using MATLAB and de-embedding to allow accurate dielectric properties extraction of PST thin films doped with Mn, has been developed and presented. Presented as poster presentation in ISIF 2008 - published in Journal of Applied Physics [36]. (section 3.4)

- A variety of Au bottom electrode structures are studied for reduction of resistive losses in ferroelectric varactors. The significance of the underlying barrier and adhesion layers on the electrode quality is investigated. Crack-free thin film PST is deposited on the most suitable Au electrode configuration to obtain ferroelectric tunable varactors. The performance of the varactors is shown to improve compared to the Pt bottom electrode varactors. Presented as an oral presentation in ISIF 2011 - submitted in Integrated Ferroelectrics Journal. (chapter 4)

- The design, simulation and fabrication of C-band, resonant switches on silicon, integrating electroplated, micromachined inductors and sol-gel PST tunable varactors, are presented. Presented as an oral presentation in International Symposium on RF MEMS and RF Microsystems, MEMSWAVE 2009 - to be resubmitted in IEEE Ultrasonics Journal. (section 5.2)

- The design and fabrication of monolithic tunable bandstop resonators and filters, based on sol-gel PST ferroelectric varactors embedded in a CPW defected ground structure are presented. Presented as an oral presentation in European Microwave Conference 2008 (EuMC 2008) - published in EuMC 2008 Proceedings [20].(section 5.3)

- Acoustic modeling has been used to simulated acoustic resonances in PST MIM varactors and the design and fabrication of a free-standing PST ferroelectric thin-film bulk acoustic wave resonator is presented. Presented as an oral presentation in International Symposium on RF MEMS and RF Microsystems, MEMSWAVE 2009. (section 5.4)

- The design, modeling and fabrication of a tunable FBAR made by monolithic integration of a conventional zinc oxide (ZnO) GSM based FBAR with a PST ferroelectric varactor is presented. Pending Submission.(section 6.3)

## 1.5 Thesis Overview

The thesis overview is as follow:

**Chapter 2** discusses tunable dielectric materials and techniques for electrical characterization of ferroelectric thin films.

**Chapter 3** presents the development of PST thin films and the design, electrical and acoustic modeling and fabrication of a PST ferroelectric varactor. A two port automatic extraction technique using MATLAB and de-embedding has been developed and presented.

**Chapter 4** proposes a novel bottom electrode stack, which improves the RF performance of the tunable varactor lowering the overall metalization resistance.

**Chapter 5** presents the design, modeling and fabrication of tunable microwave devices and systems based on tunable sol-gel ferroelectric varactors. A ferroelectric resonant switch, a bandstop filter and an electrostrictive FBAR are presented.

**Chapter 6** presents the design, modeling and fabrication of a ferroelectric varactor tunable ZnO bulk acoustic wave resonator. Tuning of the FBAR resonance by applying an electric field across the tunable ferroelectric varactor, has been demonstrated..

**Chapter 7** concludes the thesis and outlines the directions for future work.

Chapter 2

# Tunable dielectrics

## 2.1 Introduction

This chapter highlights the essential background information on tunable dielectric materials, including ferroelectrics. Several reviews and books deal with the tunable material background more in depth [6], [148], [160], [88]. A short comparison of tunable varactor technologies is attempted. Furthermore, electrical characterization techniques for material properties extractions, such as dielectric constant and loss, from low (kHz) to high (GHz) frequencies, are presented and discussed. Using some of these methods and for the interest of this thesis, MATLAB software has been developed in order to automatically extract the tunable dielectric properties from S-parameter measurements of test structures, such as CPWs on PST thin films and PST MIM capacitors. These programs can be found in Appendix A-1 - A-3 and are fully documented.

## 2.2 Tunable dielectrics background

Whereas all materials can exhibit a small change in dielectric constant with the application of an external electric field, in certain high-permittivity materials, including ferroelectrics, the effect is much more pronounced [148]. The permittivity change of these materials when a DC field is applied, is due to the saturation of dielectric polarization [101] and the permittivity decreases with the application of an external electric field. On the contrary, in normal dielectric materials, the electrical polarization is linearly dependent on the applied electric field and the resultant permittivity, which is equal to the slope of the polarization versus electric field (PE) curve, is a fixed quantity.

A crystal is said to be ferroelectric when it has two or more orientational states in the absence of an electric field and can be shifted from one to another of these states by an electric field [88]. Most ferroelectric crystals undergo a phase transition from a high temperature, high symmetry paraelectric phase to a lower symmetry ferroelectric one. The temperature associated with this phase change is called the Curie temperature ($T_C$) . The behavior of a ferroelectric material below and above the Curie temperature is shown on figure 2.1.

In the ferroelectric phase below $T_C$, the material exhibits hysteresis in the PE response. Ferroelectric random-access memory (FeRAM) [146] is an application of this memory effect. Above $T_C$ the material is paraelectric with a large dielectric constant, field-dependent nonlinearity and is almost non-hysteretic. Even in the paraelectric phase, the material is still colloquially called as ferroelectric. In both phases the electrical properties are strongly temperature-dependent. In order to meet the high specifications of the wireless communications market, electronically tunable materials are desired to be non-hysteretic, highly tunable and low loss.

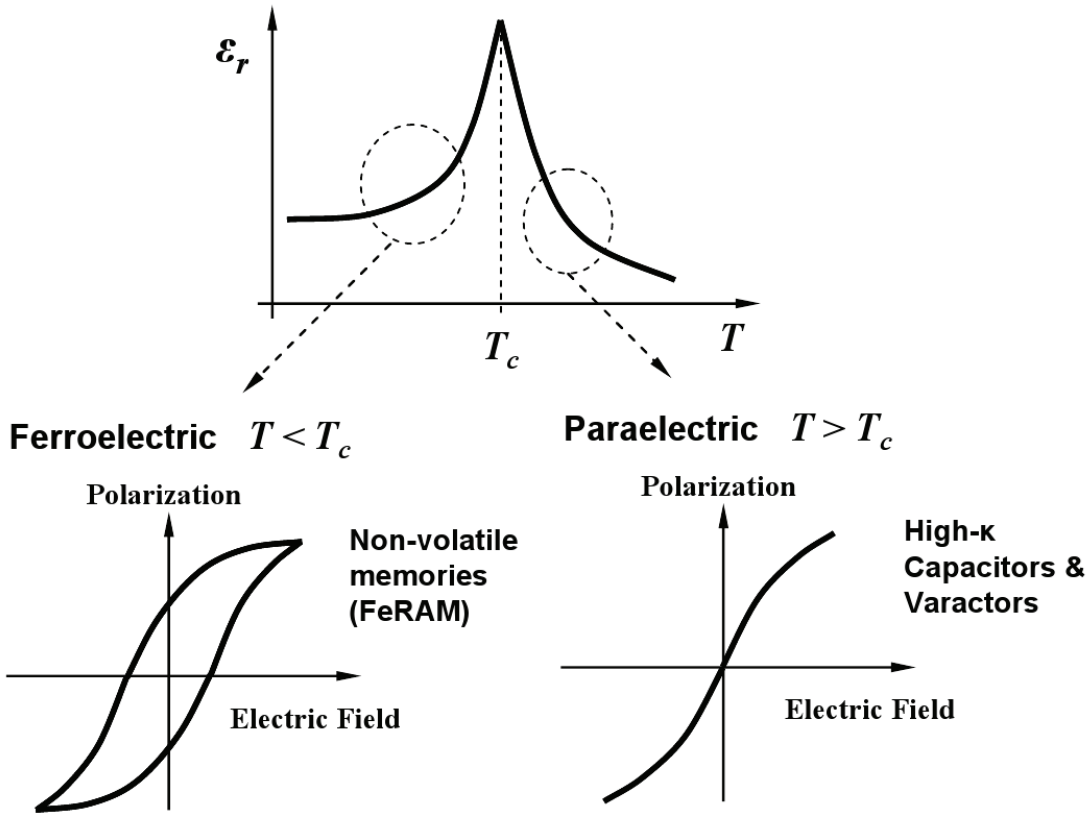



**Figure 2.1:** Behavior of ferroelectric materials around the Curie temperature [148].

### 2.2.1 Tunability

The tunability (n) is defined as the ratio of the dielectric permittivity at zero electric field bias to the permittivity under the application of an electric field, E. The relative tunability ($n_r$) is defined as the relative change of the permittivity between zero and electric field E with respect to the zero electric field value [6]. Both are given in equation 2.1 :

$$n = \frac{\epsilon^{'}(0)}{\epsilon^{'}(E)}, n_{\tau} = \frac{\epsilon^{'}(0) - \epsilon^{'}(E)}{\epsilon^{'}(0)} \tag{2.1}$$

, where $\epsilon^{'}$ is the real part of the permittivity.

Starting from a maximum capacitance ($C_{max}$) at zero bias, the capacitance of a ferroelectric varactor monotonically decreases and reaches a reduced capacitance value ($C_V$), when a voltage (V) is applied across it. Recently, based on a power-series expansion for the PE relation and the Landau-Devonshire-Ginzberg (LDG) model [88], a capacitance-voltage relation has been derived [16], which can be useful for RF design. Given that one knows the voltage ($V_2$) at which the capacitance reduces to half of the starting capacitance - a measurable quantity -, equation 2.2 can predict the voltage at which a certain capacitance value will be reached.

$$V = \frac{1}{4} V_2 \left( \frac{C_{max}}{C_V} + 2 \right) \sqrt{\frac{C_{max}}{C_V} - 1} \tag{2.2}$$

The figure of merit (K) is defined as the ratio of the relative tunability (n) and the dielectric loss tangent ($\tan\delta$). It is often used for comparison of the quality of ferroelectric thin films.

### 2.2.2 Ferroelectric perovskite materials

A very important group of ferroelectrics (and tunable dielectrics) is known as the perovskites from the mineral perovskite $CaTiO_3$ [88]. The perfect perovskite structure is an extremely simple one with general formula $ABO_3$, where A is a monovalent or divalent metal and B is a tetra- or pentavalent one. Shown in figure 2.2, it is cubic, with the A atoms at the cube corners, B atoms at the body centres and the oxygens at the face centres.

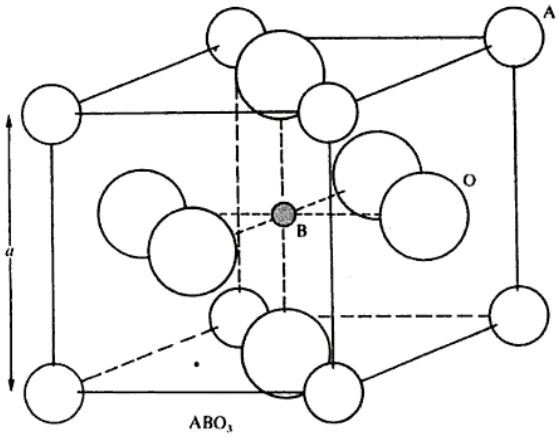



**Figure 2.2:** The cubic $ABO_3$ perovskite structure [88].

Ionic substitutions of A or B atoms can alter the material properties. BST is the most popular ferroelectric thin films which is currently studied for tunable RF and microwave circuits.

#### 2.2.2.1 Barium Strontium Titanate (BST)

Barium strontium titanate is the solid solution of barium titanate (BTO) and strontium titanate (STO) . In BST, the A site $Ba^{2+}$ ion in barium titanate, $BaTiO_3$ is substituted by the $Sr^{2+}$ ion. Since the Curie temperature of the material depends on the composition, the material properties can be altered and large dielectric constants and tunability have been reported close the Curie point [6]. Figure 2.3a shows the almost linear decrease of the Curie temperature of different BST compositions with increasing amounts of strontium. The Curie point is approximately at room temperature in the $Ba_{0.7}Sr_{0.3}TiO_3$ composition. The cubic perovskite structure of BST can be seen in more detail in figure 2.3b. In this structure, the material has a large permittivity. This is due to the induced

polarization, when an electric field is applied, distorting and displacing the Ti ion in the structure. Figure 2.3c presents the dielectric constant tunability of bulk ceramic $Ba_{0.7}Sr_{0.3}TiO_3$ [93] under a range of electric fields.

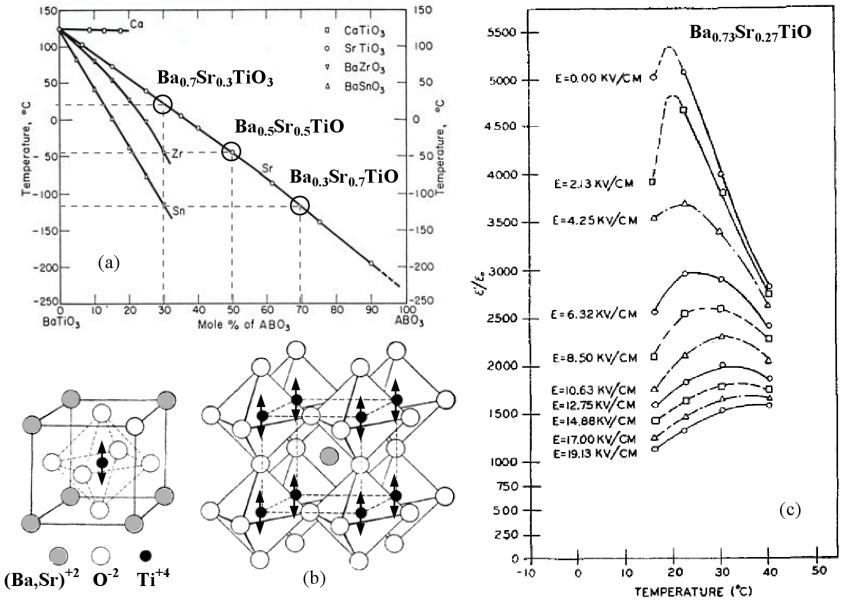



**Figure 2.3:** (a) Variation in Curie temperature of bulk BTO with various additives [58], (b) Structure of BST showing oxygen octahedra surrounding the titanium ion [169], (c) Field dependence near the Curie temperature for a high-barium BST ceramic [93].

The application of thin film ferroelectrics, including BST in thin film tunable MIM varactors has been of interest for tunable systems [3], [106], [164], [151], [142], as quite large tunabilities can be achieved with relatively low voltages applied. This is possible as large electric fileds can be applied in the very thin thicknesses (usually in the range of 100-500 nm) of tunable materials. However, thin-film tunable dielectrics can exhibit different dielectric properties compared to bulk ceramics [148], including lower dielectric constants, different temperature dependence and

no obvious ferroelectric-paraelectric transition. This phenomenon is attributed to factors [6] such as substrate-induced strain due to mismatch with the film, charged defects and structural imperfections causing local strains, a 'dead' layer near the interface between the substrate and the electrodes and stoichiometry. For BST thin films, dielectric constant tunabilities up to 92.7% using RF sputtering [121] and dielectric losses as low as $7\times10^{-3}$ using MOSD [21] and PLD [170] have been reported.

#### 2.2.2.2 Lead Strontium Titanate (PST)

Although certainly the most well established, BST is not the only material which has been investigated for tunable microwave devices based on thin films. In fact, the $Pb_{1-x}Sr_xTiO_3$ (PST) system has also been researched as a promising candidate for thin-film tunable microwave applications, since Somiya [147] reported dielectric loss values of less than 0.1% in PST ceramics. The PST system is remarkably similar to the BST system, in that the Curie temperature for the cubic-to-tetragonal transition can be adjusted over an exceedingly large temperature range by adjusting the Pb-to-Sr content ratio.

Figure 2.4a shows the relative dielectric permittivity of a PST composition with Pb:Sr ratio of 4:6 against temperature. The Curie temperature of this PST composition is slightly below room temperature [96], around $17^oC$ [56]. Compositions with higher Pb:Sr content start exhibiting ferroelectric and hysteretic behavior since the Curie temperature is shifted to higher temperatures. Figure 2.4b shows hysteresis loops of PST thin films with different Pb:Sr content, ranging from 4:6 to 8:2 [17]. Among other research efforts, PST thin-films deposited by RF sputtering [17], PLD [84], MOCVD [27] and chemical solution deposition (CSD) [56] have been reported.

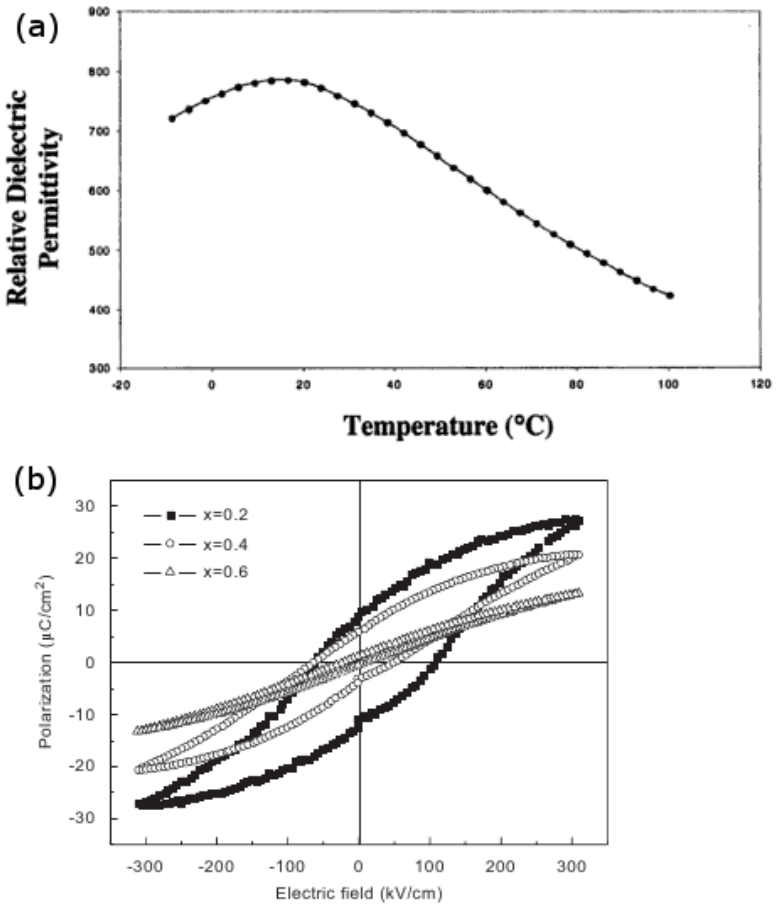



**Figure 2.4:** (a) Relative permittivity as a function of temperature of a thin-film $Pb_{0.4}Sr_{0.6}TiO_3$ [96] and (b) Hysteresis loops of $Pb_{1-x}Sr_xTiO_3$ films with variable Sr content, for x=0.2, 0.4 and 0.6 [17].

### 2.2.3 Comparison of varactor technologies

Ferroelectric thin film based varactors can present many advantages such as low dielectric loss for high quality films, high tunability with low operation tuning

voltage for MIM varactors, small footprint due to high dielectric constants, high power handling capability and low-cost fabrication processes. However, other varactor technologies such as semiconductor varactor diodes and MEMS varactors may also offer distinct advantages.

A semiconductor varactor diode is a p-n junction diode made of Gallium-Arsenide (GaAs) , Silicon (Si) or Silicon-Germanium (SiGe) . The depletion area in the p-n junction forms a capacitor, whose capacitance can be varied by changing the reverse bias voltage across the diode. The advantages of varactor diodes include large tunability (>10:1), small footprint, fast tuning speed and low operational voltage [185]. However, semiconductor varactor diodes are known to become lossy at frequencies higher than 5 GHz. Furthermore, they can suffer from poor power handling, as their reverse bias operation does not allow for large RF voltage swings. On the contrary, ferroelectric varactors, have no forward conduction region, and hence can sustain large RF voltage swings [148].

The basic structure of RF MEMS varactors [90], consists of two metal traces (signal and ground) separated vertically by an air gap, forming a parallel-plate capacitor. With the application of an electric field between the upper bridge and the lower signal trace, the resultant electrostatic force pulls down the bridge arm and the capacitance increases due to the decreased gap. Whereas MEMS varactors are superior in the Q factor and linearity especially at high frequencies, they can face limited tuning due to the mechanical rigidness of the moving parts, stiction and dielectric charging effects. Therefore challenges of reliability and expensive packaging can be detrimental in their application.

A comparison of ferroelectric varactor technologies with the other two aforementioned varactor technologies is shown in Table 2.1.

Figure 2.5 shows reported quality factors for ferroelectric (BST) varactors and

**Table 2.1:** Comparison of the properties of semiconductor GaAs, MEMS and ferroelectric BST thin film varactors [6].

| | GaAs | MEMS | Ferroelectric (BST) |
|---|---|---|---|
| Tunability(n) | ∼2-6:1[a] | ∼1.5-3:1[b] | ∼2-4:1 |
| Quality factor (Q) | ∼20-50 at 10 GHz[a] | Very high | ∼20-100 at 10 GHz |
| Operation voltage | <15V[a] | <50V[b] | <15V[a] (MIM) |
| Tuning speed (s) | $\sim 10^{-6}$s | $>10^{-5}$ | $\sim 10^{-9}$s[c] |
| Reliability | Good[a] | Poor | Good |
| Cost | High | High | Low |
| Power handling | Poor | Good | Good[c] |

[a] Refer to http://www.mbelectronique.fr/

[b] Refer to Peroulis D et al 2003 MTT-S Int. Microwave Symp.Digest vol 2, pp 1117.

[c] Refer to Kozyrev et al 1998 Integr. Ferroelectr. 22 329.

other semiconductor varactor technologies over a wide frequency range. At 45 GHz the quality factor of the ferroelectric varactors are comparable with the GaAs dual Schottky diode [170]. Since the the measured loss tangent of the ferroelectric varactors is about one order of magnitude more than the STO single crystal [140], there is still scope for improving further the performance of the devices.

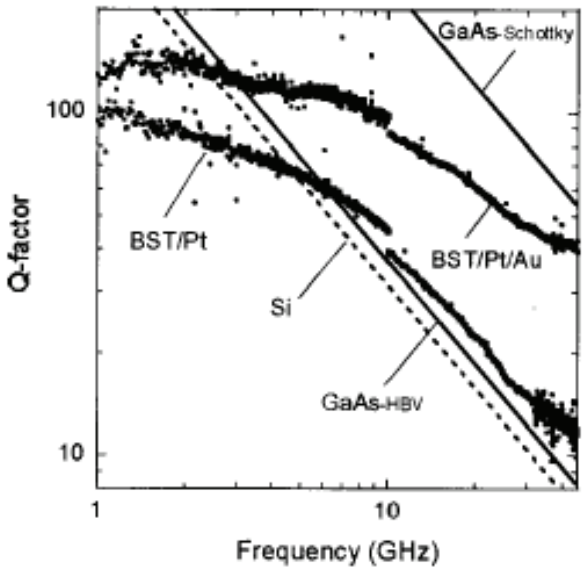



**Figure 2.5:** Frequency dependencies of the Q factor of BST/Pt/Au and BST/Pt varactors at zero bias [170]. Shown are also Q factors of: Si abrupt junction varactor (Metelics, MSV34,060-C12, Q=6500@50 MHz, V=-4V), GaAs HBV (Darmstadt University of Technology, $f_{cutoff}$=370GHz), and GaAs dual Schottky diode (United Monolithic Semiconductors, DBES105a, $f_{cutoff}$=2.4THz).

## 2.3 Electrical characterization techniques

Tagantchev [160] addresses the methods and techniques that enable the measurements of the complex dielectric permittivity and tunability of thin-film ferroelectric materials. All measurement techniques require firstly the monitoring of the electrical characteristics of a device containing the ferroelectric and secondly the evaluation of the dielectric permittivity and loss tangent of the material from the obtained data. According to Tagantchev, all measurement methods can be divided into three groups :

- **Direct methods**, where the capacitance and loss tangent of a capacitor containing the ferroelectric material is measured directly using an impedance analyzer and then fitted to an equivalent lumped element network. For higher frequencies, the scattering matrix [22] of the ferroelectric capacitor is measured by a vector network analyzer (VNA) , converted to impedance and then again fitted an equivalent lumped element network.

- **Waveguide methods**, in which the scattering matrix of a ferroelectric containing waveguide is measured using a network analyzer. The electromagnetic propagation constant ($\gamma$) is calculated and used in the extraction of the dielectric properties.

- **Resonance methods**, where the characteristics of a resonator which contains the investigated material are measured.

The precision and limits of the above measurement methods strongly depend on the frequency range, the ferroelectric material and the test structure used. For frequencies in which the wavelength of the electromagnetic wave is significantly larger than the dimensions of the capacitor, the tunable capacitor can be regarded as a lumped element network. Hence, the direct methods can be used and the capacitance and loss tangent can be measured directly by a standard impedance analyzer or by extracting the impedance of a VNA. At higher frequencies, where the capacitor cannot be considered as a lumped element and the distributed effect of the electrodes of the capacitor becomes relevant or the impedance of the capacitor becomes small compared to the resolution of the impedance analyzer, waveguide measurements are appropriate. The techniques used in the current literature are listed below.

### 2.3.1 Direct Methods

In the direct method, the dielectric permittivity and loss tangent of the thin-film ferroelectric are evaluated from direct impedance measurements made on a capacitor which incorporates the material. Because this method is based on fitting the measured impedance on a lumped element equivalent circuit, the physical length of the capacitor must be significantly smaller than the length of the electromagnetic wave in the frequency of measurement, for the technique to be valid. The full equivalent lumped element network for a ferroelectric varactor is shown on figure 2.6, where R and L, are the resistance and inductance of the electrodes and C and G are the capacitance and conductance of the ferroelectric thin film, respectively.

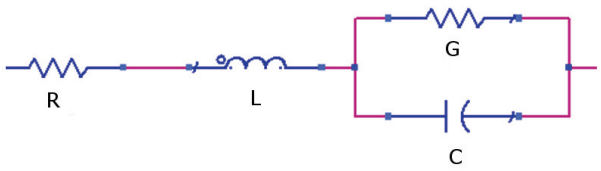



**Figure 2.6:** The full equivalent lumped element network for a ferroelectric capacitor.

If the frequency of interest is from DC up to 10s of MHz, the electrodes of the capacitor (R, L) are usually ignored and simple impedance analyzers (Wayne Kerr Precision Component Analyzer 6425B) can automatically extract the capacitance (C) and conductance (G) of the material. Depending on whether the capacitor structure is vertical - MIM structure see figure 2.7 - or planar - interdigitated structure see figure 2.8, the dielectric constant and loss can be then calculated from

the capacitance and conductance extracted. More specifically the MIM formulas 2.3, 2.4 and the interdigitated capacitor (IDC) analytical formula [31] 2.5 are used.

$$\epsilon = \frac{C \times d}{\epsilon_0 \times A} \tag{2.3}$$

$$tan\delta = \frac{G}{\omega \times C} \tag{2.4}$$

$$\epsilon = e_S + \left\{ \frac{C_f - [1 + \epsilon_S]}{K\left[1 - exp\left(\frac{-4.6d}{L}\right)\right]} \right\} \tag{2.5}$$

, where d is the thin-film thickness, A is the effective area of the capacitor, $\epsilon_0$ is the vacuum permittivity, $\omega$ is the angular frequency, $\epsilon_S$ is the substrate dielectric permittivity, K is a constant which has units of pF, $C_f$ is the measured capacitance per unit finger length per electrode section of width L.

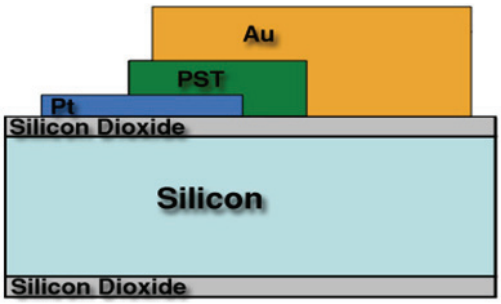



**Figure 2.7:** Cross-section schematic of a MIM parallel plate capacitor. The effective area of the capacitor is formed by the overlap of the top and bottom electrode.

For higher frequencies, S-parameter measurements must be made with a VNA. These are then converted to impedance and fitted to the full equivalent network, including the electrodes, as their impedance contribution becomes more

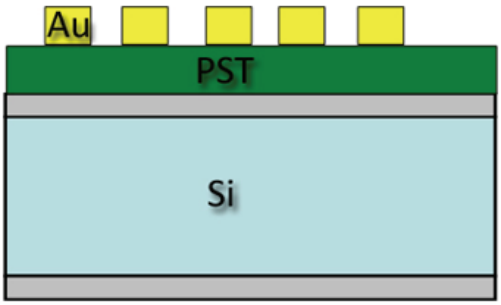



**Figure 2.8:** Cross-section schematic of an interdigitated capacitor.

important. For the MIM structure, 1-port [23] and 2-port [161] VNA measurements for characterization have been reported and the S-parameters are then converted to impedance and fitted into the lumped network equivalent [186]. The impedance extraction from S-parameters, is usually done by means of converting S-parameters to Y-parameters [98],[124], so that the $Y_{21}$ parameter can be directly linked to the series admittance of the lumped MIM capacitor equivalent. A detailed analysis and an optimized version of these techniques including pad parasitics and CPW de-embedding has been developed and is presented as part of this thesis in chapter 3. For high frequency IDC structures, conformal mapping techniques [108] are used to extract the dielectric properties of the thin-film in the CPW-IDC case [30], [69], [181].

### 2.3.2 Waveguide methods

The filled waveguide technique is one of the first methods [155] developed for characterization of dielectric materials at microwave frequencies. It involves the calculation of the characteristic impedance and propagation constant of the electromagnetic wave traveling through a waveguide filled with the dielectric under test. The technique is readily used for the characterization of materials with rela-

tively low dielectric permittivity, because of the problem of impedance matching to the measurement equipment. For materials having including very high dielectric constants, including thin-film ferroelectrics, the transmission line (TL) method is used.

The transmission line method is a special case of the waveguide method. It involves the measurement of the electromagnetic propagation constant and characteristic impedance of a transmission line, which is patterned onto the ferroelectric film as seen on figure 2.9. After the frequency dependent propagation constant and characteristic impedance are extracted from VNA measurements, the dielectric properties of the thin-film are evaluated either through conformal mapping techniques or calibration comparison techniques.

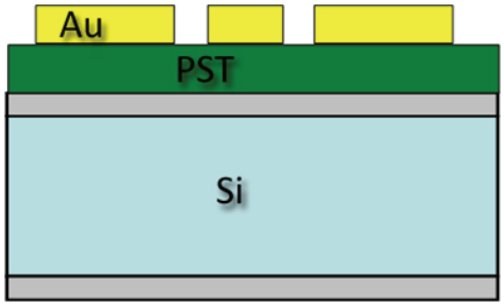



**Figure 2.9:** Cross-section schematic of CPW patterned on ferroelectric (PST) thin film.

There are several assumptions made in using the TL method. Electromagnetic propagation is assumed to occur in a quasi-TEM mode. The CPW conductors are assumed to have perfect conductivity and the dielectric substrates are assumed to have perfect relative permittivity. The structure is considered to be lossless. Also, the dielectric substrate materials are considered to be isotropic. Finally

the conductor thickness is assumed to have zero thickness and magnetic walls are present along all dielectric boundaries, including the CPW signal-to-ground gaps.

The most well-known and used TL methods are the partial capacitance technique and the reference technique. These are described in more detail below.

#### 2.3.2.1 Partial Capacitance technique

In the partial capacitance technique, initially, the electromagnetic propagation constant ($\gamma$) is extracted from VNA measurements. This can be achieved using one of the following methods : the probe-tip method, the ratio method, the calibrated ratio method or the multiline method [26]. The multi-line method [97], [25] and recently updated statistically updated multiline algorithm [175], [176], give more precise evaluations of the propagation constant according to Williams [174]. Then the capacitance per unit length is evaluated using the Telegrapher's equation [73], assuming quasi-TEM electromagnetic propagation. Finally, using conformal-mapping techniques [108] and the Schwarz - Christoffel transformation, the partial capacitance of each layer in the absence of the others is calculated [42].

Using the TL partial capacitance technique, a MATLAB program (Appendix A-1) was developed to extract the frequency dependent propagation constant ($\gamma$), characteristic impedance ($Z_{0l}$) and finally the capacitance of a Au CPW patterned on top of PST and Alumina. The partial capacitance of each layer was extracted and can be seen in figure 2.10. The dielectric permittivity and loss of the film was then calculated from these capacitances using conformal mapping techniques. Figure 2.11 shows the dielectric permittivity calculated from VNA measurements of a 6 mm Au CPW on PST/Alumina with a CPW signal width and gap of 0.1 mm and 0.08 mm respectively. The low dielectric constant of PST is attributed to the reduced crystallization as compared to when the PST is grown on Pt. In

the same way, a partial loss [39], [41] and partial conductance [40] technique can be used to evaluate the dielectric loss of the thin-film ferroelectric.

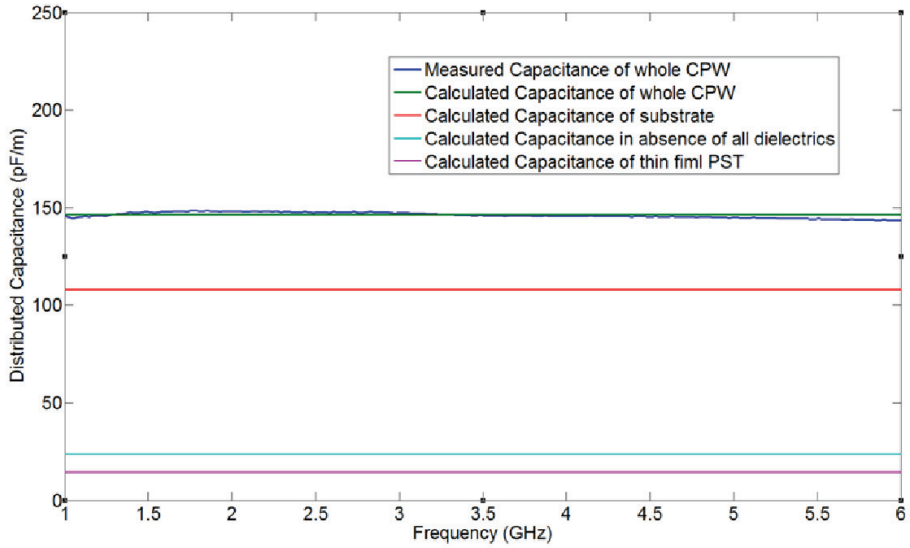



**Figure 2.10:** Partial Capacitances calculated from VNA measurements on a 6 mm CPW on PST/Alumina.

In line with literature, several mathematical approximations were made in the developed MATLAB software. These are mentioned as comments in the software code (Appendix A-1). The TL partial capacitance technique has extended literature, including approximations on the conformal mapping formulas used [50] (elliptic integral estimation), applications of the technique in special cases like the finite ground CPW [168], the conductor backed and shielded CPW [166], [61], [167] and the CPW on very thin-films [42], [184]. Conformal mapping techniques have been measured against finite element (FEM) simulations [14] and slight discrepancies at very high frequency are reported [165]. Although increasing complexity,

Heinrich [48] takes account of the effects of non-ideal conductors, as well as finite conductor thickness in his conformal mapping technique.

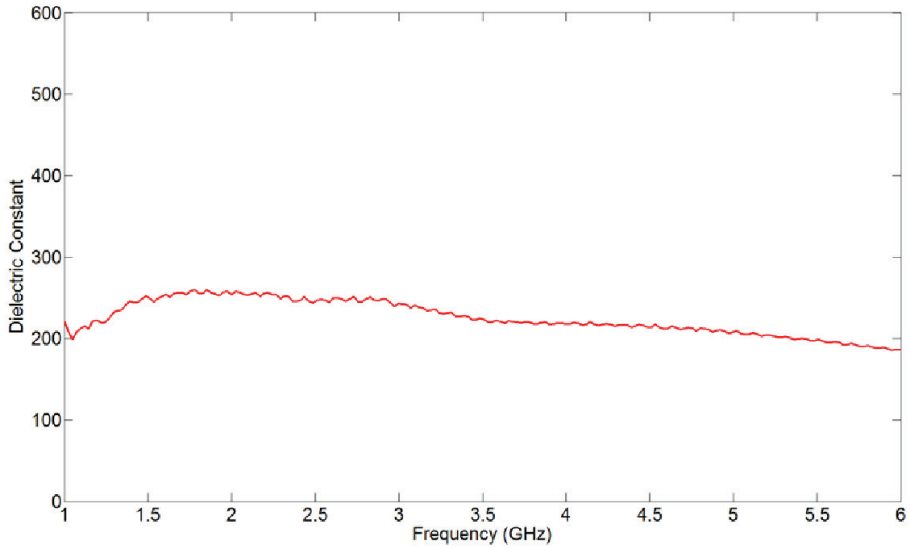



**Figure 2.11:** Dielectric constant of PST grown on Alumina extracted using the TL partial capacitance method.

#### 2.3.2.2 Reference technique

The reference TL technique [152], [57], [153], [28] differs slightly from the partial capacitance technique, because two measurements of CPWs - one on the ferroelectric thin-film and one with the CPW directly on the substrate - are used. Other than that, the same conformal mapping techniques are implemented to evaluate the dielectric permittivity and loss tangent from the extracted capacitance. Assuming that the CPW conductors on the two samples are identical, one can find the capacitance and conductance of the thin-film sample by simply dividing the

propagation constants of the two samples. These are then linked to the dielectric properties using conformal mapping.

### 2.3.3 Resonance methods

Although not for thin-film characterization, the Hakki-Coleman method [47] and the techniques based on the excitation of the transverse magnetic field (TM) resonance modes [158] are the most common methods for bulk material characterization. The measuring structure is a resonator made up of a right circular cylindrical dielectric rod placed between two parallel conducting plates. For measurement of permittivity two or more resonant transverse electric (TE) mode frequencies are determined. The dielectric or magnetic properties are computed from the resonance frequencies, structure dimensions, and unloaded Q.

For thin-film characterization, resonance perturbation techniques like microwave scanning microscopy [180] and transmission line resonator methods [29] can be used. These were not pursued in this thesis due to their increased complexity compared with the partial capacitance TL technique.

Chapter 3

# Ferroelectric MIM varactor

## 3.1 Introduction

This chapter outlines the design, fabrication and testing of PST ferroelectric varactor structures, which will be used as the tuning elements in high frequency devices in following chapters. Different PST compositions were prepared, deposited by sol-gel deposition and electrically characterized to investigate their possible use in RF varactors and devices. For the varactor analysis, doping of PST with Mn, has been investigated and the dielectric properties in the frequency range 1 - 25 GHz were extracted from RF measurements on fabricated parallel-plate capacitors. An extraction method, that takes parasitic impedances fully into account is described in some detail. Peaks in dielectric loss due to electrostriction were observed and their possible usefulness in PST thin films has been investigated.

## 3.2 PST thin films

### 3.2.1 Sol-gel PST thin film preparation and deposition

Chemical solution deposition (CSD) is a Complementary metaloxidesemiconductor (CMOS) technology compatible deposition technique, which has been widely investigated for thin film growth for nearly two decades and much of these activities have been aimed at ferroelectric thin films for electronic applications. The main advantages of CSD are: (a) the composition of compounds is easy to control by altering the stoichiometric ratio of the original material to ensure high homogeneity, (b) relatively low processing temperatures are required and (c) cost effectiveness [8]. It also allows quick experiments of a large number of film compositions in a cost-effective manner. The general principle involved in fabrication of ferroelectric thin films by CSD involves four basic steps: (1) synthesis of a precursor solution, (2) deposition by spin-coating, where the solvent starts drying, (3) low-temperature heat treatment for solvent evaporation, pyrolysis of organic species (usually 300-400$^o$C), and the formation of an amorphous film, and (4) high temperature annealing for densification and crystallization of the thin film ferroelectric coating into the desired oxide phase (usually 600-1100$^o$C).

Two PST ferroelectric compositions, $Pb_{0.4}Sr_{0.6}TiO_3$ and $Pb_{0.25}Sr_{0.75}TiO_3$, were prepared, characterized using X-Ray diffraction (XRD) and scanning electron microscopy (SEM) and electrically tested using low frequency MIM structures. This was done for initial testing of the dielectric properties before fabricating tunable MIM capacitors for use in microwave systems. It is desirable for the ferroelectric material to be highly tunable, have a low dielectric loss, a high dielectric strength and present no obvious hysteresis. The two specific PST compositions were chosen as $Pb_{1-x}Sr_xTiO_3$ with a Sr content higher than x=0.6 is known to be in the

paraelectric regime in room temperature [96], and hence expected not to exhibit hysteresis. To compare the hysteresis of both materials, a lead zirconium titanate (PZT) $Pb_{0.3}Zr_{0.7}TiO_3$ ferroelectric composition, known to be in the ferroelectric phase at room temperature, was also investigated. The procedures for the preparation of the precursor solution of different PST compositions can be found in Appendices B-1 and B-2.

Six layers of the 3 materials (∼220nm for PST 25/75 and ∼420nm for PST 40/60 and PZT 30/70) were deposited by sol-gel deposition on Pt(100nm)/Ti/$SiO_2$/Si substrates. For the PST thin films, each layer was baked 5 minutes at 350$^o$C and annealed for 10 minutes at 700$^o$C. For the PZT thin films, each layer was baked 30 seconds at 200$^o$C and annealed for 5 minutes at 530$^o$C. These films were characterized by XRD and SEM and shown in figure 3.1 to be well crystallized. Figure 3.2 shows a dense uniform grain structure for the $Pb_{0.25}Sr_{0.75}TiO_3$ thin film.

### 3.2.2 PST thin film low frequency electrical characterization

The ferroelectric thin films were wet-etched using a mix of hydrofluoric (HF) and hydrochloric (HCl) acids and Cr/Au circular dots were evaporated on top to form low frequency MIM varactors for electric measurements with a Wayne Kerr 6425 impedance analyzer. Initially, dielectric constant and loss - shown in figure 3.3 - were extracted for frequencies from 20 Hz to 300 KHz. Then, capacitance-voltage measurements - seen in shown in figure 3.4 - allowed for tunability and approximate dielectric strength for each material composition.

The extracted dielectric properties suggest that both $Pb_{0.4}Sr_{0.6}TiO_3$ and $Pb_{0.25}Sr_{0.75}TiO_3$ thin films can be of use for the fabrication of high frequency agile varactors. $Pb_{0.4}Sr_{0.6}TiO_3$ displays a small hysteresis but also 60% tunability under a relative

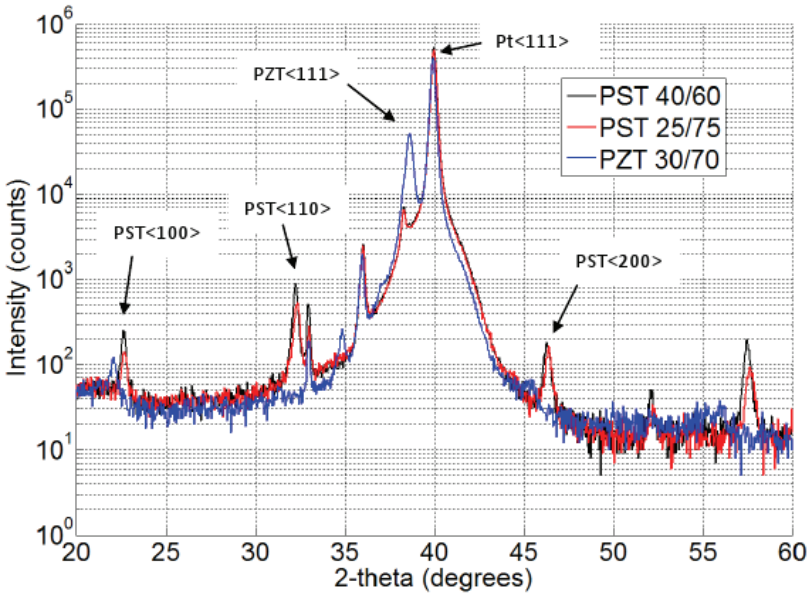



**Figure 3.1:** XRD of $Pb_{0.3}Zr_{0.7}TiO_3$, $Pb_{0.4}Sr_{0.6}TiO_3$ and $Pb_{0.25}Sr_{0.75}TiO_3$ thin films.

small electric field of ∼350kV/cm and a dielectric constant of ∼480. $Pb_{0.25}Sr_{0.75}TiO_3$ on the other hand, shows almost no hysteresis, has a tunability of ∼50% and can withstand electric fields of ∼1MV/cm, exhibiting a lower dielectric constant of ∼200. The dielectric loss in $Pb_{0.4}Sr_{0.6}TiO_3$ thin films is ∼3.5% and ∼3% in $Pb_{0.25}Sr_{0.75}TiO_3$ thin films. Increased dielectric constants with higher Pb content is observed as expected and the dielectric properties are similar to other reports [56].

### 3.2.3 Mn doped PST

For the fabrication and analysis of the high frequency test structures in the next section, doping of PST with Mn - a B-site acceptor dopant well known for lowering dielectric loss in perovskite ferroelectrics [179] - has been investigated, since

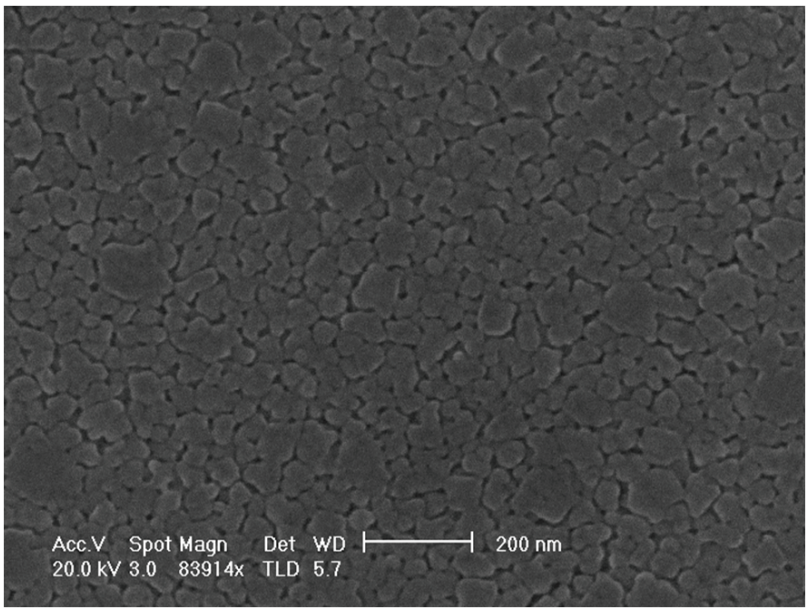



**Figure 3.2:** Scanning electron micrograph of $Pb_{0.25}Sr_{0.75}TiO_3$ on a Pt(100nm)/Ti/$SiO_2$/Si substrate.

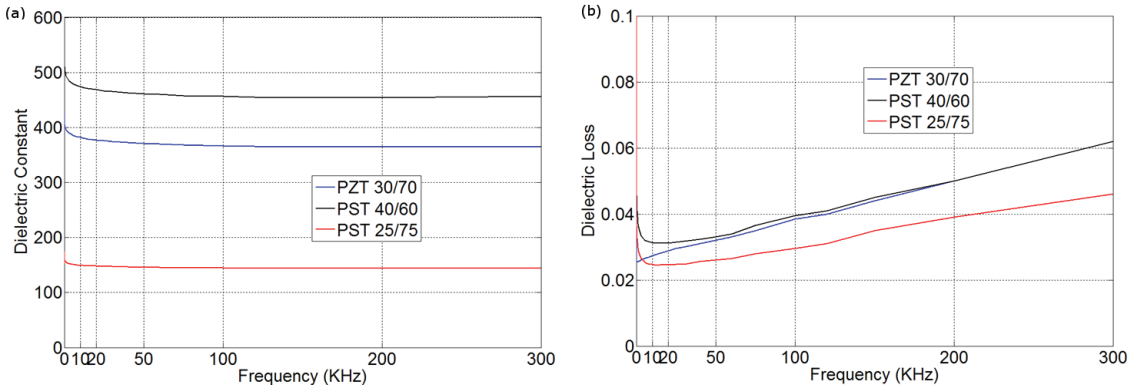



**Figure 3.3:** (a)Dielectric constant and (b) dielectric loss of $Pb_{0.3}Zr_{0.7}TiO_3$, $Pb_{0.4}Sr_{0.6}TiO_3$ and $Pb_{0.25}Sr_{0.75}TiO_3$, measured at a low frequency range.

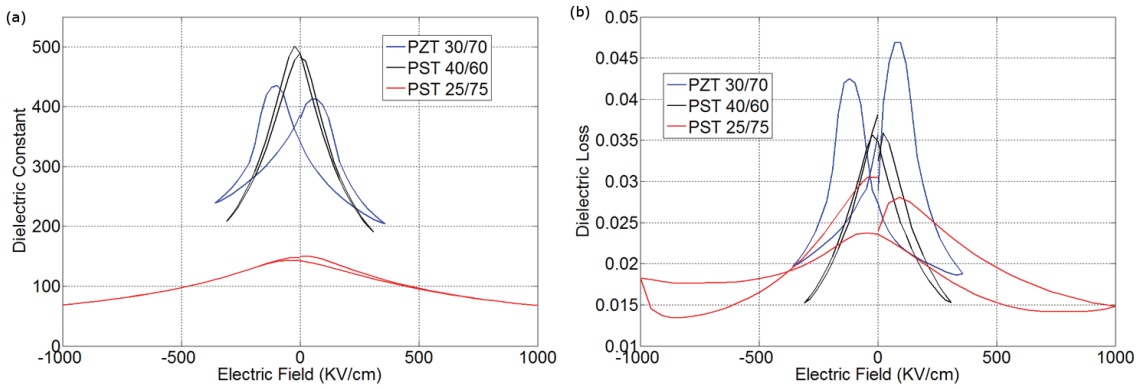



**Figure 3.4:** (a)Dielectric constant tunability and (b)dielectric loss of $Pb_{0.3}Zr_{0.7}TiO_3$, $Pb_{0.4}Sr_{0.6}TiO_3$ and $Pb_{0.25}Sr_{0.75}TiO_3$ measured at at 10KHz with an externally applied electric field.

enhanced dielectric properties with Mg [85] and La [32] doping of PST have been reported.

Sol-gel $(Pb_{0.4}Sr_{0.6})(Ti_{1-x}Mn_x)O_3$, thin films with x = 0, 0.01, 0.03 and 0.05, were deposited on Pt/Ti/SiO2/Si. These films were also characterized by XRD and SEM and shown to be well crystallized with a dense uniform grain structure and to exhibit a notable decrease in grain size with increasing Mn concentration [36]. It was found that the 3 mol% Mn films had the highest dielectric constant and tunability with maximum values of ∼1000 and 72% - see figure 3.5 - respectively measured at 100 KHz and these films were chosen for further high frequency characterization. The capacitance variation in a limited range around room temperature was measured and the monotonic decrease with temperature observed indicated that the material is in the paraelectric state at room temperature.

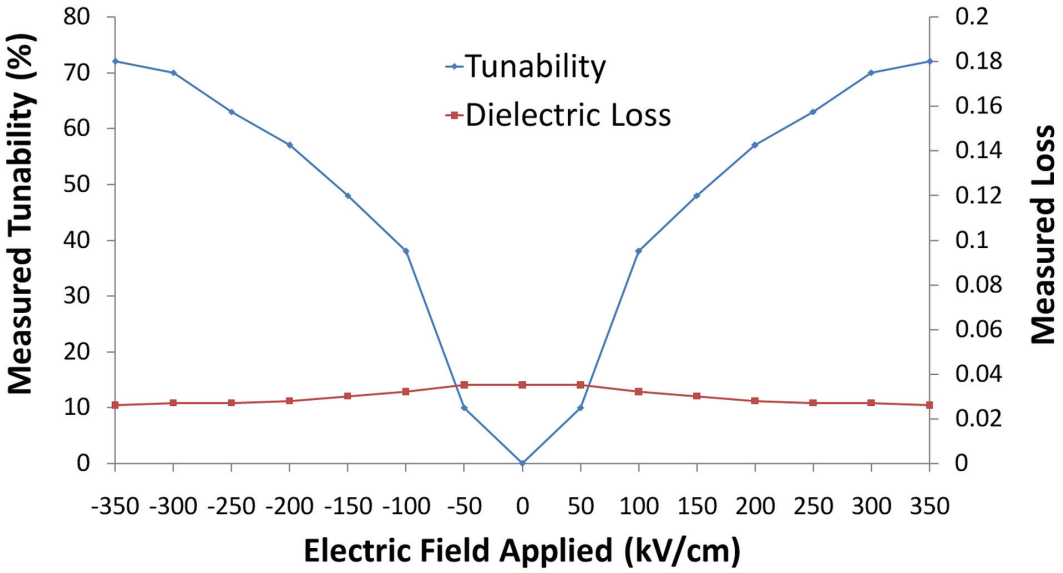



**Figure 3.5:** Dielectric constant tunability and dielectric loss at 100KHz as a function of applied electric field for 3% mol $Mn^{2+}$ PST measured on a 0.75mm diameter circular capacitor.

## 3.3 High frequency test structures

### 3.3.1 Design and simulation

There are a number of possible measurement configurations for high frequency impedance characterization of ferroelectric films, but all have in common the requirement to facilitate connection to a network analyzer via on-wafer ground-signal-ground RF probes. MIM capacitors are preferred to inter-digital capacitors both for varactor devices and test structures, as these have lower operating voltages. Bao [6] and Suzuki [156] report the use of one-port reflection measurements of MIM capacitors for characterization of ferroelectric varactors, including short

de-embedding structures, but both these are prone to contact resistance or probe dependency problems which have significant impact on measurement errors [123]. According to Cramer [23] and Zhu [186], two-port measurements techniques, can overcome these limitations, but the configurations they have used have limitations themselves. Cramer's is only suitable for large area capacitors and Zhu's has two MIM capacitors in series, which presumes that bias voltage is equally distributed between them. The configuration used to characterize the microwave properties of our PST films is based on the design proposed by Kulke et al [128], shown in figure 3.6. This was chosen particularly for its suitability for two-port measurements of the very small overlap area (5um × 5um) MIM capacitors used. The CPW dimensions were chosen so as to have an impedance of approximate 50 Ohms. The signal line width was $W_S = 0.1$ mm, and the gap was $W_G = 0.1$ mm.

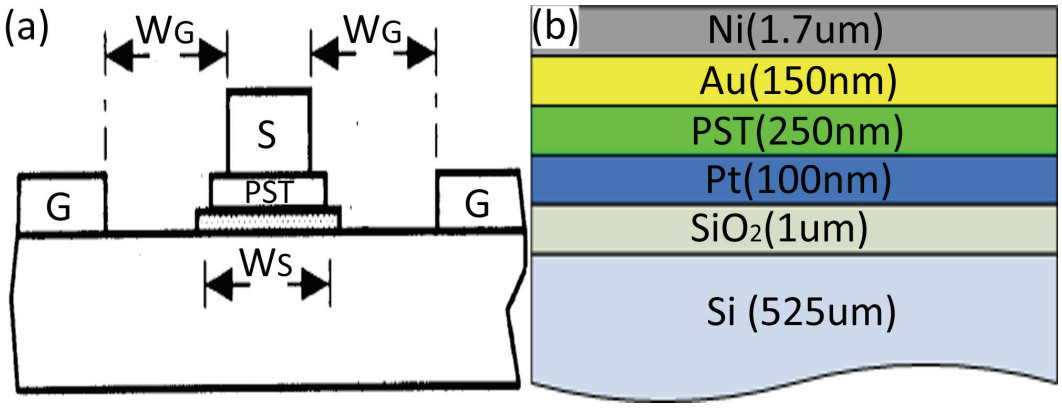



**Figure 3.6:** Schematic cross-sections showing (a) the CPW configuration and (b) the layer stack of the MIM capacitor.

The equivalent circuit, shown in figure 3.7, is similar to that used by Kulke, but includes the impedances due to overlap of the top and bottom electrodes and also a resistance in parallel with the PST capacitance to account for the dielectric loss. $R_{TE}$, $R_{BE}$, $L_{TE}$, $L_{BE}$ are the resistances and inductances of the top and

bottom electrodes in the MIM stack, while $R_{PST}$ and $C_{PST}$ are the resistance and capacitance of the PST thin film. $C_{GAP}$ represents the parasitic capacitance between the open end of the top electrode and the center strip conductor below the ferroelectric film. Also, $C_{P1}$ and $C_{P2}$ are the parasitic shunt capacitances of the MIM stack to the CPW ground. As assumed by Kulke, $C_{GAP}$, $C_{P1}$ and $C_{P2}$ are very small for the dimensions used and can be neglected.

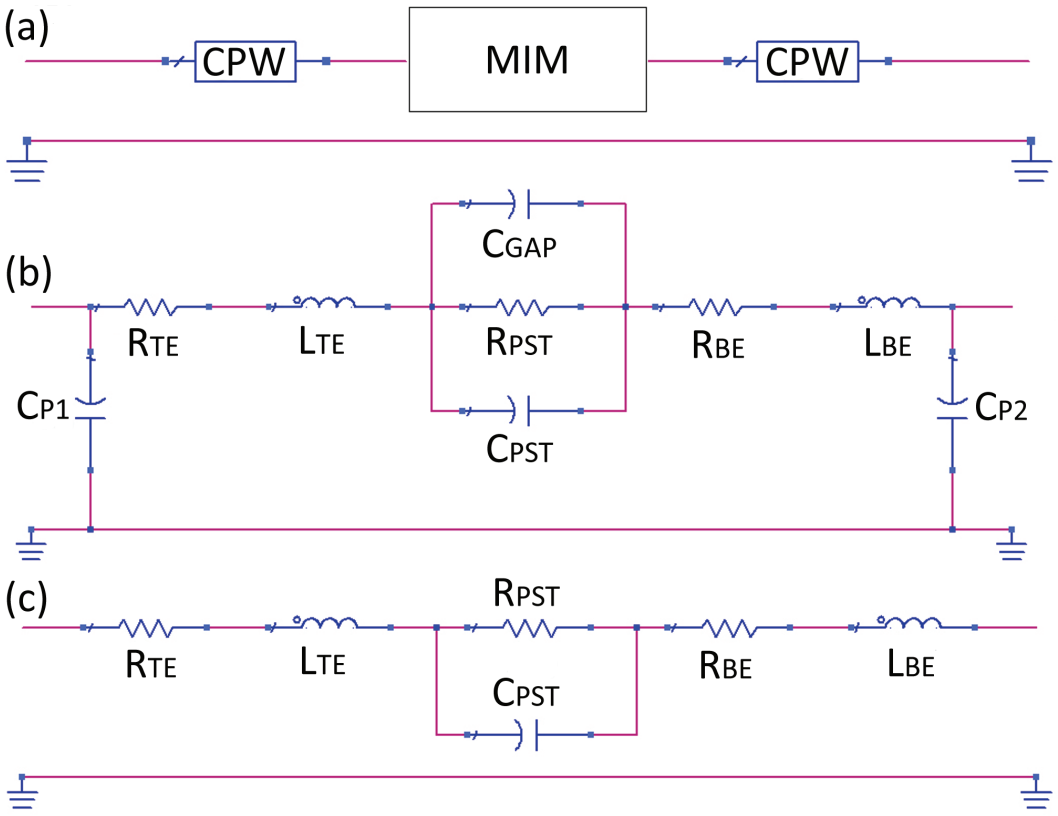



**Figure 3.7:** 2-port network equivalent circuits for MIM capacitor RF measurements: .(a) with connecting CPWs included, (b) showing the lumped element equivalent circuit of the MIM capacitor alone , (c) simplified lumped element equivalent of the MIM capacitor.

In the case of the simplified equivalent circuit displayed in figure 3.7c, the impedance, $Z_S$ of the signal path can be calculated analytically as follows:

$$Z_S = R_{EL} + j\omega L_{EL} + \frac{1}{G_{PST} + j\omega C_{PST}} \tag{3.1}$$

$$R_{EL} = R_{TE} + R_{BE}, L_{EL} = L_{TE} + L_{BE}, G_{PST} = \frac{1}{R_{PST}} \tag{3.2}$$

### 3.3.2 Fabrication process

PST MIM capacitors were fabricated on 4" diameter thermally oxidized high resistivity Si wafers. The full fabrication process for the MIM varactors can be found in Appendix C-1. In these devices, the process described earlier was used to deposit thin film PST to a thickness of 250nm on top of a 100nm thick RF magnetron sputtered Pt layer, which had been previously patterned using a lift-off process. The thermal oxide serves two purposes: it acts as a barrier against products, principally Pb from the PST sol diffusing into the Si and also prevents interaction of the Pt and Si at the high temperatures used for PST growth. A convenient feature of PST in contrast to thin film PZT for example, is that it can be deposited on $SiO_2$ without need of an additional barrier layer to prevent deleterious interactions between the sol and $SiO_2$.

To form the specific capacitor areas and provide access to the bottom electrode, the PST film was etched using a dilute HF and HCl solution. For the top electrode, 150nm of RF magnetron sputtered Au were used as a seed layer for a 1.7um electroplated Ni layer, in order to reduce the ohmic losses. The fabricated devices are shown in figures 3.8 and 3.9.

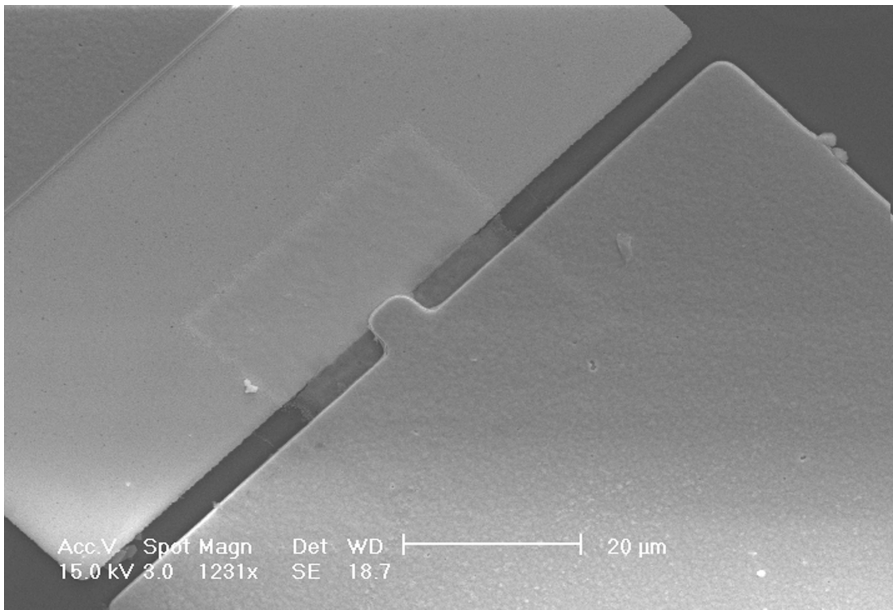



**Figure 3.8:** SEM micrograph of a 5um×5um fabricated series PST capacitor.

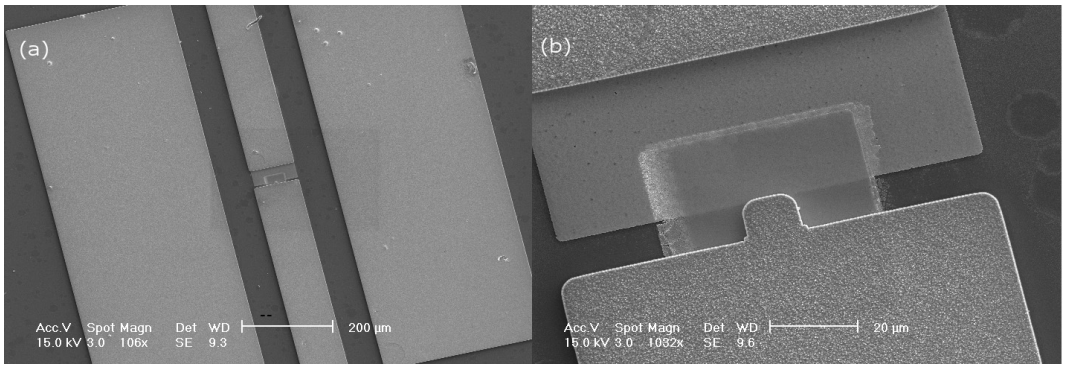



**Figure 3.9:** SEM micrographs of a 10um×10um fabricated parallel PST capacitor viewed on a: (a) 200um scale and (b) 20um scale.

## 3.4 Automatic dielectric property extraction technique

To accurately calculate the frequency dependent dielectric properties - mainly the dielectric constant, loss and tunability - from two-port S-parameter measurements

of the CPW MIM test structures, it is necessary to evaluate $C_{PST}$ and $R_{PST}$ at every frequency. The MIM capacitor's intrinsic S-parameters, were obtained by cascade de-embedding [18] of the connecting CPWs seen in figure 3.10, thus bringing the reference plane from the probe tips to the overlap of the MIM capacitor.

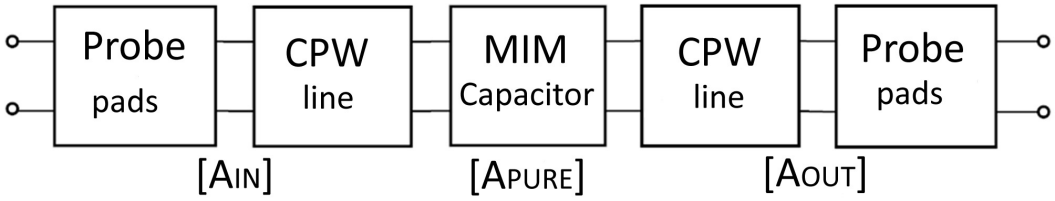



**Figure 3.10:** ABCD cascade matrix of the whole CPW MIM capacitor.

The probe pads were treated as an additional length of transmission line, since they have the same geometry as the connecting CPWs. The frequency dependent propagation constant and characteristic impedance of the connecting CPWs were evaluated by separate S-parameter measurements on a single 0.5mm CPW, fabricated directly on the substrate and implementation of existing formulas [73]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ \frac{1}{Z_0}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} & \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{bmatrix} \tag{3.3}$$

$$Z_{0l} = \sqrt{\frac{B}{C}} \tag{3.4}$$

$$\gamma = \frac{1}{0.0005} cosh^{-1}(A) \tag{3.5}$$

,where $Z_{0l}$ is the characteristic impedance of the CPW and $\gamma$ is the propagation constant of the electromagnetic wave.

Then the $A_{IN}$ and $A_{OUT}$ were deducted from the lossy transmission line formula:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh\,(\gamma l) & Z_{0l} sinh\,(\gamma l) \\ \frac{1}{Z_{0l}} sinh\,(\gamma l) & cosh\,(\gamma l) \end{bmatrix} \tag{3.6}$$

,where l is the length of connecting CPWs before and after the MIM.

Finally the MIM's intrinsic ABCD matrix was extracted by means of :

$$[A_{PURE}] = [A_{IN}]^{-1} [A_{OR}] [A_{OUT}]^{-1} \tag{3.7}$$

,where $A_{OR}$ is the full original measured matrix. The resulting $A_{PURE}$ was converted back to S-parameters.

Based on the $\pi$ equivalent circuit for a general two-port [129], the intrinsic MIM stack de-embedded data ($A_{PURE}$), could then be fitted to the equivalent MIM lumped element circuit. To do this, the de-embedded S-parameters were converted to Y-parameters [38].

Evaluating the admittance $Y_S$ from equation 3.1, after some transformations, we arrive at:

$$Re(Y_s) = \frac{R_{EL} G_{PST}^2 + G_{PST} + \omega^2 C_{PST}^2 R_{EL}}{(R_{EL} G_{PST} - \omega^2 L_{EL} C_{PST} + 1)^2 + (\omega R_{EL} C_{PST} + \omega L_{EL} G_{PST})^2} \tag{3.8}$$

$$Im(Y_s) = \frac{\omega C_{PST} - \omega L_{EL} G_{PST}^2 - \omega^3 L_{EL} C_{PST}^2}{(R_{EL} G_{PST} - \omega^2 L_{EL} C_{PST} + 1)^2 + (\omega R_{EL} C_{PST} + \omega L_{EL} G_{PST})^2} \tag{3.9}$$

It can be seen that there are two equations with 4 unknowns ($G_{PST}$, $R_{EL}$, $C_{PST}$ and $L_{EL}$).

As the length of the capacitor (5 um) is very small compared to the wavelength (i.e., 15 mm at 20 GHz), the MIM capacitor can be considered as a lumped element and the top and bottom electrodes combined are considered as a resistor $R_{EL}$ and inductor $L_{EL}$ in series. $R_{EL}$ can then be approximated as follows :

$$R_{EL} = R_{TE} + R_{BE} = \frac{\rho_{TE} l}{t_{TE} w} + \frac{\rho_{BE} l}{t_{BE} w} \tag{3.10}$$

, where $\rho_{TE}$ and $\rho_{BE}$ are the resistivities of the metal used for the top and bottom electrodes, l is the length of the top electrode, w is the width of the top electrode and $t_{TE}$ and $t_{BE}$ are the thicknesses of the top and bottom electrodes respectively. For this particular test structure, the platinum bottom electrode having a thickness of only 100 nm dominates the total resistance of the electrodes and would be the main factor limiting the Q of a potential PST varactor. However, a way to overcome this which has been recently demonstrated [131] is to transfer bond the fabricated device onto a separate substrate which would enable the bottom electrode to be thickened up.

The total inductance, $L_{EL}$=$L_{TE}$+$L_{BE}$ can be approximately extracted from the measured self - resonance of the MIM capacitor's phase and was found to be approximately ∼0.02nH. This small inductance, along with the electrode resistance, can give rise to large characterization errors if neglected - see figure 3.11 - by forming a resonator with the test capacitor, but these can be fully accounted for if equations 3.8 and 3.9 are used.

Using the symbolic toolbox of MATLAB, the algorithm solves all the equations, outputting the frequency dependent values of $C_{PST}$ and $R_{PST}$. The Palmer formula is used to relate the capacitance to the dielectric constant of the PST, due to the small area of capacitor and the effect of the fringing capacitance [52].

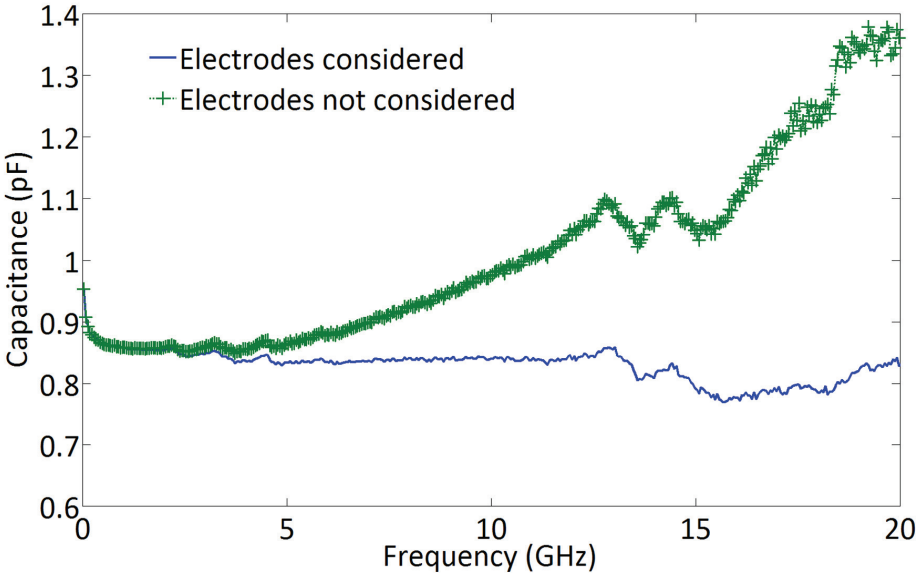



**Figure 3.11:** Extracted capacitance for a 5 um × 5 um PST MIM capacitor with and without taking the electrodes into consideration.

$$C = \frac{\epsilon w l}{d}\left\{1 + \frac{d}{\pi w}\left[1 + ln\left(\frac{2\pi w}{d}\right)\right]\right\}\left\{1 + \frac{d}{\pi w}\left[1 + ln\left(\frac{2\pi w}{d}\right)\right]\right\} \tag{3.11}$$

Finally the dielectric loss is computed by :

$$tan\delta = \frac{1}{R_{PST}\omega C_{PST}} \tag{3.12}$$

The MATLAB software developed for the above calculations can be found in Appendix A-3. It must be noted that for the above analysis the resistance and inductance of the electrodes has been considered as a constant value. In a later section (section 5.2), frequency-dependent values for the resistance and inductance

of the electrodes were extracted from a 'short' test structure (Appendix A-2), allowing the even more accurate extraction of the dielectric properties.

## 3.5 Measurements and results

After having first carried out an accurate line-reflect-reflect-match (LRRM) calibration using a Cascade calibration substrate, to bring the reference plane to the probe tips, S-parameter measurements from 1 GHz to 25 GHz, were made using an Agilent E8361A Vector Network Analyzer (VNA) and a Cascade Microtech Summit 12000 automatic probe station with 1601 frequency points and an IF bandwidth of 300Hz. The contact position and contact pressure of the probes were initially adjusted and then fixed, so as to ensure reproducibility of the measurements. Also, the microscope light was turned off during the measurements - to avoid photo-voltaic effects in the highly resistive silicon - and sufficient time was allowed for stabilization of the measurements. Contact sensitivity experiments revealed that for five subsequent measurements (in which contacts were made and released), the capacitance and loss ratio of standard deviation over mean values were less than 1% and 3%, respectively. The MIM capacitors were biased up to 6 V (=240 kV/cm) via the VNA's external bias ports and the extracted PST dielectric values are shown on figure 3.12. The devices broke down prematurely (at $\sim$ 6.5V) compared to low frequency measurements an effect that has yet to be understood but as observed by Xu [51], may be due to surface leakage and so may be amenable to the solution they used, which was to include a $SiO_2$ passivation layer. There is little change in the extracted dielectric properties with $\epsilon\sim$1000 and tan$\delta\sim$0.03 in the range 1 - 5 GHz, and these agree quite well with low frequency measurements. In this regime, the material would be suitable for many frequency agile applications although not at the high performance end requiring tan$\delta<$0.01.

The observed tunability, ∼50%, is not considered representative as it was affected by the earlier noted premature device breakdown but would need to be increased up to, and preferably beyond, the observed low frequency value of 72% for useful device operation. As the frequency increases the dielectric loss shows with monotonic increase in tan$\delta$, similar to that observed for other candidate tunable dielectrics, BST and $SrTiO_3$ [6] and as discussed by Tagantsev [159] intrinsic effects (ac field interaction with the phonon distribution, and quasi-Debye losses) and extrinsic effects such as mobile charged defects can account for this behavior.

The spikes in figure 3.12b, which become increasingly intense with to those observed in $SrTiO_3$ by Gevorgian [43] and Morito [102] and are tentatively identified as due to electromechanical resonances associated with the combined action of electrostrictive and piezoelectric effects. Although these acoustic vibrations can be deleterious to varactor operation, particularly with regard to tan$\delta$, devices can be carefully designed to suppress them [44]. Furthermore, these acoustic resonances have already been made use of [7], [187] in thin film bulk acoustic resonators for tunable applications. As shown in figure 3.12b, small loss peaks are present even at zero bias, which suggests that the PST has some weak background piezoelectricity. These have also been observed by Gevorgian [43] in $SrTiO_3$ and following his suggestion these may be due to a lowering of the symmetry of the crystal lattice caused by thin film stress. To investigate the possible usefulness of this effect in PST, a one dimensional Mason model has been developed similar to those previously presented for $SrTiO_3$ and BST [43], [110]. In this model, the well known formalism used for describing piezoelectric transducer operation has been modified to allow for field dependence of the effective piezoelectric and elastic constants and hence also of the electromechanical coupling coefficient ($k^2_{33}$) and acoustic velocity ($V_{ac}$) - the parameters that appear directly in the equations.

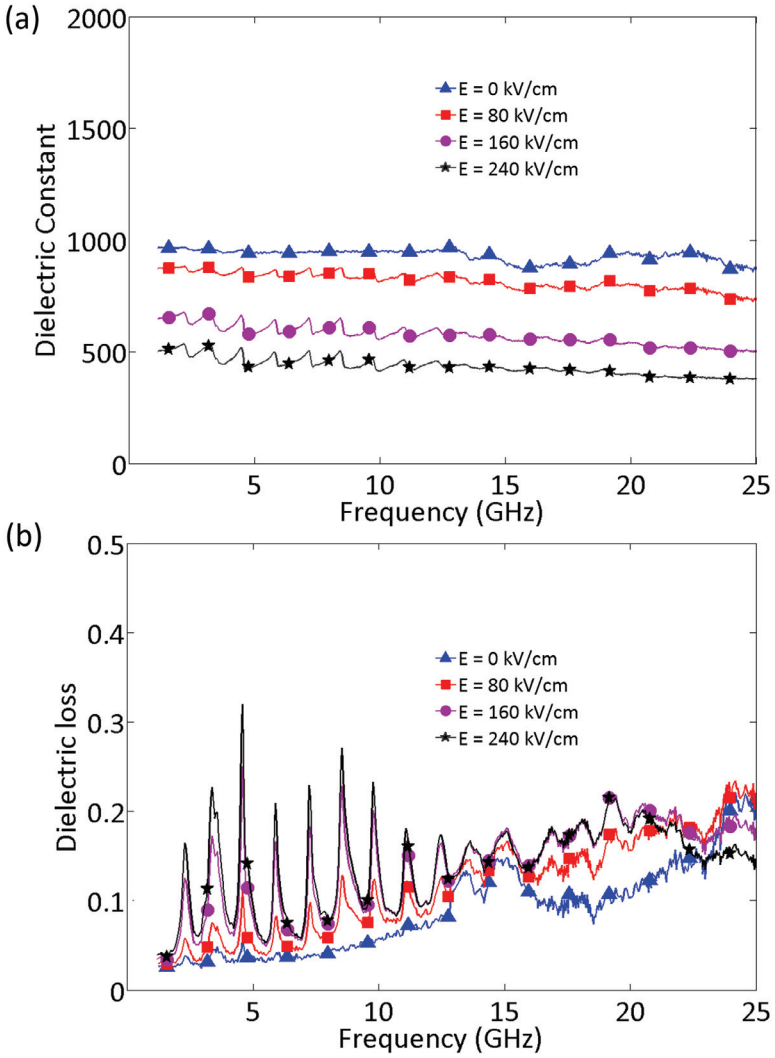



**Figure 3.12:** Extracted values for (a) dielectric constant and (b) dielectric loss of the thin-film PST up to 240 kV/cm applied electric field.

## 3.6 Acoustic modeling

The MATLAB modeling software used for the acoustic simulations is found in Appendix A-4. Using solutions of the one dimensional plane wave boundary value

problem as given by Rosenbaum [132] and Lakin [75], a piezoelectric layer - in this case PST - with mechanically loaded end faces, has the following electrical impedance :

$$Z = \frac{1}{j\omega C_0}\left(1 - K^2\frac{tan(\phi)}{\phi}\right)\frac{Z_{PST}(Z_t + Z_b)cos^2(\phi) + jZ_{PST}^2 sin(2\phi)}{Z_{PST}(Z_t + Z_b)cos(2\phi) + j(Z_{PST}^2 + Z_t Z_b)sin(2\phi)} \tag{3.13}$$

$K^2$=$k^2_{33}$/(1+$k^2_{33}$), $\phi$=$\beta$d/2, and $\beta$=$\omega$/$V_{ac}$, where $\omega$ is the angular frequency, $V_{ac}$ is the PST acoustic velocity, d is the thickness of the PST film, $Z_t$, $Z_b$, $Z_{PST}$ are the acoustic impedances at the top and bottom end faces and of the PST film respectively and $k^2_{33}$ is the longitudinal electromechanical coupling coefficient. $Z_t$ and $Z_b$ are obtained by successive application of the transmission line equation to all the layers in the device stack. Starting from the outermost layer (i=1) the impedance at the i/i+1 boundary is :

$$Z_{i/i+1} = Z_i\left(\frac{Z_{i/i-1}cosh(\gamma_i d_i) + Z_i sinh(\gamma_i d_i)}{Z_i cosh(\gamma_i d_i) + Z_{i/i-1}cosh(\gamma_i d_i)}\right) \tag{3.14}$$

, where $Z_0$, $Z_i$ and $\gamma_i$, $d_i$, are are the acoustic impedances of the zeroth layer, air (taken as zero) and layer i, the propagation constant and thickness of layer i, respectively. The propagation constant $\gamma_i$ is related to the acoustic attenuation ($\alpha_i$) and wave number ($\beta_i$) by: $\gamma_i$=$\alpha_i$+j$\beta_i$, $\alpha_i$=$\omega$/2$V_{ac}Q_i$, $\beta_i$=$\omega$/$V_{ac}$ and $Q_i$ is the acoustic quality factor of each material. Although $Q_i$ varies with frequency and phenomenologically it is found to have a dependence [132] in many materials, for simplicity in this work it was assumed frequency independent and the values used for the different layers in the structure are given along with other acoustic properties in table 3.1. Finally, acoustic attenuation for the PST thin film is introduced in equation 3.13 as a resistive term by adding an , part into the phase

- in equation 3.15.

$$\phi_{PST} = \left( \frac{\omega}{V_{ac}} - j\alpha_{PST} \right) d_{PST} \tag{3.15}$$

**Table 3.1:** Acoustic properties of materials.

| Material | Density $\rho$ (kg/m$^3$) | Longitudinal acoustic velocity (m/s) | Acoustic impedance (kg/m$^2$s) | Acoustic quality factor $Q_i$ |
|---|---|---|---|---|
| Ni | 8900 | 5600 | $49.84\times10^6$ | 150 |
| Au | 19300 | 3210 | $61.95\times10^6$ | 120 |
| $SrTiO_3$ | 3720 | 8050 | $29.94\times10^6$ | 9500 |
| Pt | 21500 | 3260 | $70.09\times10^6$ | 150 |
| $SiO_2$ | 2460 | 5900 | $14.51\times10^6$ | 500 |
| Si | 2340 | 8433 | $19.73\times10^6$ | 100 |

In the absence of firm data for PST, values for $SrTiO_3$ [43] were used as an approximation. It is also important to note that both $k^2{}_{33}$ and $V_{ac}$ for PST are field dependent, the field dependence of $V_{ac}$ following from the relation [132] :

$$V_{ac} = V_{ac}^{(0)} \sqrt{(1 + k_{33}^2)} \tag{3.16}$$

$$V_{ac}^{(0)} = \sqrt{\frac{c}{\rho}} \tag{3.17}$$

, where c is the appropriate elastic constant of PST.

Taking measured RF data for 4 bias fields (0, 80, 160 and 240 KV/cm), the best fit to these - shown in figure 3.13a - was obtained by making fine adjustments to the parameters, principally the acoustic velocities in Pt and Ni, until with

these fixed it was only necessary to vary $k^2_{33}$ to obtain best fit for the different biases. In figure 3.13b the plot for 240 kV/cm bias field has been selected and compared with measured data. As can be seen the fit is quite good: the difference between the model's predicted resonant frequencies and the measured values is never more than 5%. However, to get a better fit, especially to the magnitude of the resonances, more accurate material properties and frequency dependent acoustic quality factors must be used. The resulting $k^2_{33}$ variation with bias field is shown in figure 3.13ac and is roughly linear as would be expected for electrostrictive behavior. An interesting feature is the observed maximum value of $k^2_{33}\sim0.04$ which is significantly higher than the value for the same field, $\sim0.013$, recently reported by Noeth [110] for $Ba_{0.3}Sr_{0.7}TiO_3$. Although $k^2_{33}$ may be lower due to the slightly composite nature of the resonant structure used by Noeth [110], it does show that the effect in PST would be potentially useful for tunable FBAR applications. As noted above, there is also a slight piezoelectric response even at zero bias, which translates into a very small but still existent electromechanical coupling coefficient ($k^2_{33}\sim0.0025$).

## 3.7 Conclusion

The sol-gel growth of 3% Mn doped PST films with good crystallinity and dense uniform grain structure on 4" Si wafers has been demonstrated. MIM capacitors have also been fabricated and development of an improved de-embedding technique that takes into account the whole test structure impedance has enabled accurate extraction from these of the high frequency dielectric properties of the PST films. In the low GHz range (1-5 GHz) practically useful values of $\epsilon\sim1000$ and $\tan\delta\sim0.03$ have been obtained. Although a similarly useful tunability of 72% has been obtained on low frequency test structures further work is needed to un-

derstand the premature breakdown effect which has limited the RF tunability to ∼50%. Peaks in the dielectric loss due to acoustic resonance have been modeled and found to be in accordance with electrostrictive behavior and the calculated electromechanical constant for this effect compares well with values recently reported for other tunable ferroelectric materials.

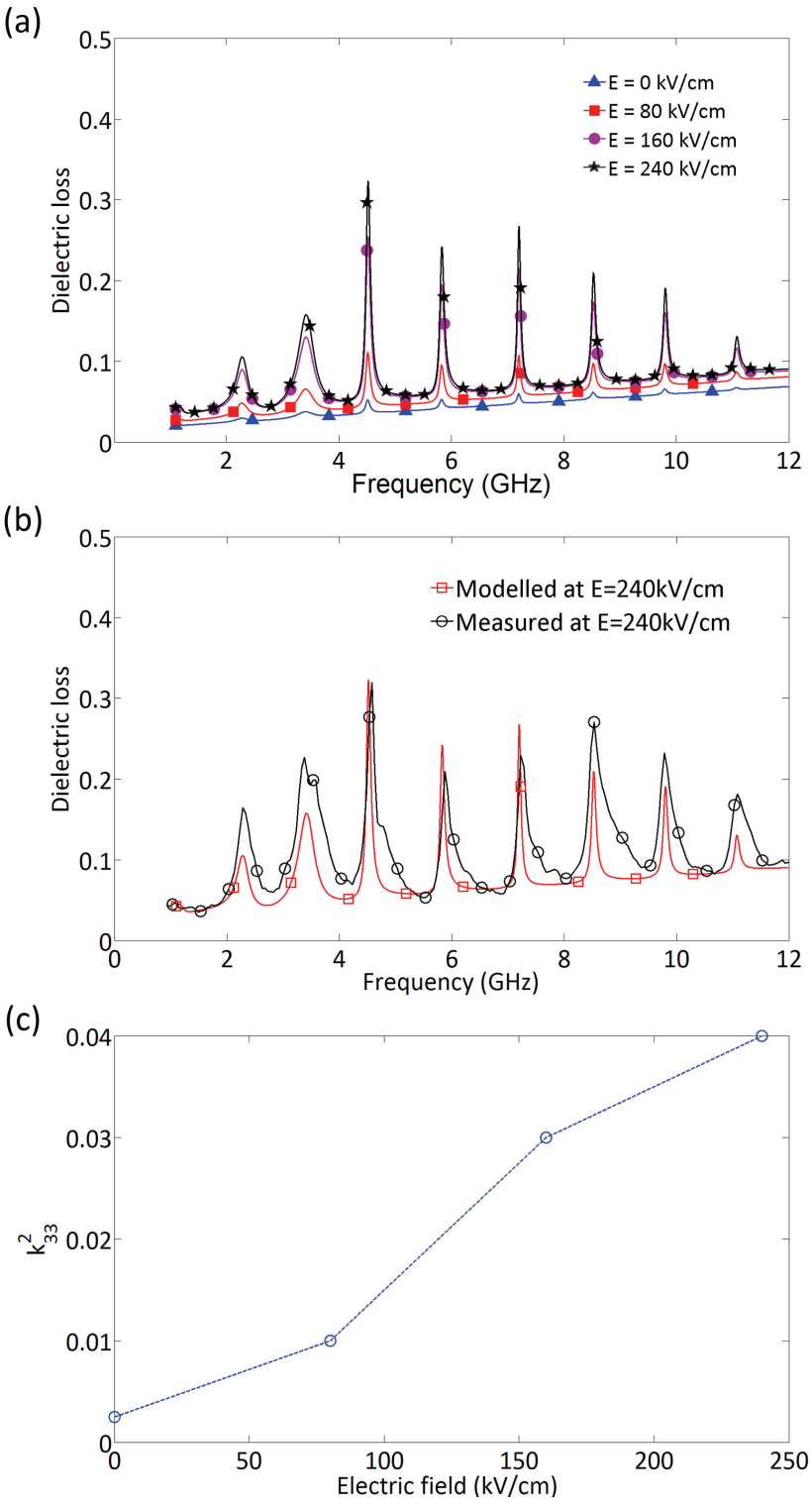



**Figure 3.13:** Modeling results for a 5um×5um PST capacitor: (a) simulated loss tangent for a range of bias fields up to 240 kV/cm, (b) simulated and measured loss tangent at 240 kV/cm, (c) against applied electric field.

Chapter 4

# Ferroelectric varactor electrode optimization

## 4.1 Introduction

On the previous chapter, the de-embedding of the ferroelectric varactor electrode resistance and inductance, allowed the more accurate extraction of the thin film ferroelectric properties. Although, this is a valid technique for material properties extraction, the electrodes of the ferroelectric varactor will be attributing to the losses of any microwave device which will be incorporating them. Therefore, optimizing the electrodes in terms of electrical resistance is important. At the same time, adhesion and surface quality of the electrodes must be sufficient to allow device fabrication with a good yield. In this chapter, an investigation into a variety of Au bottom electrode structures for implementation in ferroelectric varactors is presented. A defect free electrode structure with low resistance was established and thin film PST ferroelectric tunable varactors were fabricated. Measurements made at low and high frequencies demonstrate the enhanced performance compared to ferroelectric varactors with - commonly used - Pt bottom electrodes.

## 4.2 High conductivity Au bottom electrodes for lead-based ferroelectric RF varactors

Thin film ferroelectric capacitors have been researched as candidates to varactor diode, semiconductor-switched capacitor and RF MEMS tunable capacitor technologies for the realization of microwave tunable capacitors, due to their low cost and miniaturization potential [162]. This possible varactor size reduction originates from their high dielectric constant, but realizing minuscule high Q varactors involves not only implementing ferroelectrics with very low dielectric loss, but also minimizing the resistive losses of the electrodes of the capacitor stack, while still complying with the high thermal budget of ferroelectric varactor fabrication. Ferroelectric annealing can create defects from thin film strains due to lattice mismatches between the underlying substrates and films or due to different thermal expansion coefficients of substrates and films. Furthermore, at high temperatures, the adhesion layers used for the bottom electrode materials - usually Ti and Cr - are known to diffuse and oxidize and this can lead to defect and crack formations on both the electrodes and the ferroelectric film.

Pt is the most widely used electrode material for ferroelectric growth as it has high thermal conductivity, good stability in a high temperature oxygen environment and gives rise to a low leakage current [105], but has the disadvantage of poor conductivity. Thickening of the Pt layer will of course reduce resistive loss but there is limited scope for this as with thicker layers the increased mechanical load on the substrate due to stress in the Pt can cause delamination of electrodes during later device processing and also the preferred orientation of the perovskite phase is reduced. Highly conductive metals like Ag [112] and Cu [35] have been investigated as bottom electrodes for ferroelectric growth with some success, though either additional barrier layers are required or complex annealing schedules. Pt-Au inte-

gration electrodes have been studied for thermal stresses in power transistors [19] and recently, a bottom electrode consisting of a multilayer of inert Pt-Au layers on $TiO_2$ [170],[2] has been implemented for high Q BST varactors. This composite electrode structure results in a radical decrease in electrode resistance compared to pure Pt, but due to Pt diffusion in Au [145],[104],[19] the final electrode resistance can degrade, when compared to before the ferroelectric deposition, depending on the process and annealing time. Although ferroelectrics and specifically BST, have been also deposited on pure Au [55],[144] electrodes, the properties of the whole Au bottom electrode stack including $SiO_2$ and $TiO_2$ barrier layers and adhesion layers, in terms of adhesion, resistance, surface and crystal structure have not been fully investigated for ferroelectric annealing temperatures.

The use of Au in bottom electrode layer structures for RF devices incorporating sol-gel deposited $Pb_xSr_{1-x}TiO_3$ (PST) and by extension to other lead based thin film ferroelectrics, is investigated. The study focused on single layers of Au and combinations of Pt and Au and compared these in terms of adhesion, sheet resistance, surface morphology and crystallinity with the more conventionally used single Pt layers both before and after subjecting them to a simulated PST crystallization cycle.

### 4.2.1 RF Performance of Ferroelectric devices

The importance of electrode resistance to ferroelectric RF device performance can be appreciated by considering the simplified equivalent circuit of figure 4.1a.

This is the same as that used to model the conventional semiconductor varactor, but with C as the capacitance of the ferroelectric capacitor structure - seen in figure 4.1b - rather than junction capacitance and $R_p$ the resistance arising from dielectric loss ($\tan\delta$) in the ferroelectric - $R_p=1/(2\pi f\times\tan\delta\times C)$, at frequency f -

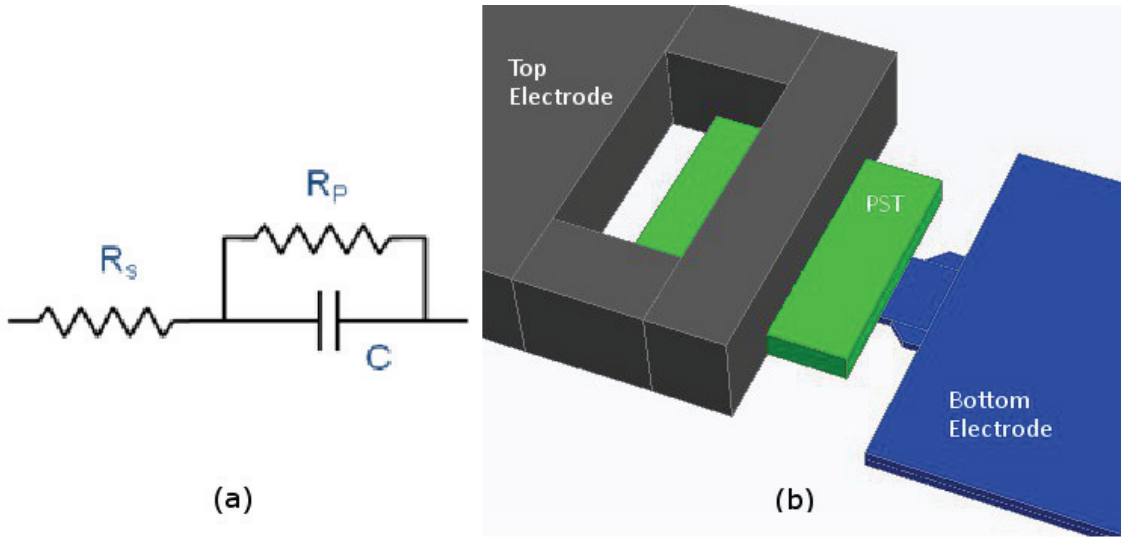



**Figure 4.1:** (a) Simplified equivalent circuit and (b) 3D schematic of a PST ferroelectric varactor.

rather than junction leakage. For this circuit the maximum quality factor (Q), a measure of energy stored to energy dissipated and a key figure-of-merit for device performance, is approximately given by [157] $(R_p/4R_s)^{0.5}$ where $R_s$ is the series resistance, which if resistive interface layers can be neglected, is dominated by the resistance of the electrodes. The problem of minimizing $R_s$ and hence maximizing Q for a given metal and electrode geometry (i.e. track length to width ratio or number of 'squares') is exacerbated at high frequencies ($>\sim$1GHz) since electrode resistance can only be reduced to a limited extent by increasing the metal thickness. This arises due to the skin effect, whereby as frequency increases the RF current is increasingly confined to a surface layer on the conductor, the thickness of which is governed by the skin depth, $d_s=(\rho/\pi f\mu)^{0.5}$, where $\rho$ is the DC resistivity and $\mu$ the permeability. As conductor thickness is increased up to several skin depths the sheet resistance approaches a minimum given by $\rho/2d_s$.

A plot of this minimum sheet resistance as a function of frequency (figure 4.2) clearly shows the advantage that Ag, Cu and Au electrodes have over Pt for RF applications.

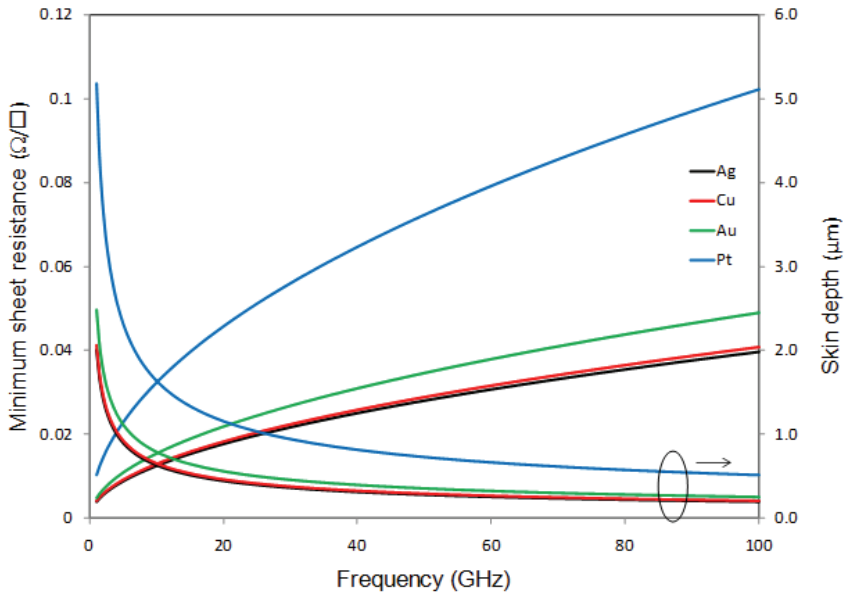



**Figure 4.2:** Skin depth and resulting minimum sheet resistance for various metals as a function of frequency.

## 4.3 Experimental

The metal films for all the electrode systems investigated were deposited on thermal oxide ($SiO_2$) coated silicon substrates (oxide thickness: 200 nm) by RF magnetron sputtering, the conventionally used technique for providing thin film ferroelectric and other device metalization. A range of layer combinations were investigated which are listed in the first column of Table 4.1: 100 and 400 nm

thick single layers of Pt and Au, Au-Pt multilayers, and all of these with and without an underlying thin (7 nm) Ti adhesion layer. In a sub-set of test samples a $TiO_2$ layer was included on top of the $SiO_2$ which was formed by oxidizing a sputter deposited Ti layer. To ensure complete oxidation of the Ti throughout its thickness two 40nm thick Ti films were deposited with an oxidation step after each deposition which was carried out using rapid thermal annealing (RTA) in an air ambient. For this step samples were heated from room temperature up to $700^oC$ over approximately 30 seconds and held at this temperature for 3 minutes before being removed. The final thickness of the $TiO_2$ was measured to be 120 nm.

For all the electrode systems, a hotplate bake in air at $700^oC$ for 10 minutes was used as the annealing condition. This was chosen to simulate the sol-gel PST crystallization bake used in our laboratory and is also representative of those used in other growth techniques such as pulsed laser deposition (PLD) and sputtering. The effects of the annealing process on the electrical properties and adhesion of the metal layers were assessed by 4-point probe sheet resistance measurements and tape tests before and after annealing, respectively. Although tape testing, in this case using polyimide adhesive tape, is only qualitative, it does give a good indication as to whether an electrode structure will survive device processing. The effects of annealing on crystal structure and surface morphology were assessed by XRD, SEM and atomic force microscopy (AFM) .

## 4.4 Results and discussion

### 4.4.1 Layer adhesion and Sheet resistance measurements

Results for the (Ti)Au, (Ti)Pt and (Ti)Au-Pt electrode systems are discussed with reference to Table 4.1.

*$Au/SiO_2$*: With both the 100 nm and 400 nm thick films, adhesion was poor as indicated by their failing the tape test both before and after annealing. These results are consistent with previous studies which have shown that $Au/SiO_2$ has a quite low adhesive energy ($\sim$0.4 J/m$^2$ for type I delamination) [64] and also with the general empirical evidence that noble metals have low adhesion due to their unreactivity. The strong dependence of sheet resistance on grain size in thin films makes comparison with other work difficult but the measured values are broadly in line with those previously reported [24]. The slight decrease in sheet resistance on annealing observed for these single Au layers is an effect that has previously been reported [95] and explained in terms of mechanisms involving grain growth following annealing of defects, giving a more highly packed film. Such defect annealing is likely to take place in all the layer combinations studied here though usually another effect will dominate.

*$Au/Ti/SiO_2$*: To improve the adhesion of Au to the underlying $SiO_2$ a thin Ti(7 nm) layer was incorporated between the Au and oxide layer. It has been shown that whether diffusion of Ti occurs through the volume of the grains or along the grain boundaries depends on whether the sample is annealed under vacuum or in air. Here the annealing is done in air so the predominant diffusion will be along grain boundaries [99]. As shown in Table 4.1, the presence of a thin Ti layer underneath a 100 nm Au layer improves the adhesion whereas this is not the case on the thicker 400 nm Au layer which fails the tape test, presumably because of

increased layer stress. For this system the sheet resistance increases on annealing which could be due to Ti-Au phases being formed or as seems more likely due to Ti diffusing along grain boundaries possibly as far as the top surface of the Au where it would form $TiO_2$. There is some evidence for this in the SEM images as will be discussed later. This increase is only seen for the 100 nm Au layer and presumably for the thicker, 400 nm, Au the dominant effect is the lowering of the resistivity due to the annealing of defects, grain growth and possibly depletion of the Ti layer.

*$Au/TiO_2$ and $Au/Ti/TiO_2$*: Direct deposition of Au on $TiO_2$ resulted in poor adhesion, a surprising result as quite good adhesion, at least on the nano-scale, is reported with reasonable $\sim$1 J/m$^2$ adhesion energies. It is thought this may be due to the need to break the vacuum in the sputtering system between the Ti and Au depositions to enable the Ti to be oxidized to $TiO_2$. With this process there is the danger that the $TiO_2$ surface becomes contaminated so giving poor adhesion. The addition of a thin Ti layer on top of the $TiO_2$ followed by deposition of the Au layer without breaking the vacuum in the sputtering system results in good adhesion for both the 100 nm and 400 nm Au layers both as deposited and after annealing. We note that other studies have shown that the introduction of an in-situ ion clean process between layers in the $Pt/TiO_2$ system results in a robust system [45]. For the $TiO_2$/Ti/Au(400 nm) system there was no change in the measured sheet resistance on annealing which is an indication of a stable metalization system. The improved adhesion obtained when a thin Ti layer is introduced can be explained by the reduction of impurities and bonding to Ti. The mechanism whereby Ti diffuses through Au grain barriers to the top surface will also occur in this system.

**Table 4.1:** Sheet resistance values and the outcome of adhesion tape tests for all electrode configurations. For the adhesion tests a tick indicates no delamination either immediately after electrode deposition or following the annealing schedule. An '×' indicates failure and delamination during the tape test.

| | Sheet Resistance (Ω/sq) | | Tape test | |
|---|---|---|---|---|
| | R.T. | $700^o$ | R.T. | $700^o$C |
| Au(100nm) | 0.35 | 0.3 | × | × |
| Au(400nm) | 0.096 | 0.091 | × | × |
| Ti(7nm)/Au(100nm) | 0.4 | 0.49 | ✓ | ✓ |
| Ti(7nm)/Au(400nm) | 0.1 | 0.092 | × | × |
| $TiO_2$/Au(100nm) | 0.4 | 0.35 | × | ✓ |
| $TiO_2$/Au(400nm) | 0.1 | 0.099 | × | × |
| $TiO_2$/Ti(7nm)/Au(100nm) | 0.48 | 0.42 | ✓ | ✓ |
| $TiO_2$/Ti(7nm)/Au(100nm) | 0.12 | 0.12 | ✓ | ✓ |
| Pt(100nm) | 2.56 | 1.47 | ✓ | ✓ |
| Ti(7nm)/Pt(100nm) | 2.55 | 2 | ✓ | ✓ |
| Ti(7nm)/Pt(300nm) | 0.67 | 0.63 | ✓ | ✓ |
| Ti(7nm)/Pt(500nm) | 0.37 | 0.37 | × | × |
| Ti(7nm)/Pt/Au(200nm)/Pt | 0.14 | 0.74 | ✓ | ✓ |
| Ti(7nm)/Pt/Au(400nm)/Pt | 0.065 | 0.295 | ✓ | ✓ |
| $TiO_2$/Ti(7nm)/Pt/Au(200nm)/Pt | 0.166 | 0.851 | ✓ | ✓ |
| $TiO_2$/Au(200nm)/Pt(100nm) | 0.144 | 0.79 | × | × |

### 4.4.2 Crystal structure and surface texture of Au on $SiO_2$/Si substrates

XRD measurements were performed on all the samples discussed above before and after annealing, see figures 4.3 and 4.5, and in all cases a preferred (111) orientation of the gold films parallel to the substrate surface was obtained with no evidence of deleterious phase formations. XRD rocking curve full width half maximum (FWHM) values were also reduced on annealing which is suggestive of the increased order-defect reduction on annealing discussed above. For all samples there is no evidence of Ti-Au interactions although this cannot be ruled out because of the thin Ti layers.

Figure 4.4 shows SEM images of the surfaces of the $Au/SiO_2$ and $Au/Ti/SiO_2$ samples after annealing, in all of which it can be seen that substantial grain growth has occurred, in line with previous reports. More ordered and larger polygonal grains are observed for Au deposited directly on $SiO_2$ with grain diameters varying from 0.3-1 um. The addition of the thin Ti layer leads to more irregular crystallite growth (figure 4.4c), and smaller grains. Recrystallization kinetics would be expected to be more rapid for Au than Ti due to the lower melting temperature - 1063$^o$C compared to 1720$^o$C. Figure 4.4c and to some extent 4.4d indicate that the slower increase of grain size with annealing for Ti imposes a constraint on the increase for Au upon annealing for thin Au layers. This influence is likely to be less for the thicker Au (400 nm) layer as is indeed seen (figure 4.4d). As previously discussed, Ti diffuses along Au grain boundaries and this could also restrict grain growth. Another feature observed in the $Au/SiO_2$ sample (Figure 4.4a) is a high density of hillocks. These form to reduce the compressive stress and many of the smaller ones blister and delaminate from the substrate. Such blistering does not occur in $Au(100nm)/Ti/SiO_2/Si$ samples and in this case the hillocks are faceted suggesting that they consist mainly of Au. As expected larger grains, 1-4 um, are

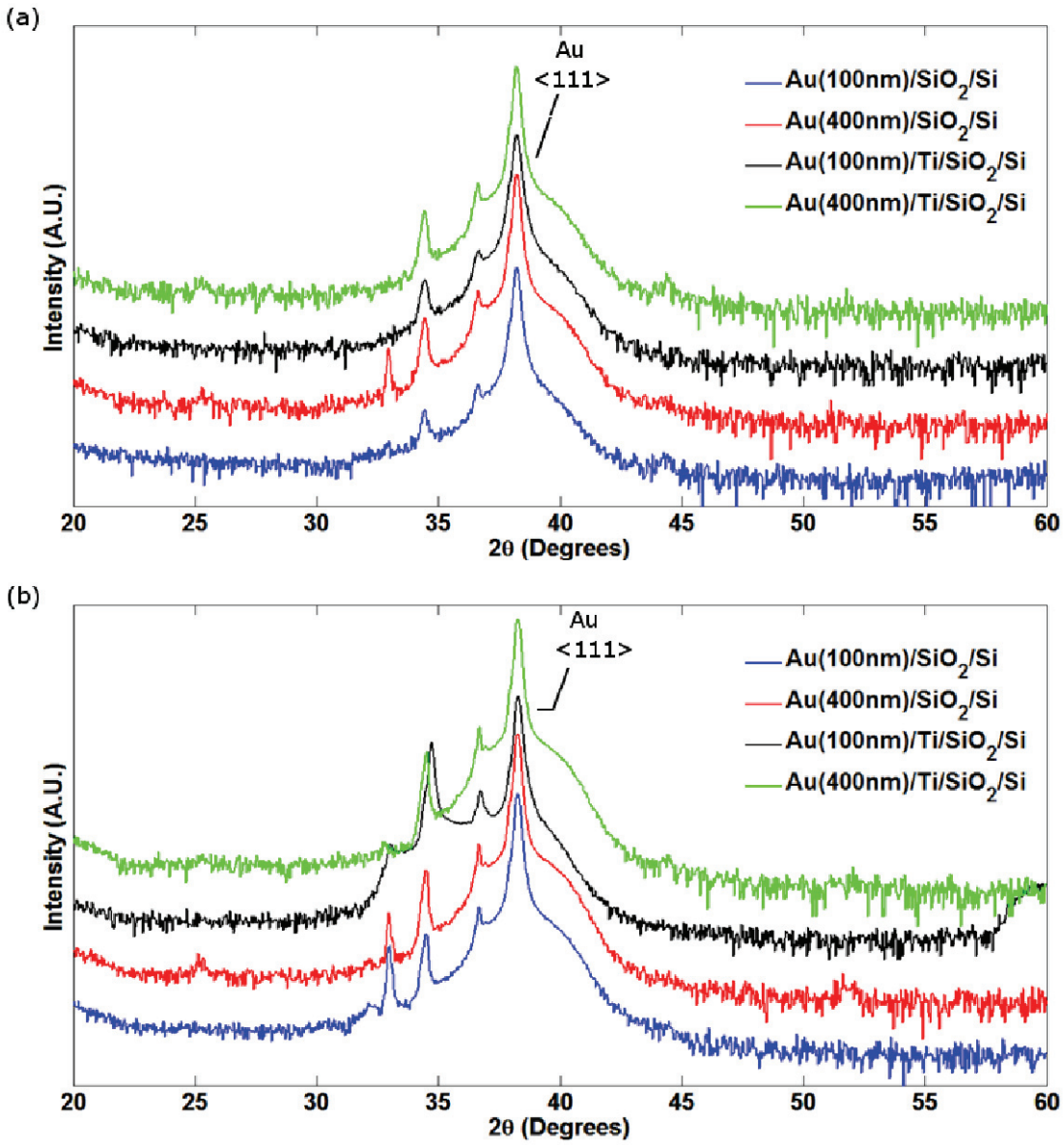



**Figure 4.3:** X-ray diffraction on (a) $SiO_2$/Si at room temperature, (b) $SiO_2$/Si annealed at 700$^o$C for 10 minutes.

observed for the thicker Au films (Figure 4.4b and 4.4c) with the blocking of grain boundaries being less effective presumably because of the depletion of diffusing Ti.

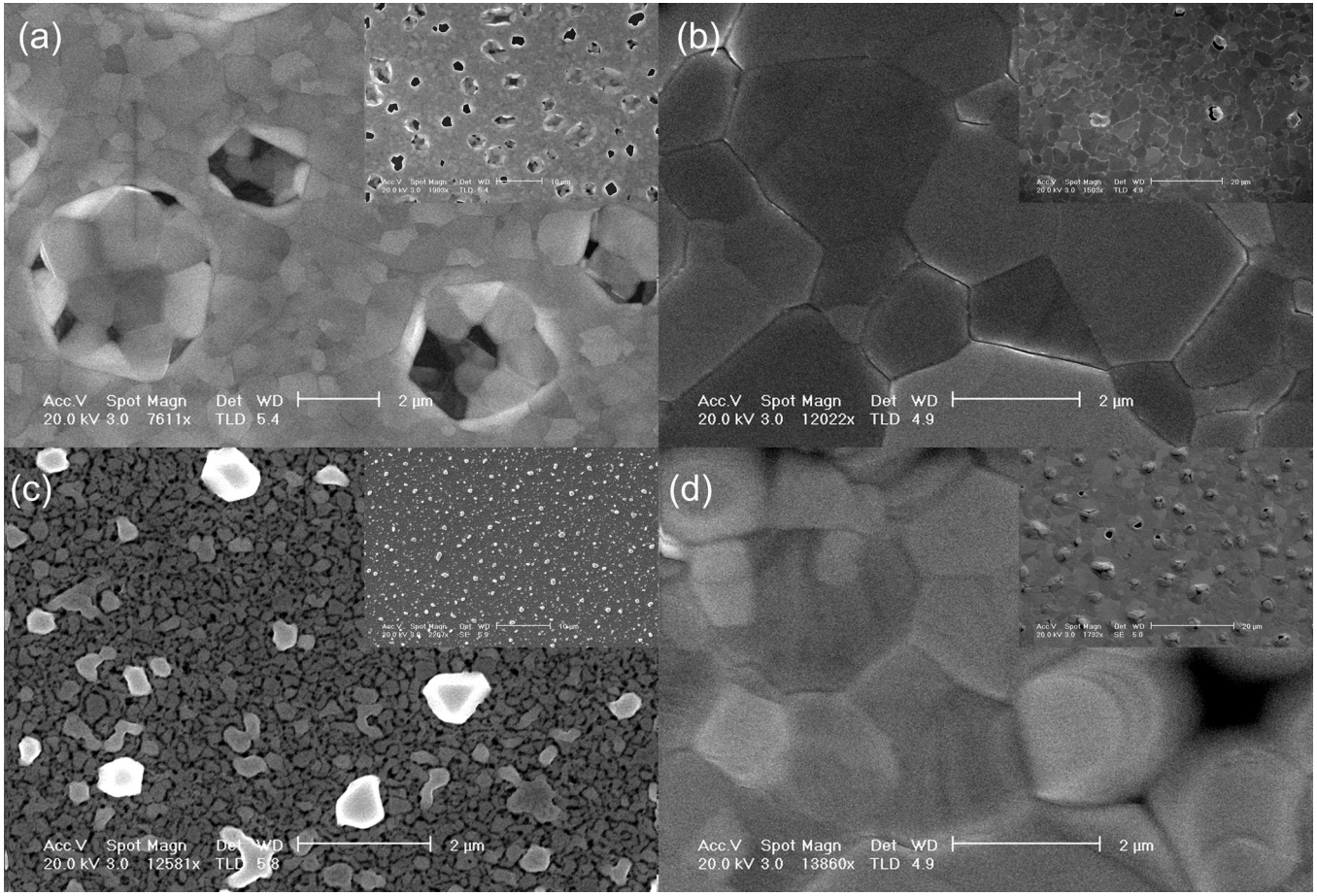



**Figure 4.4:** Scanning electron micrographs of electrodes consisting of: (a) Au(100nm)/$SiO_2$/Si, (b) Au(400nm)/$SiO_2$/Si, (c) Au(100nm)/Ti/$SiO_2$/Si and (d) Au(400nm)/Ti/$SiO_2$/Si after annealing.

### 4.4.3 Crystal structure and surface texture of Au on $TiO_2/SiO_2/Si$ substrates

To form the $TiO_2$ layer 2×40nm thick layers of Ti were deposited and oxidized in air. The deposition and oxidation - consisting of heating the sample from room temperature to 700$^o$C, using RTA and then ramping down to avoid thermal shock - were performed twice to be sure of complete oxidation of the Ti. A final thickness of 120 nm $Ti0_2$ was measured consistent with complete oxidation.

SEM images of the surfaces of the $Au/TiO_2$ and $Au/Ti/TiO_2$ samples are shown in figure 4.6 and comparing these with figure 4.4 it can be seen that there are fewer defects in the Au layer when a $TiO_2$ layer is included. In the case of the $Au(100nm)/TiO_2/SiO_2/Si$ and $Au(400nm)/TiO_2/SiO_2/Si$ samples, figures 4.6a and 4.6b, besides the decreased defect density observed, the growth of the Au crystallite faces is also reduced compared to those without the $TiO_2$ interlayer. In the $Au(100nm)/Ti/TiO_2/SiO_2/Si$ sample (figure 4.6c) although there is Ti diffusion, no significant interlayer reaction resembling that shown in figure 4.4c is observed. Instead, there are areas populated by smaller defects interspersed with areas with no defects. Finally, in the $Au(400nm)/Ti/TiO_2/SiO_2/Si$ sample (figure 4.6d) no large defects can be seen. However, higher magnification SEM examination, figure 4.7, reveals that grooving, whereby gold diffuses down grain boundaries, has taken place although, it is believed to a limited extent because of the diffusion of Ti in the opposite direction and formation of $TiO_2$ on the surface [83]. Contrary to the findings of Riekkinen et al. [131], we do not observe the cracks that appear in gold layers during annealing. It is further suggested that the absence of blistering in this sample is due to electrode stress reduction and adhesion improvement. Firstly, the $TiO_2$ interlayer has a thermal expansion coefficient value (9ppm/$^o$C), which lies between that of the Si substrate (3.2ppm/$^o$C) and the Au film (14.2ppm/$^o$C), making it an effective buffer layer for thermal

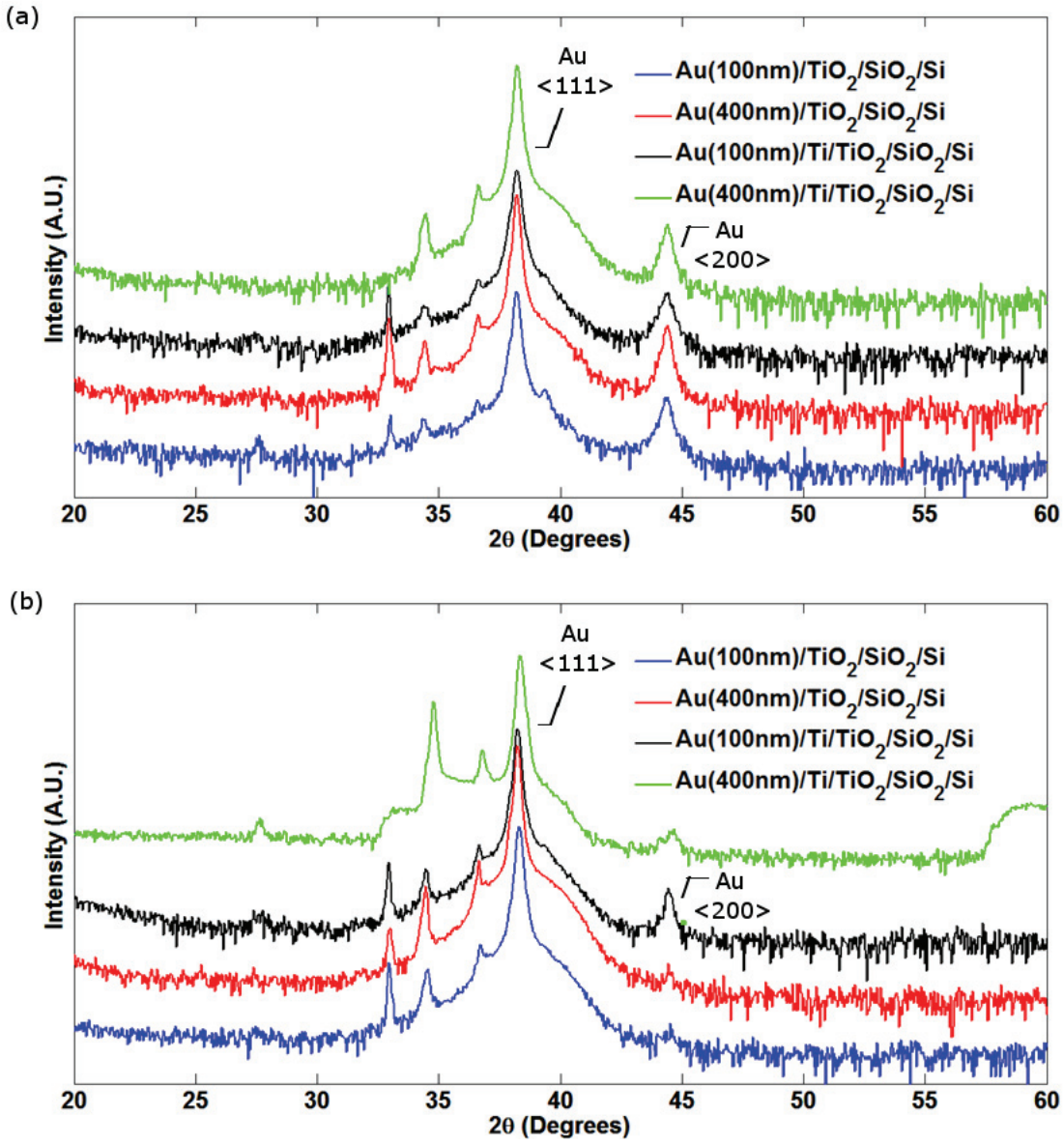



**Figure 4.5:** X-ray diffraction on (a) $TiO_2/SiO_2/Si$ at room temperature and (b) $TiO_2/SiO_2/Si$ annealed at 700$^o$C.

stress reduction [173], [172] and thus adhesion improvement. Secondly, Ti-$TiO_2$ inter-diffusion may improve adhesion [126] by forming more titanium oxides at the interface.

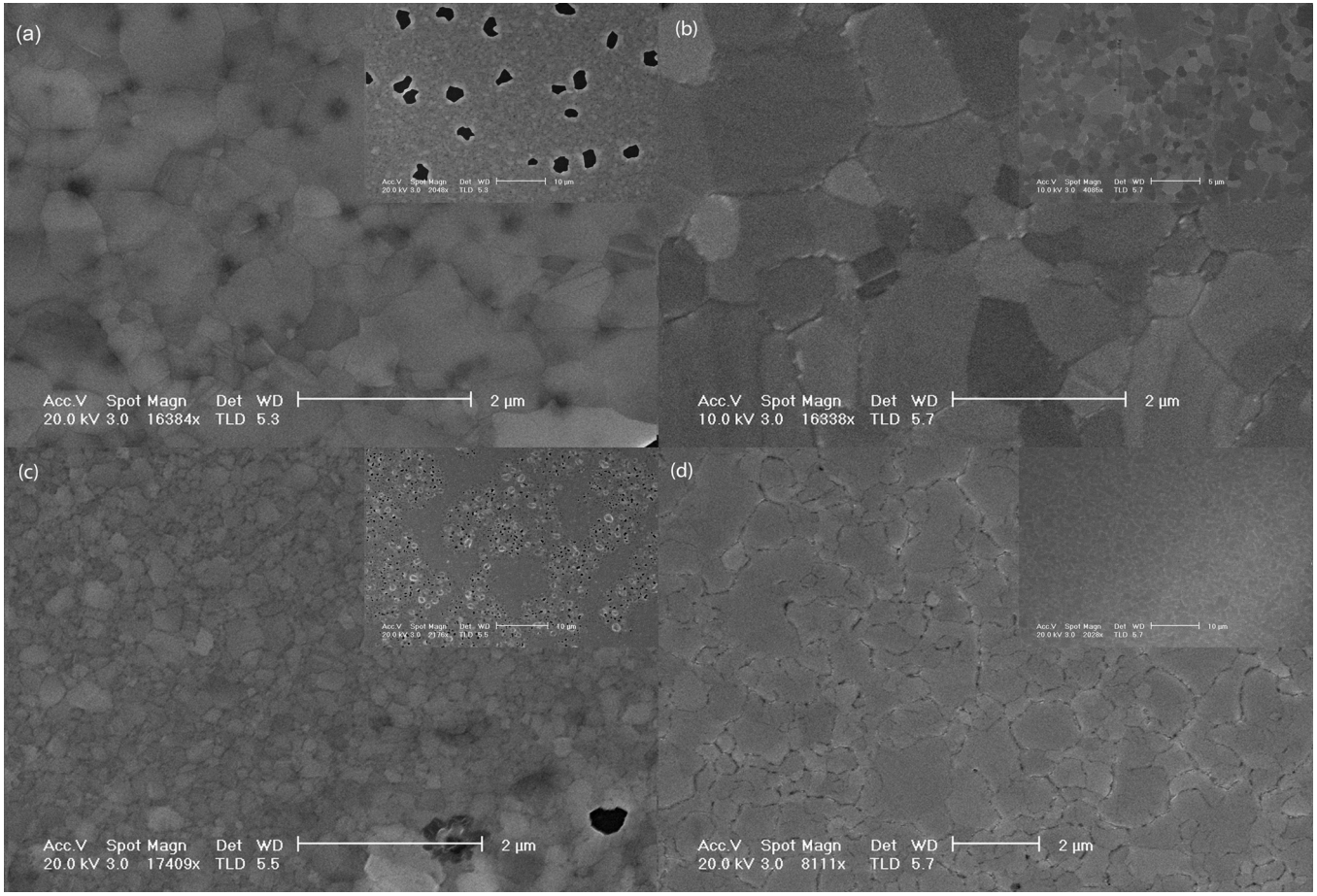



**Figure 4.6:** Scanning electron micrographs of electrodes consisting of: (a) Au(100nm)/$TiO_2$/$SiO_2$/Si , (b) Au(400nm)/$TiO_2$/$SiO_2$/Si, (c) Au(100nm)/Ti/$TiO_2$/$SiO_2$/Si and (d) Au(400nm)/$TiO_2$/$SiO_2$/Si after annealing.

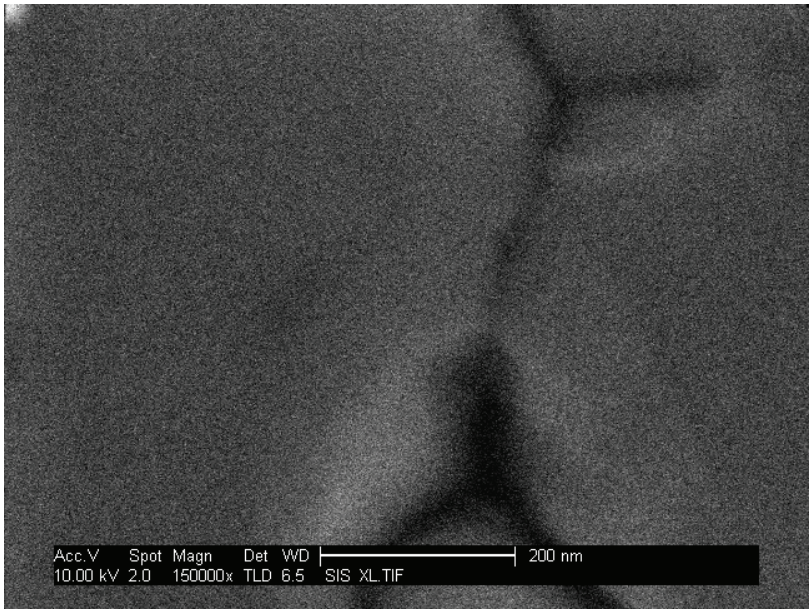



**Figure 4.7:** Scanning electron micrograph (close-up) of Au(400nm)/$TiO_2$/$SiO_2$/Si after annealing, showing grooves in the grain structure.

### 4.4.4 Preferred high conductivity electrode system for lead based devices operating at high frequencies

Several differences between the behavior of the Au-Pt-Ti and Au-Ti-$TiO_2$ electrode systems have been observed in the context of their suitability as high conductivity electrodes in high frequency devices and their capability for surviving the rigours of processing and acting as a template for growth of lead based ferroelectrics. For the Ti-Pt-Au system, adhesion is good except when thick layers are used and when the thin Ti layer is omitted as in the Pt(500nm)/Ti and Pt(100nm)/Au(200nm)/$TiO_2$ structures, respectively. However, following annealing all Au-Pt combinations have increased sheet resistance and in some cases despite Au being included, sheet resistance values greater than the conventionally

used electrode system - Pt(100nm)/Ti - are obtained. The resistance values in this system before and after annealing also lack consistency compared to Au-Ti-$TiO_2$. The lowest sheet resistance values are obtained with the Au-Ti-$TiO_2$ system and in particular Au(400nm)/Ti(7nm)/$TiO_2$ has low sheet resistance and good adhesion before and after annealing and a smooth, defect-free surface after annealing. It should be stressed though that although the Au-Ti-$TiO_2$ shows high conductivity the deposition of ferroelectrics onto Pt surfaces gives preferred orientation. For varactor applications the relative importance of these advantages and disadvantages is unclear.

## 4.5 PST ferroelectric on optimized electrodes

### 4.5.1 PST deposition

Thin film PST has been deposited, using a previously described process - see chapter 3 -, on the optimized Au(400nm)/Ti/$TiO_2$/$SiO_2$/Si electrode structure discussed in the previous section. Good crystallization with mixed orientation similar to that observed with a Pt bottom electrode was obtained - see figure 4.8 - with no sign of deleterious second phases. The highly preferred (111) orientation is generally not observed with such high crystallization temperatures but also included in the figure is the XRD trace for PZT deposited on the same electrode structure which shows that with the lower crystallization temperature of 530$^o$C a highly preferred (111) orientation is obtained.

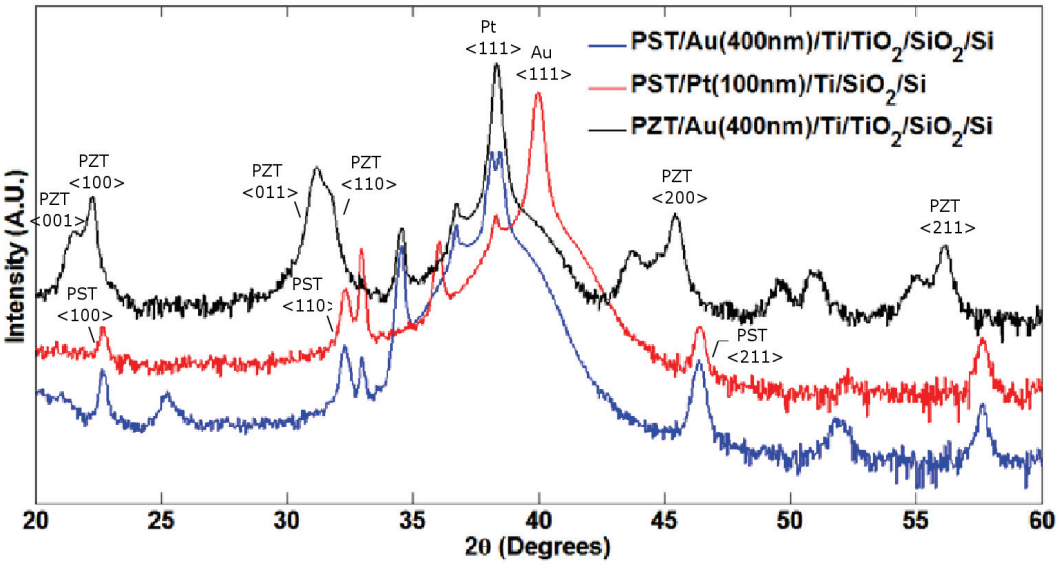



**Figure 4.8:** X-ray diffraction of PST(300nm)/Au(400nm)/Ti/$TiO_2$/$SiO_2$/Si, PST(300nm)/Pt(100nm)/Ti/$SiO_2$/Si and PZT(720nm)/Au(400nm)/Ti/$TiO_2$/$SiO_2$/Si after annealing.

### 4.5.2 PST device fabrication

Thin film PST varactors - seen on figure 4.9 - have been fabricated using the above optimized Au/Ti/$TiO_2$/$SiO_2$/Si electrode structure. The deposition of the Au/Ti/$TiO_2$ electrodes is described in more detail in Appendix C-2. The device processing details have been reported in chapter 3. By combining these with micromachined inductors, a range of band reject RF switches have also been fabricated. These are described in more detail in chapter 5, but measurements have been placed here to demonstrate the improved performance achieved when using the Au(400nm)/Ti/$TiO_2$ bottom electrode system instead of Pt, for RF devices.

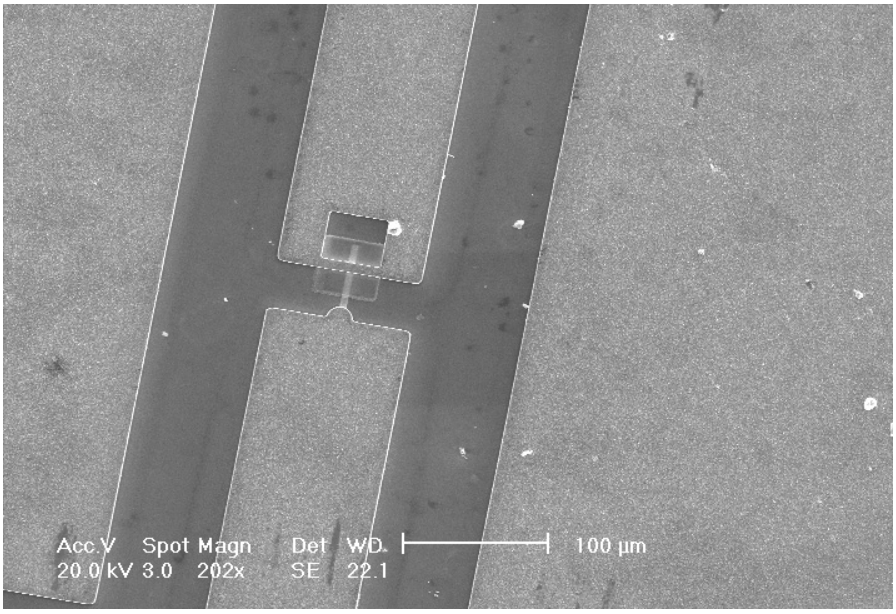



**Figure 4.9:** A varactor fabricated using PST as the voltage tuneable dielectric and Au(400nm)/Ti(7nm)/$TiO_2$/$SiO_2$/Si for the bottom electrode. This demonstrates that the interface between electrode layers is sufficiently strong that devices can be processed.

It has been found that the effect of the improved bottom electrode on varactor performance, as measured by for example device Q, becomes more pronounced with increasing frequency. Figure 4.10a compares the zero bias Q values obtained using Pt(200nm)/Ti/$SiO_2$/Si and Au(400nm)/Ti/$TiO_2$/$SiO_2$/Si bottom electrodes and as can be seen, at 3 GHz, there is almost a factor of 10 difference - of the same order as the relative DC sheet resistances of the two. The improved Q in the band reject RF switch leads to a higher insertion loss ($S_{21}$) at resonance, figure 4.10b, and almost a factor of 10 decrease in transmitted signal power at zero bias, whilst maintaining a high transmission state on application of a DC bias to the varactor, which shifts the resonance to higher frequencies. The fact that devices have been

fabricated also confirms the tape test result that the interface between electrode layers is sufficiently strong to avoid delamination.

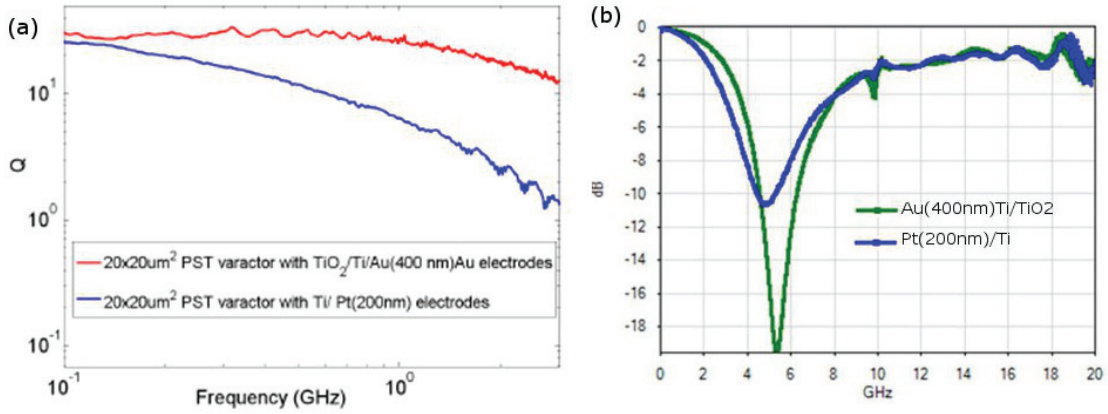



**Figure 4.10:** RF performance of Au(400nm)/Ti/$TiO_2$/$SiO_2$/Si and Pt(200nm)/Ti/$SiO_2$/Si bottom electrode configurations. (a) Quality factors of 20um×20um PST ferroelectric varactors and (b) Insertion loss of a PST ferroelectric band reject switch.

## 4.6 Conclusion

The resistance to degradation during high temperature annealing of a variety of bottom electrode structures incorporating Au have been investigated for implementation in ferroelectric varactors. The sheet resistance of the electrode is of great significance for device performance, but adhesion and surface quality are also important as defects and hillocks can cause electrical shorts, high loss or even low electric field dielectric breakdown in the generally used metal-insulator-metal (MIM) device structures. The effect of Ti adhesion layer diffusion through the Au

grain boundaries on sheet resistance and surface texture of the film was investigated. A $TiO_2$ interlayer barrier and increased Au thickness were found to reduce the surface defect density. A defect-free electrode structure with low resistance has been established and thin film PST ferroelectric tunable varactors and band reject switches with improved performance have been fabricated. For very high performance ferroelectric varactors, the Au/Ti/TiO2 electrode system might allow for further improvements of of BST varactor quality factors achieved with the Pt/Ti and Pt/Au/Pt/TiO2 system [170], thus increasing the competition between ferroelectric and GaAs semiconductor varactor technologies.

Chapter 5

# Frequency Tunable Microwave Devices

## 5.1 Introduction

In this chapter, a range of designed, modeled and fabricated tunable RF devices utilizing thin film PST ferroelectric tunable varactors are presented. The devices investigated are novel and as such the investigation concentrates on the device concept, design, fabrication and analysis. Although some minimal optimization of the performance of the devices is performed, some of the well-used commercial techniques for improving electrical performance such as i.e. thick Au or Cu plating have not been pursued. The performance of these devices is still away from commercial specifications, but there is large scope for improving the performance by improving the tunable dielectric properties using different materials such as BST, alternate deposition techniques that may provide better material properties such as PLD, doping, decreasing the metalization losses by plating electrical connections and optimizing design.

## 5.2 PST varactor - inductor (LC) resonant switch

### 5.2.1 Ferroelectric switch background

RF switches are used to route the RF signals to particular waveguides and their most important attributes consist of their isolation, insertion loss, impedance/return loss, switching speed and power handling capability. Whereas, RF MEMS switches [130] can offer almost wideband high isolation, low insertion loss and high power handling capability, they suffer in terms of switching speed, reliability and life-cycle. PIN diode, field effect transistor (FET) or even hybrid solid-state switches are very popular as despite their moderate isolation and high insertion loss at high frequencies compared to MEMS, offer fast switching speeds, low cost and long life for most of the current wireless applications. Thin-film ferroelectrics like BST and PST have been used for the realization of electric field tunable ferroelectric varactors [170], [36], which can in turn be used in tunable microwave components and even in integration with MEMS to provide for new operation modes for RF switches [141]. Although integration through flip-chip bonding or soldering of ferroelectric varactors in FR4 substrates has been frequently reported [89], [107], [20], there have been fewer reports of fully monolithic integration [74], [148], which can present miniaturization advantages and minimize parasitic inductances due to mounting of external components. Recently, a new type of a ferroelectric BST varactor-tuned resonant switch was proposed for frequencies higher than 35 GHz [151], [154], offering an alternative to solid-state RF switches for fast switching speed wideband applications, showing good isolation, but suffering in terms of insertion and return loss.

In this section, the performance limitations and restrictions of RF switches integrating ferroelectric varactors are discussed and a narrowband frequency mode

of operation is proposed to allow for improved switch performance with the use of high Q inductors. The design, simulation and fabrication of C-band, resonant switches on silicon integrating thickly-plated free-standing inductors and sol-gel PST tunable varactors, are presented. For analysis and optimization purposes, each section of the device is also investigated separately using test structures. Finally, electronic computer-aided design (CAD) software is used to simulate the performance of cascaded switches and the use of current state-of-the-art materials.

### 5.2.2 Ferroelectric switch design

Similar to a CPW MEMS electrostatic switch, the ferroelectric switch design consists of a ferroelectric varactor shunting a CPW and thus controlling the signal-to-ground isolation. In both designs, due to its physical length, the capacitor also includes a small parasitic inductance, giving rise to a self-resonance of the switch. MEMS switches achieve almost wideband operation out of this self-resonance, but the implementation of ferroelectrics in such a design, introduces some practical limitations. Ferroelectric varactors are not very well suited - as are MEMS electrostatic capacitors - to wideband switch applications as these require extremely high $C_{ON}/C_{OFF}$ ratios, without which the insertion loss can be high [151]. Although technology improvements in the ferroelectric tunability research may close the gap - especially in BST thin films with $\sim$90% tunability reported [122] - there will always be the limitation due to a known trade-off between dielectric tunability and dielectric loss in ferroelectrics [162].

Due to this restriction, a narrowband mode of the switch implementing a high Q inductor is proposed, which trades bandwidth of operation with tunability required by exploiting the self-resonance of the switch. The complete proposed equivalent lumped element network for the RF switch can be seen in figure 5.1

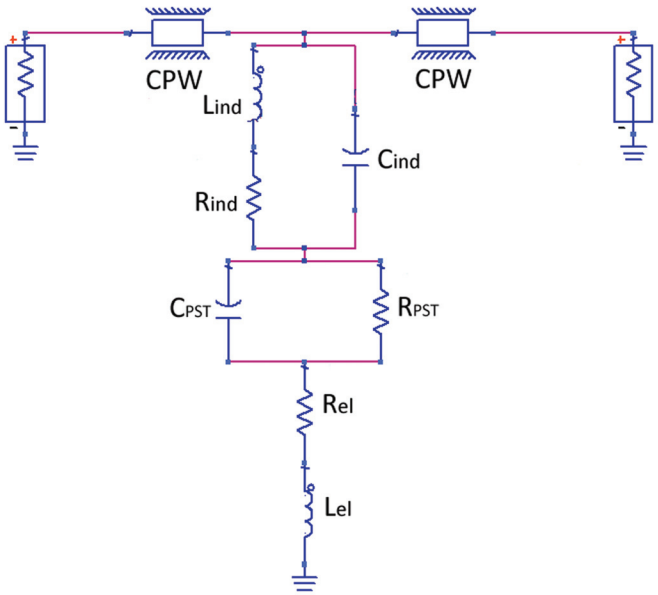



**Figure 5.1:** The proposed lumped element equivalent network for simulation of a narrowband PST ferroelectric RF switch integrating a high Q inductor.

and is divided in three main sections. The first section is the series CPW transmission line, the second is the shunt meander micromachined inductor comprising of inductance $L_{IND}$, resistance $R_{IND}$ and inter-winding capacitance $C_{IND}$ and the third is the shunt PST varactor comprising of electrode resistance and inductance $R_{EL}$, $L_{EL}$ and PST ferroelectric intrinsic capacitance and resistance $C_{PST}$ and $R_{PST}$. The inductor-to-ground parasitic capacitance is intentionally ignored as the inductor is micromachined.

The principle of operation is that at zero bias, the device resonates at a specific frequency where there is maximum insertion loss isolation of the switch - and at an increased bias, the resonance of the device shifts - due to the dielectric constant decrease in the ferroelectric minimizing the insertion loss of the switch, always

with reference to the same operating frequency. The isolation of the resonant switch depends on the Q of the resonance of the structure, which itself is linked to the quality factors of its constituents, the PST varactor and the micromachined inductor. At high frequencies, it is expected that increased dielectric losses and electrode resistive losses will degrade the performance. For this reason, although it is theoretically possible to design narrowband devices to operate at even higher frequencies, the C (4-8 GHz) and X (8-12 GHz) frequency bands were selected for device operation, as comparatively good quality factors can be achieved for both Si MEMS inductors and ferroelectric varactors. The lumped component design was based on the ideal LC resonant circuit equation 5.1. Multiple combinations of different area PST ferroelectric varactors and inductors were realized, with capacitances and inductances varying from 0.2 pF - 6 pF and 0.4 nH - 2 nH respectively. To achieve such inductance values, the silicon bulk micromachined meander topology was favored instead of surface micromachined and out of plane inductors, because of its fabrication simplicity  no surface micromachining is required - and relative high quality factors reported, especially when the inductors are plated thick [82]. The Sonnet EM Suite was used to design and simulate the meander inductors.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5.1}$$

At the point of resonance, single values can be obtained for all the lumped components of the equivalent network. For a wideband fit of the measurements though, because the PST varactor and the meander inductor equivalent circuit values are intrinsically frequency dependent, this results in inadequate wideband fitting on the switch RF measurements. Since the S-parameter measurements of the whole switch do not provide enough information to calculate all these frequency-dependent component values, each section of the switch  the CPW, PST varactor

and micromachined inductor was designed, fabricated on the same wafer and then measured independently to give insight not only on the RF performance of the switch but on its components as well. The return loss when the switch is ON is also important so that very little power is reflected back and the CPW dimensions were chosen so as to have an impedance of approximate 50 Ohms on the silicon substrate. In this respect, the signal line width selected was $W_S = 0.1$ mm, and the gap was $W_G = 0.08$ mm.

### 5.2.3 Fabrication process

Devices were fabricated on high resistivity (>10 KΩ/cm), thermally oxidized 4-inch Si wafers using process steps described previously (Appendix C-1, C-2), with the addition of a deep reactive ion etch (DRIE) step to etch through the Si substrate and fully release the inductors. Patterning of the 280nm thick ferroelectric PST enabled access on the bottom electrode and therefore the application of electric field on a single varactor. To ensure low metalization losses, 400 nm Au on $TiO_2$ was chosen as the bottom electrode and the inductor thick nickel plating step was increased to 16um with a Au seed layer of 200nm. A 3D schematic of the PST varactor and the whole shunt section of the switch are shown on figure 5.2. SEM micrographs of the fabricated switch and test structures are shown in figure 5.3.

### 5.2.4 Measurements and Simulations

S-parameter measurements from 500 MHz to 20 GHz with 2000 frequency points were obtained from an Agilent E8361A vector network analyzer (VNA) using a Cascade Microtech Summit 12000 automatic probe station. A short-open-line-

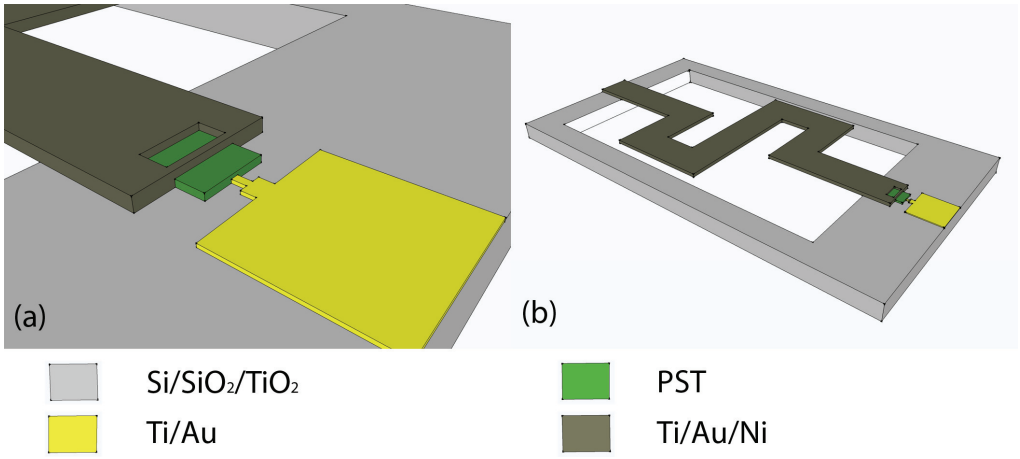



**Figure 5.2:** 3D schematics of : (a) the ferroelectric varactor and (b) the shunt section of the switch.

through (SOLT) calibration using a reference substrate was realized to bring the reference plane to the probe tips and 1.5 KHz was used as the IF. To avoid photovoltaic effects in the high resistive silicon the microscope light was turned off during measurements and sufficient time was allowed for measurement stabilization. DC Bias was introduced through the use of bias-tees and the design of the switch allows for DC bias application through the signal and ground port of one of the two VNA probes. The S-parameter measurements of 3 different varactor size combinations with the 100 um width inductor - shown in figure 5.3a, operating at different sections of the C and X band, can be seen on figure 5.4. Due to calibration error, a small notch can be seen at ∼10 GHz in the $S_{21}$ measurements and this was ignored in comparison with simulations. At higher frequencies, the quality factor of the switch is smaller due to the higher PST dielectric loss and total electrode metalization losses. It was confirmed from the equivalent network simulations that the increase of bandwidth of the resonance occurs when there is deterioration due to the above reasons. From these, the 7 GHz switch was chosen

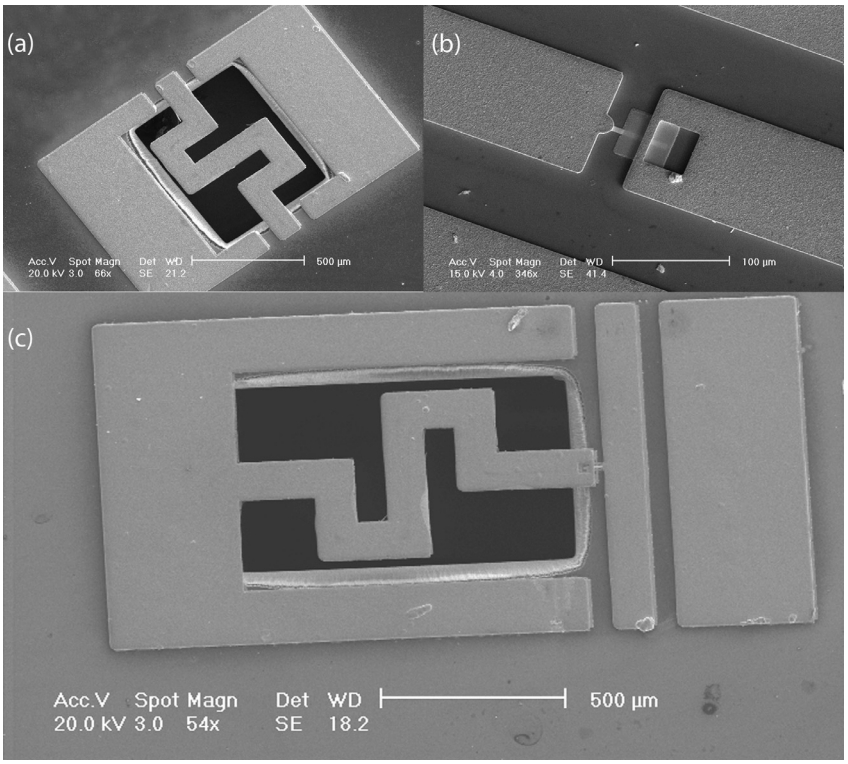



**Figure 5.3:** SEM micrographs of fabricated : (a) 100um width meander micro-machined inductor, (b) 25 um2 PST varactor and (c) complete PST L-C shunt switch.

for further test structure analysis and device biasing.

#### 5.2.4.1 Test Structures

After measuring the capacitor and inductor test structures, their quality factor - shown on figure 5.5 - was extracted by dividing the imaginary part to the real part of the impedance. The frequency dependent values for $R_{EL}$ and $L_{EL}$ of the capacitor electrodes were extracted separately from a 'short' test structure

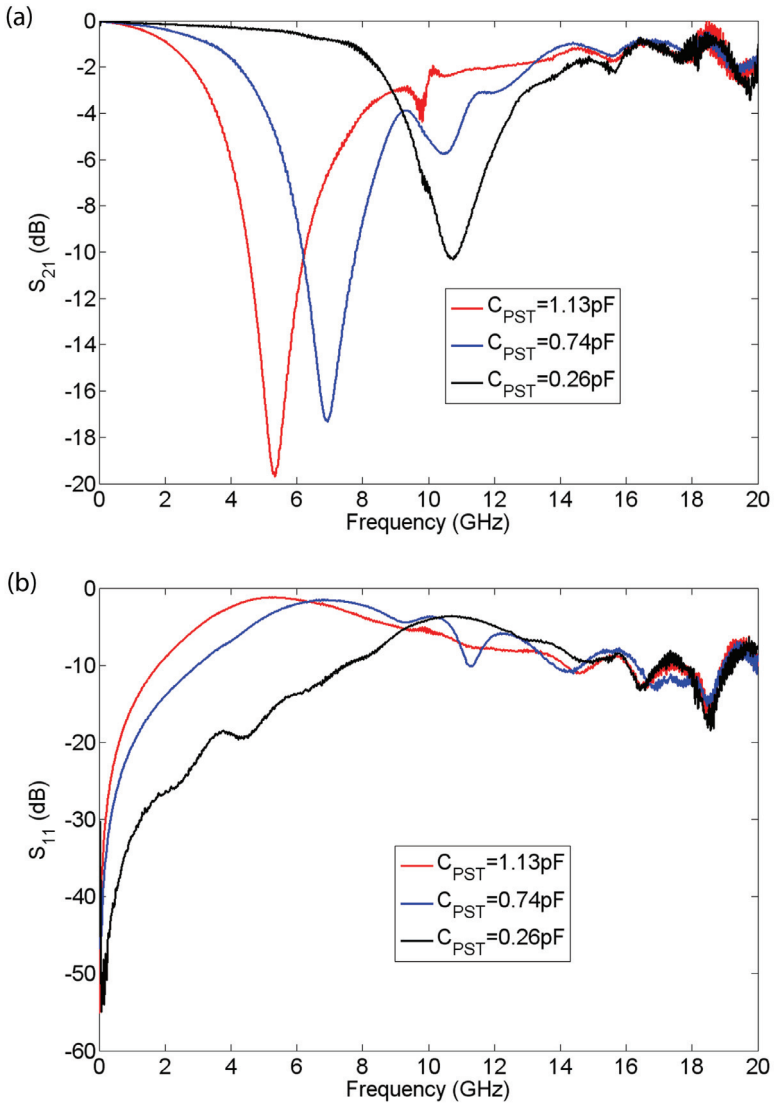



**Figure 5.4:** S-parameter (a) Insertion and (b) return loss measurements of 3 different varactor integrations with a 100um width inductor, at no bias.

(Appendix A-2). Extraction of the intrinsic PST electrical properties was realized using previous developed techniques (chapter 3)[36]. The quality factor of the

inductor before micro-machining is also displayed for comparison. As similarly reported [82], the bulk micro-machining of the inductor on very high resistive (>10 KΩ/cm) silicon substrates, slightly increases the quality factor and shifts it to the higher frequencies by removing the inter-winding and ground-coupling capacitance. This step would also enable the parasitic removal and significant quality factor improvement of inductors in lower cost, low resistivity Si. The comparatively high Q measured value of ∼25 at 7 GHz can be mostly attributed to the thick nickel plating, which minimizes resistive losses.

The extracted microwave properties of the PST thin film were found to be similar tan$\delta$=∼0.03 at 0.5GHz and tan$\delta$∼0.1 at 14 GHz - to other sol-gel reported values for PST and BST [36], [65], although still lacking compared to achieved PLD BST dielectric loss values [170] and these BST values are used to simulate the possible performance of the device on a later section. At the low GHz region, there is an increase in the quality factor when electric field is applied and the resonances observed in the PST loss are due to acoustic resonances generated in the PST due to electrostriction [43]. Also, due to the design of the capacitor requiring values in the pF region and ease and accuracy in feature aligning, the bottom electrode of the MIM stack has a width of 5-20 um and this introduces an undesirable series resistance ($R_{EL}$), which degrades the overall capacitor quality factor. Although, 400 nm of Au was chosen as bottom electrode to resolve the issue, the series resistance of a 5um × 5um capacitor was still found to be >1 Ω at GHz frequencies and this common resistance problem on small ferroelectric varactors has recently given rise to layout optimization investigations [111]. Biasing measurements reveal that a varactor tunability of approximately 55% can be achieved under an electric field of 714 kV/cm.

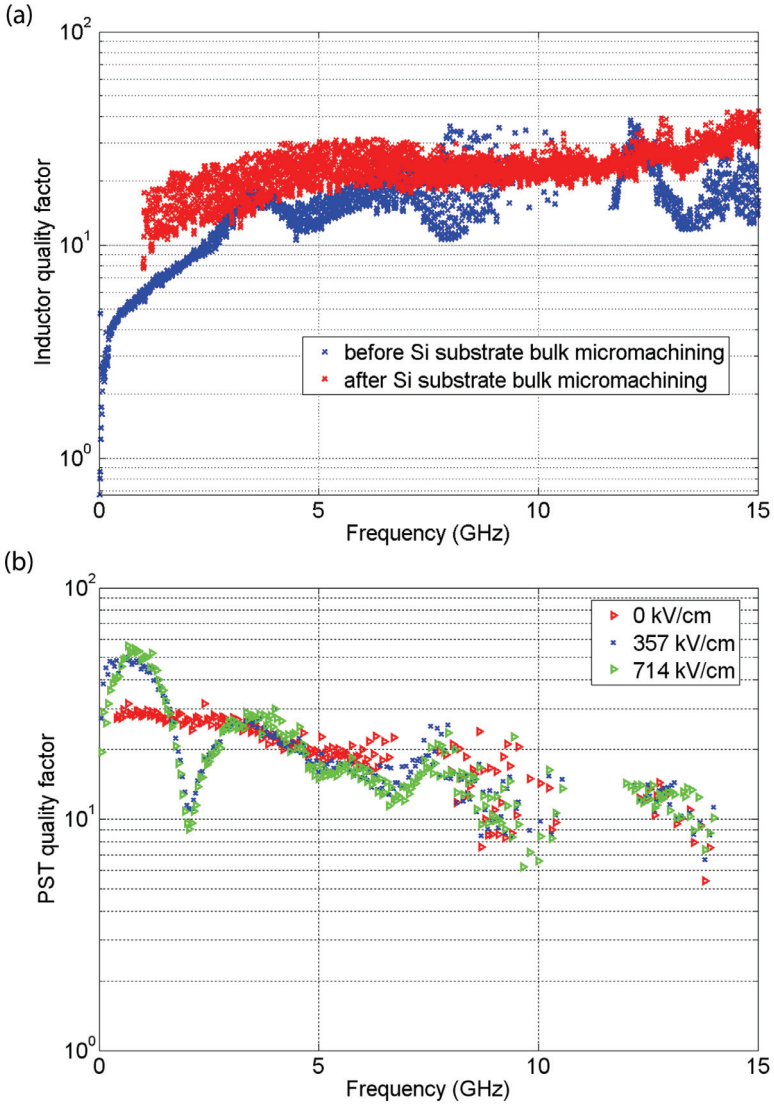



**Figure 5.5:** Quality factors of (a) inductor and (b) PST dielectric extracted from S-parameter measurements of the test structures.

#### 5.2.4.2 Switch

The measured transmission parameters ($S_{21}$) and reflection parameters ($S_{11}$) for the implemented 7 GHz switch are presented on figure 5.6. When electric field

is applied, the device is continually tunable with a minimum insertion loss of $\sim$ 1.5 dB at 893 kV/cm and return loss of approximately 10dB. Also, the return loss for the zero-bias state at 7 GHz is not exceeding 1.4dB, making blocking the signal at that frequency region possible. In this case, the decreased quality factor of the resonance originating from the reduction of the varactor quality factor and resistive losses at higher frequencies - when the electric field is increased, favors the performance of the switch, with the out-of-resonance insertion loss becoming smaller. Good agreement between the equivalent lumped network simulations and measurements has also been achieved. The lumped component values extracted from test structures were frequency-dependent and from these, only the values at the point of resonance were used in the Agilent Design System simulation to fit the CPW LC shunt switch and a good fit was achieved. It can be observed from the graph, that the out-of-resonance part is not as well fitted and this is due to the frequency dependence of the lumped element values of the equivalent network. Table 5.1 lists all the lumped component values of the equivalent network at the point of resonance for 0, 5, 10, 20 and 25 Volts applied. Except from the expected increase in the dielectric loss of the PST with increasing frequency, the same was observed for the resistive components $R_{IND}$ and $R_{EL}$. This observed increase of resistance with frequency can be attributed to skin and proximity effects due to the time-varying electromagnetic field, as previously reported and analytically calculated in inductors [149] and includes the DC resistance of the conductors, resistances due to skin effect, eddy current excitation and dielectric loss in the substrate - where applicable. The inductance value of the inductors is generally considered constant with frequency as it is mainly decided by the inductor geometry, but in practice it can slightly vary at high frequency [81], as also confirmed by the Sonnet model simulations. The slight $C_{PST}$ decrease of tunability extracted, compared to the single test structure is attributed to the application of the electric field through the inductor and the fabrication tolerances

throughout the wafer.

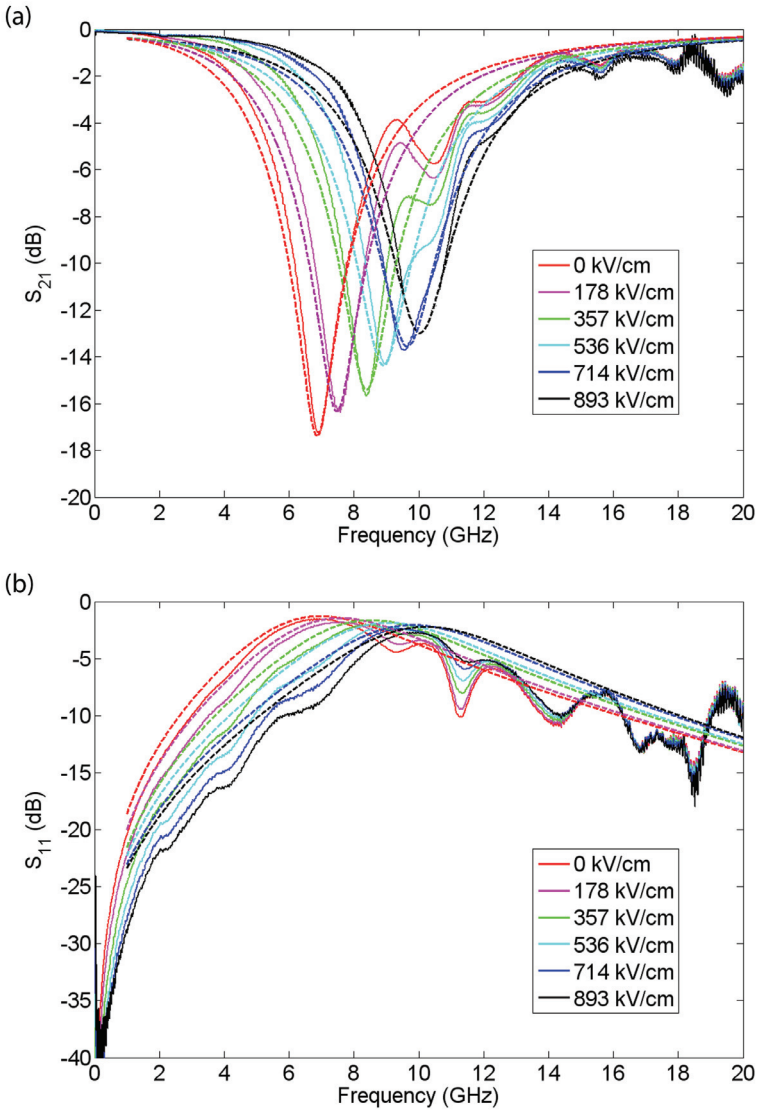



**Figure 5.6:** Biased (a) insertion and (b) return loss measurements (normal) and simulations (dashed) of 7GHz switch, up to an electric field of 893kV/cm.

**Table 5.1:** Table of equivalent network lumped component values for the simulation of the 7GHz switch at point of resonance for 0, 10 and 20 Volts applied.

| Electric field (kV/cm) | $f_r$ (GHz) | $C_{IND}$ (fF) | $L_{IND}$ (nH) | $R_{IND}$ ($\Omega$) | $C_{PST}$ (pF) | $R_{PST}$ ($\Omega$) | $R_{EL}$ ($\Omega$) | $L_{EL}$ (nH) |
|---|---|---|---|---|---|---|---|---|
| 0 | 6.94 | 38 | 0.62 | 1.3 | 0.74 | 700 | 1.1 | 0.08 |
| 178 | 7.56 | 38 | 0.62 | 1.4 | 0.62 | 670 | 1.2 | 0.08 |
| 357 | 8.38 | 38 | 0.61 | 1.5 | 0.5 | 650 | 1.2 | 0.07 |
| 536 | 8.93 | 38 | 0.61 | 1.6 | 0.44 | 590 | 1.3 | 0.07 |
| 714 | 9.57 | 38 | 0.6 | 1.7 | 0.38 | 560 | 1.3 | 0.06 |
| 893 | 9.99 | 38 | 0.6 | 1.8 | 0.35 | 540 | 1.3 | 0.06 |

#### 5.2.4.3 Ferroelectric tunable material considerations for improved switch performance

The ideal tunable material for improved performance of this type of device is based on the nature of application. A tunable material with a higher tunability for the same dielectric properties, would realize a device with lower insertion loss, as the two different capacitance value switches of figure 5.4 suggests. On the other hand, improved isolation and resonance quality factor of the device would follow the use of current state of the art tunable materials with very low loss, as well as from better conductors like copper, silver or even thicker gold - if the fabrication allows for their integration. As previously reported [20], [154], a wide improvement of performance would result from cascading multiple devices, albeit at the expense of additional series insertion loss and device area as the transmission line length between the repeat of the shunt networks is optimal at quarter wavelength ($l_{CPW} \sim$

$\lambda/4$). Simulations of the above possible improvements were realized and figure 5.7 shows the simulated switch performance. In case (a), the presented 7 GHz original PST switch is cascaded in series with itself. Secondly the performance of a single switch is simulated as before but the tunability of the dielectric is changed to ∼90% [122]. Finally, the simulation of the single switch is repeated but the dielectric loss is changed to 1% [170] regardless of frequency. Table 5.2, summarizes the results in terms of switch performance. In these simulations the switch design and fabrication capacitor area, interconnects, inductor, CPW and metal conductors are kept identical to the presented switch and so further improvements can be implemented by better inductor and varactor design to minimize resistive losses [111] and even the introduction of a $SiO_2$ layer surrounding the varactors [178] for increased varactor dielectric strength, which can lead to increased varactor tunability. The simulations clearly demonstrate, that this type of narrowband switching device largely benefits from the implementation of a ferroelectric with as high tunability as possible, thus reducing the switch insertion loss.

**Table 5.2:** Summary of simulation results in terms of switch performance and area.

| | Isolation (dB) | Insertion loss (dB) | Return loss (dB) | Area ($mm^2$) |
|---|---|---|---|---|
| Single switch Measured | 18 | 1.5 | 10 | 0.6 |
| Cascaded simulation | 38 | 2.4 | 16 | 4 |
| Simulated ∼90% tunability | 18 | 0.5 | 19 | 0.6 |
| Simulated ∼1% loss | 20 | 1.8 | 6 | 0.6 |

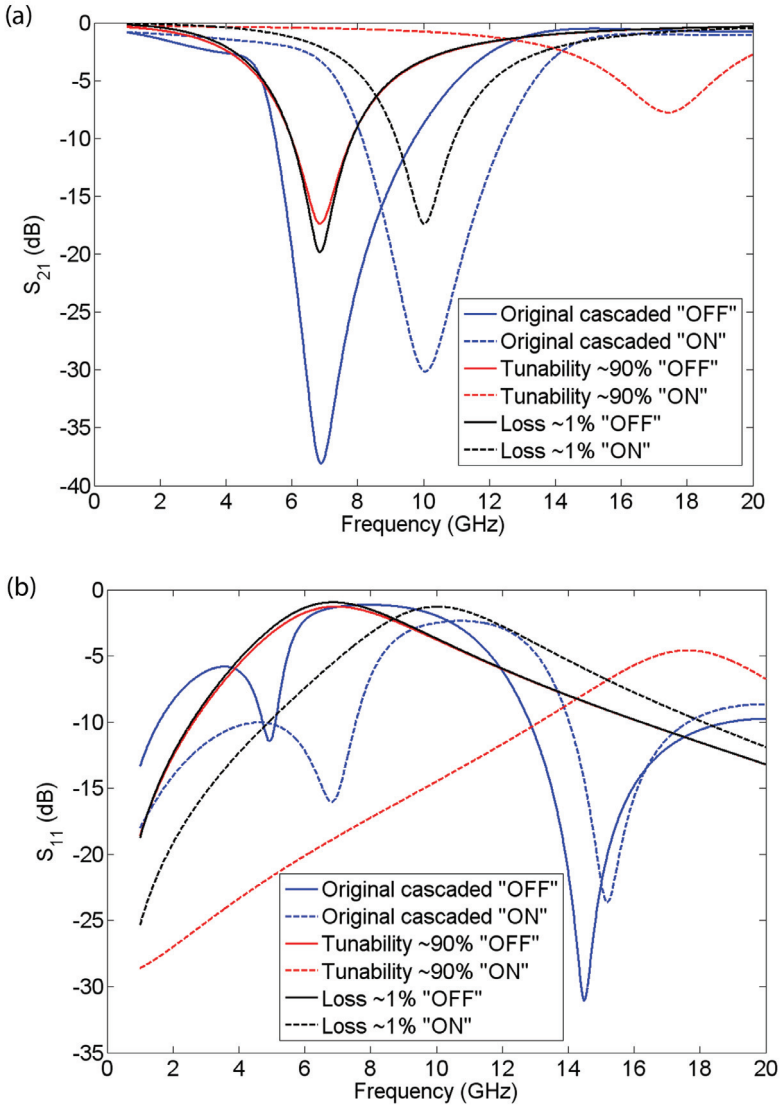



**Figure 5.7:** Simulated (a) insertion and (b) return loss of series cascaded (double) 7GHz switch, single 7GHz switch with dielectric tunability ∼90% and single 7 GHz switch with constant dielectric loss ∼1%.

### 5.2.5 Conclusion

The principle of monolithic integration of ferroelectric varactors with high Q inductors in order to achieve narrowband ferroelectric RF switches, within the limits of ferroelectric thin film tunability is discussed and demonstrated for a single stage 7 GHz resonant switch and an insertion loss of ∼1.5 dB, isolation of ∼18 dB and return loss of ∼10 dB have been achieved. The limitations of this type of device are discussed. As the proposed switch performance is still a long way from commercial requirements, further improvements in performance with the use of state of the art tunable materials and cascaded device design are proposed and simulated.

## 5.3 Band-stop Resonators and Filters with a CPW defected ground structure

### 5.3.1 Band-stop filters background

High frequency band operation and UWB systems can offer a solution by naturally offering more frequency spectrum and the ability to share spectrum with other users, respectively. However, the frequency spectrum, as a resource is valuable and limited. It is constantly being crowded by several applications and devices, meaning the desired frequency of operation can be full of un-wanted signals. Bandstop filters or notch filters block unwanted signals, especially for wideband applications. Moreover, tunable microwave filters have become even more critical [54],[143], for the requirements of recent wireless communications.

Periodic structures such as photonic bandgap (PBG) [139] and defected ground

structures (DGS) [86] for planar transmission lines have drawn great interest due to their great potential applicability. PBG research was originally established in the optical fields, but the photonic bandgap structures can be applied to wide frequency ranges including the microwave frequency band by properly scaling the dimensions. A periodic photonic bandgap structure, is known to provide rejection of certain frequency bands, i.e., bandgap or stopband effect [127]. However, it is difficult to use a PBG circuit for the design of the microwave or millimeter-wave components due to the difficulties in finding of its equivalent circuit and parameters [119]. Similar to PBG, the DGS for a transmission line has etched defects in the metallic [66]. Since an etched defect of the ground plane disturbs the shielded current distribution in the ground plane, the DGS with a periodic or non-periodic shape provides a rejection band in some frequency range due to increasing the effective inductance of a transmission line. This disturbance can change characteristics of a transmission line such as line capacitance and inductance [4], [182], [87].

Transmission lines combined with the periodic structures have a finite pass and rejection band like low pass filters (LPF) , while the standard transmission lines show only the simple transmission characteristics over broadband. Therefore, this type of periodic structure exhibits frequency regions in which electromagnetic waves cannot propagate [62] and a direct application of such frequency selective characteristics is in microwave filters [139], [67], [15]. Having a real uniplanar, 1-D structure, periodic structures for CPW can be realized and fabricated with ease on the same plane. Recently, the characterization and fabrication of a new compact CPW design with defected ground structure on RT/Duroid 6010 substrate, formed by a pair of meandered slotlines on the ground, was presented [63]. The resonant and coupling characteristics were also described. The following section presents the novel monolithic integration of sol-gel PST varactos with CPW DGS structures for the realization of tunable resonators and bandstop filters on silicon. The use

of the tunable ferroelectric varactors in these devices, enables the tuning of the fabricated resonators and 3-pole bandstop filters.

### 5.3.2 Design of tunable bandstop resonator and filter

The design and simulation of the defected ground band stop devices (section 5.3) was done in Herriot Watt university by Dr. Young-Hoon Chun and Prof. Jia-Seng Hong. The schematic diagram of a resonator with a CPW defected ground structure, is depicted in figure 5.8(a). In the figure, W is the width of the CPW line, S is the CPW signal to ground gap and $\alpha$ is the position where the PST varactors are loaded. It is known that the equivalent L-C components of the defects, seen in 5.8(b), give rise to form a band rejection characteristic, in other words, a cut-off frequency and rejection for a certain frequency band [70], [4]. The slotted resonators in each ground plane are both coupled with the CPW and their resonance frequency is decided by the total slotted inductor length, $L_{slot}$ in equation 5.2.

$$L_{slot} \sim 2L_1 + L_2 + W_1 \tag{5.2}$$

, where $L_1$, $L_2$ and $W_1$ are the dimensions of the slot inductor.

The coupling between the CPW signal line and the slotted resonator is mainly decided by the shape and the critical dimensions of both, namely the width of the slot, $S_1$, thickness of substrate, h, and width and gap of CPW line, W and S, respectively. A full-wave electromagnetic (EM) analysis has been performed to identify the optimal varactor loading points, so as to adjust the resonance frequency of the resonators and achieve maximum notch filter tunability. EM analysis has identified the positions where the charges concentrate or there are

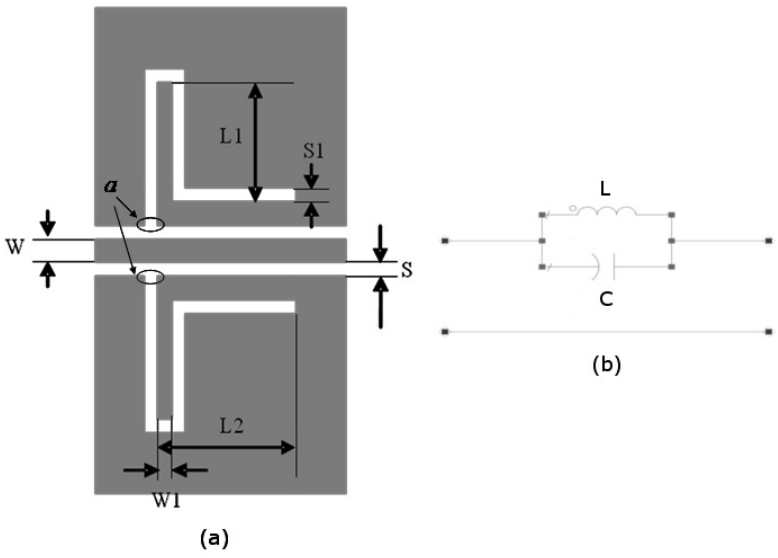



**Figure 5.8:** Resonator with slotted CPW ground structure : (a) schematic diagram and (b) equivalent circuit.

large differences in current density as the optimal tuning points. These positions can modify the overall charge and current distributions more efficiently, resulting in altering the effective electrical length of the resonator. The optimal varactor loading positions are shown in figure 5.8 as positions $\alpha$. The EM simulations were performed by using a commercial em-simulator, SONNET EM.

The loaded MIM PST varactors were designed in a 'hook' layout, so as errors in lithographic alignment would not affect the value of the capacitance of the varactors. Two types of PST varactors were used for 5 and 10 GHz applications - 5um $\times$ 10um and 5um $\times$ 5um, respectively. The layout of the varactor is shown in figure 5.9(a), and their capacitances are shown in 5.9(b), where permittivity of PST is modeled to vary from 300 to 500. These type of simulations were

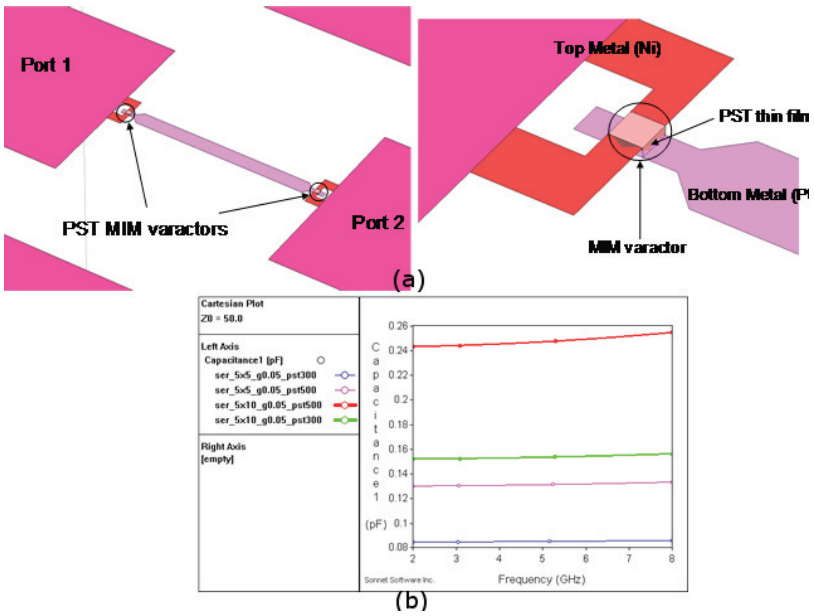



**Figure 5.9:** PST MIM varactors: (a) 3-dimensional view of cascaded varactors and (b) extracted equivalent capacitance values of PST varactors which have a capacitor area of 5um×5um and 5um×10um when $\epsilon_r$ of PST varies from 300 to 500.

used to estimate the sensitivity of the performance of these devices to fabrication tolerances.

Figure 5.10 shows S-parameter simulation results of DGS tunable resonators and 3-pole bandstop filters, where the thickness of the PST thin film is 500 nm and the dielectric constant of the PST thin film varies from 300 to 500. Although estimation of the resonance frequency is possible from equation 5.2, again a full EM analysis was done to take into account all the effects of discontinuities along the meandered slotline, including the open end coupled to the main signal line of the CPW. Three single resonators were periodically repeated for the realization of the 3-pole bandstop filters. The identical resonators were separated with a

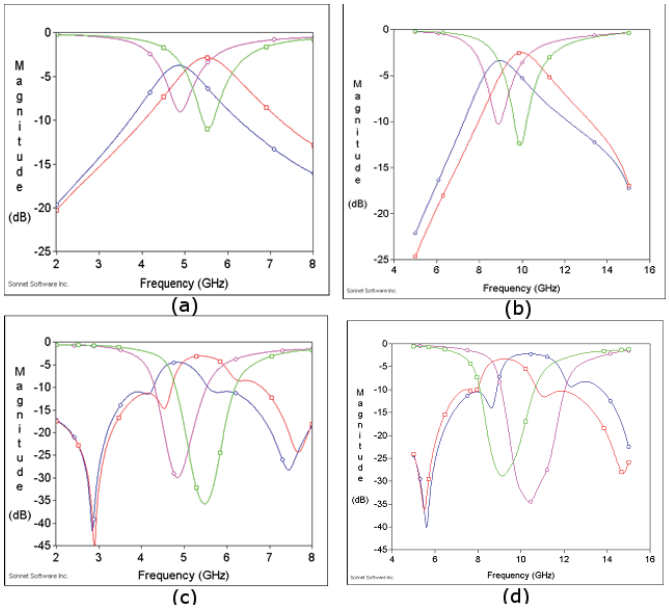



**Figure 5.10:** Simulation results where $\epsilon_r$ of PST varies from 300 to 500: (a) 5 GHz resonator, (b) 10 GHz resonator, (c) 5 GHz 3-pole BSF and (d) 10 GHz 3-pole BSF.

distance of about a quarter wavelength at the required operating frequency. In order to tune the PST varactors in the resonators and filters, distinct DC bias pads were designed, shown in figure 5.11. The DC biasing lines were insulated from the CPW ground lines using the PST ferroelectric layer.

### 5.3.3 Fabrication

The fabrication process for the defected ground devices is similar to the PST MIM varactor fabrication process described previously (Appendix C-1). The substrates were 4-inch, 525 um thick silicon wafers, coated with 1 um $SiO_2$ polished buffer layer. High-resistivity oxidized silicon ($\geq$10K$\Omega$/cm) was used, in order to

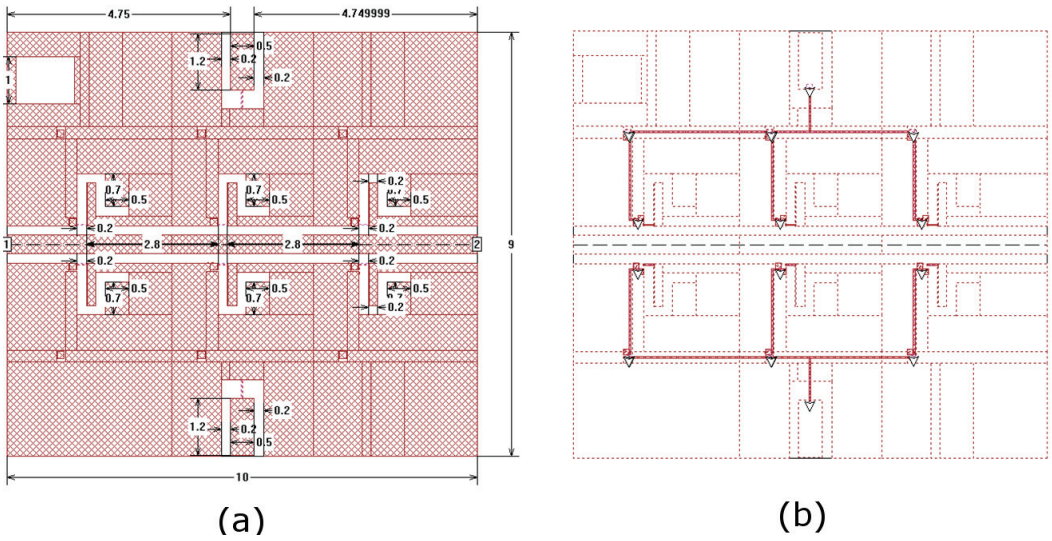



**Figure 5.11:** (a) Top and (b) bottom metalization layers of the resonators and filters in the SONNET EM software. DC voltages are applied through the bottom metalization layer, which is connected to pads in the top metalization layer.

minimize substrate conduction losses, that heavily occur in low resistivity silicon. 200 nm of Pt was RF sputtered and patterned using photolithographic processes as the bottom electrode. Then, a 0.3 um thick PST (Mn doped) thin film was deposited on the bottom electrodes by sol-gel deposition and subsequent high temperature (700$^o$C) annealing of multiple thin (∼50 nm) PST layers. The PST film was then patterned using a diluted HF and HCl etch solution, with standard positive photoresist as a wet-etching mask. Finally, in order to reduce the ohmic losses from a thin electrode, we used our Nickel electroplating facility to deposit 1.7 um thick Nickel top electrodes, using a 100 nm Au seed layer. Scanning electron micrographs of fabricated tunable resonators and filters are shown in figure 5.12.

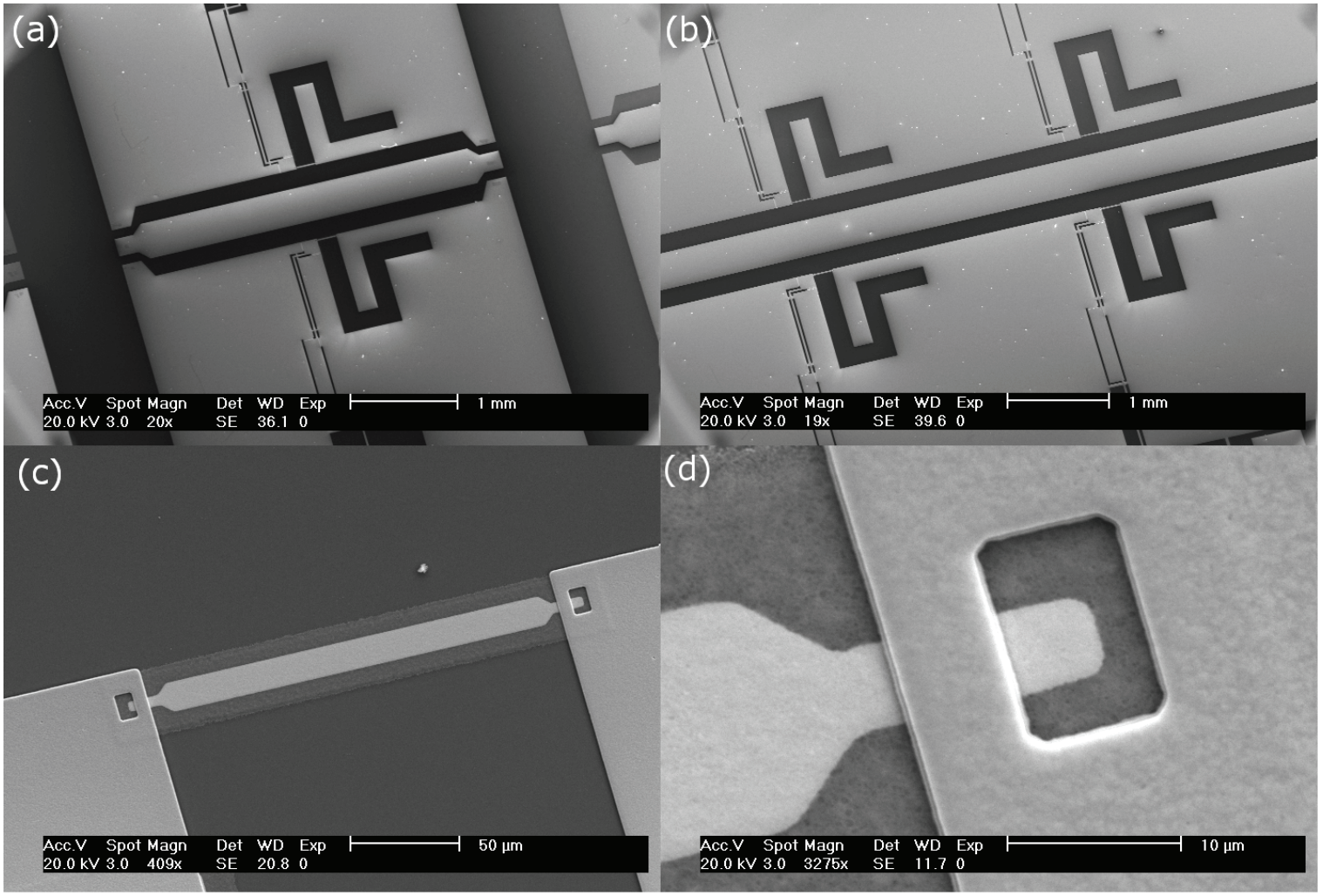



**Figure 5.12:** Scanning electron micrographs: (a) the fabricated tunable resonator, (b) a part of a 3-pole BSF, (c) cascaded PST varactors at the aperture of a slotted resonator and (d) close-up on a PST varactor.

### 5.3.4 Measurements

Performed in Birmingham university, S-parameter measurements from 500 MHz to 20 GHz with 2000 frequency points were obtained from an Agilent E8361A VNA using a Cascade Microtech Summit 9000 automatic probe station. A SOLT calibration using a reference substrate was realized to bring the reference plane to the probe tips and 1.5 KHz was used as the IF. To avoid photovoltaic effects in the high resistive silicon the microscope light was turned off during measurements and sufficient time was allowed for measurement stabilization. DC Bias was introduced through the use of bias-tees and separate probes were made to connect to the designed DC bias pads on the devices. The complete measurement setup can be seen in figure 5.13.

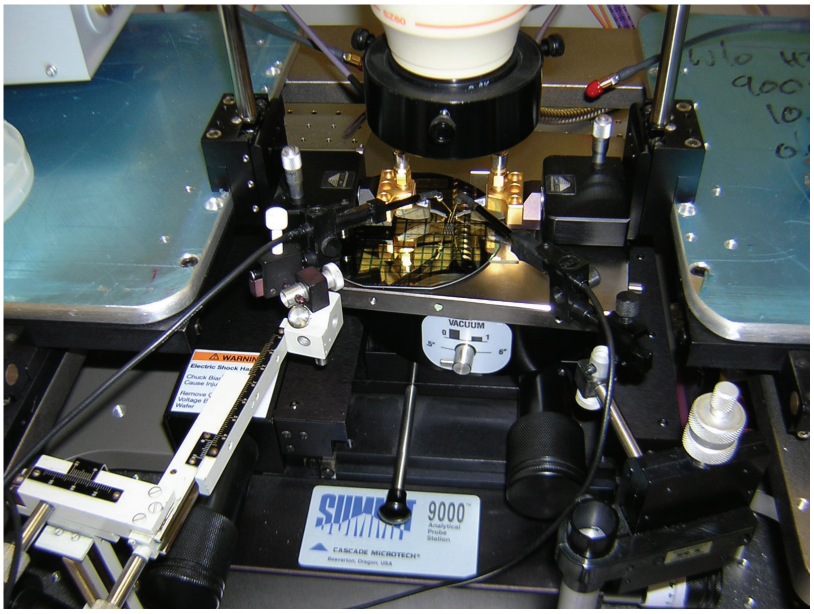



**Figure 5.13:** Photograph of the measurement setup.

Analysis was performed on capacitor test structures situated on the same fabricated wafer and the dielectric properties of the fabricated PST thin film were ex-

tracted. The measured dielectric constant ($\epsilon_r$∼1000) and PST thickness ($d_{PST}$∼300) were far from the ones used for design simulations - estimation from design was $\epsilon_r$∼400-, which resulted in discrepancies between measurements and the simulations presented in figure 5.10. The measured dielectric properties were inserted in the model and new simulations were performed and compared with the measurement results as seen in figure 5.14. The resonators operate at the center frequency from 3.65 to 4.23 GHz and from 5.8 to 7.1 GHz and the measured tuning ranges are 13.7% and 18.3%, respectively. The 3-pole band-stop filter of figure 5.14(c) has maximum rejection of 13.8dB at the center frequency of 3.65 GHz under zero bias.

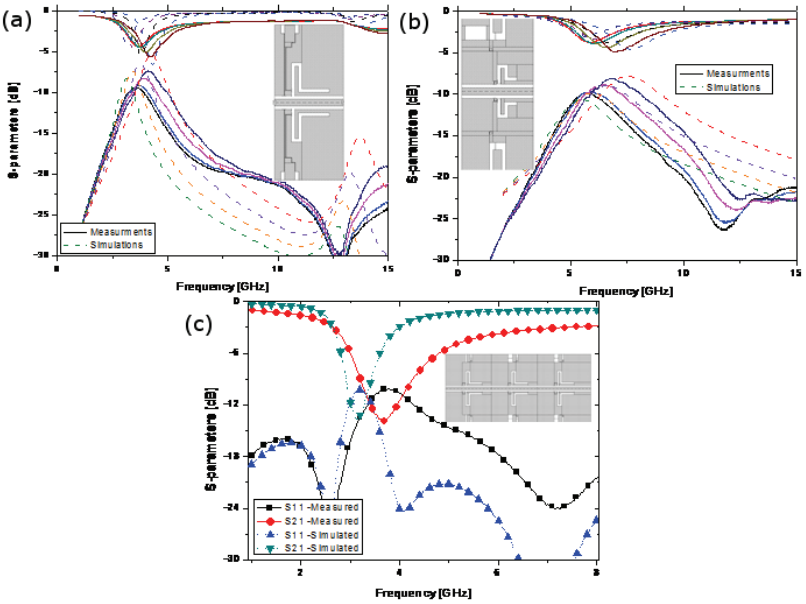



**Figure 5.14:** S-parameter of measured results and adjusted simulation with $\epsilon_r$∼1000 and $d_{PST}$∼300 : (a) tunable resonator at 5 GHz and (b) tunable resonator at 10 GHz when the control voltage is adjusted from 0 to 6 V at 2 V steps, and (c) 3-pole BSF at 4 GHz at zero bias.

### 5.3.5 Optimization of devices

The decreased performance of the monolithic fabricated devices on silicon in figure 5.14 compared to the RT/Duroid 6010 substrate [63] can be attributed to a multitude of factors such as high ferroelectric loss ($\tan\delta_{PST}$ was measured to be ∼3-4% at the operating frequencies), high resistive losses in the thin Pt bottom electrodes, as well as the top large area Ni metalization surface (thick Cu in [63]) and even semi-shorts in the DC bias path, where the PST ferroelectric is used as an insulator so as to reach the slotted ground tuning capacitors. Furthermore, the wrong estimation of dielectric properties and thickness, did not allow for maximum band rejection as the devices (and lithographic masks) were designed.

To establish the possibilities of the original design, which demanded for severely lower tunable capacitance values, a new wafer was fabricated with an increased PST thickness of 1 um, the varactors of which would achieve the designed optimal capacitance values. Figures 5.15, 5.16 and 5.17 present the performance of the resonators and filters in the new wafer. Despite the obvious increased performance, the overall tuning of the resonators and filters is not particularly high, given that individual PST varactor test structures were measured to have a tunability of ∼72%. When a higher electric field than the one shown for each individual device in figure 5.17 was applied, the devices did not tune more, as expected from simulations, shown in figure 5.18. Rather, the leakage current measured by our DC bias source increased, indicating some sort of leakage in the DC bias lines. This can be attributed to defects in large area of the ferroelectric thin film and in its inability to act as a good insulator over large areas. Therefore, the limited tuning and high leakage current was explained by means of top to bottom electrode defects and semi-shorts - meaning shorts that can develop when an electric field is applied. With its high dielectric breakdown strength, $SiO_2$ is an excellent insulator and is proposed to be used as an insulator in the DC bias

path to solve the limited tuning in these devices for future work.

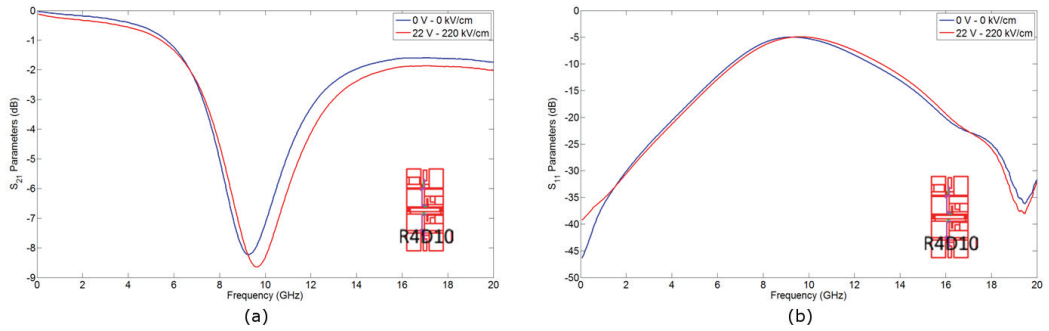



**Figure 5.15:** (a)Transmission and (b) Reflection S-parameters of measured results for a single resonator operating at ∼10GHz at zero and 220KV/cm electric field.

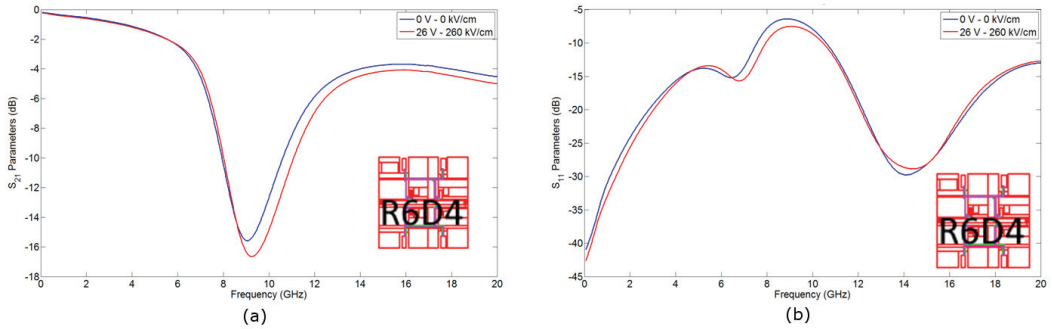



**Figure 5.16:** (a)Transmission and (b) Reflection S-parameters of measured results for a 2-stage filter operating at ∼10GHz at zero and 260KV/cm electric field.

### 5.3.6 Conclusions

Tunable band-stop resonators and notch filters using sol-gel PST ferroelectric varactors in a CPW defected ground structure are fabricated and measured. The

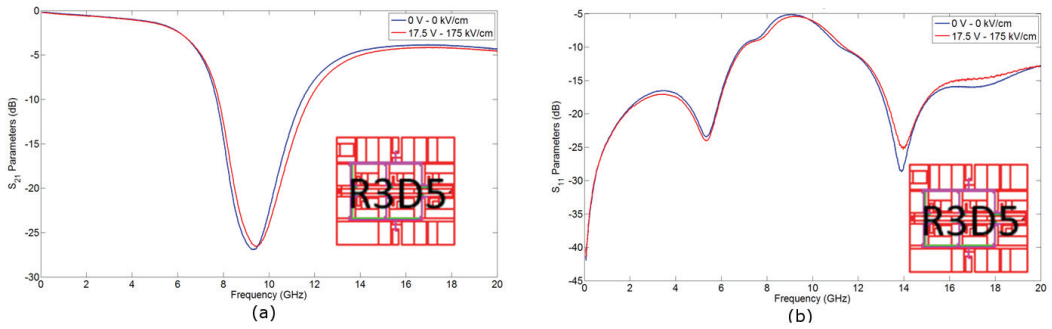



**Figure 5.17:** (a)Transmission and (b) Reflection S-parameters of measured results for a 3-stage filter operating at ∼10GHz at zero and 175KV/cm electric field.

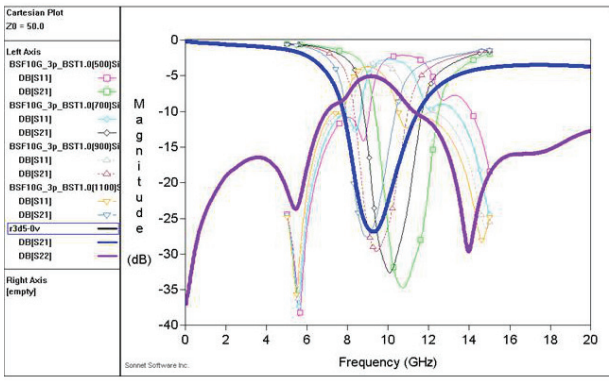



**Figure 5.18:** (a)Transmission and (b) Reflection S-parameters of simulated results for a 3-stage band stop filter operating at ∼10GHz for ∼50% tunability (device R3D5).

PST varactors tune single resonators and 3-pole band-stop filters, operating at the center frequency of 4 and 8 GHz, having a maximum rejection of more than 13.8 dB at the stop band, while the insertion loss at the pass band is less than 3

dB. An improved process allows for fabrication of a 3-stage filter with a maximum rejection of 28dB, albeit with a reduced tuning range, possibly due to leakage.

## 5.4 PST ferroelectric thin-film bulk acoustic wave resonator

### 5.4.1 Background

The design and fabrication of a PST ferroelectric thin-film bulk acoustic wave resonator is presented in this section. The operation of this type of device is governed by acoustic resonances in the ferroelectric thin film due to electrostrictive and piezoelectric forces, induced by the application of an external electric field, as encountered and modeled in section 3.6. Switchable resonators based on paraelectric BST, which operate above the Curie point by means of an electrostriction induced piezoelectric effect have also been reported [7], [187]. The device presented is novel, in that PST is used as the ferroelectric thin film and the resonator stack is completely free-standing, with the connecting electrodes being supported by plated Ni. Similar electrostrictive devices using BST [43] have been reported and a more detailed literature review on realizing tunable thin-film bulk acoustic wave resonators can be found in section 6.2.

One of factors influencing the quality factor of this electric field induced acoustic resonance is the acoustic loss of the whole ferroelectric varactor stack. As the acoustic wave propagates through the stack, each layer presents a different acoustic impedance, which depends on the thickness and the material properties of the layer. As a result, the removal of all but the absolutely essential elements of the effective MIM area is necessary to improve the performance of the device.

### 5.4.2 Fabrication and measurements

PST thin film on a platinized high resistive thermally oxidized Si substrate was used to achieve electrode thermal stability, low acoustic loss (Pt) and low parasitics at microwave frequencies. Substrate bulk micromachining and specifically DRIE, to form acoustically isolating membranes is commonly used to remove the underlying substrate. This serves to increase the amplitude of the resonance by minimizing acoustic losses. To further increase the performance, the removal of the thermal oxide ($SiO_2$) allowed completely free-standing FBARs. An interesting frequency range of interest for mobile communications is ~800MHz to 2.5GHz and devices have been designed and fabricated for this range. A schematic cross-section through a device and SEM micrographs of a fabricated 10 um $\times$ 10 um free-standing PST FBAR are shown in figure 5.19. The RF response of the devices was measured with bias fields up to 460 KV/cm and the results for a typical 20 um $\times$ 20 um FBAR are shown in figure 5.20.

The field variation in the series and parallel resonant frequencies and effective electromechanical coupling constant were extracted from the series and parallel resonant frequencies and plotted in figure 5.21. The wide tuning range observed and slightly hysteretic behavior are as expected for a conventional ferroelectric FBAR and show that in this particular sample the PST Curie point may be slightly above room temperature. Although the Q is significantly lower than the best values for PZT FBARs, in terms of tunability the performance appears to be superior at least to that observed in [188].

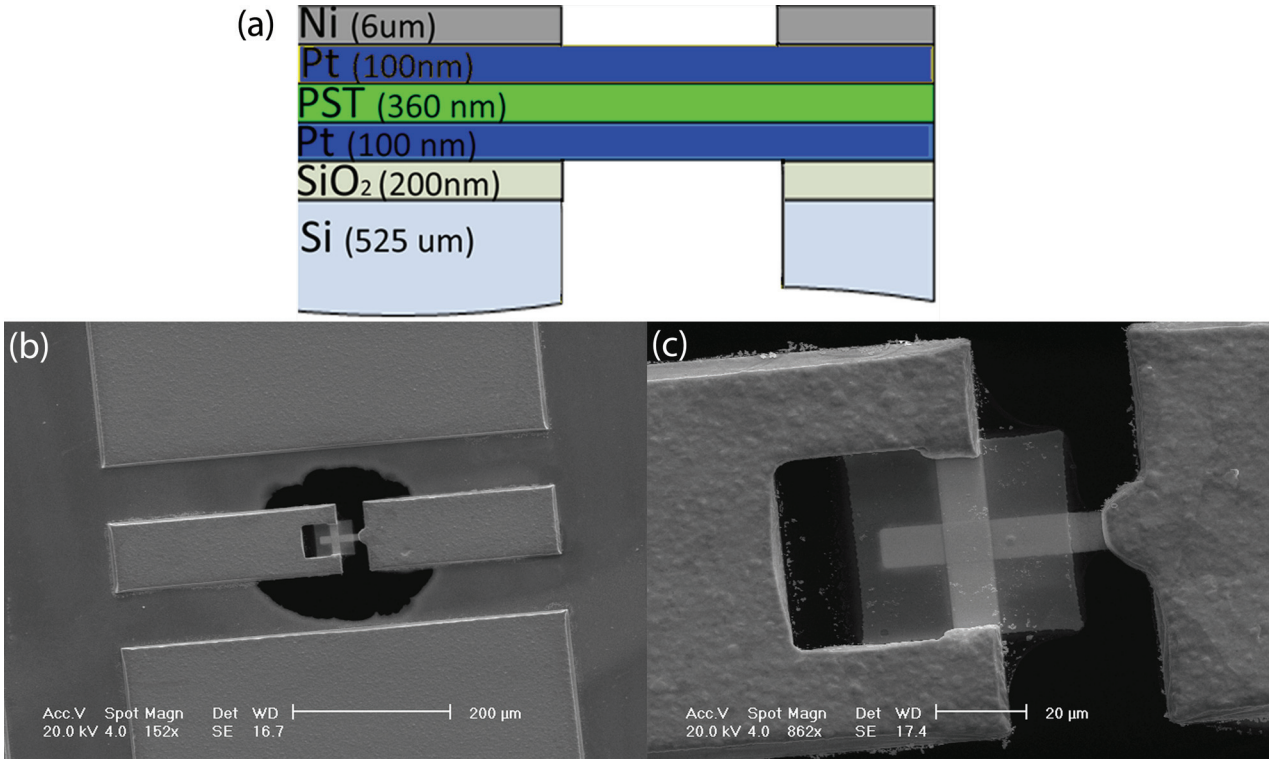



**Figure 5.19:** PST FBAR with Ni supporting layer: (a) Schematic cross-sectionand, and SEM micrographs of a fabricated 10 um $\times$ 10 um series configured PST FBAR shown at a (a) 200um and (b) 20um scale.

### 5.4.3 Conclusion

The design and fabrication of a PST ferroelectric thin-film bulk acoustic wave resonator is presented. The device exhibits a purely capacitive behavior when there is no external electric field and a high frequency resonance when an external electric field is applied. Depending on the lectric field applied, the effective electromechanical constant is shown to vary from 0 - 16% and series resonance $f_s$ is shown to vary $\sim$ 10 MHz. Further investigation in the acoustic loss of both the

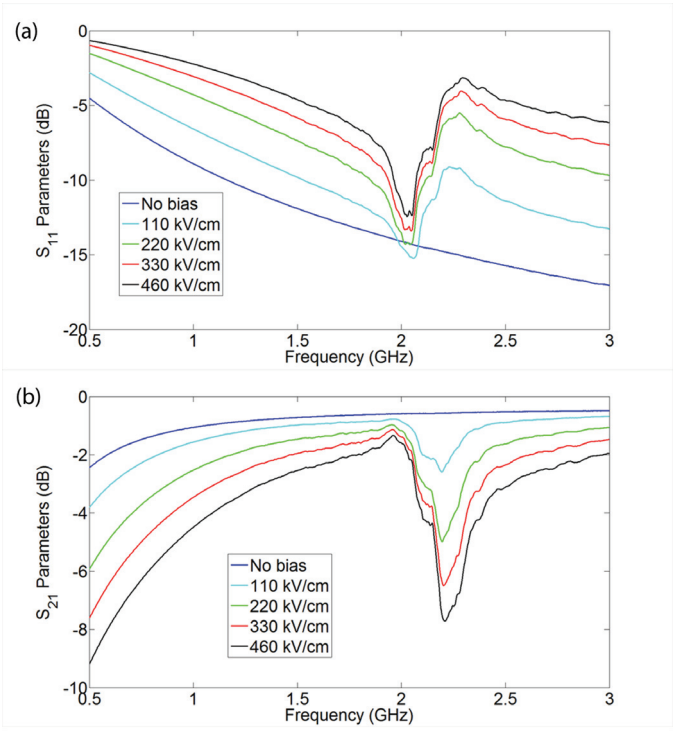



**Figure 5.20:** Measured (a) return loss and (b) insertion loss of a 20 um $\times$ 20 um series configured PST FBAR.

electrode and the PST ferroelectric material is needed to improve the Q of the resonator when the external electric field is applied.

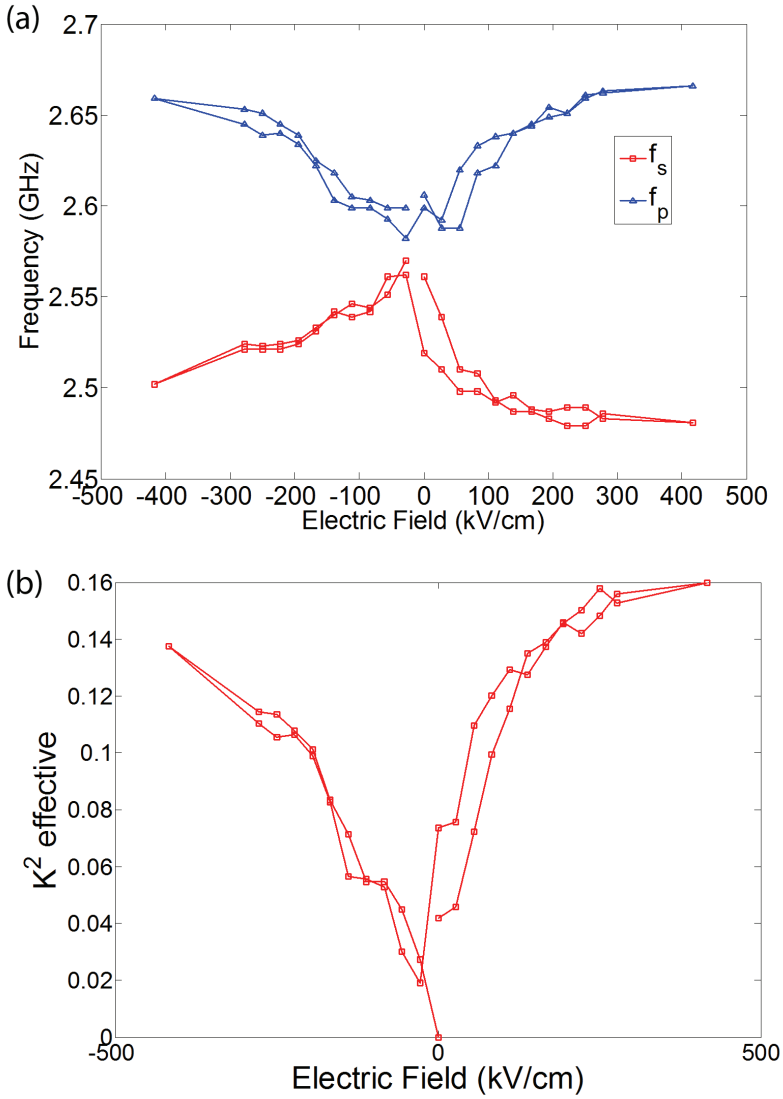



**Figure 5.21:** Measured (a) series ($f_s$) and parallel ($f_p$) resonant frequencies and (b) effective electromechanical constant up to ~420 kV/cm.

Chapter 6

# Integration of tunable varactor with FBAR

## 6.1 Introduction

In this chapter, the tunable ferroelectric varactor is considered as a means of tuning a conventional FBAR. The design, simulation, fabrication and analysis of the FBAR device that is to be integrated, is presented. A high performance resonator is needed, as integration is expected to somehow degrade the performance of the whole device, due to ohmic resistances, parasitic and substrate losses. The performance limiting factors are discussed through the fabrication of conventional piezoelectric thin film FBARs. The novel design, modeling and fabrication of a ferroelectric varactor tunable ZnO bulk acoustic wave resonator is presented. Tuning of the FBAR resonance by applying an electric field application across the ferroelectric varactor is demonstrated, with a maximum resonance tuning of 0.45% at 1.5 GHz.

## 6.2 Conventional FBAR technology

Apart from tunable radio architecture concepts, improving the performance and reducing the size of individual RF components, can also play a significant role in the miniaturization of a mobile handset. Particularly, having replaced the more bulky ceramic and surface acoustic wave (SAW) filters - see figure 6.1 -, FBAR filters have dramatically shrunk the size of duplexers, multiplexers and filters in mobile handsets [1], [135]. Commercially widely implemented, their low insertion loss and performance shift over temperature, along with their high rejection and power handling capability, makes them ideal for UMTS requirements. Since the first publication on FBAR duplexers [137], much work has been done on FBAR filters and duplexers for PCS/GPS/800 MHz [9], PCS1900 [137], [49], UMTS (bands 2 and 8) [11] and UMTS W-CDMA [120], [183] standards. Furthermore, FBAR quintplexers that combine PCS, Cellular duplexers and GPS filters into a single miniature package and eliminate the need for antenna switching, have been realized [10] and are commercially available [1].

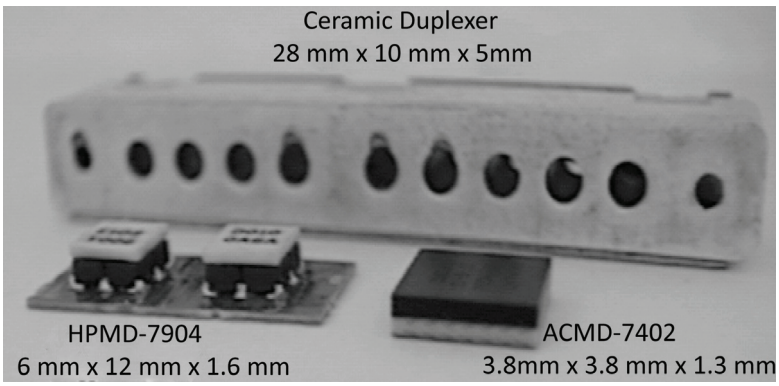



**Figure 6.1:** Photograph of ceramic, SAW and FBAR duplexers.

The FBAR consists of a piezoelectric - usually zinc oxide (ZnO) or aluminum nitride (AlN) - thin film sandwiched between two metal electrodes and device

operation relies on the large electrical impedance change which accompanies RF signal excitation of a longitudinal thickness mode acoustic resonance in the structure. As an approximation, the operating resonant frequency is inversely proportional to the thickness of the piezoelectric layer and for device operation in the low GHz regime, the thickness of the acoustic layer is usually in the micrometer range. Present wireless standards for mobile handset applications lie in the 0.1 - 10 GHz frequency range and although different technologies - such as dielectric (ceramic) resonators [60], transmission line resonators [125] and SAW resonators [177] - are also widely implemented, FBAR technology offers distinct advantages in these frequencies, in terms of size and Q [134]. FBAR devices are electromechanical resonators and utilize electroacoustic rather than electromagnetic (EM) resonance and thus are considerably smaller than EM resonators, since the acoustic velocity is approximately four orders of magnitude lower than the velocity of light [133]. SAW resonators are also electroacoustic devices, but are usually limited to below 2 GHz because of stringent lithography issues and the Q of FBAR devices are superior, with reported values up to 5200 [135].

Dating back to the early 1980s [79], FBAR research has been embraced by the majority of established microwave companies such as Agilent [100], [103], [137], Avago [1], Fujitsu [109], Samsung [118], [46], EPCOS [49], TFR [77], [78], Infineon [5] and LG [120]. FBAR packaging technology, whether employing wafer bonding - microcap invented by Agilent [136] - or spin-on processes - Infineon [5] -, further reduces the size and ultimately the cost of devices. Furthermore, concerning the integration of FBAR technology with integrated circuits (IC) and standard CMOS fabrication technology, both hybrid [34] - wire-bonding and flip-chip bonding - and monolithic approaches [33] have been reported, albeit in spite of the elegance of monolithic integration, its complexity, compatibility issues and costs are some challenges that need to be overcome [12].

### 6.2.1 Background

The FBAR consists of a piezoelectric thin film sandwiched by two metal electrodes and its fundamental resonance occurs when the thickness of the piezoelectric film is equal to half of the wavelength (6.1).

$$f = \frac{\upsilon_{piezo}}{2d} \tag{6.1}$$

, where $\upsilon_{piezo}$ and d are the acoustic velocity and the thickness of the piezoelectric layer respectively.

FBAR devices are electromechanical resonators, which utilize electro-acoustic rather than EM resonance, thus making them considerably smaller than EM resonators, since the acoustic velocity is approximately four orders of magnitude lower than the velocity of light [133]. One of the key points on the design of the resonator is its supporting membrane, which provides acoustic isolation.

As seen in figure 6.2, three major configurations are distinguished based on the medium which provides the acoustic impedance discontinuity and 'traps' the acoustic energy in the resonator, assuring minimal acoustic losses. The two first configurations, rely on air being the acoustic discontinuity, but do so with different configurations. The membrane supported FBAR, is bulk micromachined from the back to remove the substrate, while the air-gap resonator is surface micromachined. Having air as the acoustic discontinuity, they both provide excellent confinement of the acoustic energy, but are also mechanically fragile, due to the membrane. The air-gap FBAR can be fabricated on low-loss substrates, though. The third configuration is the solidly mounted resonator (SMR) , where Bragg reflectors - layers with very different acoustic impedance - are used to provide the acoustic confinement. The finite bandwidth of the SMR reflector array limits the

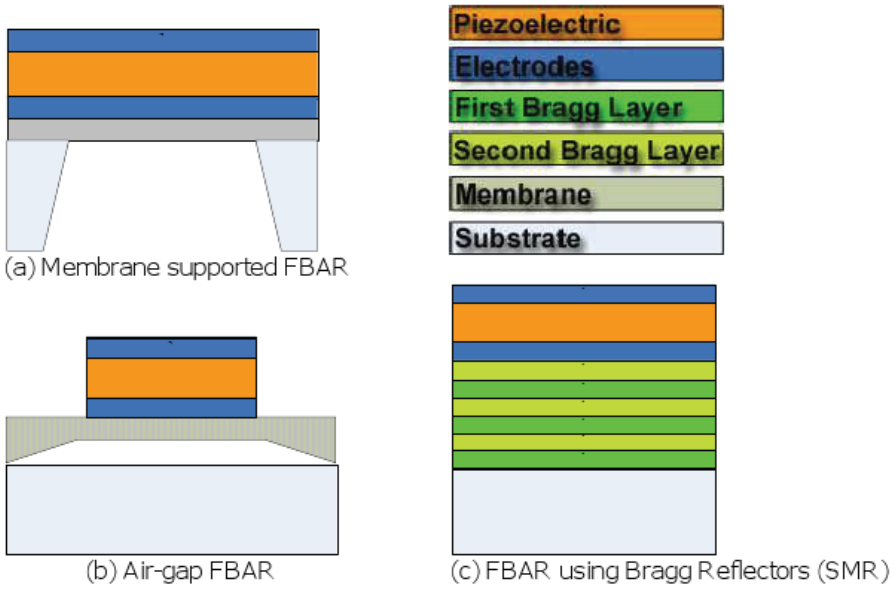



**Figure 6.2:** The three most common FBAR structures : (a) Membrane supported FBAR, (b) Air-gap FBAR and (c) FBAR using Bragg reflectors.

spurious response that would have been obtained for the fundamental membrane structure [76].

On figure 6.3, the impedance response of an FBAR is simulated and contrary to classic resonators, there are two resonances, the resonance and the anti-resonance. The frequency interval between the two resonances is a factor of merit of piezoelectric resonators called the electromechanical constant ($K^2$). As this constant is very important for the bandwidth of filters, it sometimes determines which piezoelectric material must be used for which device. Another very important FBAR characteristic is its quality factor (Q), which measures the influences of the mechanical, dielectric and resistive losses on the performance of the resonator. Due to two resonances being exhibited, two quality factors - series ($Q_s$) and parallel

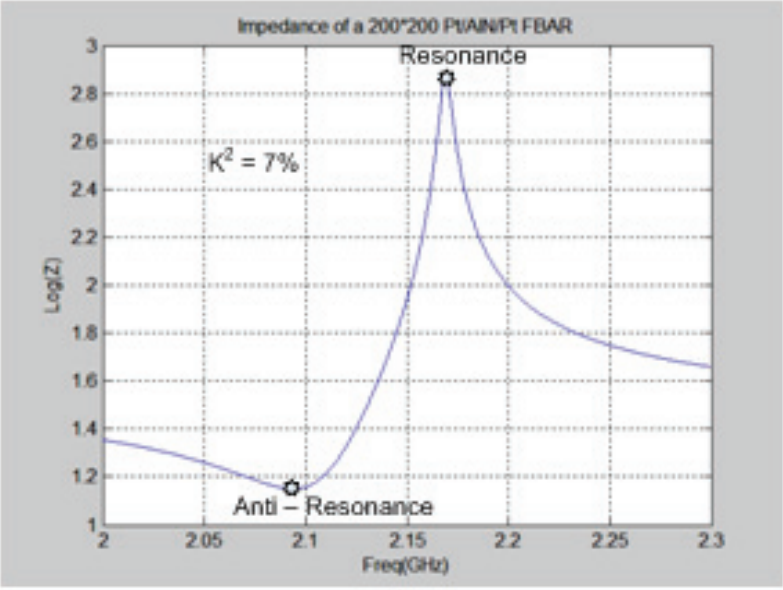



**Figure 6.3:** Simulation of the impedance response of a piezoelectric resonator showing the resonance, antiresonance and calculated electromechanical coeffiecient ($K^2$).

($Q_p$) - exist. The main method of calculating them is from the impedance phase at the resonant frequency [75] using equations 6.2. Another method for calculating the quality factors - although not specifically made for FBARs, but resonators - is the -3 dB technique, which is widely used due to its triviality [80].

$$Q_s = \frac{f_s}{2}\frac{\partial\varphi}{\partial f}|_{f=f_s}, Q_p = \frac{f_p}{2}\frac{\partial\varphi}{\partial f}|_{f=f_p} \tag{6.2}$$

### 6.2.2 The piezoelectric layer and the electrodes

The main factor affecting the performance of the FBAR is the piezoelectric layer, as not only it sets the resonant frequency, but also largely determines the quality factor. The characteristics of the piezoelectric layer that need to be investigated when designing an FBAR are : (a) the electromechanical constant ($k_t^2$), which determines the degree of energy transfer between the electrical and the acoustic domain, (b) the dielectric constant ($\epsilon_{piezo}$), which influences the impedance of the FBAR, (c) the longitudinal velocity ($\upsilon_{piezo}$), which has an impact on the resonant frequency and (d) the acoustical losses and dielectric losses, which influence the Q. The most common piezoelectrics used, are AlN, ZnO and PZT. Table 6.1, shows their characteristics for comparison purposes. It must be noted that these piezoelectrics have been shown to produce good FBAR performance, only when they are grown in a highly preferential c-axis orientation.

**Table 6.1:** Comparison of piezoelectric materials used for FBARs.

| | ZnO | AlN | PZT |
|---|---|---|---|
| Dielectric constant | ∼10 | ∼10 | ∼400 |
| Electromechanical constant | 6.5% | 7% | 8-18% |
| Acoustic velocity | 10400 | 6400 | 4700 |
| Mechanical losses | moderate | moderate | high |
| CMOS integration | no | yes | no |

The electrodes of the FBAR contribute both acoustically and electrically and as such, they produce both acoustic and resistive losses. To avoid electrical losses a material with high conductivity like gold or copper would be satisfactory, but these are not good materials to deposit AlN and high mechanical losses would

occur. Molybdenum (Mo) has been reported [53] as a very good candidate as it provides a good balance between electrical and acoustic loss, as well as promotes the AlN growth. Therefore, all these considerations must be taken into account when designing the FBAR.

## 6.2.3 Experimental

### 6.2.3.1 Fabrication

RF sputtering was used to deposit the ZnO piezoelectric thin films. The parameters used were 250 Watts, 20 mTorr gas flow (90% Ar,10% $O_2$) and the substrate was heated at 200$^o$C during deposition. Good performance of the FBARs is generally attributed to obtaining good columnar c-axis (001) ZnO crystallization and dense grain structure. Figure 6.4 shows that the ZnO grown on both Au(100nm)/Ti/$SiO_2$/Si and Au(100nm)/Ti/$TiO_2$/$SiO_2$/Si was highly crystallized in the c-axis orientation. Furthermore the dense structure of the obtained films -seen in figure 6.5 - was observed using scanning electron microscopy.

FBARs were fabricated on a 1 um thick $SiO_2$ coated high resistance Si substrate. The fabrication process is similar to that used in section 5.3, with the obvious exception of using a piezoelectric ZnO thin film in the place of the ferroelectric PST thin film and the use of Au electrodes for all (top and bottom) electrodes. Figure 6.6 shows a fabricated 200 um $\times$ 200 um ZnO FBAR.

### 6.2.3.2 Measurements

Measurements of the fabricated FBAR are presented in figure 6.7. The highest Q observed, was from an FBAR with a square active area of 120 um $\times$ 120 um. The

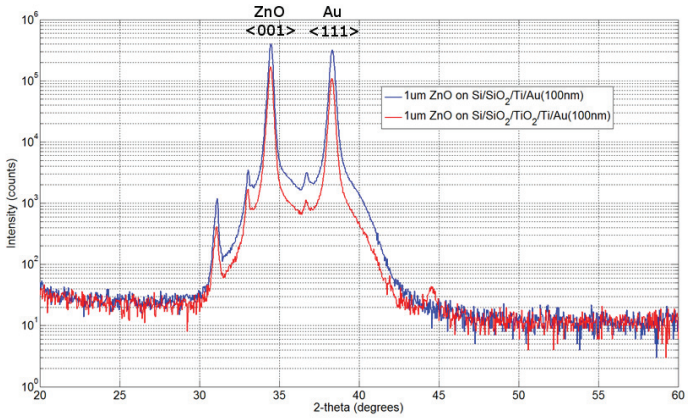



**Figure 6.4:** XRD of ZnO thin films grown on Au(100nm)/Ti/$SiO_2$/Si and Au(100nm)/Ti/$TiO_2$/$SiO_2$/Si substrates.

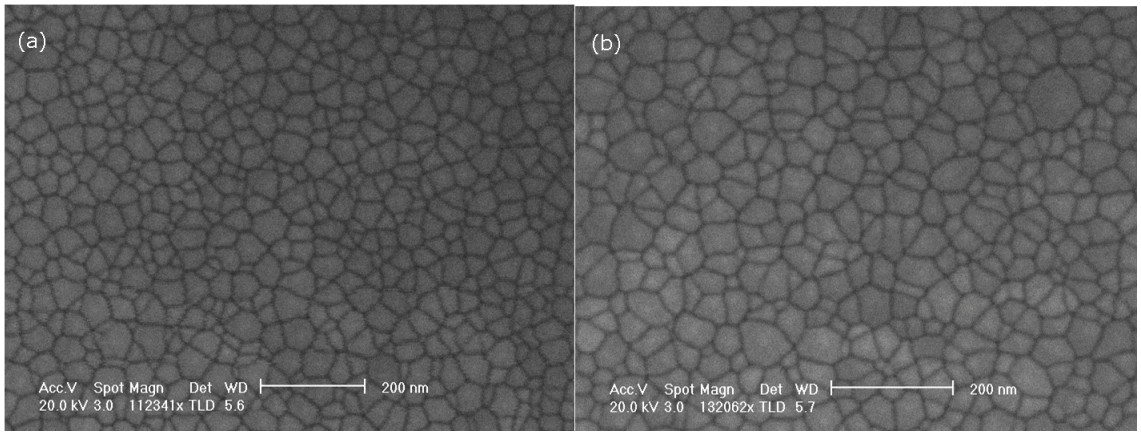



**Figure 6.5:** Scanning electron micrographs of ZnO thin films grown on (a)Au(100nm)/Ti/$SiO_2$/Si and (b) Au(100nm)/Ti/$TiO_2$/$SiO_2$/Si substrates.

microscope light was turned off as this had a negative effect on the measurements. Two resonances can be observed up to 3 GHz, this is due to the FBAR acting as a

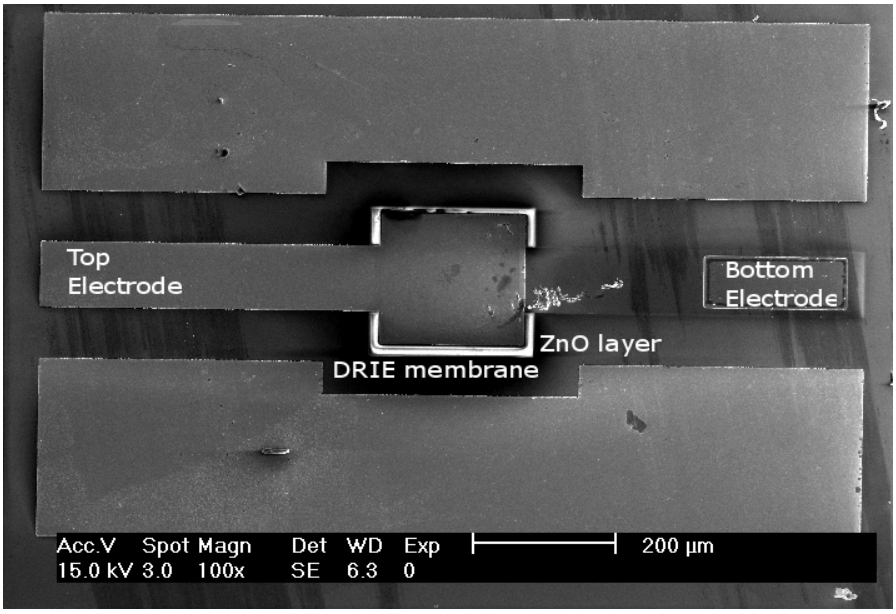



**Figure 6.6:** Scanning electron micrograph of a fabricated 200um×200um ZnO FBAR.

composite resonator, with the thick (∼1 um) $SiO_2$ membrane beneath the piezoelectric stack. The parameters of the main resonance of the FBAR, were extracted from the measurements: series resonance frequency ($f_s$)=1.2384375 GHz, parallel resonance frequency ($f_p$)=1.2669375 GHz, series quality factor ($Q_s$)=404.387755, parallel quality factor ($Q_p$)=965.285714 and effective electromechanical constant ($K^2_{eff}$)=0.054256. The Au electrodes improved the insertion loss compared to older fabricated Pt/AlN/Pt FBARs, also shown in figure 6.7 for comparison.

### 6.2.4 Discussion

It has been suggested that the integration of the conventional ZnO FBAR with a ferroelectric varactor will degrade the overall device performance. The achieved Q

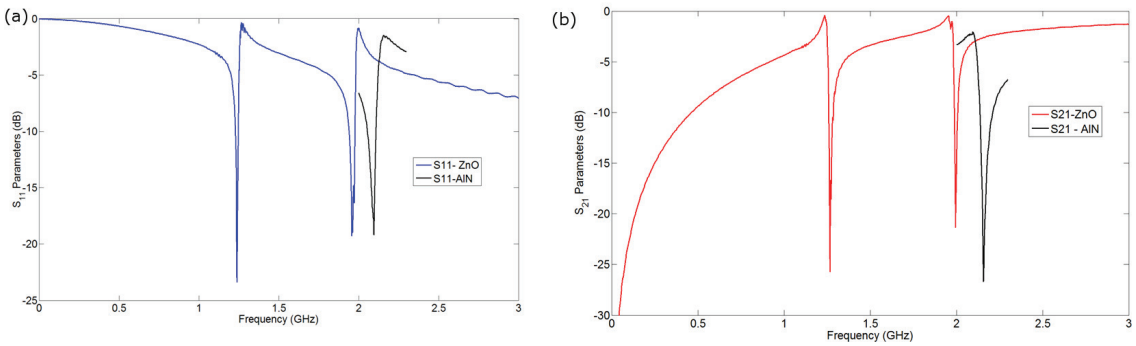



**Figure 6.7:** S-parameter measurements of a fabricated 120um×120um ZnO FBAR: (a)Insertion loss and (b) return loss.

for the stand-alone ZnO FBARs are considered sufficiently higher than reported stand-alone ferroelectric FBAR Qs(∼200) [187] to warrant the integration worth investigating.

## 6.3 Tunable FBAR

In this section, the design, modeling and fabrication of a tunable FBAR made by monolithic integration of a conventional ZnO based FBAR with a PST ferroelectric varactor is presented. The operating principle is similar to that of the MEMS device [113], except that the capacitance change is derived from the decrease - instead of increase - of the dielectric constant in the PST on application of a biasing electric field. Although little different in performance to the MEMS device with no moving parts, there are expected to be significant advantages in speed, reliability, and packaging cost and also the potential for higher power operation.

### 6.3.1 Tunable FBAR in literature and motivation

The motivation for research towards a tunable FBAR originates from the necessity of frequency adjusting the FBAR devices, either post-fabrication or actively in order to compensate for environmental disruptive effects, such as electromagnetic disturbances, aging and temperature changes. For typical mobile phone filters, the required tolerance for the resonance frequency is around $\pm 0.1\%$ [5], requiring extreme film deposition thickness and uniformity control, which can not be met by standard tools for semiconductor processes, typically offering $\sim 5\%$ accuracy. Even if the run-to-run variations can be optimized to a tighter specification, thickness uniformity across the wafer will be an issue. Therefore, accurate tuning of the operating frequency is normally carried out post-fabrication by mass-loading [138] of the resonator - a step which adds additional processing time and cost. Furthermore, although efforts towards minimizing the operating FBAR temperature coefficient (TCF), using careful design of the thin-film layers of the FBARs have been reported [171], post-fabrication resonance drifts due to temperature variations, aging and electromagnetic disturbances can only be actively compensated by the introduction of a real-time resonance tuning method.

Among current research efforts towards achieving tunable FBARs, a widely used approach is to substitute the piezoelectric layer with a ferroelectric perovskite oxide thin film [72],[188],[7],[187], whose electromechanical properties can be tuned by application of a biasing electric field. Lead zirconium titanate (PZT) FBARs [72], [188] have shown resonance tunabilities up to 3%, but are inherently hysteretic due to the ferroelectric nature of the material and are therefore not ideal for implementing in tunable devices. Switchable resonators based on paraelectric BST, which operate above the Curie point by means of an electrostriction induced piezoelectric effect have also been reported [7],[187]. Although no hysteresis is observed in these devices, they show little or no resonance at zero - and small - bias

fields, thus reducing their effective tuning range and reported Q values (∼200) [187] are also still rather limited. Owing to their very high Q (>1000), realization of tunable FBARs based on the conventional ZnO and AlN piezoelectric materials is the most attractive option, and approaches investigated have included the use of heating elements [68] and piezoelectric stiffening [37]. However, limitations such as low tuning speed and very low tunability respectively in the examples cited have meant that these have not been widely implemented. An interesting alternative approach to FBAR tunability, is integration of the FBAR with an active tuning device, a popular choice for which has been the electrostatically actuated MEMS capacitor - either separated from [116], [117] or integrated into the FBAR [113], [114], [115]. This device is capable of high tunability (∼1.47%) [117], but reliability issues such as premature pull-in, stiction and the high cost of MEMS packaging will limit its applicability. Therefore, whereas a tunable FBAR made by monolithic integration of a conventional FBAR with a ferroelectric varactor would have the same operating principle to that of the MEMS device [113], the capacitance change would be derived from the variation of the dielectric constant in the ferroelectric on application of a biasing electric field with significant advantages expected such as ease and cost of fabrication, tuning operation speed, reliability, packaging costs and also the potential for higher power operation.

### 6.3.2 Modeling and design

The principle of tuning the FBAR with a ferroelectric varactor, presented schematically in figure 6.8a is similar to the electrostatic MEMS capacitor integration [10]. An intrinsic difference though, is the field dependent capacitance which reduces in ferroelectric varactors instead of increasing in MEMS capacitors. Composite passive equivalent networks for both the FBAR and the ferroelectric varactor, shown in figure 6.8b and 6.8c respectively, are utilized to accurately model the electrical

impedance. In the modified Butterworth-Van Dyke (MBVD) FBAR network, $L_1$, $C_1$, $R_1$ model the acoustic resonance, $R_S$ is the resistance of the FBAR electrodes, $C_0$ is the piezoelectric plate capacitance and $R_0$ is a resistor component added to produce substantial agreement to measured data [80], while in the ferroelectric varactor network, $R_{EL}$ is the electrode resistance, $L_{EL}$ is the electrode inductance and $C_{PST}$, $R_{PST}$ are the dielectric capacitance and resistance respectively.

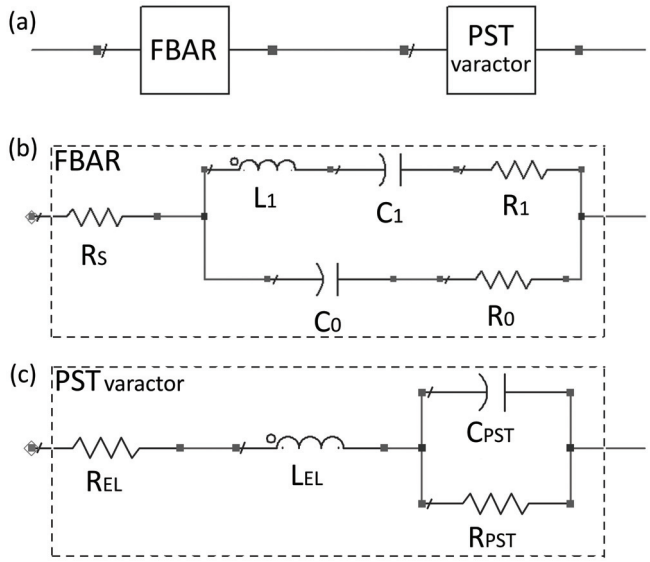



**Figure 6.8:** Equivalent network circuits: (a) series tunable FBAR, (b) FBAR MBVD, (c) ferroelectric varactor.

In the lossless case, all resistances are zero ($R_1$, $R_S$, $R_0$, $R_{EL} = 0$), $L_{EL}$ is negligible and the total impedance ($Z_T$) of the tunable FBAR and the series ($f_S$) and parallel ($f_P$) frequencies can be analytically calculated:

$$Z_T = \frac{-j}{\omega}\left[\frac{L_1C_1\left(C_{PST}+C_0\right)\omega^2-\left(C_1+C_0+C_{PST}\right)}{\left[\omega^2L_1C_1C_0-\left(C_1+C_0\right)\right]C_{PST}}\right] \tag{6.3}$$

$$f_P = \frac{1}{2\pi}\sqrt{\frac{(C_1 + C_0)}{L_1 C_1 C_0}} \tag{6.4}$$

$$f_S = \frac{1}{2\pi}\sqrt{\frac{(C_1 + C_0 + C_{PST})}{L_1 C_1 (C_1 + C_0)}} \tag{6.5}$$

It is observed from equation 6.4 that the parallel resonance is not affected by the tunable varactor. Based on equation 6.5 and previous measurements of ZnO FBARs [150], where the ratio $C_1/C_0$ was found to be 0.0852 for a 100 um $\times$ 100 um ZnO FBAR, the series resonance tunability expected for different values of $C_{PST}$ is presented in figure 6.9 for the lossless case. If no reductions are made, the impedance formula of the whole tunable FBAR is very complicated to calculate manually and therefore in order to model the lossy integration (where $R_1$, $R_S$, $R_0$, $R_{EL} \neq 0$), electronic cad software was used with element values extracted from discrete FBARs and PST varactors. Losses do not seem to significantly hinder the ability of the series ferroelectric varactor to tune the FBAR. For a specific $C_{PST}$ tuning range, higher tunability of the series resonance can be achieved with values of $C_{PST} \leq C_0$. Therefore, using equation 6.6 and 6.7, since the dielectric constants of ZnO and PST are $\sim$9 and $\sim$160 respectively, the PST varactor was designed to be significantly smaller in area than the ZnO FBAR.

$$C_0 = \frac{\epsilon_0 \epsilon_{ZnO} A_{FBAR}}{d_{ZnO}} \tag{6.6}$$

$$C_{PST} = \frac{\epsilon_0 \epsilon_{PST} A_{VAR}}{d_{ZnO}} \tag{6.7}$$

, where $\epsilon_0$ is the the fundamental vacuum permittivity constant, $\epsilon_{ZnO}$, $\epsilon_{PST}$ are the dielectric constants of ZnO and PST, $d_{ZnO}$, $d_{PST}$ are the thicknesses of the

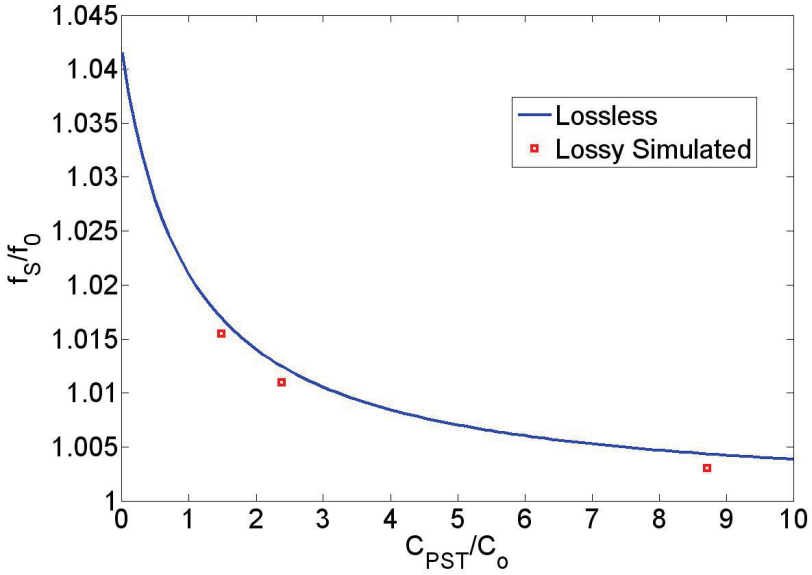



**Figure 6.9:** Tunability of series frequency for different CPST assuming a lossless and lossy tunable FBAR.

ZnO and PST layers and $A_{FBAR}$, $A_{VAR}$ are the areas of the FBAR and varactor overlap respectively. Furthermore, the connecting CPW dimensions were chosen as to have an impedance of approximately 50 Ω and the signal linewidth and gap were 0.1 mm and 0.08 mm respectively.

### 6.3.3 Fabrication

The complete fabrication process of the tunable FBAR is presented in figure 6.10.

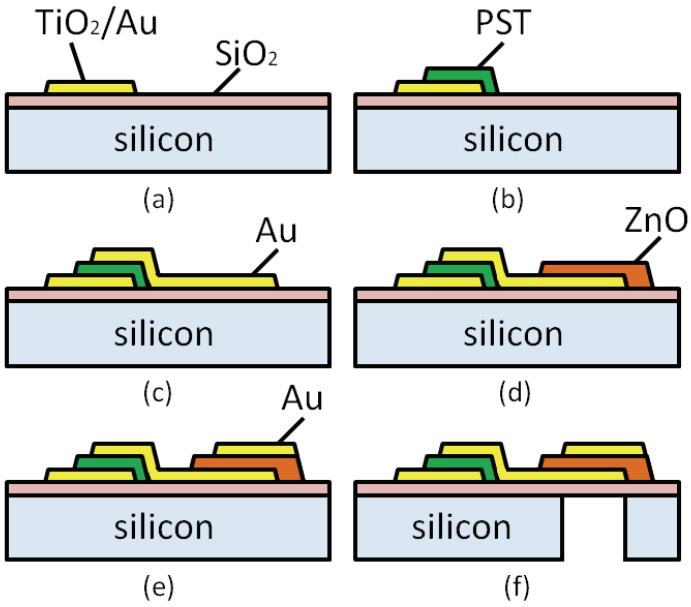



**Figure 6.10:** Fabrication process: (a) Bottom electrode deposition and patterning, (b) PST deposition and patterning, (c) Middle electrode deposition and patterning, (d) ZnO deposition and patterning, (e) Top electrode deposition and patterning and (f) Si bulk micromachining.

The devices were fabricated on high resistivity (>10K$\Omega$/cm), thermally oxidized (4") Si wafers combining process steps described previously for ZnO FBARs [150] and ferroelectric varactors [36]. The PST varactor was fabricated first, in order to avoid the presence of a ZnO film at the high temperature annealing of the ferroelectric thin film, which is necessary for crystallization. $TiO_2$(100nm)/Au(400nm)

bottom electrodes were first patterned, followed by sol-gel deposition and patterning of the PST ferroelectric using a mixture of HF and HCl wet-etching. Subsequently, a Ti(8nm)/Au(100nm) middle electrode was deposited, acting both as the varactor top electrode and the FBAR bottom electrode. 1 um ZnO was sputtered and patterned using acetic acid wet-etching and the top Ti(8nm)/Au(100nm) electrode of the FBAR was deposited and patterned. Ti(8nm)/Au(500nm) was used to thicken the connecting CPW and finally a DRIE bulk micromachining step removed the silicon under the FBAR forming the acoustic isolation membrane. Figure 6.11 shows SEM micrographs of two fabricated tunable FBARs.

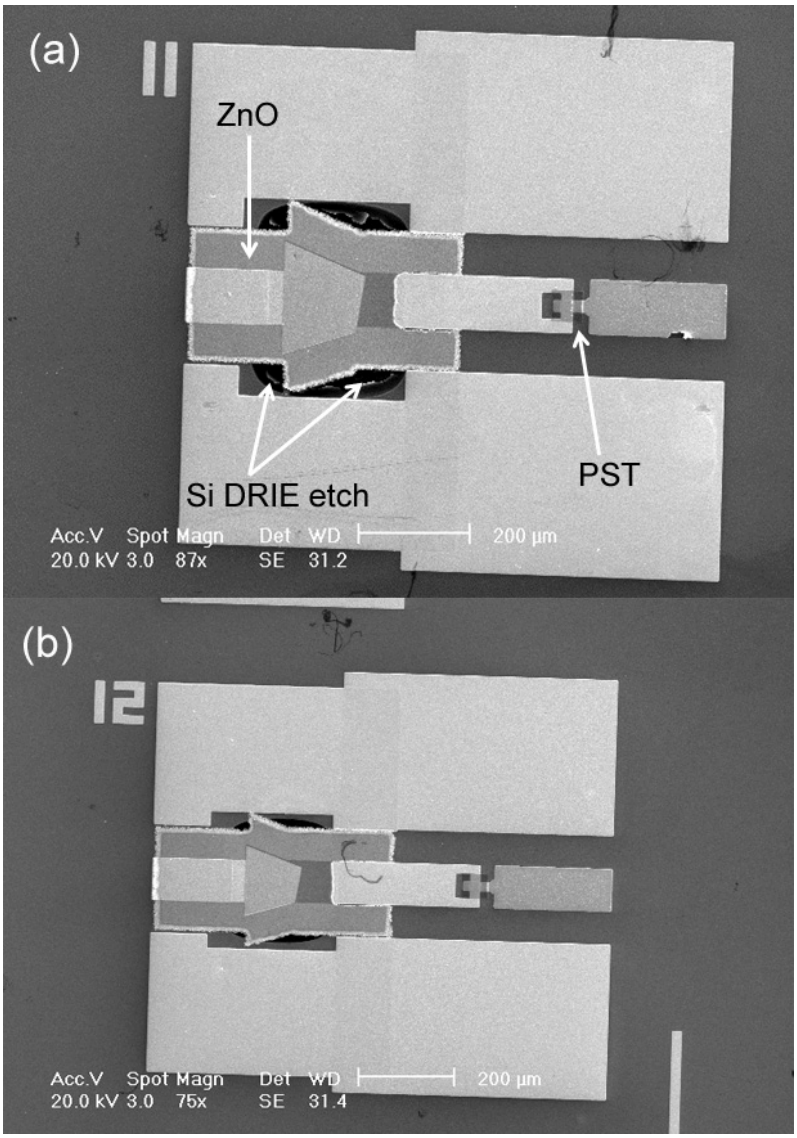



**Figure 6.11:** SEM micrographs of fabricated tunable FBARs consisting of: (a) device 11 - apodized ∼150um×150um ZnO FBAR in series with a 20 um × 20 um PST varactor and (b) device 8 - 120 um × 120 um square ZnO FBAR in series with a 20 um × 20 um PST varactor.

### 6.3.4 Measurements and discussion

After a SOLT calibration using a reference substrate was realized to bring the reference plane to the ground-signal-ground (GSG) probe tips, two port S-parameter measurements of the tunable FBARs were obtained from a HP8753D VNA. To avoid photovoltaic effects in the high resistive silicon, the microscope light was turned off during measurements and sufficient time was allowed for measurement stabilization. DC Bias was introduced through the signal lines of the microwave probes. The admittance $Y(\omega)=G(\omega)+jB(\omega)$ of the tunable FBARs was extracted from S-parameters and $f_S$ was calculated from the point of maximum conductance. Close to 0.45% tunability was observed for a 1.5 GHz ZnO FBAR and figure 6.12a presents the measured S-parameters. and field dependent tunability. The field-dependent tunability in figure 6.12b, agrees with previous predictions [117] that for the same voltage applied, a higher tunability is expected from tunable FBARs with smaller $C_{PST}/C_0$ and higher $C_{PST}/C_0$ ratios.

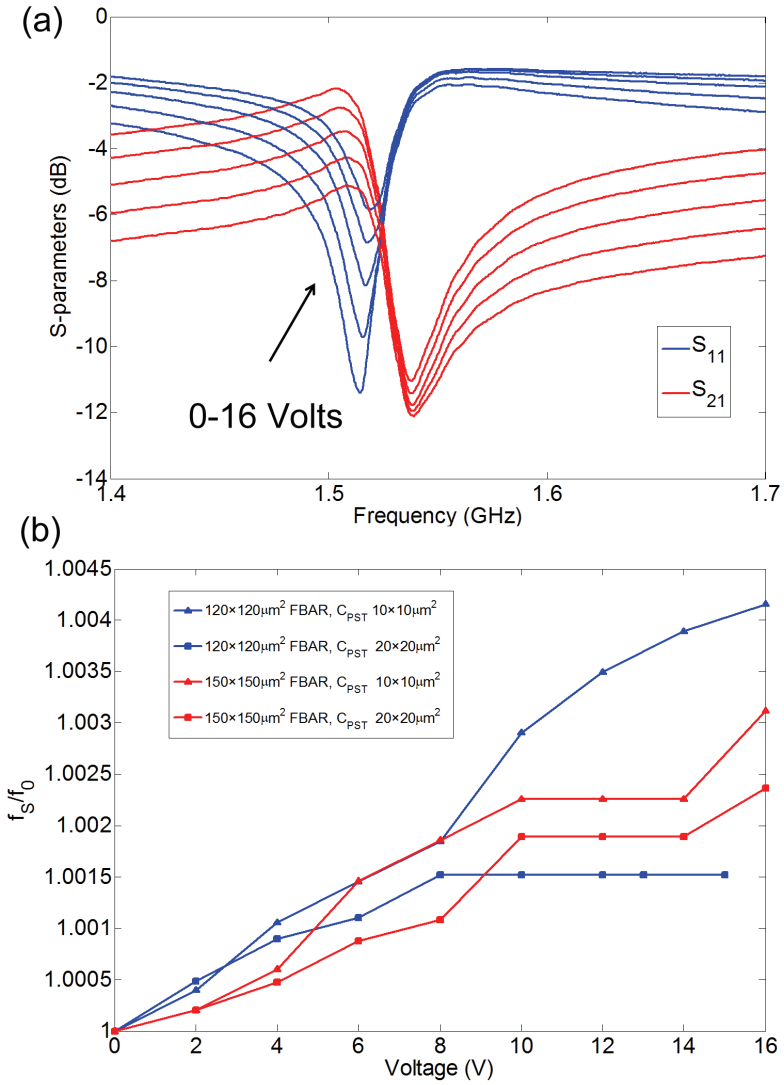



**Figure 6.12:** Measurements of tunable FBARs: (a) S-parameters of 120 um $\times$ 120 um square ZnO FBAR in series with a 10 um $\times$ 10 um PST varactor and (b) normalized tunability of FBAR series resonance against voltage applied for different integrations.

The tunable FBARs always deformed at a specific position near the ZnO membrane, if more than 16 V were applied. At that voltage, the maximum tunability for the 10 um × 10 um and the 20 um × 20 um PST varactor were found to be 41% and 48% respectively. Since both PST [36] and BST [122] are capable of much higher capacitance tunabilty, it is suggested that significant performance can be gained from a design and fabrication which solves the premature deforming, shown in figure 6.13. This can be achieved by make the membrane smaller, by patterning the ZnO wider or by changing the bias scheme so that the DC field is not applied through the ZnO FBAR. Finally, more compact design can minimize the connecting CPW resistive and parasitic losses.

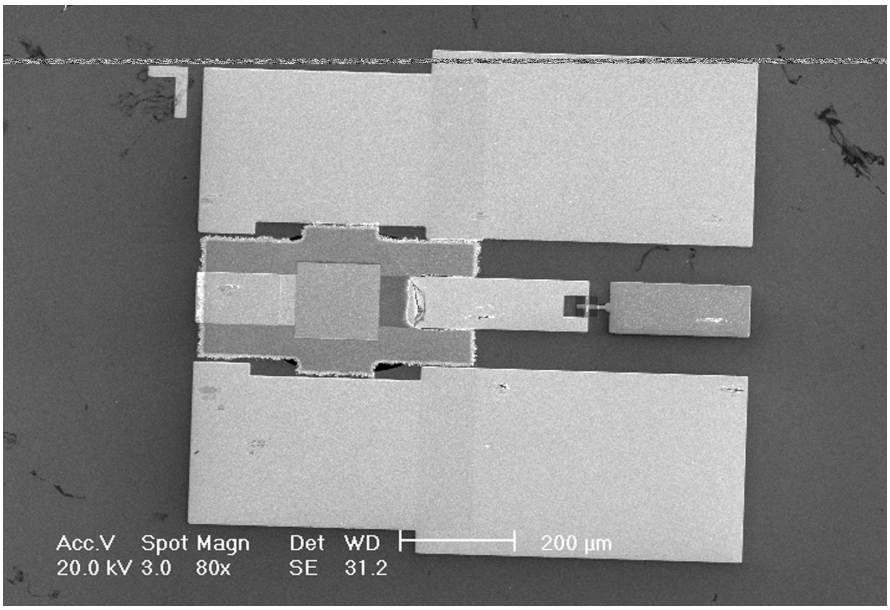



**Figure 6.13:** Field induced deformation at a specific point over the ZnO membrane.

### 6.3.5 Conclusions

The tuning of the series resonant frequency of a conventional ZnO FBAR with a ferroelectric varactor has been demonstrated. Field induced deformation limits the maximum shift of the resonance to 0.45% at 1.5GHz, for 41% tunability of the ferroelectric varactor. This suggests a big scope for possible improvements in performance by improving the design and fabrication. Furthermore, given the high Q achieved in the conventional ZnO FBARs, it is suggested that the low Q of the tunable FBAR is not only the outcome of the ferroelectric varactor and FBAR integration, but that the fabrication process has somehow degraded the FBAR performance as well. A reason for this could be the 'poisoning' of the substrate from Pb diffusion or the subsequent HF etching of the ferroelectric thin films, which may effect the growth and properties of the subsequent ZnO film.

Chapter 7

# Conclusions and Future Work

## 7.1 Conclusions

Concerning viability of tunable ferroelectric materials for microwave applications, the BST material demonstrates superior characteristics compared to any other tunable dielectric material and has been shown to be competitive to GaAs semiconductor diodes at frequencies higher than 45 GHz for the realization of tunable varactors. Although ferroelectric materials are very sensitive to the methods used in material preparation and device processing, there is still large scope of improving the performance in ferroelectric tunable varactors. Commercial acceptance can be achieved through the emergence of a specific application (i.e. improved security in Ferroelectric RAM), lowering the fabrication cost and even minimizing the thermal budget constraints.

The work detailed in this thesis focuses on the development and optimization of sol-gel lead strontium titanate (PST) thin-film tunable varactors and their application in realizing RF tunable devices, such as resonators and filters. As the fundamental tuning components, PST MIM varactors, with capacitances ranging in the pF region, are fully characterized in terms of their electrical and acous-

tic performance. Furthermore, MATLAB software is developed allowing accurate PST thin film characterization from S-parameter measurements of a range of test structures, such as CPWs on PST thin films and CPW MIM PST thin film varactors. Based on the above analysis, the significance of the MIM varactor electrode contribution to the electrical performance is noted. An optimized bottom electrode stack using Au/$TiO_2$ (instead of Pt) is proposed and shown to minimize electrode metallization losses and increase the performance of the MIM PST thin film varactors. Novel tunable RF devices, integrating the PST MIM capacitor have been presented. The tuning of the device operation for a CPW LC shunt switch-resonator, CPW defected ground band-stop filter and electrostictive PST FBAR has been demonstrated. Finally, the novel integration of PST thin film varactors with conventional FBAR technology has been shown to allow the tuning of the operational frequency.

- The sol-gel growth of PST films with good crystallinity and dense uniform grain structure on 4" Si wafers has been demonstrated. CPW MIM capacitors with an active rectangular overlap ranging from 3um×3um to 100um×100um have been fabricated. In the low GHz range (1-5 GHz) practically useful values of $\epsilon\sim1000$ and $\tan\delta\sim0.03$ have been obtained for the 3% Mn doped PST, yielding tunable varactors with capacitance values in the pF region. A tunability of 72% has been obtained on low frequency PST test structures and a premature breakdown effect has limited the RF tunability to ∼50%. It is likely that the varactor structure is burnt by a rise in the temperature induced by the external electric field. This can be attributed to the very thin and therefore resistive electrodes and high frequency current crowding. A better design and increased conductivity using either thicker or more conductive electrodes may prove useful.

- A method for accurate extraction of the high frequency dielectric properties

of the PST films based on high frequency vector network analyzer (VNA) S-parameter measurements is presented. The method includes an improved de-embedding technique that takes into account the whole test structure impedance to isolate the ferroelectric thin film properties. Using a 'short' test structure, identical to the varactor but without the ferroelectric film, frequency-dependent values for the resistance and inductance of the varactor electrodes can be extracted. Not surprisingly, dielectric loss measurements show a monotonic increase with frequency. Intrinsic effects, such as relaxation processes (Debye law) and ac field interaction with the phonon distribution, and extrinsic effects, such as mobile charged defects, can account for this behavior.

- The substitution of Pt, which is the most widely used electrode material for ferroelectric growth but exhibits poor conductivity, has been considered. A variety of Au bottom electrode structures were tested against high temperature annealing deterioration for implementation in ferroelectric varactors. The Au electrodes exhibited improved conductivity, especially after the annealing process, where degradation of conductivity was generally observed for Pt or Au-Pt electrodes. In terms of surface quality and adhesion, a $TiO_2$ interlayer barrier was found to be necessary to allow ferroelectric device fabrication with Au bottom electrodes. A defect-free electrode structure with low resistance was established and thin film PST ferroelectric tunable varactors were fabricated. Measurements made at low and high frequencies present the enhanced performance, compared with Pt. For state-of-the-art ferroelectric varactors, the Au/Ti/$TiO_2$ electrode system might allow for further improvements of BST varactor quality factors achieved with the Pt/Ti and Pt/Au/Pt/$TiO_2$ system [170], thus increasing the competition between ferroelectric and GaAs semiconductor varactor technologies at mm-wave frequencies.

- High frequency peaks in the dielectric loss due to acoustic resonance were observed. These have been modelled using a one dimensional Mason approach and found to be in accordance with electrostrictive behavior. The calculated electromechanical constant for this effect compares well with values recently reported for other tunable ferroelectric materials. Devices that can exhibit a purely capacitive behavior with no external electric field and a high frequency resonance when an external electric field is applied, have been realized. The devices feature a completely free-standing ferroelectric varactor. Further investigation in the acoustic loss of both the electrode and the PST ferroelectric material is needed to improve the Q of the resonator when the external electric field is applied.

- Successful fabrication of a ferroelectric varactor-based RF switch-resonator, integrating an optimized - $Au/TiO_2$ bottom electrode - thin film sol-gel PST ferroelectric varactor with a high Q micro-machined inductor is presented. An insertion loss of $\sim$1.5dB, isolation of $\sim$18dB and return loss of $\sim$10dBs have been achieved for a single 7 GHz resonant switch with a device area of 0.6mm $\times$ 1mm. As the proposed switch performance is still a long way from commercial requirements, further improvements in performance with the use of state of the art tunable materials and cascaded device design are proposed and simulated. The performance of a series cascaded (double) switch, has been simulated using a cascaded equivalent lumped element network and was found to be $\sim$38dB with an increased insertion loss of $\sim$2.4dB.

- Tunable band-stop resonators and notch filters using sol-gel PST ferroelectric varactors in a coplanar waveguide (CPW) defected ground structure are fabricated and measured. The PST varactors tune single resonators and 3-pole band-stop filters, operating at the center frequency of 4 and 8 GHz, having a maximum rejection of more than 13.8 dB at the stop band, while

the insertion loss at the pass band is less than 3 dB. Full-wave analysis is performed to identify the critical points, where PST varactors are implemented to adjust the resonance frequency of the devices. The electrical performance of the device is optimized by reducing metallization losses and increasing the PST thickness. The optimized fabrication process allows for fabrication of a 3-stage filter with a maximum rejection of 28dB, albeit with a reduced tuning range. The limited tuning in the optimized devices is attributed to dielectric leakage in the DC bias path. A $SiO_2$ insulating layer is proposed as a means of reducing the problem.

- Conventional ZnO and AlN are fabricated and measured. ZnO growth is optimized for dense grain growth and high c-axis growth orientation. A fabrication approach where a ferroelectric varactor is integrated with a conventional zinc oxide (ZnO) acoustic wave resonator is demonstrated for the first. The approach avoids the piezoelectric thin film degradation due to the ferroelectric annealing at $700^oC$ by first fabricating the ferroelectric varactor and superimposing the conventional FBAR on top of it. The tuning of the series resonant frequency of a conventional ZnO FBAR with a ferroelectric varactor is demonstrated. Field induced deformation limits the maximum shift of the resonance to 0.45% at 1.5 GHz, for 41% tunability of the ferroelectric varactor, suggesting a big scope for possible improvements in performance by improving the bias design and fabrication. Furthermore, given the high Q achieved in the conventional ZnO FBARs, it is suggested that the low Q of the tunable FBAR is not only the outcome of the ferroelectric varactor and FBAR integration, but that the fabrication process has somehow degraded the FBAR performance as well. A reason for this could be the 'poisoning' of the substrate from Pb diffusion or the subsequent HF etching of the ferroelectric thin films, which may effect the subsequent growth and properties of the ZnO film.

## 7.2 Future Work

- Further characterization of PST thin films and varactors at higher frequencies, such as 10-110GHz, to establish if PST tunable ferroelectric varactors are applicable for high data rate wireless applications. For example, 60 GHz wireless technology is a promising candidate for multi-gigabit wireless indoor communication systems. These measurements will require measurement equipment (vector network analyzers) and calibration techniques capable of providing accurate S-parameter measurements up to these frequencies [92]. Furthermore accurate test structures and de-embedding techniques are needed.

- Investigate premature electrical breakdown and fatigue of PST thin films. This affects the reliability of the ferroelectric tunable varactor and limits the minimum thickness of thin film ferroelectric that can be used. In a thin tunable dielectric, very high electric fields can be applied with low operational voltages. This can be very beneficial for example inside mobile handsets, where a transformer may be needed for high voltage generation. Statistical analysis of dielectric strength using time dependent dielectric breakdown (TDDB) tests [17] could provide insight in this topic.

- Investigate electrical properties of PST thin films annealed at lower temperatures, which can potentially allow for flexible substrate or even post-CMOS integration applications.

- Investigate the existence of dead layers [6] in PST MIM varactors and their effects on tunability and quality factor.

- Investigate the theoretical limit of useful conductivity in the electrodes of the ferroelectric MIM varactor. Although, the effect of reducing the resistance

of the electrodes has been recognized, the growth and crystallization of ferroelectrics in for example very thick Au or Cu electrodes may be detrimental for the properties of the tunable material.

- Revisit the tunable microwave devices presented in this thesis in order to enhance their electrical performance. For the CPW LC shunt switch, fabricate series cascaded switch, shown to further improve isolation in simulations. Use a $SiO_2$ and addition photolithographic mask in the CPW defected ground (DGS) devices to better insulate the DC bias path and solve the limited tuning problem. For the PST tunable ZnO FBAR, a better biasing design will allow further tuning of the resonance.

## Chapter 8

# Publications

### Submitted / Pending submission

Fragkiadakis, C., Wright and Kirby, P. B., 'High conductivity Au bottom electrodes for lead-based ferroelectric RF and mm-wave devices' (Submitted in Integrated Ferroelectrics, January 2012)

Fragkiadakis, C., Wright and Kirby, P. B., 'Ferroelectric varactor tunable zinc oxide (ZnO) thin film bulk acoustic resonator' (Pending submission)

Fragkiadakis, C., Wright, R. V., Laister, A. and Kirby, P. B., 'C-band implementation of a PST ferroelectric narrowband switch' (Pending re-submission in IEEE Ultrasonics)

### Already Published

Gkotsis, P., Kilchytska, V., Bhaskar, U., Militaru, O., Tang, X., Fragkiadakis, C., Kirby, P., Raskin, J.-P., Flandre, D. and Francis, L., 'Neutron and Gamma Radiation Effects on MEMS Structures', Procedia Engineering, 2011, 25, 172 - 175

Fragkiadakis, C., Luker, A., Wright, R. V., Floyd, L. and Kirby, P. B., 'Growth and high frequency characterization of Mn doped sol-gel $Pb_xSr_{1-x}TiO_3$ for fre-

quency agile applications', Journal of Applied Physics, 2009, 105, 061635 -061635-7

Fragkiadakis, C., Wright, R.V., Zhang, Q. and Kirby, P.B., 'Tunable RF Components Based on Sol-gel Deposited $Pb_xSr_{1-x}TiO_3$', Proceedings of the 10th International Symposium on RF MEMS and RF Microsystems, Trento-Italy, 2009(only in print)

Chun, Y.H., Keller, R., Jia-Sheng, H., Fragkiadakis, C., Wright, R.V. and Kirby, P.B., 'Lead-Strontium-Titanate varactor-tuned CPW bandstop filter on liquid crystal polymer substrates', Proc. 39th European Microwave Conference(EuMC 2009), pp.1373-1376

Chun, Y.H., Fragkiadakis, C., Bao, P., Luker, A., Wright, R.V., Jia-Sheng, H., Kirby, P.B., Zhang, Q., Jackson, T.J. and Lancaster, M.J., 'Tunable Bandstop Resonator and Filter on Si-Substrate with PST Thin Film by Sol-Gel Deposition', Proc. 38th European Microwave Conference(EuMC 2008), pp.13-16

Fragkiadakis, C., Wright, R.V., Zhang, Q. and Kirby, P.B., 'Frequency Agile Materials and Microwave Device Fabrication', Cranfield Multi-Strand Conference Proceeding, Cranfield University Press 2008

Mastropaolo, E., Gundlach, A.M., Fragkiadakis, C., Kirby, P.B. and Cheung, R., 'Reactive ion etching of zinc oxide (ZnO) in $SiCl_4$ based plasmas,' Electronics Letters , vol.43, no.25, pp.1467-1469, 2007.

# References


[1] Avago technologies, www.avagotech.com.

[2] Acikel, B., Taylor, T., Hansen, P., Speck, J., and York, R. A new high performance phase shifter using baxsr1-xtio3 thin films. *Microwave and Wireless Components Letters, IEEE 12* (2002), 237 –239.

[3] Acikel, B., Taylor, T., Hansen, P., Speck, J., and York, R. A new x-band 180 deg; high performance phase shifter using (ba, sr)tio3 thin films. In *Microwave Symposium Digest, 2002 IEEE MTT-S International* (2002), vol. 3, pp. 1467 –1469.

[4] Ahn, D., Park, J.-S., Kim, C.-S., Kim, J., Qian, Y., and Itoh, T. A design of the low-pass filter using the novel microstrip defected ground structure. *Microwave Theory and Techniques, IEEE Transactions on 49* (2001), 86–93.

[5] Aigner, R. Mems in rf-filter applications: thin film bulk-acoustic-wave technology. In *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on* (2005), vol. 1, pp. 5 – 8.

[6] Bao, P., Jackson, T. J., Wang, X., and Lancaster, M. J. Barium strontium titanate thin film varactors for room-temperature microwave device applications. *Journal of Physics D: Applied Physics 41* (2008), 063001.

[7] Berge, J., Norling, M., Vorobiev, A., and Gevorgian, S. Field and temperature dependent parameters of the dc field induced resonances in baxsr1-xtio3-based tunable thin film bulk acoustic resonators. *Journal of Applied Physics 103* (2008), 064508 –064508–8.

[8] Bhuiyan, M. S., Paranthaman, M., and Salama, K. Solution-derived textured oxide thin filmsa review. *Superconductor Science and Technology 19*, 2 (2006), R1.

[9] Bradley, P., Kim, J., Ye, S., Nikkei, P., Bader, S., and Feng, C. 2x size and cost reduction of film bulk acoustic resonator (fbar) chips with tungsten electrodes for pcs/gps/800 mhz multiplexers. In *Ultrasonics Symposium, 2007. IEEE* (2007), pp. 1144 –1147.

[10] Bradley, P., Kim, J., Ye, S., Yu, B., Grannen, K., Lee, D., Hula, D., and Kim, W. A 6-port film bulk acoustic resonator (fbar) multiplexer for u.s. cdma handsets permitting use of pcs, cellband, and gps with a single antenna. In *Ultrasonics Symposium* (2006), pp. 325–328.

[11] Bradley, P., Ye, S., Kim, J., Kim, J., Wang, K., Ko, H., and Xie, Y. A generic 2.0 x 2.5 mm2 umts fbar duplexer based on 8-pole near-elliptic filters. In *Ultrasonics Symposium (IUS), 2009 IEEE International* (2009), pp. 839 –842.

[12] Campanella, H. *FBAR fabrication, heterogeneous integration with CMOS technologies, and sensor applications*. PhD thesis, Centre National de Microelectronics, Barcelona, 2007.

[13] Carey-Smith, B. E., Warr, P. A., Rogers, P. R., Beach, M. A., and Hilton, G. S. Flexible frequency discrimination subsystems for reconfigurable radio front ends. *EURASIP J. Wirel. Commun. Netw.* (2005), 354–363.

[14] Carlsson, E., and Gevorgian, S. Conformal mapping of the field and charge distributions in multilayered substrate cpws. *Microwave Theory and Techniques, IEEE Transactions on 47* (1999), 1544 –1552.

[15] Chappell, J., Little, M., and Katehi, L. High isolation, planar filters using ebg substrates. *Microwave and Wireless Components Letters, IEEE 11* (2001), 246 –248.

[16] Chase, D., Chen, L.-Y., and York, R. Modeling the capacitive nonlinearity in thin-film bst varactors. *Microwave Theory and Techniques, IEEE Transactions on 53* (2005), 3215 – 3220.

[17] Chen, H. Y., Wu, J. M., Huang, H. E., and Bor, H. Y. Characteristics of (pb,sr)tio3 thin films with various sr content. *Journal of Crystal Growth 308* (2007), 213–217.

[18] Cho, M.-H., Huang, G.-W., Chen, K.-M., and Peng, A.-S. A novel cascade-based de-embedding method for on-wafer microwave characterization and automatic measurement. In *Microwave Symposium Digest, 2004 IEEE MTT-S International* (2004), vol. 2, pp. 1237 – 1240.

[19] Christou, A., Jarvis, L., Weisenberger, W. H., and Hirvonen, J. K. Sem, auger spectroscopy and ion backscattering techniques applied to analyses of au/refractory metallizations. *Journal of Electronic Materials 4* (1975), 329–345.

[20] Chun, Y.-H., Fragkiadakis, C., Bao, P., Luker, A., Wright, R., Hong, J.-S., Kirby, P., Zhang, Q., Jackson, T., and Lancaster, M. Tunable bandstop resonator and filter on si-substrate with pst thin film by sol-gel deposition. In *Microwave Conference, 2008. EuMC 2008. 38th European* (2008), pp. 13 –16.

[21] Cole, M. W., Nothwang, W. D., Hubbard, C., Ngo, E., and Ervin, M. Low dielectric loss and enhanced tunability of ba0.6sr0.4tio3 based thin films via material compositional design and optimized film processing methods. *Journal of Applied Physics 93* (2003), 9218 –9225.

[22] Collin, R. *Foundations for Microwave Engineering*, 2 ed. McGraw Hill, New York, 1992.

[23] CRAMER, N., PHILOFSKY, E., KAMMERDINER, L., and KALKUR, T. S. Vector network analyzer characterization of parallel plate capacitors with high-k dielectrics. *Integrated Ferroelectrics 66* (2004), 171–178.

[24] de Vries, J. W. C. Resistivity of thin au films as a function of grain diameter and temperature. *Journal of Physics F: Metal Physics 17* (1987), 1945.

[25] DeGroot, D., Jargon, J., and Marks, R. Multiline trl revealed. In *ARFTG Conference Digest, Fall 2002. 60th* (2002), pp. 131 – 155.

[26] Degroot, D., Walker, D., and Marks, R. Impedance mismatch effects on propagation constant measurements. In *Electrical Performance of Electronic Packaging, 1996., IEEE 5th Topical Meeting* (1996), pp. 141 –143.

[27] Dey, S., Wang, C. G., Cao, W., Bhaskar, S., Li, J., and Subramanyam, G. Voltage tunable epitaxial pb x sr(1- x )tio3 films on sapphire by mocvd: Nanostructure and microwave properties. *Journal of Materials Science 41* (2006), 77–86.

[28] Dey, C. B. and, S. G., and Chen, G. A. *Microwave dielectric properties of Mn:BST and PST thin-films*, vol. 77. 2006, pp. 189–197.

[29] D.Galt, J.Price, J., and T.Harvey. In *IEEE Trans. On Applied Superconductivity* (1995), vol. 5, p. 2575.

[30] Dib, N., Ababneh, J., and Omar, A. Cad modeling of coplanar waveguide interdigital capacitor: Research articles. *Int. J. RF Microw. Comput.-Aided Eng. 15* (2005), 551–559.

[31] Dimos, D., Raymond, M., Schwartz, R., Al-Shareef, H., and Mueller, C. Tunability and calculation of the dielectric constant of capacitor structures with interdigital electrodes. *Journal of Electroceramics 1* (1997), 145–153.

[32] Du, P., Li, X., Liu, Y., Han, G., and Weng, W. Effect of la doping on tunable behavior of solgel-derived pst thin film. *Journal of the European Ceramic Society 26* (2006), 2147 – 2150.

[33] Dubois, M. A., Billard, C., Muller, C., Parat, G., and Vincent, P. Integration of high-q baw resonators and filters above ic. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International* (2005), vol. 1, pp. 392 –606.

[34] Elbrecht, L., Aigner, R., Lin, C.-I., and Timme, H.-J. Integration of bulk acoustic wave filters: concepts and trends. In *Microwave Symposium Digest, 2004 IEEE MTT-S International* (2004), vol. 1, pp. 395 – 398.

[35] Fan, W., Saha, S., Carlisle, J. A., Auciello, O., Chang, R. P. H., and Ramesh, R. Layered cu-based electrode for high-dielectric constant oxide thin film-based devices. *Applied Physics Letters 82* (2003), 1452 – 1454.

[36] Fragkiadakis, C., Luker, A., Wright, R. V., Floyd, L., and Kirby, P. B. Growth and high frequency characterization of mn doped sol-

gel pbxsr1-xtio3 for frequency agile applications. *Journal of Applied Physics 105* (2009), 061635 –061635–7.

[37] Frederick, A., Su, H., and W.W., C. Frequency tuning of film bulk acoustic resonators. In *Proc. SPIE Smart Structures and Materials 2006* (2006), vol. 61, p. 7203.

[38] Frickey, D. Conversions between s, z, y, h, abcd, and t parameters which are valid for complex source and load impedances. *Microwave Theory and Techniques, IEEE Transactions on 42* (1994), 205 –211.

[39] Gevorgian, S. Basic characteristics of two layered substrate coplanar waveguides. *Electronics Letters 30* (1994), 1236 –1237.

[40] Gevorgian, S., Berg, H., Jacobsson, H., and Lewin, T. Application notes - basic parameters of coplanar-strip waveguides on multilayer dielectric/semiconductor substrates, part 1: high permittivity superstrates. *Microwave Magazine, IEEE 4* (2003), 60 – 70.

[41] Gevorgian, S., Kaparkov, D., and Vendik, O. Electrically controlled htsc/ferroelectric coplanar waveguide. *Microwaves, Antennas and Propagation, IEE Proceedings - 141* (1994), 501 –503.

[42] Gevorgian, S., Linner, L., and Kollberg, E. Cad models for shielded multilayered cpw. *Microwave Theory and Techniques, IEEE Transactions on 43* (1995), 772 –779.

[43] Gevorgian, S., Vorobiev, A., and Berge, J. Electromechanical modelling and reduction of the electroacoustic losses in parallel-plate ferroelectric varactors. In *Microwave Conference, 2006. 36th European* (2006), pp. 851 –853.

[44] Gevorgian, S., Vorobiev, A., and Lewin, T. dc field and temperature dependent acoustic resonances in parallel-plate capacitors based on srtio3 and ba0.25sr0.75tio3 films: Experiment and modeling. *Journal of Applied Physics 99* (2006), 124112 –124112–11.

[45] Guerre, R., Drechsler, U., Bhattacharyya, D., Rantakari, P., Stutz, R., Wright, R., Milosavljevic, Z., Vaha-Heikkila, T., Kirby, P., and Despont, M. Wafer-level transfer technologies for pzt-based rf mems switches. *Microelectromechanical Systems, Journal of 19* (2010), 548 –560.

[46] Ha, B., Song, I., Park, Y., Kim, D., Kim, W., Nam, K., and Pak, J. J. Novel 1-chip fbar filter for wireless handsets. In *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on* (2005), vol. 2, pp. 2069 – 2073.

[47] Hakki, B., and Coleman, P. A dielectric resonator method of measuring inductive capacities in the millimeter range. *Microwave Theory and Techniques, IRE Transactions on 8* (1960), 402 –410.

[48] Heinrich, W. Quasi-tem description of mmic coplanar lines including conductor-loss effects. *Microwave Theory and Techniques, IEEE Transactions on 41* (1993), 45 –52.

[49] Heinze, H., Schmidhammer, E., Diekmann, C., and Metzger, T. 3.8 x 3.8 mm2 pcs-cdma duplexer incorporating thin film resonator technology. In *Ultrasonics Symposium, 2004 IEEE* (2004), vol. 1, pp. 425 – 428.

[50] Hilberg, W. From approximations to exact relations for characteristic impedances. *Microwave Theory and Techniques, IEEE Transactions on 17* (1969), 259 – 265.

[51] Hongtao, X., Pervez, N. K., and York, R. A. Tunable microwave integrated circuits using bst thin film capacitors with device structure optimization. *Integrated Ferroelectrics 77* (2005), 27–35.

[52] Hosseini, M., Zhu, G., and Peter, Y.-A. A new formulation of fringing capacitance and its application to the control of parallel-plate electrostatic micro actuators. *Analog Integr. Circuits Signal Process. 53* (2007), 119–128.

[53] Huang, C.-L., Tay, K.-W., and Wu, L. Effect of aln film thickness and top electrode materials on characteristics of thin-film bulk acoustic-wave resonator devices. *Japanese Journal of Applied Physics 44* (2005), 1397–1402.

[54] Hunter, I., and Rhodes, J. Electronically tunable microwave bandstop filters. *Microwave Theory and Techniques, IEEE Transactions on 30* (1982), 1361 –1367.

[55] Imanaka, Y., Shioga, T., and Baniecki, J. Decoupling capacitor with low inductance for high-frequency digital applications. *FUJITSU Sci. Tech. J. 38(1)* (2002), 22–30.

[56] JAIN, M., KARAN, N. K., KATIYAR, R. S., and BHALLA, A. S. Synthesis and characterization of lead strontium titanate thin films by chemical solution technique. *Integrated Ferroelectrics 82* (2006), 55–64.

[57] Janezic, M., and Williams, D. Permittivity characterization from transmission-line measurement. In *Microwave Symposium Digest, 1997., IEEE MTT-S International* (1997), vol. 3, pp. 1343 –1346.

[58] Jona, F., and Shirane, G. *Ferroelectric Crystals*. New York, 1993.

[59] Jondral, F. K. Software-defined radio: basics and evolution to cognitive radio. *EURASIP J. Wirel. Commun. Netw.* (2005), 275–283.

[60] Kajfez, D., and Guillon, P. *Dielectric Resonators*. Artech House, 1986.

[61] Kang, B., Cho, J., Cheon, C., and Kwon, Y. Nondestructive measurement of complex permittivity and permeability using multilayered coplanar waveguide structures. *Microwave and Wireless Components Letters, IEEE 15* (2005), 381 – 383.

[62] Karyamapudi, B., and Hong, J.-S. Coplanar waveguide periodic structures with resonant elements and their application in microwave filters. In *Microwave Symposium Digest, 2003 IEEE MTT-S International* (2003), vol. 3, pp. 1619 – 1622.

[63] Karyamapudi, B.M., B. M., and Hong, J. S. Characterization and applications of a compact cpw defected ground structure. *Microwave and Optical Technology Letters 47* (2005), 26–31.

[64] Kennedy, M., Moody, N., Adams, D., Clift, M., and Bahr, D. Environmental influence on interface interactions and adhesion of au/sio2. *Materials Science and Engineering: A 493* (2008), 299 – 304.

[65] Khalfallaoui, A., Velu, G., Burgnies, L., and Carru, J. Characterization of doped bst thin films deposited by sol-gel for tunable microwave devices. In *Frequency Control Symposium, 2009 Joint with the 22nd European Frequency and Time forum. IEEE International* (2009), pp. 295 –298.

[66] Kim, C.-S., Lim, J.-S., Nam, S., Kang, K.-Y., Park, J.-I., Kim, G.-Y., and Ahn, D. The equivalent circuit modeling of defected ground

structure with spiral shape. In *Microwave Symposium Digest, 2002 IEEE MTT-S International* (2002), vol. 3, pp. 2125 –2128.

[67] Kim, C.-S., Park, J.-S., Ahn, D., and Lim, J.-B. A novel 1-d periodic defected ground structure for planar circuits. *Microwave and Guided Wave Letters, IEEE 10* (2000), 131 –133.

[68] Kim, H.-T., Lee, H.-M., Choi, H.-K., Park, J.-Y., Bu, J.-U., and Lee, K. A thermally driven tunable tfbar bandpass filter. In *Microwave Conference, 2004. 34th European* (2004), vol. 1, pp. 491 – 494.

[69] Kim, J.-Y., and Grishin, A. M. Processing and on-wafer test of ferroelectric film microwave varactors. 192905.

[70] Kim, T., and Seo, C. A novel photonic bandgap structure for low-pass filter of wide stopband. *Microwave and Guided Wave Letters, IEEE 10* (2000), 13 –15.

[71] Kingsley, N., Ponchak, G., and Papapolymerou, J. Reconfigurable rf mems phased array antenna integrated within a liquid crystal polymer (lcp) system-on-package. *Antennas and Propagation, IEEE Transactions on 56* (2008), 108 –118.

[72] Kirby, P., Su, Q., Komuro, E., Zhang, Q., Imura, M., and Whatmore, R. Pzt thin film bulk acoustic wave resonators and filters. In *Frequency Control Symposium and PDA Exhibition, 2001. Proceedings of the 2001 IEEE International* (2001), pp. 687 –694.

[73] Kiziloglu, K., Dagli, N., Matthaei, G., and Long, S. Experimental analysis of transmission line parameters in high-speed gaas digital circuit interconnects. *Microwave Theory and Techniques, IEEE Transactions on 39* (1991), 1361 –1367.

[74] Kuylenstierna, D., Vorobiev, A., and Gevorgian, S. 40 ghz lumped element tunable bandpass filters with transmission zeros based on thin ba/sup 0.25/sr/sup 0.75/tio/sup 3/ (bst) film varactors. In *Silicon Monolithic Integrated Circuits in RF Systems, 2006. Digest of Papers. 2006 Topical Meeting on* (2006), p. 4 pp.

[75] Lakin, K. Modeling of thin film resonators and filters. In *Microwave Symposium Digest, 1992., IEEE MTT-S International* (1992), vol. 1, pp. 149 –152.

[76] Lakin, K. Coupled resonator filters. In *Ultrasonics Symposium, 2002. Proceedings. 2002 IEEE* (. 2002), vol. 1, pp. 901 – 908.

[77] Lakin, K., Andrus, C., Belsick, J., McCarron, K., and Thornhill, W. Wide bandwidth thin film baw filters. In *Ultrasonics Symposium, 2004 IEEE* (2004), vol. 1, pp. 407 – 410.

[78] Lakin, K., Kline, G., and McCarron, K. High q microwave acoustic resonators and filters. In *Microwave Symposium Digest, 1993., IEEE MTT-S International* (1993), vol. 3, pp. 1517 –1520.

[79] Lakin, K. M., and Wang, J. S. Acoustic bulk wave composite resonators. *Applied Physics Letters 38* (1981), 125–127.

[80] Larson, J.D., I., Bradley, P., Wartenberg, S., and Ruby, R. Modified butterworth-van dyke circuit for fbar resonators and automated measurement system. In *Ultrasonics Symposium, 2000 IEEE* (2000), vol. 1, pp. 863 –868.

[81] Lee, J., Park, S., Kim, H. C., and Chun, K. Substrates and dimension dependence of mems inductors. *Journal of Micromechanics and Microengineering 19* (2009), 085014.

[82] Lee, S.-S., Nishino, T., Yuasa, T., Yoshida, Y., and Taguchi, M. Fabrication of a novel micromachined solenoid inductor and delay line and investigation of substrate influence on their characteristics. *Journal of Micromechanics and Microengineering 16*, 6 (2006), S96.

[83] Lee, S. Y., Hummel, R., and Dehoff, R. On the role of indium underlays in the prevention of thermal grooving in thin gold films. *Thin Solid Films 149* (1987), 29 – 48.

[84] Li, X., Du, P., Zhu, L., Mak, C., and Wong, K. Structure and dielectric properties of highly (100)-oriented pst thin films deposited on mgo substrates. *Thin Solid Films 516* (2008), 5296 – 5299.

[85] Li, X., Huo, W., Mak, C., Sui, S., Weng, W., Han, G., Shen, G., and Du, P. Effect of mg doping on ferroelectric pst thin films for high tunable devices. *Materials Chemistry and Physics 108* (2008), 417 – 420.

[86] Lim, J.-S., Kim, C.-S., Lee, Y.-T., Ahn, D., and Nam, S. A spiral-shaped defected ground structure for coplanar waveguide. *Microwave and Wireless Components Letters, IEEE 12* (2002), 330 – 332.

[87] Lim, J.-S., Kim, H.-S., Park, J.-S., Ahn, D., and Nam, S. A power amplifier with efficiency improved using defected ground structure. *Microwave and Wireless Components Letters, IEEE 11* (2001), 170 –172.

[88] Lines, M. E., and Glass, A. M. *Principles and Applications of Ferroelectrics and Related Materials*.

[89] Lourandakis, E., Schmidt, M., Seitz, S., and Weigel, R. Tunable lumped element filters with bst thin-film varactors. In *Microwave Conference, 2008. EuMC 2008. 38th European* (2008), pp. 1691 –1694.

[90] Lu, Y., Katehi, L., and Peroulis, D. High-power mems varactors and impedance tuners for millimeter-wave applications. *Microwave Theory and Techniques, IEEE Transactions on 53* (2005), 3672 – 3678.

[91] Lucyszyn, S. Review of radio frequency microelectromechanical systems technology. *Science, Measurement and Technology, IEE Proceedings - 151* (2004), 93 – 103.

[92] Lucyszyn, S. *Microwave Measurements*. IET, 2007, ch. 11. RFIC and MMIC Measurement Techniques, pp. 217–262.

[93] Luther Davis, J., and Rubin, L. G. Some dielectric properties of barium-strontium titanate ceramics at 3000 megacycles. *Journal of Applied Physics 24*, 9 (1953), 1194–1197.

[94] Maddela, M., Ramadoss, R., and Lempkowski, R. A mems-based tunable coplanar patch antenna fabricated using pcb processing techniques. *Journal of Micromechanics and Microengineering 17* (2007), 812.

[95] Mancini, N., and Rimini, E. Annealing of polycrystalline au and au-ag thin films. *Surface Science 22* (1970), 357 – 364.

[96] Mantese, J. V., and Alpay, S. P. *Graded ferroelectrics, transpacitors, and transponents*. Springer, 2005, ch. Strain-gradient induced GFDs, pp. 84–88.

[97] Marks, R. A multiline method of network analyzer calibration. *Microwave Theory and Techniques, IEEE Transactions on 39* (1991), 1205 – 1215.

[98] Marks, R., Jargon, J., Pao, C., and Wen, C. Microwave characterization of flip-chip mmic components. In *Electronic Components and Technology Conference, 1995. Proceedings., 45th* (1995), pp. 343 –350.

[99] Martinez, W. E., Gregori, G., and Mates, T. Titanium diffusion in gold thin films. *Thin Solid Films 518* (2010), 2585 – 2591.

[100] Matta, F. Mems for wireless: Fbar and limms. In *Radio Science Conference, 2006. NRSC 2006. Proceedings of the Twenty Third National* (2006), vol. 0, pp. 1 –6.

[101] Meitzler, A. H., Trolier-Mckinstry, S., Ballato, J., Bhalla, A., Bloomfield, P., Cao, W., Cross, L. E., Dougherty, J. P., Fousek, J., Guo, R., Newnham, R. E., Pilgrim, S. M., Randall, C. A., and Zhang, Q. Draft 16 of a working document for a proposed standard to be entitled: Ieee standard definitions of terms associated with ferroelectric and related materials. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on 50* (2003), 1613 – 1646.

[102] Morito, K., Iwazaki, Y., Suzuki, T., and Fujimoto, M. Electric field induced piezoelectric resonance in the micrometer to millimeter waveband in a thin film srtio[sub 3] capacitor. *Journal of Applied Physics 94* (2003), 5199–5205.

[103] Mueller, W. A brief overview of fbar technology. White paper, Agilent Technol. Inc., 2001.

[104] Nakashima, S., Kanamori, S., and Izumi, K. Temperature measurement technique using pt diffusion into au for ion-implanting wafers mounted on a spinning disc. *Electronics Letters 21* (1985), 1229 –1230.

[105] Nam, H.-J., Choi, D.-K., and Lee, W.-J. Formation of hillocks in pt/ti electrodes and their effects on short phenomena of pzt films deposited by reactive sputtering. *Thin Solid Films 371* (2000), 264 – 271.

[106] Nath, J., Fathelbab, W., Franzon, P. D., Kingon, A., Ghosh, D., Maria, J. P., and Steer, M. B. A tunable combline bandpass filter using barium strontium titanate interdigital varactors on an alumina substrate. In *Microwave Symposium Digest, 2005 IEEE MTT-S International* (2005), p. 4 pp.

[107] Nath, J., Ghosh, D., Maria, J.-P., Kingon, A., Fathelbab, W., Franzon, P., and Steer, M. An electronically tunable microstrip bandpass filter using thin-film barium-strontium-titanate (bst) varactors. *Microwave Theory and Techniques, IEEE Transactions on 53* (2005), 2707 – 2712.

[108] Nguyen, C. *Analysis Methods for RF, Microwave, and Millimeter-Wave Planar Transmission Line Structures*. Wiley-Interscience, 2001.

[109] Nishihara, T., Yokoyama, T., Miyashita, T., and Satoh, Y. High performance and miniature thin film bulk acoustic wave filters for 5 ghz. In *Ultrasonics Symposium, 2002. Proceedings. 2002 IEEE* (2002), vol. 1, pp. 969 – 972.

[110] Noeth, A., Yamada, T., Sherman, V. O., Muralt, P., Tagantsev, A. K., and Setter, N. Tuning of direct current bias-induced resonances in micromachined ba0.3sr0.7tio3 thin-film capacitors. *Journal of Applied Physics 102* (2007), 114110 –114110–7.

[111] Norling, M., Kuylenstierna, D., Vorobiev, A., and Gevorgian, S. Layout optimization of small-size ferroelectric parallel-plate varactors. *Microwave Theory and Techniques, IEEE Transactions on 58* (2010), 1475 –1484.

[112] Palukuru, V., Komulainen, M., Tick, T., Perantie, J., and Jantunen, H. Low-sintering-temperature ferroelectric-thick films: Rf proper-

ties and an application in a frequency-tunable folded slot antenna. *Antennas and Wireless Propagation Letters, IEEE 7* (2008), 461 –464.

[113] Pan, W., Soussan, P., Nauwelaers, B., Mertens, R., and Tilmans, H. A comparison between tunable fbars with an integrated and with a discrete variable mems capacitor. In *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on* (2006), pp. 902 –905.

[114] Pan, W., Soussan, P., Nauwelaers, B., and Tilmans, H. Design and fabrication of a surface micromachined frequency tunable film bulk acoustic resonator with an extended electrostatic tuning range. In *Ultrasonics Symposium, 2005 IEEE* (2005), vol. 3, pp. 1840 – 1843.

[115] Pan, W., Soussan, P., Nauwelaers, B., and Tilmans, H. A. A surface micromachined electrostatically tunable film bulk acoustic resonator. *Sensors and Actuators A: Physical 126* (2006), 436 – 446.

[116] Pang, W., Yu, H., Zhang, H., and Kim, E. S. Electrically tunable and temperature compensated fbar. In *Microwave Symposium Digest, 2005 IEEE MTT-S International* (2005), p. 4 pp.

[117] Pang, W., Zhang, H., Yu, H., Lee, C.-Y., and Kim, E. S. Electrical frequency tuning of film bulk acoustic resonator. *Microelectromechanical Systems, Journal of 16* (2007), 1303 –1313.

[118] Park, H.-S., Lee, J., Shin, J., Kwon, J., Sul, S., hwan Kim, D., Shin, K.-J., Gu, M.-K., and Song, I. Newly developed high q fbar with mesa-shaped membrane. In *Microwave Conference, 2006. 36th European* (2006), pp. 1281 –1283.

[119] Park, J.-I., Kim, C.-S., Kim, J., Park, J.-S., Qian, Y., Ahn, D., and Itoh, T. Modeling of a photonic bandgap and its application for the low-pass filter design. In *Microwave Conference, 1999 Asia Pacific* (1999), vol. 2, pp. 331 –334.

[120] Park, J. Y., Lee, H. C., Lee, K. H., Ko, Y. J., and Bu, J. U. Silicon bulk micromachined fbar filters for w-cdma applications. In *Microwave Conference, 2003. 33rd European* (2003), pp. 907 –910.

[121] Pervez, N., Hansen, P., and York, R. Optimization of high tunability barium strontium titanate thin films grown by rf magnetron sputtering. In *Applications of Ferroelectrics, 2004. ISAF-04. 2004 14th IEEE International Symposium on* (2004), pp. 278 – 280.

[122] Pervez, N. K., Hansen, P. J., and York, R. A. High tunability barium strontium titanate thin films for rf circuit applications. *Applied Physics Letters 85* (2004), 4451 –4453.

[123] Pervez, N. K., and York, R. A. Geometry-dependent quality factors in ba0.5sr0.5tio3 parallel-plate capacitors. *Microwave Theory and Techniques, IEEE Transactions on 55* (2007), 410 –417.

[124] Piquet, J., Bermond, C., Thomas, M., Flchet, B., Farcy, A., Vo, T., Lacrevaz, T., Torres, J., Cueto, O., and Angnieux, G. High frequencies characterization of cu-mim capacitors in parallel configuration for advanced integrated circuits. *Microelectronic Engineering 83* (2006), 2341 – 2345.

[125] Pozar, D. M. Introduction to microwave systems. In *Microwave Engineering*, 2 ed. Wiley, 1998, ch. 12, pp. 655–696.

[126] Pyun, S.-I., Yoon, Y.-G., Lugscheider, E., and Mathesius, R. Relationship between interfacial reaction and adhesion at pvd tio2 film-metal (ti or al) interfaces. *Surface and Coatings Technology 61* (1993), 233 – 237.

[127] Qian, Y., Radisic, V., and Itoh, T. Simulation and experiment of photonic band-gap structures for microstrip circuits. In *Microwave Conference Proceedings, 1997. APMC '97, 1997 Asia-Pacific* (1997), vol. 2, pp. 585 –588.

[128] R. Kulke, P. Pogatzki, D. K. T. S., and Wolff, I. In *Proc. 24th European Microwave Conf. Dig.* (1994), vol. 1, p. 258262.

[129] Ramo, S., W. J., and Van Duzer, T. *Fields and Waves in Communications Electronics*, 1 ed. John Wiley, 1965.

[130] Rebeiz, G. *RF MEMS: Theory, Design, and Technology.* Wiley, 2003.

[131] Riekkinen, T., Molarius, J., and Ylilammi, M. Electrode metallization for high permittivity oxide rf thin film capacitors. *Journal of the European Ceramic Society 27* (2007), 2983 – 2987.

[132] Rosenbaum, J. F. *Bulk Acoustic Wave Theory and Devices.* Artech House, 1945.

[133] Rosn, D. *Studies of the Reactive Sputtering Process and its Application in Electro-Acoustic Devices.* PhD thesis, Uppsala University, 2006.

[134] Ruby, R. Fbar from technology development to production. In *2d International Symposium on Acoustic Wave Devices for Future Mobile Communication Systems* (2004).

[135] Ruby, R. Review and comparison of bulk acoustic wave fbar, smr technology. In *Ultrasonics Symposium, 2007. IEEE* (2007), pp. 1029 –1040.

[136] Ruby, R., Barfknecht, A., Han, C., Desai, Y., Geefay, F., Gan, G., Gat, M., and Verhoeven, T. High-q fbar filters in a wafer-level chip-scale package. In *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International* (2002), vol. 2, pp. 142 –440.

[137] Ruby, R., Bradley, P., Larson, J.D., I., and Oshmyansky, Y. Pcs 1900 mhz duplexer using thin film bulk acoustic resonators (fbars). *Electronics Letters 35* (1999), 794 –795.

[138] Ruby, R., Bradley, P., Oshmyansky, Y., Chien, A., and Larson, J.D., I. Thin film bulk wave acoustic resonators (fbar) for wireless applications. In *Ultrasonics Symposium, 2001 IEEE* (2001), vol. 1, pp. 813 –821.

[139] Rumsey, I., Piket-May, M., and Kelly, P. Photonic bandgap structures used as filters in microstrip circuits. *Microwave and Guided Wave Letters, IEEE 8* (1998), 336 –338.

[140] Rupprecht, G., and Bell, R. O. Microwave losses in strontium titanate above the phase transition. *Phys. Rev. 125* (1962), 1915–1920.

[141] Sallese, J.-M., and Fazan, P. Switch and rf ferroelectric mems: a new concept. *Sensors and Actuators A: Physical 109* (2004), 186 – 194.

[142] Scheele, P., Goelden, F., Giere, A., Mueller, S., and Jakoby, R. Continuously tunable impedance matching network using ferroelectric varactors. In *Microwave Symposium Digest, 2005 IEEE MTT-S International* (2005), p. 4 pp.

[143] Shaman, H., and Hong, J.-S. Asymmetric parallel-coupled lines for notch implementation in uwb filters. *Microwave and Wireless Components Letters, IEEE 17* (2007), 516 –518.

[144] Sheng, S., Zhang, X.-Y., Wang, P., and Ong, C. Effect of bottom electrodes on dielectric properties of high frequency ba0.5sr0.5tio3 parallel plate varactor. *Thin Solid Films 518* (2010), 2864 – 2866.

[145] Sinha, A., Smith, T., and Sheng, T. Thin film diffusion of platinum in gold. *Thin Solid Films 22* (1974), 1 – 10.

[146] Sinharoy, S., Buhay, H., Lampe, D. R., and Francombe, M. H. Integration of ferroelectric thin films into nonvolatile memories. vol. 10, AVS, pp. 1554–1561.

[147] Somiya, Y., Bhalla, A. S., and Cross, L. Study of (sr, pb)tio3 ceramics on dielectric and physical properties. *International Journal of Inorganic Materials 3* (2001), 709 – 714.

[148] Steer, M., Palmer, W., and York, R. *Multifunctional Adaptive Microwave Circuits and Systems*. Scitech Publishing, 2009, ch. Tunable Dielectric Materials.

[149] Stojanovic, G., Damnjanovic, M., Desnica, V., Zivanov, L., Raghavendra, R., Bellew, P., and Mcloughlin, N. High-performance zig-zag and meander inductors embedded in ferrite material. *Journal of Magnetism and Magnetic Materials 297* (2006), 76 – 83.

[150] Su, Q., Kirby, P., Komuro, E., and Whatmore, R. Edge supported zno thin film bulk acoustic wave resonators and filter design. In *Frequency Control Symposium and Exhibition, 2000. Proceedings of the 2000 IEEE/EIA International* (2000), pp. 434 –440.

[151] Subramanyam, G., Ahamed, F., and Biggers, R. A si mmic compatible ferroelectric varactor shunt switch for microwave applications. *Microwave and Wireless Components Letters, IEEE 15* (2005), 739 – 741.

[152] Subramanyam, G., Heckman, E., Grote, J., and Hopkins, F. Microwave dielectric properties of dna based polymers between 10 and 30 ghz. *Microwave and Wireless Components Letters, IEEE 15* (2005), 232 – 234.

[153] Subramanyam, G., Heckman, E., Grote, J., Hopkins, F., Neidhard, R., and Nykiel, E. Microwave dielectric properties of marine dna based polymers. *Microwave and Optical Technology Letters 46* (2005), 278–282.

[154] Subramanyam, G., Neidhard, R., Stamper, K., and Calcatera, M. Improved rf performance characteristics of cascaded ferroelectric varactor shunt switches. In *Applications of ferroelectrics, 2006. isaf '06. 15th ieee international symposium on the* (2006), pp. 352 –355.

[155] Sucher, M., and Fox, J. *Handbook of Microwave Measurements*, vol. 2. Interscience, New York, 1963.

[156] SUZUKI, T., MORITO, K., and IWAZAKI, Y. The latest advances in high-dielectric thin-film capacitor technology for ghz-rf devices. *Integrated Ferroelectrics 76* (2005), 47–57.

[157] Sze, S. M. *Physics of semiconductor devices.* Wiley, 1936.

[158] Tagantsev, A. K., and F., A. K. Intrinsic limitation for microwave performance of a tunable component based on srtio3 and baxsr1-xtio3 ferroelectrics. In *Proc. of StPetersburg Electrotech. Univ., Ser. Solid State Phys. and Electronics* (2002), pp. 204–220.

[159] Tagantsev, A. K., Sherman, V. O., Astafiev, K. F., Venkatesh, J., and Setter, N. *J. Electroceram. 11*, 5–20.

[160] Tagantsev, A. K., S. V. O. A. K. F. V. J., and Setter, N. Ferroelectric materials for microwave tunable applications. *Journal of Electroceramics 11*, 1/2 (2003), 5–66.

[161] Tiggelman, M., Reimann, K., Klee, M., Beelen, D., Keur, W., Schmitz, J., and Hueting, R. Electrical characterization of thin film ferroelectric capacitors. In *Proceedings of the 9th annual workshop on Semiconductor Advances for Future Electronics and Sensors 2006* (2006), pp. 439–443.

[162] Tiggelman, M., Reimann, K., Van Rijs, F., Schmitz, J., and Hueting, R. On the trade-off between quality factor and tuning ratio in tunable high-frequency capacitors. *IEEE Transactions on Electron Devices 56* (2009), 2128–2136.

[163] Tilmans, H. A. C. Rf-mems: An enabling technology for reconfigurable radio front-ends. In *Proc. 29th Int. Union Radio Science* (2008).

[164] Tombak, A., Maria, J.-P., Ayguavives, F., Jin, Z., Stauf, G., Kingon, A., and Mortazawi, A. Voltage-controlled rf filters employing thin-film barium-strontium-titanate tunable capacitors. *Microwave Theory and Techniques, IEEE Transactions on 51* (2003), 462 – 467.

[165] Van Keuls, F. W., Chevalier, C. T., Miranda, F. A., Carlson, C. M., Rivkin, T. V., Parilla, P. A., Perkins, J. D., and Ginley, D. S. Comparison of the experimental performance of ferroelectric cpw circuits with method-of-moment simulations and conformal mapping analysis. *Microwave and Optical Technology Letters 29* (2001), 34–37.

[166] Verma, A., Nasimuddin, and Singh, H. Dielectric loss of multilayer coplanar waveguide using the single layer reduction (slr) formulation. In *Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings* (dec. 2005), vol. 1, p. 3 pp.

[167] Verma, A. K., and Bhupal, A. Dielectric loss of multilayer microstrip line. *Microwave and Optical Technology Letters 17* (1998), 368–370.

[168] VEYRES, C., and FOUAD HANNA, V. Extension of the application of conformal mapping techniques to coplanar lines with finite dimensions. *International Journal of Electronics 48* (1980), 47–56.

[169] von Hippel, A. *Dielectrics and Waves.* Wiley, 1954.

[170] Vorobiev, A., Rundqvist, P., Khamchane, K., and Gevorgian, S. Silicon substrate integrated high q-factor parallel-plate ferroelectric varactors for microwave/millimeterwave applications. *Applied Physics Letters 83* (2003), 3144 –3146.

[171] Wang, J. S., and Lakin, K. M. Low-temperature coefficient bulk acoustic wave composite resonators. *Applied Physics Letters 40* (1982), 308–310.

[172] Wei, C., and Chen, C.-H. The effect of thermal and plastic mismatch on stress distribution in diamond like carbon film under different interlayer/substrate system. *Diamond and Related Materials 17* (2008), 1534 – 1540.

[173] Wei, C., Yang, J.-F., and Tai, F.-C. The stress reduction effect by interlayer deposition or film thickness for diamond like carbon on rough surface. *Diamond and Related Materials 19* (2010), 518 – 524.

[174] Williams, D., and Marks, R. Accurate transmission line characterization. *Microwave and Guided Wave Letters, IEEE 3* (1993), 247 –249.

[175] Williams, D., Wang, C., and Arz, U. An optimal multiline trl calibration algorithm. In *Microwave Symposium Digest, 2003 IEEE MTT-S International* (2003), vol. 3, pp. 1819 – 1822.

[176] Williams, D., Wang, J., and Arz, U. An optimal vector-network-analyzer calibration algorithm. *Microwave Theory and Techniques, IEEE Transactions on 51* (2003), 2391 – 2401.

[177] Wright, P. A review of saw resonator filter technology. In *Ultrasonics Symposium, 1992. Proceedings., IEEE 1992* (1992), vol. 1, pp. 29 –38.

[178] Xu, H., Pervez, N., and York, R. A. Tunable microwave integrated circuits using bst thin film capacitors with device structure optimization. *Integrated Ferroelectrics 77* (2005), 27–35.

[179] Xu, Y. *Ferroelectric Materials and their applications.* North-Holland Elsevier, 1991.

[180] Y.G. Wang, M.E. Reeves, W. C. H., and Kim, W. In *Materials Research Sosiety Symposium Proceedings,* (2000), vol. 603, p. 289.

[181] You, H.-W., and Koh, J.-H. Ag(ta,nb)o3 thin-film interdigital capacitors for microwave applications. *Microelectronics Journal 38* (2007), 222 – 226.

[182] Yun, J.-S., Kim, G.-Y., Park, J.-S., Ahn, D., Kang, K.-Y., and Lim, J.-B. A design of the novel coupled line bandpass filter using defected ground structure. In *Microwave Symposium Digest. 2000 IEEE MTT-S International* (2000), vol. 1, pp. 327 –330.

[183] Yun-Kwon, P., Kuang-Woo, N., Seok-Chool, Y., Byeoung-Ju, H., Seog-Woo, H., Chul-Soo, K., Jea-Shik, S., and In-Sang, S. Fabrication of monolithic 1-chip fbar duplexer for w-cdma handsets. In

*Micro Electro Mechanical Systems, 2007. MEMS. IEEE 20th International Conference on* (2007), pp. 803 –806.

[184] Zhao, J.-X. Characteristic parameters for cpws on a very thin dielectric layer. *Microwave and Optical Technology Letters 45* (2005), 240–241.

[185] Zhu, X. *Switchable and Tunable Ferroelectric Thin Film Radio Frequency Components*. PhD thesis, University of Michigan, 2009.

[186] Zhu, X., Chen, D.-Y., Jin, Z., Phillips, J., and Mortazawi, A. Characterization of thin film bst tunable capacitors using a simple two port measurement technique. In *Microwave Symposium Digest, 2005 IEEE MTT-S International* (2005), p. 4 pp.

[187] Zhu, X., Phillips, J., and Mortazawi, A. A dc voltage dependant switchable thin film bulk wave acoustic resonator using ferroelectric thin film. In *Microwave Symposium, 2007. IEEE/MTT-S International* (2007), pp. 671 –674.

[188] Zinck, C., Defay, E., Volatier, A., Caruyer, G., Tanor, D., and Figuiere, L. Design, integration and characterization of pzt tunable fbar. In *Applications of Ferroelectrics, 2004. ISAF-04. 2004 14th IEEE International Symposium on* (2004), pp. 29 – 32.

# Appendices

# A-1 MATLAB Code : Dielectric properties extraction from S-parameter measurements of CPW on ferroelectric thin films

```
% MATLAB program for Thin Film dielectric constant calculation
% TL partial capacitance technique using conformal mapping
%
%   Conventional CPW on a thin film/single substrate substrate - Air/CPW/Thin Film/Substrate
%   Finite grounds taken into account
%   Based on Quasi-static Conformal Mapping Techniques to determine Effective
%   Dielectric constant and Characteristic impedance


% Assumptions :
%
%        CPW conductors and dielectric substrates assumed to have perfect
% conductivity and relatiive permittivity. Structure considered to be
% lossless.
%        Dielectric substrate materials are considered to be isotropic.
%        Conductor thickness t=0 and magnetic walls are present along all
%        the dielectric boundaries, including CPW slots.

% RLGC extraction from S-parameter file
Up_to =6; % Up to Frequency (GHz)

%Insert directory of TL .s2p file here
directory='c:\';  %Directory Read

%Insert file here and Transmission Line length
TL_length = 6*1e-3;  % In mm
s2p=[directory '6mmAu200nm-PST.s2p'];
file=dir(s2p);
filename=[directory file.name];
data =rfdata.data;
read(data,filename);

%Load S-Parameters into matrices
freq= data.Freq;
S_Param =extract(data,'S_PARAMETERS');
```

```
s11=S_Param(1,1,:);
s21=S_Param(2,1,:);
s12=S_Param(1,2,:);
s22=S_Param(2,2,:);
wmega=2*pi.*freq;

%Conversion in dB
s11dB=20*log10(abs(s11));
s21dB=20*log10(abs(s21));

%Get ABCD parameters
Z0=50;
ABCD_Params = s2abcd(S_Param, Z0);

%Get Charachteristic Impedance (Z0l)
for a=1:1601
    Z0l(a)= sqrt(ABCD_Params(1,2,a)/ABCD_Params(2,1,a));
end

%Get Propagation Constant
for a=1:1601
    Propagation1(a)= (1/TL_length)*acosh(ABCD_Params(1,1,a));
end

%Get RLGC Data
for a=1:1601
    R_RLGC(a)=real(Propagation1(a)*Z0l(a));
    L_RLGC(a)=imag((Propagation1(a)*Z0l(a))/(2*pi*freq(a)));
    G_RLGC(a)=real(Propagation1(a)/Z0l(a));
    C_RLGC(a)=(imag((Propagation1(a)/Z0l(a)))/(2*pi*freq(a)));
end

% Conformal Mapping Simulation of same CPW

% Global Constants
e0 = 8.8541878176 *1e-12;                % Permittivity of free space
c_light = 3*1e8;                         % Velocity of light

% Set dielectric constants and heights of films and substrate
h_substrate =500 *1e-6;
e_substrate= 10.1;
tanD_sub=0.0005;
h_film = 300*1e-9;
```

```
e_film = 300;

%Heights used in calculations
h1=h_substrate; %   Substrate
h2=h_film;      %   Film

%Set diemnsional size of CPW (in mm)
S = 0.1*1e-3;            % Width of CPW
a=S/2;
W = 0.08*1e-3;           % Gap
th=200*1e-9;
%W=W+(th/pi)*(1+log(4*pi*W/th))
b=(S+2*W)/2;
FG=0.37*1e-3;            % Finite ground width
c=(S+2*W+2*FG)/2;


% Filling factors for finite-width ground planes

% In absence of all dielectric layers (Air)
k = (c/b)*sqrt((b^2-a^2)/(c^2-a^2));
kd = sqrt(1-(k^2));

%   Substrate
k1=(sinh((pi*c)/(2*h1))/sinh((pi*b)/(2*h1)))*sqrt((((sinh((pi*b)/(2*h1)))^2)
-((sinh((pi*a)/(2*h1)))^2))/(((sinh((pi*c)/(2*h1)))^2)-((sinh((pi*a)/(2*h1)))^2)));
k1d=sqrt(1-(k1^2));

% Elliptic Integrals Ratios calculation

%Air
Kk=ellipk(k);
Kkd=ellipk(kd);
Kk1=ellipk(k1);
Kk1d=ellipk(k1d);
k_kd_ratio =Kk/Kkd;
k1_k1d_ratio =Kk1/Kk1d;

%  Film
k2_k2d_ratio=W/h2;
% k2_k2d_ratio2=(log(16)/pi)+(h2/W);

% Partial Capacitances calculation
```

```
%C_air = 4*e0*(Kkd/Kk)           % Calculation of C_air : Partial capacitance in absence of all layers
C_air = 4*e0*(1/k_kd_ratio)

%C1 = 2*e0*(e_substrate-1)*(Kk1d/Kk1)    % Calculation of C1 : Partial capacitance with only substrate
C1=2*e0*(e_substrate-1)*(1/k1_k1d_ratio)
% G1=2*e0*(e_substrate-1)*(1/k1_k1d_ratio)
C2 = 2*e0*(e_film-e_substrate)*(1/k2_k2d_ratio)
c_Calc_Measurements=C_RLGC(10)

% Total Capacitance of CPW
C_CPW = C1  + C2 + C_air

for ss=1:1601
e_calc(ss)=e_substrate+((C_RLGC(ss)-C_air-C1)/(2*e0*(1/k2_k2d_ratio)));
end

for a=1:1601
    tanD(a)=G_RLGC(a)/((2*pi*freq(a)*C_RLGC(a)));
    C1pF(a)=C1*1e12;
    C_airpF(a)=C_air*1e12;
    C_CPWpF(a)=C_CPW*1e12;
    C_RLGCpF(a)=C_RLGC(a)*1e12;
    C2pF(a)=C2*1e12;

%Partial Conductance
    tanD_PST(a)=  ((((G_RLGC(a)/2*pi*freq(a)*2*e0)-
    (tanD_sub*e_substrate*(1/k1_k1d_ratio)))/(1/k2_k2d_ratio))+(tanD_sub*e_substrate))/e_film;
end

figure(1)
plot(freq/1e9,C_RLGCpF,freq/1e9,C_CPWpF,freq/1e9,C1pF,freq/1e9,C_airpF,freq/1e9,C2pF)
legend('Measured Capacitance of whole CPW','Calculated Capacitance of whole CPW'
,'Calculated Capacitance of substrate','Calculated Capacitance in absence of all dielectrics'
,'Calculated Capacitance of thin fiml PST');
TITLE('Measured Distributed Capacitance Vs Calculated Distributed Capacitance of whole CPW')
XLABEL('Frequency (GHz)')
YLABEL('Distributed Capacitance (pF/m)')
axis([1 Up_to 0 250])

figure(2)
plot(freq/1e9,e_calc,'r')
TITLE('Calculated dielectric constant of substrate from measurements')
XLABEL('Frequency (GHz)')
```

```
YLABEL('Dielectric Constant')
axis([1 Up_to 0 600])

figure(3)
plot(freq/1e9,tanD,'r')
TITLE('Calculated dielectric loss of substrate from measurements')
XLABEL('Frequency (GHz)')
YLABEL('Dielectric Loss')
axis([1 Up_to 0 0.2])

% e_eff - UNDER QUASI-STATIC APPROXIMATION [alternate calculation/compare with above]
   e_eff = C_CPW/C_air
   U_ph = c_light / sqrt(e_eff);
   Z0= 1/(C_CPW*U_ph)

% Partial Filling Factors
%q1=  (1/2)*(k1_k1d_ratio)*(1/k_kd_ratio);
e_eff = 1+(1/2)*(e_substrate-1)*(k_kd_ratio*(1/k1_k1d_ratio))
+(1/2)*(e_film-e_substrate)*(k_kd_ratio*(1/k2_k2d_ratio))% For CPW on multilayer dielectrics
%e_eff = 1+(1/2)*(e_substrate-1)*(k_kd_ratio*(1/k1_k1d_ratio))% For CPW on multilayer dielectrics
Z0 = 1/(c_light*C_air*sqrt(e_eff)) % Absolute Value
Z0 = ((30*pi)/(sqrt(e_eff)))*(k_kd_ratio) % Used in papers ~ absolute value
% e_eff = C_CPW/C_air

figure(4)
plot(freq/1e9,tanD_PST,'r',freq/1e9,tanD_sub,'b',freq/1e9,tanD,'k')
TITLE('tanD_PST')
XLABEL('Frequency (GHz)')
YLABEL('Dielectric Loss')
axis([1 Up_to -0.05 0.05])

figure(5)
plot(freq/1e9,G_RLGC)
TITLE('tanD_PST')
XLABEL('Frequency (GHz)')
YLABEL('Dielectric Loss')
```

# A-2 MATLAB Code : CPW MIM series electrode ($R_s$, $L_s$) extraction from CPW MIM short test structure

```
num=201;
% Transmission line length left and right from the DUT
TL_length_L=0.25 *1e-3;
TL_length_R=0.25 *1e-3;
TL_length_through=1 *1e-3;

% Read THROUGH s2p file
directory='C:\';  %Directory to Read
s2p=[directory 'SHORT.S2P'];
file=dir(s2p);
filename=[s2p];
data =rfdata.data;
read(data,filename);

% Extract of THROUGH S-Parameters / Y-Parameters
freq_through= data.Freq;
S_Param_through =extract(data,'S_PARAMETERS');
S11_through=S_Param_through(1,1,:);
S21_through=S_Param_through(2,1,:);
%Y_Param_through = s2y(S_Param_through, 50);
%Y11_through=Y_Param_through(1,1,:);
%Y12_through=Y_Param_through(1,2,:);

% Conversion in dB
S11dB_through=20*log10(abs(S11_through));
S21dB_through=20*log10(abs(S21_through));

%Get ABCD parameters and charachteristic impedance from THROUGH
Z0=50;
ABCD_Params_through = s2abcd(S_Param_through, Z0);
for a=1:num
    Z0l(a)= sqrt(ABCD_Params_through(1,2,a)/ABCD_Params_through(2,1,a));
end

%Get Propagation Constant
for a=1:num
```

```
    Propagation(a)= (1/TL_length_through)*acosh(ABCD_Params_through(1,1,a));
end

% Calculation of interconnects matrix A_INT1 and A_INT2
for counter=1:num
    A_INT1(:,:,counter)=[cosh(Propagation(counter)*TL_length_L),Z01(counter)
    *sinh(Propagation(counter)*TL_length_L);(1/Z01(counter))
    *sinh(Propagation(counter)*TL_length_L),cosh(Propagation(counter)*TL_length_L)];
    A_INT2(:,:,counter)=[cosh(Propagation(counter)*TL_length_R),Z01(counter)
    *sinh(Propagation(counter)*TL_length_R);(1/Z01(counter))
    *sinh(Pr    opagation(counter)*TL_length_R),cosh(Propagation(counter)*TL_length_R)];
end

% Calculation of input/output matrix A_IN and A_OUT
for a=1:num
    A_IN(:,:,a)=A_INT1(:,:,a);
    A_OUT(:,:,a)=A_INT2(:,:,a);
end

% Get R_el,L_el
hold on
from=0.03;
Up_to=3; %In GHz

do=num;% Number of points
directory='C:\';  %Directory to Read
s2p=[directory 'CS10_SH.S2P'];
file=dir(s2p);
filename=[s2p];
data =rfdata.data;
read(data,filename);

% Extract of DUT S-Parameters / ABCD-Parameters
freq_dut= data.Freq;
S_Param_dut =extract(data,'S_PARAMETERS');
S11_dut=S_Param_dut(1,1,:);
S21_dut=S_Param_dut(2,1,:);
A_dut = s2abcd(S_Param_dut, 50);

% Conversion in dB
S11dB_dut=20*log10(abs(S11_dut));
S21dB_dut=20*log10(abs(S21_dut));
Y_Param_dut = s2y(S_Param_dut, 50);
```

```
Y11_dut=Y_Param_dut(1,1,:);
Y12_dut=Y_Param_dut(1,2,:);
Y21_dut=Y_Param_dut(2,1,:);
Z_Param_dut = s2z(S_Param_dut, 50);
Z11_dut=Z_Param_dut(1,1,:);
Z12_dut=Z_Param_dut(1,2,:);
Z21_dut=Z_Param_dut(2,1,:);
Z0=50;

% Inverse matric calculation
for a=1:num
    A_IN_inverse(:,:,a)=inv(A_IN(:,:,a));
    A_OUT_inverse(:,:,a)=inv(A_OUT(:,:,a));
end

% Pure ABCD extraction
for a=1:num
    A_pure(:,:,a)= A_IN_inverse(:,:,a)*A_dut(:,:,a)*A_OUT_inverse(:,:,a);
end
S_pure = abcd2s(A_pure, 50);
S11_pure=S_pure(1,1,:);
S21_pure=S_pure(2,1,:);
Y_pure = s2y(S_pure, 50);
Y11_pure=Y_pure(1,1,:);
Y12_pure=Y_pure(1,2,:);
Y21_pure=Y_pure(2,1,:);

for a=1:do
     w(a) = 2*pi*freq_dut(a);
     R_pure(a)=real(1./-Y21_dut(:,:,a));
     L_pure(a)=(imag((1./-Y21_dut(:,:,a))))/(w(a));
     R_pure2(a)=real(1./-Y21_pure(:,:,a));
     L_pure2(a)=(imag((1./-Y21_pure(:,:,a))))/(w(a));
end

figure (1)
plot(freq_dut/1e9,R_pure,'k',freq_dut/1e9,R_pure2,'r')
%axis([from Up_to 0 50])
ylabel('R_series - Resistance')
xlabel('Frequency (GHz)')
hold on

figure (2)
```

```
plot(freq_dut/1e9,L_pure*1e9,'kx',freq_dut/1e9,L_pure2*1e9,'rx')
axis([from Up_to 0 1])
ylabel('L_series - Inductance (nH)')
xlabel('Frequency (GHz)')
hold on
```

## A-3 MATLAB Code : Dielectric properties ($\epsilon_{PST}$, tan$\delta_{PST}$) extraction from CPW MIM varactor

```
% MATLAB program for De-embedding and obtaining pure DUT S-parameters
%
%    Using symbolic toolbox to solve 2 equations-2 unknowns
%    For more accurate results use R_el and L_el extracted from Appendix A-2

up_to=10; %In GHz
% Number of points
num=1601;

% Transmission line length left and right from the DUT
TL_length_L=0.4575 *1e-3;
TL_length_R=0.4575 *1e-3;
TL_length_through=1 *1e-3;

% Read OPEN s2p file
directory='C:\';  %Directory to Read
s2p=[directory 'LCS_OP.S2P'];
file=dir(s2p);
filename=[s2p];
data =rfdata.data;
read(data,filename);

% Extract of OPEN S-Parameters / Y-Parameters
freq_open= data.Freq;
S_Param_open =extract(data,'S_PARAMETERS');
S11_open=S_Param_open(1,1,:);
S21_open=S_Param_open(2,1,:);
Y_Param_open = s2y(S_Param_open, 50);
Y11_open=Y_Param_open(1,1,:);
Y12_open=Y_Param_open(1,2,:);
```

```
% Conversion in dB
S11dB_open=20*log10(abs(S11_open));
S21dB_open=20*log10(abs(S21_open));

% Calculation of parasitic pads matrix A_pad
for counter=1:num
    A_pad(:,:,counter)=[1,0;Y11_open(:,:,counter)+Y12_open(:,:,counter),1];
end

% Read THROUGH s2p file
directory='C:\';  %Directory to Read
s2p=[directory '1mmNi.s2p'];
file=dir(s2p);
filename=[s2p];
data =rfdata.data;
read(data,filename);

% Extract of THROUGH S-Parameters / Y-Parameters
freq_through= data.Freq;
S_Param_through =extract(data,'S_PARAMETERS');
S11_through=S_Param_through(1,1,:);
S21_through=S_Param_through(2,1,:);
%Y_Param_through = s2y(S_Param_through, 50);
%Y11_through=Y_Param_through(1,1,:);
%Y12_through=Y_Param_through(1,2,:);

% Conversion in dB
S11dB_through=20*log10(abs(S11_through));
S21dB_through=20*log10(abs(S21_through));

%Get ABCD parameters and charachteristic impedance from THROUGH
Z0=50;
ABCD_Params_through = s2abcd(S_Param_through, Z0);

for a=1:num
    Z0l(a)= sqrt(ABCD_Params_through(1,2,a)/ABCD_Params_through(2,1,a));
end

%Get Propagation Constant
for a=1:num
        Propagation(a)= (1/TL_length_through)*acosh(ABCD_Params_through(1,1,a));
end
```

```
% Calculation of interconnects matrix A_INT1 and A_INT2
for counter=1:num
    A_INT1(:,:,counter)=[cosh(Propagation(counter)*TL_length_L),Z01(counter)
    *sinh(Propagation(counter)*TL_length_L);(1/Z01(counter))*sinh(Propagation(counter)
    *TL_length_L),cosh(Propagation(counter)*TL_length_L)];
    A_INT2(:,:,counter)=[cosh(Propagation(counter)*TL_length_R),Z01(counter)*sinh(Propagation(counter)
    *TL_length_R);(1/Z01(counter))*sinh(Propagation(counter)
    *TL_length_R),cosh(Propagation(counter)*TL_length_R)];
end

% Calculation of input/output matrix A_IN and A_OUT
for a=1:num
    A_IN(:,:,a)=A_pad(:,:,a)*A_INT1(:,:,a);
    A_OUT(:,:,a)=A_pad(:,:,a)*A_INT2(:,:,a);
end

% Read DUT s2p file
directory='C:\';  %Directory to Read
s2p=[directory 'LSCs5DEV.s2p'];
file=dir(s2p);
filename=[s2p];
data =rfdata.data;
read(data,filename);

% Extract of DUT S-Parameters / ABCD-Parameters
freq_dut= data.Freq;
S_Param_dut =extract(data,'S_PARAMETERS');
S11_dut=S_Param_dut(1,1,:);
S21_dut=S_Param_dut(2,1,:);
A_dut = s2abcd(S_Param_dut, 50);

% Conversion in dB
S11dB_dut=20*log10(abs(S11_dut));
S21dB_dut=20*log10(abs(S21_dut));

Y_Param_dut = s2y(S_Param_dut, 50);
Y11_dut=Y_Param_dut(1,1,:);
Y12_dut=Y_Param_dut(1,2,:);
Y21_dut=Y_Param_dut(2,1,:);

Z_Param_dut = s2z(S_Param_dut, 50);
Z11_dut=Z_Param_dut(1,1,:);
```

```
Z12_dut=Z_Param_dut(1,2,:);
Z21_dut=Z_Param_dut(2,1,:);

% Inverse matric calculation
for a=1:num
    A_IN_inverse(:,:,a)=inv(A_IN(:,:,a));
    A_OUT_inverse(:,:,a)=inv(A_OUT(:,:,a));
end

% Pure ABCD extraction
for a=1:num
    %A_pure(:,:,a)= A_IN_inverse(:,:,a)*A_dut(:,:,a)*A_OUT_inverse(:,:,a);
    A_temp(:,:,a)=A_dut(:,:,a)*A_OUT_inverse(:,:,a);
    A_pure(:,:,a)= A_IN_inverse(:,:,a)*A_temp(:,:,a);

end

S_pure = abcd2s(A_pure, 50);
S11_pure=S_pure(1,1,:);
S21_pure=S_pure(2,1,:);

S11dB_pure=20*log10(abs(S11_pure));
S21dB_pure=20*log10(abs(S21_pure));
Y_Param_pure = s2y(S_pure, 50);
Y11_pure=Y_Param_pure(1,1,:);
Y12_pure=Y_Param_pure(1,2,:);
Y21_pure=Y_Param_pure(2,1,:);
Y22_pure=Y_Param_pure(2,2,:);

Z_Param_pure = s2z(S_pure, 50);
Z11_pure=Z_Param_pure(1,1,:);
Z12_pure=Z_Param_pure(1,2,:);
Z21_pure=Z_Param_pure(2,1,:);
Z22_pure=Z_Param_pure(2,2,:);

Z0=50;
ABCD_Params_pure = s2abcd(S_pure, Z0);

% Ferroelectric Varactor Dimensions
d=300*1e-9;
e0=8.8541878176 * 1e-12;
A=(5*1e-6*5*1e-6);
```

```
% Electrode estimation and approximations (Constant / Not precise)
th_te=1.7*1e-6;
th_be=100*1e-9;
l=20*1e-6;
w=20*1e-6;
r_ni=7.366*1e-7;
r_pt=14.117*1e-7;
R_te=(r_ni*l)/(th_te*w)
R_be=(r_pt*l)/(th_te*w)
R_total=R_te+R_be
R=R_total;
L=0;

% Electrode measurements (Frequency dependent / More accurate)
% Insert frequency dependent R and L from results of Appendix A-2

%Symbolic toolbox equation solve (for C_p, R_p and hence \epsilon, tan\delta)
for a=1:num
     wmega(a) = 2*pi*freq_dut(a);

     syms C_p R_p
        [C_p,R_p] = solve((real(-Y21_pure(:,:,a))-(R*((1/R_p)^2)+(1/R_p)+wmega(a)^2*C_p^2*R)
        /((R*(1/R_p)+1-wmega(a)^2*L*C_p)^2+wmega(a)^2
       *(R*C_p+(1/R_p)*L)^2)),(imag(-Y21_pure(:,:,a))-(wmega(a)*C_p-wmega(a)*(1/R_p)^2*L-wmega(a)^3*C_p^2*L)
       /((R*(1/R_p)+1-wmega(a)^2*L*C_p)^2+wmega(a)^2*(R*C_p+(1/R_p)*L)^2)));
        Call(a)=double(C_p(1));
        Rall(a)=double(R_p(1));
        C_pure(a)=((imag(-Y21_pure(:,:,a))/(2*pi*freq_dut(a))));
        C_dut(a)=((abs(imag(Y11_dut(:,:,a))))./(2*pi*freq_dut(a))));
        G_pure(a)=real(-Y21_pure(:,:,a));
        G_dut(a)=(1/(1/(abs(real(Y11_dut(:,:,a))))));
        E_pure(a)=((C_pure(a)*d)/(e0*A));
        E_dut(a)=((C_dut(a)*d)/(e0*A));
        E_all(a)=((Call(a)*d)/(e0*A));
        tand_pure(a)=(G_pure(a)/(C_pure(a)*(2*pi*freq_dut(a))));
        tand_dut(a)=(G_dut(a)/(C_dut(a)*(2*pi*freq_dut(a))));
        tand_all(a)=((1/Rall(a))/(Call(a)*(2*pi*freq_dut(a))));
        sprintf('Currently solved %d of %d equations.',a,num)
    sprintf('C_PST is %d\nR_PST is %d\nDielectric loss of PST is %d\n',Call(a),Rall(a),tand_all(a))
 end

figure(4)
plot(freq_dut/1e9,E_pure(:),'r',freq_dut/1e9,E_dut(:),'b',freq_dut/1e9,E_all(:),'y')
```

```
TITLE('Calculated Dielectric Constant')
axis([1e9/1e9 Up_to*1e9/1e9 0 2000])

figure(6)
plot(freq_dut,tand_pure(:),'r',freq_dut,tand_dut(:),'b')
TITLE('Calculated Dielectric Loss')
axis([1e9 Up_to*1e9 0 1])
```

# A-4 MATLAB Code : One-dimensional MASON acoustic modeling

```
% Change layers to the ones needed - CurrentlyPt/PZT/Pt/SiO2/Si stack

%Graph up to
from=1;   %X low
up_to=12 %X high
Y_low=-20;
Y_high=0;

% Densities
dens_Pt=2.15*1e4;
dens_Au=1.93*1e4;
dens_PZT=5.5*1e3;
dens_PST=5.13*1e3;
dens_SiN=3*1e3;  % LPCVD
dens_SiN=3.46*1e3;
dens_Si=2340;
dens_SiO=2460;
dens_Ni=8.9*1e3;   % bulk 8.9
dens_Ti=4.5*1e3;

% Capacitor dimensions
d1=1.7*1e-6;    % Top electrode
d11=100*1e-9;
d12=8*1e-9;
d13=50*1e-9;
d14=8*1e-9;
d2=250*1e-9;    % Ferroelectric PZT
```

```
d3=100*1e-9;    % Bottom electrode
d4=1*1e-6;      % Membrane layer (Buffer layer)
d5=525*1e-6;    % Silicon beneath membrane
wd=5*1e-6;        % Side length of capacitor (Square electrodes assumed)

% Acoustic velocities
V_Pt=4.26*1e3;%zhaorong4
V_Au=3.21*1e3;
V_SiN=4.3*1e5;
V_SiO=5900;    % V_SiO=5000-5970
V_PZT=8.05*1e3;
V0_PST=8.05*1e3;
V_Si=8433;  % Si acoustic velocity now revised
V_Ni=5600; %5600
V_Ti=6130;

% Electromechanical coupling coefficients for piezoelectrics/weakly
% ferroelectric PST
K2_PST_eff=0.002;
V_PST=V0_PST*sqrt(1+K2_PST_eff);

% Dielectric Constants
e0=8.854*1e-12;
e_PZT=400;
e_PST=1000;          % Under 6V bias dielectric constant

%Acoustic Attenuation (Np/m) frequency dependent so estimate (8.7dB/m=1Np/m)
%Consnant
% Qa_PZT=17500;        % at 1.5GHz
% Qa_PST=1700;        % at 1.5GHz - To evaluate!!!!
% Qa_Pt=3000;          % at 1.5GHz
% Qa_SiN=130;          % at 1.5GHz
% Qa_Au=2302;          % at 1GHz
% Qa_Si=1200;           % at 1GHz Approximation!!!
% Qa_SiO=400;          % at 1 GHz
% Qa_Ni=3000;      %Guess!!!!

nn=0;
%Nth law dependency
% Qa_PZT=17500;        % at 1.5GHz
% Qa_PST=(2*pi*1.5*1e9)/(2*40*V_PST)        % at 1.5GHz - To evaluate!!!!
% Qa_Pt=(2*pi*1.5*1e9)/(2*6000*V_Pt)          % at 1.5GHz
% Qa_SiN=130;          % at 1.5GHz
```

```
% Qa_Au=(2*pi*1e9)/(2*12234*V_Au);         % at 1GHz
% Qa_Si=(2*pi*1e9)/(2*3300*V_Si)           % at 1GHz Approximation!!!
% Qa_SiO=(2*pi*1e9)/(2*38034*V_SiO)         % at 1 GHz
% Qa_Ni=(2*pi*1e9)/(2*3000*V_Ni)     %Guess!!!!
% Qa_Ti=(2*pi*1e9)/(2*1000*V_Ti)

% Work out Qa '1 Hz' attenuation
% Ha_Si=(Qa_Si/((1*1e9)^nn));
% Ha_SiN=(Qa_SiN/((1*1e9)^nn));
% Ha_SiO=(Qa_SiO/((1*1e9)^nn));
% Ha_Pt=(Qa_Pt/((1.5*1e9)^nn));
% Ha_Ni=(Qa_Ni/((1*1e9)^nn);
% Ha_PZT=(Qa_PZT/((1*1e9)^nn));
% Ha_PST=(Qa_PST/((1.5*1e9)^nn));
% Ha_Au=(Qa_Au/((1*1e9)^nn));
% Ha_Ti=(Qa_Ti/((1*1e9)^nn));
Ha_Si=(100*((1*1e9)^nn));
Ha_SiN=(20000*((1*1e9)^nn));
Ha_SiO=(500*((1*1e9)^nn));
Ha_Pt=(150*((1*1e9)^nn));
Ha_Ni=(150*((1*1e9)^nn));
Ha_PZT=(9500*((1*1e9)^nn));
Ha_PST=(120*((1*1e9)^nn));
Ha_Au=(120*((1*1e9)^nn));
Ha_Ti=(500*((1*1e9)^nn));

% Capacitances
Cp=((e0*e_PST*(wd^2))/d2);

% Acoustic Impedances
Z_SiN=dens_SiN*V_SiN;
Z_SiO=dens_SiO*V_SiO;
Z_Si=dens_Si*V_Si;
Z_Pt=dens_Pt*V_Pt;
Z_Ni=dens_Ni*V_Ni;
Z_Ti=dens_Ti*V_Ti;
Z_PZT=dens_PZT*V_PZT;
Z_PST=dens_PST*V_PST;
Z_Au=dens_Au*V_Au;

% Define range of frequencies in GHz to scan over
start_freq=from;
stop_freq=up_to;
```

```
points=16001;
sstep=(stop_freq-start_freq)/points;
n=[0:(points-1)];
freq=start_freq+n*sstep;

% Calculate frequency dependent attenuation
w=2*pi*freq;
Fqa_SiN=Ha_SiN./((freq*1e9).^nn);
Fqa_SiO=Ha_SiO./((freq*1e9).^nn);
Fqa_Si=Ha_Si./((freq*1e9).^nn);
Fqa_Pt=Ha_Pt./((freq*1e9).^nn);
Fqa_Ni=Ha_Ni./((freq*1e9).^nn);
Fqa_Ti=Ha_Ti./((freq*1e9).^nn);
Fqa_Au=Ha_Au./((freq*1e9).^nn);
Fqa_PZT=Ha_PZT./((freq*1e9).^nn);
Fqa_PST=Ha_PST./((freq*1e9).^nn);
Fa_SiO=(w*1e9)./(2*V_SiO*Fqa_SiO);
Fa_Si=(w*1e9)./(2*V_Si*Fqa_Si);
Fa_Pt=(w*1e9)./(2*V_Pt*Fqa_Pt);
Fa_Ni=(w*1e9)./(2*V_Ni*Fqa_Ni);
Fa_Ti=(w*1e9)./(2*V_Ti*Fqa_Ti);
Fa_Au=(w*1e9)./(2*V_Au*Fqa_Au);
% h_PZT=(Fqa_PZT*2*V_PZT)./(2*pi*freq*1e9);
% Z_PZT=dens_PZT*V_PZT*((1+j*h_PZT).^0.5);
h_PST=(1./(2*Fqa_PST));
% Z_PST=dens_PST*V_PST*((1+j*h_PST).^0.5);
% Z_PST=dens_PST*V_PST*((1+j*h_PST).^(0.5));
Z_PST=dens_PST*V_PST;
%  Z1=Z_Ni.*tanh((Fa_Ni+j*k1)*d1);    % Top electrode

% Calculate wavenumber k in the different layers at each frequency
k1=w*(1e9/V_Ni);                                    %  Top electrode
k11=w*(1e9/V_Au);
k12=w*(1e9/V_Ti);
k13=w*(1e9/V_Au);
k14=w*(1e9/V_Ti);
% k2=(w*1e9)./((V_PST*((1+j*h_PST).^(0.5)))); %  Piezoelectric/Ferroelectric
k2=((w*1e9)./(V_PST)).*(1-0.5*j*h_PST);
k3=w*(1e9/V_Pt);                                    %  Bottom electrode
k4=w*(1e9/V_SiO);                                   %  Membrane Layer
k5=w*(1e9/V_Si);                                    %  Silicon Layer

Z11=Z_Ni.*tanh((Fa_Ni+j*k1)*d1);
```

```
Z12=Z_Au.*((Z11.*cosh((Fa_Au+j*k11)*d11)+Z_Au.*sinh((Fa_Au+j*k11)*d11)).
/(Z_Au.*cosh((Fa_Au+j*k11)*d11)+Z11.*sinh((Fa_Au+j*k11)*d11)));
Z13=Z_Ti.*((Z12.*cosh((Fa_Ti+j*k12)*d12)+Z_Ti.*sinh((Fa_Ti+j*k12)*d12)).
/(Z_Ti.*cosh((Fa_Ti+j*k12)*d12)+Z12.*sinh((Fa_Ti+j*k12)*d12)));
Z14=Z_Au.*((Z13.*cosh((Fa_Au+j*k13)*d13)+Z_Au.*sinh((Fa_Au+j*k13)*d13)).
/(Z_Au.*cosh((Fa_Au+j*k13)*d13)+Z13.*sinh((Fa_Au+j*k13)*d13)));
Z1=Z_Ti.*((Z14.*cosh((Fa_Ti+j*k14)*d14)+Z_Ti.*sinh((Fa_Ti+j*k14)*d14)).
/(Z_Ti.*cosh((Fa_Ti+j*k14)*d14)+Z14.*sinh((Fa_Ti+j*k14)*d14)));

Z5=Z_Si.*tanh((Fa_Si+j*k5)*d5);    % Silicon
Z4=Z_SiO.*((Z5.*cosh((Fa_SiO+j*k4)*d4)+Z_SiO.*sinh((Fa_SiO+j*k4)*d4)).
/(Z_SiO.*cosh((Fa_SiO+j*k4)*d4)+Z5.*sinh((Fa_SiO+j*k4)*d4)));
Z3=Z_Pt.*((Z4.*cosh((Fa_Pt+j*k3)*d3)+Z_Pt.*sinh((Fa_Pt+j*k3)*d3)).
/(Z_Pt.*cosh((Fa_Pt+j*k3)*d3)+Z4.*sinh((Fa_Pt+j*k3)*d3)));
Z31=Z_Ti.*((Z3.*cosh((Fa_Ti+j*k14)*d14)+Z_Ti.*sinh((Fa_Ti+j*k14)*d14)).
/(Z_Ti.*cosh((Fa_Ti+j*k14)*d14)+Z3.*sinh((Fa_Ti+j*k14)*d14)));
Z3=Z31;

Y_all=(Z_PST.*(Z1+Z3).*(cos((k2.*d2)/2).^2)+(Z_PST).^2.*sin(k2.*d2)*j).
/(Z_PST.*(Z1+Z3).*cos(k2.*d2)+(((Z_PST).^2)+(Z1.*Z3)).*sin(k2.*d2)*j);
%Y_all=((Z1+Z3).*cos((k2.*d2)/2).^2+sin(k2.*d2)*j).
/((Z1+Z3).*cos(k2.*d2)+((Z1.*Z3)+1).*sin(k2.*d2)*j);

k2_factor=(K2_PST_eff)/(1+K2_PST_eff);
Zsys=(-j*(1-((((k2_factor).*(tan((k2.*d2)/2))./((k2.*d2)/2)))).*Y_all))./(w*1e9*Cp);
%Zsys=1-(((((k_PZT).^2).*(tan((k2.*d2)/2))./((k2.*d2)/2)))).*Y_all;

% Resistances

R1=0.8;                % Electrode Resistance
%R2=1.5*1e6;          % R2?
tand=0.015;
R2=1./(w.*1e9*tand*Cp);
%R2=1.5*1e6;
Z_total=R1+((Zsys.*R2)./(R2+Zsys));
%ZCC=R2-j./(w*1e9*Cp);
Loss_model=abs(real(Z_total)./imag(Z_total));
%Loss_model=abs(real(Zsys)./imag(Zsys));
%Loss_model=abs(imag(ZCC)./real(ZCC));
% S-parameters

S11dB_model=20*log10(abs(Z_total./(100+Z_total)));
S21dB_model=20*log10(abs((100./(Z_total+100))));
```

```
%Load measured
num=1601;
%Read Files
directory='C:\';      %Directory to read from

s2p=[directory '0V.S2P'];      % File to read

filename=[s2p];
data =rfdata.data;
read(data,filename);

%Extract of Parameters
freq2= data.Freq;
freq2=freq2/1e9;
S_Param =extract(data,'S_PARAMETERS');
S11m=S_Param(1,1,:);
S21m=S_Param(2,1,:);
S12m=S_Param(1,2,:);
S22m=S_Param(2,2,:);

%Conversion in dB
S11dB_measured=20*log10(abs(S11m));
S21dB_measured=20*log10(abs(S21m));

 figure(1)
 plot(freq,S11dB_model,'b--',freq,S21dB_model,'r--',freq2,S11dB_measured(:),'b',freq2,S21dB_measured(:),'r')
 %plot(freq,S21dB_model,'b',freq2,S21dB_measured(:),'r')
 legend('S_1_1 modelled with Mason model', 'S_2_1 modelled with Mason model', 'S_1_1 measured varactor',
 'S_2_1 measured varactor')
 axis([from up_to Y_low Y_high])
 TITLE('Mason modelled Vs. Measured ')
 XLABEL('Frequency (GHz)')
 YLABEL('S-Parameters (dB)')

 figure(2)
 plot(freq,real(Z_total)/50,'b')
 axis([from Up_to 0 0.2])
```

# B-1 $Pb_{0.25}Sr_{0.75}TiO_3$ 0.4M Sol preparation process

- (Chem Lab) Get and clean 2 bottles, 2 bottle holders and 2 magnetic stirrers. Put one (first) under a fume hood and the other one (second) with open lid in the Glove Box interlock. Close the compartment from the outside and press 'auto purge'.
- Get Lead Acetate - $Pb(OAc)_2{:}3H_2O$ - from the poison cupboard. Weigh lead acetate and sign the weight book.
- Put a small (25ml) resist holder on the Waysafe scale and zero it. Put in the first bottle 1.177g (7.31mmol) strontium acetate ($Sr(OAc){:}1/2H_2O$). Zero the scale again. Put in the first bottle 0.79g (2.1mmol) of lead acetate) - this includes 10% excess Pb. Re-weigh the lead acetate. Sign the book. Put the lead acetate/strontium acetate back in cupboards. Pour the resist holder mix in the first bottle under the fume hood.
- After Vacuum Box is ready, retrieve second bottle and lid from interlock. Put second bottle on scale, switch on and zero. Use pipette and pour 2.489g (7.31mmol) of Titanium Butoxide ($Ti(O_nBu)_4$) which is moisture sensitive, in the second bottle. Close Titanium Butoxide bottle, close lid. Switch off scale. Put second bottle and pipette in interlock and close interlock. Push START and put back metal things. Retrieve bottle.
- Put 8ml of Acetic Acid glacial with a new pipette in the strontium acetate/lead acetate mix (first) bottle. Put on stirrer at room temperature for 2 h.
- Put 15ml of Acetic Acid glacial in titanium butoxide (second) bottle. Retrieve Acylacetanone from Chem lab small fridge (must be kept in the dark). With a new pipette add 1ml of Pentanedione (acylacetone) in titanium Butoxide bottle (becomes yellow). Put Acylacetanone back to the fridge - bottom of shelf. Put the second bottle on another stirrer for 2h at room temperature. Throw away pipettes.
- After 2 hours of stirring the 2 bottles, pour the lead acetate-strontium acetate mix in the titanium butoxide bottle. Stir the mix for another 2 h at room temperature. Clean the other bottle. Finally pour the sol in a new/clean bottle and label.

# B-2 $Pb_{0.4}Sr_{0.6}TiO_3$ 0.4M Sol preparation process

- (Chem Lab) Get and clean 2 bottles, 2 bottle holders and 2 magnetic stirrers. Put one (first) under a fume hood and the other one (second) with open lid in the Glove Box interlock. Close the compartment from the outside and press 'auto purge'.
- Get Lead Acetate - $Pb(OAc)_2{:}3H_2O$ - from the poison cupboard. Weigh lead acetate and sign the weight book.
- Put a small (25ml) resist holder on the Waysafe scale and zero it. Put in the first bottle 1.177g (7.31mmol)1.177g (5.48mmol) strontium acetate ($Sr(OAc){:}1/2H_2O$). Zero the scale again. Put in the first bottle 1.591g (4.19mmol) of lead acetate) - this includes 10% excess Pb. Re-weigh the lead acetate. Sign the book. Put the lead acetate/strontium acetate back in cupboards. Pour the resist holder mix in the first bottle under the fume hood.
- After Vacuum Box is ready, retrieve second bottle and lid from interlock. Put second bottle on scale, switch on and zero. Use pipette and pour 3.245g (9.53mmol) of Titanium Butoxide ($Ti(O_nBu)_4$) which is moisture sensitive, in the second bottle. Close Titanium Butoxide bottle, close lid. Switch off scale. Put second bottle and pipette in interlock and close interlock. Push START and put back metal things. Retrieve bottle.
- Put 8ml of Acetic Acid glacial with a new pipette in the strontium acetate/lead acetate mix (first) bottle. Put

on stirrer at room temperature for 2 h.
- Put 15ml of Acetic Acid glacial in titanium butoxide (second) bottle. Retrieve Acylacetanone from Chem lab small fridge (must be kept in the dark). With a new pipette add 1ml of Pentanedione (acylacetone) in titanium Butoxide bottle (becomes yellow). Put Acylacetanone back to the fridge - bottom of shelf. Put the second bottle on another stirrer for 2h at room temperature. Throw away pipettes.
- After 2 hours of stirring the 2 bottles, pour the lead acetate-strontium acetate mix in the titanium butoxide bottle. Stir the mix for another 2 h at room temperature. Clean the other bottle. Finally pour the sol in a new/clean bottle and label.

# C-1 High frequency Ferroelectric varactor fabrication process (Pt bottom electrodes)

**1. High Resistive Si Wafer with 200nm $SiO_2$**

**2. Bottom Electrode (lift-off)**

a. 5×(Spin LOR2A 30sec@3000rpm / Bake 5min@115C) for ∼1um LOR2A

b. Bottom electrode mask S1818 lithography, develop 2m15s with MF-319

c. Measure undercut(∼2-2.3um) / B.A. 10m@12W

d. Deposit blanket Ti(10nm) 30sec@300W RF sputtering, Pt(100nm) 45sec@0.7A DC sputtering, 5mTorr Ar flow $\sim 5\times 10^{-7}$

e. Acetone liftoff 2h / MF319 1m / BA 10m@12W

**3. PST layer**

a. Deposit 6 layers of PST

i. Deposit / spin PST layer 30sec@3000rpm (use 0.2mm filter)

ii. Bake 5 min @∼350$^o$C (Cimarek hotplate)

iii. Bake 10 min @700$^o$C (Sawatec hotplate)

**4. PST etching**

a. PST etch mask AZ5214E lithography, BA 15m@12W

b. ∼20-22min. in HF PZT I(0.5%HF)

c. Resistance checking

d. Anneal ∼300-350$^o$C then ∼700$^o$C

**5. Top Electrode**

a. Seed layer : Deposit blanket Ti(10nm) 30sec@300W RF sputtering, Pt(100nm) 45sec@0.7A DC sputtering, 5mTorr Ar flow, $\sim 5\times 10^{-7}$

b. Top electrode mask AZ9260 lithography, B.A. 10m@12W

c. Nickel plating : for 1h(∼1mA/cm2) change side after 30m (∼)1um Ni deposited

d. AZ9260 stripping, (Acetone/IPA - spin/clean), BA 15m@12W

e. RIE etching Au/Ti seed layer

# C-2 Conductive bottom electrode : Au/$TiO_2$ process

**1. High Resistive Si Wafer with 200nm SiO2**

**2. Bottom Electrode**

a. Deposit blanket Ti(40nm) 2min @ 300W in Nordiko and oxidize in RTA 4min @700$^o$C

b. Re-deposit blanket Ti(40nm) 2min @ 300W and oxidize in RTA 4min @700$^o$C c. Bake 5min@150$^o$C / Thin layer S1818(1:25 acetone) / Bake 5min@150C d. 5 X (Spin LOR2A p.4 / Bake 5min@115$^o$C) for ∼1um LOR2A e. Bottom electrode mask S1818 lithography, develop 2m15s at MF-319 f. Measure undercut(∼2-2.3um) / BA 10m@12W g. DONE IN STEPS SO AS NOT TO HEAT RESIST!!!! Deposit blanket Ti(8nm) 25s @300W and Au(500nm) - 15min @ 100W in Nordiko 10s@300W steps(Ti) / 1m@100W(Au) h. Acetone liftoff 2h / MF319 1m / BA 10m@12W