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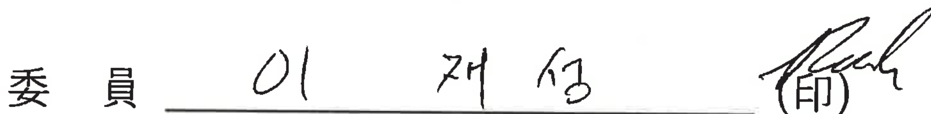

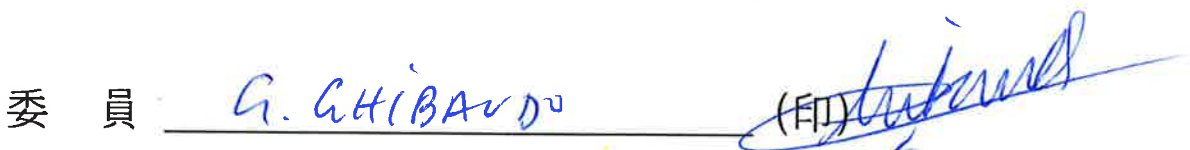

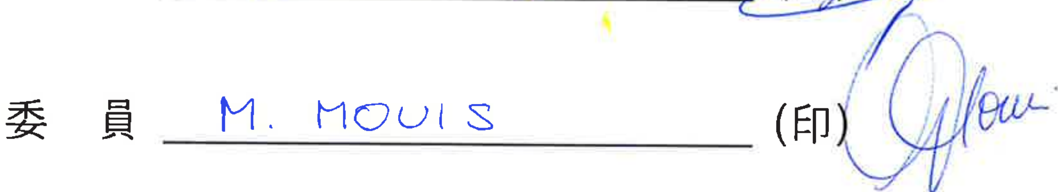

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Electrical characterization of junctionless transistors with numerical simulation

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Abstract

In this dissertation, the performance of junctionless transistors (JLTs) as possible candidates for the continuation of Moore's law was investigated experimentally based on an in-depth study of their electrical characteristics. Current-voltage I-V and capacitance-voltage C-V were analyzed in a wide range of temperatures (from 80 K to 350 K) in correlation with device operation mechanism. Low-frequency noise was also studied and compared to that of inversion-mode transistors. This study required new parameter extraction methods to be defined for JLTs. Their validity was confirmed by 2-dimensional (2D) simulation results. They will be detailed in this dissertation.

In order to characterize devices performance, or to feed transistors models with relevant parameters about effective dimensions, doping level or electron transport properties after full device processing, it is mandatory to be able to extract a number of parameters from device electrical characterization. Junctionless Transistors (JLT) fabricated on (100) silicon on insulator (SOI) wafer with 145 nm thick BOX and ≈ 9 nm silicon thickness were considered here. These field-effect devices, which are exploiting conduction in a semiconducting thin layer which features the same type from source to drain, are operating differently from inversion mode transistors. Indeed, when gate voltage V_g varies, they are progressively switching from full depletion (OFF state) to bulk conduction (for $|V_g| > |V_{th}|$, V_{th} being the threshold voltage) and surface accumulation (for $|V_g| > |V_{fb}|$, V_{fb} being the flat-band voltage), while inversion mode transistors are switching directly from depletion to inversion. Due to this essential difference in operation, it was necessary to reassess the parameter extraction methodologies. It was found that some extraction methods could still be used with some adaptations, while others needed to be revised more deeply. Revised methods were developed to extract such parameters as threshold voltage, flat-band voltage, drain induced barrier lowering (DIBL), low field mobility and channel doping level. The so extracted parameters were shown to reveal the specific features of JLT operation compared to that of conventional inversion-mode transistors.

In addition, the electrical behavior of tri-gate JLTs depending on top-effective width (W_{top_eff}) was investigated, experimentally. With decreasing W_{top_eff}, the amount of bulk neutral channel is relatively getting smaller than that of surface accumulation channel, whereas the channel sidewall gate effect was reinforced. These cause the shrinkage of the shoulder shape on the gate-to-channel capacitance characteristics (C_{gc}-V_g), resulting in a noticeable change in the effective mobility (μ_{eff}) behavior from that in wide JLT devices, an increase of the threshold voltage (V_{th}), while the flat-band voltage (V_{fb}) doesn't change. 2D numerical simulation results, well consistent to the experimental results, confirmed the significant sidewall gate effect in the tri-gate JLT devices with a narrow structure.

The electrical performance of JLTs with planar structures was investigated under low-temperature and compared to that of the traditional inversion-mode (IM) transistors. The low-field mobility (μ_0) of JLT devices was found to be limited by phonon and neutral defects scattering mechanisms for long gate lengths, whereas scattering by charged and neutral defects mostly dominated for short gate lengths, likely due to the defects induced by the source/drain (S/D) implantation which had been added in the process for series resistance considerations. Moreover, the temperature dependence of flat-band voltage (V_{fb}), threshold voltage (V_{th}) and subthreshold swing (S) of JLT devices was also discussed.

Low-frequency (LF) noise characteristics of wide planar JLTs were investigated. Interestingly, we found that carrier number fluctuation is the main contributor to LF noise of the JLT devices under study, even though their bulk conduction features were clearly proved by the extracted flat-band voltage (V_{fb}). This is explained by the fact that free electrons in depletion, originating from the bulk neutral channel or source/drain regions, can interact with slow traps in the gate oxide, giving rise in return to fluctuations of the charge density in the bulk neutral channel. Similar values of trap density (N_t) were extracted in JLT devices and IM transistors, which also supports our conclusion that the LF noise of JLTs is well explained by the carrier number fluctuation model.

A new method for the extraction of flat-band voltage (V_{fb}) and channel doping concentration (N_d) in Tri-gate JLTs is presented. The new method, based on the relationship between the top-effective width (W_{top_eff}) in accumulation and the effective width (W'_{eff}) in partial depletion, enables the extraction of V_{fb} and N_d of JLT devices (here as ≈ 0.61 V and ≈ 6.4×10^{18} cm^{-3}, respectively). The validity of the new method is also proved by 2D numerical simulations. Furthermore, it is emphasized that the sidewall accumulation current (I_{d_side}) behavior of Tri-gate JLT devices is found to decrease dramatically near V_{fb}, allowing an estimation of the V_{fb} position of JLT devices.

Furthermore, another new and simple method for the extraction of electrical parameters in JLTs was presented. The bulk channel mobility (μ_{bulk}) and flat-band voltage (V_{fb}) were successfully extracted from the new method, based on a linear dependence between the inverse of transconductance squared ($1/g_m^2$) vs gate voltage in the partially depleted operation regime ($V_{th} < V_g < V_{fb}$). The validity of the new method is also proved by 2D numerical simulation and a newly defined Maserjian's-like function for g_m of JLT devices.

Keywords: Junctionless transistors (JLTs), Parameter extraction method, Sidewall gate effects, Numerical simulation, Scattering mechanisms, Low-frequency noise, New method for electrical parameter extraction in JLTs

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Introduction

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1. Current trend of CMOS technology and future roadmap

1.1 CMOS scaling and challenges owing to short-channel effects

The invention of first transistor at Bell laboratory (Shockley's group) in 1947 was followed by the integrated-circuit (IC) era. The minimum critical feature size (physical gate length) of metal-oxide semiconductor field-effect transistors (MOSFET) has been successfully reduced by more than two orders of magnitude according to Moore's law until now and International Technology Roadmap of Semiconductors 2012 (ITRS) recently foresaw that the minimum feature size will still decrease from 22 nm in 2011 to around 6 nm in 2026 [1].

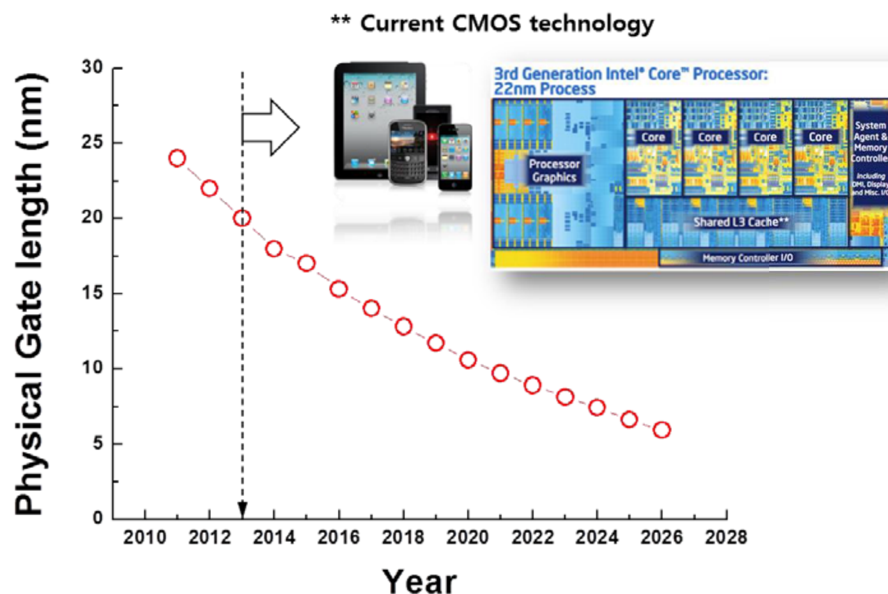

Figure 1. Scaling trend of high performance logic technologies with Year [1].

However, when the MOSFET dimensions are decreasing, it is hard to keep long-channel behavior due to unwanted side effects [2]. As the channel length is reduced, the depletion widths of source and

drain junctions are becoming comparable in size to the channel length. This readily causes the punch-through effect [3], where the electric-field (E-field) between drain and source allows electrons from the source region (in the case of N-type MOSFET) to flow directly to the drain regardless of any gate voltage value. To prevent this, a higher channel doping level is required to reduce the depletion width at the junctions between channel and source/drain (S/D). However, the increased channel doping also raises the threshold voltage (V_{th}). Therefore, in order to keep a reasonable V_{th}, it is necessary to use a thinner oxide.

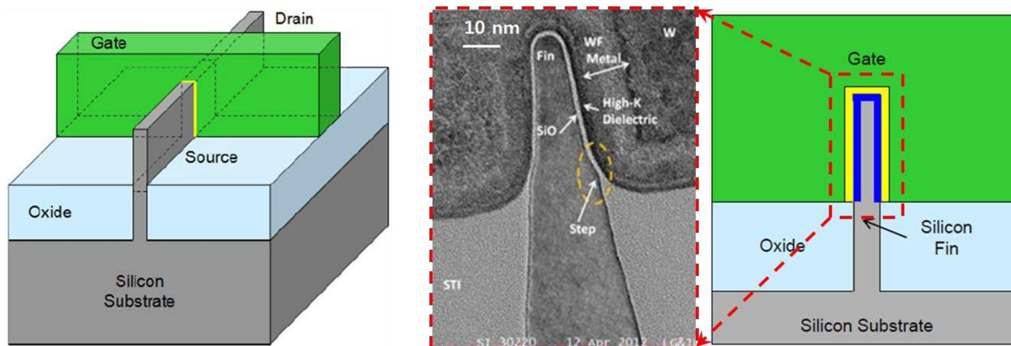

Figure 2. Intel's 22 nm bulk fully-depleted Tri-gate Transistor, 2011.

Likewise, the device parameters are strongly interrelated. It is the reason why a scaling rule should be needed to optimize the device performance. The constant-field scaling, which means that the internal E-field is kept the same during scaling down, is shown in Table 1 [4]. However, unfortunately, the constant-field scaling might not give an optimal condition regarding the scaling down, due to other factors that are fundamentally not scalable. For instance, in the case of the scaling down of gate oxide thickness, tunneling and the quantum-mechanical effect are fundamental limitations which put a stop the ideal scaling rule. For this reason, other scaling rules have been followed to account for these limitations, including constant-voltage scaling, quasi-constant-voltage scaling and generalized scaling.

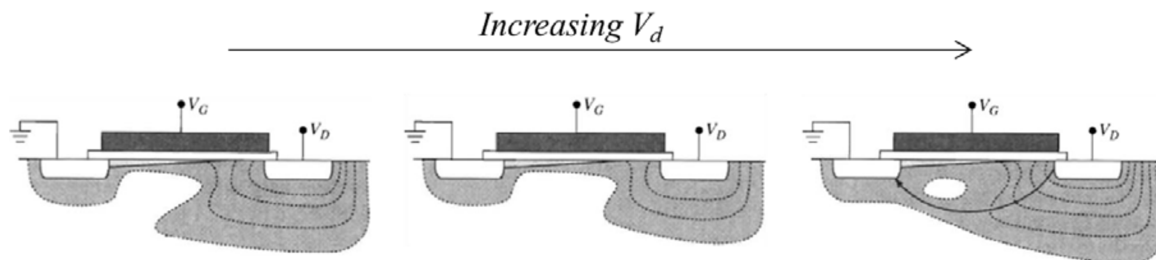

Figure 3. Punch through effect in a short-channel MOS transistor [3].

Even with the best scaling rules, it is not always possible to optimize the scaled-down devices without deviation from long-channel behavior [2]. Deviations in scaling down arise as a result of

short-channel effects (SCE), which are mainly due to the two-dimensional nature of potential distribution in short channel devices. Then, the gradual-channel approximation, which assumes that E_x induced by gate voltage >> E_y induced by drain bias, is no longer valid. The short channel effects can be summarized as follows [1, 2]:
(1) Drain current (I_D) does not saturate with V_D bias due to channel-length modulation effect, (2) drain-induced barrier lowering (DIBL) which lead to the reduced gate controllability in regard to the channel, (3) rolling-off of V_{th} as reducing channel length owing to charge sharing from S/D, (4) hot carrier generation (electron-hole pair creation) in the pinch-off region owing to increased longitudinal E-field in the short lengths.

Table 1. Scaling rules for MOS transistors [4].

Device and circuit parameters	Constant E-field scaling:	Generalized scaling:
Device dimensions (L,W,T_{ox})	$1/\kappa$	$1/\kappa$
Body doping level (N_a)	κ	$\alpha\kappa$
Electric field (E)	1	α
Supply voltage (V_{dd})	$1/\kappa$	α/κ
Intrinsic delay ($\tau \sim CV_{dd}/I$)	$1/\kappa$	$1/\kappa$
Power dissipation ($P \sim IV_{dd}$)	$1/\kappa^2$	α^2/κ^2

1.2 Various approaches for the continuation of Moore's law

Many improvements, in terms of including channel doping profile, gate stack, S/D design, mechanical strain engineering, 3-dimensional (3D) architectures with multi-gates, and alternate channel material, have been proposed to overcome such short-channel effects and enhance device performance [1, 2, 5]:
(1) In the 90's, retrograde channel doping profiles in the channel allowed punch-through and other SCE to be better controlled. It also reduced the junction capacitance and V_{th} sensitivity to substrate-bias.

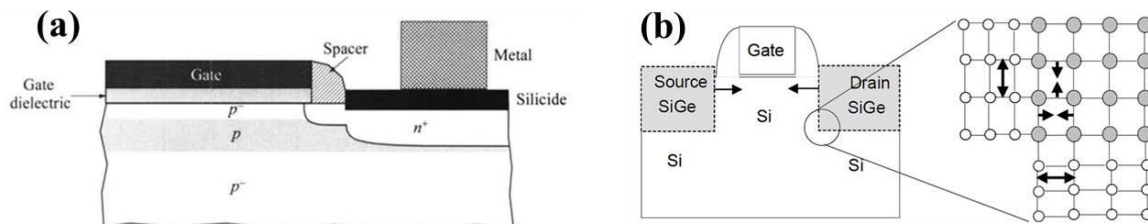

Figure 4. (a) Retrograde channel doping profile gives a high-performance in a MOS transistor. (b) The lattice mismatch between SiGe and Si can improve the mobility of MOS transistors [2].

(2) High-k gate dielectrics, such as Al_2O_3, HfO_2, ZrO_2, Y_2O_3, La_2O_3, Ta_2O_5 and TiO_2, have been introduced to overcome the fundamental problem of gate leakage current, since they can keep a thicker physical thickness for the same capacitance compared to silicon dioxide (SiO_2) insulators.

(3) Poly-silicon (Si) has been used as gate materials for a long time, thanks to its advantages, such as good compatibility with silicon processing, ability to bear high-temperature process and easy control of its work function by N-type or P-type doping. It has thus been used until gate resistance on one side, and the thin depleted region at the interface between poly-Si and gate oxide on the other side, could not be neglected. It is progressively replaced by silicides and metals such as TiN, TaN, W, Mo and NiSi.

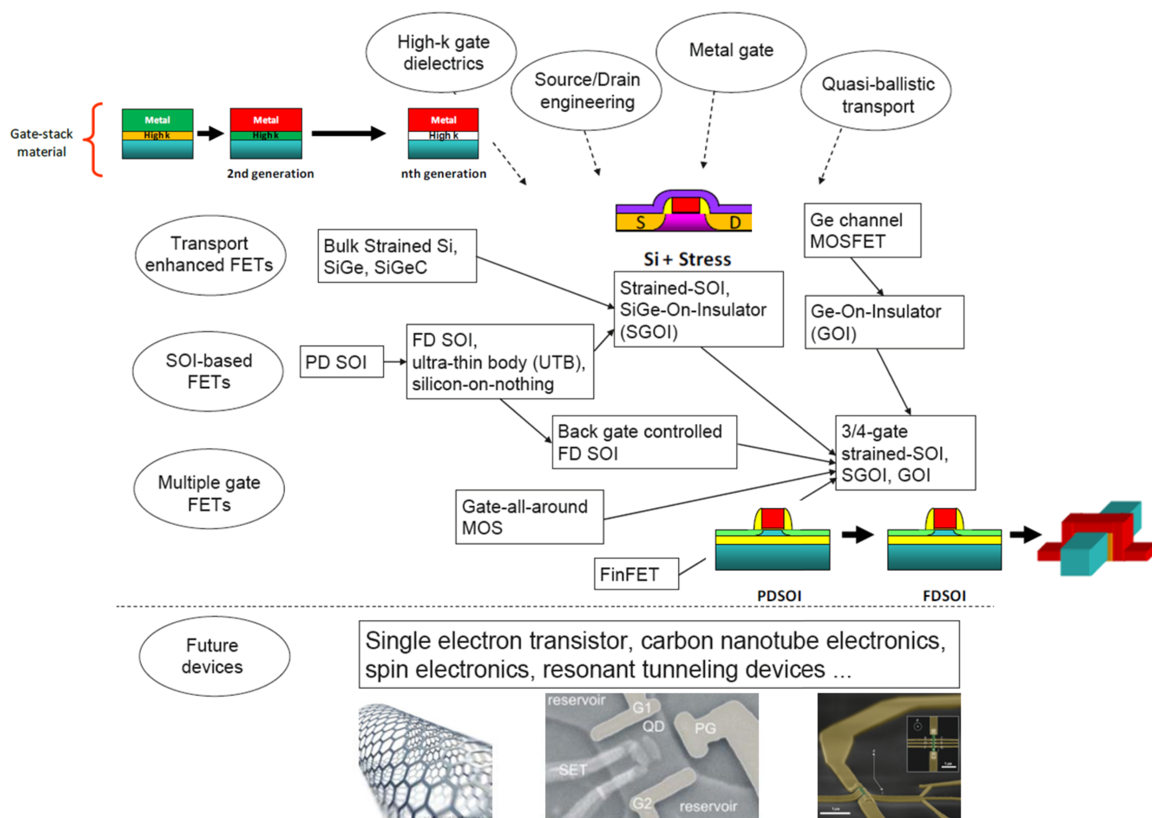

Figure 5. CMOS technology overview for the continuation of Moore's law [5].

(4) A lightly doped drain (LDD) can effectively minimize hot-carrier generation by reducing the lateral E-field and the development of the silicide contact technology gives very small contact resistance at self-aligned S/D to the gate. Moreover, Schottky-barrier contacts for S/D instead of p-n junction can also minimize the SCE owing to its very small junction depth close to almost zero.

(5) Silicon on insulator (SOI) based devices have less difficulty in controlling SCE compared to planar bulk complementary MOS (CMOS) devices. A thin channel body the SOI substrate can successfully remove most problems regarding current leakage through the substrate and punch-through effect. It also allows the channel to be lightly doped, giving rise to higher speed. However, there are disad-

vantages of SOI such as expensive wafer cost, the kink effect due to floating body effect and worse heat conduction.

(6) 3D devices with multi-gate structures (double-, triple- or quadruple- gate devices) have evolved for the suppression of SCE, optimum gate control with minimized leakage and increase of current drive. A 3D device so called Fin-FET has been also developed not on SOI substrate but on bulk Si substrate. This can lead to lower wafer cost and better compatibility with conventional bulk planar CMOS devices.

(7) Strain engineering can give the improvement of device mobility, since the Si crystal lattice constant altered by external applied stress causes the changing of the band structure, the density of states and the effective mass of the carriers. For instance, embedded SiGe S/D produces a compressive stress in the channel due to its larger lattice constant than Si. This improves holes mobility in PMOS devices. SiC S/D structures can also lead to the electron mobility. (8) Finally, for further boost of device performance, III-V (for N-type) and Ge (for P-type) combination can be considered as forward-looking solutions of future channel materials to be able to replace Si.

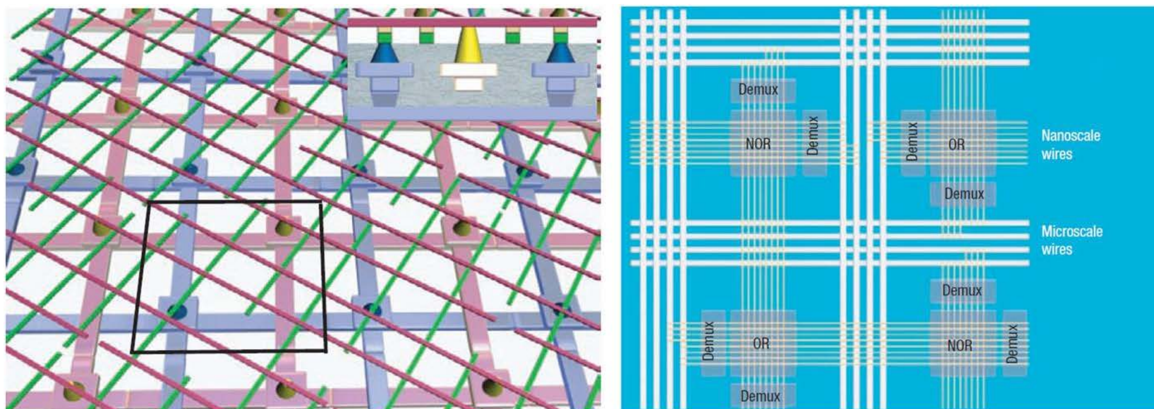

Figure 6. Schematic of Hybrid crossbar/CMOS circuits made of bottom-up based nanowires materials [9].

In addition, the bottom-up approaches, analogous to the way that biology so successfully works, has other possibilities for beyond Si era, since it might be a solution for diverse technical and fundamental challenges today's top-down industry faced [9]. Materials for the bottom-up processing include semiconductor nanowires (NWs), carbon nanotube (CNTs) and graphene nanoribons [6-8]. Hybrid bottom-up/top-down technology with crossbar/CMOS structures also have a potential for next-generation circuits, since it could take advantage of the ultra-high device density of cross-bar architectures together with compatibility with CMOS circuitry [9]. For practical applications with these, collaboration between chemists, physicists and electrical and computer engineers should be needed.

2. Overview of junctionless transistors

Junctionless transistors (JLTs, also called gated resistors [10] or junctionless accumulation transistors) are currently in the spotlight, owing to their promising advantages which are expected from their simple structures, without PN-junction at S/D regions [10-12]. Challenges as scaling down, related to the formation of ultra-shallow junction with high doping concentration gradient, in conventional transistors might be overcome by JLTs, which have no junctions and no doping gradients. For fabrication of JLTs, very thin Si layer (typically around 10 nm or less than maximum depletion width for a doping concentration) should be needed to allow for full depletion of carriers in heavily doped channel so that the device can be tuned off with a small gate voltage. The heavily doped channel (normally more than 5×10^{18} cm^{-3}) close to typical S/D doping level in JLTs allow for not only quite simple device structures without junctions, but also enough current flow even around flat-band voltage (V_{fb}) when the device is turned on.

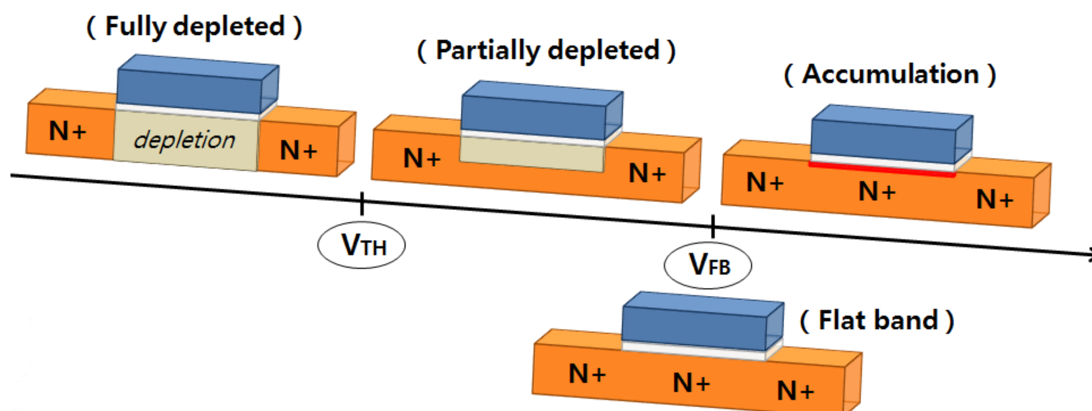

Figure 7. Schematic showing all operation modes in Junctionless transistors.

For off-state in JLTs, the heavily doped channel is fully depleted by the work function difference between the gate metal and Si channel with additional applied gate bias, while the S/D junction in IM-FET blocks any current flow when no inversion channel between S/D regions is created. As gate voltage (V_g) is increased, operation mode is evolving from full depletion (no conduction) to partial depletion (bulk conduction in the neutral channel with gate controlled channel thickness). When V_g reaches V_{fb}, the depletion region vanishes completely and the neutral channel takes up the whole Si layer, where the electric field perpendicular to current flow is basically very close to zero (bulk conduction). This can give more robust performance than IM transistors in terms of relaxed requirement for gate insulator thickness, effective gate length variability and mobility degradation by transverse electric field. Moreover, the bulk conduction of JLTs is in principle credited for reduced low-frequency (LF) noise [14].

Figure 8 schematically compares the behavior of drain current with gate voltage in the three dif-

ferent types of transistors (inversion-mode N+PN+, accumulation-mode N+NN+ and JLTs N+N+N+) for better understanding of JLTs operation. For inversion-mode device, the flat-band voltage V_{fb}, which leaves the p-type body neutral, is located below V_{th}. Above V_{th}, a surface depletion layer is formed, with an inversion channel at the interface between silicon and gate oxide. In contrast, for both accumulation-mode devices and JLTs, V_{fb} is above V_{th} and both devices are fully depleted below V_{th}. However, in the case of JLTs, the distance between V_{th} and V_{fb} in JLTs is much longer than that in accumulation device, owing to high channel doping concentration in JLTs.

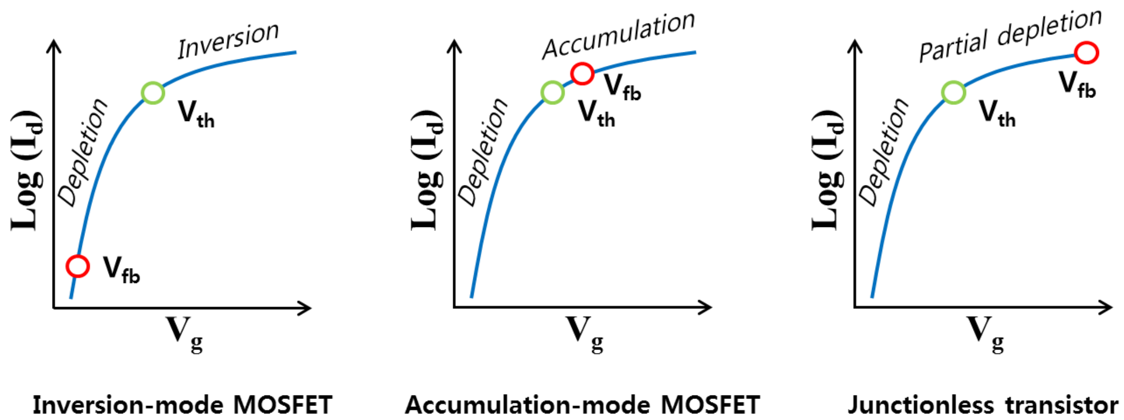

Figure 8. Drain current vs V_g characteristics in an inversion-mode MOSFET, an accumulation-mode MOSFET and a heavily-doped junctionless transistor [10].

This allows JLTs to drive enough current even around V_{fb}, while gate voltage would need to be increased much to above V_{fb} to obtain proper amount of drive current in an accumulation device (in order to create a surface accumulation channel).

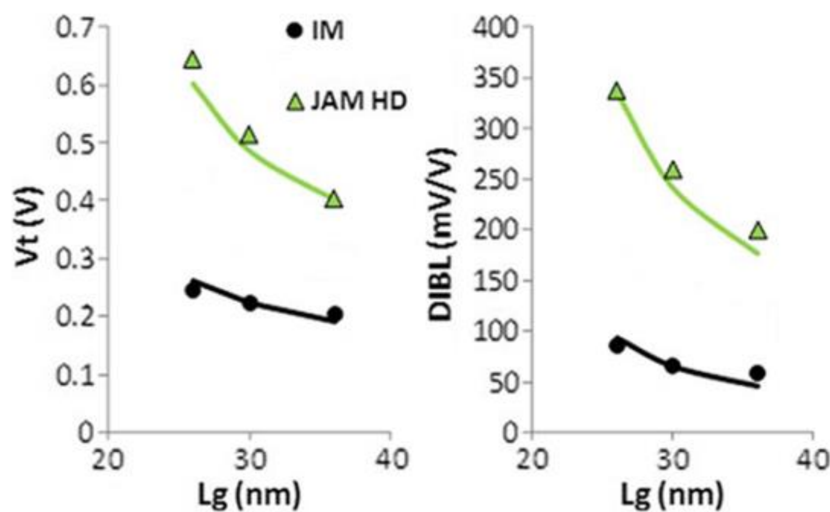

Figure 9. Length dependence of V_{th} and DIBL in both inversion-mode MOSFET and Junctionless transistor. JLTs show relatively large SCE [14].

Of course, it is also possible to further increase V_g to create surface accumulation channels even in JLTs. In such regime, JLTs combine a bulk neutral channel, not any more affected by V_g and a surface accumulation channel controlled by V_g.
However, JLTs are facing some issues such as mobility degradation by their high channel doping, reduced gate controllability due to partial depletion regions under gate insulator and V_{th} variability induced by fluctuation of Si thickness and doping atoms spatial distribution [13, 14]. Nevertheless, the extremely simple structure of JLTs could lead them to be a feasible candidate for the realization of sub-22 nm CMOS technology.

3. Dissertation scope and outline

The work described in this dissertation has been mainly carried out at IMEP-LAHC laboratory, with the support of European Union 7th Framework program project SQWIRE under Grant Agreement No. 257111.
The main purpose of this thesis was to investigate the performance of JLTs devices, as a possible candidate for the continuation of Moore's law, through diverse electrical characterization. Furthermore, new method for the extraction of electrical parameters in JLTs was also proposed in this thesis and its validity was confirmed from 2-dimensional (2D) numerical simulation works.

In chapter 1, many parameter extraction methods for conventional IM transistors were explained and semiconductor device measurement technique with diverse instruments was discussed. These provide theoretical and experimental backgrounds for electrical characterization with JLTs.

Chapter 2 includes the revisited parameter extraction methodology for electrical characterization of JLTs. Issues in JLTs was studied from the extracted parameters and compared to IM transistors fabricated by the same process only except for channel doping concentration. Moreover, the variation of JLTs electrical properties as changing widths in terms of V_{th}, V_{fb} and effective mobility (μ_{eff}) data analysis is covered. The strong side wall gate effect in very narrow JLTs was also proven by 2D numerical simulation results.

In chapter 3, the electrical performances of JLTs are discussed based on the analysis of temperature dependence (80 K ~ 350 K) of low-field mobility (μ_0), V_{th}, V_{fb} and subthreshold swing (SS).

In chapter 4, the low-frequency (LF) noise behavior of JLTs was investigated and compared to IM transistors fabricated with the same process only except for channel doping.

Chapter 5 introduces a new method for the extraction of V_{fb}, doping concentration in the channel (N_d) and bulk mobility (μ_{bulk}). The validity of the new method is also proven by 2D numerical simulation results.

Finally, chapter 6 concludes all results and discussions in this work.

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Chapter 1

Theoretical and experimental backgrounds

1.1 Low temperature characterization in MOS devices

1.2 Low-frequency noise theory and measurements in MOS devices

1.3 MOSFET parameter extraction method

1.4. Measurement technique with instruments and numerical simulation

1.1 Low temperature characterization in MOS devices

Device operation under cryogenic temperature leads to improved performance owing to an increase of carrier mobility, lower thermal electrical noise and reduced parasitic effects [1]. Low temperature characterization also allows for a better understanding of physical operation and electrical performance of electronic devices. This section deals with the low temperature properties for MOSFET devices.

1.1.1 Scattering mechanism and temperature dependence

The MOSFET channel mobility can be derived from the Matthiessen's rule, which assumes that the main scattering mechanisms present in the channel are independent from each other to write total reciprocal mobility as the sum of reciprocal mobilities resulting from each scattering mechanism [2]. In general, total mobility can be expressed as:

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \qquad (1)$$

where μ_c, μ_{ph} and μ_{sr} mean Coulomb, phonon and surface roughness scattering mobility, respectively. Phonon (or lattice) scattering probability decreases at low temperature, since the lattice vibration gets frozen. In contrast, the effect of Coulomb (or ionized impurity) scattering is reinforced as temperature decreases. This is because a slowly moving carrier, due to less thermal motion at lower temperature, is more likely to be scattered by the ionized impurities. Moreover, surface roughness scattering and neutral defect scattering are less dependent to temperature.

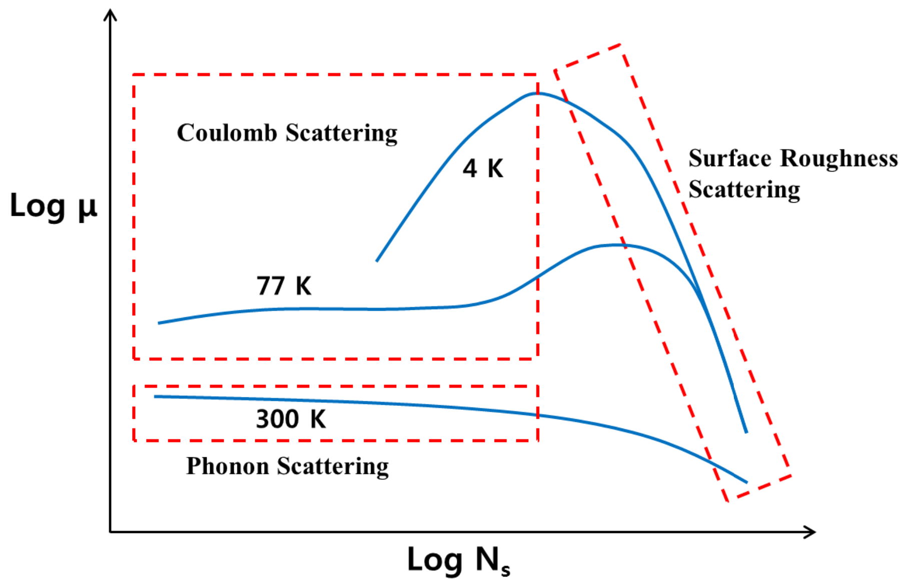


Figure 1. The channel mobility dependence on inversion layer carrier density (N_s) [2].

Figure 1 shows the channel mobility dependence on inversion layer carrier density N_s as a function of temperature. At strong inversion region, surface roughness scattering predominates the channel mobility behaviors regardless of temperature. On the other hand, at weak inversion, the channel mobility is mainly affected by Coulomb scattering at low temperature, while phonon scattering governs it at high temperature.

1.1.2 Empirical model based on Matthiessen's rule

When we deal with low-field mobility, the surface roughness scattering can be neglected. Therefore, the low-field mobility μ_0 as a function of temperature can be fitted with simple empirical model as [3]:

$$\frac{1}{\mu_0} = \frac{1}{\frac{300}{T}\cdot\mu_{ph}} + \frac{1}{\frac{T}{300}\cdot\mu_c} + \frac{1}{\mu_{neu}} \qquad (2)$$

The overall tendency of dominant mobility contribution at a device, among Coulomb scattering (μ_c), phonon scattering (μ_{ph}) and neutral defect scattering (μ_{neu}) contribution, can be estimated from the empirical model.

1.1.3 Temperature dependent series resistance and threshold voltage

Under low temperature, the series resistance in lightly doped drain (LDD) region has been shown to significantly increase due to their relatively low doping level (non-degenerated) compared to S/D region. However, high-field assisted impurity ionization, induced from high enough drain and gate biases, could allow a strong reduction of the increased series resistance at low temperature [4].
The trend of V_{th} roll-off due to the charge sharing effect in short gate lengths could be varied as decreasing temperature. However, a strong roll-off of V_{th}, regardless of changing temperature, has shown at very short lengths owing to the additional side effects [4].

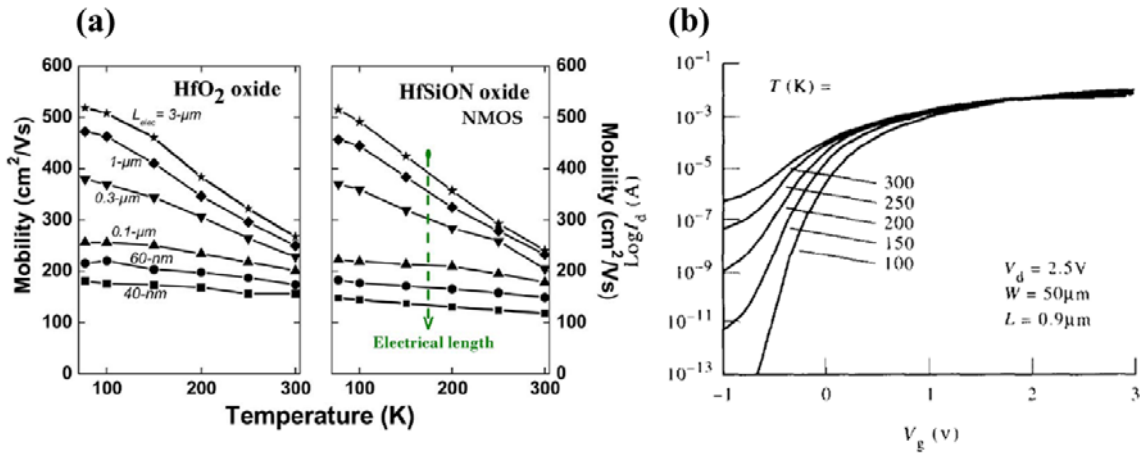


Figure 2. (a) Temperature dependence of the MOSFET channel mobility by varying the lengths [3] (b) The suppression of punch through effect as decreasing temperature [4].

1.1.4 Reduced Punch through effect at low temperatures

The punch through effect is mainly induced from the thermo-ionic emission over the junction barrier between source and drain. Therefore, the punch through current can be reduced by decreasing temperature. The reduced punch through effect strongly affects the subthreshold swing and threshold voltage [4].

1.2 Low-frequency noise theory and measurements in MOS devices

The unwanted noise perturbs to distinguish the desired signal in an electronic system. The noise source can be categorized as external source and internal source. The external source is arisen from adjacent circuits, AC power lines, various disturbing owing to electrostatic and electromagnetic coupling, whereas the internal source originate from internal random fluctuations (physical process) of the electron transport in a device. This chapter will mainly focus on the internal source.

1.2.1 Noise in electronic systems

The internal random noise source cannot be completely eliminated, while the external one can be significantly reduced by appropriate shielding, filtering and proper design of the circuits. However, understanding of the internal noise needs inevitably to minimize its effects and estimate the accuracy of detected signals [5].

The current I(t), with a randomly fluctuating current component $i_n(t)$, through a device can be expressed as $I(t) = I_{avg} + i_n(t)$, where I_{avg} is the average bias current. Fourier transformation is powerful method to convert the noise signal from the time domain to the frequency domain for better and easier characterization.

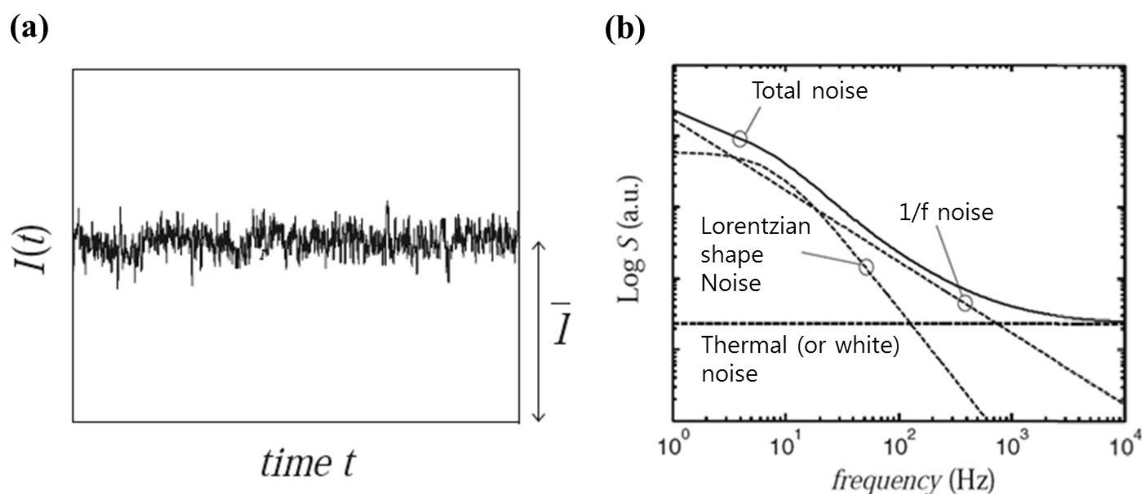


Figure 3. (a) Illustration of a typical noise waveform in time domain. (b) The PSD for low-frequency noise and thermal noise vs frequency [5].

Figure 3(b) shows the different types of noise sources from the frequency variation of the power spectral density (PSD) and more details with that will be discussed in next paragraph.

1.2.2 Fundamental noise sources

Thermal noise (Nyquist or Johnson noise), stemming from the random thermal motion of electrons in

a material, exists in all resistor and resistive component in a device. The PSD of the thermal noise current (or noise voltage) in a material with resistance R can be given as:

$$S_I = \frac{4kT}{R}(or, S_v = 4kTR) \qquad (3)$$

where k and T denote the Boltzmann constant and the absolute temperature in Kelvin, respectively. The thermal noise also sets a minimum signal detection limit in an electric circuit. The thermal noise can be also called a white noise, since it is independent of frequency up to 10^{11}–10^{12} Hz.

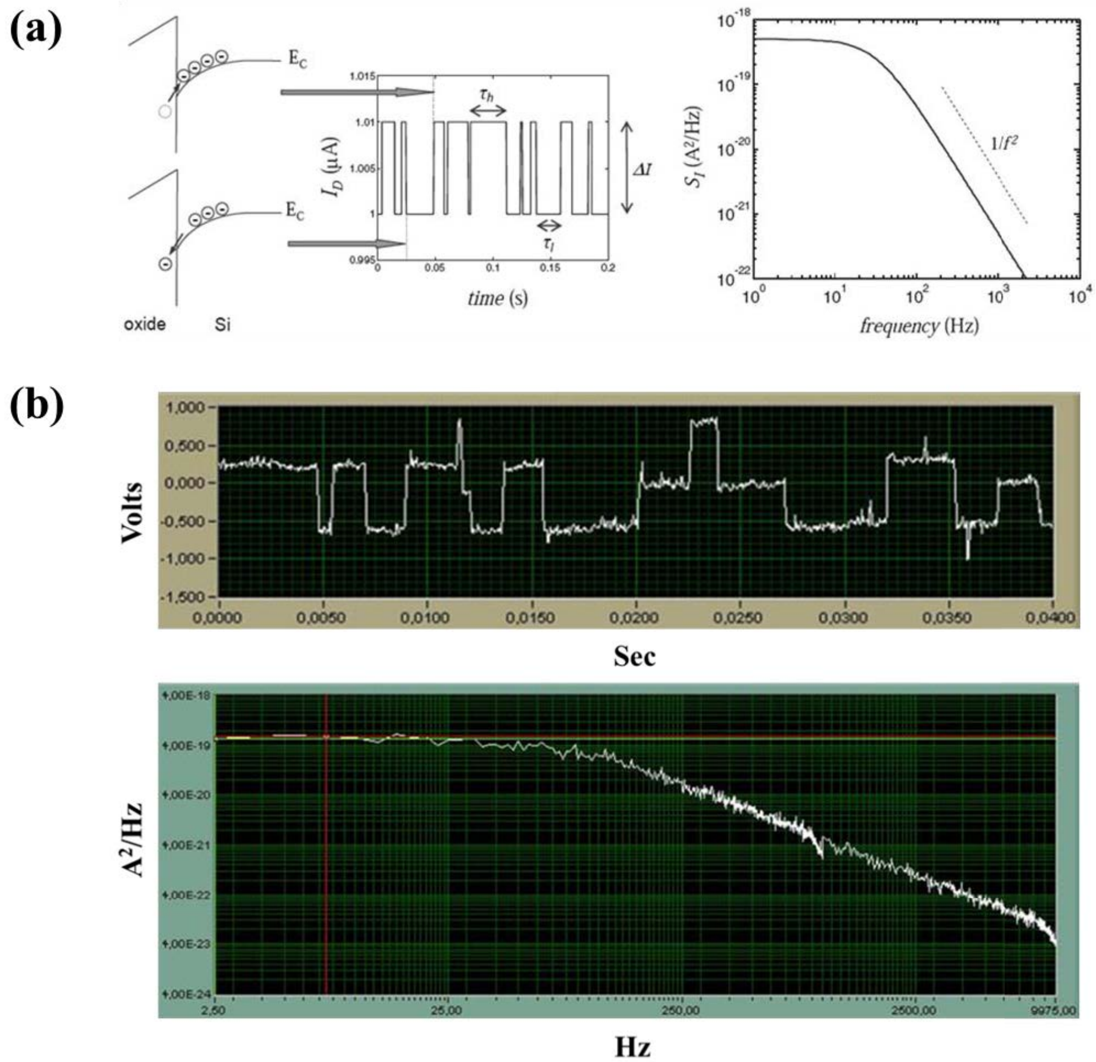


Figure 4. (a) Schematic showing the drain current fluctuations owing to RTS noise in a MOSFET and a Lorentzian shaped PSD (or RTS noise behavior with frequency) [5]. (b) Measured RTS noise behavior in a FD-SOI MOSFET with very small area (L=40nm and W=80nm).

Random-Telegraph-Signal (RTS) noise is resulted from random trapping and detrapping motion of carriers with only a few traps. There are three main RTS parameters such as the average drain current

RTS amplitude ΔI_d and the average values of the high and low level time constants (the capture time τ_h and the emission time τ_l). The transition times from low to high level (also high to low) are Poisson distributed random variables. The drain current PSD of a RTS exhibits a Lorentzian spectrum as fol-lowings [5, 6]:

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)\left[\left(\frac{1}{\tau_l} + \frac{1}{\tau_h}\right)^2 + (2\pi f)^2\right]} \quad (4)$$

Provided the background noise is low, the RTS noise in MOS devices can be easily investigated with a small gate area involving only few traps, normally below L×W=1 μm^2. Moreover, the RTS charac-terization is a powerful tool for the analysis of traps in MOS devices, since it can provide the key in-formation related to the carrier trapping dynamics at the Si/SiO_2 interface.

1/f noise (or flicker noise) denotes a PSD proportional to $1/f^{\gamma}$, where γ is usually in the range from 0.7 to 1.3. The superposition of many Lorentzian spectrum with a large number of traps can produce the 1/f noise behavior. The 1/f noise study is a valuable tool for the evaluation of insulator quality and performance reliability in electronic devices, especially in recent scaled down devices. The measure-ment principle, physical mechanism and diverse issues concerning the 1/f noise in CMOS devices will be dealt in detail with the next chapters.

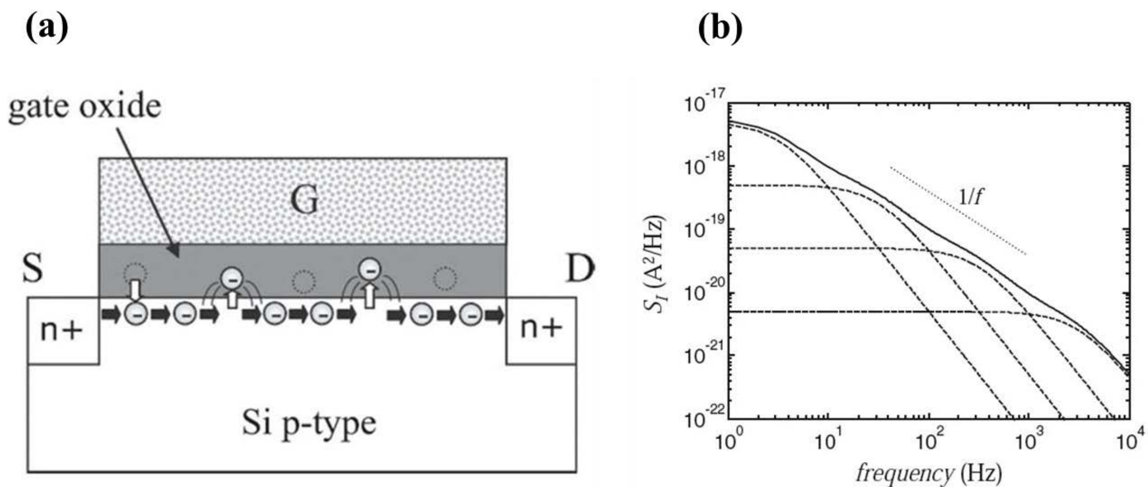


Figure 5. (a) Illustration showing the origin of drain current fluctuations due to moving electrons in and out of interface traps (carrier number fluctuation). (b) Superposition of several Lorenzians gives a 1/f dependence [5].

1.2.3 Low-frequency noise measurement set-up

Two key instruments for the low-frequency (LF) noise measurements are pre-amplifier (current to voltage) and spectrum analyzer (or oscilloscope for the detection of RTS noise in the time domain). The current fluctuation signal through a sample (or so called DUT device-under-test) can be converted into a voltage signal via the pre-amplifier and then the spectrum analyzer can read the voltage signal from the output port of the pre-amplifier. Finally, the spectrum analyzer displays the PSD from a current in the sample according to frequency domain [5].

A low noise amplifier (LNA) is needed to send the amplified weak noise signal to the spectrum analyzer. The internal noise in LNA strongly affects the measurement limit of the system, since it is added to the noise signal we want to observe. Therefore, its own internal noise should be minimized for the better accuracy.

A spectrum analyzer uses the Fast Fourier transform (FFT) algorithm to convert the measured voltage signal from the time domain to the frequency domain. A narrower resolution bandwidth of the spectrum measurements gives better frequency resolution, but it also makes the measurement time slower. The voltage noise PSD in the analyzer is displayed with V^2/Hz unit (or A^2/Hz for current noise) and averages over typically 50-100 samples must be used for the reliable measurements.

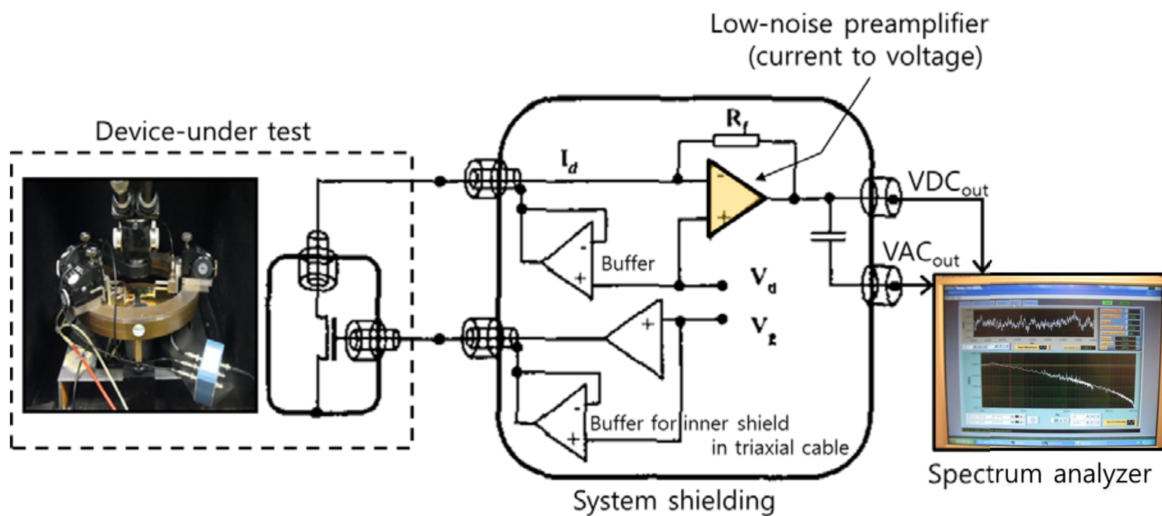


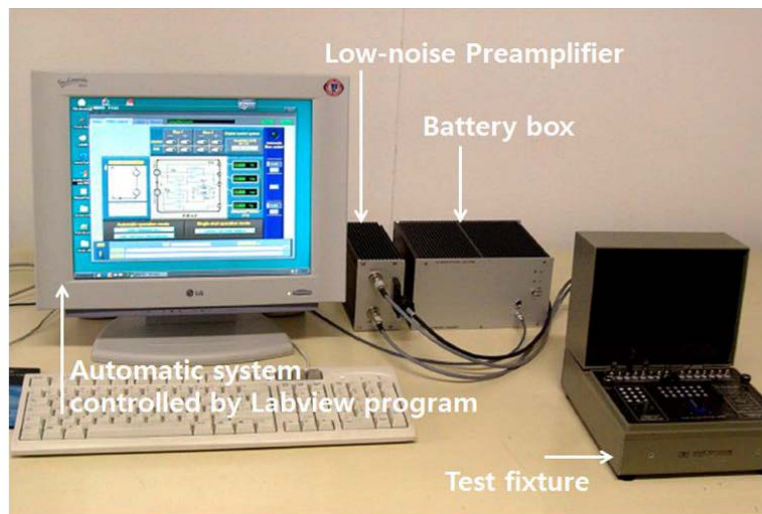
Figure 6. A schematic diagram of Low-frequency measurement set-up [7].

Shielding for the noise measurement system should be done to prevent undesirable disturbances from external electromagnetic signals. A good idea is to use batteries, for bias circuit to power DUT, to eliminate completely 50 Hz or 60 Hz disturbances.

For the performance test of the measurement system, the background noise induced from the thermal noise source should be checked by varying the sensitivity of the pre-amplifier. The background noise PSD is given as [7]:

$$S_I = 4kT\left(\frac{1}{R_f} + \frac{1}{R_g}\right) \quad (5)$$

where R_g is a load resistance under DUT and R_f is the resistance related to pre-amplifier sensitivity in the feedback-loop.



** System noise characteristics and Cut-off frequency

Range [V/A] $\log G_{AC}/\log G_{DC}$	V_s $[\mu V_{rms}/Hz^{1/2}]$	A_s $[pA_{rms}/Hz^{1/2}]$	f_{max} [kHz]
8/7	6.5	0.065	35
7/6	4.5	0.45	50
6/5	4.0	4	>100
5/4	2.5	25	>100
4/3	2.5	250	>100
3/2	2.5	2500	>100

Figure 7. Programmable Point-Probe Noise Measuring System (3PMS) and Background noise characteristics and the frequency where the output signal is reduced by 3dB in 3PMS system [7].

1.2.4 1/f noise characterization in MOSFETs

1.2.4.1 Carrier number fluctuations and correlated mobility fluctuations

The carrier number fluctuation model explains that 1/f noise behavior in MOS devices resulted from the dynamic trapping-detrapping of free carriers into slow oxide traps. The trapping-detrapping motion causes the fluctuation of the drain current nearby Si-SiO_2 interface [5, 6, 8]. The interface charge fluctuation density δQ_{ox} is given as (since $V_{fb}=\Phi_{ms}-Q_{ox}/C_{ox}$, where Φ_{ms} denotes the work-function dif-

ference between gate electrode and Si):

$$\delta V_{fb} = -\delta Q_{ox} / C_{ox} \qquad (6)$$

where C_{ox} means the oxide capacitance per unit area. Then, the fluctuation in the drain current I_d=f(V_{fb}, μ_{eff}), which takes into account the additional mobility changes $\delta\mu_{eff}$ by the interface charge fluctuations, is expressed as:

$$\delta I_d = \frac{\partial I_d}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_d}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \qquad (7)$$

Since $\partial I_d/\partial V_{fb} = -\partial I_d/\partial V_g = -g_m$ due to the gate charge conservation relation and Id $\propto$ μ_{eff},

$$\delta I_d = -g_m \delta V_{fb} + \frac{I_d}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta Q_{ox} \qquad (8)$$

where the Coulomb scattering coefficient α equals $\partial\mu_{eff}/(\mu^2_{eff}\times\partial Q_{ox})$. The α has ≈$10^4$ Vs/C for electrons and ≈10^5 Vs/C for holes. Moreover, the positive sign in front of α denotes donor-like traps and its negative sign represents acceptor-like traps.

Therefore, the normalized spectral density of the drain current can be derived as:

$$\frac{S_{Id}}{I_d^2} = \left(1 + \alpha \mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \qquad (9)$$

Also, the equivalent input gate voltage spectral density is given by

$$S_{Vg} = \left(1 + \alpha \mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 S_{Vfb} \qquad (10)$$

After replacing I_d and g_m by their analytical expressions, this can be again expressed as:

$$S_{Vg} = S_{Vfb} \left[1 + \alpha \mu_0 C_{ox} \left(V_g - V_{th}\right)\right]^2 \qquad (11)$$

where μ_0 means the low field mobility.

In addition, the flat band voltage spectral density can have the following form (which considers the trapping probability via a tunneling process decreased exponentially with oxide depth):

$$S_{Vfb} = \frac{q^2 kT \lambda N_t}{WLC_{ox}^2 f^{\gamma}} \qquad (12)$$

where f denotes the selected frequency, γ represents the characteristic exponent close to 1, λ is the tunnel attenuation distance (in the case of SiO_2, typically $\approx$ 0.1 nm), kT means the thermal energy and N_t is the oxide trap density per unit volume (eV/cm^3).

If there is a significant series resistant effect on a device, this contributes the excess noise to overall LF noise behavior. In this case, one gets the revised the PSD of drain current with considering the PSD (S_{Rsd}) of S/D series resistance as:

$$\frac{S_{Id}}{{I_d}^2} = \left(1 + \alpha \mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} + \left(\frac{I_d}{V_d}\right)^2 S_{Rsd} \qquad (13)$$

1.2.4.2 Hooge mobility fluctuations

The Hooge model explains that the origin of the drain current noise PSD stems from the carrier mobility fluctuation. Hooge's empirical formula in ohmic operation is given as [5, 6, 8]:

$$\frac{S_{Id}}{{I_D}^2} = \frac{q \alpha_H}{fWLQ_i} \qquad (14)$$

where Q_i is the inversion charge and α_H denotes the Hooge parameter (typically 10^{-3} to 10^{-6}). The flicker noise in metal or bulk semiconductors (volume conduction devices) has been successfully explained by the Hooge model. The S_{Id}/I_d^2 is approximately proportional to I_d^{-1} for Hooge mobility noise (in ohmic operation), while, in the case of trapping noise, it starts from a plateau at weak inversion before decreasing as I_d^{-2} at strong inversion region.

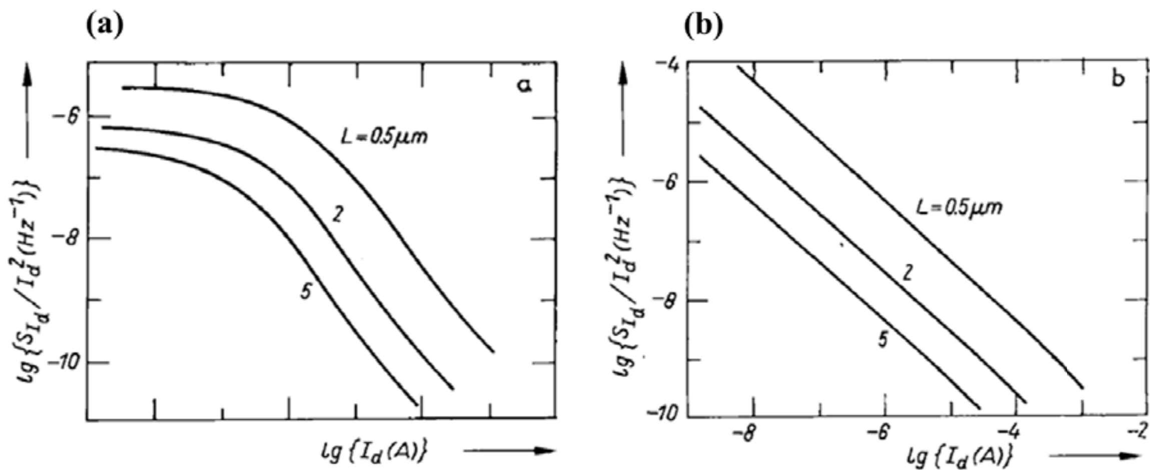


Figure 8. Theoretical variation of the normalized drain current PSD with drain current as given by (a) Carrier number fluctuation with correlated mobility fluctuations. (b) Hooge mobility model [8].

1.2.5 1/f noise related to CMOS scaling issues

As scaling a transistor down, the LF noise is becoming a major issue more and more as following reasons [5, 6, 8]. First, the 1/f noise increases as the reciprocal of the device dimension (L×W). Indeed, the normalized drain current PSD significantly increases as reducing lengths in Fig. 9. The reduced supply voltage according to a scaling rule causes a degradation of the signal to noise ratio. The normalized PSD is also raised at high drain current due to S/D series resistance (note equation 13).

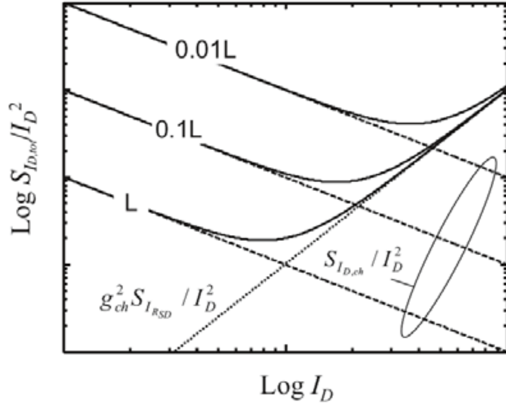


Figure 9. Simulation of the normalized drain current PSD with varying lengths in MOSFETs [5].

Moreover, the increased effects induced by defects and imperfections in the short length devices can strongly affect the 1/f noise. The choice of alternative gate oxide and channel material for the next generation devices should also be considered by the 1/f noise performances. Finally, the new device architecture and fabrication process should also importantly consider low frequency noise performance [5].

1.3 MOSFET parameter extraction method

1.3.1 Y function method and R_{sd} extraction using first order attenuation factor

For strong inversion ($V_g > V_{th}$) and linear operation region (small V_d), the drain current I_d in MOS transistor has been well expressed as [9]:

$$I_d = \frac{WC_{ox}}{L}\frac{\mu_0}{\left[1+\theta\left(V_g - V_{th}\right)\right]}\cdot\left(V_g - V_{th}\right)\cdot V_d \qquad (15)$$

where θ is the mobility reduction coefficient.

Then, the transconductance g_m is readily calculated by differentiation of above equation as:

$$g_m = \frac{W}{L}C_{ox}\frac{\mu_0}{\left[1+\theta(V_g - V_{th})\right]^2}\cdot V_d \qquad (16)$$

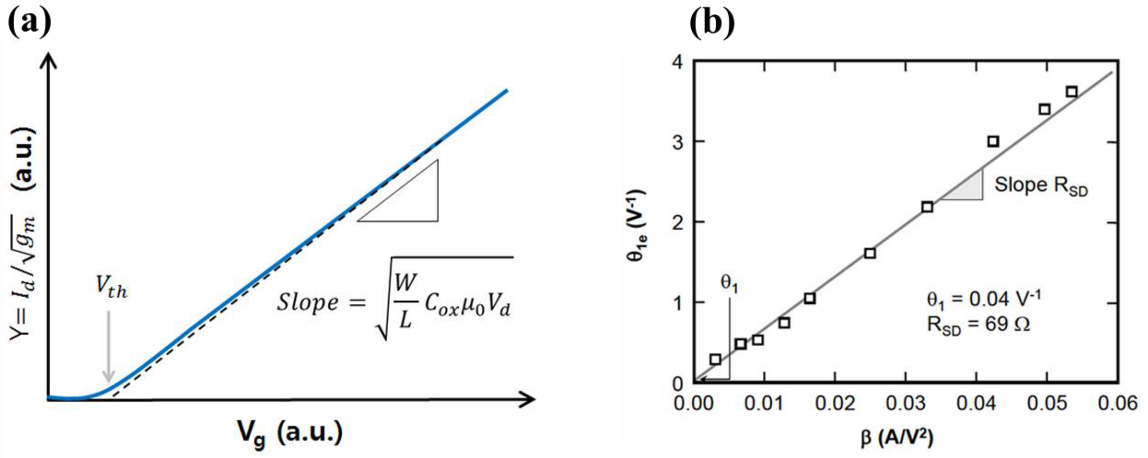


Figure 10. (a) Illustration of Y-function method [9]. (b) Extraction of the series resistance through first-order attenuation factor values [10].

Finally, one can obtain the following equation by a proper combination of above two equations.

$$\frac{I_d}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox}\mu_0 V_d\right)^{1/2} (V_g - V_{th}) \qquad (17)$$

It should be noted that the influence of the mobility attenuation with gate voltage was eliminated by this equation. The $I_d/g_m^{1/2}$ should be linear in gate voltage and the intercept and the slope in $I_d/g_m^{1/2}$ vs V_g give V_{th} and μ_0, respectively. This method allows a separate, but consistent, determination of V_{th} and μ_0 with avoiding the effects of mobility reduction and S/D series resistance.

The series resistance R_{sd} in a MOSFET can be extracted from the plot of the first order attenuation factor (θ_e), which includes degradation effect by R_{sd}, as a function of their conductance gain ($\beta = W/L \times C_{ox} \times \mu_0$) [10]:

$$\theta_e = \frac{\beta \cdot V_d}{I_d} - \frac{1}{V_g - V_{ty}} = \theta + \beta \cdot R_{sd} \qquad (18)$$

where V_d and V_g refer to the applied drain and gate voltage including the presence of R_{sd} and θ represents the first order mobility attenuation factor, respectively.

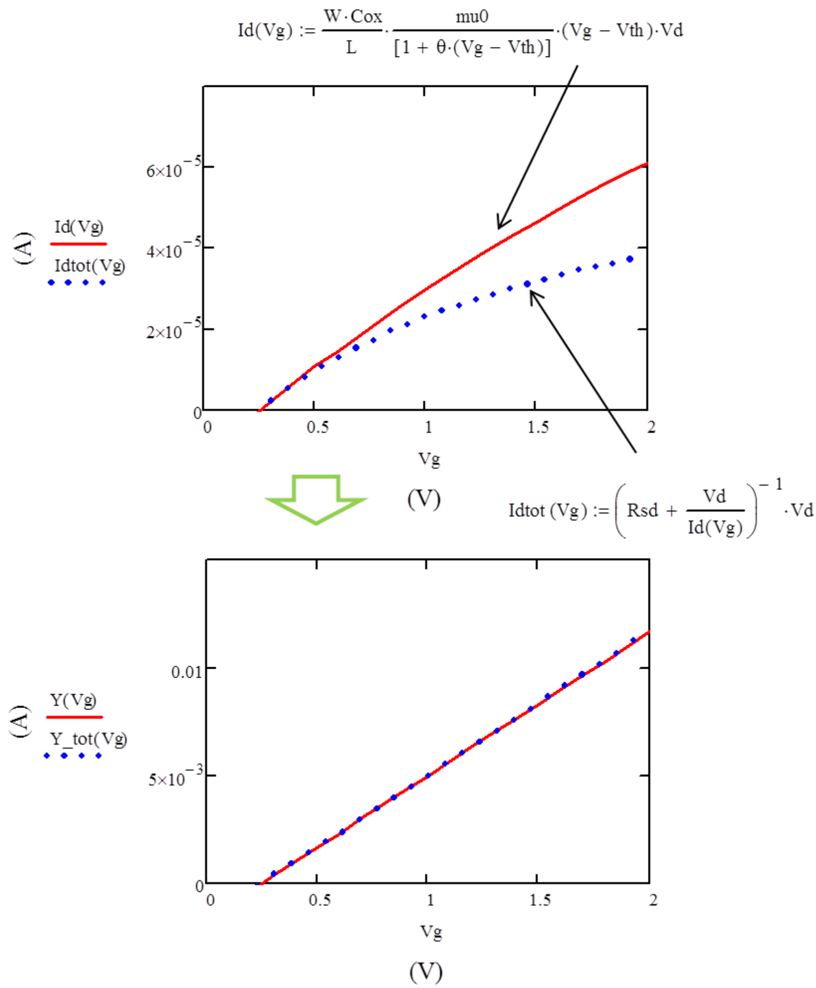


Figure 11. Influence of series resistance on the transfer curve and Y-function in a MOSFET.

1.3.2 Other methods for the extraction of threshold voltage

1.3.2.1 Linear extrapolation method (V_{text})

The V_{text} can be defined as the linear extrapolation to zero drain current on I_d vs V_g curve at a V_g decided at a maximum in the transconductance g_m as [11]:

$$V_{text} = V_{g_max} - \frac{I_{d_max}}{g_{m_max}} \qquad (19)$$

where V_{g_max} and $Id_{_max}$ are the gate voltage and the drain current at a maximum transconductance (g_{m_max}), respectively. However, the linear extrapolation method is readily affected by series resistance and mobility degradation effects.

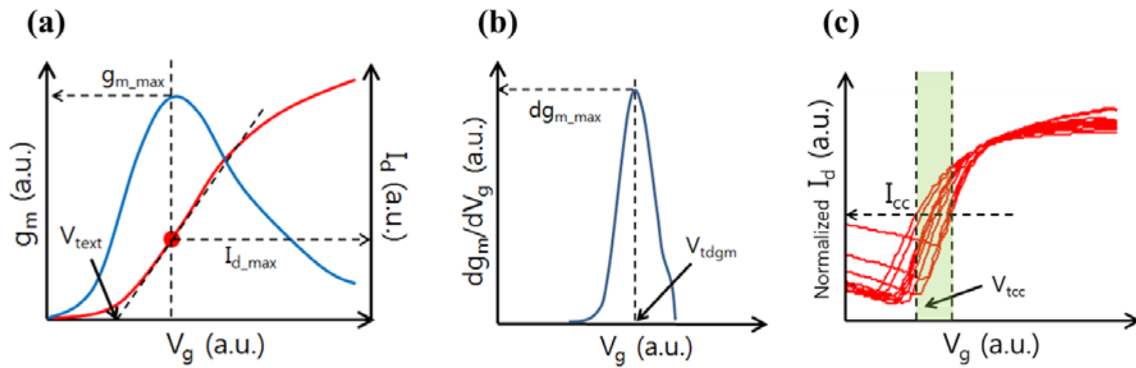


Figure 12. Extraction of threshold voltage by using (a) linear extrapolation method, (b) maximum derivative of transconductance and (c) constant current technique.

1.3.2.2 Maximum derivative of transconductance (V_{tdgm})

The V_{tdgm} can be extracted from the peak in the derivative of transconductance. This method is known as less affected by series resistance and mobility degradation effect.

1.3.2.3 Constant current technique (V_{tcc})

V_{tcc}, which is a widely used method, can be determined at V_g for a given drain current normalized by device geometry [V_{tcc}=V_g at I_d×(L/W)=$I_{constant}$]. This method is very little affected by series resistance or mobility attenuation effects.

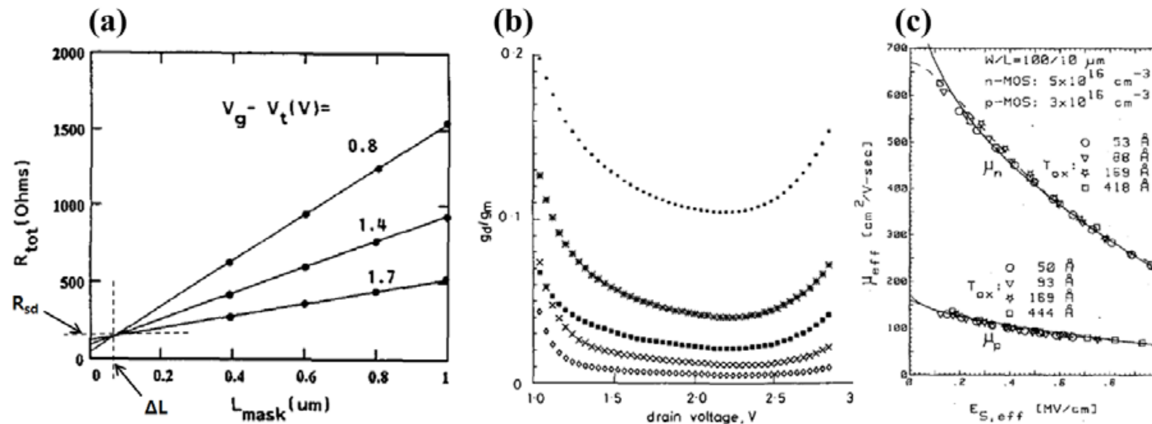


Figure 13. (a) TLM method for the extraction of R_{sd} and ΔL [12]. (b) Variations of g_d/g_m vs V_d for DIBL. (c) The relation between effective mobility and transverse electric-field [15].

1.3.3 Transfer length method (TLM)

If the channel width W of a transistor is long enough, the total resistance including both the channel and S/D resistance can be given as [12]:

$$R_{tot}(V_g) = R_{sd} + \rho_{ch}(V_g) \cdot \frac{L_M - \Delta L}{W_M} \qquad (20)$$

where ρ_{ch} is the channel sheet resistance and ΔL is the channel length difference between effective and on-mask channel lengths (L_M). Therefore, the R_{tot} can be plotted as a function of on-mask gate length and one can also obtain several R_{tot} vs L_M plots with varying V_g. Finally, the R_{sd} is extracted from the common intersection point of the straight lines obtained at each V_g. One can also get the channel length reduction ΔL from the common intersection point as shown in Fig. 13(a).

1.3.4 Drain induced barrier lowering (DIBL)

When the drain becomes very close to the source in the short length device, the drain voltage can influence the potential barrier at the source end. In this case, the gate controllability for the channel is reduced and this can be called the drain induced barrier lowering (DIBL). The magnitude of the DIBL is normally defined as [13]:

$$DIBL = \frac{V_{th}|_{V_{d1}} - V_{th}|_{V_{d2}}}{V_{d2} - V_{d1}} \qquad (21)$$

where V_{d1} and V_{d2} are usually tens of mV range (≈ 50 mV) and ≈ 1 V, respectively. However, this method has an issue regarding the uncertainties associated with the determination of V_{th}. Another method for the extraction of DIBL has been suggested [14]. The DIBL parameter λ can be obtained by the normalized sensitivity of the saturation drain current with respect to the gate voltage sensitivity as:

$$\lambda = \left[\frac{d\ln(I_d)}{dV_d} \Big/ \frac{d\ln(I_d)}{dV_g} \right] = \frac{g_{d_sat}}{I_d} \Big/ \frac{g_{m_sat}}{I_d} \qquad (22)$$

where g_{d_sat} and g_{m_sat} mean the saturation output conductance and the saturation transconductance, respectively. One can extract the DIBL parameter for all the regions from linear to saturation operation in MOS devices and it can also avoid the uncertainties about V_{th} values.

1.3.5 Effective mobility and its degradation due to the transverse electric field

The effective mobility (μ_{eff}) in MOSFET can be calculated as [11, 12]:

$$\mu_{eff} = \frac{I_d \cdot L^2}{Q_n \cdot V_d} \quad (23)$$

where Q_n represents the mobile channel charge. In strong inversion, Q_n can be approximately given by Q_n=$C_{ox}(V_g-V_{th})\times LW$, although the mobile charge starts to grow in the sub-threshold regime. The Q_n measured from the so called split CV technique gives better results according to:

$$Q_n = \int C_{gc}(V_g)dV_g \qquad (24)$$

where C_{gc} is the gate to channel capacitance. C_{gc} measurement method by the split CV technique will be detailed in next chapter.

As the gate voltage increases, the μ_{eff} is reduced owing to enhancement of surface roughness scattering. The μ_{eff} affected by the transverse electric field from the gate voltage is expressed as [15, 16]:

$$\mu_{eff} = \frac{\mu_0}{1+(E_{eff}/E_c)^{\alpha}} \quad (25)$$

where E_{eff}, E_c and α represent the effective transverse electric field, the critical electric field and exponent for mobility attenuation (typically, ≈ 1.5 for electrons and ≈ 1 for holes), respectively.
Figure 13(c) shows the reduced μ_{eff} as increasing the transverse electric field $E_{s.eff}$.

1.3.6 Doping concentration extraction using Maserjian's function

The effective (or activated) doping concentration in the MOS transistors can be extracted by using the so called Maserjian's function (Y_M) written as [17, 18]:

$$Y_M = \frac{1}{C_{gc}{}^3} \cdot \frac{\partial C_{gc}}{\partial V_g} = \frac{1}{C_{sc}{}^3} \cdot \frac{\partial C_{sc}}{\partial V_s} \qquad (26)$$

where C_{sc} and V_s are the semiconductor capacitance and the surface potential, respectively. It is important to note that Y_M is related to the characteristics of the substrate capacitance alone, regardless of oxide capacitance.

In depletion regime, the conventional $1/C^2$ vs V_g relation is given as:

$$\frac{1}{C_{gc}{}^2} = \frac{1}{C_{ox}{}^2} + \frac{2}{q\varepsilon_{si}N_a}(V_g - V_{fb}) \qquad (27)$$

where N_a and ε_{si} are the P-type substrate doping concentration and the silicon permittivity. Finally, the doping concentration is expressed by proper calculation between above two equations:

$$N_a = -\frac{1}{q \cdot \varepsilon_{si} \cdot Y_M} \qquad (28)$$

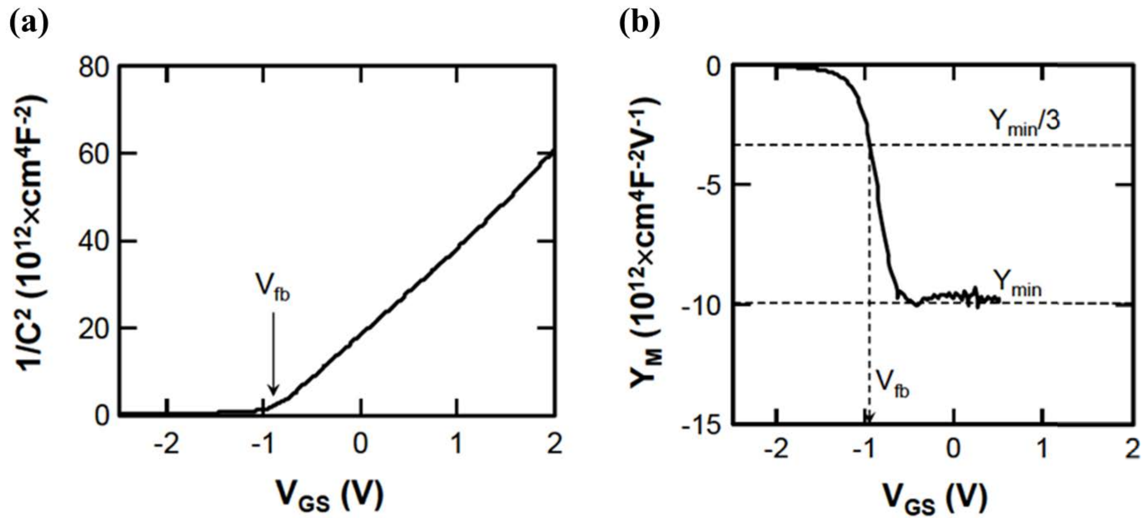


Figure 14. (a) $1/C^2$ plot vs V_{gs} for V_{fb} extraction. (b) Maserjian's function vs V_{gs} for V_{fb} and the substrate doping [17].

1.3.7 Subthreshold swing (S)

The weak inversion channel between flat band and threshold leads to some drain conduction even below threshold. This is called as subthreshold conduction. The drain current under the subthreshold region can be equal to [19]:

$$I_d = \mu(C_d + C_{it})\frac{W}{L}\left(\frac{kT}{q}\right)^2 \cdot \left(1 - e^{\frac{-qV_d}{kT}}\right) \cdot e^{\frac{q(V_g - V_{th})}{\left(1+\frac{C_d + C_{it}}{C_i}\right)kT}} \qquad (29)$$

where C_i, C_d and C_{it} denote gate insulator, depletion and interface-state MOS capacitance per unit area, respectively. Then, the subthreshold swing (S) showing the steepness of the transition between the off-state and the on-state is defined as:

$$S = \frac{dV_g}{d(\log I_d)} = \ln 10 \frac{dV_g}{d(\ln I_d)} = 2.3\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_i}\right) \qquad (30)$$

The S value cannot be lower than 2.3kT/q (i.e. 60 mV/decade) at room temperature (T = 300 K), since it is limited by thermodynamics.

1.4 Measurement technique with instruments and numerical simulation

1.4.1 Theoretical measurement limits for different type of instruments

The sensitivity in any measurements is limited by the fundamental noise generated by their own resistance (so-called thermal noise) in the samples. The voltage noise from this theoretical limit is proportional to the resistance. For instance, it is impossible to measure a 1μV signal from a 1T Ω resistance due to the limit of the theoretical sensitivity, even with any great instruments [20].

All instruments also have input offset current, whose unwanted current makes an error. The measurement sensitivity in the instruments is also limited by the magnitude of the input offset current. Therefore, one should firstly choose a proper instrument with carefully considering above limitations before starting the measurements.

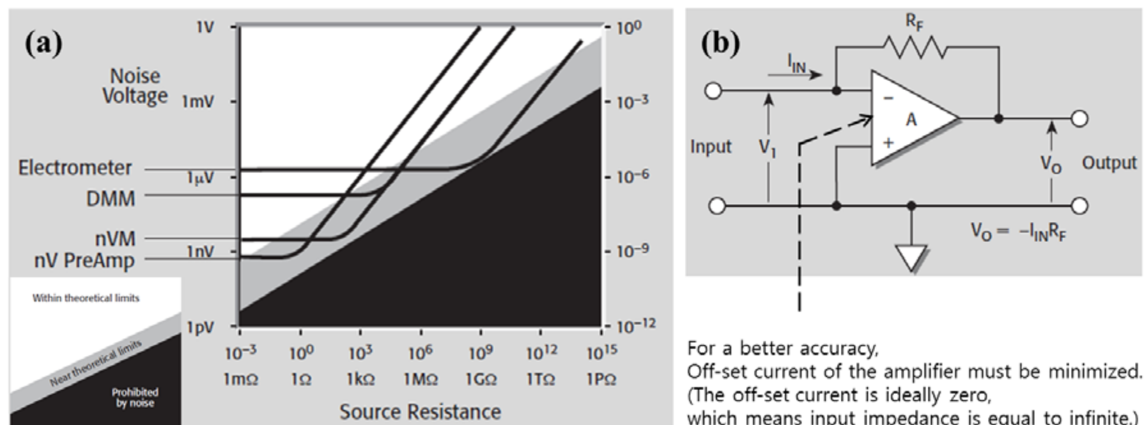


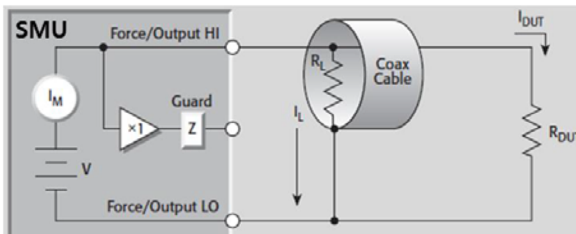
Figure 15. (a) Theoretical limits of voltage measurements and system limits in instruments. (b) Electrometer circuit [20].

1.4.2 Principle of guarding the tri-axial connector for measuring high resistance

There are two general type of connectors such as coaxial connector BNC and triaxial connector including an additional inner shield (Guard). In the case of unguarded circuits with BNC, the leakage current between signal line to ground shield could occur with very high resistance sample. The guard-

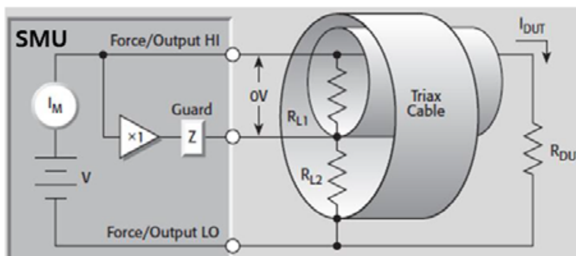
ed circuit with triaxial cable can completely remove the unwanted leakage current using guard line connected to signal with buffer [20]. Moreover, RC delay time in the measurements with high resistance samples can be significantly removed using the guarded circuit, owing to zero capacitance between the signal line to the guard.

Unguarded circuit



R_L=Coaxial cable leakage resistance
I_L=Leakage current
R_{DUT}=Resistance of device under test
Therefore, $I_M=I_{DUT}+I_L$

Guarded circuit



R_{L1}=Triaxial cable inside shield leakage resistance
R_{L2}=Leakage resistance between shields
R_{DUT}=Resistance of device under test
Therefore, $I_M=I_{DUT}$

Figure 16. Illustration showing the principle of the guarded circuit with triaxial cable [20].

1.4.3 Split C-V method

The split C-V method uses two separated measurements for the gate capacitance in MOS transistors [10, 21], such as the bulk vs V_g (for bulk capacitance C_b) and S/D vs V_g (for S/D capacitance C_d+C_s or gate to channel capacitance C_{gc}).

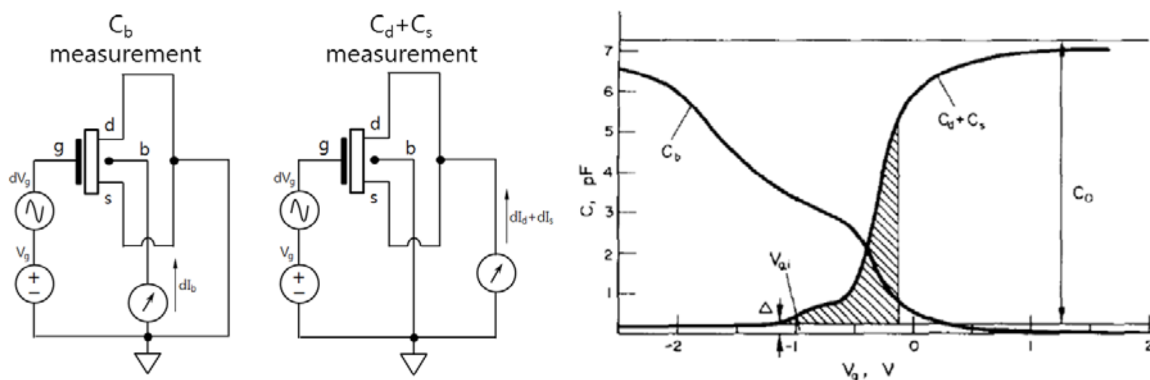


Figure 17. Scheme of split CV measurement and its typical characteristics [21].

The C_b has been measured with respect to mobile charges in accumulation mode, while the C_d+C_s is related to inversion carriers. The charge trapped interface states in weak and intermediate inversion and the bulk doping density can be simply determined by the split C-V method.

1.4.3.1 C_b measurement

For V_g<V_{fb}, the C_b saturated toward C_b maximum value, which provide to extract C_{ox}. Then, with the increase of V_g, the C_b is getting decreased due to the depletion regions grow. For further increasing V_g up to V_g>V_{th}, the C_b goes to zero, since the inversion channel from source to drain shields the small signal variation of V_g for the capacitance measurements.

1.4.3.2 C_d+C_s measurement

For V_g<V_{fb}, the C_d+C_s goes toward zero, since the mobile carriers in the accumulation mode cannot be observed due to S/D depletion regions. However, the C_d+C_s starts to increase as increasing V_g. Then, it reaches its maximum value. This can also give the information about C_{ox}.

1.4.4 The iteration method and overview of numerical simulation

Let us assume a 2-dimensional potential problem with a region divided into squares of side h [22]. There are five potential values indicated as V_0, V_1, V_2, V_3 and V_4. We will see how V_0 can be reasonably decided from other 4 values (V_1 to V_4). If the defined region is in charge-free space and contains a homogeneous dielectric, then $\nabla \cdot D = 0$ and $\nabla \cdot E = 0$. In 2-dimensions,

$$\frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0 \qquad (31)$$

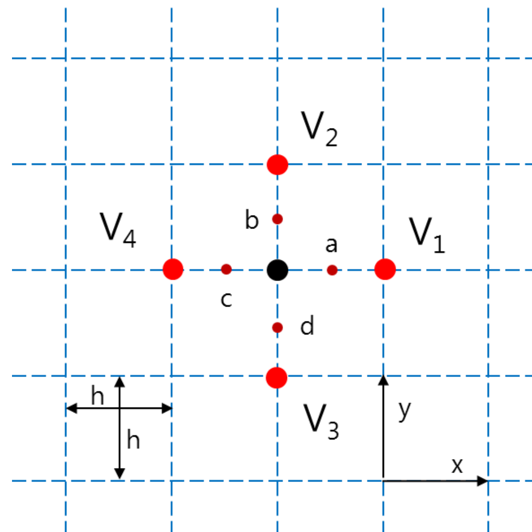


Figure 18. The potential V_0 in the center (black dot) is approximately calculated by the average of the potentials from the four near points. $V_0 = (V_1+V_2+V_3+V_4)/4$.

The values for these partial derivatives may be approximately obtained in terms of the assumed potentials:

$$\left.\frac{\partial V}{\partial x}\right|_a \approx \frac{V_1 - V_0}{h} \quad \text{and} \quad \left.\frac{\partial V}{\partial x}\right|_c \approx \frac{V_0 - V_4}{h} \qquad (32)$$

$$\text{therefore,} \quad \left.\frac{\partial^2 V}{\partial x^2}\right|_0 \approx \frac{\left.\frac{\partial V}{\partial x}\right|_a - \left.\frac{V}{x}\right|_c}{h} \approx \frac{V_1 - V_0 - V_0 + V_4}{h^2} \qquad (33)$$

$$\text{and similarly,} \quad \left.\frac{\partial^2 V}{\partial y^2}\right|_0 \approx \frac{V_2 - V_0 - V_0 + V_3}{h^2} \qquad (34)$$

So, one can get

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} \approx \frac{V_1 + V_2 + V_3 + V_4 - 4V_0}{h^2} = 0 \qquad (35)$$

Finally, $V_0 \approx \frac{1}{4}(V_1 + V_2 + V_3 + V_4)$

If the h value is very small, V_0 will be exactly same to $1/4 \cdot (V_1+V_2+V_3+V_4)$. Likewise, the iterative method uses these equations to determine the potential at every subdivision square in turn, and then the process is repeated until all the values don't change any more.

As the process and the structure of current device become more complex for the better performance, solving the analytical equations for interpretation of the device is getting more difficult. In addition, the experimental method is getting difficult to design and the cost for the experiments increases, respectively [23].

On the other hand, numerical simulation becomes more attractive thanks to noticeable progress in personal computer (PC) technology. The physical fabrication process as well as the electrical performance prediction of devices can be numerically simulated with high accuracy. The numerical simulation can also combine with analytical expressions for the better results and save the required calculation time. However, experimental analysis should be done to confirm the predictions of simulations.

1.4.5 Quantum effects considered calculation

With the fin height or width of less 10 nanometers in 3D Fin-FET structure devices, volume inversion channel can appear in the center of the Si, which is quite different from what is interpreted by classi-

cal theory [24]. To account for quantum effects at the interfaces, we used the quantum correction proposed by Haensch [25], transposed to a 2D geometry:

$$n_{QM} = n_C \cdot \left[(1-e^{\frac{-y^2}{\lambda^2}}) \cdot (1-e^{\frac{-(H_{si}-y)^2}{\lambda^2}}) \right] \cdot \left[(1-e^{\frac{-x^2}{\lambda^2}}) \cdot (1-e^{\frac{-(W_{si}-x)^2}{\lambda^2}}) \right] \qquad (36)$$

where n_c is the carrier density derived from classical theory. H_{si}, W_{si} and λ also denote Fin-height, Fin-width and the electron thermal wave length (typically ≈ 1nm), respectively.

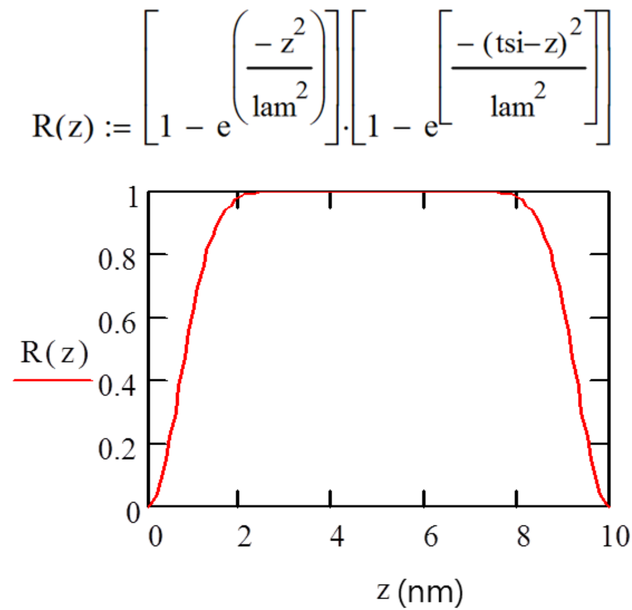


Figure 19. The function leading to Quantum effects with λ ≈ 1 nm [25].

The quantum correction leads to an increase of mobility, since the volume inversion carriers includes less interface scattering compared to surface conduction carrier. However, the inversion carriers in the extremely thin Si film are affected again to surface scattering owing to their physical limits to the interfaces.

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Chapter 2

Electrical characterization of junctionless transistors

2.1 Revisited parameter extraction methodology

2.2 Effects of channel width variation on electrical characteristics of tri-gate junctionless transistors

Several electrical parameters characterize device performance, electron transport and doping level in MOS transistors. In this chapter, Junctionless Transistors (JLT) fabricated on (100) silicon on insulator (SOI) wafer with 145 nm thick BOX and ≈ 9 nm silicon thickness were considered. Parameter extraction methodologies were revisited in order to account for the unique electrical properties of JLT devices. Some of the revisited conventional methods used for the parameter extraction in JLT devices are still valid, because JLT devices show the surface accumulation channel behavior at $V_g > V_{fb}$ like inversion mode transistors. On the other hand, the other conventional methods should be revised for JLT devices even though the methods allow us to assume the electrical performance of JLT devices. The deduced parameters, such as threshold voltage, flat-band voltage, drain induced barrier lowering (DIBL), low field mobility and channel doping level, are shown to reveal the specific features of JLT compared to conventional inversion-mode transistors.

The electrical behavior of tri-gate Junctionless transistors (JLT) depending on top-effective width (W_{top_eff}) was investigated, experimentally. As decreasing W_{top_eff}, the amount of bulk neutral channel is relatively getting smaller than that of surface accumulation channel, whereas the channel sidewall gate effect is reinforced. These cause the shrinkage of the shoulder shape on the gate-to-channel ca-

pacitance characteristics (C_{gc}-V_g), resulting in a noticeable change in the effective mobility (μ_{eff}) behavior from that in wide JLT devices, an increase of the threshold voltage (V_{th}), while the flat-band voltage (V_{fb}) doesn't change. 2D numerical simulation results, well consistent to the experimental results, confirm the significant sidewall gate effect in the tri-gate JLT devices with a narrow structure.

2.1 Revisited parameter extraction methodology

2.1.1 Introduction

Recently, much attention has been focused on the Junctionless Transistor (JLT) as a possible candidate for the continuation of Moore's law [1, 2]. Although its operation is governed by field-effect, the use of a doped channel, with the same doping type as in source and drain regions, brings specific features to the JLT, with promising advantages compared to the standard inversion-mode (IM) MOSFET. The most immediate advantage is that JLT fabrication is made easier thanks to its simple structure, without PN junctions nor doping concentration gradient near source and drain regions. Secondly, the field-effect operation is based on bulk conduction instead of surface conduction for IM transistors so that the requirement in terms of gate insulator thickness can be relaxed and mobility degradation by transverse electric field is reduced. However, there are still several issues related to JLT devices such as trade-off between high level of channel doping and bulk mobility degradation, reduced gate controllability due to larger electrical oxide thickness and the variability of threshold voltage according to both device silicon thickness (t_{si}) and doping concentration [1-4].

For this chapter, JLT devices with nanowire-like tri-gate structures, as well as planar structures, were fabricated on silicon on insulator (SOI) wafers with a silicon thickness, t_{si}, of ≈ 9 nm. The methodologies used to extract electrical parameters were revisited and adapted to the JLT mode of operation, in order to allow above mentioned issues to be studied on a physically grounded basis. Some of electrical properties of JLT devices were also compared to those of undoped inversion-mode (IM) transistors fabricated by the same process except for channel doping concentration. The electrical parameters extracted for the JLT devices give clear evidence of the specificities of their operation.

2.1.2 Device fabrication and experiment

For this study, N-type JLT devices with high-k/metal gate stack were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick BOX and Si body thinned down to ≈ 9 nm. The channel implant was performed before gate patterning with a phosphorus doping targeted at 1×10^{19} cm^{-3} or 2×10^{19} cm^{-3}. After optical lithography (193 nm tool), channel width was trimmed by reactive ion etching (RIE). The gate consisted in an HfSiON/ TiN/ Polysilicon stack. Equivalent oxide thickness was 1.2 nm. An

additional implantation was performed to source and drain regions with the aim of improving electrical performance by reducing access resistance. Figure 1(a) displays the schematic architecture of the fabricated JLT devices, as well as the transmission electron microscopy (TEM) cross-section of a narrow device. As shown in Fig. 1(b), on-mask gate width W_M was ranging from 10 μm (wide planar devices) to 80 nm (nanowire-like tri-gate devices). On mask gate length L_M ranged from 10 μm down to 30 nm. Arrays of nanowires were available, making capacitance measurements possible for the smallest devices.

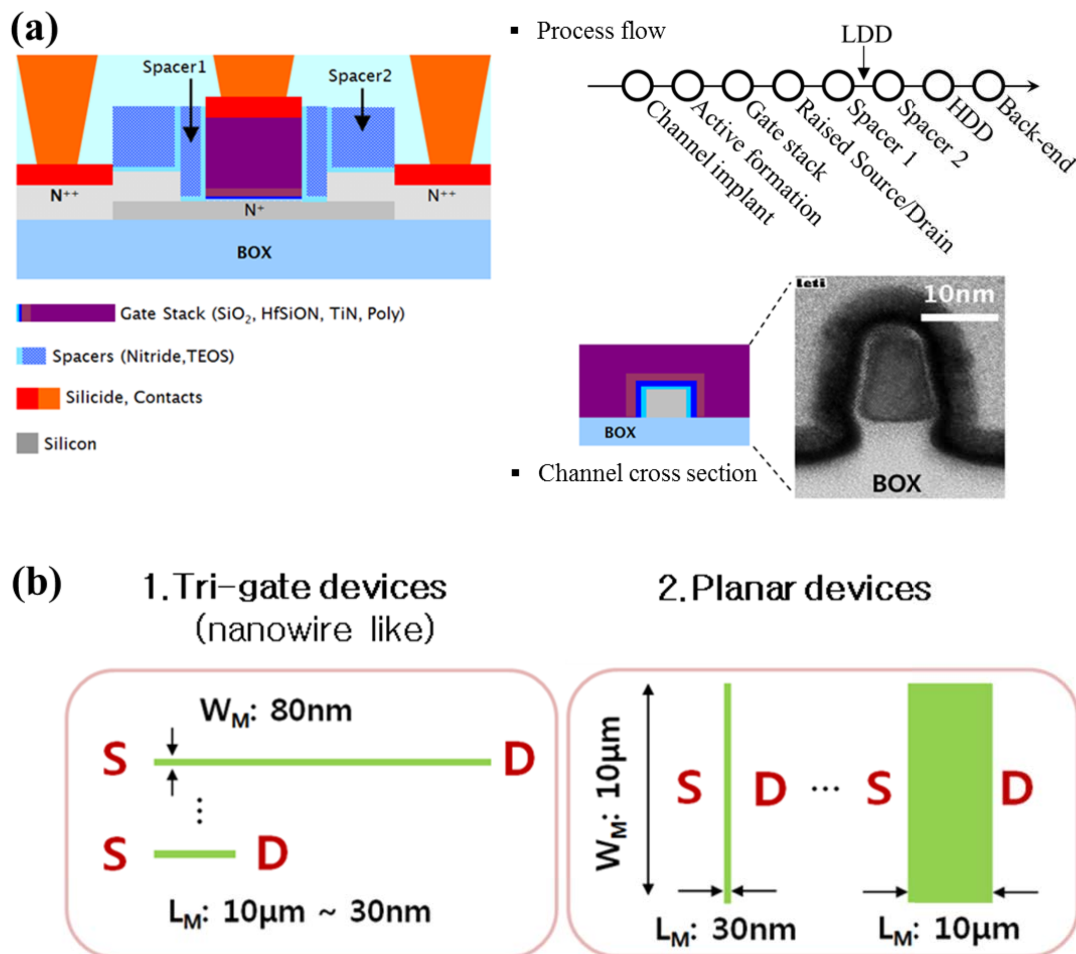

Figure 1. (a) Schematic cross-section along channel direction (left) and across the channel of a narrow device and transmission electron microscopy (TEM) cross-section showing the structure of a fabricated narrow device (bottom right). (b) Schematic plane-view showing the range of length and width dimensions of the JLT devices used for this study, ranging from nanowire-like tri-gate structures to wide planar structures, both of varying length.

The I-V current-voltage characteristics were recorded using an HP4155a measurement unit and the C-V capacitance-voltage measurements were carried out using HP4294a with a 50 mV sm

all signal at 500 kHz. The gate-to-channel capacitance C_{gc} was extracted from C-V measurements by connecting the “high” terminal of HP4294a to gate electrode and “low” terminal to source and drain electrodes, while the bias applied to the substrate was varied from −30 V to +30V. Gate voltage will be called V_{gf}.

2.1.3 Experimental results and discussion

2.1.3.1 Electrical parameters of JLT devices based on Current-Voltage characteristics

Starting with planar devices (W_M = 10 µm), drain current (I_d) and transconductance (g_m) were measured as a function of V_{gf} for gate lengths down to 30 nm (Figs. 2(a) and 2(b)). The corresponding $Y(V_{gf})$ function, defined as [5]:

$$Y(V_{gf}) = I_d / \sqrt{g_m} \qquad (1)$$

which was used for threshold voltage (V_{ty}) and low field mobility (μ_0) extraction, is plotted in Fig. 2(c).

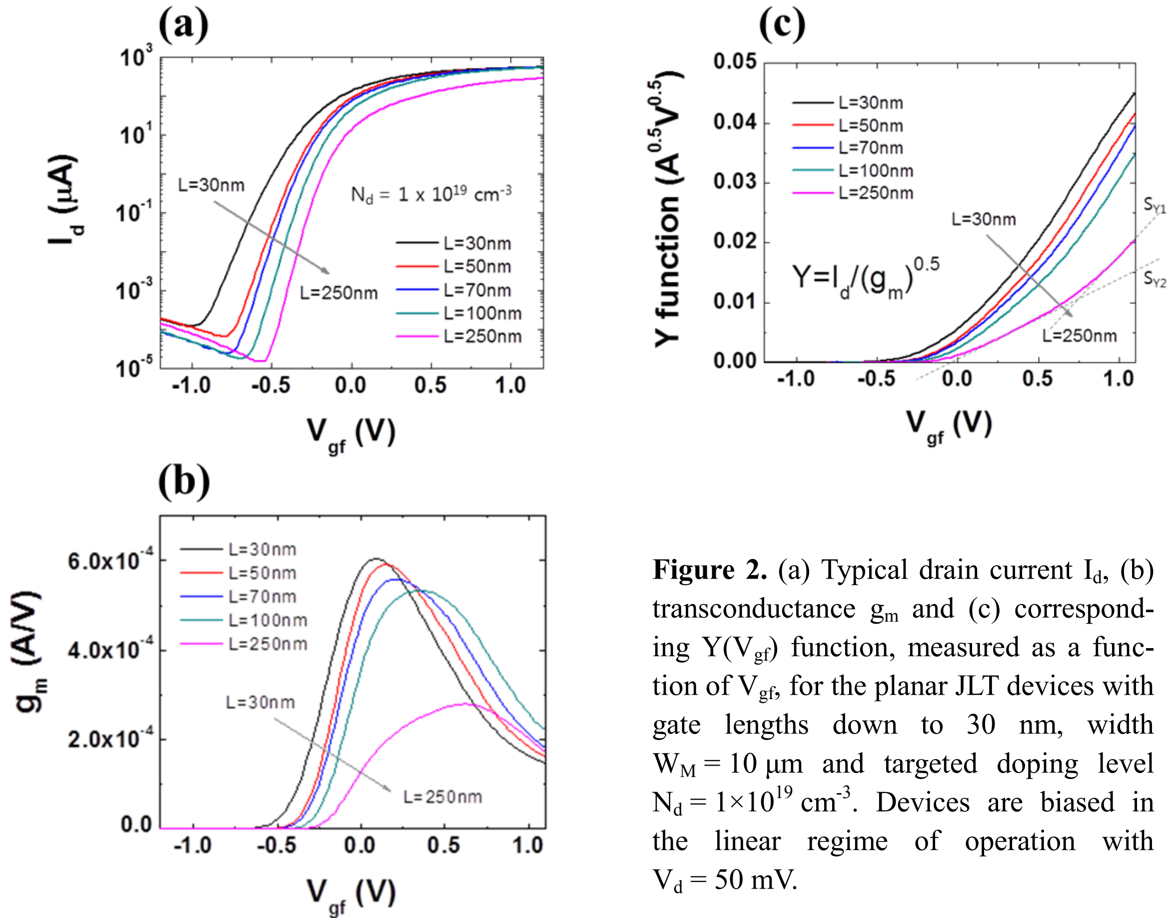

Figure 2. (a) Typical drain current I_d, (b) transconductance g_m and (c) corresponding $Y(V_{gf})$ function, measured as a function of V_{gf}, for the planar JLT devices with gate lengths down to 30 nm, width W_M = 10 µm and targeted doping level $N_d = 1\times10^{19}$ cm^{-3}. Devices are biased in the linear regime of operation with V_d = 50 mV.

Before discussing these plots, it is worth remembering the principle of JLT operation. Below threshold, the channel of n-type JLT devices is fully depleted. As gate voltage is increased, operation mode is evolving from full depletion (no conduction) to partial depletion (bulk conduction with gate controlled channel thickness). When gate voltage reaches flat-band voltage (V_{fb}), the depleted region vanishes and the whole silicon layer becomes neutral with a carrier concentration equal to doping level N_d. As gate voltage is further increased above V_{fb}, an accumulation layer grows at the front gate interface. Thus, JLT devices operation involves two successive conduction regimes separated by the flat-band voltage V_{fb}: volume conduction through a neutral bulk channel below V_{fb}, and dominant conduction through a surface accumulation layer above V_{fb}. [1, 2].

Flat-band voltage

Interestingly, two slopes showing evidence of accumulation regime (S_{Y1}) and neutral channel (S_{Y2}) were recognized on the Y-function in Fig. 2 (c). This is clearly different from IM transistors, which normally show one single slope only. The existence of these two slopes is better evidenced in Fig. 3 (b) where plateaus are seen on the derivative of $Y(V_{gf})$ functions. Moreover, Figure 3 (a) shows the derivative of the transconductance (dg_m/dV_{gf}) corresponding to Fig. 2(b). Two peaks on the dg_m/dV_{gf} plots were observed, although for large gate lengths only, owing to reduced mobility degradation and series resistance (R_{SD}) effects as compared to smaller gate lengths. The gate voltage at first peak is representative of the conduction threshold voltage (V_{th}), which corresponds to the turning point from full to partial depletion in the channel, whereas the second peak gives V_{fb} position, separating neutral channel from surface accumulation. The value of V_{fb}, as obtained from the second peak on the dg_m/dV_{gf} plots, was found equal to about 0.56 V, which is consistent with the theoretical value of 0.528 V calculated using the following equation:

$$V_{fb} = \Phi_{MS} = \Phi_M - \left\lfloor \chi + \frac{E_g}{2} - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_d}{N_i}\right) \right\rfloor \quad (2)$$

where Φ_M, χ and N_i denote work function of metal, electron affinity and intrinsic carrier density, respectively. $V_{fb} \approx 0.56$ V is also consistent with the value of V_{gf} at near boundary between first and second plateau regions in Fig 3. (b) (see the dotted grey line across Figs. 3(a) and 3(b)). A higher V_{fb} value of ≈ 0.62 V and lower threshold voltages were observed in JLT devices featuring a larger doping level of 2×10^{19} cm^{-3}, as shown in Fig. 3 (c) and (d). These results for V_{th} and V_{fb} agree well with the expected doping concentrations in the channel.

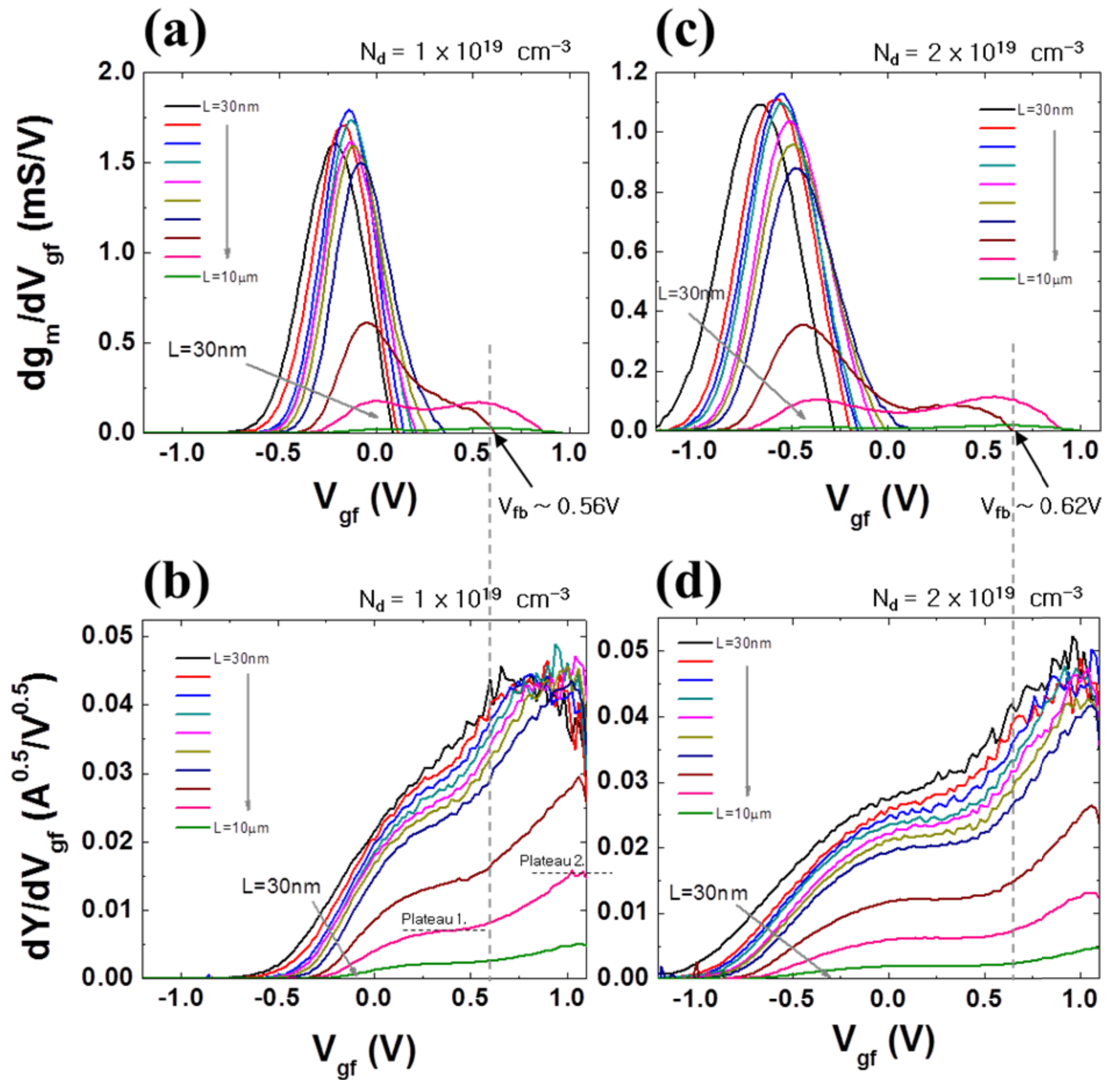

Figure 3. (a) Derivative of the transconductance (dg_m/dV_{gf}) and (b) derivative of the Y function (dY/dV_{gf}) corresponding to the results shown in Fig. 2 with a doping level $N_d = 1\times10^{19}$ cm^{-3}. (c) and (d): Same plots for twice as large doping concentration, $N_d = 2\times10^{19}$ cm^{-3}.

Conduction threshold voltage

In previous section, the conduction threshold voltage (V_{th}) of JLT devices was defined as the gate voltage at the boundary between full and partial channel depletion. Interestingly, another kind of threshold voltage, called V_{ton}, which is positioned between V_{th} and V_{fb}, has also been defined in the literature for JLTs [4]. The threshold voltage V_{ty} extracted using Y-function was compared with the values deduced from other methods such as linear extrapolation of transfer characteristics (V_{text}), maximum derivative of transconductance (V_{tdgm}) and constant current technique (V_{tcc}) [6]. V_{text} and V_{ty} extraction was carried out using the maximum value of transconductance (g_{m_max} in Fig. 2(b)), and Y-

function extrapolation in the accumulation region (at $V_{gf} \approx 1.0$ V in Fig. 2(c)), respectively. The position of the first peak in the dg_m/dV_{gf} plots was selected for the determination of V_{tdgm}, and the drain current normalized by L_M/W_M was set to a constant value of 10^{-7} A for V_{tcc} extraction. The comparison between all these different definitions of the threshold voltage is displayed in Fig. 4 for the whole range of gate lengths. One should note an overall roll-off of threshold voltages with decreasing gate lengths, due to short channel effects, regardless of methods. However, using V_{text} and V_{ty}, it is hard to find the exact information about V_{th} for JLT devices. Indeed, V_{th}, V_{ton} and V_{fb} cannot be distinguished from the transconductance plot for the V_{text} method, as seen from Fig. 2(b).

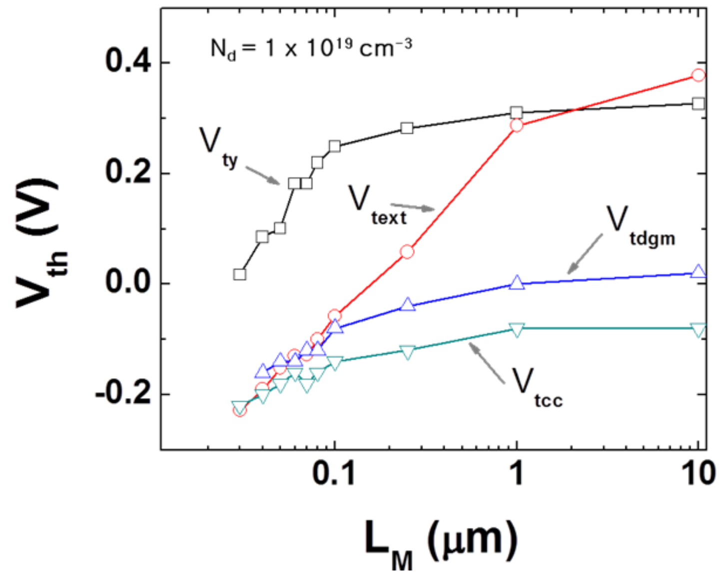

Figure 4. Threshold voltages (V_{th}) versus gate lengths extracted by various methods, such as Y-function (V_{ty}), linear extrapolation of transfer characteristics (V_{text}), maximum derivative of transconductance (V_{tdgm}) and constant current technique (V_{tcc}).

It is also known that the linear extrapolation method is affected by series resistance and mobility degradation effects. Moreover, even if the Y function could in principle allow extraction of V_{th} using the intermediate V_{gf} range (slope S_{Y2} in Fig. 2), this range of voltages is too narrow to allow precise extraction, while extraction at large gate voltage, as performed for Fig. 4, mixes information about V_{th}, V_{ton} and V_{fb}. This explains why V_{text} and V_{ty} are relatively larger than V_{tdgm} and V_{tcc} in Fig. 4 and further study should be needed for the revised linear extrapolation and Y-function method to extract the exact V_{th} in JLT devices. On the other hand, V_{tdgm} and V_{tcc} can provide relevant information about V_{th} in JLT devices, as the peaks on the derivative of transconductance in Fig. 3 can provide the positions of V_{th} and V_{fb} rather accurately and as there are relatively less series resistance and mobility degradation effects compared to other methods.

Source/Drain series resistance

The series resistance (R_{SD}) of JLT devices was first extracted from the plot of the first-order attenuation factor (θ_e), measured for devices of varying length, as a function of their conductance gain (β), with the equation given by [7] in the Y-function formalism:

$$\theta_e = \frac{\beta \cdot V_d}{I_d} - \frac{1}{V_g - V_{ty}} = \theta + \beta \cdot R_{SD} \qquad (3)$$

where V_d and V_g refer to the applied drain and gate voltage, including the presence of R_{SD}, at source and drain terminals and θ represents the first order mobility attenuation factor, respectively. The value of R_{SD} obtained from the slope of this plot was around ≈ 620 Ω·μm for 10 μm wide JLT devices, as shown in Fig. 5(a). The R_{SD} value can also be found by the transfer length method (TLM). The total resistance of the device (R_{tot}) including R_{SD} and channel resistance can be expressed by [6]:

$$R_{tot}(V_g) = R_{SD} + \rho_{ch}(V_g) \cdot \frac{L_M - \Delta L}{W_M} \qquad (4)$$

where ρ_{ch} is the channel sheet resistance. ΔL is the channel length difference between effective and on-mask channel lengths, L_{eff} and L_M, respectively. R_{tot} is plotted as a function of gate length in Fig. 5(b).

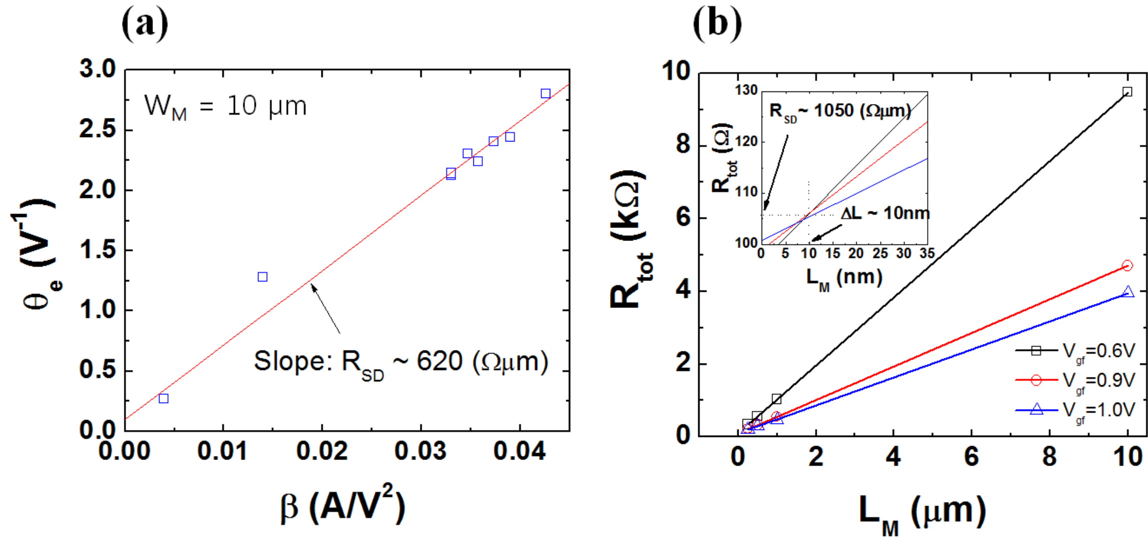

Figure 5. (a) Extraction of the series resistance of wide JLT devices (W = 10 μm) using the first-order attenuation factor (θ_e) versus conductance gain (β) plot, based on Y-function extraction for JLT devices of varying gate length. The extracted value amounts to R_{SD} ≈ 620 Ω·μm. (b) Direct plot of the total resistance (R_{tot}) versus gate length for determination of R_{SD} (≈ 1050 Ω·μm) and ΔL (≈ 10 nm).

The R_{SD} value was extracted from the common intersection point of the straight lines obtained at each V_{gf}, as shown in the zoomed view in the inset of Fig. 5(b). It amounted to ≈ 1050 Ω·µm, which is quite consistent with the R_{SD} (≈ 620 Ω·µm) extracted from the first order attenuation factor, even though further study is needed with an analytical model for JLT devices in the Y-function based method. Moreover, it allowed channel length reduction (ΔL) to be obtained, with a value of ≈ 10 nm, from the common intersection point.

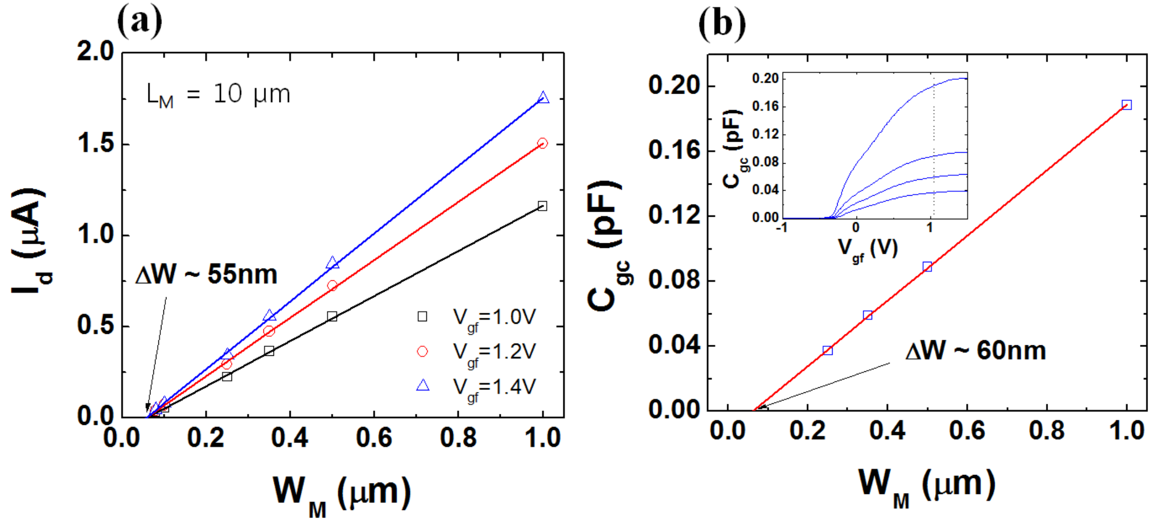

Figure 6. (a) Drain current I_d versus gate width for extraction of ΔW (≈ 55 nm). (b) Gate-to-channel capacitance C_{gc} versus gate width for extraction of ΔW (≈ 60 nm). For better accuracy of C_{gc} values, long JLT devices (L = 10 µm) were used, in arrays of 50 parallel channels. Devices were biased in the linear regime of operation with V_d = 50 mV.

Channel width reduction

The extraction of channel width reduction in JLT devices (ΔW, between effective and on-mask device widths) can be carried out using the linear relationship between drain current (I_d) and channel width (W_M) with following equation [6]:

$$I_d(V_g) = \frac{V_d}{\rho_{tot}}(V_g) \cdot \frac{W_M - \Delta W}{L_M} \quad (5)$$

where ρ_{tot} represents the total sheet resistance containing both channel and series resistance. Extrapolation to zero gate width led to a value of ≈ 55 nm for ΔW, as shown in Fig. 6(a). Similarly, the linear relationship between gate-to-channel capacitance (C_{gc}) and channel width (W_M) can provide ΔW. Indeed, C_{gc} can be expressed as [7, 8]:

$$C_{gc} = C_{ox} \cdot L_M \cdot (W_M - \Delta W) \quad (6)$$

where C_{ox} is the oxide capacitance per unit area. For long devices, L_M can be used instead of L_{eff} in this equation. A value of ≈ 60 nm, which fits well to previous value (≈ 55 nm), was extracted from the plot of C_{gc} versus W_M in Fig. 6(b). However, the value of ≈ 60 nm obtained from the C_{gc} versus W_M plot might be closer to the exact value of ΔW, because there is no mobility degradation and series resistance effects in this method.

Mobility

Figure 7 shows the low field electron mobility (μ_0) and the maximum field effect mobility (μ_{femax}) as a function of effective channel length (L_{eff}) for JLT devices with different doping levels (1×10^{19} cm^{-3} and 2×10^{19} cm^{-3}). The low-field mobility was extracted from the square of Y-function slope $(dY/dV_{gf})^2$, taken in the linear region of $Y(V_{gf})$ which is observed in accumulation, using the following relationship [5]:

$$\left(\frac{dY}{dV_{gf}} \right)^2 = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot V_d \qquad (7)$$

Extraction was performed for $V_{gf} \approx 1.0$ V, larger than V_{fb} (refer to Fig. 2(c)). The low-field mobility μ_0 extracted by equation 7 has the advantage of not being subjected to the influence of mobility attenuation or series resistance effect, as it is based on the Y-function method. In contrast, the maximum field-effect mobility μ_{femax} deduced from the maximum g_m, with Equation 8 below, is reliable for long gate lengths only, due to degradation effect by R_{SD} at small gate lengths.

$$\mu_{fe\max} = \frac{g_{m_\max} \cdot L}{W \cdot C_{ox} \cdot V_d} \quad (8)$$

As shown in Figure 7, the extracted μ_0 was close to μ_{femax} for long gate lengths only. They both give evidence of a degradation at higher doping concentration (2×10^{19} cm^{-3}) compared to the value obtained at relatively lower doping concentration (1×10^{19} cm^{-3}), consistently with an increased impurity scattering in more heavily doped channels. Moreover, they both show degradation at short gate length, although the field-effect mobility seems to be affected at much larger gate length. A possible error in our Y function extraction of μ_0 could arise from the fact that the current in JLT devices flows not only through the accumulation channel but also through the neutral channel below. This adds a constant charge of $q \cdot N_d \cdot W \cdot L \cdot t_{si}$ independent on V_{gf}, where t_{si} is the thickness of the silicon film.

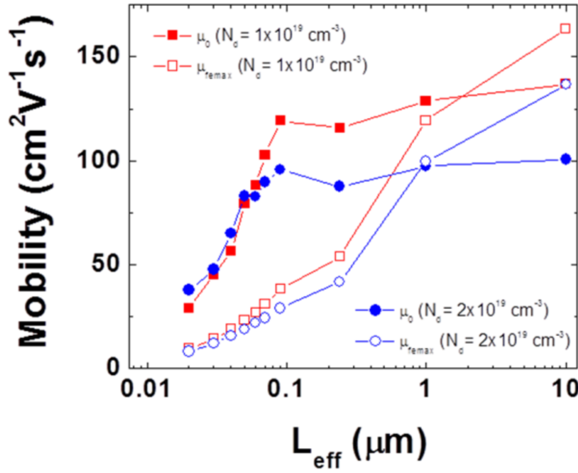

Figure 7. Low field electron mobility (μ_0) and maximum field effect mobility (μ_{femax}) of wide JLT devices (W = 10 µm) as a function of effective gate length (L_{eff}) for two different doping levels (red curve: 1×10^{19} cm^{-3} and blue curve: 2×10^{19} cm^{-3}).

However, using an analytical model of JLT devices in the depletion approximation [4], it can be shown that the error introduced by the constant channel conductance in extracting μ_0 from Y-function slope is at first order equal to $(qN_dt_{si}\theta)/C_{ox}$. In our case, considering a maximum doping level of 2×10^{19} cm^{-3} and a typical value of $\theta \approx 0.1$ V^{-1}, the maximum error on the low field mobility shown in Fig. 7 is about 10%. Therefore, the degradation of the low-field mobility μ_0 extracted from Y-function is well reliable and reflects a physically based degradation of the mobility at small gate length, regardless of channel doping. This feature could be likely associated to process induced defects near source and drain regions as in inversion mode thin film FDSOI devices [9]. Moreover, note that, unlike μ_0, μ_{femax} mobility data are much more degraded at short L, due to strong impact of series resistance, not eliminated in the latter case. Finally, it should be mentioned that the μ_0 values of ≈ 130 $cm^2V^{-1}s^{-1}$ (1×10^{19} cm^{-3}) and ≈ 100 $cm^2V^{-1}s^{-1}$ (2×10^{19} cm^{-3}) which were found here for long channels are comparable to the value of bulk silicon electron mobility reported by C. Jacoboni *et al.* for the same range of doping levels [10].

Drain induced barrier lowering (DIBL)

The DIBL of JLT devices with nanowire like structures (W_M = 80 nm i.e. $W_{eff} \approx 20$ nm) was discussed comparatively to IM devices featuring the same structure. The DIBL parameter λ can be obtained by the normalized sensitivity of the saturation drain current with respect to the gate voltage sensitivity as [11]:

$$\lambda = \left[\frac{d\ln(I_d)}{dV_d} \bigg/ \frac{d\ln(I_d)}{dV_g} \right] = \frac{g_{d_sat}}{I_d} \bigg/ \frac{g_{m_sat}}{I_d} \qquad (9)$$

Where g_{d_sat} and g_{m_sat} mean the saturation output conductance and the saturation transconductance, respectively. Equation 9 allows the DIBL to be determined for all the regions of transistor operation, including subthreshold region, while avoiding the uncertainties related to the extraction of V_{th} [11]. DIBL was extracted from characteristics such as that of Fig. 8(a), which was obtained for L_{eff} = 40 nm.

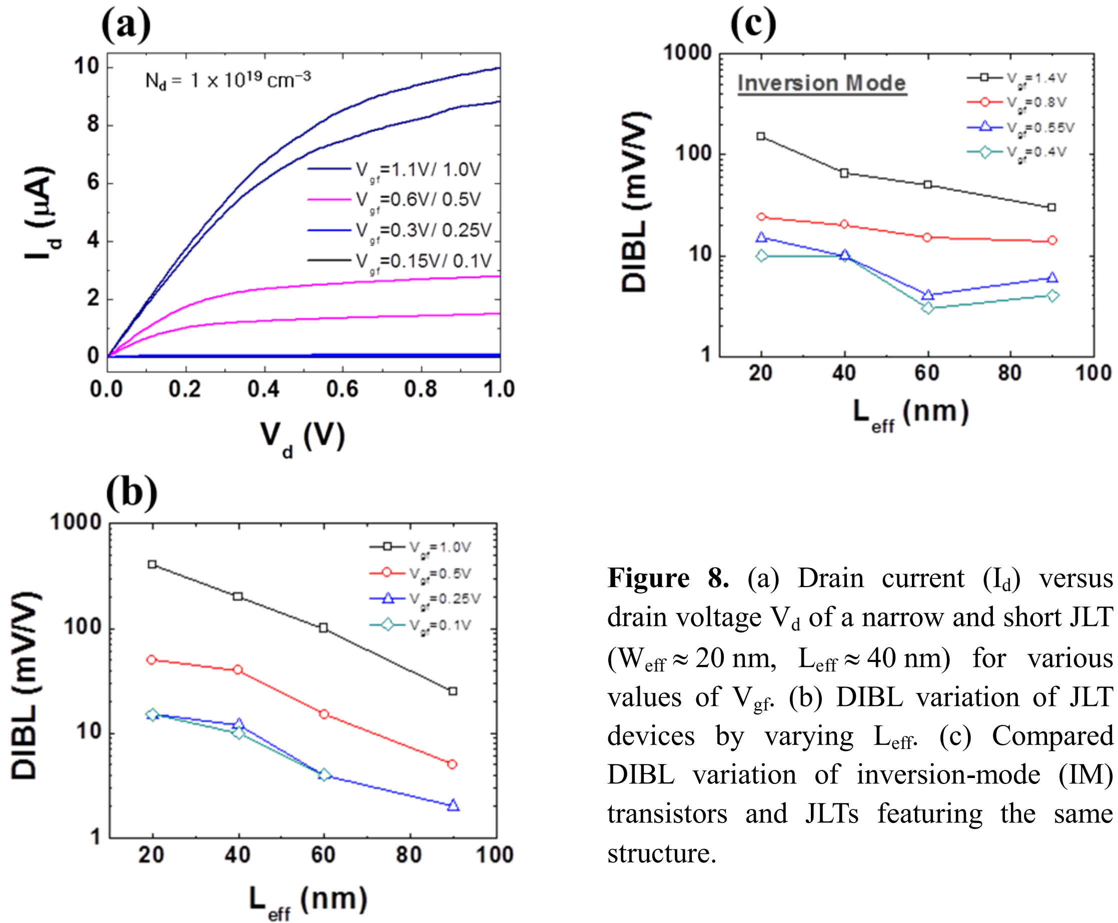

Figure 8. (a) Drain current (I_d) versus drain voltage V_d of a narrow and short JLT ($W_{eff} \approx 20$ nm, $L_{eff} \approx 40$ nm) for various values of V_{gf}. (b) DIBL variation of JLT devices by varying L_{eff}. (c) Compared DIBL variation of inversion-mode (IM) transistors and JLTs featuring the same structure.

It was plotted versus effective lengths in Fig. 8(b) for all regimes of JLT operation, such as near flat-band and accumulation as well as subthreshold regimes. Comparison to the DIBL of IM devices is displayed in Fig. 8(c). Near subthreshold, DIBL was found similar for JLT and IM devices. For long channels, DIBL was slightly smaller for JLTs, but the values were similar at short gate length due to faster degradation for JLTs. The main difference occurred at large V_{gf}. The larger DIBL found for JLT devices at high V_{gf} might be a consequence of the presence of the neutral channel below the accumulation channel. This neutral channel, which is not affected by the gate electric field in the accumulation regime of operation, could result in reduced gate controllability. It is also known that the DIBL of JLT devices is sensitive to channel doping concentrations [4]. However, further studies are needed to fully elucidate this issue.

2.1.3.2 Electrical parameters of JLT devices based on Capacitance-Voltage characteristics

Typical gate-to-channel capacitance (C_{gc}) curves, as shown in lower inset of Fig. 9, were obtained on a long channel JLT device (L = W = 10 µm) when varying substrate bias (V_{gb}) in the range of -30 V to +30 V. The darker lines on the plots in Fig. 9 were obtained with V_{gb} = 0 V. Back-gate biasing affects the carrier and electric field distributions in thin silicon on insulator films. It is a useful biasing scheme to study charge coupling effects, separate front and back interfaces or modulate V_{th} in ultra-thin body fully-depleted (FD) SOI devices [12]. This biasing scheme was implemented here for the JLT.

Threshold and flat-band voltages as a function of back-gating

The C_{gc} values measured at V_{gf} leading to fully depleted channel ($V_{gf} < V_{th}$) were very small, and only limited by a constant parasitic capacitance.

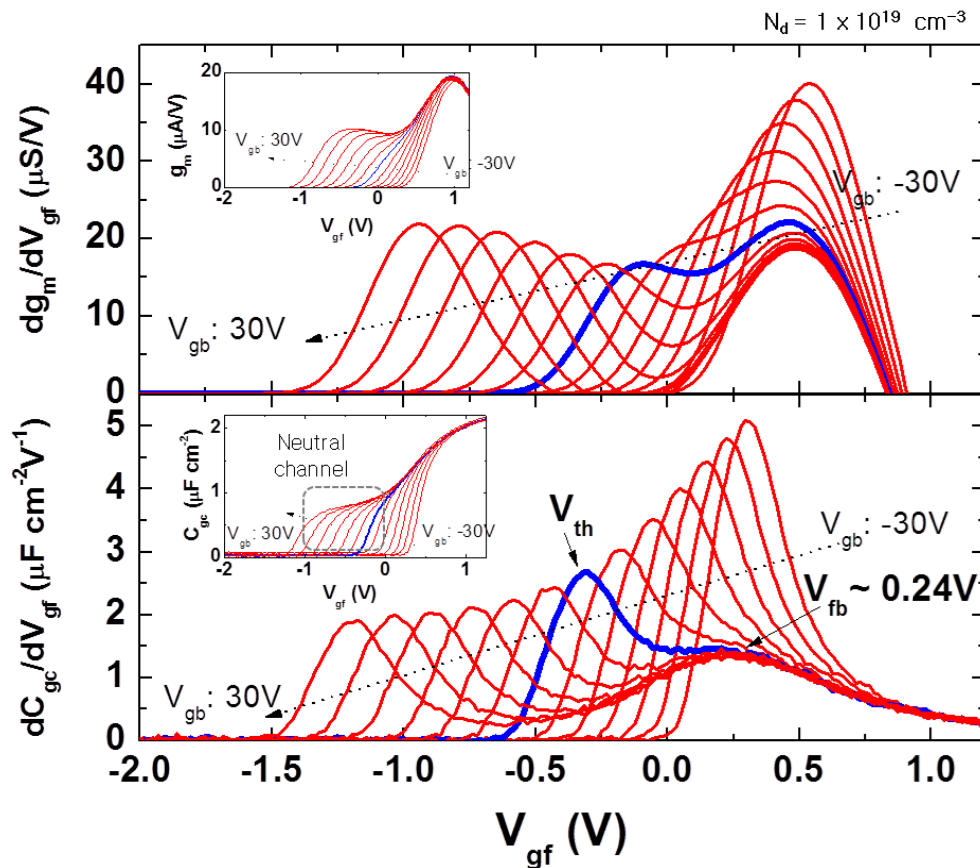

Figure 9. Derivative of g_m (upper) and of C_{gc} (lower) for large JLT devices (W = L = 10 µm) with various values of the substrate bias voltage V_{gb}. The two peaks, in both dg_m/dV_{gf} and dC_{gc}/dV_{gf}, were observed even in the condition of V_{gb} = 0 V (blue curve).

As V_{gf} was increased (above threshold voltage V_{th}), C_{gc} started to increase as a result of the formation of the bulk neutral channel and of the squeezing of the depleted region. This led to a first shoulder on the C_{gc} (V_{gf}) plots, which was indicative of the partially depleted state and was therefore shifted by back-biasing. Another shoulder, independent of back-bias, appeared at flat band. In order to better visualize these features, we calculated the derivative of C_{gc} (dC_{gc}/dV_{gf}) as well as the derivative of the transconductance (dg_m/dV_{gf}). Both are plotted in Fig. 9. The first peak of the dC_{gc}/dV_{gf} plot corresponds to the conduction threshold V_{th}, separating full depletion state from partial depletion regime, while the second peak, independent of V_{gb}, corresponds to the flat-band voltage ($V_{fb} \approx 0.24$ V) where the depletion region in the channel has completely vanished. The mobility degradation and series resistance effects alter the dg_m/dV_{gf}. This explains why there are differences in the peak positions deduced from dC_{gc}/dV_{gf} and dg_m/dV_{gf}, even though the methods are quite similar in principle [12].

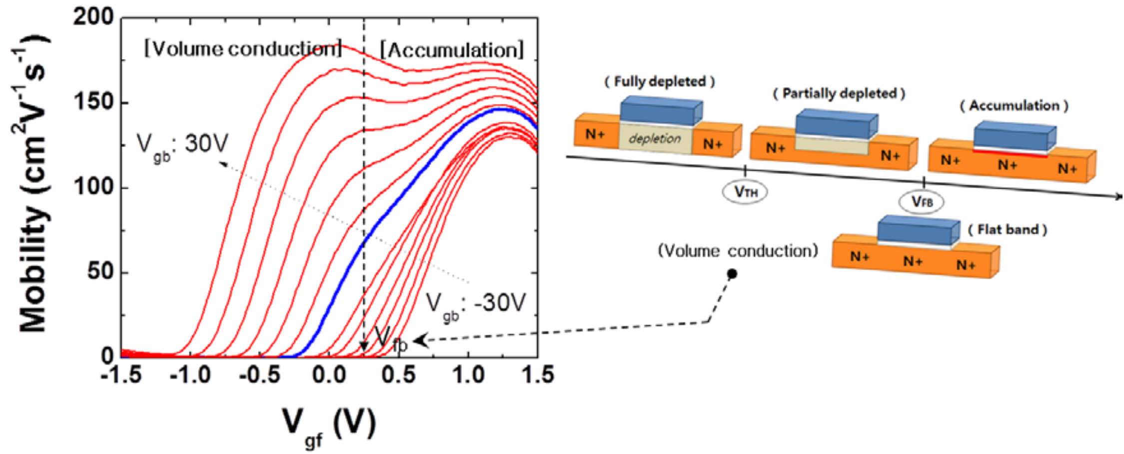

Figure 10. Effective mobility (μ_{eff}) deduced from the results in Fig. 9 versus V_{gf} with V_{gb} ranging from -30 V to +30 V. Extracted μ_{eff} could be distinguished as dominated by bulk conduction or by accumulation, the two regimes being separated by V_{fb}. The schematic view explains the operation modes of JLT devices according to gate voltages.

Gate-voltage dependent split C-V mobility

Figure 10 shows the effective mobility (μ_{eff}) deduced by split C-V method from the results of Fig. 9 using the following equation:

$$\mu_{eff} = \frac{L \cdot I_d(V_{gf})}{q \cdot n_s(V_{gf}) \cdot V_d \cdot W} \qquad (10)$$

where V_d is the applied drain voltage (50 mV) and n_s denotes the sheet density of mobile carriers in the channel, which is deduced by integration of C_{gc}:

$$n_s = \int \frac{C_{gc}(V_{gf})}{q \cdot L \cdot W} dV_{gf} \qquad (11)$$

The μ_{eff} could be distinguished as dominated by volume conduction (left-hand side) or accumulation (right-hand side), with $V_{fb} \approx 0.24$ V separating the two regimes as shown in Fig. 10.

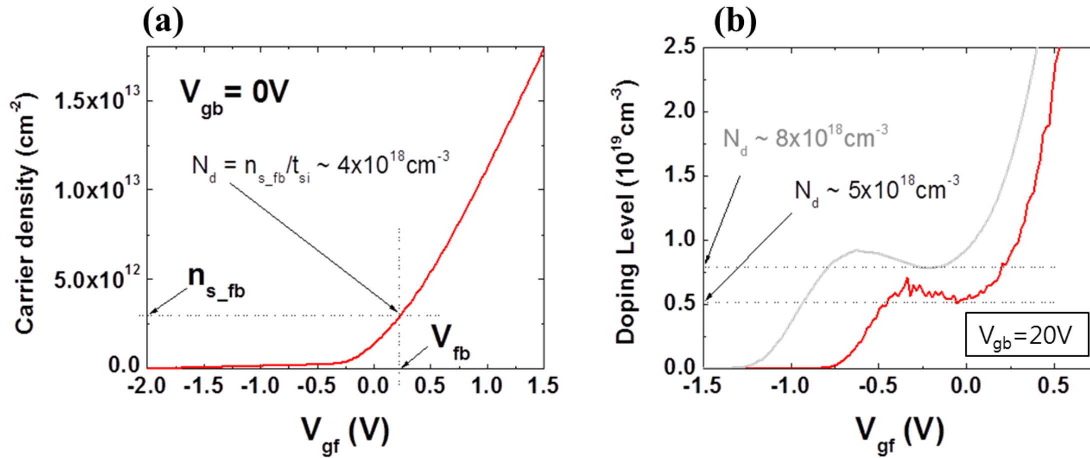

Figure 11. (a) Sheet density of mobile electrons (n_s) according to V_{gf}. n_{s_fb} is the sheet density of mobile carriers at the flat-band voltage estimated from Fig. 9 (≈ 0.24 V). (b) Doping level (N_d) from Maserjian function plotted against V_{gf} for two values of the targeted doping level: 1×10^{19} cm^{-3} (red curve) or twice as much (2×10^{19} cm^{-3}, grey curve). The values of N_d extracted from the plateau of the plots were ≈ 5×10^{18} cm^{-3} and ≈ 8×10^{18} cm^{-3}, respectively.

Doping level

The channel doping concentration can be deduced from sheet carrier density at flat-band. The value of n_s deduced from C_{gc} integration (Eq. 11) was plotted in Fig. 11(a) as a function of V_{gf}, for the condition V_{gb} = 0V. The doping level was determined from mobile carrier density (n_{s_fb}) at the estimated flat-band voltage (≈ 0.24 V) as:

$$n_{s_fb} = N_d \cdot t_{si} \qquad (12)$$

The value of N_d (≈ 4×10^{18} cm^{-3}) which is extracted by this method is lower than the targeted value of 1×10^{19} cm^{-3}. Moreover, this method for calculating channel doping is quite sensitive to the value of

V_{fb}. Another method for doping level extraction is based on the Maserjian function (Y_M) which is written [13, 14]:

$$Y_M = \frac{1}{C_{gc}^3} \cdot \frac{\partial C_{gc}}{\partial V_{gf}} = \frac{1}{C_{sc}^3} \cdot \frac{\partial C_{sc}}{\partial V_s} \quad (13)$$

where C_{sc} and V_s are the semiconductor capacitance and the front surface potential, respectively. The Y_M function is independent of oxide capacitance and depends on substrate characteristics only. Doping concentration N_d can be calculated by equation 14, as in the conventional $1/C^2$ versus V_g plot in the depletion regime, as [13]:

$$N_d = \frac{1}{q \cdot \varepsilon_{si} \cdot Y_M} \quad (14)$$

where ε_{si} refers to silicon permittivity. The value of N_d which is representative of channel doping level was extracted from the plateau in the plot of doping level versus V_{gf}, as shown in Fig. 11(b). The extracted value was $\approx 5\times10^{18}$ cm^{-3}, which is slightly closer to the targeted doping level (1×10^{19} cm^{-3}). Similar extraction provided a $\approx 8\times10^{18}$ cm^{-3} value for N_d for a targeted doping level of 2×10^{19} cm^{-3}, as shown by the grey curve in Fig. 11(b). Finally, it should be emphasized that these extracted doping levels are perfectly consistent with the low field mobility values previously shown in Fig. 7 for long channels and bulk silicon data [10].

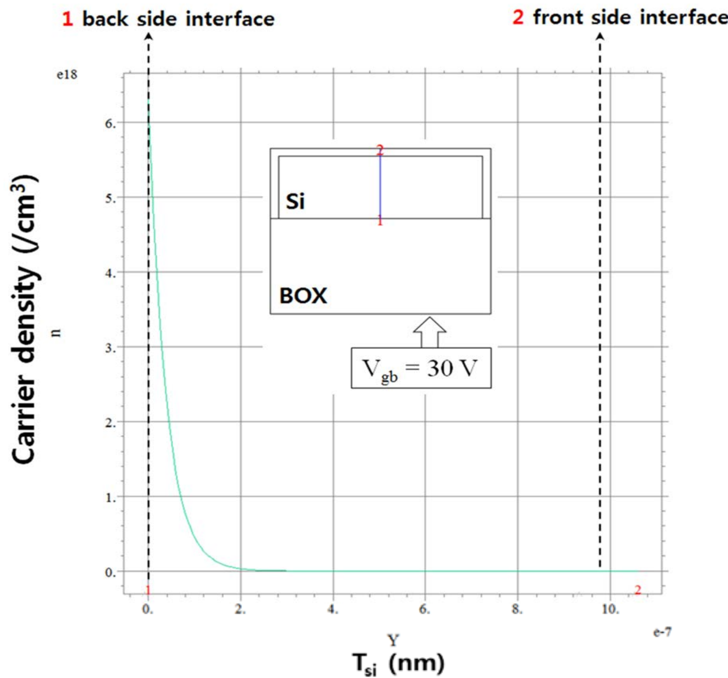

Figure 12. Simulation results showing the carrier concentration at back and front interface of Si channel.

Consideration regarding the accumulation channel at the back-side interface

The applied back gate voltage (V_{gb}) cannot make the accumulation channel due to very thick BOX oxide of 145 nm. The value of electric field from the back gate is too small to make the accumulation channel at the back side interface even at V_{gb} = 30 V, which is different from traditional inversion mode transistor [12]. We confirmed the above fact in JLT devices through the numerical simulation (FlexPDE software) results as shown in Fig. 12. Figure 12 shows the distributions of carrier concentrations at back and front interface, between Si channel and top gate oxide or BOX, with the condition of V_{gb} = 30 V and V_{gf} at first peak point on dC_{gc}/dV_{gf}. We can see that there is the neutral channel (≈ 6×10^{18} /cm^3) at back interface between Si channel and BOX, not the accumulation channel.

2.1.4 Conclusions

Junctionless transistors (JLT) fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick BOX and ≈ 9 nm thick silicon have been extensively characterized. Both nanowire-like geometries with tri-gate structure (W_M = 80 nm) as well as planar structures (W_M = 10 μm) were studied. Their electrical parameters were extracted by Current-Voltage (I-V) and Capacitance-Voltage (C-V) characterization, based on methodologies which were drawn from those used for inversion-mode (IM) transistors. These methodologies were systematically and analytically revisited to account for the specificities of JLT operation. Interestingly, experimental results brought evidence of the unique properties of JLT devices, such as the observation of two slopes in the Y-function and of two peaks in the dg_m/dV_{gf} and dC_{gc}/dV_{gf} plots, each of them being associated to the neutral and accumulation channel, respectively. We extracted a broad range of electrical parameters such as conduction threshold (V_{th}), flat-band voltage (V_{fb}), drain induced barrier lowering (DIBL), low field mobility (μ_0) and doping concentrations (N_d). Their variation with gate length, doping level and back-gating was discussed, and a comparison with inversion mode transistors carried out.

2.2 Effects of channel width variation on electrical characteristics of tri-gate junctionless transistors

2.2.1 Introduction

Junctionless transistors (JLT) is considered as a possible candidate for the realization of sub 22 nm CMOS devices, owing to their promising advantages such as quite simple device structures without PN junction and the bulk conduction based operation principle [1-3, 15]. Recently, most of attention has been focused on JLT devices with a nanowire structure so far, which exhibits better immunity against short channel effects (SCE). However, JLT devices with a planar structure show more clearly their unique intrinsic properties than nanowire like JLT devices [16]. For instance, the conduction threshold (V_{th}) and flat-band voltage (V_{fb}), which are key parameters in JLT devices operation, were clearly revealed through the derivative of gate to channel capacitance (dC_{gc}/dV_g) in wide planar JLT devices only. Therefore, the electrical properties of JLT devices depending on width variation, from planar to nanowire like structure, can provide helpful information for their practical applications as well as for a better understanding of JLT devices with a nanowire structure.

In this chapter, the electrical characteristics of tri-gate JLT devices with various widths were investigated in terms of V_{th}, V_{fb} and effective mobility (μ_{eff}) data analyses. The overall electrical behavior of tri-gate JLT devices with very narrow structure (top-effective width $W_{top_eff} \approx 25$ nm) was strongly affected by the sidewall gate effect. In addition, the experimental results related to the sidewall gate effect were confirmed by two-dimensional (2D) numerical simulations.

2.2.2 Device fabrication and experiment

For this study, N-type tri-gate JLT devices were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) [17]. After thinning Si body down to ≈ 9.4 nm, a full-sheet implantation was carried out before active patterning with a phosphorus doping targeted at 1×10^{19} cm^{-3} and the effective doping concentration extracted from Maserjian's function (Y_M) was ≈ 0.5×10^{19} cm^{-3} [16]. The high-k gate stack is composed of HfSiON/ TiN/ Polysilicon, with an equivalent oxide thickness of 1.2 nm. Figure 13(a) displays the schematic architecture of the tri-gate JLT devices as well as the transmission electron microscopy (TEM) cross-section of a narrow device, showing well defined gate stack. On-mask gate width W_M was ranging from 1μm down to 100 nm and the top channel width difference ΔW_{top} as defined in Fig. 13(b), which amounted to ≈ 75 nm, was obtained by the linear relationship between C_{gc} and W_M at strong accumulation operation regime of the tri-gate JLT devices [6, 16]. For a better accuracy of the C_{gc} values, the tri-gate JLT devices with very long gate length (L = 10 μm) were selected, in arrays of 50 channels.

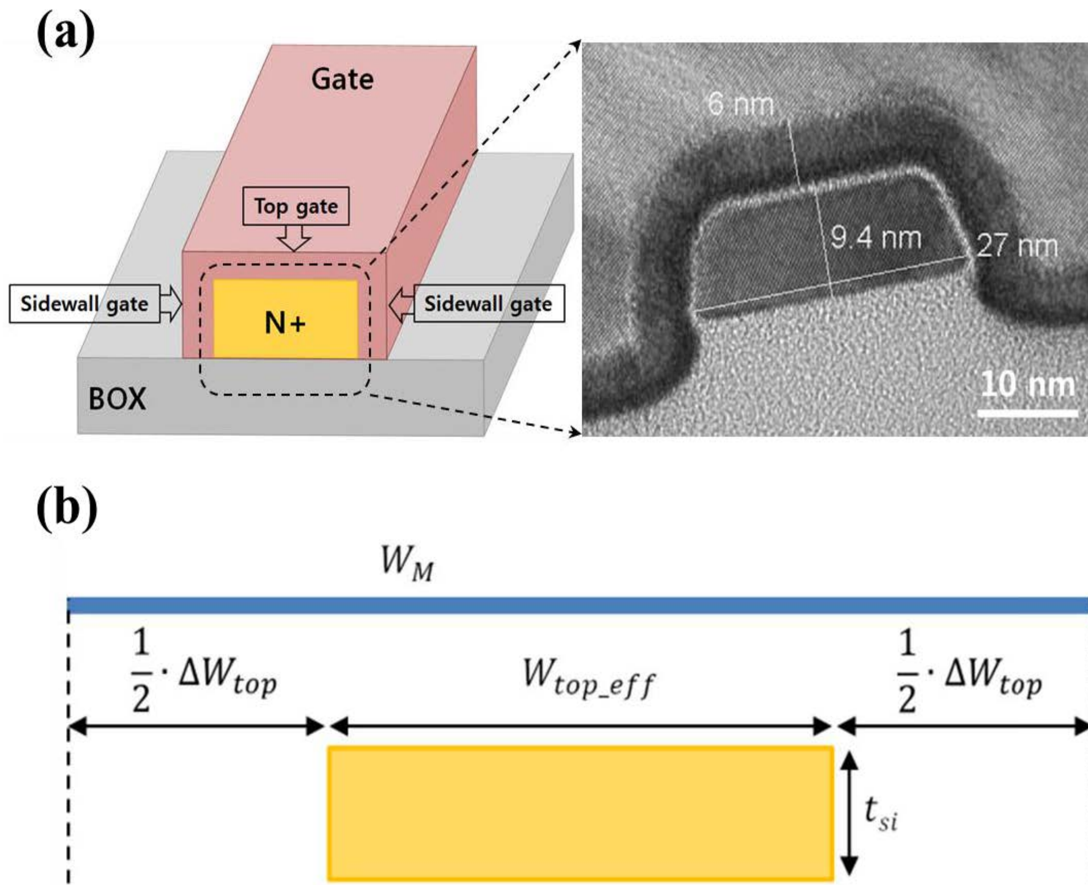

Figure 13. Schematic architecture of the tri-gate JLT devices (left) and transmission electron microscopy (TEM) cross-section (right) showing well defined gate stack with thinned Si body. (b) Illustration explaining the defined W_M, W_{top_eff} and ΔW_{top}.

The capacitance-voltage measurements C-V were recorded using an HP4294a with a 50 mV small signal at 500 kHz and the current-voltage I-V characteristics were taken out using HP4155a measurement unit. Besides, FlexPDE 5.0 software based on the finite element method was used for 2D Poisson equation numerical simulations.

2.2.3 Experimental results and discussion

2.2.3.1 Experimental results

Gate-to-channel capacitance (C_{gc}) curves versus gate voltage V_g normalized by maximum C_{gc} values were obtained on the tri-gate JLT devices with various top-effective widths (W_{top_eff}) as shown in Fig. 14(a).

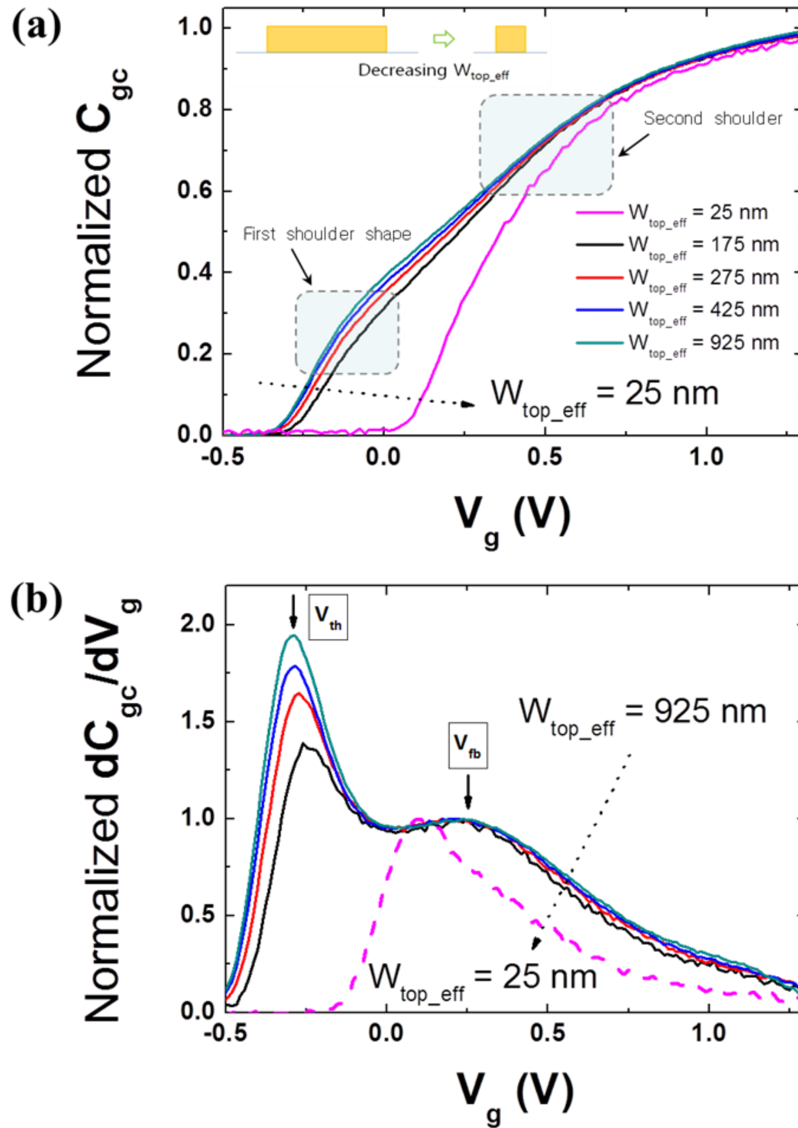

Figure 14. (a) Normalized C_{gc} as a function of V_g with varying W_{top_eff} and (b) corresponding dC_{gc}/dV_g normalized by its second peak (right-hand side) values.

As V_g is increased, the normalized C_{gc} starts to increase as a result of the formation of the bulk neutral channel in the initially fully-depleted channel. This allows that a first shoulder (left-hand side) appeared on the normalized C_{gc} plots, which indicates the partially depleted state. On the other hand, another shoulder (right-hand side) on the normalized C_{gc} corresponds to the border between partial depletion and accumulation mode of tri-gate JLT devices. Interestingly, the first shoulder shape was shrinking as decreasing W_{top_eff} and completely vanished in the tri-gate JLT device with W_{top_eff} = 25 nm. As decreasing W_{top_eff}, the amount of bulk neutral channel in the tri-gate JLT devices is relatively getting smaller as compared to that of surface accumulation channel. Accordingly, the reduced portion of neutral channel as regard to the accumulation channel in the narrow structure makes the first shoul-

der shrinking on the normalized $C_{gc}(V_g)$ curves.

Figure 14(b) shows the derivative of C_{gc} (dC_{gc}/dV_g) normalized by its second peak (right-hand side) values. The first peak of the normalized dC_{gc}/dV_g plot corresponds to the conduction threshold voltage V_{th} and the second peak denotes the flat-band voltage V_{fb} [16]. As decreasing W_{top_eff}, the height of the first peak is getting smaller due to the reduced influence of the bulk neutral channel with respect to the surface accumulation channel. In addition, it should be noted that V_{th} (first peak position) was increased as decreasing W_{top_eff}, while V_{fb} position doesn't change. For wide top-effective widths, the electrical behavior of tri-gate JLT device shows a planar behavior because the JLT device is mainly controlled by the top gate. Whereas, for narrow top-effective widths, the sidewall gate as well as the top gate mainly control the overall potential distribution in the channel of the JLT devices. In the case of partial depletion operation, the sidewall gate effect through the depletion region strongly affects the formation of the bulk neutral channel and causes a tri-gate behavior. That is the reason why V_{th} was changed as reducing W_{top_eff}. In particular, only a single peak (dotted curve) as shown in Fig. 14(b) was observed in the JLT device with the shortest W_{top_eff} = 25 nm. This feature shows that the sidewall gate effect is very strong in such a very narrow structure. This is in agreement with Choi *et al.* results, who reported the rise of V_{th} as reducing the width in gate-all-around (GAA) JLT devices. They also demonstrated the fact that the width dependent V_{th} variation in JLT devices was much larger than that in inversion-mode (IM) transistors [18].

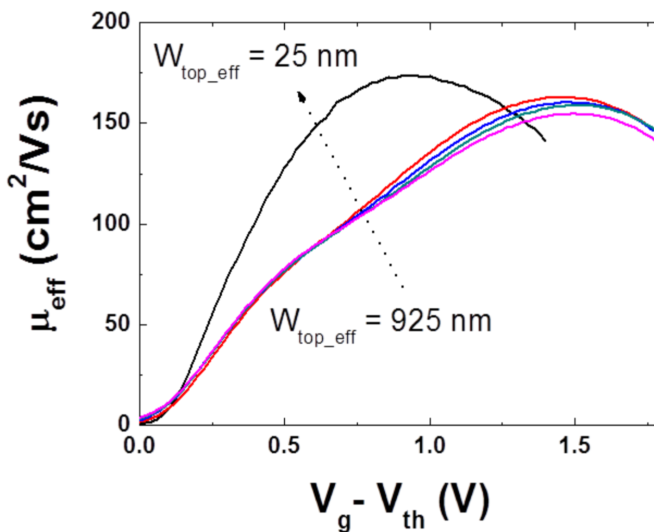

Figure 15. μ_{eff} as a function of gate voltage overdrive (V_g-V_{th}) with varying W_{top_eff}. In order to obtain drain current (I_d), the devices are biased in the linear regime of operation with V_d = 50 mV.

Figure 15 shows the effective mobility (μ_{eff}) as a function of the gate voltage overdrive (V_g-V_{th}), deduced by using the following equation:

$$\mu_{eff} = \frac{L^2 \cdot I_d}{Q \cdot V_d} \quad (1)$$

where Q is the mobile channel charge derived from integration of C_{gc} vs V_g and V_d is the applied drain voltage (here 50 mV). The trend of μ_{eff} in very narrow JLT device (W_{top_eff} = 25 nm) is highly deviated from those in wide JLT devices. The sidewall gate effect in a narrow structure makes the different mobile charge distribution comparable to that in a wide structure. As a result, the change in the distribution of mobile charges in narrow width devices induced a μ_{eff} deviation as compared to wide JLT devices.

2.2.3.2 2D numerical simulation results of the sidewall gate effect

2D numerical simulations of the Poisson equation was carried out for confirming the strong sidewall gate effect causing a tri-gate behavior in tri-gate JLT devices with a narrow W_{top_eff}. The trend of the normalized $C_{gc}(V_g)$ and $dC_{gc}/dV_g(V_g)$ as shown in Fig. 16 was quite consistent to that in previous experimental results reported in Fig. 14.

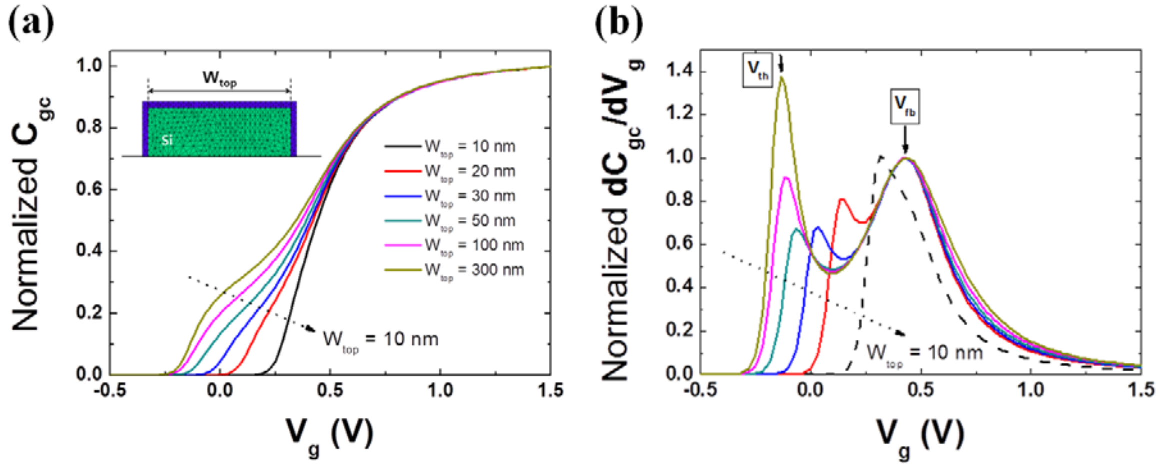

Figure 16. Same plots as in Fig. 14: (a) normalized C_{gc} with various W_{top} and (b) corresponding dC_{gc}/dV_g normalized by its second peak (V_{fb}) in the simulated tri-gate JLT devices.

As decreasing W_{top} from 300 nm to 10 nm, the shrinkage of the first shoulder, which is related to bulk neutral channel in the partial depletion mode, is clearly observed as shown in Fig. 16(a). In addition, the second peak (V_{fb}) in Fig. 16(b) is keeping constant, while the position and height of the first peak (V_{th}) is also increasing and getting smaller, respectively. Interestingly, the first peak point is going toward the second peak in the true tri-gate structures (from W_{top} = 30 nm). Finally, the JLT device with a very narrow structure of W_{top} = 10 nm shows only a single peak on the normalized $dC_{gc}/dV_g(V_g)$ (dot-

ted curve) in Fig. 16(b), owing to the strong sidewall gate effect in that structure.

The V_{th} extracted from the first peak in Fig. 16(b) was plotted as a function of W_{top} (black curve) as shown in Fig. 17(a). For relatively large widths, the V_{th} was slightly increasing as decreasing W_{top}. However, below W_{top} = 50 nm, it was dramatically raised. This result means that the sidewall gate effect starts manifesting strongly in that regime.

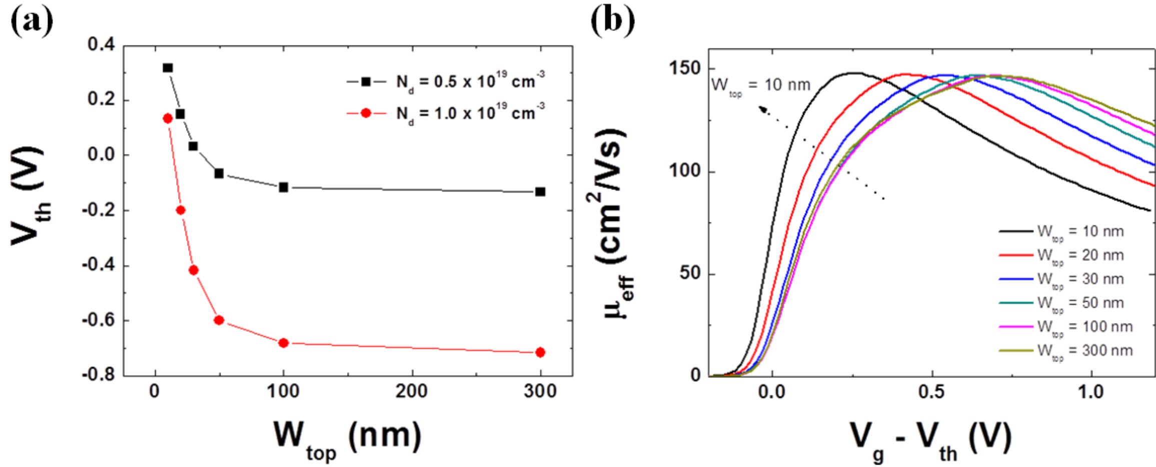

Figure 17. (a) Calculated V_{th} as a function of W_{top}. (b) μ_{eff} as a function of gate voltage overdrive (V_g-V_{th}) in the simulated tri-gate JLT devices.

In addition, as increasing doping concentration, the V_{th} at the same W_{top} is reduced and its variation by changing W_{top} is much increased as shown in red curve of Fig. 17(a). The μ_{eff} behavior depending on W_{top} variation as shown in Fig. 17(b) was also similar to that of experimental results reported in Fig. 15. For instance, in the case of W_{top} = 10 nm, the μ_{eff} curve as shown in Fig. 17(b) is noticeably deviated from the others, because the sidewall gate effect is very strong in this structure. It should be mentioned that, for the calculation of μ_{eff} in the simulation, a universal relationship between the effective channel mobility and the transverse electrical field was used as [19, 20]:

$$\mu_{eff} = \frac{\mu_0}{1+\left(\frac{E_{eff}}{E_c}\right)^{\alpha}} \qquad (2)$$

where μ_0, E_{eff}, E_c and α represent low-field mobility, effective transverse electrical field, critical electric field and exponent for mobility attenuation, respectively.

In order to clarify the sidewall gate effect in tri-gate JLT devices, the potential distribution, along the arrow line across the center of Si body in the inset of Fig. 18(a), has been calculated for various W_{top} as shown in Fig. 18. Fig. 18(b) shows the potential distribution in the partially depleted state (V_g <

V_{fb}) of tri-gate JLT devices. For large widths, the potential distribution across the channel is mainly governed by the V_g applied from the top gate only. However, as decreasing the width, the influence from the sidewall gate is strengthened as much as that from the top gate.

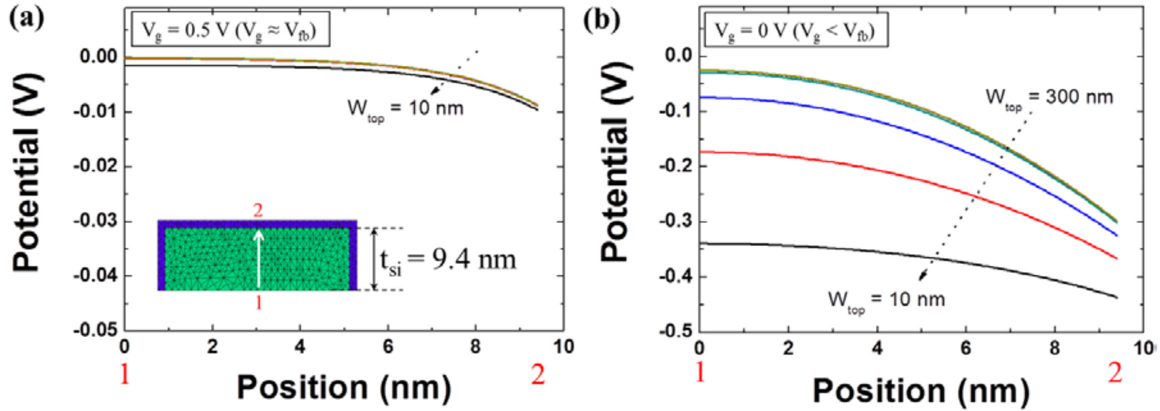

Figure 18. Calculated potential distribution along the arrow line (1 → 2 in inset) in the tri-gate JLT devices with varying W_{top}: (a) at around flat-band condition (V_g = 0.5V) and (b) at the partially depleted state (V_g = 0V).

Therefore, for narrow structures (W_{top} < 50 nm), the large variations on the potential distribution was observed as shown in Fig. 18(b), while the potential distribution behavior for wide devices showed almost the same trend regardless of varying W_{top}. On the other hand, when the applied V_g is around V_{fb}, there were no significant differences with respect to W_{top} variation (for both narrow and wide widths) on the potential distribution in Fig. 18(a). This explains why the second peak (V_{fb}) on the normalized $dC_{gc}/dV_g(V_g)$ doesn't shift in Fig. 14(b) and Fig. 16(b), even though the first peak (V_{th}) is increasing as reducing W_{top_eff} or W_{top}.

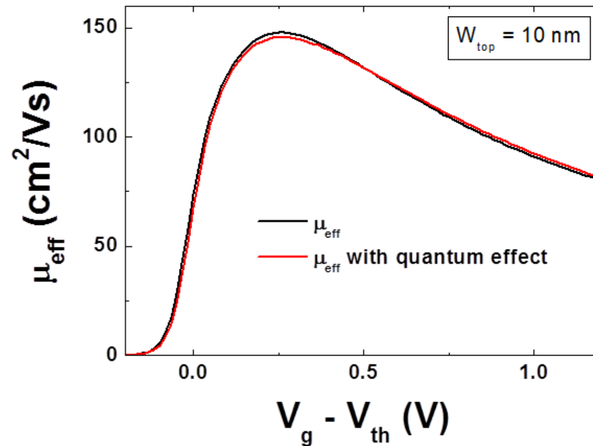

Figure 19. The effective mobility behavior considered with quantum effects and its comparison to classical method.

Actually quantum effects were taken into account using the Hansch approximation for the carrier profile. In this study, we couldn't find significant difference between classical and quantum results as can be seen from the plots with W_{top} = 10 nm device (Fig. 19). Note also that multi-gate FETs are significantly affected by quantum effects when their thickness and width reach values that are less than 10 nanometers [21].

2.2.4 Conclusions

The width dependent electrical behavior of tri-gate Junctionless transistors (JLT) was investigated, experimentally. As decreasing the top-effective width (W_{top_eff}), the first shoulder on the normalized gate-to-channel capacitance characteristics $C_{gc}(V_g)$ was shrunk and the first peak on the normalized $dC_{gc}/dV_g(V_g)$ related to threshold voltage (V_{th}) was lowered in amplitude and its position was up-shifted, while the flat-band voltage (V_{fb}) location doesn't change. This is because the amount of bulk neutral channel in tri-gate JLT devices with a narrow structure is getting smaller as compared to the contributions of surface accumulation channels and the sidewall gate effect also strengthens. Moreover, the trend of the effective mobility (μ_{eff}) in very narrow JLT devices (W_{top_eff} = 25 nm) was found noticeably different from those in wide JLT devices, due to the strong sidewall gate effect. Finally, the sidewall gate effect was also proved through 2D Poisson equation numerical simulations, which were quite consistent to the experimental results.

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Chapter 3

Low-temperature electrical characterization of junctionless transistors

The electrical performance of Junctionless transistors (JLT) with planar structures was investigated under low-temperature and compared to that of the traditional inversion-mode (IM) transistors. The low-field mobility (μ_0) of JLT devices was found to be limited by phonon and neutral defects scattering mechanisms for long gate lengths, whereas scattering by charged and neutral defects mostly dominated for short gate lengths, likely due to the defects induced by the source/drain (S/D) implantation added in the process. Moreover, the temperature dependence of flat-band voltage (V_{fb}), threshold voltage (V_{th}) and subthreshold swing (S) of JLT devices was also discussed.

3.1 Introduction

Junctionless transistors (JLT) are currently in the spotlight, owing to the advantages which are expected from their simple structure, without PN junctions, and from their operation principle, based on bulk conduction instead of surface conduction for the standard inversion-mode (IM) MOSFET [1]. For example, JLT devices are known as more robust than IM transistors in terms of effective gate length variability and mobility degradation by transverse electric field. However, JLT devices are fac-

ing some issues such as mobility degradation by their high channel doping, reduced gate controllability due to partial depletion regions, and threshold voltage variability induced by fluctuation of silicon thickness and doping atoms spatial distribution. Many specific electrical properties of JLT devices have been investigated, so far mainly at room temperature [1-4]. In particular, JLT devices with planar structures recently revealed very interesting features, including two peaks in the plots of transconductance derivative, which distinguish the (bulk) neutral and (surface) accumulation channels [5]. Only few papers have dealt with low temperature operation, concentrating mainly on the identification of conductance oscillations in nanowire JLTs [6], and on temperature dependence of the threshold voltage of such narrow structures [7]. More generally, low-temperature characterization allows for a better understanding of physical operation and electrical performance of electronic devices [8, 9]. Extraction of the electrical parameters of JLT devices in the low-temperature range is a powerful tool to get deeper insight into their operation mechanism and more quantitative information about their performance.

This chapter deals with JLT devices with a planar structure ($W = 10\ \mu m$) fabricated from silic on on insulator (SOI) wafers with a silicon thickness t_{si} of 9.4 nm. The electrical parameters of JLT devices were extracted at low-temperature and compared to those of IM transistors fab ricated by the same process including an additional implantation on source and drain (S/D) regions, except for channel doping concentration. The electrical performances of JLT devices, including scattering mechanisms and short channel effects, are discussed based on an analysis of temper ature dependence of low-field mobility, threshold voltage, flat-band voltage and subthreshold s wing.

3.2 Device fabrication and experiment

This study was based on N-type JLT devices with high-k/ metal gate stack, fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) and a Si body thinned down to 9.4 nm. A full-sheet implantation was performed before active patterning with a phosphorus doping targeted at $1\times10^{19}\ cm^{-3}$ or $2\times10^{19}\ cm^{-3}$. The gate is composed of HfSiON/ TiN/ Polysilicon, with an equivalent oxide thickness of 1.2 nm. An additional implantation was performed to S/D regions with the aim of improving electrical performance by reducing access resistance. The S/D implantation process (doping level $\approx 10^{20}\ cm^{-3}$) is exactly same with that of IM transistors. Figure 1 displays the schematic architecture of the fabricated JLT devices, as well as a transmission electron microscopy (TEM) cross-section showing well defined gate stack on the thinned Si channel. On-mask gate length L_M ranged from 1 μm down to 30 nm and on-mask gate width W_M was 10 μm.

The I-V current-voltage characteristics were recorded using an HP4156b measurement unit, wh

ile temperature was varied from 80 K to 350 K. The channel length difference ΔL between ef fective and on mask channel lengths, which amounted to 10 nm, was obtained by the transfer length method (TLM) [10].

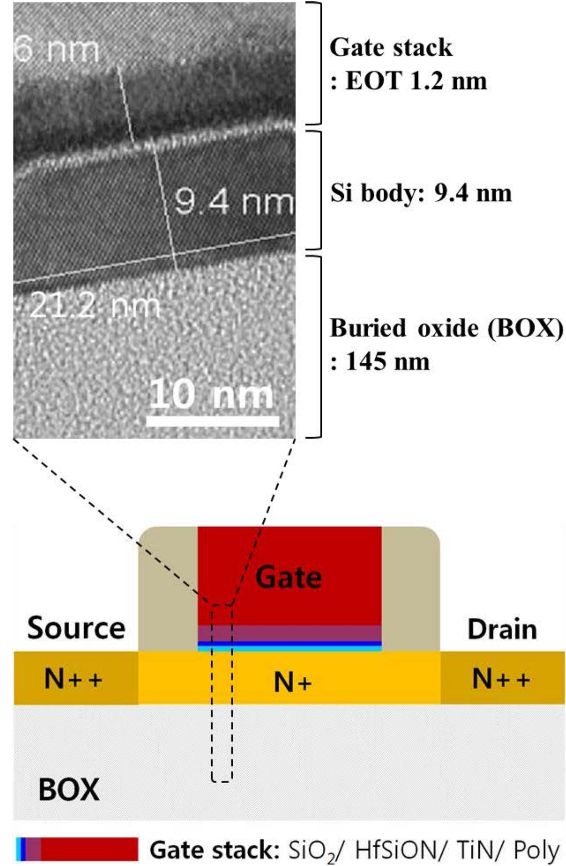

Figure 1. Schematic architecture of the fabricated JLT devices (lower) and transmission electron microscopy (TEM) cross-section showing well defined gate stack with thinned Si body (upper). An HfSiON/ TiN/ Polysilicon gate stack (EOT = 1.2 nm) was used and an additional source/drain (S/D) implantation was performed to reduce S/D access resistance.

3.3 Experimental results and discussion

3.3.1 I-V characteristics at low-temperature

Drain current (I_d) of JLT devices for short and long gate lengths (i. e. effective length L_{eff} = 20 nm, and L = 1 μm, respectively) was measured as a function of gate voltage (V_g), with temperature varying in the range of 80 K to 350 K (Figs. 2(a) and 2(c)). The common intersection point, the so called zero-temperature coefficient (ZTC) point [11], where I_d does not depend on temperature due to the compensated temperature effects of mobility and conduction threshold voltage (V_{th}), was found only for long gate lengths (Fig. 2(c)). This feature is explained from the fact that V_{th} and carrier mobility were both increased at decreasing temperature for long gate length, while they varied in opposite directions (increased and decreased, respectively) at decreasing temperature for short gate length. In contrast, for IM transistors featuring the same structure as JLT devices (Figs. 3(a) and 3(c)), the ZTC

was found for both short and long gate lengths, consistently with an increase of V_{th} and carrier mobility at low temperature, whatever the gate length.

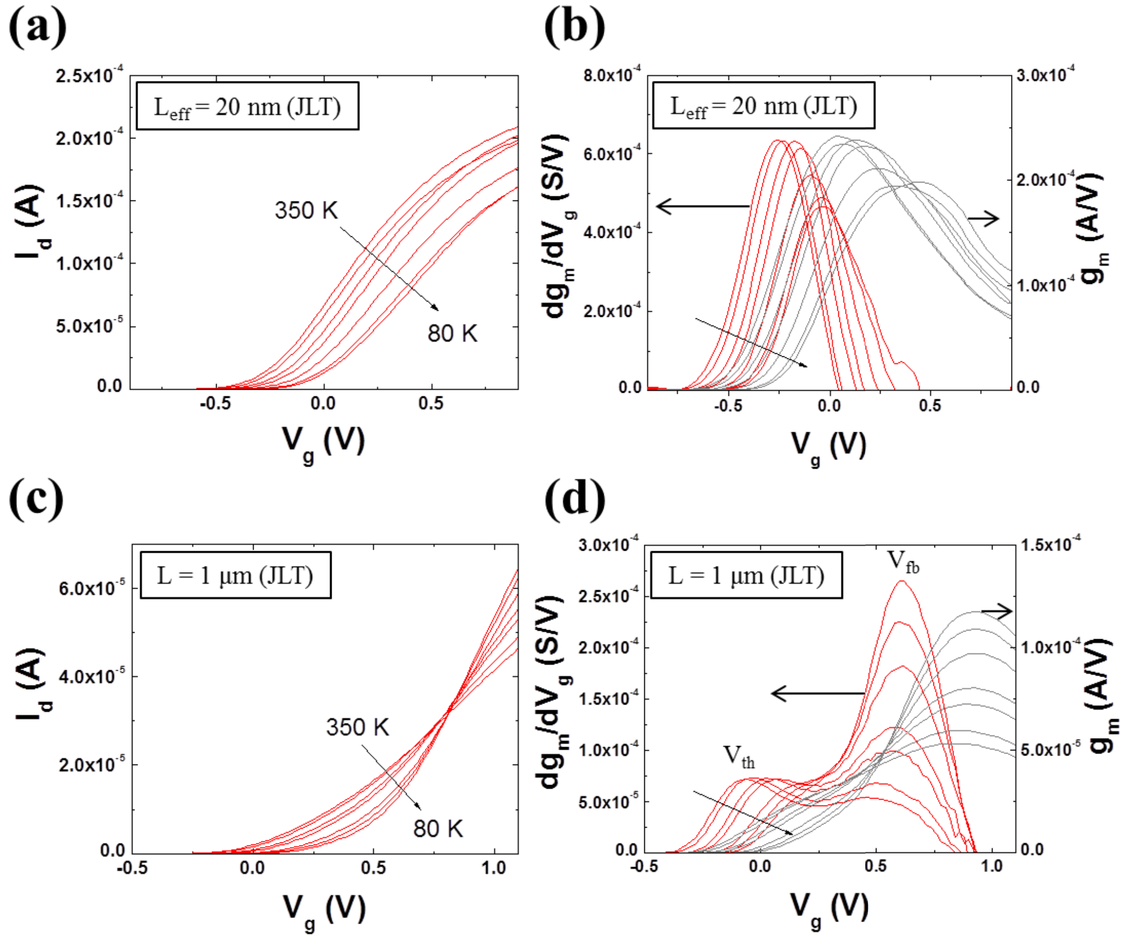

Figure 2. Drain current I_d of JLT devices measured as a function of V_g with temperature varying in the range of 80 K to 350 K, together with the corresponding transconductance g_m (gray) and derivative of transconductance dg_m/dV_g (red). Gate width is W = 10 µm and targeted doping level $N_d = 10^{19}$ cm^{-3}. Devices are biased in the linear regime of operation with V_d = 20 mV.

For JLT devices, the corresponding transconductance (g_m) and transconductance derivative (dg_m/dV_g) were plotted in Figs. 2(b) and 2(d), respectively. Two peaks were observed on the dg_m/dV_g plots (red curve), but for long gate length only (Fig. 2(d)), owing to reduced mobility degradation and series resistance effects as compared to short gate length. The existence of these two peaks in long JLTs is a clear difference with IM transistors [5], which normally show one single peak regardless of gate length as confirmed in Figs. 3(b) and 3(d). As already discussed in a previous paper [5], the first peak (left-hand side peak) in Fig. 2(d) is representative of V_{th}, which corresponds to the turning point from full to partial depletion in the channel, whereas the second peak (right-hand side peak) gives the flat-

band (V_{fb}) position, separating bulk neutral channel from surface accumulation. Interestingly, dg_m/dV_g plots in Fig. 2(d) clearly show that the V_{fb} and V_{th} of JLT devices were increased at decreasing temperature. The V_{th} of IM transistors, derived from the peak points in dg_m/dV_g plots as shown in Figs. 3(b) and 3(d), was also increased at low temperature.

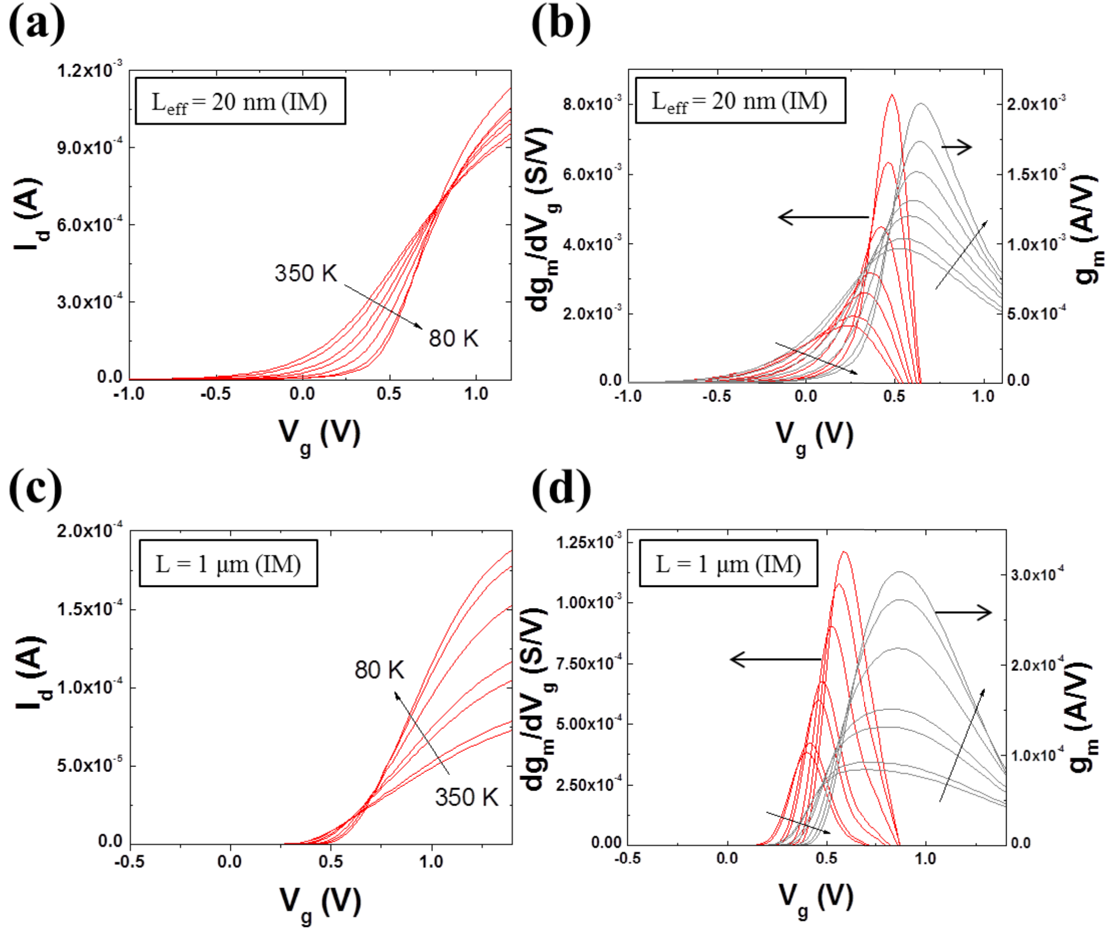

Figure 3. Same plots as in Figure 2 for IM transistors featuring exactly the same structures as JLT devices. Devices are biased in the linear regime of operation with V_d = 20 mV.

3.3.2 Temperature dependences of threshold and flat-band voltage

The temperature dependence of V_{fb} and V_{th} is displayed in Fig. 4(a) for JLT devices with a long gate (L = 1 µm). The positions of the first and second peaks in the dg_m/dV_g plots (Fig. 2 (d)) were selected for the determination of V_{th} and V_{fb}, respectively. It is known that the V_{th} of JLT devices can be derived from the depletion approximation or the charge-based analytical model according to the following equation, valid for wide structures [4, 12]:

$$V_{th} = V_{fb} - \frac{q \cdot N_d \cdot t_{si}^2}{2\varepsilon_{si}} - \frac{q \cdot N_d \cdot t_{si}}{C_{ox}} \qquad (1)$$

where q, N_d, ε_{si} and C_{ox} denote electronic charge, doping concentration in the channel, silicon permittivity and gate oxide capacitance per unit area, respectively. From Equation 1, threshold voltage variation with temperature (dV_{th}/dT) should be equal to the flat-band voltage variation (dV_{fb}/dT), because the V_{th} term in equation 1 contains temperature independent parameters only, except for V_{fb}. This explains why there was no significant difference between the variations of V_{th} and V_{fb} with temperature in Fig. 4(a).

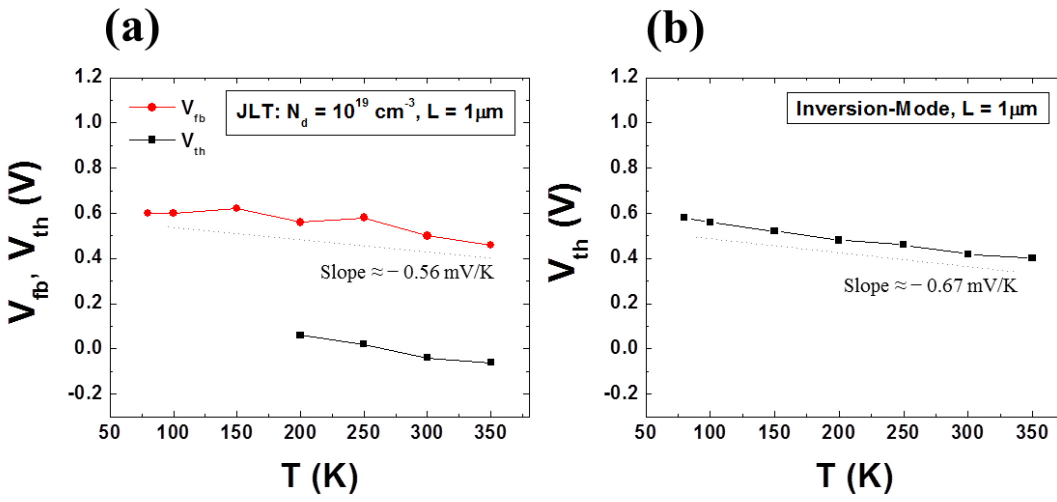

Figure 4. (a) Temperature dependences of V_{fb} and V_{th} of JLT device with L = 1 μm. The V_{th} and V_{fb} were extracted from the positions of the first and second peaks in the dg_m/dV_g plots as shown in Fig. 2(d). (b) Temperature dependent V_{th} of IM transistor with L = 1 μm, which was obtained from the peak points of dg_m/dV_g plots in Fig. 3 (d).

In addition, the V_{fb} and dV_{fb}/dT of JLT devices can be written as an explicit function of temperature, as:

$$V_{fb} = \Phi_{MS} = \Phi_M - \left[\chi + \frac{E_g}{2} - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_d}{n_i} \right) \right] \qquad (2)$$

$$\frac{dV_{fb}}{dT} = \frac{dV_{th}}{dT} = \frac{k}{q} \cdot \ln\left(\frac{N_d}{n_i} \right) - \frac{k \cdot T}{q} \cdot \frac{1}{n_i} \cdot \frac{dn_i}{dT} \qquad (3)$$

where Φ_M, χ, k and n_i denote metal work function, electron affinity, Boltzmann constant and intrinsic carrier density, respectively. The n_i is also affected by temperature according to following relationship [13]:

$$n_i \approx n_{i0} \cdot T^{\frac{3}{2}} \cdot e^{-\frac{E_g}{2kT}} \qquad (4)$$

where E_g is the energy band-gap and n_{i0} is around 3.9×10^{16} cm^{-3} in silicon. The dV_{fb}/dT value of ≈ -0.56 mV/K which was extracted from Fig. 4 (a) is comparable to the one, of ≈ -0.25 to -0.40 mV/K, which was calculated based on equations 1-4.

On the other hand, the V_{th} of undoped fully depleted (FD) SOI transistors with a thick BOX can be obtained in first approximation by [14]:

$$V_{th} = \Phi_{Mi} + \frac{kT}{q}\ln\left[\frac{C_{ox}\cdot kT/q}{q\cdot n_i \cdot t_{si}}\right] \qquad (5)$$

where Φ_{Mi} represents the work-function difference between metal gate and intrinsic silicon. In our case, the value of Φ_{Mi} was assumed to be close to zero, because the gate metal used was featuring a work function close to mid-gap. The dV_{th}/dT (≈ -0.52 to -0.59 mV/K) of IM transistor, estimated using equations 4 and 5, was quite consistent with the value of ≈ -0.67 mV/K extracted from experimental results in Fig. 4 (b), as obtained from the selected peaks in dg_m/dV_g plots (in Fig. 3 (d)).

3.3.3 Temperature dependences of mobility and scattering mechanisms

The temperature dependence of low-field mobility (μ_0) is shown in Fig. 5 for both JLT devices and IM transistors with various channel lengths. The μ_0 was extracted from a Y-function based method, which is not affected by the mobility degradation and series resistance effects, defined as [15]:

$$\left(\frac{dY}{dV_g}\right)^2 = \frac{W}{L}\cdot C_{ox}\cdot \mu_0 \cdot V_d \qquad (6)$$

where Y is equal to $I_d/(g_m)^{1/2}$. For long gate lengths, regardless of device types, the low field mobility tends to increase with decreasing temperature, following a very general behavior resulting from acoustic phonon-dominated scattering. However, the increase rate of μ_0 as temperature decreases ($|d\mu_0/dT|$) was smaller for JLT devices than for IM transistors. This attenuated sensitivity to temperature was attributed to the increased weight of impurity scattering in the JLT devices, which featured heavily doped channels, in comparison with lightly doped IM transistors. The role of impurity scatter-

ing is further confirmed by the fact that heavily doped channels ($N_d = 2\times10^{19}$ cm^{-3}) lead to a reduced rate of $|d\mu_0/dT|$, as can be seen in Figure 5(b).

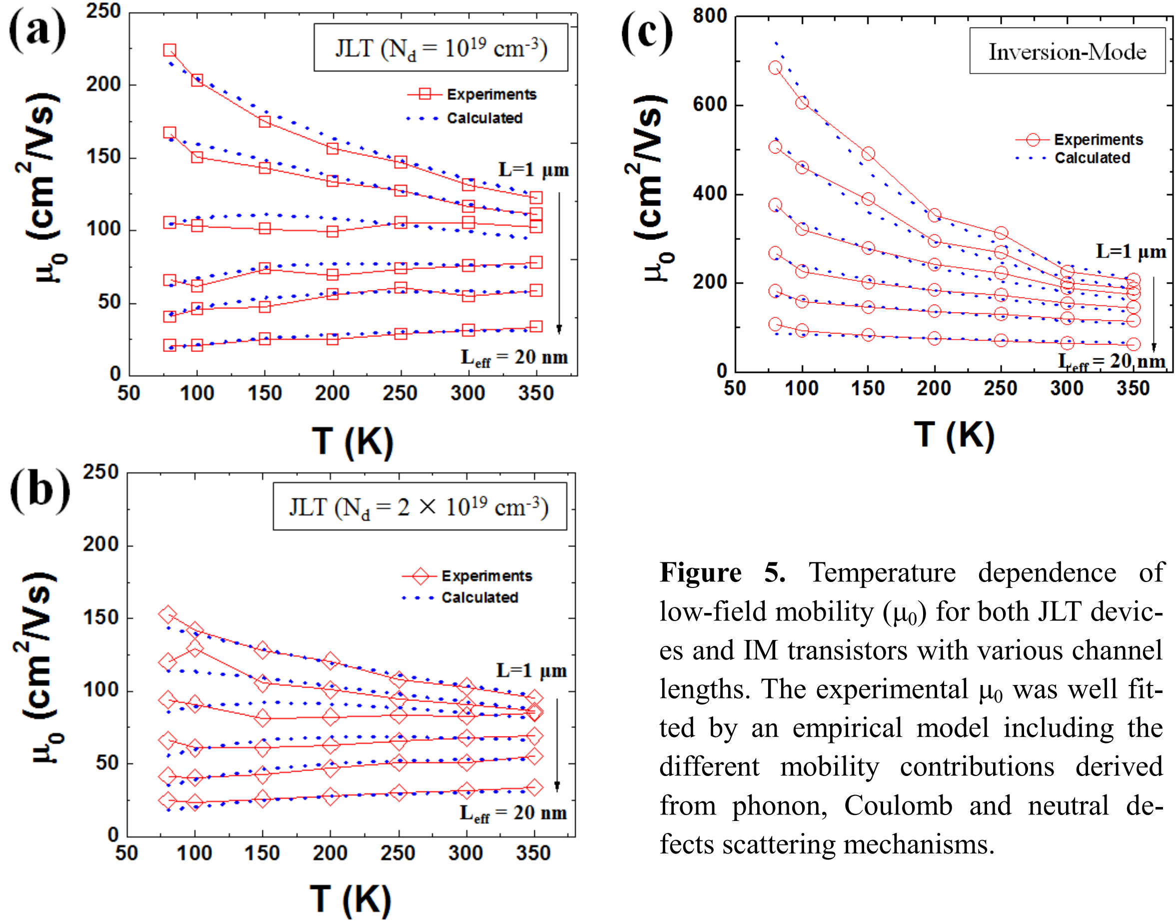

Figure 5. Temperature dependence of low-field mobility (μ_0) for both JLT devices and IM transistors with various channel lengths. The experimental μ_0 was well fitted by an empirical model including the different mobility contributions derived from phonon, Coulomb and neutral defects scattering mechanisms.

Moreover, it should be mentioned that the μ_0 values, extracted at 300 K for long gate length JLTs (L = 1 μm, where the channel can reasonably be considered as free from channel edge parasitic effects, such as the injection of doping atoms or defects in the vicinity of the S/D regions), were found around of 130 $cm^2V^{-1}s^{-1}$ ($N_d = 10^{19}$ cm^{-3}) and 100 $cm^2V^{-1}s^{-1}$ ($N_d = 2\times10^{19}$ cm^{-3}) and are thus fully consistent with bulk silicon electron mobility values reported by C. Jacoboni *et al*. for the same range of doping levels [16].

For short gate lengths, the low-field mobility μ_0 was found to slightly decrease as temperature was lowered for JLT devices, while it was still slightly increasing for IM transistors (although much less than for longer gate lengths). This feature suggests the presence of additional scattering mechanisms, with strong contribution to mobility μ_0, in the vicinity of the S/D regions [17-19]. In order to better analyze the short channel behavior of low-field mobility, the μ_0 values extracted for JLT devices with $N_d = 10^{19}$ cm^{-3} and for IM transistors were plotted again in Fig. 6, this time as a function of gate

length, for only two temperatures (80 K and 300 K). Interestingly, one can note that the μ_0 differences according to varying doping and temperature for short gate lengths are much less than those for long gate lengths.

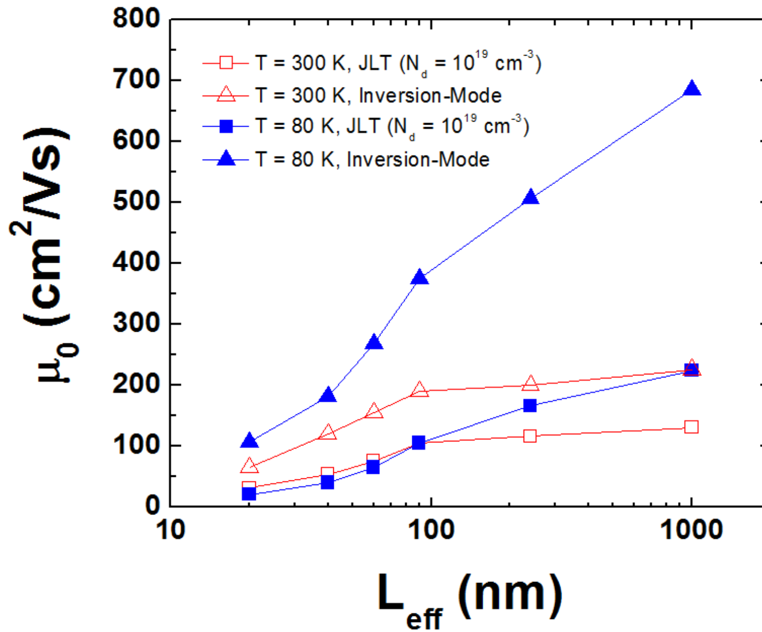

Figure 6. Low-field mobility (μ_0) for JLT devices (N_d = 10^{19} cm^{-3}) and IM transistors as a function of gate length for two temperature values (80 K and 300 K).

This feature can be interpreted by the strengthening of additional scattering mechanisms, which are getting the upper hand at short gate length while being suspected to be poorly influenced by channel doping and temperature.

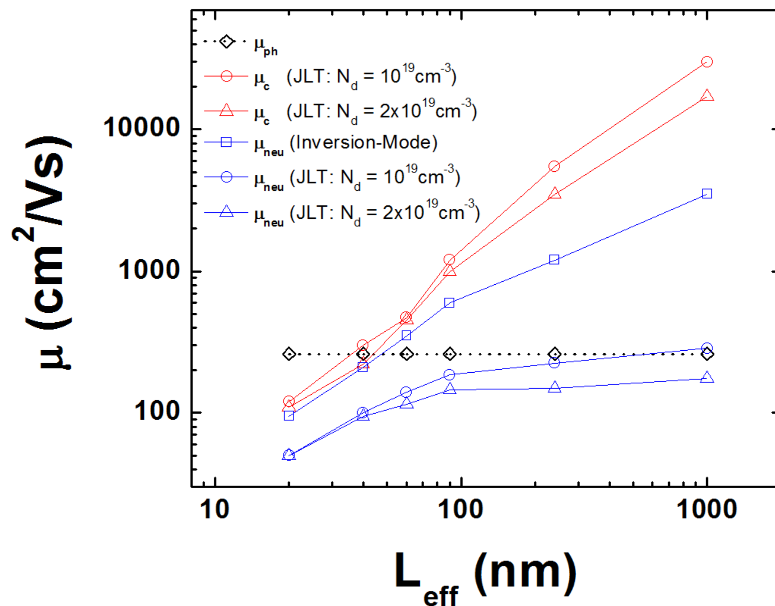

Figure 7. Components of the low-field mobility as a function of gate length, indicating the dominant scattering mechanisms according to device type (JLT or IM) and gate length. The mobility contribution due to phonon scattering could be kept constant, while the influence of neutral defects and Coulomb scattering increased as gate length decreased.

The additional scattering can be further analyzed by fitting the experimental μ_0 in Fig. 5 to an empirical model based on Matthiessen's rule as below [17]:

$$\frac{1}{\mu_0} = \frac{1}{\frac{300}{T} \cdot \mu_{ph}} + \frac{1}{\frac{T}{300} \cdot \mu_c} + \frac{1}{\mu_{neu}} \qquad (7)$$

where μ_{ph}, μ_c and μ_{neu} denote the mobility contributions derived from phonon scattering, Coulomb scattering and temperature independent neutral defects scattering, respectively. The values of the individual mobility components contributing to μ_0 are collected in Table 1 and displayed in Fig. 7 as a function of gate length in order to discriminate the different mobility contributions.

For long gate lengths, the phonon scattering and neutral defects scattering mechanisms were together limiting the overall μ_0 behavior of JLT devices, while for IM transistors phonon scattering was dominant. In particular, the influence of Coulomb and neutral defects scattering was reinforced in JLT devices with higher doping concentration ($N_d = 2\times10^{19}$ cm^{-3}) due to the increased impurity level and implantation induced defects in the channel [18]. In contrast, for short gate lengths, the μ_0 of JLT devices was mostly limited by Coulomb and neutral defects scattering, whereas the neutral defects scattering dominated that of IM transistors.

Table 1. Extracted values of the low field mobility components derived from a fit of experimental results taking into account phonon scattering (μ_{ph}), Coulomb scattering (μ_c) and neutral defects scattering (μ_{neu}).

JLT ($N_d = 10^{19}$ cm^{-3})

L_{eff} (nm)	20	40	60	90	240	1000
μ_{ph} (cm^2/Vs)	260	260	260	260	260	260
μ_c (cm^2/Vs)	120	300	470	1200	5500	30000
μ_{neu} (cm^2/Vs)	50	100	140	185	225	285

JLT ($N_d = 2 \times 10^{19}$ cm^{-3})

L_{eff} (nm)	20	40	60	90	240	1000
μ_{ph} (cm^2/Vs)	260	260	260	260	260	260
μ_c (cm^2/Vs)	110	220	450	1000	3500	17000
μ_{neu} (cm^2/Vs)	50	95	115	145	150	175

Inversion-Mode

L_{eff} (nm)	20	40	60	90	240	1000
μ_{ph} (cm^2/Vs)	260	260	260	260	260	260
μ_c (cm^2/Vs)	100000	100000	100000	100000	100000	100000
μ_{neu} (cm^2/Vs)	95	210	350	600	1200	3500

Convincingly, the extraction led to physically sounded results, such as a constant value of phonon scattering, whatever the gate length, operation mode and channel doping [17]. In addition, it has already been found that defects such as vacancies, interstitial atoms and clusters of (charged or neutral) defects can be produced near the source and drain regions of MOS devices by the S/D ion-implantation process, and that these defects strongly attenuate mobility variation with temperature for shorter channels [18]. This phenomenon can explain mobility degradation at short gate length, not only for IM transistors, but also for the JLT devices tested here. Indeed, although it is not mandatory from a theoretical point of view in such JLT devices, an additional implantation was used in order to reduce access series resistance. In short JLT devices, this implantation is at the origin of an extra defect-induced scattering, localized near the source and drain, which adds to the Coulomb scattering due to heavily doped channel.

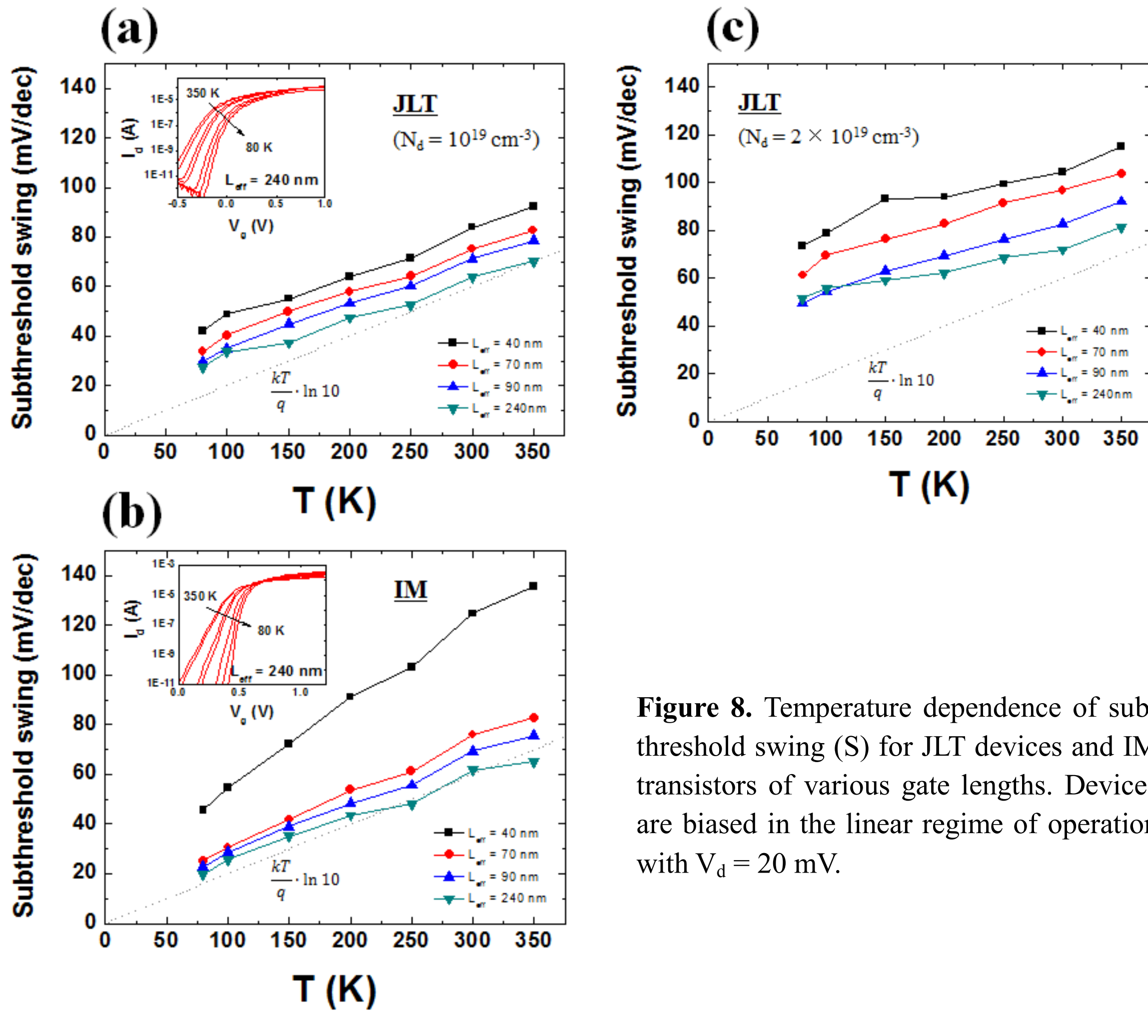

Figure 8. Temperature dependence of subthreshold swing (S) for JLT devices and IM transistors of various gate lengths. Devices are biased in the linear regime of operation with V_d = 20 mV.

3.3.4 Subthreshold swing

The temperature dependence of the subthreshold swing (S) extracted from S = $dV_g/d[\log(I_d)]$ is plotted in Fig. 8 for JLT devices and IM transistors of various gate lengths. For long gate lengths, the S values extracted for JLT devices ($N_d = 10^{19}$ cm^{-3}) were comparable to those of IM transistors, and close to the ideal value, (kT/q)×ln10. For shorter gate lengths, JLT devices featured only slightly higher S values than IM transistors. These relatively higher S values in JLT devices might originate from their reduced gate controllability, due to their larger equivalent electrical oxide thickness [4]. The S values of more heavily doped JLT devices ($N_d = 2\times10^{19}$ cm^{-3}) were also slightly larger than those of JLT devices with $N_d = 10^{19}$ cm^{-3}, as shown in Fig. 8(c). However, for the shortest channel lengths, L_{eff} = 40 nm, the subthreshold swing of IM transistor was abruptly raised due to short channel effects. No such increase was observed for JLT devices due to a better electrostatic immunity against the highly doped S/D regions, which proved to be much more robust against short channel effects in the subthreshold regime. This can be one of their strong advantages compared to the traditional IM transistors.

3.4 Conclusions

Junctionless transistors (JLT) with planar structures (W = 10 μm) were fabricated on (100) SOI wafers with 145 nm thick BOX and 9.4 nm thick silicon. The electrical performances of the JLT devices were investigated under low temperature, in the range of 80 K to 350 K, and compared to those of inversion-mode (IM) transistors featuring the same structure, and fabricated by the same process except for channel doping level. From its overall temperature dependence, it was found that the low-field mobility (μ_0) of JLT devices was limited by phonon and neutral defect scattering for long gate lengths, whereas Coulomb and neutral defect scattering mainly dominated for short lengths, due to defects induced by the additional S/D implantation process, close to source/drain (S/D) regions. There was no significant difference between the temperature dependent variations of flat-band (V_{fb}) and threshold (V_{th}) voltages extracted by the transconductance derivative (dg_m/dV_g) in JLT devices. Moreover, the subthreshold swing (S) of JLT devices was only slightly higher than that of IM transistors, due to their reduced gate electrostatic control. However, the robustness of the subthreshold swing against short channel effects for the shortest gate lengths is a strong advantage of JLT devices. Therefore, it should be noted that JLT devices are more robust to short channel effect in terms of S fluctuations than IM transistors for future technology nodes.

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Chapter 4

Low-frequency noise behavior of junctionless transistors

Low-frequency (LF) noise characteristics of wide planar junctionless transistors (JLT) are investigated. Interestingly, carrier number fluctuation is the main contributor to the LF noise behavior of JLT devices, even though their bulk conduction features are clearly proved by the extracted flat-band voltage (V_{fb}). This is explained by the fact that mobile electrons in depletion, originating from the bulk neutral channel or source/drain regions, can interact with slow traps in the gate oxide, giving rise in return to fluctuations of the charge density in the bulk neutral channel. The similar values of trap density (N_t) are extracted from in JLT devices and inversion-mode (IM) transistors, which also supports that the LF noise of JLT is well explained by the carrier number fluctuation model.

4.1 Introduction

Reduced LF noise is a quality and reliability indicator for electronic devices. It is also required for RF applications in order to limit phase noise. Junctionless transistors (JLT) have several promising advantages such as no need of ultra-shallow and abrupt junctions thanks to their quite simple structures without PN junctions, relaxed requirements for the down-scaling of gate insulator thickness and re-

duced electric field perpendicular to the channel [1-4]. In addition, the bulk conduction of JLT devices, instead of surface conduction for inversion-mode (IM) transistors, is credited for reduced surface roughness scattering and low-frequency (LF) noise [1, 5, 6].

In general, in surface conduction dominated IM transistors, LF noise results from carrier number fluctuations at the interfaces between channel and gate dielectric layer, whereas for bulk conduction based devices it arises dominantly from Hooge mobility fluctuations. Therefore, as JLT devices operate in the bulk conduction regime, it might be expected that their LF noise is explained by the Hooge mobility fluctuations model [7-10]. Recently, it has been shown that the regime of bulk conduction can be clearly observed in wide planar JLT devices through the flat-band voltage (V_{fb}) extracted from the derivative of transconductance [11].

This is the aim of this chapter to investigate the LF noise behavior of JLT devices with planar st ructures (W = 10 μm), which show clear features of bulk conduction and to compare it to that of IM transistors fabricated with the same process except for channel doping.

4.2 Device fabrication and experiment

For this study, N-type JLT devices with high-k/ metal gate stack were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) and Si body thinned down to 9. 4 nm.

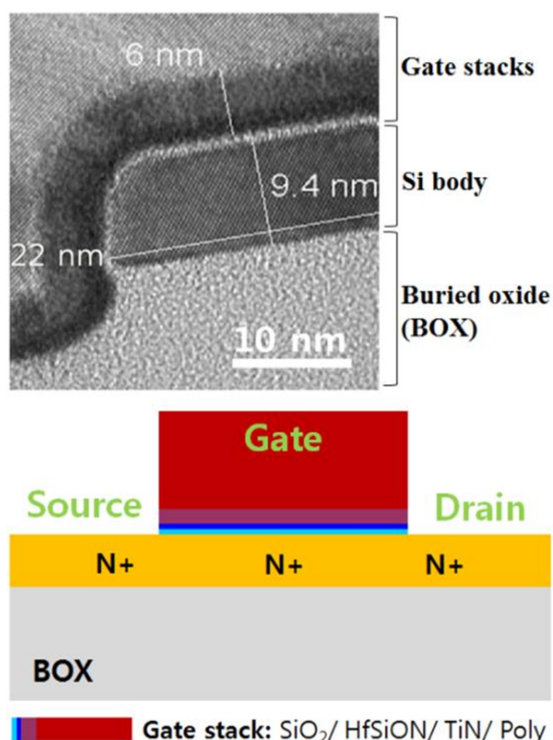

Figure 1. Schematic architecture of the fabricated JLT devices (lower) and transmission electron microscopy (TEM) cross-section showing well defined gate stack with thinned Si body (upper).

A full-sheet implantation was performed before active regions patterning, with a phosphorus dop ing targeted at $N_d = 2\times10^{19}$ cm^{-3}. The effective doping concentration extracted from Maserjian's function (Y_M) was $\approx 0.9\times10^{19}$ cm^{-3} [11]. The gate was composed of an HfSiON, ALD TiN and Pol ysilicon stack, with an equivalent oxide thickness of 1.2 nm. Figure 1 displays the schematic a rchitecture of the fabricated JLT devices, as well as a transmission electron microscopy (TE M) cross-section showing well defined gate stack on the thinned Si channel. The I-V current-voltage characteristics were recorded using an HP4155a measurement unit and the LF noise measurements were carried out using Programmable Point-Probe Noise Measuring System (3P NMS) from 10 Hz up to 10 kHz [12].

4.3 Experimental results and discussion

Drain current (I_d) of JLT devices with gate lengths of L = 250 nm and L = 1 μm was measured as a function of gate voltage (V_g) as shown in Fig. 2(a). The corresponding transconductance (g_m) and de-rivative of transconductance (dg_m/dV_g) were plotted in Fig. 2(b), respectively. The two peaks on the dg_m/dV_g plots (blue curve), which have been shown to be characteristic of JLT devices [11], were ob-served. This curve shape with two peaks is clearly different from that obtained for IM transistors, which normally shows one single peak only, as illustrated in Fig. 2(c). The first (left-hand side) peak on the dg_m/dV_g curve in Fig. 2(b) corresponds to the conduction threshold (V_{th}), which is the turning point from full channel depletion to partial surface depletion, whereas the second (right-hand side) peak gives the flat-band (V_{fb}) position, which separates surface depletion regime, with a bulk neutral channel, from surface accumulation [11]. The value of V_{fb} for JLT device with long gate length (L = 1 μm, where the channel can reasonably be considered as free from mobility degradation and series re-sistance effects) was equal to about 0.54 V. This extracted value is fully consistent with the theoretical value of 0.545 V calculated using the following equation [13]:

$$V_{fb} = \Phi_{MS} = \Phi_M - \left[\chi + \frac{E_g}{2} - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_d}{n_i} \right) \right] \quad (1)$$

where Φ_M, χ, E_g and n_i denote metal work function, electron affinity, energy band-gap of silicon and intrinsic carrier density, respectively. In our case, the gate metal used was featuring a work function close to mid-gap. The dotted line follows the V_{fb} position across Figs. 2(a) and 2(b) in order to draw attention to the portion of the JLT devices I-V characteristics, on the left-hand side of this line, where current is governed by bulk conduction.

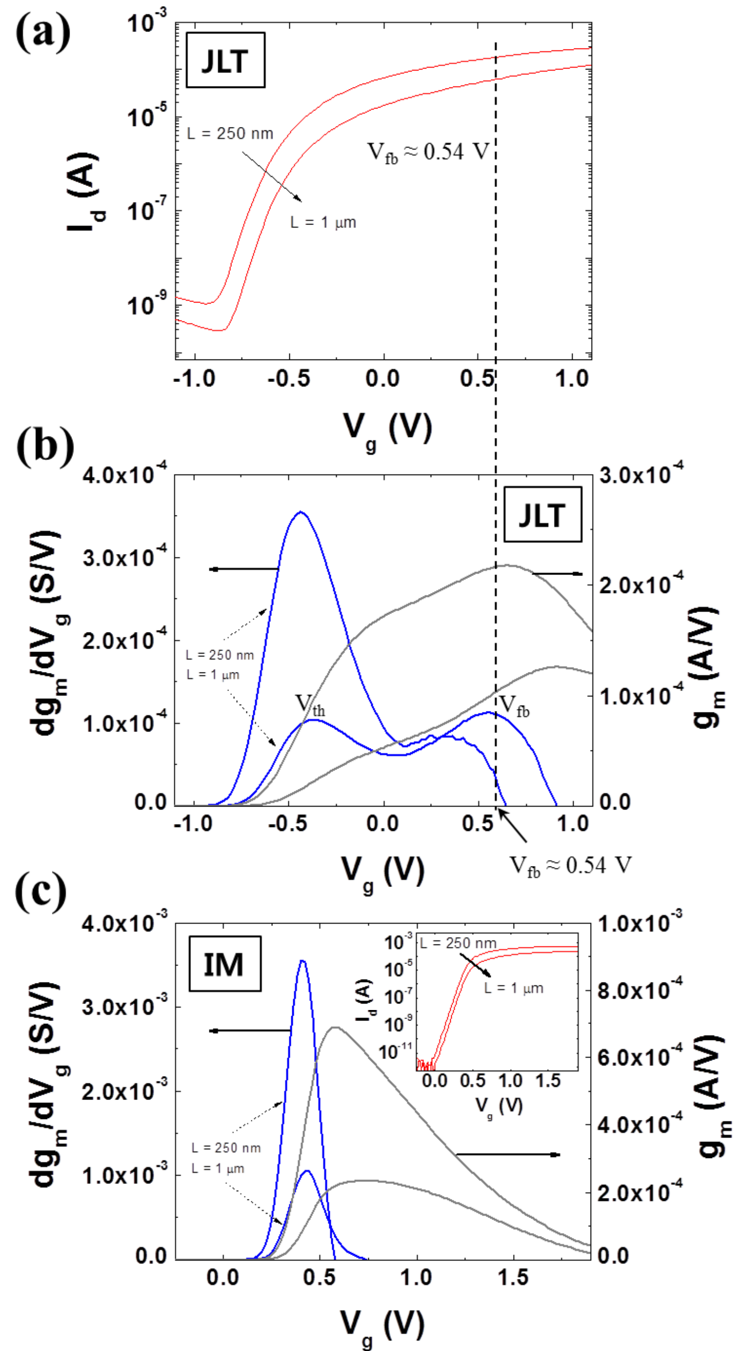

Figure 2. (a) Drain current I_d of JLT devices with W = 10 µm measured as a function of V_g and (b) its corresponding transconductance g_m (gray) and derivative of transconductance dg_m/dV_g (blue), (c) the compared I_d (inset), g_m and dg_m/dV_g of IM transistors with same structures. Devices are biased in the linear regime of operation with V_d = 50 mV.

Figure 3(a) displays the frequency dependence of LF noise power spectrum density (PSD), as measured for JLT and IM transistors, at same drain current level ($\approx 1.7 \times 10^{-4}$ A). They both show typical 1/*f* dependence. Variation of the normalized drain current PSD (S_{Id}/I_d^2) as a function of drain current was also plotted, in Fig. 3(b) for JLT devices and in Fig. 3(c) for IM transistors.

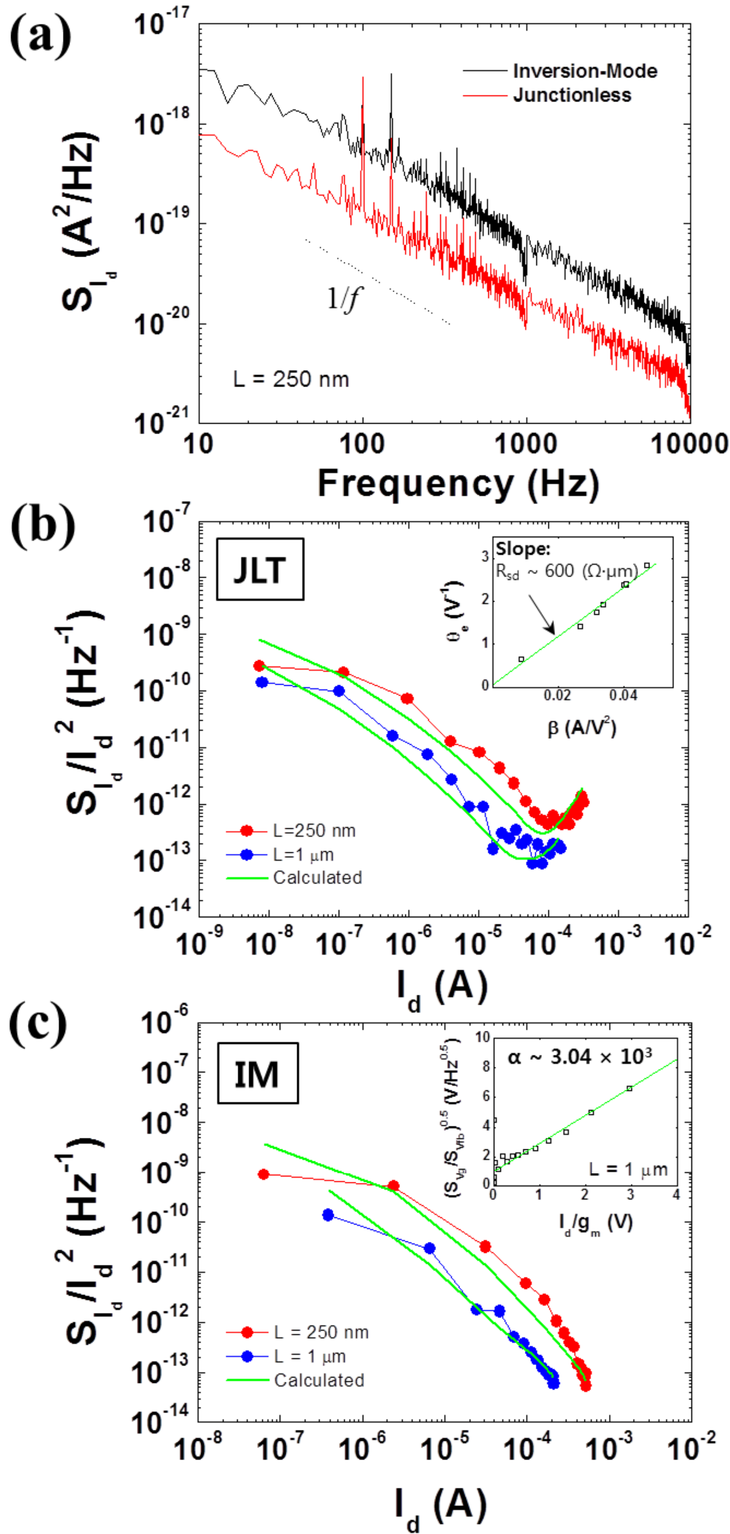

Figure 3. (a) Typical power spectrum density (PSD) of LF noise for both JLT device and IM transistor at same drain current of ≈ 1.7 × 10^{-4} A (V_d = 50 mV). (b) Variations of the normalized drain current PSD (S_{Id}/I_d^2) extracted at 1 kHz as a function of drain current for JLT devices. The inset shows the first order mobility attenuation factor (θ_e) versus conductance gain (β) plot. (c) Variations of S_{Id}/I_d^2 as a function of drain current for IM transistors with the inset regarding $(S_{Vg}/S_{Vfb})^{1/2}$ versus I_d/g_m for the extraction of the Coulomb scattering coefficient α.

There are two main models to explain LF noise in MOSFETs. One is the carrier number fluctuation model with correlated mobility fluctuation, originating from the flat-band voltage (V_{fb}) variation due

to slow oxide traps in the gate insulator, with associated variation of mobility due to remote Coulomb scattering. From this model, the normalized drain current PSD can then be expressed as [7-10]:

$$\frac{S_{I_d}}{I_d^2} = (1+\alpha\mu_{eff}C_{ox}I_d/g_m)^2\left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \quad (2)$$

where α is the Coulomb scattering coefficient, μ_{eff} is the effective mobility, C_{ox} is the gate oxide capacitance per unit area and S_{Vfb} denotes the flat-band voltage PSD. The other one is the Hooge mobility fluctuation model, from which S_{Id}/I_d^2 varies approximately as I_d^{-1}. It is widely accepted that the carrier number fluctuations model is well suited to the interpretation of LF noise in surface channel devices, whereas the Hooge model better explains LF noise behavior in bulk conduction based devices. However, it was found here that, the normalized drain current PSD was varying with drain current as the transconductance to drain current ratio squared $(g_m/I_d)^2$, not only for the surface conduction dominated IM transistors (Fig. 3(c)) but also for JLT devices (Fig. 3(b)). This suggests that the overall LF noise of JLT devices is governed by carrier number fluctuations even though the evidence of bulk conduction was clearly proved through the extracted V_{fb} as shown in Fig. 2(b). In addition, the normalized drain current PSD of JLT devices in Fig. 3(b) was raising at high drain current. This is a series resistance (R_{sd}) effect [7]. Indeed, the R_{sd} extracted from the first order mobility attenuation factor (see inset of Fig. 3(b) [14]) was significantly larger for JLT devices ($R_{sd} \approx 600\ \Omega\cdot\mu m$) than for the optimized fully depleted SOI wafer devices used as IM reference ($R_{sd} \approx 200\ \Omega\cdot\mu m$). Using this value of R_{sd}, the normalized drain current PSD of JLT devices was well fitted in Fig. 3(b) using a revised version of the carrier number fluctuations model of equation 2, which includes the additional channel current noise stemming from the R_{sd} as follows [7]:

$$\frac{S_{I_d}}{I_d^2} = (1+\alpha\mu_{eff}C_{ox}I_d/g_m)^2\left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} + \left(\frac{I_d}{V_d}\right)^2 S_{R_{sd}} \quad (3)$$

where S_{Rsd} represents the PSD of series resistance. No such correction was needed for the optimized IM transistors due to their lower series resistance. In IM transistors, it was possible to extract the Coulomb scattering coefficient α from the relationship between $(S_{Vg}/S_{Vfb})^{1/2}$ and I_d/g_m derived from equation 2, where S_{Vg} is the input gate voltage noise (see inset of Fig. 3(c)). The extracted value of α, around 3.0×10^3 Vs/C, is comparable to the typical value, of about 10^4 Vs/C, for electrons in MOSFETs [9].

Figure 4(b) is schematically illustrating the possible physical mechanisms explaining why LF noise, could indeed originate from carrier number fluctuation in JLT devices despite their bulk conduction.

Although, below V_{fb}, the bulk neutral channel of n-type JLT devices is separated from the interface by the depleted region (surface depletion regime), diffusion through the depletion region followed by tunneling to the traps, or direct tunneling from the neutral regions to the traps, can allow some mobile electrons from the bulk channel or from S/D regions to interact with slow traps in the gate oxide. The variation of the interfacial oxide charge density (δQ_{ox}), induced by the dynamic trapping-detrapping of the mobile electrons, causes a fluctuation of the flat band voltage, $\delta V_{fb} = -\delta Q_{ox}/C_{ox}$. In turn, fluctuations of V_{fb} are giving rise to fluctuations of the total charge density (Q_{sc}), including mobile and fixed charges, in the channel located under the depletion region, as shown in Fig. 4(b). Indeed, it is set by charge conservation that [6]:

$$V_g = V_{fb} + \Phi_s - \frac{Q_{sc}}{C_{ox}} \qquad (4)$$

where Φ_s is the surface potential. This explains why the carrier number fluctuation model can fit LF noise for JLT devices.

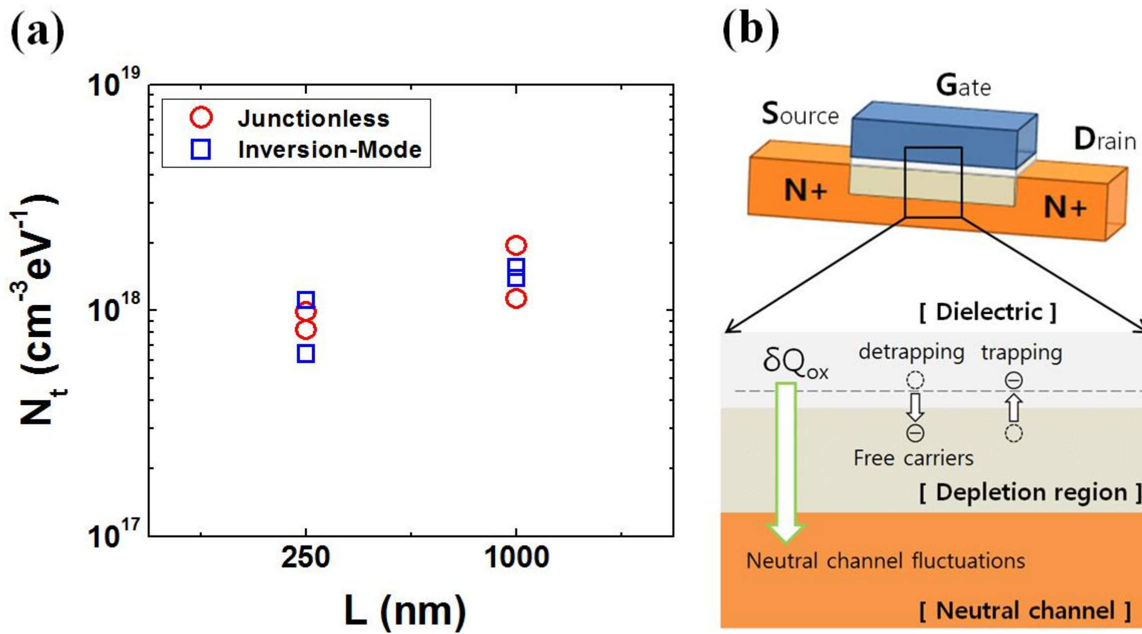

Figure 4. (a) The extracted trap density according to gate lengths for both JLT devices and IM transistors. (b) Schematic illustrating possible physical mechanisms of the LF noise behavior originating from the carrier number fluctuation for JLT devices based on bulk conduction.

In addition, the trap density (N_t) was extracted from the flat-band voltage PSD given by [7, 9, 10]:

$$S_{V_{fb}} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f} \qquad (5)$$

where q, k, T and λ denote electronic charge, Boltzmann constant, temperature and the tunnel attenuation distance, respectively. Trap density values extracted for both JLT devices and IM transistors are displayed in Fig. 4(a). They reach very similar values ($\approx 10^{18}$ $cm^{-3}eV^{-1}$) irrespective of de vice type. This clearly supports the above mentioned explanation about carrier number fluctuati on mechanism for LF noise behavior in JLT devices. The trap density values in Fig. 4(a) are al so consistent with the typical values of $10^{18} \sim 10^{20}$ $cm^{-3}eV^{-1}$ generally found for metal gate/hi gh-k CMOS transistors [9]. Moreover, it should be noted that D. Jang *et al*. recently reported that the carrier number fluctuations model also well explained the LF noise of JLT devices with nanowire like structures [15].

4.4 Additional issues regarding this study

It is possible for mobile electrons (in bulk neutral channel) to interact with slow traps in the buried oxide (thick 145 nm SiO_2), while the back contact was always grounded for 1/f noise measurements. This could affect to the overall 1/f noise behavior with interaction at the top gate oxide. However, the interaction at the top gate oxide (high-k) mainly dominates the overall 1/f noise behavior, since the carrier fluctuation at the high-k dielectrics is generally known as much higher than that at pure SiO_2 dielectrics [9]. Moreover, the extracted trap density (N_t) of $\approx 10^{18}$ $cm^{-3}eV^{-1}$ in JLT devices as shown in Fig. 4(a) was consistent to the typical values for high-k CMOS transistors and also was close to that in the counterpart, IM transistors. This proves the overall 1/f noise is dominantly derived from the trapping-detrapping interaction at the high-k top gate dielectrics.

There is V_{fb} difference between L = 1 μm and L = 250 μm of JLT devices due to the series resistance and mobility degradation effects. The V_{fb} of ≈ 0.54 V in the case of L = 1μm is closer to the exact V_{fb} value, because there is less series resistance and mobility degradation effects in long-length devices. Moreover, if we can extract the V_{fb} from dC_{gc}/dV_g, the V_{fb} should be very close to the exact value. However, C_{gc} measurements need as large-scale devices as possible for a better accuracy.

The effective doping concentration extracted from Maserjian function was $\approx 0.9 \times 10^{19}$ cm^{-3} [11]. With this extracted doping, the threshold voltage V_{th} and the maximum depletion width W_{max} were calculated as ≈ – 0.54 V and ≈ 12 nm, respectively, using following equations [4]:

$$V_{th} = V_{fb} - \frac{q \cdot N_d \cdot t_{si}^2}{2\varepsilon_{si}} - \frac{q \cdot N_d \cdot t_{si}}{C_{ox}} \qquad (6)$$

$$W_{\max} = 2 \cdot \left(\frac{\varepsilon_{si} \cdot kT \cdot \ln\left(\frac{N_d}{n_i}\right)}{q^2 N_d} \right)^{0.5} \qquad (7)$$

where ε_{si} and k denotes silicon permittivity and Boltzmann constant, respectively. The $W_{max} \approx 12$ nm means that it is possible for the fully depleted state to be created in that JLT devices, since Si thickness is around 9.4 nm.

4.5 Conclusions

In summary, N-type junctionless transistors (JLT) with planar structures (W = 10 μm) were fabricated on (100) SOI wafers with 145nm thick BOX and 9.4 nm thick silicon. The low-frequency (LF) noise of the JLT devices was investigated and compared to that of inversion-mode (IM) transistors with same structure. Interestingly, the LF noise behavior of the JLT devices was represented by a carrier number fluctuation model, even though the evidence of bulk conduction in the JLT devices was clearly proved by the flat-band voltage (V_{fb}) extracted from the derivative of the transconductance (dg_m/dV_g). These results are interpreted by the possible trapping-detrapping into slow traps in the gate oxide of mobile electrons that diffused from the bulk neutral channel or source/drain regions into the depletion region or that directly tunnel from the neutral regions to the traps. The extracted trap density of JLT devices was quite similar to that of IM transistors. This feature also supports our finding that the LF noise behavior of JLT devices is originated from carrier number fluctuations.

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Chapter 5

New parameter extraction method for junctionless transistors

5.1 A new method for the extraction of flat-band voltage and doping concentration in tri-gate junctionless transistors

5.2 New method for the extraction of bulk channel mobility and flat-band voltage in junctionless transistors

A new method for the extraction of flat-band voltage (V_{fb}) and channel doping concentration (N_d) in Tri-gate Junctionless transistors (JLT) is presented. The new method, based on the relationship between the top-effective width (W_{top_eff}) in accumulation and the effective width (W'_{eff}) in partial depletion, enables the extraction of V_{fb} and N_d of JLT devices (here as ≈ 0.61 V and ≈ 6.4×10^{18} cm^{-3}, respectively). The validity of the new method is also proved by 2D numerical simulations. Furthermore, it is emphasized that the sidewall accumulation current (I_{d_side}) behavior of Tri-gate JLT devices is found to decrease dramatically near V_{fb}, allowing an estimation of the V_{fb} position of JLT devices.

A new and simple method for the extraction of electrical parameters in junctionless transistors (JLTs) is presented. The bulk channel mobility (μ_{bulk}) and flat-band voltage (V_{fb}) were successfully extracted from the new method, based on a linear dependence between the inverse of transconductance squared ($1/g_m^2$) vs gate voltage in the partially depleted operation regime ($V_{th} < V_g < V_{fb}$). The

validity of the new method is also proved by 2D numerical simulation and newly defined Maserjian's-like function for g_m of JLT devices.

5.1 A new method for the extraction of flat-band voltage and doping concentration in tri-gate junctionless transistors

5.1.1 Introduction

Junctionless Transistors (JLT) have been considered as a possible candidate for the continuation of Moore's law, owing to their promising advantages such as quite simple structures without PN junctions, the relaxed requirements of gate insulator thickness in terms of the down-scaling rule and the reduced electric-field perpendicular to the channel [1, 2]. Especially, the operation of JLT devices is quite different from the standard inversion-mode (IM) transistors. Indeed, it is based on bulk conduction suspected to reduce surface roughness scattering, as well as accumulation conduction separated by the flat-band voltage (V_{fb}). However, there are also several issues related to the channel doping concentration (N_d) of JLT devices such as trade-off between high level of channel doping and bulk mobility degradation and the variability of both threshold voltage and drain induced barrier lowering (DIBL) [3-6]. Therefore, V_{fb} and N_d of JLT devices are key parameters for a better understanding of their physical operation. That is the reason why the exact determination of V_{fb} and N_d in JLT devices is a very important issue.

This chapter presents a new method for the extraction of both V_{fb} and N_d in Tri-gate JLT devices. The principle of the new method is based on the fact that the electrical top-effective width (W_{top_eff}) of Tri-gate JLT devices at the onset of accumulation should be the same as the effective width (W'_{eff}) of bulk neutral channel near the ending of depletion at the flat-band condition. The V_{fb} and N_d extracted from the new method are well consistent to those from previously reported method such as the derivative of transconductance and Maserjian's function [7]. The validity of the new method is also proved by two-dimensional (2D) numerical simulations. Furthermore, a specific gate voltage (V_g^*), where the side-wall accumulation current (I_{d_side}) extracted using the W_{top_eff} is found to vanish dramatically, is interestingly similar to the V_{fb} extracted from the new method.

5.1.2 Device fabrication and experiment

For this study, N-type Tri-gate JLT devices with high-k/metal gate stack were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) and a Silicon (Si) body thinned down to ≈ 9.4 nm. A full-sheet implantation was performed before active patterning with a phosphorus doping

targeted at 1×10^{19} cm^{-3} or 2×10^{19} cm^{-3}. The gate is composed of HfSiON/ TiN/ Polysilicon, with an equivalent oxide thickness of 1.2 nm. Figure 1 displays the schematic architecture of the fabricated Tri-gate JLT devices, as well as a transmission electron microscopy (TEM) cross-section clearly showing well defined gate stack, with top surface and sidewall component on the thinned Si channel. On-mask gate widths W_M were 350 nm, 500 nm and 1 μm, respectively. For a better accuracy of the gate-to-channel capacitance (C_{gc}) values, long JLT devices (L_M = 10 μm) were used, in arrays of 50 channels.

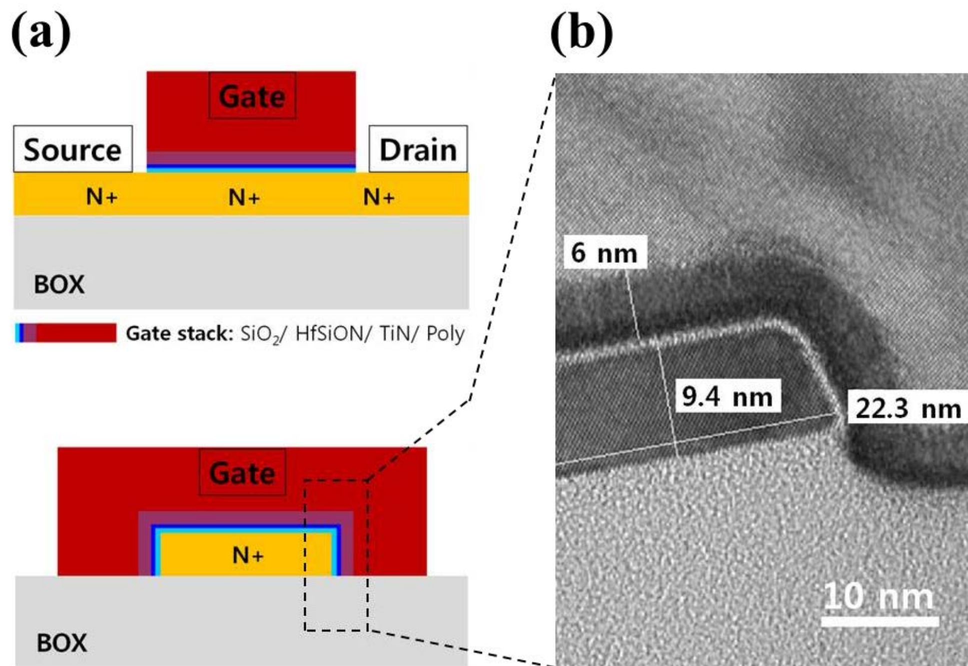


Figure 1. (a) Schematic cross-section of the fabricated Tri-gate JLT devices (upper: longitudinal direction , lower: transverse direction), (b) transmission electron microscopy (TEM) showing well defined gate stack, with top surface and sidewall component on thinned Si (≈ 9.4 nm). The gate is composed of HfSiON/ TiN/ Polysilicon layers with an equivalent oxide thickness of 1.2 nm.

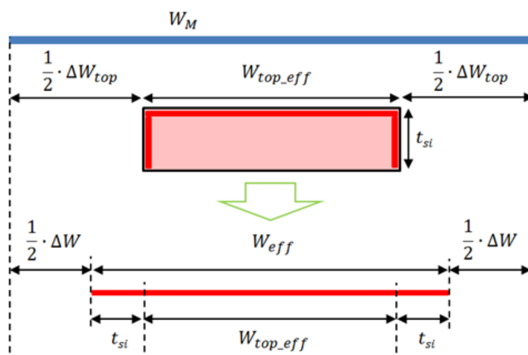
The C-V capacitance-voltage measurements were recorded using an HP4294a with a 50 mV small signal at 500 kHz and the C_{gc} was extracted from C-V measurements by connecting the “high” terminal of HP4294a to gate electrode and “low” terminal to source and drain electrodes. The I-V current-voltage characteristics were also taken out using HP4155a measurement unit. Moreover, FlexPDE 5.0 software based on the finite element method was used for 2D Poisson equation numerical simulations.

5.1.3 Experimental results and discussion

5.1.3.1 Principle of the new method

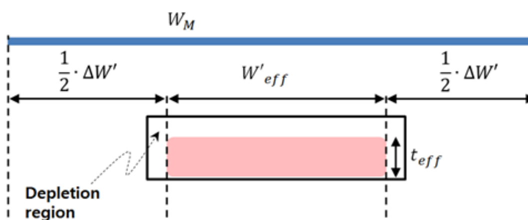
As increasing V_g, the operation of JLT devices is evolving from full depletion (no conduction) to partial depletion (bulk neutral channel with gate controlled thickness). At $V_g = V_{fb}$ condition, the whole device Si body is full of a bulk neutral channel and then an accumulation layer appears at high-k/silicon interface of Tri-gate devices according to further increased gate voltage ($V_g > V_{fb}$).

- Accumulation region: $V_g > V_{fb}$



$$C = C_{ox} \times L \times (W_M - \Delta W)$$

- Partially depleted region: $V_g < V_{fb}$



$$\frac{Q}{q} = N_d \times L \times t_{eff} \times W'_{eff}$$
$$= N_d \times L \times t_{eff} \times (W_M - \Delta W')$$

Accumulation channel

Bulk neutral channel

- At flat-band condition: $V_g = V_{fb}$

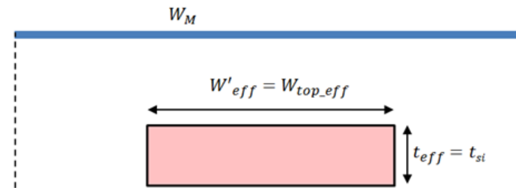


Figure 2. Illustration explaining the principle of a new method for the extraction of V_{fb} and N_d in Tri-gate JLT devices. At flat-band (V_{fb}) condition, the W'_{eff} and t_{eff} in bulk neutral channel should be equal to the W_{top_eff} and t_{si} (≈ 9.4 nm) in accumulation, respectively.

Figure 2 illustrates the principle of the new method for the extraction of V_{fb} and N_d parameters in Tri-gate JLT devices, using a correlation between the electrical top-effective width (W_{top_eff}) at accumulation mode and the effective width (W'_{eff}) of bulk neutral channel at partially depleted mode in JLT devices operation. In general, the effective width (W_{eff}) of JLT devices can be extracted from the linear relationship between C_{gc} and on-mask channel width (W_M) at the accumulation mode [7]. Indeed, the C_{gc} can be expressed as:

$$C_{gc} = C_{ox} \cdot L_M \cdot W_{eff} = C_{ox} \cdot L_M \cdot (W_M - \Delta W) \quad (1)$$

where C_{ox} is the oxide capacitance per unit area and ΔW means channel width reduction between effective and on-mask width. The W_{eff} of Tri-gate JLT devices consist of W_{top_eff} and Si body thickness (t_{si}) as illustrated in Fig. 2. Therefore, the W_{top_eff} can be easily calculated as:

$$W_{top_eff} = W_{eff} - 2 \cdot t_{si} \quad (2)$$

The linear relationship between the number of carrier electrons (Q/q) and on-mask channel width (W_M) should also work in the partially depleted region of JLT devices as shown in Fig. 2. One can define the Q/q with the effective width (W'_{eff}) and the effective thickness (t_{eff}) of bulk neutral channel, as the following equation:

$$\frac{Q}{q}(V_g) = N_d \cdot L_M \cdot t_{eff}(V_g) \cdot W'_{eff}(V_g) = N_d \cdot L_M \cdot t_{eff}(V_g) \cdot [W_M - \Delta W'(V_g)] \quad (3)$$

where Q, q, N_d and $\Delta W'$ represent the total charge, the electronic charge, the doping concentration per unit volume and the channel width reduction between W'_{eff} and W_M in bulk neutral region, respectively. The values of W'_{eff} and t_{eff} is increasing with V_g owing to shrinking the depletion region and then those values can be increased up to $W'_{eff} = W_{top_eff}$ and $t_{eff} = t_{si}$ at flat-band condition ($V_g = V_{fb}$), as illustrated in Fig. 2. Then, the doping concentration (N_d) of JLT devices can be simply extracted from equation 3 as:

$$\frac{Q}{q}(V_{fb}) = N_d \cdot L_M \cdot t_{eff}(V_{fb}) \cdot W'_{eff}(V_{fb}) = N_d \cdot L_M \cdot t_{si} \cdot W_{top_eff} \quad (4)$$

5.1.3.2 Extraction of V_{fb} and N_d in JLT devices based on Experimental Capacitance-Voltage characteristics

The C_{gc} were measured as a function of V_g with varying W_M as shown in Fig. 3 (a). Then, the selected C_{gc} at an accumulation regime (V_g = 1.3V) was plotted again as a function of W_M as shown in Fig. 3 (b). The ΔW ($W_M - W_{eff}$) of Tri-gate JLT devices was extracted through extrapolation to zero channel

width led to a value of ≈ 57.6 nm with equation 1. The difference (ΔW_{top}) between W_{top_eff} and W_M can be also calculated as ≈ 76.4 nm using equation 2 with Si thickness of 9.4 nm.

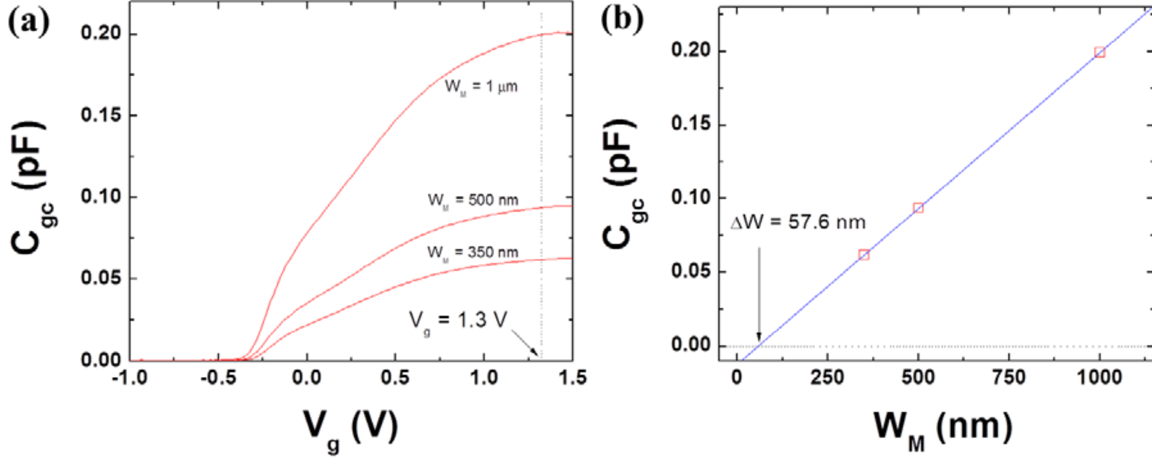


Figure 3. (a) Gate-to-channel capacitance (C_{gc}) of Tri-gate JLT devices measured as a function of V_g with various W_M. Long JLT devices (L_M = 10 µm) in arrays of 50 parallel channels were used for a better accuracy. (b) C_{gc} versus W_M at V_g = 1.3 V (an accumulation regime) for extraction of ΔW.

Figure 4(a) shows the number of electrons in the channel of Tri-gate JLT devices deduced by integration of the C_{gc}:

$$\frac{Q}{q} = \int \frac{C_{gc}(V_g)}{q} dV_g \qquad (5)$$

The ΔW' resulting from the extrapolation to zero channel width using equation 3 was extracted for various gate voltages ranged from -0.2 V to 1.5 V, as shown in the inset of Fig. 4(a). Then, one defines the V_{fb} position of Tri-gate JLT devices at a gate voltage where the value of ΔW' is equal to that of ΔW_{top}. The value of ΔW' was found as ≈ 76.5 nm, which is almost the same as ΔW_{top} ≈ 76.4 nm. Finally, the extracted V_{fb} of JLT devices was around 0.61 V. This value is comparable to that of ≈ 0.56 V derived from the second peak of the transconductance derivative (dg_m/dV_g) in Fig. 5 [7].

In addition, the Q/q at the extracted V_{fb} (≈ 0.61 V) was plotted with various W_M in Fig. 4(b). The value of N_d obtained from the slope as shown in Fig. 4(b) was ≈ 6.4×10^{18} cm^{-3}. This N_d value is quite consistent with the previously reported one of ≈ 5×10^{18} cm^{-3} extracted from the Maserjian's function (Y_M) [7] and also closer to the targeted doping level of 1×10^{19} cm^{-3}.

Figure 4. (a) The number of electrons (Q/q) versus V_g deduced from integration of C_{gc} in Fig. 3. The inset shows the extracted $\Delta W'$ as a function of V_g ranging from -0.2 V to 1.5 V. (b) Q/q versus W_M at the V_g suspected as a V_{fb}, where $\Delta W' = \Delta W_{top}$, for the extraction of N_d.

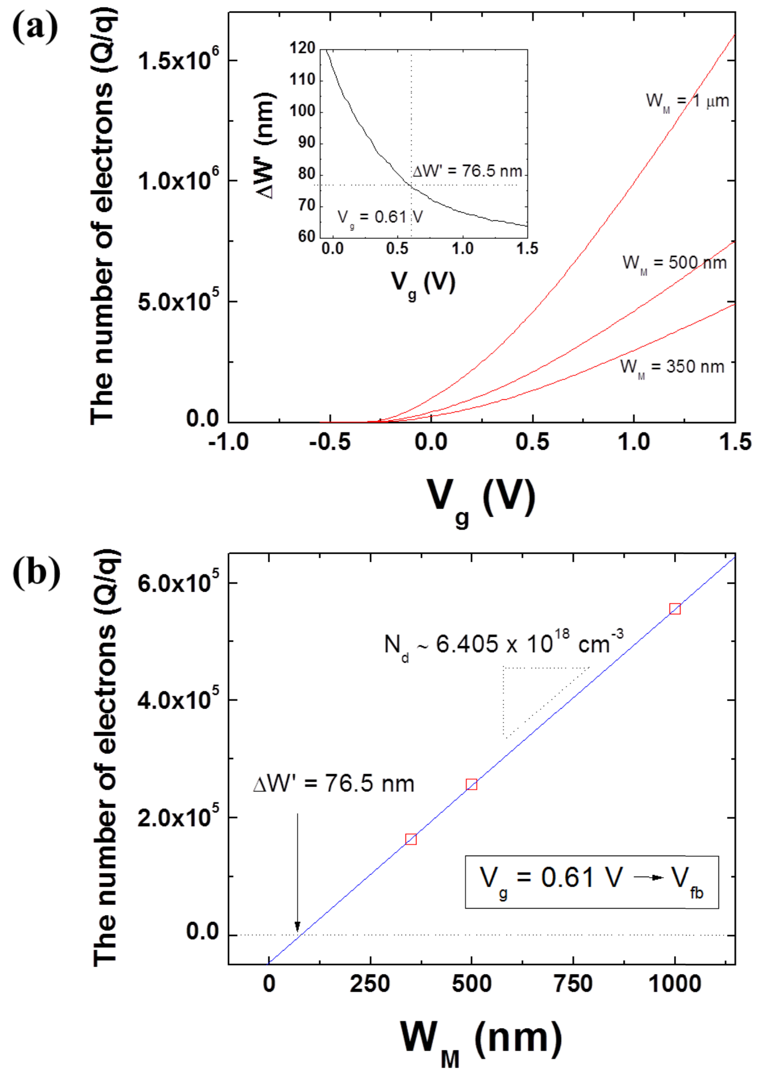
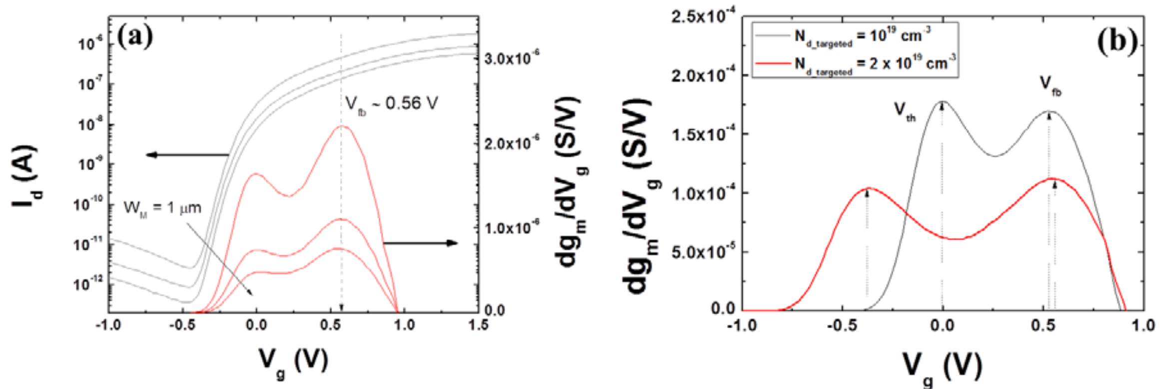


Figure 5. (a) Drain current (I_d, gray) and transconductance derivative (dg_m/dV_g, red) as a function of V_g. The V_{fb} obtained from the second peak point on dg_m/dV_g was ≈ 0.56 V. Devices are biased in the linear regime of operation with V_d = 50 mV. (b) dg_m/dV_g as a function of V_g with two doping levels. As increasing doping concentration, the V_{th} is decreased, while the V_{fb} is slightly increased (W = 10 μm, L = 1 μm).



The same procedure for the extraction of V_{fb} and N_d was carried out with more doped Tri-gate JLT devices (targeted doping level: 2×10^{19} cm^{-3}) as shown in Fig. 6. The extracted V_{fb} and N_d were ≈ 0.65 V and ≈ 1.1×10^{19} cm^{-3}, respectively.

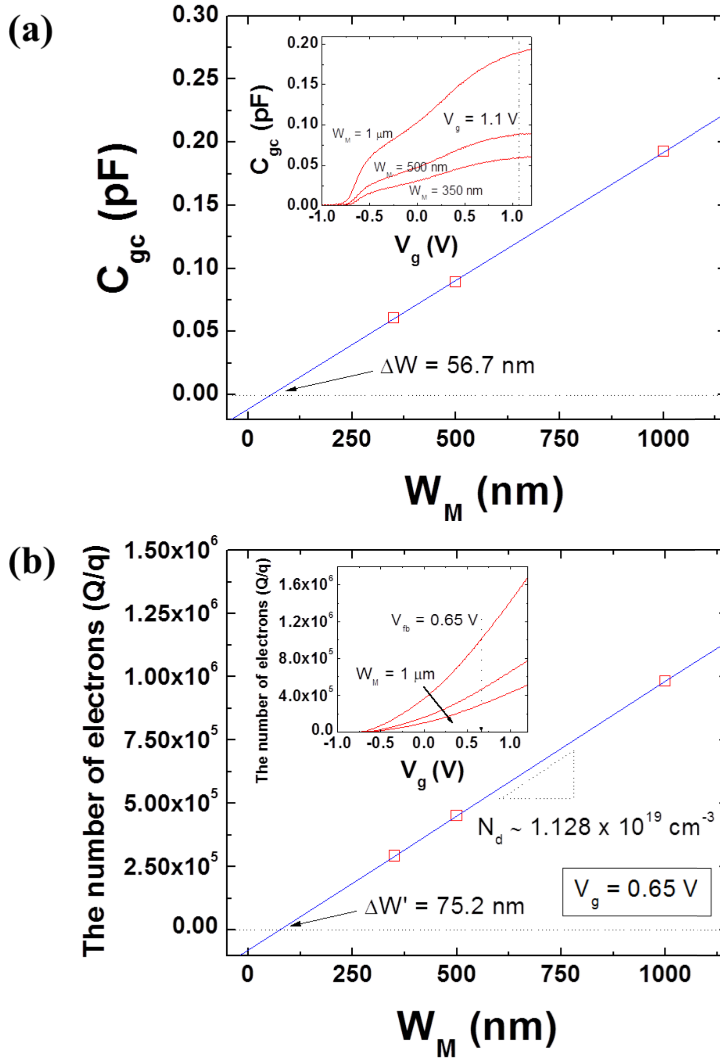


Figure 6. Same plots as in Fig. 3-4 for the extraction of V_{fb} and N_d in more doped Tri-gate JLT devices (targeted doping level: 2×10^{19} cm^{-3}).

The slightly increased V_{fb} (≈ 0.65 V) in the more doped JLT devices compared to that (≈ 0.61 V) of JLT devices in Fig. 3-4 (targeted doping level: 1×10^{19} cm^{-3}) agrees well with both the experimental trend determined from dg_m/dV_g in Fig. 5(b) and the theoretical tendency related to $V_{fb} = kT/q\cdot\ln(N_d/n_i)$, where k, T and n_i denote Boltzmann constant, temperature and intrinsic carrier density, respectively. The N_d ≈ 1.1×10^{19} cm^{-3} (targeted doping level: 2×10^{19} cm^{-3}) was nearly two times compared to N_d ≈ 6.4×10^{18} cm^{-3} (targeted doping level: 1×10^{19} cm^{-3}) in Fig. 3-4, which is also quite reasonable.

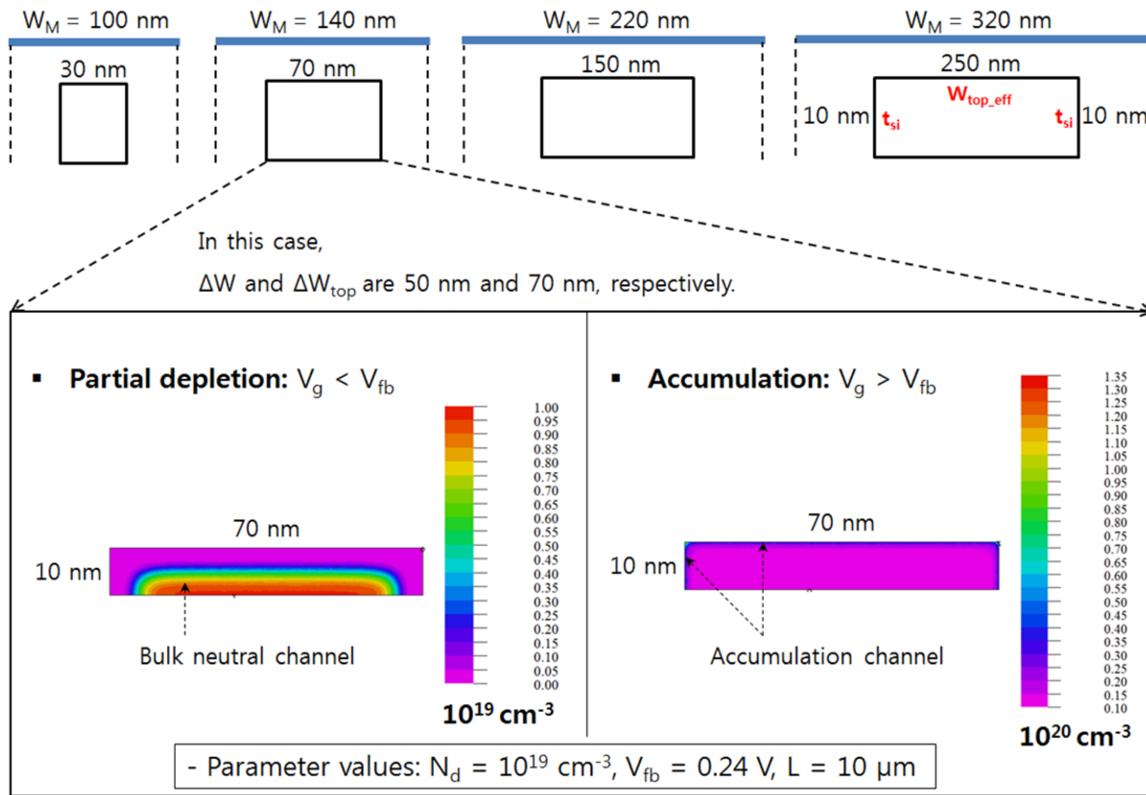


Figure 7. Defined JLT device structures for the numerical simulation and 2D contour plot showing charge density in JLT devices according to operation mode (partial depletion or accumulation).

5.1.3.3 2D numerical simulation for verifying the new method for extraction of V_{fb} and N_d in JLT devices

2D numerical simulations of the Poisson equation was carried out using FlexPDE software based on the finite element method for confirming the validity of the new extraction method of V_{fb} and N_d in Tri-gate JLT devices. Figure 7 shows the defined JLT device structures and electrical parameters including $N_d = 1\times10^{19}$ cm^{-3} and V_{fb} = 0.24 V used for the simulation. In this case, the exact values of ΔW and $ΔW_{top}$ are 50 nm and 70 nm due to t_{si} = 10 nm, respectively. The 2D contour plot representing the charge density in Fig. 7 shows clearly the bulk neutral channel ($V_g < V_{fb}$) and surface accumulation channel ($V_g > V_{fb}$) in JLT devices with the defined structure. Eventually, the parameter values, extracted from the new method studied in the previous section, were ΔW ≈ 48.5 nm, $ΔW_{top}$ ≈ 68.5 nm, $N_d \approx 1.1\times10^{19}$ cm^{-3} and V_{fb} ≈ 0.3 V, respectively as shown in Fig. 8. One can see that the extracted values are very close to the exact values of ΔW = 50 nm, $ΔW_{top}$ = 70 nm, $N_d = 1\times10^{19}$ cm^{-3} and V_{fb} = 0.24 V, which theoretically confirm the validity of the extraction procedure. Furthermore, the slight difference between the extracted values and the defined values could be due to the corner effect, which affects to the device characteristics in tri-gate structures [8].

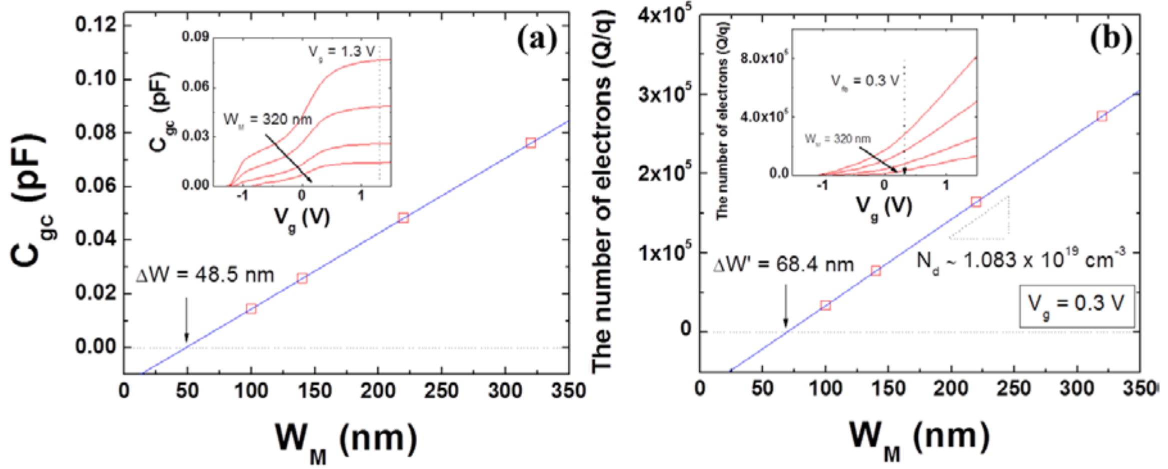


Figure 8. Same plots as in Fig. 3-4 for the extraction of V_{fb} and N_d in the simulated JLT devices.

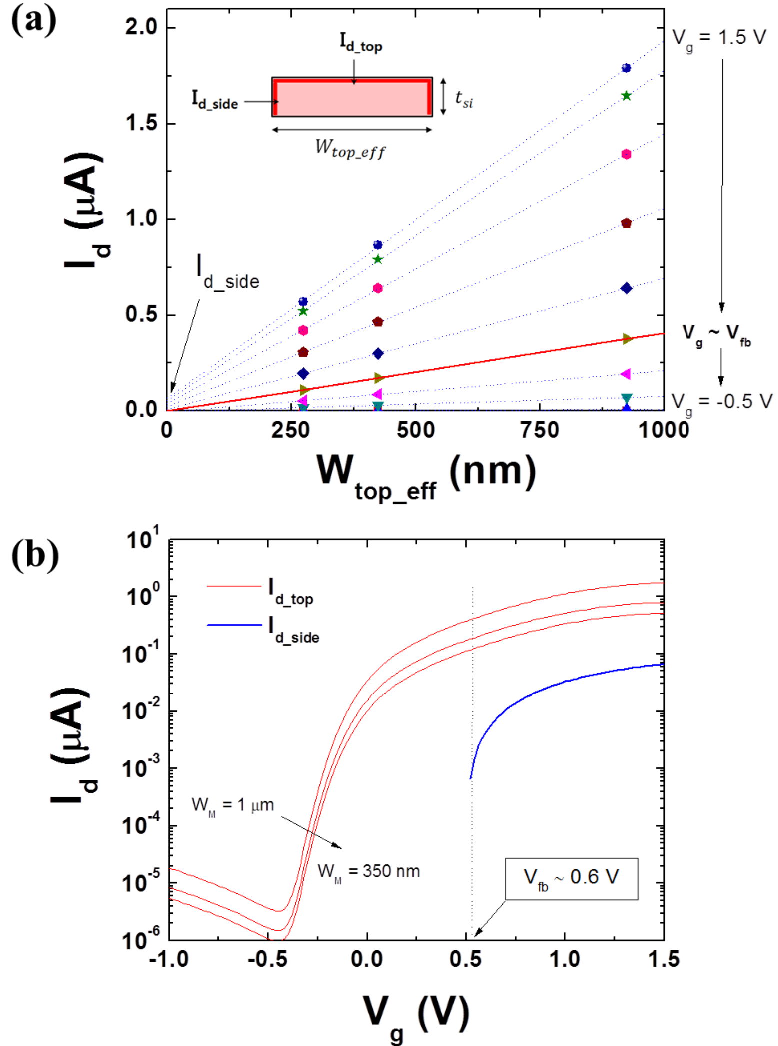
5.1.3.4 Sidewall accumulation current (I_{d_side}) and top side current (I_{d_top}) of JLT devices

The sidewall accumulation current component of Tri-gate JLT devices was separated from the linear relationship between the total drain current (I_d) and the obtained W_{top_eff} as [9-11]:

$$I_d(V_g) = I_{d_top_unit}(V_g) \cdot W_{top_eff} + I_{d_side}(V_g) \qquad (6)$$

where $I_{d_top_unit}$ and I_{d_side} represent the top side current per unit width, which contains top surface accumulation and bulk neutral channel, and the sidewall accumulation current component of JLT devices, respectively. The I_{d_side} for the whole V_g regime was extracted by a linear extrapolation of the total drain current, $I_d(V_g)$ with the W_{top_eff} to zero, as shown in Fig. 9(a). A very interesting feature was revealed on the behavior of the extracted I_{d_side} as plotted in Fig. 9(b). The I_{d_side} (V_g) of Tri-gate JLT devices is dramatically decreasing at near flat-band voltage, whereas, for typical inversion-mode (IM) transistors, this phenomenon was appearing at the conduction threshold (V_{th}) [9]. The abrupt decrease of I_{d_side} near V_{fb} in Tri-gate JLT devices can be explained by the fact that the bulk neutral conduction instead of the surface conduction dominates the JLT device operation under V_{fb}. Since, the I_{d_side} extraction method is based on the assumption that the total drain current of Tri-gate JLT devices mainly takes place at the interface between the gate oxide and surface of device Si, this explains why I_{d_side} vanishes below the flat band voltage. Therefore, it should be mentioned that one can estimate the V_{fb} position of JLT devices from a V_g point where the I_{d_side} is dramatically reduced.

Figure 9. (a) Total drain current (I_d) versus W_{top_eff} for the extraction of the sidewall accumulation current component (I_{d_side}) of Tri-gate JLT devices (targeted doping level: 1×10^{19} cm^{-3}). (b) The extracted top side drain current (I_{d_top}, red) and I_{d_side} (blue). The I_{d_side} was dramatically decreased at near V_{fb}. Devices are biased in the linear regime of operation with V_d = 50 mV.



5.1.4 Conclusions

The flat-band voltage (V_{fb}) and channel doping concentration (N_d) of Tri-gate Junctionless Transistors (JLT) were extracted from a new method, which is based on the fact that at V_{fb} condition, the top-effective width (W_{top_eff}) in accumulation mode should be equal to the effective width (W'_{eff}) of bulk neutral channel in partially depleted region. The extracted $V_{fb} \approx 0.61$ V and $N_d \approx 6.4\times10^{18}$ cm^{-3} were well consistent to those previously obtained from the derivative of transconductance (dg_m/dV_g) and Maserjian's function (Y_M). The 2D Poisson equation numerical simulation results also proved the validity of the new method. Moreover, the sidewall accumulation current component (I_{d_side}) of Tri-gate JLT devices, separated from the linear relationship between the total drain current (I_d) and the obtained W_{top_eff}, was dramatically decreased near the extracted V_{fb} position. Interestingly, this feature enables to estimate the flat band voltage position V_{fb} in JLT devices from the gate voltage point where the I_{d_side} is dramatically reduced.

5.2 New method for the extraction of bulk channel mobility and flat-band voltage in junctionless transistors

5.2.1 Introduction

Junctionless transistors (JLTs), recently considered as a possible candidate for the realization of sub 22 nm CMOS owing to their promising advantages, are based on bulk conduction operation [1, 2]. Although the heavily doped channel in JLT devices can allow enough drive current originating from the bulk conduction even near flat-band voltage (V_{fb}), further increased gate voltage ($V_g > V_{fb}$) creates accumulation channel at the interface between gate oxide and silicon (Si) channel [1, 2, 12]. Therefore, bulk conduction mobility (μ_{bulk}) and V_{fb} of JLT devices are key parameters revealing their unique electrical features different from typical inversion-mode (IM) transistors. This is the reason why the exact determination of μ_{bulk} and V_{fb} in JLT devices is a very important issue for a better understanding of their physical operation.

This chapter presents a new and simple method for the extraction of μ_{bulk} and V_{fb} in JLT devices. The principle of the new method is based on the reciprocal transconductance squared, $1/g_m(V_g)^2$, characteristics. The validity of the new method is proved by two-dimensional (2D) numerical simulation results and newly defined Maserjian's-like function with respect to g_m for JLT devices.

5.2.2 Device fabrication and experiment

For this study, N-type JLT devices with high-k/metal gate stack were fabricated at CEA-LETI on SOI wafers with 145 nm buried oxide (BOX) and a Si body of ≈ 9.4 nm. The effective doping concentration (N_d) on active channel regions of JLT devices was ≈ 0.8×10^{19} cm^{-3} [7]. An additional source/drain (S/D) implantation was performed for improving electrical performance by reducing access resistance. The current-voltage characteristics were recorded using HP4155a measurement unit. Moreover, FlexPDE 5.0 software was used for 2D Poisson equation numerical simulations.

5.2.3 Experimental results and discussion

5.2.3.1 Principle of the new method

For partially depleted regime ($V_{th} < V_g < V_{fb}$), the electron charge (Q_n) of JLT devices can be derived from the depletion approximation as follows [6]:

$$Q_n(V_g) = \left\lfloor q \cdot N_d \cdot t_{si} - \frac{q \cdot \varepsilon_{si} \cdot N_d}{C_{ox}} \left(\sqrt{1 - \frac{2(V_g - V_{fb}) \cdot C_{ox}^2}{q \cdot \varepsilon_{si} \cdot N_d}} - 1 \right) \right\rfloor \quad (1)$$

where q, t_{si}, ε_{si} and C_{ox} represent the electronic charge, Si body thickness, Si permittivity and oxide capacitance per unit area, respectively. Therefore, drain current (I_d) of JLT devices in ohmic regime can be given as:

$$I_d(V_g) = \frac{W}{L} \cdot \mu_{bulk} \cdot Q_n(V_g) \cdot V_d \qquad (2)$$

where W and L are effective channel width and length and V_d means drain voltage. Since, in the partial depletion region ($V_{th} < V_g < V_{fb}$), the channel resistance is relatively higher than the series resistance (R_{sd}), we hereafter neglect its influence in that regime. However, the longer JLT device can give better accuracy with equation 2, since it has much higher channel resistance and is not affected by the S/D implantation induced defects [13]. The transconductance (g_m) of JLT devices is also obtained by differentiation from I_d (equation 2) as:

$$g_m(V_g) = \frac{dI_d}{dV_g} = \frac{W}{L} \cdot \mu_{bulk} \cdot \frac{C_{ox}}{\sqrt{1 - \frac{2(V_g - V_{fb}) \cdot C_{ox}^2}{q \cdot \varepsilon_{si} \cdot N_d}}} \cdot V_d \qquad (3)$$

Finally, a linear function for gate voltage can be readily achieved through the inverse of transconductance squared ($1/g_m^2$) as:

$$\frac{1}{g_m(V_g)^2} = \frac{1}{\left(\frac{W}{L} \cdot \mu_{bulk} \cdot V_d \cdot C_{ox}\right)^2} - \frac{2}{\left(\frac{W}{L} \cdot \mu_{bulk} \cdot V_d\right)^2 \cdot q \cdot \varepsilon_{si} \cdot N_d}(V_g - V_{fb}) \qquad (4)$$

It is clear from equation 4 that μ_{bulk} and V_{fb} can be easily extracted from the slope and intercept of the linear function ($1/g_m^2$ vs V_g), respectively, since all other parameters such as W, L, C_{ox} and N_d are already known from the transfer length method (TLM) and Maserjian's function applied to capacitance data [7].

5.2.3.2 Experimental results for verifying the new method

The drain current, the corresponding transconductance and transconductance derivative (dg_m/dV_g) of JLT devices were plotted as a function of V_g as shown in Fig. 10. The two peaks in dg_m/dV_g plot are clearly different from IM transistors. The second peak (right-hand side) gives V_{fb} position of JLT device, while the first peak (left-hand side) means conduction threshold voltage (V_{th}) [7, 13]. Fig. 11 shows the corresponding $1/g_m(V_g)^2$ characteristics. A linear slope with gate voltage is distinctly observed around partial depletion regime ($V_{th} < V_g < V_{fb}$) investigated from Fig. 10. Interestingly, this

linear dependence was expected from equation 4. The μ_{bulk} of bulk channel in JLT device extracted from the slope in the $1/g_m^2$ vs V_g plot was ≈ 123 cm^2/Vs, which is fully consistent with bulk Si electron mobility value reported by C. Jacoboni et al. for the same doping level [14]. In addition, the V_{fb} of ≈ 0.6 V was extracted from a proper calculation with the intercept of the linear function. This value is also very close to that of ≈ 0.63 V from the second peak of dg_m/dV_g in Fig. 10.

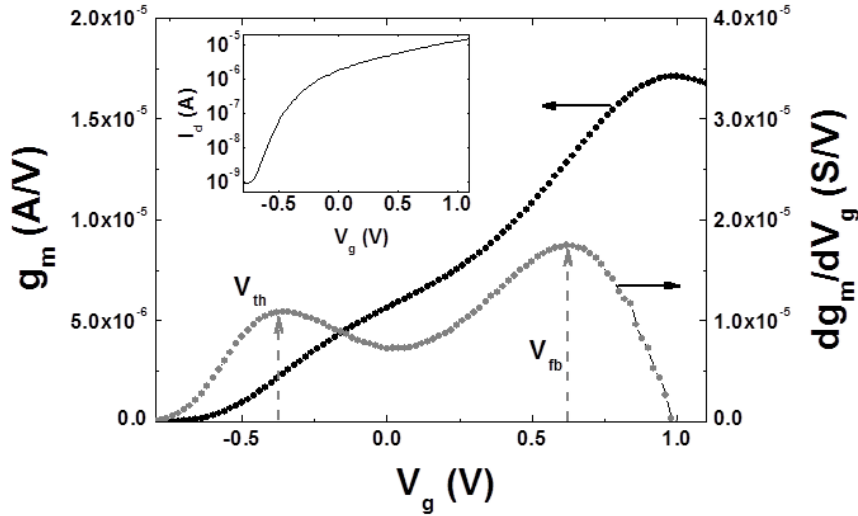


Figure 10. Drain current I_d (inset) of JLT device measured as a function of V_g, together with the corresponding transconductance g_m and derivative of transconductance dg_m/dV_g (V_d = 50 mV, W = L = 10 μm).

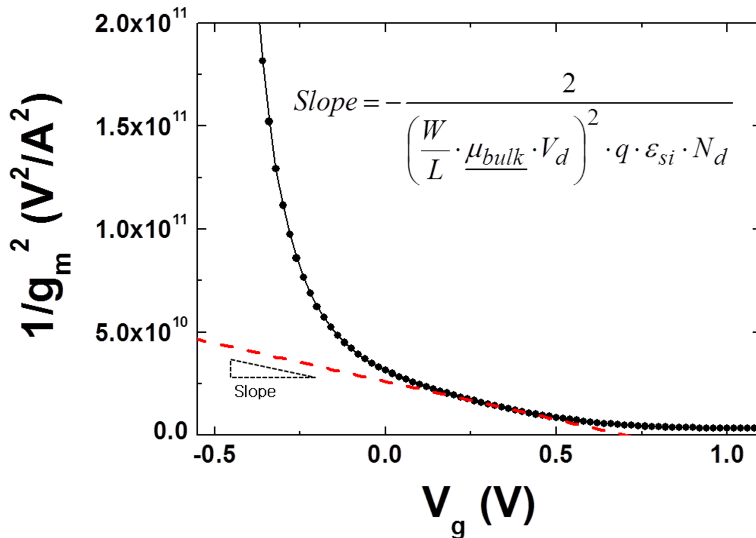


Figure 11. The inverse of transconductance squared $1/g_m(V_g)^2$ versus gate voltage for the extraction of μ_{bulk} and V_{fb} in JLT device (W = L = 10 μm).

5.2.3.3 2D numerical simulation for verifying the new method

The same procedure for the extraction of μ_{bulk} and V_{fb} was carried out with numerical simulation as shown in Fig. 12. In this simulation, the defined exact values of μ_{bulk} and V_{fb} are 150 cm^2/Vs and 0 V, respectively. A better linear behavior was obtained as shown in Fig. 12, compared to the experimental results in Fig. 11, since the μ_{bulk} in the measured results could be affected by the transverse electric field from gate bias, Coulomb scattering from charged defects in high-k dielectrics. Eventually, the parameter values extracted from the new method were $\mu_{bulk} \approx$ 149 cm^2/Vs and $V_{fb} \approx$ 0 V, which are very close to the exact values. This confirms the validity of the new method.

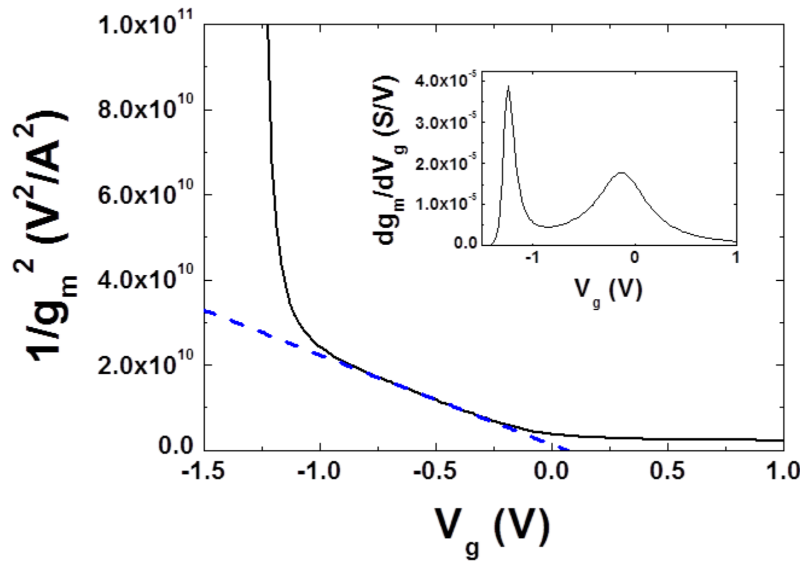


Figure 12. Same plot in Fig. 2 for the extraction of μ_{bulk} and V_{fb} in the simulated JLT device. Inset denotes derivative of transconductance dg_m/dV_g versus V_g.

5.2.3.4 Comparison with newly defined Maserjian's-like function for g_m of JLT devices

The transconductance of equation 3 can be also simply expressed as:

$$g_m = \frac{W}{L} \cdot \mu_{bulk} \cdot C_{gc} \cdot V_d \qquad (5)$$

where C_{gc} denotes gate to channel capacitance. Therefore, Maserjian's-like function for g_m in the JLT device can be newly defined as [15]:

$$Y_{M_gm} = \frac{1}{{g_m}^3} \cdot \frac{dg_m}{dV_g} \qquad (6)$$

Finally, μ_{bulk} in JLT devices can be calculated by an appropriate combination of the newly defined Y_{M_gm}, the conventional $1/C_{gc}^2$ vs V_g equation [16] and equation 5 as:

$$Y_{M_gm} = \frac{1}{\left(\frac{W}{L}\mu_{bulk}V_d\right)^2} \cdot \frac{1}{q\varepsilon_{si}N_d} \qquad (7)$$

It should be noted that, as for capacitance data, the transconductance Maserjian's-like function Y_{M_gm} is also independent of C_{ox}. The μ_{bulk} estimated from the partial depletion plateau-like region ($V_{th} < V_g < V_{fb}$) in the plot as shown in Fig. 13 was ≈ 125 cm^2/Vs, which is also well consistent to the value (≈ 123 cm^2/Vs) extracted from the new method in Fig. 11.

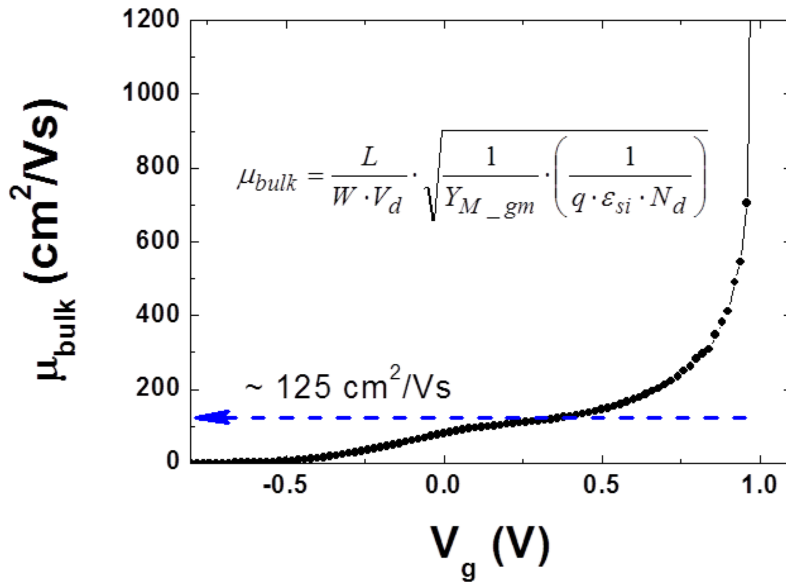


Figure 13. Bulk channel mobility μ_{bulk} extracted from newly defined Maserjian's-like function for g_m of JLT devices versus gate voltage.

5.2.4 Conclusions

The bulk channel mobility (μ_{bulk}) and flat-band voltage (V_{fb}) in junctionless transistors (JLTs) were successfully extracted from a new and simple method. The new method is based on a linear dependence of reciprocal transconductance squared, $1/g_m(V_g)^2$, characteristics for gate voltage in partial depletion regime ($V_{th} < V_g < V_{fb}$). The 2D numerical simulation results proved the validity of the new method. Moreover, the μ_{bulk} extracted using the newly defined Maserjian's-like function (Y_{M_gm}) for g_m of JLT devices also confirms its validity.

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Chapter 6

Conclusions

Junctionless transistors (JLTs) are currently in the spotlight as a possible candidate for the realization of sub 22 nm CMOS, owing to their promising advantages such as very simple structures without PN-junction, their operation principle based on bulk conduction. For electrical characterization with this JLTs, conventional parameter extraction methods and semiconductor device measurement technique were explained to provide theoretical and experimental backgrounds in chapter 1.

JLTs fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick BOX and ≈ 9 nm thick silicon have been extensively characterized with both nanowire-like geometries (W_M = 80 nm) as well as planar structures (W_M = 10 μm) in chapter 2. Interestingly, experimental results firstly brought evidence of the unique properties of JLT devices, such as the observation of two slopes in the Y-function and of two peaks in the dg_m/dV_{gf} and dC_{gc}/dV_{gf} plots, each of them being associated to the neutral and accumulation channel, respectively. We also extracted a broad range of electrical parameters such as conduction threshold (V_{th}), flat-band voltage (V_{fb}), drain induced barrier lowering (DIBL), low field mobility (μ_0) and doping concentrations (N_d). Their variation with gate length, doping level and back-gating was discussed, and a comparison with inversion mode transistors carried out.

Moreover, in chapter 2, the width dependent electrical behavior of tri-gate JLTs was investigated, experimentally. As decreasing the top-effective width (W_{top_eff}), the first shoulder on the normalized gate-to-channel capacitance characteristics $C_{gc}(V_g)$ was shrunk and the first peak on the normalized $dC_{gc}/dV_g(V_g)$ related to threshold voltage (V_{th}) was lowered in amplitude and its position was up-shifted, while the flat-band voltage (V_{fb}) location doesn't change. This is because the amount of bulk neutral channel in tri-gate JLT devices with a narrow structure is getting smaller as compared to the contributions of surface accumulation channels and the sidewall gate effect also strengthens. In addition, the trend of the effective mobility (μ_{eff}) in very narrow JLT devices (W_{top_eff} = 25 nm) was found

noticeably different from those in wide JLT devices, due to the strong sidewall gate effect. Finally, the sidewall gate effect was also proved through 2D Poisson equation numerical simulations, which were quite consistent to the experimental results.

In chapter 3, the electrical performances of the JLT devices were investigated under low temperature, in the range of 80 K to 350 K, and compared to those of inversion-mode (IM) transistors featuring the same structure, and fabricated by the same process except for channel doping level. From its overall temperature dependence, it was found that the low-field mobility (μ_0) of JLT devices was limited by phonon and neutral defect scattering for long gate lengths, whereas Coulomb and neutral defect scattering mainly dominated for short lengths, due to defects induced by the additional S/D implantation process, close to source/drain (S/D) regions. There was no significant difference between the temperature dependent variations of flat-band (V_{fb}) and threshold (V_{th}) voltages extracted by the transconductance derivative (dg_m/dV_g) in JLT devices. Moreover, the subthreshold swing (S) of JLT devices was only slightly higher than that of IM transistors, due to their reduced gate electrostatic control. However, the robustness of the subthreshold swing against short channel effects for the shortest gate lengths is a strong advantage of JLT devices. Therefore, it should be noted that JLT devices are more robust to short channel effect in terms of S fluctuations than IM transistors for future technology nodes.

The low-frequency (LF) noise of the JLT devices was investigated and compared to that of inversion-mode (IM) transistors with same structure in chapter 4. Interestingly, the LF noise behavior of the JLT devices was represented by a carrier number fluctuation model, even though the evidence of bulk conduction in the JLT devices was clearly proved by the flat-band voltage (V_{fb}) extracted from the derivative of the transconductance (dg_m/dV_g). These results are interpreted by the possible trapping-detrapping into slow traps in the gate oxide of mobile electrons that diffused from the bulk neutral channel or source/drain regions into the depletion region or that directly tunnel from the neutral regions to the traps. The extracted trap density of JLT devices was quite similar to that of IM transistors. This feature also supports our finding that the LF noise behavior of JLT devices is originated from carrier number fluctuations.

Chapter 5 introduces new method for the extraction of electrical parameters in JLTs. The flat-band voltage (V_{fb}) and channel doping concentration (N_d) of Tri-gate JLTs were extracted from a new method, which is based on the fact that at V_{fb} condition, the top-effective width (W_{top_eff}) in accumulation mode should be equal to the effective width (W'_{eff}) of bulk neutral channel in partially depleted region. The extracted $V_{fb} \approx 0.61$ V and $N_d \approx 6.4\times10^{18}$ cm^{-3} were well consistent to those previously obtained from the derivative of transconductance (dg_m/dV_g) and Maserjian's function (Y_M). The 2D

Poisson equation numerical simulation results also proved the validity of the new method. Moreover, the sidewall accumulation current component (I_{d_side}) of Tri-gate JLT devices, separated from the linear relationship between the total drain current (I_d) and the obtained W_{top_eff}, was dramatically decreased near the extracted V_{fb} position. Interestingly, this feature enables to estimate the flat band voltage position V_{fb} in JLT devices from the gate voltage point where the I_{d_side} is dramatically reduced.

In addition, the bulk channel mobility (μ_{bulk}) and flat-band voltage (V_{fb}) in JLTs were successfully extracted from other new and simple method. The new method is based on a linear dependence of reciprocal transconductance squared, $1/g_m(V_g)^2$, characteristics for gate voltage in partial depletion regime ($V_{th} < V_g < V_{fb}$). The 2D numerical simulation results proved the validity of the new method. Moreover, the μ_{bulk} extracted using the newly defined Maserjian's-like function (Y_{M_gm}) for g_m of JLT devices also confirms its validity.

Appendices

A. Nano device fabrication

B. Simple method for the fabrication of nanogap IDE arrays

C. AFM imaging of M13 bacteriophage on the functionalized substrate

D. Portable handmade electrometer

E. Labview programing for data acquisition

F. FlexPDE software

Appendix A. Nano device fabrication by using E-beam lithography with the homemade CAD program

The electrodes on bottom-up based materials, such as semiconducting nanowires (NWs), carbon nano-tube (CNTs) and graphene, can be selectively defined by using the electron beam (e-beam) lithography technique with the homemade CAD program. The procedure of the selective patterning technique is as followings [1-3]:

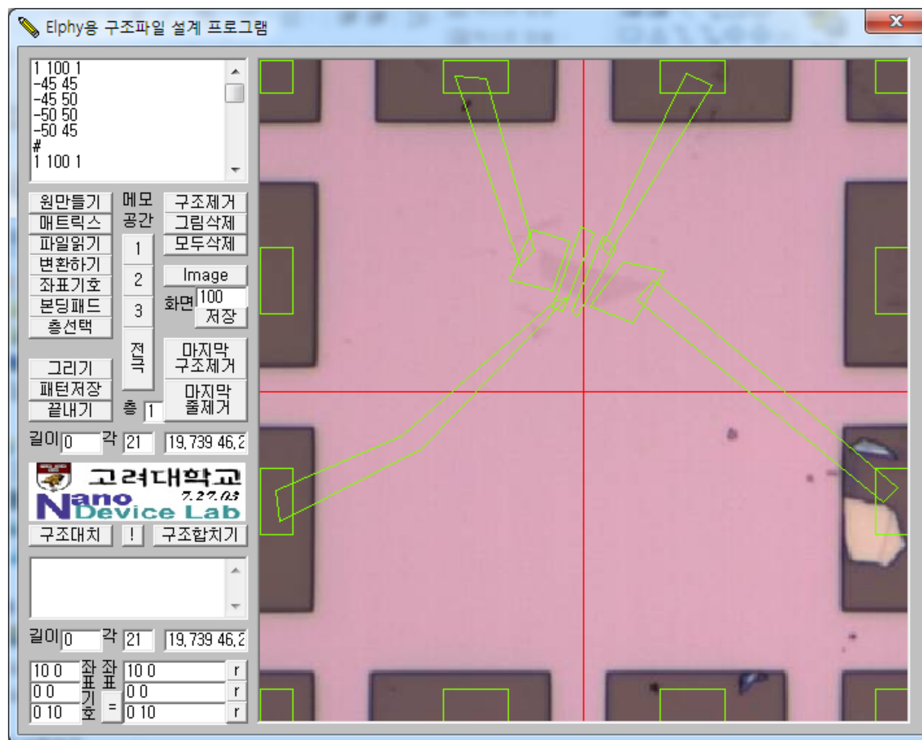


Figure 1. CAD design on the captured OM image (a graphene sample) by using homemade program.

1. Deposition of nano-materials on the substrate. 2. Optical microscope (OM) image capture of the deposited nano-materials with align-markers. 3. CAD design of the electrode pattern by the homemade program. 4. E-beam lithography and metallization for defining electrodes.

The method can allow the selective electrode patterning with any location of nano-material samples. Moreover, the usage of atomic force microscope (AFM) and scanning electron microscope (SEM) images instead of OM images gives very precise selective patterns.

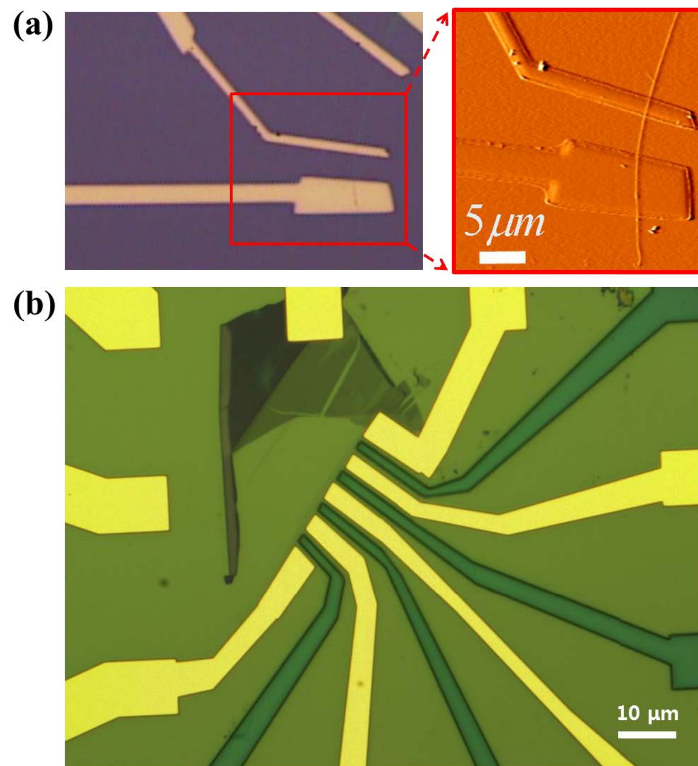


Figure 2. Fabricated nano devices by using E-beam lithography. (a) GaN NWs devices (b) Graphene transistors with top gate.

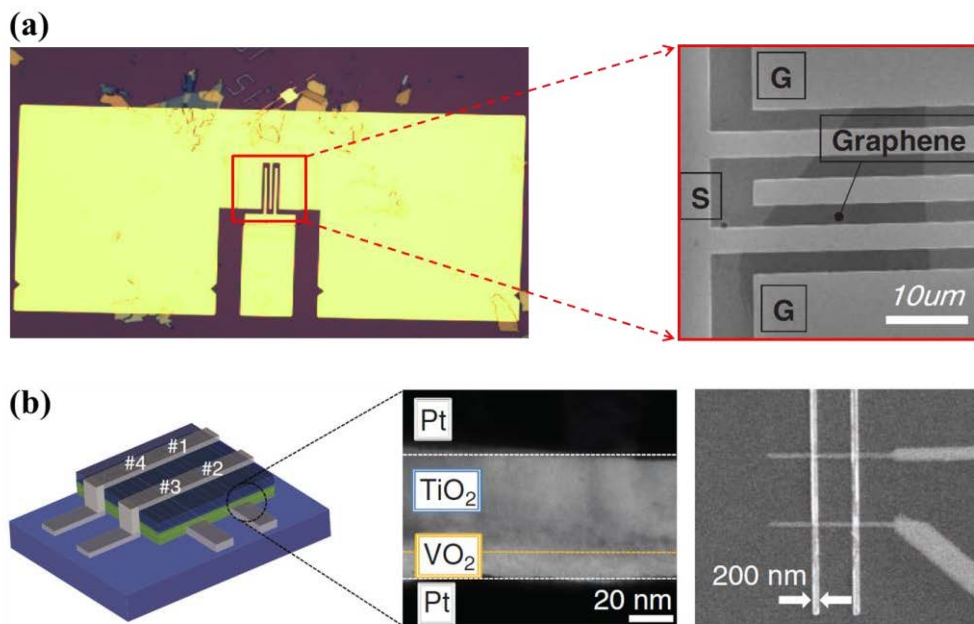


Figure 3. (a) Graphene device for radio frequency application, the E-beam lithography was used for a selective pattering on randomly deposited graphene. (b) Nano scale oxide RAM (TiO_2/VO_2 stacks) fabricated by E-beam lithography.

Appendix B. Simple method for the fabrication of nanogap IDE arrays

B.1 Tilted angle evaporation method for nanogap interdigitated electrode (IDE) arrays

Aluminum IDE array with a nano-scale gap was fabricated on 300-nm-thick silicon dioxide (SiO_2) thermally grown on heavily P-doped silicon (Si) substrate using two key processes. The first process involved e-beam evaporation at a given tilted angle based on anisotropy deposition due to the large mean free paths of gas molecules with good directionality. The second process was dry etching on the SiO_2 substrate. The electrode was separated vertically by the e-beam evaporation due to the tilted angle, which caused a shadow over the initially formed metal on a micro-scale level.

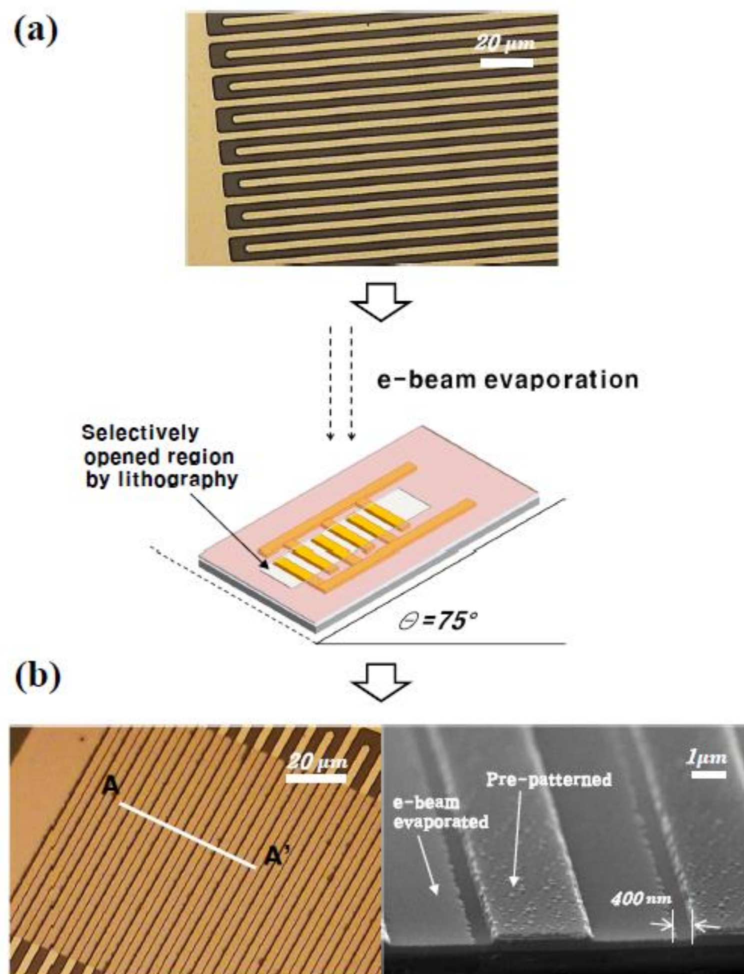


Figure 4. (a) The pre-patterned IDE arrays with 3 μm width and spacing. (b) The realized nanogap IDE arrays with 400 nm spacing between electrodes.

Conventional photolithography was used to define IDE patterns with a micro-scale width and a spacing of 3 μm. Inductively coupled plasma (ICP) metal etching was carried out to realize an aluminum IDE pattern with 300-nm thickness using a pre-patterned photoresist as a hard mask. Subsequently, a 100-nm-thick SiO_2 substrate was etched using a P-5000 instrument. Finally,

nanogap IDE arrays were fabricated by depositing an aluminum film with a thickness of 100 nm using e-beam evaporation with a tilted angle θ after opening the specific area on the micro-scaled IDE arrays by conventional lithography.

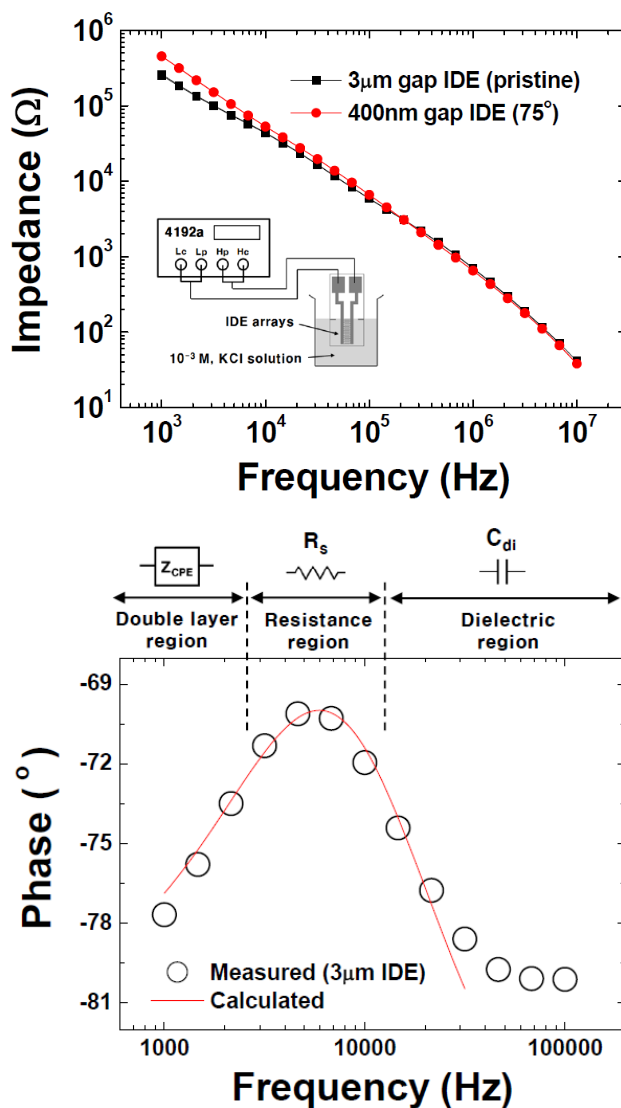


Figure 5. Impedance spectra (upper) and phase shifts (lower) of nano-gap IDE arrays.

B.2 Impedance characterization of nano-gap IDE arrays

The impedance characteristics of the nanogap IDE arrays in 10^{-3} M and 10^{-2} M KCl solution we re recorded using an HP4192a impedance analyzer in the range of 10^3 to 10^7 Hz at 10-mV

oscillator level. Typically, the impedance spectrum of interdigitated electrodes in electrolyte solution can be explained by three different regimes, which are the double-layer region, solution-resistance region and dielectric region, depending on the dominant circuit elements in the specific frequency range [4]. Z_{CPE} in the double-layer region dominates the impedance signal in the low-frequency range. The solution-resistance region can be observed in the intermediate frequency range; a peak point on phase signals corresponding to the plateau of the impedance magnitude can be identified in this region. If a solution has a higher resistance, the peak point on the phase appears in a relatively low-frequency region compared to that of a highly conductive solution. At high frequencies, this peak point on the phase vanishes again because the dielectric behavior of solution dominates the overall impedance signal.

Appendix C. AFM imaging of M13 bacteriophage on the functionalized substrate

The AFM images were obtained in air using Mobile S (Nanosurf AG, Switzerland) equipped with a 110 μm scanner in a non-contact mode. For the non-contact mode imaging, a commercial Si cantilever called the NCLR was used with a force constant of 48 N/m and a resonance frequency of 190 kHz provided by Nanoworld AG, Switzerland.

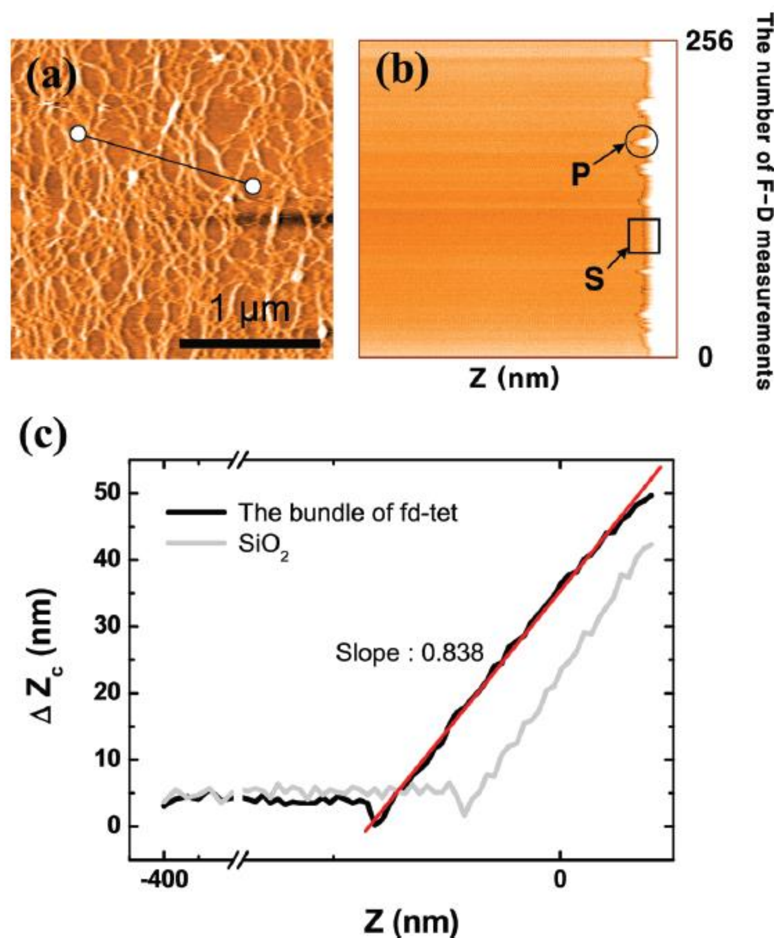


Figure 6. (a) AFM image of the bundle of fd phage in contact mode. (b) Force-distance (F-D) spectroscopy along a defined line in the X-Y plane. (c) The plotted F-D curve along the selected P and S regions.

In the case of the F-D spectroscopy, the fd phages on the substrates were characterized by scanning in a contact mode using the Si cantilever (CONTR) with a force constant of 0.13 N/m. At a specific line on the pre-scanned image, the F-D spectroscopy was investigated both on the SiO_2/Si substrates and on a selected specific region including a fd phage bundle at the same time. In the contact mode, the set point value of the applied force was maintained at 4 ~ 5 nN for good imaging without any damage to

the fd phage. The reliability and reproducibility of the force-distance spectra were first checked on the bare SiO_2/Si substrate with no fd phage and then confirmed by repeated measurements on the same area of the substrate with fd phage, where the spectral changes were not observed. The AFM data, including the sample images and the F-D curves, were analyzed with a Nanosurf Mobile S version v2-1-1-4 program.

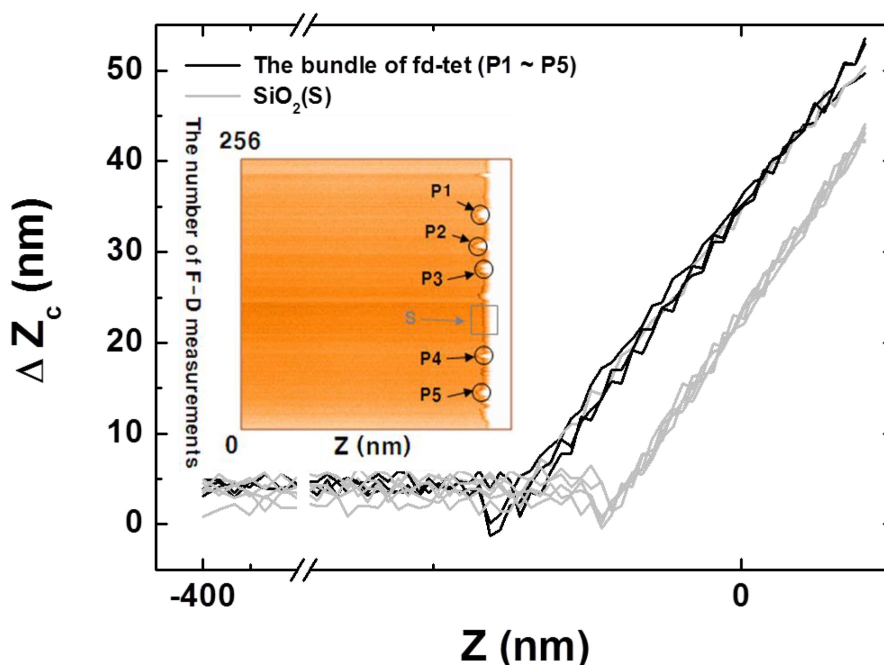


Figure 7. Uniform results indicating the reliability and the reproducibility of the F-D spectroscopy.

An effective spring constant of the bundle of fd phage was evaluated by the following equation reported by Arnoldi:

$$k_p = \frac{k_c s}{1-s},$$

which considers two linear springs in series, the AFM cantilever and the other materials such as cells and bacteriophage. k_c denotes the spring constant of the AFM tip, k_p represents the effective spring constant of the fd phage bundle and s is the slope of the linear regime of the F-D curve. The effective spring constant of the fd phage bundle was calculated to be 0.672 N/m, using the equation reported by Arnoldi with a cantilever spring constant of k_c = 0.13 N/m [5]. This value from the fd phage bundle is

bigger than that (0.04 ~ 0.05 N/m) of the bacteria cell.

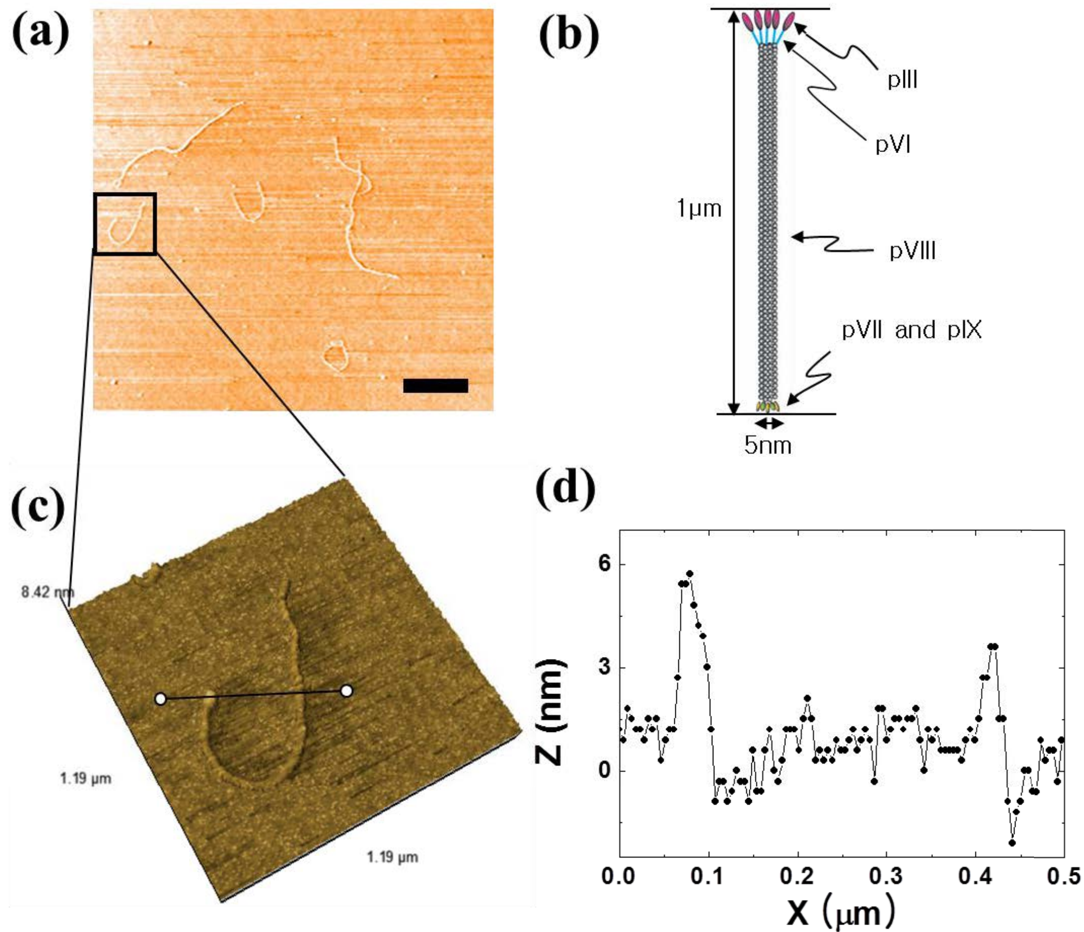


Figure 8. (a) Non-contact AFM image of the modified fd phage (p8DD type phage, displayed with double aspartic acid groups) and (c) the enlarged image in the same mode clearly showing the structure of the individual fd phage corresponding to (b) the expected schematics. The black scale bar represents 1 μm. (d) The height profile along the line in (c) showing the Z height values of 4 ~ 5 nm (in pVIII) and 6 nm (in pIII).

Appendix D. Portable handmade electrometer with DAQ, Pre-amplifier and Labview program

Portable handmade electrometer instrument controlled by personal computer (PC) was fabricated by using data acquisition board (DAQ), handmade Pre-amplifier (current to voltage) and Labview programing.

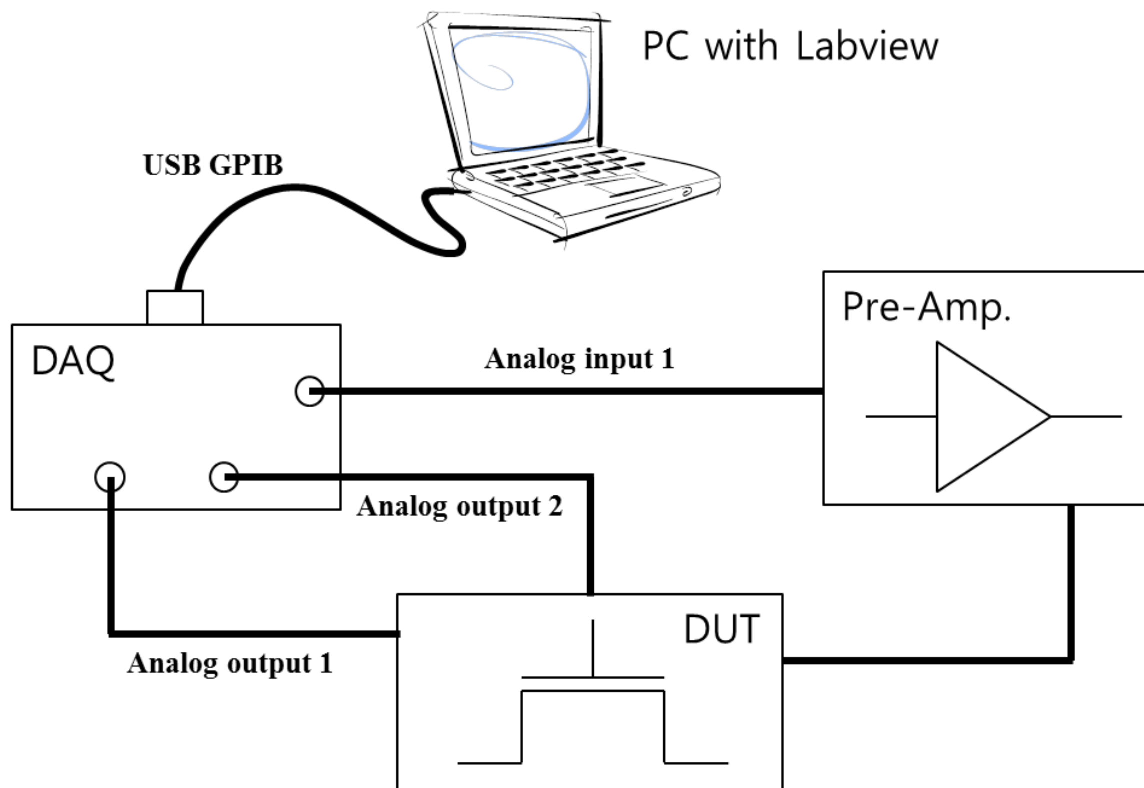


Figure 9. A schematic diagram of handmade electrometer with DAQ and Pre-amplifer (current to voltage).

OP-Amp (model: AD515A) with ultra-low offset current was used for the handmade pre-amplifier. DAQ (model: NI USB-6211) can provide voltage bias to a sample (DUT: device under test) through the analog output port. The current signal through a sample can be converted as voltage signal by the pre-amplifier. Finally, DAQ can read the converted voltage signal for further analysis. Proper Labview programing allows for PC to easily control the DAQ regarding the measurements for electrical characterization of samples.

Figure 10. Electrometer systems with NI-DAQ and handmade Pre-amplifier.

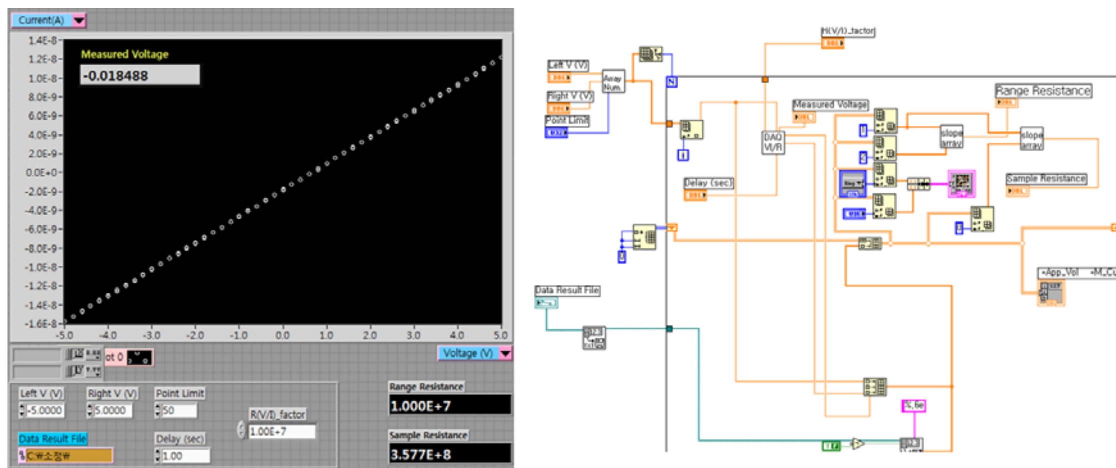
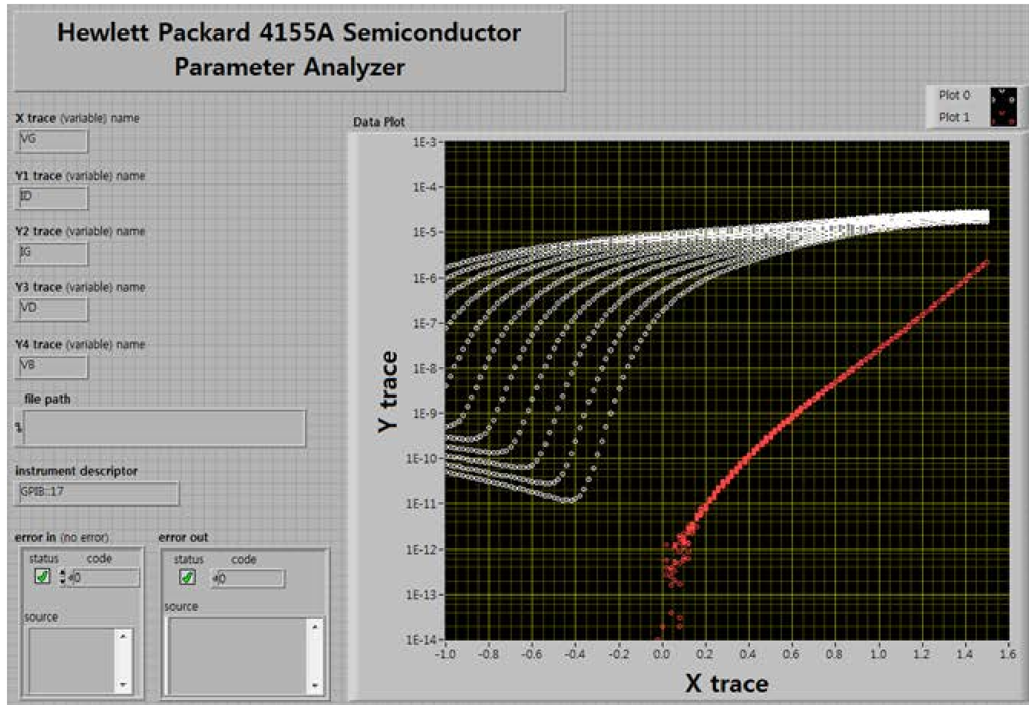
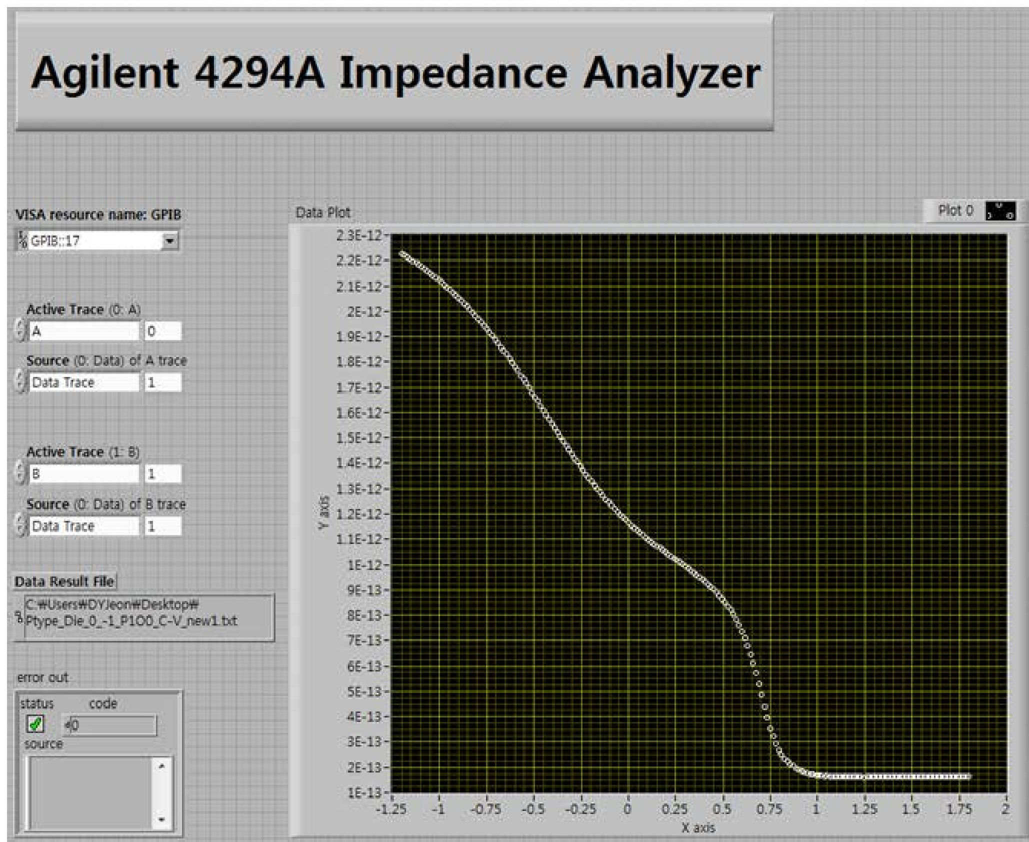


Figure 11. Labview programing and its test results for easy controlling of NI-DAQ.

Appendix E. Labview programing for data acquisition from instruments





Appendix F. FlexPDE software

FlexPDE is a numerical solver based on scripted finite element models (http://www.pdesolutions.com). The most frequently used script sections are as followings:

1. TITLE – Label for the works.

2. VARIABLES – Defined the dependent variables.

3. DEFINITIONS – useful parameters, relationships or functions could be defined.

4. EQUATIONS – To be solved a partial differential equation with the defined variables.

5. INITIALVALUES – starting values for nonlinear or time-dependent problems.

6. BOUNDARIES – the desired geometry for the solving by numerical method.

7. PLOTS – the graphical outputs (CONTOUR, SURFACE, ELEVATION or VECTOR plots).

For instance, a simple example on a square geometry might also look like as below:

****

```
TITLE 'A simple example'
VARIABLES
  u
DEFINITIONS
  k=3
EQUATIONS
  div(k*grad(u))=0
BOUNDARIES
  region 1
  start(0,0) line to (1,0) to (1,1) to (0,1) to finish
PLOTS
  contour(u)
  vector(k*grad(u))
END
```

****

In a FlexPDE script, proper designation of boundary condition is very important to the solving of problems and the primary types of the boundary conditions are VALUE and NATURAL.

The VALUE boundary condition denotes the value at the boundary of the domain. On the other hands, the NATURAL boundary condition specifies a flux at the boundary of the domain.

In the presented above example, we may add the VALUE with fixed values and the NATURAL with zero-flux conditions as follows:

```
********************************************************************************
        BOUNDARIES
            region 1
            start(0,0)
            value(u) = 0        line to (1,0)
            natural(u)=0        line to (1,1)
            value(u)=1          line to (0,1)
            natural(u)=0        line to finish
********************************************************************************
```

In this thesis, FlexPDE was used for confirming of the sidewall gate effect (chapter 2) and the verification of the suggested new methods (chapter 5) in JLT devices with below key theoretical equations:

```
…
DEFINITIONS
   Vfb=-kT*ln(ni^2/Ng/Nd)          { Flat band voltage }
   E=-grad(V)                      { Electric field }
   n=R*n0*exp(V1/kT)               { Electron concentration in a field }
   Qn=q*INTEGRAL(n,2)              { Electron charge density, INTEGRAL(integrand, region) }
   Cox=epsox/tox*(2*tsi+W)         { 2D-GateOxide capacitance }
   Gd0=integral(mun*q*Nd,2)/L      { Conductance, surface integral means t*W }
…
EQUATIONS
   V: div(eps*grad(V))=s           { s means whole charges }
…
BOUNDARIES
   region 2                        { Silicon }
   eps=epssi
   s=q*(R*n0*exp(V/kT)-R*p0*exp(-V/kT)-Nd) { Whole charges (n, p, space charges) in Si }
   n=R*n0*exp(V/kT)
   p=R*p0*exp(-V/kT)
   s1=q*(R*n0*exp(V1/kT)-R*p0*exp(-V1/kT)-Nd)
   n1=R*n0*exp(V1/kT)
   mu=mun/(1+Emag/Ec*0)
   mu1=mun/(1+Emag1/Ec*0)
…
```

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List of publications

A. Published journals

B. Conference proceedings

C. Conferences

D. Patents

A. Published journals

1. Min-Kyu Joo, Mireille Mouis, **Dae-Young Jeon,** Gyu-Tae Kim, Un Jeong Kim and Gérard Ghibaudo, “Static and low frequency noise characterization of N-type random network of carbon nanotubes thin film transistors”, Journal of Applied Physics, 114, 154503 (2013).

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국문초록

본 논문에서는 현재 차세대 소자로 주목 받고 있는 Junctionless 트랜지스터의 전기적인 특성을 다양한 온도 범위에서 (80 K ~ 350 K) 변화하는 소자의 동작 메커니즘을 중심으로 깊이 있게 연구하였다. 또한, Junctionless 트랜지스터의 저주파 잡음 특성이 기존의 Inversion-mode 트랜지스터와도 비교/분석 되었고, Junctionless 트랜지스터에 적용할 수 있는 새로운 개념의 전기적 변수 추출 방법들이 제안 되었으며, 제안된 방법들은 이차원 수치 모사 방법을 통해 그 신뢰성이 확인 되었다.

Junctionless 트랜지스터의 동작은 기존의 트랜지스터와는 달리 완전 공핍 모드, 부분 공핍 모드 그리고 표면 축적 모드 이렇게 세 가지로 요약될 수 있다. 문턱전압, 평탄밴드 전압, DIBL, 저전계 전하 이동도 등의 추출된 소자 변수들은 Junctionless 트랜지스터의 독특한 전기적 특성을 잘 보여주었다. 또한, Junctionless 소자의 폭이 작아 질수록 변화하는 전기적 특성이 문턱 전압과 평탄밴드 전압을 중심으로 심도 있게 분석되었다.

길이가 긴 채널 구조에서는, 저전계 전하 이동도가 phonon과 neutral defects에 주로 영향을 받는 반면에, 짧은 채널 구조에서는 Coulomb과 neutral defects이 주요하게 영향을 미쳤다. 이는 접촉저항을 줄여 소자의 성능을 향상시키기 위한 S/D implantation 공정에 의해 생성된 결함의 영향이라고 예상된다. 그리고 Junctionless 소자의 문턱전압, 평탄밴드전압, subthreshold swing (S) 값의 온도 의존성이 논의 되었다.

Junctionless 트랜지스터의 동작 메커니즘이 기존의 트랜지스터와 확연히 다름에도 불구하고, 그것의 저주파 잡음 특성이 carrier number fluctuation 모델로 잘 설명되었고, 추출된 trap 농도도 Inversion-mode 소자에서의 농도와 매우 비슷하였다. 공핍층에 남아 있는 소수의 자유 전하들이 절연 막에 위치해 있는 slow trap과 상호 작용을 일으키고, 결과적으로 이러한 상호 작용이 채널의 요동을 일으킬 수 있다.

제안된 새로운 소자 변수 추출방법은, Junctionless 트랜지스터의 평탄밴드전압, 도핑농도, 전하 이동도를 정확하고, 간단하게 추출하였다. 추출된 소자 변수 값들은 동일한 소자 조건에서 기존의 방법으로 추출된 값들과 매우 유사했고, 제안된 방법은 이차원 수치모사 방법으로도 그 신뢰성이 확인 되었다.

주요어: Junctionless 트랜지스터, 소자변수 추출방법, 수치모사방법, 저온특성, 저주파잡음.

Résumé en français

Introduction :

L'invention du premier transistor à Bell lab's, dans le groupe de W. Shockley, en 1947 a été suivie d'une ère de développement des circuits intégrés (IC). Depuis plusieurs dizaines d'années, la dimension critique des transistors métal/oxyde/semi-conducteurs (les transistors MOS), la longueur physique de la grille, a diminué à un rythme régulier. Cette évolution, motivée par des raisons économiques, a été anticipée par G. Moore, et est de ce fait connue sous le nom de "loi de Moore". La dimension de grille a d'ores et déjà été réduite de plus de 2 ordres de grandeur et, dans son édition 2012, l'association ITRS prédit qu'elle décroîtra encore, de 22nm en 2011 à environ 6nm en 2026 [1]. Toutefois, cette réduction des dimensions fait apparaître un certain nombre d'effets secondaires qui altèrent le fonctionnement idéal des transistors MOS [2].

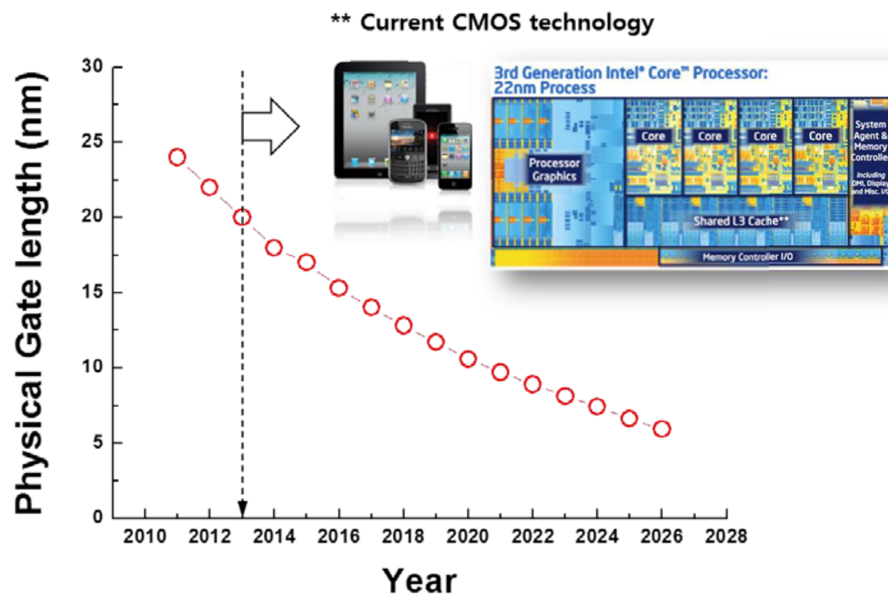


Figure 1. Illustration de l'évolution annuelle des dimensions pour les technologies logiques haute performance [1].

De nombreuses améliorations ont dû être apportées pour surmonter ces effets, dits de canal court, et améliorer les performances, notamment en ce qui concerne le profil de dopage de canal, l'empilement de grille, la fabrication des contacts de source et de drain (S/D), l'ingénierie des contraintes mécaniques ou l'utilisation de matériaux de canal alternatifs au silicium [1-3]. En parallèle, l'approche

dite *bottom-up*, qui s'appuie sur des processus d'auto-organisation, de façon analogue à la biologie, offre d'autres possibilités qui peuvent potentiellement apporter des solutions pour l'ère pos-silicium, afin de résoudre certains des défis technologiques et fondamentaux que l'industrie actuelle (dite *top-down*) commence à rencontrer [4]. Parmi les matériaux qui se prêtent à l'approche bottom-up, mentionnons par exemple les nanofils semi-conducteurs (NWs), les nanotubes de carbones (CNTs,) et les nanorubans de graphène.

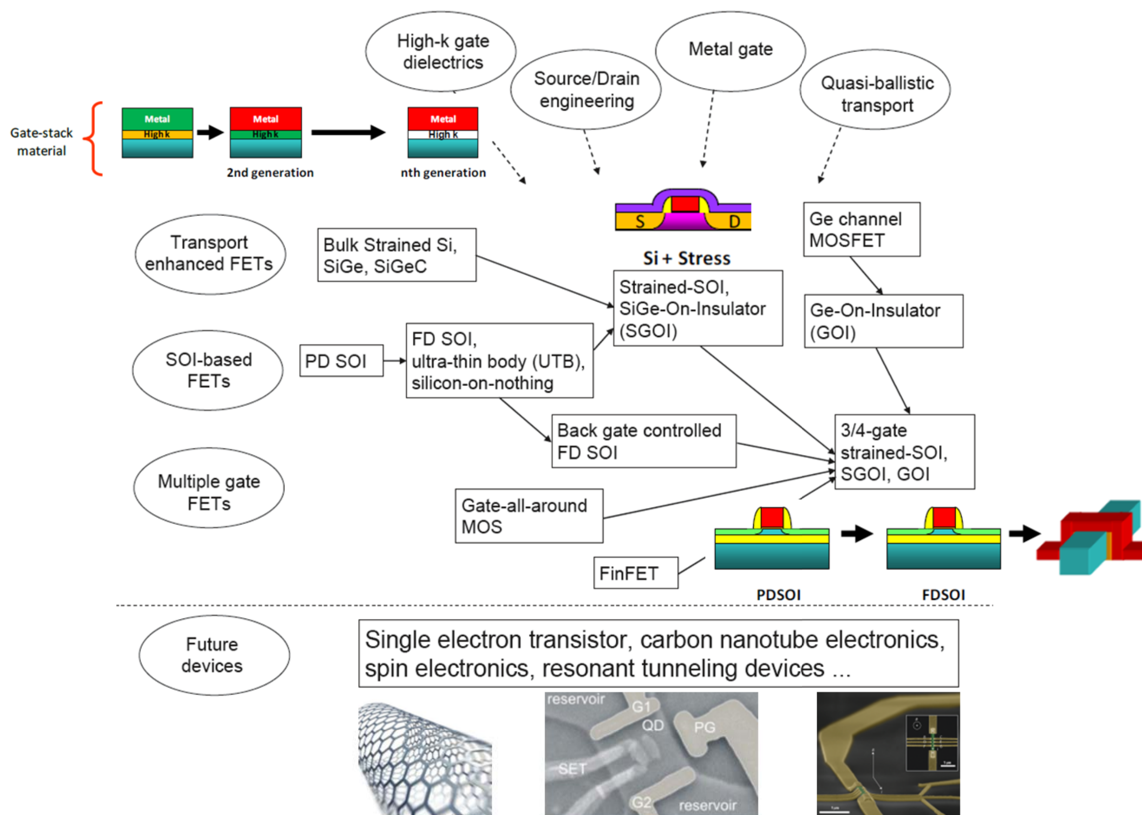


Figure 2. Vue d'ensemble de l'évolution des technologies CMOS développées pour poursuivre la loi de Moore [3].

La figure 2 montre l'évolution des technologies CMOS telle qu'elle est appréhendée actuellement. Dans cette perspective, le transistor sans jonction (JLT) [5], parfois appelé également résistance commandée pour une utilisation à faible tension ou transistor sans jonctions à accumulation, fait l'objet de nombreuses études. Il présente plusieurs avantages, liés notamment à sa simplicité de réalisation technologique. Il peut en effet fonctionner avec un dopage uniforme sans jonctions PN au niveau des contacts S/D [5-7]. Certains des défis liés à la miniaturisation du transistor MOS, comme la nécessité de réaliser des jonctions ultra-minces, de faible résistance de contact, avec des gradients de concentrations extrêmement abrupts, sont ainsi éliminés.

Dans un transistor MOS classique l'état OFF est obtenu lorsque la barrière à la jonction source/canal

bloque l'injection des porteurs tandis que l'état ON est obtenu lorsque la polarisation de grille permet d'abaisser suffisamment cette barrière pour permettre la formation d'un canal d'inversion. Dans les JLTs, l'état OFF est obtenu lorsque le canal est entièrement déserté par la grille. Un fonctionnement normally-OFF peut être obtenu en réglant le travail d'extraction du métal de grille vis à vis du canal. Cet ajustement n'est devenu possible que récemment, avec la fabrication de films SOI de très faible épaisseur qui peuvent être effectivement désertés, même lorsqu'ils sont très dopés, pour des valeurs réalistes de travail d'extraction. Lorsqu'on polarise la grille (tension V_g), le canal passe de complètement déserté (pas de conduction) à :(1) un régime partiellement déserté en surface et neutre en volume, où c'est l'épaisseur du canal qui est contrôlée par la grille, puis à (2) un régime d'accumulation où un canal d'accumulation, contrôlé par la grille, se forme en surface, le reste du film restant neutre. La limite entre ces deux régimes est définie par la tension de bandes plates V_{fb}, pour laquelle le champ électrique perpendiculaire au canal est nul, avec un canal neutre qui occupe toute l'épaisseur du film. Du fait de son principe de fonctionnement, le JLT a été présenté comme moins exigeant en termes d'épaisseur du diélectrique de grille, de variabilité de la longueur effective de grille ou de dégradation de la mobilité par le champ transverse. De plus, s'appuyant sur une conduction en volume, il est censé présenter un bruit à basse fréquence (LFN) moins élevé [8].

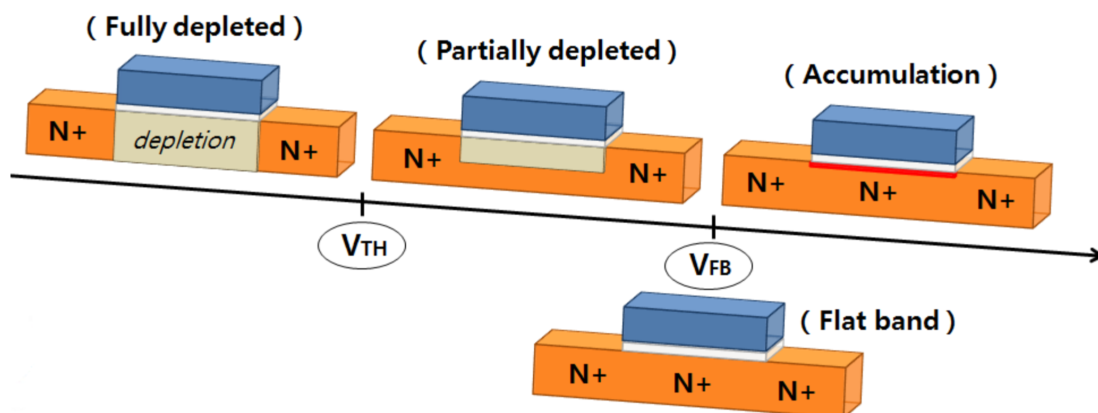


Figure 3. Schéma montrant les différents modes de fonctionnement du JLT, selon la tension appliquée sur la grille (ici, à faible tension de drain).

Toutefois, les JLT présentent quelques défauts: dégradation de mobilité par la forte concentration de dopants dans le canal, réduction du contrôle par la présence d'une zone partiellement désertée sous la grille, fluctuations de tension de seuil associées aux fluctuations de l'épaisseur du film de silicium ou de la distribution des atomes dopants dans le canal [8,9]. Néanmoins, leur simplicité de fabrication peut en faire un candidat crédible pour les technologies sub-22nm.

Cette thèse a pour objectif d'étudier en détail les performances des transistors JLTs, en tant que

candidat pour la poursuite de la loi de Moore, par le biais de diverses méthodes de caractérisation électrique. Nous avons de plus fait évoluer les méthodes d'extraction de paramètres pour les adapter au mode de fonctionnement particulier du composant. Ces nouvelles méthodologies ont été validées par simulation numérique.

Les travaux présentés dans cette thèse ont été obtenus en grande majorité à l'IMEP-LAHC, avec le support du 7ème PCRD de la commission européenne, dans le cadre du projet SQWIRE (FP7/ICT/CSA n° 257111). Le CEA/LETI nous a fourni les transistors JLT dans le cadre de ce projet. Ceux-ci avaient été fabriqués sur de substrats SOI (100) avec un oxyde enterré (BOX) de 145nm et un film de silicium (Si-body) aminci jusqu'à une épaisseur de ≈ 9.4 nm. Il s'agissait de transistors de type N. L'implantation de canal a été effectuée avec du phosphore, avant la formation de la grille, avec une valeur cible de 1×1019 cm-3 ou de 2×1019 cm-3, selon les échantillons, pour le dopage de canal. Après l'étape de lithographie optique (à 193nm), la largeur de canal a été réduite par gravure ionique réactive (RIE). La grille *high-κ* était constituée d'un empilement HfSiON/ TiN/ Si polycristallin. L'épaisseur équivalente d'oxyde (EOT) était de 1.2 nm. Dans cette technologie, une implantation supplémentaire, de même type que l'implantation de canal, est réalisée pour réduire les résistances d'accès des zones de source et de drain et améliorer ainsi les performances électriques.

Caractérisation électrique des transistors sans jonctions.

Extraction de paramètres à partir des caractéristiques statiques

Une des techniques d'extraction de paramètres utilisée pour les transistors MOS est la méthode Y qui permet en particulier d'extraire de façon cohérente les valeurs de la mobilité et de la tension de seuil sans perturbation par la présence éventuelle de résistances parasites d'accès. Cette méthode s'appuie sur le fait que, dans les transistors à inversion (IM), la fonction $Y = I_d \big/ \sqrt{g_m}$ est une fonction linéaire de la tension de grille en régime d'inversion (au dessus de la tension de seuil). Nous avons appliqué cette méthode au JLT (Fig. 4). On observe alors deux zones linéaires dans la fonction Y, l'une, de pente S_{Y1}, correspondant au régime d'accumulation, l'autre, de pente S_{Y2}, correspondant au régime de désertion (Fig. 4-c). On observe également deux pics sur les courbes dg_m/dV_{gf}. Le premier pic est localisé au niveau de la tension de seuil (V_{th}), c'est à dire au passage du régime complètement déserté à la conduction en volume, tandis que le second pic est localisé au niveau de la tension de bandes plates (V_{fb}), c'est-à dire à la transition entre conduction en volume et accumulation en surface. Ces pics ne sont toutefois discernables que pour les canaux longs, probablement du fait de la dégradation de mobilité et du rôle accru des résistances d'accès dans les canaux courts.

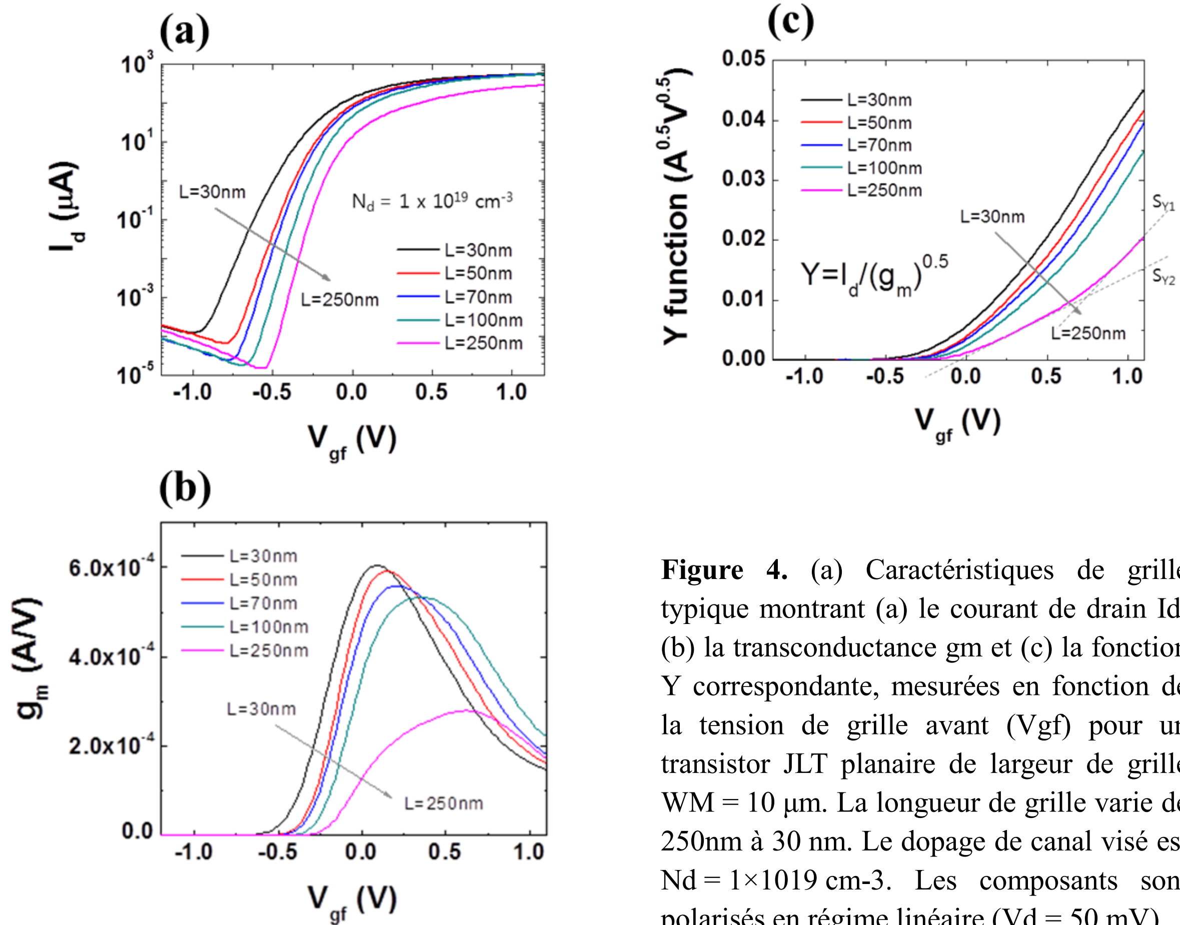


Figure 4. (a) Caractéristiques de grille typique montrant (a) le courant de drain Id, (b) la transconductance gm et (c) la fonction Y correspondante, mesurées en fonction de la tension de grille avant (Vgf) pour un transistor JLT planaire de largeur de grille WM = 10 µm. La longueur de grille varie de 250nm à 30 nm. Le dopage de canal visé est Nd = 1×1019 cm-3. Les composants sont polarisés en régime linéaire (Vd = 50 mV).

Nous avons comparé la tension de seuil extraite par la fonction Y (V_{ty}) aux valeurs obtenues par d'autres méthodes, notamment par extrapolation linéaire des caractéristiques de transfert (V_{text}), par le maximum de la dérivée de la transconductance (V_{tdgm}) et en utilisant une densité de courant sous le seuil de référence (V_{tcc}). Pour V_{text} l'extrapolation a été faite à la tension de seuil où la transconductance est maximale. La tension V_{ty} a quant-à-elle été extraite en régime d'accumulation, le régime intermédiaire de désertion partielle n'étant pas toujours aisé à localiser. Enfin, c'est le premier pic de dg_m/dV_{gf} qui a été utilisé pour extraire V_{tdgm}, tandis que le courant de référence, normalisé par le rapport L_M/W_M, a été pris égal à 10^{-7} A pour l'extraction de V_{tcc}. La comparaison de ces différentes définitions de la tension de seuil est présentée sur la Fig. 5 pour toute la gamme de longueurs de grille. On observe dans tous les cas une décroissance de la tension de seuil à faible longueur de grille. Ce "roll-off" est dû aux effets de canal courts. La tension V_{text} est la moins informative, parce qu'elle est affectée par la dégradation de mobilité, qu'elle est très sensible à la présence de résistance d'accès, et enfin parce qu'il est difficile de se positionner dans le bon régime pour l'extrapolation. Les tensions V_{tdgm} et V_{tcc} fournissent une meilleure évaluation de V_{th} dans la mesure où, pour V_{tdgm}, les pics sur la dérivée de la transconductance permettent de décorréler de façon assez précise V_{th} and V_{fb}. Ces techniques sont également moins sensibles à la dégradation de mobilité à faible longueur de canal.

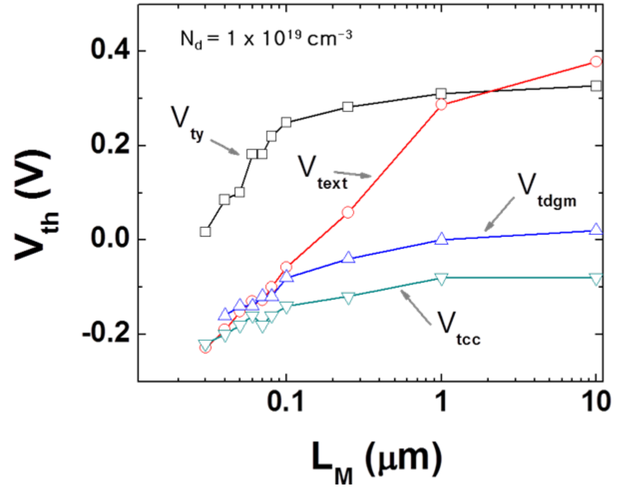


Figure 5. Valeurs de la tension de seuil (V_{th}) extraite par différentes techniques en fonction de la longueur de grille. L'extraction a été faite par la méthode Y en inversion (V_{ty}), par extrapolation linéaire de la caractéristique de transfert (V_{text}), par le maximum de la dérivée de la transconductance (V_{tdgm}) et par référence à une densité de courant sous le seuil donnée (V_{tcc}).

La figure 6 montre la variation de la mobilité à faible champ transverse (μ_0) et de la mobilité d'effet de champ maximum (μ_{femax}) en fonction de la longueur effective de canal (L_{eff}) pour des transistors JLT dont le canal a été dopé à 1×10^{19} cm^{-3} ou à 2×10^{19} cm^{-3}. La mobilité faible champ a été extraite à partir du carré de la pente de la fonction Y, $(dY/dV_{gf})^2$, dans la gamme de tensions de grille où la fonction Y est linéaire, c'est-à-dire ici en régime d'accumulation grâce à l'expression [10]:

$$\left(\frac{dY}{dV_{gf}}\right)^2 = \frac{W}{L}\cdot C_{ox}\cdot \mu_0 \cdot V_d \qquad (1)$$

La mobilité à effet de champ a quant à elle été extraite au maximum de grâce à l'équation 2 ci-dessous. Sa valeur n'est toutefois fiable que pour les canaux longs. En canal court, elle est artificiellement dégradée par la résistance d'accès R_{SD}.

$$\mu_{fe\max} = \frac{g_{m_\max}\cdot L}{W\cdot C_{ox}\cdot V_d} \qquad (2)$$

Les mobilités μ_0 et μ_{femax} ne prennent des valeurs similaires qu'en canal long (Figure 6). Elles sont toutes deux dégradées lorsque le dopage de canal est plus élevé, ce qui est cohérent avec une augmentation des interactions avec les dopants ionisés. De plus, elles montrent toutes les deux une dégradation de mobilité à faible longueur de canal. Cette dégradation apparait pour des longueurs de grille plus grandes pour μ_{femax}, vraisemblablement, comme nous l'avons dit plus haut, du fait de la sensibilité de cette méthode d'extraction à la présence de résistances série. Notons que la valeur de μ0 extraite en canal long, qui vaut ≈ 130 cm^{2}V^{-1}s^{-1} pour un dopage de 1×10^{19} cm^{-3} et ≈ 100 cm^{2}V^{-1}s^{-1} pour un dopage 2 fois plus élevé de 2×10^{19} cm^{-3}, est tout à fait comparable aux valeurs de mobilité électronique mesurées dans du silicium massif dopé par *Jacoboni et al.* dans la même gamme de dopages [11].

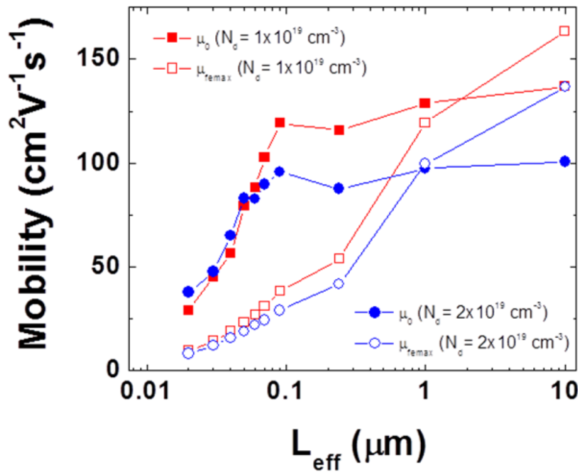


Figure 6. Evolution avec la longueur de grille Leff de la mobilité à faible champ transverse (μ_0, symboles pleins) et de la mobilité d'effet de champ maximum (μ_{femax}, symboles vides) extraites pour des transistors JLT larges (W_M = 10 µm) pour deux valeurs du dopage de canal: (1×10^{19} cm^{-3} courbes rouges) ou (2×10^{19} cm^{-3}, courbes bleues)

Nous avons également étudié l'abaissement de barrière source/canal sous l'effet de la tension de drain (DIBL) en comparant de ce point de vue des transistors JLT avec des transistors à inversion dans le cas de structures étroites dont le canal peut être considéré comme un nanofil (W_M = 80 nm i.e. $W_{eff} \approx$ 20 nm). Le DIBL (noté λ) a été obtenu comme le rapport entre la sensibilité du courant de drain aux variations de tension de drain (g_{d_sat}) et sa sensibilité aux variations de tension de grille (g_{m_sat}) en un point de polarisation donné [12]:

$$\lambda = \left[\frac{d\ln(I_d)}{dV_d} \Big/ \frac{d\ln(I_d)}{dV_g} \right] = \frac{g_{d_sat}}{I_d} \Big/ \frac{g_{m_sat}}{I_d} \qquad (3)$$

où g_{d_sat} et g_{m_sat} représentent la conductance de sortie et la transconductance en régime de saturation du courant. L'équation (3) a l'avantage de définir le DIBL dans tous les régimes de fonctionnement, y compris sous le seuil, et de s'affranchir des problèmes d'extraction de V_{th} [12]. La variation du DIBL en fonction de la longueur effective de canal est reportée sur la figure 7-b sur toute la plage de fonctionnement du JLT, depuis le régime sous le seuil jusqu'u régime de bandes plates puis d'accumulation. Les valeurs obtenues dans un transistor à inversion de même structure sont données sur la figure 7-c. Près du seuil, on observe des valeurs similaires pour les deux types de transistors (JLT et IM). Pour les canaux longs, le DIBL est légèrement plus faible pour les JLTs mais il se dégrade plus vite et les valeurs deviennent similaires pour les canaux les plus courts. Les différences les plus significatives apparaissent à fort V_{gf}. Les valeurs plus élevées obtenues pour les JLT sont probablement une conséquence de la présence du canal neutre, qui reste présent et est mal contrôlé par la grille, une fois que le régime d'accumulation est atteint (alors que le silicium est entièrement déserté sous le canal d'inversion des transistors IM). Cette conduction parasite en volume expliquerait un moindre contrôle par la grille et une plus grande sensibilité aux variations de tension de drain dans ce régime.

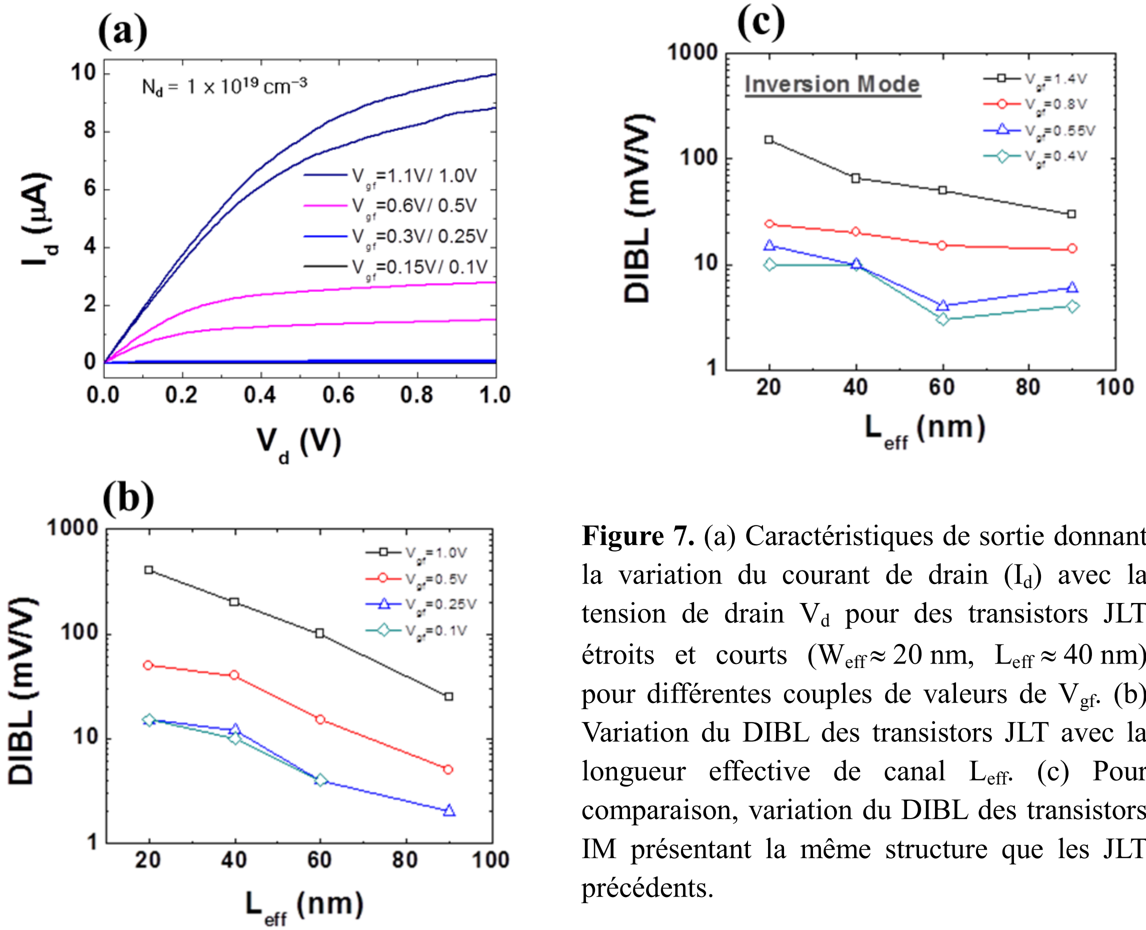


Figure 7. (a) Caractéristiques de sortie donnant la variation du courant de drain (I_d) avec la tension de drain V_d pour des transistors JLT étroits et courts ($W_{eff} \approx 20$ nm, $L_{eff} \approx 40$ nm) pour différentes couples de valeurs de V_{gf}. (b) Variation du DIBL des transistors JLT avec la longueur effective de canal L_{eff}. (c) Pour comparaison, variation du DIBL des transistors IM présentant la même structure que les JLT précédents.

Dopage du canal

La concentration de dopants dans le canal peut être déduite de la densité surfacique de porteurs libres (n_{s_fb}) à la tension de bandes plates (≈ 0.24 V):

$$n_{s_fb} = N_d \cdot t_{si} \qquad (4)$$

C'est ce qui est fait sur la figure 8.a. On extrait ainsi une valeur de N_d (≈ 4×10^{18} cm^{-3}) plus faible que la valeur cible qui était de 1×10^{19} cm^{-3}.Cependant, cette façon d'extraire le dopage est assez sensible à la précision avec laquelle V_{fb} est extraite. Nous avons donc testé également une autre méthode, qui utilise la fonction de Maserjian (Y_M), définie comme [13, 14]:

$$Y_M = \frac{1}{C_{gc}^3} \cdot \frac{\partial C_{gc}}{\partial V_{gf}} = \frac{1}{C_{sc}^3} \cdot \frac{\partial C_{sc}}{\partial V_s} \qquad (5)$$

où C_{sc} et V_s représentent respectivement la capacité du semi-conducteur et le potentiel de surface. La fonction YM a l'avantage d'être indépendante de la capacité d'oxyde. Elle ne dépend que des caractéristiques du substrat. Le dopage peut être extrait dans le régime de désertion partielle grâce à l'équation 6, en utilisant la méthode usuelle qui consiste à tracer $1/C^2$ en fonction de V_g [13]:

$$N_d = \frac{1}{q \cdot \varepsilon_{si} \cdot Y_M} \qquad (6)$$

où est la permittivité relative du silicium. On obtient ainsi une courbe en fonction de V_{gf} (Fig. 8-b). La valeur de Nd qui représente le dopage de canal correspond au plateau qu'on observe dans cette courbe. Les valeurs obtenues ainsi confirment que les valeurs réelles de dopage sont plus faibles que les valeurs cibles, d'environ un facteur 2. Ces valeurs de dopage sont tout à fait cohérentes avec les valeurs obtenues pour la mobilité faible champ en canal long (Fig. 6) et pour le silicium massif [11].

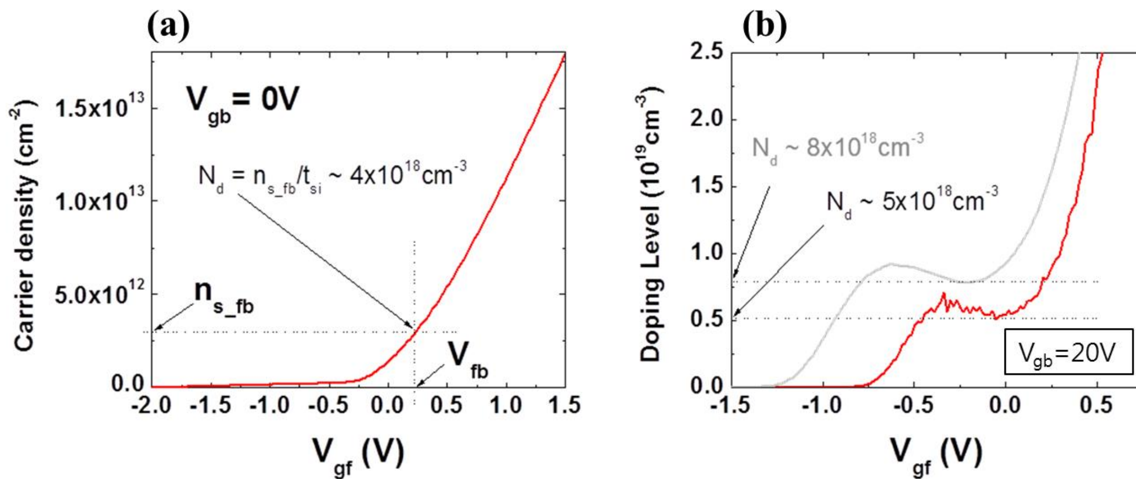


Figure 8. (a) Densité surfacique de porteurs libres (n_s) en fonction de V_{gf}.. Le dopage de canal est déduit de la valeur n_{s_fb} de la densité surfacique de porteur à la tension de bandes plates (≈ 0.24 V). (b) Variation en fonction de V_{gf} du dopage apparent extrait par la fonction de Maserjian pour des JLT de dopage différent. Le dopage visé valait 1×10^{19} cm^{-3} (courbe rouge) ou 2×10^{19} cm^{-3} (courbe grise). Les valeurs de N_d extraites au niveau du plateau valent respectivement ≈ 5×10^{18} cm^{-3} et ≈ 8×10^{18} cm^{-3}.

Extraction de paramètres à partir de la capacité grille-canal

Nous avons également analysé les variations de la capacité grille canal par unité de largeur, C_{gc}. La figure 9-a montre comment C_{gc} varie avec V_g en fonction de la largeur du JLT. Le paramètre W_{top_eff} représente la largeur effective du JLT vu de dessus. Il faut lui ajouter deux fois l'épaisseur du film pour obtenir la largeur effective utilisé pour la normalisation de C_{gc}. Lorsque V_g augmente, on observe d'abord une augmentation de C_{gc}, liée à la transition entre le régime entièrement déserté et la formation du canal neutre en volume. Cela se traduit par un premier épaulement sur la gauche de la courbe. Un second épaulement apparait ensuite à la transition entre le régime de désertion partielle en surface et le régime d'accumulation. Ces épaulements se traduisent par des pics sur la dérivée de Cgc. Au vu de ce qui a été dit précédemment, ces pics permettent d'extraire les valeurs de V_{th} et de V_{fb} (Figure 9-b) [15].

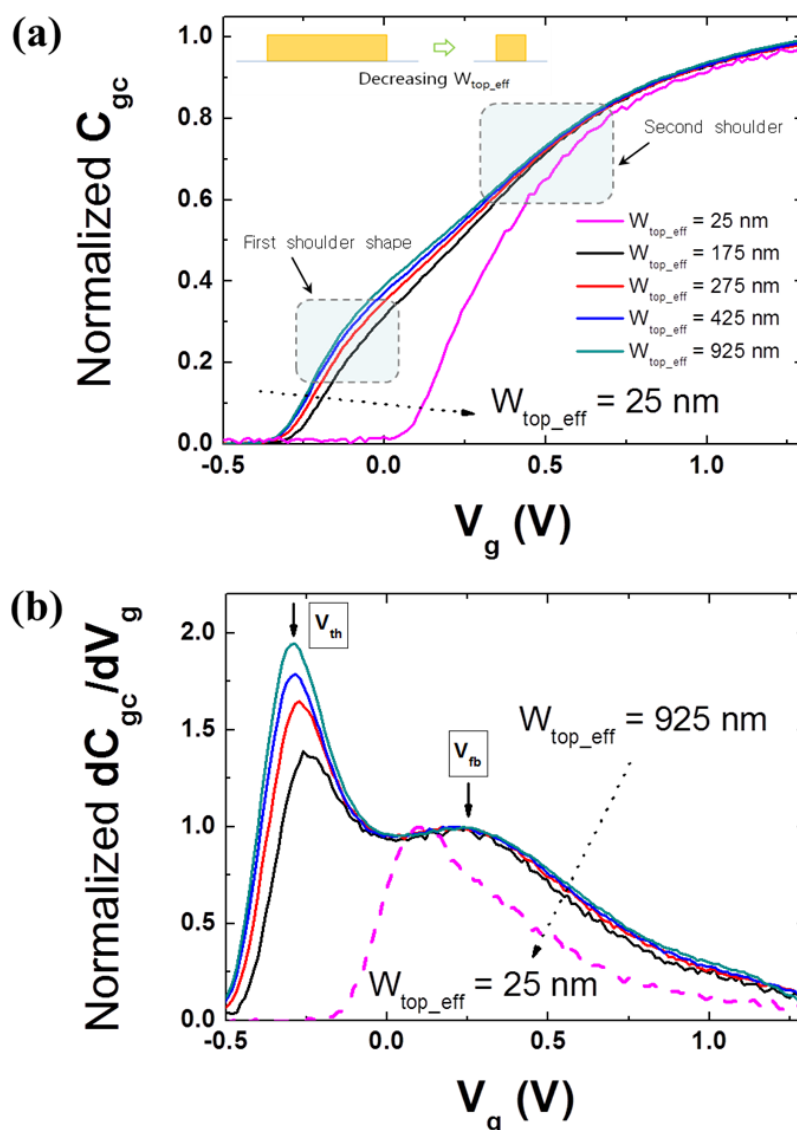


Figure 9. (a) Variation, en fonction de Vg, de la capacité par unité de largeur de grille (Cgc) pour différentes valeurs de la largeur effective vue de dessus (Wtop_eff) et (b) courbes dCgc/dVg normalisées en fonction de l'amplitude du second pic.

Par ailleurs, on constate sur la figure 9-a que le premier épaulement s'atténue lorsque la largeur décroit, pour disparaitre complètement dans les JLT les plus étroits (W_{top_eff} = 25 nm) - qui peuvent être considérés comme des transistors JLT tri-gate à nanofil. Cela traduit le fait que le canal en volume joue un rôle relatif de plus en plus faible par rapport au canal d'accumulation en surface au fur et à mesure que le canal se rapproche d'un JLT tri-gate. On retrouve cette tendance sur la dérivée. Lorsque W_{top_eff} décroit, l'amplitude du premier pic décroit par rapport au second (pour faciliter la comparaison, ce dernier a été maintenu constant par normalisation de la dérivée), traduisant une décroissance du poids relatif de la conduction en volume par rapport à la conduction en surface dans les transistors JLT les plus étroits. On constate par ailleurs que la position du premier pic (V_{th}) se décale légèrement vers des valeurs plus élevées lorsque W_{top_eff} décroit, tandis que la position du second pic (V_{fb}) reste

inchangée. En effet pour les JLT larges, le transistor se comporte comme un composant planaire contrôlé par la grille supérieure. Quand la largeur du canal diminue, une proportion non négligeable du canal est également contrôlée par les côtés (grilles latérales). Cet effet est particulièrement visible en désertion partielle: dans ce régime la distribution du potentiel est fortement affectée par la présence des grilles latérales. C'est au moment de la formation du canal neutre que la différence entre un fonctionnement planaire à un fonctionnement tri-gate est la plus visible. C'est ce qui explique la sensibilité de V_{th} à la valeur de W_{top_eff}. Nous exploiterons plus loin cette idée pour en déduire une méthode d'extraction du dopage et la tension de bandes plates. On observe notamment qu'il n'existe plus qu'un seul pic (en pointillés sur la figure 9-b) pour les JLT de type nanofil tri-gate (W_{top_eff} = 25 nm). Ceci traduit le fait que les grilles latérales jouent un rôle primordial pour des largeurs aussi faibles. Cette constatation confirme les résultats de *Choi et al.* qui avaient montré une augmentation de V_{th} lorsqu'on réduit la largeur du canal dans le cas de transistors JLT à grille enrobante (GAA). Ces auteurs ont également montré que la tension de seuil des JLT était beaucoup plus sensible aux variations de largeur de canal que celle des transistors à inversion. [16]

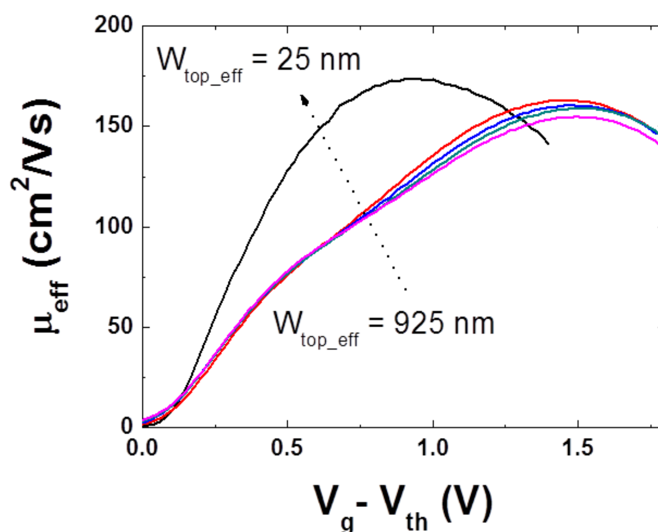


Figure 10. Mobilité effective μ_{eff} extraite par la technique split CV, à partir des mesures de la capacité grille-canal et du courant de drain. Variation en fonction de la tension de grille V_g-V_{th} (référencée par rapport à la tension de seuil) pour différentes valeurs de la largeur de canal. Pour cette extraction, les composants sont polarisés en régime linéaire (V_d = 50 mV).

La mesure de la capacité de grille-canal permet d'extraire la mobilité effective par la méthode split CV, ainsi que sa variation en fonction de la tension de grille. La figure 10 montre les courbes obtenues pour différentes des composants de largeur différente. Les JLT très étroits (W_{top_eff} = 25nm) se comportent très différemment des JLT plus larges (W_{top_eff} entre 175nm et 975nm). Ceci est dû à l'effet des grilles latérales qui modifie profondément la distribution des charges mobiles par rapport à un composant planaire, notamment dans les régimes de tension intermédiaires entre désertion totale et accumulation. C'est cette modification de la charge qui se traduit par une variation apparente de la mobilité effective - dans une zone de polarisation où le canal d'accumulation n'est pas encore complètement formé. Il s'agit du même type d'artefact qui fait que la valeur de μ_{eff} extraite près du

seuil est sous-estimée dans les transistors à inversion. Le rôle des grilles latérales a été confirmé grâce à des simulations numériques 2D. Nous avons vérifié que les courbes $C_{gc}(V_g)$ et $dC_{gc}/dV_g(V_g)$ normalisées déduites de la simulation présentaient les mêmes caractéristiques que les courbes expérimentales montrées ci-dessus.

Caractérisation électrique des transistors JLT à basse température

Nous avons mesuré les caractéristiques de transfert en $I_d(V_g)$ de transistors JLT respectivement courts et longs (i. e. de longueurs de grille respectives L_{eff} = 20 nm et L = 1 μm) pour des températures variant de 80 K à 350 K (voir les figures 11-a et 11-c).

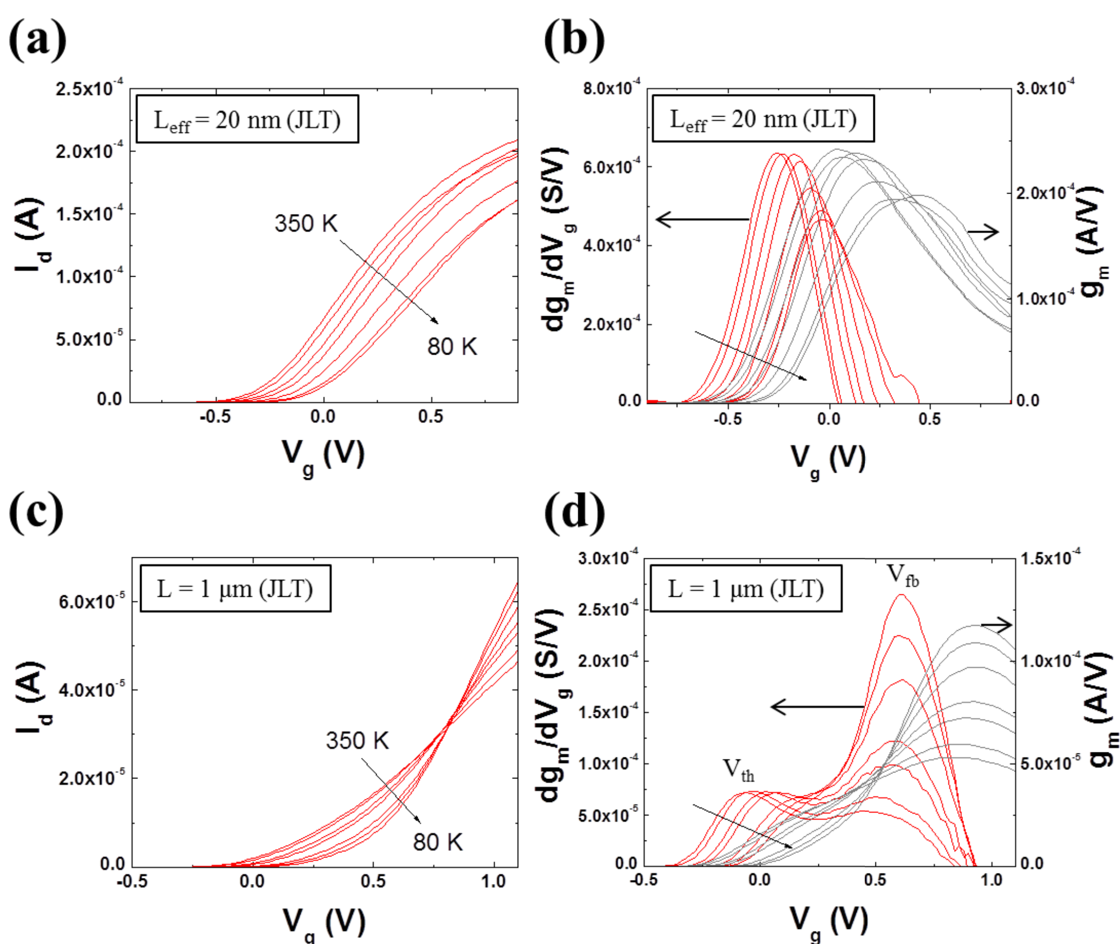


Figure 11. Drain current Id of JLT devices measured as a function of Vg with temperature varying in the range of 80 K to 350 K, together with the corresponding transconductance gm (gray) and derivative of transconductance dgm/dVg (red). Gate width is W = 10 μm and targeted doping level Nd = 1019 cm−3. Devices are biased in the linear regime of operation with Vd = 20 mV.

Ce n'est que pour les dispositifs à canal long que ces caractéristiques se coupent en un même point, appelé ZTC (*zero temperature coefficient*) [17], pour lequel les dépendances en température de la mobilité et de la tension de seuil se compensent (Figure 11-c). On ne retrouve pas ce fonctionnement

en canal court. De fait, pour les canaux longs, la mobilité et la tension de seuil augmentent toutes les deux lorsque la température décroît, tandis qu'elles varient en sens inverse (la mobilité augmente mais la tension de seuil diminue) pour les canaux courts.

La figure 12-a montre la dépendance en température de V_{th} et de V_{fb} pour des transistors JLT longs (L = 1 µm). Pour déterminer V_{th} et V_{fb}, nous avons utilisé la position des pics dans la courbe dg_m/dV_g (Figure 11-d). La tension de seuil du JLT peut être calculée en faisant l'approximation d'une transition abrupte entre zone désertée et zone neutre, dans une géométrie planaire valable pour les transistors larges. Elle s'exprime comme [8, 18]:

$$V_{th} = V_{fb} - \frac{q \cdot N_d \cdot t_{si}^2}{2\varepsilon_{si}} - \frac{q \cdot N_d \cdot t_{si}}{C_{ox}} \qquad (7)$$

où q, N_d, ε_{si} et C_{ox} représentent respectivement la charge électronique, la concentration de dopants dans le canal, la permittivité du silicium et la capacité d'oxyde par unité de surface. D'après l'équation 7, la variation en température de la tension de seuil (dV_{th}/dT) devrait être la même que celle de la tension de bandes plates (dV_{fb}/dT). En effet, dans l'expression de V_{th} donnée par l'équation 7, V_{fb} est le seul terme qui dépend de la température. C'est effectivement ce que l'on constate sur la figure 12-a qui montre qu'il n'y a pas de différence notable entre els variations en température de V_{th} et V_{fb}.

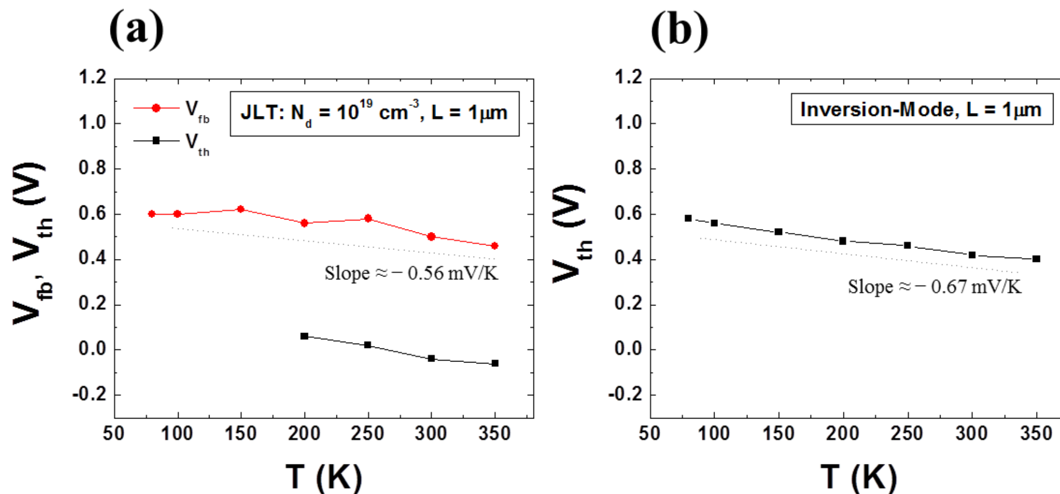


Figure 12. (a) Dépendance en température de V_{fb} (en rouge) et de V_{th} (en noir) pour un JLT long (L = 1 µm). Les valeurs de V_{th} et de V_{fb} ont été extraites à partir de la position des pics dans la courbe dg_m/dV_g, comme indiqué sur la figure 11-d. (b) dépendance en température de V_{th} obtenue pour un transistor à inversion de même structure et de même longueur (L = 1 µm).

La variation en température de la mobilité est montrée sur la figure 13 pour les JLT (figures 13-a et 13-b, correspondant à deux dopages différents) et pour le transistor à inversion de même structure (figure 13-c). Pour les canaux longs, la mobilité faible champ augmente à basse température et ce quel que soit le type de composant. Elle suit donc la tendance très généralement observée qui correspond à une mobilité limitée par l'interaction avec les phonons acoustiques, qui augmente donc du fait du gel

des phonons à basse température. Toutefois, cette amélioration de mobilité à basse température est beaucoup plus limitée dans les JLT ($|d\mu_0/dT|$ plus faible) que dans les transistors IM. Ceci est dû au poids accru de l'interaction avec les impuretés ionisées dans les JLT, du fait de leur fort dopage de canal. Le rôle de l'interaction avec les impuretés ionisées est confirmé par le fait que l'augmentation du dopage de canal ($N_d = 2\times10^{19}$ cm^{-3}) se traduit par une diminution de $|d\mu_0/dT|$, comme on peut le vérifier sur la figure 13-b.

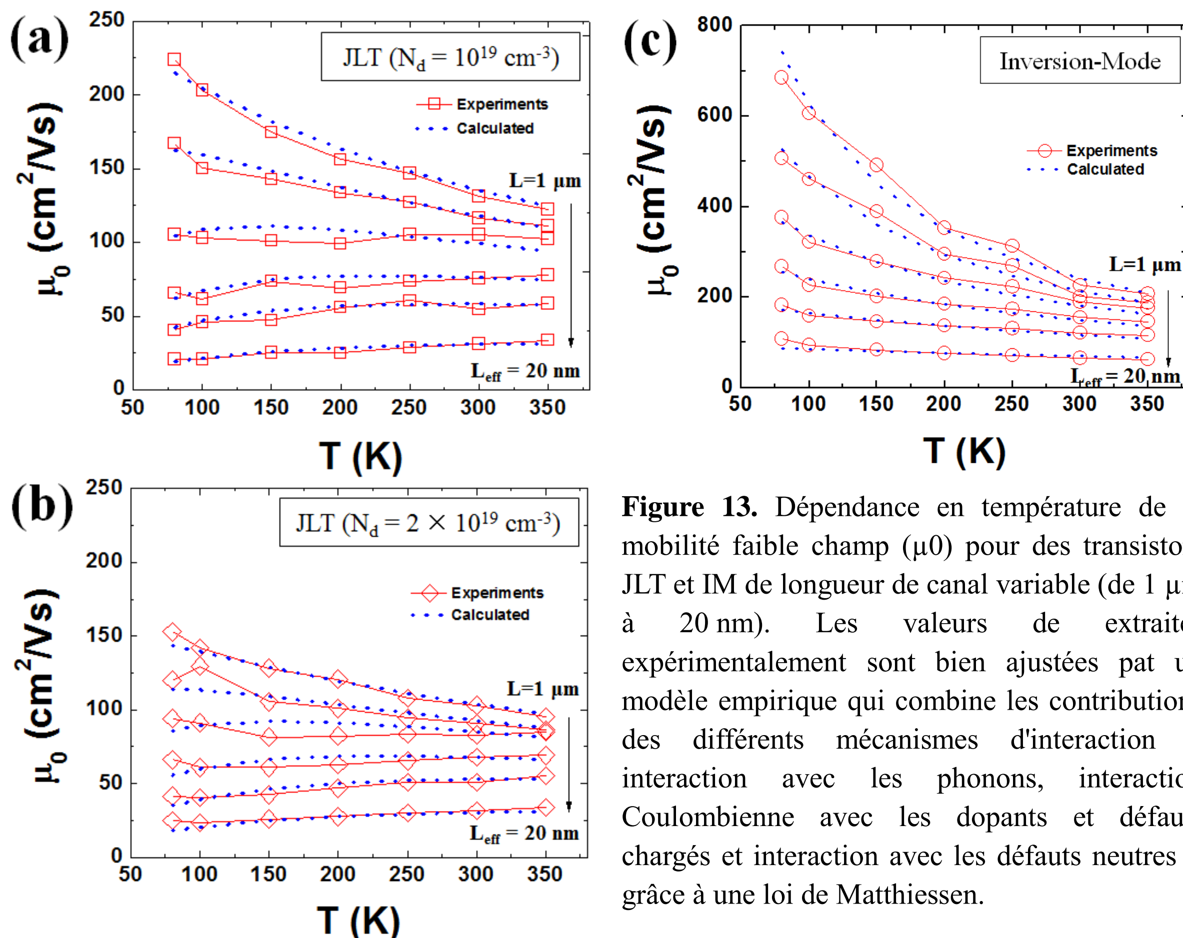


Figure 13. Dépendance en température de la mobilité faible champ (µ0) pour des transistors JLT et IM de longueur de canal variable (de 1 µm à 20 nm). Les valeurs de extraites expérimentalement sont bien ajustées pat un modèle empirique qui combine les contributions des différents mécanismes d'interaction − interaction avec les phonons, interaction Coulombienne avec les dopants et défauts chargés et interaction avec les défauts neutres − grâce à une loi de Matthiessen.

Pour les canaux courts, on constate que la mobilité faible champ décroît légèrement dans les JLT lorsque la température décroît, alors qu'elle augmente toujours (moins que pour les canaux longs malgré tout) dans les transistors IM. Ceci laisse penser qu'il existe près des contacts de source et de drain des mécanismes d'interaction supplémentaires dont l'effet ne se manifeste clairement que dans les transistors courts [19-21]. Compte tenu de leur effet sur la variation en température de la mobilité, ces interactions additionnelles semblent être relativement peu influencées par la température. L'analyse peut être approfondie en ajustant les résultats expérimentaux de la figure 13 sur un modèle empirique de la mobilité faible champ qui consiste à combiner grâce à la loi de Matthiessen les contributions des différents types d'interaction susceptibles d'intervenir. Dans le cas présents,

l'ajustement nécessite de prendre ne compte trois contributions [19]:

$$\frac{1}{\mu_0} = \frac{1}{\frac{300}{T} \cdot \mu_{ph}} + \frac{1}{\frac{T}{300} \cdot \mu_c} + \frac{1}{\mu_{neu}} \qquad (8)$$

où μ_{ph}, μ_c et μ_{neu} représentent les contributions respectives à température ambiante des interactions avec les phonons, des interactions Coulombiennes avec les dopants ionisés et défauts chargés et des interactions avec les défauts neutres.

Pour les transistors IM longs, on obtient un ajustement satisfaisant en ne conservant que les interactions avec les phonons. Il faut rajouter les interactions avec les défauts neutres et dans une moindre mesure les interactions Coulombiennes pour les JLTs. Ces dernières sont toutes deux renforcées lorsque le dopage est plus élevé ($N_d = 2\times10^{19}$ cm^{-3}). Ceci est cohérent dans la mesure où une augmentation du dopage est en principe associée à une augmentation des défauts induits par le processus d'implantation [20]. Pour les transistors courts, le comportement de μ_0 en température est déterminé par les interactions avec les défauts chargés et neutres pour les JLTs et par les seuls défauts neutres pour les transistors IM. On retrouve un comportement déjà observé dans de nombreux transistors d'architectures différentes. Il a été attribué à la présence de défauts d'implantation près des S/D. On se trouve dans une situation similaire ici, même pour les JLT. De fait, bien qu'il ne soit en principe pas indispensable d'implanter les S/D dans un transistor JLT, une implantation supplémentaire, de même type que le canal, a été utilisée pour réduire les résistances d'accès et améliorer les performances des transistors JLT testés ici. Cette implantation peut donc être à l'origine d'une concentration accrue de défauts chargés et neutres près des S/D des JLTs.

La figure 14 montre la dépendance en température de la pente sous le seuil, $S = dV_g/d[\log(I_d)]$), extraite pour des transistors JLT et IM. Leur longueur de grille varie de 240nm à 40nm. Pour les canaux longs, les valeurs de S extraites pour les JLT les moins dopés ($N_d = 10^{19}$ cm^{-3}) sont comparables à celles des transistors IM, et proches de la valeur idéale (kT/q)×ln10. Pour les longueurs de grille intermédiaires, les transistors JLT ont une pente sous le seuil légèrement supérieure à celle des transistors IM. Ceci peut être dû à un contrôle de grille légèrement dégradé par leur épaisseur équivalente d'oxyde plus importante [8]. Toutefois, pour les grilles les plus courtes, la pente sous le seuil des transistors IM augmente très fortement, phénomène qui n'est pas observé pour les JLT. Ces derniers se révèlent beaucoup plus robustes vis à vis des effets de canal court, avec une meilleure immunité contre l'influence électrostatique des contacts de source et de drain dans le régime sous le seuil. Ceci constitue certainement l'un de leurs points forts vis à vis des transistors à inversion.

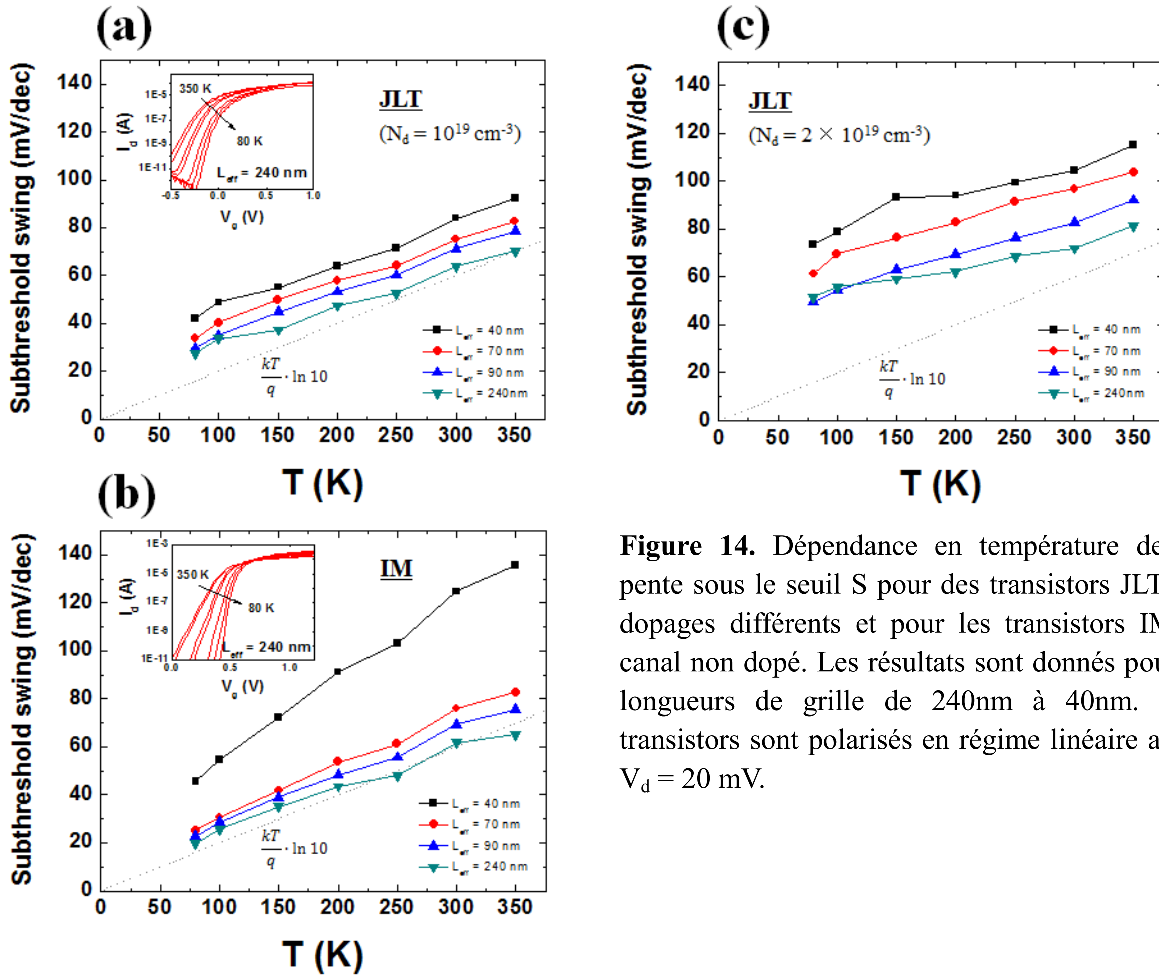


Figure 14. Dépendance en température de la pente sous le seuil S pour des transistors JLT de dopages différents et pour les transistors IM à canal non dopé. Les résultats sont donnés pour 4 longueurs de grille de 240nm à 40nm. Les transistors sont polarisés en régime linéaire avec V_d = 20 mV.

Caractérisation du bruit basse fréquence dans les transistors sans jonctions

Ces mesures ont été effectuées sur une autre série de transistors JLT qui ont donc préalablement été caractérisés en statique de façon à localiser les différents régimes de fonctionnement.

Ainsi que le montre la figure 15-b, on retrouve les deux pics caractéristiques du JLT sur la courbe dg_m/dV_g [15] alors qu'on n'observe bien qu'un seul pic pour les transistors IM (Fig. 15-c). Ainsi que nous l'avons expliqué plus haut, le pic de gauche permet d'extraire la tension de seuil (V_{th}), qui correspond à l'apparition à la conduction en volume, à la transition entre désertion complète et désertion en surface, tandis que le pic de droite permet d'extraire la tension de bandes plates (V_{fb}) qui correspond à l'apparition du canal d'accumulation [15]. La ligne en pointillé permet de suivre la position de V_{fb} à travers les figures 15-a et 15-b. On peut ainsi repérer la gamme de tension de grille, à gauche de cette ligne, où le courant circule dans le canal neutre, en volume ainsi que la gamme de courant de drain correspondante.

La figure 16-a montre la variation en fréquence de la densité spectrale de bruit (PSD) mesurée pour un même niveau de courant de drain (≈ 1.7 × 10^{-4} A) dans les transistors JLT et IM. Dans les deux cas, on observe une dépendance classique, en 1/f.

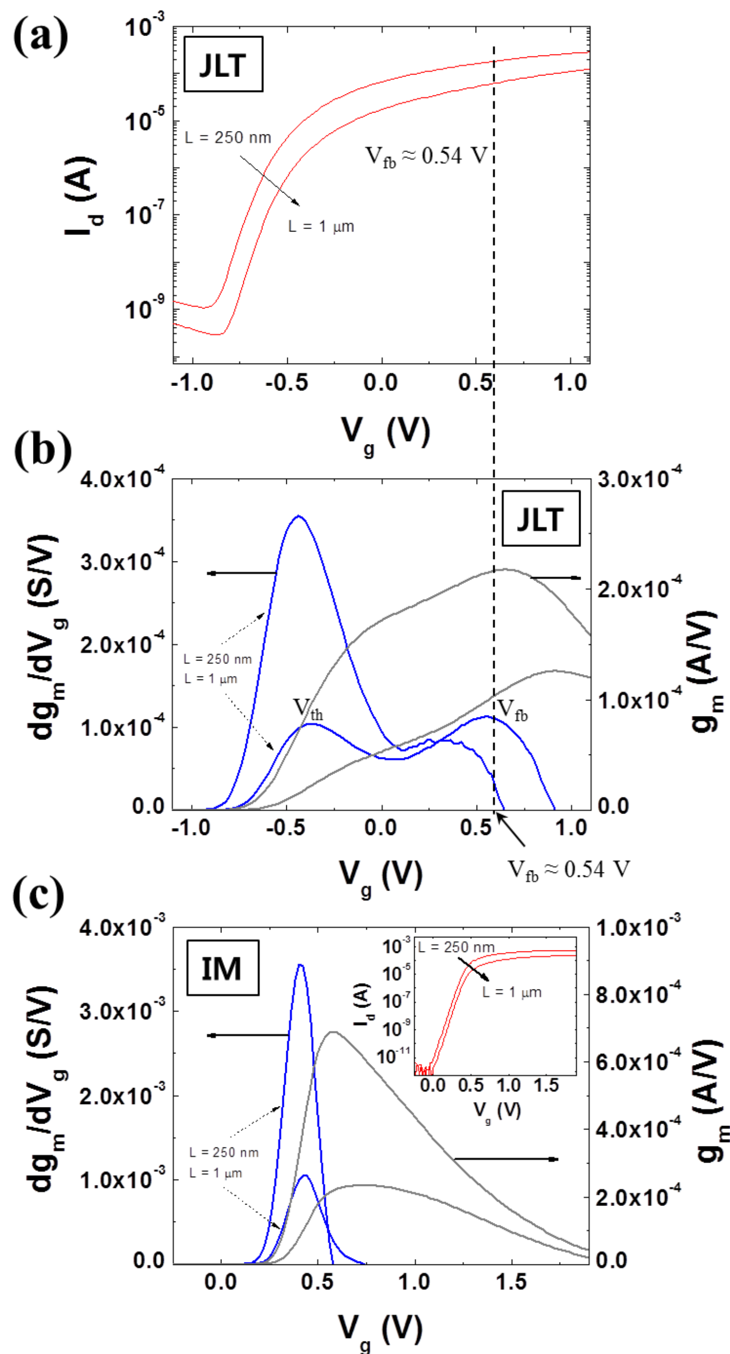


Figure 15. (a) Caractéristiques de transfert montrant la variation du courant de drain I_d avec V_g dans un JLT planaire (W=10µm) pour deux longueurs de grille. (b) Variation de la transconductance g_m (courbes grises) et de sa dérivée dg_m/dV_g (courbes bleues) pour le même composant. (c) pour comparaison, résultats obtenus pour un transistor IM de même structure, avec les caractéristiques de transfert en insert. Dans tous les cas, les composants sont polarisés en régime linéaire, avec V_d = 50 mV.

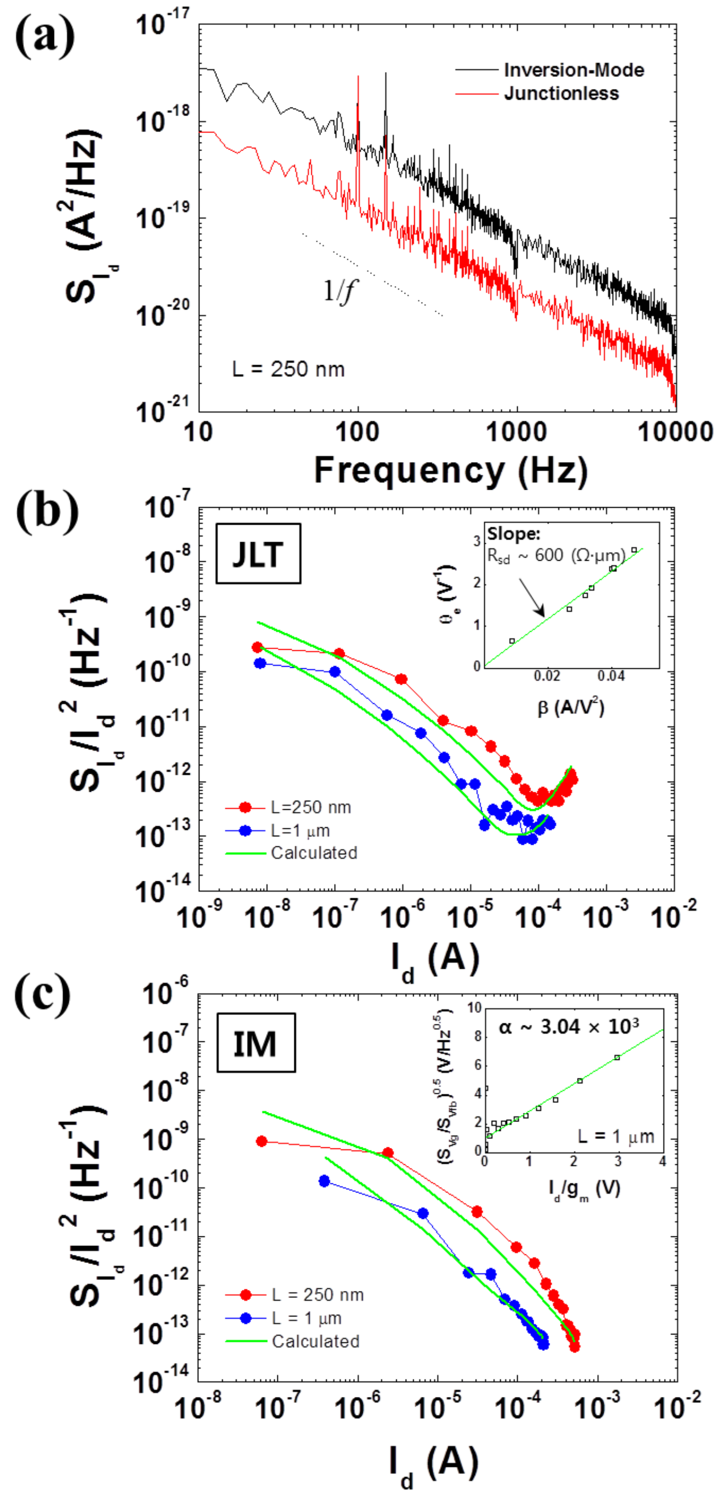


Figure 16. (a) Densités spectrales de puissance (PSD) du bruit en courant mesurées pour un même courant $I_d \approx 1.7 \times 10^{-4}$ A en régime linéaire ($V_d = 50$ mV) pour les transistors JLT et IM. (b) Variation de la PSD normalisée du bruit en courant (S_{Id}/I_d^2) à 1 kHz, en fonction de I_d, pour les JLTs (symboles). Les courbes vertes montrent l'ajustement obtenu avec l'équation 9. En insert: variation du coefficient d'atténuation d'ordre 1 de la mobilité (θ_e) en fonction du gain en conductance (β) qui permet d'extraire les résistances d'accès. (c) Variation de S_{Id}/I_d^2 en fonction de I_d pour les transistors IM. En insert: variation de $(S_{Vg}/S_{Vfb})^{1/2}$ en fonction de I_d/g_m , qui permet d'extraire le coefficient de Coulomb α.

Rappelons qu'il existe deux modèles principaux pour expliquer l'origine du bruit basse fréquence. Dans l'un d'eux, le bruit basse fréquence trouve son origine dans des fluctuations du nombre de porteurs, corrélées à des fluctuations de mobilité. Ces fluctuations corrélées s'expliquent par le piégeage / dépiégeage des porteurs libres par des pièges lents présents dans le diélectrique de grille, avec une variation corrélée de l'interaction Coulombiennes à distance avec les charges correspondantes. Les fluctuations de la charge dans le diélectrique de grille sont associées à des fluctuations de la tension de bandes plates V_{fb}. Dans ce modèle la densité spectrale de bruit normalisée du courant de drain s'exprime sous la forme [22, 23]:

$$\frac{S_{I_d}}{I_d^2} = (1 + \alpha\mu_{eff} C_{ox} I_d / g_m)^2 \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \qquad (9)$$

où α est le coefficient d'interaction de Coulomb, μ_{eff} est la mobilité effective, C_{ox} est la capacité d'oxyde par unité de surface et S_{Vfb} est la PSD de la tension de bandes plates. L'autre modèle, proposé par Hooge, suppose uniquement des fluctuations de mobilité. Dans ce cas, varie S_{Id}/I_d^2 en $1/I_d$. En général, on observe de façon assez générale que le modèle de Hooge convient pour les composants où la conduction se fait en volume, tandis que les fluctuations du nombre de porteurs expliqent mieux le bruit basse fréquence des composants où la conduction se fait le long d'une interface.

Pour déterminer l'origine du bruit basse fréquence dans les JLT, nous avons donc également reporté sur la figure 16-b la densité spectrale de puissance normalisée du courant de drain (S_{Id}/I_d^2) en fonction du courant de drain, pour les transistors JLT sur la figure 16-b et pour les transistors IM sur la figure 16-c. Les figures 16-b et 16-c montrent que, dans le cas présent, la PSD normalisée du bruit en courant varie en réalité de façon assez similaire dans les JLT et dans les transistors IM. Elle tend notamment à saturer à fréquence basse. Les courbes vertes qui correspondent à un ajustement selon l'équation 9 (avec prise en compte du bruit lié aux résistances d'accès et de la corrélation avec les fluctuations de mobilité) montre que le modèle de fluctuation du nombre de porteurs est mieux adapté non seulement pour les transistors IM (Fig. 16-c), ce qui était attendu, mais également pour les JLT (Fig. 16-b) alors même qu'on est dans un régime de polarisation où la conduction a bien lieu en volume (se référer à la Fig. 15-b qui montre que le courant de drain pour lequel est mesuré le bruit correspond bien à une tension de grille inférieure à la tension de bandes plates).

Nous pensons que ce résultat peut s'expliquer en remarquant que la zone désertée en surface ne constitue pas un gros obstacle vis à vis de la capture ou de l'émission de porteurs libres par des pièges dans le diélectrique de grille. Même dans les transistors à conduction en surface, le piégeage se fait par un mécanisme d'effet tunnel entre des états délocalisés dans le canal et des états localisés situés à une certaine profondeur dans le diélectrique. La transition entre la zone désertée en surface et le canal neutre en volume est par ailleurs loin d'être abrupte à température ambiante. Par conséquent, même en dessous la tension de bandes plates, c'est-à-dire dans une zone ou le canal est séparé du diélectrique de grille par une zone désertée, il y a une forte probabilité que des porteurs libres du canal puissent être

capturés par des pièges présents dans le diélectrique de grille que ce soit par une diffusion vers l'interface suivie d'une capture par effet tunnel ou par effet tunnel direct à travers la zone désertée et la barrière diélectrique (voir le schéma de la figure 17-b). Des processus équivalents sont mis en jeu pour le processus inverse d'émission depuis un piège vers le canal.

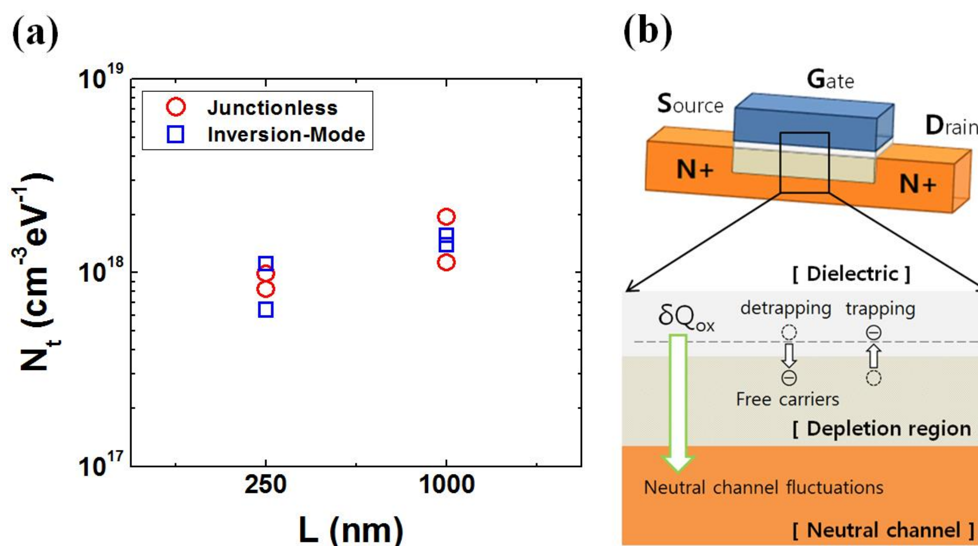


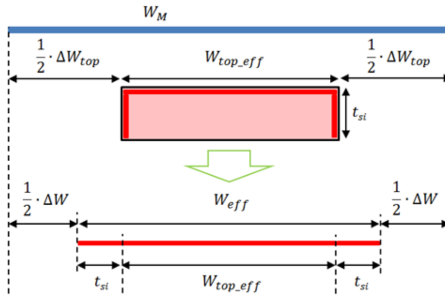
Figure 17. (a) Densité d'états d'interface extraite pour des transistors JLT et IM pour deux longueurs de grille. (b) Schéma illustrant le mécanisme qui conduit à observer un bruit basse fréquence lié à des fluctuations du nombre de porteurs dans les transistors JLT, y compris en dessous de la tension de bandes plates, dans un régime où le transistor conduit en volume.

Développement de nouvelles méthodologies d'extraction de paramètres pour les transistors sans jonctions.

Nous avons tout d'abord développé une nouvelle méthodologie d'extraction de la tension de bandes plates (V_{fb}) et du dopage de canal (N_d) pour les transistors JLT tri-gate.

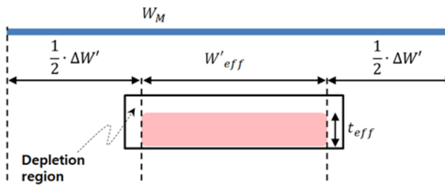
La nouvelle méthode se base sur une analyse de la variation du courant de drain en régime linéaire avec la largeur de canal. Comme le montre la figure 18, cette dépendance s'analyse différemment selon qu'on est en régime de conduction en volume (désertion du canal sous l'interface supérieure et le long des côtés) ou en régime d'accumulation (accumulation sur les trois faces du canal). Les dimensions extraites doivent converger vers la même valeur à la tension de bandes plates. La continuité entre les deux régimes au niveau de la tension de bandes plates permet de trouver une relation entre la largeur effective du canal en accumulation et la largeur effective en désertion partielle. Connaissant l'épaisseur du film de silicium, cette relation de continuité permet d'extraire les valeurs de V_{fb} et de N_d.

- Accumulation region: $V_g > V_{fb}$



$$C = C_{ox} \times L \times (W_M - \Delta W)$$

- Partially depleted region: $V_g < V_{fb}$



$$\frac{Q}{q} = N_d \times L \times t_{eff} \times W'_{eff}$$
$$= N_d \times L \times t_{eff} \times (W_M - \Delta W')$$

Accumulation channel

Bulk neutral channel

- At flat-band condition: $V_g = V_{fb}$

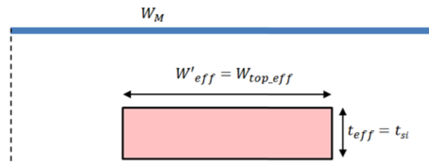


Figure 18. Schéma expliquant le principe sur lequel se fonde notre nouvelle méthode d'extraction de V_{fb} et de N_d dans les transistors JLT tri-gate. Lorsque le transistor est polarisé en bandes plates, les paramètres W'_{eff} et t_{eff} extraits en régime de conduction en volume doivent être égaux aux paramètres W_{top_eff} extrait en accumulation et t_{si} supposé connu.

Dans le cas considéré, on trouve $V_{fb} \approx 0.61$ V et $N_d \approx 4\times10^{18}$ cm^{-3}. Ces valeurs sont tout à fait cohérentes avec les valeurs extraites précédemment. La nouvelle méthode est particulièrement adaptée pour les composants tri-gate pour lesquels les techniques usuelles ne permettent pas d'identifier V_{fb} de façon fiable (voir plus haut). Nous avons également vérifié la validité de la méthode grâce à une simulation numérique bidimensionnelle du contrôle de la charge. Enfin, nous avons constaté que la composante du courant associée aux bords latéraux du canal décroît de façon abrupte lorsque la tension de grille approche la tension de bandes plates. Cette caractéristique peut également être utilisée pour extraire V_{fb} dans les JLT.

Nous avons également proposé une autre méthode pour extraire cette fois la mobilité de volume (μ_{bulk}) et la tension de bandes plates (V_{fb}). Nous nous appuyons cette fois-ci sur le fait que, dans le régime de désertion partielle ($V_{th} < V_g < V_{fb}$), le carré de l'inverse de la transconductance ($1/g_m^2$) est une fonction

linéaire de la tension de grille. Là encore, nous avons vérifié la validité de la méthode d'extraction par simulation numérique. La fonction ainsi définie est une sorte d'équivalent, pour g_m, de la fonction de Maserjian dont la pente permet d'extraire μ_{bulk} et dont l'abscisse à l'origine fournit V_{fb} (voir Figure 19).

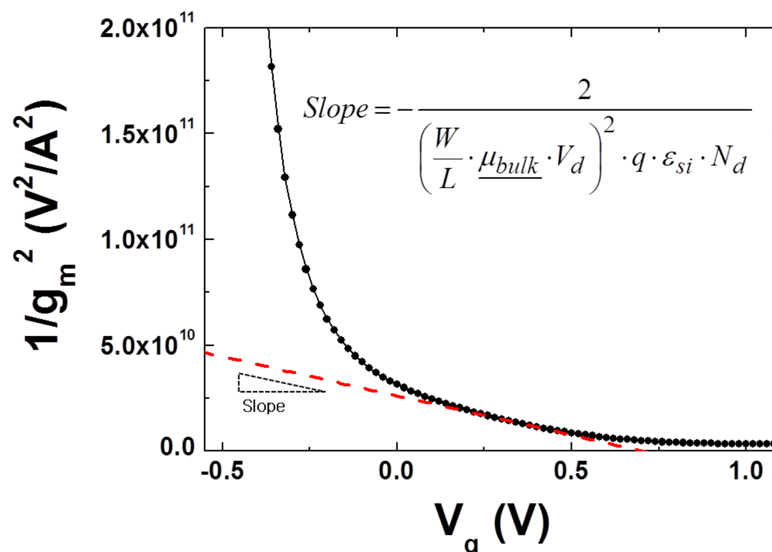


Figure 19. Variation en fonction de la tension de grille de la fonction $1/g_m(V_g)^2$ calculée comme l'inverse du carré de la transconductance. Dans un JLT, cette fonction varie linéairement dans la zone de désertion partielle. Dans cette zone, sa pente permet d'extraire la mobilité en volume selon l'équation indiquée, tandis que l'abscisse à l'origine donne la tension de bandes plates.

Conclusions

Dans ce manuscrit de thèse, nous présentons une étude expérimentale approfondie des performances et des caractéristiques électriques des transistors sans jonctions (JLT). Les caractéristiques courant-tension I-V et capacité-tension C-V ont été analysées dans une large gamme de température (de 80K à 350K) en corrélation avec les différents régimes de fonctionnement de ce type de composants. Nous avons également étudié l'origine du bruit basse fréquence dans les JLT. Toutes ces études ont été menées en parallèle sur des transistors JLT et sur des transistors de référence fonctionnant en inversion (IM), fabriqués de la même façon que les JLT et qui n'en diffèrent que par leur dopage de canal. Pour mener à bien ce travail, nous avons effectué une comparaison critique des différentes méthodologies d'extraction de paramètres utilisées pour les transistors MOS de façon à analyser la façon dont elles peuvent éventuellement s'adapter aux JLT et leurs limitations. Nous avons en outre développé de nouvelles méthodes d'extraction, adaptées au JLT, pour extraire les paramètres spécifiques à ce composant et notamment la tension de bandes plates, le dopage de canal et la mobilité en volume. La validité de ces méthodes a été validée par simulation numérique.

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