# A Flexible Scan-in Power Control Method in Logic BIST and Its Evaluation with TEG Chips


doi: https://doi.org/10.1109/TETC.2017.2767070

# A Flexible Scan-in Power Control Method in Logic BIST and Its Evaluation with TEG Chips

Takaaki Kato†, Senling Wang††, Yasuo Sato†, Seiji Kajihara† and Xiaoqing Wen†

**Abstract**— High power dissipation in scan-based logic built-in self-test (LBIST) is a crucial issue that can cause over-testing, reliability degradation, chip damage, and so on. While many sophisticated approaches to low-power testing have been proposed in the past, it remains a serious problem to control the test power of LBIST to a predetermined appropriate level that matches the power requirements of the circuit-under-test. This paper proposes a novel power-control method for LBIST that can control the scan-shift power to an arbitrary level. The proposed method modifies pseudo-random patterns generated by an embedded test pattern generator (TPG) so that the modified patterns have the specific toggle rate without sacrificing fault coverage and test time. In order to evaluate the effectiveness of the proposed method, this paper shows not only simulation-based experimental results but also measurement results on test element group (TEG) chips.

**Index Terms**— logic BIST, low power test, scan design, scan-in power control, pseudo-random pattern

## 1 INTRODUCTION

IT is well-known that scan testing for logic circuits suffers from excessive power consumption compared with normal operations. While there are two modes in scan testing, namely the shift mode and the capture mode, excessive power consumption may occur in both modes, and it may cause over-testing, reliability degradation, and so on. In shift mode, even chip damage may occur [1][2].

Over the years, many sophisticated low-power-testing approaches have been proposed, which are based on the reduction of switching activity during testing. For scan testing with deterministic test patterns, *don't-care (X) filling*, which assigns appropriate logic values to unspecified bits of test patterns, is a typical approach [2][3]. As a design for testability (DFT) based approach, *blocking circuitry insertion* blocks the propagation of signal transitions from flip-flops to the combinational portion of a circuit-under-test (CUT) [4][5]. *Scan segmentation* is known as an effective technique to reduce shift power, which splits a scan chain into multiple segments and performs the shift operation of each segment at different time cycles [6][7].

The test power issue is especially severe for logic built-in self-test (LBIST) because pseudo-random patterns generated by a test pattern generator (TPG), such as a linear feedback shift register (LFSR), are used. Because correlation between successive bits of pseudo-random patterns is low, the power issue more likely occurs. Various low-power-testing methods for LBIST have been proposed. For example, *vector inhibition and selection* eliminates (or masks) useless test patterns for fault detection [8][9][10], *TPG modification* manipulates the toggle rate of pseudo-random patterns through many ingenious low-power TPG design to reduce the scan-in power (power dissipation caused by shifting test patterns into scan chains), such as *LT-RTPG* [11], *ALP-RTPG* [12], *pseudo low-pass filter* (*PLPF*) [13][14], *low-power decompressor* [15], *preselected toggling TPG* [16] and *programmable LP-PRPG* [17]. In addition, a method to reduce the scan-out power (power dissipation caused by shifting test responses out of scan chains) was also proposed in [14][18] by filtering test vectors with high toggle rates on capture responses before the scan-out operation is conducted.

While the above low-power approaches can significantly reduce the scan-shift power for LBIST, two problems still remain. One is the over-reduction of test power that may lead to test escape. According to power requirement for each design, an appropriate level of test power for the CUT should be determined. The other is the fault coverage loss due to test pattern modification. It is known that the loss of randomness of pseudo-random test patterns may lead to the degradation of fault coverage. For the fault coverage problem, several methods have been proposed e.g., *test point insertion* [19][20][21], *reseeding* [22], and *sequential observation under multi-cycle tests* [13][14][23]. Since the requirements of power-consumption and fault coverage vary with applications and devices, a low-power scheme for LBIST that can provide flexible and scalable scan-shift power control is strongly required.

This paper presents a low-power LBIST method that can control the scan-shift power to an arbitrary target level without sacrificing fault coverage or test time. As a circuit for reducing scan-shift power, the proposed method employs two or more types of PLPFs [13] that suppresses the toggles of a scan-in bit sequence. Each PLPF can change a given scan-in bit sequence to the one with a fixed toggle rate, but the proposed method realizes the target toggle rate by switching an active PLPF among the prepared PLPFs according to a precomputed scheduling. Because a trade-off exists among scan-in power reduction, fault coverage improvement and hardware overhead, this paper provides three types of power control approaches

• † *Authors are with Kyushu Institute of Technology, Kawazu 680-4, Iizuka, Fukuoka, 820-8502, Japan. E-mail: {katou,sato,kajihara,wen}@aries30.cse.kyutech.ac.jp*
• †† *The author is with Ehime University, 10-13, Dogo-Himata, Matsuyama, Ehime, 790-8577, Japan. E-mail: wang@cs.ehime-u.ac.jp*

with different priorities. In addition, optimally designed PLPF circuits consisting of fewer logic gates than the original design [13] are described.

Experimental results to evaluate the effectiveness of the proposed method consist of two parts, which are logic/fault simulation to calculate toggle rates and fault coverage, and TEG chip measurements to observe the reduction of circuit current and delay during scan-shift operation. Simulation results show that the proposed method can control the scan-in toggle rate to a given target level within 0.2% errors, and fault coverage were increased by 8.41% for the stuck-at fault model and 4.94% for the transition-fault model. The TEG measurement results confirm a strong correlation between the toggle rate and circuit current, or between the toggle rate and circuit delay. These results imply that the proposed method can flexibly control the circuit current and delay during the scan-shift operation.

This paper is a complement to our previous paper presented in [24] that addresses the fundamental idea of the flexible scan-in power control and shows simulation based experimental results. This paper adds the TEG based experimental results to the previous paper. Furthermore, this paper newly includes examples of the scan-in power control method and simulation-based experimental results in terms of the transition fault coverage and the detailed area overhead using CMOS 65nm technology.

The remainder of the paper is organized as follows: Section 2 describes the underlying scan-in power reduction method using the PLPFs proposed in [13]. Section 3 introduces the optimized PLPF design. Section 4 presents the novel scan-in power control method. Section 5 shows the experimental results of the proposed method in terms of toggle rates, fault coverage and area overhead. Section 6 shows the TEG chip design and the measurement results of actual physical power under scan-in power control. Finally, Section 7 concludes the paper.

## 2 PLPF FOR SCAN-IN POWER REDUCTION

A circuit named PLPF has been developed for reducing the scan-in power of LBIST [13]. Fig. 1 shows the structure of the PLPF which is a combinational circuit composed of $2n\text{-}1 (n \geq 1)$ inputs. Input $T_j$, where $j$ corresponds to a time, is directly extracted from the TPG which is typically composed of an LFSR and a *phase shifter for filter (PSF)* [25]. $T_j$ is referred to as the *current* bit. Inputs $T_{j+n-i}$ $(0<i<n)$ are the next $n\text{-}1$ bits to the current bit $T_j$ and they are referred to as the *future* bits. Remaining inputs $S_{j-n+i}$ $(0<i<n)$ are the feedbacks from the first $n$-1 flip-flops (FFs) of the scan chain and are referred to as the *past* bits. The output $S_j$ of the PLPF is directly connected with the input of the scan chain. The combinational logic of the PLPF calculates the moving average and outputs $S_j$ instead of the current bit $T_j$. The future bits $T_{j+n-i}$ and the past bits $S_{j-n+i}$ work as a filter to eliminate the parts with high toggles in the pseudo-random patterns, and thus a modified low-power scan-in pattern to be inputted to the scan chain is generated.

The toggle rate of the generated scan-in pattern is determined from the number of inputs of the PLPF. The larger the number of the inputs becomes, the lower becomes the derived toggle rate from the PLPF. On the other hand, the area of the PLPF becomes larger as the number of inputs increases. Note that the PSF for extracting the future bits from the LFSR is simple and easy to implement. Fig. 2 shows an example of the PSF structure for a 4-bit LFSR, which can provide scan-in bit sequences for four scan chains. Note that only one EXOR gate is needed to generate the future bit $T_{j+2}$ for the second scan chain (denoted by SC2).

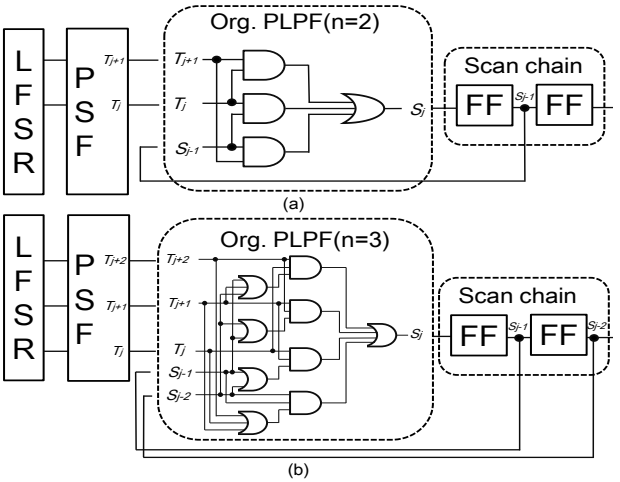
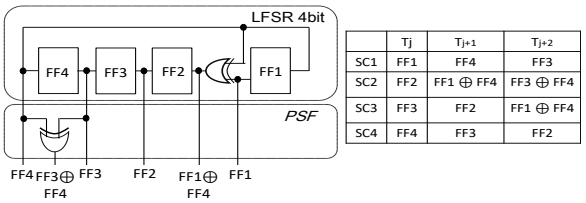



Fig. 1 Structure of the original PLPF (a) n=2 and (b) n=3 [13]




| | Tj | Tj+1 | Tj+2 |
|---|---|---|---|
| SC1 | FF1 | FF4 | FF3 |
| SC2 | FF2 | FF1 ⊕ FF4 | FF3 ⊕ FF4 |
| SC3 | FF3 | FF2 | FF1 ⊕ FF4 |
| SC4 | FF4 | FF3 | FF2 |

Fig. 2 Example of PSF structure for 4-bit LFSR

## 3 OPTIMIZED PLPF DESIGN

### 3.1 *Logic structure*

The combinational logic of the PLPF requires a larger number of logic gates as the number of the PLPF inputs increases. As shown in Fig. 1, if the combinational logic to calculate the moving average is implemented as a majority function, the number of logic gates may increase exponentially to the number of PLPF inputs. This paper proposes an alternative PLPF design which consists of fewer logic gates than the original one and yet provides the same toggle reduction capability as the original one.

Fig. 3 shows the logic structure of the proposed PLPF where the current bit $T_j$ and the future bit $T_{j+n-i}$ $(0<i<n)$ extracted from the PSF are directly connected with an OR gate and an AND gate. A multiplexer is used to select the output of either the OR gate or the AND gate to the input of the scan chain and the multiplexer is controlled by the value of the past bit $S_{j-1}$ as a feedback from the first flip-flop of the scan chain. The output value of the PLPF only toggles when the past bit $S_{j-1}$ is different from the current

bit $T_j$ and the future bit $T_{j+n-i}$ ($0<i<n$). Note that for $n$=2, the logic function of the proposed PLPF is the same as that of the original one, i.e. the logic functions of $S_j$ for both of the circuits are the same. On the other hand, for $n$=3, the proposed PLPF is implemented with a different logic function from the original one. This is obvious from the fact that the input $S_{j-2}$ is not in the proposed PLPF. Such optimization becomes possible considering the nature of the moving average so that the value of $S_{j-2}$ is dependent on the values of $S_{j-1}$ and $T_j$.

### 3.2 *Toggle rate of modified scan-in patterns*

The toggle rate at the output of the PLPF can be calculated by the following formulas:

$$E_n = \sum_{n=1}^{n} (n + E_n) \cdot \frac{1}{2}^n + n \times \frac{1}{2}^n = 2^{n+1} - 2 \qquad (1)$$

$$T_n[\%] = \frac{1}{E_n} = \frac{1}{2^{n+1} - 2} \qquad (2)$$

Here, $n$ denotes the number of input bits of the PLPF from the PSF, $E_n$ denotes the average number of bits to toggle, and $T_n$ denotes the toggle rate of the output value of the PLPF.

Fig. 4 shows the state transition diagram of the PLPF for $n$=2. The left bit of the state denotes the value of the past bit $S_{j-1}$ and the right bit denotes the value of the current bit $T_j$. The value labeled at each arc denotes the future bit $T_{j+1}$. The output value of the PLPF will toggle, only when the current bit and the future bit have the same value but the current bit value and the past bit are different. The toggle rate of the output of the PLPF can be calculated using Formula (1) and Formula (2). As the occurrence probability of value 0 and value 1 in a pseudo random pattern are 0.5 respectively, the probability of every state transition in Fig. 4 becomes 0.5. Table 1 shows the expected toggle rate of the PLPF with 2$n$-1 bit inputs from an LFSR. It can be seen that the PLPFs reduce the toggle rates of the scan-in patterns as the number of input bits increases. Compared with the structure of the original PLPFs, the proposed PLPFs need fewer logic gates i.e. an AND gate and an OR gate with $n$-bit inputs and a multiplexer, to achieve the expected toggle rates. In addition, it makes the DFT easier and it will be generalized to $n$-bit inputs for more scan-shift power reduction.

TABLE 1
EXPECTED TOGGLE RATE WITH PLPFS

| *PLPF input bits* | Average toggle bits | Expected toggle rate (%) |
|---|---|---|
| 1 bit ($n$=1) | 2 | 50 |
| 3 bit ($n$=2) | 6 | 16.67 |
| 5 bit ($n$=3) | 14 | 7.14 |
| 7 bit ($n$=4) | 30 | 3.34 |

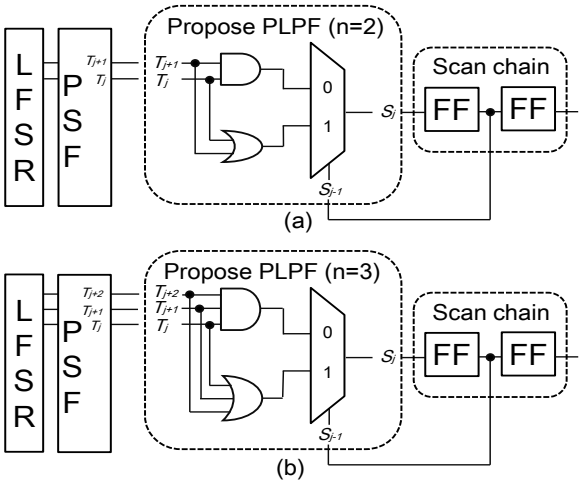


Fig. 3 Optimized PLPFs (a) n=2 (b) n=3

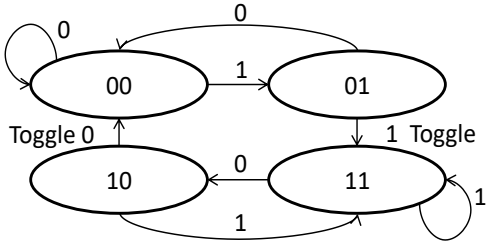


Fig. 4 State transition diagram of PLPF for $n$=2

## 4 SCAN-IN POWER CONTROL

One PLPF can generate scan-in patterns with a fixed toggle rate as shown in Table 1 by specifying the number of inputs. However, it cannot control the toggle rate to an arbitrary level using one PLPF only. For example, although a PLPF can generate scan-in patterns with a toggle rate of 16.67% or 7.14%, no PLPF can generate patterns with a toggle rate of 10%. In order to match various low-power requirements of devices and test applications, a method that can control the scan-in power to any user-specified level is necessary. In this section, a novel method to realize a flexible scan-in power control is proposed.

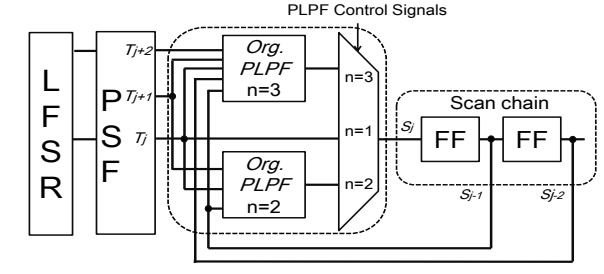
### 4.1 *Scan-in Power Control Circuit*

To control the scan-in power flexibly, it is necessary to generate a scan-in pattern with any specified toggle rate. To generate such a pattern, it is a good way to divide a scan-in pattern into several partial patterns and to make the partial patterns with different PLPFs so that a partial pattern has a different toggle rate each other. By combining the partial patterns into a complete scan-in pattern, the toggle rate of the complete scan-in pattern can be different from the one obtained by only one PLPF. Depending on the dividing points in the scan-in pattern and the PLPF type used for the partial pattern, it is possible to realize an arbitrary toggle rate of the complete scan-in pattern. Such dynamic PLPF control in generation of a scan-in pattern achieves the flexible scan-in power control.

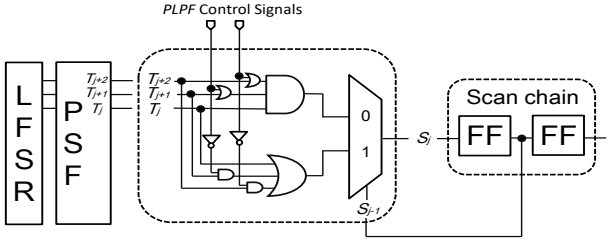
Fig. 5(a) shows the structure of a dynamically controlled PLPF including two PLPFs for $n$=2 and $n$=3. The

scan-in bit $S_j$ can take its value from the current bit $T_j$ directly, and it corresponds to choosing a PLPF for $n$=1. Hence there exist PLPFs for $n$=1, $n$=2 and $n$=3 in parallel between the PSF and the scan chain, and a multiplexer switched by predetermined control signals chooses a PLPF's pattern to be used in the scan-in pattern. If every partial pattern is obtained using a PLPF for either $n$=2 or $n$=3, the toggle rate of the scan-in pattern will be larger than 7.14% but less than 16.67%. In this way, the dynamically controlled PLPF can generate a scan-in pattern with an arbitrary toggle rate. However, this structure has a scalability problem that the circuit of scan-in power control will become very large and complex when more PLPFs with a large number of inputs are implemented for a design of multiple-scan chains. So this paper also proposes an optimized structure of the dynamically controlled PLPF.

The circuit in Fig. 5(b), which is the optimized structure of the circuit in Fig. 5(a), is implemented with less area overhead. Instead of using two PLPFs for $n$=2 and $n$=3, a circuit consisting of invertors, OR gates, and AND gates, is used with the *PLPF Control Signals* for the future bits $T_{j+1}$ and $T_{j+2}$. When the values of the PLPF Control Signals are "11", the future bits $T_{j+1}$ and $T_{j+2}$ are inactive and the value of the current bit $T_j$ with a toggle rate of 50% is applied to the scan chain. When the values of the PLPF Control Signals are "00", the values of the future bits become active and a partial pattern, which is the same as the pattern generated by the PLPF for $n$=3, is applied to the scan chain. Thus, a scan-in pattern with different toggle rates from 7.14% to 50% can be generated by dynamically controlling the PLPF Control Signals.




(a) Logic structure using the original PLPFs




(b) Optimized logic structure

Fig. 5 Dynamically controlled PLPF

### 4.2 Scan-in Power Control Approaches

By controlling the PLPF Control Signals during the scan-shift operation, it is possible to generate a scan-in pattern with any required toggle rate. The problem is how to decide PLPF types and when to change the values of the PLPF Control Signals for generating a scan-in pattern.

In this paper, the *switch timing* means the times scheduled to switch the PLPF for generating a scan-in pattern with the target toggle rates during scan-shift operation. Since there are many combinations of times that can achieve the target toggle rate, it is necessary to search the optimal switch timing, which controls the scan-in power to the specified level with high accuracy but prevents fault coverage loss due to the toggle reduction. During the scan-shift operation, more toggles occurring at the head part of a scan-in sequence can cause higher scan-in power than that at the tail part. Therefore, low toggle rate at the head part of the scan-in sequence should be more effective to reduce the total scan-shift power. On the other hand, the scan-in patterns have a trade-off between the toggle rate and fault coverage, that is, a low toggle rate pattern generally degrades fault coverage. It is necessary to avoid fault coverage degradation by remaining a part of the scan-in pattern with higher degree of randomness such as an LFSR pattern. In order to find an optimal solution in the trade-off, this paper proposes a method to determine a switch timing such that a scan-in pattern consists of the head and tail-part with lower toggle rate, and the middle part with high toggle rate. The scan-in power control circuit shown in Fig. 5 controls scan-in patterns in the order of PLPF for n=3 → PLPF for $n$=1 → PLPF for $n$=3. There are two constraints for deciding the switch timing:

(1) When a PLPF of $n$-input bits is used, a partial scan-in pattern through the PLPF should include at least successive $2^{n+1}$-2 bits that are shown in the column headed as "Average toggle bits" of Table 1. This is because the remaining values in the scan flip-flops just after switching disturb the partial pattern being at the expected toggle rate.

(2) The partial pattern with a low toggle rate generated by the PLPF need to be applied to the head and tail parts of a test pattern, respectively. Although toggle reduction at the tail part does not contribute to the total toggle reduction so much, it is necessary for the toggle reduction at the scan-out operation because most flip-flops often keep their logic values at the capture operation followed by the scan-out operation.

As parameter to express the switch timing, this paper uses three parameters $\alpha$, $\beta$ and $\gamma$, which denote the length of the tail part, the length of the middle part and the length of the head part of a complete scan-in pattern, respectively. The length of the scan chain denoted by $L$, which is the number of bits of a scan-in pattern, equals to $\alpha+\beta+\gamma$. The *weight transition metrics (WTM)* [26] is used to estimate the scan-in power, and the *WTM* of scan-in pattern $t$ under scan-in power control by $\alpha$, $\beta$ and $\gamma$ can be calculated by Formula (3) according to the expected toggle rate in Table 1:

$$WTM_{in}(t) = \frac{\sum_{i=1}^{\alpha} i \times 0.0714}{\sum_{j=1}^{L} j} + \frac{\sum_{i=\alpha+1}^{\alpha+\beta} i \times 0.5}{\sum_{j=1}^{L} j} + \frac{\sum_{i=\alpha+\beta+1}^{\alpha+\beta+\gamma} i \times 0.0714}{\sum_{j=1}^{L} j} \quad (3)$$

For a required scan-in power, a combination of ($\alpha$, $\beta$, $\gamma$)

has to be computed so that the $WTM_{in}$ is as close as possible to $WTM_{rq}$ corresponding to the required scan-in power.

In this paper, three types of scan-in power control approaches, *Basic*, *Swap*, and *Moving* are proposed for different purposes that are the fault coverage improvement and the area overhead reduction. Table 2 shows their features.

TABLE 2
THREE CONTROL APPROACH

| *Approach* | *Switch timing of PLPF* | *Fault coverage* | *Area overhead* |
|---|---|---|---|
| ***Basic*** | - One switch timing | Low | Small |
| ***Swap*** | - Two switch timings<br>- Swap switch timing each test | Medium | Medium |
| ***Moving*** | - One *switch timing*<br>- Move the switch timing each test | High | Large |

### 1) Basic Control

In the *Basic Control* approach, the head part and the tail part of the scan-in pattern generated by the PLPF of $n$=3 have the same length, i.e., $\alpha$=$\gamma$, for all scan chains. Therefore, it only needs to calculate $\beta$ which can be uniquely determined from the required $WTM_{rq}$. Fig. 6 shows an example. This approach is easy to apply, but high fault coverage may not be guaranteed because flip-flops where pseudo random values are applied are fixed during testing.

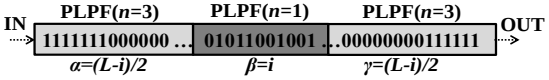



Fig. 6 Basic Control approach

### 2) Swap Control

In the *Swap Control* approach, the length of the head part $\alpha$ and the tail part $\gamma$ are set to $\alpha$=$L$/2-$\beta$ or $\gamma$= $L$/2. The values of $\alpha$ and $\gamma$ are swapped between $L$/2-$\beta$ and $L$/2 for each scan chain and each test vector. Fig. 7 illustrates the Swap Control approach. For a scan chain, the switch timing ($\alpha$, $\beta$, $\gamma$) for test vectors with odd index number is ($L$/2-$i$, $i$, $L$/2), and the switch timing for test vectors with even index number is set as ($L$/2, $i$, $L$/2-$i$). For a test vector, the switch timing ($\alpha$, $\beta$, $\gamma$) for scan chains with odd index number is ($L$/2-$i$, $i$, $L$/2), and the switch timing for scan chains with even index number is set as ($L$/2, $i$, $L$/2-$i$).

In this approach, the partial patterns of the PLPF for $n$=1 are applied to more FFs, that is, the range applying the pseudo random values is wider on the scan chains. As a result, the fault coverage improvement can be expected. On the other hand, this approach requires more additional circuit to realize the swapping operation compared with the Basic Control approach.

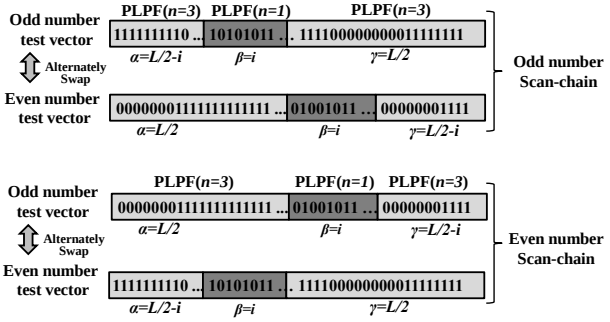



Fig. 7 Swap Control approach

### 3) Moving Control

The *Moving Control* approach is developed toward the most significant fault coverage improvement under the limitation on the required scan-in power. In this approach, a scan-in pattern with a high toggle rate at the middle part of the scan-in pattern is moved bit by bit in the scan chain every time a new scan-in pattern is applied. Fig. 8 illustrates the Moving Control approach. For test vector $N$, if the length of the tail part $\gamma$ is set to $j$ and the length of the middle part $\beta$ is set to $i$, then the length of the head part $\alpha$ becomes $L$/2-$i$-$j$. For the next pattern $N$+1, the length of the tail part $\gamma$ increases by 1 ($\gamma$ = $j$ +1), and the length of the head part $\alpha$ decreases by 1 ($\alpha$ = $L$/2-$i$-$j$-1). Since the middle part $\beta$ moves from the tail to the head on the scan chain, the partial patterns with pseudo random values are applied to all FFs. As a result, higher fault coverage can be expected. On the other hand, this approach requires the most additional circuit to control the moving operation among the proposed three approaches.

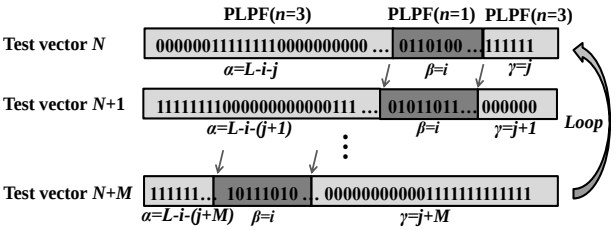



Fig. 8 Moving Control approach

## 4.3 On-chip Scan-in Power Control Scheme

The scan-in power control circuit in Fig. 5(b) needs some external input-pins for the PLPF Control Signals. Fig. 9 shows the circuit structure of a PLPF controller to generate the PLPF Control Signals for the Basic Control approach. The PLPF controller consists of two AND gates, one OR gate and one Trigger-FF. A *Scan-Shift Counter* is usually used to control the *Scan-Enable* (*SE*) signal in scan-based LBIST. According to the state of the FFs in the Scan-Shift Counter, the PLPF controller circuit switches the PLPFs dynamically. As shown in Fig.9, two AND gates are connected with this counter at the switch timing ($\alpha$, $\alpha$+$\beta$). For example, if the switch timing ($\alpha$, $\alpha$+$\beta$) is set to (3, 10) for a 4-bit scan-shift counter, the inputs of AND gate will be 0011 and 1010. When the output of AND gate is 1 at the switch timing $\alpha$, the T-FF changes its value from 0

to 1 and the value of $n$ of the current PLPF changes from $n$=3 to $n$=1. When the output of AND gate is 1 at the switching timing $\alpha$+$\beta$, the T-FF changes from 1 to 0 and the value of $n$ of the current PLPF changes from $n$=1 to $n$=3. The Swap Control approach requires double size of the additional controlling circuit compared with the Basic Control approach, and more combinational gates are needed to realize the Moving control approach.

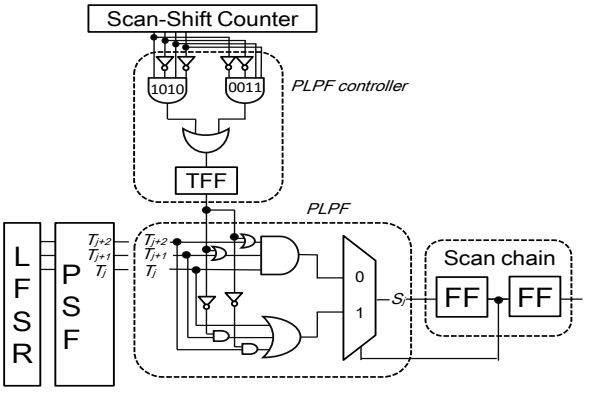



Fig. 9 Logic structure of a PLPF Controller for Basic approach

## 5 Experimental Results of Toggle Rate and Fault Coverage

### 5.1 Experimental Setup

This section shows experimental results of the proposed scan-in power control method using ISCAS'89 and ITC'99 benchmark circuits for three control approaches. 30k pseudo-random patterns were generated by a 16-bit LFSR with characteristic polynomial $X^{16}+X^{15}+X^{13}+X^4+1$ from a seed "1010….1010". A parallel scan structure was assumed to all the circuits with the maximum scan-chain length set to 100 or 200 (the number of FFs >1600). The primary inputs are fed with the patterns generated by another LFSR. An in-house fault simulator was used to calculate fault coverage for the single stuck-at fault model with single capture and the transition delay fault model with the launch-on-capture clocking scheme [2]. The scan-shift power was evaluated by $WTM_{in}$ as described in Section 4.

### 5.2 Scan-in power reduction by the optimized PLPF

At the first experiment, the toggle rate of scan-in patterns with single PLPF for $n$=2 and $n$=3 was calculated. Table 3 shows $WTM_{in}$ achieved with the original PLPFs in Fig. 1 and the proposed PLPFs in Fig. 3. It can be seen that the proposed PLPFs have the same capability of toggle control as the original PLPFs. All toggle rates are slightly different from the theoretical values given in Table 1. This should be because the initial values of scan flip-flops just before starting the scan-in operation affect the toggle rate. In addition, due to the different feedback structures of the PLPFs, generated scan-in patterns are different between two PLPFs. The proposed PLPFs for $n$=3 generated scan-in patterns with 0.03% lower average $WTM_{in}$ than the original PLPFs.

TABLE 3
TOGGLE RATE OF INDIVIDUAL PLPF ($WTM_{IN}$)

| *Circuits* | *$WTM_{in}$ (%)* | | | |
|---|---|---|---|---|
| | *Org.PLPF (n=2)* | *Pro.PLPF (n=2)* | *Org.PLPF (n=3)* | *Pro.PLPF (n=3)* |
| ***s9234*** | 16.72 | 16.72 | 7.41 | 7.34 |
| ***s13207*** | 16.93 | 16.93 | 7.47 | 7.46 |
| ***s15850*** | 17.01 | 17.01 | 7.60 | 7.56 |
| ***s38417*** | 16.78 | 16.78 | 7.35 | 7.32 |
| ***s38584*** | 16.86 | 16.86 | 7.45 | 7.42 |
| ***b14*** | 16.99 | 16.99 | 7.66 | 7.57 |
| ***b15*** | 16.83 | 16.83 | 7.35 | 7.35 |
| ***b20*** | 16.70 | 16.70 | 7.22 | 7.20 |
| ***b21*** | 16.70 | 16.70 | 7.22 | 7.20 |
| ***b22*** | 16.78 | 16.78 | 7.37 | 7.35 |
| ***Average*** | 16.83 | 16.83 | 7.41 | 7.38 |

### 5.3 Evaluation of scan-in power control approaches

The second experiment was conducted to confirm the flexibility of the scan-in power control. Table 4 shows the switch timing ($\alpha$, $\beta$, $\gamma$) for a target $WTM_{rq}$ for each benchmark circuit. In this experiment the target $WTM_{rq}$ was set to the average toggle rate at FFs in the normal functional operation computed by logic simulation for pseudo-random patterns. The variation of $WTM_{rq}$ implies that the ideal scan-in power may be different depending on the CUT, and therefore flexible scan-in power control is necessary.

The switch timings ($\alpha$, $\beta$, $\gamma$) of the three proposed approaches for each circuit are shown from the fifth to the tenth columns, which are calculated with Formula (3).

TABLE 4
SWITCH TIMING

| *Circuits* | *$WTM_{rq}$* | *# FF of SC* | *# scan chain* | *Basic* | | | *Swap Moving* | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | *α* | *β* | *γ* | *α* | *β* | *γ* |
| ***s9234*** | 17.81 | 76 | 3 | 28 | 19 | 29 | 38 | 19 | 19 |
| ***s13207*** | 26.32 | 96 | 7 | 26 | 43 | 27 | 14 | 43 | 39 |
| ***s15850*** | 19.03 | 100 | 6 | 36 | 28 | 36 | 50 | 28 | 22 |
| ***s38417*** | 17.63 | 182 | 9 | 69 | 44 | 69 | 91 | 44 | 47 |
| ***s38584*** | 27.53 | 97 | 15 | 25 | 46 | 26 | 14 | 46 | 37 |
| ***b14*** | 13.14 | 82 | 3 | 35 | 11 | 36 | 41 | 11 | 30 |
| ***b15*** | 5.95 | 90 | 5 | 42 | 5 | 43 | 45 | 5 | 40 |
| ***b20*** | 13.08 | 98 | 5 | 42 | 14 | 42 | 49 | 14 | 35 |
| ***b21*** | 13.08 | 98 | 5 | 42 | 14 | 42 | 49 | 14 | 35 |
| ***b22*** | 13.12 | 82 | 9 | 39 | 13 | 40 | 46 | 13 | 33 |

Table 5 shows the difference of $WTM$ with the launch-on-capture between the target $WTM_{rq}$ and the obtained $WTM_{in}$. It can be seen that every switch timing can derive $WTM_{in}$ within ±0.51% *for* $WTM_{rq}$, and the average difference for all circuits is less than 0.2% for any approach. Also, both $WTM_{in}$ of the Swap and Moving control approaches are 0.08% higher than that of the Basic Control approach because the initial switching in the Swap and Moving control approaches might have caused some uncontrollable toggles.

TABLE 5
SCAN-IN POWER CONTROL RESULT (WTMIN)

| *Circuits* | *ΔWTMin* | | |
|---|---|---|---|
| | *Basic* | *Swap* | *Moving* |
| ***s9234*** | -0.09 | 0.05 | 0.03 |
| ***s13207*** | 0.12 | 0.32 | 0.33 |
| ***s15850*** | 0.50 | 0.50 | 0.51 |
| ***s38417*** | 0.18 | 0.24 | 0.24 |
| ***s38584*** | -0.11 | 0.11 | 0.12 |
| ***b14*** | 0.00 | 0.06 | 0.08 |
| ***b15*** | 0.09 | 0.13 | 0.11 |
| ***b20*** | 0.11 | 0.12 | 0.12 |
| ***b21*** | 0.11 | 0.12 | 0.12 |
| ***b22*** | 0.07 | 0.15 | 0.17 |
| ***Average*** | 0.10 | 0.18 | 0.18 |

Table 6 and Table 7 show results of fault coverage of pseudo random patterns generated by an LFSR, patterns generated with single PLPF for $n$=3, and patterns generated by the three proposed approaches. For comparison, results of two well-known low-power approaches *LT-RTPG* [11] and *ALP-RTPG* [12] are added to the Table. The columns named "$WTM_{in}$" and "*FC*" show $WTM_{in}$ and fault coverage of the generated patterns, respectively.

From the results on fault coverage, it is confirmed that the Moving Control approach can achieve higher fault coverage than the Basic and Swap approaches. It is worthy to note that, for circuit b15, the Moving Control approach recorded the highest fault coverage among PLPF for $n$=3, *LT-RTPG* ($n$=4) and *ALP-RTPG* ($n$=3) in spite of lower $WTM_{in}$ than the others. The results show that fault coverage loss for the Moving Control approach is only 0.5% for the single stuck-at fault model and 1.93% for the transition delay fault model compared with the LFSR. For some circuits, the Moving Control approach derived even higher fault coverage than the LFSR.

TABLE 6
FAULT COVERAGE EVALUATION FOR STUCK-AT FAULTS

| *Circuits* | *LFSR* | | *PLPF(n=3)* | | *Basic* | | *Swap* | | *Moving* | | *LT-RPTG(n=4)[11]* | | *ALP-RPTG(n=3)[12]* | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* |
| ***s9234*** | 50.00 | 85.71 | 7.18 | 77.77 | 17.73 | 81.94 | 17.86 | 85.58 | 17.84 | 86.72 | 6.68 | 79.66 | 9.75 | 64.23 |
| ***s13207*** | 50.00 | 88.39 | 7.49 | 69.75 | 26.51 | 79.43 | 26.72 | 80.47 | 26.72 | 80.61 | 6.71 | 72.60 | 7.66 | 79.20 |
| ***s15850*** | 50.00 | 87.38 | 7.51 | 79.69 | 19.55 | 79.29 | 19.56 | 82.00 | 19.56 | 85.83 | 6.98 | 80.19 | 8.03 | 80.83 |
| ***s38417*** | 50.00 | 93.69 | 7.26 | 90.13 | 17.65 | 90.23 | 17.65 | 91.20 | 17.66 | 92.97 | 7.01 | 90.20 | 7.96 | 83.39 |
| ***s38584*** | 50.00 | 90.96 | 7.32 | 83.62 | 27.57 | 86.24 | 27.77 | 88.99 | 27.79 | 88.83 | 6.61 | 86.07 | 7.39 | 81.72 |
| ***b14*** | 50.01 | 84.61 | 7.51 | 79.42 | 13.13 | 79.22 | 13.20 | 79.49 | 13.21 | 89.4 | 6.90 | 79.09 | 10.02 | 81.93 |
| ***b15*** | 49.99 | 68.10 | 7.34 | 39.28 | 6.04 | 37.36 | 6.08 | 37.39 | 6.06 | 58.71 | 6.53 | 40.40 | 8.30 | 51.44 |
| ***b20*** | 50.00 | 83.95 | 7.15 | 81.35 | 13.17 | 79.61 | 13.17 | 80.55 | 13.18 | 88.92 | 6.41 | 83.55 | 8.34 | 81.09 |
| ***b21*** | 50.00 | 85.73 | 7.15 | 83.04 | 13.17 | 80.45 | 13.17 | 81.88 | 13.18 | 90.23 | 6.41 | 85.23 | 8.34 | 82.98 |
| ***b22*** | 49.99 | 85.22 | 7.28 | 80.53 | 13.16 | 78.95 | 13.24 | 82.88 | 13.25 | 86.45 | 6.61 | 82.93 | 7.53 | 81.27 |
| ***Average*** | 50.00 | 85.37 | 7.32 | 76.46 | 16.77 | 77.27 | 16.84 | 79.04 | 16.85 | 84.87 | 6.69 | 77.99 | 8.33 | 76.81 |

TABLE 7
FAULT COVERAGE EVALUATION FOR TRANSITION DELAY FAULTS

| *Circuits* | *LFSR* | | *PLPF(n=3)* | | *Basic* | | *Swap* | | *Moving* | | *LT-RPTG(n=4)[11]* | | *ALP-RPTG(n=3)[12]* | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* | $WTM_{in}$ | *FC* |
| ***s9234*** | 50.00 | 61.61 | 7.34 | 49.73 | 17.72 | 51.00 | 17.86 | 55.41 | 17.84 | 56.10 | 6.68 | 51.12 | 9.75 | 41.65 |
| ***s13207*** | 50.00 | 61.39 | 7.46 | 47.66 | 26.44 | 57.08 | 26.64 | 63.44 | 26.65 | 62.57 | 6.93 | 50.21 | 7.87 | 54.78 |
| ***s15850*** | 50.00 | 51.20 | 7.56 | 46.70 | 19.53 | 46.47 | 19.53 | 48.76 | 19.54 | 50.89 | 7.37 | 48.40 | 8.07 | 45.25 |
| ***s38417*** | 50.00 | 84.58 | 7.32 | 78.92 | 17.81 | 79.36 | 17.87 | 81.06 | 17.87 | 82.93 | 6.60 | 79.69 | 7.48 | 71.73 |
| ***s38584*** | 50.00 | 59.94 | 7.42 | 49.07 | 27.42 | 54.89 | 27.64 | 58.52 | 27.65 | 58.19 | 6.70 | 53.56 | 8.02 | 46.73 |
| ***b14*** | 50.00 | 73.50 | 7.57 | 72.58 | 13.14 | 72.80 | 13.20 | 73.00 | 13.22 | 74.10 | 7.04 | 73.07 | 10.24 | 73.23 |
| ***b15*** | 49.99 | 58.85 | 7.35 | 34.73 | 6.04 | 29.23 | 6.08 | 29.42 | 6.06 | 40.60 | 6.54 | 35.61 | 8.31 | 35.53 |
| ***b20*** | 50.00 | 73.60 | 7.20 | 74.94 | 13.19 | 72.88 | 13.20 | 74.06 | 13.20 | 76.19 | 7.19 | 75.73 | 8.37 | 76.43 |
| ***b21*** | 50.00 | 75.58 | 7.20 | 77.11 | 13.19 | 75.26 | 13.20 | 76.07 | 13.20 | 78.12 | 7.17 | 77.49 | 8.37 | 77.90 |
| ***b22*** | 49.99 | 75.18 | 7.35 | 75.26 | 13.19 | 75.07 | 13.27 | 75.74 | 13.29 | 76.36 | 7.14 | 73.30 | 7.63 | 73.72 |
| ***Average*** | 50.00 | 67.54 | 7.38 | 60.67 | 16.77 | 61.40 | 16.85 | 63.55 | 16.85 | 65.61 | 6.94 | 61.82 | 8.41 | 59.70 |

### 5.4 Area Overhead

Table 8 shows area overhead and its breakdown of the proposed method. The breakdown is shown by the number of additional cells, which are combinational logic gates and flip-flops (shown in parenthesis). The CUT used in this experiment is a benchmark circuit b22 in which there are 9 scan chains with the maximum chain length 83. The circuit was synthesized with *Synopsys Design Compiler*™ in a CMOS 65nm technology. For comparison, the column named "*Ori.PLPF*" denotes results using the original PLPF in Fig. 5(a), and the column named "*PRESTO (fully)*" denotes results of an existing low-power method (*PRESTO*) [17]. The second row headed "*one scan chain*" shows the number of cells of the dynamically controlled PLPF added to each scan chain. The third row headed "*PLPF controller*" shows the number of cells of the PLPF controller in Fig. 9. The fourth and the fifth rows show the total number of additional cells and the percentage of the additional cell area in the entire circuit, respectively. The column named "*Ori.PLPF*" denotes results using the original PLPF in Fig. 5(a), and the columns under "*Proposed PLPF*" show results using the proposed approaches. For comparison, the column named "*PRESTO (fully)*" denotes the area overhead of the low-power method (*PRESTO*) [17].

The proposed scan-in power control using the Basic Control approach and the Swap Control approach need less area overhead than the "*Ori.PLPF*". The total area overhead is reduced from 0.76% of the original PLPF to 0.36% and 0.43% of the Basic Control and the Swap Control, respectively. However, the Moving Control approach incurs larger area overhead than the original PLPF or other approaches because more FFs are needed to move the switch timing dynamically. From these results, a trade-off between area overhead and fault coverage can be observed. The "*PRESTO*" method needs less combinational logic gates than the proposed scan-in power control method; however, it requires more FFs that result in larger area overhead than the proposed method.

TABLE 8
AREA OVERHEAD OF PROPOSED METHOD FOR B22

| *Combinational cell+(FF)* | *Ori. PLPF* | *Proposed PLPF* | | | *PRESTO (fully)* [17] |
|---|---|---|---|---|---|
| | *Basic* | *Basic* | *Swap* | *Moving* | |
| *PLPF for one scan chain* | 18 | 7 | 7 | 7 | 4+(3) |
| *PLPF controller* | 5+(1) | 5+(1) | 24+(2) | 59+(7) | 18+(13) |
| *Total cell* | 167+(1) | 68+(1) | 87+(2) | 122+(7) | 54+(40) |
| *Total area overhead (%)* | 0.76 | 0.36 | 0.43 | 0.84 | 0.95 |

## 6 EXPERIMENTAL RESULTS USING TEG CHIPS

### 6.1 TEG Chip Design

Experiments using a TEG chip were conducted to observe a relation between $WTM_{in}$ and the physical power in terms of the current and delay variation. The designed TEG chip implements ten copies of b22 as a CUT and the scan-in power control method introduced in Fig. 5(a) was embedded. The chips were fabricated using the 65nm CMOS technology. Fig. 10 shows the floorplan and the picture of a TEG chip.

A structure of parallel scan chains was implemented with ten copies of b22. Each b22 contained 9 scan chains with the maximum length of 83. The primary inputs and outputs of each b22 are isolated from the internal scan chains using the boundary scan cells. One 22-bit LFSR module with the characteristic polynomial of $X^{22}+X^{21}+1$ from a seed of all 1 and one 11-bit MISR module with the characteristic polynomial of $X^{9}+X^{8}+1$ are placed on the left and right side of the chip. The PLPF module including a PSF is inserted between the LFSR and the input pins of all scan chains. The PLPF consists of a PLPF ($n$=2), a PLPF ($n$=3) and a multiplexer shown in Fig. 5(a).

In order to evaluate delay variations affected by heat (temperature) during the scan-shift operation, three types of ring oscillators, $RO_1$, $RO_2$ and $RO_3$ proposed in [27][28] are placed at the center of the TEG chip. $RO_1$, $RO_2$ and $RO_3$ consist of 51-stages of 2-inputs 1-fanout NAND gates, 51-stages of 3-inputs 1-fanout NAND gates, and 51-stages of 4-inputs 1-fanout ORNAND gates, respectively. The oscillation frequency of each RO varies with the fluctuation of the chip temperature caused by scan-in power control. While the high temperature increases the circuit delay and retards the oscillation frequency, the low temperature decreases the circuit delay or increases the oscillation frequency. The LBIST function and the ROs were controlled from external pins. Table 9 shows detailed configuration of the TEG chip.

An external tester *CX1000D* provided by *CloudTesting Service*™ [29] was used to control and observe the I/O pins of the chip. Since the tester has a function to measure the average supply current, power dissipation during the scan-shift operation can be observed as the average supply current.

TABLE 9
CONFIGURATION OF TEG CHIP

| *Process* | *CMOS 65nm SOTB* |
|---|---|
| CUT | b22 circuits × 10 |
| # of gates | 15264 × 10 |
| # of FFs | 741 × 10 |
| # of scan chains | 9 × 10 |
| Length of scan chains | 83 or 82 |
| Clock | 50 MHz |

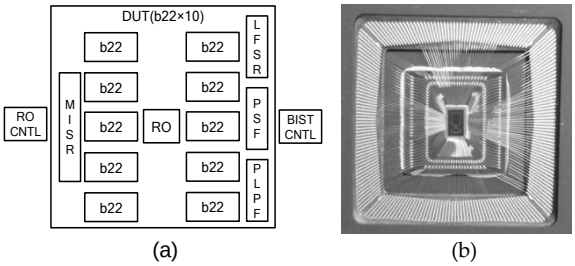



Fig.10 (a) The floorplan and (b) the picture of TEG

### 6.2 Result of scan-in power control method with chip measurement

In the experiments, the Basic Control approach described in Section 4 is applied with the target $WTM_{rq}$ 7%, 10%, 15%, 20%, 25%, 30% and 50%. Note that the simulated $WTM_{in}$ for each $WTM_{rq}$ is less than 0.1%. Table 10 shows the switch timings which are calculated by Formula 3 for each $WTM_{rq}$. The clock frequency was set to 50MHz. The measurement time of the ROs was set to 40.96μs (20ns × 2048 clocks).

Table 11 shows the average supply current and the average frequency of three ROs measured for the ten TEG chips under the scan-in power control. It can be seen that the supply current increases but the frequency of the ROs decreases as the $WTM_{rq}$ increases. The bottom row of Table 11 shows a strong positive correlation between the $WTM_{in}$ and the current as well as a strong negative correlation between the $WTM_{in}$ and the frequency of the ROs. These correlations indicate that the proposed scan-in power control method can control the scan-in power to an arbitrary level with high accuracy.

Fig. 11 and Fig. 12 show the supply current and the frequency of $RO_1$ in 10 TEG chips, respectively. The deviation of the current and the frequency result from the process variation in TEG chips. The values of the supply current and the frequency change linearly to the target $WTM_{rq}$. From Fig. 12, it is observed that the scan-in power control method can control an additional delay due to the IR-drop and the heat caused by high power consumption during the scan-shift operation. These results confirm the effectiveness to avoid test malfunctions.

TABLE 10
SWITCH TIMING FOR TEG CHIP

| *Target* $WTM_{rq}$ | *Switch timing* | | |
|---|---|---|---|
| | $\alpha$ | $\beta$ | $\gamma$ |
| ***7%*** | 83 | 0 | 0 |
| ***10%*** | 35 | 12 | 36 |
| ***15%*** | 34 | 15 | 34 |
| ***20%*** | 29 | 25 | 29 |
| ***25%*** | 24 | 35 | 24 |
| ***30%*** | 19 | 44 | 20 |
| ***50%*** | 0 | 83 | 0 |

TABLE 11
AVERAGE CURRENT VALUES AND FREQUENCY OF ROS

| *Target* $WTM_{rq}$ | *Current value (mA)* | *Frequency (MHz)* | | |
|---|---|---|---|---|
| | | *RO1* | *RO2* | *RO3* |
| ***7%*** | 14.87 | 287.54 | 194.78 | 138.02 |
| ***10%*** | 15.32 | 286.92 | 194.31 | 137.71 |
| ***15%*** | 15.93 | 286.14 | 193.73 | 137.35 |
| ***20%*** | 16.59 | 285.33 | 193.15 | 136.96 |
| ***25%*** | 17.26 | 284.56 | 192.57 | 136.59 |
| ***30%*** | 17.86 | 283.80 | 192.02 | 136.23 |
| ***50%*** | 20.07 | 280.76 | 189.80 | 134.79 |
| ***Correlation*** | 0.9988 | -0.9996 | -0.9995 | -0.9994 |

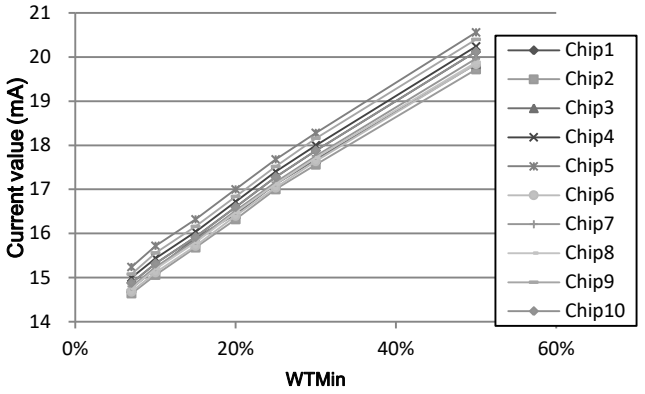



Fig. 11 Average Current value of 10 TEG chips

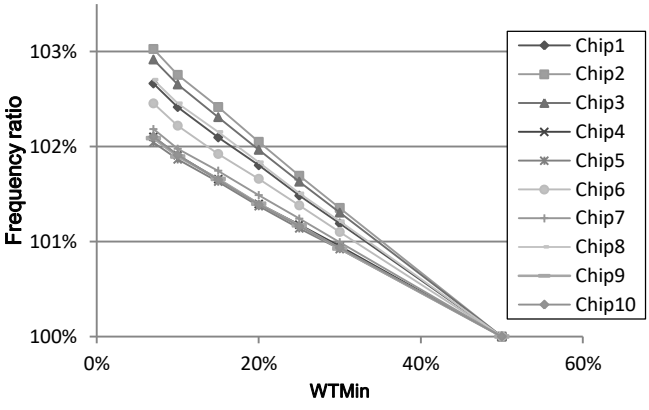



Fig. 12 Average of RO1 frequency ratio of 10 TEG chips

## 7 CONCLUSIONS

This paper has proposed a low-power test method to realize flexible scan-in power control for LBIST. Three types of power control approaches named Basic, Swap and Moving Control have been introduced to meet the different requirements in terms of fault coverage improvement, small hardware overhead, and high power control accuracy. Experimental results on the benchmark circuits confirms that the proposed method can control the toggle rate of CUTs during the scan-in operation with small hardware overhead and without sacrificing fault coverage.

To evaluate the effectiveness of the scan-in power control method on the actual device, a TEG chip was designed and fabricated. The measurement results on the supply current and the circuit delay show a linear change to the scan-in power. These results confirm high flexibility and accuracy of the proposed scan-in power control method.

In the future, the scan-out power and the peak scan-shift power will be taken into account as well as combining the proposed method with scan-out power reduction [14][18] and multi-cycle test [13][14][23] for reducing scan-out power and capture power, and improving fault coverage further.

## ACKNOWLEDGMENT

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc. and Mentor Graphics Corporation. The VLSI chips in this study have been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Renesas Electronics Corporation.

## REFERENCES

[1] M. Bushnell, V. Agrawal, *Essential of Electronic Testing for Digital, Memory & Mixed-Signal* VLSI *Circuits*, New York: Kluwer Academic Publisher, 2000.

[2] P. Girard, N. Nicolici, and X. Wen, *Power-Aware Testing and Test Strategies for Low Power Devices*, Springer, 2009.

[3] Balatsouka, S., Tenentes, Vasileios, Kavousianos, X. and Chakrabarty, K. "Defect aware X-filling for low-power scan testing," *IEEE DATE*, 2010.

[4] S. Gerstendorfer and H.-J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST," *Proc. ITC*., pp. 77-84, 1999.

[5] A. Hertwig and H.-J. Wunderlich, "Low Power Serial Built-In Self-Test," *Proc. European Test Workshop*, pp. 49-53, 1998.

[6] L. Whetsel, "Adapting Scan Architecture for Low Power Operation," *Proc. IEEE ITC*, pp. 863-872, 2000.

[7] R. Wangy, B. Bhaskaranz, K. Natarajanz, A. Abdollahia, "A Programmable Method for Low-Power Scan Shift in SoC Integrated Circuits,", *Proc. IEEE VLSI Test Symp.*, pp. 1-6, 2016.

[8] F. Corno, M. Rebaudengo, M. S. Reorda and M. Violante, "A new BIST architecture for low power circuits," *Proc. IEEE European Test Workshop*, pp. 160-164, 1999.

[9] P. Girard, L. Guiller, C. Landrault and S. Pravossoudovitch, "A Test Vector Inhibiting Technique for Low Energy BIST Design," *Proc. IEEE VLSI Test Symp.*, pp. 407-412, 1999.

[10] C. Zoellin, H.-J. Wunderlich, N. Maeding and J. Leenstra, "BIST Power Reduction Using Scan-Chain Disable in the Cell Processor," *Proc. IEEE ITC*, paper 32.3, 2006.

[11] S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BISTTPG for Low Heat Dissipation," *Proc. IEEE ITC*, pp. 85-94, 1999.

[12] X.Lin and J. Rajski, "Adaptive Low Shift Power Test Pattern Generator for Logic BIST," *Proc. ATS*, pp. 355-360, 2010.

[13] Y. Sato, S. Wang, T. Kato, K. Miyase and S. Kajihara, "Low Power BIST for Scan-Shift and Capture Power," *Proc. IEEE ATS*, pp. 173-178, 2010.

[14] S. Wang, Y. Sato, S. Kajihara and H. Takahashi, " Physical Power Evaluation of Low Power Logic-BIST Scheme Using Test Element Group Chip," *Journal of Low Power Electronics*, pp. 528-540, 2015.

[15] M. Filipek, Y. Fukui, H. Iwata, G. Mrugalski, J. Rajiski, M. Takakura and J. Tyszer, "Low Power Decompressor and PRPG with Constant Value Broadcast," *Proc. IEEE ATS*, pp. 84-89, 2011.

[16] J. Rajski, J. Tyszer, G. Mrugalski and B. N.-Dostie, "Test Generator with Preselected Toggling for Low Power Built-In Self-Test," *Proc. IEEE VLSI Test Symp.*, pp. 1-6, 2012.

[17] M. Filipek, G. Mrugalski, N. Mukherjee, B.-Dostie, J. Rajski, J. Solecki and J. Tyszer, "Low-Power Programmable PRPG WithTest Compression Capabilities," *IEEE Trans. on VLSI systems*, Vol. 23, Issue 6, pp. 1063-1076, 2015.

[18] S. Wang, Y. Sato, K. Miyase and S. Kajihara, "A Scan-Out Power Reduction Method for Multi-cycle BIST," *Proc. IEEE ATS*, pp. 272-277, 2012.

[19] C. Schotten, H. Myer, "Test-Point Insertion for an Area-effi*cient BIST", Proc. ITC*, pp. 515-523, 1995.

[20] N. A. Touba and E. J. McCluskey, "Test point insertion based on path tracing," *Proc. IEEE VLSI Test Symp.*, pp. 2–8, 1996.

[21] J.-S. Yang, N. A. Touba, and B. Nadeau-Dostie, "Test point insertion with control points driven by existing functional flip-flops," *IEEE Transactions on Computers*, vol. 61, no. 10, pp. 1473–1483, 2012.

[22] C. V. Krishna and N. A. Touba, "Reducing test data volume using LFSR reseeding with seed compression," *Proc. ITC*, 2002, pp. 321-330.

[23] S. Wang, H. T. Al-Awadhi, S. Hamada, H. Iwata and J. Matsushima, "Structure-Based Methods for Selecting Fault-Detection-Strengthened FF under Multi-Cycle Test with Sequential Observation," *Proc. IEEE ATS*, pp.209-214, 2016.

[24] T. Kato, S. Wang, Y. Sato, S. Kajihara and X. Wen," A Flexible Power Control Method for Right Power Testing of Scan-Based Logic BIST", *Proc. IEEE ATS*, pp. 204-209, 2016.

[25] J. Rajski, N. Tamarapalli, and J. Tyszer, "Automated synthesis of phase shifters for built-in self-test applications," *Proc. IEEE CAD*, pp. 1175-1188, 2000.

[26] R. Sankaralingam, R. R. Oruganti and N. A. Touba, "Static Compaction Techniques to Control Scan Vector Power Dissipation," *Proc. IEEE VLSI Test Symp.*, pp. 35-40, 2000.

[27] Y. Miyake, Y. Sato, S. Kajihara, and Y. Miura, "Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test," *Proc. of ATS*, pp. 156-161, 2014.

[28] Y. Miyake, Y. Sato, S. Kajihara, and Y. Miura, "Temperature and Voltage Measurement for Field Test Using an Aging-Tolerant Monitor," *IEEE Trans. on VLSI Systems*, Vol. 24, Issue 11, pp. 3282-3295, 2016.

[29] Cloud Testing Service. https://www.cts-advantest.com/en

**Takaaki Kato** received B.E. degree in the Computer Science and Electronics from Kyushu Institute of Technology in 2012 and M.E. degree in the Computer Science and Electronics from Kyushu Institute of Technology in 2014. Currently, he studies to receive Ph.D degree in the Computer Science and Systems Engineering from Kyushu Institute of Technology. His research interest includes Low power testing, Low power Logic BIST and Field testing.

**Senling Wang** received B.S. degree in the college of Electrical and Information Engineering from BeiHua University, China, in 2008, and the M.S. and Ph.D. degree from the Department of Computer Science and Electronics of Kyushu Institute of Technology, Japan, in 2011 and 2014, respectively. Currently, he is a Senior Assistant Professor in Ehime University, Japan. His research interest includes Field testing, Low power testing, Delay testing, Fault Diagnosis for Digital Systems, and Design for Testability. Dr. Wang is a member of the IEEE.

**Yasuo Sato** received the B.E. and M.S. degree in mathematics from Tokyo University in 1976 and 1978, respectively. He received Ph.D. in engineering from Tokyo Metropolitan University in 2005. He was in Hitachi, Ltd. working in computer-aided design from 1978 to 2008. From 2003 to 2006, he was a senior manager of DFT (Design for Testability) group at the Semiconductor Technology Academic Research Center (STARC). He was a research professor in the Department of Computer Science and Electronics, Kyushu Institute of Technology from 2009 to 2013, and currently is a visiting professor. His particular interest area includes Field test, Delay testing, Low power BIST, Fault diagnosis and FPGA application-independent test. Dr. Sato is a member of the IEEE.

**Seiji Kajihara** received the B.S. and M.S. degrees from Hiroshima University, Japan, and the Ph.D degree from Osaka University, Japan, in 1987, 1989 and 1992, respectively. From 1992 to 1995, he worked with the Department of Applied Physics, Osaka University, as an Assistant Professor. In 1996, he joined the Department of Computer Science and Electronics of Kyushu Institute of Technology, Japan, where he is a full professor currently. His research interest includes test generation, delay testing, and design for testability. He received the Young Engineer Award from IEICE in 1997, the Yamashita SIG Research Award from IPSJ in 2002, and the Best Paper Award from IEICE in 2005. Prof. Kajihara is a member of the IEEE, and the IPSL. He serves in the editorial board of the Journal of Electronic Testing: Theory and Applications.

**Xiaoqing Wen** received the B.E. degree from Tsinghua University, China, in 1986, the M.E. degree from Hiroshima University, Japan, in 1990, and the Ph.D. degree from Osaka University, Japan, in 1993. From 1993 to 1997, he was an Assistant Professor at Akita University, Japan. He was a Visiting Researcher at University of Wisconsin, Madison, USA, from Oct. 1995 to Mar. 1996. He joined SynTest Technologies, Inc., USA, in 1998, and served as its Chief Technology Officer until 2003. In 2004, he joined Kyushu Institute of Technology, Japan, where he is currently a Professor and the Chair of the Department of Creative Informatics. He founded Dependable Integrated Systems Research Center in 2015 and served as its Director until 2017. His research interests include VLSI test, diagnosis, and testable design. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (Springer, 2009). He holds 43 U.S. Patents and 14 Japan Patents on VLSI testing. He received the 2008 IEICE-ISS Best Paper Award for his pioneering work on X-filling-based low-capture-power test generation. He is a fellow of the IEEE, a senior member of the IPSJ, and a member of the IEICE. He is serving as associate editors for IEEE Transactions on Computer-Aided Design, IEEE Transactions on VLSI, and the Journal of Electronic Testing: Theory and Applications.