Comparisons of instability in device characteristics at high temperature for thin-film SOI power n- and p- channel MOSFETs

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Comparisons of instability in device characteristics at high temperature for thin-film SOI power n- and p- channel MOSFETs

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This paper investigate instability in device characteristics related to the hot carrier effect, Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature (PBTI) under DC stress for n- and p-channel thin-film Silicon on Insulator (SOI) power MOSFET at high temperature. The threshold voltage shift increases as the temperature rises due to PBTI for n-MOSFET and NBTI for p-MOSFET. Drain Avalanche Hot Carrier (DAHC) occurs when the gate stress voltage is near the threshold voltage and Channel Hot Carrier (CHC) occurs when the gate voltage is high. The threshold voltage shift and the degradation rate of on-resistance of the n-MOSFET is larger than that of the p-MOSFET due to the difference in the impact ionization coefficient between electrons and holes.

Keywords—Hot carrier effect, Negative bias temperature instability, Positive bias temperature instability, Thin-film SOI power MOSFET

I. INTRODUCTION

Silicon-on-insulator (SOI) power MOSFETs have attracted attention as one of the promising devices for high temperature, high frequency, and high voltage applications [1-4]. In particular, the thin-film SOI power MOSFET is quite promising because the thin active layer suppresses the thermally induced leakage current and latch-up[4-6].

One of the most important concerns related to the thin film SOI power MOSFET is how to reduce the on-resistance and gate charge. The effective way to do it is to reduce the channel length, however the hot carrier effect is enhanced and device characteristics become unstable[7,8].

We previously reported the device characteristic of the thin-film SOI power n- and p-channel MOSFETs at high temperature [6,9]. In addition, we reported AC and high temperature hot carrier effect of the thin-film SOI power n-MOSFET and also confirmed that the hot carrier effect of power n-MOSFET is more serious than that of the p-MOSFET at room temperature under DC stress[10-13]. However, hot carrier effect of the thin-film SOI p-MOSFET at high temperature and difference in hot carrier effect between power n- and p-MOSFETs have not been clarified.

In this paper, we describe the instability of device characteristics at high temperature of thin-film SOI power n- and p-MOSFETs cased by hot carrier effect, NBTI(Negative Bias Temperature Instability), and PBTI(Positive Bias Temperature Instability)

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II. DEVICE STRUCTURE AND FABRICATION PROCESS

The schematic cross section of the thin-film SOI power n- and p-MOSFETs used in this study is shown in Fig. 1. The body contacts are formed to suppress the parasitic bipolar effect. The thin-film SOI power MOSFET was fabricated using the 0.5-μm-rule poly-Si gate process with local oxidation of silicon (LOCOS) isolation[14].

The main structural parameters are listed in Table 1.

TABLE I. THE MAIN STRUCTURAL PARAMETER

Top Si layer(μm)	0.14
Buried oxide(μm)	0.4
Gate oxide(nm)	11
Channel length(μm)	0.5
Drift Length(μm)	0.5
Gate Width(μm)	10

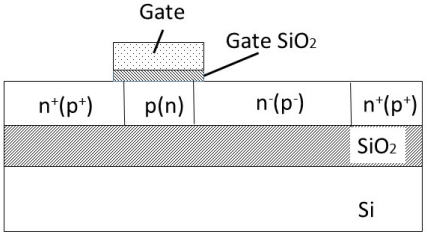


Fig. 1 Schematic cross section of the thin-film SOI power MOSFET.

III. EXPERIMENTAL PROCEDURE

Experimental procedure at high temperature is shown in Fig. 2. First, we measure the on-resistance and the threshold voltage at room temperature. Then, we heated the wafer and applied electrical stress. After applying electrical stress, we measured the on-resistance and threshold voltage at high temperature again. Finally, we calculated the degradation rate of on-resistance and the threshold voltage shift by comparing the results.

IV. Results and Discussion

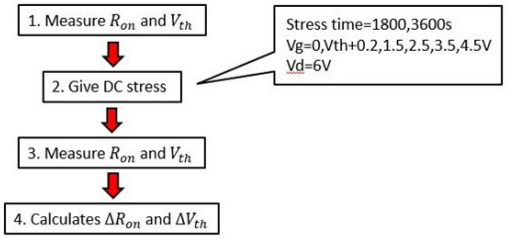
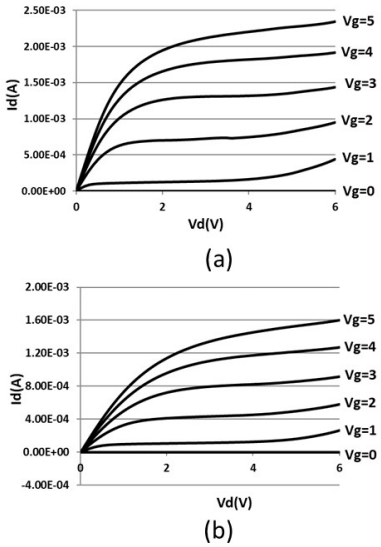
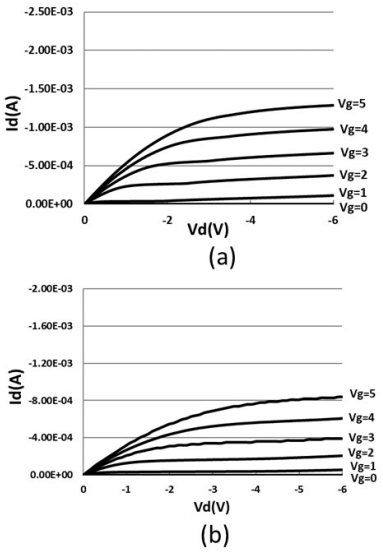


Fig. 2 Experimental procedure.



Figs. 3 Drain current - drain voltage characteristic at (a) room temperature and (b) 573 K.



Figs. 4 Drain current - drain voltage characteristic at (a) room temperature and (b) 573 K.

Drain current-drain voltage I_d - V_d characteristics for n-channel power MOSFET at room temperature and 573 K are shown in Figs. 3 (a) and (b), respectively. Figures 4 (a) and (b) show the I_d - V_d characteristics for p-channel power

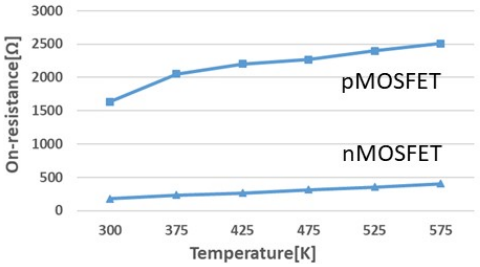
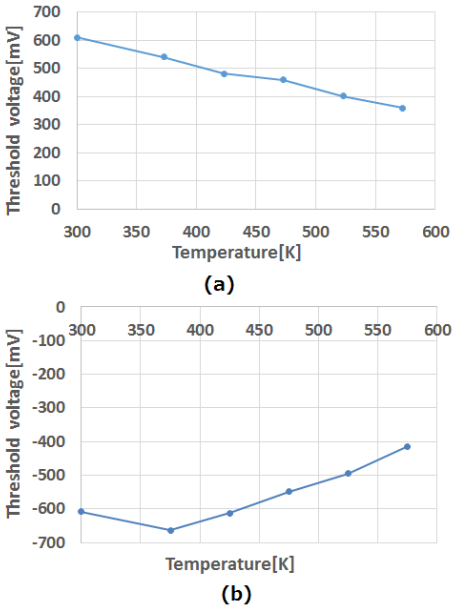


Fig. 5 Dependence of the on-resistance of n- and p-channel MOSFETs.



Figs. 6 Dependence of threshold voltage on temperature for (a) n- and (b) p-channel MOSFETs.

MOSFET at room temperature and 573K. For the n-channel MOSFETs, the drain current increases at the high drain voltage due to the parasitic bipolar effect[4,7]. The drain current decreases at high temperature as shown in Figs. 3(b) and 4(b) because the mobility decreases as temperature increases[15]. In addition, the parasitic bipolar effect is suppressed at high temperature for n-channel MOSFET as shown in Fig. 3(b) because the impact ionization coefficient decreases as the temperature increases[15].

Dependences of the on-resistance of n- and p-channel MOSFETs on temperature are shown in Fig. 5. From 300 K to 575 K, on-resistance of the n-channel MOSFET is increased by 128% and that of p-channel MOSFET is increased by 53%. The rate of increase in on-resistance is larger for n-channel MOSFET than for p-channel one because the rate of decrease in mobility for electron is larger than that for hole[15].

Figures 6(a) and (b) show dependences of threshold voltage on temperature for n- and p-channel MOSFETs. For both n- and p- channel MOSFETs, the absolute value of threshold voltage decreases as the temperature rises.

Dependence of the threshold voltage shift of p- channel MOSFET on the stress gate voltage is shown in Fig. 7. Stress time is 3600 sec. and drain voltage is 6V.

Threshold voltage shift = V_{th}(3600s)-V_{th}(0s)

V_{th}(0s): the threshold voltage before the stress,

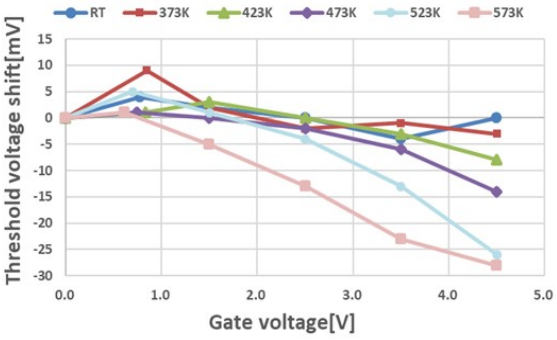


Fig. 7 Dependence of the threshold voltage shift of p-channel MOSFET on the stress gate voltage. The gate voltage is absolute value.

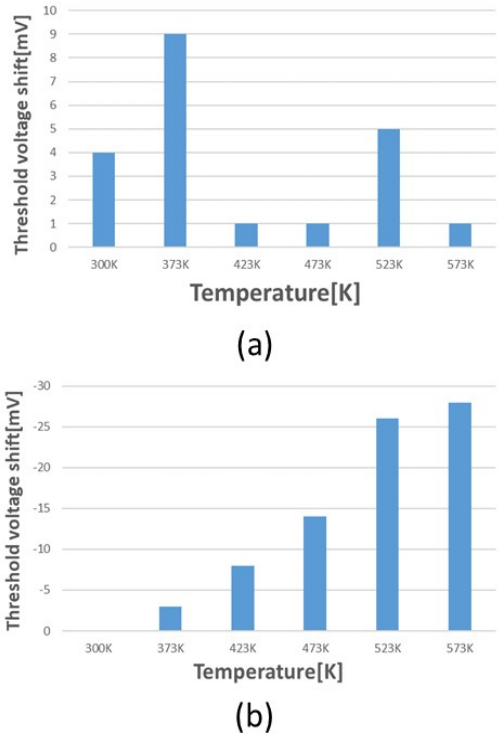


Fig. 8 Dependence of the threshold voltage sift on temperature at stress voltage of (a) (Vth – 0.2) V and (b) -4.5 V.

V_{th}(3600s): the threshold voltage after the stress for 3600 seconds.

The threshold voltage shift is positive when the gate voltage is near threshold voltage (Vth + 0.2 V) because hot electron injection is occurred by DAHC. The positive threshold voltage shift decreases as temperature increases because DAHC is suppressed as temperature increases. The threshold voltage shift is negative when the gate stress voltage is more than 2.5V at room temperature. The threshold voltage shift increases with increasing temperature and stress gate voltage when the temperature is more than 473 K because NBTI occurs[16].

Figures 8 (a) and (b) summarizes the results of Fig. 7 for gate stress voltage of (a) (Vth-0.2)V and (b) - 4.5 V. When the stress gate voltage is near the threshold voltage ((Vth - 0.2) V), the threshold voltage shift becomes maximum at 375K. The threshold voltage shift of p-channel MOSFET is negative

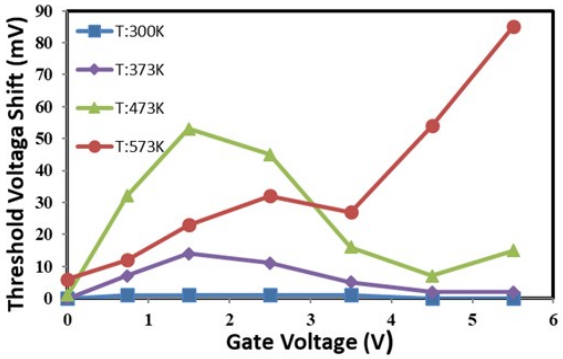


Fig. 9 Dependence of the threshold voltage shift of n-channel MOSFET on the stress gate voltage[10].

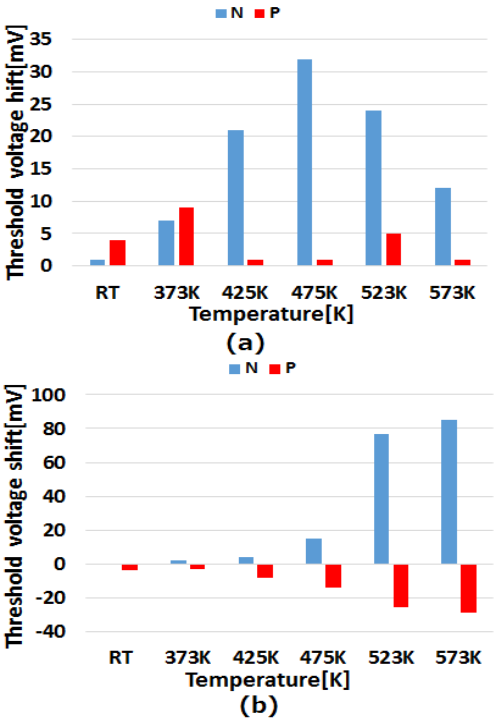


Fig. 10 Comparisons of the threshold voltage shift (a) (Vth – 0.2) V and (b) -4.5 V.

and absolute value of the threshold voltage increases as temperature increases when the gate stress voltage is high(–4.5 V) because NBTI occurs and effect of NBTI becomes stronger as temperature increases.

Dependence of the threshold voltage shift of n-channel MOSFET on the stress gate voltage is shown in Fig. 9[10]. The threshold voltage shift does not observed at room temperature and it increases as temperature increases and shows a maximum value at 473 K when the stress gate voltage is less than 2.5 V. The threshold voltage shift at 573 K is lower than that at 473 K because of high temperature annealing effect[10]. When the stress gate voltage is high, the threshold voltage shift increases with temperature rise. In this case, the threshold voltage shift is promoted by PBTI. The threshold voltage shift caused by PBTI is not recovered by the high temperature annealing effect[10].

Figures 10 (a) and (b) show comparisons of the threshold voltage shift at gate stress voltage of (a) (Vth-0.2) V and (b) -4.5V. (a) (Vth-0.2)V, when the stress gate voltage is near

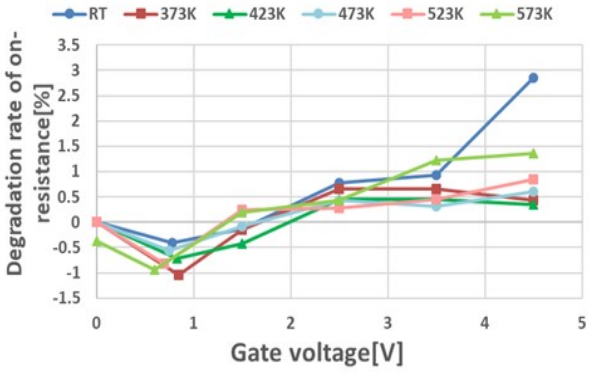
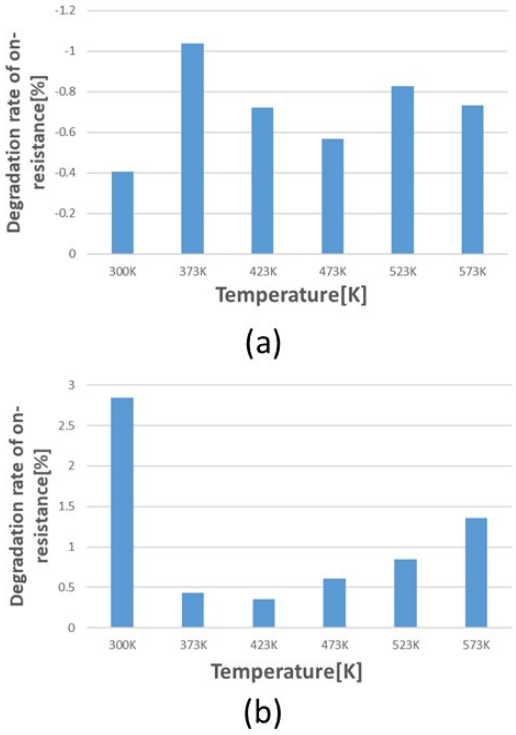


Fig. 11 Dependence of degradation rate of on-resistance of p-channel MOSFET on stress gate voltage.



Figs. 12 Dependence of the degradation rate of on-resistance on temperature at stress voltage of (a) (Vth – 0.2) V and (b) -4.5 V.

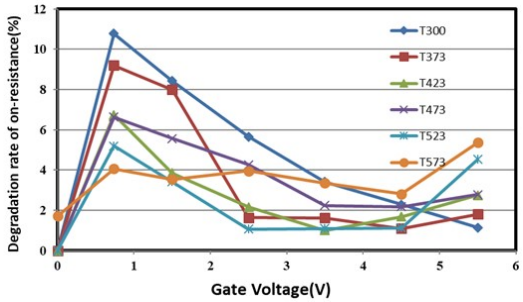


Fig. 13 Dependence of degradation rate of on-resistance of n-channel MOSFET on stress gate voltage[10].

threshold voltage. For the n-channel MOSFET, the threshold voltage shift increases as the temperature rises. On the other hand, it decreases when the temperature exceeds 473 K due to the high temperature annealing effect and decrease in DAHC injection. For both n- and p-MOSFETs, the threshold voltage shift also increases as the temperature increases at Vg = 4.5 V. This increase is caused by PBTI and NBTI effects. The threshold voltage shift of n-MOSFET is larger than that of p-MOSFET is due to the difference in impact ionization coefficient between electrons and holes.

Dependence of degradation rate of on-resistance of p-MOSFET on stress gate voltage is shown in Fig. 11. Stress time is 3,600 seconds and drain voltage is 6 V.

degradation rate= (R_{on}(3600s)/R_{on}(0s))*100-100

R_{on}(0s): on-resistance before the stress,

R_{on}(3600s): on-resistance after the stress for 3600 seconds

Degradation rate of on-resistance is negative (on-resistance decrease) when the gate voltage is near the threshold voltage (Vth + 0.2). This result indicated that DAHC occurs and electrons are injected. The degradation rate of on-resistance is positive when the stress gate voltage is more than 2.5 V. Degradation rate of on-resistance increases as the stress voltage increases when the stress gate voltage is more than 3.5 V. These results indicated that Channel Hot Carrier injection(CHC) occurs.

Figures 12 (a) and (b) summarize the results of Fig. 11 at the stress gate voltage of (Vth - 0.2) V and -4.5 V, respectively.

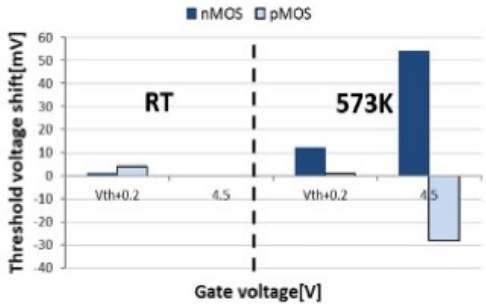


Fig.14 The comparison of the threshold voltage shift for n- and p-MOSFETs at room temperature and 573 K.

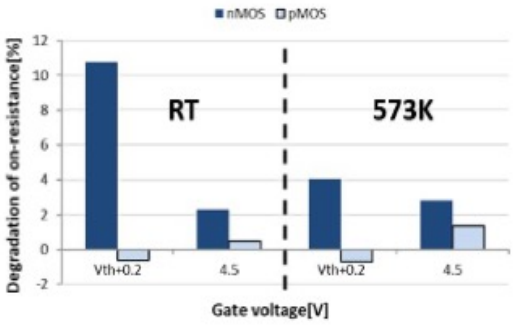


Fig. 15 Comparison of degradation rate of on-resistance for n- and p-MOSFETs at room temperature and at 573 K.

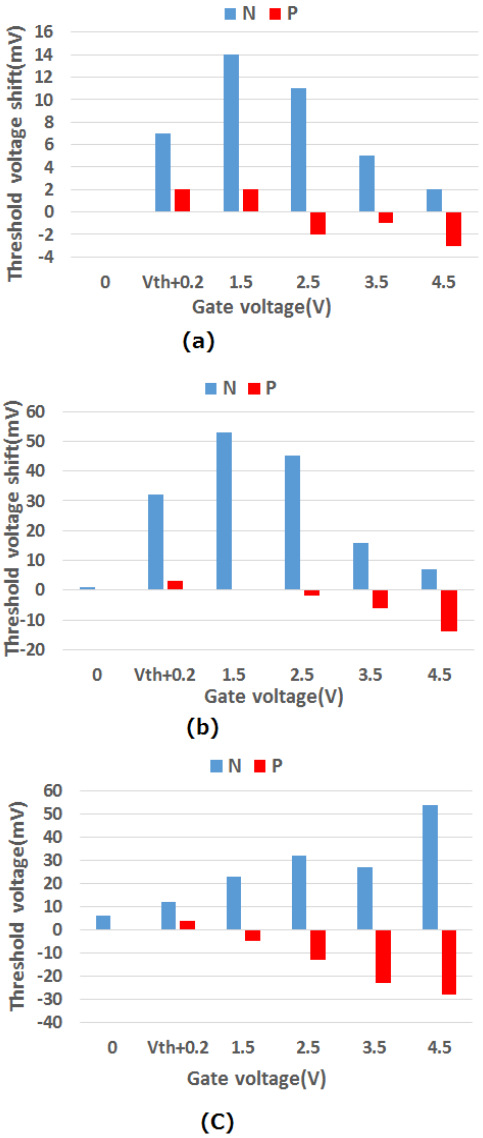
The degradation rate is smaller and does not change even if the temperature rises when the stress gate voltage is near the threshold voltage, as shown in Figs. 12 (a). The degradation rate of on-resistance is the maximum at 300 K and shows minimum at 423 K when the stress gate voltage is - 4.5 V. In addition, the degradation rate of on-resistance increases as the temperature rises when temperature is more than 423 K because NBTI enhances as temperature increases.

Dependence of degradation rate of on-resistance of n-channel MOSFET on stress gate voltage is shown in Fig. 13[10]. When the stress gate voltage is near the threshold voltage, degradation rate of on-resistance decreases as the temperature increases because the impact ionization coefficient decreases as the temperature rises, and the hot carrier injection is suppressed[10]. At 573 K, the degradation of on-resistance occurs even at the stress gate voltage of 0 V because of thermally induced leakage current[10]. The degradation rate of the on-resistance increases as temperature rises because PBTI enhances as temperature rises.

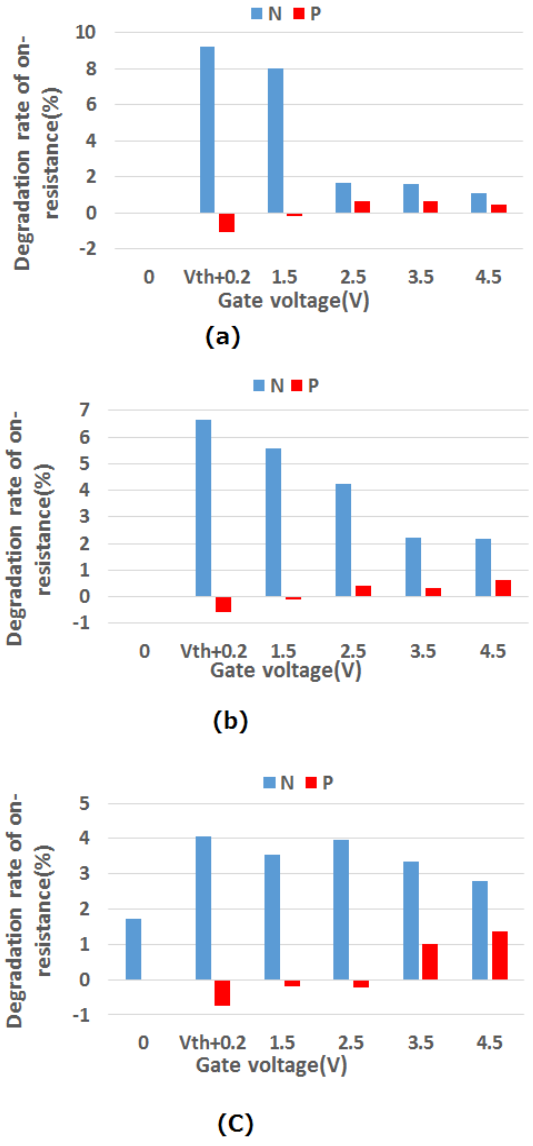
The comparison of the threshold voltage shift for n- and p-channel MOSFETs at room temperature and 573 K is shown in Fig. 14. Threshold voltage shift is smaller at room temperature. The absolute value of the threshold voltage shift of n-channel MOSFET is larger.

The comparison of degradation rate of on-resistance for n- and p-channel MOSFETs at room temperature and 573 K is shown in Fig. 15. When the stress gate voltage is near the threshold voltage, the degradation rate of on-resistance at room temperature is higher than that at 573 K for n-channel MOSFET. The degradation rate of on-resistance does not change for p-MOSFETs. This is because the impact ionization coefficient decreases as the temperature increases. On the other hand, that of holes are less affected because that of hole is smaller. The degradation rate increases due to PBTI for n-MOSFETs and NBTI for p-MOSFET when the stress gate voltage is high (Vg = 4.5 V).

Figures 16 (a), (b), and (c) show comparisons of the threshold voltage shift at 373 K and at 473 K, and 573 K, respectively. For the n-channel MOSFET, the maximum threshold voltage shift shows at gate stress voltage of 1.5 V at 373 K and 473 K, while that shows gate stress voltage of 4.5 V at 573 K. On the other hand, for the p-channel MOSFET, the threshold voltage shift is hard to observe when the gate voltage is near the threshold voltage. In addition, the threshold voltage shift is negative and absolute value increases with increasing temperature caused by NBTI when the gate voltage is - 4.5 V. The threshold voltage shift of n-channel MOSFET is larger than that of p-channel MOSFET.



Figs. 16 Comparisons of the threshold voltage shift (a) 373 K, (b) 473 K, and (c) 573 K.



Figs. 17 Comparisons of the degradation rate of on-resistance (a) 373 K, (b) 473 K, and (c) 573 K.

Figures 17 (a), (b), and (c) show comparisons of the degradation of on-resistance of n and p-channel MOSFETs at 373 K, at 473 K, and at 573 K. For n-channel MOSFET, the degradation rate of on-resistance decrease when the stress gate voltage is near the threshold voltage because impact ionization coefficient decreases as the temperature rises and high temperature annealing effect[10]. On the other hand, for the p-channel MOSFET, the threshold voltage shift is hard to observe when the gate voltage is near the threshold voltage. For both n- and p-channel MOSFETs, degradation rate of on-resistance increases with increasing temperature caused by PBTI for n-channel MOFET and NBTI for p-channel one. Degradation rate of on-resistance for n-channel MOSFET is larger than that for p-channel MOSFET.

V. CONCLUSION

We compared DC hot carrier effect, NBTI and PBTI of the thin-film SOI power n- and p-channel MOSFETs at high temperature and clarified their mechanisms.

For p-channel MOSFET, the threshold voltage shift becomes positive when the stress gate voltage is near the threshold voltage, and the absolute value of the threshold voltage shift increases as temperature increases due to NBTI when the stress gate voltage is high. For n- channel MOSFET, the threshold voltage shift becomes positive. The threshold voltage shift increases as temperature increases due to PBTI, when the stress gate voltage is high. The degradation rate of on-resistance is maximum for n-channel MOSFET due to DAHC when the stress gate voltage is near the threshold voltage, and become negative for p-channel MOSFET. On the other hand, the degradation due to CHC is smaller for n-channel MOSFET when the stress gate voltage is high. On the contrary, the CHC is the maximum for p-channel MOSFET when the stress gate voltage is high. The degradation rate of on-resistance does not depend on the temperature for the p-channel MOSFET when the gate voltage is near the threshold voltage, while the degradation rate decreases as the temperature rises for the n-channel MOSFET. When the gate voltage is high, the degradation increases as the temperature rises in both n- and p-channel MOSFETs. The instability in n-channel MOSFET caused by hot carrier effect and bias-temperature is more serious than that in p-channel MOSFET.

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