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Evaluation of gate drive circuit effect in Cascode GaN-based applications

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Abstract. This work evaluates the influence of gate drive circuitry to cascode GaN device's switching waveforms. This is done by comparing three PCBs using three double-pulse-test (DPT) with different gate driving loop design. Among important parasitic elements, source-side inductance shows a significant impact to gate-source voltage waveform. A simulation model based on experimental measurement of the cascode GaNFET used in this work is modified by author. The simulation model is implemented in a synchronous buck converter topology and hereby to assess the impact of gate driving loop of cascode GaN device in both continuous conduction mode (CCM) and critical conduction mode (CRM). Apart from simulation, a synchronous buck converter prototype is presented for experimental evaluation, which shows a 99.15% efficiency at 5A under soft-switching operation (CRM) with a 59ns dead-time.

Key words: cascode GaNFETs; parasitics; buck-conerter; gate drive design.

1. INTRODUCTION

Si-based devices have been a cornerstone in power electronics field and implemented in a wide range of applications in order to assist signal processing or energy conversion [1]. Si-based devices have dominated power electronics for several decades. However, an increasing demand for energy conversion has been observed in global power electronics market. The development and adoption of wide bandgap (WBG) power semiconductors are projected to result in a breakthrough in power electronics field.

Recently, significant efforts have been made by researchers in wide bandgap (WBG) power devices owing to their superior characteristics and properties over that of current dominant Si devices, such as higher breakdown field, higher mobility and higher power density [2]–[5]. GaN-based device has been assumed as a very promising candidate in the low-medium voltage range applications [6]–[12], owing to GaN device presents excellent performance in accordance with its theoretical characteristics and corresponding technological process among all potential candidates [13]. Currently, there are two types of GaN power devices available in the commercial market, namely, enhancement-mode GaNFETs and cascode GaNFETs. The traditional e-mode GaNFETs have relatively low gate threshold voltage (V_{th}) and narrow gate driving voltage safety margin, which poses a significant difficulties in terms of gate drive circuitry design. Different from e-mode GaNFET, cascode GaNFET is constructed by two discrete devices, a LV Si MOSFET and a HV GaN HEMT as illustrated in Fig. 1.

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Thanks to the implementation of LV Si MOSFET within cascode GaN device package, the gate threshold voltage is much higher than that of e-mode GaN device. Moreover, cascode GaNFETs can withstand a maximum 10V over-driving gate voltage [14].
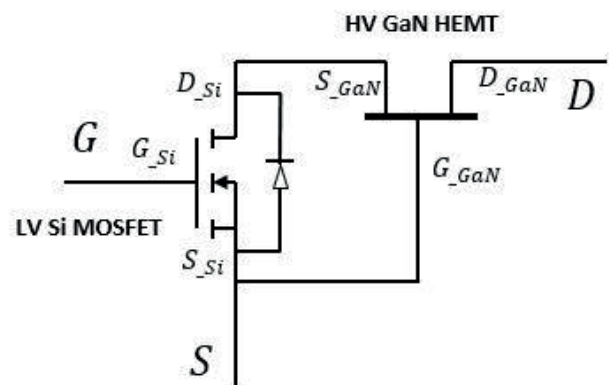
Fig.1. Cascode GaN device configuration

There are multiple cascode GaN-based converters/inverters that have been introduced by Transphorm [15]. In the meantime, significant research related to parasitic effect in GaN-based design have been studied in [16]–[21]. All of these presented research works are mainly focusing on the evaluation of the effect of common source inductance and parasitic inductance in power loop for GaNFET-based design. It is worth pointing out that cascode GaNFETs exhibit higher input capacitance in comparison with e-mode GaNFET, due to the existence of an unavoidable high-frequency gate-source

voltage ringing. In this work, TPH3205WSB in TO-247 package from Transphorm is used for evaluation.

This paper evaluates the effect of gate drive circuit design to cascode GaN devices and accordingly proposes a simple approach to improve system efficiency for cascode GaN-based design. A SPICE-based simulation model is made in accordance with the experimental measurement of cascode GaNFET (TPH3205WSB), which is used further to access the effect of different gate driving loop design to the overall efficiency of cascode GaN-based buck converter. Moreover, a synchronous buck converter prototype with proposed gate drive design is made and tested with hard switching (CCM) and soft-switching (CRM) for the aim of evaluation. The hard switching operation, also known as continuous conduction mode (CCM), where the energy in the load inductor continuously flows through the converter during normal operation. The power transfer can be simply divided into two steps. When top switch is ON, the inductor stores energy; when top switch is OFF, the energy stored in load inductor will be transferred to output load. The critical conduction mode (CRM) is selected for soft switching demonstration. Due to the CRM can easily achieve zero voltage switching turn-on for top switch and zero current switching turn-off for bottom switch with synchronous buck converter topology used in this work. Fig. 2 shows the buck converter scheme and the CRM soft switching operation principle used in this work.
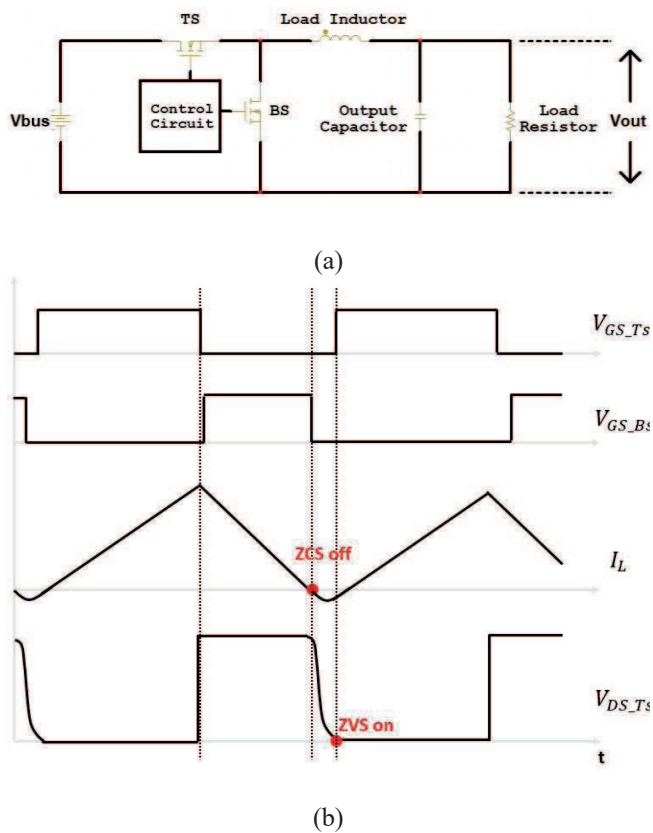

(a)

(b)

Fig. 2. (a) Buck converter scheme; (b) CRM operation principle

2. Gate drive circuit consideration for cascode GaN devices

A. Finds in experimental measurement

In order to find out the impact of gate drive circuit to the switching performance of cascode GaN device. A series of double pulse test (DPT) were conducted to collect experimental result, which consists of a DUT (TPH3205WSB) and a SiC diode (FFSH3065B-F085). Three PCBs with different gate drive circuitry design were made for the comparison purpose. Table.1 shows the two critical parasitic inductance extracted via Ansys Q3D from gate drive loop in three PCBs. The PCB Version 1 exhibit highest gate turn-on inductance and source-side inductance among three PCBs. The PCB Version 2 is made with higher gate turn-on inductance and smaller source-side inductance in comparison to PCB Version 1 for investigation purpose. The PCB Version 3, which has least gate turn-on inductance and source-side inductance. Methods to lower PCB Version 3 inductance in gate driving loop is: (a) ground plane is used to minimize the physical trace length between GND pin of the gate driver IC and the source pin of the device; (b) remove all vias around gate driving loop/switching node; (c) place gate turn-on path and return path as close as possible.

The gate turn-on inductance indicates the total parasitic inductance in gate turn-on path, whereas source-side inductance is the sum of the parasitic inductance in gate return path. Fig. 3 shows the location of these two important parasitic inductance and the way to measure the voltage ringing caused by source-side inductance.

Table 1. Parasitic inductacnce extraction within gate drive loop

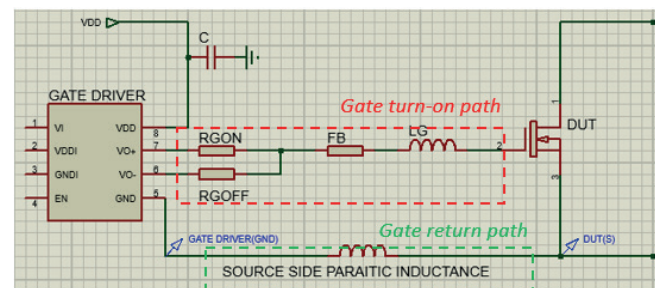| Parameter	PCB Version 1 (Original board)	PCB Version 2	PCB Version 3
Gate turn-on inductance/nH	5.6012	9.4462	4.4326
Source-side inductance/nH	10.376	4.2235	1.092

Fig. 3. Key parasitic inductance in gate driving loop and source-side ringing measurement

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Fig. 4 shows the gate-source voltage and drain-source voltage measurement from oscilloscope. All data as concluded in Table 2. In accordance with the measurement result, the PCB Version 1 shows a significant gate-source voltage oscillation as large as 28.4V in turn-on event, which is 8.4V higher than specified V_{gs_max} (20V) [22]. Even the high gate-source voltage spikes disappear within 6ns, the drain-source voltage waveform still affected by this high gate-source voltage oscillation as depicted in Fig. 4(a). Compared to PCB Version 1, the Version 2 exhibits 3.845nH higher gate turn-on inductance while 6.1525nH lower source side inductance. However, the Version 2 board shows a 15.4V reduction in gate-source voltage during turn-on process. Furthermore, the source-side high frequency ringing has reduced from 510ns in PCB Version 1 to 360ns in PCB Version 2. In contrast, the turn-on inductance is not the only one determinant of gate-source voltage. The PCB Version 3 is made for further investigation, which has minimum turn-on inductance (4.4326nH) and source-side inductance (1.092nH) among these three boards. As shown in Table 3, PCB Version 3 attain a 15.5 V reduction in source-side ringing and a 320ns shorter source-side ringing duration in comparison to those of PCB Version 1.

In accordance with the gate-source voltage and source-side voltage measurement as shown in Fig. 5. The gate-source voltage waveform is very similar to the source-side voltage waveform in term of duration time and frequency. As a result, the source-side inductance shows a more significant influence on the gate-source voltage in comparison with that of gate turn-on inductance. In an extreme case, such as PCB Version 1, such high frequency gate voltage ringing caused by source-side inductance can affect the drain-source waveform as illustrated in Fig. 4(a)
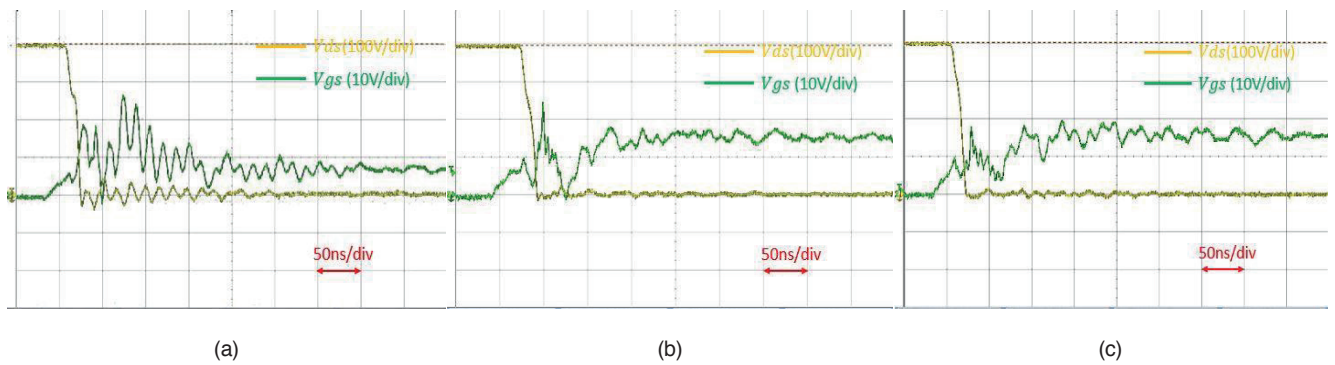

Fig. 4. Gate-source voltage and drain-source voltage measurement @400V/5A turn-on of (a) PCB Version 1; (b) PCB Version 2; (c) PCB Version 3
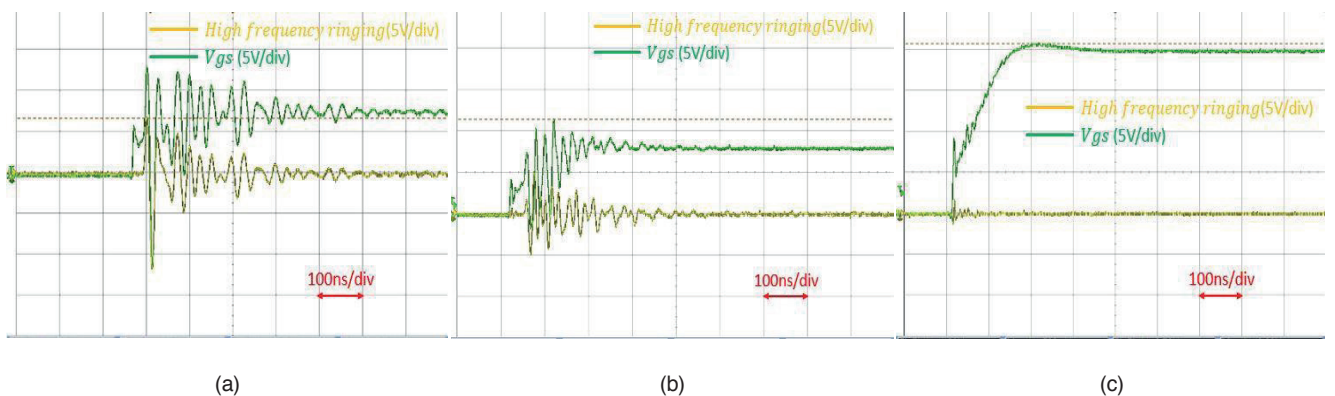
Fig. 5. Gate-source voltage and source-side voltage measurement @ Vds=100V of (a) PCB Version 1; (b) PCB Version 2; (c) PCB Version 3

Table 2. Detailed three PCBs experimental measurement result

Parameter / unit	PCB Version 1 (Original board)		PCB Version 2		PCB Version 3	
	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off
Vgs_{pk-pk} / V	28.4	10.3	13	10	10.3	10

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Vgs$_{Max}$ / V	26.3	7.8	12.2	8.1	9.6	8.1
Vds$_{pk-pk}$ / V	438	403	413	406	409	400
Vds$_{Max}$ / V	400	400	397	400	402	399
Source-side ringing @ Vds=100V / V	18.3		9.9		2.8	
Time duration of source-side ringing @ Vds=100V/ ns	510		360		190	

B. Simulation model of TPH3205WSB cascode GaNFET

Transphorm provides the original SPICE model of cascode GaNFET TPH3205WSB, and this model has been modified by author based on experimental measurement result. The detailed comparison between simulation model and experimental measurement as illustrated in Fig. 6. According to Fig. 7, when the device operating at 5A or lower current, the simulation model shows 3.9% and 5.8% difference from practical turn-on and turn-off switching loss respectively.
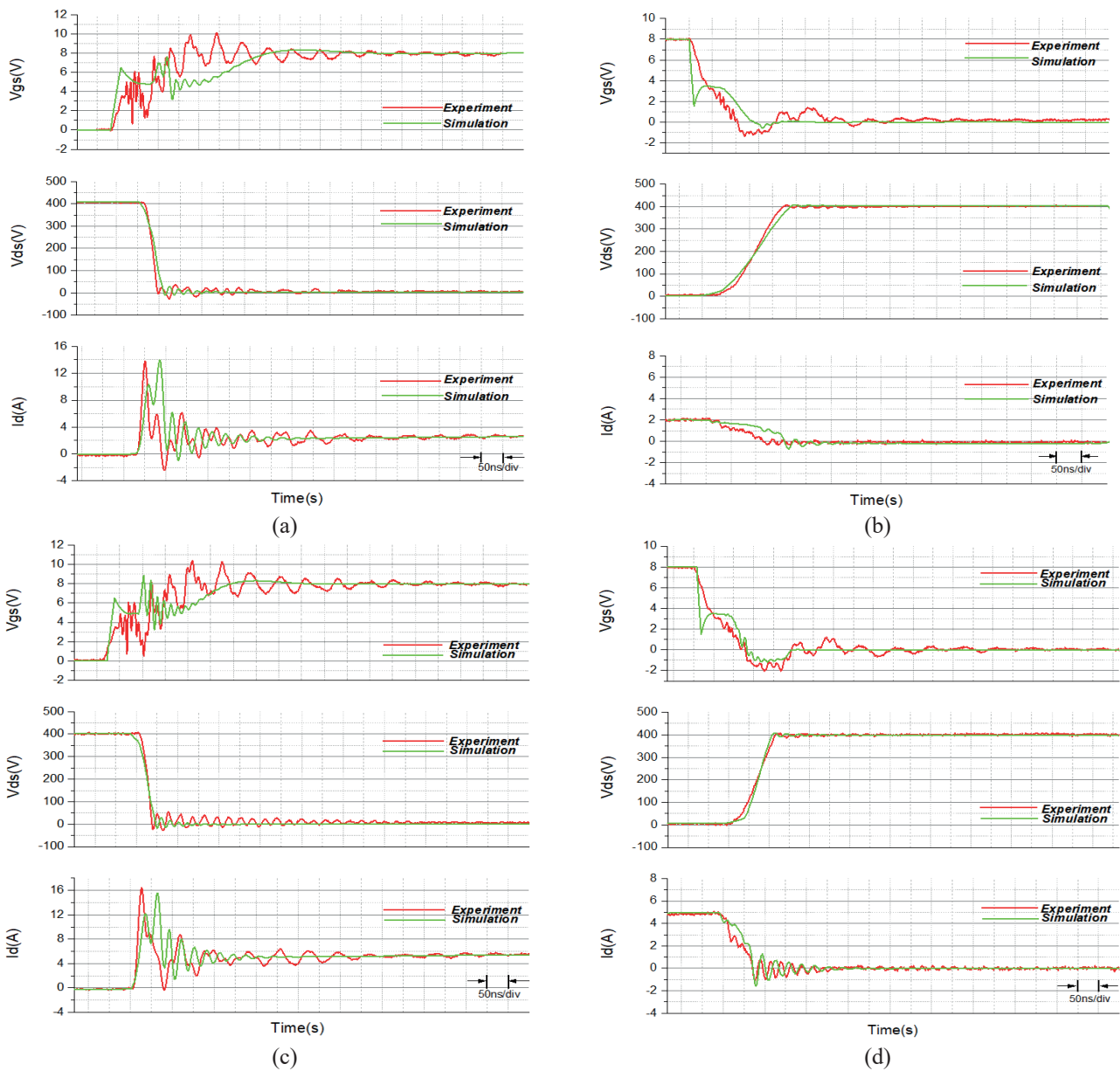

Fig. 6. PCB Version 3 switching waveform comparison between simulation model and experimental measurement of (a) turn-on @400V/2A; (b) turn-off @ 400V/2A; (c) turn-on @ 400V/5A; (d) turn-off @ 400V/5A
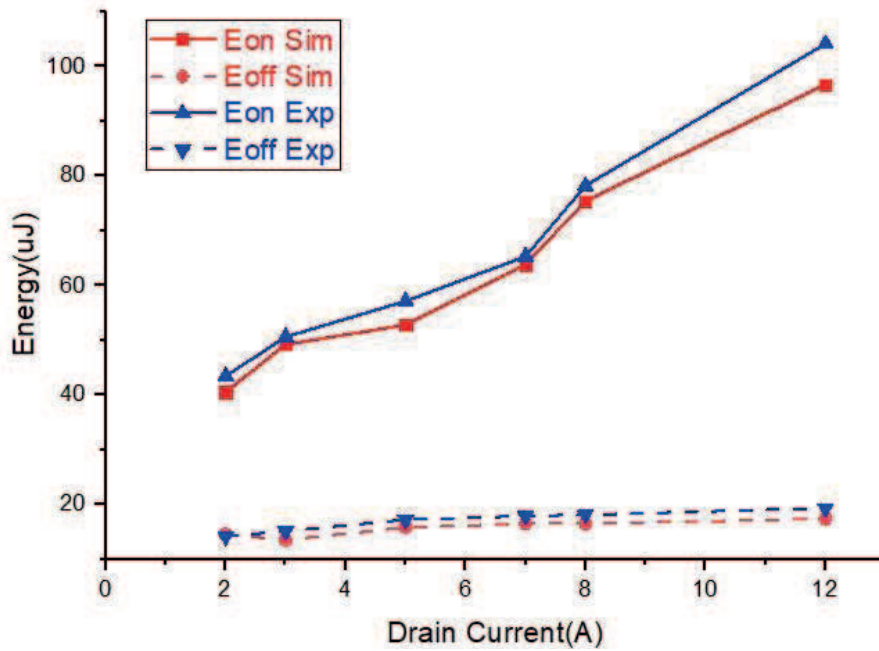
Fig. 7. PCB Version 3 switching loss comparison between simulation model and practical measurement

3. Implementation of optimized gate drive circuitry in buck converter

As drawn in Fig. 6 and Fig. 7, the simulation model only has very little difference from practical measurement. Therefore, a synchronous buck converter topology has been chosen in order to find out the advancement of PCB Version III with optimized source-side inductance.

A. Power loop parasitic inductance extraction.

Apart from parasitic inductance shown in Table 1, the inductance in power loop also play an important role in overall performance. In PCB Version 3, the value of power loop parasitic inductance is also extracted via Ansys Q3D as indicated in Fig. 8, which is formed by the power communication path from freewheeling diode to the coaxial current shunt.

All parasitic elements in PCB traces and components are included in the buck converter simulation in order to ensure the accuracy of the result. The list of key components and parameters used in simulation as shown in Table 3.
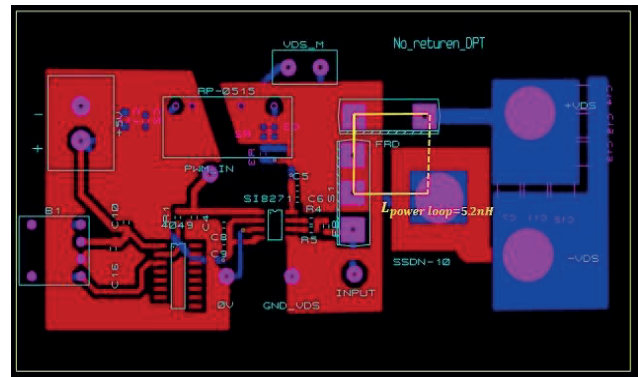

Fig. 8. Power loop parasitic inductance extraction of PCB Version 3

Table 3. Parameters/components used in SPICE-based simulation

Component/parameter name		Value	Unit
Load inductor		500	uH
Turn-on resistor		10	Ω
Turn-off resistor		2	Ω
Gate driving loop	Gate turn-on inductance	5.6(Ver I)/4.43(Ver III)	nH
	Source-side inductance	10.376(Ver I)/1.092(Ver III)	nH
Power loop inductance		5.2	nH
Bus voltage		400	V
Output voltage		200	V
Switching frequency		100	kHz

Cadence Orcad is a SPICE-based simulation software, which is selected to compare buck converter performance respect to different gate driving loop design. A synchronous buck converter is built in Cadence Orcad, consisting of two identical cascode GaN power devices, which are implemented as top and bottom switch in the design. All parameters filled into simulation are the same as PCB V1 and V3 for comparison purpose. Both hard-switching (CCM) and soft-switching (CRM) operation are conducted in the simulation in order to determine the possible maximum efficiency of the converter with proposed gate drive circuitry. Meanwhile, a synchronous buck converter prototype with optimized gate driving loop and similar power loop parasitic inductance has made for experimental verification. Fig. 9 shows the synchronous buck converter prototype made in this work. An integrated gate driver (Si8230) with high CMTI and ultra-low propagation time from Silicon Laboratories is implemented in hardware. Regarding to CRM operation, the dead time between two switches is set to 59ns by connecting a 5.9kΩ resistor from the DT pin of the gate driver to its ground.
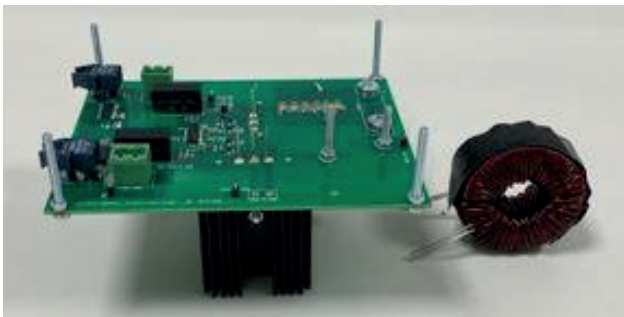
Fig. 9. Side-view of synchronous buck converter prototype and load inductor

Fig. 10 shows the efficiency comparison between simulation result and prototype experimental result in CCM and CRM operation. The main difference between PCB V1 and PCB V3 is the gate drive circuitry design. PCB V3 has significant lower source-side parasitic inductance in gate return path in comparison to that of PCB V1 as shown in Table 1. Therefore, an obvious improvement in efficiency can be observed under both hard and soft switching modes in synchronous buck converter according to the simulation result. It is necessary to mention that the simulation model is less accurate at high current operation (>5A), due to simulation environment is set under constant room temperature. A hardware prototype with proposed gate drive design is made, which only exhibits 1nH parasitic inductance in gate return path. As drawn in Fig. 9, the prototype can attain a maximum efficiency of 98.79% at 4.4A under hard switching operation (CCM) and 99.15% efficiency at 5A under soft switching operation (CRM).
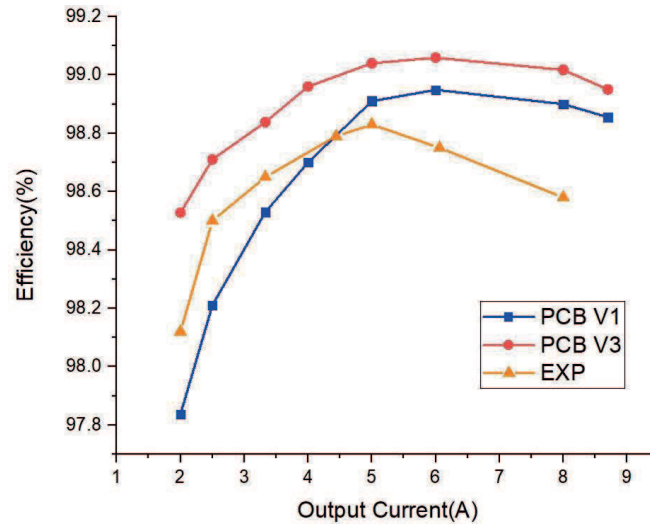
(a)
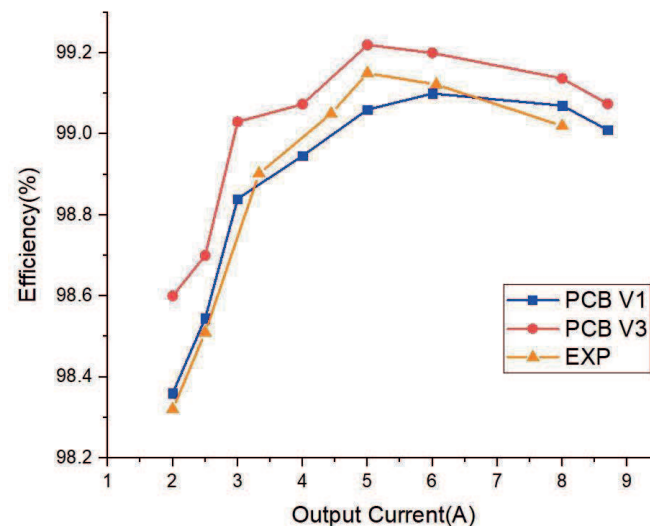
(b)

Fig. 10. Efficiency comparison between PCB V1&V3 simulation result and experimental measurement in (a) hard-switching (CCM); (b) soft-switching (CRM)

4. Conclusion

This paper analyses the impact of gate driving loop to cascode GaNFET switching performance. As proved in this work, a careful gate drive circuit design with minimum source-side inductance can greatly reduce such voltage oscillation. Therefore, for any cascode GaN-based design, additional care for source-side inductance should be taken due to gate return path is more critical in comparison with gate turn-on path.

Although this is not covered in this work, it is worth to point out that higher input capacitance (Ciss) of cascode GaN device in comparison with e-mode GaNFET leading to a slower switching transient and lower maximum operation frequency.

The purpose of such high input capacitance is to protect the unwanted gate-source voltage ringing caused by source-side inductance in gate driving loop. As analyzed in this work, when gate return path is optimised, cascode GaN devices no longer require that high input capacitance to ensure the stability of gate-source voltage. Hence, further development of cascode GaNFETs can be done by implementation of LV Si MOSFET with lower input capacitance. This can boost the switching speed of cascode GaNFETs, and hereby making use of the advantages that GaN brings.

A SPICE model is modified based on experimental measurement. Accordingly, a series of simulations using the modified model are conducted in order to find the influence of different gate drive circuit design. An improved operation of cascode GaNFET-based applications can be achieved with proposed gate drive circuitry design. Namely, an optimized gate return path is more important in comparison with gate turn-on path when cascode GaNFETs are used in the design. A synchronous buck converter prototype is made in this work, which attains a 99.15% efficiency at output current of 5A under soft switching mode.

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