Fabrication of a MEMS Micromirror Based on Bulk Silicon Micromachining Combined With Grayscale Lithography

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***Abstract*— A 1D MEMS (Micro-Electro-Mechanical Systems) mirror for LiDAR applications, based on vertically asymmetric comb-drive electrostatic actuators, is presented in this work employing a novel fabrication process. This novel micromachining process combines typical SOI-based bulk micromachining and grayscale lithography, enabling the fabrication of combs actuators with asymmetric heights using a single lithography step in the active layer. With this technique, the fabrication process is simplified, and the overall costs are reduced since the number of required lithography steps decrease. The fabricated mirrors present self-aligned electrodes with a 2.8 μm gap and asymmetric heights of the movable and the fixed electrodes of 20 μm and 50 μm, respectively. These asymmetric actuators are an essential feature for the operation mode of this device, enabling both in resonant and static mode operation. A mirror field of view (FOV) of 54° at 838 Hz was achieved under low-pressure, when resonantly operated, and a FOV of 0.8° in the static mode.**

***Index Terms*— Bulk-micromachining process, grayscale, MEMS mirror, scanner, vertically asymmetric electrodes.**

I. Introduction

NOWADAYS , MEMS mirrors are present in many applications such as endoscopic imaging, fiberoptic communications, micro spectrometers, and laser scanner systems (i.e., LiDAR - Light Detection and Ranging, image projection, displays, and head-up displays [1]). Devices fabricated by surface and bulk micromachining are widely presented in the literature [2], mainly using electrostatic, electromagnetic, thermal or piezoelectric actuation. Electrostatically actuated MEMS mirrors are typically fabricated in simple fabrication processes, being extremely compact and compatible with other micromachining technologies [1], with the advantage of not requiring rare materials, as is the case of piezoelectric and electromagnetic devices, and have the capability of being actuated at higher frequencies compared to thermal actuation.

MEMS mirrors using electrostatic actuators have been presented in literature, where the primary schemes can be divided into vertical comb actuators and parallel-plate actuators. In general, comb actuation allows for larger mirror angles (θ) and, consequently, a larger field of view (FOV) when compared to parallel-plate actuation [2], because the electrodes relative positions do not restrain displacement. Vertical comb-drive actuators offer key advantages: it does not restrict the maximum deflection angle such as the use of parallel-plates and the pull-in associated with parallel-plates can be avoided. Several ways of combining vertical comb-drive actuators with micromirrors have been presented in the literature, mainly in staggered vertical combs, SVC (same electrode dimensions but with z-axis offset) [3] and [4], angular vertical combs, AVC (same electrode dimensions but with an angular offset) or vertically asymmetric combs-drives (different heights and with z-axis offset) [5] and [6].

Typical vertically asymmetric comb electrodes fabrication relies on the use of several lithography steps to define the masks to fabricate electrodes with thickness asymmetry on a single silicon layer, as presented in [5] that uses different materials to create a two level mask and in [6] that uses two layers of the same material defined in different lithographic processes. These are often prone to misalignments between actuators, and when designing a device with a minimal electrodes gap (smaller than 3 μm given a 50 μm SOI layer), this misalignment can compromise the final device performance or process yield. More recently, new attempts to develop self-aligned comb electrodes have been presented. In [7], higher alignment tolerance is achieved by using dummy electrodes and SOI-SOI wafer bonding. Other approaches use electrodes with the same thickness and the offset is induced by out-of-plane actuation [3] and [4] or by using suspended actuators and mechanically deflecting those at the expense of complex assembly procedures [8].

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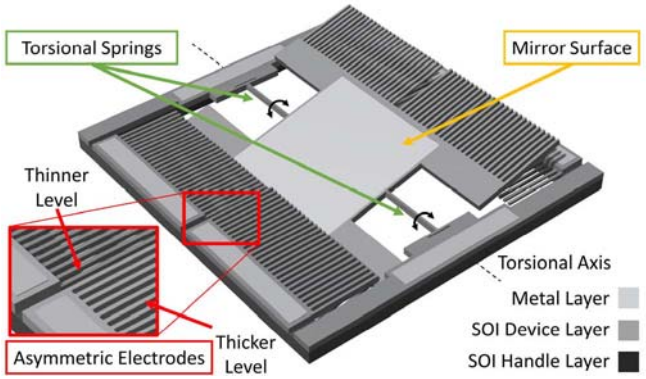


Fig. 1. 3D schematic of the 1D MEMS mirror.

In this work, a 1D (one torsional axis) MEMS mirror is presented employing vertical asymmetric comb-drive electrostatic actuation for automotive LiDAR applications, micromachined using a novel self-aligned, dicing-free [9] and low-cost fabrication process, capable of achieving a FOV of 54° under low pressure. This novel fabrication process combines typical SOI-based bulk micromachining and grayscale (GS) lithography to create a single mask with multilevel topography, followed by a sequence of etching and mask thinning steps, creating vertically asymmetric structures enabling a small and self-aligned electrode gap of approximately 2.8 μm. This process when compared to previous references [3]–[8], presents a simpler and cost-effective process to achieve non-resonant torsional motion using a single layer device.

II. 1D MEMS Mirror Model and Design

The MEMS mirror schematic is depicted in Fig. 1. A 1×1 mm^2 mirror is attached to two torsional springs and four pairs of vertically asymmetric electrodes. The mechanical model that represents the mirror motions is presented in equation (1):

$$J\ddot{\theta} + B\dot{\theta} + k\theta = T \tag{1}$$

where J is the mirror moment of inertia, B the damping coefficient, k the torsional spring constant, T the torque necessary to the mirror movement, and θ the mirror angle. The correspondent natural frequency f_0 is estimated by the equation (2), and as can be seen, is influenced by the torsional spring elastic constant and the mirror moment of inertia.

$$f_0 = \frac{1}{2\pi}\sqrt{k/J} \tag{2}$$

Each electrode pair consists of fixed and movable combs actuators, and an electrostatic torque is generated when a voltage is applied between the comb electrodes thus rotating the mirror around the springs' axis. The implementation of vertical comb-drive electrostatic actuators is an essential feature for the operation of this device, enabling it to be operated both in resonant and static mode, unlike the symmetrical actuators which only allow the resonant mode. In resonant operation asymmetric actuators require higher voltages than equivalent symmetric actuators to achieve the same FOV (to achieve the same electrostatic torque given the smaller overlapping area). The device static mode operation is due to the height asymmetry between the movable and fixed in the rest position that enables a vertical displacement of the mirror structure, allowing an out-of-plane, pull in safe motion. When a DC voltage is applied between both electrodes, a constant electrostatic torque is generated, twisting the mirror to a fixed angle around the springs' axis. The higher the DC actuation voltage, the greater the torque applied; until the equilibrium between the torque produced and spring restoring elastic torque. The maximum angle attainable in static mode is geometrically defined. Table. I presents the designed dimensions and mechanical features.

TABLE I
MEMS Mirror Design Features

Mechanical Features		1D MEMS Mirror
Mirror area (l × w)		1000 μm × 1000 μm
Springs dimensions (l × w × h)		600 μm × 20 μm × 50 μm
Number of electrostatic electrodes		100
Electrodes dimensions (l × w × h)	Fixed	500 μm × 20 μm × 50 μm
	Movable	500 μm × 20 μm × 20 μm
Electrodes gaps		2 μm

III. Microfabrication Process

A. Grayscale Lithography

Standard lithography is a process that creates a pattern on photo-resist, a photo-sensitive polymeric material, to be used as a sacrificial layer in etching or deposition processes of surface and bulk micromachining. This photoresist is polymerized using ultra-violet light and this exposure can be done either by using a pre-existent hard mask and a collimated light source or using a direct-write-laser (DWL). A development step follows, in which the pattern is revealed by removal of the exposed region (a positive photoresist is assumed, while the unexposed material is removed in the case of a negative photoresist) thus creating a binary level mask and uncovering selected regions of the underlying substrate for further processing.

On the other hand, grayscale (GS) lithography enables the creation of masks with multiple levels of photoresist thickness. In GS lithography, the photoresist layer is exposed using a lateral variation of the exposure dose using an intensity-controlled laser beam. The local development rate of the exposed photoresist changes according to the exposure dose, as represented in Fig. 2, and the desired resist topography is created during the development process, resulting in a multilevel mask with different thickness levels on the photoresist.

Grayscale lithography is often used to pattern micro-lenses, diffractive optical elements, computer-generated holograms, among others [10]. However, this can also be used to create discrete photoresist levels, as shown in Fig. 2 (a), that when combined with a sequential bulk micromachining process, transpose this discrete mask to the substrate. This technique enables the patterning of perfectly aligned (no alignment between separate lithography steps is required) asymmetric

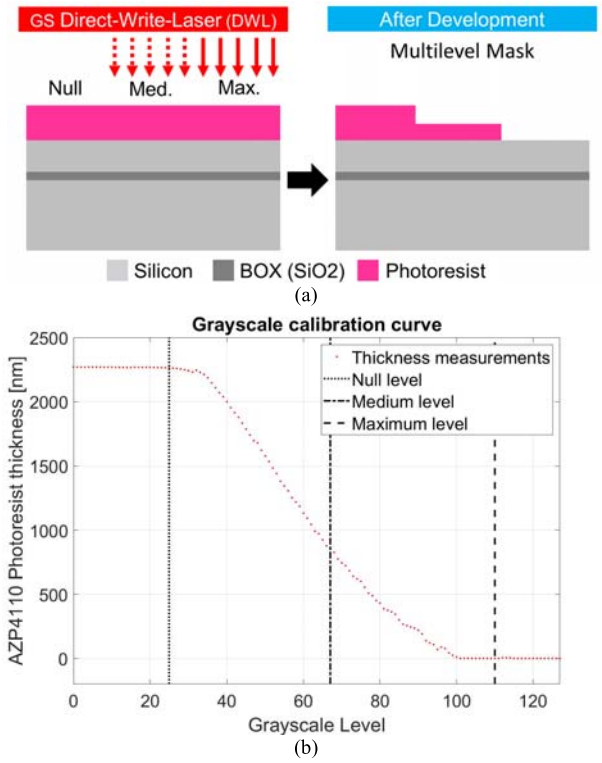


Fig. 2. GS lithography process schematic (a). Grayscale characterization curve, showing that at least 80 different GS levels are possible (b).

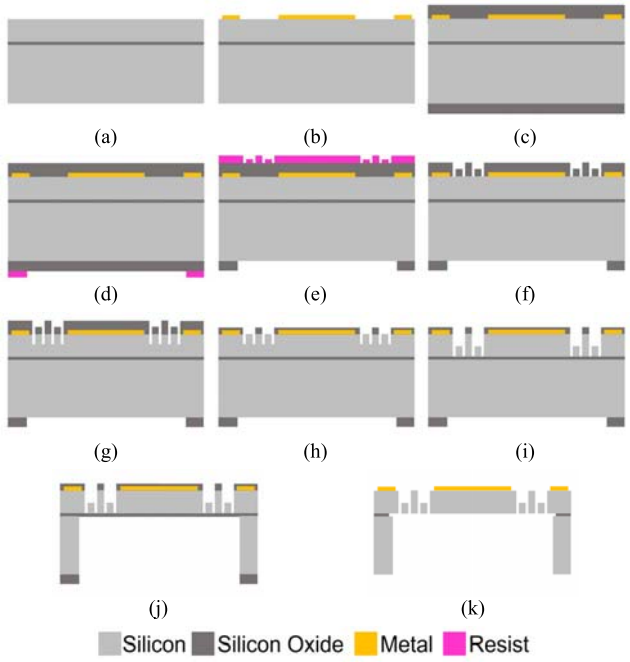


Fig. 3. MEMS mirrors main fabrication steps. (a) SOI Wafer; (b) AlSiCu thin-film patterning; (c) FS and BS SiO_2 layer deposition; (d) BS hard-mask lithography; (e) BS hard-mask patterning and FS GS lithography; (f) FS GS hard-mask patterning; (g) FS 1st DRIE; (h) FS GS hard-mask thinning; (i) FS 2nd DRIE; (j) BS DRIE; (k) HF structures release.

structures that, in this particular application, enables the creation of self-aligned electrostatic combs where each GS level corresponds to a different thickness to be patterned on the silicon substrate. The fact that no alignment between separate lithography steps is required, bypasses most misalignment sources from the lithography process, that may arise due to the resolution of the system camera or from the alignment marks quality, among others.

The final thickness of photoresist after being developed, for each intensity level, was characterized to ensure the optimum laser intensity that would be needed during the process. For this calibration, an initial AZP4110 photoresist layer with a thickness of 2.2 μm was used. The calibration curve is shown in Fig. 2 b) and presents over 80 grayscale levels in the linear region defined between thickness 2.2 μm and 0 μm. However, in this particular design, only three GS levels were used to define the asymmetric comb electrodes, which presented a final thickness of 0 μm (maximum level), 1.1 μm (medium level) and 2.2 μm (null level).

B. Micromachining Process

The devices were fabricated on a 50 μm-thick SOI wafer, Fig. 3 (a), where initially a thin layer (500 nm) of AlSiCu was sputtered and patterned through Reactive Ion Etching (RIE) on the wafer front-side (FS), Fig. 3 (b), to create the device electrical contacts, the mirror coating, and the FS alignment marks. The AlSiCu coating patterned on the mirror surface aims to increase the mirror reflectivity for the near-infrared laser, wavelength used in the LiDAR application.

With the target interelectrode gap aspect ratio of the MEMS mirror of 25 (on FS, 50 μm deep/2 μm wide), the difficulty to obtain the multilevel topography in the silicon without removing and damaging the GS photoresist mask increases, given the etch rate of both materials and the resulting selectivity during the etching process. In order to address this constraint and work with a better selectivity rates, hard-mask layers were employed. Thus, a thick layer of silicon oxide (3 μm of SiO_2) was deposited on both sides of the SOI wafer by Plasma-Enhanced Chemical Vapor Deposition (PECVD), Fig. 3 (c).

The back-side (BS) oxide layer was then patterned by RIE, Fig. 3 (d), to define the BS hard-mask for the subsequent silicon patterning. In this layer, the BS mirror cavities combined with the BS alignment marks (aligned to the front side marks) were patterned. These marks are essential to ensure that the BS mask is aligned with the FS mask already patterned and to ensure a final functional device.

For the FS mirror design (mirror structure, springs, and electrodes) a GS mask with three different thickness of photoresist was exposed, Fig. 3 (e).

The multilevel photoresist mask previously developed was then transferred to the SiO_2 layer through a sequential process of silicon oxide etching by RIE and photoresist mask thinning through O_2 plasma strip to achieve the multilevel topography on the hard-mask layer, Fig. 3 (f), with three different levels/thicknesses: 3 μm, 1.5 μm, and 0 μm. Each mask step height must include extra thickness to compensate for the mask material removed during the etching of the substrate material.

Taking advantage of a high substrate to mask selectivity of the etching process, a sequential iterative etching process

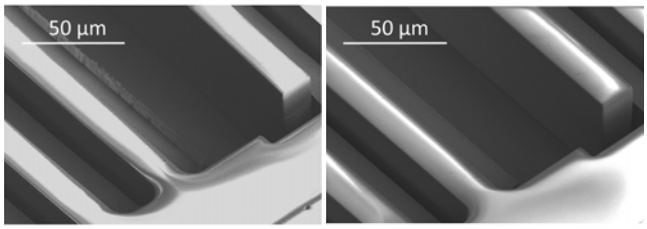


Fig. 4. SEM images of the thinned electrodes (a) before and (b) after the cleaning of the organic residues due to the DRIE process.

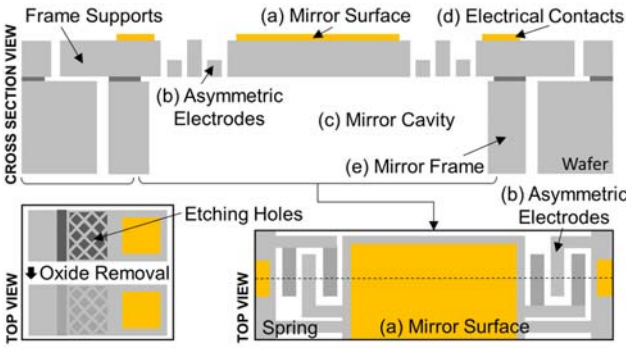


Fig. 5. Cross-section schematic overview of the MEMS mirror components, such as, (a) mirror surface, (b) asymmetric electrodes, (c) mirror cavity, (d) electrical contacts, (e) mirror frame and dicing-free features.

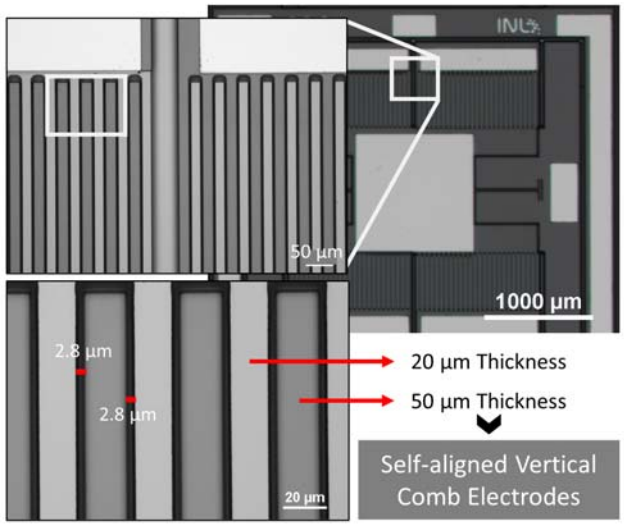


Fig. 6. Optical microscopic images of the fabricated devices, showing self-aligned electrodes with 2.8 μm gaps.

was used to etch the FS silicon layer to different discrete depths in the various regions defined by the multiple GS mask levels. The exposed substrate is etched, in different steps, through DRIE (Deep Reactive Ion Etching), based on the etch time, Fig. 3 (g). Each substrate etching step is followed by a hard-mask thinning process to expose the substrate in the next GS region, Fig. 3 (h), enabling further etching of the substrate, and by a cleaning process of the organic residues due to the DRIE process, Fig. 4, since this during the substrate thinning can become a mask and pattern the silicon.

In the first etching step, a depth of 30 μm is defined in the substrate, creating the necessary depth ratio that allows in the next etch process, to achieve the desired substrate topography. The SiO_2 mask on top of the thinner electrodes is then removed, exposing the substrate in these regions. Subsequently, during the second etching process, the exposed substrate is etched, resulting in a 20 μm thickness in the electrodes, while in the previously partially etched regions the BOX (buried oxide) is reached, decoupling the movable from the fixed asymmetric electrodes, Fig. 3 (i).

The BS was etched (DRIE), to open the mirror cavities to allow a free movement of the mirror, Fig. 3 (j). Finally, the structures were released using hydrogen fluoride (HF) vapor etching, Fig. 3 (k), removing the sacrificial buried oxide (BOX) layer that is exposed and the remaining oxide hard-masks. Fig. 5 presents a cross-section schematic of the MEMS mirror, illustrating also the HF dicing-free designed features (described in [9]), which consist of FS and BS overlapping trenches around each device and FS grid supports. During the HF process, the BOX layer between the supports and the handle layer is removed, leaving each die suspended by the FS supports on the wafer. These features bypass the need for an extra dicing step, and consequently increasing functional devices yield since these are not submitted to dicing stress.

C. Fabricated Devices

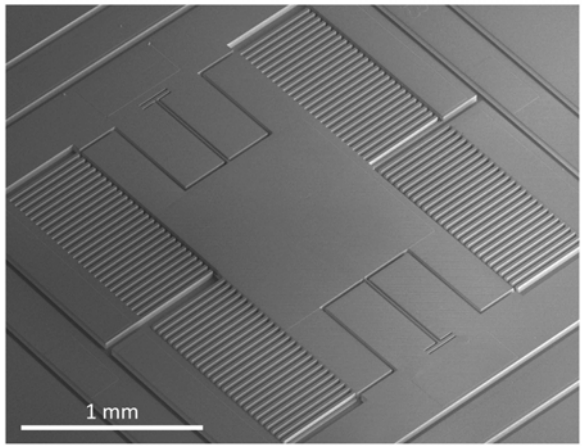
The mechanical characterization of the fabricated devices was performed to ensure that all the designed features meet the fabrication specifications.

Using an optical microscope, the fabricated devices were inspected, and as depicted in Fig. 6. The gaps between the two electrodes are entirely aligned, i.e., the gaps are equal in both sides of the electrodes. This is a crucial feature in electrostatic actuation since when an actuation voltage is applied, the in-plane electrostatic forces must be in equilibrium, and only the out-of-plane force should induce the torsional motion of the mirror. It can also be noticed that the gap of 2 μm was over etched, resulting in a gap of 2.8 μm in the final manufactured devices. This over-etch of the trenches in respect to the mask is typical of DRIE processes and geometry/depth dependent and was accounted for in order to not compromise the performance of the mirror.

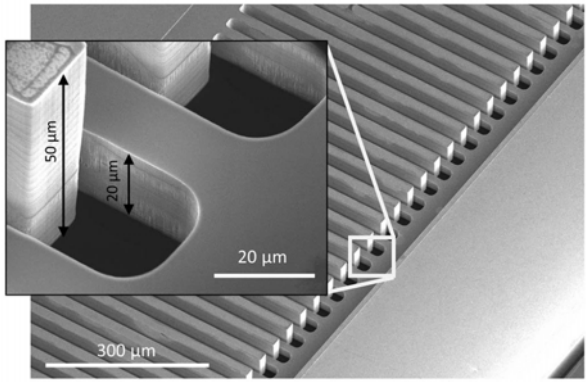
All the other mechanical features, such as spring dimensions and mirror area, are within the design specifications with variations below 4 % and 0.08 % respectively.

Fig. 7 presents SEM images of the mirror and its actuators. The two silicon levels are easily identified in both figures (a) and (b), where the lower electrodes present a lighter grey color (20 μm), and the full silicon thickness ones a darker grey color (50 μm).

The fabricated devices presented the desirable features concluding that this dicing free process combined with this manufacturing process simplified by the grayscale lithography ensured a good yield and the proof of concept of this new low-cost process.



(a)



(b)

Fig. 7. SEM images of the fabricated devices: (a) Overall MEMS mirror; (b) Close-view SEM image of the electrostatic actuators.

IV. Experimental Characterization and Results

A. Packaging of MEMS Mirror

The devices were arranged in a PCB chip-carrier, and the MEMS mirror connections between the chip-carrier pads and the device pads were performed through wire-bonding.

In order to experimentally characterize the device under low pressure, the chip carrier pin-out used was compatible with the vacuum chamber. In these tests, the devices were placed in the vacuum packaging with a glass cover, to enable the laser path to the mirror surface, and using a vacuum pump, the device was submitted to low pressure conditions reducing the damping coefficient and increasing the quality factor.

B. Experimental Setup

The resonance frequency of the device was experimentally characterized, using a laser scanner vibrometer. Here, it was possible to track the mechanical resonant modes amplitude, when the mirror is electrically excited with low voltage white noise signal. The mirror presented a first resonance mode (torsional) frequency, f_0, of 838 Hz. This frequency was then used to test and characterize the device with higher voltages to increase the FOV taking advantage of the mechanical amplification due to intrinsic high quality-factor of these type of mechanical structures.

In order to evaluate the mirror performance and FOV, an experimental setup using a laser source (1) and a linear CCD camera (3) was assembled to characterize the mirrors for larger deflection angles. An overview schematic of the experimental setup is shown in Fig. 8. This setup has a laser source pointing to the MEMS mirror (2) that can be inside the vacuum packaging to keep the mirror under low pressure. The mirror reflects the beam onto a linear CCD, aligned perpendicular to the beam, enabling a precise measurement of the FOV that the mirror is achieving using simple trigonometric calculations. The mirror deflection angle corresponds exactly to half of the FOV since the incident angle changes with the mirror motion and results in a FOV range twice larger than the mirror deflection angle range. Multiple linear stages are also integrated in the setup, to precisely adjust the distance between the mirror and the linear CCD, aligning the reflected beam with the CCD camera with a minimal error below 13.4 m°.

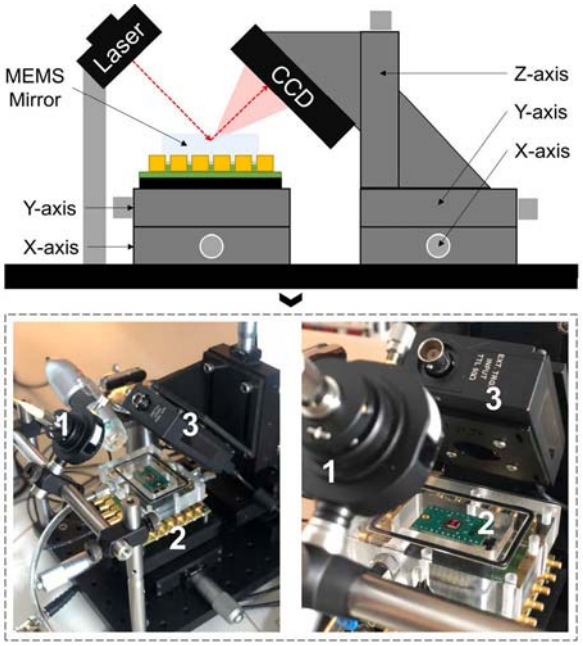


Fig. 8. Experimental setup overview.

C. Performance Analysis

Both static and resonant performance were optically characterized to validate the analytical behavior that was expected to achieve. The performance analysis was divided in two steps:

1) Static Mode: A constant actuation voltage was applied between the asymmetric combs at ambient pressure. In this mode, the air damping coefficient does not affect the mirror behavior. The actuation voltage was varied from 0 V to 80 V. Fig. 9 presents the correspondent mirror performance, and it is possible to conclude that the mirror deflection angle presents a linear behavior with the applied torque. The quadratic characteristic between the angle and the applied voltage is due to the electrostatic torque since this is proportional to the square of the applied voltage, as stated in equation (3) where V is the voltage applied, C is the capacitance of the combs and θ is the angle deflection of the mirror.

$$T_{electrostatic} = -\frac{1}{2}V^2\frac{\partial C}{\partial \theta} \tag{3}$$

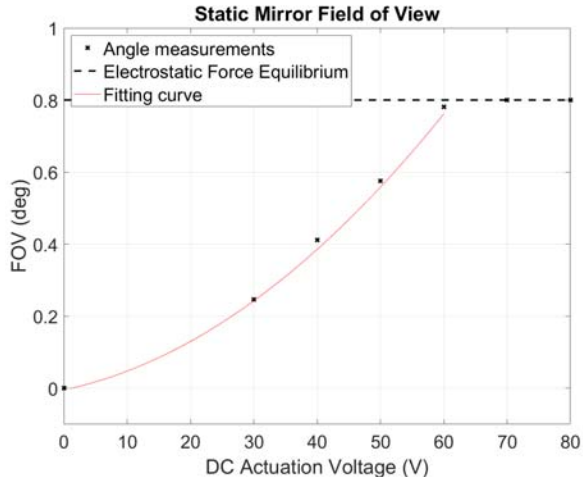


Fig. 9. Static mirror deflection performance, for an applied DC voltage between 0 V and 80 V, showing a maximum static angle of 0.8°.

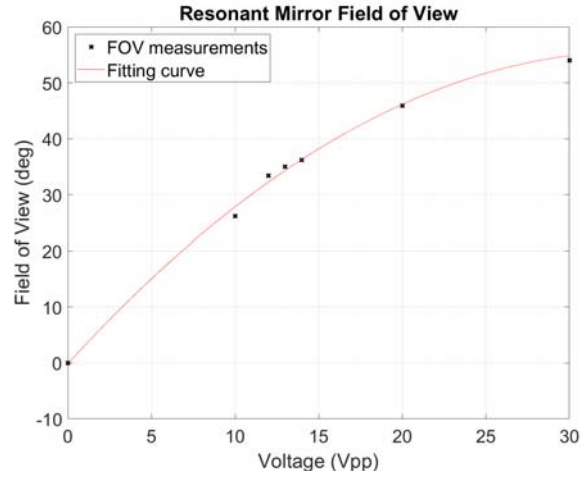


Fig. 10. Resonant mirror FOV, for an applied AC voltage between 0 Vpp and 30 Vpp, with a frequency equal to the mirror natural resonance frequency, showing a maximum FOV of 54°, under low pressure.

The mirror achieved, as analytically expected, a static maximum deflection angle of 0.8° at 70 V since this is the mechanical alignment between the asymmetric electrodes, and in this point the generated electrostatic forces are in equilibrium.

2) Resonant Mode: In this case, to electrically excite the mirror, a signal generator was used, applying a phase synchronized signal in the mirror right and left actuators independently. This experiment was performed under low pressure (below 5e-5mbar) to reduce the damping coefficient, using the vacuum chamber. The FOV for an applied AC voltage between 0 Vpp and 30 Vpp, is presented in Fig. 10. A maximum FOV of 54° was achieved, with 30 Vpp at the resonance frequency.

V. Conclusion

The fabrication and characterization of a 1D MEMS mirror for LiDAR application, based on vertical asymmetric electrostatic actuation, was presented. It was introduced a novel micromachining technique to create the asymmetry between the vertical comb actuators, merging typical SOI-based bulk micromachining processes and grayscale lithography. This technique simplifies and reduces the overall fabrication costs by also reducing the number of required lithography steps. Moreover, it bypasses the misalignment problems arising from using separate lithography steps for the different sets of electrodes with different heights.

The asymmetric combs electrodes have consistent and reproducible 2.8 μm gap, which proves this process to be an effective way to fabricate self-aligned and robust structures with different silicon levels, enabling both operation modes of the fabricated devices, static mode and resonant mode.

The mirrors were optically characterized and resonantly actuated, in a low-pressure chamber to reduce the damping coefficient, achieving a reflection FOV of 54°, at a resonance frequency of 838 Hz. When operated in the static mode, these devices achieved a maximum FOV of 0.8° at 70 V, corresponding also to the combs' electrostatic force alignment angle due to the different electrodes' heights.

In the future, this novel self-aligned multilevel micromachining process will be used in a 2D MEMS mirror that can be optimized in order to fabricate devices with more than three levels, as well as to enable the patterning of different materials, such as the metal layer and the silicon structures in a single GS mask. A typical fabrication process for this specific device would require four different lithographic processes. This has the potential to reduce the number lithography steps required for processing such MEMS structures to two (one for the front-side and another for the backside of the SOI wafer). This process could also be optimized to create more levels in the SOI device layer, such as to create membranes or springs with thinner or varying heights, which are self-aligned with the rest of the MEMS structure.

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