Enhancing Course Objectives for a Sophomore Electronic Devices Class via Peer-Led Team Learning (PLTL) Model and Attached Projects

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***Abstract*— This Full Innovative Practice paper presents a new Peer-Led team Learning (PLTL) recitation model for the sophomore Electronics Analysis and Design course, emphasizing device physics, device models, and analog and digital applications in the Department of Electrical and Computer Engineering at IUPUI. This new PLTL model with small number of students assigned to one peer-leader has enabled students to cooperate with each other and build teamwork, to get more practice with course software, and to better understand the course design component. This new model has overall improved the students' performance in the course. The new model has also enabled the instructor to introduce students to some research topics which led to students being encouraged to enroll in higher level related courses and to pursue further research in these areas. This paper details the structure of this new model, the feedback from students, the PLTL model recitation guidelines for the course semester, and attached projects. The paper also assesses the course objectives using this new model as compared to previous offerings.**

Keywords—PLTL, ECE, sophomore, Electronics, Projects

I. INTRODUCTION

In a Peer-Led Team Learning (PLTL) model, undergraduate students who have leadership skills and who have previously done very well in the course are encouraged to apply for and are recruited to become peer-leaders. Each peer-leader, typically once a week and as an integral part of the course, leads a small team of four to six students (focus group) from a class in a problem-solving PLTL workshop. IUPUI has a history of using this PLTL model. It started over a decade ago with the Chemistry Department implementing the model in its Level 1 and 2 Chemistry courses. This model has seen incredible success, and research on the courses showed a 60% increase in students achieving a C or higher in the course [1] – [6]. The prior successes led the Purdue School of Engineering and Technology at IUPUI to consider this model. The goal was to target courses with historically high D and F grades and with high Withdraw rates (DFW) within the sophomore year of study. The intention was to increase student success while also bolstering retention rates. The motivating theory was that once students pass their 2nd year, they have obtained the required skills and tend to finish their degree. With the help of the Engineering and Technology Student Council (ETSC), the Biomedical Engineering department implemented the first PLTL Engineering courses. In the Fall of 2017, the Mechanical Engineering department began a PLTL workshop in ME 20000 (Thermodynamics I). The first iteration of the model hired 12 student leaders to teach approximately 120 students based on candidate applications and their demonstrated high

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performance in the previous semester's course. Workshops were offered within the schools to publicize the new PLTL models for enhanced education. Spring 2019 marks the first implementation of the PLTL model for the ECE program, where it is offered in the ECE25500, Introduction to Electronics Analysis and Design course. Typically sixty students are enrolled in this introductory required course for electrical engineering majors; six peer leaders were hired for the implementation of the new PLTL model.

Various assessment tools have been utilized in order to evaluate the success of the new model. Among those were a survey questionnaire collecting students' feedback for the focus group sessions to determine the effectiveness of the workshops, along with identifying possibilities for improvement. Close scrutiny to feedback from surveys collected from both the student-leaders and the students, has assisted with this new model. The survey results have led to modifying the way the sessions are conducted, for better understanding of course materials. The course is offered once each year, at each spring semester, and the same instructor has been teaching the course for many years. The difficulty level of the course exams are comparable from one semester to the next, so that the students' performances in similar exams over two successive years are considered for assessing the class performance and the impact of this new PLTL model.

Through IUPUI's Center for Teaching and Learning (CTL), the school has offered a mandatory leadership course for all the student-leaders for this PLTL program. It was realized that more effort should be put into developing leaders and teaching skills in order to make the peer-leaders more effective. A current development has been to hire "Superleaders" to direct each of these courses. These superleaders are previous leaders who managed the details of the course, ran the application process, and supported the leaders via workshops. Superleaders meet with student-leaders at least twice a semester to discuss areas of improvement, both in the program and in the student-leaders' effectiveness.

Prior to PLTL, these courses used the traditional method of recitation, by working through questions or by additional example problems done with the entire class. It was noticed that students didn't seem to learn much through this passive mode of learning and often were too afraid to ask questions in front of such a large group of peers. Additionally, unless required to be present, many students skipped recitation sessions. PLTL, on the other hand, focuses on collaborative study in small groups with active learning. Students are given a quiz at some point in the PLTL workshop to encourage attendance and to check learning, but then the students work collaboratively through a worksheet of problems. The student-leaders are paired in groups with about 10 students to each leader. Beyond just leading the workshop, the student-leaders help students solve problems with different approaches, giving more time behind the reasoning of every step in the approach. Since the leaders are peers, students feel much less intimidated to ask questions. One of the main principles of PLTL is the idea of redirection; asking questions to guide students towards a solution through their own problem-solving skills. Rarely will the leader answer a question, but rather they "redirect" the question back to the student's knowledge from lectures. This helps identify gaps in understanding and teaches students how to think through problems on their own. Leaders meet once a week with the professor to discuss that week's material as well as work through issues that came up the previous week. This allows the professor to gain feedback on how students are receiving the lectures so that adjustments can be made.

II. COURSE MODEL

The teaching model used for the Introduction to Electronics Analysis and Design course during the spring semester of 2019 at IUPUI consists of several parts, with the components for grades being split.

First, the students meet twice a week for a lecture given by the course instructor. During this time the material is taught and several examples are explained in appropriate detail. Once every two to three weeks a test is given, primarily over material recently covered but also over material covered in prior sections. The final at the end of the semester is also given during this (normally instructed) part of the class. In total, 95% of the class grade comes from this instructed part of the class: 55% from the best four of five tests, 40% from the final.

Second, the students meet once a week with peer-leaders for a mandatory PLTL workshop. According to the PLTL model, the students are given several problems to work through in groups of five or six students with the guidance of the PLTL leaders, who answer questions or direct students toward the solutions. During this time the students are free to ask whatever questions they may have in order to get a better understanding of the material or to clarify specific elements of the lecture and material. Toward the end of the PLTL workshop, a quiz is given that acts as both an attendance grade and an understanding check. A quiz typically consists of two or three questions from the workshop session, and is closed-note. These quizzes make up 5% of the total course grade.

Throughout the semester the students are also given weekly homework for extra practice of the material. This is usually only a few questions over material covered in recent lectures. The homework is due at the beginning of the PLTL workshop session and is graded by one of the peer-leaders. The homework makes up of 5% of the total course grade.

All of the above results in a course total of 105%, resulting in a built-in 5% of extra credit that comes from the course

attached projects.

Finally, course projects using CADENCE and PSPICE are assigned periodically for extra credit, the purpose of which is to show how to use circuit analysis tools to build and simulate semiconductor technologies, and to develop a better, "hands-on" understanding of how these devices work. Students work in teams of three to integrate the course knowledge from various sections into an integrated circuit system. The system consists of mainly three stages: (1) The input stage such as a differential amplifier for a given input impedance and voltage gain, (2) the intermediate stage designed for a given amplification and for differential input to single-ended output conversion, and (3) an output stage such as a class AB power amplifier. The integrated circuit could be from CMOS, BJT, or BiCMOS technology.

The peer-leaders also grade these course projects; the majority of students end up completing the projects. The amount of extra credit will vary, depending on the project type and the difficulty level.

III. COURSE OBJECTIVES

The ABET accreditation objectives for this course are as follows.

Upon successful completion of the course, students should be able to:

1. Use the Shockley diode equation for simple voltage-current calculation.
2. Determine parameters in the Shockley diode equation from voltage and current data.
3. Solve for the voltage and current in a single-diode circuit using the Shockley diode equation.
4. Determine the states of diodes in a DC circuit using the Methods of Contradiction and Confirmation.
5. Perform dc bias analysis and design for bipolar transistor and MOSFET circuits.
6. Perform ac analysis and ac design for BJT and FET circuits.
7. Determine the lower 3 dB frequency of a transistor amplifier.
8. Select coupling capacitor values for a prescribed lower 3 dB frequency.
9. Analyze a capacitive-coupled multi-stage amplifier.
10. Design a cascaded amplifier to achieve voltage gain, frequency bandwidth, input impedance, and output impedance.
11. Analyze integrated circuit biasing circuitries.
12. Simulate a cascaded combined MOSFET BJT amplifiers using PSPICE.

IV. ISSUES ADDRESSED BY THE PLTL MODEL

In general, Peer-Led Team Learning helps students to gain more understanding and a firm grasp of the subject or the chapter. This new method employed in the Introduction to Electronics Analysis and Design course, ECE 25500, solves prior issues such as:

Limited time for practicing software

In the past, there was only one teaching assistant (TA) for the entire class. Introduction to Electronics Analysis & Design is a class that introduces MOSFET, CMOS, and BJT device to students; therefore, actual simulation ability should be prioritized. But it was difficult for one TA to effectively cover all these parts. With the new PLTL model, there are 6 peer-leaders for the class which allows each peer-leader to help a small number of students to understand the software (Cadence) and start building different types of amplifiers. This simulation skill will be useful in future related courses, where the students can produce their own components.

Design component

The design component in ECE 25500 is somewhat challenging and sometimes complex; having multiple peer-leaders has been beneficial and helpful for students. Peer-leaders have successfully completed the design component of the course in the past, and therefore their knowledge will help the small groups in their sessions. By not relying only on one TA for the entire class, and spreading the work between six peer-leaders, design concepts are better related to the students.

Team work

The role of each peer-leader is to foster team work which helps students to develop critical thinking or a different way to approach a problem. Having a small group, allows students to feel free to ask any question without having to worry about what classmates will think about the question. Increased levels of comfort and cooperation produce improved team skills compared to the prior methods.

V. NOVELTY OF THE NEW MODEL

The novelty of this new PLTL model used in the Introduction to Electronic Circuits, Analysis and Design (ECE25500 at Purdue system) is three-fold:

1) The new PLTL model has enabled the instructor to introduce students to some research issues. For instance, after covering the silicon devices, the following topics were introduced:

- Low power consumption
- High switching speed, and
- Level of integration

In the research topics, other materials, such as Graphene, are introduced. With these introduced topics, five students continued to do research in summer. Three devices were pursued: FinFET (Fin Field Effect Transistors), GNRFET (Graphene Nano Ribbon Field Effect Transistors), and TFET (Tunneling Field Effect Transistors). Students have worked in collaboration with ECE graduate students. A weekly research

meeting was formed during summer time with weekly progress presentations from students. Discussions on research challenges and approaches are always applied. The outcomes of these summer activities often result in publishable work in journals and conference proceedings.

2) The new revised course is required for the electrical engineering (EE) majors, while computer engineering (CmpE) students may take it as an elective. EE majors may follow up with the semiconductors course (ECE30500 at Purdue System), then sign up for the ECE55900 (MOS VLSI at Purdue system). In the past, CmpE students may not have been prepared to take the follow-up ECE55900 course. However, with the new model, they may be allowed to pursue the ECE55900 with a permission from the curriculum committee.

3) The new course has highly motivated students and has given them confidence in using CAD tools such as Cadence and ADS. Many of them have been encouraged and have signed up for the next electronics course ECE45500 (Integrated Circuit Engineering).

The positive response from students who pursued the PLTL model has encouraged the department to try the same model with other courses. The next course in the PLTL list now is the Introduction to Electrical and Electronics (ECE20400) course which is required for mechanical and energy engineering students.

VI. Exam Results Data

A clear improvement of overall test performance (as compared to the Spring 2018 section of this course offered without the PLTL) can be noted across all data.

In Spring 2018, the average scores for test 1, test 2, test 3, test 4, and test 5 were 69.1%, 71.4%, 66.5%, 80.8%, and 65.9% respectively. In Spring 2019, the average scores for test 1, test 2, test 3, test 4, and test 5 were 79.4%, 77.9%, 70.3%, 85%, and 67.9% respectively. This shows average scores for test 1, test 2, test 3, test 4, and test 5 increased by 15%, 9%, 6%, 5%, and 3% respectively. However, the average score did drop in Spring 2019 compared to Spring 2018 for the final exam, from 62.8% to 57.3%. Nevertheless, the overall average exam score increased by 7.6%.

Table 1 and Figure 1 show the comparisons of different exam average scores.

Averages	No PLTL (Spring 2018)	PLTL (Spring 2019)
Test 1	69.1	79.4
Test 2	71.4	77.9
Test 3	66.5	70.3
Test 4	80.8	85
Test 5	65.9	67.9
Final Exam	62.8	57.3

Table 1: Exam Average Scores

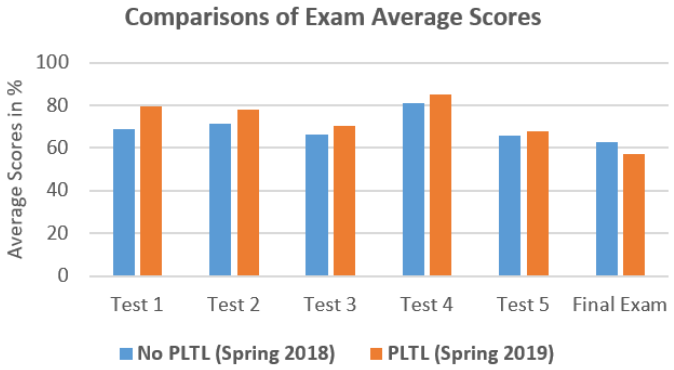

Fig. 1: Comparisons on Exam Average Scores

The medians for each test also improved. The median on test 1 in 2018 was 70%, with a median of 83.3% in 2019. For test 2 the median improved from 78% two 83.3%. For test 3 the median improved from 68% up to 70%. The median on test 4 increased from 84% to 90%. The median on test 5 improved from 64% to 73.3%. The median on the final exam, however, dropped from 63.8% in 2018 to 59.4% in 2019.

Table 2 and Figure 2 show the comparisons of different exam median scores.

Medians	No PLTL (Spring 2018)	PLTL (Spring 2019)
Test 1	70	83.3
Test 2	78	83.3
Test 3	68	70
Test 4	84	90
Test 5	64	73.3
Final Exam	63.8	59.4

Table 2: Exam Median Scores

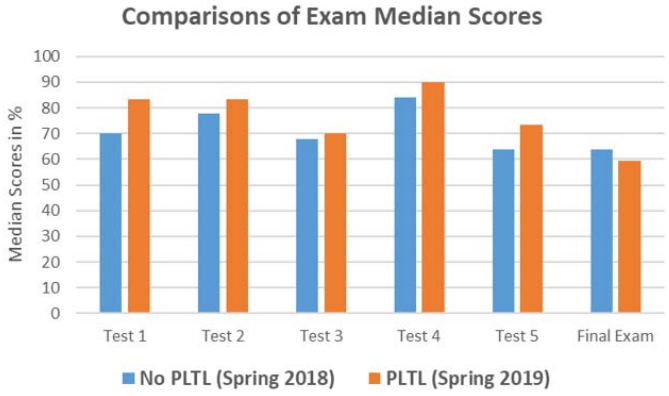

Fig. 2: Comparisons on Exam Median Scores

The standard deviations of all test scores are illustrated in Table 3 below.

Standard Deviations	No PLTL (Spring 2018)	PLTL (Spring 2019)
Test 1	18.66	18.22
Test 2	19.67	19.15
Test 3	19.05	17.38
Test 4	12.87	14.61
Test 5	18.05	25.78
Final Exam	17.04	21.98

Table 3: Standard Deviation of Exam Scores

The grading scale for ECE 255 is replicated below in Table 4. Upon analysis and as shown in Figure 3, the letter grades for students were shifted upward for the spring 2019 cohort as compared to spring 2018.

Letter Grade	Percentage
A+	90%
A	83%
A-	80%
B+	76%
B	73%
B-	70%
C+	66%
C	63%
C-	60%
D+	56%
D	53%
D-	50%

Table 4: ECE 255 Grading Scale

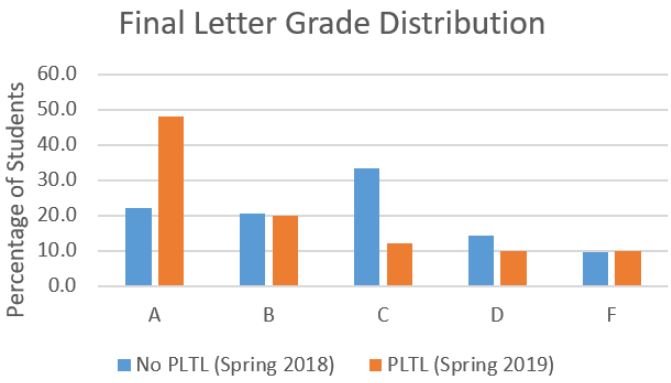

Fig. 3: Comaprisons of Final letter Grade Distribution

VII. SURVEY RESULTS DATA

In addition to comparing test results data, a survey was taken to gauge student satisfaction with the PLTL model as implemented. Students were offered five points of extra credit to complete a brief multiple-choice survey to gauge the effectiveness of the PLTL model.

The multiple-choice questions allowed five responses, ranging from Strongly Disagree, Somewhat Disagree, Neutral, Somewhat Agree, and Strongly Agree. These responses are ranked from 1 to 5 in the data below.

Students were asked more specific questions regarding the PLTL model. First they were asked to rank a response to the statement "Working with my classmates in small groups has helped me gain a greater understanding of the material."

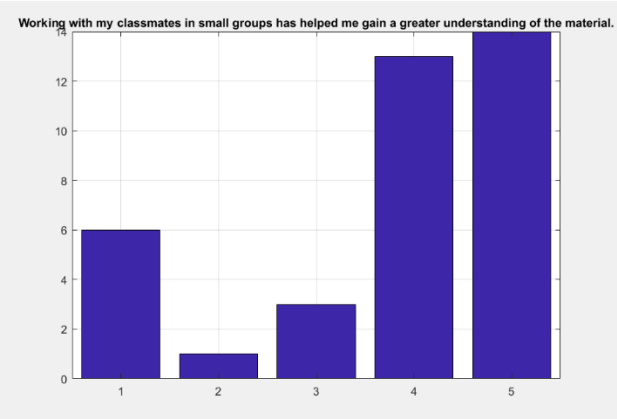

Fig. 4: Responses to "Working my classmates…"

When asked more specifically about classmate team work, students tended to agree more strongly. The numerical average for this question was a 3.8 out of 5, indiciating a more favorable disposition.

Next, students were asked to rank their response to the statement "The problems in the recitation help me in understanding the course material better." These responses were by far the most favorable, indicating that the material covered in the (PLTL model) recitation was deemed helpful by the students.

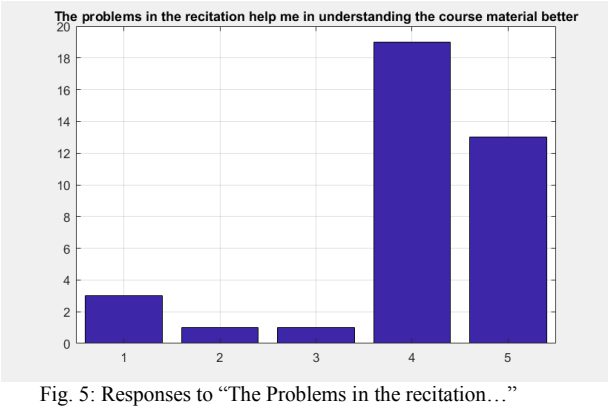

Fig. 5: Responses to "The Problems in the recitation…"

The numerical average response to this question was a 4.0 out of 5.

Finally, the students were asked to rank their agreement with the statement that the (PLTL model) recitation had improved their performance on exams.

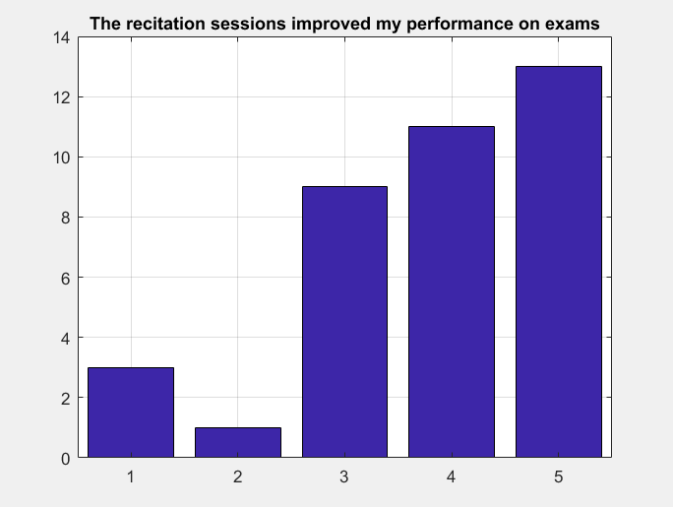

Fig. 6: Responses to "The recitation improved…"

For the most part, it is clear that students believe that the (PLTL model) recitation has helped to improve their exam grades. The average numerical response to this question was 3.8 out of 5.

VIII. CONCLUSION

Though it is certain that there are refinements that can be made to the implementation of the PLTL model into ECE 25500, the above data clearly indicates a marked improvement in student success in the course as compared to the previous semester's use of a traditional recitation style. The higher numbers from 2018 final exam were attributed to a higher bonus point (5%) that was given to encourage students to do extra project since the attached projects in 2018 were not applied.

The new model requires more hours from and compensation for undergraduate peer-leaders. Extra efforts are also needed for scheduling and to ensure appropriate rooms for conducting the PLTL workshop sessions. The outcomes of the this new model, better reveal the students' and peer-leaders' talents, and assist them to pursue research work in related areas.

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