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ORIGINAL RESEARCH PAPER

Electronic-photonic board as an integration platform for Tb/s multi-chip optical communication

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Abstract

Chip-on-board silicon photonics O-band wavelength-division multiplexing transceivers have been developed that will eventually enable high-throughput on-board optical communication for multi-socket on-board communication. This direct, any-to-any configuration yields low-latency, low-power optical communication among multiple compute nodes on the board. Silicon photonic transceiver chips are flip-chipped on a polymer waveguide containing an electro-optical circuit board using adiabatic coupling and then completed with driver and amplifier electronic chips. A transceiver assembly based on wire-bond technology verifies 50 Gb/s operation per channel, and the flip-chip version demonstrates the chip on-board assembly techniques for compact on-board transceivers.

1 | INTRODUCTION

The need for low-latency, high-data throughput for multi-socket boards is caused by the trend of increasing inter-core cooperation and workload parallelization to sustain constant growth in computing power [1]. The European research and innovation project ICT-STREAMS proposes a combination of wavelength multiplexing, a cyclic arrayed waveguide grating router, and board-level optical interconnects as a potential solution. This yields collision-free, all-to-all connectivity among multiple sockets with potential data throughput of 12.8 Tb/s in a 16-socket configuration [2].

Compact on-board transceivers located very close to the compute nodes are a crucial aspect of this optical multi-socket board approach. They convert signals between the electrical and optical domains. Optical signal routing is realized by embedded board-level waveguides, the so-called electro-optical printed circuit board (EOCB). Chip-on-board (COB) direct attachment is considered a very effective way to realize a compact transceiver. This is accomplished by directly bonding integrated silicon photonic chips and electronic chips onto the board and interfacing them with the optical and electrical interconnects of the EOCB [3]. Basic devices for this type of on-board transceiver are low-energy drivers and amplifiers and high-performance integrated photonic chips with transmitting and receiving capabilities on eight wavelength-division multiplexing (WDM) channels at 50 Gb/s line rate.

Development of the on-board transceiver as basic optical communication unit, which is required to eventually form the proposed multi-socket board, is reported on herein.

2 | CHALLENGES AND APPROACHES FOR PHOTONIC INTEGRATION

2.1 | System aspects

For large systems with multiple computing nodes, the direct connections among nodes are critical in terms of bandwidth, latency, and power consumption. Optical interconnects provide a solution to these challenges, and with integrated photonic chips aiming for cost-efficiency in the near term, they will eventually become commercially viable [2,4]. Placing the electro-optical conversion device—for example, the optical transceiver—close to the computing node and therefore minimizing the length of the electrical trace will help in overcoming

electrical limitations [5]. Low-latency, non-blocking, any-to-any communication is enabled by an arrayed waveguide grating router (AWGR) [1,6,7]. In this case, the AWGR chip includes adiabatic taper structures that enable direct optical coupling to the waveguides on the host board.

A main driver for on-board photonic integration is the optical link budget. Minimizing the number of interfaces and increasing the efficiency of the optical coupling are eventually beneficial for system performance.

2.2 | Transceiver development

The WDM O-band transceiver development discussed herein is based on an eight-channel silicon photonics transceiver mounted in combination with high-speed electronics on a host board. In the first stage, a transceiver assembly (type W) is realized to verify that the developed components achieve the targeted optical data transmission performance. In the second stage, similar components are used to demonstrate the anticipated on-board transceiver module (type F). While the electronics chips are identical, silicon photonic transceiver chips allow for adiabatic optical coupling from silicon to polymer waveguides.

2.3 | Fast and efficient integrated electronics

The fast and power-efficient modulator driver and transimpedance amplifier (TIA) are key devices to enable Tb/s multi-chip optical communications. The driver has been realized in a SiGe (silicon germanium) BiCMOS (bi-complementary metal oxide semiconductor) 55 nm technology featuring on-chip equalization and a differential driving scheme. In a single-ended driving stage, the current in the dummy supply rail or load does not contribute to modulation but still consumes significant power. When driving differentially, we also drive the cathode when transmitting at zero rather than dumping this current in a dummy load. This improves driver performance in two areas: (a) power consumption and (b) drive voltage. For the same drive voltage, we thus halve the power consumption (e.g. 20 mA static current in the differential driver vs. 40 mA in the single-ended case). Additionally, unlike a conventional differential pair, we have proposed a new differential output scheme using a modified supply network to DC-couple and bias the modulator. Integrated with a 50-µm-long GeSi electro-absorption modulator (EAM), open eye diagrams for 70 Gb/s after transmission over 2 km standard single-mode fiber were demonstrated. Total power consumption is 61 mW, corresponding to 0.87 pJ/b at 70 Gb/s [8].

We also propose a new differential TIA scheme for the high-speed receiver input. A conventional TIA input is typically connected to either the anode or cathode of the photodiode (PD), while the other PD pin is connected to a bias voltage. Receiver (Rx) sensitivity can be improved by processing the PD current (IPD) differentially using both cathode and anode as high-speed inputs. Sensing IPD differentially doubles TIA gain and improves the signal-to-noise-ratio by $\sqrt{2}$. The increased front-end gain reduces the contribution of the amplifying stages to the total input referred noise and reduces their gain requirement by 6 dB. This lowers the power consumption, as fewer gain stages are required. Integrated with a silicon photonic PD, receiver operation below KP4 forward error correction (2.4×10^{-4}) is demonstrated up to 90 Gb/s with a sensitivity of −7.1 dBm optical modulation amplitude while only consuming 222 mW, corresponding to 2.47 pJ/b [9].

2.4 | Integrated silicon photonic chips

An eight-channel WDM silicon photonics transceiver chip fabricated on imec's ISIPP50 G platform is deployed in this work. The transmitting section is based on four carrier-depletion-type micro-ring modulators. Ring diameter is 7.5 µm with a Q-factor of approximately 5000 and a −3 dB bandwidth of 33.8 GHz. Integrated heaters are used for wavelength fine tuning of each RM. Signal multiplexing is based on cascaded double-ring resonators. Four Ge-based waveguide photodetectors with a −3 dB bandwidth of 50 GHz together with a cascaded double-ring resonator demultiplexer constitute the receiver section of the TRx chip [10].

The wire-bond version of the transceiver chip is used for the transceiver assembly and provides grating couplers to access the optical signals with a fiber array block from the top side. The flip-chip version contains an array of adiabatic tapers that interface with the polymer waveguide cores on the board.

2.5 | Photonic host board

The EOCB as photonic host board provides an electrical or optical interface to photonic integrated chips (PICs), integrated chips, and the various other components required to complete the system.

2.5.1 | Optical interface

An inherent challenge in assembling PICs remains the small spot size (mode field diameter)—in the range of 1 µm. Position accuracy and spot size conversion need to be well controlled to reduce optical coupling loss to below a system-dependent target value. Conventional butt coupling to a board-type waveguide would rely on on-chip spot size converters. The small mode field diameter of demonstrated converter prototypes would still yield a large mode field mismatch (coupling loss) and a very tight alignment tolerance when coupled to on-board waveguides with mode field diameters compatible with conventional single-mode fibers. The use of conventional grating couplers in this WDM application is limited by their strong wavelength dependence, relatively high insertion loss, and missing on-board light-turning features.

A solution to this problem provides the adiabatic coupling approach between silicon photonic waveguide taper and polymer waveguide cores [11,12]. It inherently provides

adequate spot size conversion, low insertion loss over a wide wavelength range (>200 nm) and for both polarizations (within 1 ± 0.5 dB for TE (transversal electric) and TM (transversal magnetic)), and relaxed, lateral alignment tolerances (approximately ±1.5 μm) [13]. Thus, adiabatic coupling has been implemented in this work based on the advantages provided for PIC on-board integration. Figure 1 illustrates the adiabatic conversion from the silicon taper to polymer waveguide mode. The basic flip-chip configuration is shown in Figure 2.

The polymer waveguide core is mainly defined by a targeted low-mode file mismatch to the standard single-mode fiber (SMF-28). Core and cladding material exhibit a difference in refractive index. This difference is defined by the material formulation and to some extent by the processing of core and cladding. An eventual absolute difference in refractive index ($n_{core} - n_{clad}$) of approximately 0.005 leads to a targeted core size of 5.5 μm to yield single-mode operation and low coupling loss to fibers.

2.5.2 | Electrical interface

Flip-chip bonding is used as a compact integration scheme for the final on-board transceiver module (type F), while wire bonding is preferred for the transceiver assembly (type W). An evaluation revealed the TRX70 (Ardent Concepts) as suitable solderless compression connector for good signal integrity up to 70 GHz for multiple differential signals.

2.5.3 | Chip interface

Besides the optical and electrical interface, the chip needs an adequate mechanical interface on the board for a successful flip-chip assembly. The top side of the polymer waveguide cores—for example, the counterpart of the silicon photonic tapers—must be very planar to ensure a bond line thickness between silicon and polymer core thinner than a few hundred nanometers.

2.6 | Assembly challenges

The challenges of the assembly are to realize a multi-chip module in COB technology where the demands of radio frequency (RF) performance and of the optical functions of the EOCB are combined. The requirement for good RF performance results in very short low-loop wire bonding on small bond pads to minimize parasitics. For the optical function, the board material has turned out to be more difficult to handle by the wire-bonding process because of its lower rigidity and the more difficult metallization processes of the board. The combination of electrical and optical coupling in a single flip-chip process step using different adhesives while requiring lateral alignment tolerances within a region of a few micrometers is very difficult to realize.

3 | PHOTONIC BOARD: DESIGN AND MANUFACTURING

3.1 | Photonic board requirements

The key requirements for the EOCB are derived from the optical and electrical interface between chip and host board. Due to the compact size of silicon photonic chips, the exposed polymer core waveguides, which are part of the adiabatic coupling interface, must be placed close to electrical pads on the board; see Figure 5. In addition, the relative positioning tolerance (lateral and vertical) between electrical pads on the chip and the board is in the range of ±5 μm. The fabrication of polymer waveguides with precise vertical control in terms of core thickness and position in order to reach high optical performance requires the

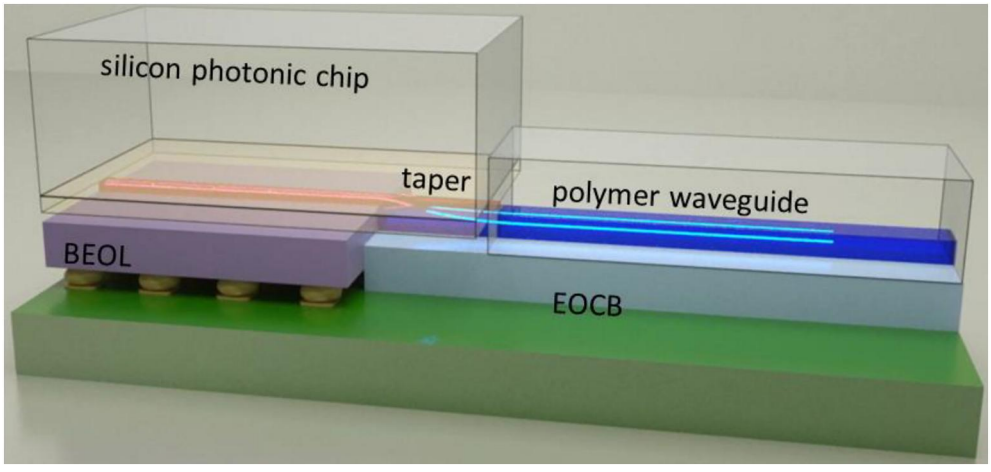

FIGURE 1 Illustration of adiabatic coupling from silicon photonics into polymer waveguide (electro-optical printed circuit board [EOCB]) in a flip-chip configuration (movie on www.ict-streams.eu)

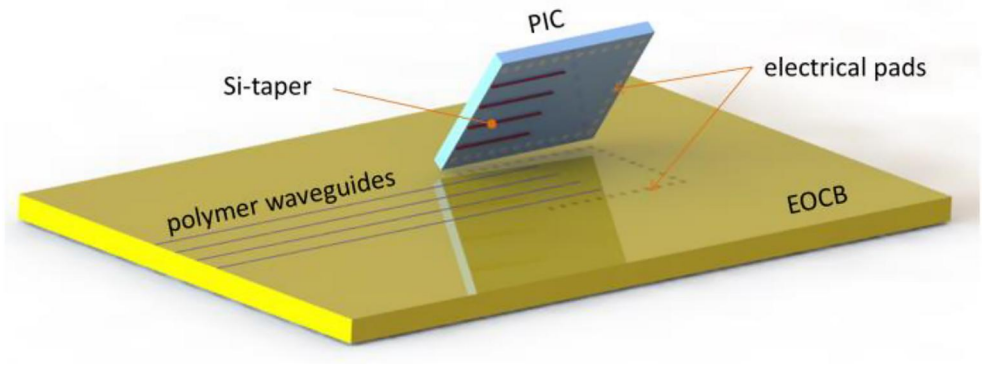

FIGURE 2 Illustration of electro-optical printed circuit board (EOCB) and photonic integrated chip (PIC) with respective adiabatic optical coupling interface and electrical pad arrays before assembly

substrate, in this case the electrical circuit board, to have low thickness variation and topography. The target data rate for non-return to zero (NRZ) signals over the electrical transmission lines is 56 Gbps to the PIC. The bond pads on the board should provide good adhesion for wire and solder bonds [3].

3.2 | Layer build-up

The layer build-up of the photonic board has been developed to fulfil requirements for flatness, topography, lateral thermal expansion, and high-speed signals. The dielectric core of the four-layer build-up is based on a low coefficient of thermal expansion (CTE, approximately 0.5 ppm/K) material. The outer dielectrics provide excellent high-frequency (HF) properties (dissipation factor, Df, of approx. 0.002).

The electrical high-speed traces, which are directly below the optical polymer cladding (layer O1 in Figure 3), are embedded in the HF dielectric with the top side flush. As a result, the impact of cladding on electrical performance is minimized [3].

3.3 | Board design

All RF test structures and transmission lines have been designed in Keysight ADS and simulated with the Momentum Microwave EM tool. The design substrate model is illustrated in Figure 3. Only L1 and L2 are considered in the HF simulation because L2 acts as a perfect ground (for shield). The transmission lines exhibit good signal integrity for 60 Gb/s NRZ signals [3].

Three different board types have been investigated in the course of this work. The first board, EL1, was designed for Dk_{eff} (effective dielectric constant) characterization using ring resonators (Figure 4a). The Dk_{eff} is verified through comparison of simulated and measured ring resonators on board EL1. The ring resonators are designed as microstrip lines. Compared with coplanar waveguides, microstrip lines couple more to the bottom ground plane (L2) through the dielectric layer (D12). Therefore, they increase Dk_{eff} and the contribution of the dielectric under test to Dk_{eff}. The interference pattern of the ring converts even small Dk_{eff} differences into measurable frequency differences.

In a second step, to verify the impact of the optical polymer layer on electrical coplanar waveguide performance, a test board, EL2 (Figure 4b), has been designed, and identical layouts are manufactured with and without optical cladding. Coplanar waveguides are chosen to minimize radiation losses and increase the isolation between test lines.

Finally, the transceiver module (type F) was designed as the host board for the electronic integrated chip and PIC. It provides an adiabatic coupling area below the PIC with polymer waveguides running easterly towards the board edge; see Figure 5 (top). Landing areas for HF connectors are located at the north and south sides of the EOCB.

3.4 | Photonic board manufacturing

The fabrication process of the electrical substrate starts with the patterning and lamination of HF signal layers L1 and L2 for ground and power. A via formation (L1–L2) completes this stack. Layers L3 and L4 are patterned, and the blind vias formed, prior to the lamination of the complete stack using the low-CTE dielectric as the core. Through-chip vias complete the stack. Finally, the bond pads and connector areas are coated with bond-quality electrolytic nickel gold. The embedded signal traces (L1) and applied lamination sequence enable a very low-topography substrate [3].

The boards with the layout for the transceiver assembly (type W) are now ready for wire-bond assembly, and the subpanels containing boards for type F transceiver modules are used as electrical substrate for the EOCB manufacturing process.

The lower cladding layer is applied to the subpanels using a linear coating system and structured using mask lithography. A thin layer of fine-patterned polymer, which acts as solder resist, lies thereby between the board surface and lower cladding. Subtracting the solder resist thickness of 10 μm from the targeted vertical gap dimension between chip pads and board

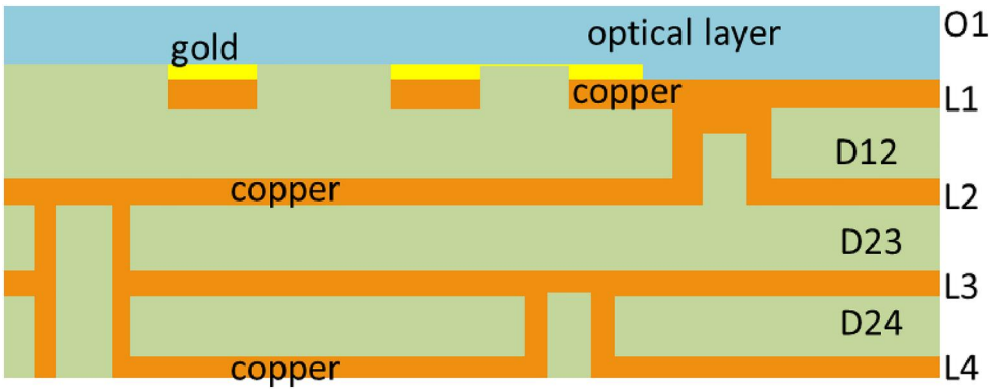

FIGURE 3 Illustration of layer build-up for four-layer (L1–L4) and two-layer (L1–L2) boards

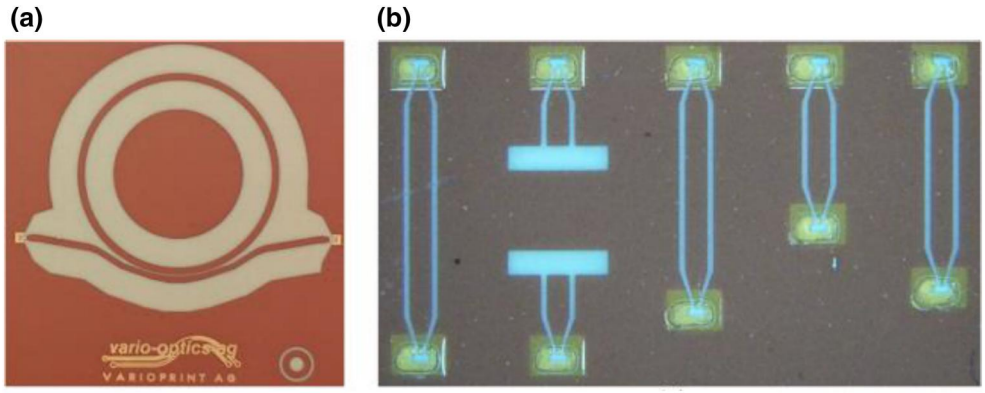

FIGURE 4 Photograph of (a) ring resonator on the EL1 board and (b) transmission lines placed on the EL2 board

pads yields the lower cladding thickness—for example, a 40 μm vertical gap dimension yields a lower cladding thickness of 30 μm. An important design consideration is to minimize the total area of openings and the size of each opening in the lower cladding near the adiabatic area in order minimize the distortion of the polymer core layer thickness. A separation of about four hundred micrometers between optical waveguide and pad array are ideal. The liquid polymer core layer is applied to the lower cladding using a precision linear coating system to yield a 5-μm-thick wet layer with an anticipated variation below ±5%. The tool has been qualified for ±3% thickness variation at 7 μm layer thickness on planar substrates.

A UV (ultraviolet) laser spot is used to pattern the photosensitive optical polymer. The laser direct imaging system (custom equipment) references the position of the pad layer and compensates for unavoidable distortions in the electrical substrate. This enables good position tolerance between the optical interface (waveguide and taper) and the electrical interface between chip and board. The optical waveguide layer is completed with a patterned cladding layer that exhibits a thickness of approximately 20 μm. The polymer optical layer consists of a proprietary silicone compound with excellent reliability [3].

Figure 5 (top) shows a photograph of the final EOCB for the transceiver module (type F), with the polymer waveguides running easterly from the PIC area. Figure 5 (bottom) shows a close-up of the PIC area on the board. Inside the u-shaped electrical pad area, one can recognize the array of exposed waveguide cores ready to engage with the adiabatic taper structures in the silicon photonic chip. The waveguide core top side is planar within approximately 0.5 μm. In combination with the mechanical compliance of the rather soft polymer material and the very small contact line, this should enable the required maximum vertical gap specification between silicon taper and polymer core. The assembly areas besides the PIC are for the TIA and laser diode, respectively.

4 | ASSEMBLY CONCEPT AND IMPLEMENTATION

4.1 | Concept

The described electrical system relies on high RF performance. Therefore, the components must be be mounted directly on the substrate (EOCB). This COB process [14] can be realised for both a wire-bonded assembly where the components are attached to the rear side on the board and a flip-chip assembly where the components are mounted to the top side on the board. The first variant has the benefit of electrical connections

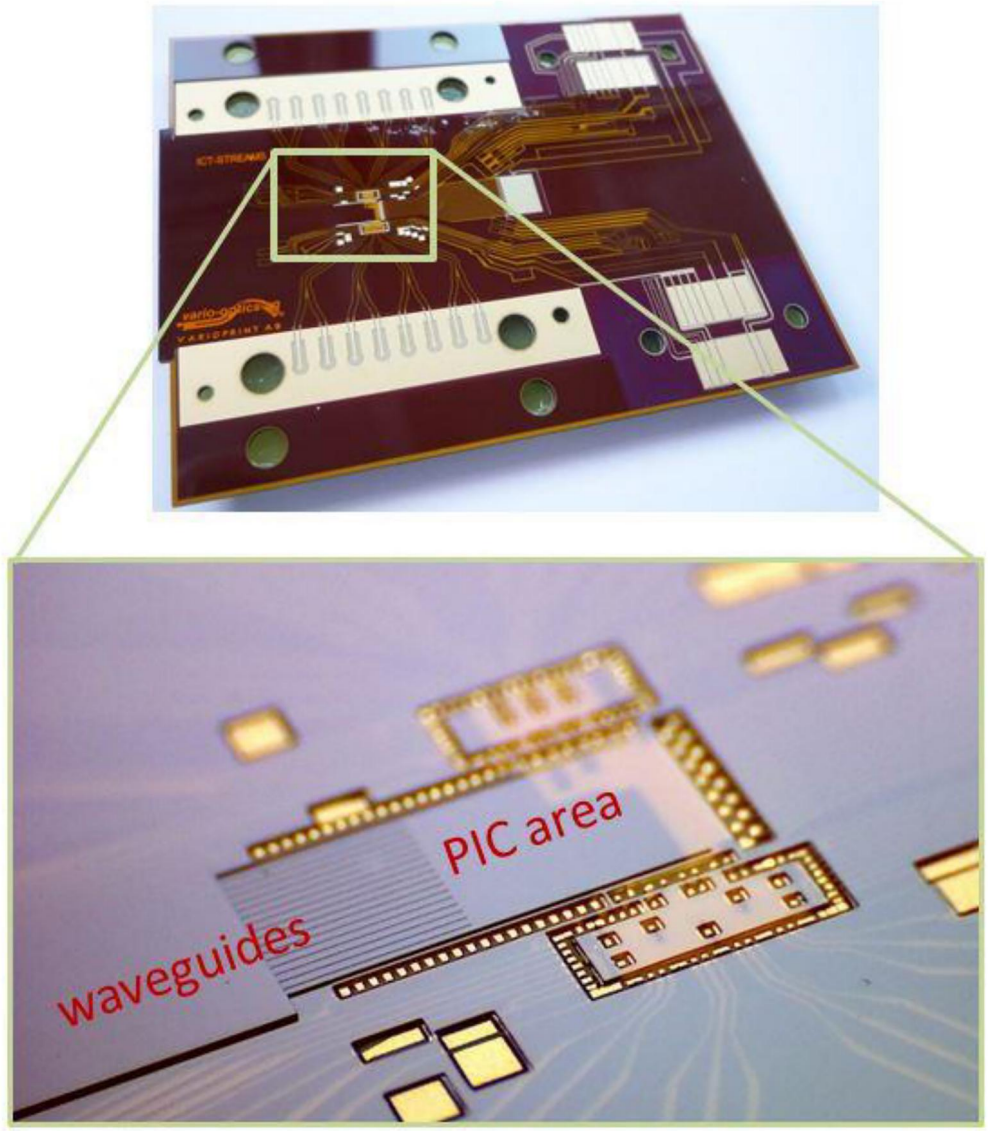

FIGURE 5 Photograph of finalized photonic board (top) and close-up of the photonic integrated chip assembly area (4h TRx version)

that remain visible and chips that are accessible for debugging purposes from the top. The flip-chip variant has the advantages of connections that are shorter in length and thus have better RF performance, and electrical and optical connections that are completed in a single process step so that higher throughput and lower manufacturing costs are possible.

Although high-precision alignment with self-alignment structures via solder surface tension is possible [15,16], gold wire bumps in combination with conductive adhesive are chosen here to simplify the process design and achieve lower assembly temperatures.

4.2 | Implementation

In a first step—the wire-bonded assembly—the PIC, TIA, and voltage driver (VD) are mounted on the EOCB and afterwards wire bonded (type W). This demonstrator enables a first evaluation of the single components of the multi-chip module system. In this wire-bonding variant, the electrical connections are visible, which allows for easier debugging.

In the second step—the flip-chip variant (type F)—each component is bumped with a gold ball wire bonder. Due to the mechanical tolerances of flip-chip bumped optical components, the height of the gold ball bumps must be controlled within a tolerance of +/− 3 μm. To control this tight tolerance, the process parameters are set by measuring the bump height with a 3D-scanning microscope. After bumping, the bumped components are dipped into electrically conductive adhesive and flip-chip bonded to the EOCB. The PIC has the highest demands on the position accuracy of the PIC optical waveguides in relation to the polymer waveguides on the EOCB to enable adiabatic coupling; the target specification of the lateral offset tolerance of those waveguides is +/− 2 μm from ideal position. This is done by passive alignment of both, using a high-precision die bonder from Paroteq [17], by visually

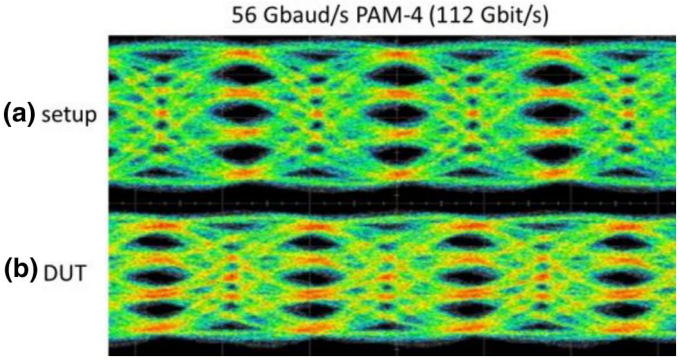

FIGURE 6 Measured 56 GBaud (112 Gbit/s) PRBS9 PAM-4 eye-diagrams transmitted through (a) the reference setup and (b) the device under test (DUT)

overlapping the waveguides in an overlay image just before joining the components. Additionally, an optical underfill must be dispensed between the components in the area of the exposed polymer waveguides on the EOCB so that the area surrounding the waveguides has the correct refraction index to enable light guiding.

5 | RESULTS AND DISCUSSION

5.1 | Board electrical performance

The electrical test board (Figure 4) is first measured with RF probing. To calibrate the probe launch and the probes themselves, through-reflect-line (TRL) calibration kits are added—one for each type of line. The lines are measured with 40 and 67 GHz RF probes and a 67 GHz PNA-X network analyzer.

TRL calibration is done both offline and with the calibration software of the PNA-X, and both cases produce very similar results. Extraction of the effective permittivity was first done using ring resonators. When comparing the simulated and measured S21 for both rings, we observe that Dk_{eff} is 3% larger than the values obtained by simulation. The error is very small and has little impact on the other test features. Extracted S-parameters after TRL on the network analyzer, including renormalization to 50 Ω impedance, indicate a very limited loss penalty due to the addition of optical cladding without adapting the design. Best loss values for 50 GHz signals are −0.37 dB/cm and −0.44 dB/cm for uncovered and cladding-covered transmission lines, respectively.

To visualize the performance of the EOCB technology, a comparative time domain measurement is made. The differential output of a 92 GSa/s arbitrary waveform generator is split into two branches with identical cables and connectors. In one branch, the device under test, consisting of two 67 GHz GSG-150 probes and a 1.8-cm-long transmission line with cladding, is inserted. The probes have typical insertion losses of −0.95 dB and −0.75 dB at 67 GHz and 50 GHz, respectively (Picoprobe® Model 67A). The output eyes are compared with a 70 GHz sampling scope. The 67 GHz RF probes and their launch sections are not calibrated in this measurement. Even in this case, the measurement does not indicate significant eye closure, confirming the HF performance of the EOCB lines. As shown in Figure 6, we have obtained open eye-diagrams at 112 Gb/s using PAM-4 modulation format through the longest transmission lines on EL2.

5.2 | Board optical performance

The polymer waveguides on the board exhibit a mode field diameter of 7 μm to ensure single-mode operation at the refractive index contrast of the current material formulation. The slightly smaller mode field compared with the 9 μm of an SMF-28 (1310 nm) is expected to cause excess coupling losses of 0.2 dB. The available materials yield propagation losses between 0.35 and 0.6 dB/cm. The fabricated boards exhibit values around 0.6 dB/cm. Eliminating this negative impact of the substrate on polymer waveguide quality requires further investigation of the aforementioned solder resist layer below the lower cladding. Low-loss coupling and spot size conversion between silicon photonic and polymer waveguides has been successfully demonstrated in simplified and isolated configurations, yielding effective coupling losses between 0.5 dB and approximately 2 dB [13].

5.3 | Assembly results

For the wire-bonding demonstrator, the PIC, TIA, and VD were die-bonded manually with tweezers using a thermally conductive but electrically insulating adhesive so that short-circuits of traces underneath the components are avoided.

Figure 7 shows the EOCB with the die-bonded components on it. The TIA and the VD are closely bonded to the PIC for shortest electrical connections and therefore highest RF performance.

The wire bonds were bonded with an FK Delvotec 62,000 ball/wedge bonder. An AW14 wire from Heraeus with a diameter of 25 μm and a PI33085-435F-ZP74 T capillary from SPT Roth were used. Figure 8 shows the fully assembled and wire-bonded demonstrator with two TIAs, two VDs, one PIC, and single-layer capacitors (SLCs) on the EOCB. The optical signals are coupled in and out of the PIC by TE-polarization grating couplers and a fiber array [18].

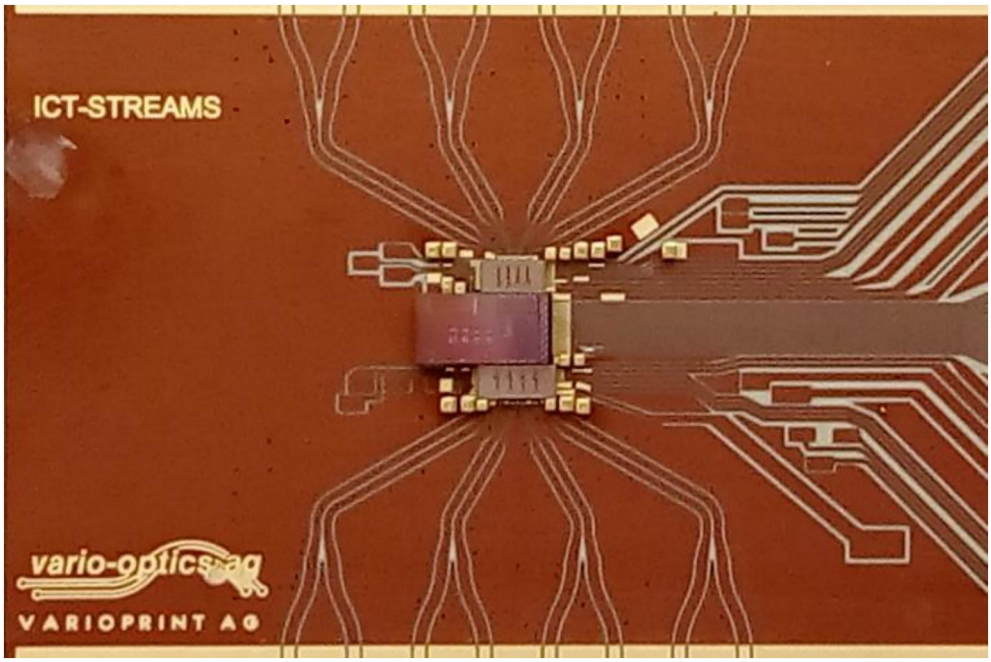

FIGURE 7 Die-bonded electro-optical printed circuit board with photonic integrated chip, transimpedance receiver, voltage driver, and single-layer capacitors

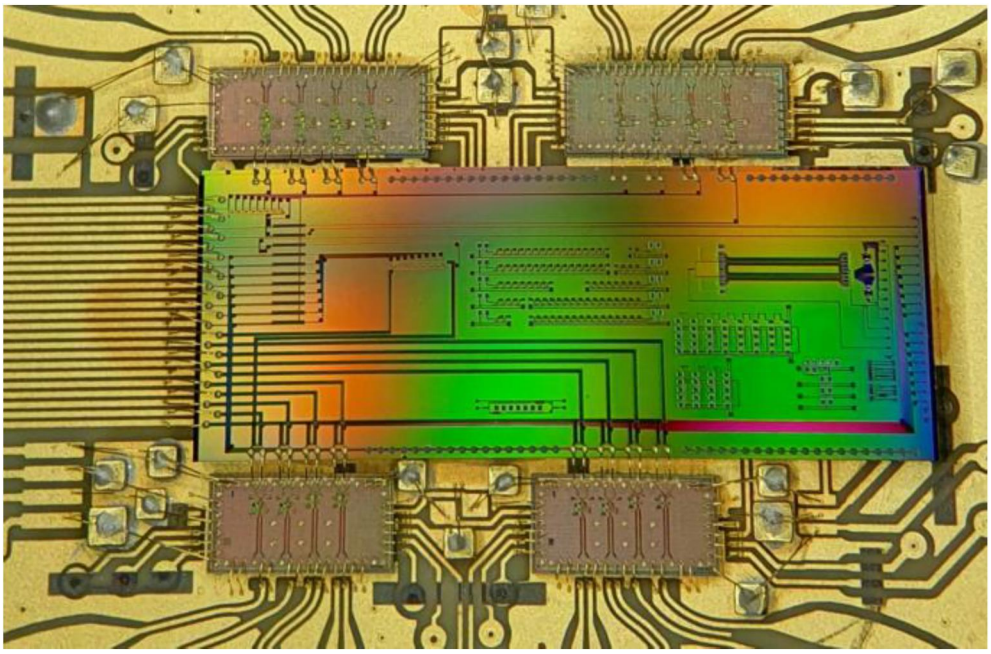

FIGURE 8 Fully assembled and wire-bonded demonstrator (eight-channel TRx)

Figure 9 shows a side view of a wire-bonded EAM driver. The wires, especially to the RF lines, are short and have low loops.

The assembly of the flip-chip variant was very challenging, since the requirements for optical and electrical connections are very different. Both connections must be realized in parallel during the same assembly step. For the flip-chip version, the electrical and optical points of the connection contacts are neither accessible nor visible after the assembly.

The requirement of the optical connection is to realize a reliable physical contact between the optical waveguide stub of the electro-optical component and the polymer waveguide on the EOCB to ensure good adiabatic coupling and a homogenous distribution of the optical underfill around the EOCB waveguides.

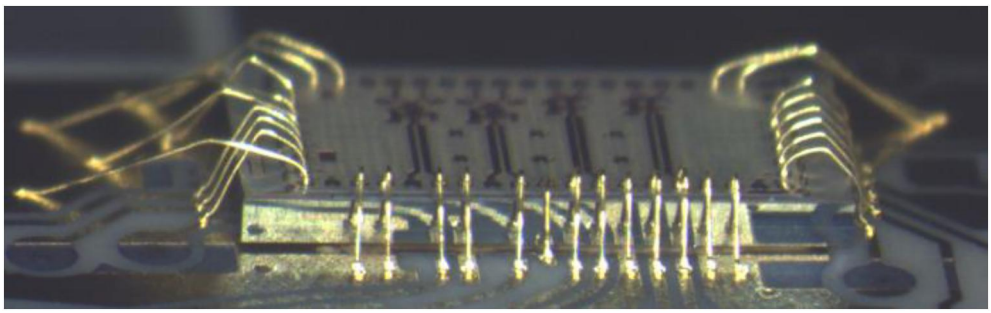

FIGURE 9 Wire-bonded electro-absorption modulator driver on electro-optical printed circuit board, side view

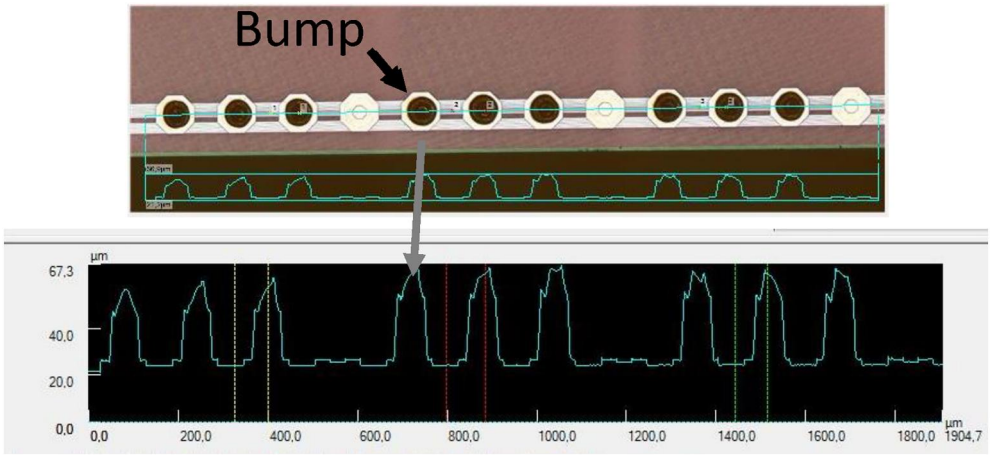

FIGURE 10 Height profile measurement of the flip-chip bumps on a photonic integrated chip

The requirement of the electrical connection is to have a reliable and stable connection with low connection resistance of the silver conductive adhesive. Figure 10 shows the profile measurement of the bumps that were wire-bonded on the PIC. Due to the high accuracy of the optical coupling, the bumps must be very accurate in height as well. The image shows the good uniformity of the bumps.

Before die-bonding these components with a high-precision die bonder from Paroteq, a silver conductive epoxy must be applied on the bumps, while optical underfill must be applied in the area of the polymer waveguides. Both adhesive applications must be completed very quickly in two steps, one after the other, and care must be taken that these adhesives do not mix or flow into each other. Additionally, care must be taken that the distribution of the optical underfill is homogenous and void-free, because any void in the area of the polymer waveguides will result in additional propagation loss.

Now the components must be aligned with each other using the overlay feature of the Paroteq die bonder. The components are then joined, and the adhesives are precured directly on the Paroteq die bonder with an integrated heating plate while applying a constant force of 5 N on the dies, which is especially important for the PIC, where the adiabatic coupling of the waveguides requires substantial force. The final cure was done in a convection oven. Figure 11 shows the fully assembled flip-chip demonstrator build-up for the ICT-STREAMS Project.

5.4 | Optical link performance

The energy efficiency of an optical link based on the herein-described eight-channel flip-chip transceiver assemblies has been estimated to be 5 pJ/b at 50 Gb/s line-rate [18].

6 | CONCLUSIONS

The fabricated boards reveal excellent electrical properties and provide a demanding electrical and optical interface for assembling silicon photonic chips. The very compact interface between the EOCB and PIC requires demanding considerations for the layout and layer build-up of the board. In addition, reducing the impact of the electrical substrate on the optical performance of the polymer waveguides is critical.

Wire-bonded and flip-chip-mounted multi-chip modules with electrical and photonic components were realized. Both assemblies were feasible, although the dimensions of the wire-bond pads, the demanding process setup of the EOCB, and the tight vicinity of the chips requires tight control of the process

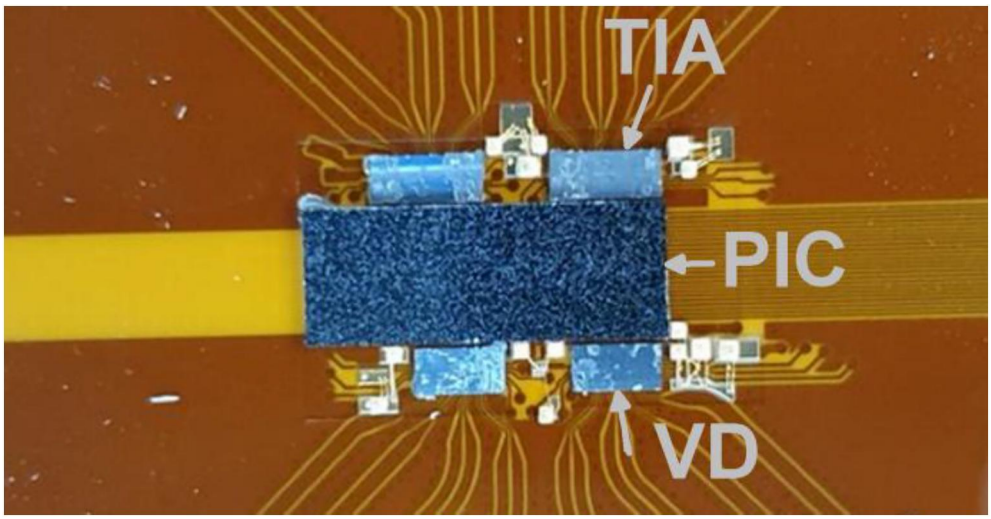

FIGURE 11 Fully assembled flip chip demonstrator with transimpedance receiver, voltage driver, photonic integrated chip, and single-layer capacitors on the electro-optical printed circuit board

parameters during production as well as experienced operators to ensure economic throughput. This is also the case for the flip-chip demonstrator, where the high demands for accuracy of the optical joints are at least partially transferred to the electrical joints. This makes the assembly of the flip-chip components challenging. On the other hand, the flip-chip assembly has the advantage of less process time and fewer process steps, which holds promise for the economic process flow of optical data transmission devices.

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