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Event: SPIE OPTO, 2021, Online Only

Wafer-Level Vacuum Sealing for Packaging of Silicon Photonic MEMS

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ABSTRACT

Silicon (Si) photonic micro-electro-mechanical systems (MEMS), with its low-power phase shifters and tunable couplers, is emerging as a promising technology for large-scale reconfigurable photonics with potential applications for example in photonic accelerators for artificial intelligence (AI) workloads. For silicon photonic MEMS devices, hermetic/vacuum packaging is crucial to the performance and longevity, and to protect the photonic devices from contamination. Here, we demonstrate a wafer-level vacuum packaging approach to hermetically seal Si photonic MEMS wafers produced in the iSiPP50G Si photonics foundry platform of IMEC. The packaging approach consists of transfer bonding and sealing the silicon photonic MEMS devices with 30 µm-thick Si caps, which were prefabricated on a 100 mm-diameter silicon-on-insulator (SOI) wafer. The packaging process achieved successful wafer-scale vacuum sealing of various photonic devices. The functionality of photonic MEMS after the hermetic/vacuum packaging was confirmed. Thus, the demonstrated thin Si cap packaging shows the possibility of a novel vacuum sealing method for MEMS integrated in standard Si photonics platforms.

Keywords: vacuum, hermetic, wafer-level packaging, sealing, iSiPP50G, Si photonics, MEMS

1. INTRODUCTION

In recent years, highly advanced commercial foundry platforms for silicon (Si) photonics have been established [1,2]. These standardized foundry platforms both enable novel photonics applications to reach the market, and provide photonics researchers easy access to state-of-the-art fabrication, thereby massively increasing the rate of innovation and development of Si photonic technology [3]. In the field of Si photonics, more diverse and novel passive components (e.g., low loss waveguides, grating couplers, splitters, and combiners) and active devices (e.g., high-speed modulators and detectors) are being developed and introduced. The introduction of standardized Si photonic foundry platforms has created an on-going trend towards improved reliability and large-scale manufacturability of integrated photonic devices. Recently, this manufacturing technology has matured enough to enable high-density integration of high-performance photonics devices, such as field-programmable Photonic Integrated Circuits (FP-PICs) [4]. Such high-density integrated devices rely on low optical loss, low power consumption, and a small footprint which can be realized by state-of-the-art photonic foundry processes. However, many active devices additionally require vacuum packaging to ensure reliable operation over long periods of time. Therefore, a reliable, cost-effective, wafer-level packaging solution is needed to transition from research devices operated in controlled lab environments, to viable products, ready for commercialization.

Wafer-level vacuum packaging is a crucial process for encapsulating emerging devices, such as photonic micro-electro-mechanical systems (MEMS) and opto-mechanics, in a vacuum environment. In the traditional MEMS field, it is an established technology that enables reliability, functionality, and protection from contamination for many commercial MEMS devices such as inertial sensors, resonators, and infrared detectors [5]. Packaging processes on wafer-level offer cost advantages for high-volume MEMS production compared to chip-level packaging [5,6]. For a successful integration

Silicon Photonics XVI, edited by Graham T. Reed, Andrew P. Knights, Proc. of SPIE Vol. 11691, 116910E · © 2021 SPIE · CCC code: 0277-786X/21/$21 · doi: 10.1117/12.2582975

of such packaging solutions into commercial foundry platforms, there are stringent requirements that need to be met, such as very high packaging yield, long-term hermeticity, small footprints, and low process temperatures. Furthermore, the resulting device thickness is an important aspect to ensure compatibility with standard integration technologies like flip chip bonding. Thus, ultra-thin sealing caps for hermetic packaging have emerged as a promising approach [7-9]. Low device thickness and small packaging footprints enable miniaturization and cost reduction of the packaged device [8,9]. If the height of the sealing caps is smaller than that of the solder bumps in a flip chip bonding process, it is possible to vertically stack photonic chips on interposers without through silicon vias (TSVs) which enables high-density 3D integration of multiple modules [10].

In this paper, we demonstrate wafer-level vacuum packaging using thin sealing caps on Si photonic foundry wafers, supplied by the standard iSiPP50G Si photonics platform of IMEC, Belgium [11]. Our packaging method is fully compatible with the photonics platform and does not require any modification to the standard foundry process. The photonic MEMS devices are sealed by using thin Si caps (30 µm) which are prefabricated on a 100 mm-diameter silicon-on-insulator (SOI) wafer. The SOI wafer with the sealing caps is bonded by Au-Al thermo-compression bonding at a low temperature of 250 °C and the hermeticity is ensured by small footprint sealing rings of 20 µm width [12]. We experimentally verified the feasibility of the proposed vacuum sealing method and the compatibility with photonic devices on the iSiPP50G Si photonics foundry wafer. The presence of vacuum inside the sealed packages was confirmed. Finally, the integrity of the encapsulated Si photonic MEMS devices was validated to verify that the sealing method does not compromise the functionality of the packaged devices.

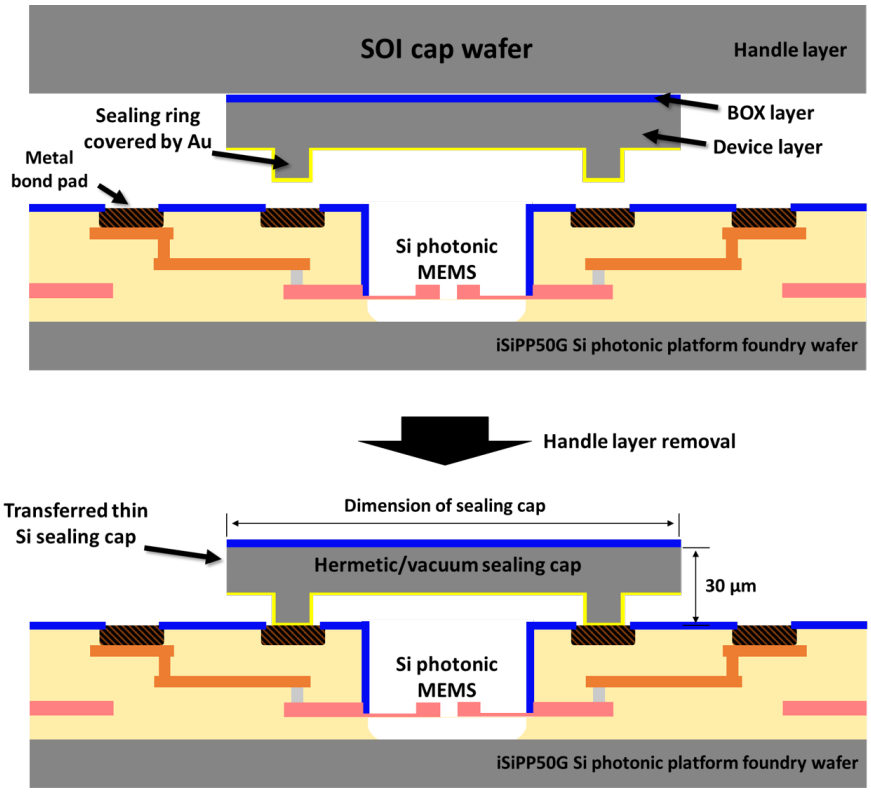

Figure 1. Schematic drawing of the demonstrated hermetic/vacuum packaging by transfer bonding of thin Si sealing cap.

2. VACUUM PACKAGING DESIGN/CONCEPT

2.1 Transfer Bonding of Thin Sealing Caps

Our wafer-level vacuum packaging approach by transfer bonding of thin Si sealing caps is illustrated in Figure 1. The thin sealing caps are patterned and fabricated in the device layer of an SOI wafer. The sealing caps consist of a flat Si lid section with a protruding sealing ring, covered by a thin gold (Au) layer, which is located along the perimeters of the

caps. Corresponding aluminum (Al) rings are designed in the bond pad layer of the iSiPP50G Si photonic device wafer to enclose each photonic MEMS device. These Al rings are defined in the standard bond pad material and can thus be fabricated within the standard iSiPP50G foundry platform process. The SOI cap wafer, containing many sealing caps, is aligned to the photonics foundry wafer and subsequently bonded inside a vacuum chamber to seal a vacuum inside the cavity. Next, the handle layer of the SOI cap wafer is removed, leaving only the individual thin sealing caps on top of all the photonic devices. The narrow sealing ring is designed to have a small sealing footprint and induce plastic deformation at the Au-Al interface due to high local pressure during the thermo-compression bonding process. Additionally, the induced plastic deformation makes the transfer bonding process relatively insensitive to the roughness of the Au and Al contact surfaces, which simplifies fabrication and greatly improves reliability.

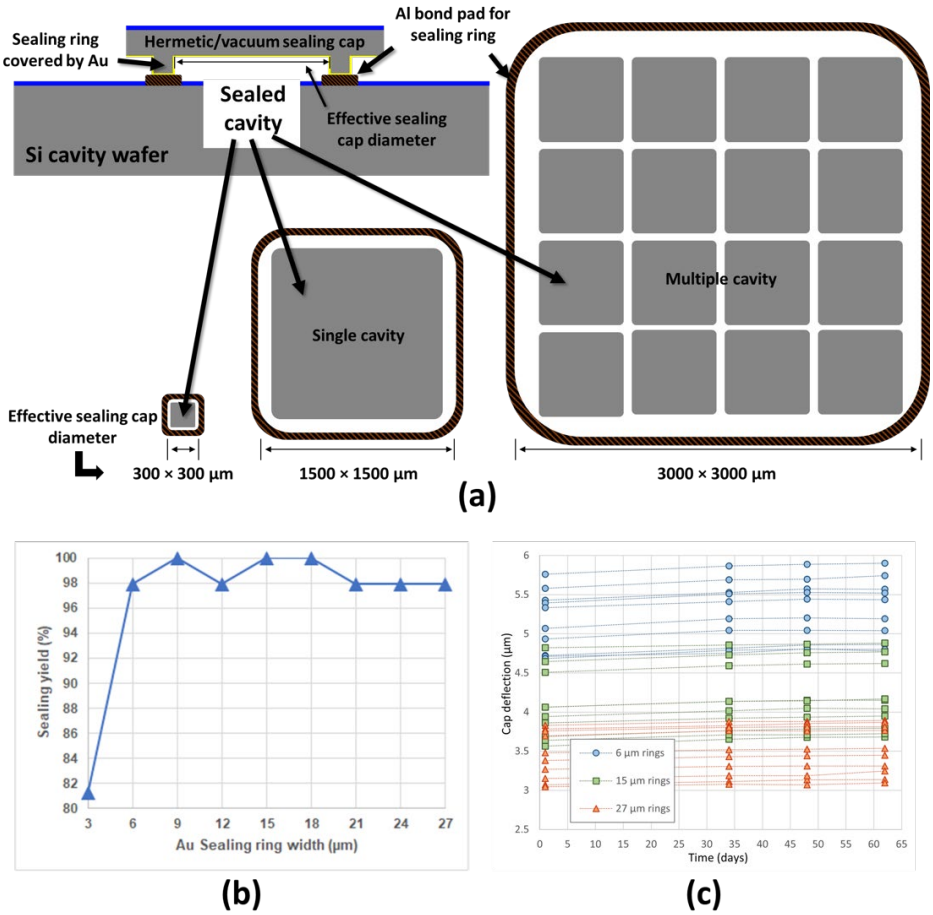

Figure 2. (a) Schematic drawing of demonstrated wafer-level hermetic packaging on Si cavity wafer with different dimensions of cavities. (b) Sealing yield of sealing caps with different ring widths. (c) Si sealing cap deflection over 62 days with different ring widths.

2.2 Sealing ring and cap design

Before demonstrating the wafer-level hermetic/vacuum packaging approach on the standard foundry wafer, we investigated the influence of the Au coated sealing ring width and cap dimension on the resulting sealing yield. Different sealing ring width from 3 µm to 27 µm were investigated. At the same time, three different dimensions of cavities were included on the wafer to verify our packaging method, as shown in Figure 2(a). Due to the gas pressure difference between the inside of the package and the outside atmospheric pressure, the thin sealing caps deflected toward the inside of the cavity. The caps with dimensions of 300 × 300 µm^2 and 1500 × 1500 µm^2 each encapsulated and sealed a single cavity. The caps with dimensions of 3000 × 3000 µm^2 were designed such that each cap enclosed multiple cavities/devices, which reduced the sealing footprint and was used to verify a method of encapsulating multiple devices

by a single sealing cap. For evaluating the wafer-scale sealing yield, a total of 432 Si sealing caps were fabricated on a 100 mm diameter wafer, including 48 cavities for each of the nine different Si sealing ring widths. After transfer bonding and handle layer removal of the SOI cap wafer, the thin Si sealing caps with different sealing ring widths had a bonding yield of between 82% and 100%. As shown in Figure 2(b), all sealing ring widths except for the 3 µm version exhibited an excellent yield of above 98%. The relatively low sealing yield of the 3 µm-wide sealing rings is because these sealing rings do not provide sufficient bond strength as a result of the small bonding area. To evaluate the hermeticity of the sealing caps with different ring widths, we measured the cap deflections by white-light interferometry (*Wyko NT9300, Veeco Inc., US*) over 62 days, as shown in in Figure 2(c). No significant change in cap deflection could be observed, which indicates maintained presence of vacuum inside the sealed cavities [12,13].

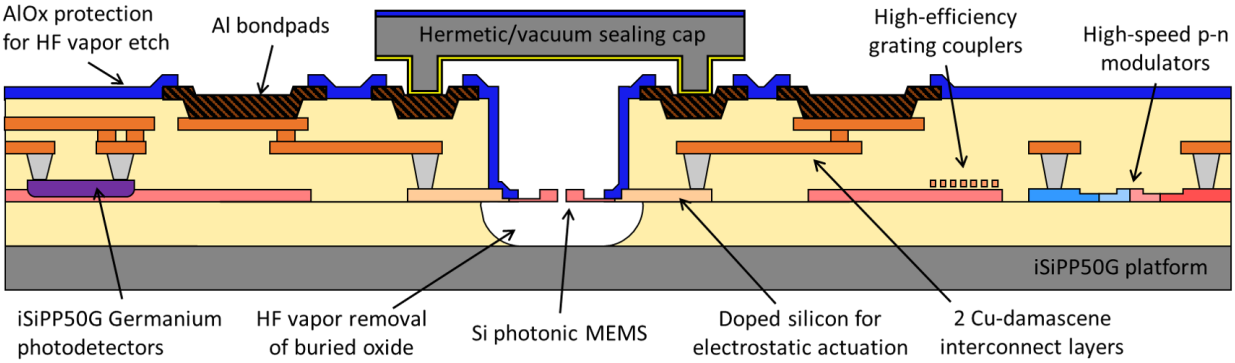

Figure 3. Cross section of photonic MEMS on the iSiPP50G foundry platform.

3. VACUUM PACKAGING OF SI PHOTONIC FOUNDRY WAFER

3.1 iSiPP50G Si photonic foundry wafer

The wafer-level hermetic/vacuum packaging was demonstrated on a photonic foundry wafer that was fabricated on the standard iSiPP50G platform by IMEC, Belgium. As shown in Figure 3, the iSiPP50G platform is based on an SOI wafer with a 220 nm-thick Si device layer on a 2 µm-thick buried oxide. In this platform, the passive structures are fabricated using three different levels of etching and additional poly-Si overlay is added to fabricate high-efficiency grating couplers. Several implantation processes are employed to create p-n modulators and efficient high-speed photodetectors. The electrical connections are fabricated by a two-level copper-damascene process and finished by Al metal bond pads. After the Si photonic wafers were through the iSiPP50G foundry process, the photonic MEMS devices were completed by local removal of the oxide cladding to allow mechanical motion. In a final step, a hydrofluoric acid vapour etching (vHF) process was used to selectively remove the oxide underneath the MEMS devices [14]. The result is a state-of-the-art photonic integrated circuit that seamlessly combines conventional non-mechanical Si photonics with novel photonic MEMS.

3.2 Hermetic/vacuum packaging of iSiPP50G foundry wafer

To demonstrate the feasibility of the proposed wafer-level hermetic vacuum packaging as illustrated in Figure 1, the process was performed on a 4-inch iSiPP50G foundry wafer. A SOI sealing cap wafer containing 30 µm thick caps with different dimensions from 450 µm × 330 µm to 2812 µm × 2945 µm was designed to demonstrate sealing of single and multiple photonic devices in the same process step. Figure 4(a) shows examples of different photonic devices using different shapes and dimensions of the sealing caps. This flexibility to adapt the sealing cap shape to each type of device allows for a small packaging footprint and thus, increased integration density and reduced system costs. Further, the Al bond rings were designed to encapsulate only the photonic devices. As illustrated in a side-by-side comparison of an unsealed and a sealed cap in Figure 4(b) and (c), the metal bond pads and grating couplers are located outside the sealing area. Thus, the electrical and optical I/O connections remain easily accessible for easy on-chip testing and chip integration.

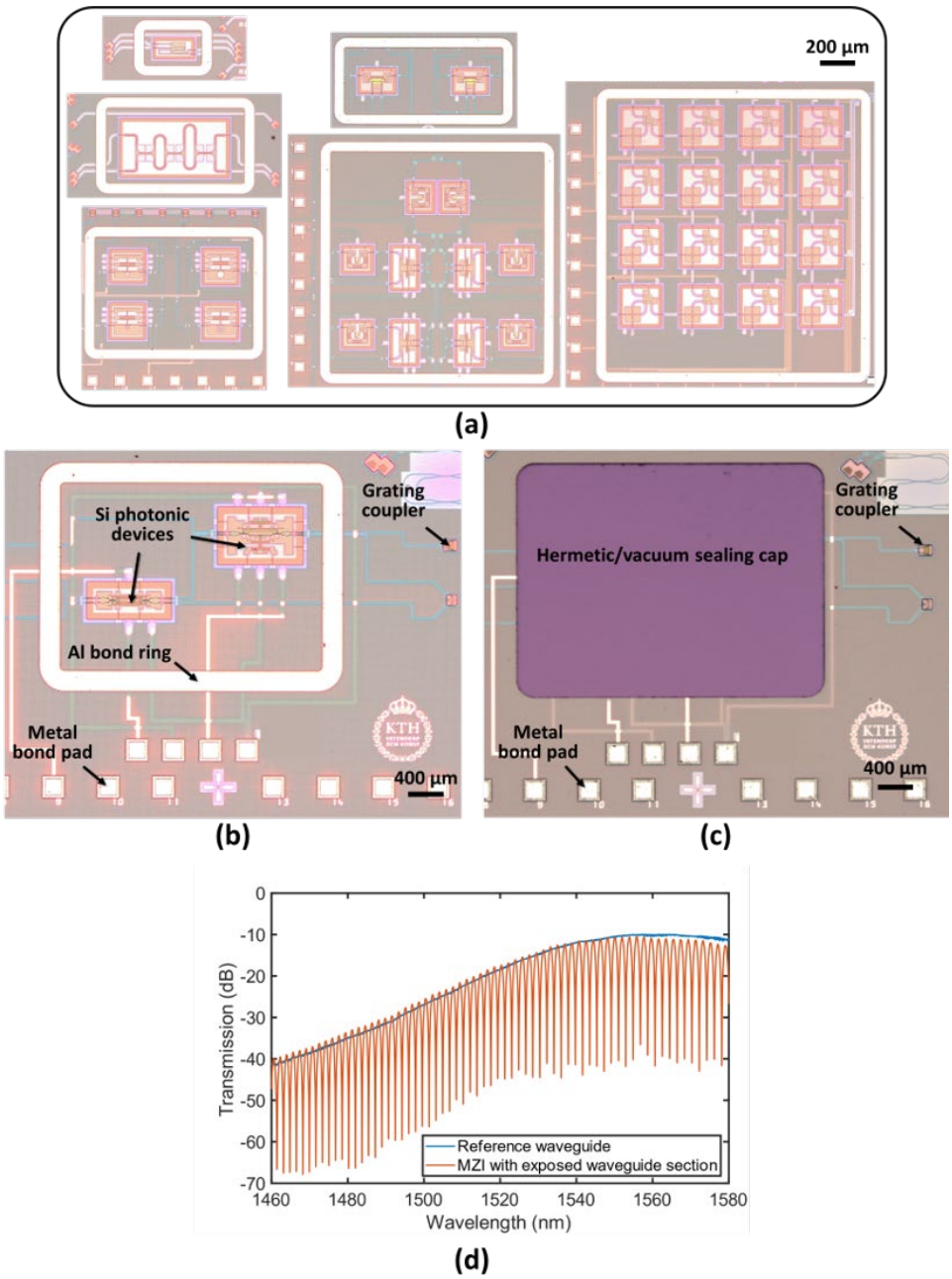

Figure 4. Different photonic devices and results of the wafer-level hermetic vacuum packaging. (a) Single and multiple photonic devices with different sealing ring dimensions. (b) Pre-defined bond rings for capping to enclose the photonic devices, designed in the bond pad layer of the Si photonic foundry process. (c) Example of thin cap sealing for exposed silicon photonic devices, adjacent to electrical (Al bond pads) and optical (grating coupler) standard interfaces. (d) Optical transmission from an integrated MZI underneath a sealed cap, with a suspended waveguide section. In blue, non-sealed reference waveguide.

The caps have a small and flexible footprint, increasing the integration density of sealed devices. However, optical losses are also crucial for photonic circuits, and the sealing should not limit circuit functionality. To verifies optical integrity, we measured the transmission through an integrated Mach–Zehnder interferometer (MZI) test circuit underneath a sealing cap, as shown in Figure 4(d). A straight grating to grating reference waveguide was also measured outside of the

cap, and we did not see any impact of the sealing on the maximum transmission. The result confirms that the wafer-level vacuum packaging approach does not damage waveguides underneath of the caps. Moreover, the tested MZI circuit included an 80 μm-long waveguide section that was suspended as part of the vHF post-processing steps. The presence of MZI interference fringes with large Extinction Ratio (~30 dB), shows that the exposed, suspended waveguide section was not noticeably affected by the sealing process either. A collapsed waveguide section would have introduced very high losses in one arm, the fringes would have disappeared, and the MZI would have displayed a total insertion loss of -6 dB with respect to the reference waveguide.

4. SUMMARY

In this paper we present a wafer-level hermetic/vacuum packaging approach for sealing photonic devices on wafers. Our method relies on thermo-compression bonding of an Au/Al interface at a low temperature of 250 °C which is compatible with standard IC processes and photonic foundry platforms. We demonstrated the sealing with 100 mm diameter wafers on two different types of wafer substrates. First, a dummy Si wafer with etched cavities, which we used to confirm the maintained presence of vacuum and sealing integrity over a duration of two months. Second, a silicon photonics wafer from IMEC's iSiPP50G Si photonic platform. The proposed wafer-level sealing did not have any noticeable impact on the standard electrical and optical interfaces, and we did not observe a drop in optical transmission for devices underneath the sealing caps. Moreover, we implemented photonic MEMS by suspending some waveguide sections with vHF prior to sealing, and the exposed, packaged devices did not collapse or show a performance drop. We believe that our approach for wafer-level hermetic packaging of silicon photonic wafers is a significant step towards commercialization of silicon photonics, optomechanics and photonic MEMS.

ACKNOWLEDGMENTS

This work has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.780283 (MORPHIC). Also, this project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.871740 (ZeroAMP). This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.825272 (ULISSES).

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