Time-encoding analog-to-digital converters: bridging the gap to advanced digital CMOS – Part 2: architectures and circuits

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I. Introduction

The scaling of CMOS technology deep into the nanometer range has created challenges for the design of high-performance analog integrated circuits: they remain large in area and power consumption in spite of the process scaling. Analog circuits based on time encoding [1], [2], where the signal information is encoded in the waveform transitions instead of its amplitude, have been developed to overcome these issues. While Part 1 of this overview article [3] has presented the basic principles of time encoding, this Part 2 follow-up article will describe and compare the main time-encoding architectures for analog-to-digital converters and will discuss the corresponding design challenges of the circuit blocks. Focus will be on structures that avoid as much as possible the use of traditional analog blocks like opamps or comparators, but instead use digital circuitry, ring oscillators, flipflops, counters, etc. The overview of the state of the art will show that these circuits can achieve excellent performances. The obvious benefit of this highly digital approach to realizing analog functionality is that the resulting circuits are small in area and more compatible with the CMOS process scaling. It also allows easy integration of these analog functions in Systems on Chip, operating at "digital" supply voltages as low as 1 volt and below. Large part of the design process can also be embedded in a standard digital synthesis flow.

In what follows, we will describe the current state of the art, the main architectures, their achievements and the corresponding circuit design challenges in VCO-based time-encoding analog-to-digital converters, explaining how to design efficient high-performance analog circuits in an advanced digital CMOS technology. In the past, VCOs and certainly ring oscillators had a bad reputation with regard to important performance characteristics such as noise and distortion. However, as will be explained, these problems can be addressed using suitable architectures and circuit design techniques. Firstly, the typical VCO nonlinearity can be tackled using proper feedforward and feedback architectures. Secondly, the problem of poor phase noise and jitter performance can be overcome by applying suitable sizing and circuit techniques such as chopping. Thirdly, the assumed poor robustness due to temperature and power supply variations (power-supply rejection), drift and aging can be overcome with techniques from as simple as using a pseudo-differential configuration up to as complex as setting up a complete closed-loop circuit. Thanks to these advancements that overcome the negative properties of the circuit blocks such as the VCOs, the resulting systems can be very compact while achieving excellent performance. Additionally, similar to conventional continuous-time Delta-Sigma modulators, VCO-based ADCs exhibit an intrinsic anti-aliasing filtering property. Combined with their very high sensitivity [3], [4], this allows to eliminate other traditional analog blocks such as pre-amplifiers and anti-aliasing filters. We will conclude with presenting the current state of the art in VCO-based analog-to-digital converters as published in literature. Together, both overview papers demonstrate how time-encoding circuits can overcome the struggles of designing high-performance analog circuits in advanced digital CMOS technologies, fully taking advantage rather than suffering from process scaling, hence bridging the analog gap to advanced nanometer CMOS.

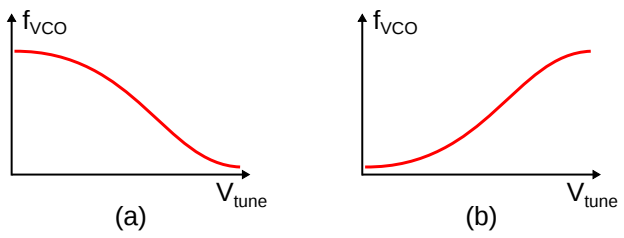

Fig. 1: Typical shape of the tuning curve of a ring-oscillator VCO, showing large nonlinearity: (a) curve corresponding to a bottom driven VCO, and (b) curve corresponding to a top driven VCO.

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II. Architectures for improved linearity

A notorious issue in ring-oscillator VCOs is their highly nonlinear tuning response. For virtually every type of VCO tuning, a tuning curve similar to Fig. 1 (whether bottom or top driven) is obtained, which is catastrophically nonlinear. A standard technique to improve this is the use of a pseudo-differential set-up (see discussion in Part 1 [3]). However, even then the large-signal linearity is still far from acceptable for most applications. An obvious solution for this is to greatly restrict the input range of the VCO, i.e. use the VCO in the small-signal regime. This strategy can often directly be followed in sensor applications, where the input signals are typically small; since the bandwidth is typically very low as well, the loss in dynamic range due to the limited input range can easily be compensated by a large oversampling ratio. However, for larger bandwidths, this straightforward approach is less obvious and more sophisticated architectural solutions come into play. We will now discuss the most important approaches: 1) the use of overall feedback architectures, 2) the use of input feedforward architectures, and 3) the use of calibration.

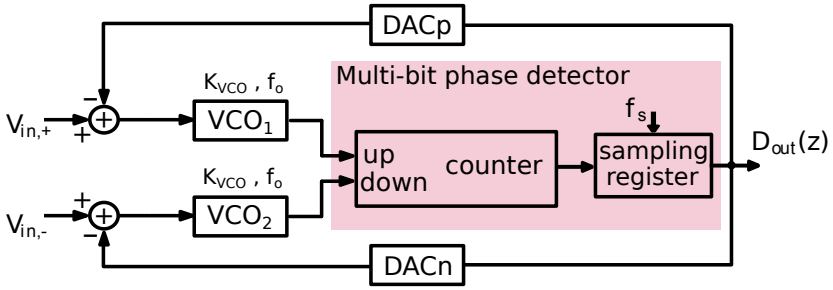

Fig. 2: Simplified diagram of a large family of closed-loop VCO-based ADC architectures.

A. Closed-loop VCO-based architectures

The basic architecture of a wide family of closed-loop VCO-based ADC structures [5]–[9] is shown in Fig. 2. The structure consists of two (nominally matched) VCOs that are in a differential feedback loop. The VCOs are driven by the difference between the (differential) input signal and the converted digital output fed back. The outputs of the two VCOs drive a phase detector. The observed phase difference steers the loop towards phase equilibrium. Many possibilities exist for the implementation of the phase detector, ranging from structures such as used in PLLs [6], [9] to counter-based structures [7], [10], as depicted in Fig. 2. The phase detector shown in the figure uses only 1 VCO output phase, but it is also possible to use multiple VCO output phases for improved performance [3]. The underlying mechanism of this architecture can readily be understood by reasoning on the established phase-domain model of a VCO as an integrator (see Part 1 [3]). In this way the depicted architecture of Fig. 2 operates as a control loop with a large loop gain, resulting in a nullator operation at the VCO input nodes, hence greatly reducing the effect of the VCOs' nonlinearity. Another important aspect of this architecture is that the quantization noise created by the (multi-bit) phase detector in combination with the sampler is injected in the loop *after* the integration performed by the VCOs. Hence, this quantization noise contribution is 1st-order noise shaped similarly as in the open-loop architectures.

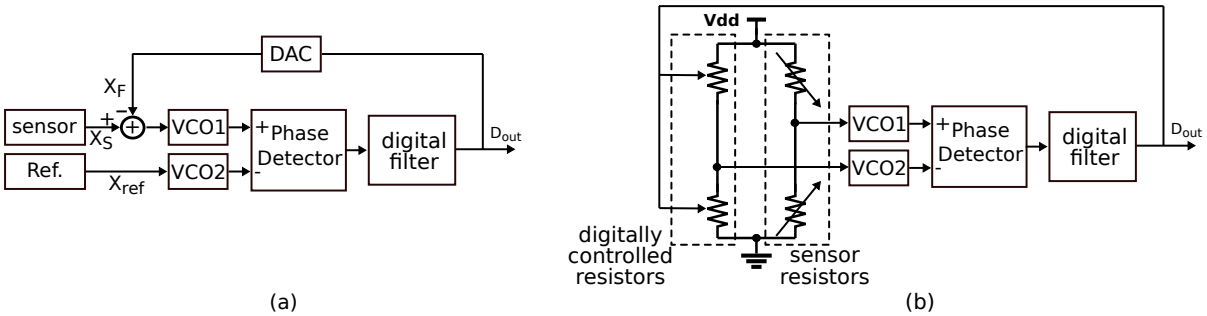

Fig. 3: Example closed-loop VCO-based ADC architectures for sensor readout: (a) the sensor, feedback and reference signals X (e.g. capacitor) directly tune the oscillators, and (b) the differential resistive sensors in the Wheatstone bridge are embedded within the feedback loop.

Designs based on the closed-loop architecture of Fig. 2 have been demonstrated for bandwidths ranging from some hundred Hz [11] up to some MHz [6]. Interesting is to apply the structure to the direct digital readout of sensors, where the low signal bandwidth allows to use large oversampling ratios, therefore achieving high resolutions. Two typical examples are shown in

Fig. 3. The structure in Fig. 3(a) shows how the analog sensor signal driving one of the VCOs can be read out directly as a digitized output [12]. When the other VCO's input is a fixed reference, then both VCOs are kept around the same operating point, improving the linearity. Fig. 3(b) illustrates this for the specific case of a differential resistive sensor configured in a Wheatstone bridge at the input, with the DAC feeding back to digitally controllable resistors in the bridge [13]. Compared to the basic structure of Fig. 2, an important modification in Fig. 3 is the incorporation of an additional digital filter in the loop, which allows the feedback DAC and the phase detector to operate at a different rate. Note that in many cases it is possible to shift the sensor inside the loop, such that the nonlinearity of the sensor itself is also suppressed by the loop gain of the feedback loop. Examples are shifting a capacitive sensor X directly into (a stage of) the controlled oscillator in Fig. 3(a) [12], or closing the loop around the Wheatstone bridge with resistive sensors in Fig. 3(b) [13].

Drawbacks of the closed-loop structures are that they are not suited for really large signal bandwidths and that any nonidealities (nonlinearity and noise) of the feedback DAC are injected directly into the output signal. In practice, some kind of linearization such as dynamic element matching may be needed here. Fortunately, several of the VCO phase readout schemes incorporate implicit DWA-type dynamic element matching [14], [15] or circuit-level averaging [16].

B. Input feedforward architectures

An alternative for closed-loop operation is the input feedforward architecture (also known as the coarse/fine structure) [17]–[19], [20]. One possible implementation is shown in Fig. 4, where both quantizers are implemented as VCO ADCs [19]. Here, the input signal is first quantized by a coarse auxiliary input quantizer to generate a coarse result that through a DAC is subtracted from the input signal. Hence a low-swing residue signal is obtained that drives the main VCO ADC operating as fine quantizer. The final output is obtained by combining the results of the coarse and fine quantizers. Surprisingly, if path 1 and path 2 are well matched, the performance of the coarse quantizer is very non-critical, while the fine quantizer is driven with only a small input swing. Like in the closed-loop structures, the nonidealities of the DAC couple directly into the overall output. The embodiment of Fig. 4 has the advantage that the coarse VCO quantizer output is encoded with implicit DWA dynamic element matching [14], [15], thus also linearizing the coarse DAC.

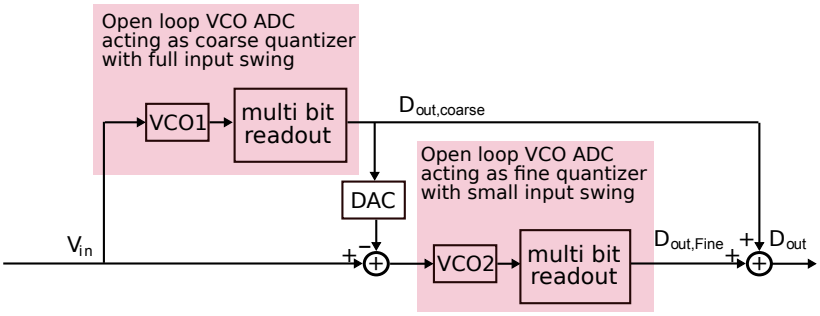

Fig. 4: Input feedforward ADC architecture (also known as coarse/fine structure): the first coarse quantizer makes a rough digital estimate, such that the main fine quantizer operates only on a very restricted input range. Both quantizers are VCO-based in this example structure [19].

C. VCO calibration

A final way to tackle the VCO nonlinearity is to apply some calibration technique. A straightforward approach for this is to apply the calibration in the digital domain after the VCO-based ADC [21]–[25]. The principle is shown in Fig. 5 and consists of inverting the VCO nonlinearity by operating on the digital output signal of the core VCO-based ADC. There are two challenges with this technique. Firstly, an accurate estimation of the VCO nonlinearity must be extracted to be available in the digital domain. Most currently published designs extract this nonlinearity curve in a lab environment [10], [21], although also a few designs with continuous adaptive calibration have been published [22]–[24]. Secondly, since the VCO output signal also contains shaped quantization noise, applying the digital nonlinearity correction to the VCO output may make this noise partially fold into the baseband. A potential solution for this problem consists of first removing a large amount of the quantization noise before doing the nonlinearity correction [10].

III. Architectures for improved noise suppression

A. Architectures for reducing quantization noise

The architectures described till now all exhibit first-order quantization noise shaping. In many cases, the oversampling ratio of VCO-based ADCs is sufficiently large such that this is sufficient. Also, polyphase sampling techniques have been attempted to increase the oversampling [25]. However, when going for a higher bandwidth or for a higher resolution of say 16 bits or

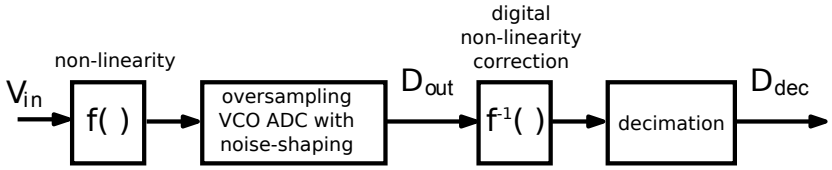

Fig. 5: Core principle of digital calibration of a VCO-based ADC.

above, a higher order of noise shaping is beneficial in order to exploit the advantages of oversampling more efficiently. To do this, additional VCOs can be cascaded and a feedback loop built around the cascade [10], [26]–[29]. The core mechanism here is to exploit the VCO as an integrating block. Fig. 6 shows a second-order noise shaping example where the first VCO is outside the loop. This set-up has the disadvantage that the nonlinearity of the first VCO directly couples to the output. To solve this, one of the techniques described above (input feedforward or calibration) can be added to the structure. Also higher-order examples [10] and structures where the VCO is inside the loop [8], [28], [29] have been presented. Although promising, currently, the bandwidth of most published high-order designs does not exceed that of 1st-order designs with similar resolution, such as [22], [23], [25].

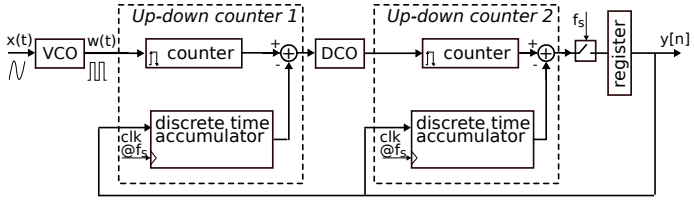

Fig. 6: Block diagram of a VCO-based ADC with second-order quantization noise shaping from [27]. Note that the first VCO is outside the feedback loop.

Also, the idea to increase the order of quantization noise shaping of VCO-based ADCs by cascading multiple units in a MASH structure has been around for some time [30]–[33]. Successful silicon implementations have been presented recently, such as a 1-1 cascade with second-order quantization noise shaping (2 MHz bandwidth, 80dB SNDR) in [34]. On the other side of the spectrum, for sensing applications with low bandwidth but high resolution, [35] has presented a 1-1 sturdy-MASH architecture with the second loop and its integrator built entirely in digital circuitry, achieving second-order noise shaping and 16.1 bits of resolution.

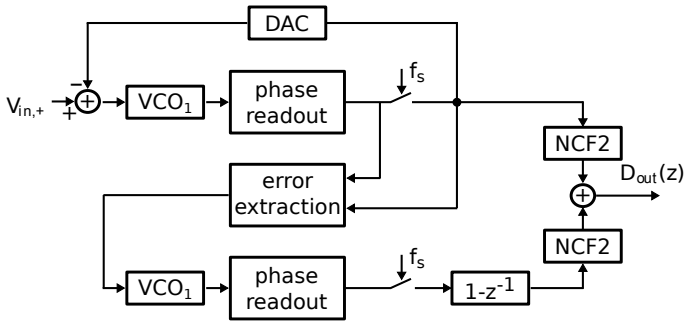

Fig. 7: 1-1 MASH VCO-based ADC with second-order noise shaping [taken from [34]].

Combining multiple VCO ADCs on the same chip and then averaging the conversion result is also a potential option. This concept is known as a stochastic VCO ADC [36]. In principle this technique does not increase the power, because the power increase due to the multiple VCOs in parallel is compensated by the reduction in thermal noise (after averaging), similar as with impedance scaling for a single ADC channel. In addition to the averaging of the circuit noise, also the quantization noise is averaged. This is thanks to the fact that in a properly designed stochastic VCO ADC, the quantization noise contributions of each ADC channel are uncorrelated. In this way, in principle, this stochastic concept is very simple, power-efficient and digital friendly: all the designer needs to do is to design a simple low-power VCO ADC channel and then put as many channels in parallel as needed to achieve the desired accuracy [36], [37]. In practice, however, the currently published designs are still far from the state of the art in terms of performance.

B. Time-domain chopping

Circuit noise is an important limitation in any analog circuit, including VCO-based ADCs. Altough many designers think about VCO noise in terms of oscillation phase noise, we advocate to reason about this in terms of input-referred circuit noise (see also Part 1 [3]), similar to amplifier noise. The white noise translates in a pretty conventional noise versus power trade-off. The $1/f$ noise in traditional amplifiers is tackled in two ways: by sizing the noise-dominant devices with large area and/or by deploying chopping. In a similar way, suitable sizing strategies have been deployed to tackle $1/f$ noise in VCO-based ADCs by properly sizing the inverting-stage transistors (e.g. [35], [38]) or by increasing the number of VCO taps (e.g. [27], [39], [40]), as far as the targeted bandwidth allows. To achieve higher resolutions, time-based chopping techniques have been introduced and demonstrated successfully, in particular for sensor readout where the bandwidth is relatively low, making it difficult to push the $1/f$ noise sufficiently low by sizing only [11]. Two examples are shown in Fig. 8: in (a) both the VCOs and the phase detector are embedded inside the choppers [41], whereas in (b) only the VCOs are chopped [13]. The latter BBPLL-based design combines chopping with VCO tuning to largely remove the errors introduced by VCO mismatches and drift, resulting in ppm-level gain and offset drift due to power-supply and temperature variations across the entire -40°C to +175°C range. This high drift resilience can be established with only a single-temperature calibration scheme and without requiring external accurate references or components [13]. An alternative to chopping the actual VCOs is to perform the chopping in the VCO drivers in front of the actual VCO-based ADC [5], [42].

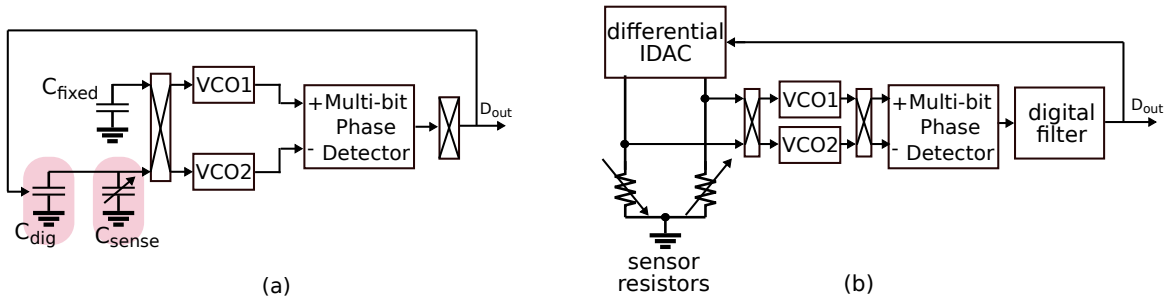

Fig. 8: Introducing time-domain chopping in a closed-loop VCO-based ADC structure with sensor in the loop: (a) the combination of VCOs and phase detector is chopped [41], and (b) only the VCOs are chopped [13].

C. Hybrid architectures: best of both worlds?

Many researchers have also used VCO ADCs as an auxiliary block or in hybrid combinations with other types of ADCs. For example, the work that caused the revived interest in VCO-based A/D conversion [15]) used the VCO ADC as embedded noise-shaping quantizer in an otherwise conventional $\Delta\Sigma$ modulation ADC. This and similar configurations have been widely researched since (e.g. [17], [43], [44], etc.), but they still use several conventional analog blocks (opamps, etc.) and therefore don't use the full scaling potential of digital CMOS. A more promising combination in this respect is the combination of a SAR ADC and a VCO ADC [45]–[47]. As shown in Fig. 9, the VCO-based ADC is used here as noise-shaping converter for the residue signal that is available at the comparator input after a SAR A/D conversion.

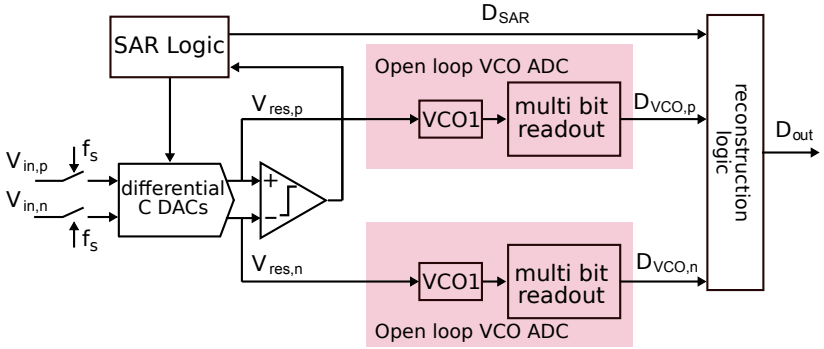

Fig. 9: SAR ADC cascaded with a VCO-based ADC (figure similar to [47]).

IV. Circuit design aspects for VCO-based analog-to-digital converters

A. Single-ended inverter-based ring oscillators

A ring oscillator consisting of basic single-ended CMOS inverters is the most straightforward digital-friendly way to build a time-encoding VCO-based ADC. A particularly important circuit aspect is how to drive the ring VCO. A first important

decision is whether the VCO will be driven at the *top* through its V_{dd} terminal (as shown in Fig. 10), or alternatively at the *bottom* through its V_{ss} control terminal (as shown in Fig. 11). This decision might be set by considerations on the input common-mode level, and both solutions also lead to different specifications on the power supply scheme.

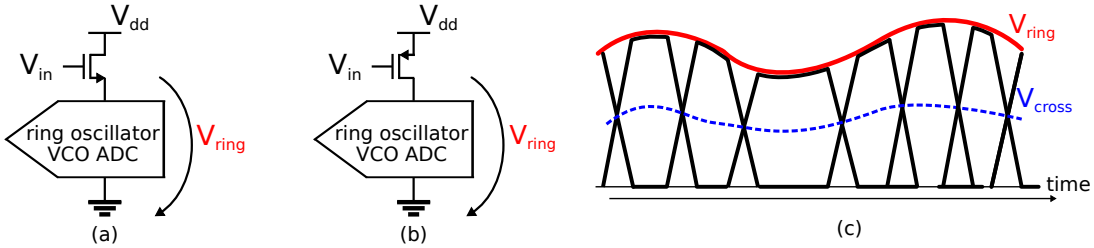

Fig. 10: Driving a ring-oscillator VCO from the 'top': (a) 'voltage' mode drive through a source follower, and (b) 'current' mode drive through a transconductor, and (c) the corresponding waveform of the VCO output signal, which exhibits an amplitude modulation due to the modulation of the voltage across the ring.

A second important decision is whether to drive the ring-oscillator VCO through a source follower transistor ('voltage' mode drive, shown in Fig. 10(a)) or through a transconductor transistor ('current' mode drive), shown in Fig. 10(b)). Clearly, for both cases the input-referred noise of the input transistor directly adds to the overall noise budget and the transistor should be sized accordingly. For both circuits the input impedance is capacitive, but the source-follower approach has a much smaller effective input capacitance due to the bootstrapping effect on the gate-source capacitance. Hence, the current drive requirements on the preceding circuits are lower for the source-follower approach. Using current drive, the transconductor approach on the other hand allows easier setting of the oscillation frequency and typically has a lower voltage swing, leaving more voltage headroom to optimally size the ring oscillator. For low-frequency circuits an additional consideration is the $1/f$ noise, which typically is lower for pMOS than nMOS transistors, although chopping can greatly relieve this aspect, as described above.

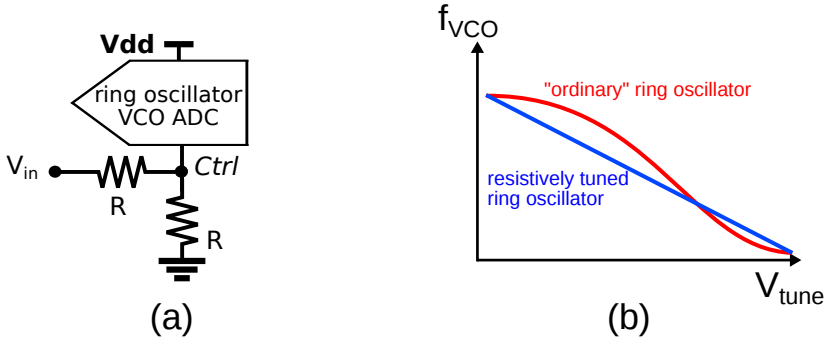

Fig. 11: (a) Resistively driving the ring VCO-based ADC [48] improves (b) the linearity of the VCO tuning curve.

In their basic form, both the source follower as well as the transconductor drive circuits of Fig. 10 are notoriously nonlinear. An improvement in this respect is the resistive drive circuit of Fig. 11(a) (the figure shows the bottom drive version), originally proposed in [48]. Various implementations [10], [48]–[50] have demonstrated up to 11 bits of linearity in a pseudo-differential VCO-based ADC.

Whichever drive circuit is used to tune the overall VCO, there will always be a significant modulation of the voltage V_{ring} across the ring oscillator. As illustrated in Fig. 10(c), this leads to an amplitude modulation of the VCO output waveform, which in turn leads to a signal-dependent variation of the ideal crossing point. To tackle these amplitude modulation effects, several published designs use a level shifter at every VCO output phase, which however can take a significant portion of the ADC's power budget [10].

B. Other oscillator circuits

An important variant from the ring oscillator with simple inverters is the one using differential delay elements (see Fig. 12(a) [51]. Advantages are that the number of delay elements can now be even, and that the phase readout can be done with a differential sense amplifier combining an excellent sensitivity with a very low power consumption [52]. This makes the readout also much less sensitive to the modulation in the crossing point of Fig. 10(c), greatly relaxes metastability problems and eliminates the need for power-consuming level shifters at the phase readout. Finally, with differential delay elements the current in the supply lines has significantly smaller spikes, also reducing the power supply noise.

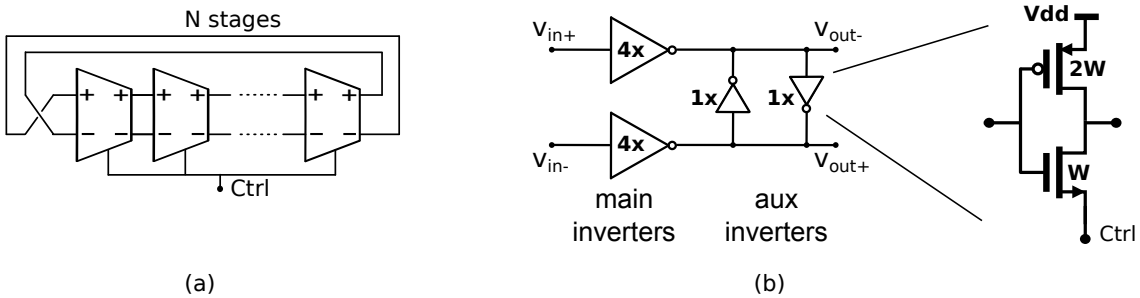

Fig. 12: (a) Ring-oscillator VCO with differential delay elements, and (b) their implementation based on inverters.

The typical circuit for such a differential delay element is shown in Fig. 12(b) and consists of two main inverters that form the main signal path, and two (small) auxiliary inverters that create a balancing mechanism, ensuring that the oscillator can not get locked in a latched state. Improved variants with lower power use a modified feedforward coupling scheme for the auxiliary inverters [49], [53]–[55]. Note that this is still a nearly-digital circuit.

Other applications may benefit from using other (be it less digital) types of oscillators or ring stages. For example, [27] uses a relaxation oscillator as second stage to avoid a power-consuming level shifter, while [13] uses a 6-stage ring oscillator with coupled sawtooth stages for higher linearity in its resistive sensor readout.

ref.	[55]	[20]	[25]	[56]	[19]	[10]	[8]	[34]	[38]	[9]
Year	2020	2020	2019	2020	2015	2017	2020	2020	2020	2020
NTF order	0	0+1	1	1	0+1	**3**	**2**	**1+1**	1	1
analog Correction†	no	FF	no	no	FF	FB	FB	FB	no	FB
Digital calibration	yes	yes	yes	yes	**no**	yes	**no**	**no**	**no**	**no**
Process [nm]	28	16	65	28	40	65	40	65	130	40
Area [mm^2]	0.023	0.34	0.244	0.023	0.017	0.01	0.086	0.26	0.04	0.025
Vdd [V]	1.0	1/1.8	1.05	1.2	0.9	1.2	1.1	0.9	1.2/1.5	0.8
BW [MHz]	**2500**	**800**	**200**	40	40	10	5.2	2	0.02	0.01
SNDR [dB]	45.2	58	57	77.8	59.5	65.7	69.4	79.7	73.8	78.5
DR [dB]	50.3	60	60	79.5	62	71	72.3	82.7	97	79
Power [mW]	22.7	280	49.7	10.9	2.57	3.7	0.86	1.25	0.24	0.0047
FoM1 (SNDR) [dB]#	155.6	153	153	**171.4**	161.4	160	167.2	**171.7**	153	**172**
FoM2 (DR) [dB]*	160.7	155	156	**173.1**	163.9	165.3	**170.1**	**174.7**	**176.2**	**172.5**

† FF refers to the input FeedForward technique as explained in section II-B. FB refers to analog FeedBack.
# FoM1 = $SNDR + 10 * log10(BW/Power)$
* FoM2 = $DR + 10 * log10(BW/Power)$

TABLE I: A review of state-of-the-art VCO-only ADC circuits.

V. Bird's eye overview of the state of the art

There is a very wide variety in published VCO-based ADC designs, even when limiting to highly-digital designs that don't require analog blocks such as opamps. A bird's eye sampler of relevant published designs is given in Table I. Apart from their wide variety, an important observation to be made from this table is that all designs are very compact and occupy a very small silicon area. If we rank the designs based on bandwidth, then [55] is one extreme of the spectrum. It is a Nyquist-rate design without noise shaping nor oversampling, and with its sampling frequency of 5 GHz has the highest-bandwidth VCO published to date. A close second is [20] which is a true oversampling converter with an effective application bandwidth of 800 MHz and around 10 effective bits resolution. Also the design reported in [25] pushes the bandwidth far in the hundreds of MHz region. It is noteworthy that none of these ultra-high-speed designs use a global feedback loop, so their noise shaping is only 1st-order, but they all have digital calibration.

At the other side of the spectrum, there are the extremely efficient designs with audio (or near-audio) bandwidth of [38] and [9] achieving high Figure of Merit (FoM) numbers. In the near MHz range up to around 40 MHz, several efficient designs have been proposed. Here, a much wider variety of the techniques discussed above has been deployed successfully: some designs use analog techniques such as closed-loop operation [8], [9], [34] or input feedforward [19], whereas others use digital calibration to obtain adequate linearity [10]. Also higher-order noise shaping structures have successfully been demonstrated, like a 1+1 MASH structure in [34] or a third-order structure in [10].

Sensor applications are a category of their own: they have a low bandwidth and, when incorporating the sensor directly in the converter, typically also higher power, yet they avoid any buffer or preamplifier. Here are some recent VCO-based examples. [5] targets neuron readout, and notwithstanding the low FoM1 of 146 dB, it has an excellent sensitivity with a full-scale input of 8 mVpp. [35] presents a highly-digital 1-1 sturdy-MASH 2nd-order converter for resistive sensor bridge readout with up to 16.1 bits of resolution and a very good FoM1 of 163.5dB.

VI. Takeaway points

- Feedback is an important instrument in the analog designers' toolkit. Also in VCO-based ADCs, feedback techniques demonstrate their value in improving the linearity as well as the noise shaping.
- Yet, several published open-loop VCO-based ADC designs have comparable or even better performance than competing closed-loop designs, which is definitely the case for ultra-high-speed circuits.
- For such open-loop VCO-based ADC circuits, feedforward and digital calibration techniques are important enablers to boost the linearity performance.
- Oversampling, time-based chopping and sensor embedding are among the tricks to improve performance and power efficiency for sensing applications.
- While the core digital ring oscillator is well known, there have been lots of circuit innovations for VCO-based ADCs in recent years, improving the large-signal linearity and boosting the speed.

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