Time-encoding analog-to-digital converters: bridging the analog gap to advanced digital CMOS – Part 1: Basic principles

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This document is an author's draft version submitted for publication in IEEE Solid State Circuits Magazine,
The actual version was published as:

Georges Gielen, Luis Hernandez and Pieter Rombouts. "Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS-Part 1: Basic Principles." IEEE Solid-State Circuits Magazine 12.2 (2020): 47-55.

Time-encoding analog-to-digital converters: bridging the analog gap to advanced digital CMOS – Part 1: Basic principles

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I. Motivation For Time Encoding

The scaling of CMOS technology deep into the nanometer range has created challenges for the design of high-performance analog integrated circuits. The shrinking supply voltage and the presence of mismatch and noise restrain the dynamic range, causing analog circuits to be large in area and have a high power consumption in spite of the process scaling. Analog circuits based on time encoding [1], [2] and hybrid analog/digital signal processing [3] have been developed to overcome these issues. Realizing analog circuit functionality with highly digital circuits results in more scalable design solutions that can achieve excellent performance. This article reviews the basic principles of time encoding, in particular applied to analog-to-digital converters (ADCs) based on Voltage-Controlled Oscillators (VCOs), one of the most successful time-encoding techniques to date. Although VCO-based ADCs have been around for a long time [4], [5] they really received a significant boost in interest after Straayer and Perrotts highly cited 2008 paper [6]. Since then, many other advancements from different research groups worldwide have been published, in application domains such as sensor readout [7]–[10], telecom [11]–[13], wideband wireless [14]–[18], Internet of Things [19], automotive [20], [21], biomedical [22]–[24], to name a few. Note that the integrating properties of VCOs have also been used to implement continuous-time filters, time to digital converters and other analog signal processing blocks [25]–[27].

This overview article is divided in two parts. This first part will introduce the basic principles of time encoding with emphasis on VCO-based ADCs, and will compare them to traditional analog circuits. The follow-up article (part 2) will describe and compare different time-encoding circuit architectures for analog-to-digital converters, and will discuss the corresponding design challenges of the building blocks. Together, they will demonstrate how time-encoding circuits can overcome many of the problems encountered when designing high-performance analog circuits that fully take advantage of advanced digital CMOS technologies, rather than suffering from it, hence bridging the analog gap to advanced CMOS.

The main idea behind time encoding consists of representing an analog signal with a modulated square wave, where the signal information is encoded in the transitions instead of the instantaneous amplitude. Such a signal is easy to handle with digital circuits and is robust against noise and distortion. Representing the signal is then done through pulse modulations, known since long ago. Pulse Width Modulation (PWM) is one of the best examples, and used extensively in, for instance, power electronics. The typical block diagram of a time-encoding ADC is shown in Fig. 1. The analog input signal is applied to a pulse modulator that encodes the information in the pulse width, frequency or position of a signal (or set of signals) with two levels only. This two-level signal, which is still analog, is sampled afterwards at a sampling frequency f_s, typically much larger than the input signal bandwidth ABW. Differently from conventional ADCs, the sampler can now be a simple flip-flop, as the signal has only two values. From the sampled square wave, a decoder can reconstruct a multi-bit approximation of the analog input signal, which is typically done with a digital low-pass filter.

Although early time-encoding ADCs used PWM [1], [2], PWM may not be the best to replace analog circuits in an ADC. Indeed, PWM modulators require sawtooth generators or analog filters, still made of operational amplifiers and other highly linear circuits [28], [29]. VCO-based ADCs, on the other hand, can be implemented very efficiently with a ring oscillator,

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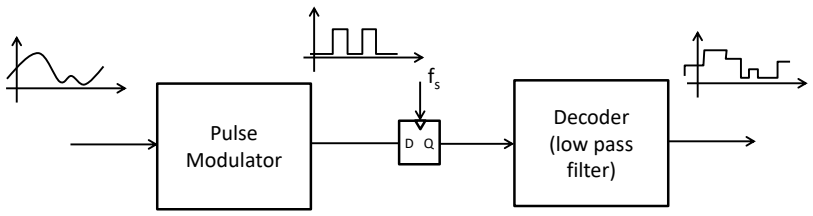

Fig. 1. Principle signal operations in a time-encoding ADC.

which is a simple digital circuit [30], [31]. To be precise, VCO-based ADCs need to be modeled using a different type of pulse modulation, called Pulse Frequency Modulation (PFM). PFM exhibits first-order noise shaping when sampled directly, contrary to other pulse modulations like PWM. The hardware simplicity and digital nature of ring oscillators and the noise-shaping properties of PFM are the reasons why VCO-based ADCs have gained large popularity. We will therefore concentrate most of our discussion on VCO-based ADCs.

II. VCO-based Analog-to-Digital Conversion: basic principles

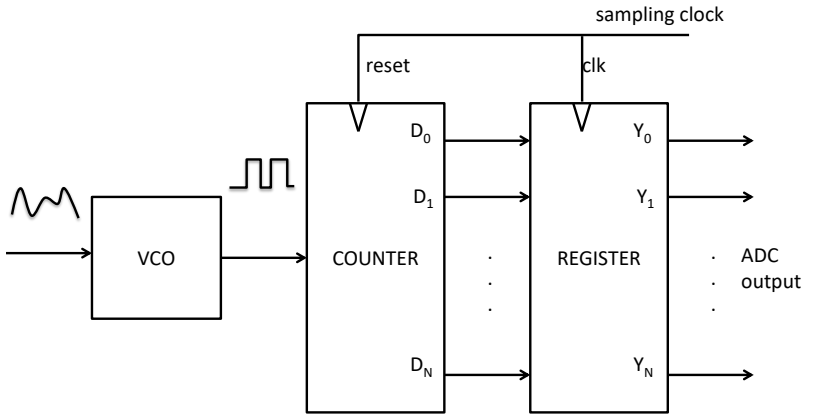

Fig. 2. Conceptual block diagram of an open-loop VCO-based ADC with counter.

So how do VCO-based ADCs digitize an analog signal? We will give an intuitive explanation of its functioning without detailed mathematics. Fig. 2 depicts the simplest VCO-based ADC architecture, which is also one of the most used. A slowly varying input signal modulates the frequency of an oscillator (the VCO). The pulses of the oscillator are then counted with a digital counter. Assuming a sampling period $T_s = 1/f_s$, the number of pulses accumulated in the counter is dumped into a register every T_s seconds and the counter is reset. The value in the register is therefore a measure of the VCO frequency and hence of the analog input signal during that sample. Clearly, the higher the oscillation frequency compared to the sampling frequency, the higher the resolution that can be achieved. This defines an important design relation in VCO-based ADCs: the resolution is proportional to the oscillator frequency relative to the sampling frequency (which corresponds to the number of quantization bits in a traditional amplitude-based ADC). In addition, if the input signal is oversampled beyond Nyquist, the sampling period T_s is shorter and apparently there would be fewer counts in the counter, resulting in a lower resolution. However, the reality is the opposite: the error introduced by quantizing the frequency of the oscillator into an integer number (the count) is first-order noise shaped. Just realize that the error obtained after and before sampling in the middle of a VCO oscillator cycle always adds to one cycle. This fact is illustrated in Fig. 3, which shows that the quantization error can be written as the first-order difference of a finite-power sequence. This first-order noise shaping in combination with oversampling and digital decimation after the counter improves the signal-to-quantization-noise ratio (SQNR) much more than increasing the oscillator frequency. The following approximate equation gives the maximum SQNR of a VCO-based ADC with analog

signal bandwidth ABW, sampling frequency f_s and oscillator rest frequency f_0 [32] :

$$SQNR[dB] \approx 6\ log_2\left(\frac{2f_0}{f_s}\right) - 5.17 + 9\ log_2\left(\frac{f_s}{2ABW}\right) \quad (1)$$

This equation shows that the SQNR improves with 6 dB every time the VCO frequency f_0 is doubled relative to the sampling frequency f_s, as the quantization resolution is increased by one bit. If the oversampling ratio is doubled in addition to the quantization resolution, i.e. the sampling frequency f_s is doubled together with the oscillator frequency f_0, the SQNR improvement is 9 dB. An additional consequence of this dependency is that, if the sampling frequency f_s is doubled for a fixed oscillator frequency f_0, the SQNR is improved by 3 dB. Therefore, the choice of the oscillator frequency and the sampling frequency allows to optimize the SQNR.

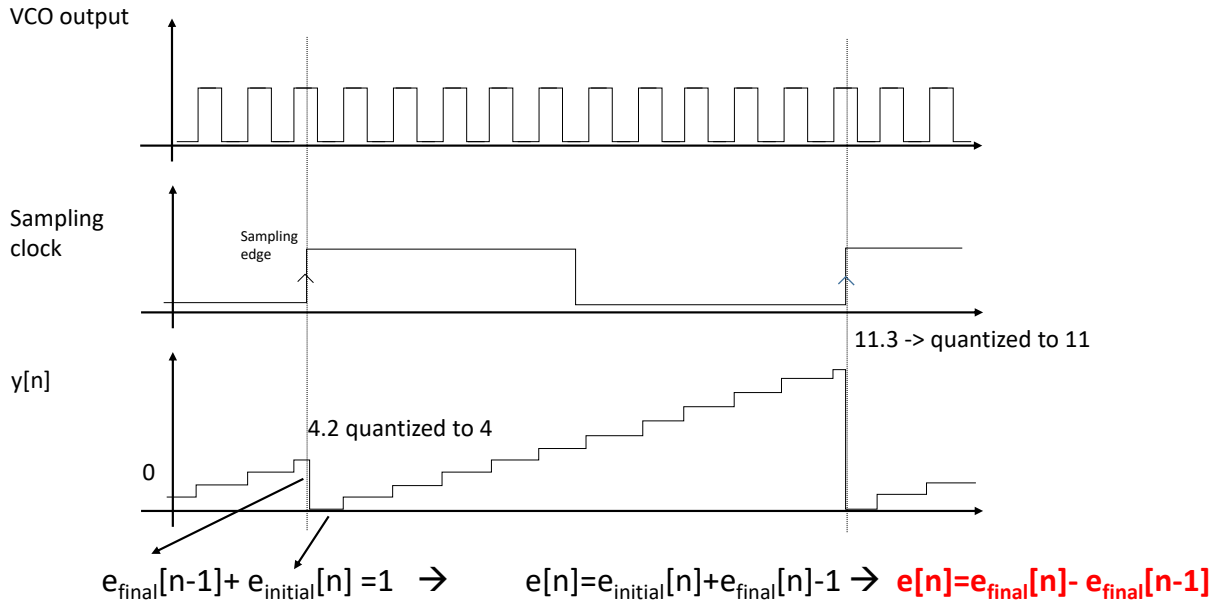

Fig. 3. Signal behavior in the VCO-based ADC of Fig. 2 with illustration of the noise shaping. The latter is due to the fact that the error e_{final} injected at the end of a counting cycle combined with the error e_{initial} at the beginning of the next counting cycle always add up to 1 LSB.

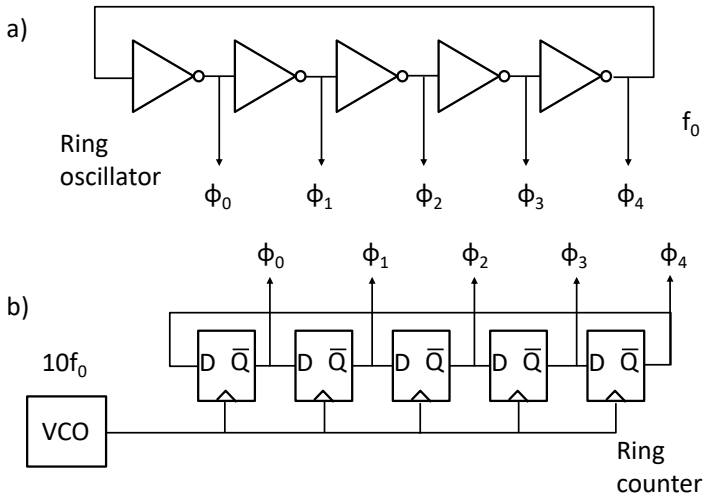

Fig. 4. Comparison of a ring oscillator with an oscillator and counter.

The typical VCO-based ADC circuit used in practice differs from the conceptual circuit of Fig. 2, although in the end it performs the same function. The difference lies in how the counter is implemented. Most VCO-based ADCs are implemented with a ring oscillator, which is a circuit that produces many similar square wave signals slightly shifted in time. Fig. 4(a) compares a 5-tap ring oscillator made of inverters and oscillating at a frequency f_0 with an equifunctional circuit in Fig. 4(b) where an oscillator oscillating at $10f_0$ is connected to a 5-tap ring counter: the outputs of both circuits are exactly the same signals. Therefore, the ring oscillator itself suffices to implement the whole system of Fig. 2 in a very compact and power-efficient way. Fortunately, as a practical implementation, the circuit of Fig. 5 allows a very easy way to measure the count increment without the need to reset the counter at every sampling clock cycle. Thanks to modulo arithmetic, this circuit encodes with minimal hardware the number of both rising and falling edges of the oscillator in a thermometric code at every clock instance. And here is the beauty of VCO-based ADCs: a many-bit, 1st-order noise-shaped sequence is obtained with only a few digital logic gates and no opamps !

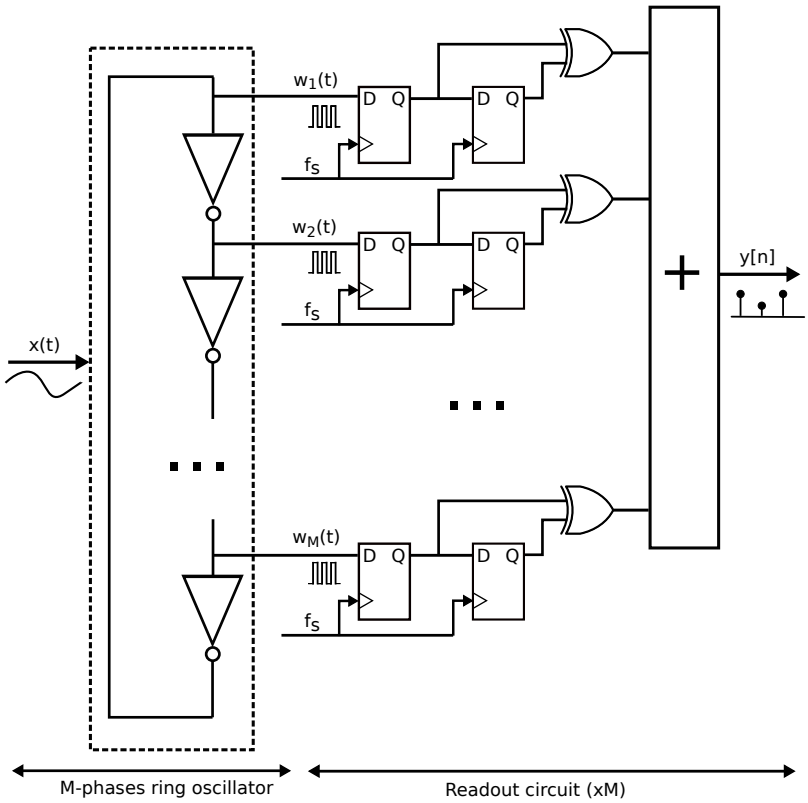

Fig. 5. Practical implementation of an open-loop ring oscillator VCO-based ADC with multi-phase readout.

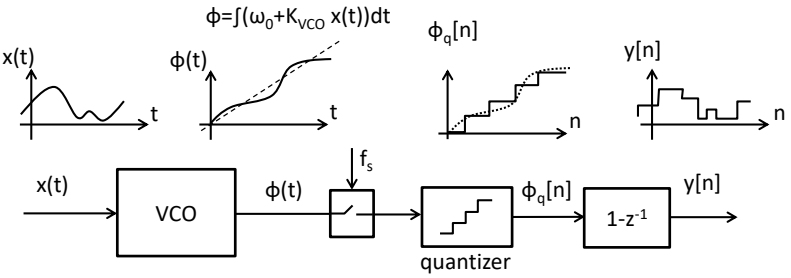

Fig. 6. Phase-referenced model of a VCO-based ADC.

Since early VCO-based ADC converters were seen as alternative implementations of Delta-Sigma modulators, the explanation given for the functioning of VCO-based ADCs can also be deducted from common Delta-Sigma modulator understanding. The

block diagram of Fig. 2 can be described in terms of the oscillator phase (see Fig. 6) in a way that resembles the equations of a multi-bit first-order Delta-Sigma modulator [14], [32]. In Fig. 6, a VCO with conversion gain k_{VCO} is modulated in frequency by the input signal $x(t)$. The phase of the VCO, $\phi(t)$, has a linearly growing component due to the rest angular frequency ω_0 (dotted line in Fig. 6) and a slowly varying additive component representing the integral of $x(t)$. The physical output of the VCO, however, is a square signal (or a set of square signals in a ring oscillator); therefore only phase advancement in discrete steps can be noticed, coincident with the square signal edges. The VCO output is then sampled into a discrete sequence by a flip-flop with sampling period T_s. The quantized and sampled phase $\phi_q[n]$ can therefore be modeled by adding a quantization noise component $q[n]$. The effect of the XOR gates in Fig. 5 is equivalent to computing the first-order difference of $\phi_q[n]$. Hence, the following equations are obtained :

$$\phi_q[n] = \omega_0 n T_s + k_{VCO} \int_{-\infty}^{nT_s} x(\tau) d\tau + q[n] \tag{2}$$

$$y[n] = \phi[n] - \phi[n-1] \tag{3}$$

$$= q[n] - q[n-1] + \omega_0 T_s + k_{VCO} \int_{(n-1)T_s}^{nT_s} x(\tau) d\tau \tag{4}$$

As can be seen, the output sequence $y[n]$ contains the input signal $x[t]$ averaged over each sampling period, plus the quantization noise that is indeed first-order shaped.

III. VCO-based Analog-to-Digital Conversion: Diving Deeper

There are, however, some tricky questions that trigger a deeper dive. For instance, how does the VCO rest frequency f_0 affect the quantization noise? Also, the behavior of the VCO-ADC is poorly modeled for large signals due to discrete tones in the output spectrum, similar to a 1st-order Delta-Sigma modulator. A different point of view is obtained by going back to the basics of Pulse Modulation theory [33], [34]. Fig. 7 shows how a VCO-based ADC can be expressed as the reference model of the time-encoding ADC of Fig. 1. The analog input signal $x(t)$ modulates the frequency of the VCO that generates the square wave $w(t)$. The signal $w(t)$ is applied to the monostable circuit that generates the signal $d(t)$, having a square pulse of fixed width T_s at every time instance where $w(t)$ has an edge. According to [35], the signal $d(t)$ is a Pulse Frequency Modulated representation of $x(t)$. In case $x(t)$ is a sinewave, the spectrum of $d(t)$ can be calculated analytically. Fig. 7 also shows a possible implementation of the monostable circuit that produces $d(t)$. It consists of the XOR operation between $w(t)$ and itself delayed over T_s seconds. This circuit in the end is the same as used in Fig. 4, if we move the flipflops that implement the first-order difference right before the sampling operation. Fig. 7 therefore unveils how the PFM analysis is connected to the phase-referenced model.

The spectrum of a pulse-modulated signal has a quite similar structure across different modulation types: it is composed of the input signal plus a modulated carrier at high frequency with modulation sidebands repeated around the harmonics of the carrier. For instance, Fig. 8(a) shows (part of) a slow sinusoidal input signal. Fig. 8(b) shows the PWM-encoded signal as a function of time (left) and the corresponding frequency spectrum (right), where the modulation sidebands have a spectrum envelope described by Bessel functions like in analog FM modulation. If the PWM signal is sampled, these modulation sidebands alias to lower frequencies in the form of quantization noise. Since VCO-based ADCs can be seen as Pulse Frequency Modulators (PFM), as described above, the frequency of the oscillator is modulated with the input and the edges are detected with the counter or an XOR function (as in Fig. 7). The carrier in this case is the rest oscillation frequency of the VCO. Pulse Frequency Modulation has a very special property: the modulation sidebands have periodic nulls in the frequency spectrum. Fig. 8(c) shows the same sinusoidal signal of Fig. 8(a) encoded with PFM in the time domain (left) and its corresponding spectrum in the frequency domain (right). The PFM time signal has many copies of the same pulse width T_s, occurring very frequently or only sparsely depending on the input signal amplitude. As long as the pulse width is always the same, signal theory predicts nulls in the periodic spectrum at frequencies corresponding to multiples of the inverse of the pulse width $1/T_s$. These periodic nulls arise from the sinc-shaped spectrum of the pulses composing the PFM signal. If this pulse width is forced to be the sampling period, then all carrier sidebands alias after sampling, replicating the nulls at DC, and hence creating the first-order

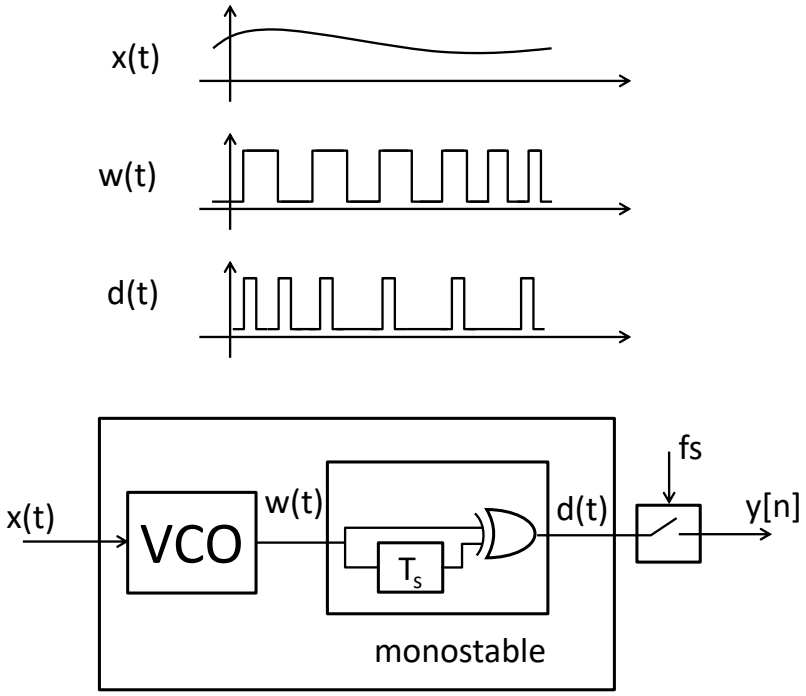

Fig. 7. Time-encoding equivalent of a VCO-based ADC.

noise shaping. This insight enables an accurate description of the more subtle behavior of VCO-based ADCs beyond the predictions of Delta-Sigma theory. For instance, it fully allows to understand the large-signal behavior and the occurrence of spurious baseband tones [34].

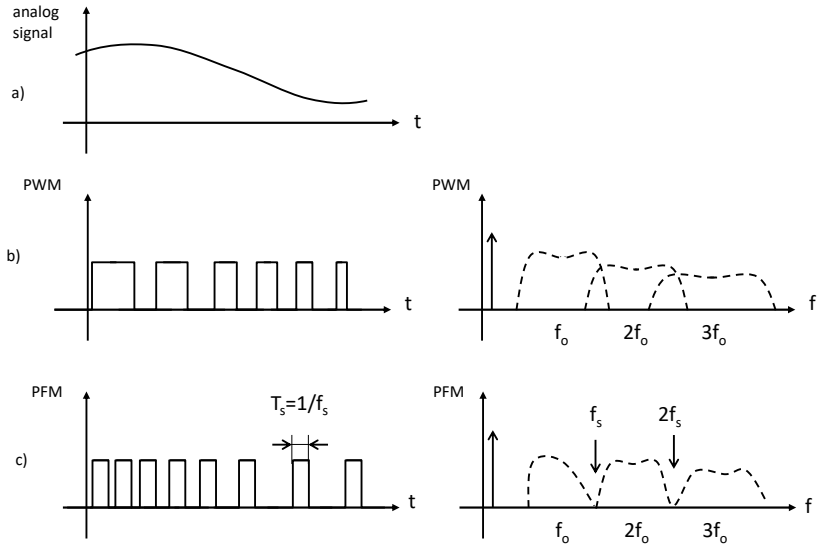

Fig. 8. Time-domain waveforms and frequency spectra of a PWM- and PFM-modulated analog signal.

IV. Circuit Design Guidelines

With the basic principles and functioning of a VCO-based ADC explained, we can now describe the major design requirements for the circuit implementation, in particular noise and distortion, as well as the impact on the design flow.

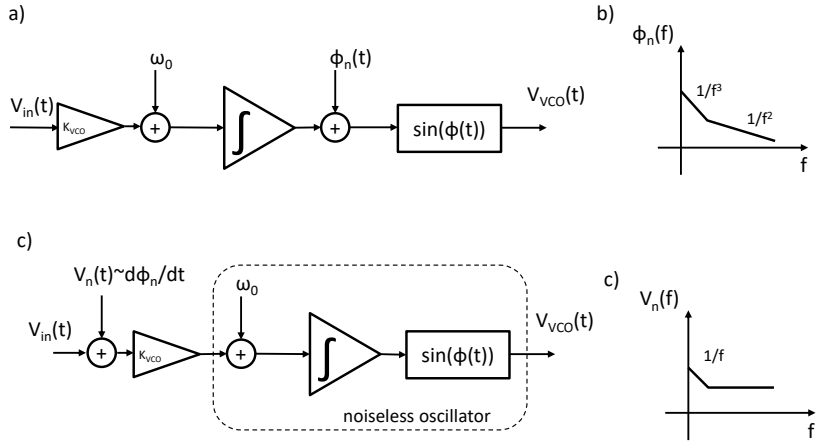

Fig. 9. Output- and input-referred modeling and corresponding spectra of phase noise in a VCO.

A. Noise

Analog ADC designers are used to calculate the input-referred noise of an ADC and to balance it properly with the quantization noise in order to optimize the power consumption of the ADC. This balance, however, tends to be a bit more tricky in VCO-based ADCs because the dominant noise typically comes from the VCO and noise in VCOs manifests itself as (output) phase noise [36]. Phase noise is described as the random fluctuation of the phase of an oscillator. Phase noise in ring oscillators has been the subject of many publications, including [30], [36], [37]. The root cause for phase noise is the thermal and flicker noise in the resistors and transistors used in the VCO. Phase noise is displayed as an additive component $\Phi_n(t)$ in the block diagram of Fig. 9(a) representing an oscillator modulated by a signal $V_{in}(t)$. Powerful simulation methods based on periodic noise analysis have been developed to predict the phase noise of an oscillator circuit, which typically has the shape of the Leeson model (see Fig. 9(b) [36]). As it is difficult to infer how such noise spectrum affects the SNR of the ADC, the VCO phase noise should be referenced to the VCO input (as in Fig. 9(c)). Referencing the VCO phase noise to the input makes the design process similar to designing any analog block [38], as the VCO's input-referred noise shows thermal and flicker noise components like any conventional analog circuit. A more straightforward approach is to use transient noise simulations, but this makes the design process very long and non-intuitive, and hence should only be done in the final design iteration [38].

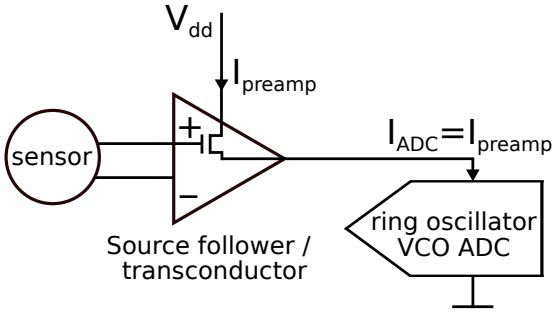

Fig. 10. VCO-based instrumentation system as application illustration.

In order to better understand the thermal noise trade-offs in the design of a VCO-based ADC system, consider as illustration the VCO-based instrumentation system shown in Fig. 10. Here, the VCO is driven by a transistor preamplifier either in current mode (by a transconductor Gm) or in voltage mode (by a source follower). Now suppose that the system is functional (with a correctly biased preamplifier, etc.), but that the noise of the system has to be reduced. This can be achieved by increasing the width of the input transistor and additionally increasing the widths of all the transistors in the ring oscillator. In this way, well established analog impedance scaling techniques are followed, sacrificing a factor of two in power for a 3 dB reduction in

circuit noise (and hence a 3 dB improvement in SNR in a circuit-noise-limited design). This is exactly the same scaling law as in conventional analog circuits, as also reflected in the typical Figure of Merit (FoM) used for ADCs[1]. As an additional perk of most VCO-based ADCs, the circuit of Fig. 10 shows that the main current driven by the Gm stage or the source follower is also supplying the ring oscillator, which means that the biasing current in the preamplifiers is shared by the active portion of the ADC, hence improving the power efficiency.

Flicker noise is also a major concern in low-bandwidth instrumentation applications. Detailed analysis of the noise in ring oscillators [30], [36], [37] has shown that flicker noise decreases proportionally to the number of oscillator taps. Loosely speaking, it is as if flicker noise is produced by a very large transistor, adding all areas of the inverters in the ring. Therefore, if low flicker noise is desired, many taps must be used in the ring oscillator. This, however, complicates the digital circuitry because more digital signals need to be sampled and processed. This shows how power is traded off between the analog and digital portions of the ADC. An important design option to reduce the impact of flicker noise in a sensing application is to use chopping [39], as will be discussed in part 2 of this paper.

B. Distortion

A huge challenge for VCO-based ADC design is the nonlinearity of the VCO characteristic. Differently from closed-loop feedback systems such as Delta-Sigma modulators, any nonlinearity in the voltage to frequency translation of the VCO used in a structure like Fig. 5 immediately degrades the SNDR of the ADC. Most of the different VCO-based ADC architectures that will be reviewed in part 2 of this article have as purpose to desensitize the ADC with respect to the VCO nonlinearity. If the input swing is small, in many cases a ring oscillator VCO can already be sufficiently linear. A standard practice to improve the distortion performance by removing even-order distortion, is to use a pseudo-differential VCO configuration (see Fig. 11), driving twin VCOs with differential input signals. This structure also has the benefit of achieving excellent PSRR values way above common belief [9]. Alternative solutions aim at limiting the signal swing using canceling feedforward paths or closed-loop feedback structures, as will be discussed in part 2.

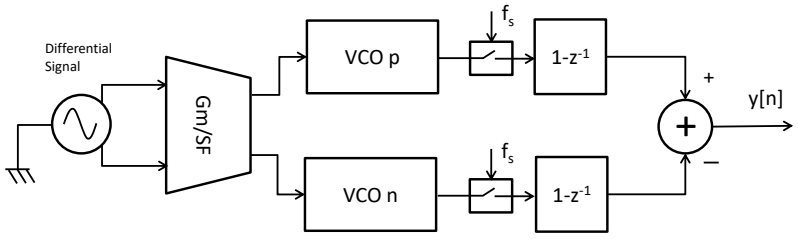

Fig. 11. Pseudo-differential VCO-based ADC configuration.

C. Design process

This takes us to a final challenge: a key problem for VCO-based ADCs is the design process itself. ADC designers usually have a background in analog circuits (e.g. capacitor-based SAR converters or Delta-Sigma modulators), and typically have little experience with ring oscillators. Phase-Locked Loop (PLL) designers might be better prepared for the job, but the kind of VCOs that they are used to design, may not be the best suited for VCO-based ADCs. A good practice is to think of the VCO as if it were an amplifier for the input signal. If one wants good noise in the ring oscillator: use large transistors [37]. If one wants improved linearity: use a differential circuit. Two oscillators with large transistors may cost power to obtain a high oscillation frequency, but then again: this is a way to save lots of biasing circuits, power-hungry opamps, capacitors and switches. ADC designers have also gotten used to minimizing the importance of digital hardware in the power budget, but in VCO-based ADCs the digital power is really significant and there may be digital logic running much faster than the sampling rate. In summary, designing time-encoding VCO-based ADCs is quite different from designing standard ADCs, and therefore requires some open-mindedness from the ADC designers.

[1]FOM = SNDR + 10 log10(BW/Power)

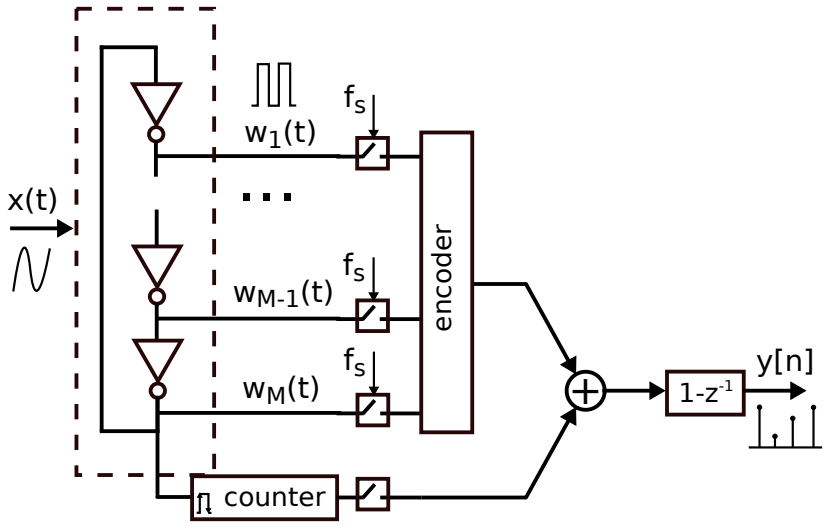

Fig. 12. Practical realization of an open-loop VCO-based ADC structure with multi-phase readout based on coarse/fine phase quantization.

V. Practical Design Example

To illustrate the above concepts and as example of the different design methodology needed for VCO-based ADCs, we now describe the circuit shown in [9], which is intended for audio applications. It is a very simple VCO-based ADC, yet it shows the full potential of time encoding. The core of the ADC consists of two twin VCOs implemented with 11-phase ring oscillators. The VCOs are driven by a differential transconductor, that isolates the VCOs from the input, which in this case is a high-output-impedance MEMS microphone. All current used by the transconductor is at the same time powering the VCOs (see Fig. 10). The transistors in the ring oscillator have widths in the order of 30μm. This large transistor size compared to what would be used for this frequency in a PLL, is needed to satisfy the input-referred noise requirement relative to the quantization noise of the converter (in the order of a few μV). The chip uses the multi-phase readout circuit shown in Fig. 12 to count the edges in the ring oscillator phases $W_1 ... W_M$ with as little power as possible. The multi-phase readout circuit is implemented with a Gray counter connected to a reference phase providing a coarse quantization code, and an encoder block that refines the total edge count from samples of the ring oscillator state. The encoder block operates at the sampling clock (2.4MHz in this case), much slower than the coarse counter (approx. 50MHz). The digital and analog power consumption are each about half of the total power. The pseudo-differential architecture pays off in distortion mitigation (the peak SNDR is 70dB in 20kHz of bandwidth without feedback) and in very good power-supply rejection (which exceeds 80dB in spite of the poor inherent power-supply rejection of a single VCO channel).

VI. Takeaway points

- Time-encoding VCO-based ADCs are an interesting ADC architecture in deeply scaled CMOS technologies, as they mostly use digital circuits and frequency-encoded square wave signals rather than voltage or current linear circuits, resulting in a small area and a good power efficiency.
- Open-loop VCO-based ADCs resemble closed-loop Delta-Sigma modulators in the sense that they behave as first-order multi-bit Delta-Sigma modulators. The key system-level design parameters to achieve a target SQNR performance are the rest oscillation frequency and the sampling frequency. Here, the phase-domain model (Fig. 6) and the corresponding SNR equation (1) should be the start of your first design iteration.
- To understand more subtle system-level effects (such as overloading and spurious baseband tones), Pulse Frequency Modulation theory is needed.
- To get good distortion and PSRR performance, always a twin setup with two pseudo-differentially driven VCOs should be used in the basic configuration. In part 2 of this paper, more complex architectures for even better performance will be discussed.

- To design the core VCO, a PLL design style is not the best approach. Instead, it is important to think in terms of the input-referred noise of the VCO, leading to large devices in the VCO core. Designing the VCO is a mixture between traditional analog amplifier design and VCO design for PLLs. Hence, it is a craft on its own !

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