Modelling the Cryogenic Properties of Germanium for Emerging Liquid Hydrogen Power Applications

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Abstract

In recent years, there has been an increase in research focused towards the reduction and/or elimination of greenhouse emissions from applications used in everyday life. In addressing this, liquid hydrogen has been highlighted as an attractive alternative fuel source for commercial vehicles due to it's lower weight, higher power density and zero greenhouse emissions in comparison to petrol and diesel fuels. Incorporating such a fuel source however introduces a cryogenic environment of 20 K affecting the power electronics used to deliver the power from source to load.

Herein, the physical properties of semiconductors influencing the overall efficiency of devices within an H-bridge circuit are considered. From this, germanium is hypothesised to be the most suitable semiconductor for power devices at or near temperatures of 20 K.

Closed-loop models are developed for the carrier concentration, carrier mobility, carrier velocity, for both electrons and holes as a function of doping concentration and temperature with critical analysis of the range of suitability for each. Multiple models are also developed for both carrier concentration and carrier mobility which offer a trade off depending on whether one requires accuracy or simplicity in calculation.

A significant influence on the device characteristics of MOSFETs is that of the oxide/semiconductor interface. For the first time, ZrO_2 is fabricated directly on germanium substrates through the thermal oxidation of zirconium on germanium. The interface state density of these capacitors are comparable to literature values offering a much cheaper and simpler fabrication method for high-κ dielectric formation on germanium substrates. The leakage

current density of the ZrO$_2$ MOS capacitors are low in comparison to reported values and are shown to decrease with decreasing temperature.

With the physical models of both bulk and interfacial germanium, multiple PiN germanium diodes are simulated using technology computer aided design (TCAD) that show the potential for germanium power devices with breakdown voltages in excess of 800 V at room temperature and 400 V at 20 K. Simulations of vertical power MOSFETs incorporating a ZrO$_2$ interlayer show great promise for low temperature power electronics at or near 20 K where other commercial devices experience significant resistive losses. With the work conducted here, vertical power MOSFETs fabricated using germanium and ZrO$_2$ open the gateway for low voltage applications incorporating liquid hydrogen fuel cells.

Table of contents

List of figures

List of tables

Nomenclature

Physical Constants

ε_0 Dielectric constant of free space

$\hbar$ Reduced Planck's constant

h Planck's constant

k_B Boltzmann's constant

m_0 rest mass of an electron

q Electronic charge

Common symbols

ε Permittivity

μ Carrier mobility

μ_e Electron mobility

μ_h Hole mobility

μ_{tot} Total carrier mobility

σ Conductivity

σ_n Conductivity of n-type region

σ_p Conductivity of p-type region

A Area

C Capacitance

C_{ox} Oxide capacitance

E Carrier energy

E_C	Conduction band energy level
E_F	Fermi energy level
E_G	Band gap
E_T	Trap energy level
E_V	Valence band energy level
F	Electric field
I	Current
J	Current density
L	Length
L_G	Gate length
m^*	Carrier effective mass
N	Doping density
n	Electron carrier density
N_A	Acceptor doping density
N_C	Density of states in the conduction band
N_D	Donor doping density
n_i	Intrinsic carrier density
N_V	Density of states in the valence band
N_{it}	Interface trap density
N_{tot}	Total doping density
P	Power
p	hole carrier density
R	Resistance
T	Absolute temperature
t_{ox}	Oxide thickness
V	Voltage

V_B	Breakdown voltage
V_D	Drain voltage
V_G	Gate voltage
V_T	Threshold voltage
V_{bi}	Built in voltage of PN junction
W	Gate Width
W_D	Depletion width of PN junction

Chapter 2

β	DC current gain
ε_r	Dielectric constant of material
ε_{ox}	Oxide permittivity
$\varepsilon_{r,high-\kappa}$	Dielectric constant of high-κ material
ε_{r,SiO_2}	Dielectric constant of SiO$_2$
ρ	Resistivity
ρ_n	Resistivity of n-type material
ρ_p	Resistivity of p-type material
B	Magnetic field strength
C_{ds}	Drain to source parasitic capacitance
C_{gd}	Gate to drain parasitic capacitance
C_{gs}	Gate to source parasitic capacitance
C_{iss}	Small signal input capacitance
C_{oss}	Small signal out capacitance
C_{rss}	Small signal reverse transfer capacitance
D	Device duty cycle
d	Distance between two plates
E_{ds}	Band edge displacement per unit dilation

E_{op}	Optical phonon deformation potential
F_M	Breakdown field
f_{sw}	switching frequency
i	Time dependent current
I_B	Base current
I_C	Collector current
I_E	Emitter current
I_{on}	On state current
L	Inductance
L	Length between rotor and magnet
P_{cond}	On state conductive losses
P_{switch}	Switching losses
P_{Total}	Total power loss
t	Time
t_{fi}	Fall time of current
t_{fv}	Fall time of voltage
t_{off}	Off time
t_{on}	On time
t_{rf}	Rise time of voltage
t_{ri}	Rise time of current
V_a	Applied voltage
EOT	Effective oxide thickness

Chapter 3

α	Canali model fitting parameter
α	Reduced conduction band energy
α_i	Philips impurity scattering fitting exponent

β	Canali model fitting parameter
β_0	Canali model fitting parameter
β_{exp}	Canali model fitting parameter
ΔE_A	Difference between valence band and acceptor energy
ΔE_D	Difference between conduction band and donor energy
η	Reduced Fermi energy
γ	Transfer electron fitting constant
μ_{app}	Apparent carrier mobility
μ_{num}	Numerically calculated carrier mobility
μ_{ac}	Acoustic phonon limited carrier mobility
μ_{DC}	Debye-Conwell carrier mobility
$\mu_{i,A}$	Philips impurity carrier mobility
$\mu_{i,L}$	Philips lattice carrier mobility
$\mu_{i,max}$	Philips maximum carrier mobility
$\mu_{i,min}$	Philips minimum carrier mobility
μ_{ii}	Ionised impurity limited carrier mobility
μ_i	Philips unified carrier mobility model
μ_{low}	Low field carrier mobility
μ_{neu}	Neutral impurity limited carrier mobility
μ_{op}	Optical phonon limited carrier mobility
τ	Carrier relaxation time
τ_{app}	Apparent relaxation time
τ_{ac}	Acoustic phonon relaxation time
τ_{DC}	Debye-conwell relaxation time
τ_{ii}	Ionised impurity relaxation time
θ_i	Philips lattice scattering fitting exponent

θ_{op}	Optical phonon temperature
$A(E)$	Neutral donor-carrier interaction function
$A_{v,sat}$	Saturation velocity fitting constant
$B_{v,sat}$	Saturation velocity fitting constant
C_l	Longitudinal elastic constant
E_A	Acceptor energy level
E_D	Donor energy level
$f(E,T)$	Fermi-Dirac occupation probability
F_T	Carrier transfer field
$F_{1/2}$	Fermi-Dirac integral of order $\frac{1}{2}$
g_A	Hole degeneracy factor
g_D	Electron degeneracy factor
l_l	Acoustic scattering length
M_C	Number of equivalent conduction band minima
m_{de}	Electron density of states effective mass
m_{dh}	Hole density of states effective mass
n'	Ionised donor screening potential
$N(E)$	Density of states
n_{deg}	Degeneracy electron concentration
$N_{i,sc,eff}$	Philips effective screening density
$N_{i,sc}$	Philips screening density
N_{neu}	Neutral donor density
N_{ref}	Philips reference doping density constant
T_{deg}	Degeneracy temperature
v	Carrier velocity
v_t	Thermal velocity

v_{sat}	Saturation velocity
x	Normalised carrier energy
Z	Charge of impurity atom in units of q

Chapter 4

β	Normalised semiconductor band bending
λ	Incident angle wavelength
μ_{acc}	Accumulation layer carrier mobility
μ_{bulk}	Bulk material carrier mobility
μ_{inv}	Inversion layer carrier mobility
$\mu_{surface}$	Surface layer carrier mobility
ω	Angular frequency
ω_{op}	Optical phonon angular frequency
ϕ_B	Bulk semiconductor potential
ψ_s	Semiconductor band bending potential
θ_c	X-ray critical angle
θ_n	X-ray maximum/minimum angle
C	Correction factor
C_s	Semiconductor capacitance
C_{HF}	High frequency capacitance
C_{ma}	Measured accumulation capacitance
C_m	Measured capacitance
C_{sFB}	Semiconductor flat band capacitance
C_{sr}	Surface roughness fitting constant
$C_{T,n}$	Terman n-type capacitance
$C_{T,p}$	Terman p-type capacitance
C_T	Terman capacitance

D_{it}	Interface trap density
G_{ma}	Measured accumulation conductance
G_m	Measured conductance
J_{DT}	Direct tunnelling current density
J_{FN}	Fowler-Nordheim current density
J_{Tun}	Tunnelling current density
L_D	Debye length
L_{ox}	Oxide length
R_D	Drain resistance
R_S	Source resistance
$R_{accumulation}$	Accumulation resistance
$R_{channel}$	Channel resistance
R_{drift}	Drift resistance
x_{acc}	Accumulation layer depth
x_{inv}	Inversion layer depth

Chapter 5

α_n	Electron ionisation coefficient
α_p	Hole ionisation coefficient
ε_r	Dielectric constant of material
ε_{ox}	Oxide permittivity
μ_c	Interface coulomb limited carrier mobility
μ_{eff}	Effective carrier mobility
μ_{FE}	Field effect carrier mobility
μ_{rp}	Interface remote phonon limited carrier mobility
μ_{sr}	Interface roughens limited carrier mobility
$\overrightarrow{J_n}$	Electron current density vector

$\overrightarrow{J_p}$	Hole current density vector
$\overrightarrow{J}$	Current density vector
τ	Minority carrier lifetime
τ_n	Electron carrier lifetime
τ_p	Hole carrier lifetime
τ_{dop}	Doping limited carrier lifetime
τ_{max}	Maximum carrier lifetime
τ_{min}	Minimum carrier lifetime
C_{rp}	Remote phonon fitting constant
D_n	Electron diffusivity
D_p	Hole diffusivity
$F_\perp$	Perpendicular field
$F_\perp$	Reference field constant
F_{eff}	Effective field
F_{ox}	Oxide field
g_m	Transistor transconductance
I_D	Drain current
$I_{D,sat}$	Drain saturation current
L_n	Electron diffusion length
L_p	Hole diffusion length
$L_{d,min}$	Minimum drift region length
n_1	Electron trap carrier density
N_{dep}	Depletion charge density
N_{inv}	Inversion charge density
n_{n0}	Zero bias majority electron carrier density
N_{ox}	Oxide trap density

n_{p0}	Zero bias minority electron carrier density
n_p	Minority electron carrier density
p_1	Hole trap carrier density
p_{n0}	Zero bias minority hole carrier density
p_n	Minority hole carrier density
p_{p0}	Zero bias majority hole carrier density
R_{net}	Net recombination rate
R_s	Series resistance
z	Interface-carrier distance

Chapter 1

Introduction

In today's world, the continued growth and development of technology has corresponded to an exponential increase in global energy consumption. This continual growth has consumed the vast majority of the worlds fossil fuels, the use of which contributes largely to global warming. To help reduce these adverse effects, great amounts of research are being focused into methods which can reduce the amount of fossil fuels needed to power daily used systems or alternative fuelling methods to reduce fossil fuel consumption [1, 2].

Conventional reduction of fossil fuel consumption in systems is achieved by increasing the overall system efficiency. In aerospace systems, the reduction of aerodynamic drag on the aircraft can greatly reduce the amount of thrust required to reach a steady-state speed, reducing the overall energy consumption. The main reduction of engine usage in early designs was achieved by creating a light, aerodynamic body that caused little drag and could manoeuvre easily. In recent years, manufacturers have created designs which incorporate a reduction in aerodynamic drag and incorporate H_2 fuel cells that have potential efficiencies over twice that of combustion engines [3, 4]. Alternative fuel allows for a significant or complete reduction of greenhouse emissions, requiring only a small alteration to system design.

Hydrogen based fuel systems have received considerable attention in recent years [3, 2] as a promising alternative to fossil fuels, with research showing successfully powered vehicles and promise for further implementation in America and Japan. Following this, there has also been an increase in hydrogen fuelling stations for public transport in the Czech Republic [5, 6]. Combustion of liquid hydrogen produces 3.196 times the power per kg compared to gasoline [7], with the added benefit that the only by-product is water when combusted in air. As such, hydrogen power designs are currently being investigated as an environmentally friendly alternative to conventional fossil fuel powered automotive systems.

1.1 Motivation: Highly efficient commercial vehicles with a H_2 based fuel source

Liquid hydrogen maintains a rest temperature of 20 K, which lies below the critical temperature of many commercial superconductors. This has been considered by NASA and the ATI who have incorporated liquid H_2 into their recent designs for more preferred forms of air and automotive travel [9]. The cruise efficient short take-off and landing (CESTOL) [10, 11] is an example of one of these proposed designs which incorporates a H_2 based fuel source,
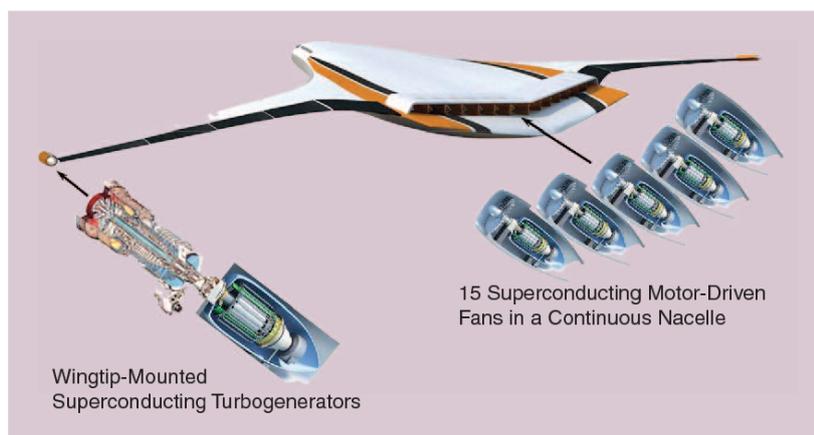
Fig. 1.1 NASA CESTOL design incorporating superconducting motors [8].

and was designed by NASA with the intentions of reducing fuel consumption by reducing take-off/landing time through an alternative aircraft design and is shown in Fig 1.1. The CES-TOL design also incorporates a boundary layer ingestion system which requires electrical control of a distributed power network connected to multiple loads. Electrical control of a distributed power system requires control electronics that can transfer power generated from the hydrogen-based source to turbines with the use of superconducting wires, which is one of the key issues preventing the realisation of the design. The superconducting wires are made from MgB_2 which has a critical temperature of 40 K [12] and can be used to deliver power at current densities sufficient for the application while maintaining zero resistive losses. MgB_2 is highly durable and can be easily weaved and manipulated within a motor, unlike other superconductors which are brittle.

One of the key issues facing further development of the CESTOL design is the require-ment of control electronics that can suitably function at a temperature of 20 K. The electrical resistance of commercial power electronics fabricated from semiconductors such as silicon and silicon-carbide exponentially increases at temperatures below 100 K and are incapable of supporting the large current densities required to drive the distributed motors.

As an alternative to the commonly used semiconductors which are available commer-cially, we have recently concluded that semiconducting germanium is a suitable alternative semiconductor for the development of control electronics at cryogenic temperatures due to its superior conductivity stability at cryogenic temperatures [13]. Germanium is becoming considered an alternative for silicon based electronics. The first germanium devices were fabricated in the late 40s at Bell laboratories and were characterised shortly after [14, 15]. Following further research, germanium was pushed aside to make way for the development of silicon based technology. The cause of this was due to the favourable native oxide of silicon which is highly stable in comparison to the water soluble oxide of germanium [10, 16]. As well as this, contacting of germanium electronics becomes an issue due to the pinning of the

Fermi-level close to valence band edge in germanium resulting in non-ohmic like conduction of carriers for n-type germanium [17, 18]. Devices fabricated from germanium also suffer from lower breakdown voltages below 100 V and are unsuitable for high power applications which consider voltages in excess of 1000 V [19, 20].

In the past 5 decades, further research into the nature of contacting [18, 21] and oxide formation [22] on germanium has removed the issues of contacting and oxide stability which prevented the commercialisation of germanium devices. As well as this, alternative device structures which use vertical topologies as opposed to the conventional lateral structure can theoretically lead to the fabrication of germanium devices with breakdown voltages in excess of 900 V [23, 24]. These recent developments coupled with the superb cryogenic stability in material conductivity [25, 26] makes germanium a highly promising candidate for emerging cryogenic power applications incorporating liquid hydrogen fuel cells.

1.2   Thesis outline

Despite the promising developments in germanium based research, there is a significant lack of computational models which would allow manufacturers to simulate how germanium based devices and/or circuits incorporating germanium devices would perform at room temperatures or in extreme environments. The work reported within this thesis aims to model the physical properties of germanium which are crucial for simulating device performance including the temperature and voltage dependence of the carrier concentration and carrier mobility for both minority and majority carriers. Coupled with these models, experimental data including the capacitance and leakage characteristics of fabricated ZrO_2 metal oxide semiconductor (MOS) capacitors on germanium that are crucial for simulating MOS devices have been analysed from room temperature down to 77 K. These models and experimental data will then be used to predict the performance of diodes and MOS based devices in order to develop closed-loop models which can be incorporated into simulation programs such as

technology computer aided design (TCAD) and SPICE.

Chapter 2: Literature review

The performance and characteristics of high power metal oxide semiconductor field effect transistors (MOSFETs) and diodes fabricated from the commonly used materials silicon, silicon-carbide and gallium-nitride are analysed at cryogenic temperatures. The physical mechanisms covering the exponential increase in electrical resistance of power electronic devices at cryogenic temperatures is explored. The characteristics of Germanium and GaAs, which retain their room temperature like conductivity down to a temperature of 20 K, are compared to the characteristics of commonly used semiconductors such as silicon, 4H-SiC and GaN. From this, the most promising material for emerging liquid hydrogen applications is concluded to be germanium.

Chapter 3: Modelling the Cryogenic Properties of Germanium for Device Simulation

Despite a significant research focus on germanium devices in the 50's and 60's, the ability to simulate and predict the performance of germanium based devices and circuits is not possible due to a lack of physical models for the material. The physical properties of germanium including carrier concentration, carrier mobility and saturation velocity are all modelled theoretically and are compared, and in some cases adapted, in order to agree with experimental data presented in literature. The models used are further adapted to match existing TCAD frameworks for simulation.

Chapter 4: Metal Oxide Germanium Capacitor Fabrication and Temperature Analysis

From analysis of commercial power devices, it is known that vertical MOSFETs are capable of supporting higher current densities at cryogenic temperatures. In order to model the performance of MOS devices at cryogenic temperatures, the interface properties of germanium MOS capacitors incorporating Al_2O_3 and ZrO_2 both with germanium interlayers are compared. For the first time, ZrO_2/Ge MOS capacitors are fabricated thorough the

thermal oxidation of zirconium on germanium that demonstrate interface densities within 2-3 times the best reported values for ZrO_2 on germanium [27, 28]. The capacitance-voltage (CV) characteristics and cryogenic leakage characteristics of thermally oxidised zirconium on germanium with an in-situ GeO_2 interlayer are measured showing a reduction in current density by two orders of magnitude at cryogenic temperatures.

Chapter 5: TCAD simulation of germanium power diode and vertical ZrO_2 n-type MOSFETs

Following the modelling of the bulk characteristics and determination of the MOS interface characteristics of chapters 3 and 4, the cryogenic characteristics of high power germanium PiN diodes and n-type vertical ZrO_2 MOSFETs are simulated using TCAD. The conduction properties of the germanium/oxide interface is modelled based on experimental data from literature and the measured ZrO_2 MOS capacitor interface trap density and oxide permittivity to estimate the transfer characteristics of a germanium power MOSFET at room temperature, 77 and 20 K. From this, it is found that germanium power diodes and ZrO_2 MOSFETs demonstrate the greatest reduction in on-state resistance from room temperature down to 20 K in comparison to commercial power devices.

Chapter 6: Conclusions

A summary of the key findings and results from this work and a list of future work.

1.3   Key contributions

A list of key contributions of this paper to the research community include:

- L.J. Bradley, C.M. Donaghy-Spargo, G.J. Atkinson, and A.B. Horsfall, Evaluating suitable semiconducting materials for cryogenic power electronics, *The Journal of Engineering*, 2019(17):4475-4479, Jun 2019.

As well as this, at least two papers are expected to be submitted based on the modelling work conducted in chapter 3 and experimental data in chapter 4. The modelling work in chapter 3 highlights the importance of using the correct mobility and ionisation model at low temperatures in order to accurately recreate experimental data for germanium at low temperatures, whilst the experimental data from chapter 4 explores the temperature dependence of leakage currents within ZrO_2 on germanium in addition to the development of a model that predicts the leakage current as a function of temperature, voltage and oxide thickness.

Chapter 2

Literature Review: Properties of cryogenic power electronics and semiconductors at cryogenic temperatures

2.1 Introduction

The area of electronics for high power applications has received a lot of attention in recent years as one of the major limiting factors of the overall efficiency in motor and generator systems is limited by the maximum switching frequency and resistive losses of the control electronics. Maintaining a lower operating temperature using proper thermal management reduces the overall resistive losses of power devices whilst choosing a highly conductive semiconducting material for device fabrication will also serve to reduce the on-state losses. This chapter aims to address the requirement for semiconducting transistor switches and

diodes in high power switching circuits with focus towards motor applications incorporating liquid hydrogen fuel cells.

2.2 Power electronics in DC control circuits

In drive applications, motors can be powered using an AC or DC power source. Both types of machines offer disadvantages and advantages in comparison to the other and manufacturers often prioritise one depending on the application. In terms of control, DC machines are far more favourable than AC motors as they have a higher speed, greater ease of control and low starting torque compared to AC motors. As such, DC motors are typically used for low voltage motors that require quick response time and precise control that is more easily achieved in comparison to AC motors [30–32].

In order for DC motors to turn, a significant drive current must be provided to the stator to induce a magnetic field within the windings of the machine. A diagram showing how
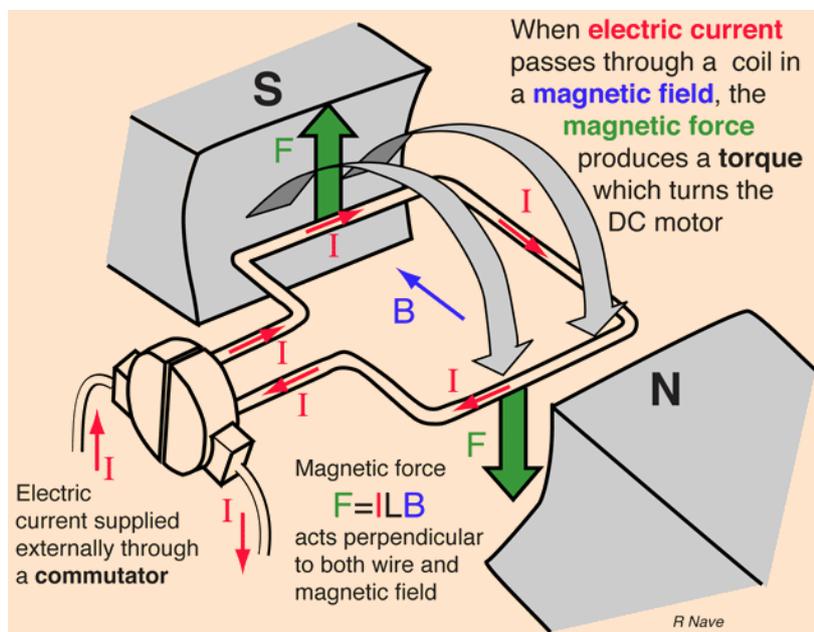
Fig. 2.1 Diagram indicating rotation inside DC motor where F is force, I is current and B is the magnetic field strength [29].

rotation is achieved in a DC machine can be seen in figure 2.1. A rotor is placed between two stationary magnets providing a continuous magnetic field. If a DC current is passed through the rotor, the rotor will experience a force given by

$$\text{Force} = BIL \tag{2.1}$$

where B is the magnetic field strength, I is the current and L is the distance between the rotor and magnet resulting in rotation. By increasing the current, the force acting on the wire can be increased, although the rotation of the motor can only be reversed by reversing the direction of the current. In order to allow for directional and speed control of the motor, a switching circuit must be employed to control the direction of current through the motor.

A commonly used method by which to control the direction and speed of a DC motor is to use an H-bridge circuit [33, 34] in which a DC motor is placed at the centre of 4 high power switches as shown in figure 2.2. When switches F1 and F2 are pressed, current can flow from left to right through the motor leading to rotation, similarly, by pressing switches B1 and B2, the direction of the current can be reversed. By replacing the switches with transistors and a subsequent transistor switching circuit, the direction and speed of the motor can be controlled.
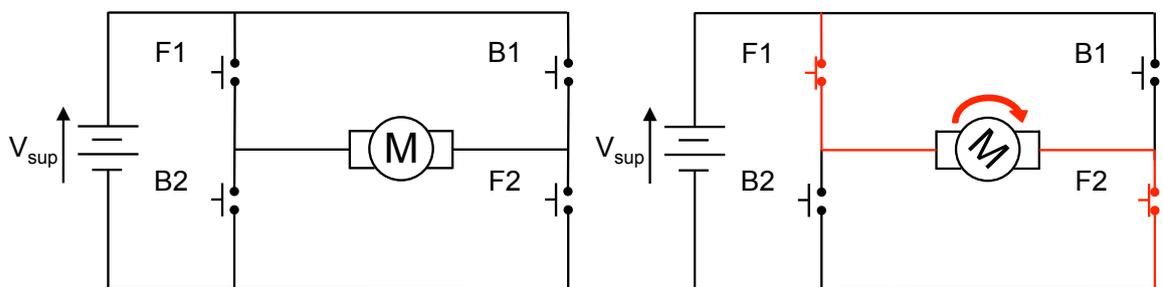
(a) H-bridge diagram using 4 push to make switches and DC motor

(b) Motor rotates forward when switches F1 and F2 are pressed

Fig. 2.2 H-bridge using push to make switches and a DC motor.

2.2.1   MOSFETs as a switch for current control

A transistor is used as a switch within an electronic circuit to control the flow of current through the application of a voltage on a gate contact. A diagram of a lateral and vertical MOSFET can be seen in figure 2.3 along with an example of the switching characteristics of a commercial 25 V n-type silicon MOSFET [35] and a commercial high power 1.2 kV SiC MOSFET [36].

For both MOSFETs, electron conduction cannot occur from source to drain unless a sufficient gate voltage has been achieved. By applying a positive gate bias, minority electrons within the p-type region of both devices are attracted to the oxide/semiconductor interface of the device. Once the gate voltage has exceeded the threshold voltage of the device, the concentration of electrons near the interface will exceed the majority hole concentration forming an n-type region at the interface. With this n-type region near the interface, electrons are able to conduct from source to drain. The threshold voltage itself has two common definitions which include the voltage at which the drain current achieves a certain level or by taking the voltage intercept of the tangent at the maximum gradient from a drain current-gate voltage ($I_D V_G$) profile.

The transfer characteristics of a low and a high power MOSFET can be seen in figures 2.3c and 2.3e. As can be seen for both devices, beyond a certain threshold voltage, the drain current increases exponentially. At higher temperatures, the threshold voltage of both devices decreases. For the power device, it can be seen that at high gate voltages, the gradient begins to decrease which is due to an increase in the resistance of the lightly doped drift region of the device [37, 38].

As shown in figures 2.3d and 2.3f, following the application of a gate bias exceeding the threshold voltage, the drain current can be increased linearly with drain to source voltage. As the drain voltage increases, the difference in the gate voltage with respect to the substrate decreases and the concentration of carriers near the drain end begins to decrease. At this point,
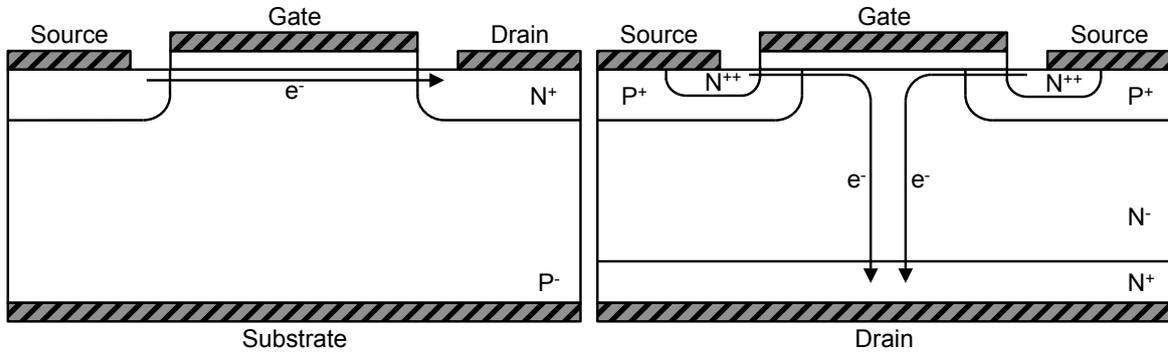
(a) Lateral n-type MOSFET

(b) Vertical n-type MOSFET
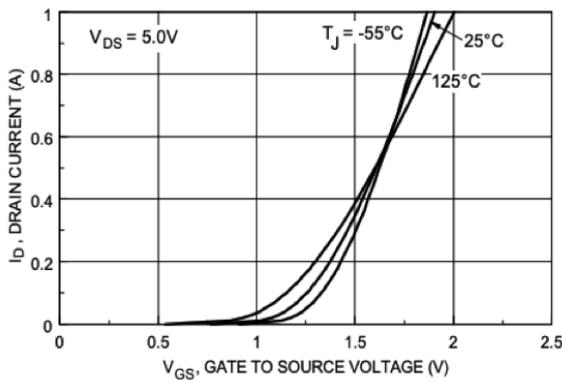
(c) IdVg of commerical FDV303N MOSFET
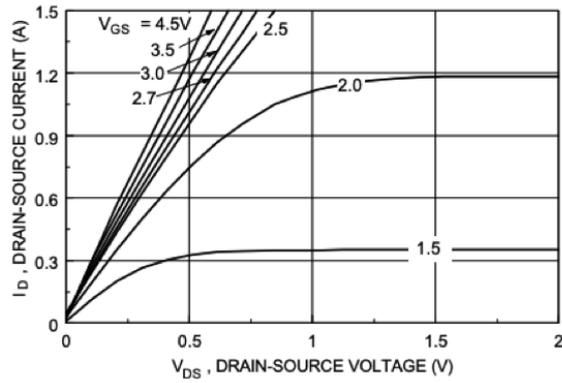
(d) IdVd of commerical FDV303N MOSFET
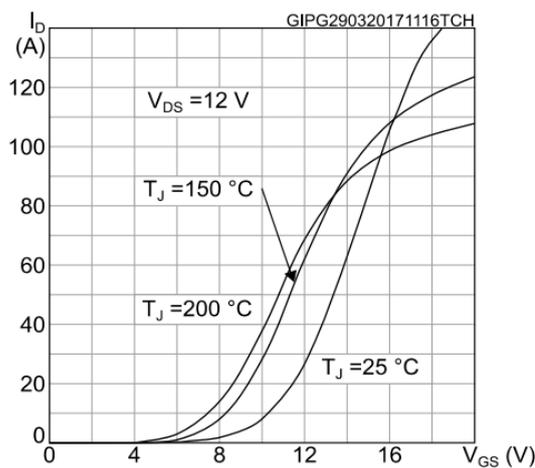
(e) IdVg of commerical SCT50N120 MOSFET
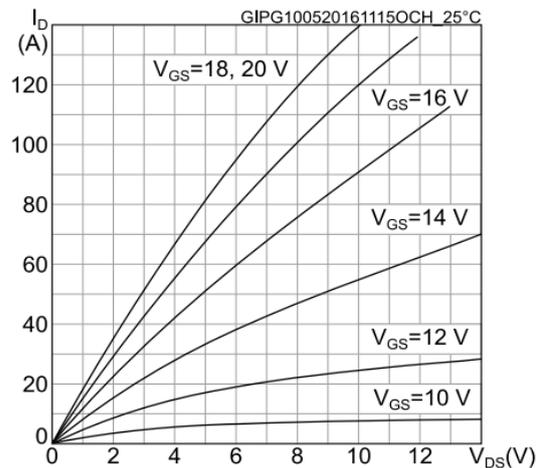
(f) IdVd of commerical SCT50N120 MOSFET

Fig. 2.3 Structure of standard n-type lateral (a) and vertical power MOSFET (b) where arrows indicate direction of electron flow. Transfer and output characteristics of low power MOSFET (c,d) and vertical power MOSFET (e,f) are taken from commercial data sheets [35, 36].

the drain current becomes sub-linear before eventually saturating to a drain independent value know as the saturation current. Once the drain current has saturated it can only be increased by increasing the gate voltage.

By including a large lightly doped drift region, the vertical power MOSFET is capable of supporting blocking voltages in excess of 1 kV [39, 40] but also results in larger threshold voltages and saturation voltages. Despite this, high power transistors are commonly used in high voltage motor applications for both DC and AC applications [41–43].

2.2.2   Power MOSFETs and Diodes in H-bridge circuits

An example of a switching circuit incorporating 4 n-type MOSFETs can be seen in figure 2.4. Similarly to the circuit in figure 2.2, by switching transistors F1 and F2, a current will flow through the motor from left to right driving the motor and the direction of the current can be switched by turning off transistors F1 and F2 and switching on B1 and B2. The switching of the transistors within the H-bridge circuit is performed through a control gate drive microprocessor that controls the signals sent to the gate contacts of each transistor. An example of the gate drive switching characteristics can be seen in figure 2.5.

For a duty cycle of 50%, both sets of transistors are switched on and off for the same period of time and the average current through the motor is zero. For a duty cycle above or below 50%, the average current through the motor will either flow in one direction or the other and the speed of the motor can be controlled by defining the duty ratio of each MOSFET.

As can be seen from the switching characteristics, there exists a short period of time where switching of the current and voltage from on to off or off to on results in a significant increase in power loss. As well as these losses, on-state and off-state losses are also present due to the ohmic losses of the transistor in steady-state conditions. As will be shown later,

these losses can be minimised by choosing a device with a low on-state resistance, low switching time and low parasitic capacitances.

Free-wheeling diode

Within the H-bridge circuit, 4 diodes are connected in reverse bias with the drain and source of each MOSFET. The purposes of these diodes are to protect each MOSFET from voltage breakdown resulting from current switching. Considering a circuit with parasitic inductances, or solely considering the motor which acts as an inductor and resistor in series within a

(a) H-bridge circuit for DC motor

(b) Parasitic components of n-type MOSFET
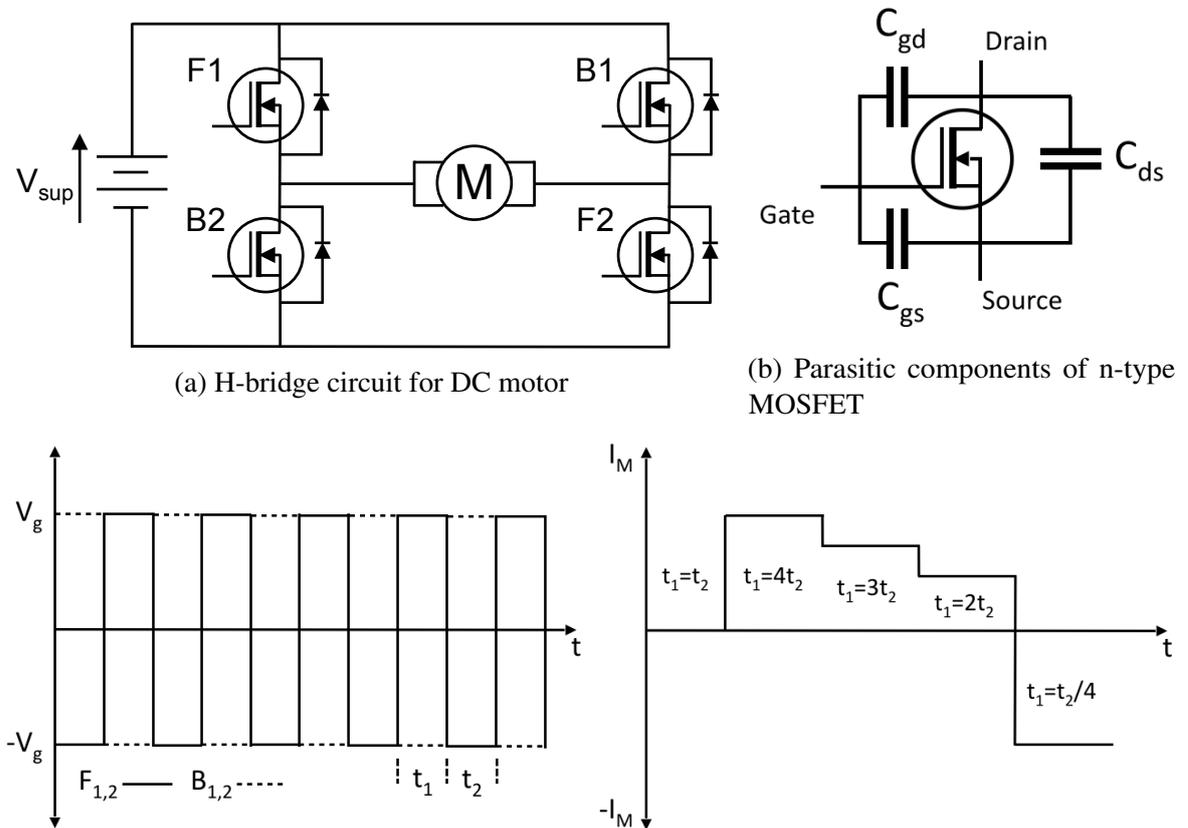
(c) Wave forms acting on the gate of MOSFETs $F_{1,2}$ and $B_{1,2}$. Different timing ratios for the MOSFET pairs allows for control of the current density through the motor.

Fig. 2.4 Circuit diagram of H-bridge circuit including pin out diagram of n-type MOSFET with parasitic capacitances. Duty cycle of 50% is achieved when both t_1 and t_2 are equal, altering this ratio results in a driving current and rotation of motor.

circuit, the voltage induced from an inductor is given by

$$V(t) = L\frac{\partial i}{\partial t} \tag{2.2}$$

where L is the inductance of either the motor or the parasitic components within the circuit and t is time. As the transistor switches from positive to negative current, the voltage induced over the drain and source of the motor will induce a large voltage in the reverse direction as charge is built up on the source contact of the MOSFET. In order to eliminate this charge, the freewheeling diode creates a loop of current through the source and drain of the MOSFET and the charge is dissipated through resistive losses.

As well as the resistive losses, extra losses in the diode can come from the reverse switching, that is, when the transistor is switched on, the diode becomes subjected to a sudden large reverse bias. As can be seen in figure 2.5, the switching of a diode from forward current to reverse current results in a large reverse current. At t_1, the current through the diode is switched from positive to negative. For a small period of time, the current through the diode in reverse direction can achieve current levels within the same order of magnitude as the current levels of the forward direction as there is a concentration of charge stored within the diode from the forward conduction. At time t_2, the voltage of the diode approaches zero
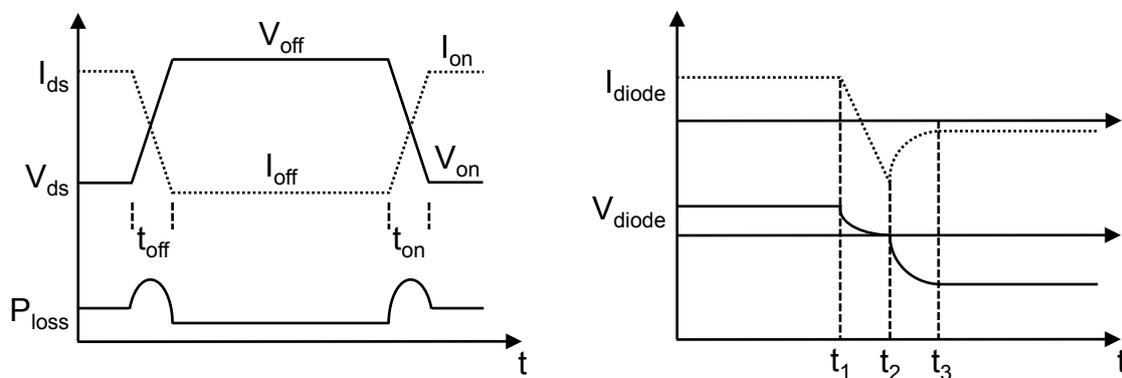
Fig. 2.5 Voltage and current switching characteristics of MOSFET and diode in H-bridge circuit. Ringing due to parasitics not included.

and the current in the reverse direction reaches the peak reverse current. At this point, the current begins to decay to the leakage current value whilst the voltage decays to the reverse of the bias applied to MOSFET drain to source. The losses incurred from the switching are dependent on the maximum recovery current and reverse recovery time equal to t_3 - t_1 and can be reduced by selecting a diode with a high carrier mobility and high carrier lifetime [44].

2.2.3 Power loss

Due to the high current densities and large supply voltages, power electronic devices experience significant power loss and must be thermally managed in order to remain within specific operating temperatures. An example of a heat map of a SiC MOSFET and a silicon isolated gate bipolar transistor (IGBT) can be seen in figure 2.6. As can be seen, during device operation, the temperature of both devices has risen to over 120 °C and is common for high-temperature power devices fabricated from silicon, SiC and GaN [45–47].

The resistive power loss of an electronic device with a time unvarying on-state current I_{on} is given by

$$P_{cond} = I_{on}^2 R \tag{2.3}$$
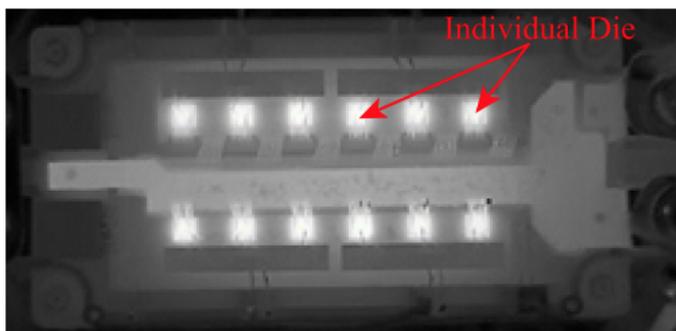
(a) Infared image of SiC module
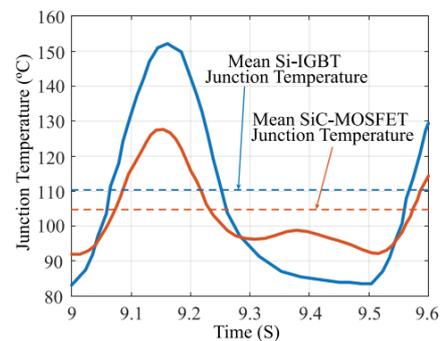
(b) Junction temperature vs time

Fig. 2.6 Infared heat map of 1.7 kV, 450 A SiC module and junction temperature of device compared to a high power silicon IGBT [48].

where R is the device resistance. The switching loss of a transistor switch is given by

$$P_{switch} = 0.5I_{on}^2 R f_{sw}(t_{on} + t_{off})$$ (2.4)

where f_{sw} is the switching frequency, and t_{on} and t_{off} are the on and off switching times given by

$$t_{on} = t_{ri} + t_{fv}$$ (2.5a)

$$t_{off} = t_{fi} + t_{rv}$$ (2.5b)

where, respectively, t_{ri} and t_{fv} are the rise time of the current and fall time of the voltage and t_{fi} and t_{rv} are the fall time of the current and rise time of the voltage. The total loss of a transistor in a switching circuit is finally

$$P_{Total} = P_{cond}D + P_{switch}$$ (2.6)

where D is the duty cycle equal to t_{on}/t_{off}. By considering the individual power loss components, it can be seen that the power loss can be minimised through minimising the series resistance.

In reducing switching losses, it has been found that the total rise time and fall time of the transistor increases with the parasitic capacitances of the device. As charge is stored at the gate and drain with respect to the ground potential at the source, parasitic capacitances will exist between the three terminals as illustrated in figure 2.4b.

Parasitic capacitance components

The influence of the parasitic capacitances on the total rise time and fall time of the devices has been shown to be directly correlated to the switching losses in power MOSFETs [49, 50, 11]. The parasitic capacitances of a device are present between the contacts of a device and are the

result of opposing charge attracting between the contacts. This attraction in charge leads to a delay in the rise time and fall time of currents and voltages at the contacts of power devices leading to an increase in switching losses. As such, utilising a device with low parasitic capacitances is preferable in reducing switching losses.

The parasitic losses of power MOSFETs are calculated based on the small-signal input capacitance (C_{iss}), small-signal output capacitance (C_{oss}) and small-signal reverse transfer capacitance (C_{rss}) defined as

$$C_{iss} = C_{gd} + C_{gs} \tag{2.7a}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{2.7b}$$

$$C_{rss} = C_{gd} \tag{2.7c}$$

where C_{gd}, C_{gs} and C_{ds} are the gate to drain, gate to source and drain to source parasitic capacitances of the device. When measuring the parasitic capacitance, the total parasitic are determined by measuring the individual capacitances between each terminal of the MOSFET as a function of drain to source voltage with zero gate bias. An example of the parasitic
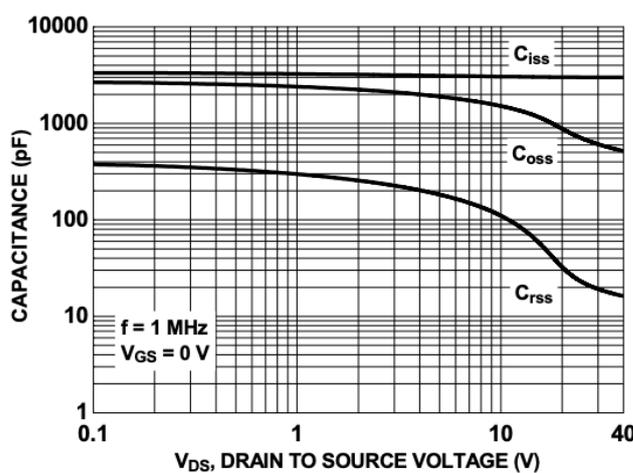
(a) 40 V silicon Trench MOSFET   (b) 1.2 kV SiC Trench MOSFET
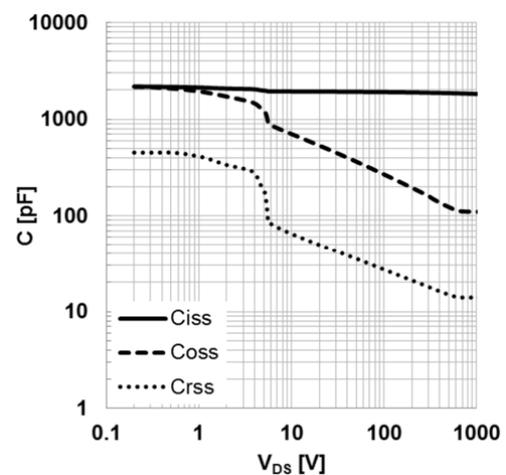
Fig. 2.7 Input, output and reverse steady-state parasitic capacitance of a low power silicon (a) and high power SiC trench MOSFET (b) [51, 52].

components measured for a silicon and SiC power Trench MOSFETs can be seen in figure 2.7. As can be seen, as the drain to source voltage increases, the output and reverse steady-state capacitance decreases monotonically. The cause of this is due to an increase in device leakage resulting in a reduction in accumulated charge at the drain contact. For the input steady-state capacitance, it can be seen that for both devices, it remains essentially voltage independent whilst also remaining the largest parasitic component of both devices.

The reason for the high input steady-state capacitance in comparison to the output and reverse steady-state is due to the close proximity of the gate and source contacts. For two parallel plates, the capacitance generating between the two plates is given by

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{2.8}$$

where ε_0 and ε_r are the dielectric constant of the vacuum and the relative dielectric constant of the medium, A is the area and d is the distance between the two plates. For air, ε_r is unity whilst it takes a value of 11.7 in silicon. Although the geometry of the contacts of the trench MOSFETs is not that of two parallel plates, the capacitance between the contacts will be greater for contacts that are within close proximity of one another in comparison to contacts that are far apart. As such, the C_{iss}, which is the only component that relies on the C_{ds} will be much greater than that of C_{oss} and C_{rss}.

For diodes, the reverse polarity of the diode when placed in parallel with any power MOS-FET results in a large capacitance that contributes to an increase in the off-state switching of the MOSFET but does not affect the on-state switching. Typically, the capacitance of power diodes varies in a similar manner to that of C_{oss} and C_{rss} of the power MOSFET with a significant contribution resulting from the length of the drift region. By incorporating a device with a large drift region, a large blocking voltage and low capacitance can be achieved; although this does result in an increased on-state resistance.

By minimising the parasitic capacitances of the power devices, the on and off times of the MOSFETs will reduce; resulting in lower switching losses. As well as this, the switching loss can be further minimised by selecting a material with a high carrier mobility as it will take less time for charge to enter/leave the device during a switching cycle.

2.3 Performance of Power Electronic Devices at Cryogenic Temperatures

With the recent development and incorporation of liquid hydrogen fuel cells in automotive vehicles, the suitability of commonly used devices and commercial power electronics has recently received a lot of attention for extreme environments [55, 56, 54, 57–59].

A plot of the on-state resistance for a SiC and GaN power MOSFETs can be seen in figure 2.8. For GaN (and also silicon) devices, the on-state resistance and thermal management of devices decreases with a reduction in temperature due to an increase in carrier mobility and thermal conductivity. For SiC devices, due to the greater breakdown field in comparison to silicon, power devices with breakdown voltages in the kV range can be
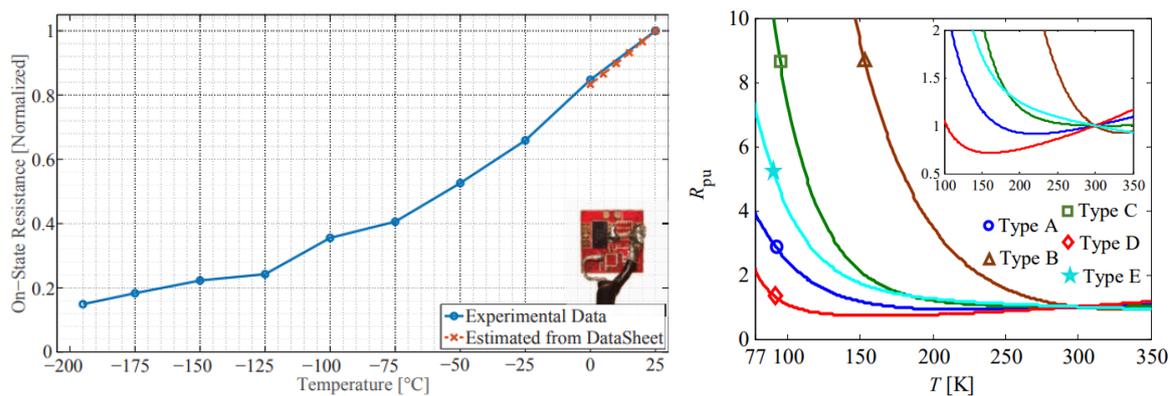
(a) 200 V GaN MOSFET from Efficient Power Conversion (EPC)

(b) 5 1.2 kV SiC MOSFETs from different manufacturers

Fig. 2.8 Temperature dependence of the on-state resistance of a high power 200 V GaN (a) and 5 different 1.2 kV SiC MOSFETs (b) [53, 54].

fabricated with drift region doping concentrations exceeding 10^{15}, although this high doping concentration results in a negative temperature coefficient for the on-state resistance as the increased scattering from dopants reduces the carrier mobility with reducing temperature.

As a result of the different temperature coefficients for the resistance of the SiC and GaN, GaN is proposed as a more suitable material for low-temperature electronics in comparison to SiC which is primarily considered for high-temperature applications.

For the majority of commercial MOSFETs, an increase in the threshold voltage of the device is experienced with a reduction in temperature. The temperature characteristics of the measured threshold voltage within selected GaN, SiC, and silicon devices can be seen in figure 2.9. The increase in threshold voltage is attributed to the reduction in minority carrier concentration within the p-region of enhancement mode devices. For GaN devices, this increase in threshold voltage is typically negligible, but for the silicon and SiC devices, the threshold voltage increases by more than 2 and 3 times respectively. Whilst this could be a problem for complimentary-MOS applications which aim to use lower driving voltages, the gate driving voltage used in the on-state regime of power electronic devices is typically of the order of 10-15 V and so this difference in threshold voltage can be neglected.
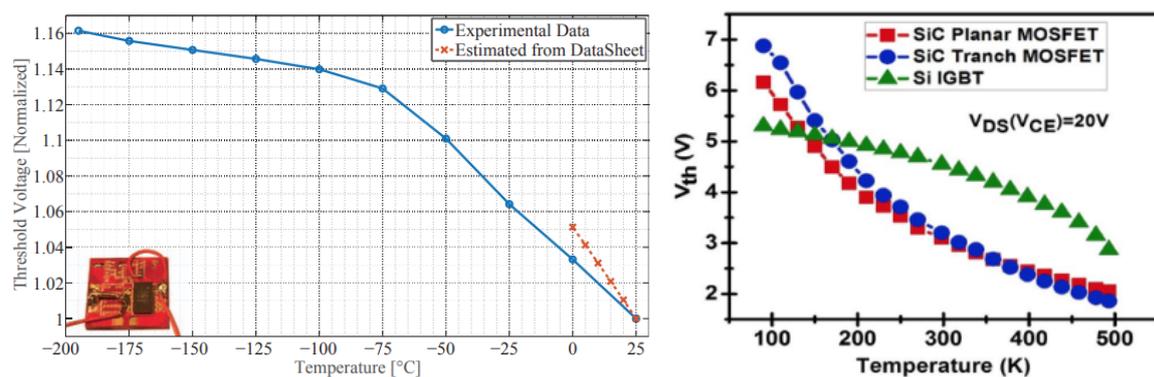
(a) 200 V GaN MOSFET from Efficient Power Conversion (EPC)

(b) Threshold voltage of two 1.2 kV SiC MOSFETs and a 1.2 kV silicon IGBT

Fig. 2.9 Measured threshold voltage in a 200 V GaN (a) and SiC and Si power FETs (b) [53, 60].

Device switching

In measuring the switching characteristics, it has been found that the losses reduce with reducing temperature for silicon and GaN devices whilst they increase for SiC [62, 60, 63]. Whilst the capacitance at high drain biases remains essentially temperature independent [58], the reduction in device switching comes from the reduced switching times due to a lower series resistance resulting in faster charging/discharging.

As a result of this, it has been found that for the majority of power electronic circuits, SiC MOSFETs are commonly deemed less suitable as the increase in switching losses and on-state losses results in a lower circuit efficiency whilst GaN and silicon increase in efficiency with reduction in temperature down to 77 K.

For diodes, switching losses have been shown to decrease for silicon and SiC with a reduction in reverse recovery time and a reduction in maximum reverse current [55, 61]. A plot of the reduction in reverse recovery time of a silicon and SiC power diode is plotted in figure 2.10. from both sets of data, it can be seen that the reverse recovery current peaks at values greater than the forward current in silicon at room temperature, whereas for SiC
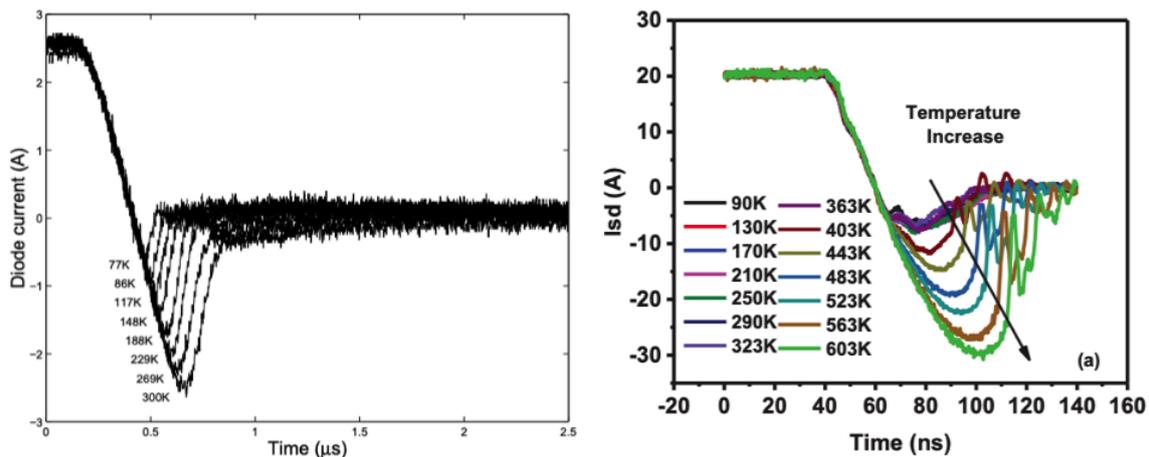
(a) Reverse recovery of 1.2 kV silicon Power diode from RS

(b) Reverse recovery of 1.2 kV SiC Power MOSFET body diode

Fig. 2.10 Measured reverse recovery time for a silicon power diode (a) and a SiC power body diode (b) [55, 61].

this only occurs when the temperature exceeds 450 K. For GaN devices, there is a negligible change in the reverse recovery characteristics of measured high power diodes [64], with quicker recovery rates than silicon although slower when compared to SiC [65–67].

Breakdown voltage

The breakdown voltage of power devices is dependent on the ionisation coefficients for electrons and holes and the distribution of the electric field within the device [70–72]. It has been shown that for low and high power devices, the ionisation factors for electrons and holes gradually increases with reducing temperature. A plot of the measured breakdown voltage for a silicon and SiC power MOSFET can be seen in figure 2.11. As can be seen for the silicon device, the breakdown voltage decreases gradually to approximately 80 % of the room temperature value. For the SiC device, the breakdown voltage can be seen to reduce gradually from 1700 to 1600 V from room temperature to 150 K for both devices. Below 150 K, the breakdown voltage reduces significantly in device (b) to 1325 V at 77 K whilst device (a) only reduces to 1550 V. The difference in breakdown voltage trend at low temperatures was not investigated further and was determined to be related to packaging

(a) silicon 650 V power MOSFET

(b) 4H-SiC 1200V power MOSFET
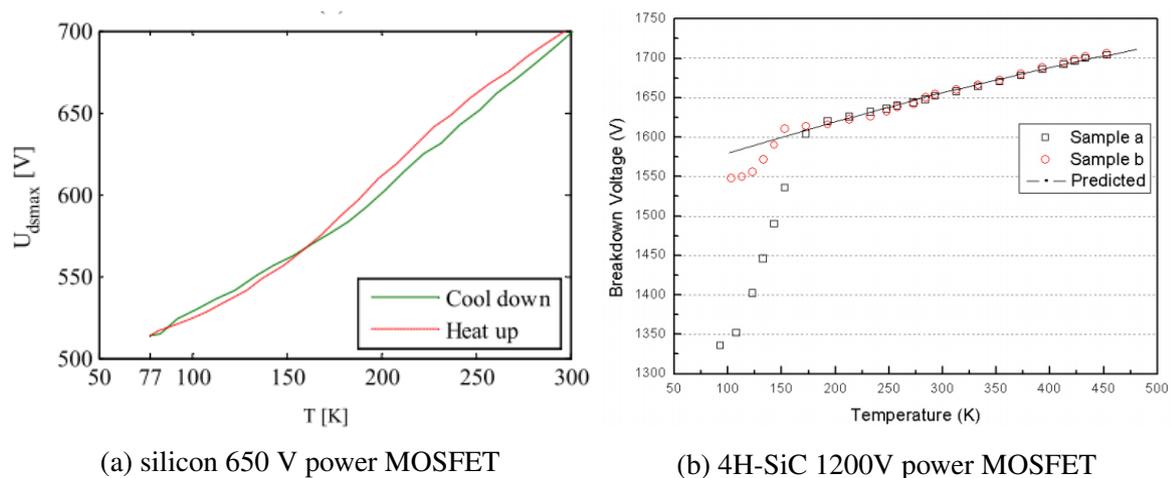
Fig. 2.11 Temperature dependence of the breakdown voltage within high power silicon (a) and SiC (b) power MOSFETs [68, 69].

issues [68]. The gradual reduction in breakdown voltage with reducing temperature must be taken into consideration when designing a power device for low-temperature applications.

2.3.1 Operation of vertical power MOSFETs

As the name implies, a vertical MOSFET is simply a linear MOSFET that has been fabricated such that the conduction of carriers is vertical rather than lateral. By doing so, it is possible for manufactures to add a thick lightly doped drift region that is essential to ensure a large breakdown voltage for power electronic devices. The two common device structures for vertical power MOSFETs are the double-diffused and trench MOSFETs both of which can be seen in figure 2.12.

Similar to the operation of the lateral MOSFET, the total current through a vertical MOSFET is limited by the gate bias and the total resistance of each region. Considering an n-type double-diffused MOSFET, conduction of electrons from source to drain cannot occur as there is a p-type region blocking conduction from the n^+ region near the source and the n^- body. In order for a current to flow, an n-type inversion channel must be created at the oxide/p-type region interface through the application of a positive gate bias. The bias required to create a sufficient channel for conduction is known as the threshold voltage which typically ranges from 1-3 V depending on the operating temperature, channel doping concentration and oxide capacitance. Once a sufficient gate bias has been achieved, electrons can conduct from source to drain. Initially, the current increases linearly with drain to source voltage. As the drain to source voltage increases, the relative difference in the gate voltage and the voltage at the oxide/p-type region near the drain decreases leading to a gradual reduction in current until eventually the current saturates to a voltage independent value.

The functionality of the trench MOSFET (or sometimes referred to as the UMOS) is equivalent to that of the double-diffused MOSFET. The key difference between the two FET designs are the direction of the current conduction in the channel and the total on-state

resistance. When considering the conduction path of electrons in double-diffused MOSFETs, it can be seen that carriers are confined between two PN regions once they pass through the channel. These carriers are scattered due to the close proximity of the current path to the
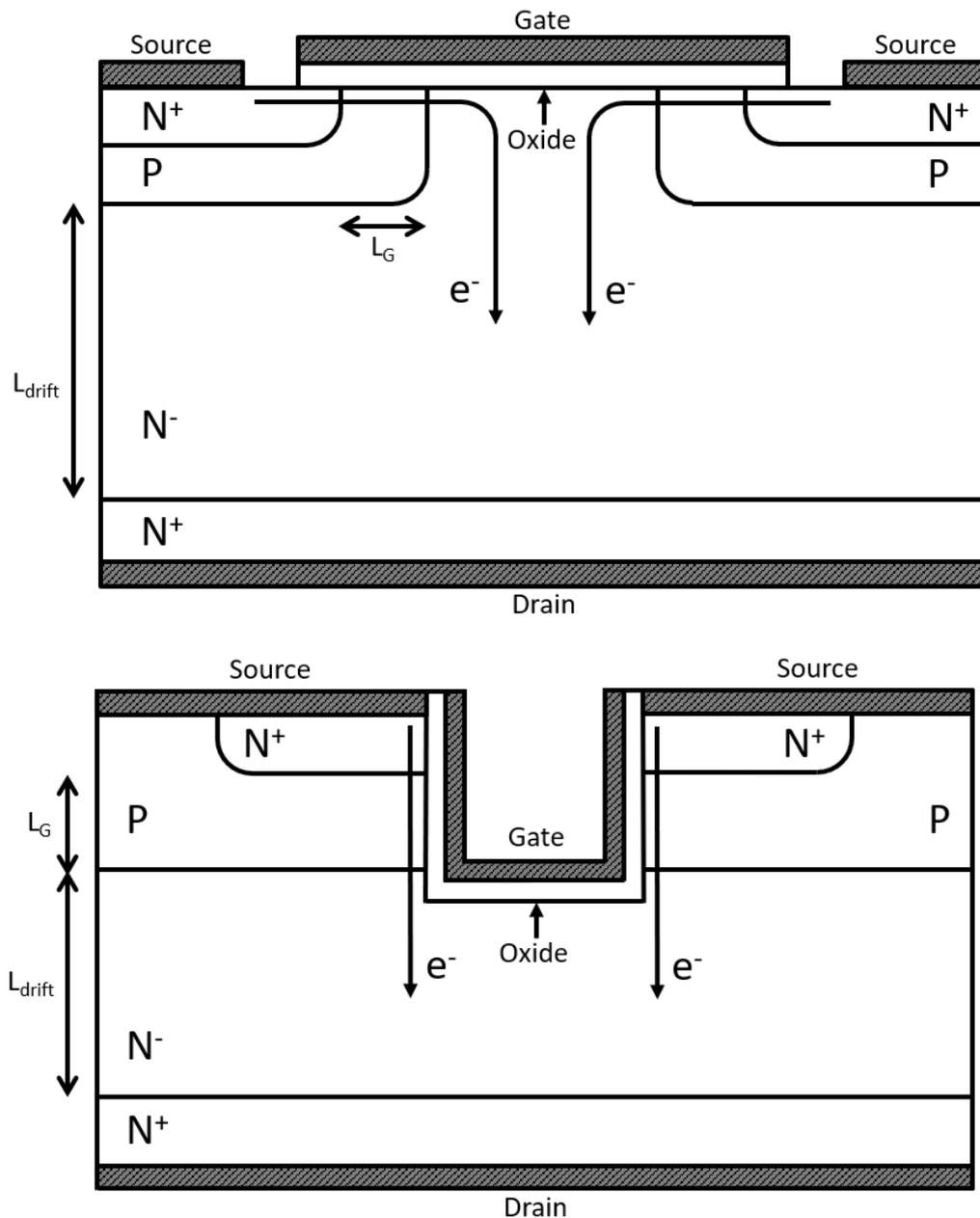
Fig. 2.12 Structure and electron conduction path in n-type double-diffused MOSFET (a) and tench MOSFET (b).

bias generated at the p-type/n-type regions reducing the total effective current area in the body. This effect is known as the parasitic JFET resistance that is observed in both n-type and p-type double-diffused MOSFETs but is not observed in trench MOSFETs due to the removal of carrier conduction in-between two diffused p-type regions.

Despite the reduced on-state resistance, trench MOSFETs are harder to fabricate due to the optimisation of the oxide trench depth and semiconductor side wall oxidation and, as such, both transistor types can be found commercially and in literature. Here, we will be considering the on-state resistance of vertical n-type trench MOSFETs as we are aiming to determine the minimum achievable on-state resistance for power electronic devices fabricated from germanium.

2.3.2 Alternative high power transistors

As well as high power MOSFETs, other transistor structures include bipolar junction transistors (BJTs), IGBTs and high electron mobility transistors (HEMTs) and are shown in figure 2.13. In the on-state, the transfer characteristics of each of these transistors is similar to that of a power MOSFET but fundamentally works on a different current conduction mechanism for each device.

For BJTs, the total emitter current is a sum of the collector current (I_C) and base current (I_B)

$$I_E = I_C + I_B = \beta I_B + I_B \tag{2.9}$$

where β is the DC current gain. The DC current gain of the bipolar transistor is based on the minority carrier diffusion current from emitter to drain which increases due to the injection of carriers at the base resulting in a magnification of the collector current. As a result of the current magnification, the on-state resistance of power BJTs are low in comparison to power MOSFETs but suffer in switching losses due to the long transport times of minority carriers within the device as well as requiring both electron and holes to traverse the length
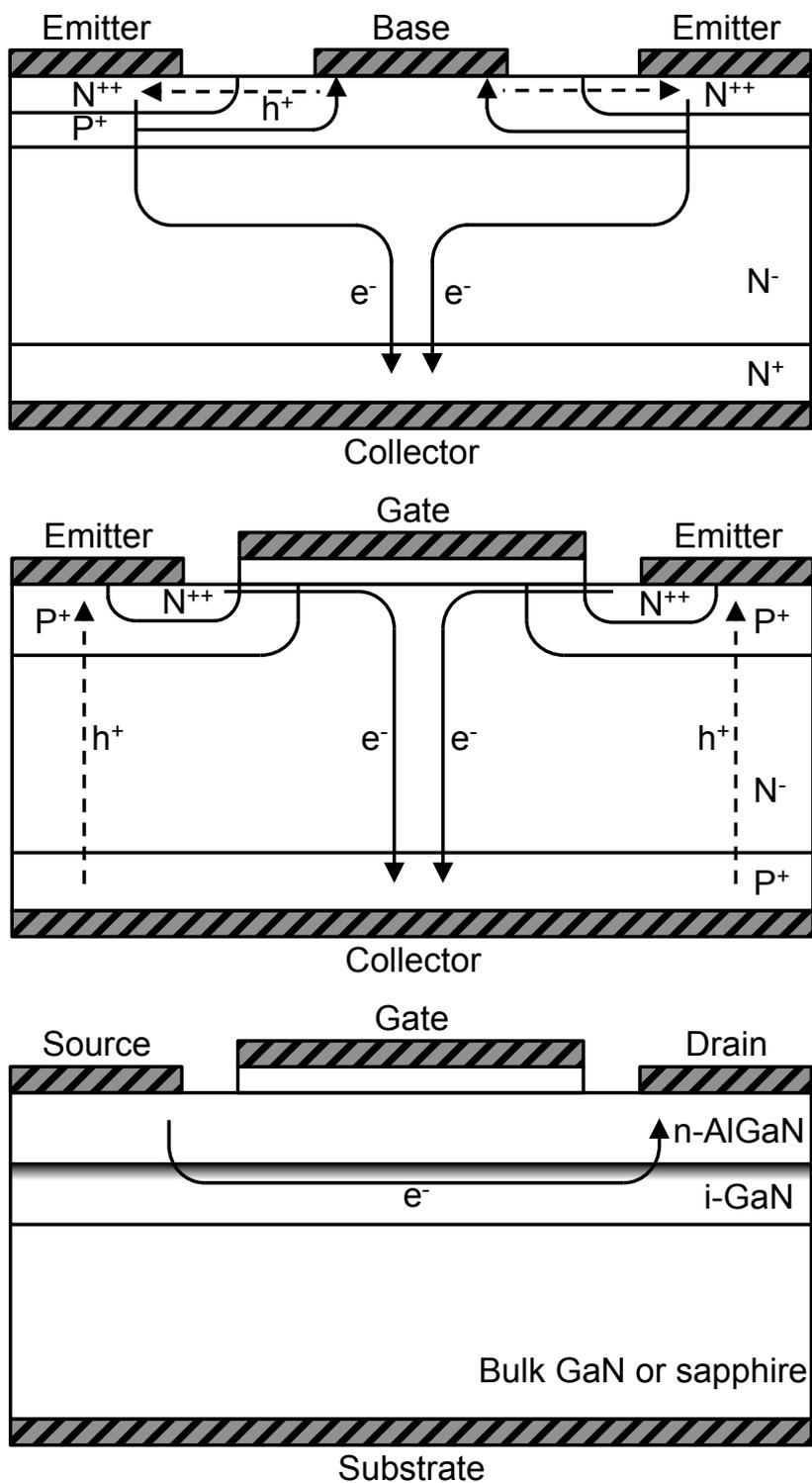
Fig. 2.13 Typical power transistor structure for a BJT (top), IGBT (middle) and HEMT (bottom) where arrows indicate electron and hole conduction.

of the device. As well is this, measurements at cryogenic temperatures show a significant reduction by nearly two orders of magnitude for the current gain at 77 K in comparison to room temperature and an increase in switching time [73–75].

The IGBT merges the current gain of the BJT with the gate control of the MOSFET and is often used for high current medium voltage applications. The current conduction of the IGBT is highlighted in figure 2.13. For an n-type IGBT, the hole conduction is based on the characteristics of a PNP bipolar transistor whilst the electron conduction is based on the MOSFET conduction through the gate and must also diffuse through the P^+ layer. Down to 77 K, the on-state and switching losses reduce compared to the room temperature value but increase for the majority of commercial devices at temperature below 77 K [60, 76].

Finally, the recent advances in GaN fabrication has lead to the commercialisation of lateral high power HEMTs with breakdown voltages in excess of 600 V [38]. At the interface, a 2-dimensional electron gas (2DEG) is formed through the polarisation of carriers generated from surface states into the channel. Due to the high carrier concentration, the carriers are effectively screened from impurities within the AlGaN layer which, when coupled with the low doping concentration of the GaN layer, results in a much greater carrier mobility in comparison to bulk GaN [77]. As a result of the high electron mobility, GaN devices have much faster switching times and higher conductivity's than the majority of commercial power devices in the same voltage range but suffer from quick degradation [78, 79].

Comparative studies [80–82, 37] on the performance of power transistors at cryogenic temperatures have shown that for temperatures below 20 K, unipolar and HEMT devices exhibit the greatest reduction in on-state resistance and switching losses of all fabricated devices. A more physical insight into the temperature dependence of the on-state and switching losses of power electronic devices shows that the main contribution to a low resistance device is a high carrier mobility and high carrier concentration which is dependant on both device structure and semiconducting material.

2.4 Determination of optimal material for cryogenic applications

The choice of semiconducting material for power devices depends largely on the application of use. For low power applications, such as logic devices, manufacturers are primarily focused towards the maximum operating frequency of a device which is dependant on the speed of charge transfer through a material. For high power applications, such as the control of driving current through an electrical actuator, the conductivity and power transfer characteristics are the key parameters which determine the suitability of a material for devices. Regardless of the application, the key figures of merit for each material are dependant on their physical properties and must be considered for all applications.

In cryogenic environments, the physical properties of semiconducting materials vary greatly from their room temperature values and is the cause of the difference in temperature dependence of the on-state resistance of SiC, GaN, and silicon power devices [80, 72, 83]. By taking into consideration the material dependant mechanisms that lead to an improvement of power electronic devices with reducing temperature, the optimal material for high power devices can be determined. In this chapter, commercially available semiconducting Si, Ge, GaAs, 4H-SiC and GaN devices are compared in order to identify the optimal semiconducting material for cryogenic power electronic applications.

2.4.1 The Requirement for highly efficient power electronics at temperatures below 77 K

A number of applications are examining the possibility of using superconducting cables for the transfer of electrical power, in an effort to increase the efficiency of circuits used to deliver power from source to load [84]. This is being driven by on-going research to identify more efficient designs for air travel, which are being pursued by organisations including

NASA and ATI [85, 10, 86]. In the last decade, NASA has proposed a hybrid-electric propulsion system, that in conjunction with a new aircraft design, is estimated to be around 70% more efficient than the conventional airliners that are in use today [87] that is based on the combustion of liquid hydrogen as a fuel source. As well as this, recently emerging applications are looking at incorporating liquid hydrogen fuel cells for low voltage DC motors [3] and standalone wind-hydrogen plants [2]. In order to provide control over the behaviour of the machine and provide isolation in the case of failure, a control circuit will be required that comprises of power electronics devices that can operate when cooled by liquid hydrogen. In an attempt to maximise the efficiency of these cryogenic power systems, the power distribution network will incorporate superconducting cables that will eliminate resistive losses [88]. The boiling point of liquid hydrogen is 20.28 K and this enables both the machine and the power distribution system to be fabricated using magnesium diboride, MgB_2 which has a superconducting transition temperature of 40 K [12].

Because of the high currents within a superconducting system, the on-state resistance of a power electronic circuit will be the most significant source of inefficiency in a cryogenic circuit. In order for a power electronic MOSFET to be suitable for liquid hydrogen applications, it must demonstrate a:

1. Reduced on-state resistance at 20 K in comparison to 300 K

2. Fast switching speeds with low parasitic capacitances

3. High thermal conductivity for good thermal management

In order to determine the ideal semiconducting material to reach these requirements, the temperature dependence of the physical properties of each material must be considered.

2.5 Temperature Dependence of Bulk Semiconducting Properties

The choice of semiconductor for the realisation of power electronics circuits is dependent on the range of operating temperatures the circuit will encounter. For high-temperature applications (T> 400 K), the superlative material properties and silicon like process technologies of the numerous polytypes of SiC have resulted in them becoming the material of choice for power electronic devices. At intermediate temperatures (123 K<T< 400 K), the significant knowledge of Si characteristics, coupled with the financial benefits of using such an abundant material has lead to it being the most technologically advanced and commonly used semiconductor, despite the presence of materials that offer more beneficial characteristics.

2.5.1 Carrier mobility as a function of temperature and doping

When considering the maximum device switching speed, the mobility and length of the device are the key figures of merit. During the charging/discharging of a device contact such as the drain, the rise time and fall time of the current is dependent on the capacitance and resistance of the device. For example, the switching and on-state losses of power MOSFETs have been shown to be directly proportional to the series resistance of the device [89, 90] which can be minimised through maximising the carrier mobility.

As the operating temperature is reduced, the physical properties of a semiconductor change, resulting in a change in how electronic devices fabricated from these semiconductors behave. For example, a comparison of the electron and hole mobilities in Ge, Si, 4H-SiC and GaAs as a function of temperature for low and intermediate doping concentrations is shown in figure 2.14. From the data, it can be seen that as the temperature reduces, the carrier mobility within all semiconductors increases although the rate of change with temperature is different for all materials.

For low doping concentrations where the net doping concentration is of the order of 10^{14} cm^{-3}, the mobility at intermediate to high temperatures is limited by the scattering from optical and acoustic phonons. Theoretically, the lattice scattering limited mobility resulting from acoustic phonons is expected to follow a T$^{-1.5}$ temperature dependence [26], although the combination of acoustic and optical phonon scattering lead to results that deviate from this form [101, 92, 98].

(a) N_D - $N_A \leq 10^{14}$ cm^{-3} [91, 25, 92, 93]

(b) N_D - $N_A \approx 10^{16}$ cm^{-3} [26, 25, 92, 94]

(c) N_A - $N_D \leq 10^{14}$ cm^{-3} [95–98]

(d) N_A - $N_D \approx 10^{16}$ cm^{-3} [99, 100, 97, 98]
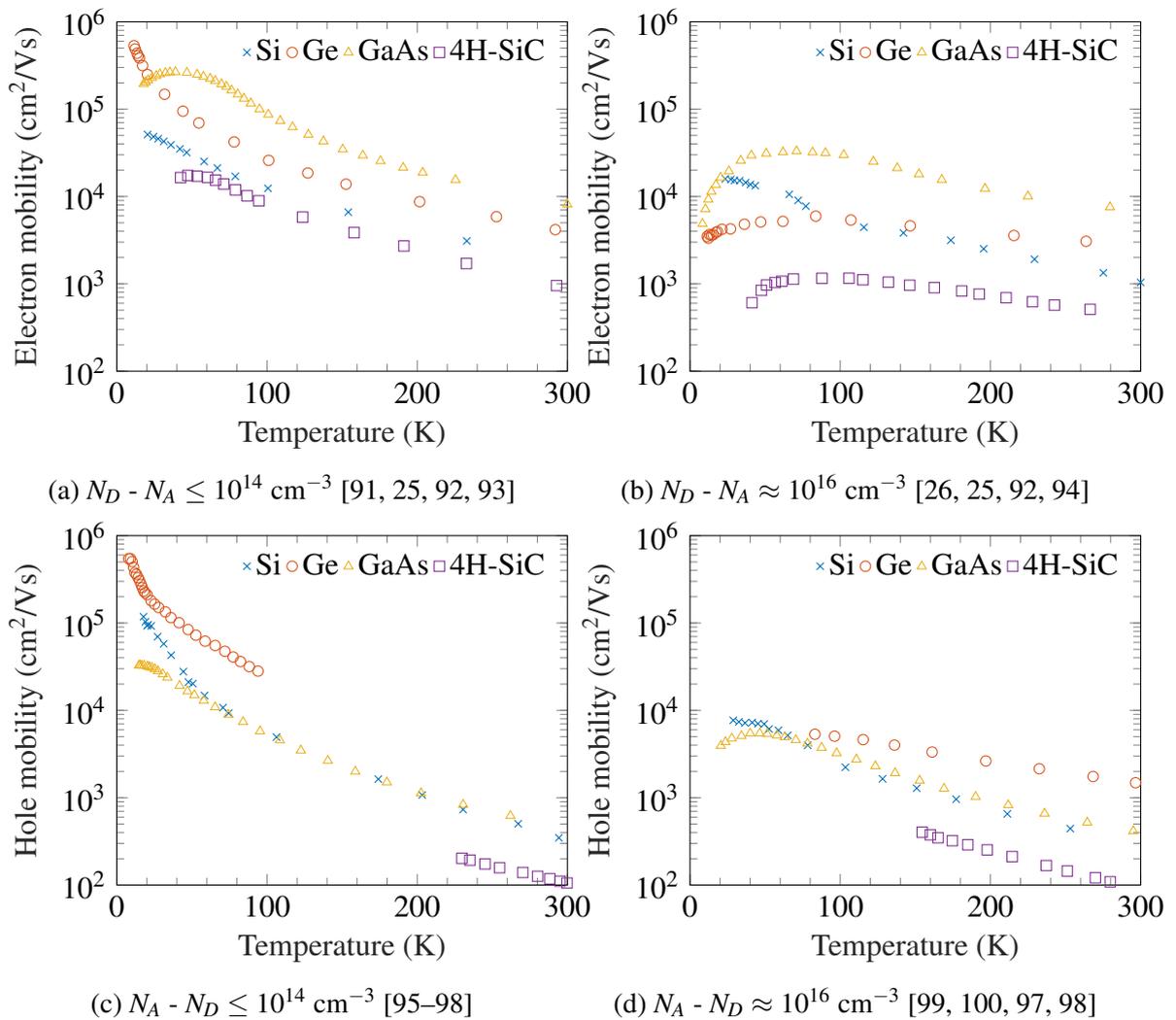
Fig. 2.14 Electron and Hole hall mobility for Si, Ge, GaAs, and 4H-SiC for highly pure (a,c) and doping concentrations close to 10^{16} cm^{-3} (b,d).

At low temperatures, or as the doping level is increased, scattering from ionised impurities reduces the mobility in each material. The cause of the increased scattering is due to the charged centres that are introduced into the lattice from ionised dopant atoms. For pure elements such as silicon and germanium with a low doping concentration, this effect is not observed but as will be shown later, this effect becomes prominent for doping concentrations above 10^{16} cm^{-3}.

The reduction of carrier mobility from ionised impurities can be mitigated by using a HEMT structure as shown in figure 2.15 for GaN. For GaN HEMT devices, the 2DEG screens carriers in the channel from ionised impurities within the AlGaN layer resulting in ultrahigh carrier mobilities at low temperatures in comparison to bulk. This can also be achieved in GaAs when creating an interface with AlGaAs [102]. Despite the low resistive losses from switching, the issues with device longevity and gate leakage have lead to GaN power HEMTs being preferred for high power electronics [78, 65, 103].
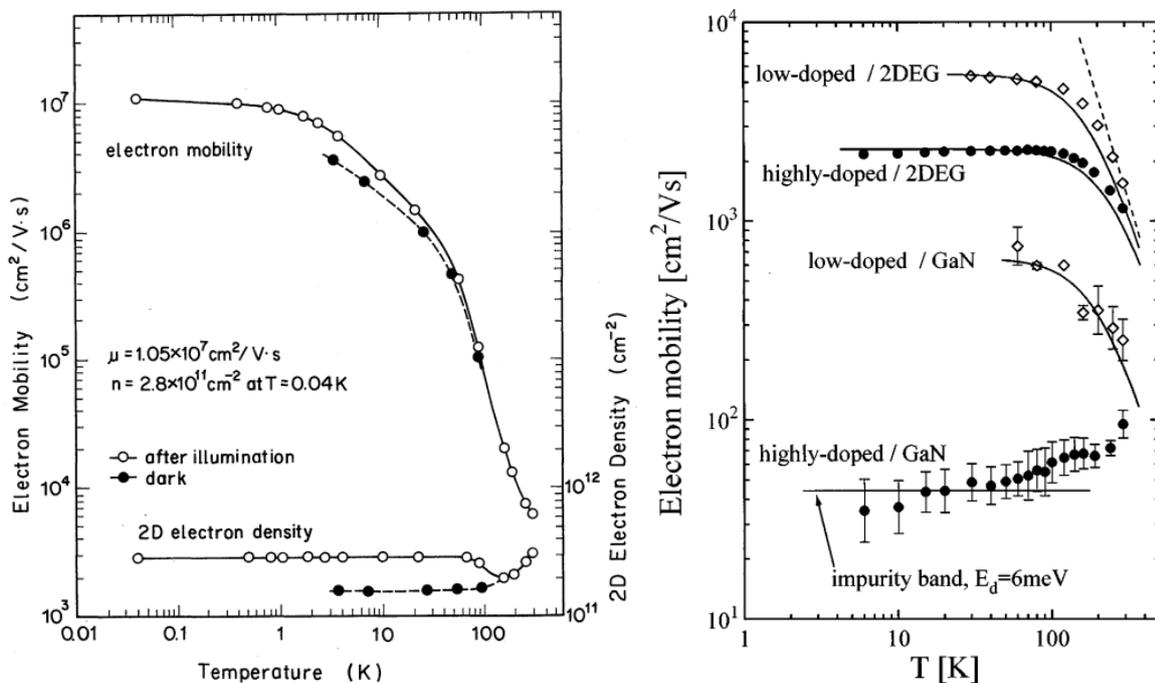
Fig. 2.15 2D electron mobility within a GaAs/AlGaAs (left) and a GaN/AlGaN HEMT (right) [102, 77]. Highly-doped and Low-doped GaN refer to bulk GaN mobilities.

2.5.2 Device resistance and breakdown voltage trade off

As well as the carrier mobility, the resistance of any semiconducting material is dependant on the carrier concentration and dimensions given through

$$R = \frac{\rho L}{A} \tag{2.10}$$

where L is the material length and ρ is the resistivity given by

$$\rho = \frac{1}{nq\mu_e + pq\mu_h} \tag{2.11}$$

where n and p are the free electron and hole concentrations and μ_e, μ_h are the electron and hole mobilities and q is the electronic charge. Whilst material lengths and areas are limited by the pitch and size of device density on a chip, the device resistance for a unipolar device can be minimised by maximising both the carrier mobilities and concentrations.

For a non-doped or intrinsic semiconductor, the electron and hole concentrations are equal and are given by the intrinsic carrier concentration (n_i) which is approximately 10^{10} and 5×10^{-9} cm^{-3} for silicon and 4H-SiC respectively. By doping regions of semiconducting materials, the carrier concentration of either electrons or holes can be increased. Assuming all dopants are ionised, the resistivity of a p-type and n-type semiconductor can be expressed as

$$\rho_p = \frac{1}{pq\mu_h} \approx \frac{1}{N_A q\mu_h} \tag{2.12a}$$

$$\rho_n = \frac{1}{nq\mu_e} \approx \frac{1}{N_D q\mu_e} \tag{2.12b}$$

where N_A and N_D are the acceptor and donor concentrations. It can be seen that the resistance of these regions is inversely proportional to the doping concentrations, but as shown in figure 2.14 and 2.15, the mobility can be maximised by minimising the doping concentration, and so a trade off is generated between the two. Studies into the resistivity of semiconducting

materials with different doping densities from near intrinsic up to 10^{17} cm^{-3} have shown that a decrease in a doping concentration by an order of magnitude only results in an increase in carrier mobility by a factor of 2-5 [25, 26, 93] and this can also be observed in figures 2.14 and 2.15. As such, it is common for manufacturers to heavily dope the semiconductors at contact regions to minimise contact region losses.

Maximum doping concentration and minimum breakdown voltage

In order for a semiconducting material to be suitable for fabricating a power electronic device, a PN diode fabricated from the material must be capable of blocking the supply voltage in reverse bias. In reverse bias, a depletion width is formed at the PN junction of a power electronic device equal to

$$W_D = \sqrt{\frac{2\varepsilon(V_{bi} - V_a)}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{2.13}$$

where $\varepsilon = \varepsilon_r\varepsilon_0$ is the permittivity, V_{bi} is the built-in potential and V_a is the applied bias. The field generated within the semiconductor is then given by

$$F = \frac{2(-V_a)}{W_D} \tag{2.14}$$

when the applied voltage is in reverse. As the applied voltage increases, the electric field increases within the device. As the electric field increases, carriers generated within the PN depletion region are forced apart due to the high electric field. If the carriers have enough kinetic energy, they are capable of ionising other carriers before exiting the depletion region leading to an avalanche effect resulting in breakdown and an exponential increase in reverse current. The voltage at which breakdown occurs is given by

$$V_B = \frac{F_M W_D}{2} \tag{2.15}$$

where F_M is the breakdown field of the material. Assuming a one-sided abrupt junction, the breakdown voltage for an abrupt PN junction is then given by

$$V_B = \frac{\varepsilon F_M^2}{2qN} \tag{2.16}$$

where N is the doping concentration of the lightly doped region. The breakdown voltage for power applications is thus dependent on the ratio of the square of the breakdown field to the doping concentration. The breakdown field and resulting breakdown voltage as a function of doping concentration for germanium, silicon, GaAs, 4H-SiC and GaN can be seen in figure 2.16. The breakdown field for all semiconductors can be seen to increases gradually by a total factor of two to three times from near intrinsic to heavy doping concentrations. The breakdown voltage, however, can be seen to decrease near linearly with doping concentration. The breakdown voltage of germanium is the lowest in comparison to all other materials whilst the breakdown voltage for SiC and GaN is over a magnitude greater than all other semiconductors at all doping concentrations. As can be seen from the data, GaN and 4H-SiC are capable of having a breakdown voltage in excess of 1 kV for doping concentrations at
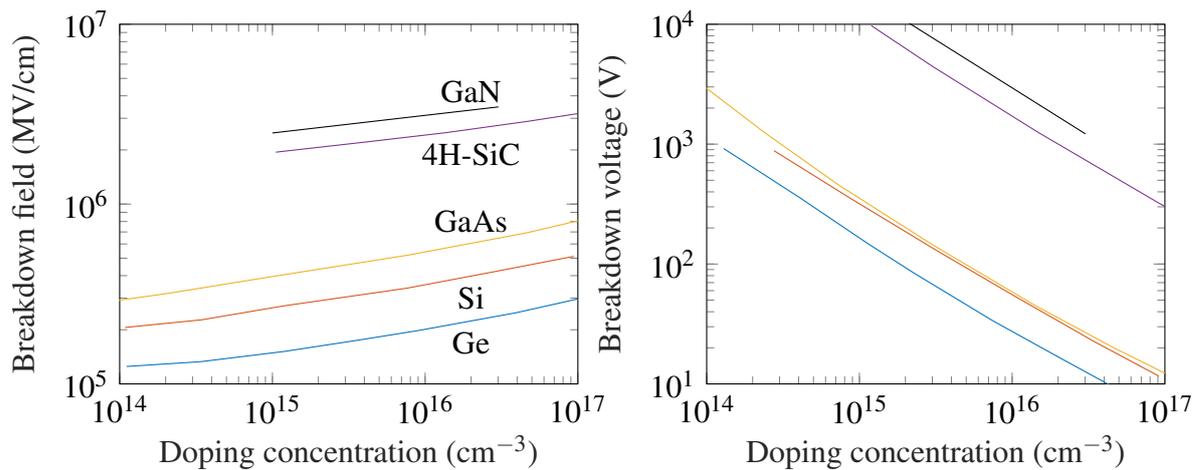
Fig. 2.16 Breakdown field (left) and resultant breakdown voltage (right) of Ge [104], Si [23], GaAs [104], 4H-SiC [105] and GaN [106]. Materials for coloured trends on left sub-figure match that of the right sub-figure.

10^{16} cm^{-3} whilst PN junctions fabricated from germanium, silicon and GaAs require doping concentrations well below 10^{15} cm^{-3} to achieve a breakdown voltage close to 1 kV.

2.5.3 Drift region resistance at low-temperature

The breakdown voltages illustrated in figure 2.16 assume that the depletion width is free to extend within the lightly doped drift region indefinitely. In order to allow for this, manufacturers must add a lightly doped drift region to the all power devices comprising of typically a lightly doped n-type region that can be seen for all vertical device structures shown in figures 2.3 and 2.13. In modelling the source of resistive losses within a power device, it has been shown that the inclusion of this lightly doped drift region contributes between 50% to over 90% of the total resistive losses within power devices [80, 107, 108].

For the majority of power electronic devices, as the temperature is reduced, the carrier mobility increases and the total on-state resistance of power electronic devices initially increases. As the temperature is reduced below 100 K however, materials such as silicon and SiC experience an exponential increase in resistivity whilst the same does not occur for germanium and GaAs devices until the temperature is reduced below 20 K.

A plot of the resistivity (or the conductivity which is the inverse of resistivity) can be seen in figure 2.17. As can be seen from the data, the conductivity of the silicon samples initially increases with decreasing temperature but begins to decrease rapidly for the majority of samples below 100 K. Below 40 K, the resistivity is two orders of magnitude greater than that of the room temperature values. In contrast, for germanium, the resistivity continues to decrease for the majority of samples down to 77 K and even as low as 20 K for the lightly doped samples. For the majority of samples, the resistivity at 20 K is better or close to the room temperature value.

For sample 58 in germanium and sample 140 in silicon, the doping concentration exceeds the degenerate limit and it can be seen that the resistivity remains essentially constant from

78 to 10 K. For degenerately doped semiconductors the concentration remains constant as dopants no longer require energy to be ionised [25]. For all other samples, below 100 K in silicon and below 20 K in germanium, the exponential increase in resistivity is due to the freezing out of carriers as the thermal energy of the system in no longer sufficient to ionise all dopants. The cause in the differing trends of resistivity with reducing temperature is due to
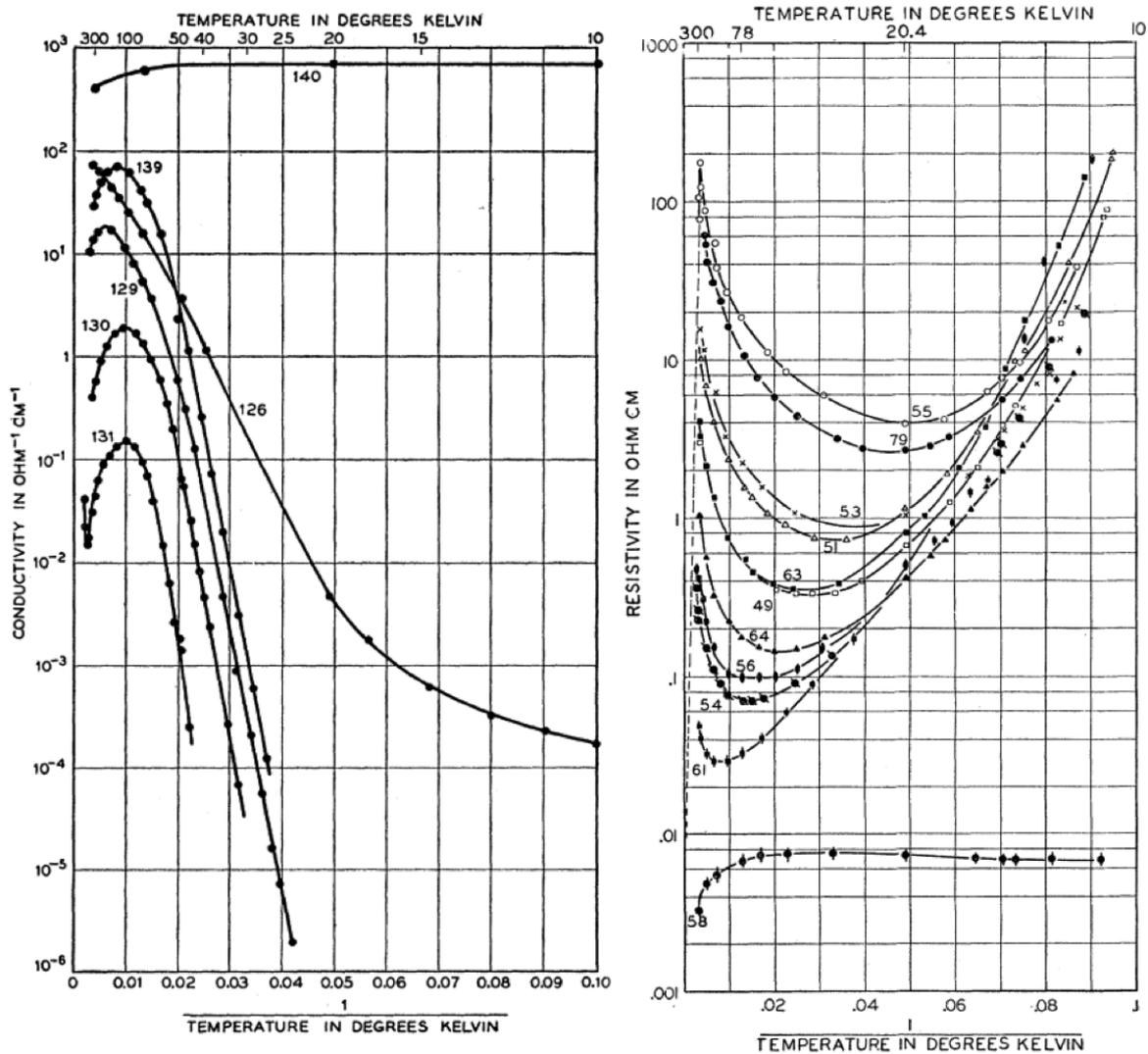
Fig. 2.17 Conductivity of n-type silicon (left) and resistivity of n-type germanium (right) [99, 25] for doping concentrations ranging from $<10^{14}$ to 10^{19} cm^{-3} in silicon and $<10^{14}$ to 5.5×10^{16} cm^{-3} in germanium. Doping concentrations are provided for each sample in the respective references based on sample number.

the material and dopant type dependence of the carrier freeze out effect. This effect is more prevalent in materials where dopants have higher ionisation energies such as SiC and GaN.

A plot of the measured carrier concentration in 4H-SiC and GaN can be seen in figure 2.18. For the higher doped samples in SiC, the room temperature carrier concentration is slightly less than the high-temperature carrier concentration. For highly doped samples above 10^{17} cm^{-3} in GaN, the carrier concentration becomes independent of temperature below 50 K which is the result of impurity conduction. Although a high carrier concentration that is temperature independent is favourable, doping concentrations of this magnitude result in ultra-low carrier mobilities and a low breakdown voltage.

Analysing data in literature, it can be seen that of all the materials considered here Germanium and GaAs are the only materials that retain low resistivities and high carrier mobilities at cryogenic temperatures near 20 K. Of these two materials, GaAs has sufficient issues involving a high wafer cost, extremely low hole mobility, and critically an inability to produce native oxides requiring deposition of oxides [111]. Reports on high quality MOSFETs fabricated from GaAs show issues with gate leakage resulting in low breakdown voltages and low on-off ratios [112, 113].
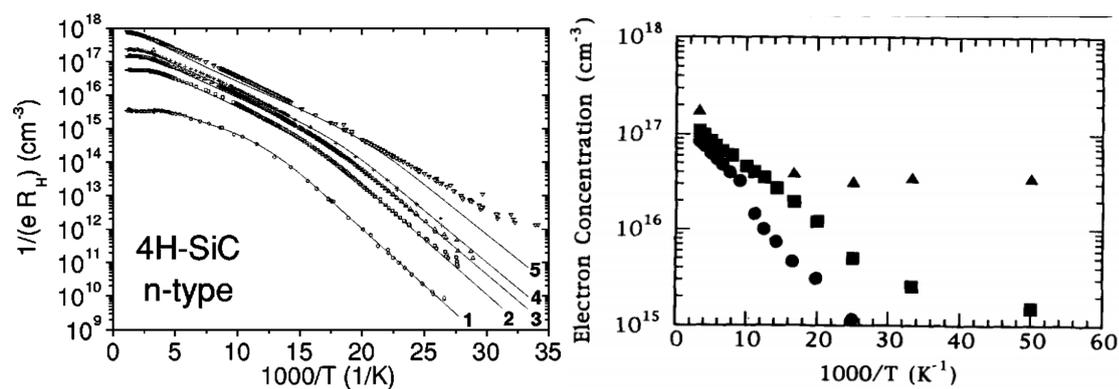
Fig. 2.18 Measured free carrier concentration in SiC (left) and GaN (right) as a function of temperature [109, 110]. Net doping concentrations range from N$_D$ - N$_A$ = 1.7×10^{15} to 3.8×10^{17} cm^{-3} for SiC and 8×10^{16} to 1.8×10^{17} cm^{-3} for GaN.

On the other hand, germanium has equally high carrier concentrations and mobilities at low temperatures and also boasts the ability to create a high quality native oxide to the interface through oxidation of the germanium surface [114, 115, 114]. As far as research has currently highlighted, the only issue with germanium is that of a low breakdown voltage that is essential for high power electronics. From this, it can be concluded that although germanium may not be able to provide power electronics for high voltage applications above 1 kV, it shows the potential to provide high current devices at the lower end of the voltage scale while still retaining an ultra low on-state resistance.

Thermal conductivity

In highlighting germanium as a superior candidate for low-temperature power electronics, the issue of thermal management must be analysed. As shown in figure 2.6, during device operation, the device temperature can exceed the ambient room temperature by more than 100 K if there is poor thermal management. From the transient data, it can be seen that the silicon devices reached a higher temperature than that of the SiC devices and whilst this may be simply due to excess resistive losses in the IGBT, it is also due to the thermal conductivity of the materials used.

The thermal conductivity of a material is a measure of the materials ability to transfer heat. If the thermal conductivity is high, then a material can cool down quickly after being heated up in contrast to materials with a low thermal conductivity. At room temperature, the thermal conductivity of germanium (0.58 W/cmK [116]) is on par with that of GaAs (0.55 W/cmK [117]) but is low in comparison to silicon, 4H-SiC and GaN (1.3, 3.7 and 1.3 W/cmK respectively [116, 118, 119]) but all increase with reducing temperature.

The thermal conductivity of semiconductors is dependant on the conductivity of phonons within the material [121]. Phonons are akin to electrons and holes within semiconductors although they transfer thermal energy as opposed to electrical charge. By eliminating material

defects and impurities, the thermal conductivity of the material can be increased. A plot of the thermal conductivity of germanium and GaN can be seen in figure 2.19 as a function of temperature. At high temperatures, the main scattering mechanism is that of the Umklapp process that is inversely proportional to temperature and so by reducing the temperature, the thermal conductivity of the material increases. At sufficiently low temperatures however, the thermal conductivity begins to decrease due to a reduction in the thermal capacity of the material [121, 117]. Aside from these two processes however, the thermal conductivity at any temperature is reduced following any fabrication process that leads to a dislocation or an increased impurity concentration as highlighted by the data for GaN.

For power electronic devices, the majority of the heat will be generated in the lightly doped drift region and so it is the thermal conductivity of this region that is key in maintaining a low device temperature in operation. Comparing the lightly doped germanium data with the doped GaN data (labelled 2 in figure 2.19), it can be seen that the thermal conductivity near 20 K is ~13 W/cmK for germanium and ~3 W/cmK for GaN. Silicon and GaAs are also found to have similar thermal conductivities at 20 K to that of germanium [116, 117]
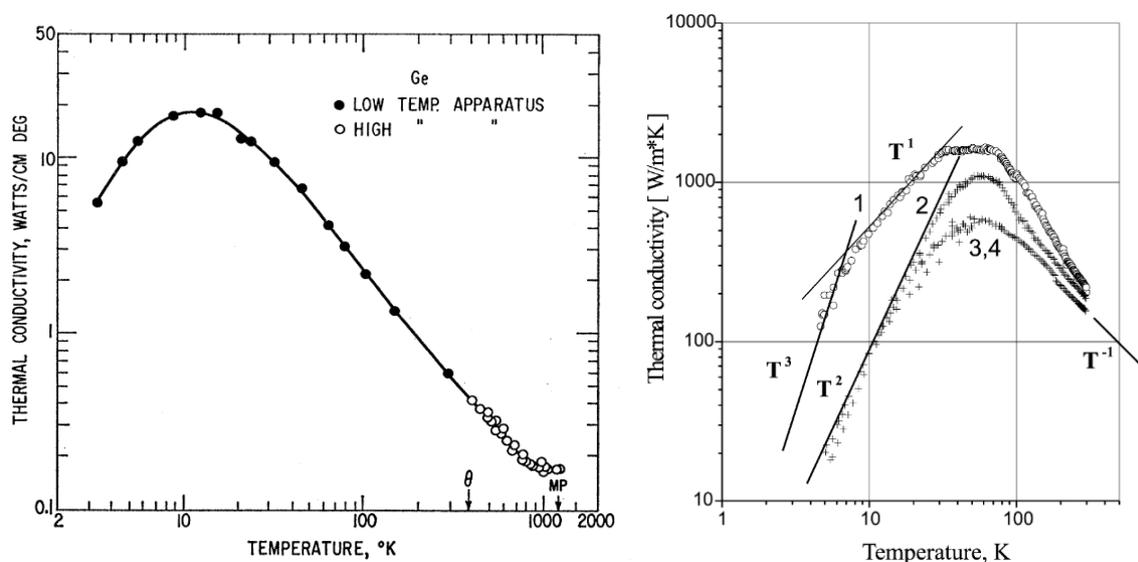
Fig. 2.19 Thermal conductivity in lightly doped germanium (left) and pure and lightly doped GaN (right) [116, 120].

whilst 4H-SiC is found to reduce with temperature below 100 K resulting in a low thermal conductivity of $\sim$0.9 W/cmK at 20 K [118].

2.6 Germanium lateral MOSFETs

As a potential replacement for silicon in CMOS applications owing to it's superior electron and hole mobilities, almost all of the published literature on fabricated germanium MOS devices has been that of a lateral structure with long channels and a heavily doped source and drain [122–124]. The key issues that have prevented the integration of germanium MOSFETs into CMOS technology is the quality and longevity of the oxide. Like silicon, germanium has a native oxide [125] that can be easily fabricated through wet or dry oxidation of the germanium surface [126, 127]. Unlike SiO_2 however, GeO_2 is water soluble resulting in difficulty in fabrication and also requires passivation to protect the device from moisture within the air.

Recent developments in germanium MOS technology however, have been promising resulting in germanium p-type and n-type MOSFETs with carrier mobilities that exceed that of silicon [128, 129]. As well as this, in efforts to increase the current density of the devices, high-κ dielectrics that incorporate alternative oxides such as Al_2O_3 and HfO_2 have shown that the native oxide can be successfully encapsulated while also providing a much higher oxide capacitance [130–132]. As such, the use of germanium in MOS technology is far more suitable for emerging applications in comparison to years ago than previously thought.

2.6.1 Channel resistance

As the second greatest contributor to overall power device resistance, the resistance of the channel region at the semiconductor/oxide interface within power MOSFETs must also be considered [133, 107]. At low drain biases for a long channel device, the drain current of a

lateral MOSFET is given by

$$I_D = \frac{W}{L} \mu_e C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D \qquad (2.17)$$

where W/L is the width to length ratio of the gate, C_{ox} is the oxide capacitance and V_G, V_D and V_T are the gate, drain and threshold voltage respectively. For high drain biases, where the drain current saturates due to pinch off in the channel, the saturation drain current is given by

$$I_{D,sat} = \frac{W}{L} \mu_e \frac{C_{ox}}{2} (V_G - V_T)^2 \qquad (2.18)$$

and remains independent of the gate bias assuming that the channel length is greater than 1 μm [134, 135]. From equations (2.17) and (2.18), it can be seen that the drain current is proportional to the mobility and oxide capacitance of the device and so by maximising their product the optimal channel resistance can be achieved.

When transistors are in the on-state, the majority of carriers are confined to within 5-10 nm of the oxide/semiconductor interface [136, 137] and so the effective area of the channel is extremely thin in comparison to the depth of the p-type region. As well as a reduced effective area, the mobility of the carriers within the channel is reduced due to increased scattering from the surface roughness of the oxide/semiconductor interface, trapped charge at the interface and remote phonons originating from the oxide [138, 139]. As such, a lot of attention has been focused on maximising the mobility of carriers within the channel whilst also maximising the oxide capacitance [130, 140].

Of the two parameters, it has been found that the carrier mobility can be increased through fabrication optimisation but the key parameter is that of the oxide capacitance. The oxide capacitance for a lateral MOSFET is given by

$$C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} \qquad (2.19)$$

where ε_{ox} is the oxide permittivity and t_{ox} is the oxide thickness. For ultrathin oxides, current leakage from the gate contact becomes a significant issue if the oxide thickness drops below 1 nm [145, 146]. In an attempt to combat the leakage current density through the gate oxides, alternative gate oxides with higher dielectric constants have been used that offer a thicker oxide while maintaining an equivalent SiO$_2$ oxide capacitance [147]. The effective oxide thickness through using alternative high-κ materials is given by

$$\text{EOT} = t_{ox} \frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,high-\kappa}} \tag{2.20}$$

where ε_{r,SiO_2} is the relative dielectric constant of SiO$_2$ (3.9) and $\varepsilon_{r,high-\kappa}$ is the relative dielectric constant of the alternative high-κ material.

An example of the published leakage current density within germanium MOS capacitors as a function of effective oxide thickness can be seen in figure 2.20. As can be seen from the data, the reduction in the effective oxide thickness of all gate dielectrics leads to an exponential increase in leakage current density through the oxide. Comparing the materials
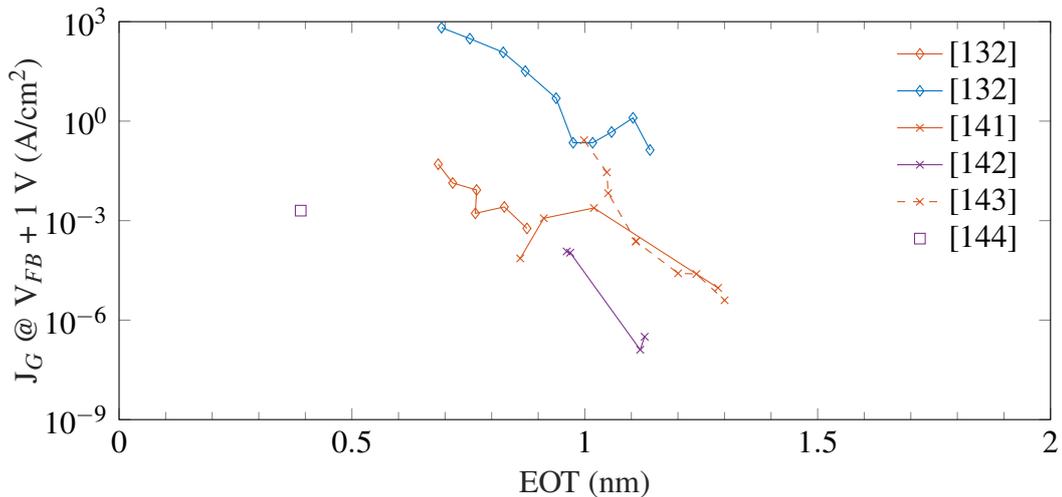
Fig. 2.20 Comparison of leakage current density of germanium MOS capacitors where the GeO$_2$ interlayer has been formed using Pre high-κ O$_2$ plasma (x), post high-κ O$_2$ oxidation ($\diamond$) and Pre high-κ rapid thermal oxidation ($\square$). high-κ dielectrics used for germanium MOS capacitors include Al$_2$O$_3$ (Blue), Al$_2$O$_3$/HfO$_2$ (Orange), and ZrO$_2$ (purple).

directly, it can be seen that the leakage current density of the ZrO_2 dielectrics is much lower than that of Al_2O_3 and HfO_2 oxide or stacks incorporating Al_2O_3 and HfO_2.

In order for complete control of the gate switching of the device, the leakage through the gate must be minimised. From the results, it can be seen that ZrO_2 with a dielectric constant of 17-45 [148–150] provides the minimum leakage current density in comparison to Al_2O_3 and HfO_2 devices. There is very little literature available for devices fabricated using ZrO_2 in recent years due to the familiarity of Al_2O_3 and HfO_2 and so here we explore the feasibility of fabricating high quality ZrO_2 through the thermal oxidation of germanium.

2.7 Conclusion

Following this review of power electronic devices at cryogenic temperatures, despite the initial increase in conductivity of silicon and GaN below room temperature, the exponential increase in device resistance fabricated from these materials at temperatures below 77 K warrants them unsuitable for emerging liquid hydrogen applications. It can be seen that, despite the superior characteristics at room and higher temperatures, the resistance of 4H-SiC devices increases with decreasing temperature at all temperatures below 300 K. Silicon and GaN power electronic devices do show improvement below 100 K but this is only true for MOS and HEMT based devices. Excluding HEMT devices due to longevity issues and high fabrication costs, the unipolar vertical power MOSFET is the most suitable device for power electronic applications. Of all the power devices, it has been shown that the resistance of the lightly doped drift region is the single greatest source of resistive losses in power devices due to the length and low doping concentration. In order to minimise the resistive losses owing to this region, a semiconducting material with a high carrier mobility should be chosen. Of the materials readily available for commercial use, germanium appears to be the most suitable due to an extremely high carrier mobility at 20 K of over 10^6 cm^2/Vs which far exceeds the bulk carrier mobilities of silicon, 4H-SiC and GaN at the same temperature. Recent

developments in germanium MOS technology also show promise for incorporating high-κ gate dielectrics to maximise the current density within germanium devices while retaining a simple fabrication approach that can be readily be achieved using an atomic layer deposition (ALD) or thermal oxidation approach.

As such, germanium appears as a promising candidate for low resistance, fast switching, power electronics for liquid hydrogen applications. Despite this, a significant lack of experimental or modelling work on the physical properties of germanium have prevented a conclusive study on the viability of germanium power electronics at low temperatures. In order to correct for this, the experimental data reported for germanium must be analysed and modelled in order to allow for a device simulation of a high power vertical germanium MOSFET at 20 K.

Chapter 3

Modelling the Cryogenic Properties of Germanium for Device Simulation

3.1   Introduction

The choice of semiconducting material for power devices critically depends on the intended application. For low power applications, such as logic devices, manufacturers are primarily focused on maximising the operating frequency of a device, which is dependent on the rate of charge transfer through a material. For high power applications, such as the control of driving an electrical actuator, the conductivity and carrier lifetimes are the key parameters which must also be considered when determining the suitability of a material for devices.

In cryogenic environments, the physical properties of semiconducting materials vary greatly from their room temperature values. Despite the maturity and development of commercially available silicon and more recently SiC and GaN, electrical characterisation at cryogenic temperatures below 100 K shows that devices fabricated from these materials are unsuitable for cryogenic applications due to the exponential increase in the resistance of these devices. Unlike silicon, SiC and GaN, semiconducting germanium does not experience the same increase in resistance until the temperature is reduced below 20 K and devices

fabricated from germanium have even been shown to function at 4.2 K with similar electrical characteristics to that at room temperature.

Despite this benefit, the electrical properties of germanium and germanium devices have yet to be modelled and the only benchmark for considering germanium devices for applications is by analysing characteristics from literature. As such, this chapter will focus on modelling the physical characteristics of germanium from literature and analysing the impact of its properties including carrier mobility, velocity saturation, free carrier concentration and minority carrier lifetime.

3.2   Closed-loop analytical model

The closed-loop analytical model which is developed in this chapter is based on the determination of the total carrier concentration and carrier mobility for a range of dopant concentrations that are relevant to power electronic devices over a range of temperatures. The total current density J through a semiconducting material can be expressed as

$$J = \sigma F \tag{3.1}$$

where F is the applied electric field and σ is the conductivity. The conductivity is related to the free carrier concentration and carrier mobility according to

$$\sigma = nq\mu_e + pq\mu_h \tag{3.2}$$

In certain regions of semiconductor devices, the concentration of electrons may be many orders of magnitudes greater than the concentration of holes or vice versa. In such instances,

the conductivity can be approximated to

$$\sigma_n = nq\mu_e|_{n>p} \tag{3.3a}$$

$$\sigma_p = pq\mu_h|_{p>n} \tag{3.3b}$$

for n-type and p-type material respectively.

For unipolar devices such as junction field effect transistors (JFETs) and MOSFETs, the total current given by equation 3.1 can be calculated using the conductivity given by either equation 3.3a or 3.3b as only electrons or holes contribute to the total current density for unipolar n-type or p-type FETs. As such, the temperature, doping and field dependence of electrons and holes will be considered independently when modelling experimental results for unipolar devices. For bipolar devices such as PiN diodes and IGBTs, the total current of the devices is dependent on the sum of the electron and hole currents and so both equation 3.3a and 3.3b must be combined. For these devices, it is the conductivity of the minority carrier concentration which dominates the overall device conductivity and so generation and recombination effects must be taken into consideration when simulating device behaviour.

3.3 Carrier concentration

At temperatures above absolute zero, the concentration of free carriers that are available for conduction is given by [151]

$$n(T) = \int_{E_C}^{\infty} N(E) f(E, T) dE \tag{3.4}$$

where T is the absolute temperature, $N(E)$ is the density of states and $f(E,T)$ is the Fermi-Dirac occupational probability which is given by

$$f(E,T) = \frac{1}{1 + \exp\left(\frac{E-E_F}{k_BT}\right)} \tag{3.5}$$

where E is the energy, E_F is the Fermi energy and k_B is Boltzmann's constant. The Fermi-Dirac occupational probability describes the probability of an energy level being occupied by an electron. At the energy denoted by E_F, the probability of occupation is 50%. For cryogenic applications, where the free carrier density is low as a result of the temperature, the parabolic-band approximation can be applied [152] as the majority of carriers are located at the conduction band edge. As such, the density of states is given by

$$N(E) = M_C \frac{\sqrt{2}}{\pi^2} \frac{m_{de}^{1.5}(E-E_C)^{0.5}}{\hbar^3} \tag{3.6}$$

where M_C is the number of equivalent minima in the conduction band, m_{de} is the electron density of states effective mass, E_C is the energy of the conduction band edge and $\hbar = h/2\pi$ is the reduced Planck's constant.

Through the use of the parabolic band approximation, the total carrier concentration can be expressed as

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_C}{k_BT}\right) \tag{3.7}$$

where N_C is the density of states in the conduction band given by

$$N_C = 2\left(\frac{2\pi m_{de}k_BT}{h^2}\right)^{3/2} M_C \tag{3.8}$$

$F_{1/2}$ is the Fermi-Dirac integral of order $\frac{1}{2}$ which is given by

$$F_{1/2}(\eta) = \int_0^\infty \frac{\alpha^{1/2}}{1 + \exp(\alpha - \eta)} d\alpha \tag{3.9}$$

where in η is the reduced Fermi-energy equal to $(E_F - E_C)/k_B T$ and α is $(E - E_C)/k_B T$. No closed-loop solutions of equation (3.9) exist and a closed-loop approximation can only be generated when the Fermi energy in a semiconductor is several $k_B T$ below the conduction band edge. In such instances, Fermi-Dirac integral of order $\frac{1}{2}$ can be approximated to an exponential of the form

$$F_{1/2}(\eta) = \frac{\sqrt{\pi}}{2}\exp(\eta) \tag{3.10}$$

and so equation (3.7) can be expressed as

$$n = N_C \exp\left(-\frac{E_C - E_F}{k_B T}\right) \tag{3.11}$$

The hole concentration in a semiconductor can be described in a similar manner with

$$p(T) = \int_{\infty}^{E_V} N(E)\left(1 - f(E,T)\right)dE \tag{3.12}$$

where E_V is the valence band energy and the term $(1 - f(E,T))$ is the probability of the energy level E being occupied by a hole. Solving equation (3.12) using the same Boltzmann approximation leads to

$$p = N_V \exp\left(-\frac{E_F - E_V}{k_B T}\right) \tag{3.13}$$

where N_V is the density of states in the valence band given by

$$N_V = 2\left(\frac{2\pi m_{dh} k_B T}{h^2}\right)^{3/2} \tag{3.14}$$

where m_{dh} is the density of states effective mass of the valence band.

At cryogenic temperatures, the functionality of devices crucially depends on the concentration of extrinsic carriers that are available for conduction. Doping a semiconductor with an impurity atom produces an energy level within the band gap of the material from which carriers can be excited from or decay to. For impurities such as antimony or arsenic in

germanium, the donor energy E_D is a single energy level below the conduction band and the concentration of electrons at the energy level is

$$n = N(E_D)f(E_D,T) \tag{3.15}$$

For a single donor level, the density of states at the energy E_D is equal to the doping concentration and the carrier concentration at the donor level is given by

$$n = N_D \frac{1}{1 + g_D^{-1} \exp\left(\frac{E_D - E_F}{k_B T}\right)} \tag{3.16}$$

where g_D is the electron degeneracy factor of the donor energy level given by E_D. The concentration of ionised donors is therefore given by

$$n(E_D) = N(E_D)(1 - f(E_D,T)) \tag{3.17}$$

which is equal to

$$N_D^+ = N_D \frac{1}{1 + g_D \exp\left(-\frac{E_D - E_F}{k_B T}\right)} \tag{3.18}$$

At cryogenic temperatures where the intrinsic carrier concentration is negligible in comparison to the donor concentration, it can be assumed that the free electron and ionised donor concentrations given by equations (3.11) and (3.18) are equal. By equating these two expressions, the Fermi-level can algebraically be expressed as

$$\exp\left(\frac{E_F}{k_B T}\right) = \frac{-1 + \sqrt{1 + 4\frac{N_D}{N_C}g_D \exp\left(\frac{E_C - E_D}{k_B T}\right)}}{2g_D \exp\left(\frac{-E_D}{k_B T}\right)} \tag{3.19}$$

Substituting this expression for the Fermi-energy into equation (3.11) gives a Fermi-energy independent electron concentration equal to

$$n = \frac{N_C \left(\sqrt{1 + 4\frac{N_D}{N_C} g_D \exp\left(\frac{\Delta E_D}{k_B T}\right)} - 1 \right)}{2 g_D \exp\left(\frac{\Delta E_D}{k_B T}\right)}$$

(3.20)

where ΔE_D is the difference between the conduction band minimum and donor energy level. For the free hole concentration, the same treatment results in

$$p = \frac{N_V \left(\sqrt{1 + 4\frac{N_A}{N_V} g_A \exp\left(\frac{\Delta E_A}{k_B T}\right)} - 1 \right)}{2 g_A \exp\left(\frac{\Delta E_A}{k_B T}\right)}$$

(3.21)

where ΔE_A is the difference between the acceptor energy level and the valence band and g_A is the hole degeneracy factor.

At temperatures where the thermal energy is lower than the energy required to ionise an electron from the donor energy level to the conduction band, the free electron concentration exponentially decreases and can be approximated by

$$n = \sqrt{\frac{N_D N_C}{g_D}} \exp\left(-\frac{\Delta E_D}{2 k_B T}\right)$$

(3.22)

A plot of $\log(n)$ against $1/T$ results in a linear freeze-out region with a gradient equal to $E_D/2$. Knowing this, it is possible to extract the ionisation energy of impurities in the semiconductor which was used to obtain an ionisation energy of 12.5 meV for antimony in germanium.

In the instance that multiple impurity atoms are present within the semiconductor, it is possible for the carrier concentration to be equal to the sum of all ionised impurities present within the material. If the semiconductor contains impurities with different ionisation energies, equation (3.18) must be modified to take into consideration the presence of multiple

impurity atoms. Doing so results in the transcendental equation

$$N_C \exp\left(-\frac{E_C - E_F}{k_B T}\right) = \sum_x \frac{N_{D,x}}{1 + g_D \exp\left(-\frac{E_{D,x} - E_F}{k_B T}\right)} \tag{3.23}$$

where x is equal to the number of donor levels and $N_{D,x}$ and $E_{D,x}$ represent the concentration and energy level of impurity x. In the presence of multiple energy levels, the Fermi energy must be solved numerically using equation (3.23) and the carrier concentration can be calculated via substitution of E_F into equation (3.11). Commonly used dopants such as antimony for n-type germanium and boron for p-type germanium have a single shallow ionisation energy close to the conduction and valence band edge respectively, and so the approximation for the carrier concentration given by equation (3.20) can be used. In regions close to contacts, or oxide/semiconductor interfaces, the presence of oxygen, or metallic impurities such as chromium, gold, or silver can introduce multiple ionisation energies within the band gap and so the calculation of the carrier concentration must be completed through solving for E_F using equation (3.23).

3.3.1   Model comparison to experimental measurements

At cryogenic temperatures, the primary cause of device failure is related to the reduction of thermal energy in the system, resulting in a reduction in the number of ionised donors. An example of the ionised dopant concentration for germanium, silicon and 4H-SiC is plotted in figure 3.1. From the figure, it can be seen that the total ionised dopant concentration tends towards equation (3.22) (in the temperature range where the thermal energy becomes insufficient to ionise all dopants). The rate of decay is inversely proportional to the ionisation energy which is high for 4H-SiC and low for germanium. As such, although nitrogen in 4H-SiC has a high ionisation energy in comparison to antimony in germanium, the reduction of ionised donors can be seen to decrease gradually in comparison.
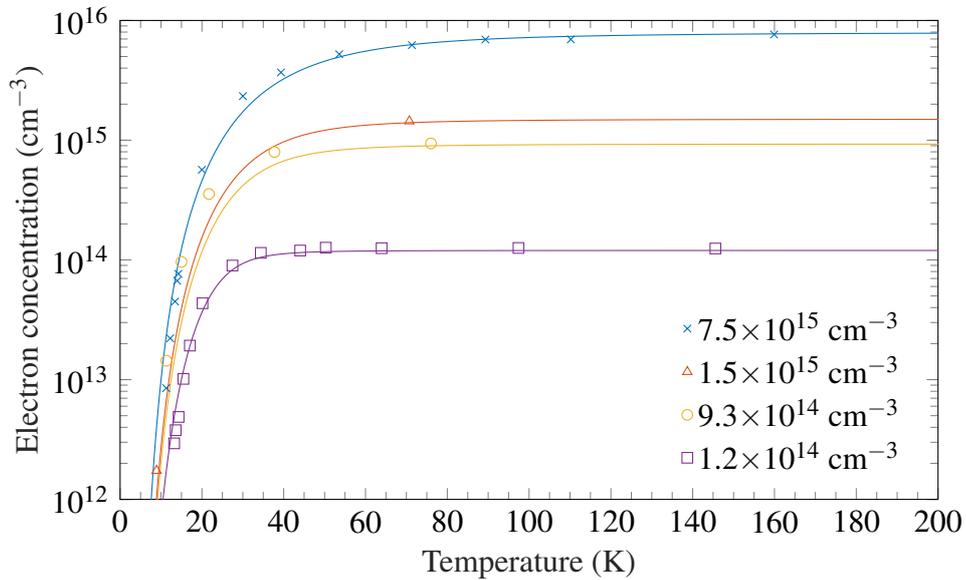
(a) Calculated electron concentration for different net acceptor concentrations compared to experimental data [25, 153].
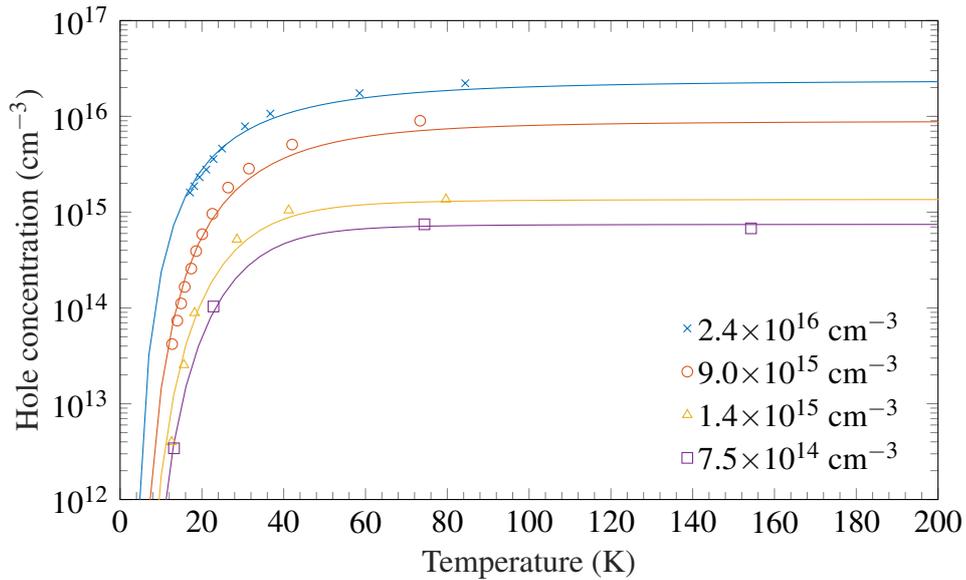
(b) Calculated hole concentration for different net acceptor concentrations compared to experimental data [154]

Fig. 3.1 Comparison of the free electron and hole concentration models to experimental data in n-type (a) and p-type (b) germanium using equations (3.25) and (3.26) in equations (3.20) and (3.21) with density of states effective masses of 0.22 and 0.34 for electrons and holes respectively.

At doping concentrations greater than 10^{16} cm^{-3}, an impurity band centred at the donor energy begins to form which results in a reduction of the ionisation effective energy [155, 25]. For silicon and 4H-SiC [155, 98, 156, 157], the effective ionisation energy for both acceptors and donors energy can be modelled using

$$E_{\text{A/D,eff}} = E_{\text{A/D,0}} - \alpha N_{\text{net}}^{1/3} \tag{3.24}$$

where $E_{\text{A/D,0}}$ is the ionisation energy for acceptors/donors at low doping concentrations, α is a fitting constant and N_{net} is the sum of the acceptor and doping concentration [155]. Based on fitting the electron concentration to experimental data, Eq. (3.26) overestimates the reduction in ionisation energy and the ionisation energy of antimony doped Ge was found to follow a quadratic nature of the form

$$E_{\text{D,app}} = E_{\text{D,0}} - 1.22 \times 10^{-19} N_{\text{net}} + 2.99 \times 10^{-37} N_{\text{net}}^2 \tag{3.25}$$

where N_{net} is the difference in the majority dopant concentration and the minority dopant concentration. Similarly, for gallium in p-type germanium, we find the acceptor ionisation energy followed the form

$$E_{\text{A,app}} = E_{\text{A,0}} - 5.65 \times 10^{-19} N_{\text{net}} + 9.12 \times 10^{-36} N_{\text{net}}^2 \tag{3.26}$$

For doping concentrations exceeding 10^{17} cm^{-3}, the ionisation energy reduces to zero as the donor/acceptor impurity band overlaps with the conduction/valence band edge and so the carriers no longer require excitation to become available for conduction. For such a case, the semiconductor can be assumed to be fully ionised.

For cryogenic applications, the intrinsic carrier concentration is negligible and the free carrier concentration can be modelled accurately using equations (3.20), (3.21) and (3.25).

For semiconductors with a dopant concentration exceeding 10^{19} cm^{-3}, the Fermi energy level is located inside the conduction/valence band and all the dopant ionisation energies $E_{D/A}$ tend towards zero. This results in a semiconductor with a carrier concentration that remains constant at cryogenic temperatures. Assuming the intrinsic carrier concentration is negligible, the temperature dependence of the resistance of these materials reduces significantly, as the only temperature-dependent term in equation (3.2) is the electron and hole mobilities. As will be described in the forthcoming section, a dopant concentration of the order of 10^{19} cm^{-3} results in a material with a very low temperature dependence as all dopants remain ionised at all temperatures and scattering from neutral impurities dominates the overall mobility. Whilst a heavily doped semiconductor exhibits a very similar conductivity at cryogenic temperatures compared to room temperature, power electronic devices cannot be fabricated solely from regions with such doping concentrations and so devices must be fabricated with regions of varying doping concentrations.

3.3.2   Effect of unintentional impurities

Although high doping concentrations reduce the resistance of power electronic devices, power electronic devices require regions of low doping concentrations ($\approx 10^{14}$ cm^{-3}) in order to ensure a high breakdown voltage and maximise device switching frequency. During the fabrication process, unintentional impurities such as oxygen and carbon can diffuse into the semiconductor generating a concentration of compensating impurities which act as traps for carriers. The effect of compensating acceptor impurities can be neglected assuming $10N_A < N_D$ but in other cases, a high acceptor concentration can reduce the overall electron concentration and the rate of carrier freeze-out with decreasing temperature. The effect of impurity compensation can be seen in figure 3.2b.

Using the model given by equation (3.20) and assuming a negligible acceptor concentration, the freeze-out regions can be corrected for by altering the ionisation energies. By
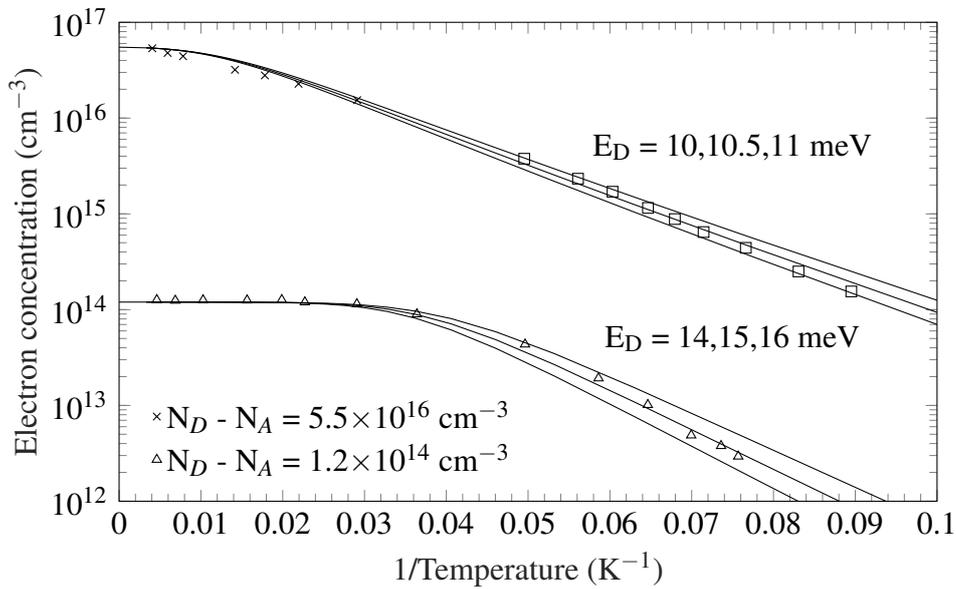
(a) Comparison of uncompensated model for different ionisation energies where the increasing ionisation energy reduces carrier concentration at low temperatures
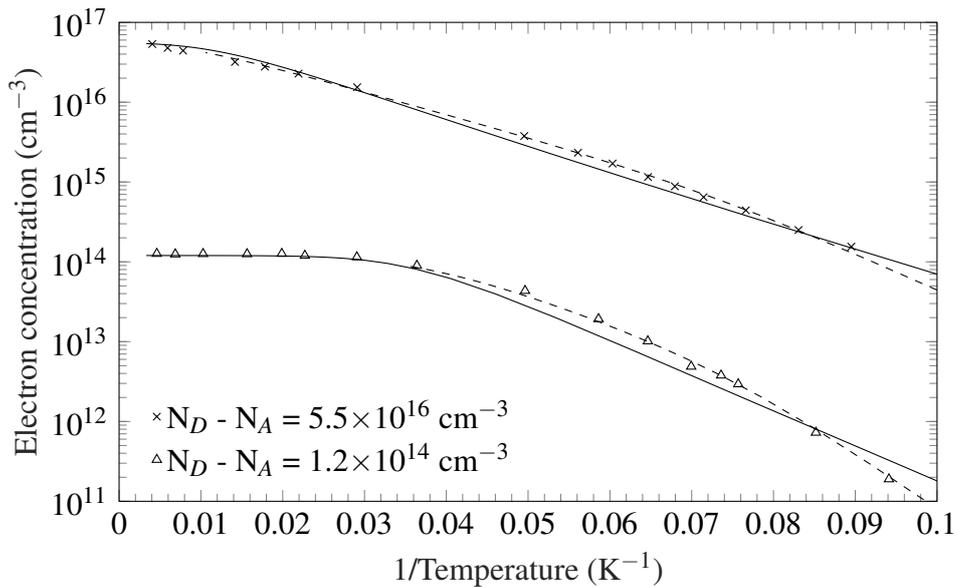
(b) Comparison of uncompensated model (solid) to compensated extrinsic model (dashed)

Fig. 3.2 Richardson plot of carrier concentration in floatzone grown germanium of low and moderate doping concentrations [25].

comparing the samples, it can be seen that samples with higher doping concentrations are

less affected by the presence of compensating carriers. The error in the freeze-out rate of

the sample with a net doping concentration of 5.5×10^{16} cm^{-3} can be corrected by assuming

the ionisation varies from 10 to 11 meV as the temperature decreases. For the lightly doped sample however, the variation in ionisation is larger rising from 14 to 16 meV.

In order to accurately model the carrier concentration for doping concentrations with compensation ratios greater than 10%, in the carrier freeze-out region, the carrier concentration must be related to the temperature through

$$\frac{n(N_A + n)}{N_D - N_A - n} = \frac{N_C}{g_D} \exp\left(-\frac{\Delta E_D}{k_B T}\right) \tag{3.27}$$

from which, the carrier concentration can be solved numerically using the acceptor concentration and the density of states effective mass as a fitting parameter. Using a density of states effective mass of $m_{de} = 0.3 m_0$ gives an acceptor concentration of 1×10^{13} cm^{-3} and 1.3×10^{14} cm^{-3} which correspond to compensation ratios of $N_D/N_A \approx 0.1$ for both samples.

It can be seen that the presence of compensating acceptor impurities results in a carrier freeze-out temperature slope that deviates from that predicted from equation (3.20). In the case where N_A is negligible in comparison to both n and N_D, the expression for the carrier concentration in equation (3.27) collapses to equation (3.22).

3.3.3 Degeneracy

The models for the carrier concentration given by equations (3.11), (3.20) and (3.27) assume that the application of Boltzmann statistics is suitable for simulating device behaviour. Boltzmann statistics apply in the assumption that Fermi energy within the band gap is at least several $k_B T$ below the conduction or above the valence band edge, from which, the Fermi-Dirac integral can be approximated by equation (3.10) as shown in figure 3.3a. If the doping concentration is great enough, or if the temperature is low enough, this approximation no longer holds and the carrier concentration will deviate from equation (3.11). In such an instance, the carrier concentration must be calculated numerically by solving equation (3.9)
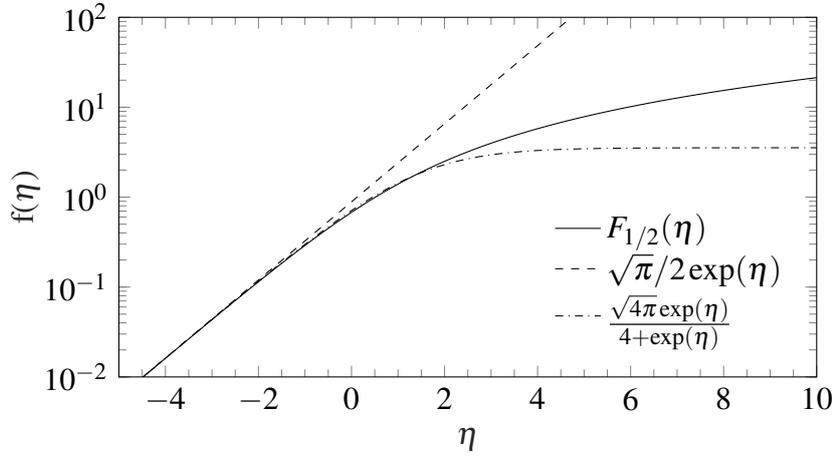
(a) Approximations of $F_{1/2}(\eta)$ using Boltzmann statistics (dashed) and more accurate model proposed by Ehrenberg (dash-dot) [158]
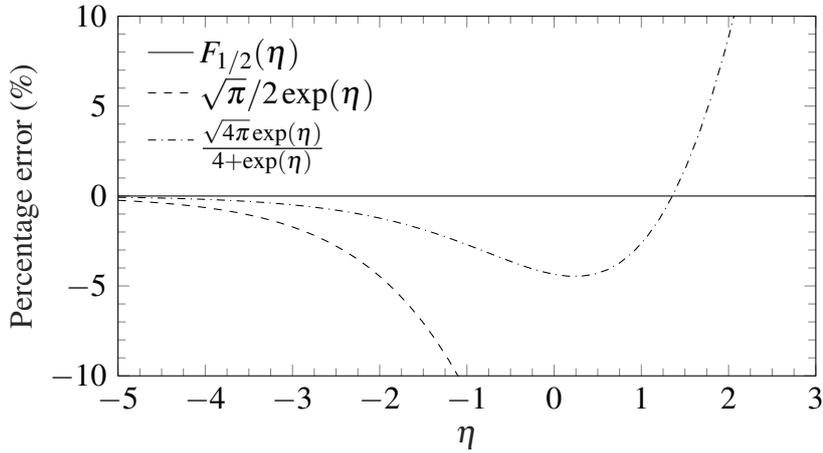
(b) Percentage error of Fermi-Dirac integral approximations. Negative error indicates an overestimation of the integral and vice versa for a positive error

Fig. 3.3 Comparison of the full Fermi-Dirac integral in comparison to the models proposed by Boltzmann and Ehrenberg

and substituting into equation (3.7). Shockley [151] provided a 'degeneracy' temperature which is given by

$$T_{\mathrm{deg}} = \left(\frac{3}{\pi}\right)^{3/2} \frac{h^2}{8k_B m_{de}} n_{\mathrm{Deg}}^{2/3} \tag{3.28}$$

Re-arranging and solving for the degeneracy carrier concentration gives a value of 3×10^{18} cm^{-3} at room temperature and 2×10^{17} cm^{-3} at a temperature of 20 K for germanium. As these

concentrations are much greater than the doping concentrations used in power electronic drift regions, it is suitable to express the carrier concentration using Boltzmann statistics.

For gate regions and contact regions where ion implantation is used to achieve doping concentrations exceeding 10^{17} cm^{-3}, or at low temperatures, the error in using the Boltzmann statistics, or the resulting approximations, results in an error in the estimated carrier concentration as shown in figure 3.3b. In order to improve the temperature/doping range in which full numeric solution is not required, multiple attempts have been made to find a more generalised solution to the Fermi-Dirac integral [159, 160]. Most solutions require a series expansion or the inclusion of an extra term which reduces the error from the original term provided by the Boltzmann approximation, but using these expressions does not allow for a closed-loop expression for n or p. Of the proposed alternatives to the Boltzmann expression, Ehrenberg proposed that the Fermi-Dirac integral be approximated by

$$F_{1/2}(\eta) = \frac{\sqrt{4\pi}\exp(\eta)}{4+\exp(\eta)} \tag{3.29}$$

which provides a more accurate expression for the Fermi-Dirac integral as shown figure 3.3. Using this approximation for $F_{1/2}(\eta)$, the carrier concentration is given by

$$n = N_c\frac{4\exp(\eta)}{4+\exp(\eta)} \tag{3.30}$$

from which, following the same treatment in the calculation of (3.20), the Carrier concentration can be expressed as

$$n = N_C\frac{4\xi\exp\left(\frac{-\Delta E_D}{k_B T}\right)}{4+\xi\exp\left(\frac{-\Delta E_D}{k_B T}\right)} \tag{3.31}$$

where

$$\xi = \frac{N_D - 4N_C + \sqrt{(N_D - 4N_C)^2 + 64N_D N_C g_D \exp\left(\frac{\Delta E_D}{k_B T}\right)}}{8g_D N_C} \tag{3.32}$$

Using this form for calculating the carrier density increases the estimated carrier concentration at low temperatures for highly doped samples but still underestimates the carrier density by over an order of magnitude at cryogenic temperatures.

As the majority of power electronic devices have lightly doped regions for high breakdown voltages, the majority of the device can be modelled using equation (3.20). The use of equation (3.31) scarcely improves the accuracy of the carrier concentration. As a result of this, Fermi statistics must be applied, or it must be assumed that all carriers are ionised for regions where the carrier density is in excess of 10^{17} cm^{-3}.

3.4 Carrier mobility

The mobility of electrons and holes in semiconductors greatly differs from room temperature values at cryogenic temperatures. At cryogenic temperatures, there is a reduction of scattering from phonons which results in an increase in carrier mobility for lightly doped semiconductors. This reduction in scattering increases the mobility of carriers leading to an increase in conductivity and the maximum switching frequency of devices. Combined with the knowledge of the conductivity from equation (3.2), the importance of a high carrier mobility cannot be understated as this ensures a fast device with low resistive losses.

The mobility of carriers in a material with multiple scattering mechanisms can be calculated using Matthiessen's rule [161]

$$\frac{1}{\mu_{tot}} = \sum_{1}^{j} \frac{1}{\mu_1} + \frac{1}{\mu_2} + ... + \frac{1}{\mu_j} \tag{3.33}$$

where each μ_j represents a different mobility mechanism.

At room temperature, the dominant scattering for unintentionally doped germanium is that of lattice scattering from acoustic phonons which for non-polar semiconductors is given

by [162, 163]

$$\mu_{ac} = \frac{2\sqrt{2\pi}q\hbar^4 C_l}{3E_{ds}^2 m^{*5/2}(k_B T)^{3/2}} \tag{3.34}$$

where C_l is the longitudinal elastic constant and E_{ds} is the displacement of the band edge per unit dilation of the lattice which is induced by the acoustic phonon and m^* is the effective mass.

The scattering rate resulting from optical phonons becomes considerable for carriers with higher energy and can be approximated to [164]

$$\mu_{op} = \frac{\sqrt{2}q\hbar^3 C_l}{m^{*5/2}E_{op}^2 \omega_{op}} \left[\exp\left[\frac{\theta_{op}}{T}\right] - 1\right] \left[\sqrt{E + k_B\theta_{op}} + \exp\left[\frac{\theta_{op}}{T}\right]\sqrt{E - k_B\theta_{op}}\right]^{-1} \tag{3.35}$$

where E is the carrier energy, E_{op} is the optical phonon deformation potential, ω_{op} is the angular frequency of the optical phonons and θ_{op} is equivalent optical phonon temperature. Following work by Debye [25], it can be shown that the scattering of carriers due to optical phonons is greatest for carriers with energies close to $3k_B T$ and so an approximation of the optical phonon limited carrier mobility can be taken by assuming $E = 3k_B T$. Making this substitution for the carrier energy and performing a best fit between the model and the experimental data gives a value of 0.42 eV for the optical phonon deformation potential and is in agreement with previously published results in germanium [164].

For doped regions at cryogenic temperatures, the dominant scattering mechanisms are ionised and neutral impurity scattering. The potential generated by an ionised impurity generates a charged region which scatters carriers that come within its vicinity during conduction. The carrier mobility for ionised impurity dominated transport is given by [165]

$$\mu_{ii} = \frac{2^{7/2}\varepsilon^2(k_B T)^{3/2}}{\pi^{3/2}m^{*1/2}(n + 2N_A)Z^2 q^3} \left(\ln\left(1 + \frac{3\varepsilon k_B T}{n'^{1/3}q^2}\right)\right)^{-1} \tag{3.36}$$

where Z is the charge of the impurity atom in units of q, $n + 2N_A$ the concentration of ionised impurities and n' represents the ionised donor screening concentration given by

$$n' = n + \frac{(N_D - N_A - n)(n + N_D)}{N_D} \tag{3.37}$$

The $2N_A$ term in the total concentration of ionised impurities arises from the fact that, in a compensated material, electrons from an energy level of E_D will be trapped by a compensating energy level E_A. The transfer of an electron from a donor atom to an acceptor atom will leave both impurities ionised with an opposite net charge. It is assumed that the polarity of this charge does not affect the overall scattering rate and the total number of ionised impurities from this compensation will be equal to $2N_A$.

During the fabrication process, it is possible for small concentration of unintentional impurities such as oxygen and nitrogen to enter the lattice leading to a perturbation of the lattice periodicity. These impurities tend to remain uncharged as they require much larger ionisation energies. As well as unintentional impurities, at temperatures where carriers begin to freeze out, the resulting dopant atoms have a resultant neutral charge. Despite the neutral charge, the perturbation of the lattice scatters carriers that come into close proximity of the impurity. Commonly, the mobility of carriers limited by neutral impurity scattering is expressed using the model developed by Erginsoy [166, 167]

$$\mu_{\text{neu}} = \frac{1}{A(E)} \frac{m^* q^3}{\varepsilon N_{\text{neu}} \hbar^3} \tag{3.38}$$

where N_{neu} is the concentration of neutral impurities, taken to be equal to $N_D - N_A - n$, and $A(E)$ is a function which takes into consideration the interaction of neutral impurities with carriers of varying energy [168]. Although fabricated devices do contain a concentration of unintentional impurities such as nitrogen and/or oxygen, these will not be considered in N_{neu} as the concentration of neutral dopants resulting from carrier freeze-out greatly exceeds the

concentration of unintentional impurities that are present from the fabrication process [169]. In determining $A(E)$, Erginsoy proposed that the interaction of neutral impurities with carriers could be assumed to be independent of the energy of the carriers and replaced this function with the modal value of 20 [166]. For higher temperatures, this assumption has shown to be more than satisfactory in silicon and 4H-SiC [101, 156, 170] where the majority of carriers have a lower kinetic energy. For germanium at temperatures below 20 K however, it has been shown [167] that energy dependence of the neutral impurity scattering rate must be taken into consideration as the value for $A(E)$ reduces monotonically with increasing carrier energy. This has also been shown to be the case for highly doped silicon [168, 171].

For modelling the mobility of carriers in germanium at temperatures below 20 K, the scattering from neutral impurities must be considered [167]. However, it shall be shown in the forthcoming section that the influence from neutral impurities can be neglected if it is assumed that all dopants remained ionised from 20 K to room temperature.

3.4.1 Model comparison to experimental results

Combining equations (3.34) to (3.38) using equation (3.33) allows a computational model for the electron mobility of a non-degenerate semiconductor to be determined from room temperature down to 20 K. At temperatures above room temperature, additional scattering mechanisms such as carrier-carrier scattering must be considered [26]. This mechanism may

C_l (N/cm^2)	1.29×10^7 [163]
E_{ds} (eV)	1.7 [162]
θ_{op} (K)	520 [172]
ω_{op} (rad/s)	62.6×10^{12} [14]
E_{op} (eV)	0.5
ε_r (1)	16.2
m^*/m_0 (1)	0.22

Table 3.1 Parameters used to calculate the electron mobility for intrinsic and n-type germanium in figure 3.4

be safely ignored for the temperature range that is the focus of this study. During device fabrication, unintentional defects and impurities lead to excess scattering and hence carrier mobilities that are lower than theoretical predictions and cannot be predicted with high levels of certainty until device fabrication has been completed.

The experimental electron mobility as a function of temperature for intrinsic and n-type germanium is plotted in figure 3.4 where the reported values for $N_D - N_A$ are 10^{13} and 5.6×10^{16} cm^{-3} based on hall measurements. Calculating the total mobility for both of these materials results in the solid line shown in the figures.

From the data in figure 3.4a, it can be seen that the total carrier mobility in lightly doped germanium is dominated by the harmonic average of the acoustic and optical phonon limited mobilities. The harmonic average of the acoustic and optical phonon scattering using equation (3.33) is more than satisfactory for modelling electrons in intrinsic germanium.

For the moderately doped sample, it can be seen that scattering from ionised impurities is grossly overestimated by over an order of magnitude at 20 K although the error is negligible for temperatures above 200 K. It should also be noted that the scattering from neutral impurities has not been considered for these calculations as has previously been shown that the presence of neutral impurities is only required for modelling at temperatures below 20 K [173, 167]. Despite the neglect of neutral impurity scattering, which would only serve to further lower the predicted mobility, the overestimation of the scattering from ionised impurities makes the harmonic average approximation unsuitable for modelling of carriers at cryogenic temperatures.

3.4.2   Higher accuracy mobility modelling

As shown, the harmonic averaging of the carrier mobility provides a satisfactory fit for mobility data for doping concentrations at and below 5.5×10^{16} cm^{-3} for temperatures above 200 K. For higher doping concentrations however and lower temperatures, the model
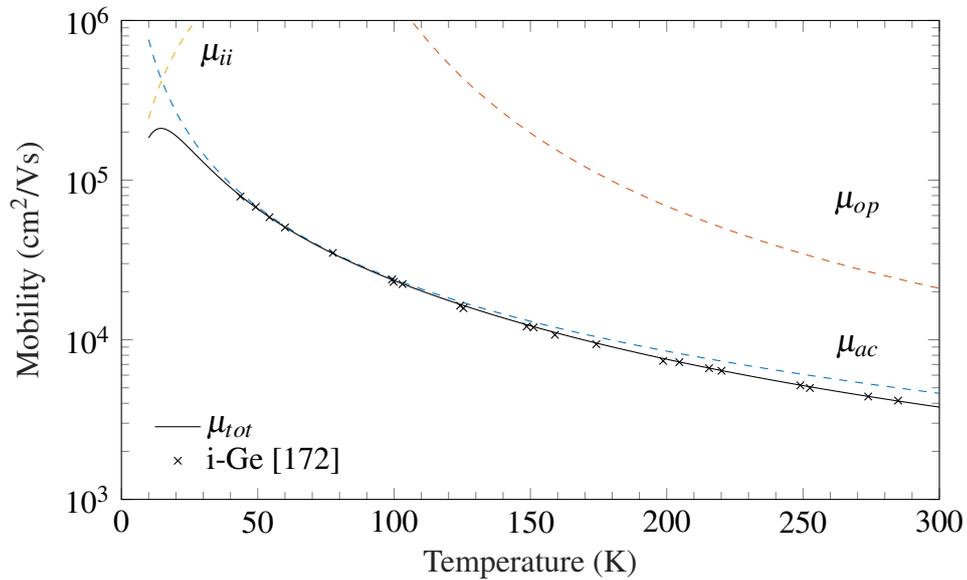
(a) $N_D - N_A = 1 \times 10^{13}$ cm^{-3}
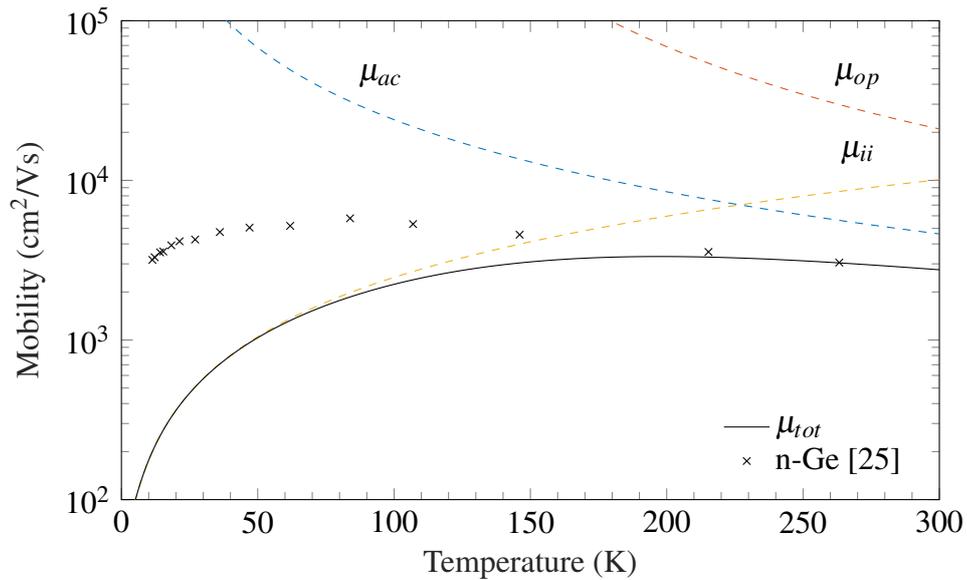
(b) $N_D - N_A = 5.5 \times 10^{16}$ cm^{-3}

Fig. 3.4 Calculated electron mobility in intrinsic (a) and n-type (b) germanium compared to experimental data. Dashed lines indicate individual scattering mobilities and solid line represent to the harmonic average of these mobilities.

begins to underestimate the carrier mobility compared to experimental data as can be seen in figure 3.4b. The mobilities provided through equations (3.34) to (3.38) were derived assuming all carriers have an energy of $3k_BT$ for reasons which shall be explained herein.

The carrier mobility of a semiconductor is given by

$$\mu = \frac{q\langle\tau\rangle}{m} \tag{3.39}$$

where τ is the energy relaxation time of carriers which can be solved for through

$$\frac{1}{\tau(x)} = \sum_n \frac{1}{\tau_n(x)} \tag{3.40}$$

in a similar to manner the calculation of the carrier mobility through the harmonic average model. The expectation values for τ can be found through the numerical solving of

$$\langle\tau\rangle = \frac{\int_0^\infty \tau(x)e^{-x}x^{3/2}dx}{\int_0^\infty e^{-x}x^{3/2}dx} = \frac{4}{3\sqrt{\pi}}\int_0^\infty \tau(x)e^{-x}x^{3/2} \tag{3.41}$$

where $x = E/k_B T$ is the normalised carrier energy.

For temperatures below 150 K, the majority of scattering arises from acoustic phonons and ionised impurities. Assuming neutral impurities and optical phonons can be neglected from the calculation of τ, the expectation value becomes

$$\langle\tau\rangle = \frac{4}{3\sqrt{\pi}}\int_0^\infty \frac{e^{-x}x^{3/2}}{\tau_{ac}^{-1}(x) + \tau_{ii}^{-1}(x)}dx \tag{3.42}$$

where the scattering rates are given by

$$\tau_{ac} = \frac{l_l}{v_t x^{1/2}} \tag{3.43}$$

and

$$\tau_{ii} = B(x)v_t^3 x^{3/2} \tag{3.44}$$

where v_t is given by

$$v_t = \sqrt{\frac{2k_B T}{m^*}}, \tag{3.45}$$

l_l is acoustic scattering length given by

$$l_l = \frac{\pi \hbar^4 C_l}{m^{*2} E_{ds}^2 k_B T} \tag{3.46}$$

and

$$B(x) = \frac{m^* \varepsilon^2}{2\pi(n + 2N_A)q^3} \frac{1}{\ln\left(1 + \left(\frac{\varepsilon x}{q^2 n'^{1/3}}\right)^2\right)} \tag{3.47}$$

In order for a closed-loop model for (3.42) to be determined, the $B(x)$ term must be substituted with a constant which is independent of x. Originally, it was found that if the expectation value for τ was calculated at temperatures where ionised impurity scattering dominates, that is assuming $\tau \approx \tau_{ii}$, then the integrand of equation (3.41) has a maximum at $x = 3$. As a result, it became common practice to calculate the relaxation time was through substituting $B(x)$ with $B(3)$. Through the substitution of $B(x) \approx B(3)$, a closed-loop expression for the acoustic phonon and ionised impurity limited relaxation time was found to be [25]

$$\tau_{\text{ac-ii}} = \tau_{ac}[1 + z^2(\text{Ci}(z)\cos(z) + \text{Si}(z)\sin(z) - \frac{\pi}{2}\sin(z))] \tag{3.48}$$

where

$$z^2 = \frac{6\tau_{ac}}{\tau_{ii}} \tag{3.49}$$

where the mobility was calculated through multiplying the previously calculated relaxation time by q/m^*.

Debye and Conwell showed that the approximation of $B(x) \approx B(3)$ allowed for the resistivity of germanium to be modelled in the temperature range of 77 to 300 K with doping concentrations ranging from 10^{14} to 5.5×10^{16} cm^{-3} when only considering acoustic and ionised impurity scattering. At low temperatures, the consideration from neutral impurities
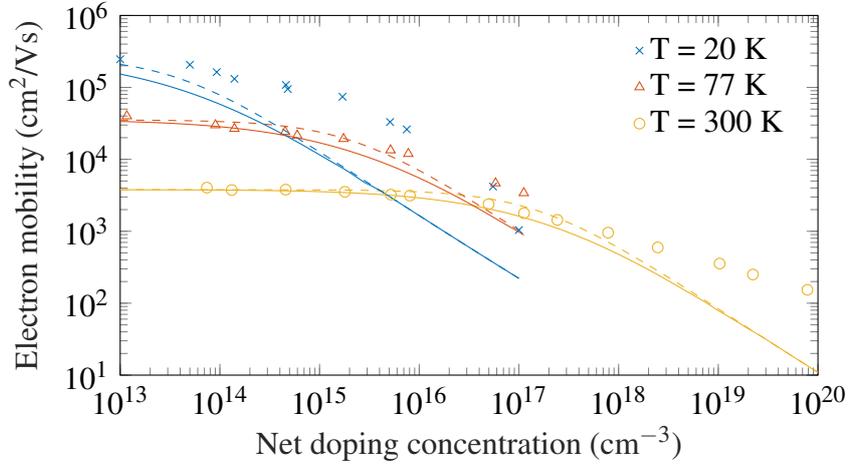
(a) Mobility model using harmonic average (dashed) and model developed by Debye and Conwell (solid) where both models substitute $B(x)$ with $B(3)$ in order to achieve equation (3.36) from (3.44)
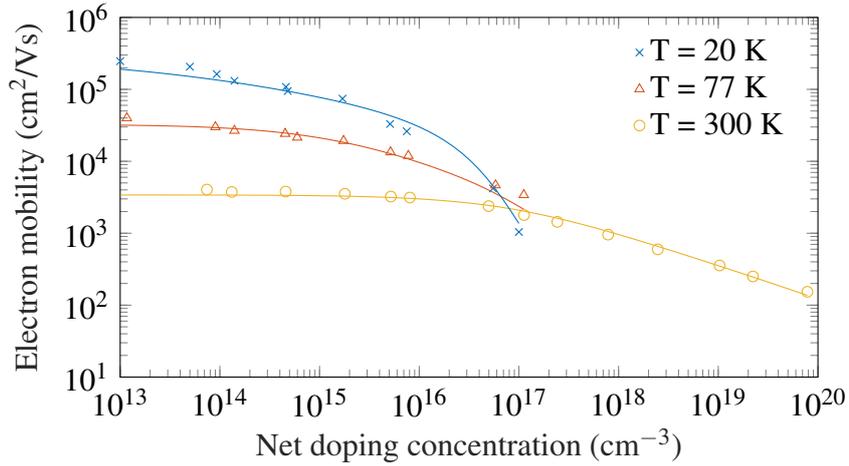
(b) Mobility model for electrons in germanium using full numerical solution for equations (3.39) and (3.41)

Fig. 3.5 Comparison of the mobility models for germanium at room temperature [174], 77 K [174] and 20 K [25]. Calculations were performed using an effective mass of $m^* = 0.22m_0$. Solid or dashed lines are based on the discussed models and data points are taken from references.

was added by assuming that

$$\frac{1}{\mu_{\text{Deb-Con}}} = \frac{1}{\mu_{\text{ac-ii}}} + \frac{1}{\mu_{\text{Neu}}} \tag{3.50}$$

although the presence of neutral impurities is only required for mobility modelling below 20 K [175].

A plot of the experimental carrier mobility in germanium in comparison to equations (3.33) and (3.48) can be seen in figure 3.5a. From the figure, it can be seen that the scattering from ionised impurities is overestimated at higher doping concentrations as the predicted mobility is lower than experimental values at room temperature once the doping concentration exceeds 10^{17} cm^{-3}. For lower doping concentrations, where the majority of scattering is dominated by optical and acoustic phonons, the harmonic average is suitable for predicting the carrier mobility. At lower temperatures, the range of suitability for these two models is reduced and it can be seen that the models underestimate the mobility for doping concentrations above 10^{15} cm^{-3} and 10^{13} cm^{-3} respectively at 77 K and 20 K. It can readily be seen from the data that the use of either the harmonic average model or the model provided by Conwell and Debye is unsuitable for carrier mobility modelling at cryogenic temperatures.

In comparison to these two approximation models, the carrier mobility predicted as a function of doping using the full numeric solution of equations (3.41) and (3.39) is plotted in figure 3.5b. The scattering from neutral impurities was not considered in this calculation and it can be seen that this does not reduce the accuracy of the model even at temperatures down to 20 K for the data presented.

For the purposes of the data considered in figure 3.5, it was assumed that all donors remain ionised and the acceptor concentration was negligible in all cases, resulting in $n = N_D$. With this assumption, the effective mass was found to best fit the data with an effective mass of $m^* = 0.22m_0$ which is in agreement with the data for modelling carrier mobility in germanium [25, 176, 167]. If carrier freeze-out was to be included within the model, then the contribution from neutral impurities must be considered.

Comparing the full numerical solution to the approximations, it can be seen that all three models converge to the same value for lattice scattering limited mobility at low doping concentrations. Where the full numeric solution has an advantage in terms of accuracy, the simplicity of equations (3.33) and (3.48) is attractive for reducing computation time in simulations. In order to find the range of suitability of both equation (3.33) and (3.48), the error in comparison to model has been calculated using

$$\%\text{Error} = 100\left(\frac{\mu_{\text{num}} - \mu_{\text{app}}}{\mu_{\text{app}}}\right) = 100\left(\frac{\langle\tau\rangle - \tau_{\text{app}}}{\tau_{\text{app}}}\right) \tag{3.51}$$

where τ_{app} is the approximation of the scattering rate given by equation (3.40) or (3.42) and is plotted in figure 3.6 as a function of temperature. It can be seen that for room temperature modelling, there is less than a 1% deviation between the full numeric model for doping concentrations less than 10^{14} cm^{-3} although the error is increased to over 10% at 20 K. Of
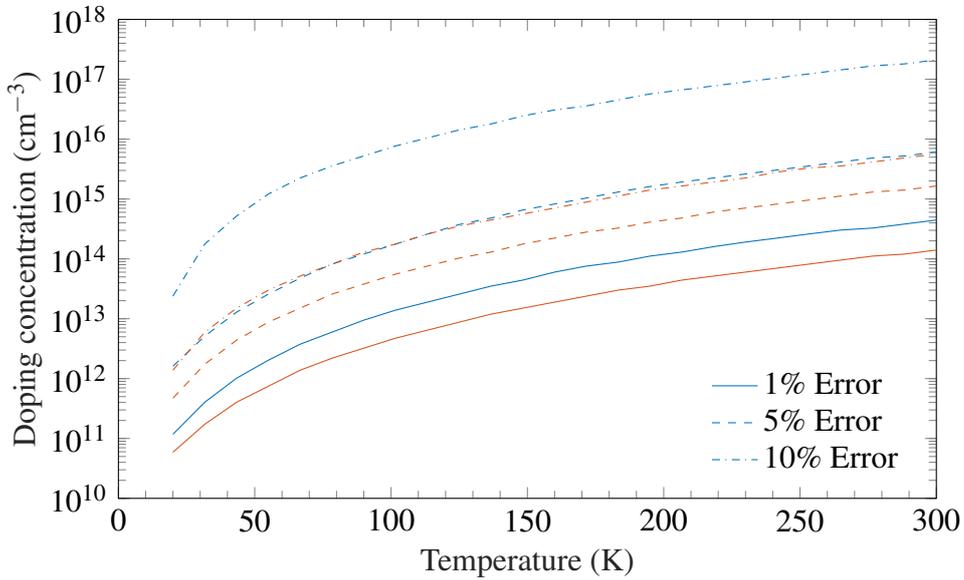
Fig. 3.6 Comparison of percentage error between approximations of the harmonic average (blue) and the model prepared by Debye and Conwell (orange) with respect to the full numerical solution for the carrier mobility. The error lines indicate doping concentration at which there is a 1% (solid), 5% (dashed) and 10% (dash-dot). Above the percentage error lines, the full numeric solution must be performed to calculate the carrier mobility.

the two models, it can be seen that the harmonic average model follows the full numeric solution for a higher range of doping compared to the Debye-Conwell model. For accurate modelling of carrier mobility at 20 K, a full numeric solution must be applied.

3.4.3 Empirical mobility model

Neglecting oxide/semiconductor interfaces which shall be considered later, computation of the carrier concentration and mobility in order to determine the conductivity, and the resulting current density can be quickly achieved for a single piece of material using the aforementioned models. However, simulating the current density at specific regions of a device where carrier densities and electric field vary as a function of position requires far more numerical effort. TCAD is a family of finite element modelling software that is capable of performing such a task but in order for this to be achieved, the built-in models must first be adapted in order to model germanium characteristics.

Within TCAD, there exists a mobility model which includes the aforementioned scattering mobilities for majority and minority carriers in semiconductors as a function of temperature and both ionised acceptor and donor concentrations [177]. The mobility model, known as the *Philips unified mobility model*, is given by

$$\frac{1}{\mu_i} = \frac{1}{\mu_{i,L}} + \frac{1}{\mu_{i,A}} \tag{3.52}$$

where $\mu_{i,L}$ represents the doping independent lattice scattering mobility equal to

$$\mu_{i,L} = \mu_{i,max} \left(\frac{T}{300} \right)^{-\theta_i} \tag{3.53}$$

where $\mu_{i,max}$ and θ are fitting constants and the subscript 'i' is altered to 'e' for electrons or 'h' for holes. $\mu_{i,A}$ is the mobility calculated from a model which takes into account all the
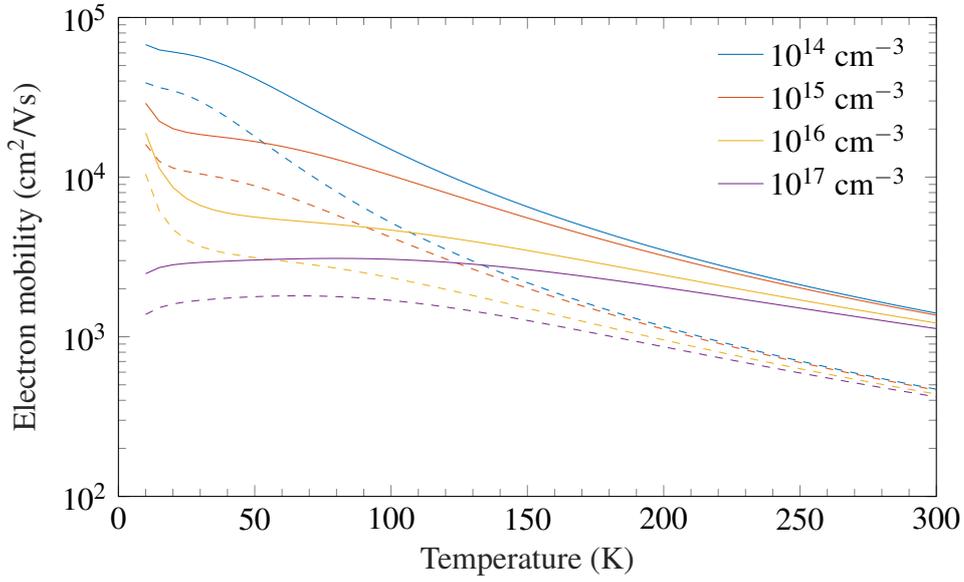
Fig. 3.7 Mobility model used in TCAD simulation of devices for n-type silicon (solid lines) and p-type silicon (dashed lines) as a function of for doping concentrations ranging from 10^{14} to 10^{17} cm^{-3}.

scattering mechanisms using an empirical formula given by

$$\mu_{i,A} = \mu_{i,N} \left(\frac{N_{i,sc}}{N_{i,sc,eff}} \right) \left(\frac{N_{i,ref}}{N_{i,sc}} \right)^{\alpha_i} + \mu_{i,c} \left(\frac{n+p}{N_{is,sc,eff}} \right) \tag{3.54}$$

where

$$\mu_{i,N} = \frac{\mu_{i,max}^2}{\mu_{i,max} - \mu_{i,min}} \left(\frac{T}{300} \right)^{3\alpha_i - 1.5} \tag{3.55a}$$

$$\mu_{i,c} = \frac{\mu_{i,max}\mu_{i,min}}{\mu_{i,max} - \mu_{i,min}} \left(\frac{300}{T} \right)^{0.5} \tag{3.55b}$$

are used as fitting terms when comparing the model to experimental data. The term $N_{i,sc}$ is used to describe the scattering from ionised impurities for majority carriers and $N_{i,sc,eff}$ represents the concentrations of carriers involved in the scattering of minority carriers as well as electron-hole scattering.

The model was originally developed for calculating the carrier mobility in silicon devices at a given temperature assuming that the donor, acceptor, electron and hole concentrations

were all known [177, 178] and can be adapted to model the carrier mobility of germanium using experimental data. An example of equation (3.52) for uncompensated n- and p-type silicon is plotted in figure 3.7. As can be seen from the data, the increased scattering from neutral and ionised impurities increases as the dopant concentration increases for both p- and n-type silicon. This model can be adapted to fit the experimental data for p- and n-type germanium as shown in figure 3.8.

For modelling the carrier mobility in germanium, the values for μ_{min} and μ_{max} were taken from the maximum and minimum carrier mobilities at room temperature as a function of doping concentration. Considering experimental mobilities, the maximum and minimum values obtained are 3900 and 120 cm^2/Vs for electrons [174] and 2250 and 100 cm^2/Vs for holes [179]. In order to determine the temperature dependence of lattice scattering limited mobility, the exponent θ must be taken from the average of the optical and acoustic scattering limited carrier mobility for both electrons and holes, that is

$$\mu_{i,L} = \mu_{i,\text{max}} \left(\frac{T}{300} \right)^{-\theta_i} \approx \left[\frac{1}{\mu_{ac}} + \frac{1}{\mu_{op}} \right]^{-1} \tag{3.56}$$

where the optical phonon and acoustic phonon limited mobilities are given by equations (3.34) and (3.35). The lattice scattering limited mobility assumes the mobility is dominated by a single temperature-dependent term which follows a power law through the implementation of θ_i. Observing the equations for both the acoustic and optical phonon limited mobilities, the lattice scattering limited mobility can be modelled using a value of 1.5 for θ. In the case of the optical phonon scattering however, the temperature dependence is exponential and so a

Eq. (3.52)-(3.55)	$\mu_{i,\text{max}}$ (cm^2/Vs)	$\mu_{i,\text{min}}$ (cm^2/Vs)	θ	α	$N_{i,\text{ref}}$ (cm^{-3})
electrons	3900	100	1.65	0.55	3×10^{17}
holes	2100	100	2	0.55	4×10^{17}

Table 3.2 Constants used for calculating carrier mobility in germanium for electrons and holes using Eq. (3.53) to (3.55)
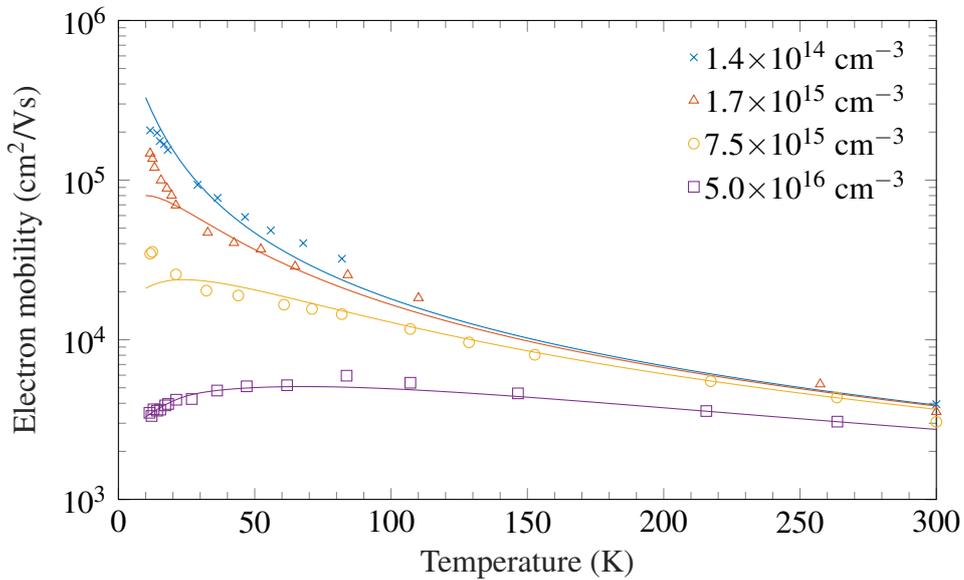
(a) n-type germanium TCAD mobility model compared to experimental data [25]
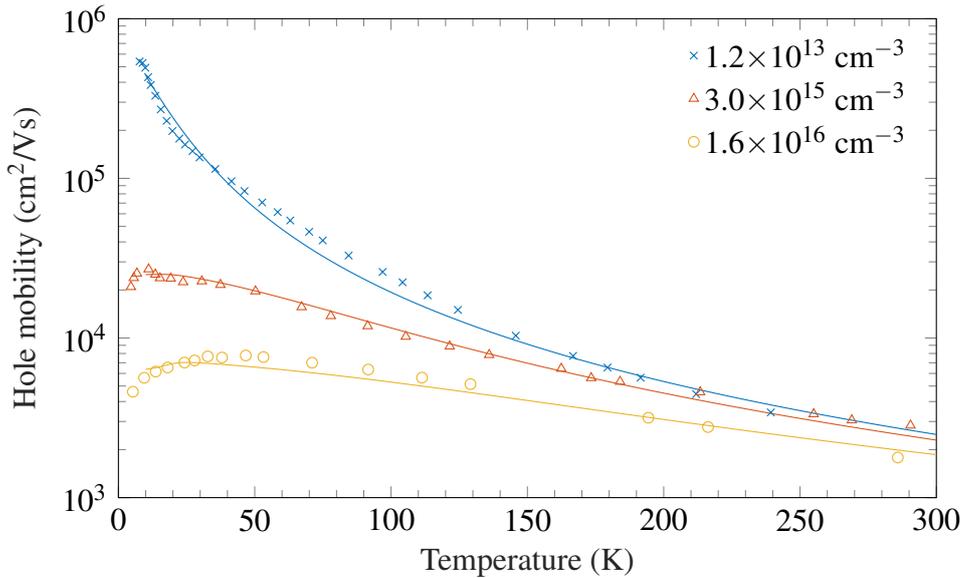
(b) p-type germanium TCAD mobility model compared to experimental data [96, 100]

Fig. 3.8 Mobility model used in TCAD simulations for germanium as a function of temperature and doping compared to experimental data.

numerical fit can only be used to approximate the mobility using the Philips unified mobility model. Using a non linear least square fitting method, it was found that $\mu_{i,max}$ for electrons and holes is 3500 and 2100 cm^2/Vs respectively and value for θ was calculated as 1.65 and

2 for electrons and holes respectively. The other constants used for fitting the data are listed in Table 3.2.

A comparison of the Philips unified mobility model, which has been adapted for modelling the carrier mobility in n- and p-type germanium as a function of both temperature and doping concentration is plotted in figure 3.8. From the figure, it can be seen that the model has been successfully adapted in order to take into account the temperature and doping dependence of the electron and hole mobilities in germanium. Consistent with what is found with the full numerical model, the temperature dependence of the carrier mobility reduces with increasing doping concentration whilst samples with low doping concentrations are dominated by the lattice scattering mobility given by equation (3.53). At temperatures below 20 K, the electron mobility for samples doped at 1.7×10^{15} and 7.5×10^{15} cm^{-3} continues to increase in contrast to what is predicted by the model. As the focus of this work was on the modelling of devices at 20 K and above, this inconsistency was not explored further. Despite this, the pre-built mobility within TCAD is suitable for predicting the carrier mobility within the drift region and doped regions of electronic devices from room temperature down to 20 K in germanium.

3.5   Velocity saturation

For low fields, the velocity of a carrier has a linear relation with the applied field according to

$$v = \mu F \tag{3.57}$$

where μ is given by equation (3.39) or it can be approximated by (3.52).

Following the application of an electric field, the carriers gain kinetic energy and are no longer in thermal equilibrium with the lattice. In order for thermal equilibrium to be reestablished, carriers in motion begin to emit phonons. The emission of phonons at low fields can be neglected and does not reduce the carrier mobility. At high fields, the emission

of phonons begins to result in increased optical phonon scattering emission and reduces the carrier mobility. The emission of phonons increases considerably and at a certain field the emission of phonons generated from the carriers becomes too great and the carriers saturate to a constant velocity as shown by experimental data in figure 3.9.

At cryogenic temperatures, this effect occurs at lower fields as the increase in carrier mobility results in a greater kinetic energy at low fields than compared to room temperature. As such, the carriers reach the saturation velocity at much lower fields than compared to room temperature. As well as this, carriers deviate from the linear velocity field relationship given by equation (3.57) at much lower fields.

As well as velocity saturation, another effect can occur in which the velocity of carriers begins to decrease with increasing field. This can be seen from the experimental data for n-type germanium in the $\langle 100 \rangle$ direction at temperatures below 130 K [180]. The origin of this effect is due to the transition of carriers from the conduction band minimum to a higher band with a lower effective mass [180]. Normally, this effect does not occur at room temperature in germanium and has only been considered in compound semiconductors such as GaAs and GaN for room temperature device modelling [181, 182]. As such, a model is yet to be developed to take into account this effect at cryogenic temperatures. The implications of this effect results in a negative differential resistance in devices at cryogenic temperatures in which the current will begin to decrease with increasing voltage. This must also be considered in order to accurately model the electrical characteristics of germanium devices at cryogenic temperatures.

The field dependence of the carrier mobility can be modelled empirically using the models that are pre-built into TCAD. For the majority of mobility cases, the carrier velocity can be modelled using the extended Canali model [186]

$$\mu(F) = \frac{(\alpha+1)\mu_{\text{low}}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{\text{low}}F}{v_{\text{sat}}} \right)^{\beta} \right]^{1/\beta}} \tag{3.58}$$
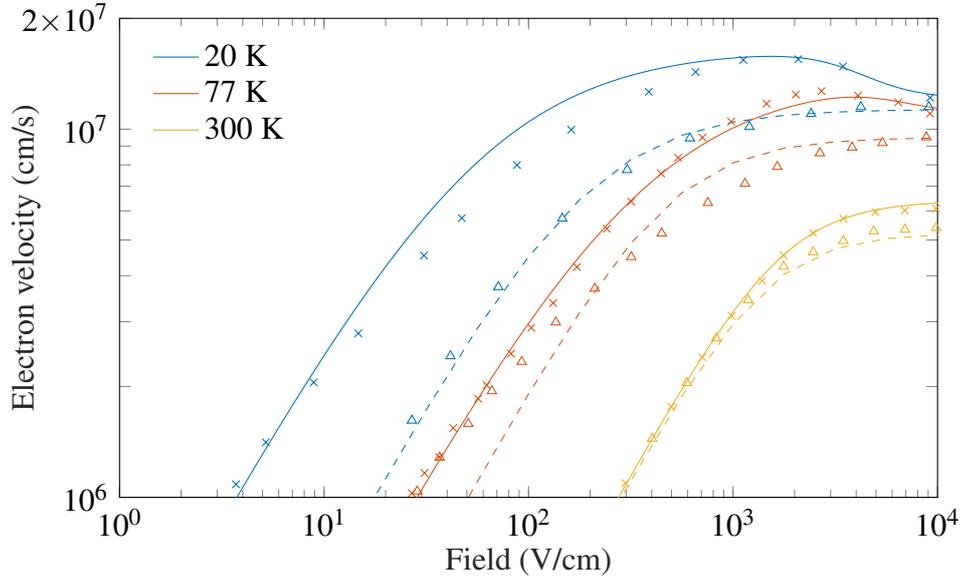
(a) Electron velocity saturation [180]
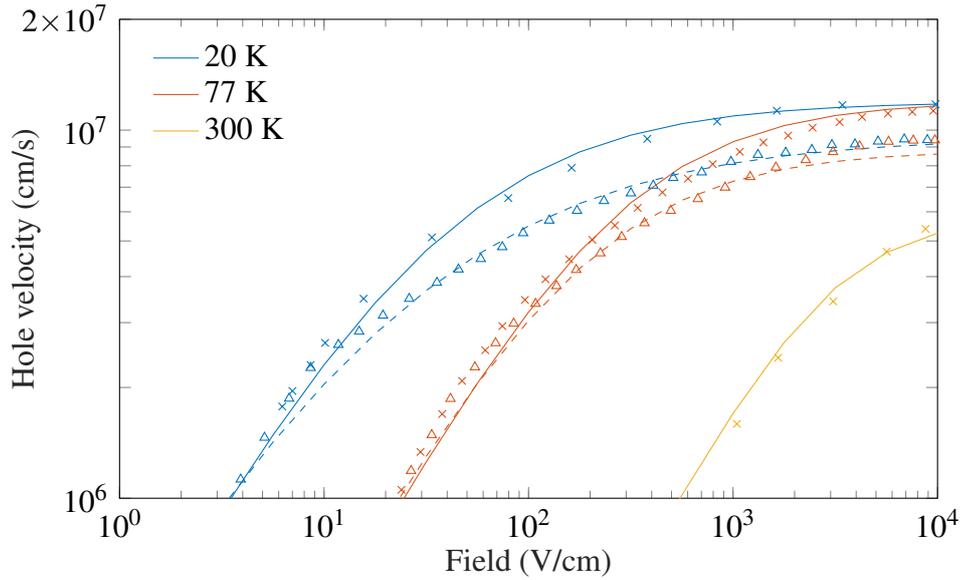
(b) Hole velocity saturation [183–185]

Fig. 3.9 Comparison of experimental velocity saturation for electrons and holes in the $\langle 100 \rangle$ (solid lines) and $\langle 111 \rangle$ (dashed lines) direction of germanium to empirical model. Crosses and open triangles indicate experimental data for the $\langle 100 \rangle$ and $\langle 111 \rangle$ directions respectively.

where F is the applied electric field, μ_{low} is the low field mobility given by Eq. (3.39) or

(3.52) and β is a temperature dependant fitting parameter given as

$$\beta = \beta_0 \left(\frac{T}{300K} \right)^{\beta_{\text{exp}}}$$

(3.59)

where β_0 and β_{exp} are fitting constants. The saturation velocity for electrons and holes in all cases were found to decrease linearly with temperature according to

$$v_{\text{sat}}(T) = \begin{cases} A_{v,\text{sat}} - B_{v,\text{sat}}\left(\frac{T}{300K}\right) & v_{\text{sat}} > v_{\text{sat,min}} \\ \\ v_{\text{sat,min}} & \text{otherwise} \end{cases} \tag{3.60}$$

where $A_{v,\text{sat}}$ and $B_{v,\text{sat}}$ are fitting constants that are given in Table 3.3.

When considering the electron mobility within the $\langle 100 \rangle$ direction, the average carrier velocity can be modelled using [187]

$$\mu(F) = \frac{\mu_{\text{low}} + v_{\text{sat}}\frac{F^{\beta-1}}{F_T^\beta}}{1 + \gamma\frac{F}{F_T}^\alpha + \frac{F}{F_T}^\beta} \tag{3.61}$$

where α, β and γ are all fitting constants and F_T is the field at which the transfer of electrons begins.

Computing the correct parameters to fit the experimental data provided shows that the temperature dependence of the transfer electron effect in the $\langle 100 \rangle$ direction of n-type germanium can be modelled when the transfer field and the value for γ are given by

$$F_T = 23.8T + 956 \tag{3.62}$$

and

$$\gamma = 262T^{-0.796} \tag{3.63}$$

Using the equations (3.58), (3.60) and (3.61), the field dependence of the carrier mobility can be modelled when simulating devices as shown in figure 3.9. All constants used for modelling the carrier velocity are listed in table 3.3.

Comparing the data to the model, a good agreement between the experimental data for holes in p-type germanium is observed at all temperatures. For the modelling of electrons

Table 3.3 Constants used for calculating field dependent carrier mobility for electrons and holes in the $\langle 100 \rangle$ and $\langle 111 \rangle$ direction

Eq. (3.58) - (3.59)	α	β_0	$\beta_{\exp}$
electrons $\langle 100 \rangle$ (T $>$ 130 K)	0	2.0	0.10
electrons $\langle 111 \rangle$	0	2.0	0.15
holes $\langle 111 \rangle$	0	0.1	0.06
holes $\langle 111 \rangle$	0	1.5	0.35

Eq. (3.60)	$A_{v,\text{sat}}$ (cm/s)	$B_{v,\text{sat}}$ (cm/s)	$v_{\text{sat,min}}$ (cm/s)
electrons $\langle 100 \rangle$	1.60×10^7	1.03×10^7	5.69×10^6
electrons $\langle 111 \rangle$	1.17×10^7	6.56×10^6	4.20×10^6
holes $\langle 100 \rangle$	1.24×10^7	6.48×10^6	5.30×10^6
holes $\langle 111 \rangle$	9.86×10^6	4.20×10^6	4.20×10^6

in germanium n-type germanium, it can be seen that the model underestimates the carrier velocity in the $\langle 111 \rangle$ direction at 77 K and overestimates the carrier velocity in the $\langle 100 \rangle$ direction at 20 K. The result of these errors is due to the assumption in both models that the carrier velocity remains linear at low fields and deviates abruptly at a certain threshold field as opposed to a gradual deviation which is observed experimentally. The models can be adapted in order to take into account this gradual reduction in carrier mobility with increasing field, although this greatly increases the error in the model when considering the rest of the experimental data. The models accurately predict the low and high field velocity of electrons and holes in germanium including the transfer electron effect within a reasonable degree of accuracy for the temperature range considered within this work.

3.6 Conclusion

The models developed within this section predict the temperature dependence of the free carrier concentration for uncompensated and compensated germanium. For both cases, as well as the degeneracy case, a complete set of equations have been provided that are capable of determining the total carrier concentrations as a function of temperature and doping

concentration. For the mobility of carriers, the harmonic average model has been shown to be suitable for room temperature samples in n-type germanium for doping concentrations up to 10^{17} cm^{-3} although the overestimation in ionised impurity scattering results in an underestimate of carrier mobility above this doping concentration. This is also the case when considering the electron mobility at doping concentration above 10^{15} and 10^{13} cm^{-3} at temperatures of 77 and 20 K. Above these doping concentrations, a full numeric solution of the carrier mobility must be performed if the scattering rates are considered. In tackling this, the Philips unified mobility model was adapted and a full set of coefficients have been provided allowing for the carrier mobility to be calculated within germanium for both electrons and holes as a function of temperature and doping concentration. The reduction of the carrier mobility at high fields has been modelled based on experimental data considering the transfer electron effect which occurs for electrons in germanium at temperatures below 130 K.

With the results reported in this chapter, a full set of models that calculate the concentration, mobility, and velocity of carriers within germanium has been presented for the first time. The models here can be used to determine the on- and off-state characteristics of germanium photodetectors and JFETs using TCAD which allows manufacturers to predict and optimise device behaviour prior to fabrication. In order to predict the performance of germanium MOS based devices, the characteristic of germanium/oxide interfaces must also be considered.

Chapter 4

Metal Oxide Germanium Capacitor Fabrication and Temperature Analysis

4.1   Introduction

The fabrication of power electronic devices necessitates the inclusion of a thick lightly doped drift region in order to withstand a large blocking voltage. The resistance of this region can contribute from 50 to 90% of the total device resistance and so modelling this region through knowledge of the carrier concentration and mobility is essential in determining the total on-state resistance of a vertical germanium power device. Following the lightly doped drift region, the semiconductor/oxide interface in MOSFET and IGBT power devices is the second largest contributor to the total device resistance due to its thin channel and low carrier mobility at the oxide/semiconductor interface [188]. In order to determine the total contribution of the channel resistance to the total power device resistance, the oxide capacitance and interface state density must be determined. Analysis of metal oxide semiconductor (MOS) leakage and CV profiles provides insight into the transfer characteristics of MOSFET and IGBT devices at the oxide interface.

Analysis into the interface properties of Si and SiC MOS based devices has been well documented in literature whereas the water solubility of native GeO_2 has generally limited analysis of germanium based MOS devices. As well as this, ohmic contacts are required for back contacts to MOS capacitors which has historically been a challenge to achieve for n-type germanium. Although, as it shall be shown within this chapter, these issues have been alleviated through recent research into alternative high-κ dielectrics and ohmic contact studies.

As discussed in the literature review, recent advancements in ohmic contacts on germanium as well as superior stable high-κ dielectrics have introduced the possibility of vertical MOS power devices using germanium. In fabricating silicon and SiC vertical MOS power devices, a lot of time and post fabrication analysis is required in order to achieve the optimal device structure when considering diffusion profiles, etch rates, trench oxidation and so on. Here, the oxide capacitance and interface quality has been extracted from newly fabricated in-situ ZrO_2 on germanium for the first time. Through the extraction of these parameters, simulations of the transfer characteristics of an optimised vertical power device using ZrO_2 as a gate dielectric can be performed.

4.1.1   Surface defects and their impact on device performance

The formation of semiconductor/oxide surfaces for MOSFET and IGBT devices is non trivial and poor oxide formation/deposition can lead to the formation of dangling bonds and interface states which serve to reduce carrier lifetime and lower carrier mobility leading to an increase in device resistance [189, 133]. Experimental modelling and characterisation of MOS based devices has shown that following the resistance of the lightly doped drift region, the resistance of the channel is the second greatest contributor to the total on state resistance of devices [189, 133, 80]. Considering the structure given in figure 4.1 the total resistance of

a MOSFET is given by

$$R = R_S + 2R_{accumulation} + R_{channel} + R_{drift} + R_D \qquad (4.1)$$

where $R_{S/D}$ is the source/drain resistance, $R_{accumulation}$ is the accumulation resistance, $R_{channel}$ is the channel resistance and R_{drift} is the drift region resistance. The main contribution to the resistance in power electronic devices is that of the drift region resistance due to its length and near intrinsic doping concentration. The extra drift region is essential to ensure a large blocking voltage from source to drain although this contributes anywhere from 50 to 90 % of the total resistance for devices reported in literature [189, 190, 80]. Due to the high doping concentrations, exceeding 10^{19} cm^{-3} for source and drains contacts, the resistance of these regions are negligible in comparison to the other components. As a result, the other main
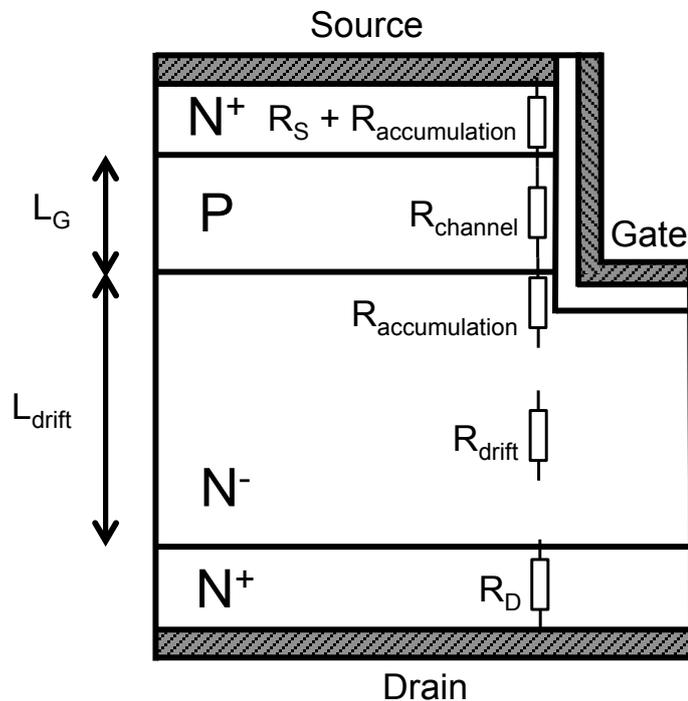
Fig. 4.1 Structure of Trench etched MOSFET with resistances highlighted.

contribution to overall device resistance is the channel and accumulation resistances at the semiconductor/oxide interface.

The channel region resistance is determined by the carrier density and mobility at the oxide/semiconductor interface. Considering the structure in figure 4.1, the electron channel is formed through the application of a sufficient gate bias which attracts minority electrons within the p-type region to the semiconductor/oxide interface in order to form an inversion channel. As the width of this channel is of the order of nanometers, and as the concentration of carriers decreases exponentially with distance from the surface, the mobility of carriers in this region is much lower than compared to the bulk due to the increased scattering from the oxide surface and interface traps. As well as the channel region, carriers near the oxide interface in the source and drift region are attracted to the oxide resulting in a reduced carrier mobility near the semiconductor/oxide interface. Considering these resistive losses in a silicon power MOSFET, Baliga [189] showed that the resistance of the channel and accumulation regions can be modelled using

$$R_{channel} = \frac{x_{inv}L_G}{2\mu_{inv}C_{ox}(V_G - V_t)} \tag{4.2a}$$

$$R_{accumulation} = \frac{Cx_{acc}(L_{ox} - L_G)}{\mu_{acc}C_{ox}(V_G - V_t)} \tag{4.2b}$$

where x_{inv} and x_{acc} are the diffusion depths of the charge in the channel and accumulation regions, L_{ox} is the total length of the oxide, L_G is the gate length, μ_{inv} and μ_{acc} are the inversion and accumulation layer mobilities, C_{ox} is the oxide capacitance and $V_G - V_t$ is the difference between the gate voltage and the threshold voltage which is assumed to be positive. C is a correction factor for the accumulation layer resistance which considers the spreading of the current away from the oxide surface near the ends of the channel. For silicon power devices, a value of 0.3 was found when fitting to experimental data [191].

Equation 4.2a shows that the channel resistance can be reduced by reducing the gate length and maximising the oxide capacitance and carrier mobility. As the oxide capacitance is given by

$$C_{ox} = \frac{\varepsilon A}{t_{ox}}$$ (4.3)

where t_{ox} is the oxide thickness, the resistance of the channel and accumulation region can be lowered by reducing the oxide thickness or by increasing the oxide permittivity. In order to ensure a low leakage current in the off-state, there is a limit to how short the gate length can become and so the majority of research focused on minimising channel/accumulation resistance is targeted towards maximising the oxide capacitance. Aside from the physical dimensions of the device, the channel and accumulation resistances can also be reduced by maximising the carrier mobility in these two regions.

At the oxide semiconductor interface, the mobility of carriers is taken as the harmonic average between the bulk and surface limited mobilities

$$\frac{1}{\mu} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{surface}}$$ (4.4)

where the bulk mobility is given by the models presented in section 3.4 and the surface mobility is given by

$$\frac{1}{\mu_{surface}} = \frac{1}{\mu_c} + \frac{1}{\mu_{rp}} + \frac{1}{\mu_{sr}}$$ (4.5)

where respectively μ_c, μ_{rp} and μ_{sr} and are the Coulomb, remote phonon and surface roughness limited mobilities.

Defects that are present at the oxide/semiconductor scatter carriers in the channel due to the charge they introduce at the interface. The charged centres can come from various types of defects. Impurity atoms in the semiconductor or oxide disturb the charge neutrality leading to charged regions which scatter carriers. The three scattering methods are dependent on the concentration of impurities at the interface at high electric fields [192] as well as the

concentration of inversion charge and interface trap density [193–195]. As well as carrier conduction, the presence of interface traps lead to an increase in leakage current and gate leakage as the traps act as hopping centres for conduction [196–198].

Due to gate control constraints, there is also a limit to how thin the oxide thickness can become. Once the EOT reduces below 1 nm, there is a non-negligible exponential increase in gate leakage that can lead to a loss of gate control of the MOSFET [199, 200, 145]. The main mechanisms by which conduction occurs within oxides is dependant on the trap density, temperature and electric field all of which must be considered in order to predict MOS based device behaviour. Unfortunately, due to focus towards CMOS applications, germanium MOS devices are usually characterised at room temperature [143, 201, 114]. Research of leakage in germanium MOS capacitors at cryogenic temperatures is scarce [202] with only one publication on leakage in Al_2O_3 MOS capacitors at cryogenic temperatures despite the popularity of current research in HfO_2 [124, 203] and ZrO_2 [204, 205] dielectrics. Here, we fabricate, measure and model the capacitance and leakage characteristics of ZrO_2 on n-type germanium from room temperature down to 20 K for the first time which, when combined with the models developed in chapter 3, the IV characteristics of a vertical germanium ZrO_2 MOSFET can be simulated.

4.2   MOS Capacitor fabrication

4.2.1   Ohmic back contact formation

Ohmic contacts have historically been an issue for n-type germanium. The presence of surface states at the boundary between metal and the germanium surface pins the Fermi level approximately 0.1 eV above the valence band edge as shown in figure 4.2. The cause of the pinned Fermi level has yet to be agreed upon in literature. One commonly used theory is that the change in the Fermi level position is due to the presence of metal-induced gap

states [17, 206] which offset the surface potential at the interface and pin the Fermi level position in the semiconductor.

For carriers to enter the semiconductor from the metal, they must have sufficient energy to overcome the potential barrier or have the depletion width of the barrier be thin enough such that a sufficient concentration of carriers can tunnel through the barrier.

The depletion width associated to the bending of the band can be reduced with doping concentration according to

$$W_D = \sqrt{\frac{2\varepsilon_s \left(V_{bi} - V - \frac{k_B T}{q} \right)}{q N_d}} \tag{4.6}$$

A high tunnelling current through the barrier can be achieved by heavily doping the contacts and this has been adopted in literature to achieve ohmic contacts [207, 208]. Other techniques which have shown success include the introduction of a thin insulator between metal and semiconductor [209, 210] and the formation of metal-germanium alloys at the boundary from a high temperature anneal [211, 212, 21].
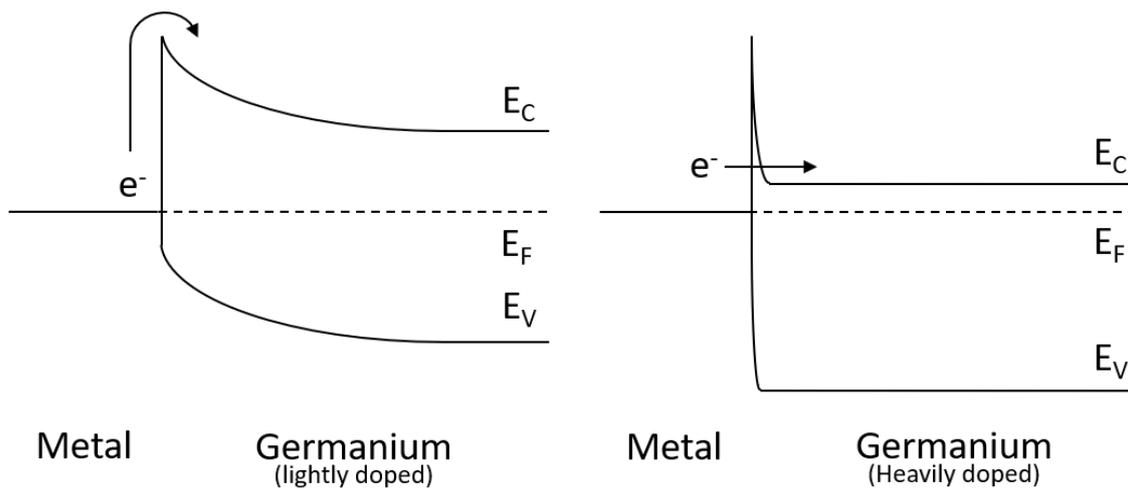
Fig. 4.2 Band diagram of metal on lightly and heavily doped n-type germanium. Arrows show electron conduction for thermionic-emission (left) and tunnelling (right).

Despite the ohmic n-type germanium results, all of these methods result in a Schottky contact to p-type germanium. Recently, a new technique has been demonstrated which involves the generation of highly energetic carriers at the semiconductor surface resulting in ohmic contacts for both n- and p-type germanium [18].

The formation of metal nano-structures trap carriers that self-heat due to the atomic size of the nano-structure. If the diameter of the nano-structure is below the Debye length, the phonons generated by the electrons cannot interact with the surrounding lattice and are trapped within the nano-structure. Electron emission spectroscopy showed the temperature of these carriers can exceed 3000 K [213] corresponding to an energy of 0.26 eV which significantly reduces the potential energy which is required in order to excite carriers over the barrier.

Gold nano-structures at the Ge interface can be fabricated by annealing a Ge/Cr/Au structure for a period of 5-10 seconds. The mismatch in the crystal lattice of the Au and Cr results in the formation of individual islands following the application of a high temperature anneal. If the annealing process is performed for too long then the nano-structures will coalesce and form a continuous gold film. In order for self-heating of electrons in the nano-structures to occur, the diameter of the nano-islands must be less than 100nm and so care must be taken when annealing the interface.

4.2.2   Ohmic back contact formation

Here, gold nano-structures were fabricated through annealing Ge/Cr/Au at the gold-germanium eutectic temperature of 360 °C [18]. Firstly, gallium and antimony doped germanium wafers with doping concentrations of $\leq 10^{15}$ cm^{-3} were organically cleaned through 10 minutes of acetone sonication at 80 °C followed by a further 10 minutes of sonication in isopropanol (IPA) before being rinsed with deionised (DI) water ($\rho > 10^{18}$ Ωcm). AZ5214 photoresist was spun onto the samples and exposed to ultraviolet light in order to pattern the device

surface. Following patterning, the samples were placed into buffer hydrofluoric acid (BHF) for 3 minutes to remove any native GeO_2 and GeO_x and were subsequently rinsed in DI water before being dried with an N_2 gun. Following this, the samples were immediately placed into an e-beam chamber were the pressure was reduced to 10^{-6} mBarr. Once the pressure was achieved, 5 nm of Cr was deposited onto the bare germanium substrate at a rate of 0.2 nm/s that was fallow by Au at a deposition rate 0.25 nm/s until a thickness of 200 nm had been achieved. Following contact formation, the samples were rapidly thermally processed in nitrogen at 360 °C for 5, 10 and 15 seconds. The IV characteristics were finally obtained using a Keithley 4200 probing station at room temperature.

The IV characteristics of Cr/Au nano-structure contacts onto n- and p-type Ge are plotted in figure 4.4. For the as-grown devices, the p-type germanium shows linear ohmic type conductivity whilst there is more than a 4 order magnitude difference between the forward
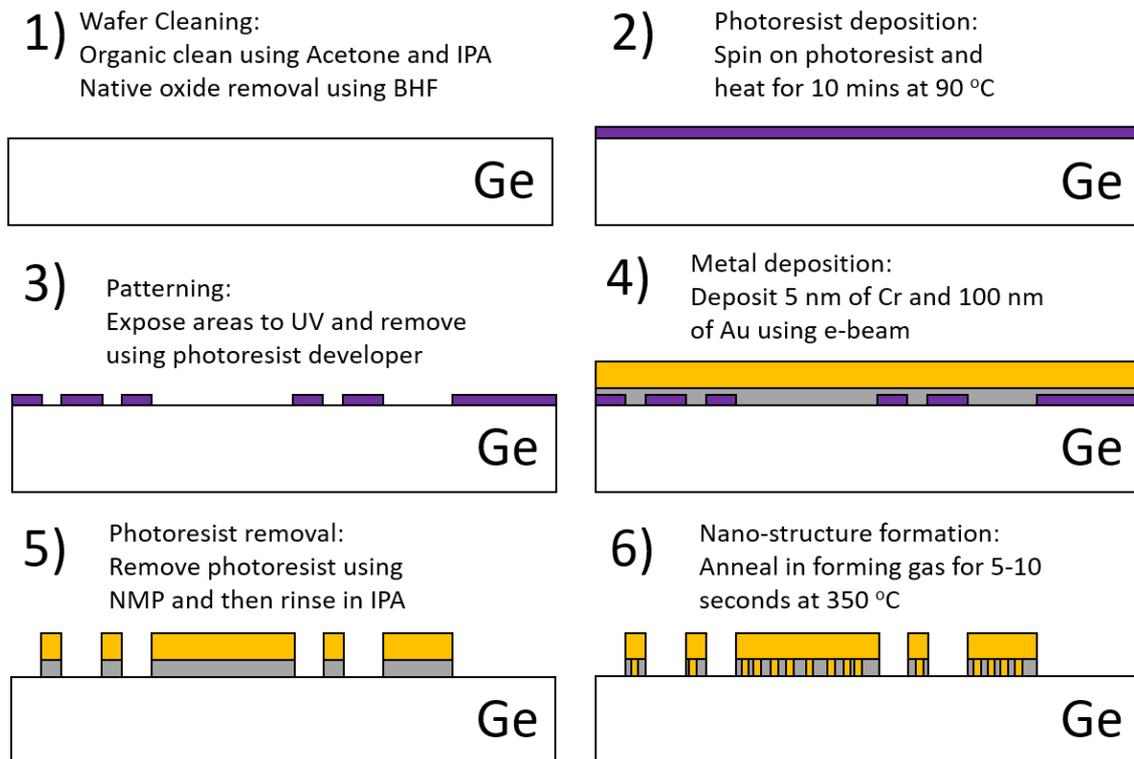
Fig. 4.3 Process flow for ohmic contacts on germanium using gold nanostrcutures.

(a) P-type $N_A \approx 10^{15}$ cm^{-3} (b) N-type $N_D \approx 10^{15}$ cm^{-3}

(c) P-type $N_A \approx 10^{15}$ cm^{-3} (d) N-type $N_D \approx 10^{15}$ cm^{-3}
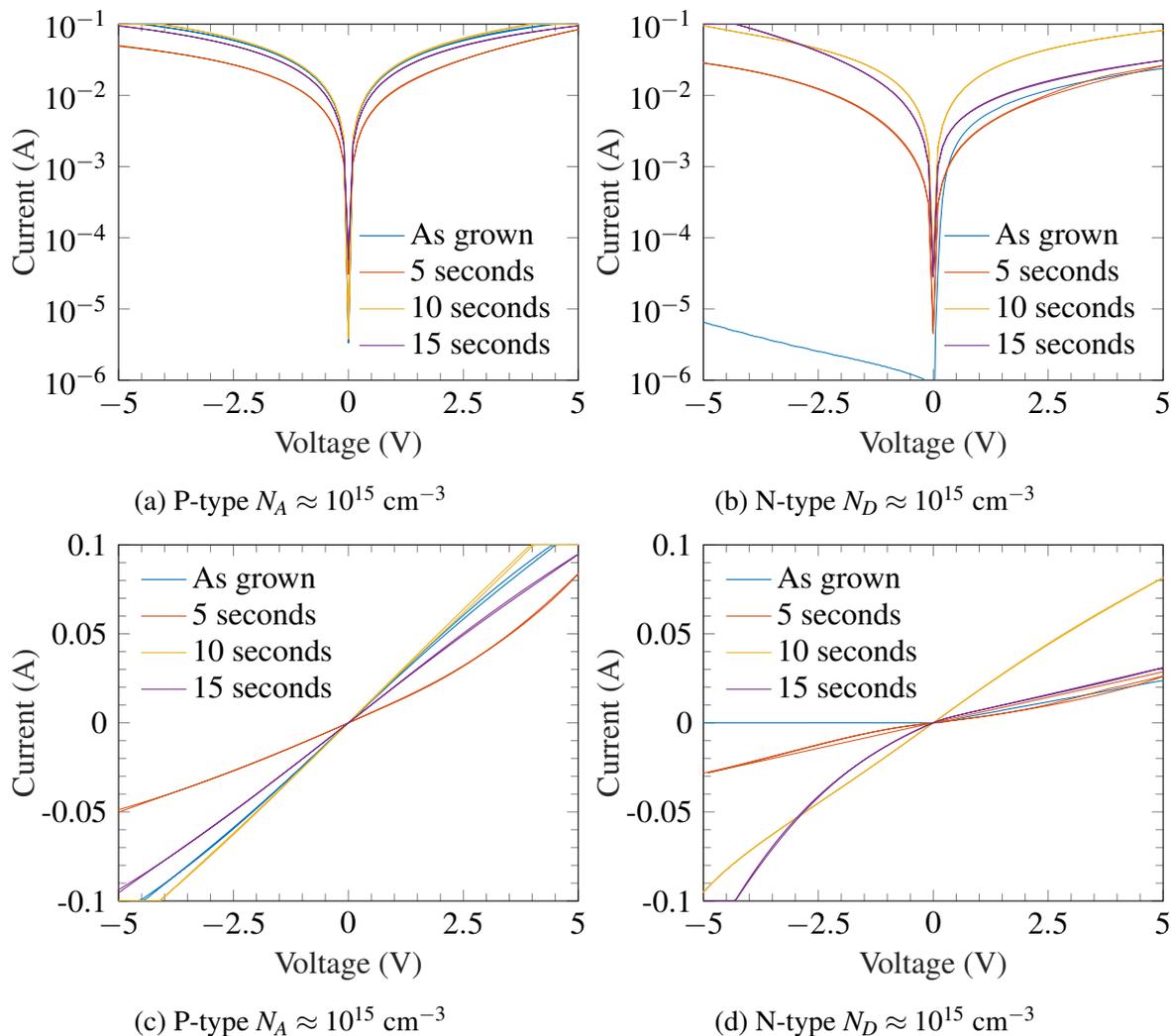
Fig. 4.4 IV characteristics showing ohmic contact formation on both n- and p-type germanium following a 450 °C anneal.

and reverse direction of the current for n-type germanium. The large difference in the current magnitude based on the bias direction clearly indicates Schottky like conduction in the as-grown Cr/Au contact on n-type germanium [17]. It can be seen that ohmic like conduction was achieved for Cr/Au on n-type germanium as the difference in forward and reverse current becomes negligible following the N$_2$ anneal. As well as this, unlike other ohmic contact fabrication methods, the p-type IV characteristics remain ohmic both before

and after annealing. Due to the non-linear nature of the IV characteristics, extraction of the specific contact resistivity cannot be achieved.

4.2.3   Fabrication of Al$_2$O$_3$/GeO$_2$/Ge MOS capacitors

As a control for the ZrO$_2$/Ge MOS capacitors, n- and p-type Al$_2$O$_3$/GeO$_2$/Ge MOS capacitors were fabricated. Al$_2$O$_3$ is an attractive alternative to native oxides that are used in industry due to its high melting point, high thermal conductivity and low diffusivity into the semiconducting substrate at high temperatures [214, 147]. As well as these benefits, the first alternative oxide for MOS capacitor fabrication aside from the native SiO$_2$ on silicon was Al$_2$O$_3$ and showed a greater ability to retain its electrical characteristics following electron bombardment in comparison to SiO$_2$ based capacitors [215].

A process flow of the fabrication of Al$_2$O$_3$/GeO$_2$/Ge MOS capacitors can be seen in figure 4.5. Firstly, in order to form a high quality Ge/GeO$_2$ interface, the native oxide was stripped to form a high quality oxide through thermal oxidation. For all devices, ohmic back contacts were fabricated using the method described previously. Following this, the top surface of the devices were organically cleaned before rinsing with DI water and drying with an N$_2$ gun. The residual native oxide was stripped using BHF for 2 minutes before rinsing with DI water. Samples were placed into a quartz glass boat before being placed into an oxidation furnace. A steady flow of O$_2$ was maintained through the chamber at 600 sccm. The gas was allowed to flow for 1 hour before heating to allow any atmospheric contamination to be evacuated. Following purging, the samples were heated at a rate of 20 °C/min and were left at the oxidation temperature for 10 minutes before being left to cool down to room temperature. Based on published literature [216], the germanium oxidation temperatures were chosen to be 475, 500, and 550 °C as this was shown to be the optimal temperature range in order to achieve a high quality GeO$_2$ with the low concentration of

1) Wafer Cleaning:
Organic clean using Acetone and IPA
Native oxide removal using BHF

Ge

2) Ohmic back contact:
Repeat recipe for Ohmic
contact without patterning

Ge

3) Native oxide formation:
Oxide surface in furnace to form
GeO_2 layer

Ge

4) Al_2O_3 deposition:
Deposit 10 nm of Al_2O_3 using
atomic layer deposition (ALD)

Ge

5) Gate contact formation:
Pattern surface us photolithography
and deposit 5 nm and 100 nm of Au

Ge

6) Oxide sintering:
Anneal in forming gas for 10
minutes at 300 °C to improve D_{it}

Ge

Fig. 4.5 Process flow for fabricating n-type and p-type Al_2O_3 MOS capacitors with a GeO_2 interlayer. Note, samples were cleaned a second time before forming GeO_2 interlayer.

interface traps. Once the samples were oxidised, they were placed into the ALD chamber and were pumped down to a pressure of 10^{-6} mBarr before deposition.

For the samples used here, 10 nm of Al_2O_3 was grown using atomic layer deposition. The deposition was performed by first placing the samples in a high vacuum chamber and evacuating the chamber of atmosphere until a pressure of 600 mTorr was achieved. Once a suitable vacuum had been achieved, the samples were heated up to 200 °C. The precursors used for the reaction in the chamber were Adduct-grade trimethylaluminium and H_2O which were transported using N_2 as a carrier gas. The pulse/purge cycles for each reactant were 0.1/4 s and 0.1/6 s for TMA and H_2O respectively following on from the recipe used in [147]. Following multiple runs, it was found that 111 cycles achieved an optimal thickness of 10 nm.

In order to determine the thickness of ALD films, X-ray refraction (XRR) was used to give the oxide thickness. In measuring the reflected X-ray intensity, as the tilt angle θ of the incident X-ray is increased, the intensity of light will begin to oscillate. The density of oscillations gives the film thickness and density through the relation

$$\sin^2(\theta_n) = \theta_c^2 + \frac{\lambda^2}{4T_{ox}^2}(n + \Delta n)^2 \tag{4.7}$$

(a) X-ray refraction of Al$_2$O$_3$/Si

(b) $\sin^2(\theta_n)$ against $(n + \delta n)^2$ for SiO$_2$/Si

(c) X-ray refraction of GeO$_2$/Ge

(d) $\sin^2(\theta_n)$ against $(n + \delta n)^2$ for GeO$_2$/Ge
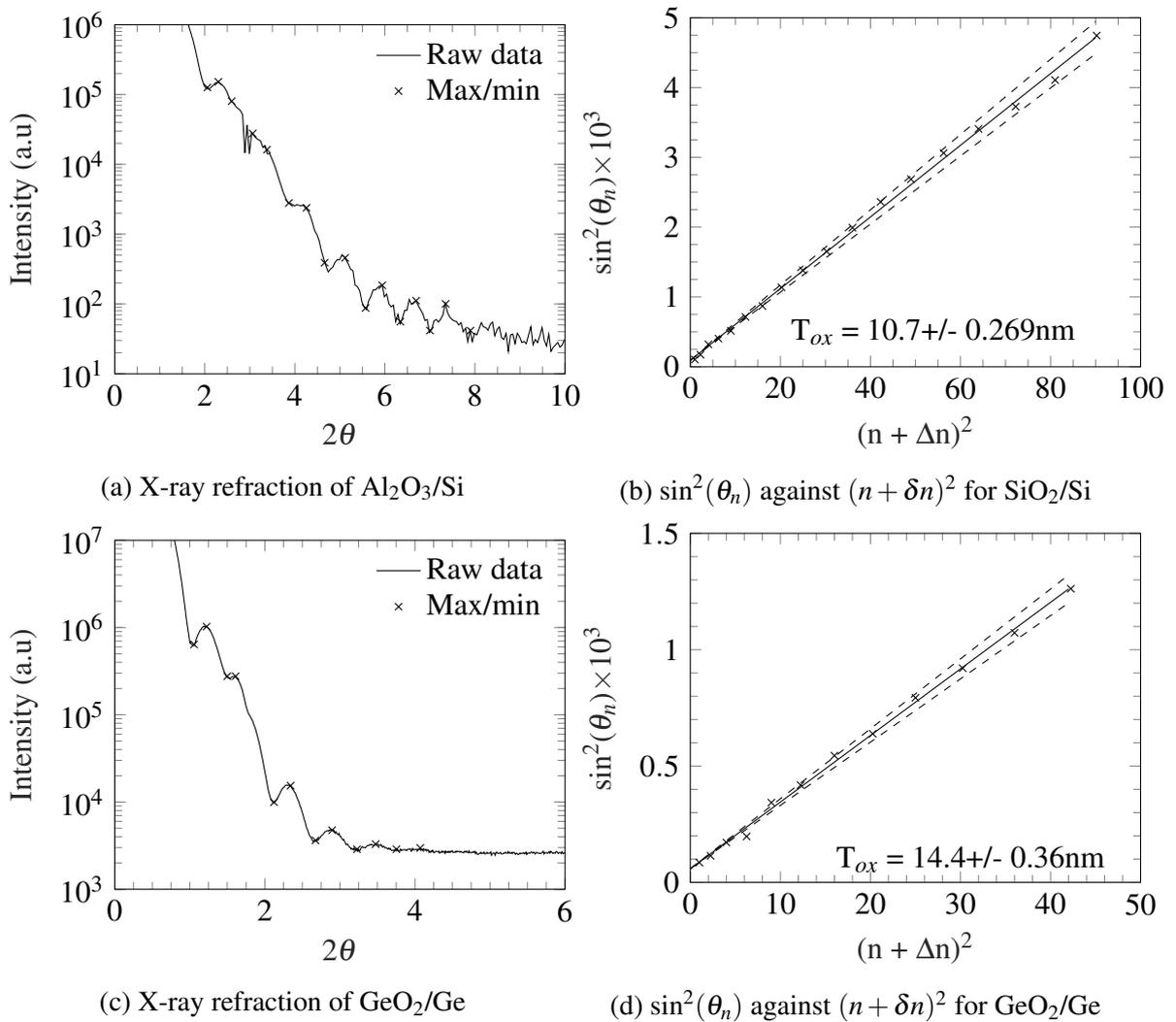
Fig. 4.6 X-ray refraction of Al$_2$O$_3$ on Si (a) and GeO$_2$ on Ge (c). The thickness of the oxides were calculated using equation 4.7 giving 10.7 +/- 0.269 and 14.4 +/- 0.36 nm for the Al$_2$O$_3$ and GeO$_2$ respectively.

where θ_n is the angle of the observed maximum or minimum, θ_c is the critical angle, λ is the wavelength of the incident x-ray equal to 0.145 nm, n is an integer equal to the fringe number (1, 2, 3...) and Δn is equal to 0.5 for a maximum and 0 for a minimum [217]. The peak and trough positions for the XRR response from an Al_2O_3 sample can be seen in figure 4.6a. As can be seen from the figure, there is little variation in the angle position of the maxima and minima. As illustrated in figure 4.6b and 4.6d, by plotting $\sin^2(\theta_n)$ against $(n + \delta n)^2$, the gradient

$$m = \frac{\lambda^2}{4T_{ox}^2} \tag{4.8}$$

can be used to find the oxide thickness. Using this relation, the thickness of the Al_2O_3 layer was determined to be 10.7 nm. Applying the same technique, the thickness of the GeO_2 on germanium was confirmed to be 14.4 nm following an oxidation time of 10 minutes at 500 °C. The thickness of the grown layer is approximately 1.5 times thicker than samples reported in literature grown in similar conditions [216]. The reason for the increased oxide thickness is a result of the increased oxidation due to the ramping and cooling stages of the furnace before and after the 10 minute dwell period.

Once the oxide thickness were calculated, top contacts were fabricated using photolithography patterning and deposition of 5 nm of chromium followed by 100 nm of gold. Chromium was deposited to ensure good adhesive contact between the gate metal and the oxide. Following gate contact formation, samples were annealed in forming gas with a composition of 5% hydrogen and 95% nitrogen to improve the interface quality [218].

4.2.4   Fabrication of ZrO_2/GeO_2/Ge MOS capacitors

As previously discussed, the introduction of Al_2O_3 as a gate dielectric has allowed for silicon MOS devices with lower gate leakage currents but greater oxide capacitances due to the higher dielectric constant of Al_2O_3. Similarly, ZrO_2 offers the same benefits, but to an even higher order of magnitude due to the much higher dielectric constant of $\sim$30 [143].

One of the key drawbacks of high-κ dielectrics in device fabrication is the higher leakage currents resulting from a greater rate of thermionic emission [219]. Generally, for lower κ dielectrics such as SiO_2, the main sources of oxide leakage are due to traps within the oxide or tunnelling through the barrier of the oxide when it is sufficiently thin. For high-κ dielectrics however, the band offset between the conduction band of the semiconductor and the oxide typically reduces with oxide permittivity leading to an increase in thermionic emission over the oxide barrier [219]. To minimise thermionic emission whilst maximising the dielectric constant, Al_2O_3 is typically used as a best of both worlds approach. At cryogenic temperatures however, the current density resulting from thermionic emission over the barrier decreases exponentially and so this issue can be neglected [17].

Previously, ZrO_2 has only been fabricated through atomic layer deposition directly onto germanium. These approaches require a GeO_2 interlayer to achieve a low D_{it} similar to Al_2O_3 MOS devices. As it will be shown in section 4.4.3, the interface state density of the GeO_2/Al_2O_3 interface reduces with increased oxidation temperature although this results in a thicker GeO_2 that reduces the oxide capacitance. In an effort to reduce the total oxide thickness, we look at the thermal oxidation of the germanium surface following zirconium deposition.

A process flow of the fabrication of the $ZrO_2/GeO_2/Ge$ MOS capacitors can be seen in figure 4.7. Prior to zirconium deposition, several n-type germanium samples were prepared using the same method for the Al_2O_3 devices before thermal oxidation. Following this, the samples were placed into an electronic-beam chamber and were pumped down to a pressure of 10^{-6} mBarr. 50 nm of zirconium was deposited at a rate of 0.2 nm/s onto the top surface of the samples which were thermally oxidised at 550 °C for 10 minutes. As the zirconium layer is thin, the germanium/zirconium interface will still be oxidised leading to the formation of a germanium oxide interlayer although the total thickness will be reduced significantly due to the diffusion barrier provided by the zirconium. Post-dielectric oxidation

1) Wafer Cleaning:
Organic clean using Acetone and IPA
Native oxide removal using BHF

2) Ohmic back contact:
Repeat recipe for Ohmic
contact without patterning

3) Zr deposition:
Deposit 50 nm of Zr using e-beam

4) ZrO_2/GeO_2 formation:
Thermally oxidise Zr at 500 °C
whilst also oxidising Ge surface

5) Gate contact formation:
Pattern surface using photolithography
and deposit 5 nm and 100 nm of Au

6) Oxide sintering:
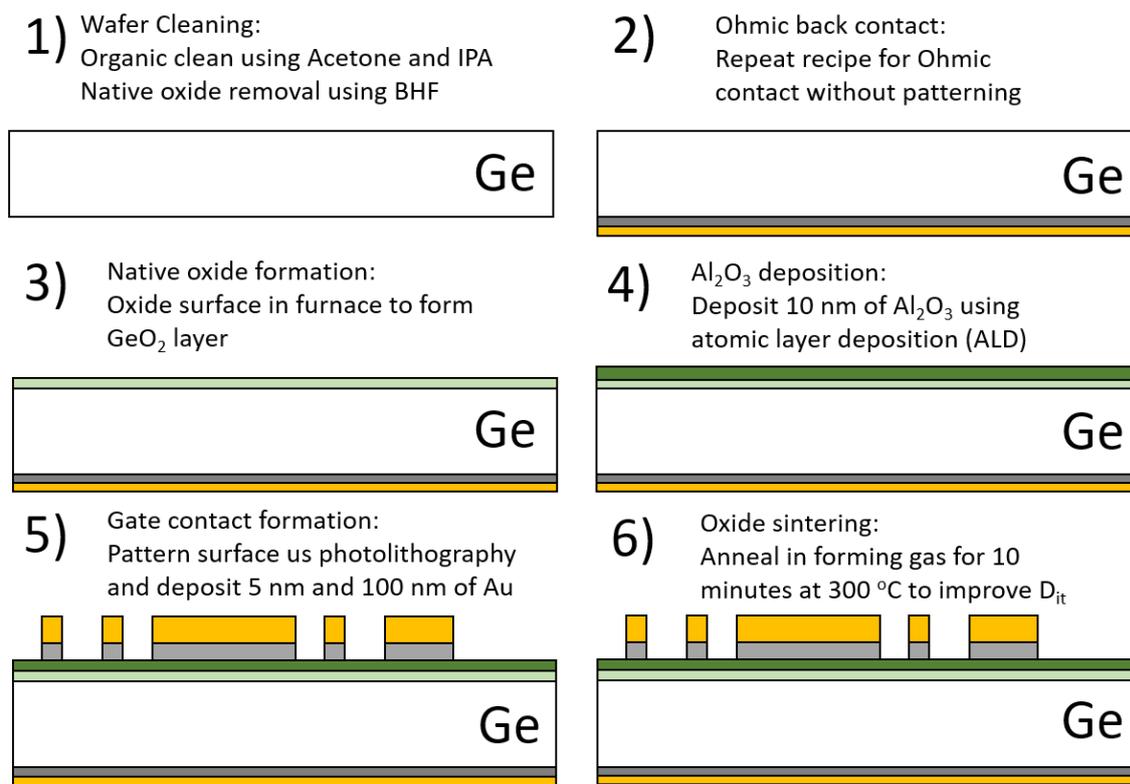Anneal in forming gas for 10
minutes at 300 °C to improve D_{it}

Fig. 4.7 Process flow for fabricating n-type and p-type ZrO_2 MOS capacitors with a GeO_2 interlayer. Note, samples were cleaned a second time before depositing Zr layer.

of the germanium surface has been explored previously [205, 122], although these methods lead to a degradation of the crystallinity of the deposited high-κ dielectrics, whilst here, we fabricate the GeO_2 in-situ with ZrO_2 during the same oxidation process. Following this, the ZrO_2 was patterned using photolithography from which 50 nm of Cr and 300 nm of Au was deposited using electron-beam deposition at rates of 0.2 and 0.3 nm/s respectively.

4.3   Theoretical MOS capacitance and leakage

As is required for simulating silicon MOS devices in TCAD, the capacitance and leakage characteristics of the germanium MOS capacitors incorporating a ZrO_2 gate dielectric must first be measured and modelled to simulate germanium MOS based devices. The key figures

of merit that are required for device simulation are that of the interface trap density, effective oxide thickness and leakage current density. Here, all of these figures of merit have been measured and modelled from the ZrO_2/GeO_2 MOS capacitors and are compared to the more conventional Al_2O_3/GeO_2 where possible.

4.3.1 Interface trap density extraction

A high concentration of defects at the semiconductor/oxide interface serves to reduce the carrier mobility in the channel of MOS devices, increasing the overall device resistance. As well as this, these defects can act as traps which can result in an increased leakage current through the oxide. The extraction of the density of traps at the semiconductor interface is essential in determining the suitability of alternative high-κ dielectrics for high power applications.

For reasons that shall be explained herein, we have used the Terman method as this allows for the interface trap density to be determined near the centre of the band gap as opposed to the low-temperature conductance method which only allows for D_{it} mapping near the band edges [220, 221, 127]. Other methods such as the high-low method allow for accurate determination of D_{it} although the energy range within the band gap is of the order of 0.05-0.1 eV which is unsuitable for modelling purposes as the total interface trap charge concentration must be calculated using the entire energy distribution of the D_{it} within the band gap.

One of the commonly used methods [222–224] for determining the density of interface traps was developed by L. M. Terman for a Si/SiO_2 MOS capacitor [225]. The method takes advantage of the slow response times of interface traps in comparison to high-frequency capacitance-voltage (CV) curves. At sufficiently high frequencies, the traps are unable to respond to the high-frequency AC signal and do not affect the measured capacitance but do

respond to the slowly varying DC gate bias. As a result, the CV curve stretches in the voltage axis in comparison to a CV curve with no interface states.

At high frequencies, assuming the capacitance from interface traps do not contribute to the total the capacitance, the high-frequency capacitance is given by

$$C_{HF} = \frac{C_S C_{ox}}{C_{ox} + C_S} \tag{4.9}$$

where C_S is the semiconductor capacitance and C_{ox} is the oxide capacitance. For a given gate bias, the surface energy ψ_s at the oxide/semiconductor surface will bend leading to a equivalent Terman capacitance equal to [226]

$$C_{T,n} = \frac{\text{sgn}(\beta) C_{sFB} [\exp(\beta) - 1]}{\sqrt{2}(\exp(\beta) - \beta - 1)} \tag{4.10a}$$

$$C_{T,p} = \frac{\text{sgn}(\beta) C_{sFB} [1 - \exp(-\beta)]}{\sqrt{2}(\exp(-\beta) + \beta - 1)} \tag{4.10b}$$

where β is given by

$$\beta = \frac{q\psi_s}{k_B T} \tag{4.11}$$

and C_{sFB} is the semiconductor flat band capacitance given by

$$C_{sFB} = \frac{\varepsilon A}{L_D} \tag{4.12}$$

where L_D is the debye length given by

$$L_D = \sqrt{\frac{k_B T \varepsilon}{q^2 N}} \tag{4.13}$$

where N is the majority doping concentration. A plot of the theoretical capacitance given by equation 4.10 results in a high-frequency CV curve that is not affected by the presence of interface traps. A plot of the measured CV and the theoretical C-ψ_s can then be used

(a) Measured CV at 1MHz   (b) Theoretical capacitance using equation 4.10
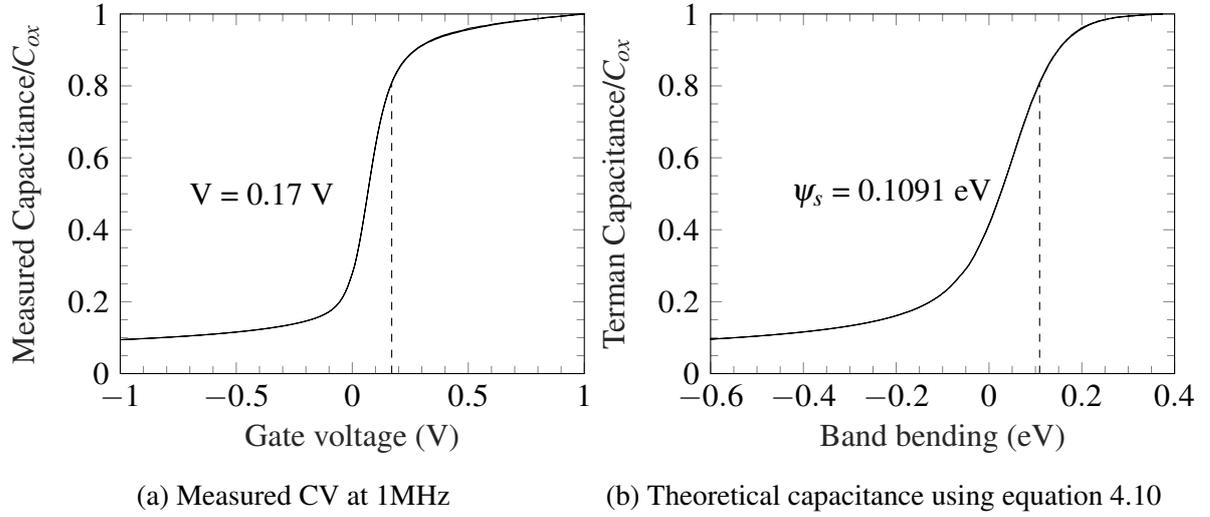
Fig. 4.8 Comparison of measured and theoretical high-frequency capacitance.

to determine the resulting band bending in the fabricated device as a function gate bias as illustrated in figure 4.8. A full plot of the band bending vs experimental gate voltage can be obtained using the capacitance matching technique illustrated in the figure 4.9. The data plotted in figure 4.9 is measured from an Al_2O_3 MOS capacitor with no germanium oxide interlayer using the ALD recipe covered in section 4.2.3. From the $\psi_s V$ relationship, the interface trap density can be found using

$$D_{it} = \left(C_{ox} \left[\frac{dV}{d\psi_s} - 1 \right] - C_T \right) \Big/ q \qquad (4.14)$$

where C_T is the equivalent Terman capacitance for a given band bending value. The position of the interface trap within the band gap is given by

$$\frac{E_C - E_T}{q} = \frac{E_G}{2q} + \psi_s - \phi_B \qquad (4.15)$$

where ϕ_B is the bulk potential given by

$$\phi_B = \frac{k_B T}{q} \ln \left(\frac{N}{n_i} \right) \qquad (4.16)$$
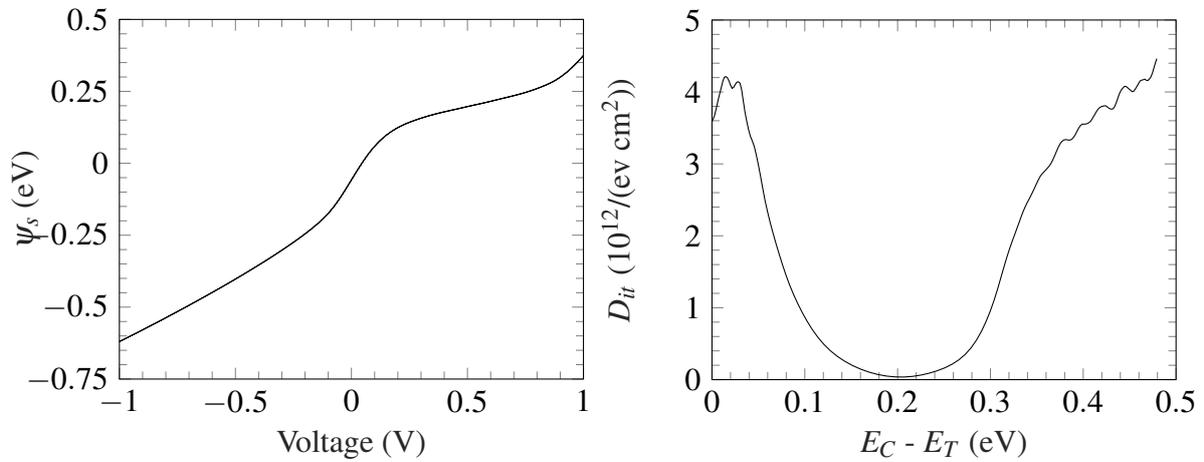
Fig. 4.9 Interface trap density for n-Ge/Al$_2$O$_3$ based on the Terman method.

The interface trap density within the band gap based on the experimental data in figure 4.8 can be seen in figure 4.9. From the figure, it can be seen that the interface trap density increases towards the conduction band edge. As well as this, a second peak can be located close to the band gap centre at ∼0.33 eV. The peak here is attributed to the defects on the germanium surfaces due to dangling bonds. As shown in literature and the work conducted here [224], the surface must first be treated to reduce/remove this peak.

4.4 Ge/GeO$_2$/Al$_2$O$_3$ and Ge/GeO$_2$/ZrO$_2$ characterisation

Following analysis of Al$_2$O$_3$ capacitors without an GeO$_2$ interlayer, Ge/GeO$_2$/Al$_2$O$_3$ MOS capacitors were fabricated on n- and p-type germanium. Samples were placed into a Keithley 4200A parameter analyser in order to perform capacitance-voltage (CV), conductance-voltage (GV) and gate leakage IV measurements. Both the CV and GV measurements were performed by first applying a DC bias to the top gate of the MOS capacitor while the back contact is forced to ground. On top of the DC bias, an AC voltage signal was applied to the gate with an amplitude of 25 mV. Following the application of the AC bias, the capacitance was measured at incremental DC biases using a dual sweep function to observe any hysteresis

effects. Following the MOS CV characterisation, a DC sweep was performed in order to observe the gate leakage characteristics of the MOS capacitors.

4.4.1 CV and GV series resistance correction

In order for parameters such as minority carrier lifetime and interface trap density to be determined, the measured capacitance and conductance must be corrected in order to remove the effects of series resistance from the analysis. The combination of cables, probes and contacts lead to a series resistance in the extracted conductance and capacitance equal to

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{4.17}$$

where G_{ma} and C_{ma} is the conductance and capacitance in accumulation and ω is the angular frequency equal to $2\pi f$. Once the series resistance has been calculated, the corrected capacitance and conductance can be calculated using

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \tag{4.18a}$$
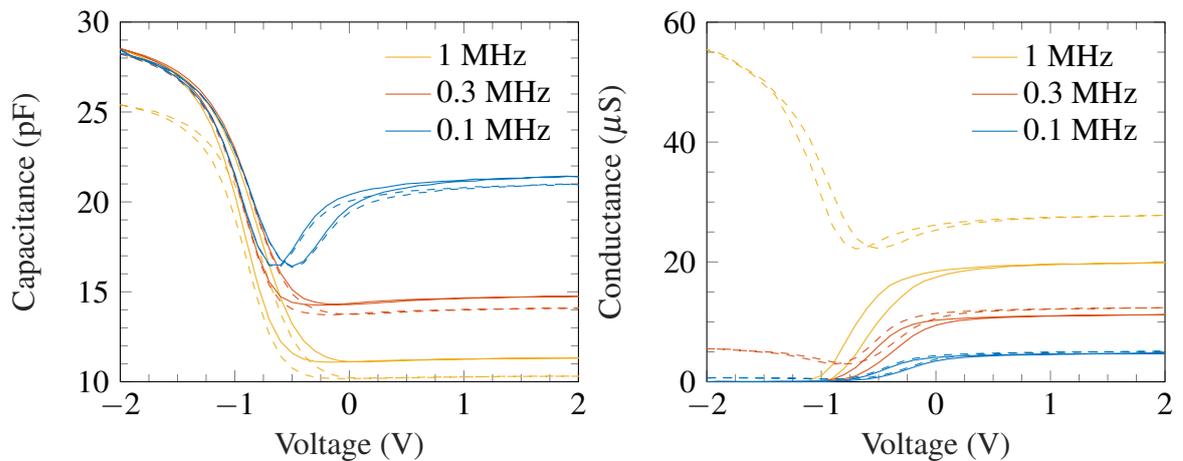
Fig. 4.10 Example of capacitance and conductance correction for a p-type germanium MOS capacitor with 14nm Al$_2$O$_3$ and 10nm GeO$_2$. Measured data are represented as dashed lines whilst the corrected data are solid.

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \tag{4.18b}$$

where

$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s \tag{4.19}$$

and G_m and C_m are the measured conductance and capacitance. An example of a CV and GV curve before and after correction can be seen in figure 4.10. As can be seen from the figure, the series resistance is crucial for high-frequency CV and GV measurements in order to ensure the accumulation capacitance and conductance become inline with the low-frequency accumulation values. Using equations 4.17 through to 4.18 will ensure the effects of series resistance do not affect the extracted interface trap density and minority carrier lifetime.

4.4.2 Ge/Al$_2$O$_3$ with no interlayer

In order to observe the trend in interface trap density and leakage current density for Al$_2$O$_3$ on germanium with and without a germanium oxide interlayer, the CV and leakage characteristics of Ge/Al$_2$O$_3$ MOS capacitors were examined. A plot of the measured capacitance from a deposited Al$_2$O$_3$ MOS capacitor on n- and p-type germanium can be seen in figure 4.11. For both n- and p-type devices, a large hysteresis can be seen in the measured capacitance
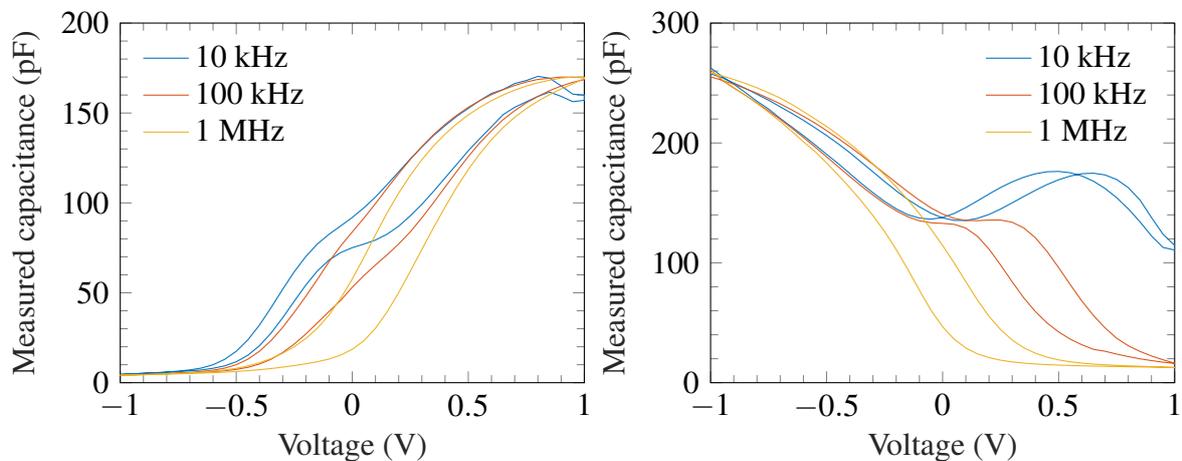
Fig. 4.11 CV characteristics of an as-deposited Al$_2$O$_3$ on n- and p-type germanium.

for the forward and reverse voltage sweep. Comparing the frequency response, it can be seen that the electrons in p-type germanium have a faster response to the AC signal than holes in n-type germanium at 10 kHz. This can be seen in the CV characteristics as the capacitance for the p-type MOS begins to shown weak inversion at 10 kHz unlike holes in the n-type MOS which only produce a small knee in the CV profile at -0.2 V. In comparing the accumulation capacitance however, it can be seen that the n-type MOS reaches accumulation whereas the p-type MOS still has not achieved accumulation indicating a high concentration of interface traps near the band edge [226].

In order to reduce the hysteresis and interface trap density, a forming gas anneal (FGA) was performed on the as-deposited Al$_2$O$_3$ capacitors at 400 °C for 5 minutes. A comparison of the CV and D$_{it}$ for pre and post FGA can be seen in figure 4.12. It can be seen that the hysteresis is almost removed from the CV profile. As well as this, the minimum capacitance in depletion has increased by ∼4 times following the FGA. As shall be covered later in section 4.4.3 when observing the ZrO$_2$ characteristics, the increase in capacitance in depletion can be attributed to diffusion of impurities from the Al$_2$O$_3$ into the surface of the germanium.
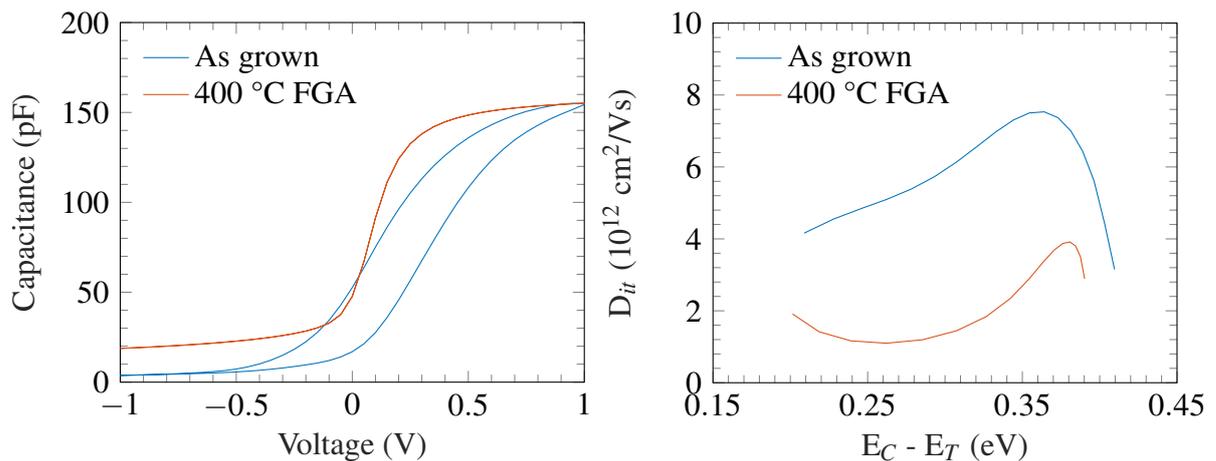
Fig. 4.12 Comparison of the CV ad interface trap density profile the n-type Al$_2$O$_3$ MOS capacitor before and after a 400 °C FGA.

Using the Terman method, the interface state density as a function of position near the centre of the band gap is also plotted in figure 4.12. Following the FGA, the interface state density decreases by ~2 times at mid gap. This indicates that the majority of charge contributing to the hysteresis in the CV profile was due to the presence of oxide trapped charge [226] which is evaporated from the oxide following a high temperature anneal [227, 228].

A comparison of the leakage current density pre- and post-FGA anneal can be seen in figure 4.13. From the data, it can be seen that the oxide leakage is more predominant in the forward bias regime for the n-type devices than the p-type devices, whereas the current density for the negative bias is greater for the as-deposited p-type MOS than the as-deposited n-type MOS. Annealing the n-type MOS results in an increase in current density for forward and reverse bias as well as a reduction in hysteresis consistent with the CV characteristics. The increase in current density could be attributed to multiple effects including an increase in oxide pin-hole density [229], Fermi level de-pinning at the semiconductor surface [230], or an increase in tunnelling current [231, 130] due to an increased carrier concentration at the interface. The de-pinning of the Fermi-level at the semiconductor surface appears to be the
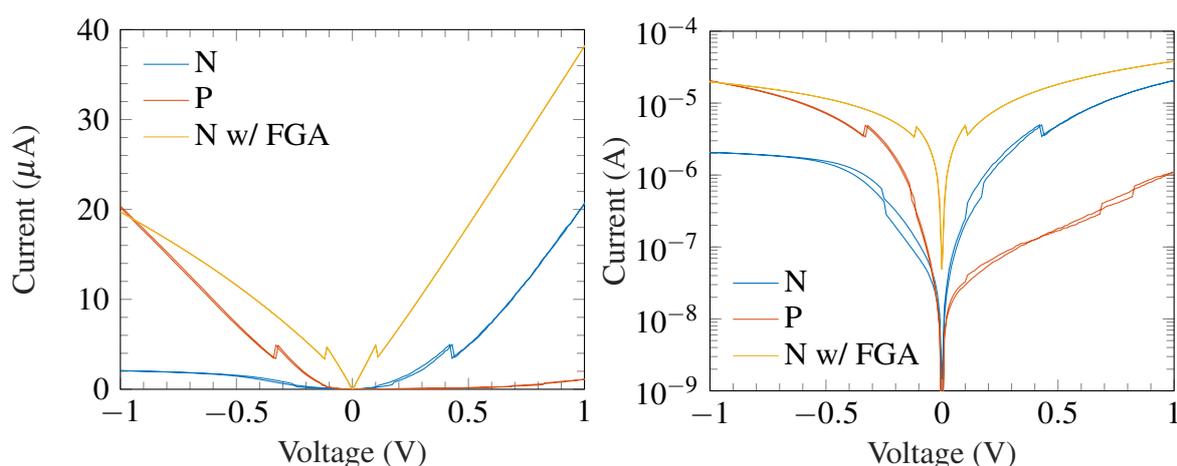
Fig. 4.13 Leakage comparison of Al_2O_3 capacitors on n- and p-type germanium. Also plotted is n-type germanium after a 400 °C FGA for comparison.

most probable cause as the ratio in positive and negative current density decreases following the FGA from 10 to 1.9. As the focus of this work is to model the characteristics of high-κ dielectrics incorporating a GeO$_2$ interlayer, this was not considered further.

4.4.3 Ge/Al$_2$O$_3$ and Ge/ZrO$_2$ characteristics

The corrected CV characteristics of both n- and p-type germanium MOS capacitors with a germanium oxide interlayer grown prior to Al$_2$O$_3$ deposition can be seen in figure 4.14 as well as this the characteristics of the ZrO$_2$ for comparison. Comparing the Al$_2$O$_3$ and ZrO$_2$ devices directly, it can be seen that the oxide capacitances of the ZrO$_2$ device are much greater than that of any Al$_2$O$_3$ device which is due to the greater dielectric constant of ZrO$_2$. Unfortunately, despite this, it can be seen that a much higher voltage of +3/-3 is required in order to achieve accumulation/inversion for the ZrO$_2$ device in comparison to the Al$_2$O$_3$ devices. As covered in section 4.4.3, this is due to the considerably greater interface density which results from the formation of low quality GeO$_x$ following oxidation of zirconium films on germanium.

Unlike the Al$_2$O$_3$ devices deposited with no GeO$_2$ interlayer, the Al$_2$O$_3$ devices with a GeO$_2$ interlayer are capable of achieving weak inversion at frequencies below 1 MHz, indicating a greater surface quality and higher minority carrier lifetime [226]. Comparing the frequency response of the Al$_2$O$_3$/GeO$_2$ devices directly, it can be seen that the MOS capacitors grown on p-type germanium fully invert at a frequency of 10 kHz whereas only two-thirds of the oxide capacitance is achieved for the same frequency on n-type germanium. The reason for this is due to the higher mobility of minority electrons in p-type germanium compared to minority holes in n-type germanium [232]. The lower minority hole mobility is due to a higher effective mass and higher Coulombic scattering of holes in germanium from phonons compared to electrons [172, 233]. As a result of this, even if both devices have identical interfaces, the channel and accumulation resistance of these interfaces would be

(a) Al$_2$O$_3$/GeO$_2$/n-Ge

(b) Al$_2$O$_3$/GeO$_2$/n-Ge

(c) Al$_2$O$_3$/GeO$_2$/p-Ge

(d) Al$_2$O$_3$/GeO$_2$/p-Ge

(e) ZrO$_2$/GeO$_2$/n-Ge

(f) ZrO$_2$/GeO$_2$/n-Ge
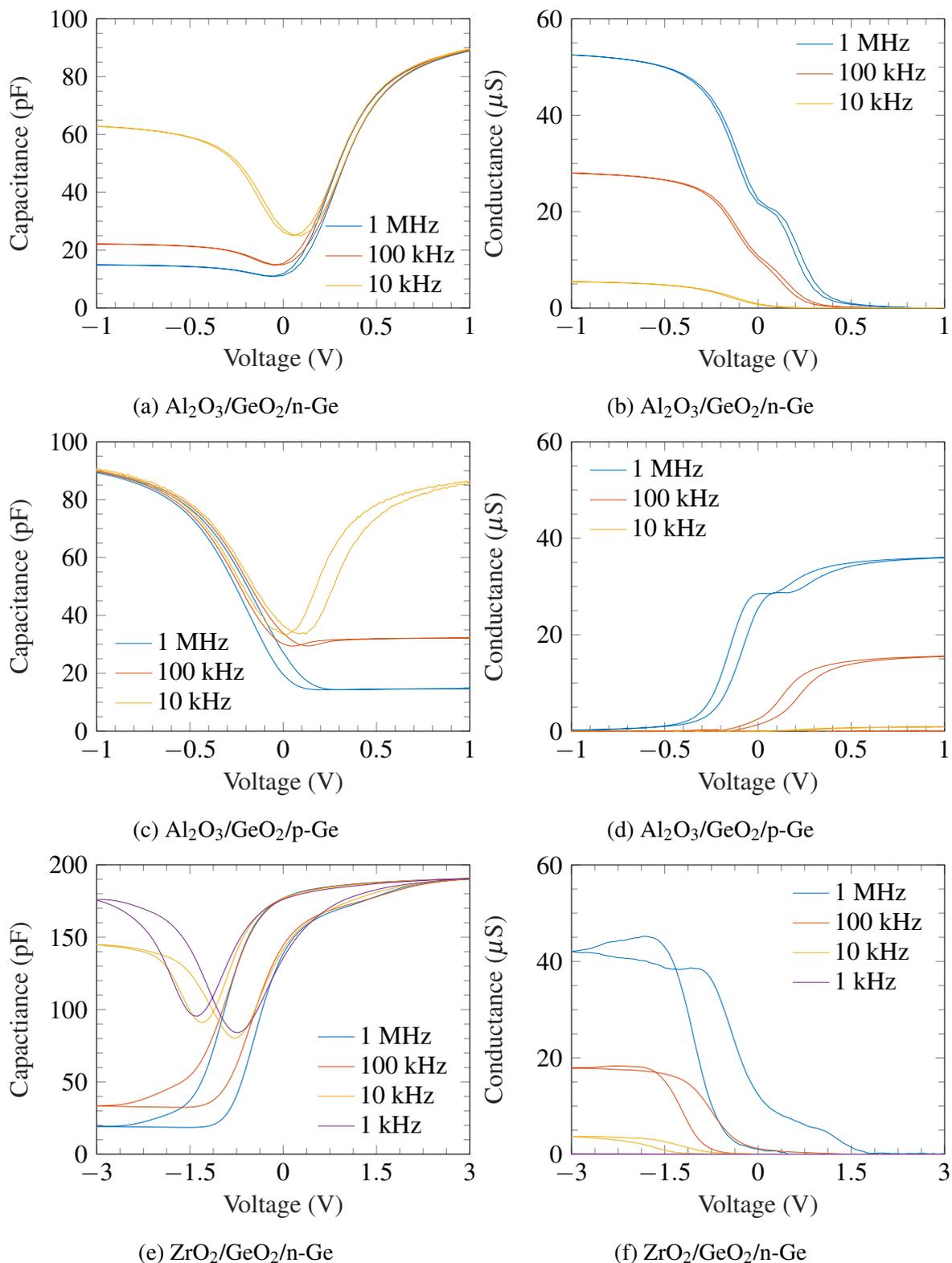
Fig. 4.14 (a-d) CV and GV of N and P type germanium with 10nm Al$_2$O$_3$ and a thermal GeO$_2$ oxidised at 475 °C before Al$_2$O$_3$ deposition. (e-f) CV and GV of ZrO$_2$ oxidised on germanium at 550 °C.

higher in unipolar hole devices compared to unipolar electron devices due to the mobility term in equation 4.2.

Considering the hysteresis however, it can be seen that the forward/reverse measurement of the CV data for the n-MOS is lower than the p-MOS device. Hysteresis can indicate traps at the interface, fixed charge within the oxide, or both. As the hysteresis was consistent over multiple devices on both n- and p-type germanium, it can be assumed that the concentration of charge trapped within the oxide is equal for both samples. As a result, the cause of the difference in hysteresis is due to a difference in minority carrier mobility and response time. The lifetime of minority carriers within traps decreases exponentially with trap energy [15]. As minority electrons in p-type germanium MOS capacitors are generating greater hysteresis, it can be assumed that a larger density of traps is located close to the valence band edge in comparison to holes responding to traps near the conduction band edge. In order to determine whether the majority of traps were located near the valence band edge, the Terman method was employed based on the experimental results shown in figure 4.14 as well as samples that
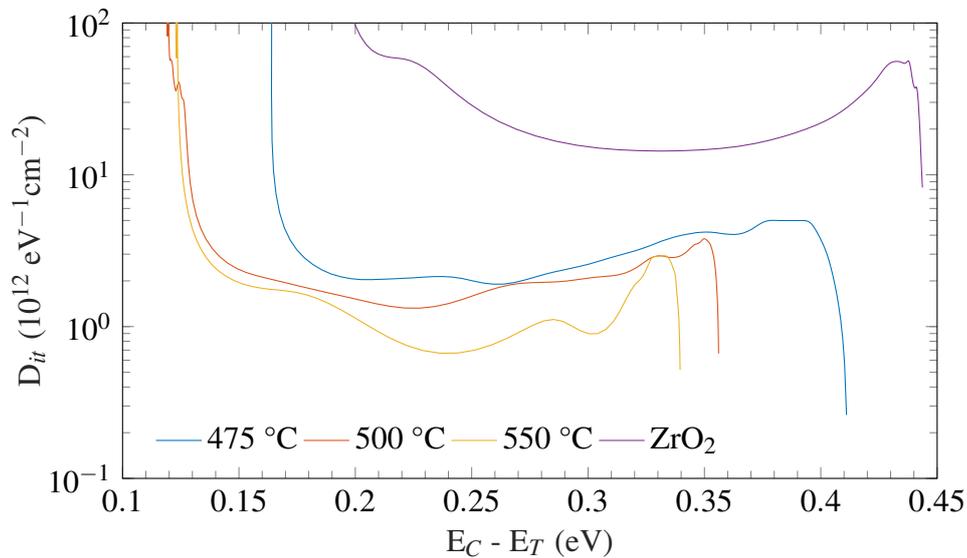
Fig. 4.15 Interface trap density as a function of position in the band gap with mid-band given as ~0.3 eV.

were prepared at oxidation temperatures of 500 and 550 °C. The interface density can be seen in figure 4.15.

It can be seen that the interface density at mid band gap is minimum for the samples that were oxidised at 550 °C. The interface trap density is lower in all GeO_2/Al_2O_3 samples compared to the Al_2O_3 samples without an interlayer. It can be seen that the oxidation of Zr on germanium produces a high interface state density in comparison to deposited Al_2O_3 on oxidised germanium, although it is common for ZrO_2 devices to have a greater D_{it} in comparison to devices incorporating Al_2O_3 [205]. The thermally oxidised ZrO_2 devices demonstrate a D_{it} within 2-3 times the best recorded values in literature [27, 28].

X-ray photoelectron spectroscopy scans of ozone oxidised zirconium show the formation of a GeO_2 oxide of approximately 1 nm thickness at the ZrO_2/Ge interface [234]. A study into the effect of germanium concentration in sputtered ZrO_2 [235] indicates that no unique peaks attributed to the possible formation of a ZrGeO alloy are observed, suggesting that there is no mixing of the ZrO_2 and GeO_2 oxide layers during the oxidation process. As a result, the high interface state density is attributed to the formation of a low quality GeO_x sub-oxide at the ZrO_2/Ge interface during the thermal oxidation process.

4.5   Oxide leakage in $ZrO_2/GeO_2/Ge$

The leakage current density of ultra-thin oxides on semiconductors is a crucial area of research. As explained in section 4.1.1, the oxide capacitance must be maximised in order to maximise the conductivity of MOS devices. Originally this was achieved through reducing the oxide thickness, although this can result in detrimental current leakage through the oxide leading to a loss of gate control. In order to further increase the oxide capacitance without reducing the oxide thickness, high-κ dielectrics have been proposed as alternatives to native oxides although the temperature dependence of the leakage through these has yet to be documented for germanium MOS capacitors. For silicon MOS devices, the leakage

current is shown to reduce by over 3 orders of magnitude in Al_2O_3 devices [236] from room temperature down to 77 K, whereas the leakage current reduces by less than an order of magnitude when using SiO_2 and Si_3N_4 dielectrics [237, 238]. To the authors' knowledge, for germanium devices, the leakage current density for Ge/Al_2O_3 is the only documented research on the low-temperature leakage characteristics of germanium MOS devices [202]. As a result, the temperature dependence of the ZrO_2 was analysed.

The IV characteristics for the ZrO_2 devices can be seen in figure 4.16 as a function of temperature. The IV measurements were performed at multiple temperatures in approximate steps of 25 K from 77 K to room temperature but only 4 measurements are shown for the
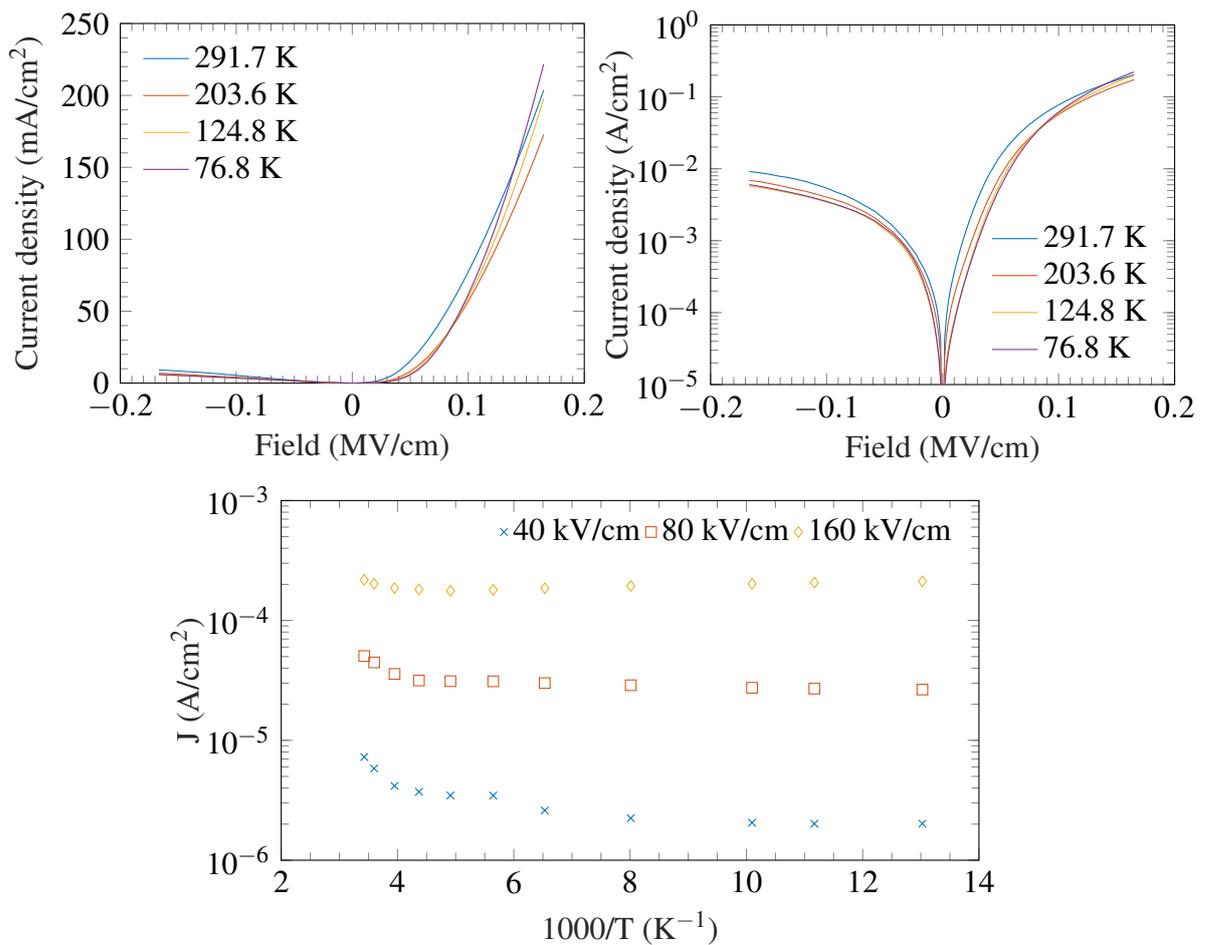
Fig. 4.16 Leakage current density as a function of applied field in ZrO_2/GeO_2/n-Ge devices and temperature.

sake of clarity. The IV data was converted to current density versus applied field (JF) by dividing through by the contact metal area and dividing by the oxide thickness respectively. The JF characteristics in the forward direction are greater than the negative direction by a factor of $\sim$25 suggesting a difference in the barrier height of the metal and semiconductor in comparison to the oxide conduction band. At high fields, the temperature dependence of the current density decreases suggesting that the current density becomes dominated by Fowler-Nordheim tunnelling current density at high fields [237, 202].

In order to analyse the temperature dependence of the JF characteristics, the leakage current density in the forward direction was plotted against the inverse of temperature and can be seen in figure 4.16. It can be seen that as the electric field increases, the temperature dependence of the leakage current decreases. At a field of 160 kV/cm, it can be seen that leakage current density becomes temperature independent with only a slight increase in the current density at temperatures above 250 K. In contrast to this, the leakage current density at a field of 40 kV/cm can be seen to first exponentially decrease as function of temperature from room temperature before reaching a temperature independent value at temperatures below 125 K. This is consistent with the measurements of leakage current density in Si_3N_4 on silicon [237]. The difference in temperature dependence of the leakage current density suggests that the transition of one current mechanism to another occurs at different temperatures for different electric fields.

The leakage current density through gate dielectrics of MOSFETs, IGBTs, and MOS capacitors can occur from one of five mechanisms. These current mechanisms include Ohmic conduction, thermionic emission, Poole-Frenkel conduction, Fowler-Nordheim tunnelling and direct tunnelling. Each mechanism dominates at different fields and temperatures.

Poole-Frenkel, thermionic emission and ohmic conduction dominate at room to high temperatures as they are based on the hopping of carriers either over the oxide barrier or hopping from defects within the oxide [237, 239, 240]. All of these mechanisms dominate at

high temperatures and have not been considered for the low-temperature analysis. At low temperatures, the dominating current mechanisms are that of Fowler-Nordheim and direct tunnelling [237, 202]. As shown in figure 4.17, at low fields, the current density through the oxide requires tunnelling of carriers through the oxide barrier which has a width equal to the oxide thickness. At high fields, the barrier begins to bend down and the shape of the barrier becomes triangular resulting in a lower width for tunnelling to occur.

The total current density through the oxide can be expressed as

$$J_{Tun} = J_{DT} + J_{FN} \tag{4.20}$$

where J_{DN} and J_{FN} are the direct tunnelling and Fowler-Nordheim tunnelling current density respectively. When modelling tunnelling currents, the transmission probability of carriers from the semiconductor to metal must be considered. For low fields, the calculation of the tunnelling coefficient for all carriers at all energies near the oxide interface is non-trivial requiring precise knowledge of the Fermi-level of the metal [135]. For degenerate carrier
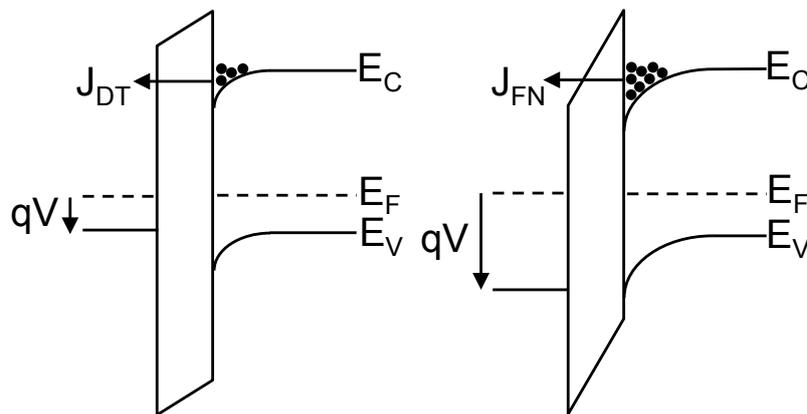
Fig. 4.17 Band diagram illustration of direct (J_{DT}) and Fowler-Nordheim (J_{FN}) tunnelling in a MOS system.

concentrations at the interface, the direct tunnelling current can be approximated as [241–243]

$$J_{DT} = \frac{AF_{ox}^2}{\left(1 - \sqrt{\frac{\phi_s + qV_{ox}}{\phi_s}}\right)^2} \exp\left(-\frac{B}{F_{ox}} \frac{\phi_s^{3/2} - qV_{ox}}{\phi_s^{3/2}}\right) \tag{4.21}$$

and the Fowler-Nordheim current density can similarly be approximated to

$$J_{FN} = AF_{ox}^2 \exp\left(-\frac{B}{F_{ox}}\right) \tag{4.22}$$
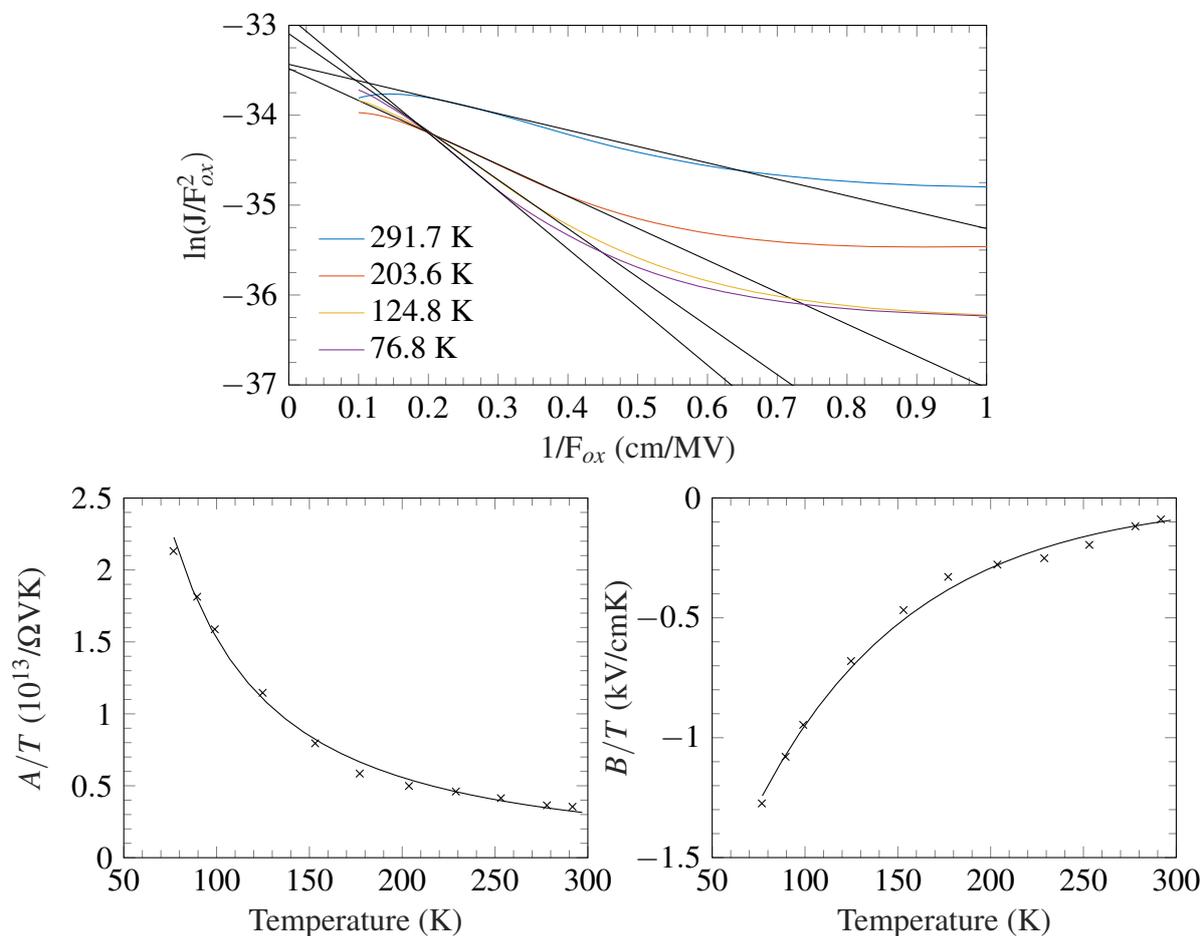
Fig. 4.18 Temperature dependence of coefficients A and B determined from ZrO_2 leakage data.

where F_{ox} is the oxide field, V_{ox} is the applied potential, and ϕ_s is the energy difference between the semiconductor at the oxide interface to the oxide. The constants A and B are dependent on the energy barrier from carriers tunnelling from the semiconductor to the metal. Although the tunnelling probability is temperature independent, the temperature dependence of the tunnelling current densities is due to the change in carrier concentration at the oxide/semiconductor interface and semiconductor barrier height. In plotting $\ln(J/F_{ox}^2)$ against the reciprocal of the field, the coefficients A and B can be found from the slope and fit of the data [243, 241].

A plot of the $\ln(J/F_{ox}^2)$ vs $1/F_{ox}$ for the ZrO$_2$/n-Ge devices can be seen in figure 4.18. From the data, it can be seen that at high fields, current densities at low temperatures appear temperature independent. As the electric field decreases, the difference in $\ln(J/F_{ox}^2)$ at low temperatures compared to room temperature increases. In order to model the temperature dependence of the coefficients for simulation, it was found that the coefficients could be modelled using

$$\frac{A}{T} = 3.71 \times 10^{-14} T^{-1.46} \tag{4.23}$$
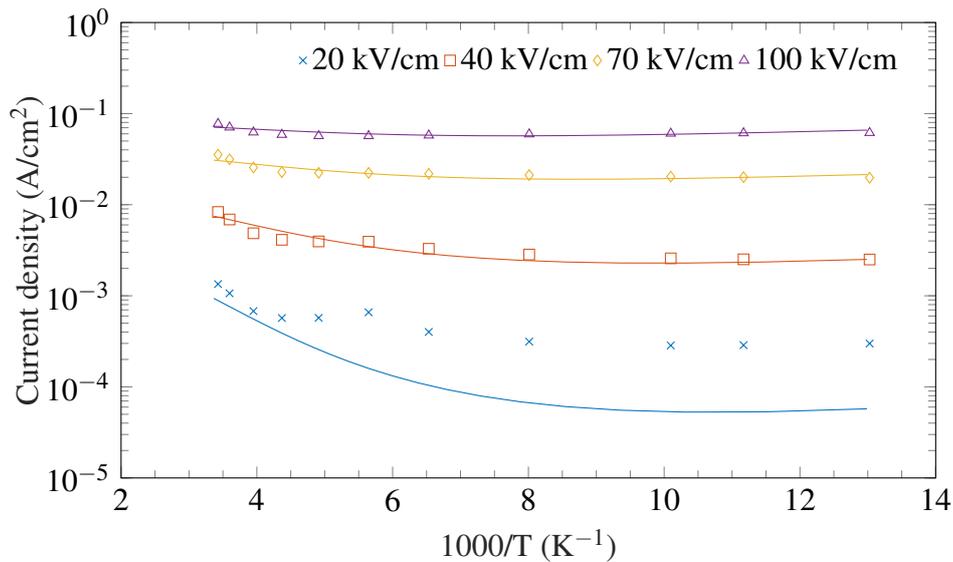
Fig. 4.19 Comparison of the current density based on Fowler-Nordheim tunnelling to leakage current measured in the ZrO$_2$/GeO$_2$/n-Ge MOS capacitor.

and

$$\frac{B}{T} = -1.81 \times 10^4 \exp\left(-\frac{T}{89.2}\right) \tag{4.24}$$

based on a best fit to the data points in figure 4.18. In order to check the validity of the models, the theoretical current density based on the Fowler-Nordheim current density was compared with the measured experimental current density as a function temperature in figure 4.19. As the thickness of the ZrO_2 oxide is of the order of 50 nm, it was assumed that the majority of the current density was a result of tunnelling from the reduced barrier width following the applied field given by the Fowler-Nordheim model. A good fit can be seen between the Fowler-Nordheim model and the measured data for fields at and above 40 kV/cm. For low fields however, the model underestimates the current density and this is believed to be due to the omission of ohmic conduction at high temperatures and direct tunnelling at low temperatures/low fields. As the devices in this study are to be operated in strong inversion or strong accumulation at low temperatures, this discrepancy in the model is not detrimental to the overall model of germanium MOS devices at cryogenic temperatures.

4.6   Conclusion

The theoretical and experimental CV, GV and leakage characteristics of fabricated germanium MOS capacitors were measured as a function of temperature with oxide stacks of Al_2O_3, Al_2O_3/GeO_2 and ZrO_2/GeO_2. Al_2O_3 MOS capacitors with no GeO_2 have the lowest hysteresis of all devices fabricated within this work although CV characteristics show that these devices cannot achieve inversion even at frequencies as low as 10 kHz. In comparison, Al_2O_3/GeO_2 and thermally oxidised ZrO_2/GeO_2 devices are capable of complete inversion at frequencies of 10 kHz for all devices. It was shown for the first time that ZrO_2 devices can be fabricated through the thermal oxidation of zirconium on germanium although this does lead to the formation a GeO_x sub-oxide which results in a high D_{it} in comparison to the

Al_2O_3/GeO_2 devices. Despite this, the thermal oxidation method for fabricating ZrO_2 from Zr on germanium has resulted in D_{it} values that are within 2-3 times the best reported values in literature without a post deposition anneal. Further reading into literature shows that for all MOS device fabrication, the D_{it} can be reduced through fabrication optimisation and post oxidation annealing leading to a potential reduction by over an order of magnitude. Despite this, the oxide capacitance of the ZrO_2 was more than twice that of the Al_2O_3 devices whilst also having a much greater oxide thickness of 50 nm compared to the Al_2O_3/GeO_2 which have a thickness of ~20 nm. The leakage current density of ZrO_2 as a function of temperature was observed for the first time on germanium where the Fowler-Nordheim current density model was able to accurately model the temperature dependence of the current density for fields above 40 kV/cm. The benefits of the results here show that thermal oxidation of ZrO_2 can produce MOS capacitors with comparable quality to ALD deposited Al_2O_3 MOS capacitors.

Chapter 5

TCAD simulation of germanium power diode and vertical ZrO$_2$ n-type MOSFETs

5.1 Drift-diffusion model for TCAD simulation

The closed-loop equations provided in the previous chapters may model each component of a device, but that is not to say that a combination of all of these effects may lead to unexpected characteristics at cryogenic temperatures. Technology computer aided design (TCAD) allows the characteristics of electronic devices to be simulated through modelling the physical properties of the materials and techniques used during fabrication.

Device simulations are performed by first defining a set of coordinates within a defined device structure that is then used to calculate the current density

$$\vec{J} = \vec{J}_n + \vec{J}_p \tag{5.1}$$

where $\overrightarrow{J}_\text{n}$ and $\overrightarrow{J}_\text{p}$ are the electron and hole current densities that must be solved numerically through the electron-hole continuity equations

$$\nabla \cdot \overrightarrow{J}_\text{n} = qR_\text{net} + q\frac{\partial n}{\partial t} \tag{5.2a}$$

$$-\nabla \cdot \overrightarrow{J}_\text{p} = qR_\text{net} + q\frac{\partial p}{\partial t} \tag{5.2b}$$

where t is time and R_net is the net recombination rate. The recombination rate is only present within regions of a device where the electron-hole product is greater than the intrinsic carrier concentration ($np > n_i^2$). Using the Shockley-Read-Hall model, the net recombination rate can be expressed as [244, 15, 245]

$$R_\text{net} = \frac{np - n_\text{i}^2}{\tau_p\left(n + n_1\right) + \tau_n\left(p + p_1\right)} \tag{5.3}$$

where n_i is the intrinsic carrier concentration, $\tau_{n/p}$ is the minority carrier lifetime for minority electrons/holes and n_1 and p_1 are given by

$$n_1 = n_\text{i}\exp\left(\frac{E_\text{trap}}{k_\text{B}T}\right) \tag{5.4a}$$

$$p_1 = n_\text{i}\exp\left(\frac{-E_\text{trap}}{k_\text{B}T}\right) \tag{5.4b}$$

where E_trap is the energy level of traps within the band gap which act as recombination centres.

In the instance that the recombination rate is negligible and the current density is perpendicular to the direction of the applied electric field, the current density given by equation (5.2) will simplify to a one-dimensional drift current which has a closed-loop form for simpler devices such as PiN diodes. The structure of PiN diodes allows for a one-dimensional analysis, whereas a two-dimensional analysis must be taken into consideration for power MOSFETs.

5.2   Germanium PiN diode simulation and characterisation

As covered in section 2.2, when using MOSFETs (or any type of FETs) in a high power switching circuit, a free-wheeling diode must be placed in parallel with each MOSFET to ensure that the diode can discharge the large potential generated during device switching [246]. The diode must have a significant breakdown voltage in excess of the supply voltage and must also have sufficiently low resistance to allow the current to free-wheel during the MOSFET switching phase. As germanium was initially considered for high current BJTs and low-temperature thermometers [19, 247], there has yet to be any documented results for germanium PiN diodes with breakdown voltages in excess of 100 V as devices with doping concentrations in the region of 10^{14} cm^{-3} are primarily PiN photodetectors which commonly have drift region lengths in the order of microns. As such, the on-state characteristics of germanium PiN diodes for free-wheeling applications with breakdown voltages in excess of 100 V at cryogenic temperatures must be considered.

5.2.1   Minority carrier concentration and lifetime

For majority carrier devices, such as MOSFETs, the dominant current mechanism is that of the drift current from majority carriers. The material-dependent parameters that determine the overall current density for these type of devices is the majority carrier mobility and carrier concentrations that were covered in chapter 3. In minority carrier devices such as PiN diodes, or in regions of a device where the conduction from minority carriers is non-negligible, modelling of the total concentration of minority carriers and their lifetime must be taken into account in order to accurately predict the total current density.

The total concentration of carriers in a semiconductor in thermal equilibrium is given by

$$n_i^2 = pn \qquad (5.5)$$

where n_i is the intrinsic carrier concentration and the free electron and hole concentrations can be computed using the models discussed in chapter 3. Considering the n-type region within a PN diode, at room temperature this can be approximated as

$$n_i^2 = p_{n0} n_{n0} \tag{5.6}$$

where the subscript n denotes the region and 0 denotes equilibrium conditions. From this, the concentration of holes within the n-type region equilibrium conditions is

$$p_{n0} = \frac{n_i^2}{n_{n0}} \tag{5.7}$$

Using the same logic, the electron concentration can be calculated in the p-type region based on the n_i and $_{p0}$. Following the application of a bias, the concentration of minority carriers at the edge of the depletion region increases according to

$$p_n = p_{n0} \exp\left(\frac{qV}{k_B T}\right) \tag{5.8}$$

where V is the applied bias.

The increase in minority carrier concentration at the edge of the depletion region results in the formation of a carrier concentration gradient resulting in the diffusion of carriers. Assuming that the concentration of carriers is uniform in the y- and z-direction, the diffusion current will only flow in the x-direction. The contribution from the hole and electron concentration gradients can therefore be given by

$$J_p = \frac{qD_p p_{n0}}{L_p}\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{5.9a}$$

$$J_n = \frac{qD_n n_{p0}}{L_n}\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{5.9b}$$

where D_n and D_p is the diffusivity of minority electrons and holes which can be calculated from the Einstein relation

$$D_n = \frac{k_B T}{q} \mu_e \text{ and } D_p = \frac{k_B T}{q} \mu_h \tag{5.10}$$

and L is the diffusion length given by

$$L_n = \sqrt{D_n \tau_n} \text{ and } L_p = \sqrt{D_p \tau_p} \tag{5.11}$$

where τ is the minority carrier lifetime.

Combining J_n and J_P results in the total current density for a PN diode as

$$J = J_n + J_p = J_0 \left[\exp\left(\frac{qV}{k_B T}\right) - 1 \right] \tag{5.12}$$

with

$$J_0 = \frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} = qn_i^2 \left[\frac{D_n}{L_n p_{p0}} + \frac{D_p}{L_p n_{n0}} \right] \tag{5.13}$$

expressing this in terms of the material-dependent properties results in the expression

$$J_0 = n_i^2 \sqrt{k_B T q} \left[\frac{1}{p_{p0}} \sqrt{\frac{\mu_e}{\tau_n}} + \frac{1}{n_{n0}} \sqrt{\frac{\mu_h}{\tau_p}} \right] \tag{5.14}$$

ignoring the influence of a series of resistance and field-dependent mobility. Although the field dependence of the carrier mobility has not been considered in the derivation, it can be seen that the total current density within a PN diode is dependent on both the electron and hole minority carrier concentrations and lifetimes. In order to simulate the current density of PiN diodes at cryogenic temperatures, the minority carrier lifetime and the variation with temperature must be considered.

The temperature dependent terms in equation (5.13) are the diffusivity, diffusion length, free carrier concentration and minority carrier concentration. The diffusivity can be modelled using equation (5.10) in tandem with the Philips unified mobility model and saturation velocity model derived in Chapter 3. As well as the carrier mobility, the majority carrier concentration can be modelled through equations 3.20 and 3.21 assuming dopants with single energy levels.

In a similar manner to the scattering mobilities described in section 3.4, the minority carrier lifetime cannot be accurately determined from first principles and must be extracted from experimental data. Experimental results for the minority carrier lifetime have been published for the majority of semiconductors [248, 245, 249, 250] and the temperature dependence of the minority lifetime can be modelled using [251]

$$f(T) = \frac{\tau_T}{\tau_0} = \exp\left[c\left(\left(\frac{T}{300}\right) - 1\right)\right] \tag{5.15}$$

where τ_0 is the room temperature carrier lifetime, c if a fitting constant and τ_{dop} takes into account the doping dependence according to [248]

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^\gamma} \tag{5.16}$$

where τ_{min}, τ_{max} and N_{ref} are all fitting parameters. Once τ_T and τ_{dop} have been determined, the total minority carrier lifetime can be calculated using

$$\tau_i = \tau_{dop} \frac{f(T)}{1 + g_c(F)} \tag{5.17}$$

where the subscript 'i' is altered to 'e' for electrons or 'h', the factor $1 + g_c(F)$ takes into account the field dependence of the minority carrier lifetime [252]. Initially, the field
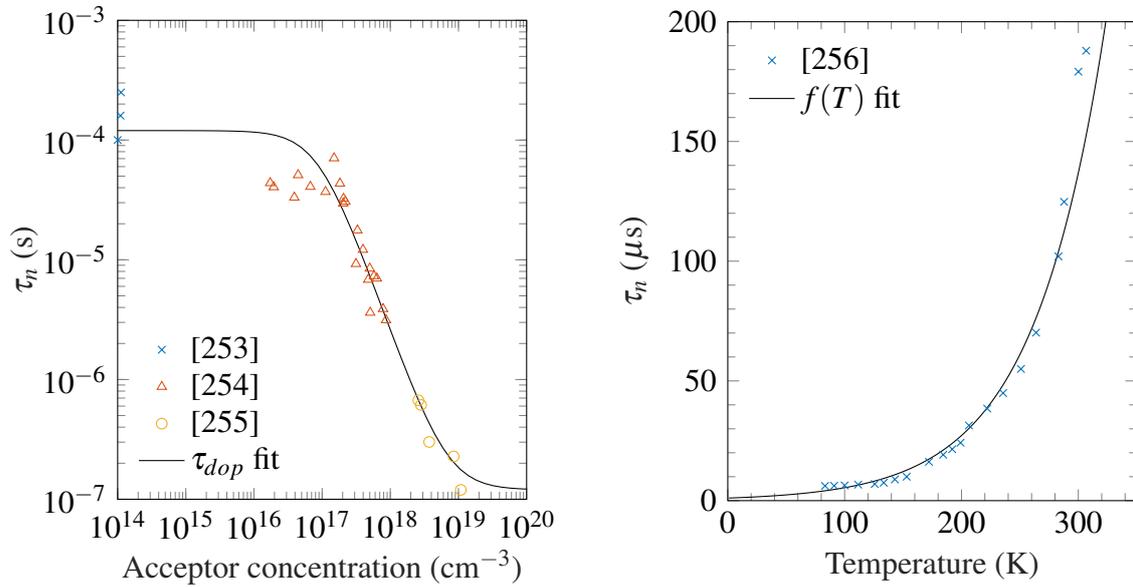
(a) Doping dependence of electron lifetime in p-Ge. (b) Temperature dependence of electron lifetime.

Fig. 5.1 Doping and temperature dependence of the electron minority lifetime in germanium as a function of doping and temperature.

dependence of the minority carrier lifetime will be assumed to be negligible ($g_c(F) = 0$) and will only be considered if there is a considerable discrepancy generated from this.

Data for the minority carrier lifetime of Si [248, 245, 249] and 4H-SiC [250] has already been well documented and is ready built into TCAD but this has yet to be performed for Ge. The minority carrier lifetime of electrons in p-Ge is plotted in figure 5.1a along with the relevant experimental data. Unfortunately, despite a range of experimental results for the lifetime of holes in n-Ge, no data can be found for hole lifetime in n-Ge with doping concentrations exceeding 10^{16} cm^{-3}. The experimental values of hole lifetime in n-Ge ranges from 10 to 200 μs [253, 257–259] and for the purposes of the work here, a dopant independent value of 100 μs was used.

The temperature dependence of the minority carrier lifetime for electrons is plotted in figure 5.1b with values of 136.9 μs for τ_0 and 4.85 for the constant c in equation (5.15). As with the doping dependence, experimental measurements of the temperature dependence of

the hole minority lifetime cannot be found and so it will be assumed to follow the same trend as the electron minority lifetime.

5.2.2 PiN diode structure

The structure of the simulated germanium PiN diode and meshing can be seen in figure 5.2. The doping profile at the anode and cathode contacts were used to generate an ohmic contact similar to the methods commonly used for silicon and 4H-SiC PiN diodes. The doping profile peaks at 10^{19} cm^{-3} for boron and antimony at the anode and cathode respectively which decay exponentially from the surface to match the doping profile values for ohmic contacts in literature [260, 261]. The doping concentration in the drift region is held at a constant value of N$_{drift}$ for a length of L$_{drift}$ which are both parameters that must be optimised in order to minimise the on-state resistance.

5.2.3 Effect of dopant geometry on device characteristics

Before optimising the drift region length and doping concentration for cryogenic applications, the structure of the doping profile must be considered. Typically, when fabricating PiN diodes, it is common to deposit a lightly doped epitaxial layer onto a highly doped N$^+$ wafer before creating the highly doped p-type region through ion implantation. During the ion implantation phase, it is common for a curved p-type profile to be produced during the fabrication process as shown in figure 5.3. It has been shown experimentally that a curved profile reduces the breakdown voltage of devices due to an abrupt increase in the electric field near these regions and is more severe for profiles with a sharper profile [262].

Firstly, in order to analyse the effect of dopant profile on device characteristics, the effect of the p-type region junction curvature was considered by simulating three devices with acceptor radii of ∞, 0.5 and 0.05 μm where the drift region length and doping concentration for the three devices were 100 μm and 2×10^{15} cm^{-3} respectively. In order to determine the
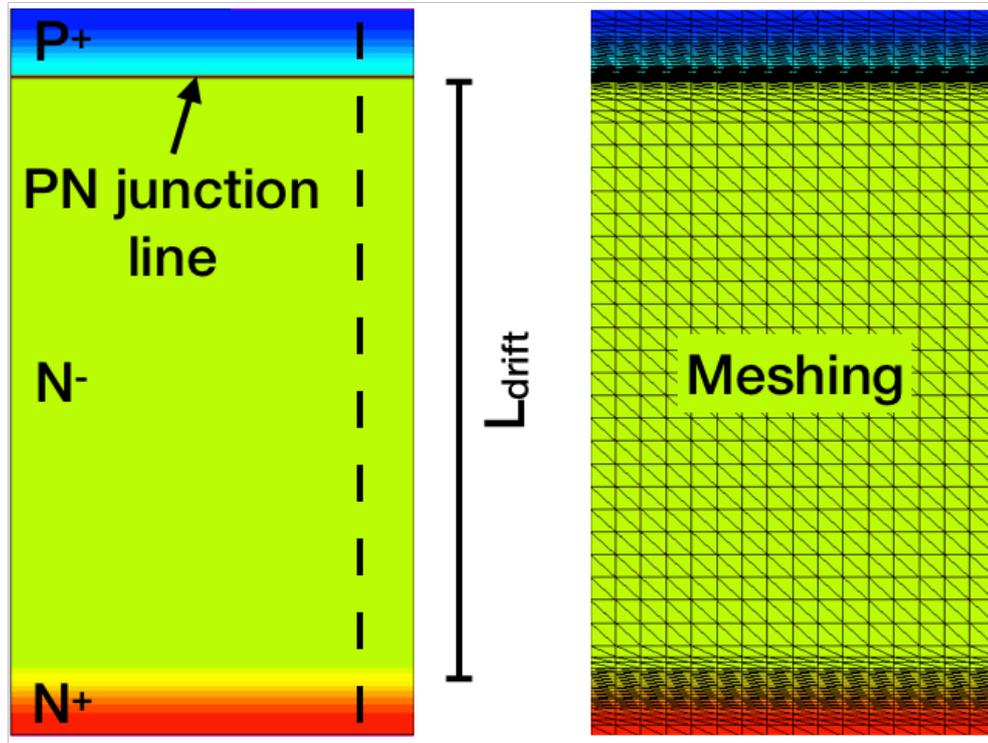
Fig. 5.2 Germanium PiN diode structure, meshing and doping profile. Dashed line on device structure gives doping profile. For each device the doping profile for the anode and cathode regions remained constant and the length and doping concentration of the drift region were varied during simulations.

breakdown voltage for the 3 devices, the commonly used multiplication factor method was employed [263, 264] in which avalanche is said to occur when

$$\int_0^{W_D} \alpha_p \exp\left[-\int_0^x (\alpha_p - \alpha_n) dx'\right] dx = 1 \qquad (5.18)$$

where $\alpha_{n/p}$ is the ionisation coefficients for electrons and holes which for germanium have been experimentally determined to be [265]

$$\alpha_n = 8.04 \times 10^6 \exp\left(-\frac{1.40 \times 10^6}{F}\right) \qquad (5.19)$$

and

$$\alpha_p = 6.39 \times 10^6 \exp\left(-\frac{1.27 \times 10^6}{F}\right) \qquad (5.20)$$

where F is the electric field. Each device was simulated from 0 to -1000 V at room temperature where the ionisation coefficients and resulting ionisation integral were determined at each voltage step. As well as the reverse characteristics, the forward characteristics were simulated from 0 to 1 V at room temperature in order to determine if there were any considerable effects on the device characteristics owing to the p-type region geometry.

The electric field distribution, forward and reverse characteristics of the germanium PiN diodes with varying p-type doping profiles can be seen in figure 5.3. Comparing the electric field distribution of the devices, it can be seen that at breakdown, the electric field is uniform in the x-direction for the p-region with no curvature ($r_A = \infty$) whereas the electric field peaks for the device with a curvature of 0.5 μm near the curve in the dopant profile. Comparing the two curved devices IV characteristics in the reverse direction, it can be seen that a sharper p-type profile results in a significant reduction in the breakdown voltage which is consistent with what has been found in literature. For shallow curvatures however, the reduction in breakdown voltage is not significant, reducing from 84 to 81 V, whilst a reduction to a curvature of 0.05 μm results in a significant drop in breakdown voltage to 53 V. Comparing

the forward characteristics, it can be seen that there is no significant alteration in the forward characteristics when considering alternative p-region geometries.

When considering the geometry of the p-region in the PiN diode, manufacturers often add guard rings to increase the breakdown voltage by reducing the crowding of the electric field near the curve of the p-region. The addition of these guard rings adds complexity to the device structure and simulation results. As the alteration in forward characteristics with different p-type region geometries is negligible, the effect of the region curvature at PN junction interfaces was not considered in subsequent simulations.
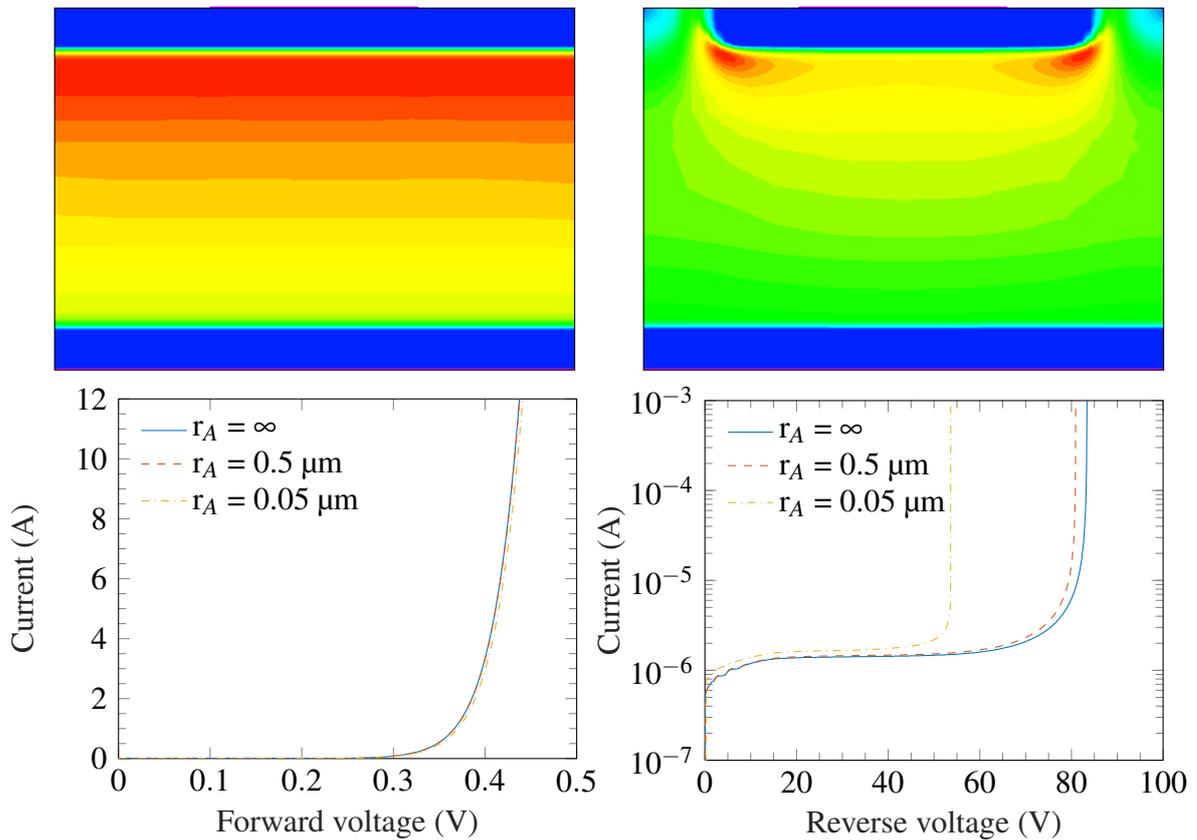
Fig. 5.3 Electric field for a continuous (top left) and a curved (top right) boron profile and resulting IV characteristics.

Drift region doping and length optimisation

In order for the on-state resistance of the PiN diodes to be minimised whilst also maintaining a suitably high breakdown voltage, the minimum drift length and maximum doping concentration for the drift region must be determined.

In order to determine the optimal length and doping concentration of the drift region, the breakdown voltage of multiple germanium diodes were simulated at room temperature with drift region lengths ranging from 3 to 250 μm and drift region doping concentrations ranging from 10^{14} to 10^{16} cm. Similar to the previous simulations considering p-region geometry, the device voltage was ramped from 0 to -1000 V and the ionisation integral was calculated at each voltage step using the ionisation coefficients formulas given by equation (5.19) and (5.20).

The extracted breakdown voltages for each simulation can be seen in figure 5.4 as a function of drift region doping concentration and length. By reducing the doping concentration, the breakdown voltage can be seen to increase for all devices below a doping concentration of 10^{16} cm^{-3} although this is eventually limited by the drift region length. The cause of the capped breakdown voltage is due to the punch-through effect from which, the depletion region extends to the heavily doped N^+ region and can extend no further resulting in a dramatic increase in electric field with decreasing voltage. The increased field leads to a premature electrical breakdown and limits the breakdown voltage of devices below a threshold doping concentration.

Also plotted in figure 5.4a is the approximation given by Sze and Gibbons. Based on calculated ionisation coefficients from germanium bipolar transistors [19] and other published data, Sze and Gibbons [23] developed an approximate expression for the breakdown voltage of germanium, silicon, GaAs and GaP to be

$$V_B = 60 \left(\frac{E_g}{1.1} \right)^{3/2} \left(\frac{N}{10^{16}} \right)^{-3/4} \tag{5.21}$$

which when evaluated for germanium gives

$$V_B = 2.79 \times 10^{13} N^{-3/4} \tag{5.22}$$

where N is the drift region doping concentration. From the figure, it can be seen that there is excellent agreement between the simulated breakdown voltages for all doping concentrations for devices that do not suffer from the punch-through effect and the theoretical trend. As well as this, the simulated breakdown voltages in the doping concentration range of 10^{15} to 10^{16} cm^{-3} match well with experimental data [19].

For the power applications considered in this work, devices are required which can support breakdown voltages in excess of 270 V, as a result, the maximum doping concentration for germanium PiN diodes is 5×10^{14} cm^{-3}. This will result in a high resistivity section of both power MOSFETs and PiN diodes although the results in figure 5.4b show that this can be
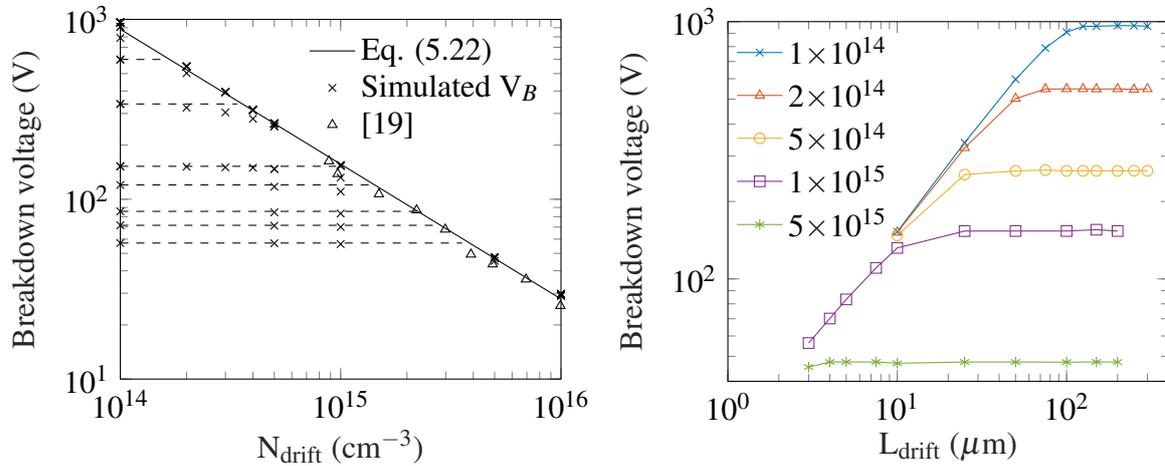
(a) Variation of breakdown voltage with drift region doping concentration. Dashed lines show capping due to L$_{drift}$.

(b) Variation of breakdown voltage with drift region length. Doping concentrations given in legend are in cm^{-3}.

Fig. 5.4 Breakdown voltage of germanium PiN diodes where the drift region length and doping concentration were varied. Both contacts were assumed to be ohmic with a 1 μm junction depth and a peak concentration of 10^{19} cm^{-3}.

minimised by using a drift length of 20 μm. Beyond this length, it will be possible to use a highly doped substrate to reduce the total resistance of the device.

Temperature dependence of ionisation coefficients

The ionisation coefficients for germanium have been determined at room temperature and when used in device simulations, they result in breakdown voltages that are in agreement with experimentally determined values. At cryogenic temperatures however, the ionisation coefficients of electron and holes increases leading to a reduction in breakdown voltage in power electronic devices [246, 266, 68]. Unfortunately, the experimental temperature dependence of the ionisation coefficients in germanium has not been published. Despite this, simulation results show that the breakdown voltage for germanium is expected to fall to 50% of the room temperature value for a doping concentration of 10^{14} cm^{-3} and 65% for doping concentrations of 10^{15} cm^{-3} [104, 263]. This reduction in breakdown voltage necessitates a lower drift region doping concentration of 2×10^{14} cm^{-3} and an increased drift region length to 45 μm in order to allow for the breakdown voltage to be in excess of 270 V at a temperature of 20 K. As the devices are primarily expected to work at 20 K, the effects of punch-through will cap the breakdown voltage at room temperature to 270 V although this is still acceptable for the application.

Forward characteristic

Following the drift region length and doping optimisation, a germanium PiN diode was simulated from room temperature down to 15 K with a drift region doping concentration of 2×10^{14} cm^{-3} and length of 45 μm. In order to perform an additional check on the results, the forward voltage was compared to experimental data for low voltage germanium PiN diodes [70]. In order to observe the effect of the drift region length on the series resistance, the PiN diode was also simulated with drift region lengths of 100 and 250 μm.
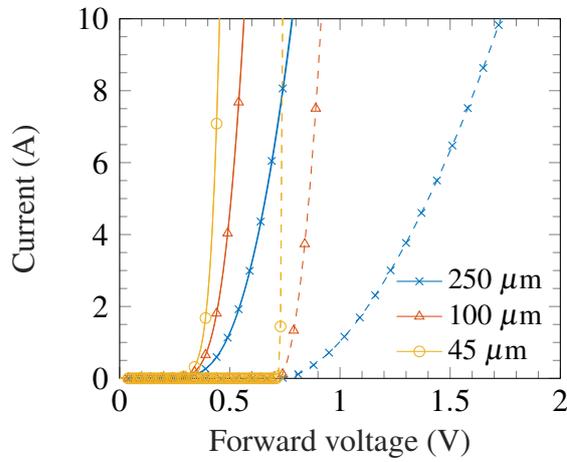
(a) Forward PiN diode IV at room temperature (solid) and 20 K (dashed)
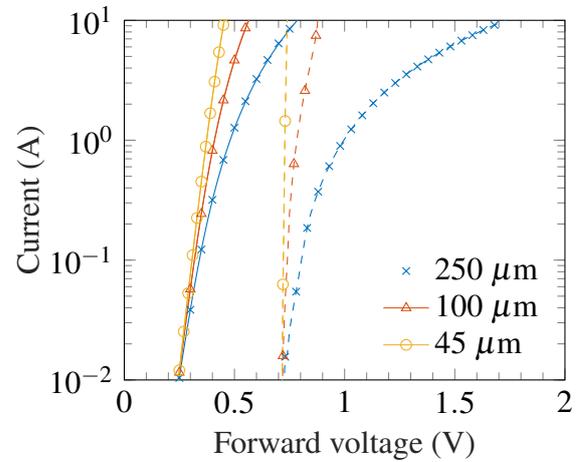
(b) Forward PiN diode IV at room temperature (solid) and 20 K (dashed)
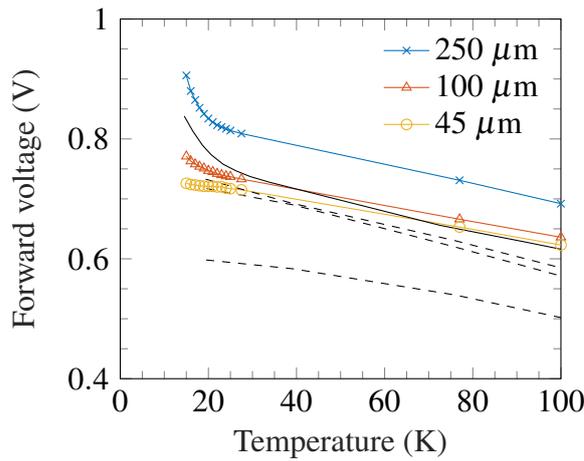
(c) Forward voltage of PiN diode at 0.2 A compared to experimental data for a germanium power diodes [70]
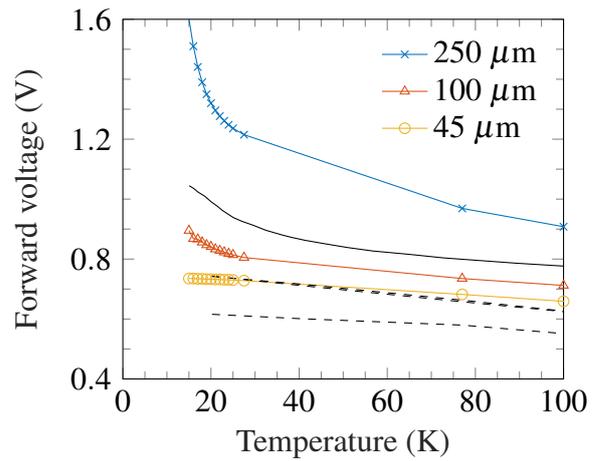
(d) Forward voltage of PiN diode at 4 A compared to experimental data for a germanium power diodes [70]

Fig. 5.5 Comparison of IV profile for germanium PiN diode for a drift region antimony concentration of 2×10^{14} cm^{-3} and varying drift region lengths (a,b). Forward voltage as a function of temperature is then compared to experimental data for germanium power diodes (c,d). Solid black line indicates experimental data for a a germanium power diode that was developed for cryogenic applications whilst dashed black lines show experimental data for commercial germanium power diodes. The drift region doping concentration and length have not been provided for the power devices [70].

The IV characteristics of the simulated germanium PiN diodes can be seen in figure 5.5a and 5.5b. For all devices, the reduction in temperate results in an increase in forward voltage at any current which is consistent with what is observed in commercial power devices [107, 103, 267]. As well as this, the leakage current can be seen to decrease for all devices as the temperature is reduced which is consistent with the reduction in intrinsic carrier concentration in equation (5.13). For a drift region length of 250 μm, it can be seen that there is an exponential increase in the forward voltage below 100 K in comparison to the near linear increases for the 100 and 45 μm devices. In order to analyse this trend further, the temperature dependence of the forward voltage at a forward current of 0.2 and 4 A was simulated for each device and can be seen in figure 5.5c and 5.5d in comparison to experimental data obtained by Ward [70].

From the data, it can be seen that the 45 μm device has an almost linear temperature dependence consistent with commercial power devices although the forward voltage at room temperature is around 0.1 V greater. At temperatures below 25 K, the cryogenic germanium PiN diode developed by Ward and the 100 and 250 μm devices exhibit an increase in the forward voltage due to the freezing out of carriers. The difference in the temperature gradient of the trends obtained from Ward and the devices simulated here are believed to be due to a difference in doping concentration in the drift and contact regions. As the trends presented by Ward closely resemble the trends simulated here, this was not studied further. From the TCAD simulation results, it can be seen that germanium PiN diodes with an intrinsic doping concentration of 2×10^{14} cm^{-3} are capable of supporting currents within the same order of magnitude of the room temperature characteristics with a breakdown voltage in excess of 270 V at 20 K. Further to this, these results show that a vertical germanium power transistors with breakdown voltages exceeding 250 V at a temperature of 20 K are achievable.

5.3   n-Type Vertical MOSFET

Although germanium based power MOSFETs are yet to be fabricated and measured, many reports on the transfer characteristics of lateral germanium MOSFETs have been published with native GeO_2 and high-κ gate oxides including Al_2O_3 and ZrO_2 [129, 198, 268]. As discussed in chapter 4, the benefits of a high-κ gate dielectric allows for a higher drain current density which can be seen through the MOSFET current equation which for an n-type MOSFET is given by

$$I_{D,sat} = \frac{W\mu_e C_{ox}}{2L}(V_G - V_T)^2 \tag{5.23}$$

where W/L is the width to length ratio of the MOSFET gate oxide, V_G is the gate voltage and V_{th} is the threshold voltage of the MOSFET which is the minimum voltage required on the gate in order for the device to turn on. As discussed in section 4.1, in order to maximise the conductivity of the channel, the mobility and oxide capacitance must be maximised. Whereas the oxide capacitance can be maximised through the placement of an oxide with a high dielectric constant, the carrier mobility within the channel can only be improved through pre- and post-treatment of the oxide/semiconductor interface.

5.3.1   Interface carrier mobility

Unlike carriers in the bulk region of a device, carriers at the oxide/semiconductor interface of MOS devices experience increased scattering from interface traps, surface phonon scattering and surface roughness [269]. A plot of the experimental effective carrier mobility within germanium n-type MOSFETs can be seen in figure 5.6 as a function of the reported inversion carrier density. From the data, it can be seen that the mobility peaks for inversion densities close to 10^{12} cm^{-2} and at densities above 5×10^{12} cm^{-2} the mobility decreases for all sets of data. The rate of decay for the electron mobility is dependent on the interface roughness and

temperature [192]. At low inversion carrier densities, the carrier mobility is dominated by the Coulombic scattering from interface and oxide trapped charge and ionised impurities.

By improving the interface quality, the Coulombic scattering resulting from interface and oxide trapped charge can be reduced increasing the low field mobility. By increasing the low field mobility, the device switching speed can be increased and as well as this, the leakage current of the MOSFET is reduced as the reduction of the interface trap density reduces the number of hopping sites for carriers. As a result, the mobility of carriers limited from surface roughness is not commonly considered as a high mobility at low transverse fields is a good indication of a low interface trap density [270, 188].

Despite this, it can be seen that the majority of devices follow a similar transverse field dependence within in the power range of -0.6 to -0.75 differing in a small range of $\sim$200 to $\sim$400 (cm^2/Vs) at an inversion concentration of 10^{13} cm^{-2}. In order to predict the performance of a vertical germanium power device, the best and worst case scenario of the surface roughness scattering must be considered from the reported experimental data.

Effective field mobility modelling

The theory for the scattering limited mobilities in the inversion layer of a MOSFET is non-trivial. For the scattering limited mobilities in the bulk regions of the device, the scattering rates that were derived in chapter 3 assumed an infinitely long semiconductor with constant impurity and defect concentrations. At the semiconductor/oxide interface, the majority of carriers are located within the first 5-10 nm of the interface with a carrier density that decays exponentially with increasing distance from the surface. As well as this, mobility modelling has shown that the quantisation of carriers within the first 5-10 nm of the semiconductor/oxide interface must be considered in order to model the mobility of carriers effectively [272, 273]. As a result, a universal model for describing the scattering rates of carriers at the semiconductor/oxide interface in MOS devices has yet to be adopted.

Despite this, it has been found that the scattering limited mobilities for the carriers in silicon could be calculated as a function of transverse field as a function of temperature and substrate doping concentration [274, 275]. For Coulombic scattering limited mobility, the carriers follow a similar trend to that of ionised impurity scattering in bulk, but the concentration of ionised impurities becomes a sum of the sheet densities of the oxide trapped charge, interface trap density and ionised impurity density

$$\mu_c \approx \mu_{ii}(N_{tot}) \tag{5.24}$$

where N_{tot} is the total the sum of the interface state density, ionised impurity density and oxide trapped charge which for an n-channel MOSFET is given by

$$N_{tot} = N_A + \frac{N_{it} + N_{ox}}{\langle z \rangle} \tag{5.25}$$
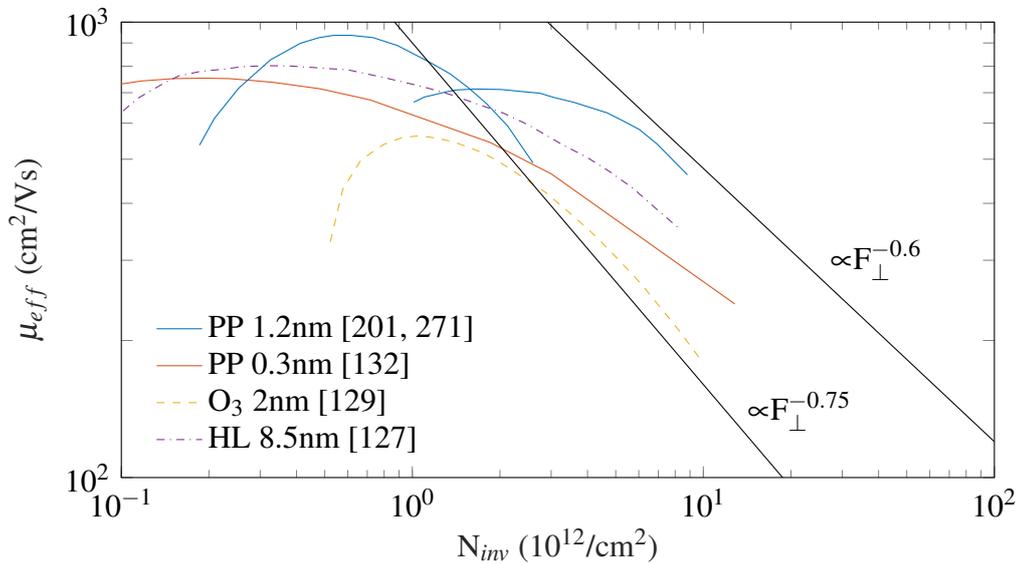
Fig. 5.6 Comparison of the effective carrier mobility within germanium nMOSFETs with a Ge/GeO$_x$ interface. The oxidation method and GeO$_x$ thickness are given in the legend. (PP = post plasma oxidation, O$_3$ = ozone oxidation, HL = high pressure and low-temperature oxidation. $F_\perp^{-0.6}$ and $F_\perp^{-0.75}$ indicate field dependence range for all data within plot at high inversion densities.

where the interface trap concentration is given by

$$N_{it} = \int_{E_V}^{E_C} D_{it} dE \tag{5.26}$$

and $\langle z \rangle$ is the average carrier-interface distance given as [275, 276]

$$\langle z \rangle = \frac{q t_{ox}}{\varepsilon_{ox}(V_G - V_{th})} \int_0^{W_D} z n(z) dz \tag{5.27}$$

The average carrier distance from the interface will reduce slowly with increasing bias leading to a field dependence of the Coulombic scattering mobility. In order to calculate the average carrier distance, the electron concentration as a function of distance from the oxide surface must be calculated. Classically, assuming the carriers can occupy an infinite selection of energy levels, the carrier concentration at the interface will decay monotonically with distance from the surface.

For accurate modelling of the carrier mobility at high fields however, the majority of carriers involved in lateral conduction are within the first few nm's of the surface and so the energy distribution of the carriers must be calculated using quantum mechanics. Using the quantum mechanical approach, the carrier density at the semiconductor/oxide interface becomes equal to zero and peaks within 1-2 nm of the oxide/semiconductor interface [136, 272]. When taking into consideration all carriers from the surface to $z = W_D$, one would assume that this difference would be negligible, but modelling of Coulombic scattering rates within silicon show that the quantum mechanical nature of carriers at the interface must be considered when modelling carrier mobility in MOS inversion layers [273]. As well as this, the screening of carriers from one another must be considered. As the carrier concentration increases, the scattering from impurities within the semiconductor decreases as the high electron concentration results in the screening of impurities from the majority of carriers in the channel [277]. Considering the quantum mechanical nature of the carriers at the interface

is cumbersome requiring significant numerical effort. The influence of Coulombic scattering can be calculated via

$$\frac{1}{\mu_{Coulombic}} = \frac{1}{\mu_{eff}} - \frac{1}{\mu_{rp}} - \frac{1}{\mu_{sr}} \tag{5.28}$$

assuming the contribution of Coulombic scattering is non-negligible.

For the remote phonon scattering and surface roughness scattering, the carrier limited mobilities have been shown to follow [275]

$$\mu_{rp} = C_{rp}T^{-1}F_{eff}^{-1/3} \tag{5.29}$$

and

$$\mu_{sr} = C_{sr}F_{eff}^{-2} \tag{5.30}$$

where C_{rp} and C_{sr} are fitting constants and F_{eff} is the effective field given by

$$F_{eff} = q\frac{N_{dep} + 0.5N_{inv}}{\varepsilon_r\varepsilon_0} \tag{5.31}$$

where N_{dep} and N_{inv} are the depletion and inversion sheet charge densities respectively given by

$$N_{inv} = C_{ox}(V_G - V_{th}) \tag{5.32}$$

and

$$N_{dep} = \sqrt{\frac{4\varepsilon\phi_B N_A}{q}} \tag{5.33}$$

where ϕ_B is the bulk potential given by

$$\phi_B = \frac{k_B T}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{5.34}$$

where it is assumed that the dopant concentration is completely ionised.

In modelling the carrier mobility within germanium, it has recently been shown for holes in pMOSFETs [278] that the additive scattering mechanisms at the interface can be accounted for through the adaptation of the Lombardi model [269]. The Lombardi model takes into consideration the added scattering from surface roughness and remote phonons generated from the oxide through the use of Matthiessen's rule, that is to say, that the effective mobility can be expressed as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{rp}} \tag{5.35}$$

where respectively, μ_b, μ_{sr} and μ_{rp} are the bulk, surface roughness and remote phonon limited mobilities. The model assumes that the field dependence of the Coulomb scattering will automatically be determined through the bulk carrier mobility model at the surface. The surface roughness and remote phonon limited mobilities are then given by

$$\mu_{sr} = \left(\frac{(F_\perp/F_{ref})^A}{\delta} + \frac{F_\perp^3}{\eta} \right)^{-1} \tag{5.36}$$

and

$$\mu_{rp} = \frac{B}{F_\perp} + \frac{C((N_A + N_D + N_2)/N_0)^\lambda}{F_\perp (T/300)^k} \tag{5.37}$$

where the constants A, δ, η, B, C, N_2, N_0, λ and k are all fitting parameters. The model was initially developed to fit the experimental data for silicon and was adapted in order to fit the experimental data in germanium as shown in figure 5.7.

Firstly, the remote phonon scattering was reduced from the silicon default value by modifying the constant C from 580 to 220 $cm^{5/3}/V^{2/3}$s. For the surface roughness scattering, as the reported mobility data was not consistent within literature, the model was adapted for the best case and worst case scenario based on the range of mobility data in the high field range as shown in figure 5.7. For both sets of experimental data, the exponent A was modified from 2 to 1.2 and the constant δ was modified from 5.82×10^{14} to 2.1×10^{10} and 2.1×10^9 cm^2/Vs for the best and worst case scenario respectively. The influence of the bulk

carrier mobility which is dominated through couloumbic scattering was calculated using

$$\frac{1}{\mu_c} = \frac{1}{\mu_{eff}} - \frac{1}{\mu_{sr}} - \frac{1}{\mu_{rp}} \qquad (5.38)$$

from which, the bulk scattering limited mobility was found to be

$$\mu_c = 1.095 \times 10^{-6} F_{\perp}^{-0.75} \qquad (5.39)$$

and was used to calculate the total effective carrier mobility for both sets of experimental data plotted in figure 5.7. Using equations (5.36), (5.37) and (5.39) for with the two values for δ in equation (5.36), it can be seen that the predicted effective mobility closely follows the reported experimental data for that mid to high field range. It can be seen that the scattering limited mobility does not accurately follow the experimental data from [129] at the lowest fields of measurement, but further correction of this model was not considered as the bulk carrier mobility will be device dependent and will rely on the interface state density, impurity concentration and oxide trapped charge density and so this bulk scattering rate is assumed to be suitable for the experimental data considered here but does not ensure it will match all
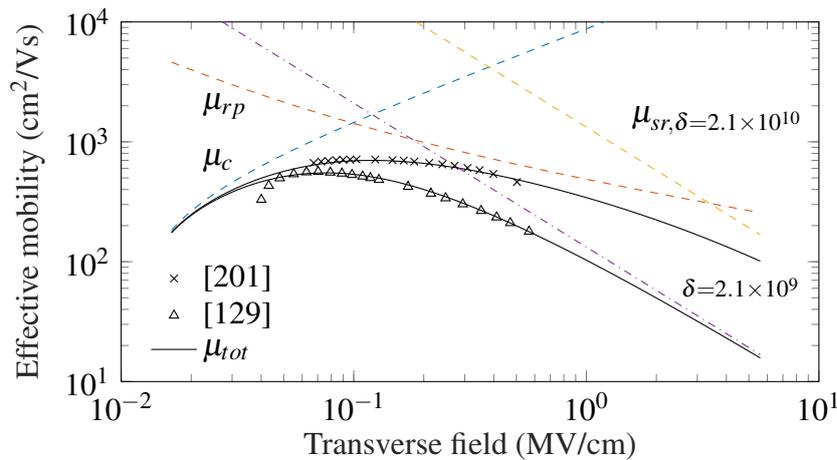
Fig. 5.7 Fitting of experimental electron mobility in germanium MOSFETs [129, 201] as a function of effective field using the adapted Lombardi model [269].

experimental data at low fields. In order for the bulk scattering mobility at low fields to be modelled, the effect of dopant concentration and interface density must be simulated in order to analyse the effect on bulk scattering limited mobility.

5.4   Vertical ZrO_2 nMOSFET simulation

Using the germanium model developed in chapter 3, coupled with the interface density and oxide capacitance extracted from chapter 4, it is possible to simulate the transfer characteristics of a vertical germanium power MOSFET incorporating a ZrO_2 gate dielectric.

Firstly, for comparative purposes, the transfer characteristics of the vertical power MOSFET were simulated with multiple drift region lengths in order to observe the dependence of the on-state resistance on the length of the lightly doped drift region at room temperature and 20 K. The structure of the ZrO_2/GeO_2/germanium power device with a drift region length of 5 μm can be seen in figure 5.8. It can be seen that the source contact of the vertical MOSFET is shorted with the P-region and this is done for all vertical MOSFET devices. This is done in order to eliminate the *body effect* in which the threshold voltage increases if a positive bias is applied to the source with respect to the body region of the device [279]. For lateral devices, the body and source contact are often shorted together but for vertical power devices, manufacturers short these regions together with the source contact in vertical devices.

Similarly to the PiN diode, the vertical MOSFET structure has been meshed in order to solve for the drift-diffusion equations. For the MOSFET simulation, the mesh density has been increased near the oxide/semiconductor interface to within a step size of 0.5 nm that gradually increases with distance from the interface. This must be done in order to compensate for the high carrier concentration and gradient near the interface.

The structure and operation of these devices are determined by both the drain and gate voltage with respect to the source. Following the formation of a channel at the oxide/semiconductor interface, electrons can flow from source contact to the drain. Whereas

in lateral devices the majority of the current flow within the device is in the channel, the electrons in the vertical channel must traverse the lightly doped drift region and through the entire wafer in order to reach the drain.

5.4.1   IdVg characteristic at room and low temperature

In order to observe the influence of the transfer characteristics as a function of drift region length, four devices with drift region length 1, 5, 10 and 100 μm were simulated at room temperature for a drift region doping concentration of 2×10^{14} cm^{-3}. The transfer characteristics can be seen in figure 5.9. It can be seen that a threshold voltage of $\sim$1 V is required for all devices whilst the effect of the added series resistance can be seen between all sets of data. For a drift region length of 1 μm, the series resistance of the drift region does not begin to influence the transconductance of the device up to 10 μA/μm, whilst a drift region of 5 μm reduces the maximum current through the device significantly to less than 6 μA/μm even at a gate drive of 5 V.

Drift region length and doping optimisation

As can be seen from the data in figure 5.9, a large drift region length can have a significant impact on the on-state resistance of the power device. In order to minimise the on-state losses resulting from the drift region, the maximum doping concentration must be found to support the breakdown voltage for a given application, and from this, the length of the drift region can be minimised.

As covered in section 5.2.3, the maximum breakdown voltage of power electronic devices can be expressed through equation (5.21) or be calculated numerically using the ionisation coefficient analysis. By analysing the temperature dependence of the ionisation coefficients, Crowell and Sze showed that the temperature dependence of the maximum breakdown voltage in silicon and germanium could be estimated numerically [280]. Since then, this
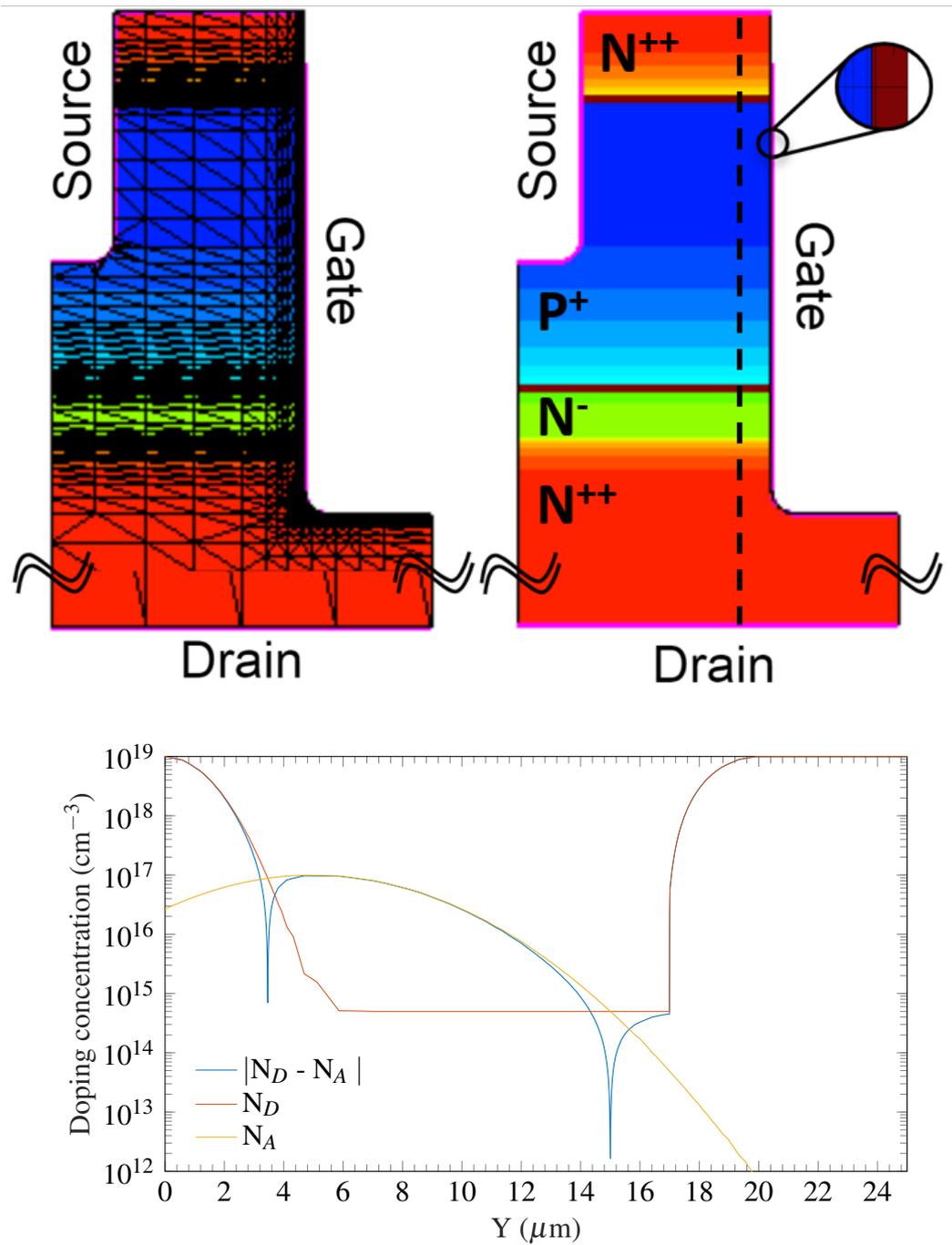
Fig. 5.8 Vertical germanium power nMOSFET with active doping concentration as a function of depth from the source. Regions from top to bottom of structure are source, channel, drift and wafer for the N^{++}, P^+, N^- and N^{++} regions respectively. Dashed line on device gives the doping concentration profile shown in the plot.

expression has been shown to accurately predict the breakdown voltage of silicon power devices at cryogenic temperatures and has even been shown to be consistent with what has been found in 4H-SiC [281–284]. Based on their data for germanium, it was found that the breakdown voltage data could modelled through

$$V_B = \frac{9.6 \times 10^{11}}{N^{0.67}} \exp\left(\frac{0.19T}{N^{0.13}}\right) \tag{5.40}$$

where N is the doping concentration of the lightly doped region of the PN junction. Assigning a breakdown voltage for a device enables the maximum doping concentration for the lightly doped drift region to be solved numerically from equation (5.40). Once the doping concentration is determined, the optimal length of the drift region can be found using

$$L_{d,min} = W_D = \frac{2V_B}{F_M} \tag{5.41}$$

where F_M for lightly doped germanium is 1.1×10^5 V/cm and gradually rises to 2×10^5 V/cm for doping concentrations of 10^{14} to 10^{16} cm^{-3} [104]. A summary of the maximum doping concentration and minimum drift region length can be seen in table 5.1 for devices with
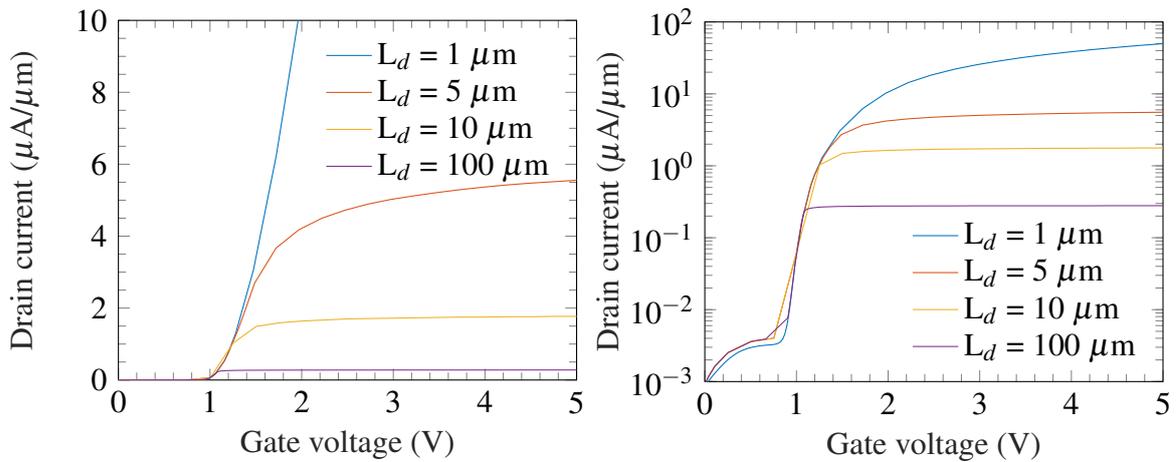
Fig. 5.9 IdVg profile of ZrO$_2$ vertical MOSFET with a varying drift region length with an antimony concentration of 2×10^{14} cm.

V_B	N_{max} (300 K)	N_{max} (20 K)	$L_{d,min}$ (20 K)
270	5×10^{14}	2×10^{14}	45
100	2×10^{15}	8×10^{14}	17
25	1×10^{16}	6×10^{15}	2.5

Table 5.1 Maximum doping concentration and minimum length of light doped drift region in germanium power electronic devices based equations (5.40) and (5.41). Doping concentration is in cm^{-3} and drift region length is in μm

breakdown voltages of 270, 100, and 25 V at a temperature of 20 K. As can be seen from the table, a lower breakdown voltage allows for a device with a lower drift region length and larger doping concentration in comparison to devices with larger breakdown voltages.

5.4.2   IdVg characteristics of optimised structure

The vertical ZrO_2 nMOSFETS were simulated using the optimised parameters from table 5.1 for three devices with breakdown voltages of 270 V, 100 V and 25 V at a temperature of 20 K. Firstly, the IdVg characteristics of the devices for a constant drain to source voltage of 1 V were simulated at room temperature, 77 and 20 K and can be seen in figure 5.10.

It can be seen that at all temperatures, the 270 V device is limited by the series resistance in the drift region resulting in a pseudo saturation effect similar to what is seen at high drain biases in IdVd characteristics. Despite a current density that is between 8 to 9 times higher at all temperatures, the effect of series resistance can also be seen in the 100 V device and is common at high gate biases for high power MOSFETs [285, 286]. For the 25 V device, the drain current can be seen to increase monotonically with gate voltage even up to a bias of 5 V with current densities near two orders of magnitude greater than the 270 V device.

The increase in current density can be attributed to a reduction in series resistance of the lightly doped drift region as well as the channel resistance due to a higher carrier mobility for carriers in both of these regions at lower temperatures [278, 53]. The trend is also consistent with the model predicted in chapter 3 which predicts an increase in carrier mobility at low
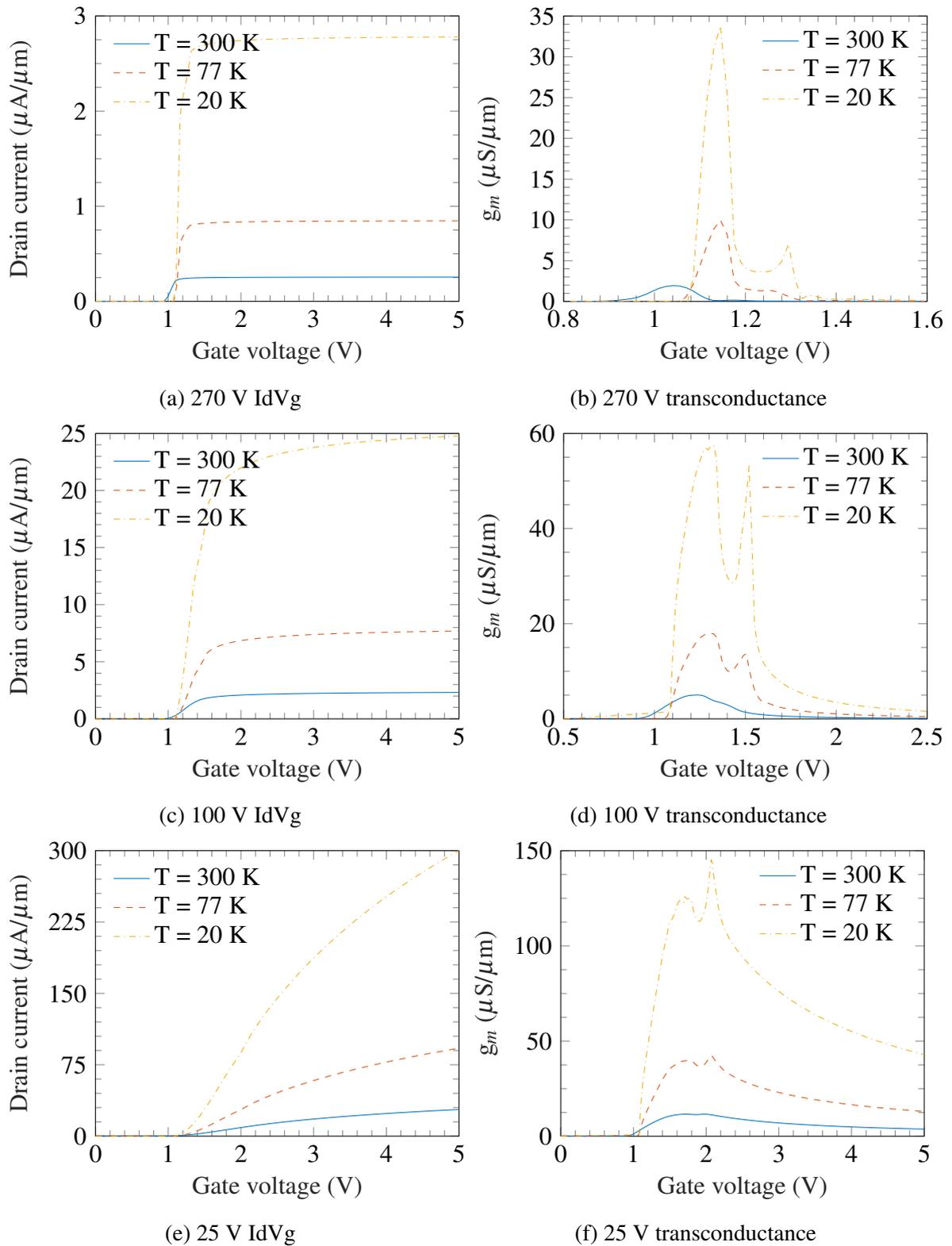
Fig. 5.10 Transfer characteristics and transconductance of vertical ZrO₂ nMOSET with breakdown voltage of 270 (a-b), 100 (c-d) and 25 V (e-f) at room temperature, 77 and 20 K.

temperatures for lightly doped germanium indicating the dominance of the lightly doped drift region on the device resistance.

In order to extract the threshold voltage for IdVd simulations, the maximum conductance method was used. The maximum conductance takes use of the conductance defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \qquad (5.42)$$

and determines the peak value as the turn-on voltage for the device. The partial derivative of drain current with respect to gate voltage for all devices was calculated using the finite difference method and can be seen in figure 5.10. For all devices at temperatures of 77 and 20 K, two distinct peaks can be seen in the transconductance as a function of gate bias. A gradual increase in transconductance, as well as the height of the second peak, can be seen when moving from a device with a higher breakdown voltage to a lower breakdown voltage.

Commonly, the transconductance is related to the field-effect mobility of MOSFETs through

$$u_{FE} = \frac{L g_m}{W C_{ox} V_{ds}} \qquad (5.43)$$

where g_m is calculated through equation (5.42) [287]. As the transconductance spectrum contains two peaks at lower temperatures, the electron mobility within the device appears to peak for two gate voltages. Normally, the carrier mobility which is limited through the harmonic average of the bulk, surface phonon and surface roughness mobilities, reaches a single peak which is determined through knowledge of the transverse field normal to the gate [135].

Use of equation (5.43) however is unsuitable for power MOSFETs as the derivation assumes that the heavily doped N-regions of the device are placed near the edges of the gate oxide. As well as this, the derivation for the drain current from a MOSFET given by equation (5.23) assumes that the electric field distribution in the y-direction (source to drain)

is for a flat geometry, whereas the curved nature of the oxide in the lightly doped drift region leaves the determination of the carrier mobility using equation (5.43) unsuitable.

A plot of the voltage at which the peaks occur as a function of temperature can be seen in figure 5.11. As can be seen from the data, the threshold voltage remains almost unchanged in comparison to the room temperature value which is a requirement for power electronic devices working in extreme environments [288]. For the 270 V device, a greater shift can be seen in both peaks when moving from room temperature down to 20 K whilst the 100 V and 25 V devices have a negligible shift. The cause of this shift for the 270 V device is believed to be due to the greater temperature dependence of the electron mobility within the lightly doped drift region that will ultimately impact the transconductance. As the 100 and 25 V devices have a greater doping concentration in the drift region, the temperature dependence of the electron mobility is reduced and remains within an order of magnitude of the room temperature value, as covered in section 3.3.
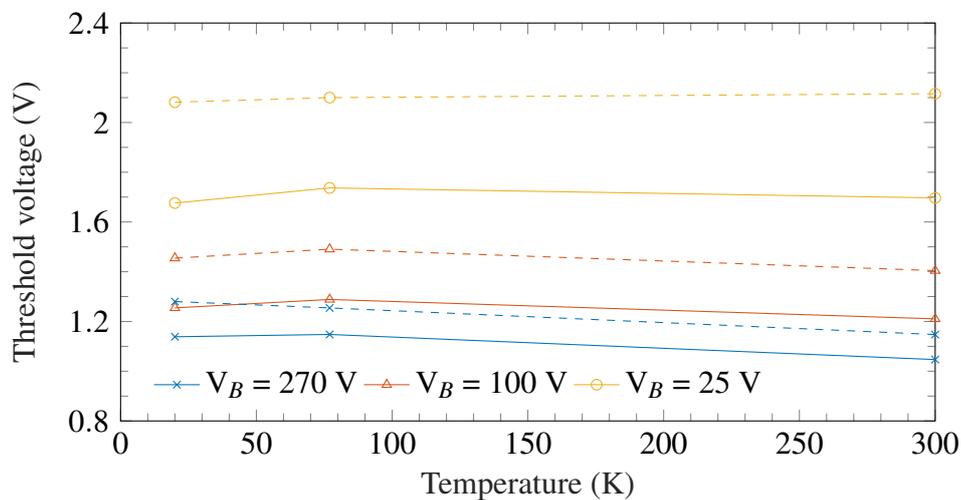
Fig. 5.11 Comparison of threshold voltage for each device using maximum conductance method. Initial peak is given by solid lines (solid) whilst the secondary peaks are given by the dashed lines (dashed).

The influence of the double peak characteristics does not negatively impact the forward characterises of all devices and so this was not considered further. As for the threshold voltage, the voltage of the first peak was taken as the threshold voltage for all devices.

5.4.3   IdVd characteristics of optimised structure

Following the threshold voltage extraction, the devices were simulated at gate overdrive (V$_G$ - V$_T$) voltages of 0, 0.2, 0.4, 0.6, 0.8 and 1 V in order to observe the IdVd characteristics. Following this, in order to make a comparison with devices in literature, the devices were simulated from 0 to 21 V with a gate voltage of 15 V in order to compare the temperature dependence of the on-state resistance.

The IdVd characteristics for the 270 and 100 V devices can be seen in figure 5.12 and the 25 V device can be seen in figure 5.13. For comparative purposes, the drain current density at a voltage of 10 V is also plotted in figure 5.13 for gate overdrive voltages of 0.6 and 1 V.

For the 25 V device, it can be seen that the saturation voltage for all devices remains low; at or below 2 V at all temperatures. The drain current density can be seen to increase by near an order of magnitude from room temperature to 20 K. A similar trend can be observed for all devices. In comparison to the 25 V device however, the 100 V and 270 V devices require much larger drain voltages of near 6 and 20 V respectively in order to achieve saturation.

The increase in saturation voltage for each device is a result of the electric field reduction at the drain end of the gate oxide resulting from the resistive losses from the drift region. By reducing the drift region resistance through a reduced length and/or increased doping, the electric field at the drain end of the oxide will increase and so the voltage at which the channel saturates decreases.

For the 270 and 100 V devices, a gradual increase in the drain current with drain bias can be seen beyond the saturation voltage at room temperature. The cause of this can be attributed to either increased leakage from the reverse biased PN body-diode or can be attributed to

(a) V$_T$ = 0.99 V, T = 300 K

(b) V$_T$ = 1.05 V, T = 300 K

(c) V$_T$ = 1.10 V, T = 77 K

(d) V$_T$ = 1.14 V, T = 77 K

(e) V$_T$ = 1.10 V, T = 20 K

(f) V$_T$ = 1.14 V, T = 20 K
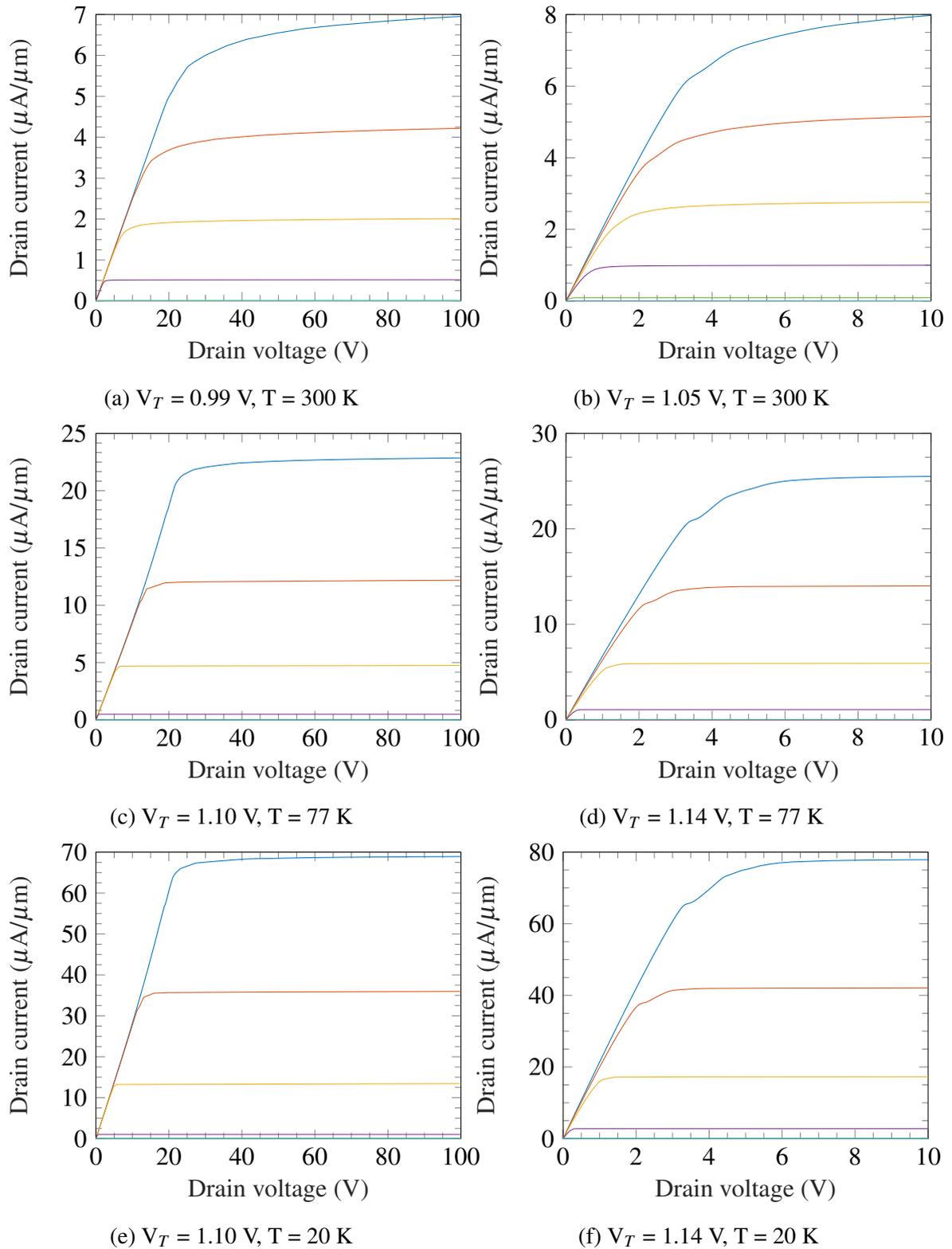
Fig. 5.12 IdVd Characteristics of 270 V (left) and 100 V (right) devices at 300, 77, and 20 K for gate overdrive (V$_G$ - V$_T$) voltages of 0, 0.2, 0.4, 0.6, 0.8 and 1 V.

(a) V$_T$ = 1.22 V, T = 300 K

(b) V$_T$ = 1.34 V, T = 77 K

(c) V$_T$ = 1.32 V, T = 20 K

(d) V$_G$ - V$_T$ = 1 V(solid), V$_G$ - V$_T$ = 0.6 V(dashed)
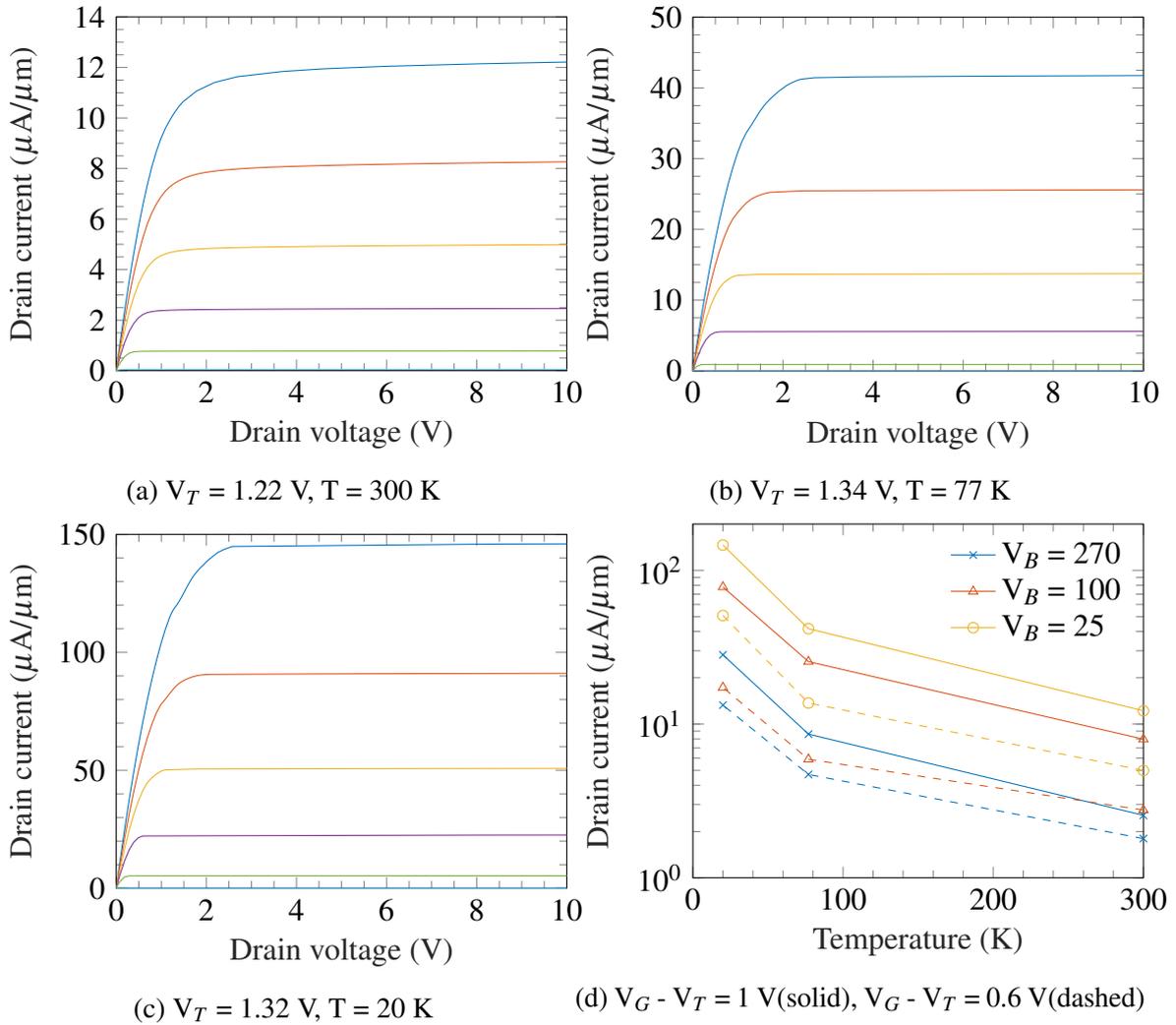
Fig. 5.13 IdVd profile for the 25 V device (a-c) for gate overdrive (V$_G$ - V$_T$) voltages of 0, 0.2, 0.4, 0.6, 0.8 and 1 V and a comparison of the drain current density at a drain voltage of 10 V.

drain induced barrier lowering (DIBL). DIBL is caused by the lowering of the conduction band near the source from the high field resulting from the drain. As DIBL is caused by a high-field effect in sub-micron devices, it can be assumed that this effect is not the source of the increase in drain current beyond saturation. By lowering the temperature, it can be seen that the gradient of the drain current in all devices decreases significantly with no readily noticeable gradient at a temperature of 20 K.
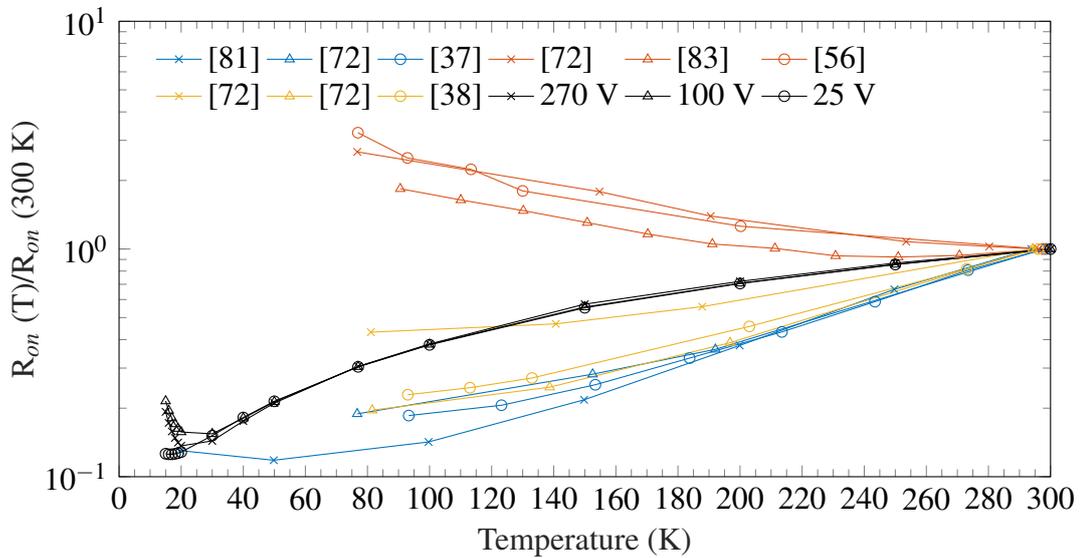
(a) blue = Silicon 500 - 600 V [37, 72, 81], red = 4H-SiC 650 - 1200 V [72, 83, 56], yellow = GaN 200 - 650 V [72, 38], black = Ge, 25 - 250 V (20 K rated V$_B$).
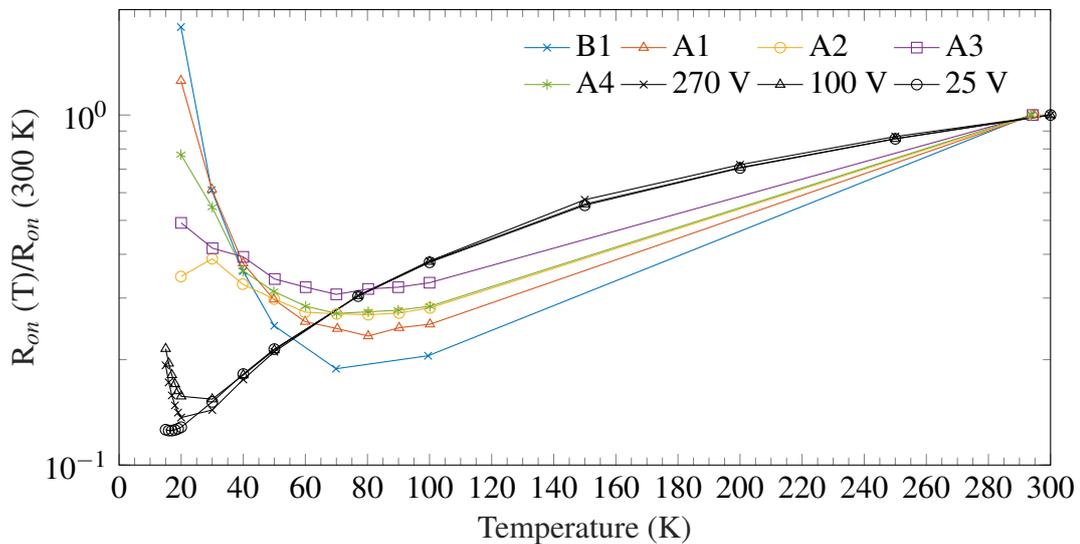
(b) Comparison of 'identical' 200 V silicon (B1 and A1-5 [80]) measured in identical conditions compared to simulation results for vertical ZrO$_2$ germanium nMOSFET.

Fig. 5.14 Temperature dependence of the on-state resistance of the simulated germanium power devices in comparison to experimentally measured data from commercial power devices (a) and 200 V rated silicon HEXFETs (b). All resistances are normalised to the resistance values at or nearest to 300 K.

In order to compare the on-state resistance of the power electronic devices to commercial power devices, the active area of the devices must be known. As well as this, in order for a fair comparison to be made, the on-state resistance should be compared to devices with similar geometries including channel length, trench depth, accumulation length and so on. As this information is not readily available, the temperature dependence of the germanium ZrO_2 nMOSFETS simulated here were compared to the temperature dependence of commercial power devices and can be seen in figure 5.14.

Following normalisation of the reported literature values near room temperature, it can be seen that the germanium power MOSFETs have a positive temperature coefficient similar to silicon and GaN devices whilst all reported 4H-SiC devices show a negative temperature gradient. For SiC and GaN devices, a marginal difference in the temperature dependence of the on-state resistance can be seen when comparing devices with different breakdown voltages, whilst the silicon and germanium devices shown have very similar trends between devices. At liquid nitrogen temperature, it can be seen that the on-state resistance of commercial silicon devices drops to around 10-20% of the room temperature value whilst the germanium devices only drop to 30%. At temperatures below 77 K, reported data for SiC and GaN power MOSFETs is scarce and no fair comparison can be made. For silicon devices, the temperature dependence of a 550 V high power silicon MOSFET down to 20 K showed that the effect of carrier freeze-out did not affect the on-state resistance of the device even at a temperature of 20 K. This result is contradictory to what has been shown experimentally for other silicon devices which experience a dramatic increase in on-state resistance below 50 K through ionised impurity scattering and/or carrier freeze-out [289].

An in depth study on the cryogenic properties of 200 V silicon high power nMOSFETs was performed from 20 K to room temperature by Leong [80] *et. al.* and can be seen in figure 5.14b. From the data, it can be seen that even for 'identical' devices, there is a great variation in resistance below 40 K with 2 devices (B1 and A1) having a greater resistance

at 20 K than at room temperature. The difference in the device resistance could be due to variations in dopant concentrations resulting in different scattering rates from ionised impurities or due to the ionisation of carriers at low temperatures through impact ionisation both of which are dependent on material doping concentration [290–292].

As such, the small variation in doping concentration of the lightly doped drift region of silicon power MOSFETs is believed to be the cause of the large variation in on-state resistance at 20 K. In contrast, it can be seen that the germanium power MOSFETs show similar trends and vary by less than 10% at 20 K in the temperature dependence of their on-state resistance at 20 K.

5.5 Conclusion

The IV characteristics of germanium PiN diodes and vertical ZrO_2 nMOSFETs with varying doping concentrations and drift region lengths have been simulated at room temperature, 77 and 20 K. All germanium PiN diodes showed an increase in turn-on voltage from 0.4 to 0.7 V when simulated from room temperature to 20 K. Diodes with large drift region lengths of 100 and 250 μm exhibited an exponential increase in on-state resistance below 30 K with reducing temperature at higher current densities whilst diodes with short drift region lengths showed a linear relationship with decreasing temperature.

The experimental data for the breakdown voltage within germanium was adapted in order to calculate the optimal length of the lightly doped drift region within power devices in order to achieve breakdown voltages of 270, 100 and 25 V. All vertical ZrO_2 power nMOSFET devices showed an increase in conductivity close to an order of magnitude when operating at 20 K in comparison to room temperature. The germanium PiN diodes and vertical ZrO_2 power nMOSFETs with a breakdown voltage in excess of 270 V experience a similar reduction in the on-state resistance with reducing temperature to the same degree

of commercial silicon and GaN devices with a resistance up to 10 times lower than that of commercial silicon power MOSFETs at a temperature 20 K.

Comparison of the data to commercial silicon power devices with the same breakdown voltage shows that germanium has the potential to have on-state resistance up to an order of magnitude lower at liquid hydrogen temperatures. As a low on-state resistance for control electronics is imperative for emerging cryogenic applications incorporating superconducting networks, this difference cannot be overlooked.

Chapter 6

Conclusions

The semiconducting properties of germanium in the temperature range of 20 to 300 K have been analysed for emerging power electronic applications. Firstly, the electron and hole carrier concentrations and mobilities as a function of temperature and doping concentration were considered. For acceptor or donor concentrations below 10^{17} cm^{-3}, it has been shown that the total carrier concentration within germanium from room temperature down to 10 K can be calculated based on a closed loop model derived using Boltzmann statistics and ionisation energy modelling. If the compensation ratio or the concentration of unintentional impurities such as oxygen is non-negligible, the carrier concentration in the freeze-out regime must be calculated numerically.

In determining the carrier mobility, the suitability of the harmonic average approximation for the electron mobility was explored for the first time at cryogenic temperatures in germanium. Through using this common approximation, it was found that that total carrier mobility is grossly underestimated by over an order of magnitude at a temperature of 20 K for doping concentrations at or greater than 10^{14} cm^{-3} due to an overestimation in ionised impurity scattering. In order for the carrier mobility to be accurately determined, a numerical solution based on the energy dependence of the scattering rates must be employed below

20 K. Using an effective mass of $0.22m_0$, the experimental data and the numerical model agree to within 5% at all temperatures.

In modelling the carrier mobility, it was found that a builtin TCAD model, defined as the Philips Unified mobility model, could be adapted to provide a satisfactory estimation of the temperature dependence of the electron and hole mobility in the temperature range of 20 to 300 K for all doping concentrations to within 5% of the experimental values. The field dependence of the electron and hole mobilities in germanium has also been modelled for simulation purposes for the first time. For temperatures below 130 K, the transferred electron effect must be taken into account in order to predict carrier mobility; although this model requires further development to predict the mobility at intermediate fields at 20 K.

In situ fabrication of ZrO_2 on germanium was developed for the first time. The characteristics were compared to that of Al_2O_3 as a control. The fabricated ZrO_2 MOS capacitors showed a higher interface density in comparison to the Al_2O_3 devices which was found to be a result of sub-oxide formation during the oxidation process. The fabricated ZrO_2/Ge MOS capacitors demonstrated interface densities of near 10^{13} cm^{-2}eV^{-1} which is within 2-3 times of the best recorded data for ZrO_2 on germanium in literature. As well as this, the fabrication method for in-situ fabrication of the GeO_x interlayer during Zr oxidation is the first demonstrated in literature and shows that a much simpler and cheaper method can be used to fabricate ZrO_2 devices on germanium in comparison to other methods that use ALD for the ZrO_2 layer and separate formation of the interlayer. This can also be further improved through fabrication optimisation and post process annealing but this has not been explored here. The leakage characteristics of ZrO_2/Ge MOS capacitor as a function of temperature down to 77 K was measured for the first time. The Fowler-Nordheim tunnelling mechanism was shown to be suitable to accurately predict the field dependence of the leakage current density within the oxide as a function of temperature.

The physical models developed in chapter 3 were combined with the experimental ZrO_2 oxide data in chapter 4 to simulate the on-state resistance of a vertical trench n-type germanium power MOSFET with simulated breakdown voltages of 25, 100 and 270 V as well as a high power vertical PiN diode. The simulated breakdown voltages as a function of drift region doping concentration were found to be in good agreement with experimental data. The on-state resistance of simulated germanium PiN diodes with breakdown voltages in excess of 550 V were found to match the temperature dependence of reported high power germanium PN diodes. The on-state resistance of the zirconium power MOSFETs was found to decrease at a similar rate to that of silicon and GaN power devices but demonstrated that the effect of carrier freeze out does not affect the on-state resistance until below 20 K whilst reported silicon devices below 77 K vary in resistance due to this mechanism.

Through the results here, it has been demonstrated that high power PiN diodes and vertical ZrO_2 MOSFETs fabricated from germanium are predicted to be capable of supporting 270 V applications incorporating liquid hydrogen as a fuel source without the requirement of thermal shielding that current commercial power devices require. As well as this, the models developed within this work allow for manufacturers and researchers to simulate low to high power germanium devices including CMOS applications. As such, the work here provides a crucial step towards the development and implementation of high power germanium electronics for emerging liquid hydrogen applications.

6.1   Future work

Following on from this work, there are a few key areas that require attention in order to achieve the optimal germanium power diode and n-type trench MOSFET. For both the PiN diode and trench power MOSFET, the optimal drift region length and doping concentration are dependant on the operating temperature of the application. As covered in section 5.2.3, due to the reduction in maximum breakdown voltage with decreasing temperature, the

optimal drift region length and doping concentration will be determined by the operating temperature. A summary of the required drift region doping concentration and minimum drift region length for 20 K and room temperature applications are summarised in table 5.1 for 270 V, 100 V and 25 V devices. Before these devices can be realised however, more work must be carried out during fabrication of both the PiN diodes and trench MOSFETs.

Firstly, when fabricating germanium PiN diodes, as covered in the literature review and section 5.2.3, a lot of care must be taken to ensure high breakdown voltages are achieved. During PiN diode fabrication, guard rings must be added to the device to ensure that a premature breakdown does not occur. The number of guard rings required for germanium power diodes, their relative spacing, and doping concentration all need to be determined in order to ensure the breakdown voltage is determined by the drift region concentration.

Secondly, for the n-type ZrO_2 trench MOSFET, work must be conducted in order to maximise the inversion layer carrier mobility at the germanium/GeO_2 interface when using a ZrO_2 dielectric. Here, we achieved a comparable D_{it} to the best reported values in literature but this was for a later structure, no work has been conducted on zirconium side wall oxidation rates. As well as this, the oxidation rate of germanium on the side wall of the etch trench will differ from the surface and so the oxidation recipe must be optimised to achieve a minimal GeO_2 thickness when using high-κ dielectrics.

As well as fabrication, the interface mobility model for the trench MOSFET requires validation through low temperature measurements. The temperature dependence of the bulk and remote phonon scattering mechanisms are based off of a silicon model and there has yet to be any reported data for the temperature dependence of the inversion layer mobility of electrons or holes in germanium MOSFETs down to 20 K. In order to validate or improve the simulations completed here, the inversion layer mobility of ZrO_2 MOS capacitors must be analysed from room temperature down to 20 K.

Although these three areas of work have yet to be fully addressed, it has been shown here that it is possible to fabricate germanium PiN diode and power MOSFETs that are capable of operating at 20 K with room temperature like conductivity and breakdown voltage in excess of 270 V.

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