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OPTIMAL CHANNEL DIMENSIONS AND TEMPERATURE CHARACTERISTICS OF SI-FINFET TRANSISTOR

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ABSTRAK

Pelbagai jenis struktur baru Transistor Kesan Medan (FET) sedang giat dikaji disebabkan oleh teknologi Transistor Kesan Medan Semikonduktor Logam-Oksida (MOSFET) yang semakin mencapai tahap terhad. Salah satu daripada alternatif baru FETs ialah FinFET. Keupayaan model baru ini mampu menjadi sumber perkembangan kepada pelbagai lagi aplikasi yang lain, di mana ianya bergantung kepada sifat nano dimensi yang dimiliki. Perkembangan generasi chip melalui kelengkapan elektronik yang baharu serta berkuasa tinggi mampu dicapai sekiranya penemuan dalam kajian ini digunapakai. Namun, rekacipta dan struktur nano-dimensi FET yang baharu masih dikelaskan sebagai kajian yang tulen serta memerlukan kajian dan pembangunan yang lebih mendalam serta pelbagai usaha inovasi, berpunca daripada beberapa halangan dalam bidang kajian sains MOSFET. Pengesan suhu berdasarkan transistor direka berdasakan sifat perubahan suhu oleh hubungan arus dan voltan dalam transistor FinFET. Kajian ini akan memfokuskan kepada menstrukturkan dimensi saluran untuk Si-FinFet bagi menghasilkan keputusan yang terbaik berdasarkan kepada sifat elektrik dan suhu. Ini akan melibatkan kajian terhadap sifat suhu (kepekaan dan kestabilan) Si-FinFet berdasarkan kepada dimensi saluran (panjang (L), lebar (W)), ketebalan oksida (T_{OX}) dan voltan operasi (V_{DD}). Kajian ini akan memfokuskan kepada simulasi dan analisis kesan voltan operasi Si-FinFET terhadap sifat elektrik sebagai faktor pengehad, iaitu voltan ambang (V_T), penukaran sub minimum (SS), dan Terowong Aruhan Penurunan Halangan (DIBL). Simulasi transistor jenis kesan medan multi-gate (MUGFET) digunakan untuk menyiasat sifat suhu dan elektrik FinFET. Hubungan antara arus-voltan dengan kepelbagaian suhu (T=250, 275, 300, 325, 350, 375 and 400 K) and panjang pintu (Lg=25, 45, 65, 85 and 105nm), lebar pintu (Wg = 5, 10, 20, 40 and 80 nm) dan penebalan oksida (T_{ox} 1, 2, 3, 4 and 5 nm) disimulasikan. Sambungan Semikonduktor Logam-Oksida untuk mengukur sensitiviti suhu FinFET juga diambilkira. Berdasarkan kajian, panjang saluran terbaik FinFET ialah 65 nm, dalam operasi voltan V_{DD} antara of 0–5 V. Selain itu, sensitiviti suhu FinFET meningkat secara lansung dengan peningkatan lebar saluran antara 5–80 nm dan peningkatan arus (ΔI) terbaik mengikut suhu boleh dicapai dengan meningkatkan ketebalan oksida kepada 5 nm dan ianya kekal stabil selepas itu walaupun ketebalan oksida terus meningkat. Kesimpulannya, nilai terbaik untuk Wg ialah 5, 10, 20 nm dan ianya konsisten serta boleh di anggap sebagai nilai optimum dan nilai terbaik untuk T_{OX} ialah 1 nm.

ABSTRACT

As metal oxide semiconductor field effect transistor (MOSFET) technology approaches its downscaling limits, many novel structures of FET have been explored extensively. One of the relatively new types of FET is FinFET. The performance of electronic devices, which may correspond to a wide array of recent applications, likely depend on the nano-dimensional characteristics of such devices. The chip generation of these powerful electronic devices with ultra-small transistors may increase in reliability when new findings from future research are consolidated. However, nano-dimensional FET designs and structures are still considered as novel technologies, thereby necessitating further study and improvement. Further innovations are needed despite the limitations in MOSFET science. Transistor-based temperature sensors are designed based on the temperature characteristics of current-voltage curves of FinFET transistors. This study aims to design channel dimensions of Si-FinFET for best performance based on electrical and temperature characteristics. The study investigates the temperature characteristics (sensitivity and stability) of Si-FinFET based on optimal channel dimensions, such as length (L), width (W)), oxide thickness (T_{OX}) and operating voltage (V_{DD}). This study focuses on simulating and analysing the effects of the operating temperature of Si-FinFET on its electrical characteristics as limitation factors, namely, threshold voltage (V_T), subthreshold swing (SS), and drain-induced barrier lowering (DIBL). A multi-gate field effect transistor (MuGFET) simulation tool is used to investigate the temperature and electrical characteristics of FinFET. Current-voltage characteristics with different temperatures (T = 250, 275, 300, 325, 350, 375 and 400 K) and gate length (Lg = 25, 45, 65, 85 and 105 nm), gate width (Wg = 5, 10, 20, 40 and 80 nm) and oxide thickness (T_{OX} = 1, 2, 3, 4 and 5 nm) are initially simulated. Then, the metal oxide semiconductor diode mode connection to measure FinFET temperature sensitivity is considered. Thus, the perfect channel length for the FinFET under the conditions considered in this thesis is 65 nm to obtain acceptable temperature sensitivity at the operating voltage range of 0–5 V. Furthermore, temperature sensitivity of the FinFET increased with channel width at the range of 5–80 nm. The best increments for the current (ΔI) in relation to temperature can be achieved by increasing T_{OX} to 5 nm, beyond which the values become stable regardless of the thickness. We can infer that the optimal Wg values are 5, 10 and 20 nm, which are consistent and may be considered as perfect values. The best T_{OX} in this study is 1 nm.

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LIST OF SYMBOLS

I	Current
I_{ds}	Drain to source current
Lg	Length of channel
Wg	Width of channel
T_{ox}	Oxide thickness
V	Voltage
V_{DD}	Drain DC voltage source
Vgs	Gate-to-source voltage
T	Temperature
Id	Drain current
Vg	Gate voltage
V_D	Drain voltage
IG	Independent gate

LIST OF ABBREVIATIONS

ΔL	Channel is effectively reduced in length
ΔI	Change of current
3D	Three dimensional
CMOS	Complementary metal-oxide semiconductor
CNT	Carbon nanotube transistor
DG-CMOS	Double-gate complementary metal-oxide semiconductor
DG-FET	Double-gate field-effect transistor
DIBL	Drain-induced barrier lowering
FinFET	Fin-shaped field-effect transistor
ITRS	International technology roadmap for semiconductors
MOSFET	Metal-oxide-field-effect transistor
SBPWM	Simple boost pulse width modulation
SCEs	Short-channel effects
SiNWT	Silicon nanowire field-effect transistor
SOI	Silicon on insulator
SS	Subthreshold swing
SWCNTs	Single-walled semiconducting carbon nanotubes
V_T	Threshold voltage

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