Practical Works on Nanotechnology

SINCE ITS EMERGENCE A FEW decades ago, nanotechnology has been shown to be a perfect example of a crossroad between different fundamentals sciences. In the last 10 years, the continuous progress of classical top-down lithography and the use of alternative bottom-up elaboration methods has allowed new and smaller components to be created. Their combination has led to very complex and innovative architectures. At the same time, flexible, low-cost, and low-ecological-footprint devices have emerged. Thus, the diversity and multidisciplinary features present challenges in addressing these issues in educational programs.

Practical works are essential for students, to assimilate the complex theoretical concepts and acquire associated skills. Here, we share our experience of introducing nanotechnologies to university students through practical work. For more than 38 years, we have proposed microelectronic-based device-fabrication training that seeks to realize devices in a clean room that is mainly dedicated to educational purposes. Hereafter, we will describe some brief (two–five days) and practical training in the field of CMOS technology, sensor (gas, strain, and

Middle school to undergraduate students.

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so on) technologies, or integrated on-chip energy storage. We will focus on the peculiar interest of each practical work, the issues tackled, and organization of the trainings. Finally, we will share our experience in addressing young middle school students.

BACKGROUND

Nanotechnology applications are increasingly present in everyday life. If the tremendous growth of research topics and the number of publications illustrate an interest in academic research, the routine applications become more present and concern many applications, such as medicine, mechanics, biology, communication, energy, and so on. Electronics are used in all human activities. Downsizing each active element in the integrated circuits has become a key parameter for increasing performances. Thus, due to the necessity of nanotechnology in our life, teaching and training the fundamental concepts used in these applications become mandatory. Therefore, introducing nanotechnology in the pedagogical content becomes more and more challenging. The difficulty arises from the complexity and number of concepts that interact in nanotechnology.

The process requires multidisciplinary knowledge where several fundamental sciences intersect, which can be addressed separately in lectures as a first step. Merging all of these concepts from different disciplines is a challenging task, especially for young, inexperienced students. Therefore, practical works in which each student can elaborate and test his or her own nanodevice are necessary. However, producing nanosized devices or materials often requires dedicated setup and adapted characterization tools, which usually are expensive. Above all, safe laboratory benches and specific infrastructures to safely manipulate hazardous chemicals and nano-objects are needed.

Our institute, Atelier Interuniversitaire de Micro et nano Electronique (AIME), is a French facility connected to the Centre national de la recherche scientifique, two engineering schools and one University Paul Sabatier in Toulouse, France. We are also partnered with the French network dedicated to education in microelectronic and nanotechnology that is coordinated by the Comité National de Formation en Microélectronique (CNFM) (http://www.cnfm.fr). The CNFM brings together 12 platforms spread over the country. These platforms are common facilities open to the French educational community as well as foreign universities.

AIME is dedicated to educating and training undergraduate and graduate students in the fields of microelectronic and nanotechnology. The trainings originally centered on manufacturing and testing silicon (Si)-based semiconductors and microelectronics devices. In the last 20 years, growing interest in nanotechnology has led us to introduce it into our activities. As such, the trainees fabricate their own devices, starting with a virgin Si wafer that will be processed on their own, for all steps of the fabrication process. The contents of these practical works have been defined in close cooperation with professors and researchers from various universities and engineering schools. These trainings provide an experimental view of the fundamental aspects introduced in lectures. Students are introduced to the practical manufacturing of real nanodevices by following the successive fabrication steps, with the appropriate validation protocols. Although the experiments typically performed by the students are from a technology transfer from factories and research laboratories, some are from works published in the literature.

In this article, we report our experience in providing these practical works, especially those focused on nanotechnology. These training are intimately connected to the field of electronics and therefore are based on standard microelectronic manufacturing procedures that require dedicated facilities (clean rooms) and associated equipment. We will first review how the training is generally conducted in a typical work. We then provide some examples of the introduction and manipulation of nanometer-sized active materials in nanodevices, in a broad range of applications. To conclude, we present our approach to introducing nanotechnologies to middle school students.

GENERAL WORKFLOWS

A typical training is provided to a group of up to 18 students for two–five days. The number of manufacturing stages with masking and photolithography (PL) steps, as well as the final electrical tests, define the duration. Therefore, short trainings (two days) involve fabricating devices that use less than two masks of PL, which is the case of Si diodes or solar cells, for instance. For longer training (five days), three to five consecutive PLs can be done in processes such as fabricating microelectromechanical systems or MOS transistors. Whatever the duration of the training, our facilities allow students to process a bare Si wafer until the final device, completing all fabrication steps to the final characterization. For this purpose, a 400-m^2 clean room is available and equipped for all of the wafer-processing, probe-testing, dicing, and die-packaging steps, as well as for the final test of the device (Figure 1).

For simplicity, let us divide the clean room into three main areas: workstations 1, 2, and 3. A typical schedule depends on the number of students and the length of the training. Typically, the students are split into pairs. For a class of 18 students, this gives us three groups of three pairs (labeled G1, G2, and G3). Each pair of students receives a bare Si wafer to process and one or

several Si wafers dedicated to the parallel characterization (test wafer). The general workflow is depicted in Figure 1(b). The idea is to delay the entrance of G2 and then G3, and to perform a rotation or permutation between all workstations. Workstations 1 and 2 are dedicated to processing the Si wafer, which will give the final device.

For workstation 1, all group manufacturing processes can be done simultaneously in parallel by three pairs of students that belong to the same group. In other words, each pair of students uses their own laboratory bench or machine. Each piece of equipment has been tripled: laboratory benches for chemistry operations (wafer cleaning, etching, and so on) or for patterning operations (three masks aligners, three spin coaters, etc.) as depicted in Figure 1(a).

Workstation 2 includes all fabrication steps in which the Si wafers from one group of students are processed simultaneously. The thermal treatment (such as diffusion, annealing, and oxidation), layers deposition [including metal, oxide, and so on using physical vapor deposition (PVD) or chemical vapor deposited], or equipment that has to be operated by our staff (reactive ion etching, ion-implantation system, semiautomatic wafer prober, dicing, saw, chip bonding, etc.).

Workstation 3 refers to all the characterization steps performed on the test wafer. This process allows students to measure the thickness of the layers to estimate the wet etching time, for instance, with different methods (profilometry or ellipsometry) or to determine the resistivity of each active layer (before and after doping, metal, and so on) using four-point probe stations. The delay between the groups is voluntarily introduced on day one and is maintained until the last day, when the students performed the final test of a single-mounted chip after testing their wafers. This step is primordial, since it allows the trainees to evaluate what they have fabricated on their own with what they have studied in the classroom, particularly through fine characterization of their devices and quantitative analysis.

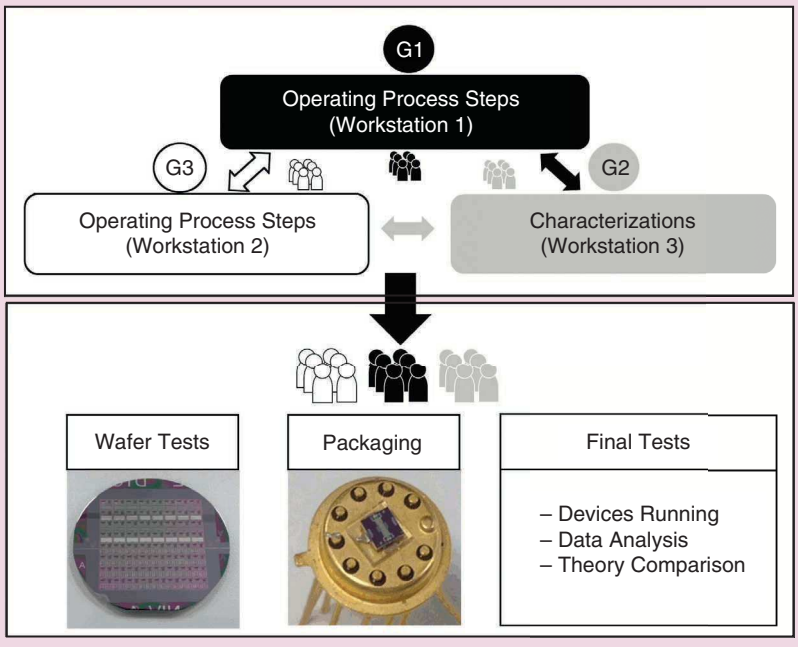
Although most of the training steps are standardized for microelectronic device fabrication, they still allow the students to work with nanometer-sized materials through the characterization of the active layers (doped Si/poly Si or metal, for instance), and by using research laboratory equipment dedicated to the submicronic scale [profilometer/atomic force microscopy, ellipsometer for thickness, and scanning electron microscope (SEM) microscopy for observation]. The same workflow can be used to integrate nano-objects as the main active building block of the devices, as will be shown in the next section.

NANO-INSIDE: SI NANOCRYSTAL INSERTED IN CMOS TECHNOLOGY

The nanocrystal inside training was derived from Grisolia et al. [1] and adapted to our NMOS process. The training consists of fabricating a conventional n-MOSFET with a monolayer of Si nanocrystals (NCs) (~3 nm) inserted inside the gate oxide.

This work allows the students to fabricate nanodevices that are compatible with CMOS technology, with potential applications such as flash memories. In addition to the standard processes of microelectronic fabrication required for the entire device (four masks and four PLs), the students have the opportunity to see how to create and incorporate nanostructures using equipment typical of semiconductor processes. Indeed, the embedded Si nanocrystals are elaborated via low-energy ion implantation (~1 keV) at the Centre d'Elaboration des Matériaux et d'Etudes Structurales. By the

(a)



(b)

FIGURE 1 (a) The PL area displaying three mask aligners and three laboratory benches. (b) The scheme of our turnover system for an 18-student typical process, from the fabrication processing to the final test of packaged devices.

The students perform the electrical characterization of their devices and demonstrate how electrical charges can be stored.

end of the training, the students perform the electrical characterization of their devices and demonstrate how electrical charges can be stored (or released) within the Si NCs [Figure 2(c)]. Fundamental physics concepts can be tackled with the students, such as a Coulomb blockade or quantum mechanics.

GAS SENSORS: INTEGRATING CHEMICALLY SYNTHESIZED NANO-OBJECTS ON CHIPS

We now present training in which the students produce gas sensor devices by means of standard semiconductor processes and nanoparticles (NPs) synthesized using chemical methods are the active material of the sensor.

NPs can be obtained and integrated into devices by different methods, one of which is the direct growth of the NPs in a localized area, such as with PVD. An alternative is to use the chemical synthesis, which is a facile and cheap route to produce NPs. Then a layer of NPs is deposited on interdigitated combs. Chemical routes allow adaptation of the composition, size, and shape of the NPs, to obtain an optimized surface-to-volume ratio to enhance the sensitivity. If the NP synthesis is straightforward (ease of implementation), especially with our clean room facilities, including NPs in the trainings programs raise several questions, particularly about cross-contamination with other processes, especially with Si-based technology. The second issue concerns the toxicity and safety of the trainees. Besides, localizing the deposit of NPs is still challenging, especially to control the electrical response of the NPs, i.e., to obtain enough percolation paths to ensure a current flowing through the entire assembly of NPs [2].

To overcome these issues, the NP synthesis takes place in a confined room dedicated to nanomaterial handling that is inside the clean room. WO_3 was chosen as the active material since it provides a good sensitivity to gas. It has a low toxicity, and NPs can be easily elaborated following simple experimental procedures that are suitable for a training.

Following the general workflow described in the "Background" section, the students rotate between all workstations, in this case mainly between the chip fabrication and the chemical synthesis. A typical sequence is to first fabricate the electrodes that will collect the NPs. Two hundred fifty-six chips are created on a 2-in Si wafer. The chips are composed of three types of components: 1) two pairs of interdigitated electrodes (Al); 2) a local heater (doped poly-Si), isolated and buried under an SiO_2 layer; and 3) a thermistor (Al) to measure the local temperature. Additional details of the process can be found in [3].

The geometry of the electrodes has a double function. First, increasing the number of fingers enhances the number of conduction paths. Second, the electrical resistance in NP assemblies are generally high. Thus, increasing the number of channels in parallel lowers the whole resistance of the array. After fabricating the chips, the students elaborate their own WO_3 NPs, with the hydrothermal decomposition of tungsten oxide precursors [4], under mild conditions. After 4 h of growth at 180 °C, they obtain needle-shape NPs, namely nanowires (NWs), with a length of 1–2 μm and a diameter of ~100 nm. These NWs are then deposited on a chip, for which the chip is mounted on a TO5 socket to facilitate handling and electrical addressing.

Dielectrophoresis [5] is used to drive the NWs between the interdigitated combs. To do so, an ac voltage with a peak-to-peak amplitude of V_{PP} = 20 V and a frequency of 100 kHz is applied. Under these conditions, the NWs are

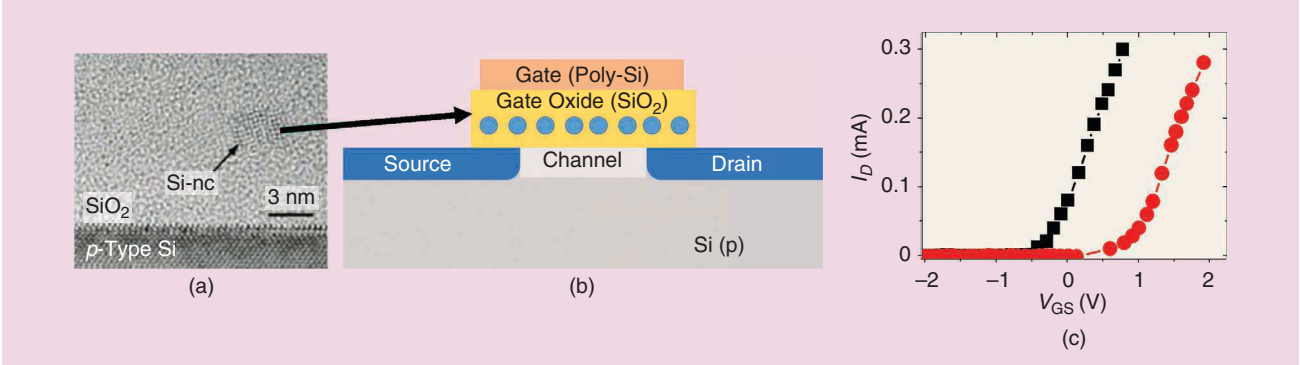


FIGURE 2 (a) A cross-section SEM micrograph of the gate oxide showing Si nanocrystals, (b) a scheme of the NMOS fabricated with embedded Si nanocrystals, and (c) the drain current for an oscillating gate voltage (9 V at 100 Hz).

trapped and cover the area between the electrodes [Figure 3(a) and (c)]. The dielectrophoresis optimizes the number of percolation paths between the terminals of the sensors. Finally, during the last days, the students test their devices in a dedicated homemade setup composed of a sealed chamber. The electrical resistance is measured under subsequent cycles of dried air (N_2 and O_2) and other selected gas [NH_3 diluted in N_2; for instance, see Figure 3(d)]. The sensitivity is measured at different local temperatures, thanks to the poly-Si heater while the temperature is controlled with the Al thermistor. WO_3 shows an efficient response to diluted NH_3 at 250 °C.

This training is very rich in terms of educational contents. It provides examples of the cooperative contributions of different fields of science to nanotechnology, including the chemical synthesis of NPs, the operating principle of sensors, and the use of electric information. The students also learn to characterize nanostructures with specific and adapted tools such as scanning electronic microscopy. Additional fundamental points can also be taught with their final electrical characterizations, including how charge transport is driven in the arrays of nanostructures or how the surface effects become crucial at the nanoscale, particularly how any impurities, voluntarily injected (NH_3) or not (surface quality of the surface of NPs) can modify the conduction properties in NP assemblies.

MICRO-SUPERCAPACITORS: CARBON-BASED DEVICES FOR ENERGY STORAGE

This training addresses the emergent field of energy storage in integrated Si devices, particularly the growing demand for mobile applications. A solution is micro-supercapacitors (micro-SCs) directly integrated onto Si chips. Despite the micrometer size of the structure (Figure 4), the nanoscale technology lies in the working principle of the micro-SC itself and the choice of the active material [Figure 4(b)]. Actually, an SC is based on the charge accumulations of ions provided by an electrolyte between two active electrodes. The capacity density is huge since it relies on subnanometer spacing. In addition, we have chosen activated carbon (commercial YP-50F, Kuraray) as active electrodes that present a high density of nanopores (< 2 nm). This high surface specific area material also provides many advantages since it yields high power density (> 10 $kW.kg^{-1}$), with an almost unlimited life span due to the absence of chemical modifications under charge/discharge cycling. This work has been realized in close collaboration with research groups from

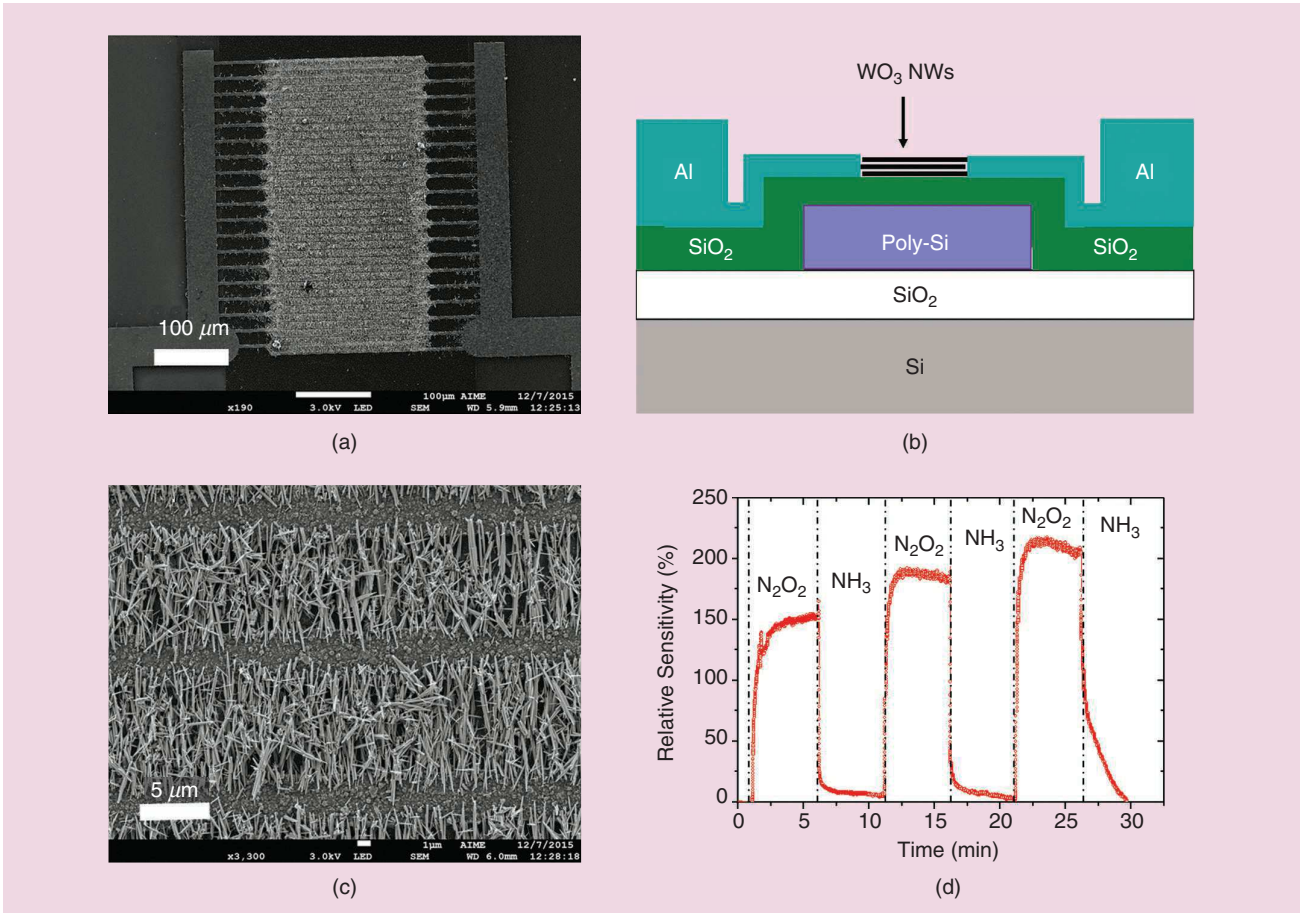


FIGURE 3 The SEM micrographs of the WO_3 nanowires trapped between electrodes: (a) large view, (b) a scheme of the device with an integrated isolated polysilicon heater, (c) magnification, and (d) the relative electrical response of the sensor under several N_2O_2/NH_3 cycles.

the Centre Interuniversitaire de Recherche et d'Ingénierie des Matériaux and represents a technology transfer of their experiments [6].

The first step of the process is dedicated to the fabrication of gold (Au) current collectors, which consist of interdigitated electrodes separated by 160 or 220 μm. The patterning of the Au layer requires a single mask. The activated carbon is then deposited by electrophoresis on the Au fingers. For that, the chip is first mounted on a TO8 socket and bonded. The mounted chip is then dipped in a solution of YP-50F while applying a dc voltage of amplitude V_{dc} = 50 V. The chip is then rinsed in acetone (still under V_{dc}) to clean up the device. As can be seen in Figure 4(c), the carbon NPs are only localized on top of the collectors and not between them, preventing any short circuits. Finally, the students characterize their micro-SCs using a VSP300 (Bio-Logic Instruments) by performing repeated cycles of current measurements with NEt_4BF_4 as an electrolyte. The micro-SCs give typically 1.2 mF (~5 mF/cm^2) depending on the amount of carbon deposited.

This training is less demanding than others that concern the fabrication processes, but it still offers an overview of a PL/etching process. Its main interest lays in the fabrication of a device for mobile and embedded electronic, which is a popular current topic.

NANO AT SCHOOL

This section is dedicated to the training session provided to middle school students. Allowing young people to have a first concrete experience of nanotechnology is a major issue considering our technological world and the critical ethical questions that are associated. Motivating young people to pursue scientific careers is another important issue. How do we address this topic? We propose a yearlong program in their class and a day with practical works in the clean room at AIME. It generally starts with a conference and an introductory discussion on the story of micronanotechnology in which the main steps in fundamental science and Si integrated technologies are presented. Their applications for and influence on everyday life are discussed. This work continues all year by introducing some basic concepts in mathematics and physics, but also in history (i.e., the impact of innovation) or literature. For instance, what were their lives anticipated to be like in comparison to ours? Later, a full day is dedicated to visiting AIME and performing practical experiments in the clean room.

The visit is depicted in Figure 5(a). The classroom is divided in two groups with two activities completed in parallel. The first is a visit to our clean room and facilities. The standard processes are

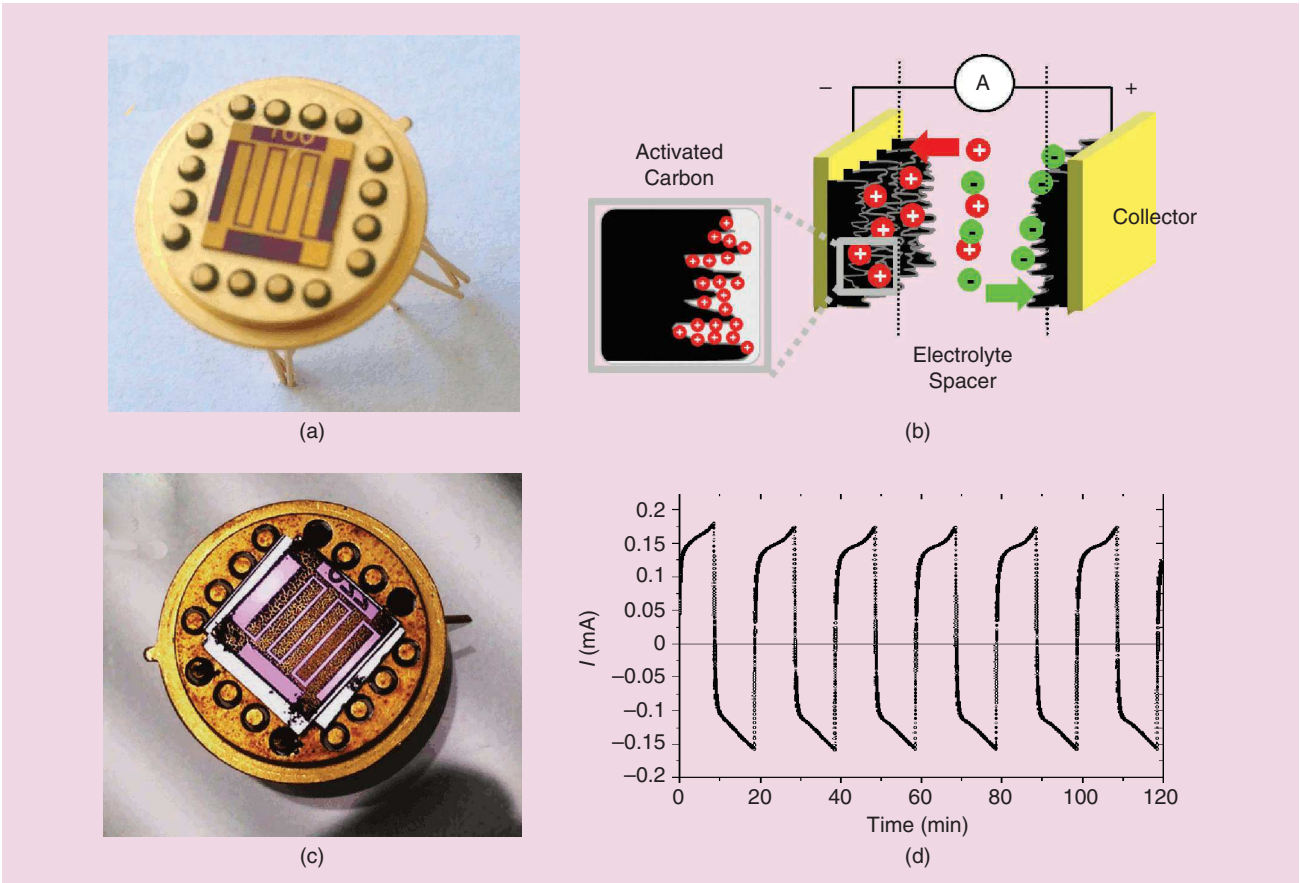


FIGURE 4 A die mounted on a TO8 (a) before and (c) after carbon deposit via electrophoresis [7], (b) a scheme of the operating device [7], and (d) the current measurement as a function of time performed with NEt_4BF_4 electrolytes.

explained, and some equipment demonstrations are performed. To illustrate the use and to show how a nanostructure can be designed on Si, the students perform a PL process on an Si-oxidized wafer capped with an Al layer. For this, they prepare a design, for instance a logo [Figure 5(b)]. Then, AIME's staff proceeds to the PL step and the final etching of Al [Figure 5(c)] with them. In parallel, the other group attends a practical work focused on nanocarbon. Students make pencil-based strain gauges on paper [Figure 5(d)], following the protocol described in [8]. First, the students color a predefined area with different types of pencils (HB and 3B for instance, with different carbon contains), and then measure the resistance of their gauges with a multimeter [Figure 5(e)]. By bending them upward or downward, they observe a change in resistivity, a decrease and an increase, respectively. A general discussion is then initiated to interpret these experimental results. What do they measure? What is the principle of a resistivity measurement? What has been deposited? What are the different types of carbon structures (diamond, graphite, graphene, nanotube, and fullerene) and their respective properties? Why does the resistance change? What kind of application can be done? What are the advantages and drawbacks of such a technology?

This simple set of experiments is of great interest for many reasons. From a theoretical point of view, we can discuss the resistance measurement based on Ohm's law, a direct application of their courses. These strain gauges are easily and quickly realized, so the experiments can be performed with minimal school furniture although a multimeter is required. Fundamental questions concerning the innovation, cost reduction, and renewability associated with technologies can therefore be tackled with the middle school students. Second, by reading the publication, they can have a first view of a typical scientific approach (structural properties, microscopy characterization, electrical

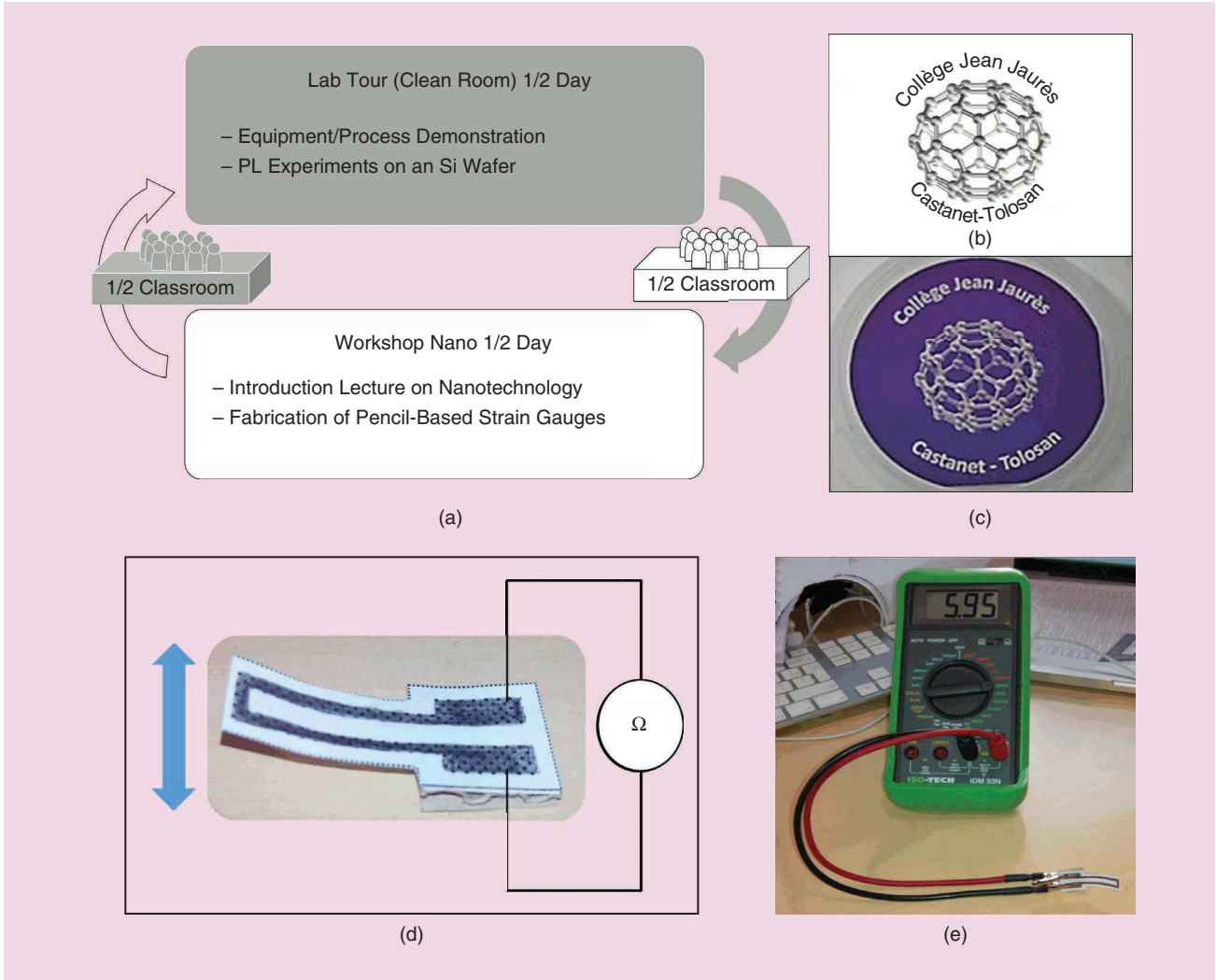


FIGURE 5 (a) A general workflow of a practical work (one day) with middle school students. (b) A design proposed by a classroom and (c) its transfer onto an Si wafer. (d) The setup of electrical measurements fabricated and characterized by the students and the (e) graphite-based strain gauges.

properties, discussion, and so on). Last but not least, this easy experiment can serve as a base to address many prospective and emerging fields related to nanotechnologies, such as the use of a flexible substrate or the introduction of devices based on organic or carbon-derived material.

CONCLUSION

In summary, we have reported some examples of our approach for teaching nanotechnology to students at different levels ranging from middle school to undergraduate, using experimental works. The aim is to provide insights about nanotechnology, and to develop skills concerning the use of the cleanroom facility, micro- and nanofabrication tools, and design of components. The important point is to confront the students with the "real" world, the use of different machines, and the strict application of safety rules, particularly regarding the use of dangerous chemicals. These long practical works take up to five days, include numerous fabrication steps, and require concentration and attention. At the end, a critical analysis of the final properties is done in light of the theoretical models, to assess the successes and difficulties, as well as to provide clues for further improvement.

The main criterion to define our practical works always is the safety of the trainees. However, from a practical point of view, the ease of implementation and the reproducibility of the experiments are necessary to reduce the inherent difficulties in experimental works. Our training sessions take place in a clean room with laboratory research facilities. Note that, as shown in the "Nano at School" section, we demonstrate that nanotechnology can also be introduced in trainings with a minimum amount of materials.

Each year, about 600–700 undergraduate and 300–400 middle school students complete one training. New programs are being prepared for a summer school format in which our trainings will be associated with high-level courses, in the framework of the NanoX graduate school. For perspective, new topics in the fields of microfluidics and 2D semiconducting systems (graphene, MoS_2, and so on) are being investigated.

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