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Power Hardware-in-the-Loop: Response of Power Components in Real-Time Grid Simulation Environment

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Abstract: With increasing changes in the contemporary energy system, it becomes essential to test the autonomous control strategies for distributed energy resources in a controlled environment to investigate power grid stability. Power hardware-in-the-loop (PHIL) concept is an efficient approach for such evaluations in which a virtually simulated power grid is interfaced to a real hardware device. This strongly coupled software-hardware system introduces obstacles that need attention for smooth operation of the laboratory setup to validate robust control algorithms for decentralized grids. This paper presents a novel methodology and its implementation to develop a test-bench for a real-time PHIL simulation of a typical power distribution grid to study the dynamic behavior of the real power components in connection with the simulated grid. The application of hybrid simulation in a single software environment is realized to model the power grid which obviates the need to simulate the complete grid with a lower discretized sample-time. As an outcome, an environment is established interconnecting the virtual model to the real-world devices. The inaccuracies linked to the power components are examined at length and consequently a suitable compensation strategy is devised to improve the performance of the hardware under test (HUT). Finally, the compensation strategy is also validated through a simulation scenario.

Keywords: power hardware-in-the-loop (PHIL); power interface (PI); hardware under test (HUT); hybrid simulation; real-time simulator (RTS)

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1. Introduction

The past few years have experienced an unprecedented growth of distributed energy resources (DER) globally. The fast moving energy transition towards decentralized energy systems leads towards several technical challenges for the grid operations, especially at low voltage distribution levels highlighted in a detailed report by CIGRE [1]. Performing simulation studies in a virtual environment is one of the ways to analyze these challenges and observe the "what-if" scenarios for power system operations. In simulation studies, the DER units interfacing grids can be modelled in detail to study the dynamics and also simply as a power (P–Q) source [2]. The latter is convenient while performing simulation studies to analyze voltage stability and power flow analysis. However, the simulation approach using a simplified DER unit model have its limitation and may sometimes be inaccurate owing to the complications in modelling the power electronic interfaces [3].

The simulation studies might not indicate the challenges involved during real operations of a device in the field such as undesirable power flow and response time to state change. Power hardware-in-the-loop (PHIL) simulation approach has provided an efficient platform to perform such experiments integrating real hardware and testing of control algorithms on the hardware to study its operational response in real-time with a virtual grid. Motivated by the increasing importance of PHIL simulation for DER integration studies, this paper presents the development of a PHIL test-bench to simulate a low voltage distribution grid (LVDG) in connection with a real power component with the ability to

operate dynamically as load and source. The idea behind is to test the dynamic behavior of the component and the inaccuracies which affects the smooth operation of a PHIL setup. Understanding these challenges gives an insight on the performance of the components in PHIL environment and enables to devise relevant remedies to eliminate the associated errors which may otherwise not be highlighted in simulation-based studies.

In most of the literature concerning PHIL framework for DER integration the commercial devices [2,4–6] and their controls are tested in a PHIL environment. This study rather focuses on an amplifier in current-controlled (CC) mode as hardware under test (HUT) to obtain desired power flow into or from the grid through reference signals generated from the virtual environment. In this paper, the operation of the amplifier as power interface (PI) and HUT will be analyzed in a PHIL setup to characterize its response and its impact on the virtual power grid simulated in real-time. This in turn would lead to the effective use of amplifier in load/regenerative mode for future PHIL tests to perform DER integration studies and analyze advance control strategies. Apparently, the use of such hardware devices coupled in a simulation environment poses operational challenges due to the dynamic behavior of its components. This paper aims to investigate the same and to propose the required adjustments in a bid to improve the components performance. A very recent study by Ustun et al. [7] analyzes the behavior of smart inverters during faults. It has also shown that software/hardware adjustments are required to study the inverters dynamics in simulation environments. The novelty of the setup in this study is also the fact, that the power flow for the HUT is controlled from the virtual environment through reference current signals evaluation algorithm synchronized with the grid voltage and based on power set-points.

A PHIL setup requires a PI to transmit signals (voltage/current) from the simulated environment to the real hardware and vice versa. Stable operation of PHIL is ensured by means of an interface to minimize the influence of measurement probes and power amplifiers on system dynamics [8]. In referenced studies [8,9] the common interface algorithms for PHIL simulation are discussed in detail. A lot of research has been carried out to improve in general the accuracy of the PHIL simulation [10–12], compensation of the PHIL simulation interface [13], and design considerations [14]. The issues related to stability of a PHIL experiment are also highlighted in detail in referenced studies [15–17]. Similarly Zha et al. [18] discusses the accuracy of the complete setup using virtual impedance method. However, in this paper the characterization is performed at component level by observing its dynamic behavior. The stability analysis of the system is not the focus but rather the inaccuracies resulting from specific power components in a PHIL setup. For the interface, the basic structure with an ideal transformer model–voltage type interface as shown in Figure 1 is adopted. The modelled grid is represented by an equivalent voltage source and impedance. The complete workflow is explained in detail in Section 3.2.

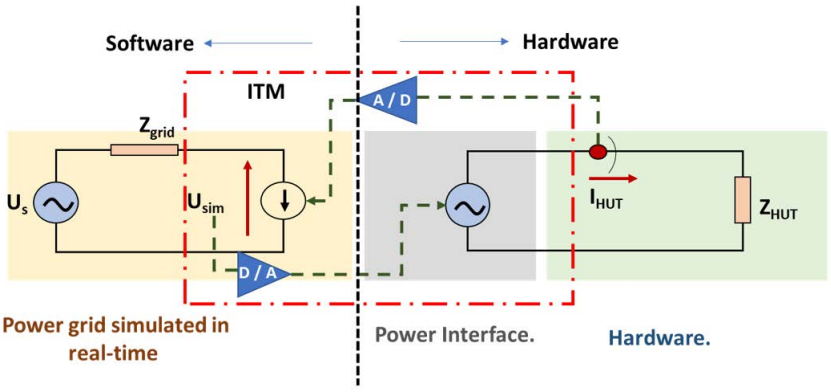

Figure 1. Power hardware-in-the-loop (PHIL) system architecture with ideal transformer model-voltage type interface.

The real-time simulators (RTSs) have discrete behavior [3] and the solution is computed at discrete time instances known as simulation time-step or sample-time. For 50/60 Hz power systems, the simulator needs to be roughly executed with a 50 µs time-step or lower to analyze the power system transients [19]. Executing power systems at such low time-steps can overload the processors of the RTS. For simulating large power systems, the parallel computational capabilities of the RTSs can be utilized by distributing and executing the grid model into multiple cores of the RTSs as shown in Hooshyar et al. [20]. In this paper, the hybrid simulation approach is implemented to model the distribution grid to ease up the burden on the processors of RTS. The general idea is mainly adopted from the PhD dissertation [21] and similar approach with different interfacing techniques is explained in referenced studies [22–25]. The complete hybrid model is developed in a single environment of Simulink®, MATLAB [26], which is also used as a software interface for real-time simulation.

The remaining paper is organized in the following structure. Section 2 presents the use of Simulink to develop a complete hybrid simulation model. Multiple scenarios are implemented, and the result is illustrated to explain the functionality and relevance of hybrid simulation with respect to PHIL simulation. Section 3 explains the development and approach related to the PHIL setup. The method to execute the setup is scripted in detail along with the scenarios to be implemented. Section 4 illustrates the comprehensive results concerning the performance of the PI and HUT. Section 5, summarizes the discussion of the results, main outcomes, and optimization recommendations for future work. Finally, Section 6, concludes the paper.

2. Development of Hybrid Simulation Model

2.1. Equivalent Circuit Representation

The phasor simulation method for power system analysis has limitations as it only computes the phasor values of the parameters such as voltages and currents at each time-step. The fundamental frequency is usually maintained throughout the simulation. On the contrary, detailed studies using electromagnetic transient (EMT) simulation method with much lower time-steps (microseconds to seconds) for large power networks to be executed on RTS would require high computational power. Hybrid simulation serves an interim purpose by incorporating both techniques, as part of the system is simulated in phasor domain and the remaining in EMT or discrete domain in which the high frequency transients needs to be studied and instantaneous values of the signals can be analyzed. The approach to define interface practices between the two connected sub-systems in a hybrid model can be found in the literature [27] along with equivalent circuit representation on both sides [22,28]. To develop the hybrid simulation interface, the important aspect is the equivalent circuit and the interface bus at which the exchange of data takes place. The equivalent circuit representation followed in this paper to exchange the boundary conditions in hybrid simulation is illustrated in Figure 2 and also summarized in PhD dissertation [21] from different studies. As shown, the discrete sub-system simulated at a time-step of 100 µs is represented by a current source in phasor domain whereas the phasor sub-system simulated at the fundamental frequency is represented by a Thevenin circuit with voltage source and grid impedance.

The Thevenin equivalent impedance for phasor sub-system representation in discrete domain needs to be calculated at the interface bus in phasor domain in order to update the Thevenin voltage source [21]. Mathematically, the relations can be represented as the following Equations (1) and (2) modified from [23] using subscripts as shown in Figure 2.

$$Z_{th(p)} = R_{th(p)} + j * w_s * L_{th(p)} \quad (1)$$

$$V_{th(p)} = V - I * Z_{th(p)} = V_{th(p)} * e^{j\theta} \quad (2)$$

where $Z_{th(p)}$ is the equivalent Thevenin impedance characterizing the grid modelled in phasor domain, $V_{th(p)}$ is the Thevenin voltage phasor in phasor domain, V and I are the phasor

domain voltage and current injection at the interface bus. Using the current source to represent the discrete sub-system is a direct approach compared to other equivalent methods which includes representation via a power source or a Thevenin (Norton) equivalent [29].

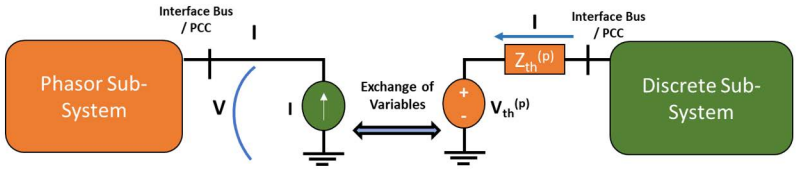

Figure 2. Equivalent circuits and boundary conditions for interaction between two simulation domains.

2.2. Data Exchange

As both the sub-systems are coupled, the output from one simulation domain is transmitted as an input to the other. Desired equivalent circuit values including impedance, voltage amplitude, voltage phase angle, current, and frequency are required to be extracted dynamically at each time-step. Firstly, in discrete domain the values from the phasor domain at the fundamental frequency are transformed into a waveform. Secondly, the phasors (magnitude and angle) are extracted from waveforms in discrete domain using fast-Fourier transform (FFT) at the fundamental frequency before feeding the values back to the phasor domain [23]. Data must be transformed into appropriate forms before exchanging between the two domains as shown in the Figure 3 below:

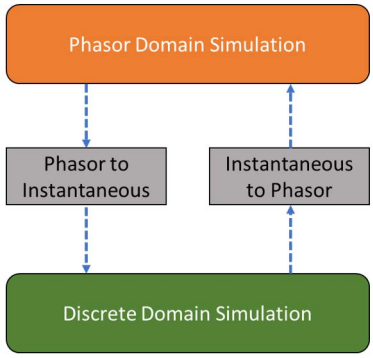

Figure 3. Data exchange during hybrid simulation between two different simulation environments.

2.3. Co-Simulation Workflow

In PHIL simulation, the interface bus represents the point of common coupling (PCC) at which the voltage is emulated in real-time and at which the hardware is connected. The simple radial LVDG network being considered in this paper follows the MONA–8002 structure from the MONA Project 2030 [30]. The topology of the distribution grid and details about the distribution line parameters are defined in Appendix A. The hybrid simulation workflow of the LVDG developed in Simulink is shown in Figure 4 with the equivalent circuits interconnected at the selected interface bus. The corresponding voltage (magnitude and phase) at the interface bus is extracted from the phasor domain. The values are transformed into three time-varying waveforms in discrete domain at the fundamental frequency using Equation (3).

$$U_a(t) = U_m * \sin(2 * \pi * f * t + \theta_a) U_b(t) = U_m * \sin(2 * \pi * f * t + \theta_b) U_c(t) = U_m * \sin(2 * \pi * f * t + \theta_c) \quad (3)$$

where U_m and θ represents the magnitude and angle of the respective voltage phasors obtained from the phasor domain. A balanced grid network is assessed for convenience; therefore voltage magnitudes will be similar with an almost fixed phase difference of

±120 degree. The voltage waveforms for each phase are fed to the controlled-voltage (CV) sources as a source signal after which the sinusoidal voltage is generated. To evaluate the Thevenin equivalent impedance of the phasor model the impedance measurement block in Simulink is used. The block measures the impedance between the two phases as seen from the interface bus, as a function of frequency. The impedance is computed during initialization. For a three-phase circuit, to acquire the positive-sequence impedance the multiplication factor of $(\frac{1}{2})$ is to be used to rescale the measured impedance [31]. The real part of the impedance represents the value of the resistance whereas for the reactive part the corresponding value of the inductor is evaluated by using Equation (4).

$$Z_{pm} = Z_r + jZ_L; R_{phase} = \frac{1}{2} * Re\{Z_{pm}\} \text{ and } L_{phase} = \frac{1}{2} * \frac{Im\{Z_{pm}\}}{2 * \pi * f_{nom}} \rightarrow \frac{1}{2} * \frac{Z_L}{2 * \pi * 50} \quad (4)$$

The equivalent impedance is only measured once and assumed constant as no modifications are made in the network configuration. The two sub-systems (phasor and discrete) are interconnected with each other in a single model which is the advantage of using Simulink environment. Two different powergui blocks are segmented separately in each sub-system. It provides the option to choose the simulation method for the circuit and is required to simulate any model with Simulink-Simscape specialized power system blocks. For the phasor sub-system the phasor solver is selected indicating that the phasor values of electrical signals will be computed at each time-step at the fundamental frequency of 50 Hz. While in discrete sub-system the solver is set to discrete with a sample-time of 100 µs indicating that this portion of the network is simulated as electro-magnetic transient with solution computed at each time-step. Both of the sub-systems are operating simultaneously in different simulation domains constituting the idea of hybrid simulation. In a nutshell, the instantaneous phasor values are transmitted to the discrete domain to be converted to waveforms. Likewise, the phasor values are extracted from waveforms in discrete domain and transmitted to phasor domain to represent the total power being consumed/injected in the network at each time instant. The whole data exchange takes place at the interface bus.

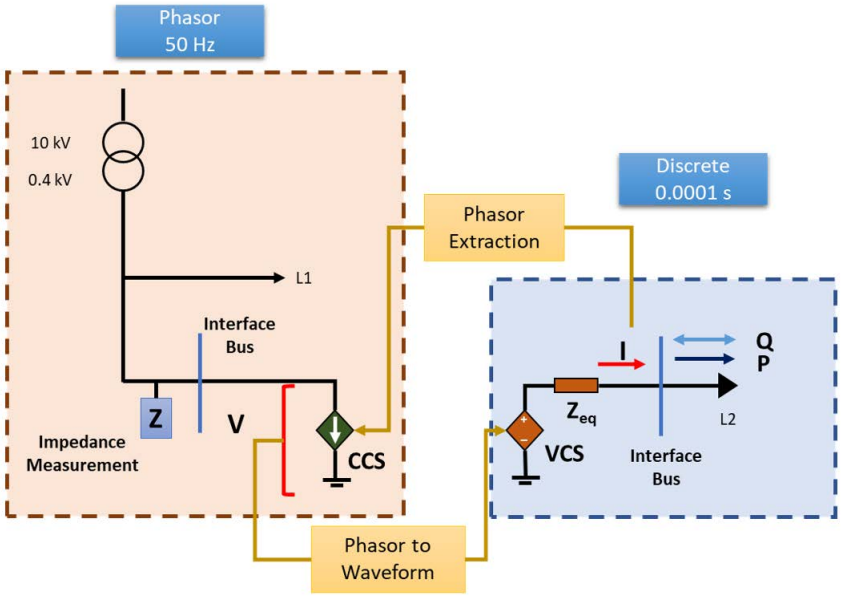

Figure 4. Development and workflow of hybrid simulation model for a power distribution grid with one interface point.

The hybrid simulation approach deems accurate for real-time simulation as part of the grid model simulated in discrete domain can provide the desired discrete instantaneous waveforms. The discretized waveforms can be processed by the RTS in PHIL simulation. That is why a small part of the distribution grid is modelled in discrete domain in this paper which serves the mentioned purpose. Similarly it also provides the interface to treat

the measured feedback signals of the HUT in discrete domain and integrate it into the virtual grid model.

2.4. Offline Hybrid Simulation

The practical functioning of the hybrid simulation is illustrated in this sub-section through two scenarios. The key parameters for the scenarios are defined in Table 1. For the first scenario, a constant three-phase resistive load is connected at the PCC in discrete domain at bus # 2. The voltage and current should be in phase at bus # 2 representing a pure active power being drawn by the resistive load. The idea behind this scenario is to observe whether the waveforms are purely in phase or if there is any sort of delay due to the partition of the network and equivalent circuit representations. As a driving signal for the CC sources in phasor domain the phasor values of the current flowing through the circuit is fed back.

Table 1. Offline hybrid simulation scenarios to assess the functioning of the hybrid model.

Scheme	Load	Network Partition Point	Phasor/Discrete Sample-Time
Constant Active Power	TP Resistive Load (0.5 kW)	Bus 2	100 ms/100 µs
Dynamic Load–Step Response	TP Resistive Load (2.5 to 5 kW)		

The result from the first offline simulation scenario is shown in Figure 5. The waveforms represent an ideal resistive load. The voltages and currents are completely synchronized and in phase with each other as observed at the zero-crossings. This presents an insight into the functioning of the hybrid model in case of a conventional load. The results show that there seems to be no lag or delay and the exchange of variables at the interface is carried out smoothly.

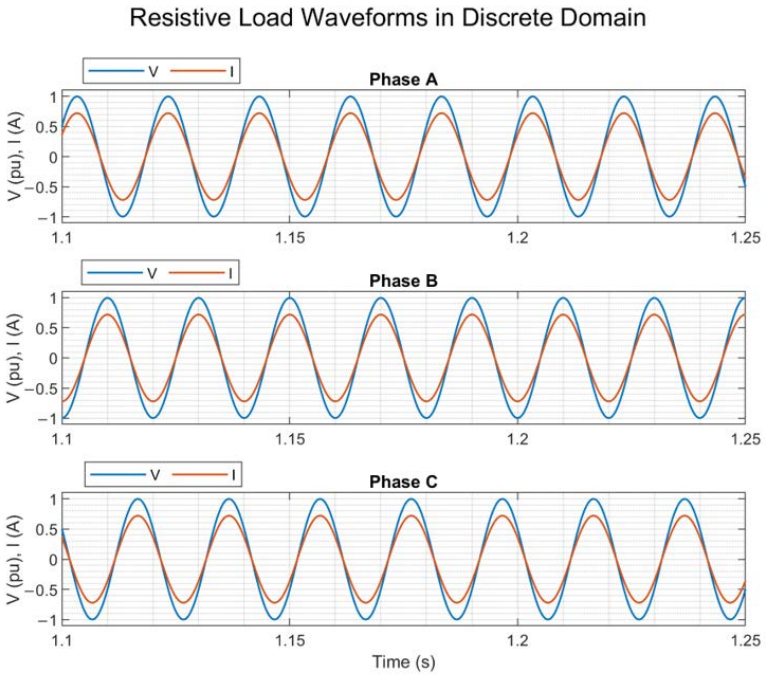

Figure 5. Instantaneous three-phase voltage/current waveforms for a resistive load connected at the interface bus in discrete domain. Represents in-phase synchronization with no undesired phase shifts.

To further observe the fidelity of the hybrid model, in the second scenario the voltage and current at the interface bus is compared from both the domains. In principle, the phasor voltage at the interface bus transmitted to the discrete domain should generate the waveform of the same amplitude. Similarly, the current fluctuations should also be

captured in discrete domain at the same time instant. The load is replaced by a three-phase dynamic load, the power demand of which is stepped-up during the simulation to observe the imminent current change in both domains. The voltage and current comparison is shown in Figure 6.

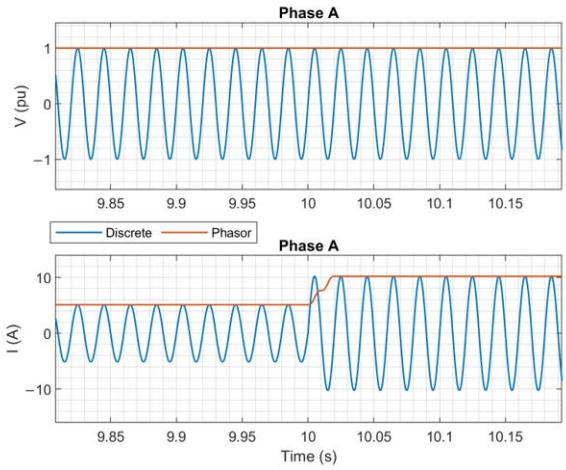

Figure 6. Step increase in power demand at 10 s. (**upper**) Voltage synchronization between the two interconnected domains. (**lower**) Prompt change in current drawn analyzed in both domains due to step increase in power demand.

The plot in Figure 6a shows the comparison of the voltage measured from both domains at the interface bus. In Figure 6b, it can be observed that there is a variation in current magnitude due to the change in power demand at that instant which is also followed by current waveform. The change in phasor magnitude is captured dynamically at the same instant as seen by the instantaneous waveform results. The change of current phasor to a new value happens over one grid cycle, i.e., 20 ms. The design of the hybrid simulation in the Simulink platform is presented at length in this section. The implemented scenarios help in understanding the functioning of the hybrid simulation model. The results from the scenarios evidently show that the hybrid model is running in synchronization, the equivalent circuit representations does not introduce any significant fluctuations or delay in voltage and current at the interface bus. For the development of PHIL simulation environment, the load connected in the discrete domain will be removed and an actual power device in real-world will serve as a load.

3. PHIL Simulation

3.1. Description of PHIL Components

The PHIL system comprises of three main parts [4] and the respective components used for this experiment are also defined as follows:

- Hardware under Test (HUT): It refers to the power component, the response and behavior of which is to be examined. In this experiment, the HUT is a switched-mode 30 kVA power amplifier operating in CC mode from Regatron AG®, Rorschach, Switzerland f type TopCon TC.ACS with a bandwidth of 5.0 kHz. This series from Regatron AG supports the operation of CC amplifiers in both "Feeding Mode" for positive power and "Regenerative Mode" for negative power [32]. This characteristic is quite helpful while performing PHIL studies for DER integration. As the HUT can serve dynamically as a load and also as a feed-in source based on the power set-points.
- Power Interface (PI): It enables to get the operating points of an electrical power system from the simulation environment and makes it available in the real world (for instance: voltage at the PCC). The power interface in this experiment is a switched-mode voltage source, a 50 kVA 4-Quadrant grid simulator from Regatron AG® also of type TopCon TC.ACS with a bandwidth of 5.0 kHz operating in voltage-controlled mode [32]. It op-

erates as a grid simulator emulating the voltage at the PCC. The TC.ACS amplifiers have built-in protection features programmed to prompt circuit breakers in case of phase overcurrent and over voltage leading to electrical isolation of the device.

The use of Regatron devices as grid simulators/power interface is quite common for PHIL simulation. The application of Regatron power amplifier as a PI is discussed in [4], to test the smart grid controls using two different PHIL setups. Similarly, in [33] a PHIL setup is implemented to validate the developed battery-model in real-time using Regatron's amplifier as a power interface. The vibrant behavior of the power amplifier is discussed in detail in this paper to illustrate the considerations that needs to be made if it is used as a PI for PHIL simulation.

- Real-Time Simulator (RTS): The real-time simulator simulates the grid model in real-time and performs digital-to-analog (D/A) conversion of the reference signals and vice versa. It transmits the scaled down analog values from the simulation environment to the power interface and from the HUT (e.g., current) back to the simulation environment. For this experiment, a Speedgoat real-time target machine [34] is used as a RTS with the mathematical grid model developed in Simulink executed on its multi-core processors. The IO334 field-programmable gate array (FPGA) boards are used for analog-to-digital (A/D) and D/A conversion of the signals. The boards are interconnected with the target CPU through peripheral component interconnect (PCI) express connection.

In general, concerning the real-time digital simulators various options are currently being utilized. Some of the most popular RTSs with their applications and software interfaces are defined in Table 2. For data acquisition during the real-time simulation, the high bandwidth DEWESOFT devices [35] are used in this experiment.

Table 2. Real-time simulators for PHIL testing of multiple applications. Modified from [36].

Simulator	Software Interface	Applications
Opal-RT	RTLAB, Simulink, MATLAB, Labview and HYPERSIM	Power electronics, control systems, HIL, Power systems like smart grid.
RTDS	RSCAD, MATLAB and Simulink	
Speedgoat Real-Time Target Machine	Simulink, MATLAB	
National Instruments (NI) Hardware	Labview	
Typhoon	Typhoon HIL Control Center, MATLAB, and Simulink	Power electronics, control systems, HIL, Microgrids.
dSPACE	MATLAB and Simulink	Power electronics, real-time control, rapid prototyping, power systems like smart grid.

3.2. PHIL Simulation Workflow

The PHIL simulation environment is represented in a layered diagram in Figure 7 with the measured signals of interest followed by the explanation of the complete workflow.

The V_{ref} is the reference voltage signal at the interface bus from the virtual simulated grid. This digital signal is scaled-down and converted to analog signal by the RTS. It is transmitted to the VC power amplifier operating as a PI. The PI which is connected to the HUT amplifies the voltage to the nominal values. The operation of the HUT as load is defined by the reference current signal I_{ref}, which is synchronized with the V_{ref} and is evaluated based on power set-points. The I_{ref} is scaled-down and sent via RTS to the HUT. The analog current that flows between the two power components is measured and extracted via the PI internal ports and converted from analog to digital by the RTS to have the actual current in the virtual simulated model. This signal is then fed back to the CC sources in the grid model. The RTS generates the reference values within the range of

$\pm 10\ V_{pk}$. The scaling factors for D/A conversion and vice versa are stated in Equation (5). A V_{ref} of 10 V_{pk} refers to a 432 V_{pk} from the PI output.

$$Actual\ Voltage_{pk} = \frac{432}{10} \times V_{RT} \tag{5}$$

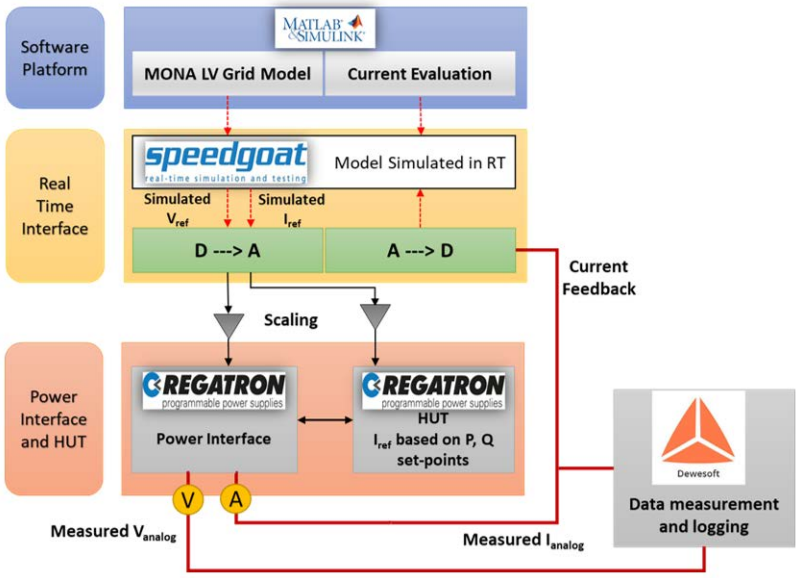

Figure 7. PHIL simulation environment illustrated with the components, data acquisition, and feedback signal.

3.3. Startup and Execution

The step by step execution of the PHIL simulation setup is listed below. The method is not lab specific but rather hardware components and simulation environment specific and can be followed for a general PHIL setup comprising of the same arrangement.

- The simulated LVDG modelled in Simulink platform is compiled in real-time by setting the simulation mode in Simulink to "external". After the model is built on the Speedgoat RT target machine, the simulation is executed which produces a scaled-down V_{ref} signal at the chosen PCC bus for the PI.
- The interface produces the amplified voltage at its terminals based on the set-points received by the RTS. The voltage limits and the reference root-mean square (rms) values must be cross checked before switching on the PI.
- After the voltage is successfully established, the scaled down I_{ref} current command is sent to the RTS. The AC voltage at the power interface is then applied to the HUT by switching it on. In this manner, the external power connection between the PI and the HUT is established.
- The measurements (current and voltage) are logged externally by means of data measurement devices from DEWESOFT. Additionally, the current of the HUT is fed back to the simulation environment. The currents can be obtained directly from the out ports of the PI by establishing a connection from respective port of the amplifier to the RTS and ultimately extracting it from analog-in channels of the RTS in simulation environment.
- Finally, the injection of acquired external currents to the CC sources in the virtual grid model closes the PHIL loop.

The reference current injection signals for the HUT are evaluated based on power set-points and voltage at the PCC. Figure 8 illustrates the simplified process flow behind the evaluation of the reference three-phase injection currents for the HUT. The three-phase voltage splits into direct and quadrature axis values inside the discrete three-phase phase-

locked loop (PLL) block. It is further treated to calculate the frequency and wt of the signal respectively by means of a variable frequency block and PI controller. The discrete three-phase PLL block is part of the three-phase dynamic load block mask in Simulink and is developed by P, Girroux and G, Sybille from the Power System Laboratory, Hydro-Québec research institute (IREQ). Detailed model of the respective Simulink block and its use in current evaluation block is shown in Appendix B.

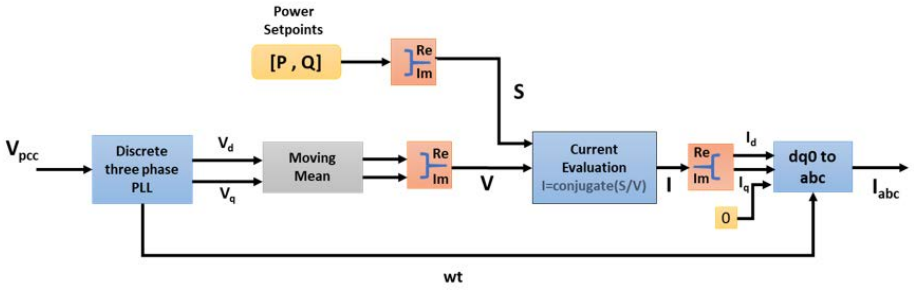

Figure 8. Reference current evaluation for current-controlled (CC)-amplifier based on voltage at the point of common coupling (PCC) and desired power set-points.

3.4. PHIL Simulation Scenarios

To observe the functioning of developed PHIL setup, the two main scenarios implemented are defined in Figure 9. The first scenario intends to observe the response of the power interface at no load (i.e., I = 0). It is to establish the characterization of the power interface to find out the associated errors, noise, or delay. In this scenario the aim is to observe whether the commanded V_{ref} signal at the PCC bus sent by the RTS is followed by the power interface or not.

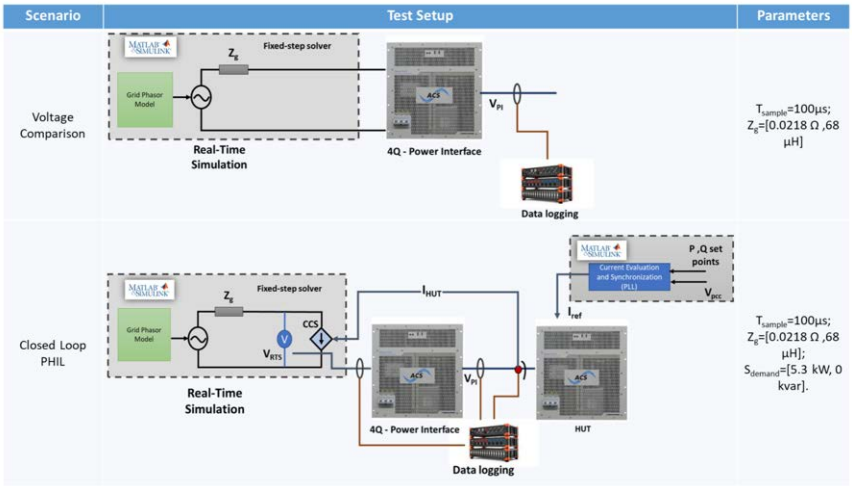

Figure 9. Scenarios to analyze the developed PHIL simulation environment, power components inaccuracies and dynamics.

The second scenario represents a closed loop PHIL setup in which the HUT is subjected to draw power through I_{ref} signals. In this scenario, the capability of the HUT is analyzed to follow up the commanded I_{ref} signals, to observe the desired power flow and more importantly the dynamic behavior of the hardware coupled with the simulation environment.

4. Results

4.1. Scenario 1: Voltage Comparison–Open Circuit Test

The plot in Figure 10 shows the comparison between the single-phase voltages. The V_{ref} is a scaled-down analog signal from the simulator that is being amplified by

the interface. For the convenience of comparison analysis, the V_{ref} is scaled-up using the mathematical relation shown in Equation (5). From the sub-plot in Figure 10a, it seems that the V_{ref} is accurately superimposed by V_{PI}. To get more details, the second sub-plot in Figure 10b is presented which is a zoomed-in version at one of the peaks and the sub-plot in Figure 10c further illustrates the zoomed-in version at the zero-crossing to visualize the time delay.

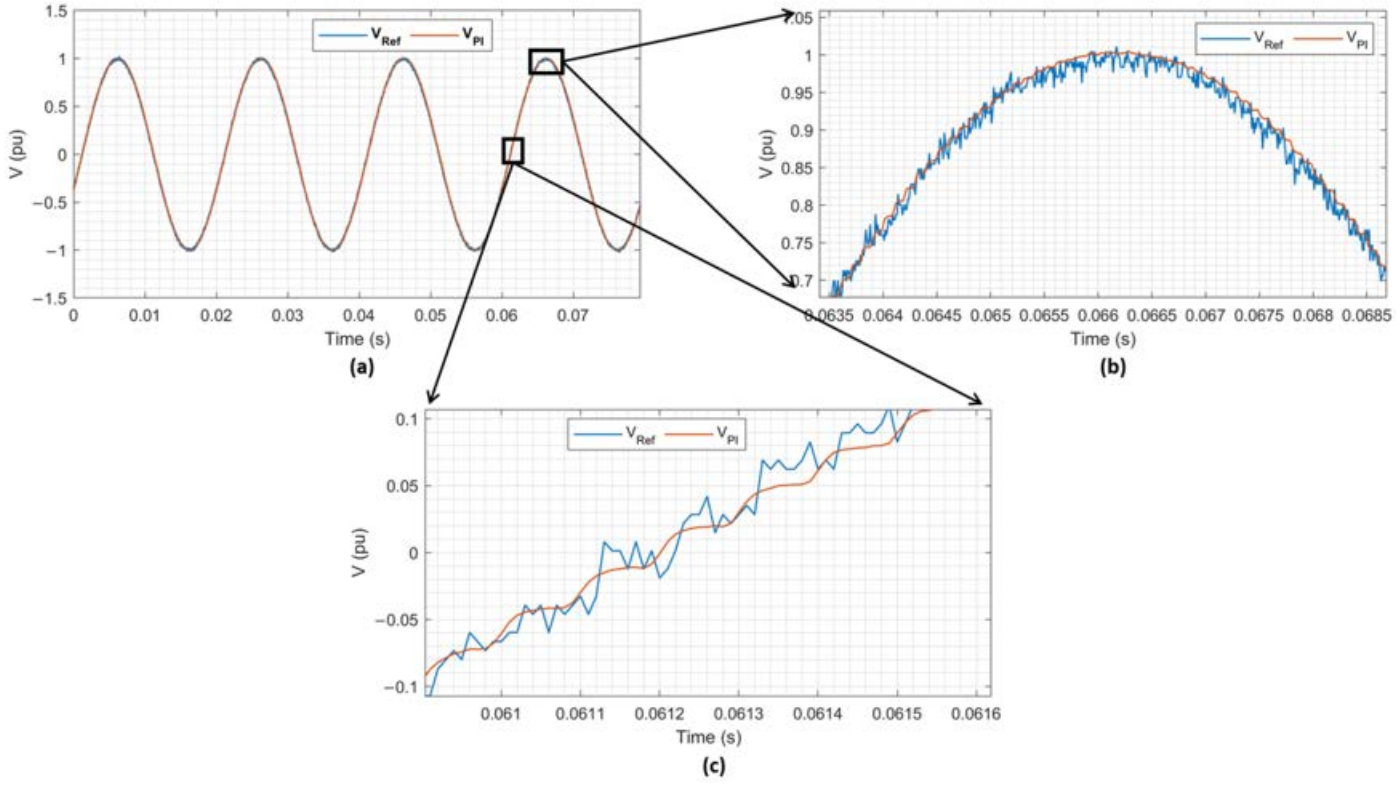

Figure 10. Voltage Comparison. (**a**) Reference and power interface generated voltage waveforms in real-time. (**b**) Zoomed-in version at one of the instants to analyze the inaccuracies between the simulated and real-world interface output voltage. (**c**) Zoomed-in version at the zero-crossing to analyze the time delay.

The noise associated with the simulator output can be easily distinguished from the sub-plots. As far as the power interface is concerned, the default built-in filters of the amplifier eradicated the noise to some extent and the output appears out to be smoother. The effective difference between the two signals results from the latency of the setup and introduces minute phase-shift in all the phases. To investigate the magnitude difference i.e., the offset due to the power interface, a test case is performed as explained in the following sub-section.

4.1.1. Test Case: Voltage Step Response

The inaccuracies in magnitude are analyzed through this interim test case. A simple grid is modelled using a Thevenin equivalent circuit depicted by a voltage source and impedance. The same parameters for impedance are utilized as defined in Figure 9 whereas for the voltage source a dynamic step-input is used to vary the voltage levels of the reference signal from (50–300 V_{rms}) at regular intervals in steps of 25 V_{rms}. The result depicting the rms offset from the interface at each V_{ref} is shown in Figure 11. An almost direct relation is thereby observed between the two. The magnitude of the reference and amplified signal is almost the same at low voltage levels with minimal difference of 0.1 V_{rms}. At standard

voltage of 230 V_{rms}, the offset is quite significant and increases further with the increase in V_{ref}.

$$V_{PI}(Offset) = 0.0049 \times V_{ref} - 0.012 \quad (6)$$

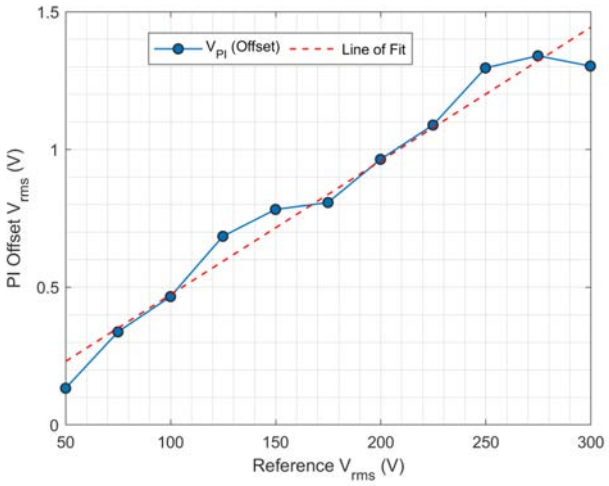

Figure 11. Relation between the rms power interface offset ($_{VPI}$) based on reference voltage (V_{ref}) from the real-time simulator (RTS).

To characterize the power interface behavior, a line of fit is generated shown by red-dotted line in Figure 11. The relation between the reference input signal and the actual generated offset by the PI at that particular input is defined by Equation (6). It is evident that for a range of low simulated reference values, the PI outputs the voltage signal of approximately same magnitude.

4.2. Scenario 2: Closed Loop PHIL Simulation

In this scenario the complete closed loop PHIL simulation is executed and the response of HUT as an active load coupled with the simulation environment is analyzed as shown in Figure 12. The instantaneous waveforms in Figure 12a show that there is a phase difference between the voltage and current as observed at the zero-crossings with power factor (pf) measured to be leading 0.97. The statement is supported with the power flow of HUT shown in Figure 12b. Apart from the commanded active power, the capacitive reactive power is also present and observed by the virtual simulated grid. The oscillatory behavior in power is due to the current harmonics introduced by the HUT. Although the I_{ref} is being generated based on active power set-points, the HUT exhibits the nature of a capacitive-resistive load due to its internal design components. This could be due to the parasitic capacities being used in switched-mode power amplifiers behaving as a low-pass filter for the output. The dynamics of the HUT's component results in an uncontrolled and undesired reactive power flow.

To acquire more insight on the configuration of parasitic capacities of the HUT, an interim test is performed. No power is being demanded from the HUT and the power exchange between the interface and HUT is established. The input voltage levels were varied again with steps of 25 V_{rms} to observe the dynamic behavior of the HUT under different voltage levels and no external active power demand. The response is shown in Figure 12c. By default, the HUT behaves as a capacitive load for the simulated grid exporting reactive power. At the standard 230 V_{rms}, a capacitive reactive power of around 1.18 kvar is present. The reactive power increases with the voltage as shown by the blue line. The green line represents the active power consumption of the HUT and it can be seen that it is almost negligible. Therefore, the dynamic behavior of the HUT can be simply

modelled as a capacitor and using the reactive power value at the standard 230 V_{rms} the default parasitic capacitance is approximated as shown in the following Equation (7).

$$Q_p = \frac{{V_{rms}}^2}{Z_c} = \frac{232^2}{\frac{1}{2*pi*50*C_p}} \rightarrow C_p = 25\ \mu F \quad (7)$$

where, C_p represents capacitance per phase. The presence of the default capacitance creates reactive power flow depending on the voltage level at the HUT terminals irrespective of the active power demand.

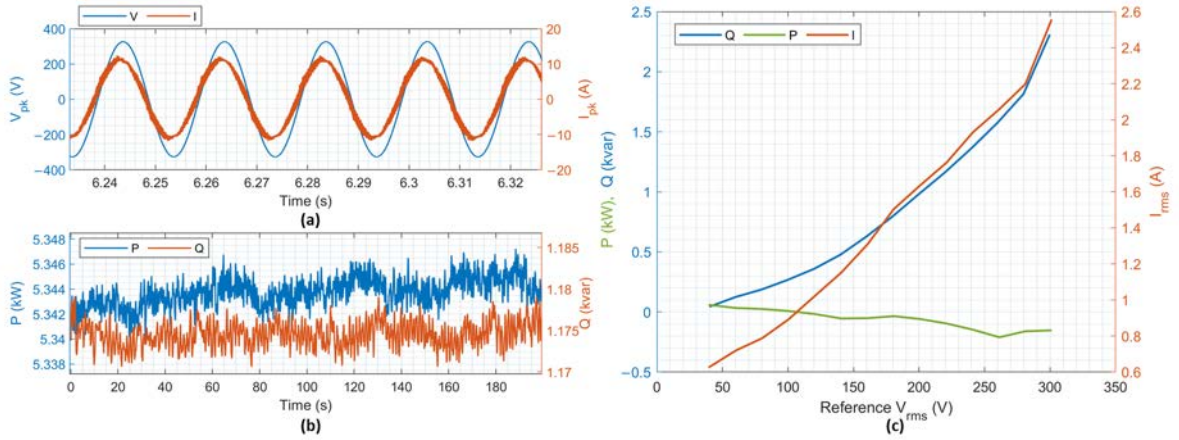

Figure 12. Response of the hardware under test (HUT). (**a**) Waveforms depicting phase difference between voltage and current for a pure active power demand. (**b**) Power flow of the hardware under test (HUT) as experienced by the virtual grid. (**c**) Dynamic behavior of the hardware under test (HUT) with variation in reference voltage (V_{ref}) to examine internal parasitic capacities.

4.3. Power Quadrants

The operation of the power components in general during the PHIL simulation can be characterized through power quadrants shown in Figure 13. The PI emulating the grid voltage is operating in the fourth quadrant and the HUT is operating in the second quadrant. As per IEC 62053-23 explanation of the power quadrants, the interface is the source of active power for the HUT but at the same time it is receiving reactive power from it. Similarly, the second quadrant for the HUT indicates that it is operating as an active power sink and reactive power source.

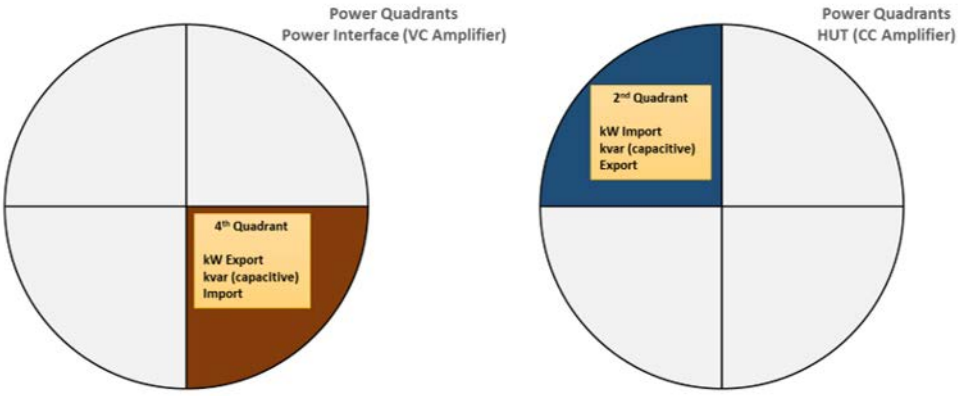

Figure 13. Power quadrants illustrating specific operation of the power components in PHIL setup.

4.4. Static Compensation

The compensation method is based on introducing an intentional delay in time-domain for the generated I_{ref} signal; the process flow of which is illustrated in Figure 14. The static time delay to be introduced is measured by comparing the phase difference between the voltage/current at the HUT terminals and at the PCC in simulation environment. This would lead to the reduction of undesired power flow from HUT. In principal, the phase angle of the I_{ref} and I_{HUT} should be the same but due to the latency of the RTS and dynamic components of the HUT there is a difference which the stated compensation method targets to account for.

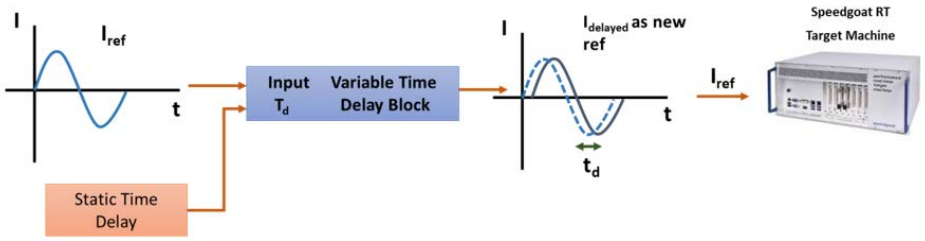

Figure 14. Process flow of static compensation algorithm to control undesired power flow from hardware under test (HUT).

After acquisition of the feedback current signals of the HUT in simulation environment the fast-Fourier transform (FFT) of the signal is performed to obtain the phase-by-phase angles in frequency domain. Only the fundamental components are considered, and the harmonics introduced by the HUT are not compensated. The difference between the phase angles of the I_{ref} and I_{HUT} is evaluated and eventually a static time delay is introduced based on the following mathematical relation shown in Equation (8). Thus the inaccuracies between the power factor (pf) for a certain active load are minimized.

$$360^\circ = 20\ ms \rightarrow x^\circ = \frac{20\ ms}{360^\circ} * x^\circ \tag{8}$$

The results illustrating the performance of mentioned compensation are shown in Figure 15. The power demand for the HUT was increased in steps of 1 kW in the range of (1–8 kW). For simplification, only active power was demanded to visualize the prominent difference as for each case the pf is supposed to be unity. The plot in Figure 15a shows the improvement in pf of the HUT for each power set-point after implementing the compensation. At low power demands, the compensation seems to contribute significantly whereas for high power demands also the compensation attempts to get close to the actual desired pf.

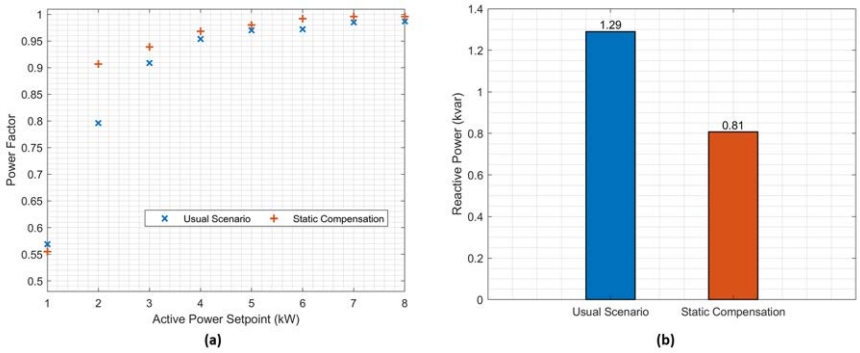

Figure 15. Comparison between usual and compensated PHIL simulation. (**a**) Improvement of power factor for different power set-points through compensation implementation. (**b**) Significant reduction of reactive power flow from the hardware under test (HUT).

The average capacitive reactive power injected by the HUT into the simulated grid is also analyzed to observe the credibility of the developed compensation method. For each power set-point the reactive power was noted, and the statistical mean is generated to visualize the difference in a usual scenario and compensated scenario as shown in Figure 15b. Operating the HUT in usual case results in an injection of 1.29 kvar on average for a specific active power demand and the compensation reduces this default value to an average of 0.81 kvar.

5. Discussion

The discussions of the results are classified scenario-wise.

5.1. Scenario 1

The results of the first scenario in Section 4.1 presented a detailed overview of the power amplifier operation as the PI. It is realized that there is a minute phase difference between the reference and actual generated voltage signals due to the time delay. The delay is contributed by the real-time simulator due to the computation and generation of reference signals within a given time-step. The power amplifier also contributes to a time delay. The amplifier used for this experiment is a switched-mode power amplifier which has high time delays [37]. The time delay ultimately creates a phase difference; however, a very minute phase difference was observed.

The associated noise of the reference signal can also be clearly seen from Figure 10b. The RTS sends an output at each discrete time-step of 100 µs for the modelled grid, which certainly seems to be inefficient for the quality of the signal. The simulator output would probably get better with lower discrete time-steps in the range of 10–50 µs. The lower sample-times were attempted, but as the model was executed on the RTS processors, due to computational limitations, the processor overload error was prompted, and the simulation was not executed. The use of FPGAs in the real-time target machine for the signal generation blocks is recommended to achieve lower sample-times and is planned for the next phase of PHIL tests.

Additionally, the offset of the PI is also studied. On literature review it has been found that the power amplifier has an impedance which prompts the rise in voltage proportional to the load current and is the reason of difference between the V_{ref} and V_{PI} magnitude [13]. In this paper, the voltage rise, i.e., the offset is found to be in direct relation with the reference voltage magnitude for open circuit configuration. The internal impedance of the PI is not evaluated in this paper; the methods to do so are discussed by Wang et al. [16]. The basics on the response of specific power amplifier in a PHIL setup are laid down in detail through the scenario performed in this paper. The scenario provides a holistic picture of the issues encountered in employing the PI for PHIL setups. Adding on to these, respective corrective measures can now be devised to enhance the accuracy of the PHIL simulation. For a general approach on compensation methods, the detailed analysis is conducted in [38] to characterize the power amplifier as power interface. Further methods for the stability and compensation for the power interface are also discussed in referenced studies [39,40].

The test case conducted as discussed in Section 4.1.1 refers to the output of the PI at different input voltages (V_{out}/V_{in}). The same method can be extended to identify the gain of the power interface just by operating it at multiple frequencies in addition to the fundamental component to estimate the transfer function. Details on the impedance and gain (transfer function) would be helpful to accurately model the dynamics of the PI and also carrying out the stability studies. The same is planned for the future work.

5.2. Scenario 2

The results of scenario 2 discussed in Section 4.2 provides insight on the dynamic behavior of the HUT (CC amplifier). The default parasitic capacitance of the HUT is responsible for the presence of capacitive reactive power. The HUT exports reactive power

into the simulated grid at the PCC. The quality of the signals exchanged between the hardware and simulator plays a significant role in accuracy of the real-time simulation, and it is observed that the HUT also causes harmonics leading to a deteriorated current waveform. At lower active power demands, the current waveform is found to be quite distorted and the pf of the system is affected badly. On average, a reactive power in the range of 1.27–1.3 kvar is exported into the simulated grid which also affects the voltage at the PCC.

A simple yet effective compensation method is developed to mitigate the unwanted reactive power. The performance of the HUT is improved after implementation of the mentioned compensation. The method does not affect the topology of the system. The method however has certain limitations as for each power set-point, first the need would be to run the usual case without compensation, observe the phase difference between the I_{ref} and I_{HUT} and then introduce the equivalent time delay. The information from the usual case scenario is necessary to implement the static compensation. On the other hand the advantage is that for active power demands, the compensation method can be implemented directly as the desired pf would be unity and the delay is to be added accordingly. For other power demand configurations (i.e., capacitive, or inductive) additional measures would be required as the HUT already operates as a capacitive load by default.

Further, the compensation reduces the default reactive power significantly by operating the HUT close to the desired behavior. The closed-loop scenario exposes the power flow challenges associated with HUT operated in amplifier mode in a PHIL environment. It shows that deploying such dynamic power components to perform PHIL simulation would require appropriate measures to deal with the challenges highlighted in this paper. For future work, the need is to devise more precise compensation algorithm using proportional integral derivative (PID) controller and implementing a dynamic method so that the phase differences can be tracked more accurately. Successful development of such an algorithm would not only compensate the effect of parasitic capacitance but also reduce the time delay of the whole PHIL setup. It is also necessary to compensate for harmonics as at low power demands the current harmonics are very dominant. An approach is defined by Sansano et al. [41], in which the reference voltage signal for the PI is subjected to phase-shifting harmonic-by-harmonic and phase-by-phase and it is shown that the PHIL simulation accuracy of low impedance grids can be improved.

6. Conclusions

The power components dynamics interconnected with the simulated environment are presented at length in this paper. The study contributes to the fundamental development of a bench-mark PHIL setup to simulate a typical LVDG in a real-time environment. The main contribution of the paper is to comprehend the dynamic response of the power components involved especially the HUT to have the desired power flow. Firstly, the corresponding inaccuracies between the reference and generated voltage related to the PI are discussed. A test case is implemented to define the correlation between the two at different voltage levels. Secondly, the operational complexities of the HUT are highlighted, and subsequent recommendation is presented. The experimental result depicts the viability of the developed compensation method. Irrespective of the Regatron device as HUT, the compensation method defined in this paper can be implemented for any power hardware component that exhibits the behavior of undesired reactive power flow to have it operated as a pure active load.

Furthermore, in the established PHIL setup, the HUT is controlled virtually from the simulation environment therefore it provides more fidelity over a commercial inverter device which is usually the case in PHIL. It can be operated as a dynamic source/sink to study integration of such dynamic prosumers at the distribution grid level. Further, advance control strategies such as machine-learning based reactive-power management can be superimposed on it; its impact in RT gird operations can be assessed and ultimately the same can be implemented on commercial inverters. To achieve that, initially the need

is to first develop the base setup and understand the basic dynamic response of the PI as well as the HUT in controlled mode and this paper presents the same. The next steps entail more research to standardize optimum compensation methods in response to the challenges and decrease collective inaccuracy/instability of the complete PHIL simulation.

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Abbreviations

Acronym	Name
CC amplifier	Current-Controlled amplifier
DER	Distributed Energy Resources
EMT	Electromagnetic Transient
FPGA	Field-Programmable Gate Array
HUT	Hardware under Test
ITM	Ideal Transformer Model
LV	Low Voltage
LVDG	Low Voltage Distribution Grid
PCC	Point of Common Coupling
PCI	Peripheral Component Interconnect
PHIL	Power Hardware-in-the-Loop
PI	Power Interface
PID Controller	Proportional Integral Derivative Controller
PLL	Phase-Locked Loop
RMS	Root-Mean Square
RT	Real-Time
RTS	Real-Time Simulator
VC amplifier	Voltage-Controlled amplifier

Appendix A. MONA Low Voltage Distribution Grid Topology

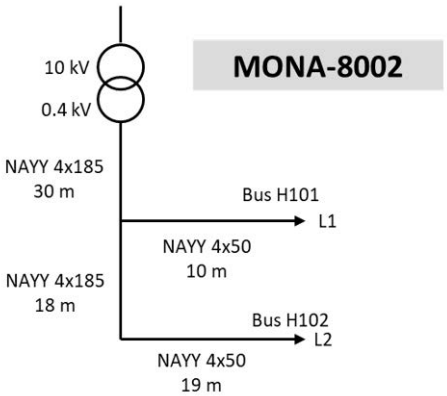

Figure A1. Single line diagram of MONA-8002 low voltage distribution grid (LVDG).

Table A1. Distribution line parameters with respect to line codes and specifications.

Line Code	Resistance (Ω/km)		Reactance (mH/km)		Capacitance (nF/km)	
	Positive Sequence (r1)	Zero Sequence (r0)	Positive Sequence (l1)	Zero Sequence (l0)	Positive Sequence (c1)	Zero Sequence (c0)
NAYY 4 × 50	0.642	2.568	0.083	0.312	670	275.7
NAYY 4 × 120	0.255	1.02	0.08	0.292	797.3	365.9
NAYY 4 × 150	0.208	0.832	0.08	0.292	830	385.9
NAYY 4 × 185	0.167	0.668	0.08	0.292	868.2	409.3

NAYY 4 × 50—The first number represents the no. of conductors while the second number represents its cross-section (mm^2).

Appendix B. Simulink Model Blocks

Appendix B.1. Discrete 3-Phase PLL Block

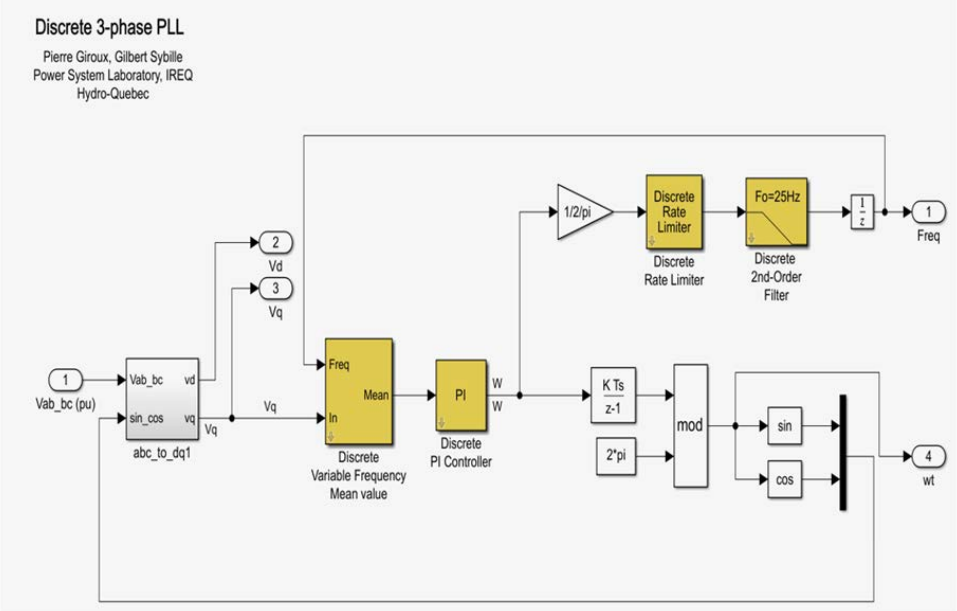

Figure A2. Discrete 3-phase Phase-Locked Loop (PLL) block.

Appendix B.2. Reference Current Evaluation Based on Power Setpoints and Vpcc

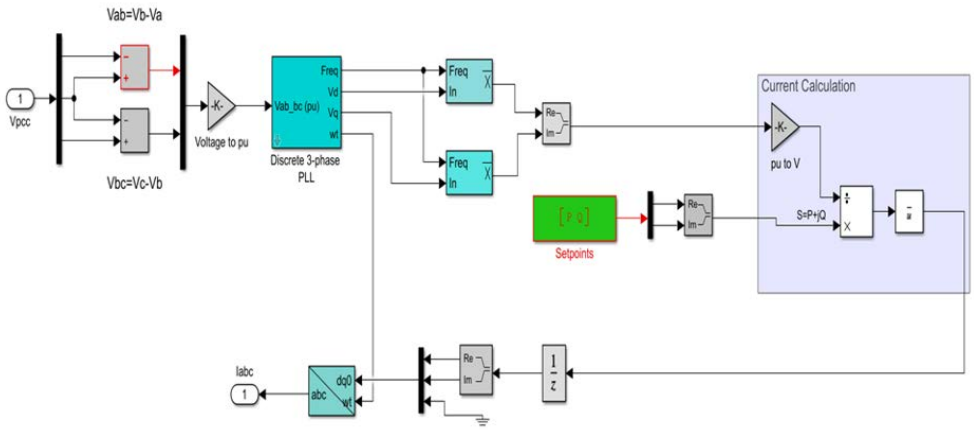

Figure A3. Current evaluation for the hardware under test (HUT) based on power set-points and voltage at the point of common coupling (PCC) in Simulink.

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