Design of an Integrated CMOS Transceiver with Wireless Power and Data Telemetry with Application to Implantable Flexible Neural Probes

Jordan Thimot

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ABSTRACT

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Recent developments in implantable medical devices (IMDs) have created
a need for communication systems integrated directly into the implant with
feedback data for various sensing systems. The need for modern communication
techniques, power delivery systems, and usable interfaces for smart implants
present an interesting challenge for engineers trying to provide doctors and
medical professionals with the best resources available for medical research.

This dissertation will cover the design of an integrated CMOS transceiver
and near-field inductive link used for an IMD and the accompanying CMOS
front end for the application space of neural recording in the brain of lab mice.
The design process of the CMOS IC, along with thinning techniques, the near-
field inductive link, and the design of an external reading system will be dis-
cussed in detail. The various wireless power and data telemetry techniques
applicable for IMDs and their strengths and weaknesses will also be described.
Software techniques and implementation for real-time analysis of a high data
rate communication system from the designed IMD will be covered. Finally,
transceiver verification will be given for both power and data telemetry under
various scenarios, with front end verification performed via controlled lab bench
experiments using input sinusoidal wave forms.

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Chapter 1

Introduction

Inductively coupled links have become commonplace in supplying both power and data to implantable medical devices (IMDs). Previous wireless IMDs have typically used off-chip receiver (Rx) antennas and circuitry for telemetry and voltage rectification, increasing the required volume of the implant considerably and creating a rigid interface between implant and tissue that triggers stronger immune response [1–4]. In our case, we seek to push down the scale and form-factor of RF transceivers and wireless powering to create millimeter-scale antennas for these links and do so on-chip, while achieving Mbps data rates and mW-scale power levels at mm-scale implantable depths. Other approaches for scaled power transfer such as ultrasound [5], which have advantages in implantation depth, do not allow high-data-rate telemetry because of MHz-scale carrier frequencies.

Our wireless implant has the Rx antennas integrated on-chip and, by thinning the

substrates to 15µm, allows the implant transceiver to displace an overall volume of less than 0.08 mm3 with the Rx coils covering an area of only 4 mm2. Once thinned, the integrated transceiver has the form factor of tissue paper allowing it to conform to tissue surface. Removal of the lossy silicon substrates also improves wireless power transfer (WPT) efficiency.

The requirements for mW-scale power and Mbps-scale data rates necessitates the use of backscatter techniques (passive modulation of Rx resonance frequency) for data uplink (IMD to outside). Other high-data-rate telemetry techniques such as the use of ultra-wide-band (UWB) transmitters or non-passive frequency modulation, require larger antennas and power amplifiers to drive the antennas to achieve acceptable bit-error-rates (BERs) [6]. The use of millimeter-scale integrated coils produces smaller transmission radii and lower power transfer efficiency (PTE) than what would be achievable with larger, lower-loss antennae. Backscatter data transfer at high-data-rates with this antenna scale through lossy media, even at mm-scale implantation depths, also presents intersymbol-interference (ISI) challenges, which we overcome with extensive equalization of the channel.

This thesis will be divided into 5 chapters including this introduction. The remainder of chapter 1 provides an background information to the three main topics covered by the application space of this work. Specifically the three section to be covered will be a discussion on the history of wireless power systems, with an emphasis on how system design changes in biological media, a discussion of wireless data communications techniques, with emphasis of reconstruction in an unknown wireless channel, an introduction to the intended application space of the transceiver system, neural interface systems for recording in the brain of mice. Chapter 2 will cover the design of the ASIC itself, specifically covering the circuit design of critical blocks and designed performance metrics. Also covered will be the thinning and post-processing that is performed on the chip to become flexible and reduce implant volume. Chapter

3 will cover the design of the external reader system. Heavily emphasis in this section will be devoted to data reconstruction of the back-scattered data signal, as a custom and rigorous equalization technique needed to be implemented to maintain connection across the wireless channel. Chapter 4 will cover the simulated and measured results of the implant systems that are covered in chapters 2 and 3. Finally, chapter 5 will conclude the work with a summary of the results and discussions of future work that can be done on comparable systems.

1.1   Wireless Near-Field Power Systems

Through the history of development of IMDs, the need for transmission of wireless energy to power the implant, typically referred to as wireless power transfer (WPT), has become a main staple in most implants [7]. Wireless power has been a topic of interest even outside of the biomedical field since Nikola Tesla's experiments for worldwide wireless power distribution in the late 19th to early 20th century [8]. The type of operation for wireless power networks can be broken down into three distinct regions: the reactive near-field region, the radiating near-field or Fresnel region, and the far-field or Fraunhofer region [9]. Far-field transmission is suitable for a variety of uses, typically either low-power sensor networks where efficiency is not a concern and the entire network could be safely illuminated with radiation to supply low amounts of power to all receivers in the field, or in military or space applications, where both the efficiency and cost hits are necessary for the application space. For most applications, where both higher power transfer and power transfer efficiency (PTE) become the driving force in the design, the transmission radius must be reduced into the near-field or Fresnel region. While this limits the physical radius of operation of systems, it greatly improves both operating efficiency of the system and safety, as the distance between receiver and transmitter is typically on the order of a wavelength or less, and

radiated power outside that zone is considerably lower and thus well outside specific absorption rate (SAR) limits as indicated by the IEEE [10]. By definition the three wireless regions are defined by:

$$
\begin{aligned}
Near-Field: & \quad R < 0.62\sqrt{D^3/\lambda} \\
Fresnel: & \quad 0.62\sqrt{D^3/\lambda} < R < 2D^2/\lambda \\
Fraunhofer: & \quad R > 2D^2/\lambda
\end{aligned}
\tag{1.1}
$$

Where R is the distance from the antenna, D is the largest dimension of the antenna, and λ is the wavelength of the electromagnetic wave [9]. Depending upon application, research into WPT based technologies are split into far-field radiation systems [11–14] and near-field systems [15–18]. In the near-field the magnetic field dominates inductive coupling between close proximity antennas, which greatly increases the coupling, mutual inductance, and wireless power transfer between a matched coil pair. This has made near-field magnetic coupling the go to method for wireless power transfer for high efficiency systems. A general model for a near-field WPT system for DC delivery in an implantable system is depicted in figure 1.1. A inductor coil pair is matched to impedance transformation networks such that the ratio of the radiation resistance for each coil is maximized. This occurs when the input matching network's impedance is designed to be the complex conjugate of each inductor's impedance at the desired resonance frequency. Examples of wireless power systems utilizing the near-field magnetic field strength for high efficiency WPT are commonly seen in the biomedical application space [19–24].

For a printed circuit board loop antenna, the self-inductance of a single loop antenna coil can be calculated by the equation:

$$
L_{self}(R, w) = \mu R[ln(\frac{16R}{w}) - 2]
\tag{1.2}
$$

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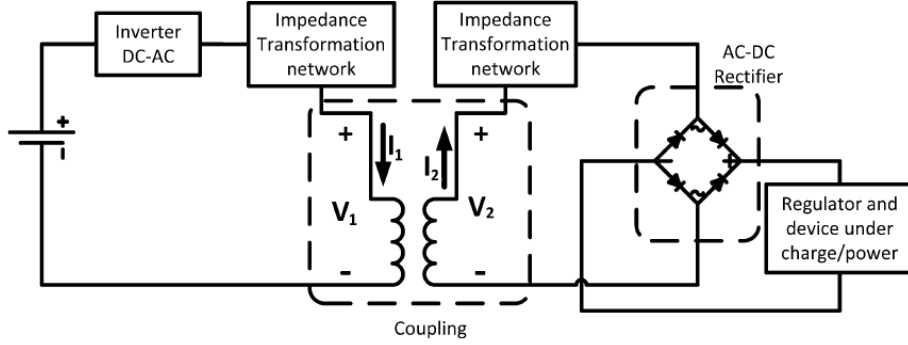
Figure 1.1: Standard WPT Model for Wireless Systems

Where R is the radius of the loop, μ is the magnetic permeability of the surrounding medium, and w is the diameter of the wire, assuming a circular cross section [25]. For an N turn loop, the self-inductance is scaled by a factor of N. When two coils are placed within close proximity, the mutual inductance for the coil pair in the near field can be calculated by the Neumann formula to be:

$$M = \frac{\mu}{4\pi} \oint \oint \frac{dI_1 \cdot dI_2}{R} \tag{1.3}$$

Which involves the double line integral of both the magnetic fields generated by the current in L_1 and the field generated by the current in L_2 [26]. Solving this integral two circular inductors, the mutual inductance between 2 coils in a link can written as functions of the effective spiral radii and number of turns of each spiral, and the separation radius:

$$M_{12}(R_1, n_1, R_2, n_2, d_{12}) = \frac{\pi \mu_o n_1 R_1^2 n_2 R_2^2}{2\sqrt{(R_1^2 + d_{12}^2)^3}} \tag{1.4}$$

Giving mutual inductance dependence and therefore coil coupling on coil separation as $\frac{1}{d^{\frac{3}{2}}}$. The coupling coefficient, k, can be written as a function of the coil inductances and mutual inductance, and the quality factor, Q, of an inductor can be expressed as a function of the coil inductance and internal resistance:

$$k_{12} = \frac{M_{12}}{\sqrt{L_1 L_2}} \qquad (1.5)$$

$$Q = \frac{\omega L}{R} \qquad (1.6)$$

Algebraically combining equations for k, Q and solving the 2-port RLC equivalent for the near-field wireless power transfer, we can determine the theoretical peak efficiency of the link without load to be:

$$\eta_{max} = \frac{k_{12}^2 Q_1 Q_2}{(1 + \sqrt{1 + k_{12}^2 Q_1 Q_2})^2} \qquad (1.7)$$

Now considering loads, At resonance for a near-field coil pair, the power delivered to a load attached to the receiver can be calculated to be:

$$P_{load} = \frac{V_{in}^2 \omega^2 M^2 R_L}{(R_1(R_2 + R_L)^2 + \omega^2 M^2)^2} \qquad (1.8)$$

Where R_1, R_2, R_L, V_{in}, and ω are the parasitic coil resistances, the resistance of the load being driven at the output of the receiver coil, the input voltage to the transmitter coil, and the frequency of operation respectively. From this equation, we see that the output power is a direct function of the input power at the TX, and will increase with mutual inductance as a function of the driven load. The power transmission efficiency for a driven load can be then written as:

$$\eta_{load} = \frac{\omega^2 M^2 R_L}{R_1(R_2 + R_L)^2 + \omega^2 M^2(R_2 + R_L)} \qquad (1.9)$$

In general this means the PTE of a wireless link increases as the series resistance of the transmitter and receiver coils are minimized. Using these equations, the WPT can be maximized by designing inductors L_1, and L_2 to have low parasitic resistance, high self and mutual inductance, and high quality factors [27, 28].

1.1.1 WPT in Biological Systems

For implantable systems, the use of near-field inductive links has become the standard technique for wireless power transfer [29–33]. Biological systems are unique transmission mediums and may, in general, be described as a fairly dense, lossy, dielectric that presents difficult challenges to maintain functionality without harming the biological system in which the system is implanted. In order to properly simulate expected electromagnetic losses in in-vivo systems, living tissue may be modeled as a planar set of layered homogenous boundaries with the appropriate permittivities and conductivities [7].

The dielectric properties of tissue result in high power absorption, particularly in terms of the electric field, making far-field communications extremely difficult, and requiring near-field inductive links [32, 34]. Luckily for magnetic coupling, the magnetic permeability in a majority of tissues is close to 1, causing the magnetic permeability to approach μ_o, the permeability in free space, favoring inductive links for both data and power transmission in implants even more [35]. Simulations highlighting this stark difference in energy radiation between electric and magnetic fields were performed by [32] can be seen in figure 1.2.

(a) Electric Field Propagation

(b) Magnetic Field Propagation
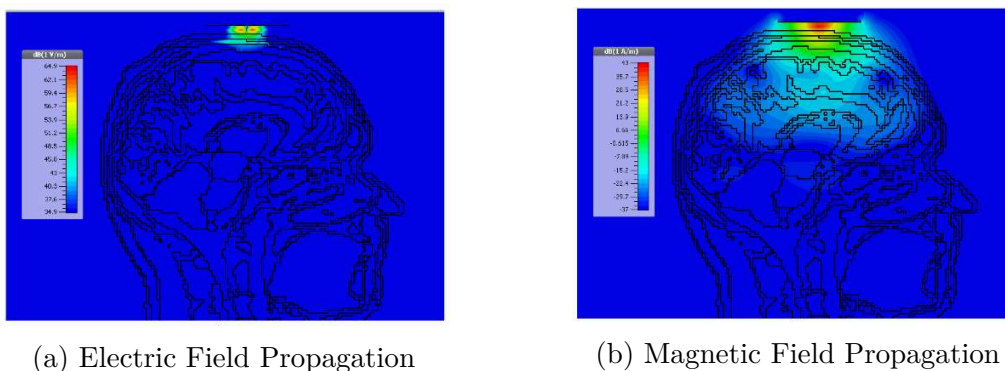
Figure 1.2: Near-field E and H penetration in a human head model

Temperature considerations are also critical for WPT in tissues, as the tissue

absorbs a significant amount of energy in radiated electromagnetic fields which is quantified as the specific absorption rate (SAR). Mathmatically SAR can be expressed as:

$$SAR = \frac{\sigma}{2\rho} \mid E \mid^2 \tag{1.10}$$

Which shows a quadratic relationship of SAR to the generated electric field [36]. In general the magnetic field in tissues are approximately equal to the equivalent field in air, since the magnetic permeability of tissues in general is close to one. Therefore energy focused into electromagnetic fields in tissue will primarily be delivered by the magnetic component, why the loss and heating components will be dominated by the electric field. Any tissue heating, particularly in brain tissue, causes damage to living cells, which places extra emphasis on power transfer efficiency to maximized as much as possible in a biological environment for implants.

1.2 Wireless Communications Links

For near-field data communications, emphasis on wireless power transfer is not as important as for near-field power links, with a large emphasis placed on signal bandwidth for increased data rate. From an antenna standpoint, wider bandwidths actually occur from a lower quality factor, meaning antenna layout needs to be adjusted to increase coupling and bandwidth at the cost of power delivery and efficiency. This section will cover the encoding techniques commonly used in implant technologies and in wireless communications in general, and will cover the primary data recovery technique on the receiver side for noisy channels, equalization.

1.2.1 Encoding Techniques

For wireless data transmission, a carrier signal is modulated in order to encode data onto a higher frequency system. In the near-field, the primary mode of energy coupling is still the magnetic field as was the case for WPT. The oldest standard in near-field coupling is the radio-frequency ID tag (RFID) which was invented in the 1940s [37], where data is measured by reflected power from a receiver coil in the presence of a transmitter. RFID was limited to 1-directional communications however, so various bi-directional near-field communications (NFC) systems were developed. The most common modulation techniques used for near-field magnetic systems include amplitude modulation methods such amplitude-shift-keying (ASK) and on-off keying (OOK), load-shift-keying (LSK), and cyclic on-off-keying (COOK). In each of these amplitude modulation methods, the magnitude of magnetic coupling occurring in the transmitting antenna is increased or decreased which can be demodulated on the receiver side using circuitry.

Frequency modulation encoding techniques include frequency-shift-keying (FSK), phase-shift-keying (PSK), passive-phase-shift-keying (PSSK), and for extremely high data rate communications, impulse radio-ultra wideband (IR-UWB) encoding is used. Frequency modulation techniques modify the phase relationship of a carrier frequency, while maintaining relatively even magnitude over time, and the binary decisions sent by the transmitter can be recovered from the frequency shifts using demodulation circuitry on the receiver, typically in the form of in-phase and quadrature (IQ) demodulation circuitry [38–42].

1.2.2 Load Shift Keying

For this work, the primary encoding technique employed is LSK. For a fully wireless link where both power and data are supplied, a 4-coil link (figure 1.3) is often created,
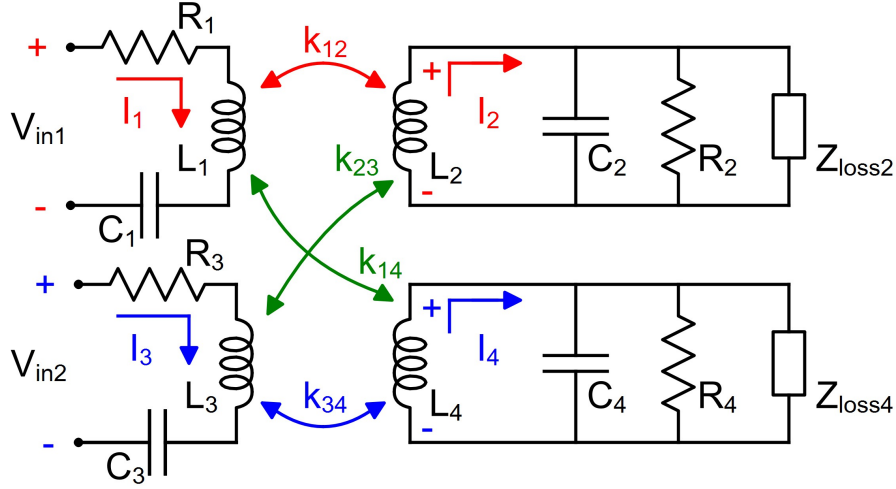
Figure 1.3: 4-Coil Model for simultaneous power and data transfer.

with one 2-coil pair (coils 1 and 2) employed for the wireless power link, and the other 2-coil pair (coils 3 and 4) employed for the data communications link. By tuning the power coil pairs to have a sufficiently different resonance frequency than the data coils, the cross coupling terms, k_{14} and k_{23} can be ignored. Typically modeled into the lumped loss impedance calculated for the wireless power transfer equations is the reflective impedance contribution from other coils in the link, Zr. This reflective impedance comes from the backscattered return path from the transmitter coil to the receiver coil and by definition can be modeled as, where the data coils are now coils 1 and 2:

$$Z_r = \frac{(\omega M_{12})^2}{Z_2} \tag{1.11}$$

Which has proportionality to the square of the mutual inductance. This means that the backscattered amplitude of an LSK signal falls off as a function of the separation radius cubed! For near-field links, which typically only operate at separation distances of 1 to 2.5 times the largest geometric feature on a transmitting inductor [43], this means the effective communication radius on an LSK link will likely fall

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below the outer diameter of the transmitting coil.

Adding the reflective impedance in the 4-port circuit depicted in 1.3, circuit analysis, and working under the assumption the coupling coefficients between the power coils and the data coils are not considered to be significant since the power coils are tuned for a different resonance, the effective 2-port network for the LSK coil pair can be changed into the form of figure 1.4. Algebraically, we can determine the impedance on the receiver side, Z_2 to be:
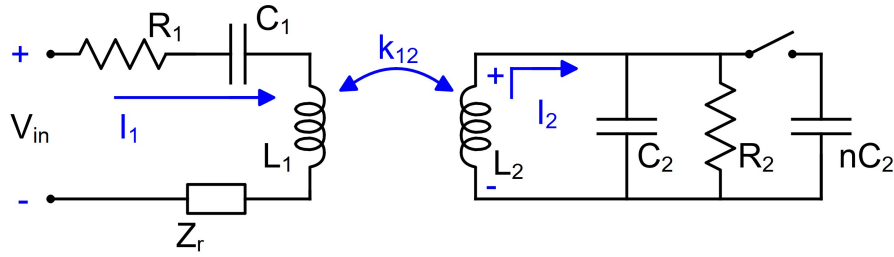
Figure 1.4: 2-Coil Model including Reflective impedance for LSK Encoding

$$Z_2 = j\omega L_2 + (R_2 \mid\mid C_2) \tag{1.12}$$

Using voltage divsion, the voltage across the transmitting inductor, V_{L1}), is :

$$V_{L1} = (\frac{j\omega L_1}{R_1 + Z_r + j(\omega L_1 - \frac{1}{\omega C_1})})V_{in} \tag{1.13}$$

Mathematically at resonance the conditions:

$$j(\omega L_1 - \frac{1}{\omega C_1}) = 0 = j(\omega L_2 - \frac{\omega C_2 R_2^2}{1 + \omega^2 C_2 R_2^2}) \tag{1.14}$$

are satisfied. Using these resonance conditions and equations for $Z2$, Zr, yields an expression at resonance for the ratio of the input voltage to the transmitter voltage in terms of the coupling coefficient and quality factors of the coils:

$$\frac{V_{in}}{V_{L1}(\omega = \omega_o)} = -j(\frac{1}{Q_1} + \frac{k^2}{Q_2}) \qquad (1.15)$$

When the LSK enabled, the switch is closed so the effective parallel capacitance increases from C_2 to $C_2' = C_2 + nC_2$. Adding this parallel capacitance to the network and rederiving the voltage ratio yields:

$$\frac{V_{in}}{V_{L1}(\omega = \omega_o)} = -j(\frac{1}{Q_1} + \frac{k^2}{Q_2}) + k^2 n \qquad (1.16)$$

Meaning the resonance shift in the receiver from load-shift-keying causes an increase in the real impedance as seen by the transmitter, which causes an extremely small dip in the output power of the transmitter power amplifier when the LSK switch is opened or closed.

1.2.3 Intersymbol Interference and Signal Equalization

As in all wireless communications systems, infinite bandwidth would be required to fully received a perfect binary waveform across a wireless medium. In physical systems, bandwidth is finite, meaning sent binary levels will be both decayed and spread out in the time domain to the point that one symbol's time response will bleed into the next and possibly multiple consecutive symbols. This bleeding effect is referred to as intersymbol interference (ISI). Figure 1.5 depicts typical ISI in a binary communication system [44].

Mathematically the original binary input waveform transmitted, $\omega_{in}(t)$, can be written as:

$$\omega_{in}(t) = \sum_n a_n h(t - nT_s) \qquad (1.17)$$

Where a_n Refers to the valid amplitude levels for different transmitted data, $h(t)$ is the unit impulse response, and $\delta(t - nT_s)$ is a unit dirac delta function with a
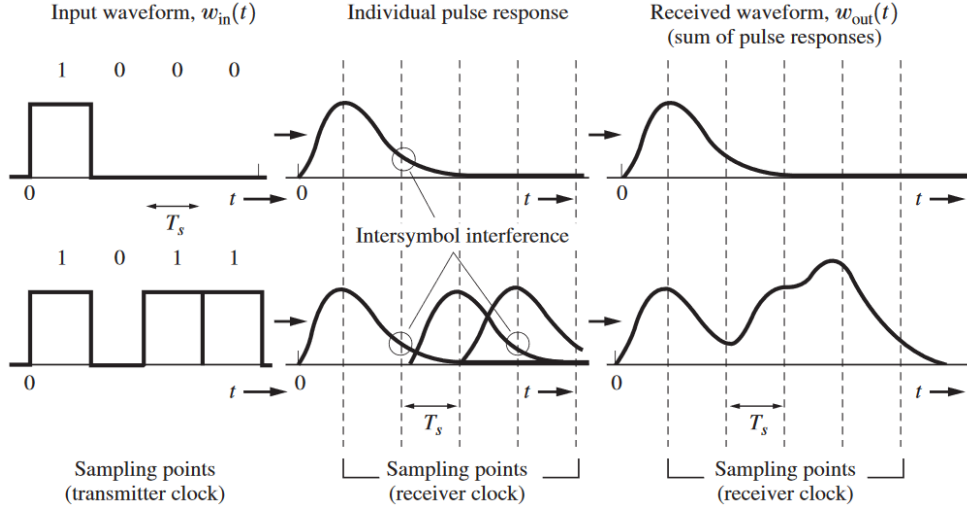
Figure 1.5: Example of ISI on received bianry pulses in a communication system

time width of $1/T_s$. For a binary phase-shift-key sequence the valid values of a_n are 1 and -1. This binary waveform gets corrupted during transmission by the channel's unknown transfer function $h_e(t)$ yielding the output corrupted waveform mathematically as:

$$\omega_{out}(t) = \sum_n a_n h_e(t - nT_s) \tag{1.18}$$

The corruption of this signal is identified as the ISI, and must be removed in order to create an accurate wireless data link. One of the primary methods of removing ISI from a signal is equalization. One form, linear channel equalization, involves the use of a linear filter, called the equalization filter, which narrows the band of a distorted digital waveform thus reducing the effects of ISI. This linear filter has a set number of taps, each with different weights corresponding to the equivalent coefficients of the filter's transfer function. A normal linear filter FIR topology is depicted in figure 1.6 [45].

Since the actual wireless channel can be unknown, and can change from causes such as interference or the multi-path problem, it becomes important for the equalizer
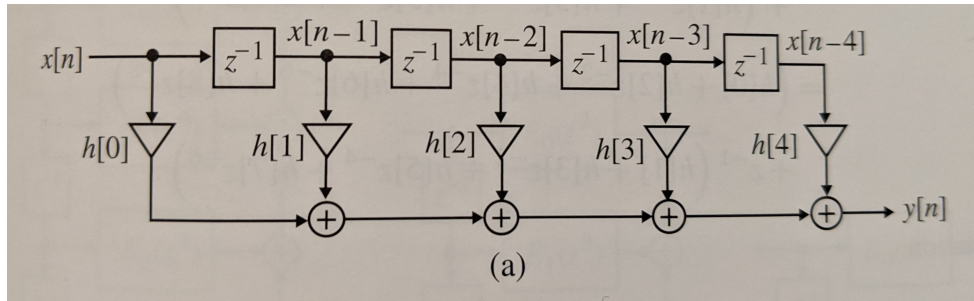
Figure 1.6: Direct form linear FIR filter with 4-taps

to be able to adapt to the channel through the use on an adaptive filter. By adapting the weights of the linear FIR filter using a feedback algorithm by defining an error function, the linear filter is transformed into a linear equalizer. The structure of a linear equalizer with adaptive feedback takes the structure depicted in figure 1.7 [46]. A linear equalizer is specified to have N taps, with M taps per symbol decision
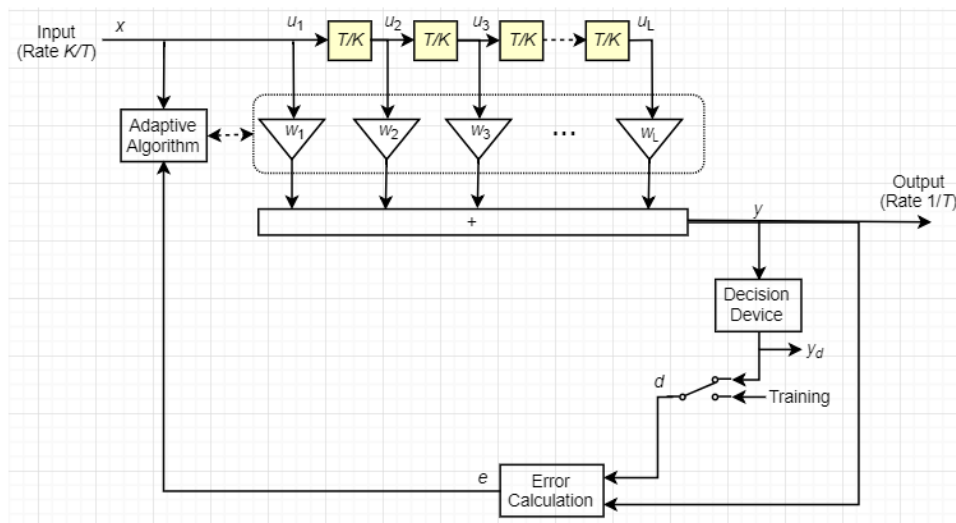
Figure 1.7: Structure of a Linear Equalizer

To determine the error of the equalization channel, desired amplitude and phase responses for respective binary values are predetermined in Hilbert space with a time width corresponding to a single symbol. Error is considered to be minimized, when the value of the hilbert-space magnitudes matches the input waveform after going through the equalization filter. Those desired points can be plotted on a quadrature

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graph called the channels desired constellation. Two of the most commonly used hilbert-space data constellations are depicted in figure 1.8 [47].
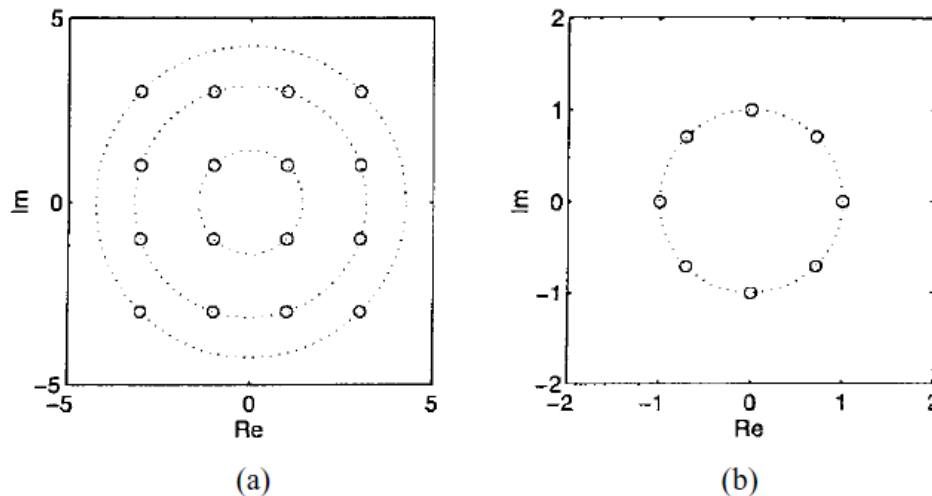
Figure 1.8: 16-QAM Constellation with a variable Modulus (a) and 8-PSK with Constant Modulus (b)

The method at which the filter weights is tuned generally referred to as the used equalization algorithm. The most common adaptive equalization algorithms are the Least Means Square (LMS), Recursive Least Squares (RLS), and the Constant Modulus Algorithm (CMA). For the LMS and RLS adaptive algorithms, the filter weights for all taps start with a normalized value of one and by recursive application of a training sequence, where the desired output is already known to the equalizer. For the CMA algorithm, no training sequence is necessary, since the filter goal is to create a constant magnitude with only phase changes for every symbol decision. Since a training sequence is not necessary, the CMA algorithm is the only application error function that is compatible with the implant transceiver [46–48].

The ultimate quality measure in optical communication links is the bit error ratio (BER). However, a direct experimental BER determination can be done only as long as the link is out of service (if not a hard-decision forward error correction (FEC) is able to report errors), because a known data sequence has to be transmitted, and it

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consumes a significant amount of time if the BER is small.

The BER of a signal is a direct function of the ratio of the energy-per-bit transmitted in the signal to the noise level of the received signal, known as E_b/N_o. For different designed hilbert-space constellations, the theoretical BER as a function of E_b/N_o is depicted in figure 1.9.
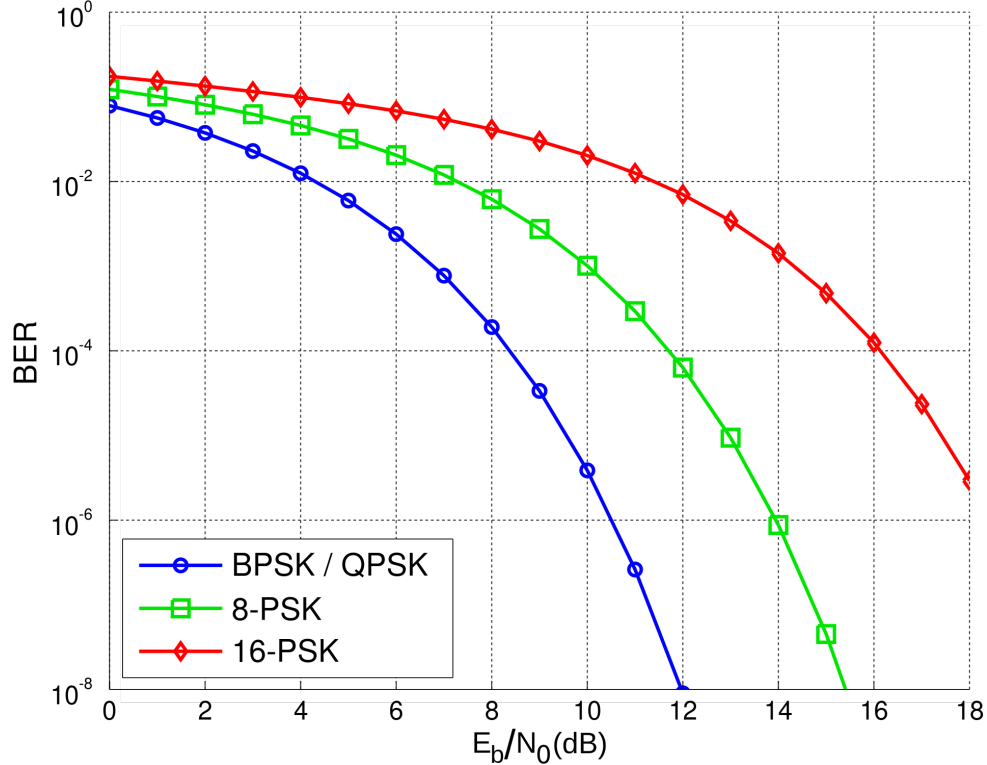
Figure 1.9: Theoretical BER vs E_b/N_0 for common constellations

Plotting at the graph of the hilbert-space function of binary-encoded constellation data over the sample period T, a pattern forms known as the eye diagram (figure 1.10). Based on both the height and width of this eye, a graph known as a bathtub curve can be generated, the spacing of which can be used to estimate the BER of an equalized signal depending upon both the amplitude and phase of the sample point in the periodic time in hilbert space. By choosing the center of the eye both in phase jitter, and in noise amplitude, BER of a wireless link can be minimized [49–51].
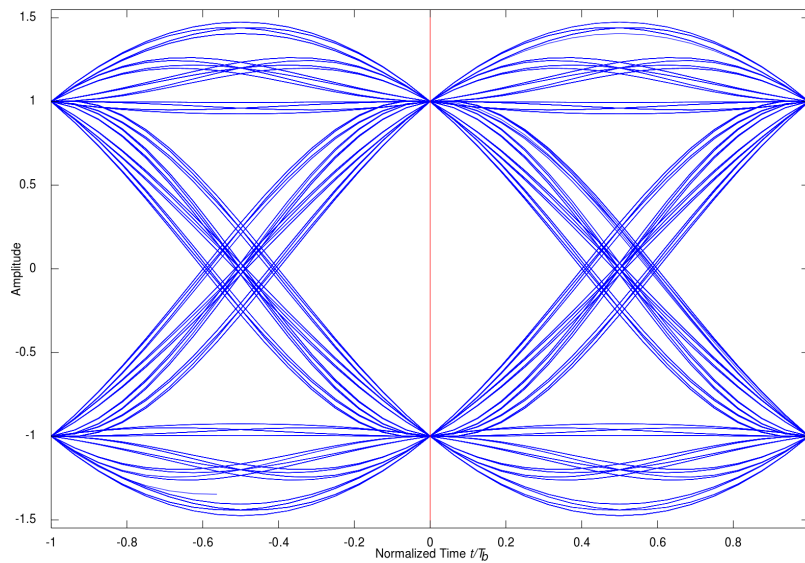
Figure 1.10: Ideeal Eye Diagram for PSK

1.3 Implantable CMOS Devices

Along with the development and advancement of microelectronics, modern IMDs have been developed to assist in treatment of a plethora of diseases for both monitoring and treatment of patients. Because of size constraints and power limitations, a variety of different power systems have been developed, typically employed using small short-term batteries that require regular charging to maintain functionality of the implant or a physical tether outside of the body that supplies both energy and data to and from the implantable system. Specifically in this thesis, the primary discussion of IMDs will pertain to neural interface systems. As opposed to larger IMD systems such as cochlear implants, pace makers, or heart monitors where a large foreign object can be easily stitched in-between tissue layers without causing a strong immune response, neural interface systems must take a much smaller form factor so as not to displace a large amount of tissue and disrupt neural behavior. The exact volume limit that an IMD is aiming for is therefore extremely dependent upon the organism in which it

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is being implanted. For our application, we have designed a transceiver system that is compatible with neural recording systems for laboratory mice. Since the mouse brain's dimensions are on the order of a couple centimeters as opposed to a primate brain which is on the order of 10s of centimeters, the volumetric displacement must be limited to far less than $1mm^3$. In addition, a shank-based approach with a several millimeter long and approximately 100 micron wide electrode interface will allow for deep brain recording in the targeted region of the mouse brain.

Most current neural recording systems utilize passive silicon shanks in which only electrodes and wires exist on the shank itself with all the electronics external. Recent advances in nanofabrication techniques have allowed these systems to scale to up to 256 recording sites per shank. More recently, active CMOS probes have been developed that incorporate the electronics on the shank itself, allowing even higher channel counts [52–54]. These CMOS neural probes, however, require a physical tether to a power source and data acquisition system requiring wiring through the skull and skin of the animal and mechanical fixation of the probe to the skull, resulting in additional damage and inflammation as the brain moves relative to the probe. A picture of the state-of-the-art neuropixel system [55] highlights how large and bulky these tethers can be.

To remove the requirement of a bulky tether, the design addition of an integrated transceiver on the ASIC itself is proposed. This transceiver will be fully wireless and is designed to be completely implanted in the brain of the mouse itself for recording, mechanically floating with the brain. Figure 1.12, depicts the intended final application space of this thesis, a small wireless implant system-on-chip, with a shank inserted deeply into the tissue of a mouse brain with both power delivery and data telemetry supplied by an external reader system that communicates with the chip via near-field RF communications. In addition, in order to lessen the immune response of the brain tissue, the chip will be thinned While other systems have used wireless

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Figure 1.11: Commercial Neuropixel System

power and data telemetry for biomedical implants, these efforts have all used multiple components, specifically large off-chip antennas, increasing the required volume of the implant considerably [1–3]. Since the system proposed decreases the entire package volume considerably, the dedicated area for a front end neural interface is limited compared to commercial systems, and this trade-off will be seen in the number of total sites that can be integrated on a single system, the speed and accuracy of integrated data converters, and the overall range of tunable controls for an amplification system.

Compared to other wireless implants, neural systems require a much higher data bandwidth than cochlear or cardiac devices, as the neural signal content covers both a much higher bandwidth, and the density of sites to be recorded from is significantly higher. To address this, while still providing a fully wireless system, the proposed system will utilize the highest data rate possible communications scheme while still maintaining a very small volumetric form factor. The primary consequence of higher data rates means significantly higher operational bandwidth than what might be seen

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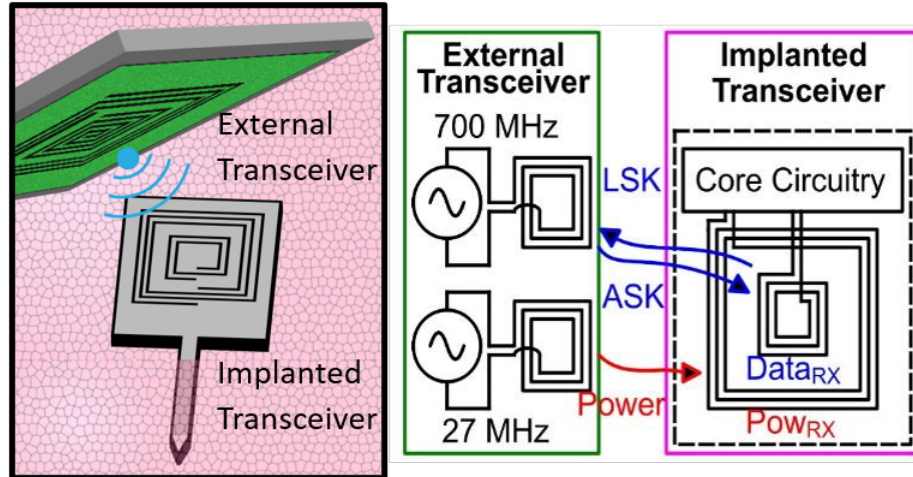
Figure 1.12: Proposed System Application

in current medical devices. While a wireless band is already dedicated for medical implant communications (known currently as the MedRadio bands) in the low 400MHz range, the data bandwidth of these bands is limited to $300kHz$ [56–58]. Neural signals cannot be properly captured at this small a data bandwidth, as the primary frequency content of high frequency potentials can be as high as 10-20kHz. As such, current neural recording systems require data bandwidths of 10-30kS/s per site! With only a 300kHz data band to work with, that would limit the total number of concurrent sampled sites to approximately 10, and that's assuming a multi-bit sample can be sent in a single cycle. To achieve higher data rates, therefore, the use of both a higher and non-standard frequency carrier is required, in addition to the use of a custom data protocol that will maximize data communication rate.

Chapter 2

Design of Implantable ASIC

2.1   Design Specifications and Goals

In the design of this ASIC implant, there are three distinct sub-blocks each with their own set of requirements to meet the desired goals of the implant system. These three blocks are the physical antennas for both power and data telemetry, the data-modulation and demodulation systems, power harvesting circuitry, including clock-and-data recovery, and the biological interface circuitry including front end amplifiers and on-chip ADC. In parallel, each of these sub-blocks was also designed to operate after being thinned post-fabrication from the foundry.

A system block of the implantable IC is depicted in figure 2.1. The overarching ASIC design goals were to be able to be fully wirelessly power-able while remaining under the Specific Absorption Rate (SAR) limit specified by the IEEE guidelines

for limited exposure for medical implants and for the transceiver to provide a high enough data-rate to be able to concurrently sample all sites in the neural amplification system at a high enough sample rate to capture the relevant data bandwidths for neural signals.
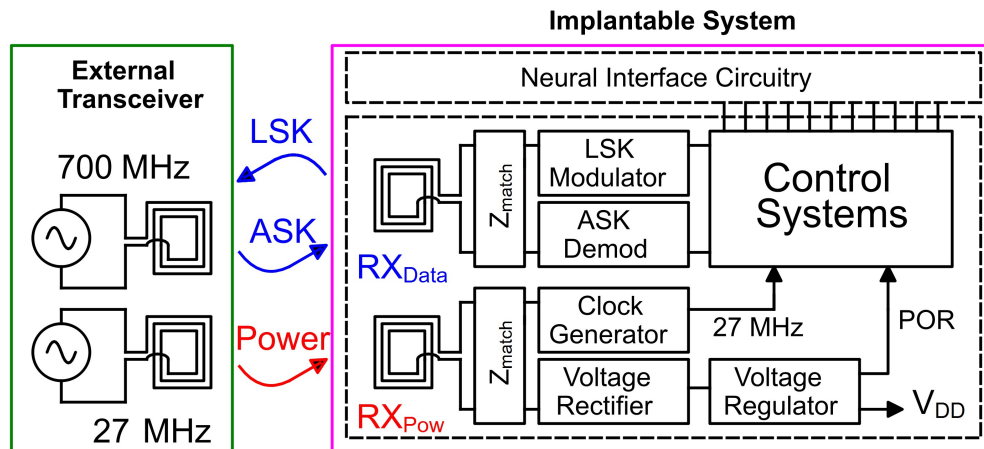
Figure 2.1: Implant IC System Block

The final IC layout with each major block labeled is depicted in figure 2.2. The shank with bio-interface circuitry measures $3.25mm$ by $70\mu m$ wide, with $60\mu m$ of metal exclude for post-processing of the shank. The antenna blocks with power and data coils measures $2mm$ by $2mm$ with all remaining circuitry encompassed in a $0.5mm$ by $2mm$ block. A majority of the remaining circuitry's area is taken up by arrays of decoupling capacitors to maintain as steady a DC voltage to power the ASIC as possible. The simulated power required to fully power the implant is 2.7mW for the transceiver circuitry, and 1.5mW for the neural interface system and ADC. Including insertion loss, this requires 10.4mW of total WPT from reader to implant to achieve full wireless functionality.
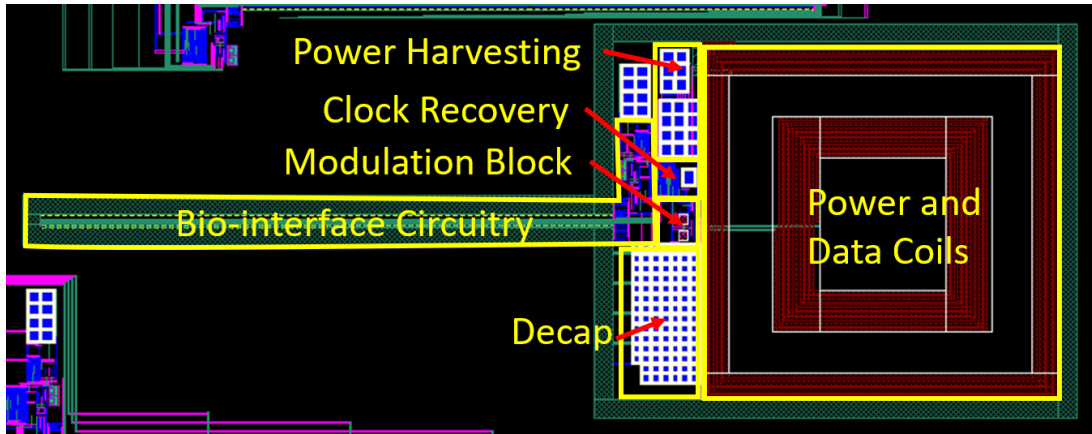
Figure 2.2: Physical Layout of Implantable ASIC

2.2 Near-field Four Coil Design

For the on-chip antennas, the first design decision was which type of wireless link to employ, with the most common link types for implant systems described in detail in Chapter 1. Also, the antennas were designed considering both the specific-absorption-rate (SAR) limits as specified for localized fields by the IEEE standards. In order to meet these absorption rates, assuming the overall PTE would be on the order of $1-3\%$ and at least 50% of the energy received by the power coils could be harvested, a total power budget of $1W$ was given at the reader transmitter, leaving $10mW$ of expected received power in the implant power coil, resulting a total of $5mW$ remaining for all the circuitry in both the transceiver and the neural amplifier system.

The downsides of using integrated inductors for transmission comes with the problem of electrical smallness. As you can see from plots of the current distributions given in figure 2.3, the transmission efficiency of IC side radiation is significantly lower than for large coils that can be fabricated on the PCB side of the system. By definition, a radiating antenna becomes electrically small when the area of the entire antenna fits inside a sphere of radius $a = \lambda/(2\pi)$ [59–63]. The effects of this electrical smallness can be observed in figure 2.3, where the energy radiated by the TX and absorbed by

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the RX is great when the PCB side is transmitting and the implant side is absorbing (2.3a), and the energy absorbed by the RX is very small when the implant side is the radiator (2.3b).

For power transmission, the implant is simply a passive receiver, so the concept of electrical smallness is not a problem since it will never actually transmit power at $27MHz$, the power transfer efficiency just takes a hit since the coils cannot be perfectly matched. For data transmission, however, this presents a challenge which greatly limits the effective range for data transmission. Also, since we are only able to use passive modulation to save power in the implant design, the data coil's backscattered matching is what is measured for the data uplink, meaning we are taking the hit for RF losses from the TX/RX separation twice. To change the backscattered matching we shift the load impedance that is attached in parallel to the inductive coil which modifies the resonance frequency of the data receiver coil. Since we are shifting the load of the coil, we call this type of modulation load shift keying (LSK). An example design from ADS where the resonance frequency of a receiver is shifting from being in tune with the RX at close to $800MHz$ (curves in black) to being completely out of tune at $< 200MHz$ (curves in blue) is depicted in figure 2.4. Without LSK enabled, the amount of power supplied by the TX side is actually effectively modulated to two separate binary states on the receiver side in terms of output power.
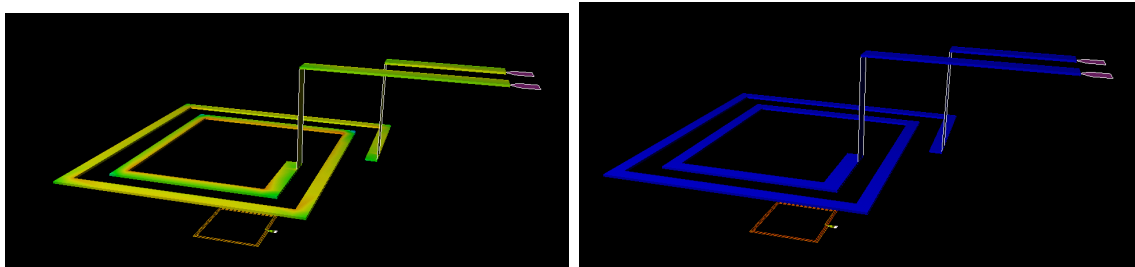
(a) EM Current Distribution with PCB side transmission

(b) EM Current Distribution with IC side transmission

Figure 2.3: IC side vs PCB side RF transmission
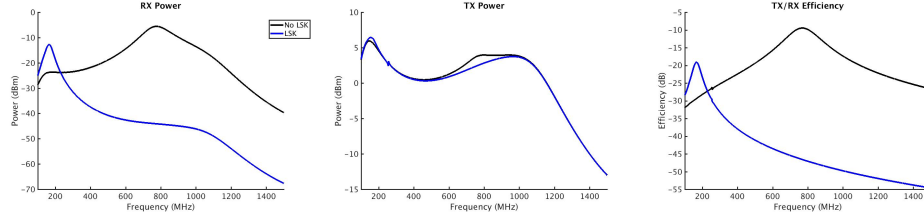
Figure 2.4: RX Power, TX Power, and TX/RX Efficiency with LSK modulation

For physical inductor size of the on-chip coils, the coil outer diameter was limited by the size limit of the implant while still being usable in the brain of a small mouse. Total implant volume was targeted to be less than $0.1mm^3$, which for assumed $20\mu m$ thickness, allowing for a total chip surface area of $5mm^2$. Budgeting 80% of surface area for the near-field inductors, yielded an outer radius of $2mm$ by $2mm$ for the power coil. For the near-field link being designed, we show in figure 2.5 that the amount of coupling between TX and RX increases with turn count as a function of N_2 where N is the number of turns in a loop inductor. Increasing the number of turns, however, also has the downside of increasing the resistive losses as a function of N, which at some point will both create too much heat loss and diminish the radiation efficiency of the coil. For our system, the optimal turn count was iteratively determined to be 5 for the power coil and 7 for the data coil.

For the cross sectional area of the antennas, the goal was to maximize the quality factor of the coils. The Q of the inductors is directly proportional to the coil inductance, and inversely proportional to the resistance per unit length of the coil. Therefore a maximal Q-factor will occur when the width, and height of the inductor is maximized, while the separation between loops is minimized, which increases L and decreases R. Unfortunately in integrated coils, the height is a set-value by the chosen technology ($4\mu m$ in 180nm SOI), and the minimum separation between metal shapes increases as wire width increases. For example, fabrication limitations limited metal trace widths to $50\mu m$, as long as spacing between traces exceeded $30\mu m$. If trace

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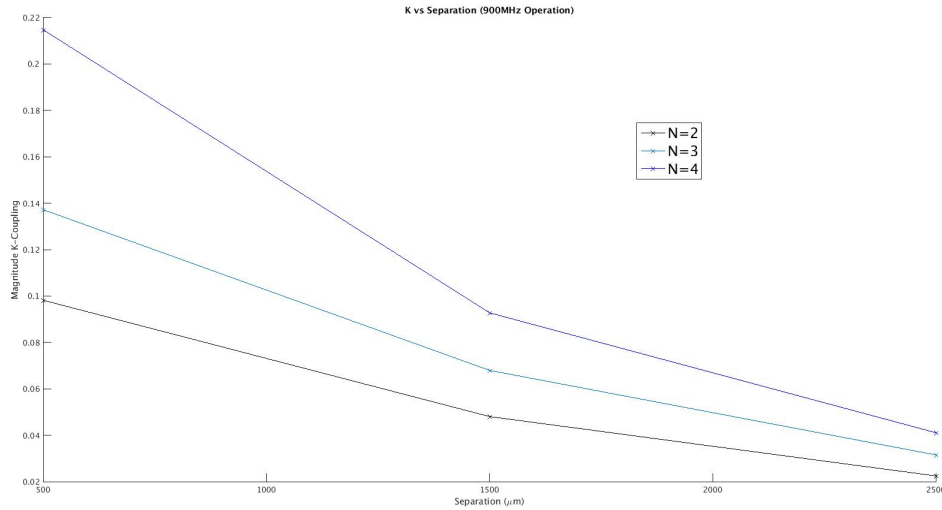
Figure 2.5: Coupling coefficient for power coils vs transceiver radius

widths were limited to $20\mu m$, spacing could be reduced to $10\mu m$, adding a series of non-allowed ratios between draw-length, trace width, and trace spacing for iterative simulation using an electromagnetic method of moments solver.

Taking these manufacturability limitations in mind, iterative analysis for the peak possible Q in the power coil showed peak PTE with an optimal trace width greater than $50\mu m$ with separation less than $30\mu m$, so the DRC limits were chosen as the power coil inductor parameters. For the data coil, the design process differed slightly, as the goal was not to maximize power transfer efficiency, but voltage coupling between the coils. Theory shows that a peak in coupling occurs at so by decreasing trace thickness and spacing to maximize draw length and Q-factor, with less importance placed on reducing resistive losses, the goal was able to reach a self-resonance frequency in the desired band of $600MHz - 800MHz$.

2.2.1 Power Systems Circuitry

With inductor parameters, and thus usable scattering parameters for an importable cadence model available, the next step was to design power harvesting circuitry to

convert the . For implantable devices, both passive and active rectifier circuit topologies have been created, with strengths and weakness of both designs [64–68]. For this implant, a passive voltage rectifier based on a voltage quadrupler circuit was implemented. The voltage qaudrupler topology used is depicted in figure 2.6 in the left most block. For this design the transistors M_1, M_2, M_3, and M_4 are all simply acting as diode connected FETs which only allow current to flow in one direction at the cost of a turn on voltage. When the AC input across the voltage quadrupler exceeds the diode-connected-FET threshold voltage, the system acts as a charge pump in both the positive and negative AC phases, effectively rectifying two times the positive AC input voltage at the output of M_2 and two times the negative AC voltage amplitude at the output of M_4. Setting the negative voltage to be the ground reference of the chip, and adjusting the magnitude of the input power signal to create 900mV on both the positive and negative phases, we yield a 1.8V DC voltage at the rectifier output. In order to reduce the 27MHz ripple on this rectified voltage, the value of the differential capacitors at the output of the passive rectifier are made large enough to limit DC ripple to less than 150mV, allowing 150mV of overhead for the regulator of the chip to create a steady 1.5V DC rail which is the suggested operating voltage for optimal performance of the 180nm SOI technology. The efficiency of this passive rectifier was simulated to be between $60 to 65\%$, or an overall insertion loss from antenna to available power of approximately $-4dB$.

To create the regulated $1.5V$ rail for the remaining chip circuitry, a low dropout regulator (LDO) was implemented with circuit topology depicted in the center of figure 2.6. A telescopic op-amp is driven by a bandgap reference set to 750mV in a non-converting gain configuration with a gain of 2. A large PFET, M_1 is placed at the output of this op-amp which acts as a current source for the regulated DC output. As long as the current average drawn by the chip never exceeds the RMS current in the power receiver coil, the LDO will be able to properly regulate. A function of the
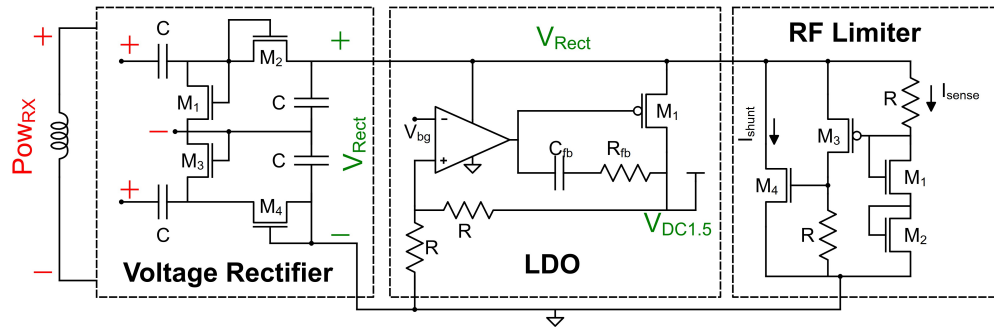
Figure 2.6: System Block for Rectification, Regulation, and RF Protection Circuitry

power supply rejection ratio, PSRR, of the designed LDO is depicted in figure 2.7.
Monte Carlo simulations for the PSRR show a minimum of 36dB at 50MHz, which
is twice the expected operating bandwidth of all signals on chip outside of the data
receiver carrier frequency.
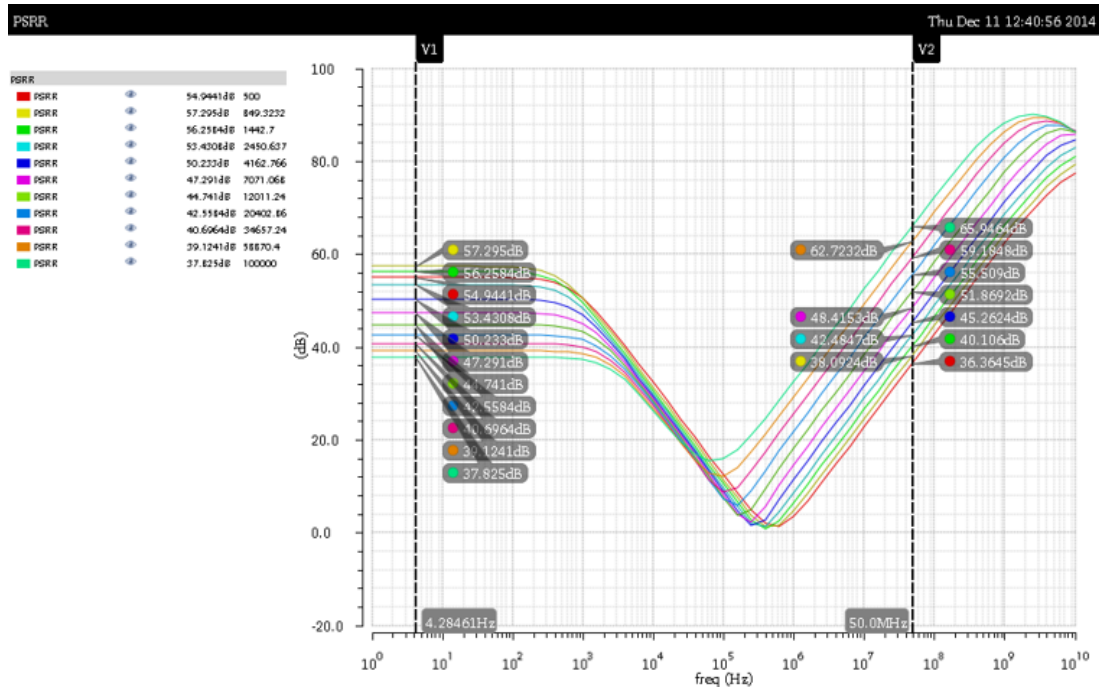
Figure 2.7: PSRR of LDO block

The final block in the power systems circuitry is the RF Limiter. The FETs used
in all subsystems outside of the rectifier and regulator blocks have a strict operating
voltage limit of $1.65V$ before permanent damage is done to the transistors. The

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bandgap reference in the LDO block, which is powered by the rectifier output, will exceed $0.8V$ in the rectifier output exceeds 1.95V, which will create a regulated LDO output that exceeds safe operating voltages for the internal circuitry. To protect the system from this, an RF limiter circuit was added in parallel to the voltage rectifier output as depicted in the rightmost circuit block of figure 2.6. In this block, a voltage sensing circuit composed of the series stack of a resistor, M_1, and M_2 generate a current called I_{sense}. When I_{sense} is small, M_3 is in cutoff and does not draw current, causing the voltage at the source to drop to zero, leaving M_4 also in cutoff. Ass the voltage output of the rectifier approaches $1.9V$, the current I_{sense} increases, creating a cascading effect of turning on M_3, which turns on M_4 creating a current shunt at the output of the voltage rectifier. This causes any excess RF energy being converted into DC power to be shunted to the implants ground reference. The RF limiter will only function up an input power level of 21.mW, however, by the time this limit is reached, the transistors in the rectification system will have already exceeded safe operating voltages and have already ceased to function. The RF limiter's primary function is to protect against unexpected rises in the transmitted power from the reader that might occur when programming the output power of the external transceiver.

2.3 Data Modulation Circuitry

In order to limit power usage and stay under SAR limits, the data modulation topologies for both uplink and downlink were chosen to be as low power as possible and passive in terms of modulation technique. For downlink, ASK modulation was chosen and for uplink, passive backscattering LSK modulation was chosen.

When powered on, the implant starts in a "blinking configuration" state. Since LSK transmission effectively shunts the received carrier signal to the no-amplitude condition to modulate a zero, only data uplink or downlink can occur at any given

time. While in the blinking state, the implant alternates between transmitting the chip's current configuration settings for eight downlink cycles and listening for an ASK response. While listening, the LSK modulation circuitry is disabled. The external data Tx tracks this blinking state and sends the configuration word in the listening phase. If one of 16 valid words (which act as input configuration gain for the biological interface circuitry) is received, the implant enters the data transmit state where it continuously sends digitized data. At this point the ASK demodulation circuitry is disabled to both save power, and to prevent the chip's configuration from changing during sampling. In order to reset the system and transmit a new input code, the system must be fully powered off by either disabling the power transmission signal, or by moving the implant out of both power and data range. Since the power transmission operation range is approximately 3-5 times longer in radius than the data link, the suggested method is to turn off the power signal. This will also have the bonus effect of preventing a false programming condition, that will be highlighted when discussing the modulation circuitry in detail. The waveform with the LSK enable and disabled on the chip-side is depicted in figure 2.8.

2.3.1 Clock Recovery

For higher power wireless systems, a local oscillator is typically used to create an on-chip clock signal. While the advantages of this include on-chip tunability of the clock signal, it comes at the heavy cost of requiring some type of phase-locked-loop (PLL) or delay-locked-loop (DLL) which can sync to the external system, adding high complexity and power requirements to the system [66, 69–71]. In this passive system, the power budget is limited to only 2.7mW for all of the transceiver circuitry, not allowing this circuitry overhead for an on-chip oscillation system.

The clock recovery circuitry used on the chip is depicted in figure 2.9. The positive
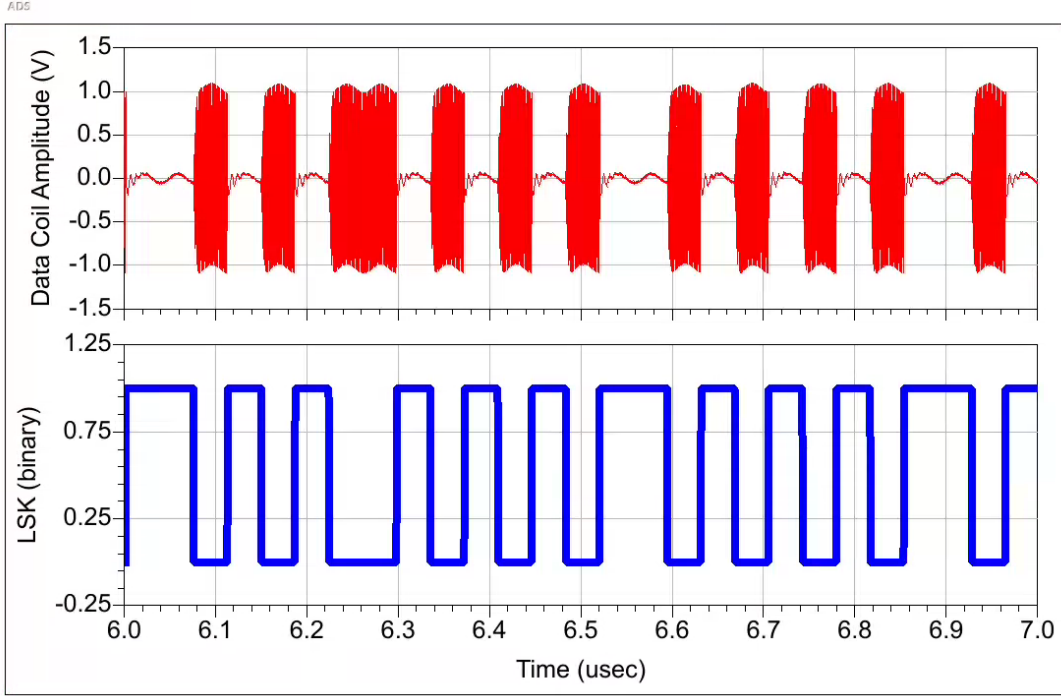
Figure 2.8: LSK Waveform on the Chip's Data Receiver

terminal of the power coil is connected to the input of the block which is AC coupled using a blocking MIM capacitor. This captures only the AC signal of the power coil, and ignores the DC value that has been set to the power coil in steady-state operation. This is then fed into an inverter that has a feedback resistance, which at no AC-input will cause both the input and output of the inverter to be set to $Vdd/2$, which for this technology is approximately 750 mV. The inverter then simply acts as a highly non-linear amplifier, amplifying the AC input from sinusoidal into a square wave with a switching time window close to the inverter time constant τ_{inv} which is approximately $50ps$ for the $180nm$ SOI process. To reduce glitching, this square waveform is fanned out to Schmitt triggers which distribute the recovered $27MHz$ clock to the control blocks of the chip. To prevent uneven loading on the positive and negative terminals of the power inductor, an unpowered replica of the MIM capacitor and inverter with resistive feedback is place on the negative terminal with closely matched wire lengths.
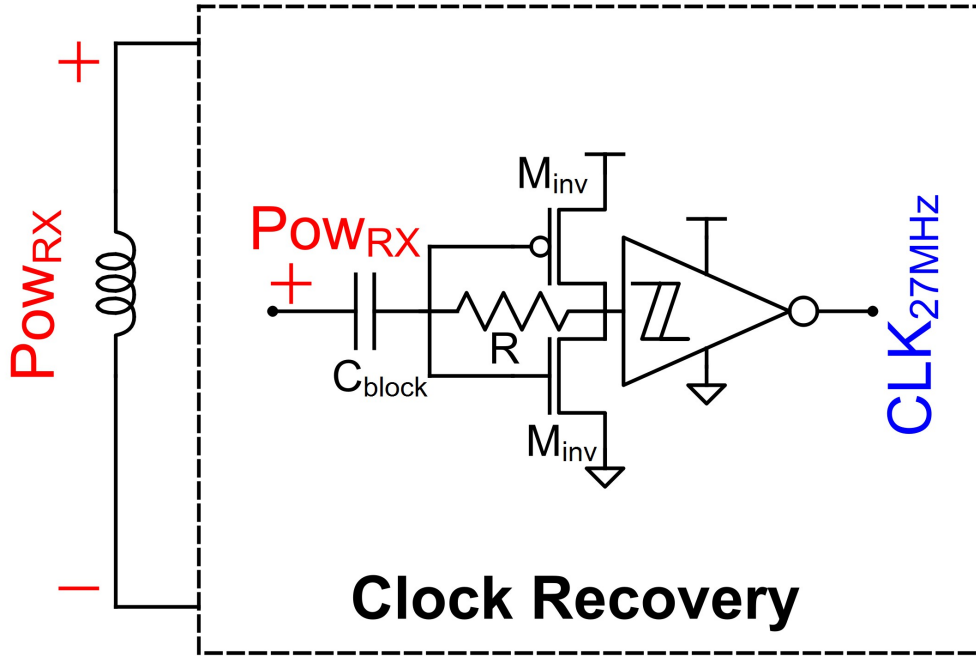
Figure 2.9: Clock Generator Circuitry

2.3.2 Data Modulation and Demodulation Circuitry

For data recovery, since the external reader is creating the power signal with a COTS PLL, the IC's clock frequency can be assumed to match the sent power signal, thus effectively phase-locking the on-chip clock to the external reader clock without the use of an on-chip PLL. For the passive LSK backscattering modulation, the circuit topology used can be seen in figure 2.10. For this block, the differential AC signal on the data receiver coil, RX_D is matched using a small MIM Capacitor, C_{match}, giving the parallel LC circuit a resonance frequency of:

$$\omega_o = \sqrt{L_{RX_{Data}} C_{match}} \tag{2.1}$$

Depending upon process corner, and the remaining bulk capacitance after thinning the silicon, this value is designed to range from $650 - 750 MHz$. A second larger detuning capacitor, C_{mod} can be added in parallel to C_{mod}. The desired modulated

data decision LSK is used to open and close pass gates, effectively changing the resonance frequency to:

$$\omega_o^{'} = \sqrt{L_{RX_{Data}}(C_{match} + C_{mod})} \qquad (2.2)$$

Where the value of C_{mod} is large enough to reduce the resonance frequency to far below $150Mhz$, which effectively shunts the received $700Mhz$ carrier signal to $0V$. The circuit topology for the ASK demodulation and LSK modulation systems are depicted in 2.10.
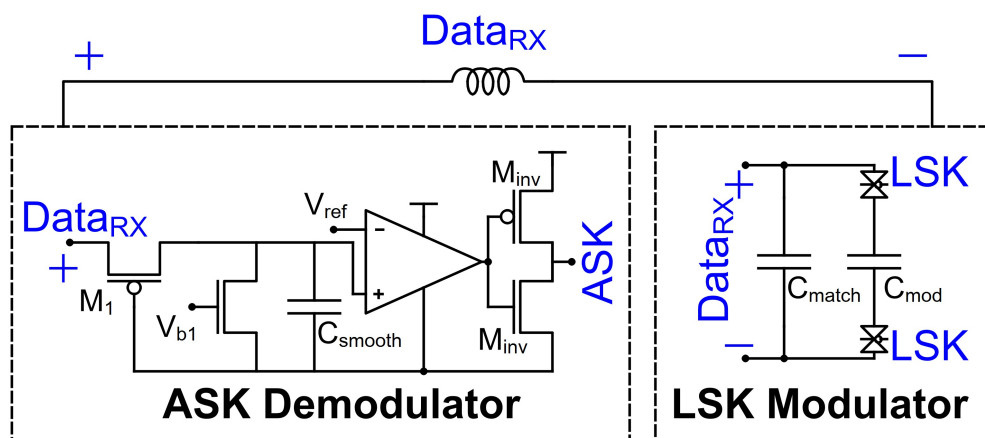
Figure 2.10: ASK Demodulation and LSK Modulation Circuitry

For the LSK circuitry, C_{match} and C_{mod} are implemented via $400fF$ and $10,000fF$ MIM capacitors, and the pass gates are implemented with $10\mu m$ width complementary gates. For the ASK circuitry (depicted on the left in figure 2.10), an envelope detector is implemented using the triode connected PFET M_1 and MoM capacitor C_{smooth}. This envelope level is compared to a bias voltage V_{ref} which will trigger an ASK value of 1 when the LSK level drops below the reference threshold. Since the time constant of this envelope detector is quite long, a shunting NFET biased by V_{b1} is placed in parallel to the envelope voltage that will attempt to pull down the envelope voltage quickly, allowing for a very fast reaction to a shift in data carrier

amplitude during ASK transmission. This shunting FET also serves a secondary purpose after programming, as the bias voltage is increase to always transmit a value '0' in the ASK, preventing accidental reprogramming during data uplink. Since the ASK detection occurs when the envelope drops below a threshold, it is also important that the data carrier frequency be switched on before the power carrier is turned on to prevent a false programming of '1111'. Since this state is the most likely accidental programming state, the '1111' state is also designed to be the minimum gain setting and most stable setting for the neural amplifier system.

The impedance load caused by the LSK circuitry and ASK demodulation system at $700MHz$ can be modeled by a parallel RC circuit with $C = 430fF$ and $R = 4.3k\Omega$ with the LSK disabled, and $C = 10.6pF$ and $R = 106k\Omega$ with the LSK enabled. To maintain equal loading the positive and negative terminals, an unpowered replica of the ASK Demodulator is placed on the negative terminal of the data coil.

2.4 Neural Interface Circuitry and Post Processing

The neural interface system is implemented with a multi-stage amplifier with time multiplexing and an 8 bit successive approximation register (SAR) ADC. A system level circuit block for the neural system is depicted in figure 2.11.

2.4.1 SAR ADC

To digitize analog input signals on the shank, an 8-bit successive-approximation-register (SAR) ADC was designed. The SAR-ADC has an asynchronous controller, providing all 8-bits in parallel in a single clock cycle. In order for the SAR data rate to match the 27MHz clock frequency, the SAR's clock was divided down by 8 for a
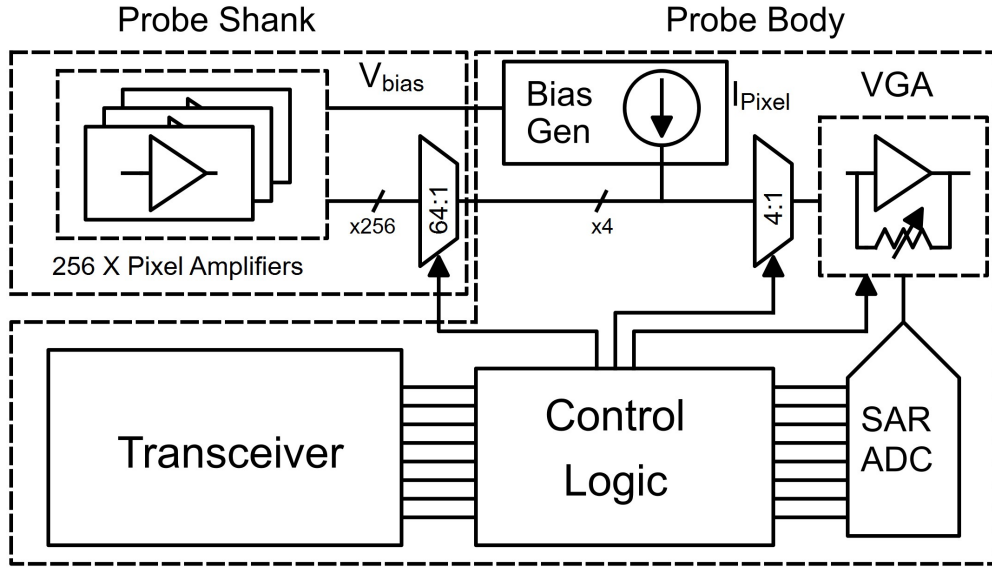
Figure 2.11: Neural Interface Circuitry and ADC System Block

designed sample rate of 3.375MS/s. The ADC runs continuously, with the previous 8-bit decision from the last clock cycle stored in a register block that is forwarded to the LSK modulator. The capacitor array for the ADC was designed using MIM capacitors, with a unit capacitance of $33fF$. In order to greatly decrease the overall capacitance of the capacitor array, a split-capacitor array was implemented with separate capacitor arrays for the upper and lower nibbles. The system block level schematic for the design SAR ADC is depicted in figure 2.12. The total capacitance in the array that needs to be driven is $2.11pF$, which without the split-capacitor array would be $16.83pF$, meaning the use of 2 4-bit nibbles in the split capacitor array reduce the required capacitance in the SAR by 87.4%. The asynchronous block arrives at the full 8-bit binary decision in under 50ns, meaning the SAR could properly function at up to 20MS/s if required.

The comparator for the ADC was implemented using a standard strong-arm topology and the input switches were implemented using large CMOS pass gates, which are capable of driving the input well before the $3.375MHz$ switching time. The reference
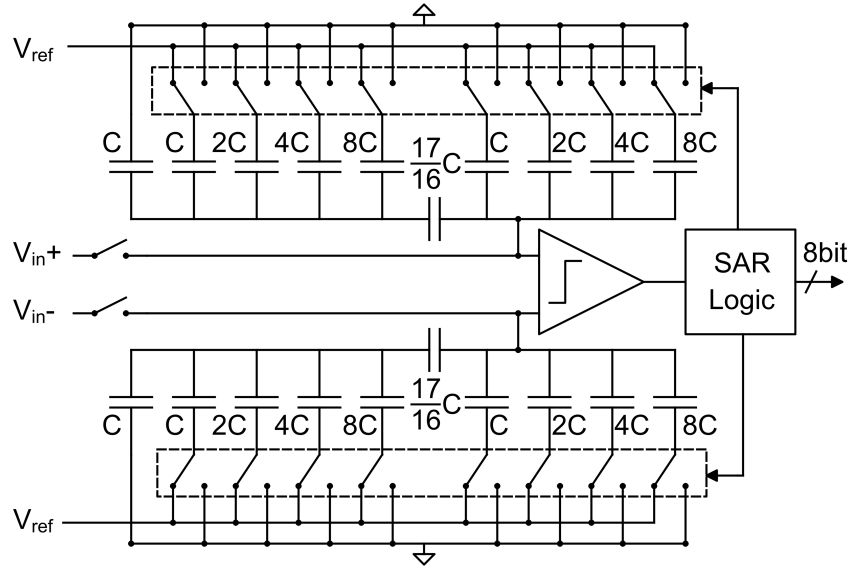
Figure 2.12: SAR ADC System Block Diagram with asynchronous controller

voltage was generated using a bandgap reference and was designed to give a reference voltage of 800mV, giving the whole switching procedure a difference dynamic range of 1.6V. The capacitor array is reset to $VDD/2$ which is $750mV$ before each sample period. This means that the SAR can operate accurately for input voltages ranging from $350mV$ to $1150mV$. The switching logic was designed to follow the asynchronous monotonic switching algorithm as highlighted by Liu, et al. [72]. The flow chart and waveforms for the logic block for the monotonic switching procedure is highlighted in figure 2.13. As the decision logic moves from MSB to LSB, the effective DC average for V_{in} approaches 350mV. The strong-arm comparator is driven with a PFET based differential input, meaning the strength of the comparison becomes stronger as the required voltage precision increases in the lower LSBs. Virtuoso simulations for the comparator block show functionality for differences as small as $540nV$.
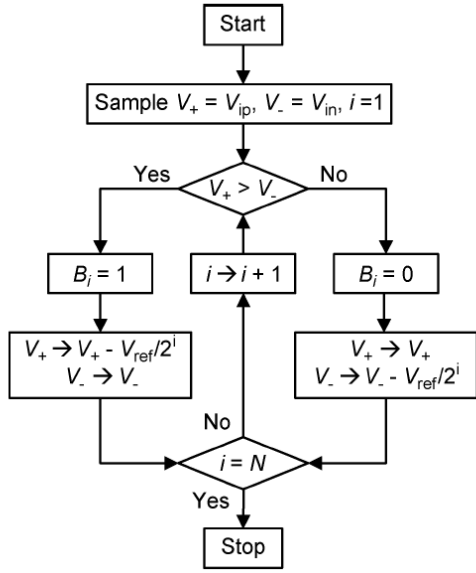
(a) Logic flow chart for Monotonic SAR
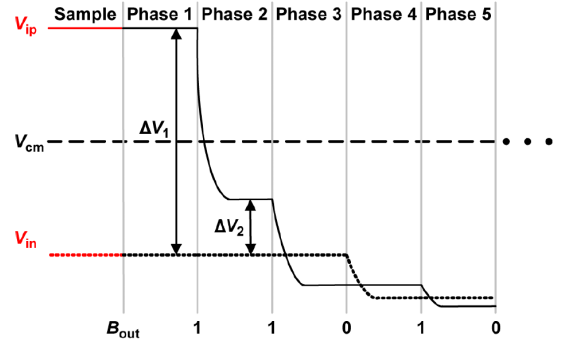
(b) Waveforms for monotonic switching procedure

Figure 2.13: Monotonic Switching Controller

2.4.2 Neural Amplification System

The neural amplification system can be summarized as a time-multiplexed 3-stage amplifier chain, with the load on the third stage being the $2.1pF$ differential capacitor array from the SAR ADC. The first stage of the amplifier has 256 copies, with an amplifier present under each site along the shank. Of these 256 electrode sites, 255 correspond to active amplifier inputs, with the 256th connected to the chip's ground as a reference. Circuit schematics for the first two stages of the amplifier chain are depicted in fig 2.14.

In the shank, there are 4 blocks of 64 amplifier stages, each connected to their own large bias generators that both supply current for the amplifier, and supply bias voltages for the gate input at the elctrode interface. Each electrode site (referred to as pixels) has a common source amplifier implemented directly under the $20\mu m$ by $20\mu m$ top metal square on the shank with the glass-cut opening to the surface sized at $14\mu m$ by $14\mu m$. To protect the gate of this amplifier from any ESD effects, an ESD diode
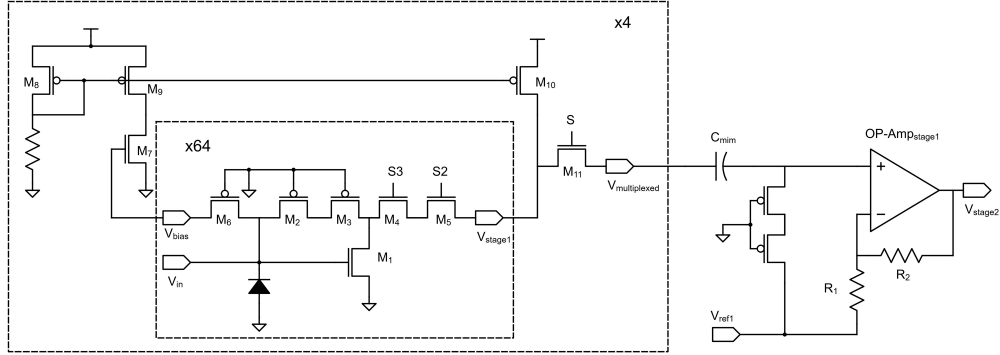
Figure 2.14: 2 Stages of Neural Amplifier System

is placed in parallel to the gate input to the chip's ground. While this is not the full recommended ESD protection circuitry for 180nm SOI, which also requires a second reverse biased ESD diode to the voltage rail, it is sufficient to prevent massive yield problems in the pixel amplifiers. To select a given pixel on the shank, digital inputs S_2 and S_3 are used to turn on transistors M_4 and M_5. The DC bias voltage at V_{on} is set by the current mirror formed M_7, M_8, M_9, and R. M_6 acts as a large resistance to provide an AC block and a DC feed through path for the current mirror. There are 4 copies of the current mirror on the base on the shank, and each one sets the DC value of 64 sites. Transistors M_2 and M_3 function as deep triode devices to maintain the DC value at the drain of M_1 when a site is not being sampled, which greatly decreases the power-on time when a given pixel is selected. At a given time, 4 pixels are selected and powered, 1 from each quadrant. A single pixel is output to the next stage of the amplifier, $Op - Amp_{stage1}$, with the selected quadrant chose by sending a digital '1' to S to close M_{11}. Each powered quadrant draws approximately $50\mu W$, meaning the total shank power drawn is limited to $200\mu W$. The mean simulated gain for the common source stage when a pixel is selected is $20dB$ for a bandwidth of 10Hz to 1MHz. Since the circuit is sampled at $12.9KHz$, this bandwidth is aliased down into the 10-6.5kHz band. The circuit topology for the amplifier $Op - Amp_{stage1}$ is depicted in 2.16b. It is a simple telescopic five transistor amplifier with a current

mirror that provides a gain of $23dB$ in closed loop for the resistance values R_1 and R_2 over the necessary bandwidth necessary bandwidth.
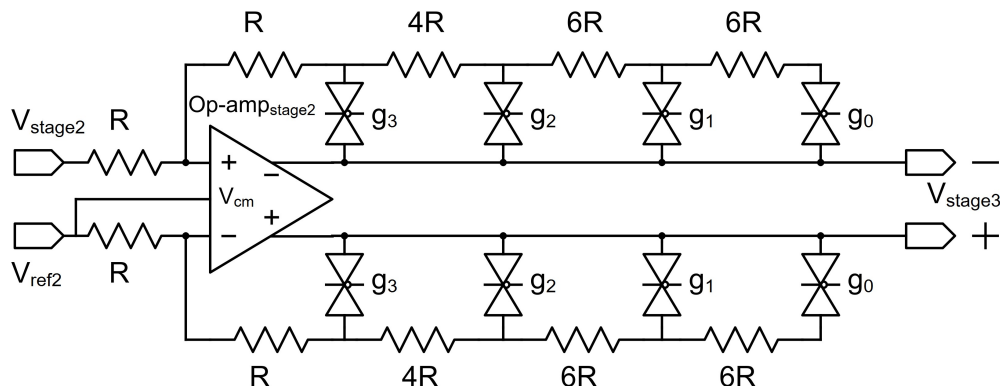

Figure 2.15: Tunable 3rd Stage of Amplifier System

The final stage of the neural amplification system is depicted in figure 2.15. This amplifier stage singled ended to differential and is tunable by opening and closing the pass gates g_3 through g_0 which are set by the ASK configuration on start-up. The unit resistance value of R for this design was $25k\Omega$, making valid tunable gains from this stage to be 0dB, 14dB, 21dB, and 24dB respectively. The input code $g_3g_2g_1g_0$ is a one-hot design, and the gain value will take the value of the left most binary '1' input code. This means the programmed gain codes are 0dB for gain codes 8 through 15, 14dB for codes 4 though 7, 21dB for codes 2 and 3, 24dB for code 1, and code 0 is invalid, leaving the amplifier in open-loop. The circuit topology for $op-amp_{stage2}$ is depicted in figure 2.16c. This topology also uses a 5 transistor telescopic base, but also uses common mode feedback to set the common-mode voltage to 750mV at both the input and output. The output common mode is of heightened importance since it will be driving the DC average sent to the SAR ADC at every clock cycle.

The DC-steady state gain for the full amplifier chain is depicted for a bandwidth of 10Hz to 1MHz, and shows a peak voltage gain of 1377 or $62.7dB$. The integrated input referred noise of the amplifier without multiplexed switching was found to be $4.2\mu V$

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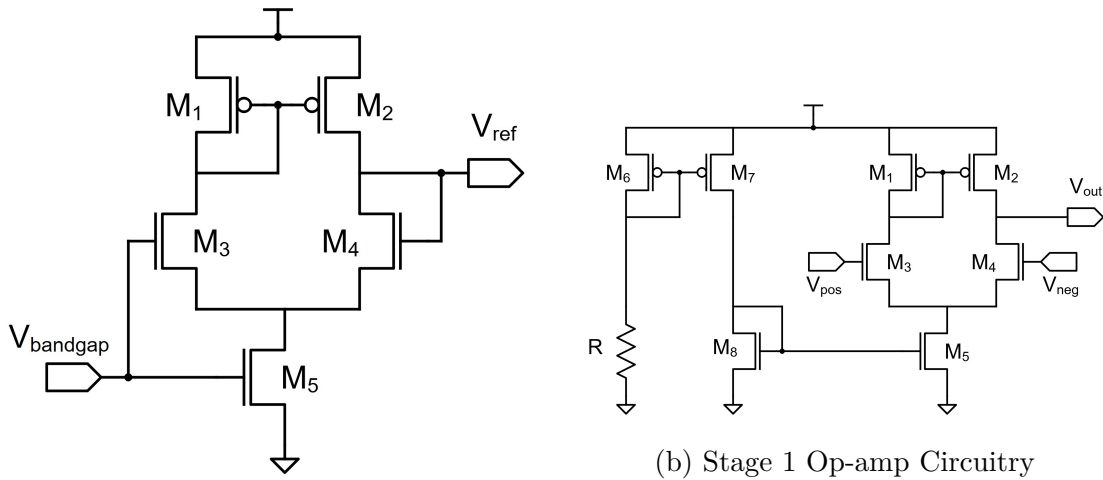
(a) Topology for Reference Generator Amplifiers

(b) Stage 1 Op-amp Circuitry
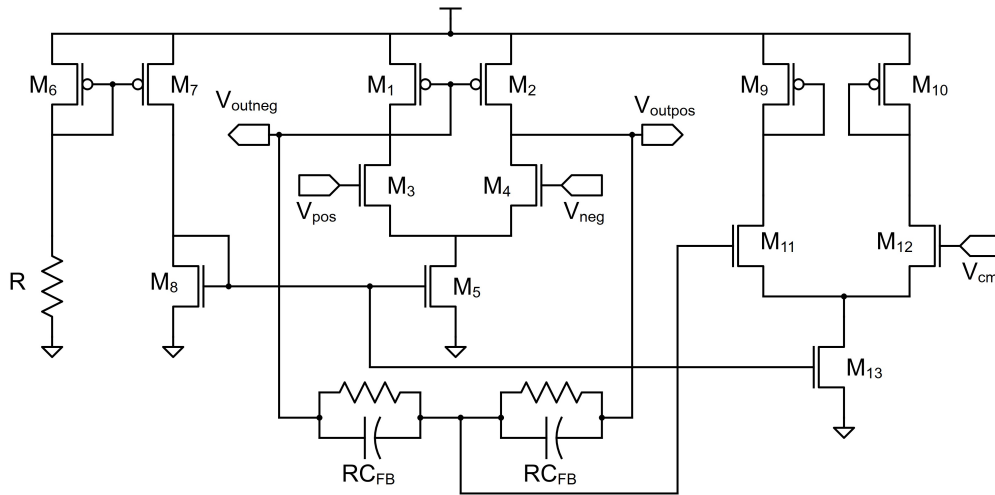
(c) Stage 2 Op-amp Circuitry

Figure 2.16: Operation Amplifier Circuit Topologies

over the 10Hz-1MHz bandwidth. The sampling frequency of the multiplexing will fold noise contributions between 6.5kHz and 1MHz into the amplifier output, and this will be reflected in a higher recorded noise value. The recommended time-multiplexing ratio to limit noise folding for neural recording systems was recommended to be 20 by Raducanu et. al [73], however our system oversamples at a rate of 64:1, leading to poor noise performance in measurement.

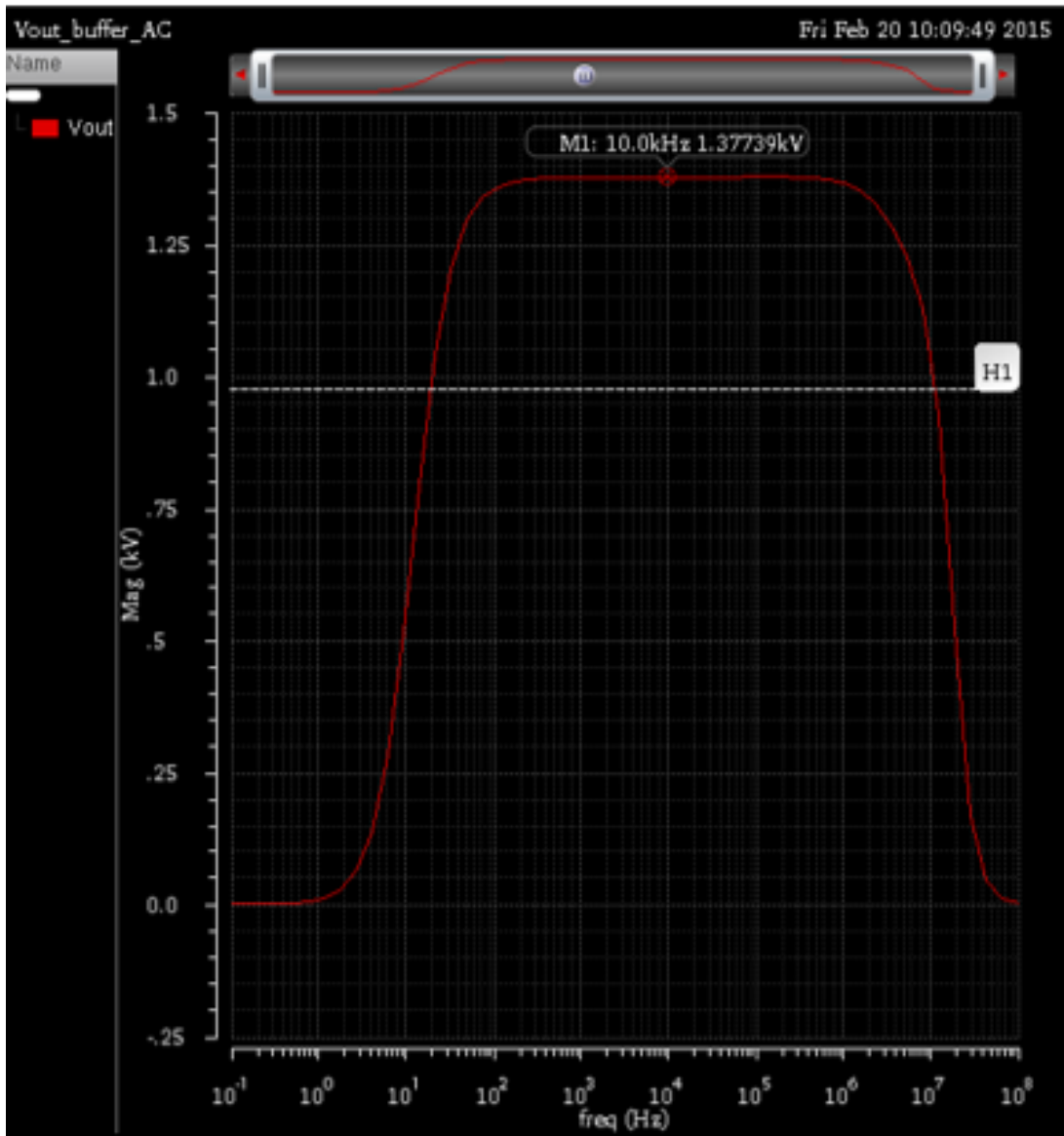Figure 2.17: Gain Performance of Amplifier Chain

2.4.3 Chip Thinning

Thinning of passive implantable medical devices has been documented with shank cross sections on the order of 10s of μms [74–76]. In our system, we perform thinning

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on after silicon electrodes after receipt from the foundry, when the probe is post-processed to thin the chip. The chip is implemented on SOI such that removal of the p-type silicon substrate has minimal effects on the bodies of the active transistors, since a blocking silicon dioxide box layer isolates the active silicon base connection from the substrate. While this comes at the cost of the circuits being vulnerable to the floating body effect, it causes chip performance and transceiver operation to be indistinguishable pre and post thinning. The passivation, dielectric of the back-end stack, and silicon substrate are trenched by successive dry etching, separating the probe from the rest of the die. The final shank is 3.2mm-long and 130µm-wide with a tapered tip. The thickness of the whole device is approximately $20\mu m$, yielded an overall implant volume of $0.08mm^3$. The trenching process can be seen in figure 2.19. First mask layers are used to etch down the metal exclude areas surrounding the perimeter of the die (2.19a), the sounding portions of the chip are then mechanically grinded down (2.19b), and finally the bulk silicon is thinned from behind until the now trenched chip is cleaved from the remaining portions of the die (2.19c). An implant post-thinning is depicted in figure 2.18a and a fully processed shank is depicted in figure 2.18b. At this thinned, the shank is flexible as is apparent in the visible curvature of the thinned die and the thinned shank. To combat this and prevent the shank from rolling to the point of damage, the chip is temporarily glued to a stiff silicon guide shank.

As can be seen in the picture, the die is now flexible, to the point that the shank is naturally curving upward. At this thickness, the probe is extremely brittle, requiring attachment to a thicker guide shank system.
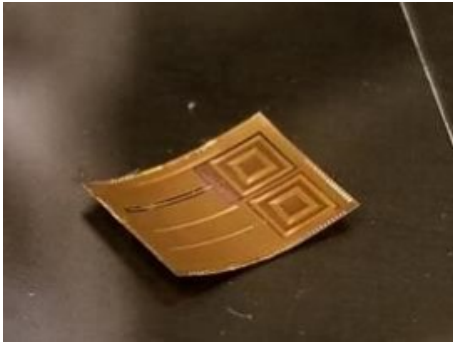
(a) Post Thinning
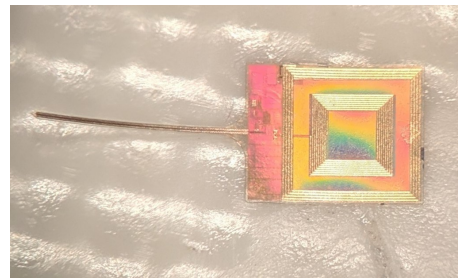
(b) Post Shank Formation

Figure 2.18: IC post thinning and shank formation
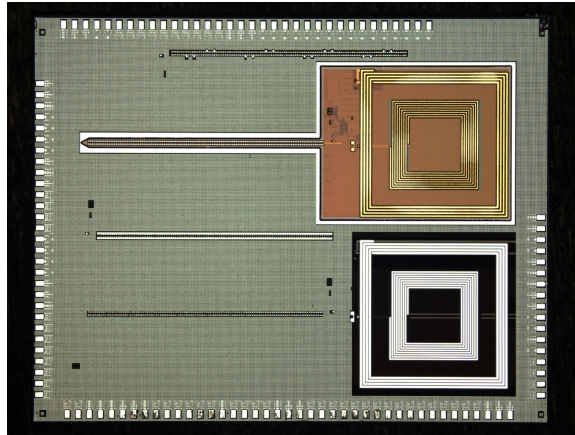
(a) IC surface post chemical etch of trench
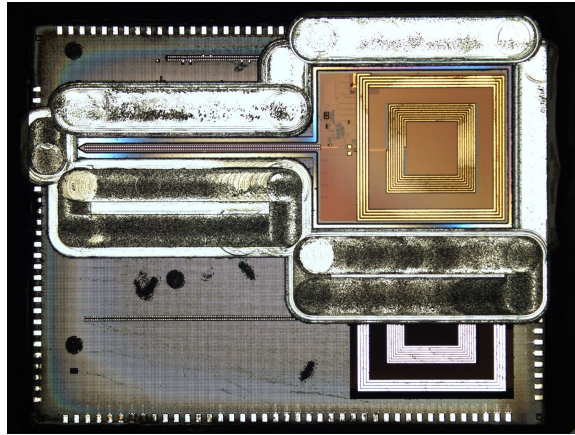
(b) IC post mechanical grinding
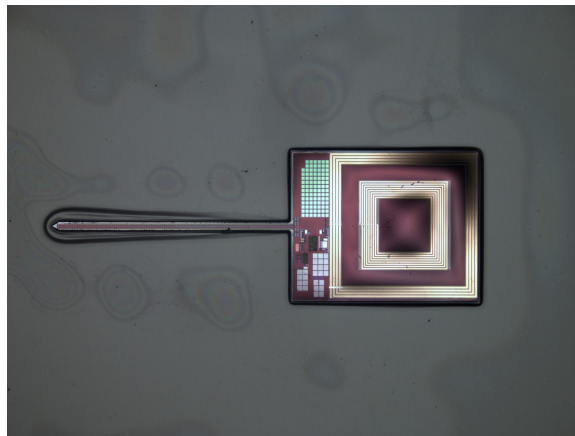
(c) IC fully detached from substrate

Figure 2.19: IC Shank Formation Procedure

Chapter 3

Design of External Reader System

The external reader system can be divided into three major sections: 1) The physical PCB trace transmitter design using electromagnetic simulations 2) The boards designed to create the power transmission signal and reconstruct and transmit the data signals 3) The verilog based reconstruction and equalization instantiation via FPGA

The system block diagram for these three systems are depicted in figure 3.1, and the physical boards can be seen in figure 3.2. The necessity for these systems come from the ISI challenges introduced by the high-data-rate backscattering through lossy media present for uplink data recovery using an integrated coil. The thickest metal layer available on the implant is limited to $4\mu m$ in $0.18\mu m$ SOI, giving the integrated

coils low quality (Q) factors from small trace cross sectional area. Low Q decreases greatly radiation efficiency, causing the received power signal to have extremely poor PTE and the data LSK signal to be >60dB lower than the transmitted 700MHz carrier. To overcome this, equalization techniques must be employed to process the LSK data and achieve acceptable BERs, and highly tunable power amplifiers must be implemented on the transmitter boards to achieve reliable powering.

3.1 PCB Coil Design

The four-coil near-field inductive link was designed using Mentor Graphics' IE3D method-of-moments solver. The power inductor pair was designed to operate at the $27MHz$ ISM band, while the data inductor pair was designed to be matched at half the self-resonance frequency of the data coil ($700MHz$), where a peak in inductor coupling is observed. Due to maximum size limitations on the RX implant coils, total coil draw length, spacing, and outer diameter could not be perfectly matched as would be ideal for maximal PTE. Instead an iterative design sweeping the minimum possible PCB line width, spacing, and copper trace thickness to find which parameters maximized radiation transfer. It was found that energy transfer efficiency was maximized when the total PCB coils internal diameter and total draw length closely matched the implant power and data coils. For the 5 turn 2mm power coil on the implant, this maximum matching occurred for a 3 turn, 6mil trace width and spacing PCB coil with an outer diameter of 4mm and inner diameter of 2mm. For the 7 turn 1.2mm data coil on the implant, maximum coupling occurred for a 3 turn, 4mil trace width and spacing with an outer diameter of 1.6mm. It was attempted to make the draw length of the data transmitter long enough to match the self-resonance frequency of the implant data receiver, since a coupling peak occurs at $1/2f_{sr}$ and is the intended carrier frequency for data uplink and downlink for the system, however
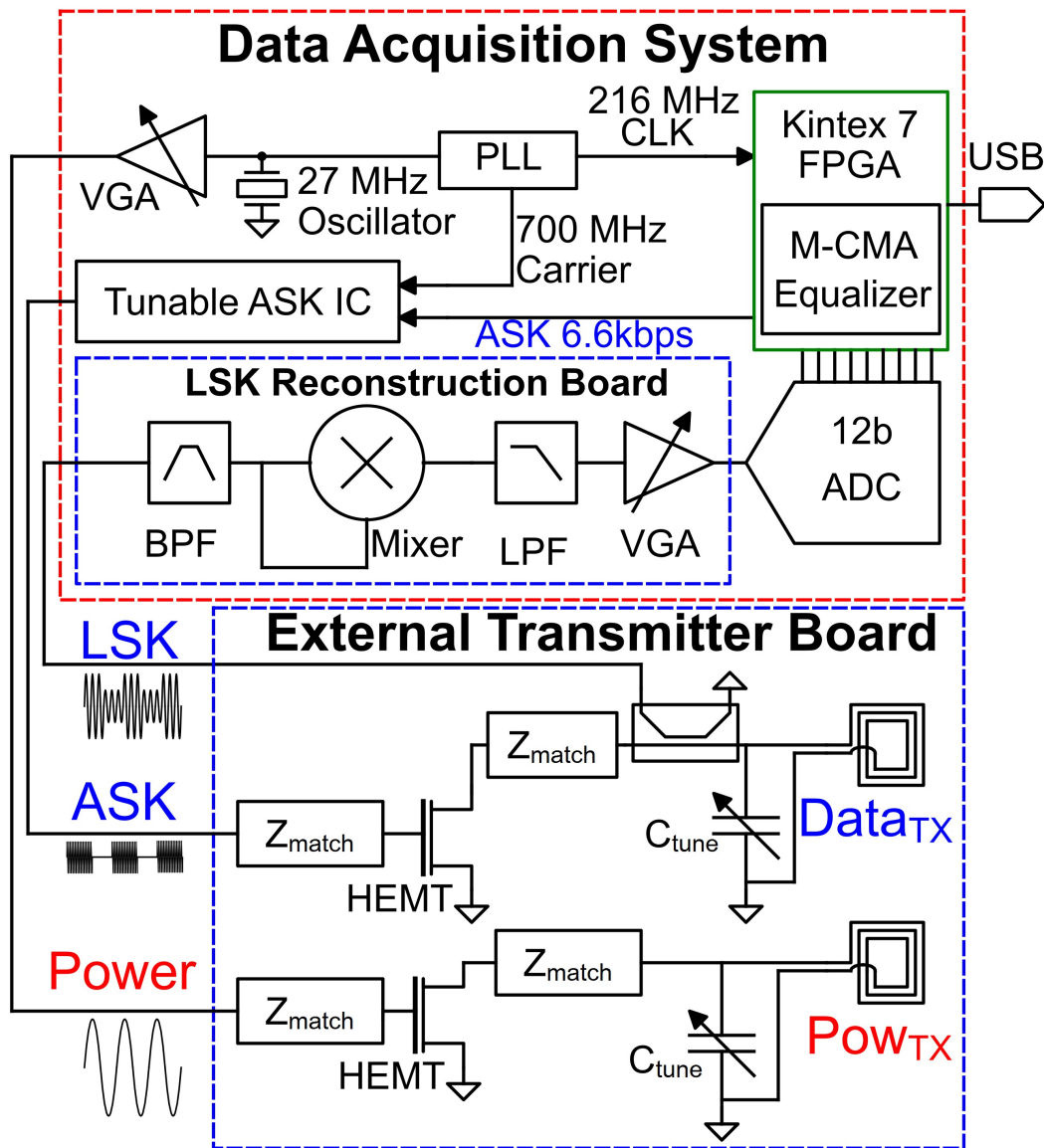
Figure 3.1: System Block of full Reader System

that draw length could not physically fit without extending past the 1.6mm outer diameter allotted and become too close to the 2mm inner diameter of the power coil. Also designed, was a differential coupled line placed on a 10 mil wide, 2 mil spaced PCB trace that is used to detect the LSK amplitude shift without effecting the tightly constrained s-parameters of the data TX coil. The 4-coil system layout is depicted in
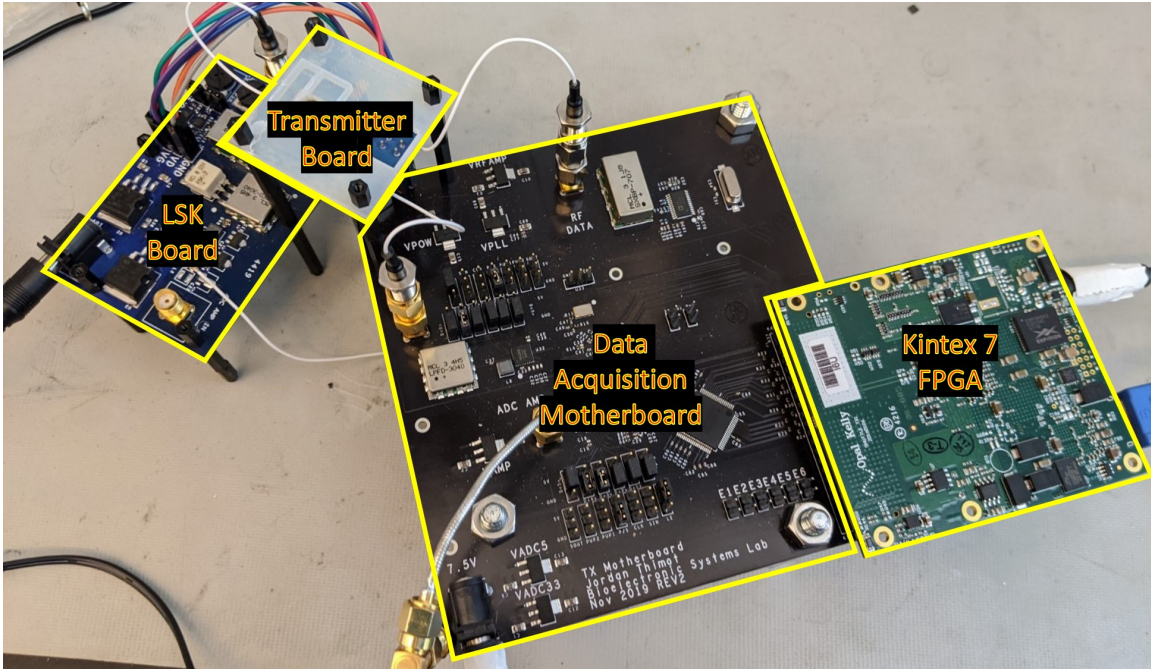
Figure 3.2: Full Physical Reader System

figure 3.3 with a 5th differential port on the coupled line. The inductor parameters for the designed 4-coil system are given in table 3.1.
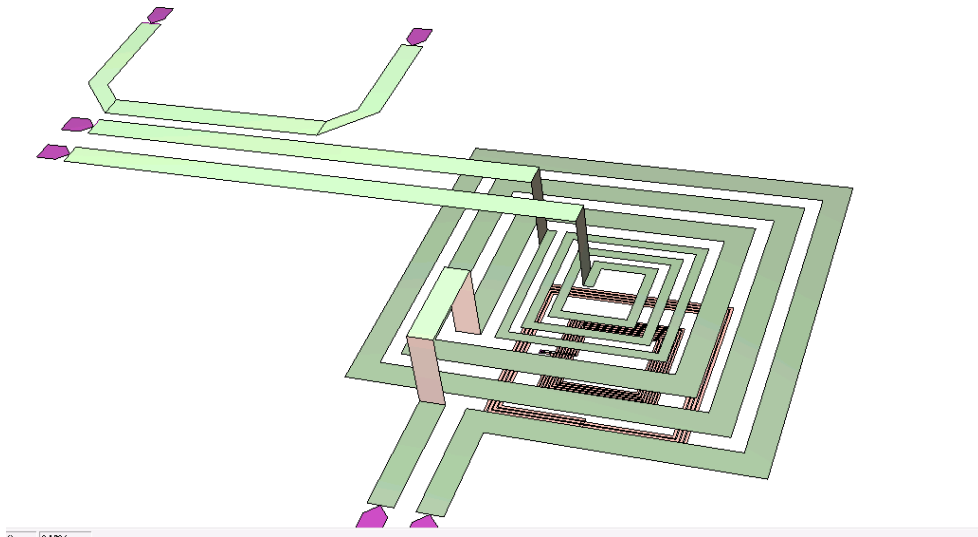
Figure 3.3: Physical Layout of 4-coil System

Matching networks for the s-parameters generated by IE3D were then designed us-

	Power TX	Power RX	Data TX	Data RX
Q_{peak}	58.9	6.1	82.0	5.8
$No.Turns$	3	5	3	7
D_{out}	$4mm$	$2mm$	$1.6mm$	$1.2mm$
F_{sr}	$1.75GHz$	$1.59GHz$	$1.88GHz$	$1.48GHz$
L	$35nH$	$55nH$	$15.4nH$	$95nH$
R_{loss}	0.33Ω	9Ω	0.91Ω	82Ω
K	$0.1(27MHz)$		$0.047(700MHz)$	

Table 3.1: 4 Coil Link Physical Parameters

ing ADS as a simulation tool. To simulate the LSK enabling and disabling, impedance parameters were generated in virtuoso for the chip in both the LSK '1' state and the LSK '0' state and an ideal switch was used to toggle the load impedance on the inductor coils for this ADS simulation. For matching the PCB side of the 4-coil link, a precise and tuanble variac was connected in parallel to the inductor output to create a 50Ω matching network as seen from the power amplifier. The resulting s-parameters for the PCB data coil with the LSK enabled and disabled on the implant side can be seen in figure 3.4a, and the simulated power transmission from reader to implant can be seen in figure 3.4b. Enabling and disabling the LSK causes the peak matching of the coil-pair to drop from approximately $-45dB$ to $-7dB$ and the peak S_{21} power transfer was simulated to be $-9.94dB$ or 10.14% PTE in air.

All of the above design considerations were performed assuming a $1mm$ separation and perfect alignment between the TX coils and RX coils in the transceiver. Also, the simulation assumes the bulk silicon has been thinned off the implant, and the ground plane lying beneath the implant coils is a biological medium with dielectric properties matching brain matter and skull. When the dielectric medium between the TX and RX coils is changed from air to biological media (instead of only below the implant system), skull/brain tissue were simulated to account for $-2.6dB$ additional electromagnetic losses for the power signal, and $-13dB$ additional electromagnetic losses for the data signal. While powering could theoretically still occur at these losses,
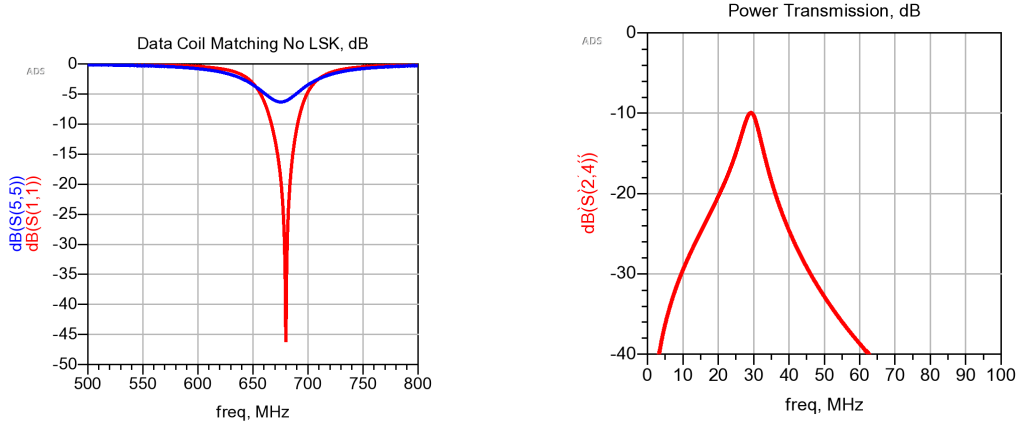
(a) Simulated LSK Performance

(b) Simulated Power Transmission Performance

Figure 3.4: Power and Data Transmission ADS Simulations

the $-13dB$ data signal loss is far too large to overcome and stay under safe SAR limits for tissue, therefore the data link can only function either with air separation or a very low loss dielectric material.

3.2 Data Acquisition System

The entire data acquisition system can be divided into three distinct boards, the external transmitter board which powers the power and data PCB coils, a low noise LSK recovery board that partially reconstructs the LSK from an extremely small unsable signal to one that can be properly digitized and equalized, and a large mother board that controls both boards and acts as a control block between the FPGA interface and any COTS components that need to be programmed. This section will include subsections detailing the design and important blocks of each board.

3.2.1 External Transmitter Board

The external transmitter board (bottom block of fig 3.1) is implemented with a 3.8-cm-by-3.8-cm transceiver board containing transmitter (Tx) antennas and power

amplifier HEMTs capable of delivering 4 W of power to each of the antennas. The circuit schematics for both TX systems on the board are depicted in figure 3.5. For the power transmitter, LC matching networks are present at both the input and output of the power HEMT, which matches the driving load to 50Ω at the $27MHz$ transmitter frequency. The data transmitter has a higher order matching network at the HEMT input in order to get a deeper voltage matching at the cost of power transfer efficiency, which is fine since we only care about the coupling and not directly energy transfer for the data coil pair. In addition, the data transmitter network has the coupled line sensing circuit for detection of the backscattered LSK data. Each amplification circuit operates with a drain voltage of $15V$ and the gate voltage is tunable using a negative voltage regulator and typically operates between $-3V$ to $-1.2V$. The radiation efficiency of the network ranges from 45% to 68% depending upon frequency of operation. The typical total power drawn from both data and power TX systems is approximately $900mW$ for each HEMT, which at 68% radiation efficiency corresponds $612mW$ of radiated energy for the power transmitter. Since this supplies the minimum amount of power the implant requires $(10.4mW)$, the PTE of the link must be greater than 1.7% to proper power the device. If operating at the maximum 4W of DC power, the PTE of the link can be as low as 0.38% and still operate.

The physical layout for transmitter board is pictured in figure 3.6, where the actual PCB coils can be seen in the alignment boxes on the silkscreen on the left side of the board. The components including the power HEMTs, matching networks and DC bias systems are located on the top side of the board. Heat sinking for the transmitter board must be performed if operating at greater than $900mW$ of DC, as the board will become hot to the touch (measured to be $> 50°C$ using a IR temperature sensor) and thus be unsuitable for placing in close proximity to brain and skull, as it will cause localized heating in the tissue.
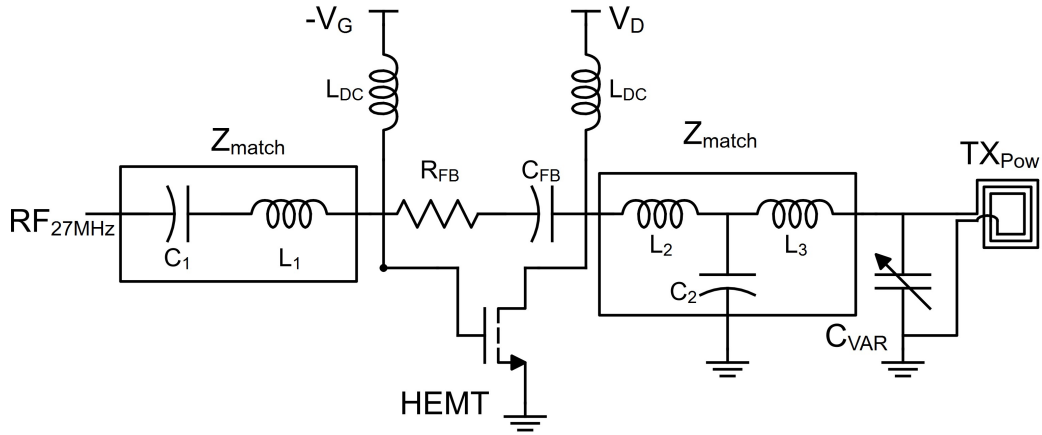
(a) Power Transmitter Schematic
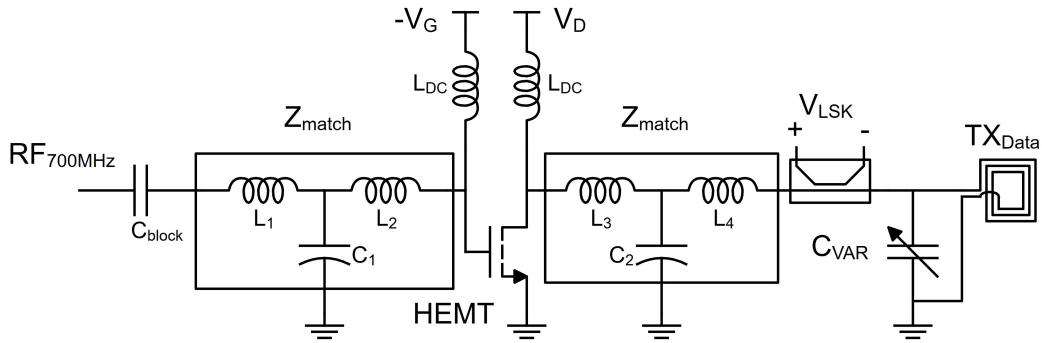
(b) Data Transmitter Schematic

Figure 3.5: Power and Data TX Board Circuitry

S-parameters of the energy transfer for the power and data transmitters is given in figure 3.7. As can be seen in 3.7a, the power amplifier can provide at least 15 dB of power gain to the TX power coil from the $25 - 30MHz$ band, and from 3.7b, the data amplifier can provide at lease 10 dB of power gain to the TX data coil across a wide band of $600 - 1000MHz$, giving a large amount of flexibility to tuning of the exact power and data frequencies.
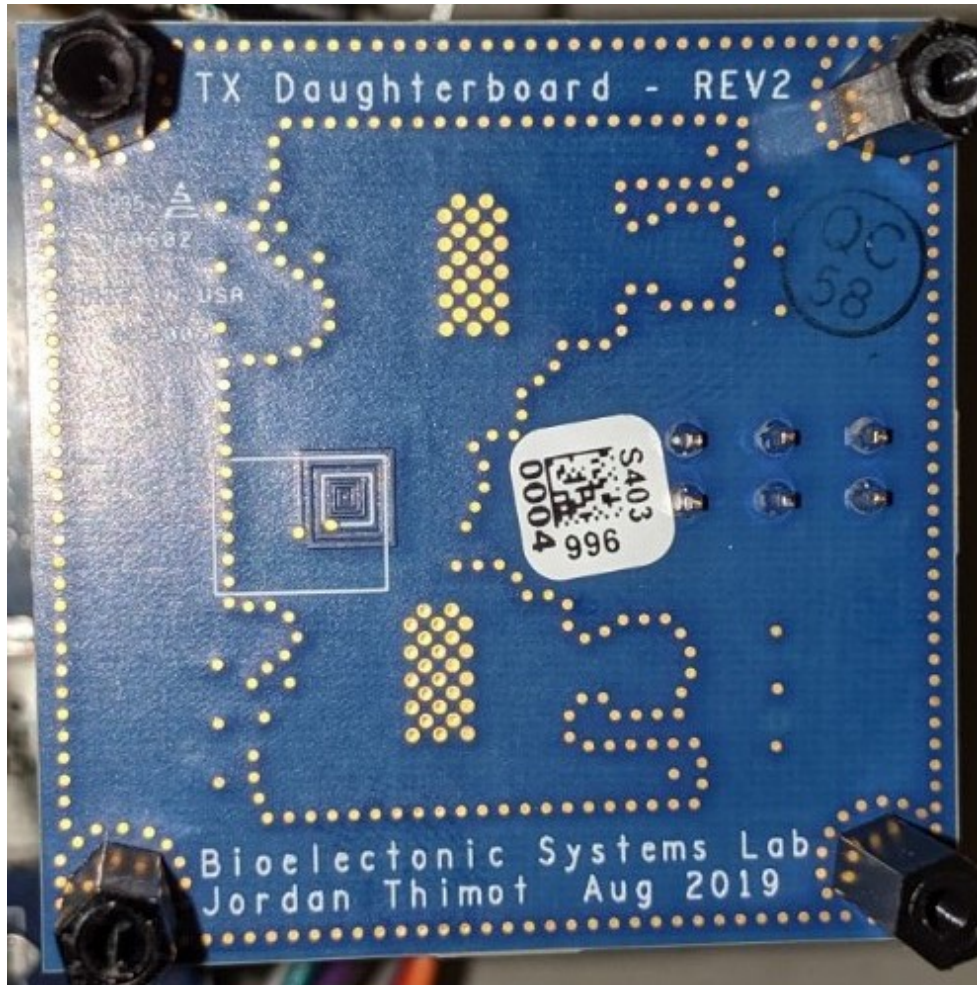
Figure 3.6: Transmitter PCB with Reader Transmitter Coils

3.2.2   LSK Reconstruction Board

An ADS simulation for the expected backscattered LSK signal is depicted in figure 3.8. Since the LSK is an incoherent amplitude modulation technique, the typical circuit based approach for data recovery is to implement an envelope detector that will track the data waveform. Unfortunately, as can be seen in 3.8, the power signal is modulated onto the 700MHz carrier at approximately a $1V$ amplitude for a 10V carrier, while the actual amplitude shift caused by the LSK for different LSK modulation states is only 10-20mV as depicted in figure 3.9. This 10-20mV shift from the LSK indicates the dynamic range for the difference in LSK states is on the order of
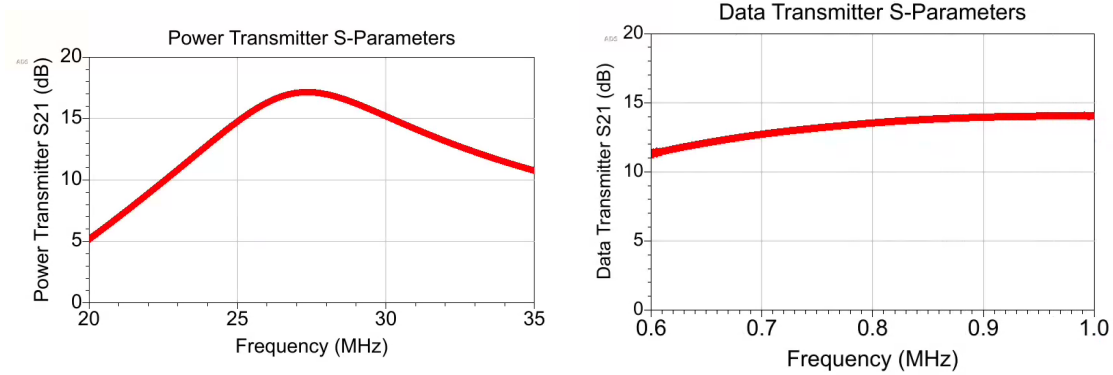
(a) Power   Transmitter   Amplifier   S-parameters

(b) Data   Transmitter   Amplifier   S-parameters

Figure 3.7: TX Board Amplifier S-parameter performance

60-80dB smaller than the carrier amplitude and 40-60dB smaller than the power signal interference. This means a simple envelope detector will not capture the required data set and a more innovative solution is required.
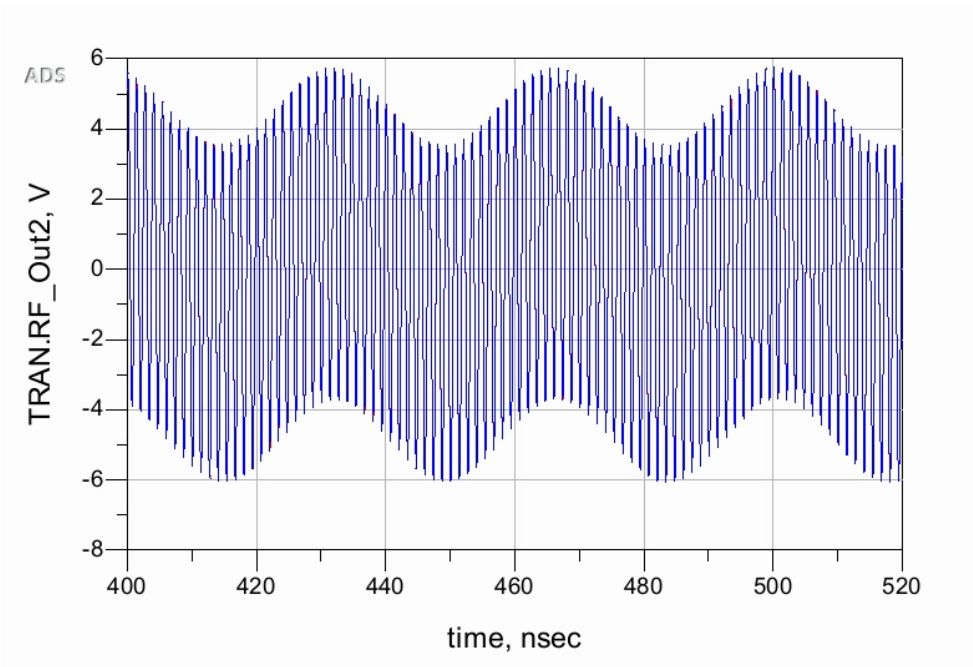
Figure 3.8: Simulated expected waveform across data TX with normal implant operation

If instead we look at the signal in the frequency domain, we observe that a random

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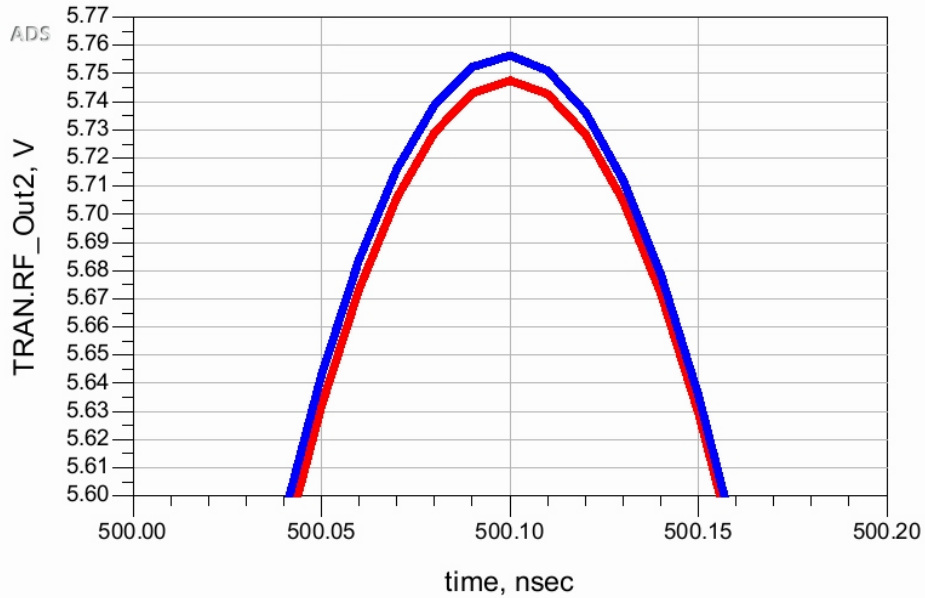
Figure 3.9: 10mV Amplitude difference on carrier with LSK at different binary states

binary sequence at $27Mbps$ will actually have very limited frequency content at $Mbps$ and instead will have non-symmetrical frequency content around half the clock data rate at $13.5MHz$ with the magnitude of spikes varying based on the percentage of '1's and '0's in the given data window. When we modulate this data signal onto the $700MHz$ carrier, we actually see these frequency spikes symmetrically distributed at $687.5MHz$ and $713.5MHz$. The power interference provides large spectral energy at $27MHz$, $673MHz$ and $727MHz$. Plotting the spectral content in a FFT, we get frequency content that looks like the distribution in figure 3.10. If we tightly bandpass filter this signal to keep only the carrier spike (blue spike in figure 3.10) and the LSK content (green spikes in figure 3.10) we can remove the 27MHz power interference. If we then self-mix the signal, we will remove this 700MHz signal entirely, and the remaining LSK spectral data will be converted back into the baseband, leaving a usable and reconstructable LSK signal for data processing via FPGA.

To create this LSK reconstruction circuitry, an 8-cm-by-5-cm low-noise board was designed. The primary circuitry blocks on this board is depicted in figure 3.11 and the

55
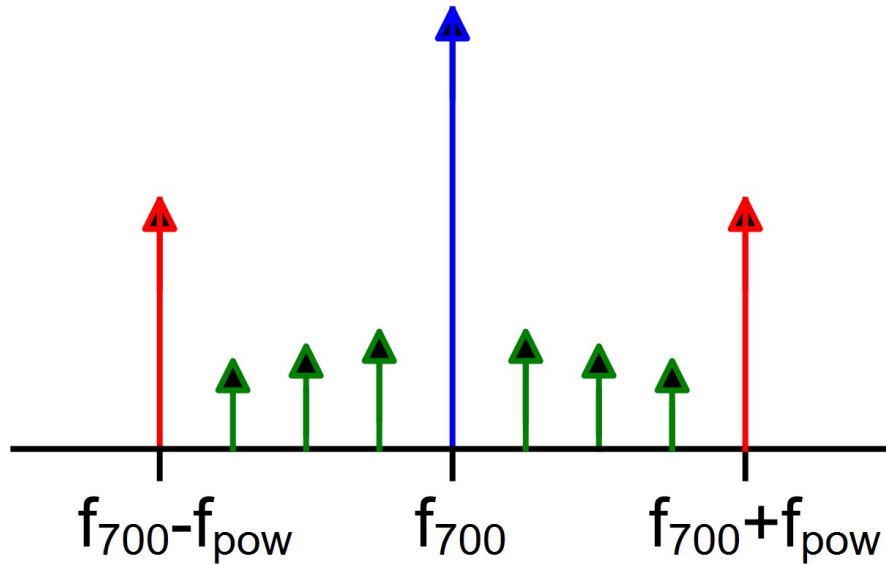
Figure 3.10: FFT content of signal at data receiver

physical was previously pictured in figure 3.2. The bandpass filter, mixer, and lowpass filter blocks are instantiated using COTS RF components. To keep the noise level low on this board, the only other components present on the board are DC regulators which are used to power the variable amplifiers on the board and to supply the tunable gate voltage and $15V$ drain voltage for the HEMTs on the external transmitter board. The power regulators for the transmitter board was moved off board and onto the LSK board to address heating concerns.
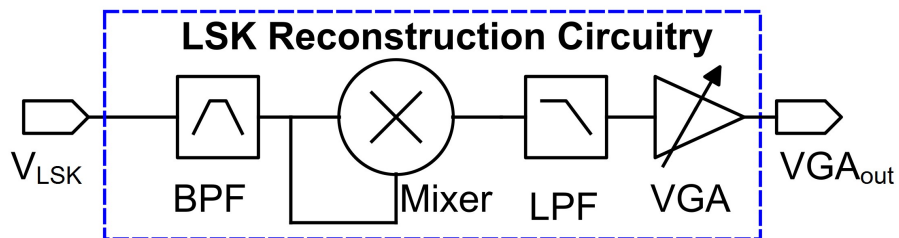
Figure 3.11: LSK Recovery Circuitry Blocks

After filtering, mixing to convert the signal to the baseband, and subsequent lowpass filtering and amplification, the resulting LSK waveform appears as in figure

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3.12. The original $10mV$ shift due to the LSK with $1V$ interference, has now been converted into a $150mV$ amplitude LSK signal with clear distinct binary states and power interference is less than $20mV$ in amplitude. While this signal is still not completely clean, it is now in a state where software reconstruction can be used to fully analyze and record the data sequence.
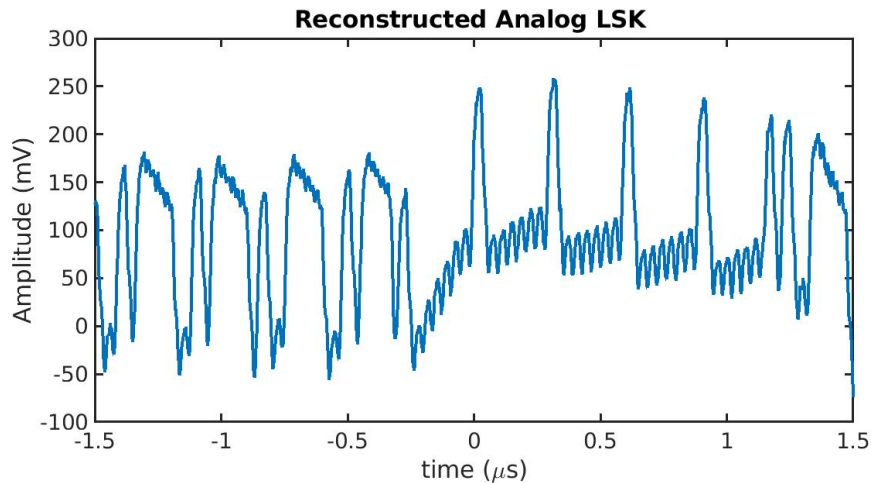
Figure 3.12: Signal Waveform at output of LSK Reconstruction Board

3.3   Data Reconstruction

The final data reconstruction can be divided into two portions, the development of a custom equalization algorithm called the Modified CMA Algorithm and the FPGA Interface that is responsible for controlling, sorting, and reading the binary decision of this equalization out to the user in a Kintex 7 FPGA controlled via a python interface.

3.3.1   Modifed CMA Algorithm

As discussed in chapter 1, depending upon the reconstructed LSK signal's properties, different data decision blocks can be used to come to a final binary decision. Since

the recovered LSK signal is incoherent and we do not have access to a training sequence, traditional adaptive filter techniques such as the least-means-square (LMS) or recursive-least-squares (RLS) algorithms are not possible. The constant-modulus algorithm (CMA) can recover incoherent signals without a training sequence but requires a constant carrier waveform amplitude that the adaptive filtering can try to match and just check the signal's phase. However, the use of self-mixing to demodulate the LSK signal only produces positive in-phase amplitude impulses for '0'-to-'1' transitions and negative in-phase amplitude impulses for '1'-to-'0' transitions that return to zero in-phase amplitude in two to three data cycles. This settling scenario is easily visible in figure 3.12, where an amplitude of $150mV$ corresponds to a '1' value at the $-1\mu s$ time stamp, but corresponds to a '0' value at $0.5\mu s$. The consequence of this setting is that three or more consecutive '0's or '1's become indistinguishable in amplitude, causing the CMA error function to fail since the signal does not have a constant average amplitude. To correct this, we change CMA error function is changed from adaptively forcing the data carrier to have a constant absolute value to only detecting if the current error function value is above or below the impulse threshold of a data transition. If the signal is above the threshold and of positive in-phase amplitude, the decision is a '1'; if of negative in-phase amplitude, the decision is a '0'. When the error function drifts below the threshold, we know the signal has settled back to zero amplitude but no change in data output has occurred. The M-CMA decision can be represented in equation 3.1 as:

$$
y_d(T) = \begin{cases} 0, 1 & e(T) > Thres \\ y_d(T-1) & e(T) < Thres \end{cases} \tag{3.1}
$$

where $y_d(T)$ is the data decision at for the current sample time, T, and $e(T)$ is the original error function for the CMA algorithm. The error threshold (thres) is

an eight-bit user defined input constant, which varies based on Tx/Rx separation and the lossy medium. Because there are eight samples per symbol, a phase-picking algorithm takes the XOR of the current and previous M-CMA-decision to identify the time stamps of data transitions, recovering the phase of the incoherent signal and centering the FPGA clock to the data's phase. The M-CMA hardware was designed using MATLAB Simulink which generated synthesizable Verilog.

From an ISI perspective, the channel response depicted in figure 1.5 had two unique power transmission levels for '1' and '0' code communications. This differs slightly from our designed ASIC with passive LSK, which transmits a positive $90°$ power impulse for a '0' to '1' transition and a negative $90°$ power impulse for a '1' to '0' transition. Graphically, this causes our ISI to take the form depicted in figure 3.13.
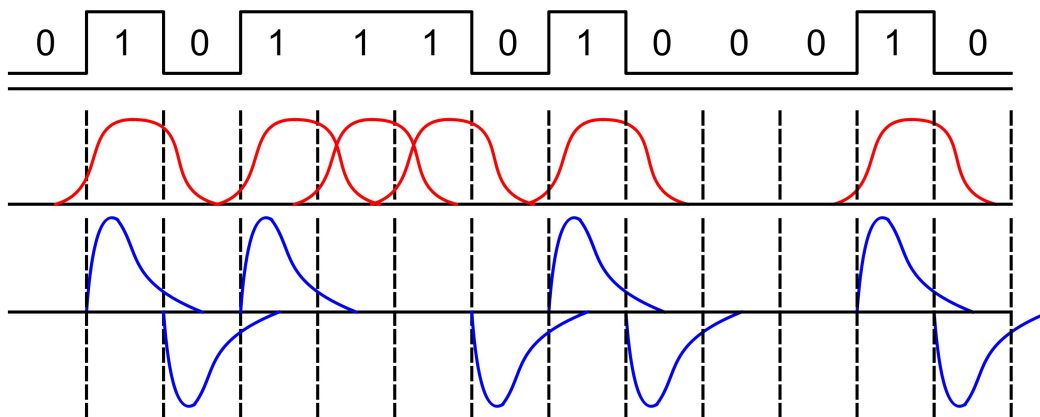
Figure 3.13: ISI for implant (blue), standard NRZ ISI (red)

The details of this ISI problem, lead the steps for creating the error function of the M-CMA algorithm. First the Raw LSK signal is filtered knowing the ratio of samples to symbols is 8:1. Then, to isolate the impulses a subtraction function is implemented between each sample and the sample from 2 previous time stamps. We then threshold the results of this subtraction using the 8-bit value of Thres and do signed boolean comparison for the subtraction result to 0. This yields three separate

strings of boolean decisions, a set that shows the time stamps of clear '0' to '1'
transitions, a sample set that shows the time stamps where the current amplitude
is below the equalizer threshold, and a final sample set that shows the time stamps
where a clear '1' to '0' transition occurred. We continuously run the previous 128
decisions from these three sample sets. 128 decisions are stored as that represents 2
bytes worth of data of subsampled data for an 8:1 sample to symbol ratio. For error
correction, we identify portions were consecutive '0' to '1' transitions occurred where
an accompanying '1' to '0' transition did not occur in between and vice versa. When
this error condition is met, it means the first transition was a false threshold flag, and
that transition is reset to a below equalizer threshold, effectively changing the value
of all final symbol decisions between the false transition and true transition. This
error correcting routine is depicted in figure 3.14.

Figure 3.14: Error Correction for M-CMA final decision

3.3.2 FPGA Interface

To perform the software reconstruction, an Opal Kelly XEM 7350T-160 was used,
which has a Kintex 7 FPGA capable of operating at 200MHz for data processing.

The final goal of the software reconstruction is to be able to select and live-plot an individual site. The expected data routine on start up is the chip's blinking configuration state. In this state we expect the imp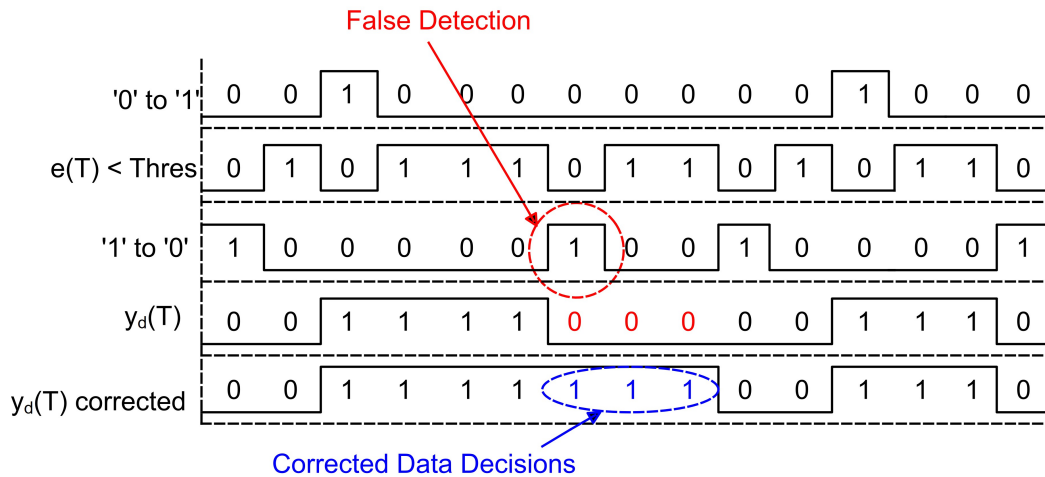lant to repeat the same configuration word for 4096 bytes cycles, then listen for the input configuration for 4096 cycles. We implement the FPGA to identify when the configuration word is repeated in excess of 4 times, and then trigger the desired input ASK code (a 4 bit code repeated twice). Upon successful writing of this configuration code, the implant will enter the data transmission routine. The expected binary sequence in the data transmission mode is depicted in figure 3.15. The programmed configuration word will be cycled every 256 bytes of data, meaning we need to sync the data to the point where the programmed implant configuration repeats itself every 2080 bits.
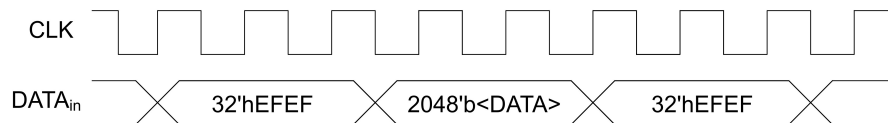
Figure 3.15: Expected Data Sequencing for input word '1111'

Now that we know what data sequence we are searching for, we can implement a data-sorting routine. The FPGA waits until the configuration word is identified and triggers a data-start flag. The system resets the pointer on an 8kB SRAM block which sorts the 2048 bit sequence into 256 consecutive 8 bit words in the expected sampled site address, starting at address 8'hFF and ending at 8'h00. The system then expects the configuration word to be repeated exactly 2080 bits after the first configuration word, and if it appears, the FPGA triggers a data-synced flag, which allows the SRAM block to move on to the next 2kB of addresses. If no configuration word is detected at 2080 bits, the system identifies the previous 2080 bits as a false flag and resets the SRAM block of address that were programmed. On three successful consecutive data-synced flags, the SRAM block is filled enough to send a full word of data for each address along the shank. With a 27Mbps data rate coming out of

the equalizer, it therefore takes $231\mu s$ for the equalizer to trigger this flag. These words of data are loaded into a FIFO using the DDR3 RAM clock provided on the XEM7350 at 100MHz. Each word entered into the fifo is of the digital form $32'h(< ADDR >, < Vsamp1 >, < Vsamp2 >, < Vsamp3 >)$, meaning the FIFO block is able to upload 24 bits of equalizer data in a single 100MHz clock cycle including the data's physical location on the shank. Doing the math, we can see that the 100MHz FIFO block is therefore able to upload the entirety of the previous 6kB of equalizer data (now with an added location address for 8kB total) in only $2.6\mu s$.

To prevent this FIFO block from overflowing and having data lost and to sort the data into long time sequences from any selected site, the FIFO block is uploaded to the 512MiB DDR3 RAM interface available on the XEM7350. The DDR3 interface was implemented using a Xilinx Mig 7 Series DDR3 RAM controller. The block is capable of burst writing up to 4 words (128bits) of data from the FIFO in a single write sequence, and read data 4 words at a time, meaning it is simple to create a pipeline system that will automatically sent four sites of data to a connected computer through the USB3 interface. A write cycle takes an average of 5-8 clock cycles to complete, while a read cycle takes 3-4 clock cycles. Time wise, this means it takes the FPGA between $13\mu s$ to $20.8\mu s$ to fully empty 8kB of data from the FIFO block, leaving approximately $200\mu s$ of excess time before the next data-sync request from the sorting block to read any stored data from the RAM block before another write block request is issued. The RAM block is able to collect data for 121 seconds before filling, requiring rewriting over previous data to continue real-time data collection.

If the user wants to continuously plot data from a quartet of sites in real time, the user can request to always read the previous 1000ms of data from the current write point in the RAM block, or a user can choose to extract and read the entirety of the 512MiB RAM for all 256 sites after the RAM is filled, which corresponds to about 2 minutes of continuous sample points. This flexibility gives a user the ability to always

be monitoring up to four sites in real time, or have the ability to massively record from all sites in a two minute window. The block diagram for the FPGA sorting block, FIFO pipeline, and DDR3 RAM interface are depicted in figure 3.16.
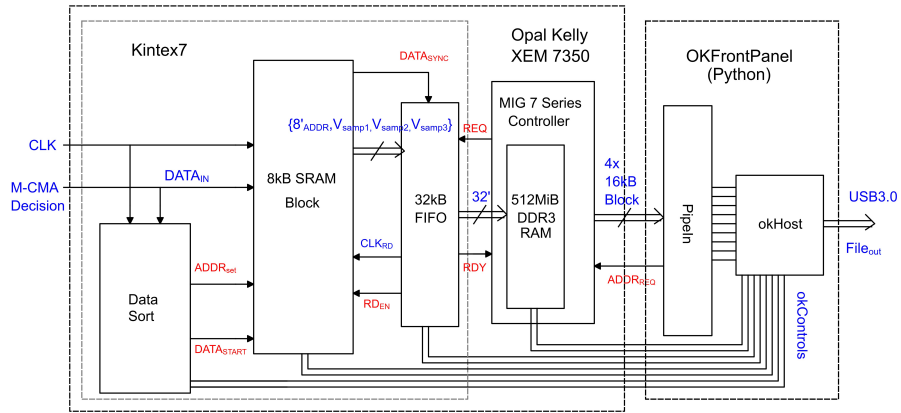
Figure 3.16: FPGA design for real-time data sorting

Chapter 4

Measurement and Simulation Results

This chapter will cover both measurement and simulation results for the power delivery systems and data transceiver, effects of post-processing and thinning the IC on the system's performance, and neural amplifier results.

4.1 Power and Data Telemetry Results

This section will cover both ADS simulations and measured analysis of the 4-coil link for both power and data telemetry performance. Direct measurements for power delivery are able to be taken through wirebonded connections to the positive and

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negative terminals of the power coils. Comparable measurements for the data coils could not be taken, as the wirebonds and cabling at the carrier frequency of $700MHz$ dominate the measurement, so data coil measurements are estimated using backscatter amplitude shifts and compared to expected simulated backscattered performance from ADS.

4.1.1 Power Harvesting

Direct measurements of the S-parameters of the power coils for an unthinned die with $250-300\mu m$ of 1000Ω-cm silicon substrate present were taken through direct wire bonds to the power receiver coil. This measurement was used to calculate and record the WPT and efficiency of the link. Measured S21 for WPT for an unthinned implant in air and phantom are depicted in figure 4.1 a. This measurement shows peak power transfer of $-15.9dB$ for the silicon substrate in air, and drops to $-19.8dB$ of peak PTE when transmitting through $1mm$ of a gelatin substrate, which has a real dielectric constant, ϵ', of approximately 85 with a small complex dielectric constant less than 10, ϵ'', which is comparable within an order of magnitude to most tissues and can accurately represent losses in an in-vivo environment [77–79]. These measured results are also comparable to ADS simulations at 1mm separation for a thinned implant transceiver with a $300\mu m$ brain and skull model representative of a mouse which show a peak expected WPT of $-14.7dB$.

Post thinning, direct WPT measurements for a thinned die was not possible to be taken as the bond pads are cleaved from the chip, making such a measurement not possible. However, ADS simulations indicate an expected WPT increase of 1.1dB post thinning, which is consistent with observed coupling at the external transceiver. Later wireless LSK signal recovery on a thinned and unthinned die will confirm this increase in expected power performance and efficiency. S_{43} simulations (Fig. 4.1

c.) for data coil coupling show a 30-dB decrease in received signal when the LSK is enabled, which is consistent with the observed amplitude shift in the backscatter LSK signal at the data Tx, and is also consistent with the expected LSK shift in frequency response as covered in chapter 2.2 and chapter 3.1. The overall measured PTE of the link is 2.57% with 1mm of air separation which drops to 1.04% through a 1-mm gelatin phantom. In both cases, this WPT exceeds the minimum required PTE required for full operation while remaining under safe SAR thresholds. Peak WPT from 1-5 mm of separation (Fig. 4.1 b.) show a decrease of 35dB from minimum to maximum separation. Beyond 2.5 mm the overall WPT drops below 0.1% where the external transceiver can no longer fully power the implant at this coil size at all, and will also exceed SAR limits for tissue and causing a high level of tissue heating and thus be incompatible for a live surgery. The exact range of wireless power transfer at which the chip turns off, could not be directly recorded, since the range of data communications is limited to $< 1mm$. It is known the power range is longer than the LSK communications range, as it is possible to move the chip out of data communications range and back into range without the system having to be reprogrammed, indicating the implant never fully lost power to reset the system.
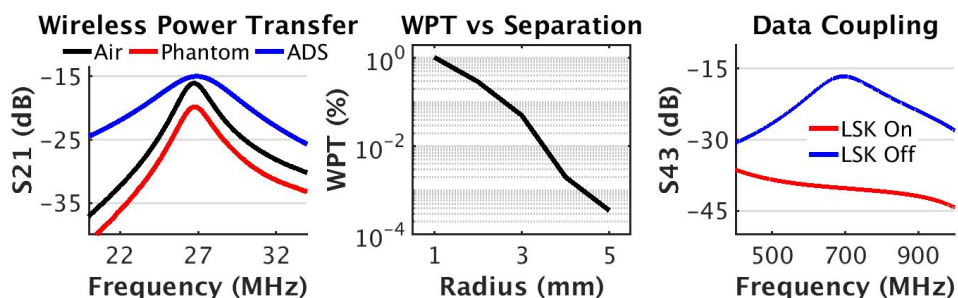

Figure 4.1: Power Loss vs misalignment

All of the above power verification measurements were taken by wirebonding the power coil connections of an unprocessed die to a small connector PCB, aligning the reader and wirebonded chip using a 3D-printed interposer, and using stacks of $250\mu m$

spacers to slowly increase the separation between the power transmitter and the implant, taking S-parameter measurements at each stage using a network analyzer. This recording process is depicted in figure 4.2.
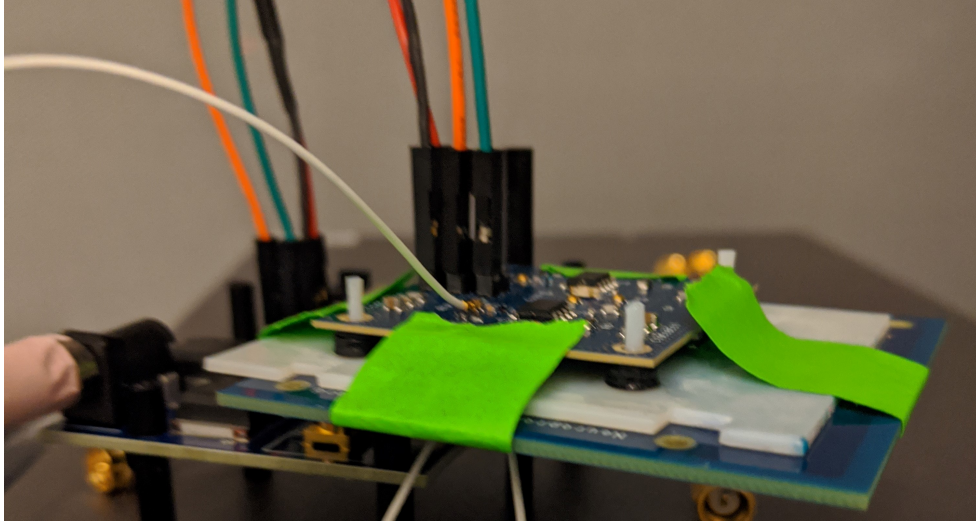
Figure 4.2: Methodology for Power Measurements

To simulate determine the sensitivity of the link to exact orientation, separate power simulations were ran in ADS comparing the power transfer efficiency of the link with perfect alignment, and when offset by $0.25mm$. The results of this simulation are depicted in figure 4.3 which shows that $0.25mm$ misalignment (an easily alignable metric by hand and visual inspection) only leads to power transfer degradation of approximately $3dB$. The relative robustness to alignment for WPT is confirmed in operation, as the chip will power on and begin to communicate the moment the radius between the reader TX and implant RX drops below approximately $1mm$.

Since the power delivery and data communications do have sensitivity to alignment within $1mm$, an aligner 3D-part was designed that will secure the chip directly over the alignment silkscreen marker on the transmitter PCB. A picture of the transmitter with this alignment interposer with a chip correctly aligned is depicted in figure 4.4.
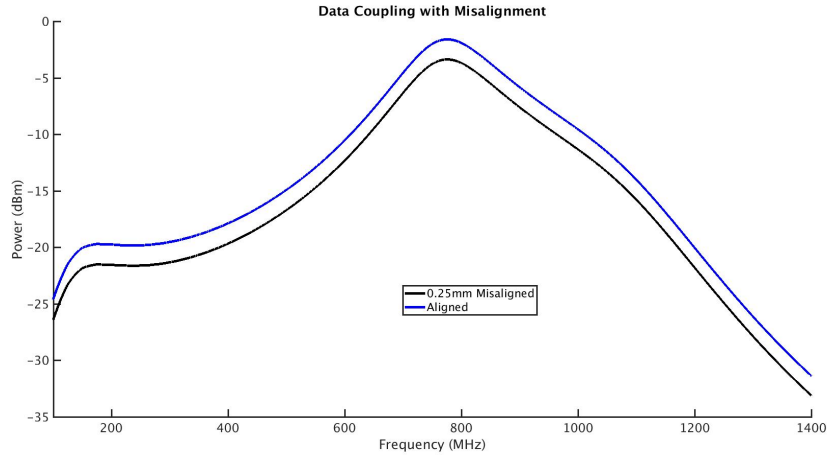
Figure 4.3: Power delivery with 0.25mm alignment offset

4.1.2 Data Telemetry Results

Backscatter waveforms for the data transmitter coil agree with ADS simulations for the implant ASIC with LSK toggled on and off as depicted in figure 3.8 with the dynamic range issue addressed in figure 3.9. The dynamic range for the difference in LSK states is on the order of 60-80dB smaller than the carrier amplitude (for this simulation, the amplitude shift was on the order of 10-20mV for a 10V carrier). To correct this problem, the LSK reconstruction algorithm covered in chapter 3 is performed, afterwards the received LSK signal has visible separate binary states as seen in figure 4.5. The curve in blue represents the raw waveform after the self-mixing stage during the LSK reconstruction, and the red curve represents the final binary decision after the M-CMA algorithm.

These separate binary states have one drawback, however, since the ISI causes the amplitude to drift. This severity of this problem is highlighted with the eye-diagram of this raw LSK signal as seen in figure 4.6. There are three distinct states visible in that eye, the high positive amplitude from '0' to '1' transitions, the high negative amplitude from '1' to '0' transitions, and a zero amplitude state that occurs when there are consecutive strings of '0's or '1's and no state transition has occured. As can be seen

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Figure 4.4: 3D Printed Well for TX/RX Alignment

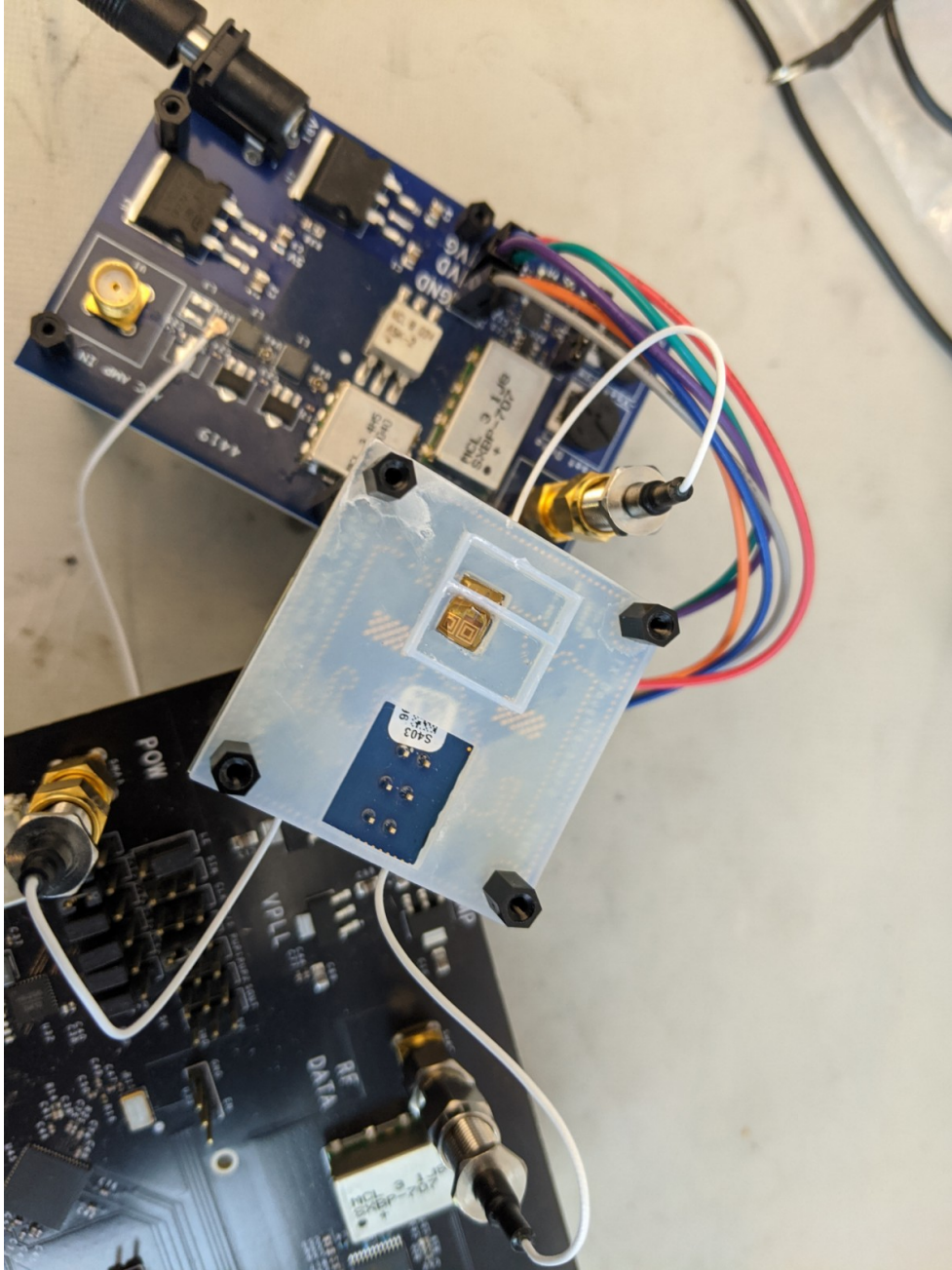in the figure, the measured eye height is actually negative (specifically $-0.08mV$), indicating an overlap in the detectable '0' states and '1' states. This indicates two problems when looking at the eye and constellation diagrams. First there will be two distinct eyes, one separating clear '1' to '0' transitions and no state transition, and a
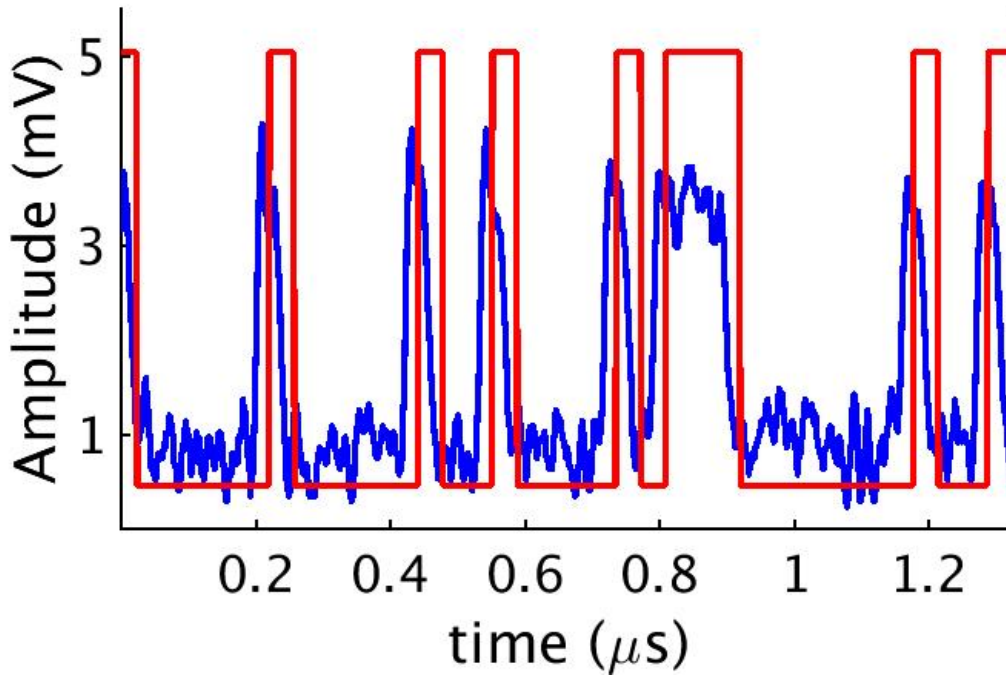
Figure 4.5: Raw waveform post mixing and amplification (blue), with expected binary decision (red)

second eye separation clear '0' to '1' transitions and no state transition. The second problem is the no-state-transition amplitude of 0 volts contains both binary decisions that should be decoded as '1', and binary decisions that should be decoded as '0'. In addition, the BER of the link here is estimated to be approximately 0.5 from the bathtub curve, since the total measured jitter is 4.99 symbols, and the width of the bathtub curve is less than 4.99 symbols for a 50% BER. This is where the M-CMA algorithm that was outlined in detail in chapter 3 comes in, which amplifies the '0' to '1' transitions, and records the decision history for a minimum of 16 symbols using the error correction code, which will allow both a clearer eye-diagram and a proper BER to be recorded.

After applying filters, difference blocks, and before we apply the final step of error correcting and sorting the no-state-transitions occurred into their respective '1' and '0' answers, if we plot the eye diagram (Figure 4.7) we can now see the split eye
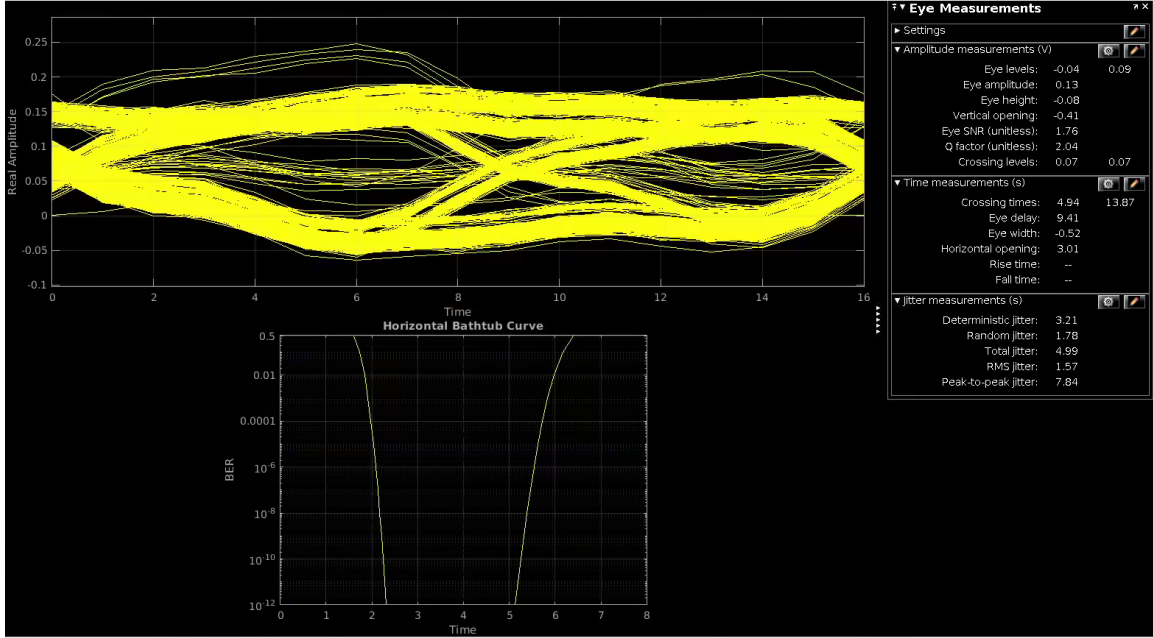
Figure 4.6: Eye Diagram of Raw LSK Signal pre-equalization

formation is now extremely distinct with two distinct eye amplitudes of greater than $0.6V$. Since there are still two openings, the physical eye-height calculation cannot be recorded until the final error correcting steps are taken, which will create a single eye-diagram.

Once we apply the final steps of the M-CMA algorithm, we arrive at the final eye formation in figure 4.8. From measuring the total jitter of the eye to be 4.88 symbols, we can estimate the BER from the corresponding bathtub curve to be approximately $1 * 10^{-9}$ using the Matlabs eye-diagram analysis tool based on the dual-Dirac Model [80].

Next, to show the state of the signal at various points of the M-CMA reconstruction algorithm, the constellation is depicted in figure 4.9. As can be seen in the figure, there are no clear binary states before any equalization steps (the green constellation), and after filtering (red) and thresholding following the M-CMA error function (blue), we can see distinct '1' and '0' states in the constellation.

For all of the eye-diagrams and constellation analysis, the LSK amplitudes used

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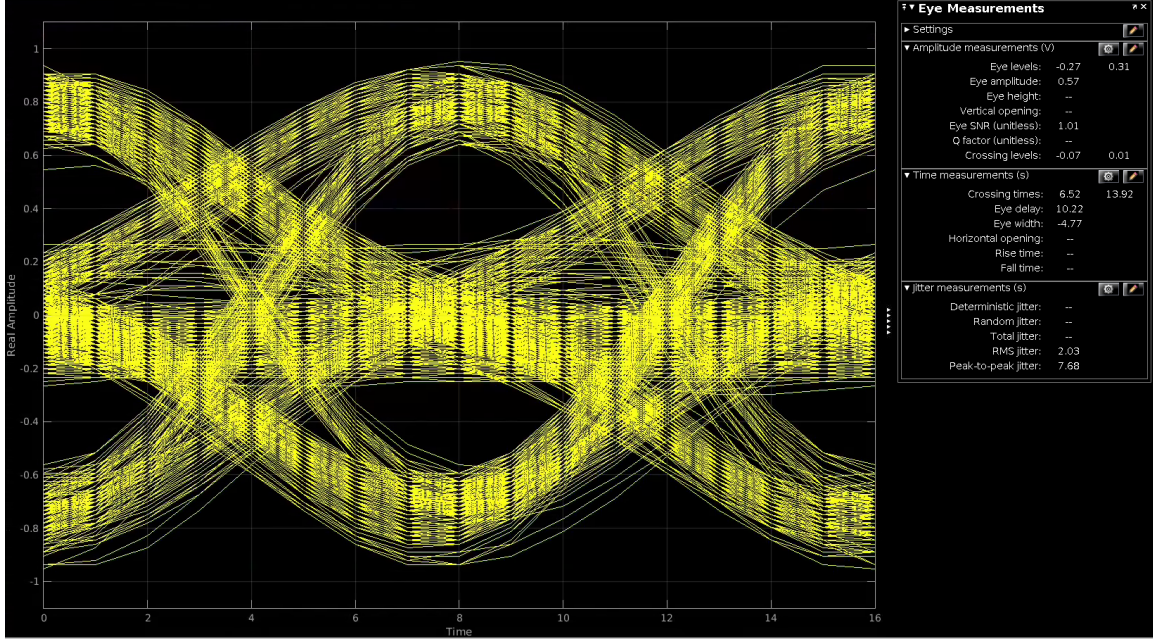
Figure 4.7: Eye Diagram mid M-CMA Equalization

for analysis are taken when the TX and RX data coils are perfectly aligned. To measure the decrease in LSK backscattering in non-ideal situations, various measurements were taken to wireless communications systems robustness to separation, misalignment, and dielectric environment. The raw LSK signal was recorded using the same $250\mu m$ spacers were used for the power transfer efficiency measurements. LSK waveforms for no misalignment, 0.5mm of misalignment, and 1.0mm of misalignment are depicted in figure 4.10a and the average RMS response vs misalignment is given in figure 4.10b. The difference in recovered LSK RMS amplitude is measured to be $16.1dB$ for 1mm of TX/RX misalignment.

For TX/RX separation, LSK waveform measurements were performed in increments of $250\mu m$ with the RMS amplitude of the response depicted in figures 4.11a and 4.11b. As can be seen in the RMS plot, the amount of transferred energy remains near 70mV until separation between TX and RX exceeds 0.4mm. While LSK reconstruction via M-CMA can still occur at both misalignment and separation of up to 0.75mm, the BER performance will be considerably worse than 10^{-9}.
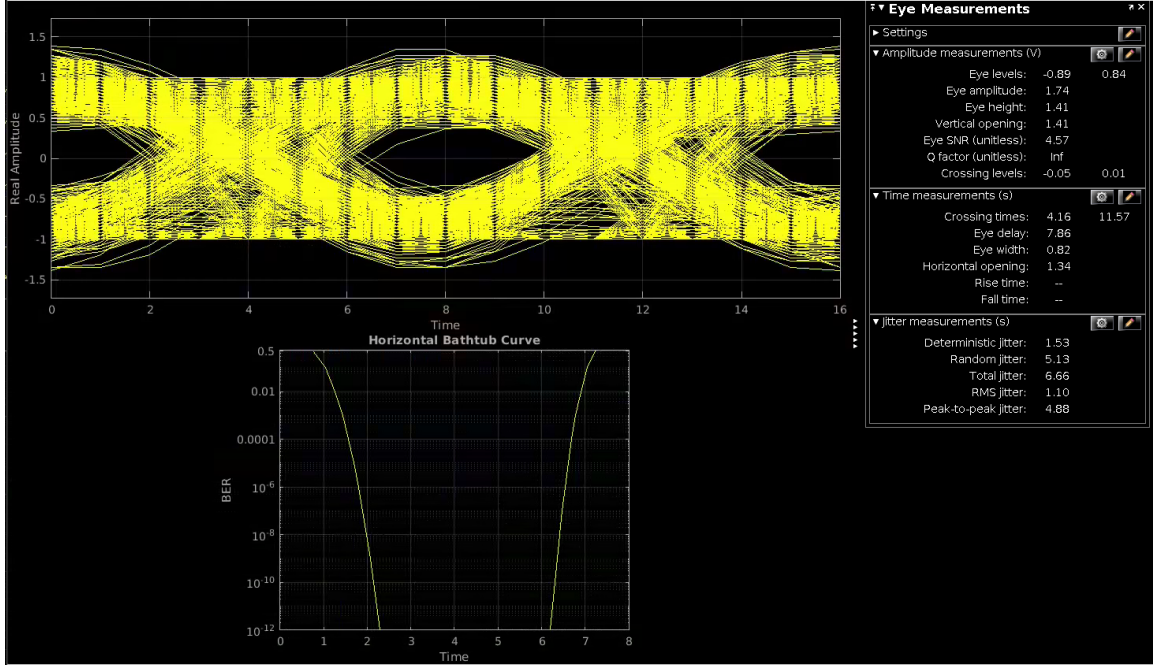
Figure 4.8: Eye Diagram post M-CMA Equalization

Finally, we measure the effects of biological tissues as a dielectric medium underneath the implant, as will be the required environment for the final application of a neural amplification system, by substituting air for skull and brain tissue in LSK noise measurements. The three dielectric environments measured with a $250\mu m$ separation between TX and RX consisting of lossy silicon substrate were air, skull from a mouse, and a skull with fixed brain tissue from a mouse. The results of these backscattering measurements in both raw waveforms, and a bar graph comparison of the RMS detected are depicted in figure 4.12. As is seen in figure 4.12b, the skull decreases the received backscattered signal by $-1.9dB$, and the brain/skull combination decreases the received signal by $-3.7dB$. These losses are acceptable, as they do not include the amplitude increase that is expected when the transceiver implant is thinned.
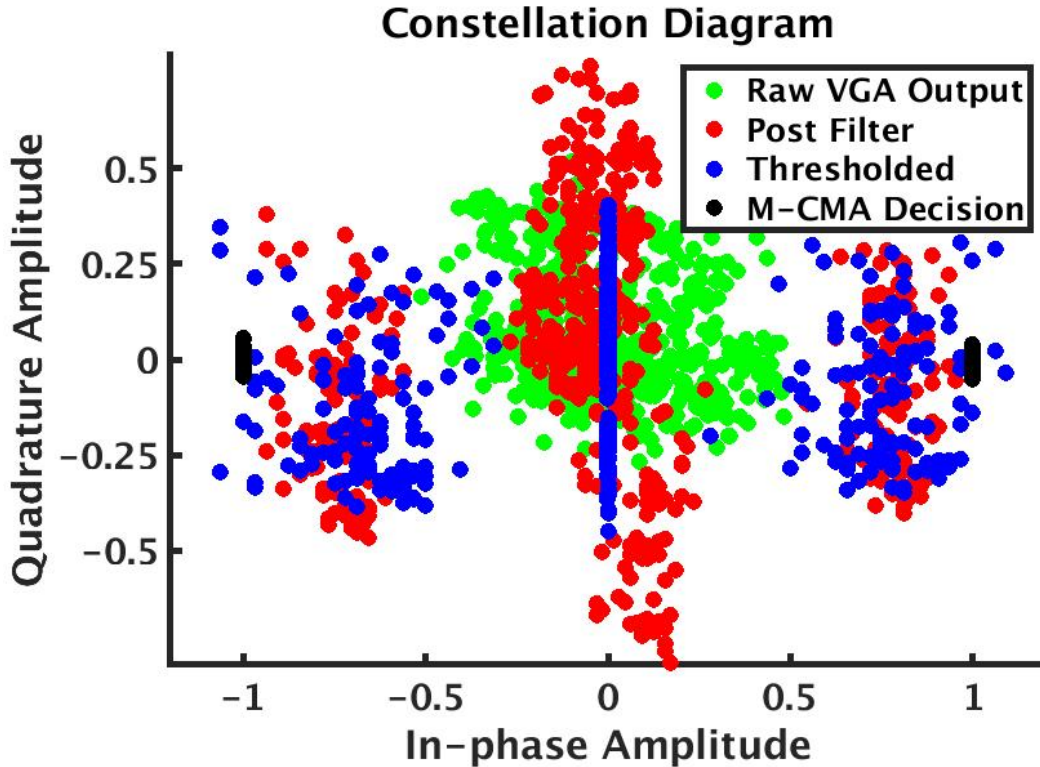
Figure 4.9: Constellation diagram at various stages of MCMA processing

4.2 Application Results: Neural Amplifier System

To test the transceiver in its intended application, in-vitro measurements were set-up to input sinusoidal waveforms into the front end amplifiers of the system. The method of in-vitro stimulation was to coat the open electrodes for each amplifier site to a conductive saline, PBS, and stimulate groups of sites in distinct wells. This measurement proved to be extremely problematic, as any coating of the coils with the conductive saline would immediately reduce the effective amplitude of any backscattered LSK to zero. To get around this physical problem, the 3D-printed alingner and interposer was also designed with 2 separate wells with a large block placed directly on top of the coils was used. This allows for stimulation of one side of the shank in 1-well, while the ground reference is placed in the 2nd well. Silver chloride electrodes

were then used to stimulate one well, while the other well was used as a ground reference. This in-vitro measurement process is depicted in figure 4.13. Using this set-up, input sinusoids ranging from input RMS amplitudes of $540\mu V$ to $5mV$ and from a frequency range of $10Hz - 3kHz$, which are used to characterize the neural amplification system.

With this setup, and using the python-based FPGA controller and M-CMA equalization system described in chapter 3, we are able to record data from all electrodes at $27Mbps$ in real-time. From these measurements we were able to record a gain of 35-37 dB from working sites at the minimum gain setting, 0000, and a gain of 51-56dB at the second lowest gain setting, 0010. The higher gain settings, 0100 and 1000 simply do not function properly and thus cannot be tested for gain, as the output voltages are stuck at the voltage rail for all input values. The measurements for the lower two gain values closely follow the expected peak gains from simulation of $43dB$ and $57dB$ respectively. The SNR was found to be between $-1dBc$ to $4dBc$ with a measured total harmonic distortion of $-12dBc$ to $-18dBc$ corresponding to approximately 20% THD. Measurements for gain, SNR, and THD are depicted in figure 4.14 for the gain setting of 0010.

Noise analysis for the amplifiers with no input at the electrode openings in air are depicted in figures 4.15, 4.16, and 4.17. As can be seen in 4.15, 254 of the 255 electrodes have a comparable input DC offset of approximately $1mV$ to $1.5mV$. The power spectral densities of the amplifiers are taken at the output of the SAR ADC, which explains why there are periodic zero-amplitude spikes that correspond to the quantization levels available at the output. For the maximum usable gain setting, the integrated quantization noise for the system is $5.9\mu V$. Using the additive noise model for quantized signals, which assumes gaussian white noise and quantization noise are uncorrelated and thus can be added by a Pythagorean sum, the quantization noise and measured integrated power spectral density yields the histogram results in 4.15,

with the top two plots representing output noise, the bottom plots showing input-referred noise, the left two plots showing the Gaussian contribution, and the right two plots including the quantization noise.

For approximately 200 of the 255 electrode sites, the quantization noise is the dominating factor, yielding a mean integrated noise of $6.12\mu V$ with a sigma of $0.37\mu V$. This value exceeds the steady-state input referred noise simulated during chip design by $3.5dB$, however this increase is expected since the steady-state simulation does not include the effect of noise folding. This noise analysis is within an order of magnitude to previously designed, however, does not match the performance of the state of the art, in particular when it comes to harmonic distortion [52, 73, 81–83].

4.3 Post Fabrication Thinning and Surgical Results

Repeating the RMS analysis on the received backscattered LSK signal at various post-processing stages, we can compare the effective recorded backscattered voltage for two fully processed shanks that are currently attached to guide shanks and glued with poly-ethylene-glycol (PEG), a pristine unprocessed die, and a thinned die that has not gone through trench etching that is approximately $30\mu m$ thick. The raw waveforms for those measurements are depicted in figure 4.18a and the RMS voltage for each system over several seconds of data transmission are depicted in figure 4.18b. As expected, the RMS value of the received LSK signal increases by approximately $3dB$ when compared to a pristine die from the foundry. This is expected behavior as we have removed the $250 - 300\mu m$ silicon substrate that was acting as a RF loss layer. In comparison to the power gain of only $1.1dB$ at 27MHz, the gains in the data TX/RX link are approximately 20% greater. For the fully processed shanks, we

would expect to see similar performance to this $30\mu m$ chip, however these shanks are still attached to both a lossy silicon guide shank and PEG, both of which will act as RF blockers and will reduce the received amplitude. The overall amplitude loss from these shanks compared to the baseline is $12dB$, which is a significant loss, but does not completely eliminate the ability to communicate with the probe. However, the expected BER will not approach $1*10^{-9}$ as that calculation assumed the 60mV LSK RMS response from the unprocessed die. It is also likely these shank measurements suffer from misalignment issues, as the 3D-interposer used for the unthinned tests is not compatible with a thinned die due to its fragility.

Post thinning, the chip die thicknesses ranged from $20 - 30\mu m$ depending upon thinning method, and all test circuitry and the bond pads have been cleaved off. At this thickness, the entire shank system volume encompasses only $0.08mm^3$. The die post-fabrication is depicted in figure 4.19. At this extremely small volume size, the die becomes physically difficult to handle and is at incredibly high risk of breaking along lattice weakness if improperly handled. In addition, the lack of a firm uniform substrate causes the stress and strain tensors from the BOEL stack-up to vastly differ from the $1\mu m$ box layer remaining on the back-side of the chip. As a result the die will "roll-up" if not carefully handled, or in this case, the rolling is offset by surface tension of water. To combat this, the processed probe is attached to a temporary and possibly dissolvable stiffener made out of PEG. The processed die still attached to this guide shank stiffener is depicted in figure 4.20 mid surgical insertion. To remove the implant from this stiffener, the PEG is dissolved with saline until the probe head separates from the stiffener, at which point the guide shank is slowly removed, leaving the implant inserted and now using the tissue to prevent curling. It is important to note that before communications with a thinned and implanted die, the power and data coils must not be coated with fluid, as it acts as a critical RF blocker.

For surgical insertion, the die and guide shank are attached to a mounting probe

using a vacuum system and micron-precise aligner. After insertion, the probe head is flattened against the surface of the brain and dried. To communicate with the surgically inserted probe, a 3D-printed transmitter interposer (depicted in figure 4.21) is used to position and align the implant to the external reader system with extremely little misalignment and a radius of separation less than $700\mu m$ in order to communicate with the implant. Figure 4.22 depicts the entire surgical process. On the left panel, the fully processed shank is seen attached to the guide shank system, the center-left panel shows the vacuum system used to hold and align the system, the center-right panels shows the slow insertion process into the brain, and finally the right panel shows the probe head flattened against the surface of the brain with the guide shank removed.

Full LSK communications were confirmed in-vivo for a thinned die without a formed shank using the same aligner methodology for the fully formed shank system. The experimental set-up for this in-vivo verification are depicted in figure 4.23 which shows the alignment of the thinned die, and figure 4.24, which shows the external transceiver aligned directly above the mouse skull during a live surgery.

The LSK blinking state during this surgical verification of transceiver operation can be seen on the scope channel output in figure 4.25, with the RMS analysis of this measurement previously shown on figure 4.18.
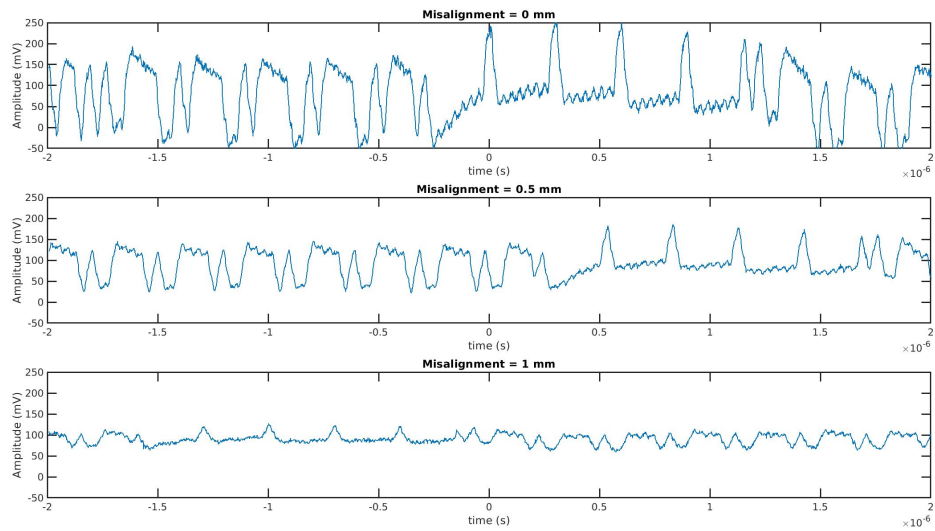
(a) LSK Waveforms at various alignment
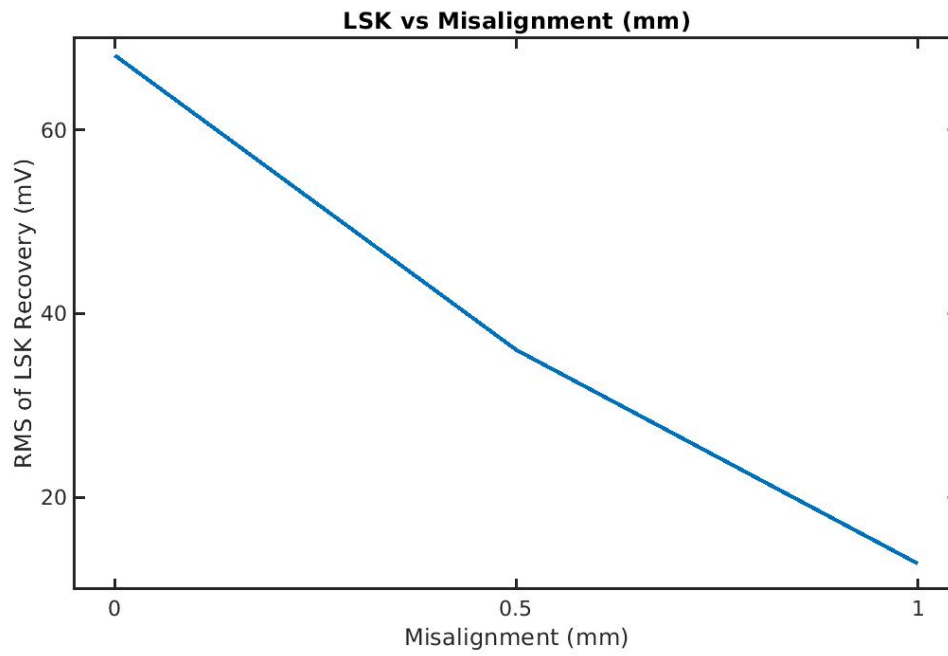
(b) LSK RMS vs alignment

Figure 4.10: Alignment effects on LSK
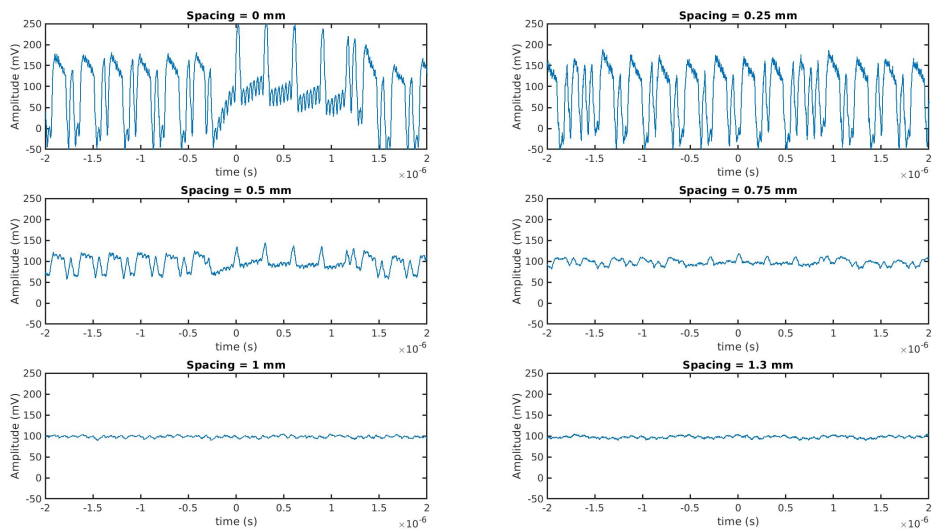
(a) LSK Waveforms at increased TX/RX radius
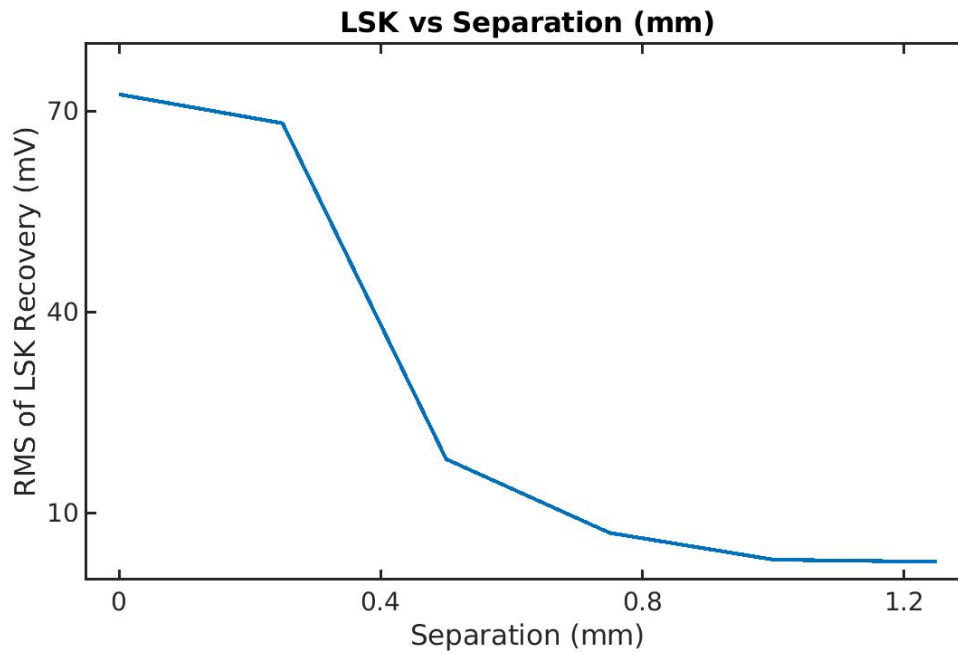
(b) RMS Amplitudes vs TX/RX Separation

Figure 4.11: TX/RX separation effects on LSK
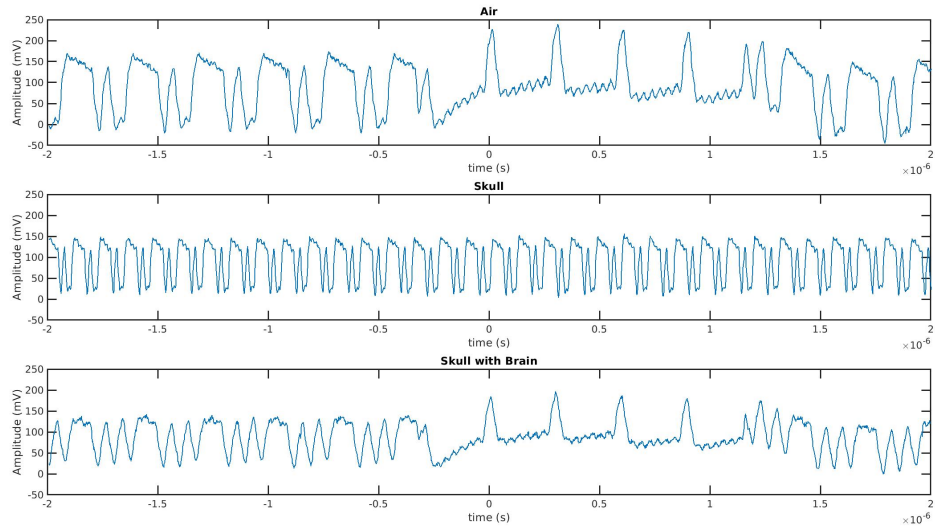
(a) LSK Waveforms at for different dielectric media
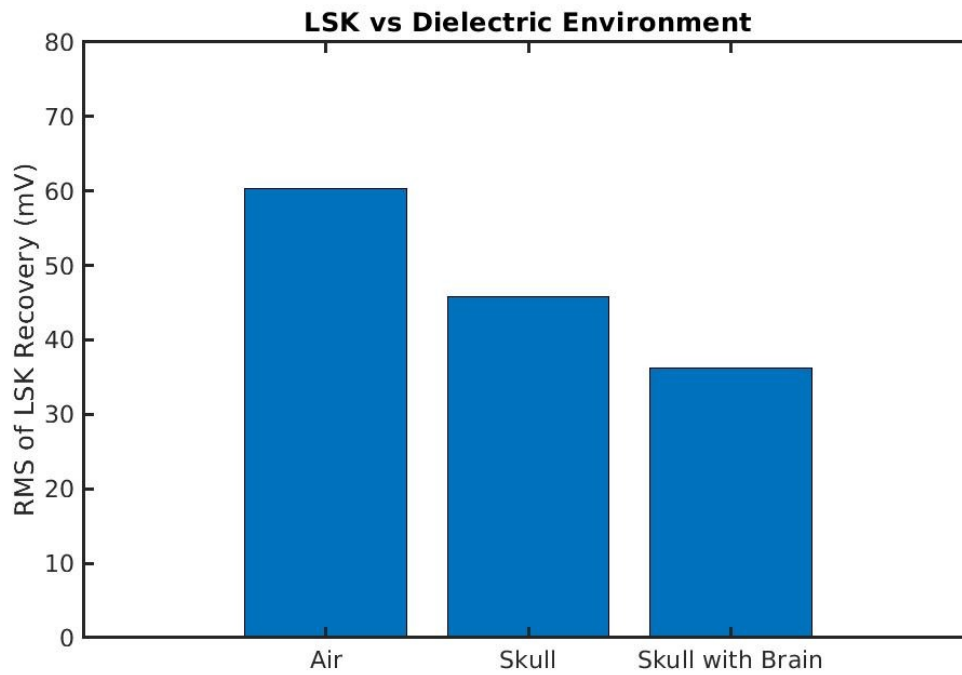
(b) RMS Amplitudes for biological dielectric media

Figure 4.12: LSK for different dielectric media
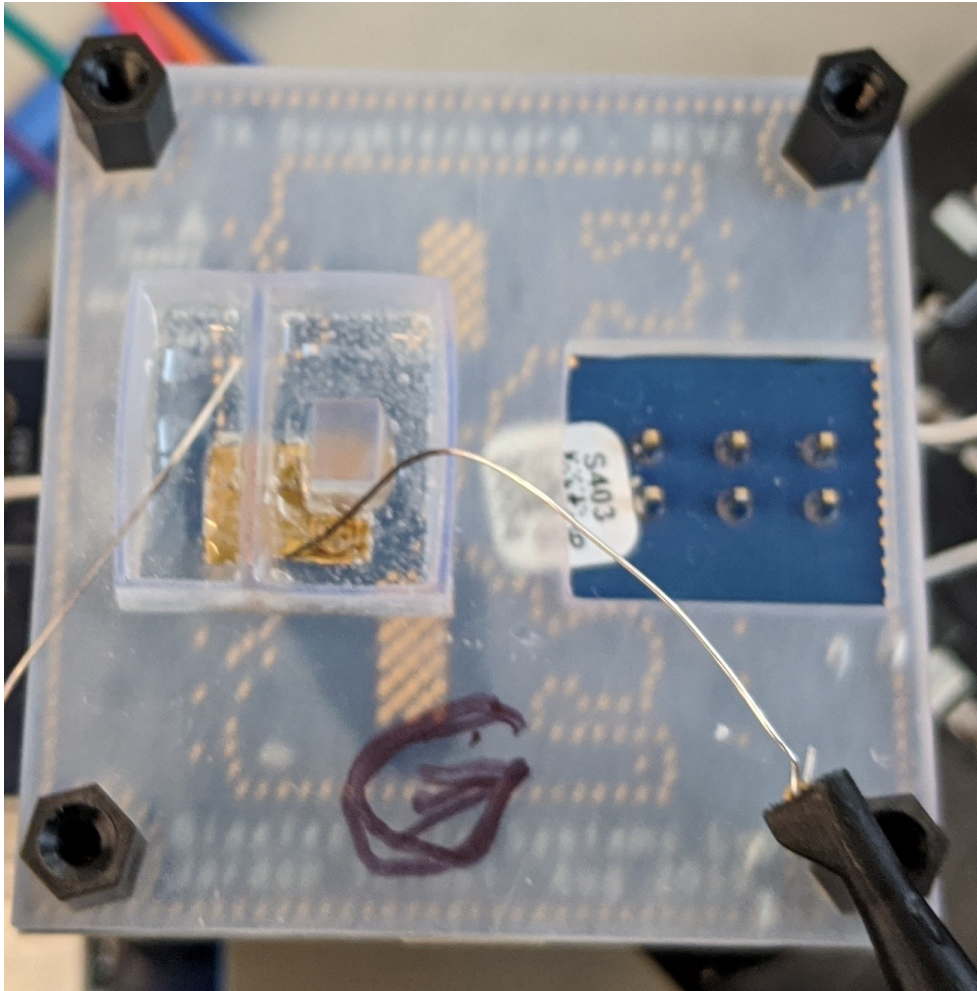
Figure 4.13: In-vitro measurement methodology
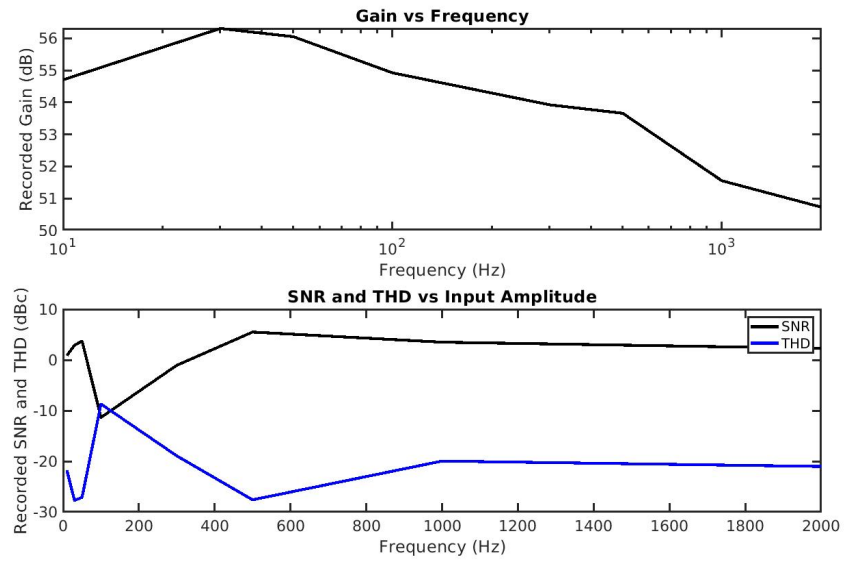
Figure 4.14: Measured SNR, THD, and Gain for Amplification System
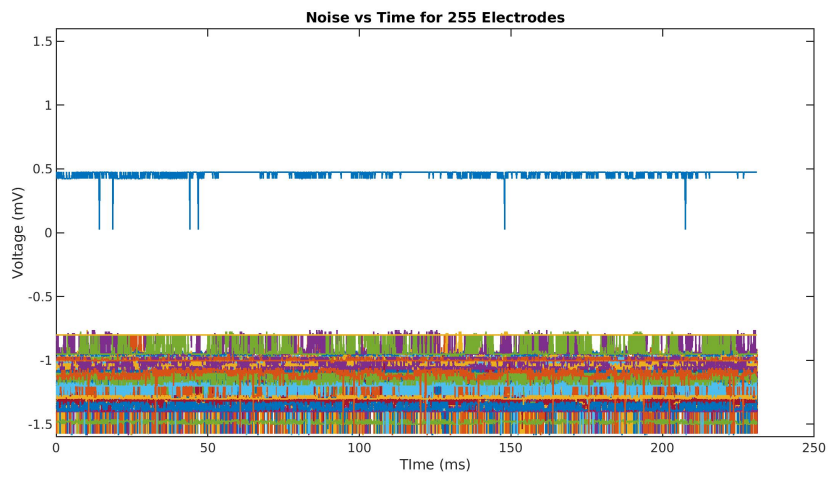
Figure 4.15: Input referred noise waveforms for all 255 electrodes

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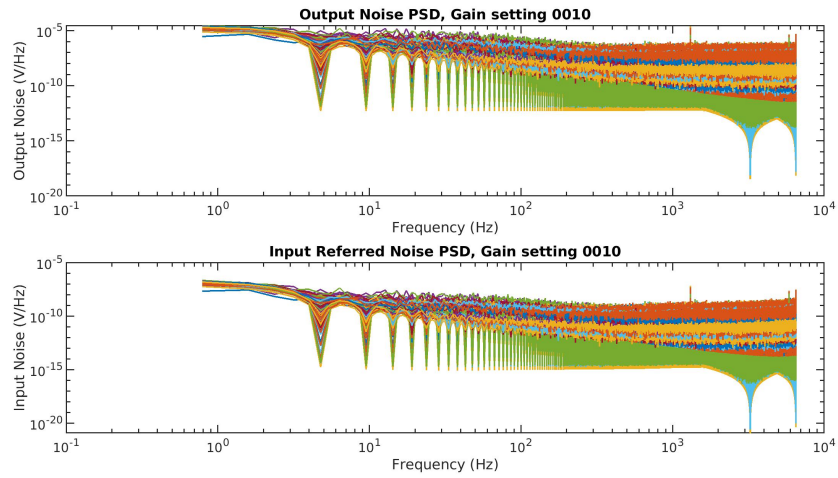
Figure 4.16: Input referred PSDs for all 255 electrodes
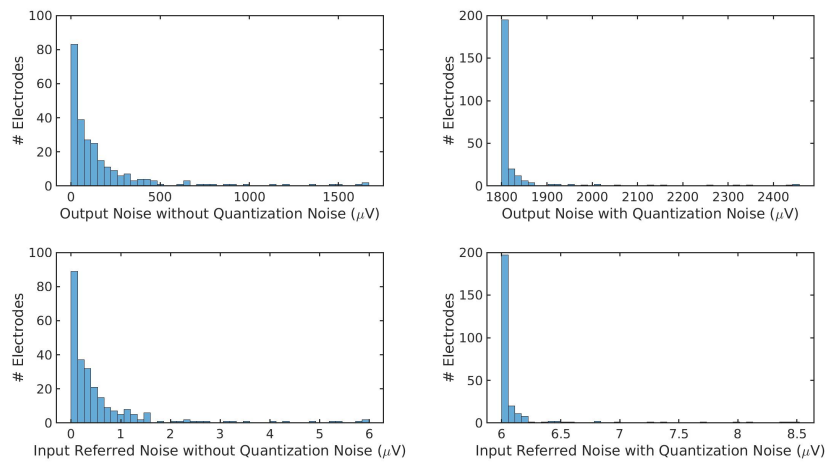
Figure 4.17: Noise histograms for all 255 electrodes
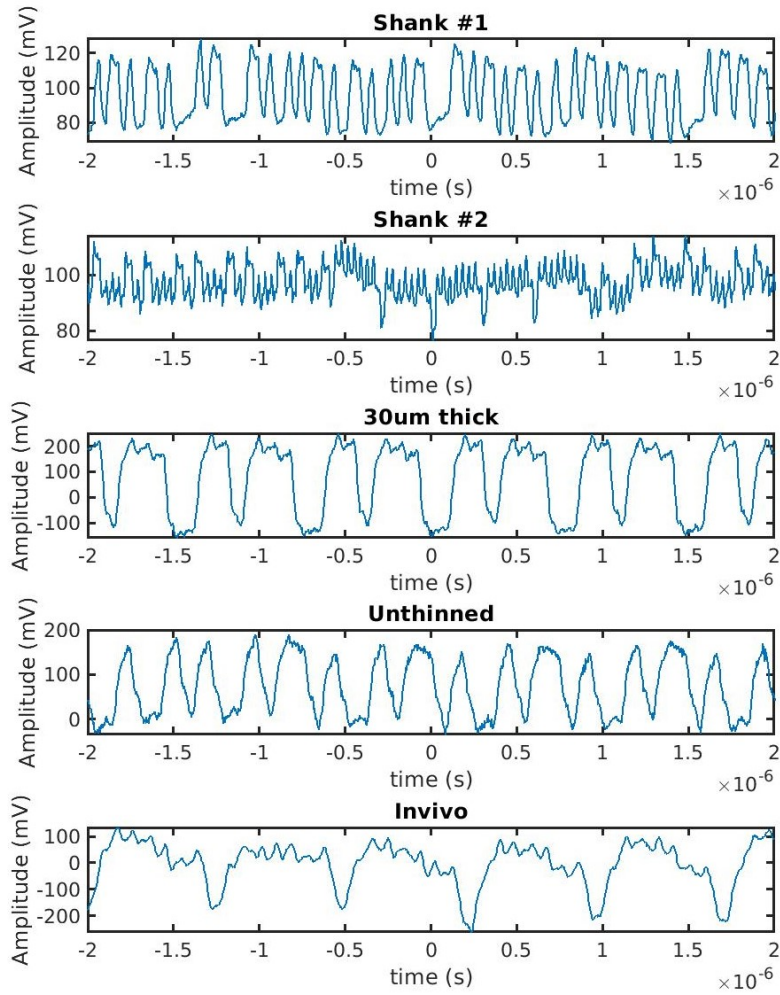
(a) Raw LSK response at various levels of chip processing
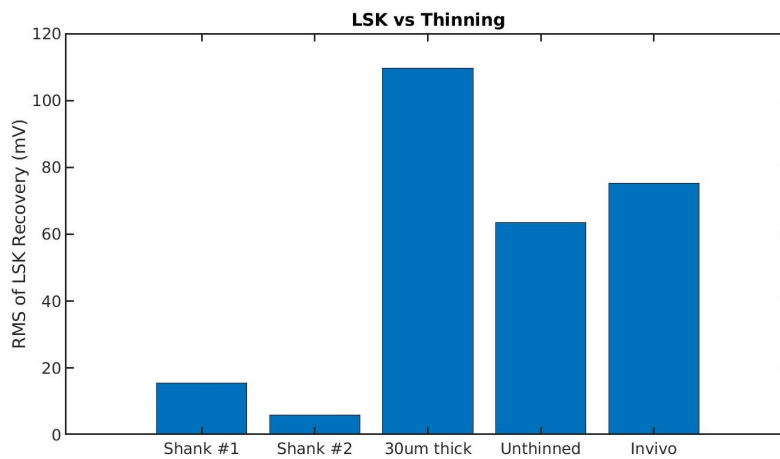
(b) RMS amplitudes at different process steps

Figure 4.18: Thinning and Processing effects on LSK

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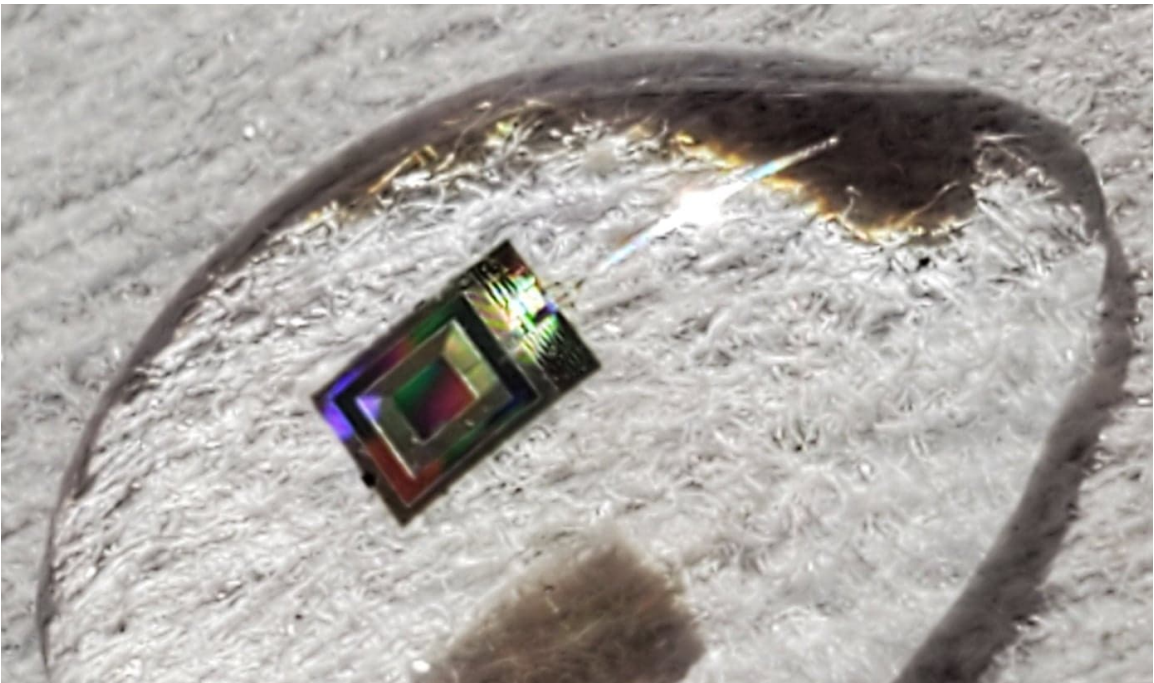
Figure 4.19: Fully processed implant
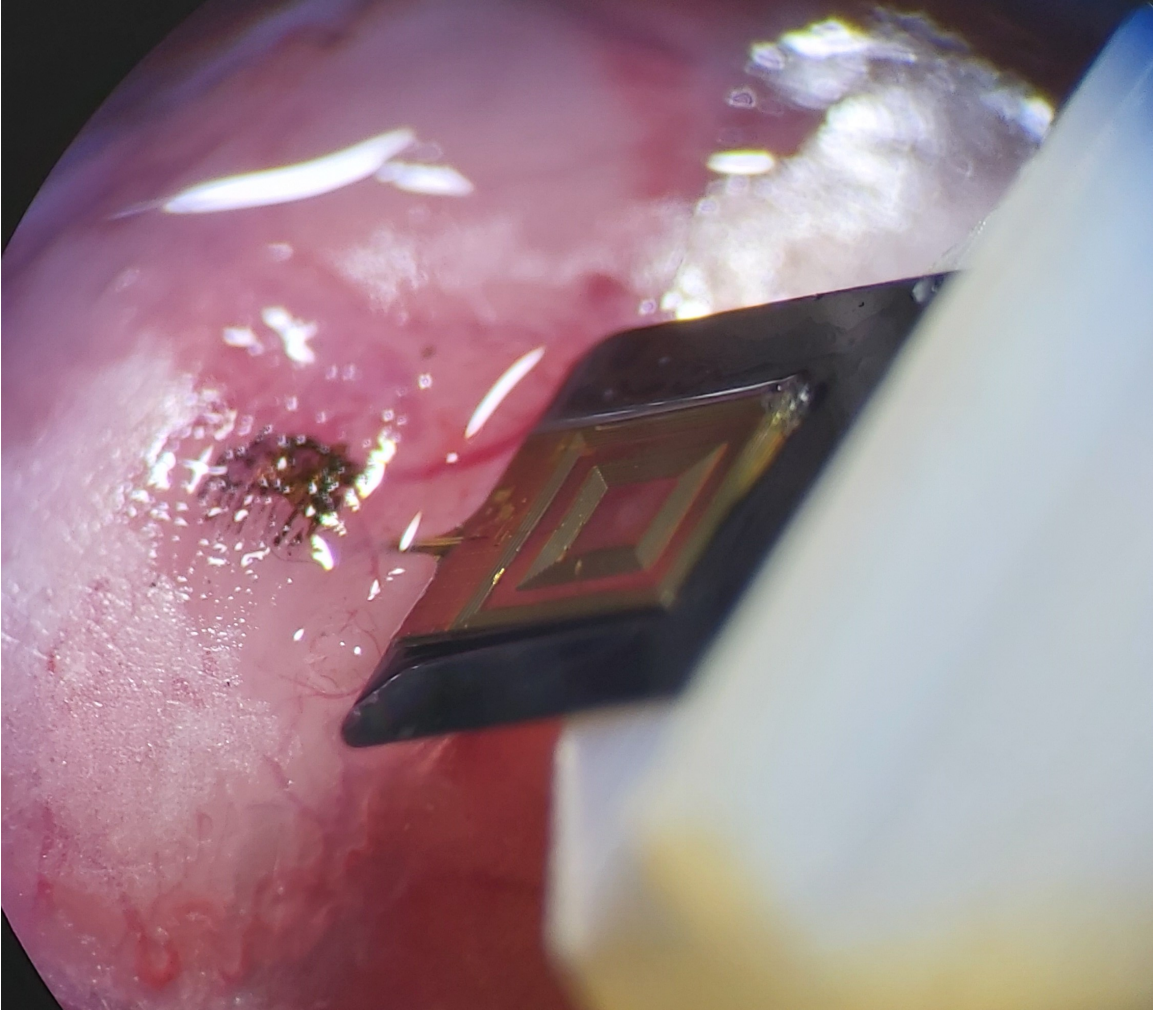
Figure 4.20: Implanted transceiver with guide shank mid insertion
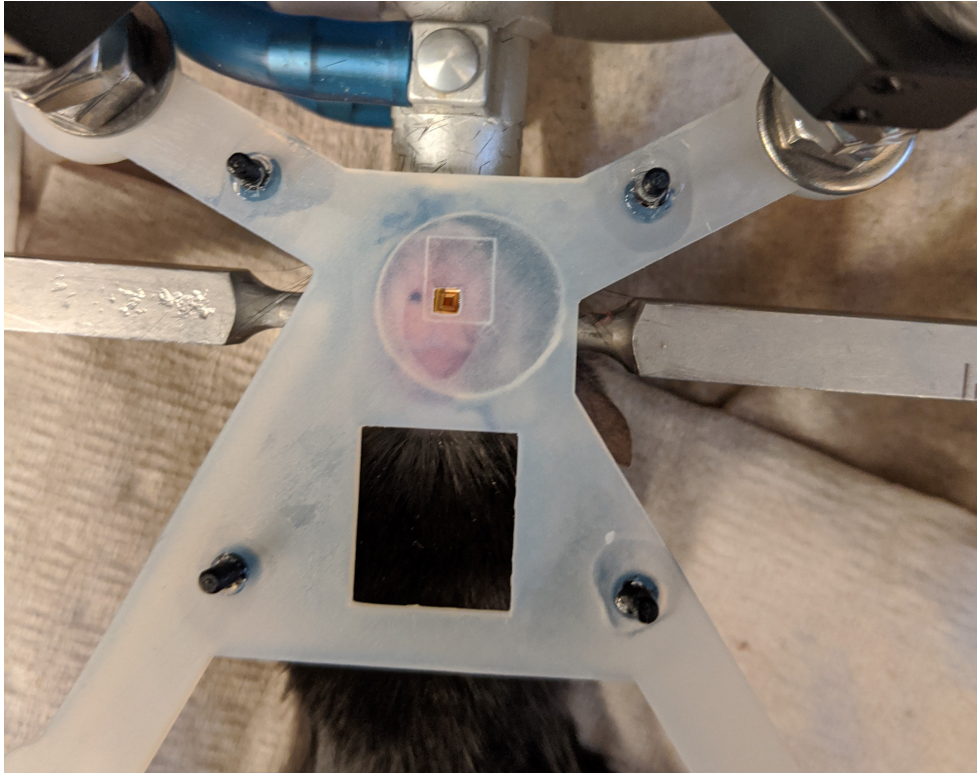
Figure 4.21: Interposer system for aligning inserted probe to reader system
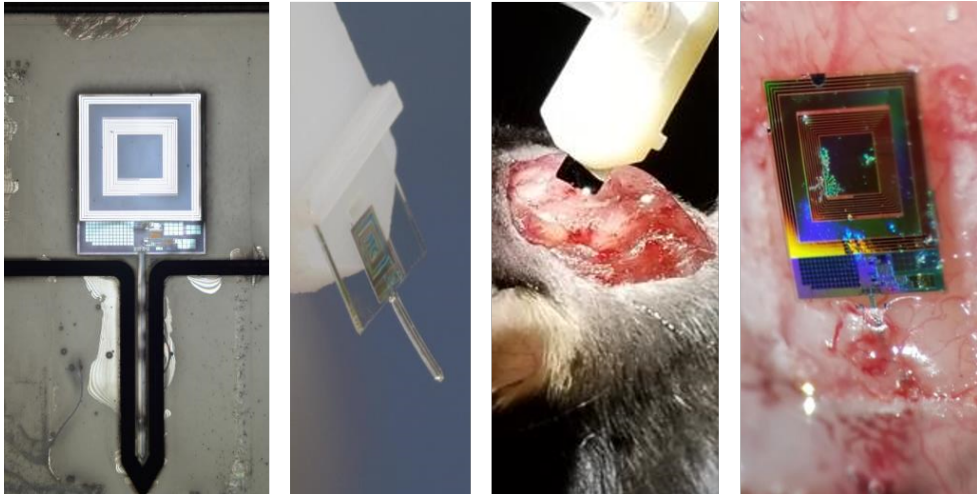
Figure 4.22: Surgical Insertion Process
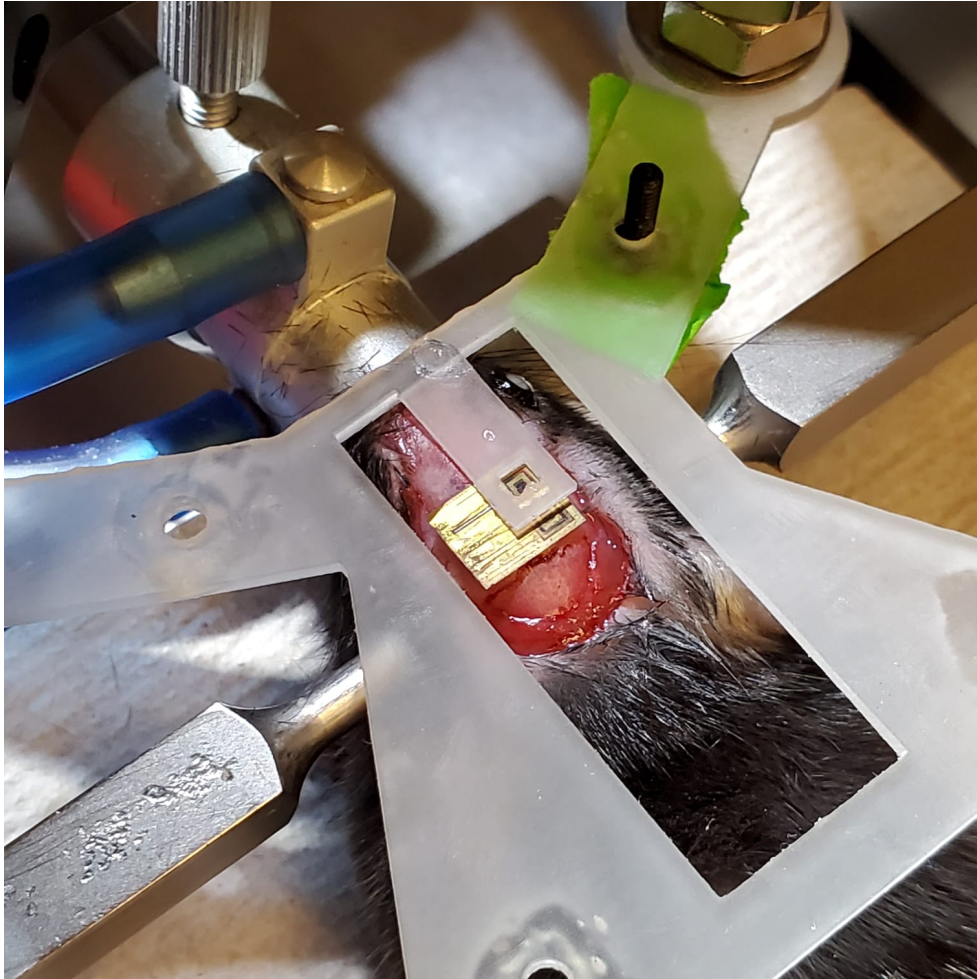
Figure 4.23: Thinned Die on surface of Mouse Brain
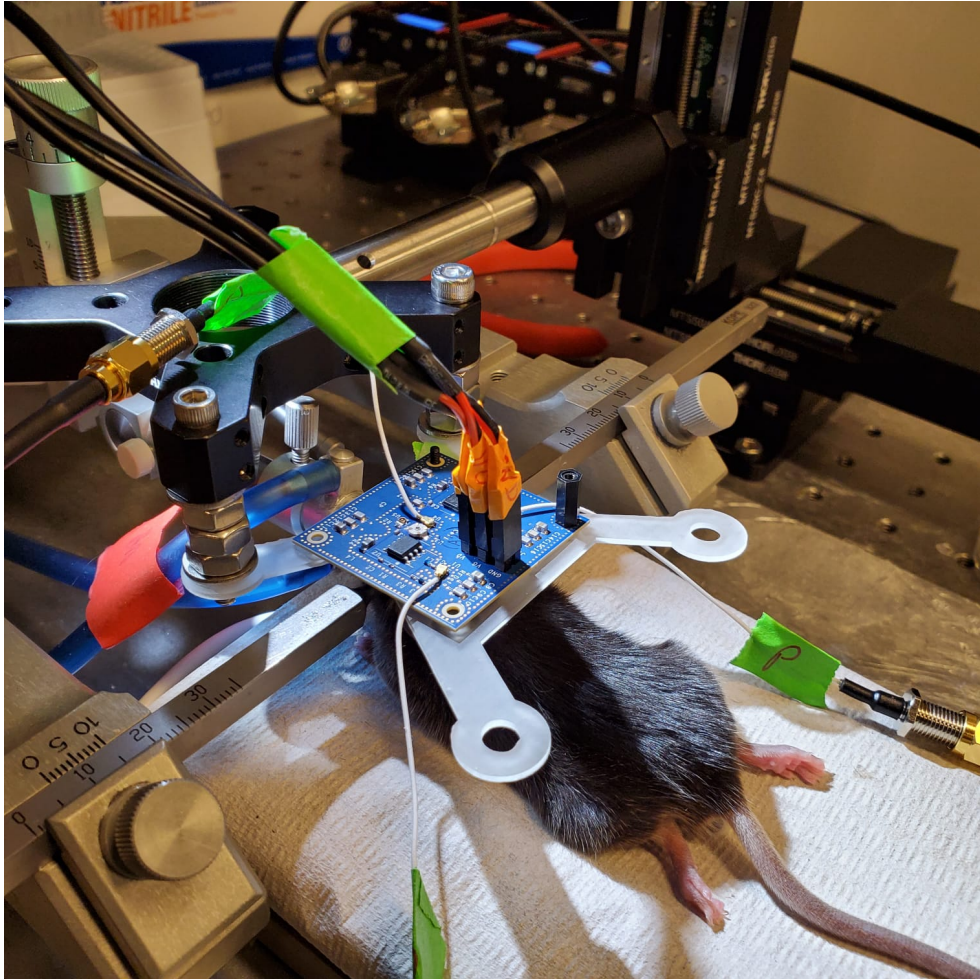
Figure 4.24: Transceiver Alignment Invivo
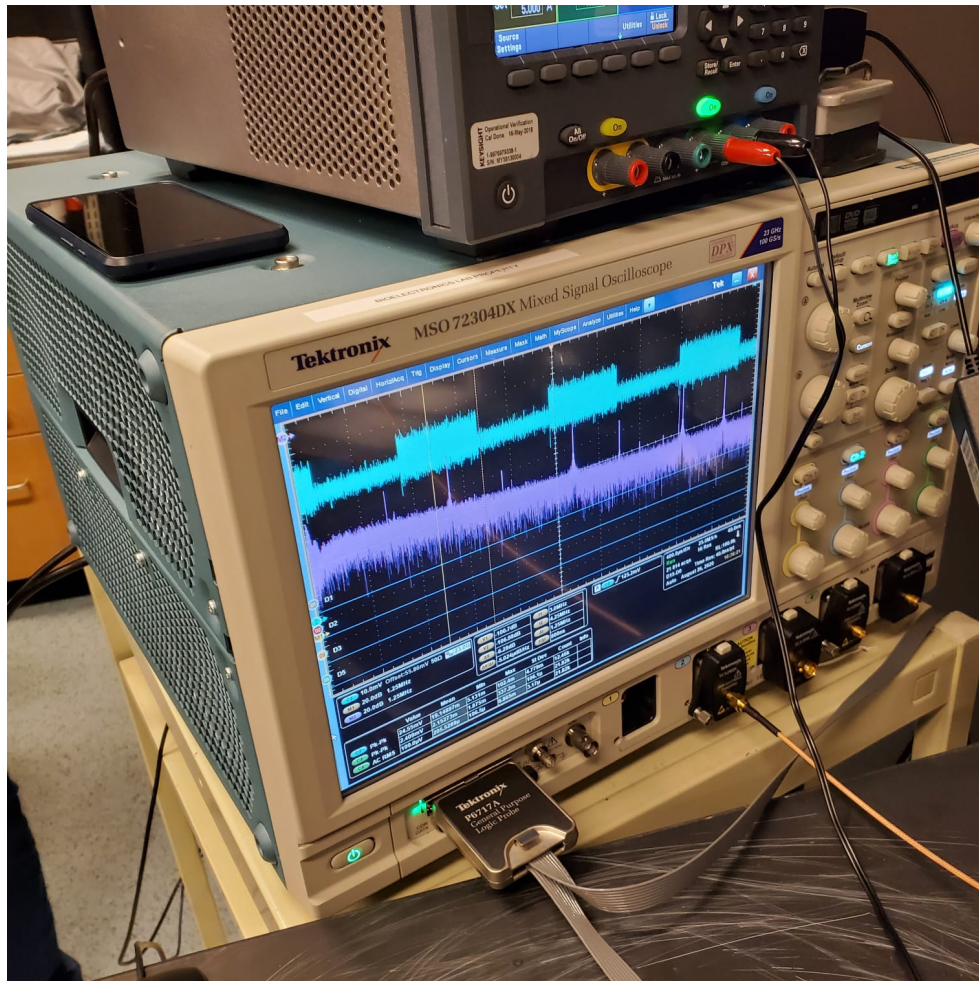
Figure 4.25: In-vivo LSK functionality

Chapter 5

Conclusions

5.1   Summary of Contributions

The designed ASIC transceiver with integrated antennas transmits backscatter LSK data at the highest data rate as opposed to previously published works [2, 84–86]. The power harvesting circuitry and power transfer efficiency is also competitive compared to other integrated coil systems [87, 88], but does not perform at the level of off-chip receivers. A summary of the IMD transceiver's performance compared to other similar systems for power harvesting performance and for data communications performance is given in table 5.1. Our system exceeds the data rate for other passive data modulation techniques, only trailing ultra-wide-band links which require both larger antenna systems and extremely power hungry power amplifiers to actively drive them at high frequencies and data rates [1–4, 6].

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Thinning of the ASIC has been confirmed to reduce the overall thickness of the die from approximately $300\mu m$ down to 20 to $30\mu m$, at which point the die is semi-translucent and quasi-flexible. Operation of the transceiver link has been verified for unthinned, thinned, shank-formed, and in an in-vivo dielectric environment implanted in the brain of a lab mouse. Transceiver operation for power transfer has been verified through 1 mm of gelatin phantom with power antenna PTE of 1.04% and 2.57% in air. Data downlink of all 16 valid ASK words has been verified in both unthinned and post-processed implants. LSK uplink at 27Mbps has been verified at a BER of <1x10-9, giving energy efficiency of 103pJ/bit for 2.7mW of transceiver power. Compared with other wireless IMDs that use near-field inductive links, this wireless shank system achieves significantly higher data rates using LSK backscattering. Our data rate is within an order of magnitude of systems utilizing UWB without the power cost of an on-chip power amplifier system or the size of large antenna. While the use of an on-chip inductor does decrease transmission radius, it reduces the volumetric form factor by several orders of magnitude when compared to previously published wireless implantable devices [1–4, 6]. This trade-off is advantageous for links where high data rate and extremely small volumetric form factors are prioritized over system efficiency. For table 5.1, since coils were implemented off-chip for the other implants, volume was calculated assuming the implant coils constituted a majority of the other system's volumes, and were implemented using an ultra-thin flex PCB board with a thickness of $220\mu m$. This large volume decrease makes integrated Rx coils an attractive option for the designed implantation application of neural recording in small rodents. A summary of this transceiver performance results can be seen at [89].

For the application in neural recording, the front end amplification system has worse noise performance with fewer ADC bits. In terms of overall number of concurrent recorded sites and data rate, this system performs well, but this increase in concurrent sites creates the noise folding problem. In addition, in comparison to very

	[1]	[4]	[2]	[3]	[6]	This Work
$PowerCarrier(MHz)$	13.56	13.56	13.56	309	-	27
$DataCarrier(MHz)$	13.56	13.56	50	309	3000-5000	700
$ModulationType$	$COOK$	$PPSK$	PDM	LSK	$UWB\text{-}OOK$	LSK
$DataRate(Mbps)$	6.78	1.35	13.56	$2GHz$	67	27
$PowerDelivered(mW)$	6.3	100	42	0.79	-	4.2
$ImplantVolume(mm_3)$	380	5	45	9.3	-	0.08
$TX/RXpower(pJ/bit)$	9.5/-	-	960/162	-/395	30/-	-/103
$Technology(nm)$	65	600	350	65	90	180
$Separation(mm)$	35	5-15	10	10	500-4000	0.5-2.5
BER	9.9^{-8}	6^{-8}	4.3^{-7}	1^{-6}	1^{-8}	$>1^{-9}$

Table 5.1: Comparison to other implantable transceivers

recent systems, the total site count is lower, but that is a consequence of integrating the entire system with a small area on the head of the shank. In other systems, the entirety of the connected die is used for amplification, data converters, and control systems. For our system, less than $1m^2$ is available for the amplifier system and multiplexing, since a majority of the chip's area is dedicated to the transceiver. A table highlighting our system application performance compared to other neural recording systems with shanks is given in 5.2. While our noise level may seem comparable, it does not capture the full bandwidth out to 10kHz, due to the 12.9kS/s sampling limitation.

	[53]	[52]	[73]	This Work
$Electrodes$	144	966	1356	256
$ConcurrentSites$	144	384	678	256
$Power/Channel(\mu W)$	46.29	49	45	52
$InputNoise(\mu V_{RMS})$	13.43	6.36	12.4	6.12
$PixelPitch(\mu m)$	70	20	22.5	25
$ADCBits$	11	10	10	8
$SampleRate(kS/s/Ch)$	30	30	20	12.9

Table 5.2: Comparison to Shank Systems

5.2 Proposed Changes for Future Iterations

5.2.1 Wireless Transceiver

To truly create a fully integrated ASIC IMD with both a proper transceiver and front end for a neural recording system, a variety of changes would need to be made to in the ASIC design. From the transceiver side, currently the data-communications protocol is both custom to this system and overly simplified in the actual handshaking between transmitter and receiver. As a result, a custom reader system is required to communicate with the probe as opposed to using a more standardized handshaking protocol typically used in RFID systems in the $10 + MHz$ range. A more complex handshaking routine between external reader and implant would also allow for more precisely tunable functionality to be implemented, primarily with a data sequence that could use an on-chip AC amplitude monitoring circuitry to either request a larger power input signal, or to increase or decrease the data carrier for backscattering. In both instances, this communication would allow for automatic gain control blocks to be more easily implemented on the reader side, requiring less user input for robust communications. If a larger area budget could be allowed, the replacement of a single data coil with passive-backscattering could be replaced with multiple inductors spaced at least 1mm away from each other on the chip surface. Since the LSK tolerance to alignment must be less than 1mm anyway, it would be possible to implement two parallel LSK receivers with minimal coupling between the pair. Each coil could also be tuned to unique resonance frequencies, which would diminish cross-talk between the links even farther.

5.2.2 Neural Recording Systems

The intended application space for the designed ASIC IMD with integrated transceiver is for neural recording and stimulation systems in the brain of mice. The mouse brain is very small, and the typical mouse skull thickness is thin enough that the transceiver can still be in range for communications if the implant transceiver is floating on the surface of the mouse's brain. The extremely small volume displacement from the ASIC's thinning is also desirable for this application.

For a redesign of the shank system, a much lower input referred noise value could be obtained in the amplifier chain was redesigned to either remove time-multiplexing entirely through the use of a single-bit quantizer in each pixel, or by limiting the time multiplexing site ratio to less than 20, and compensate with parallelization of both the final stage of the amplifier and ADC. The chip area encompassed by the neural amplifier and ADC could fit inside the 2mm x 2mm space inside the power coil with a minimum of 16 copies. Electromagnetic simulations would need to be performed to see if the circuit performance drop caused by active circuitry being placed directly under the active antennas outweighs the large parallelization of the amplifier and ADC block, but the optimal number is likely greater than one now seeing the terrible effects of noise folding. By adding the ability to only sub-sample a section of the entire shank, a greater sampling frequency could also be used, which would allow for a switch between low bandwidth measurements of many sites, or high-bandwidth measurements of a few sites.

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