SIMULATION OF AN SP8T 18 GHZ RF SWITCH USING SMT PIN DIODES

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TITLE: Simulation of an SP8T 18 GHz RF Switch Using SMT PIN Diodes

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ABSTRACT

Simulation of an SP8T 18 GHz RF Switch Using SMT PIN Diodes

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Radio frequency (RF) and microwave switches are widely used in several different applications including radar, measurement systems, telecommunications, and other areas. An RF switch can control a radar's transmit vs. receive mode, select the operating band, or direct an RF signal to different paths.

In this study, a single pole eight throw (SP8T) switch using only Surface Mount (SMT) components is designed and simulated in Keysight's Advanced Design System (ADS). Single pole eight throw is defined as one input and eight possible outputs. A star network configuration with series-shunt PIN diode switches is used to create the 8-way RF switch. There are other commercially available SP8T switches from MACOM, Skyworks, Analog Devices, and other vendors that operate around this bandwidth. However, this design uses SMT components and series-shunt diode configurations to create a device in the GHz range and power handling in the high 20 to 30 dBm range.

This study modeled components in ADS, including the PIN diodes and the bias tees. The project also analyzed multiple layouts, finalizing the optimal design to meet specifications. The insertion loss, bandwidth, isolation, return loss, power handling, and switching speed are analyzed in the final design.

Key specifications for this design are determined by comparing to other commercially available SP4T and SP8T switches from MACOM, Skyworks, Analog Devices, and other vendors, as well as developing an operational switch over the 2-18 GHz bandwidth. Additional specifications include limiting insertion loss to 2.0 dB maximum

and maximizing isolation to 30 dB minimum. Switching speed and power handling specifications are also set to 20 ns and 23 dBm, respectively.

Future projects will work on design fabrication and improvements to the manufactured switch.

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Chapter 1

INTRODUCTION

Switches are one of the oldest and most commonly used electronic devices, used in a variety of different applications to change the connection path of a signal. It essentially disconnects or connects one port from or to another, either disabling electrical current or redirecting current to another port.

Electrical switches became a part of electronics concurrently with the invention of electricity. As technology progressed, and higher frequencies became more utilized, a need for effective RF and microwave switches arose. Many applications require switching the RF signal path to route and connect to different antennas, filters, amplifiers, and other devices. With the growth and development of wireless communication, high-speed data networks and other advanced technologies, such as switchable band-pass filters, the need for high performance switching devices is increasing.

Since these switches must work up to the gigahertz region and higher, nothing about them is simple: their design, their underlying technology, the layout on the PC board, matching their performance to the application priorities, as well as several other factors must be considered.

1.1 Microwave Switch Types

RF and microwave switches can be categorized into two main groups:

- Electromechanical Switches
- Solid State Switches

The first RF switches used in wireless applications were mechanical switches, such as keys, aerial switches, and electromechanical relays. They require a good electrical contact and the use of high isolation materials. With these conditions, electromechanical switches can provide a low insertion loss, high isolation, high power handling, and a frequency range starting at DC. However, electromechanical RF switches have a low operating lifetime at around one million cycles. The operating life of an electromechanical switch can be defined as the number of cycles the switch will complete while meeting all of the RF and repeatability specifications. The operating life refers to the electrical life and RF properties of the switch, and not to the mechanical life, which is much longer. While they might not fail mechanically, their insertion loss increases due to the increasing contact resistance over time.

Solid state RF switches, which use diodes or transistors, are more reliable, exhibiting an infinite lifetime due to their superior resistance to shock, vibration, and mechanical wear. They also offer a faster switching time, down into the low ns range. However, the higher ON resistance of the solid-state switches gives them higher insertion loss at approximately 1 dB as oppose to electromechanical switches at 0.1 dB.

There are a few main types of solid-state RF switches:

- PIN diode RF switches
- Field Effect Transistors (FET) RF switches
- Hybrid (FET and PIN diode) RF switches

A comparison between all the different types of switches is shown in Table 1.1 below [16].

Table 1.1: RF Switch Performance

	PIN DIODE	FET	HYBRID	ELECTRO-MECHANICAL SWITCHES
FREQUENCY RANGE	100 MHz to >50 GHz	DC to >20 GHz	300 kHz to >20 GHz	DC to >40 GHz
INSERTION LOSS	Medium (Decreases at low frequencies)	High (Decreases at high frequencies)	High (Decreases at high frequencies)	Low
ISOLATION	Good at high frequencies	Good at low frequencies	Good at high frequencies	Good across broad frequency range
REPEATABILITY	Excellent	Excellent	Excellent	Good
SWITCHING SPEED	Fast	Average	Average	Slow
POWER HANDLING	Low	Low	Low	High
OPERATING LIFE	High	High	High	Medium
POWER CONSUMPTION	High	Low	Moderate	Moderate (use current interrupt)
SENSITIVE TO	RF power overstress, temperature	RF power overstress, temperature	RF power overstress, temperature	Vibration

1.2 Outline of Thesis

Chapter 2 describes PIN diode theory and RF switch applications. A sub-section compares transmission lines considered in this design.

Chapter 3 outlines SP8T design methods and switch construction. This includes:

- component selection for both the PIN diode as well as the bias tee.
- substrate selection, analyzing the substrate width, dielectric constant, and trade offs with the transmission line.
- transmission line selection, observing the transmission line width and performance
- star configuration, how the lines are laid out on the board to maximize performance
- bias voltage values to properly drive the PIN diode

Chapter 4 shows the simulation results of the overall performance of the design. This includes isolation and insertion loss, power handling, switching speed, as well as a sensitivity analysis to determine robustness of the design and PIN diode model..

Chapter 5 provides a brief conclusion about this thesis study.

Chapter 6 lays out future work to manufacture the design, testing several different aspects of the design with laboratory equipment, and eventually designing a second iteration of the switch to improve on any imperfections found during testing.

Chapter 2

BACKGROUND

This design employs an approach using series-shunt PIN diodes configured in a star network, where multiple input/output branches connect to the same node, to reach the desired response of the SP8T switch. This chapter will explain the background necessary to fully understand how this switch works, including PIN diode fundamentals and RF switch application advantages, basic PIN diode switch topologies, as well as the transmission lines considered for this design.

2.1 PIN Diode Fundamentals

A PIN diode is similar to the conventional PN diode, allowing current to flow through it in one direction when it is forward biased. When reverse biased, no current flows. This diode functionality is employed in several applications spanning DC to RF.

However, the PIN diode differs from the conventional PN diode because it has an "intrinsic" layer between the P and N layers, as seen in Figure 2.1. The physics of the PIN diode are quite complex, but the result is essentially a controllable switch. When the PIN diode is forward biased, RF energy flows through the diode even when the signal drops below zero volts. When reverse biased, the diode blocks RF energy. This is the basis for using the PIN diode in a wide variety of RF switch topologies and will be explained further in this chapter.

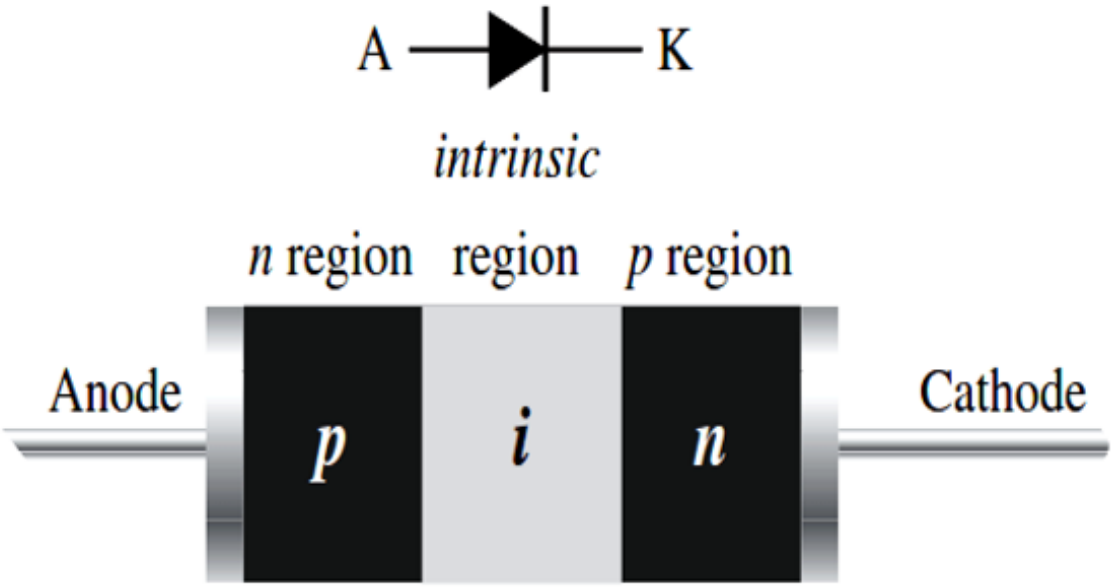

Figure 2.1: PIN Diode Symbol. Note that there is the extra undoped intrinsic region in between the P and N region.

A few simple models are applied to explain PIN diode operation. When forward biased, the PIN diode behaves like a resistor and inductor in series. When reverse biased, the diode behaves like an inductor in series with a parallel RC. These simple models are shown in Figure 2.2, where R_s is the diode resistance when forward biased, L is the parasitic inductance (package dependent), C_T is the sum of the diode junction capacitance and the package parasitic capacitance and R_p is the diode resistance when reverse biased. Assuming a low R_s and C_T value to make their impedance low and high (values dependent on application), respectively, at the device frequency, this makes this PIN diode ideal for switching applications [6]. When forward biased it has an impedance Z = R, near to a short circuit. When reverse biased it has an impedance Z = $\frac{1}{\omega C}$, near to an open circuit.

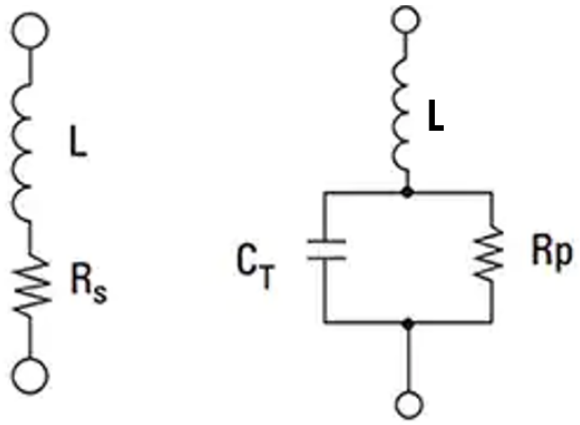

Figure 2.2: PIN Diode Model. Left: forward biased, series RL. Right: reverse biased, series L with parallel RC.

As stated before, PIN diodes mainly have two states: forward bias, when a positive voltage is applied at the anode of the diode, and reverse bias, when a negative voltage is applied at the anode of the diode. When the PIN diode is under forward bias, charges are injected into the I-region. These electrons and holes move across the I-region but eventually are recombined with another electron or hole. The average time that this takes is called carrier lifetime, τ. This results in an average charge Q to be stored in the I-region, lowering the diode resistance to a nearly short circuit equivalent. When the PIN diode is under reverse bias, there is no charge stored in the I-region. The PIN diode now behaves like a capacitor in parallel with a high ($\sim$MOhms) parasitic resistance. The PIN diodes are specified with the following parameters:

- C_T (Farads): total capacitance at reverse bias
- R_p (Ohms): parallel resistance at reverse bias
- V_r (Volts): maximum allowed reverse bias voltage
- R_s (Ohms): series resistance when forward biased

- τ (sec): carrier lifetime
- Θav (Ohms): average thermal resistance
- P_D (W): maximum average power dissipation
- W (mil): intrinsic region width

A PIN diode behaves like a regular PN diode at low frequencies ($\sim$MHz). This low frequency operation of the PIN diode to pass signals through depends on the I-region width and carrier lifetime. A wider I-region or a longer carrier lifetime leads to more carriers in the I-region and a longer time for the carriers to dissipate, meaning a lower frequency operation point. This stored charge is related to the forward bias current, I_f (A), and the carrier lifetime, τ (s), as:

$$Q = \tau I_F \quad (Coulombs) \tag{2.1}$$

2.1.1 Large Signal Model

PIN diodes only work down to a few tens of MHz due to the added I-region and carrier lifetime. At frequencies below this frequency, a PIN diode acts like a rectifier, meaning any negative component of the signal is cut off.

If an AC signal is input to a device and the user wants the full signal to pass through, a significant issue arises. The AC signal forces the diode into reverse bias, blocking the input. However, at microwave frequencies, the PIN diode behaves like a resistor throughout the entirety of the signal due to the charges in the I-region.

The resistance value is determined by the level of DC current that is present in the I-region, which is determined by the thickness of the I-region. The PIN diode is a

DC-controlled RF resistor. Additionally, if no DC current is present, the PIN diode behaves like an open circuit [18]. The PIN diode behavior at 1 kHz, 1 MHz, and 1 GHz is checked in simulation using the schematic shown in Figure 2.3.

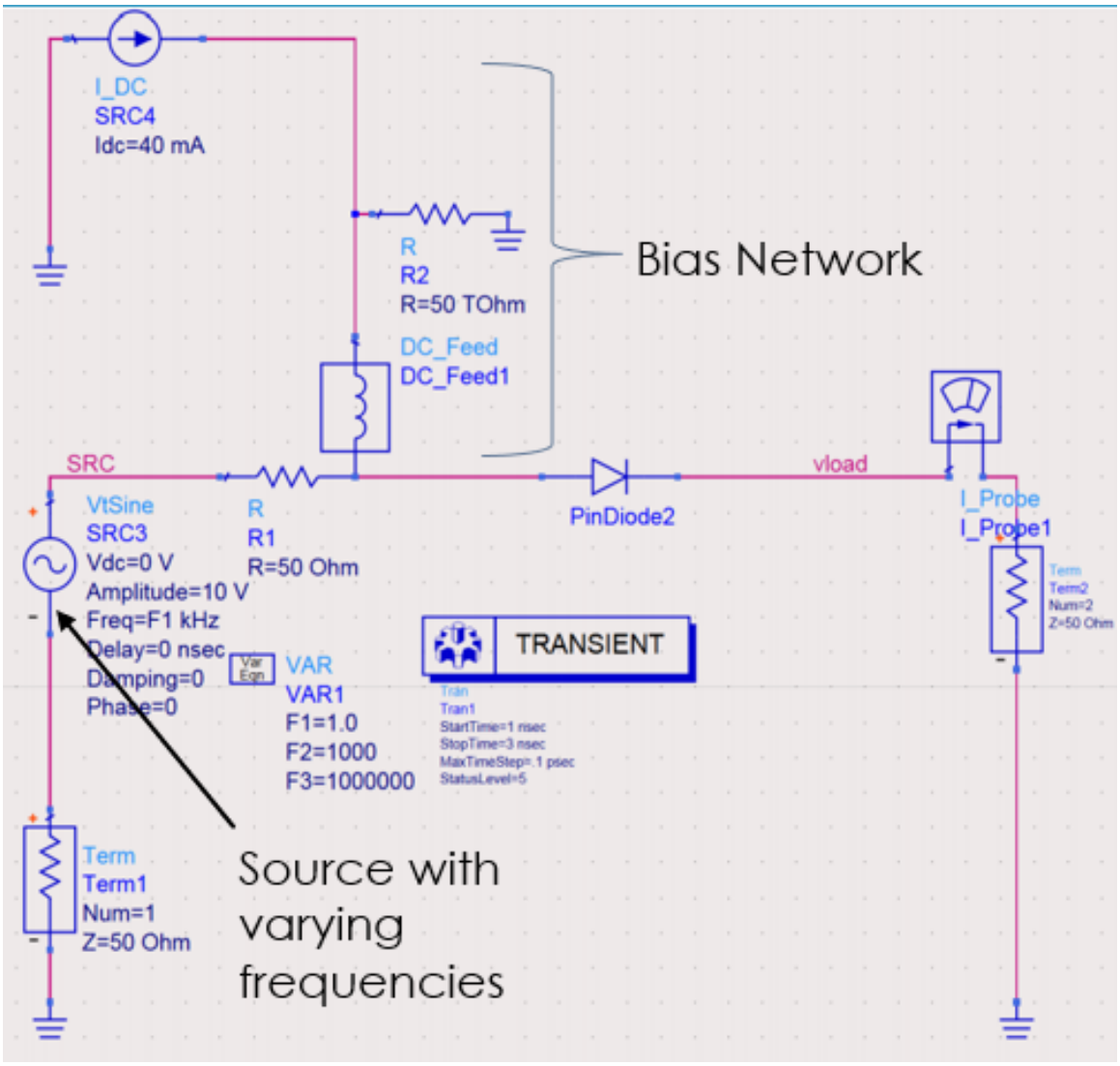

Figure 2.3: PIN Diode Rectifying Behavior Test Circuit. Source input at 1 kHz, 1 MHz, 1 GHz.

The resulting load voltage at each frequency can be seen in Figure 2.4. At frequencies in the MHz range, the diode only allows the signal above its turn on voltage through. However, as the frequency increases, the charges in the intrinsic region are not fully discharged and the diode continues conducting. Once the frequency is in the high MHz and into the GHz range, the PIN diode conducts through the positive and negative sections of the AC signal.

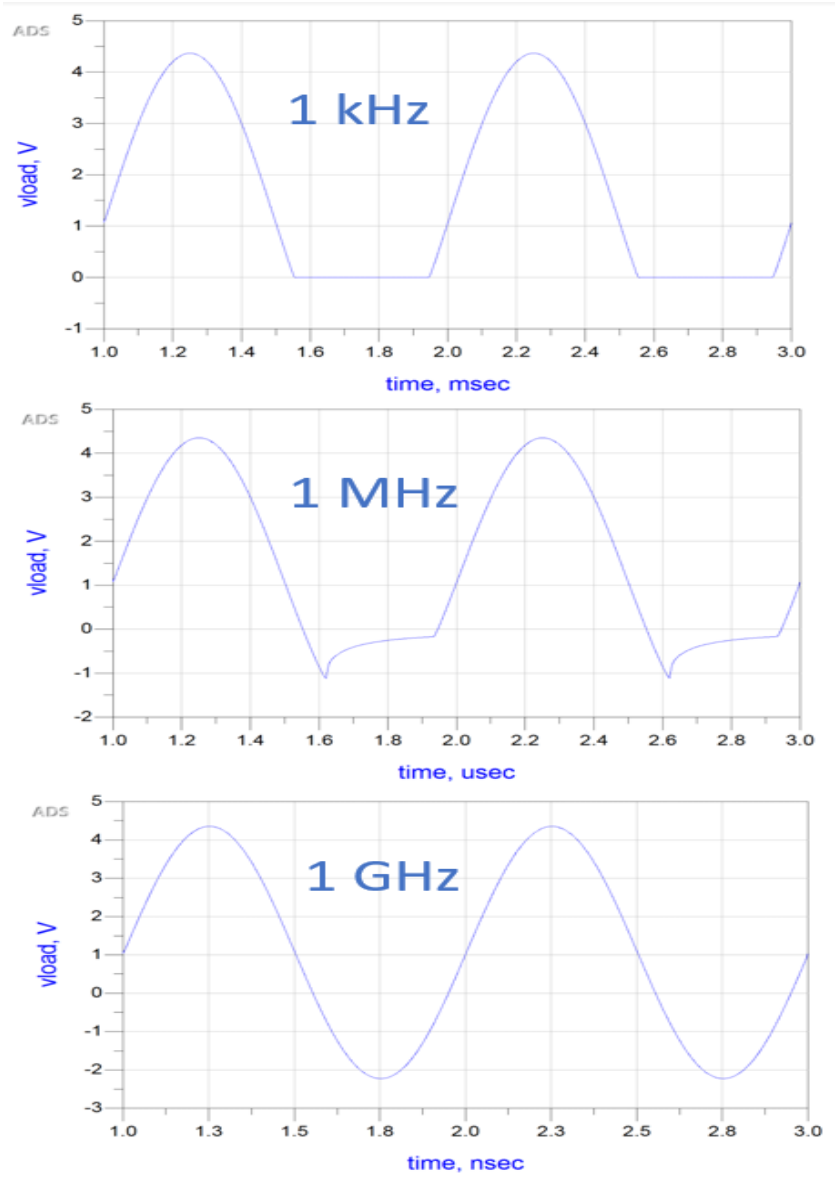

Figure 2.4: PIN Diode Rectifying Behavior. (top: 1 kHz, fully rectifying; middle: 1 MHz, mostly rectifying, bottom: 1 GHz, passes full signal).

As mentioned before, when switching from forward to reverse bias, these spare carriers need to dissipate before the PIN diode switches. This extra intrinsic layer causes more carriers and therefore, the diode takes longer to switch than a standard PN diode. Figure 2.5 shows an energy band diagram showing this concept.

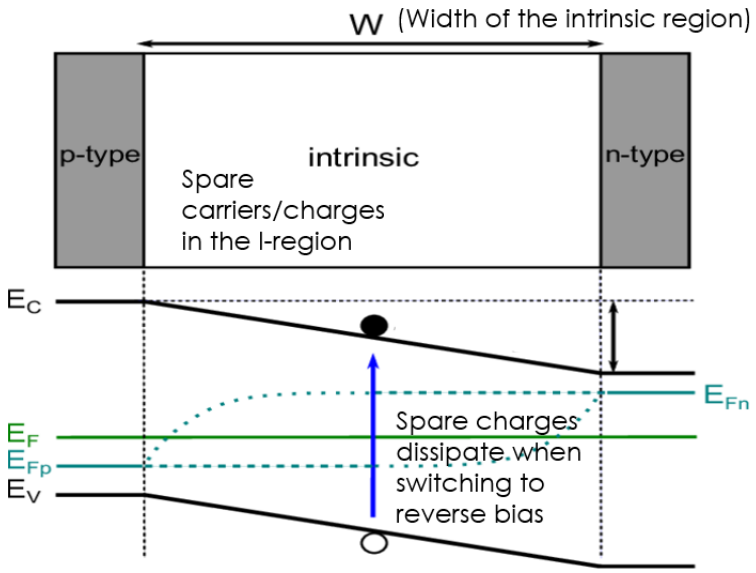

Figure 2.5: PIN Diode Band Diagram. Extra intrinsic region causes more spare carriers/electrons/holes, increasing the amount of time to discharge that charge and increasing the amount of time it takes the diode to change its mode of operation.

Forward to reverse bias transition is the reverse recovery time. The recovery time causes the PIN diode to remain ON when the frequency is in the GHz range. This is ideal for large amplitude high frequency signals because the diode continues to act as a resistor even when the signal should be forcing it into reverse bias. The intrinsic region also creates more space between the P and N regions, reducing capacitance and increasing isolation when in reverse bias.

This also allows the DC control current to be on the order of mA, while the microwave current can be on the order of A. This is a huge advantage when considering power handling [20].

2.1.2 Forward Biased PIN Diode

At forward bias, the PIN diode behaves like a small resistor in series with a small inductance. This is shown in Figure 2.6.

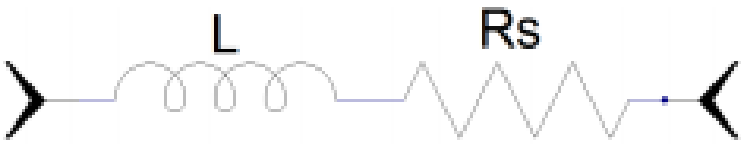

Figure 2.6: Forward Bias PIN Diode Model; a resistor and inductor in series

When a DC current passes through the PIN diode, the holes and electrons are injected into the I-region and an amount of charge is stored here. This stored charge is related to bias current and carrier lifetime in Equation 2.1.

The series resistance of the PIN diode is inversely proportional to Q:

$$R_s = \frac{W^2}{(\mu_n + \mu_p)Q} \quad (Ohms) \tag{2.2}$$

where W is the I-region width, I_f is the forward bias current, τ is the carrier lifetime, μ_n is the electron mobility, and μ_p is the hole mobility [8].

For the diode to conduct the negative portion of the AC signal through when forward biased, the stored charge, Q, must be much greater than the charge removed from the negative component of the RF current, I_{RF}. The following inequality is used to determine if this is the case:

$$Q \gg \frac{I_{RF}}{2\pi f} \tag{2.3}$$

2.1.3 Reverse Biased PIN Diode

At reverse bias, the PIN diode behaves like a capacitance in parallel with a parasitic resistance. Also a small inductance is added in series to this parallel structure as seen in Figure 2.7.

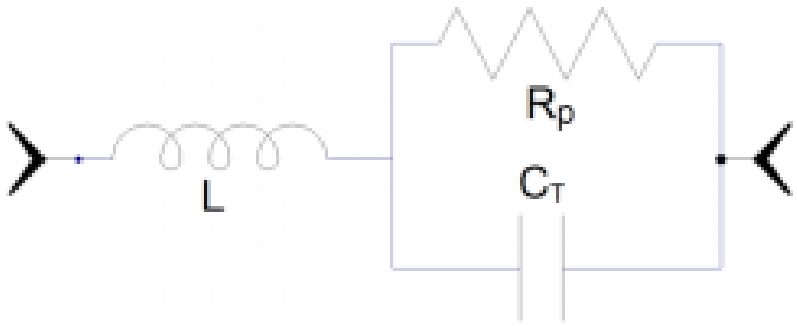

Figure 2.7: Reverse Bias PIN Diode Model; L in series with parallel RC.

When the PIN diode is in reverse or zero bias condition, the carriers are depleted from the I-region, allowing the diode to behave as an open-circuit. The reverse biased PIN diode is the parallel plate capacitance between the P and N regions.

$$C = \frac{\varepsilon A}{W} \quad (Farads) \tag{2.4}$$

where W is the I-region width, ε is the permittivity of silicon, and A is the area of the diode junction [8].

2.2 PIN Diode Switch Topologies

A PIN diode switch has three common topologies:

1. Series topology where one PIN diode is connected in series, across the transmission line,
2. Shunt topology where one PIN diode is connected in shunt, from the line to the ground,
3. Series-shunt topology where one PIN diode is connected in series and a second PIN diode is connected in shunt.

At a minimum, an RF switch based on PIN diodes needs a DC blocking capacitor to prevent the DC bias current from reaching the RF output, and an RF choke to provide a path for the DC bias current to return while blocking the RF signal. The DC bias voltage needed to control the PIN diode's mode is a function of the diode as well as the RF signal level, temperature range, and other factors. This bias voltage must be decoupled from the RF signal and be stable, as any noise or ripple will affect the diode's operating point [20].

These different topologies are shown and expanded in the following sections. Note that all of these equations are taken from Macom's AG312 application note [15].

2.2.1 Series Switch

One PIN diode switch topology is the series connected switch, as shown in Figure 2.8.

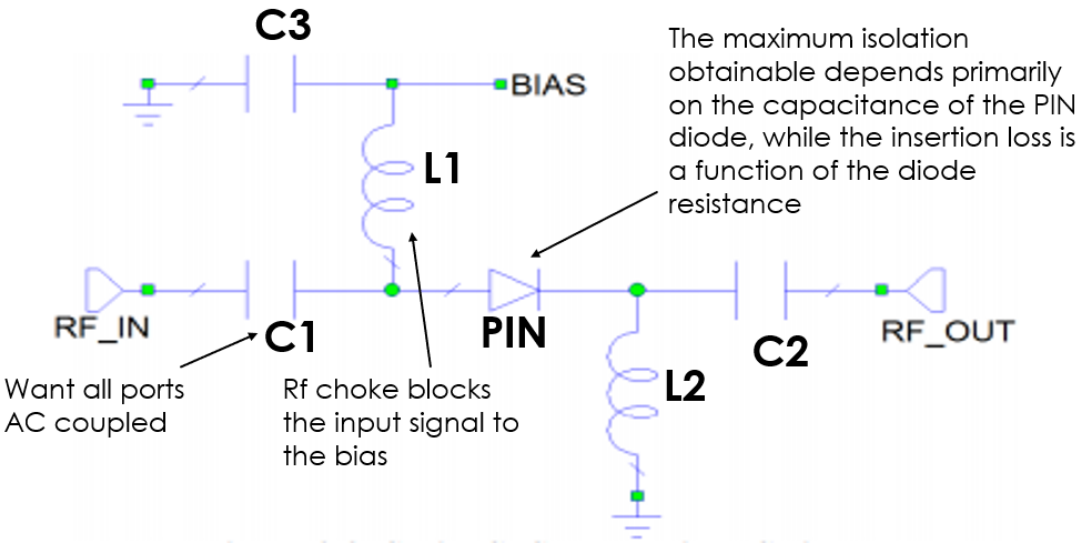

Figure 2.8: Series Connected PIN Diode Switch

In series connected switches, the maximum isolation obtainable depends primarily on the capacitance of the PIN diode, while the insertion loss and power dissipation are functions of the diode resistance. The principal operating parameters of a series switch may be obtained using the following equations:

2.2.1.1 Insertion Loss (Series Switch)

$$IL = 20log_{10}[1 + \frac{R_s}{2Z_o}] \quad (dB) \tag{2.5}$$

This equation applies to a single pole single throw (SPST), meaning one input and one output, diode switch switch and is graphically presented in Figure 2.9 for a 50 ohm impedance design. For multi-throw switches, the insertion loss is a few dBs higher due to any mismatch caused by the capacitance of the PIN diodes in the "off" arms.

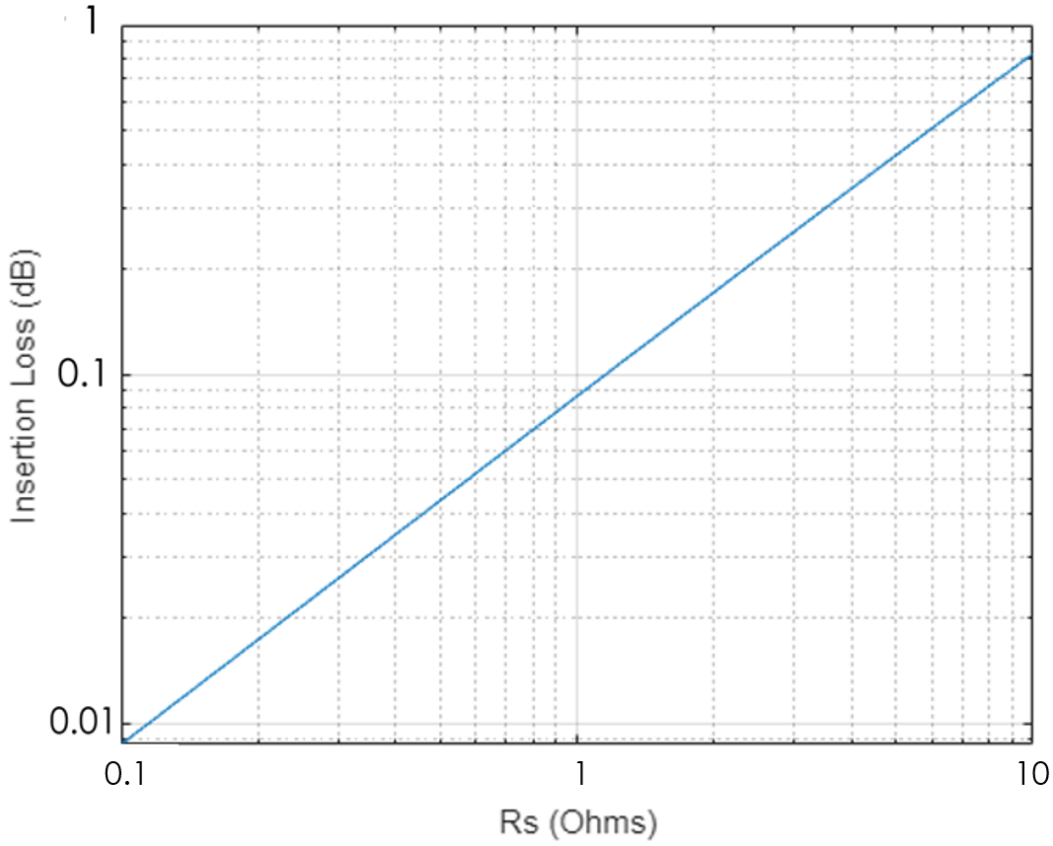

Figure 2.9: PIN Diode Series Switch Insertion Loss (50 Ohm System). Insertion loss is proportional to series resistance.

where IL is the insertion loss, R_S is the diode series resistance, and Z_O is the characteristic impedance.

2.2.1.2 Isolation (Series Switch)

$$I = 10log_{10}[1 + (4\pi fCZ_o)^{-2}] \quad (dB) \tag{2.6}$$

where I is the isolation, f is the frequency, C is the diode capacitance, and Z_O is the characteristic impedance.

This equation applies for a single pole single throw (SPST), meaning one input and one output, diode switch. Add 6 dB for a SPNT, meaning one input and N outputs, switch to account for the 50 percent voltage reduction across the "off" diode due to generator's Z_o source impedance. Figure 2.10 graphically presents isolation (with C = 0.2 pF) as a function of frequency for a simple series switch. These curves are plotted for circuits terminated in 50 Ohm loads.

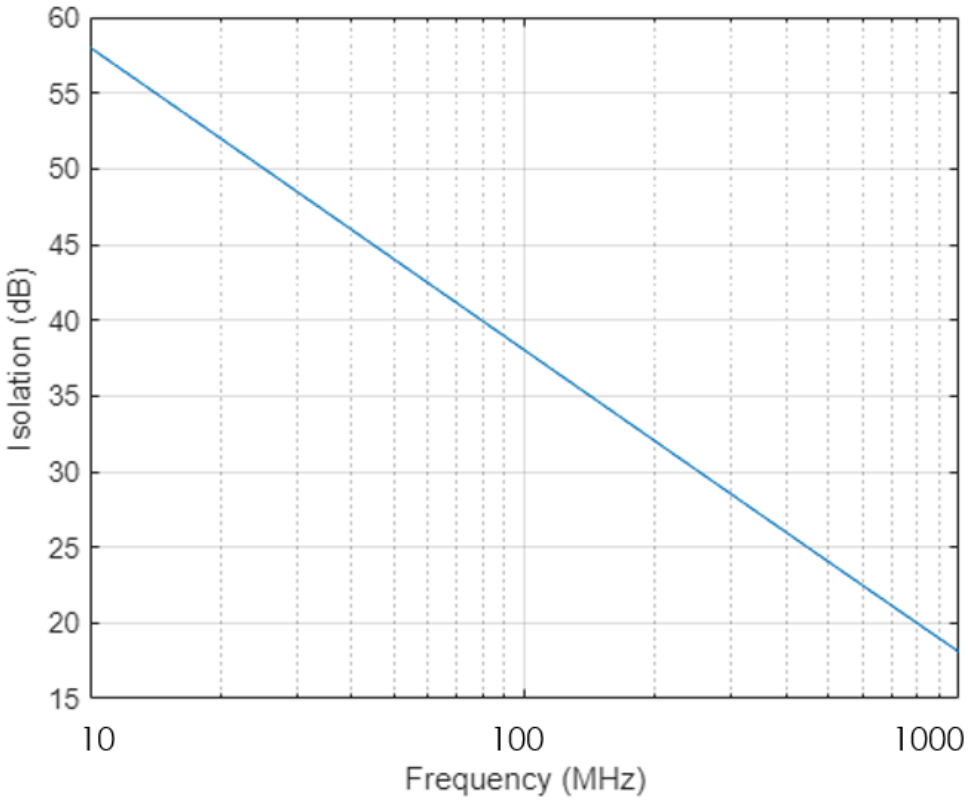

Figure 2.10: PIN Diode Series Switch Isolation (50 Ohm System with C = 0.2 pF). Isolation is inversely proportional to frequency.

2.2.2 Shunt Switch

Figure 2.11 shows a typical shunt connected PIN diode switch. These shunt diode switches offer high isolation for many applications. Unlike the series diode, the shunt diode may be heat sinked at one electrode, resulting in higher RF power handling. In shunt switch designs, isolation depends on the forward resistance, whereas insertion loss depends on the capacitance.

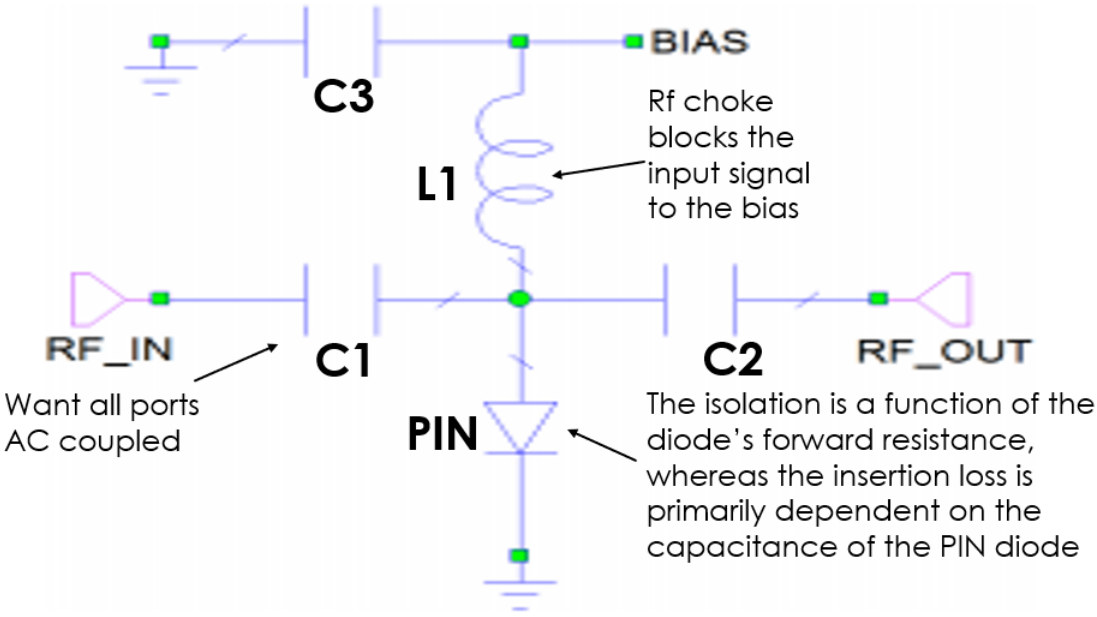

Figure 2.11: Shunt Connected PIN Diode Switch

2.2.2.1 Insertion Loss (Shunt Switch)

$$IL = 10log_{10}[1 + (\pi f C Z_o)^2] \quad (dB) \tag{2.7}$$

where IL is the insertion loss, f is the frequency, C is the diode capacitance, and Z_O is the characteristic impedance.

This equation applies to both SPST and SPNT shunt switches and is graphically presented in Figure 2.12 for a 50 ohm load impedance design with a capacitance of 0.2 pF.

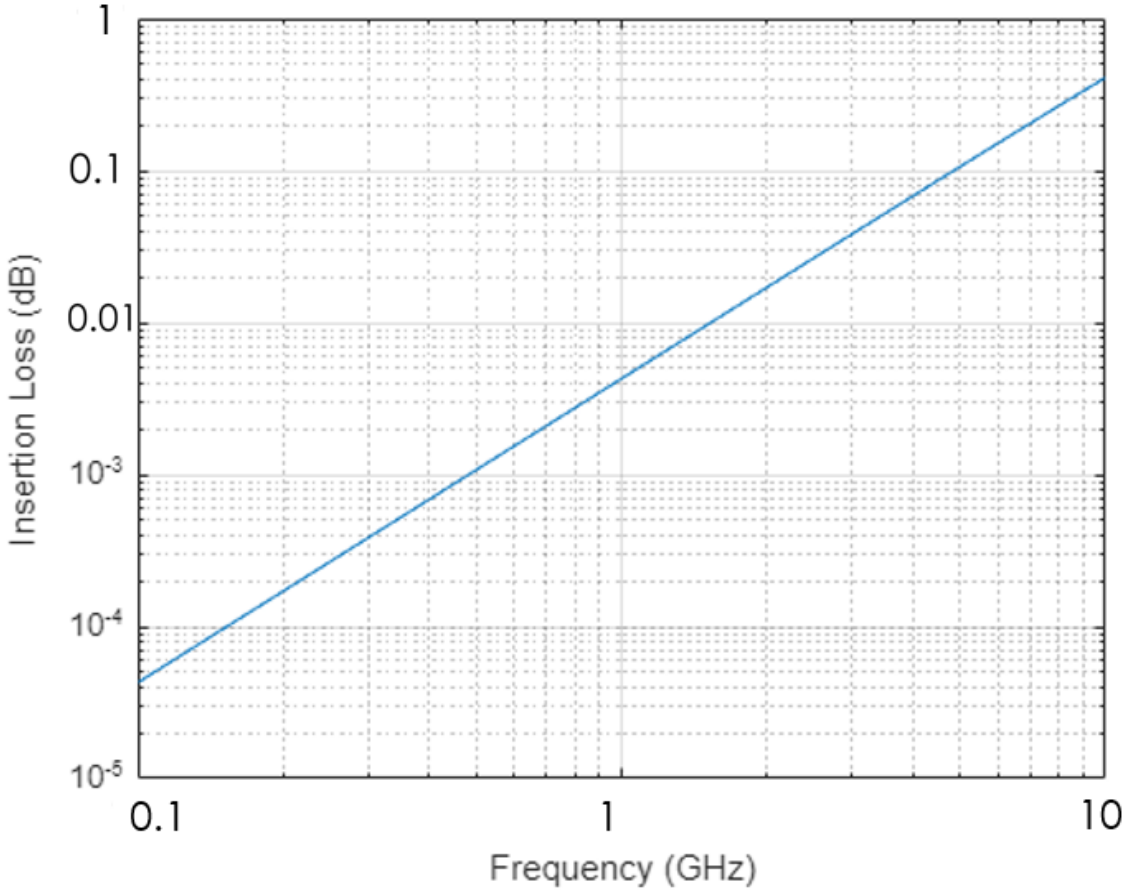

Figure 2.12: PIN Diode Shunt Switch Insertion Loss (50 Ohm System with C = 0.2 pF). Insertion Loss is proportional to frequency.

2.2.2.2 Isolation (Shunt Switch)

$$I = 20log_{10}[1 + \frac{Z_o}{2R_s}] \quad (dB) \tag{2.8}$$

where I is the isolation, Z_O is the characteristic impedance, and R_S is the diode series resistance.

This equation, which is illustrated in Figure 2.13, applies to a SPST shunt switch. Add 6 dB to these values to obtain the correct isolation for a multi-throw switch.

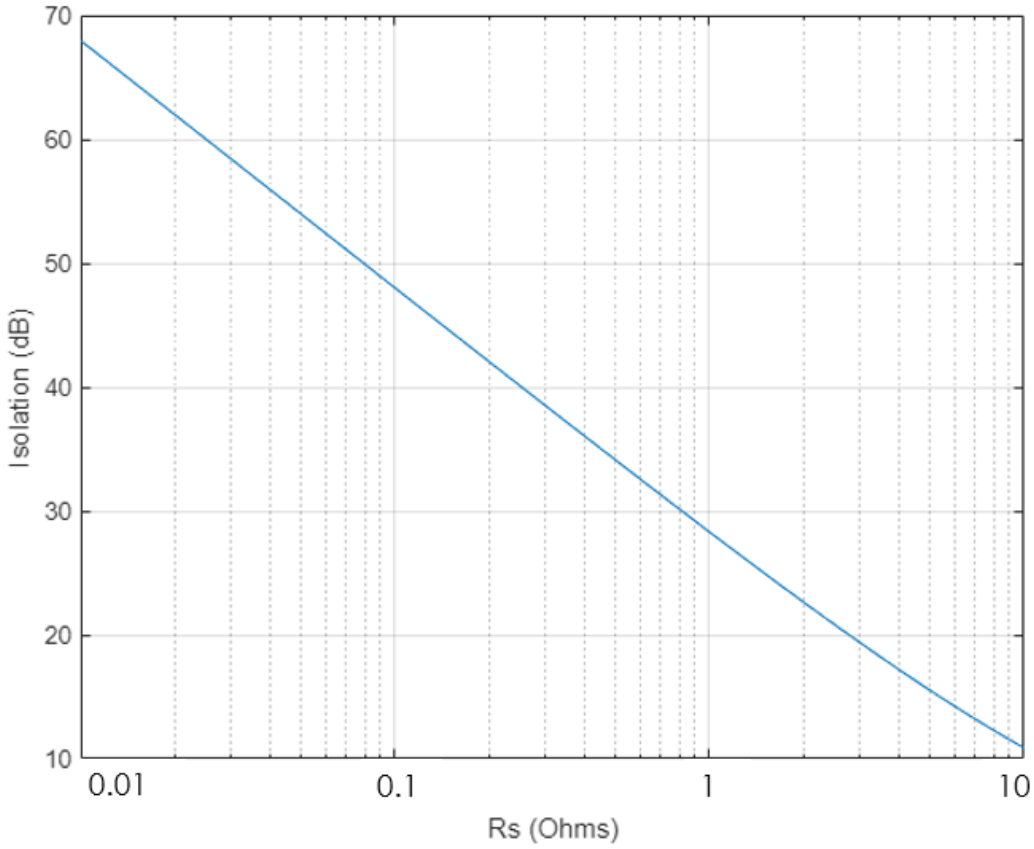

Figure 2.13: PIN Diode Shunt Switch Isolation (50 Ohm System). Isolation is inversely proportional to series resistance.

2.2.3 Series-Shunt Switch

In practice, it is usually difficult to achieve more than 40 dB isolation using a single PIN diode, either in shunt or series, at RF and higher frequencies. The causes of this limitation are generally radiation effects in the transmission medium and inadequate shielding. To overcome this there are switch designs that employ combinations of series and shunt diodes such as the series shunt switch shown in Figure 2.14.

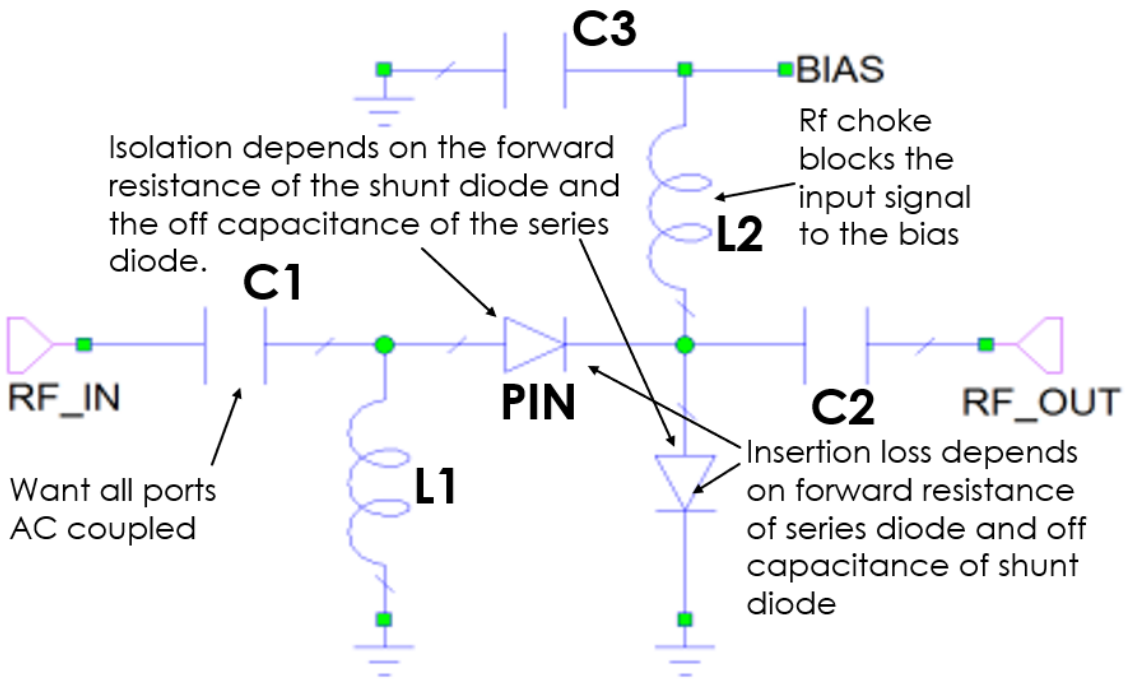

Figure 2.14: Series-Shunt Connected PIN Diode Switch

Broad band low insertion loss property of series switches is combined with broad band high isolation property of shunt switches, so the overall switch performance is improved. In this topology, when the bias is positive, the series PIN diode is reverse biased providing high impedance, while the shunt PIN diode is forward biased providing low impedance. In this situation the switch is in isolation condition and

is OFF. When the bias is negative, the switch is transferring the RF signal to the output.

2.2.3.1 Insertion Loss (Series Shunt Switch)

In series shunt switch designs, the insertion loss primarily depends on the forward resistance of the series diode and the off capacitance of the shunt diode.

$$IL = 10log_{10}[(1 + \frac{R_s}{2Z_O})^2 + (\frac{(2\pi fC)(Z_o + R_s)}{2})^2] \quad (dB) \tag{2.9}$$

where IL is the insertion loss, R_S is the diode series resistance, Z_O is the characteristic impedance, f is the frequency, and C is the diode capacitance. This equation applies to both SPST and SPNT shunt switches.

2.2.3.2 Isolation (Series Shunt Switch)

On the other hand, isolation depends on the forward resistance of the shunt diode and the off capacitance of the series diode, as shown by the equation:

$$I = 10log_{10}[(1 + \frac{Z_o}{2R_s})^2 + (\frac{1}{4\pi fCZ_o})^2 \ (1 + \frac{Z_o}{R_s})^2] \quad (dB) \tag{2.10}$$

where I is the isolation, Z_O is the characteristic impedance, R_s is the diode series resistance, f is the frequency, and C is the diode capacitance.

2.3 PCB Substrate Material

The board material drives many design choices. Not only do the material properties ultimately determine the dimensions of the layout, they also degrade signal integrity. Due to RF frequencies causing loss in the signal and variations in the material properties, the consistency and performance of the material becomes critical [18].

There are a few different properties to consider when choosing a PCB substrate material:

- Dielectric constant (ϵ_r): Dielectric constant is the ratio of the electric permittivity of the material to the electric permittivity of free space. Decreased dielectric constant improves isolation, signal propagation speed, and stray capacitance for a given trace geometry.

  As frequency increases, the dielectric constant tends to decrease. The rate of this decrease across frequency varies with the material. For a material to be suitable for RF applications in the high GHz range, the dielectric constant must remain relatively constant over the whole frequency range.

- Dielectric loss tangent ($\tan \delta$): Loss tangent is a measure of power lost due to the material, typically varying from 0.02 for common PCB materials down to 0.001 for low-loss high-end materials. As the frequency increases, the loss tangent also increases. This loss is the result of electromagnetic wave absorption in the dielectric material.

- Resistivity (ρ): Resistivity is the PCB material electrical resistance in ohm-meters (Ω-m).

- Electrical strength: Electrical strength is the ability to resist electrical breakdown through the PCB, typically 800 V/mil to 1500 V/mil.

2.4 PCB Transmission Line Technology

The device must reliably transfer signals across the transmission line.

2.4.1 Microstrip

Microstrip transmission lines, shown in Figure 2.15, has been one of the most popular microwave transmission-line formats for decades and is well characterized.

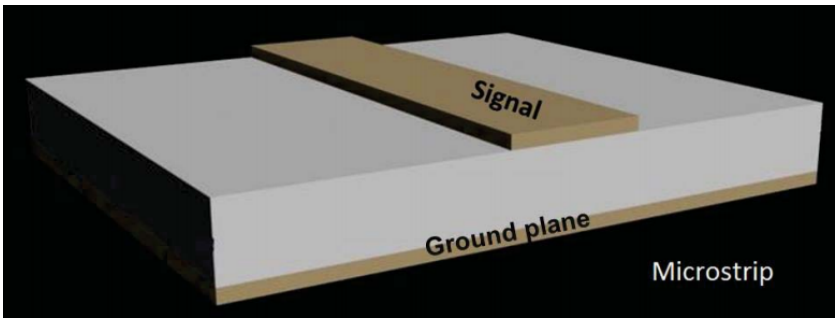

Figure 2.15: Microstrip Transmission Line. Conductor/signal line on top plane, substrate with the ground plane underneath.

Microstrip supports moderate-bandwidth circuits through microwave frequencies. However, radiation loss and mode suppression difficulties occur at millimeter-wave frequencies. Microstrip circuits benefit from minimal sensitivity to PCB tolerances including copper plating thickness variations [7]. Electric fields are primarily vertical between the signal and ground planes, as shown in Figure 2.16.

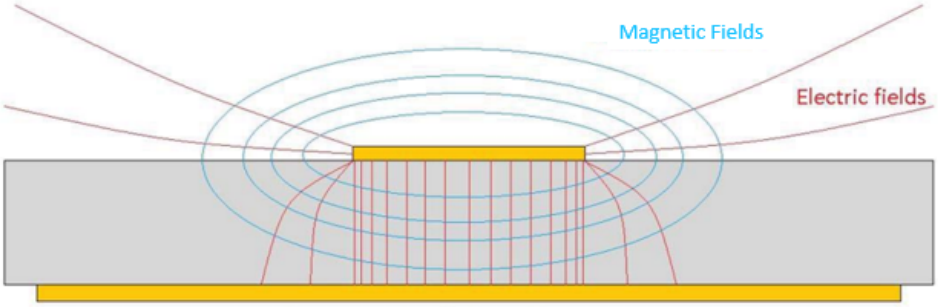

Figure 2.16: Microstrip Cross-Section. Vertical electric field lines from signal trace to bottom ground plane.

2.4.2 Coplanar Waveguide

Coplanar waveguide (CPW) transmission lines, shown in Figure 2.17 have also been used extensively in microwave PCB applications.

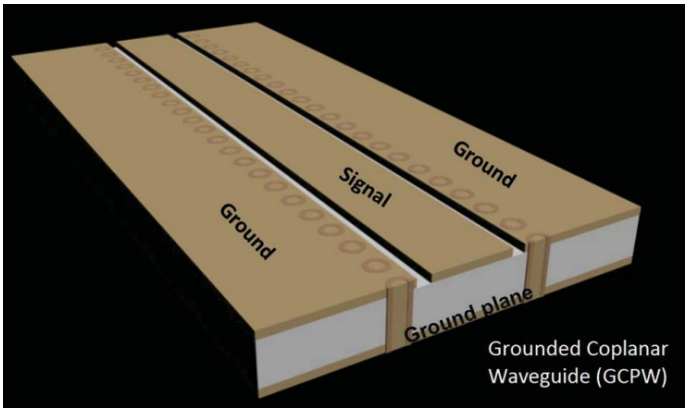

Figure 2.17: Coplanar Waveguide Transmission Line. Signal trace and adjacent ground plane on top ground plane, vias connect top and bottom ground planes through the substrate.

Coplanar waveguide suffers less radiation loss at millimeter-wave frequencies than microstrip. CPW is also more capable at suppression at millimeter-wave frequencies. It is a strong circuit technology for designs at 30 GHz and greater. CPW suffers from PCB manufacturing, requiring more precise tools to handle the few mils of

distance from the signal to ground plane, but it is still fairly easy to manufacture with accuracy [10]. In contrast to the microstrip transmission lines, the electric fields are primarily horizontal from signal trace to ground plane on the coplanar layer, as seen in Figure 2.18.

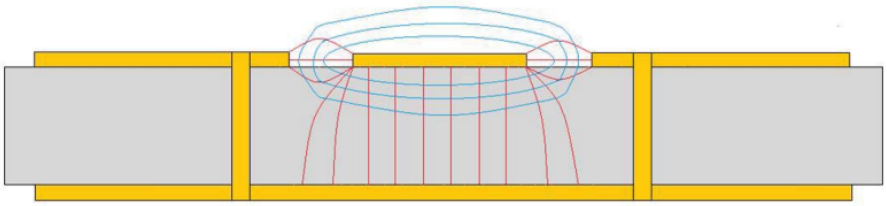

Figure 2.18: Coplanar Waveguide Cross-Section. Electric field is primarily horizontal from signal trace to adjacent ground plane.

Chapter 3

DESIGN CONSIDERATIONS

The design process involved modeling of PIN didoes to ensure accuracy in simulation, selection of components, dealing with the close proximity (in the order of a few mils) of the lines which caused coupling between the input and the outputs at the upper end of the bandwidth, routing of the lines on the board and minimizing reflection, spacing of the PIN diodes to ensure an open circuit equivalent for the OFF outputs, as well as other design considerations to maximize performance.

3.1 Design Specification Goals

The switch is designed as an 8-way RF switch, simulated in Keysight's ADS. A star network configuration with series-shunt PIN diode switches is used to create the 8-way RF switch (explained in Section 3.6 and finished design seen in Figures 4.2 and 4.1 in Chapter 4). The design specifications were based on other SP4T and SP8T switches that vendors such as MACOM (MA4AGSW8, MA4SW410B, MASW-004103) have manufactured. The design specification goals are shown in Table 3.1 below:

Table 3.1: Specifications

PARAMETER	FREQ. BAND (GHz)	GOAL
INSERTION LOSS (dB)	2 - 10	1
	10 - 14	1.5
	14 - 18	2
ISOLATION (dB)	2 - 10	50
	10 - 14	40
	14 - 18	30
POWER HANDLING (dBm)	-	23
SWITCHING SPEED (ns)	-	20
AC COUPLED	-	YES
SIZE (mil)	-	500x500

3.2 PIN Diode Modeling

PIN diode models attempt to capture basic attributes as well as changes in these attributes as a function of temperature, voltage, and frequency. Changes in characteristics such as isolation, linearity, distortion, insertion loss, and power consumption versus frequency and power can be determined with reasonable accuracy. As with all RF designs, interconnections, PC board effects, EM fields, and parasitics can distort the model. Designers must attempt to incorporate these into their simulation model in order to get a more accurate view of the performance of the PIN diode switch.

Keysight provides a library with many industry components readily available to simulate. Some vendors provide a downloadable ADS library as well. Not all PIN Diode vendors provide an ADS library; the vendors that do only provide diode models with fixed values, meaning they can not be adjusted to model other diodes. Modelithics was an alternative option. They model PIN diodes authorized access to their library, which was a promising alternative. However, the Modelitics PIN diode models faced similar issues with limited vendor models and fixed parameter values. ADS

also provides a general PIN Diode model, with over 40 adjustable parameters (See Appendix A for full list).

3.2.1 ADS PIN Diode Model Verification

The equivalent circuit for the ADS PIN diode model is shown in Figure 3.1. This model was investigated in depth, with the goal of ensuring its accuracy in representing diode characteristics.

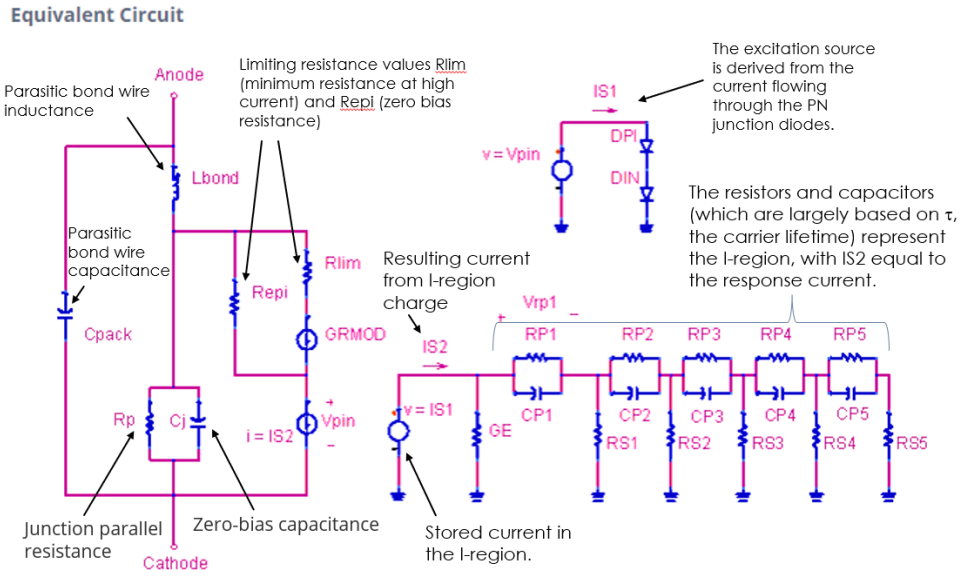

Figure 3.1: ADS PIN Diode Model Equivalent Circuit. Models the I-region stored charge, the current due to the stored charge, and the recombination of the stored charge in the PIN diode. The voltage source on the bottom right circuit is the stored current in the junction (drawn from the top right circuit). The resistors and capacitors on the bottom right (τ, the carrier lifetime, sets the values of these components, see reference [12]) represent the diode junction, with IS2 equal to the response current.

In order to ensure accuracy, simulations were compared to the results in another study that compared their results to a measured PIN diode [12]. The following figures display the PIN diode simulations.

Figure 3.2 shows the schematic used to obtain the IV curve of the PIN diode model.

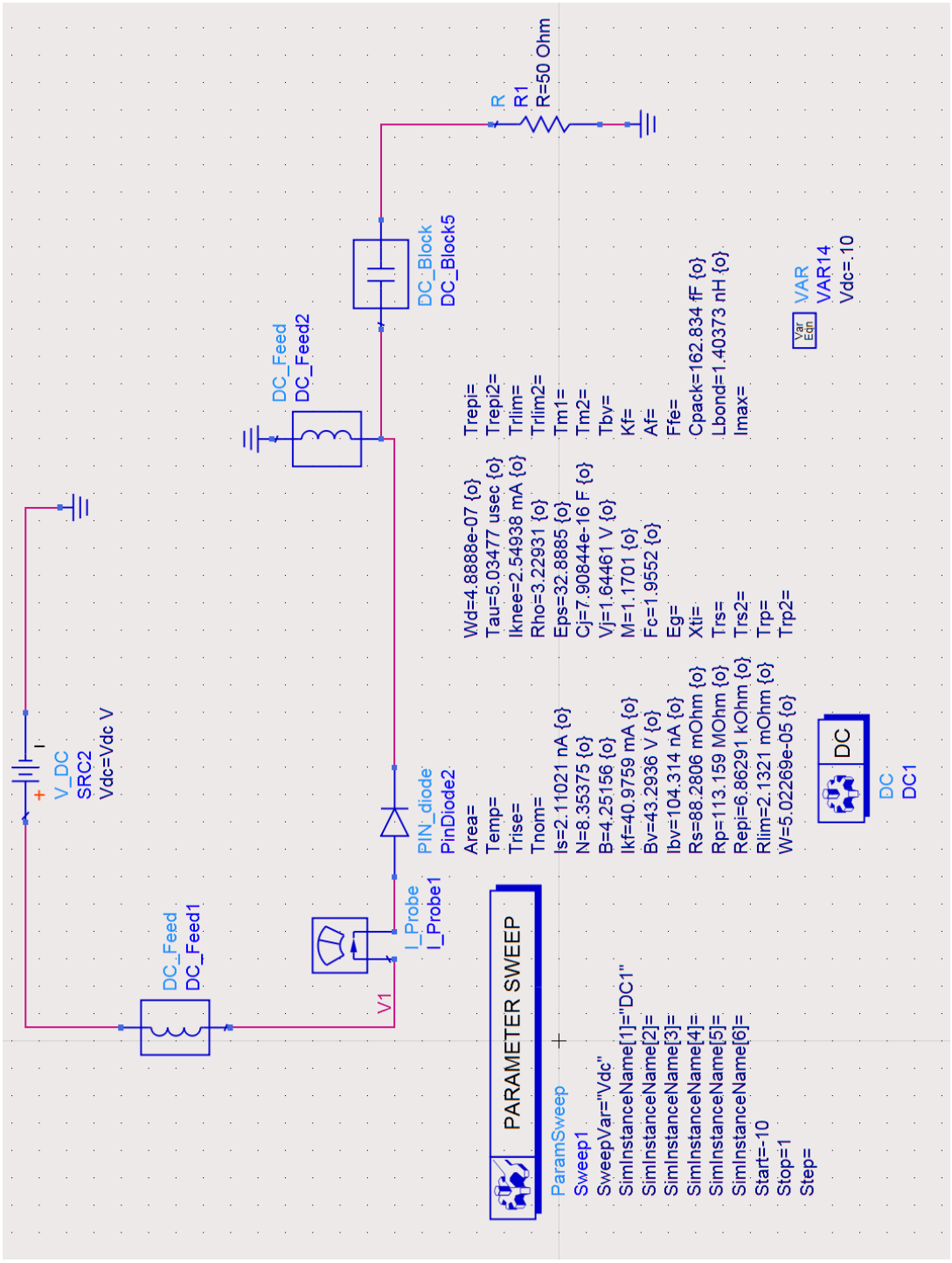

Figure 3.2: PIN Diode Voltage vs. Current Relationship Test Circuit. Source swept across the PIN diode and plotted against the current through the diode.

Figure 3.3 shows the simulation results for the IV curve simulation. Again, as expected, it matches with the model.

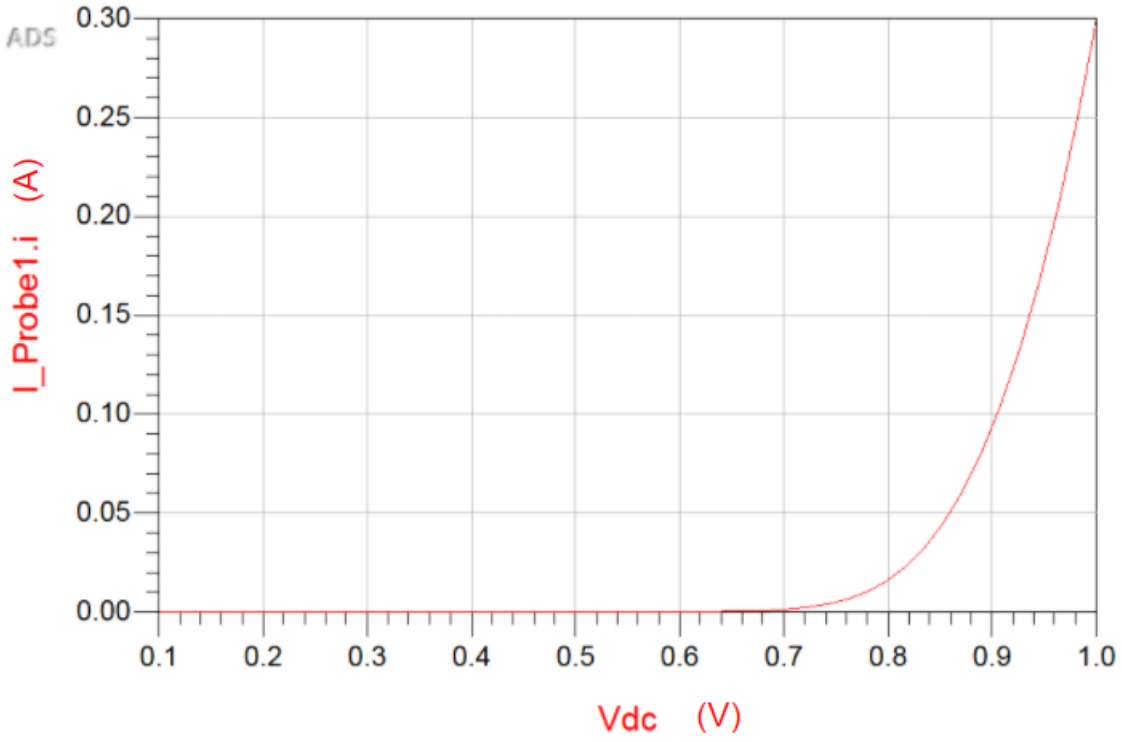

Figure 3.3: PIN Diode Voltage vs. Current. No current until diode turn on voltage ($\sim$ 0.7V).

Figure 3.4 shows the schematic for testing PIN diode capacitance vs. a reverse biased voltage.

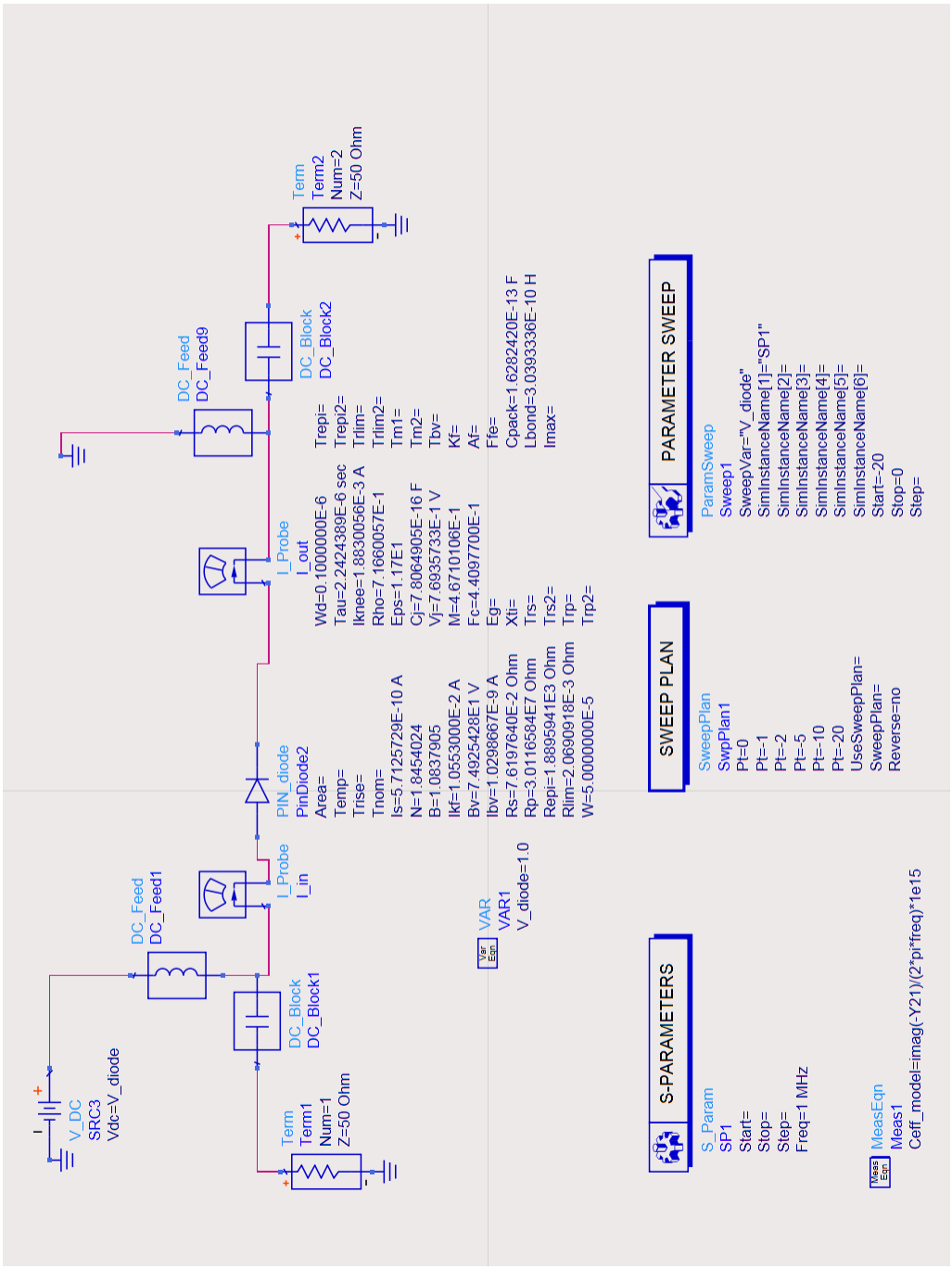

Figure 3.4: PIN Diode Capacitance Test Circuit. Bias voltage swept from 0V to -20V, observing PIN diode capacitance.

Figure 3.5 shows the simulation results for the capacitance of the diode at 1, 100, and 1000 MHz. The capacitance decreases with an increased voltage as expected.

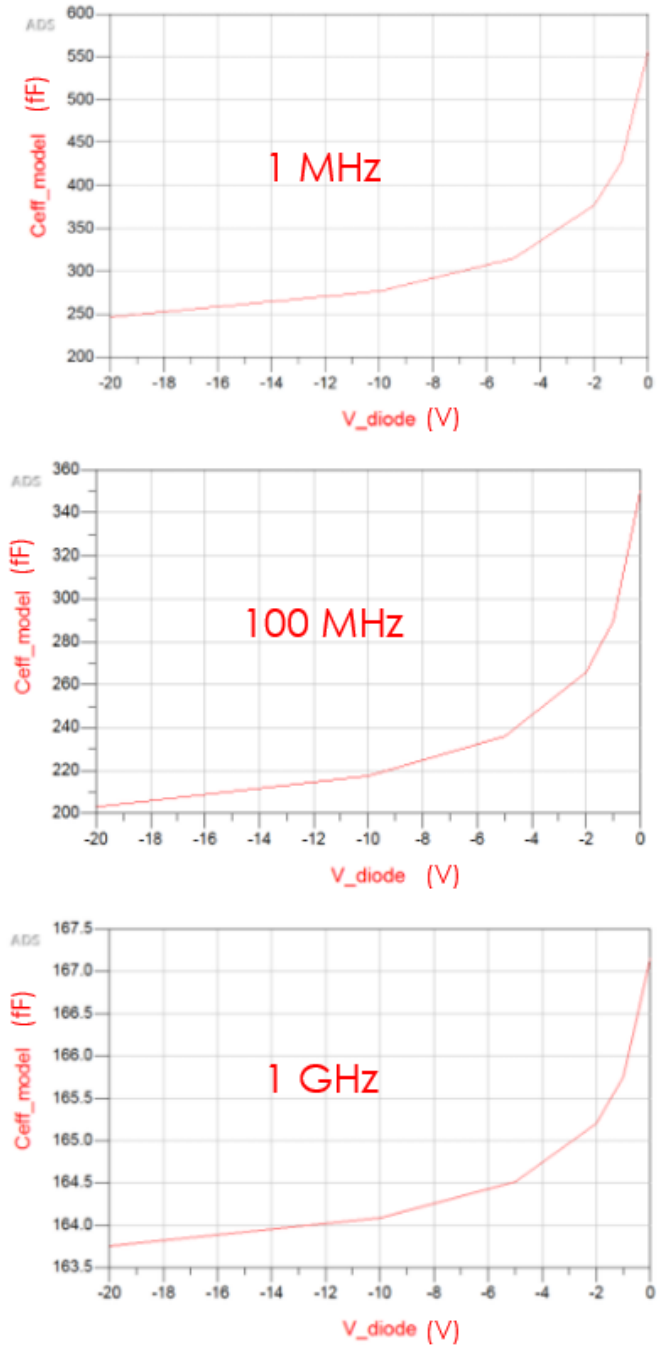

Figure 3.5: Capacitance vs. Voltage Bias at 1MHz (top), 100MHz(middle), 1GHz (bottom). Capacitance decreases with increasing reverse bias and with increasing frequency.

Figure 3.6 shows the schematic used to obtain diode resistance vs. a forward bias current of the PIN diode model.

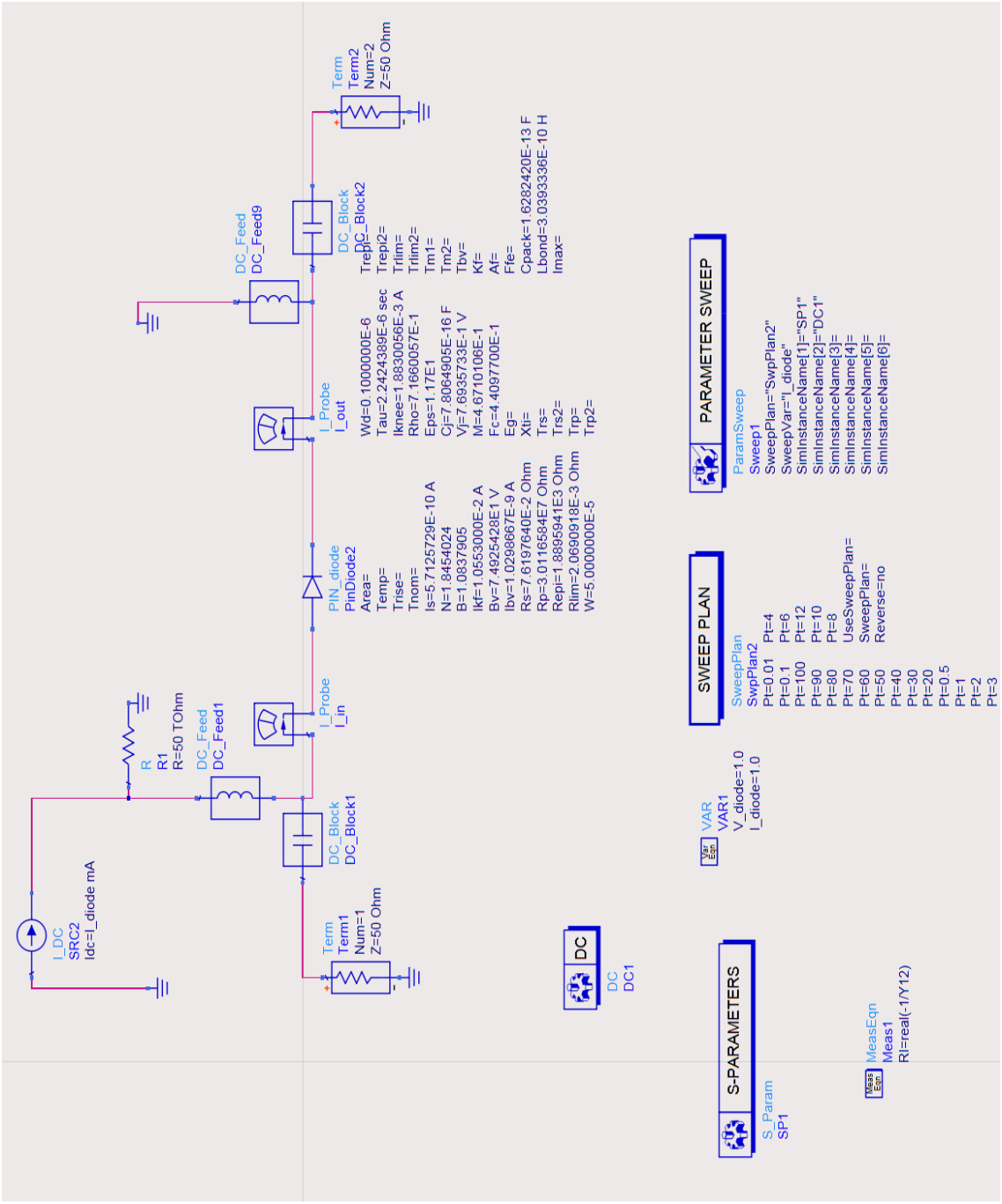

Figure 3.6: PIN Diode Resistance vs Forward Bias Current Test Circuit. Current source biasing the PIN diode swept from 0.01 to 100 mA, observing PIN diode resistance.

Figure 3.7 shows the results of the resistance vs. forward bias current for the PIN diode model. As expected, the resistance decreases with increased current.

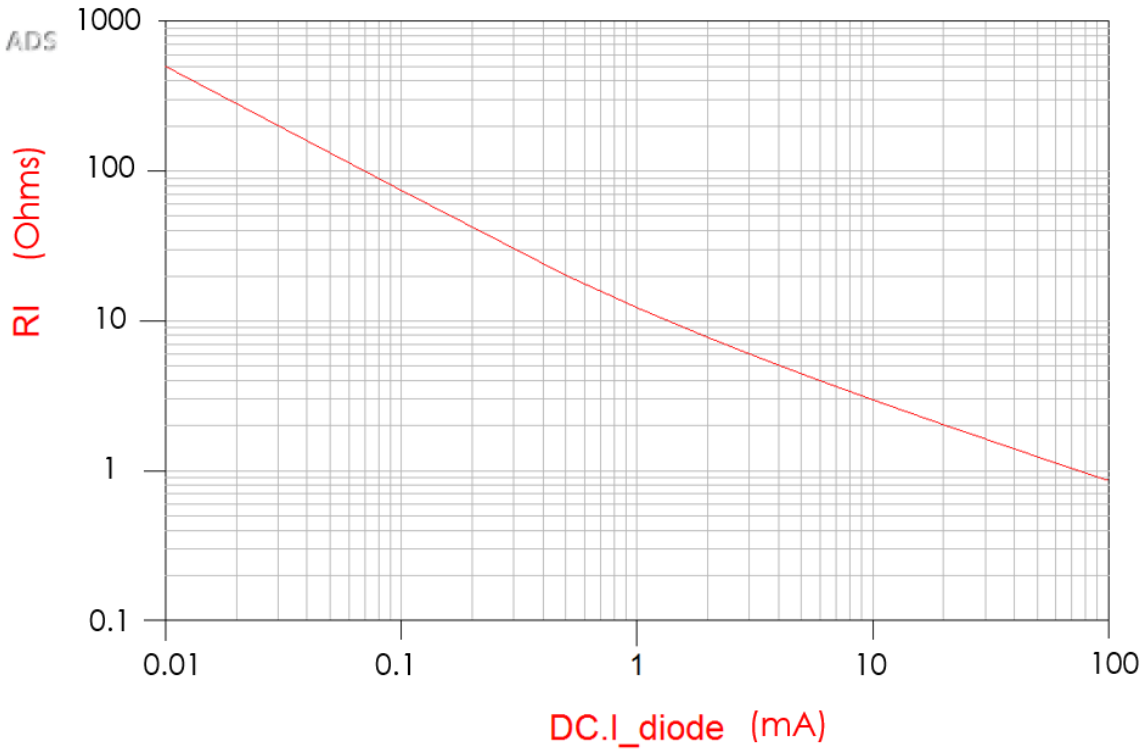

Figure 3.7: Resistance vs. Forward Bias Current at 100 MHz. Resistance is inversely proportional to forward bias current.

Figure 3.8 shows the schematic to test power handling, or how much RF power the diode can handle at a constant bias. Note that this does not incorporate temperature or overheating effects; it is only based on the bias current and the amplitude of the input signal.

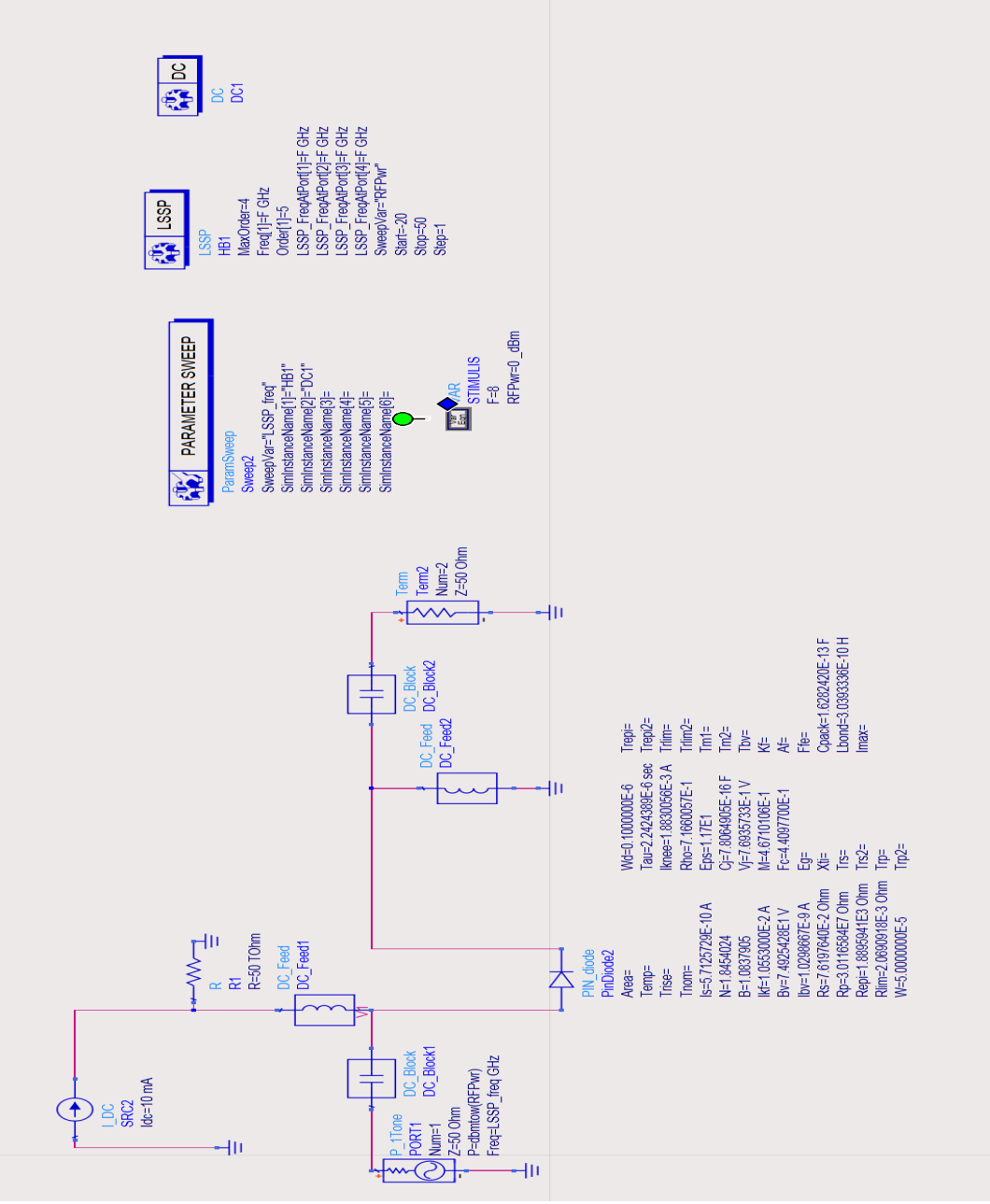

Figure 3.8: PIN Diode Power Handling Test Circuit. 8 GHz RF Input is sent through the PIN Diode with increasing amplitude power. This is done at several bias values.

The results at different bias levels are shown in Figure 3.9 where the loss significantly drops off after an amount of RF power is applied to the diode.

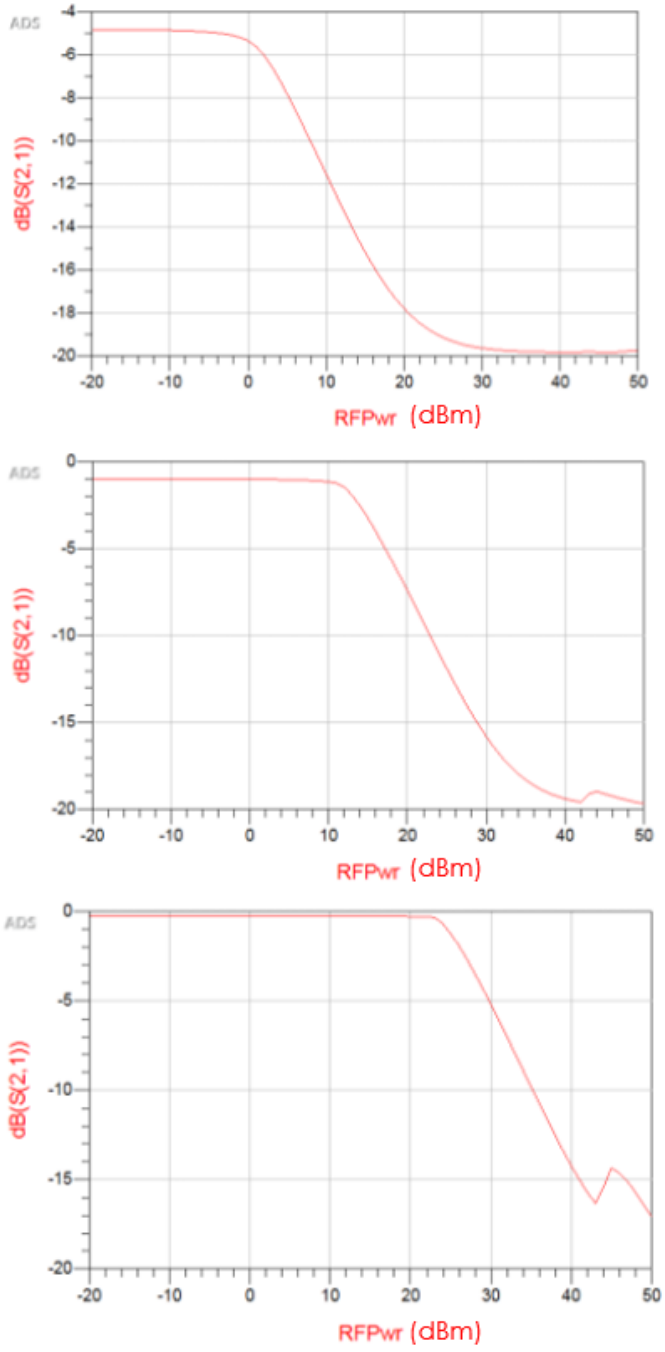

Figure 3.9: S(2,1) with Ibias = 0.1 mA (left), S(2,1) with Ibias = 1 mA (middle), S(2,1) with Ibias = 10 mA (right). Bias voltage and power handling are proportional; with a higher bias, the PIN diode can handle more RF input power before suffering signal loss (0 dBm at 0.1mA, 12 dBm at 1 mA, and 22 dBm at 10 mA).

Figure 3.10 shows the schematic used to test for reverse recovery time.

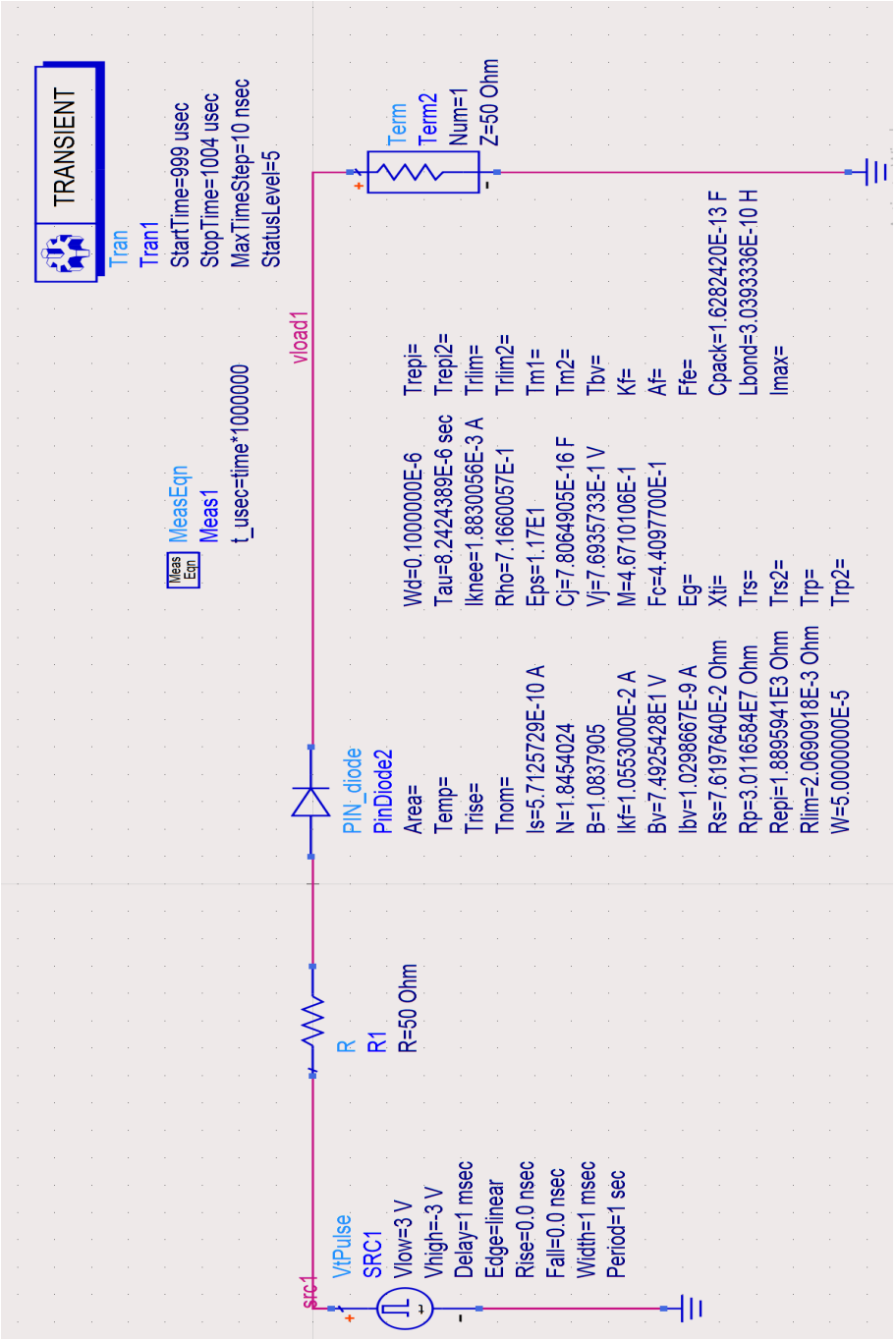

Figure 3.10: PIN Diode Reverse Recovery Time Test Circuit. Transient simulation where a pulse is sent through the PIN diode, holding a positive value for 1 ms before switching to -3 V.

The results of the simulation for two different τ minority carrier lifetime values are shown in Figure 3.11. The diode exhibits some recovery time meaning the diode is still conducting, as expected.

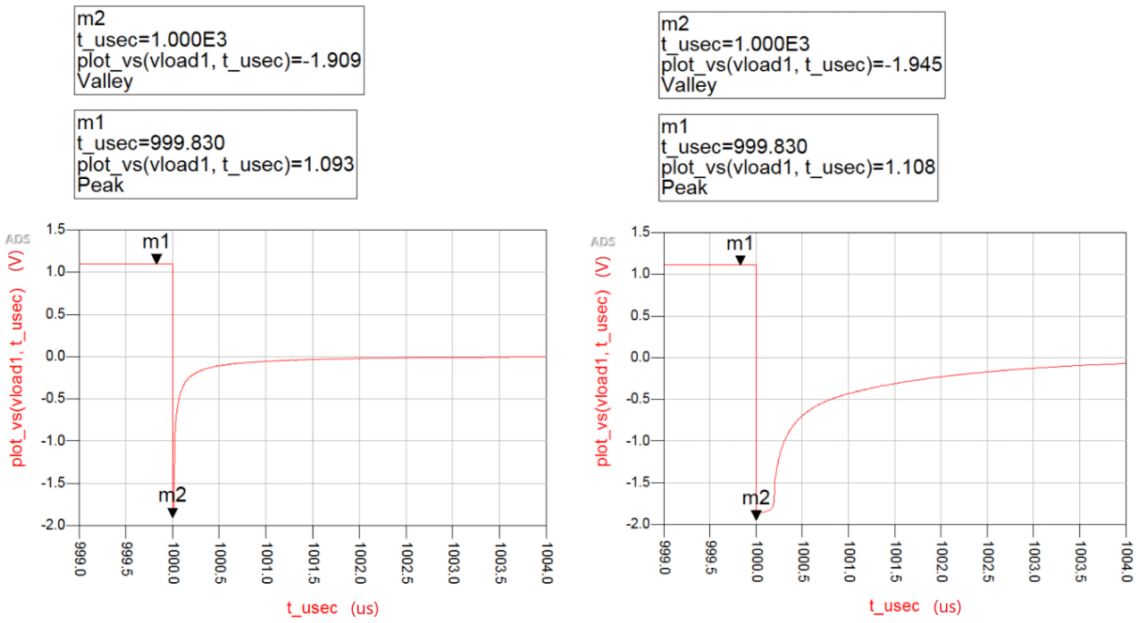

Figure 3.11: Reverse Recovery Time with τ = 2.2424389E-6 sec (left), Reverse Recovery Time with τ = 8.2424389E-6 sec (right). Voltage drops to a negative value for a short amount of time before settling to zero volts. The PIN diode is still conducting and allowing the signal to pass before switching into reverse bias, where it blocks the signal. Reverse recovery time is proportional with minority carrier lifetime value.

3.2.2 ADS PIN Diode Model Construction

The goal of this section is to develop a reliable process for obtaining a PIN Diode model in ADS for any vendor-provided diode.

The process includes the following steps.

1. Select the diode

2. Transfer direct parameters from the datasheet

3. Optimize for diode behavior based on data and graphs provided in datasheet

3.2.2.1 Select the Diode

This design calls for a low series resistance (¡ 2 Ohms) and low capacitance (¡ 0.2 pF). Once the diode is selected, the datasheet can be inspected in search of relevant parameters.

3.2.2.2 Transfer Direct Parameters from Datasheet

It is not possible to directly transfer all parameters from a diode data sheet into the ADS general PIN Diode model as the parameters in the model are based on various equations that determine the behavior of the PIN diode, while the datasheet provides absolute values in a certain testing environment. However, there exists an overlap in some significant parameters for which the values available on the data sheet directly correspond to the PIN Diode model values in ADS. The values most commonly provided on data sheets and the ADS model are reverse breakdown voltage (Bv) and current at reverse breakdown voltage (Ibv). Often times the data sheet provides good starting values for other parameters as well. In order to extract the other parameters and refine the model and its accuracy, an optimization is used to determine the parameter values. As mentioned earlier, the complete PIN diode model parameters can be found in Appendix A.

3.2.2.3 Optimize for Diode Behavior Based on Data/Graphs Provided in Datasheet

The main parameters optimized are the resistance and capacitance of the PIN diode. This is done by adding an optimization block and a goal block to the previous schemat-

ics shown in the model verification. The goal block sets the parameter values to optimize to, while the optimization block sets the settings of the optimization. Ideally both the resistance and capacitance optimizations are ran in parallel and the ADS PIN diode model simulates the vendor diode in all modes of operation. However, depending on the PIN diode chosen, and due to some limitations in the ADS model and optimization, often times this parallel optimization results in too large of an error. To combat this, multiple models would need to be created. Generally, there is one model for the forward biased PIN diode, where the resistance goals are weighted more heavily, and one model for the reverse biased PIN diode, where the capacitance goals are weighted more heavily.

The schematic for the forward bias optimization is shown in Figure 3.12.

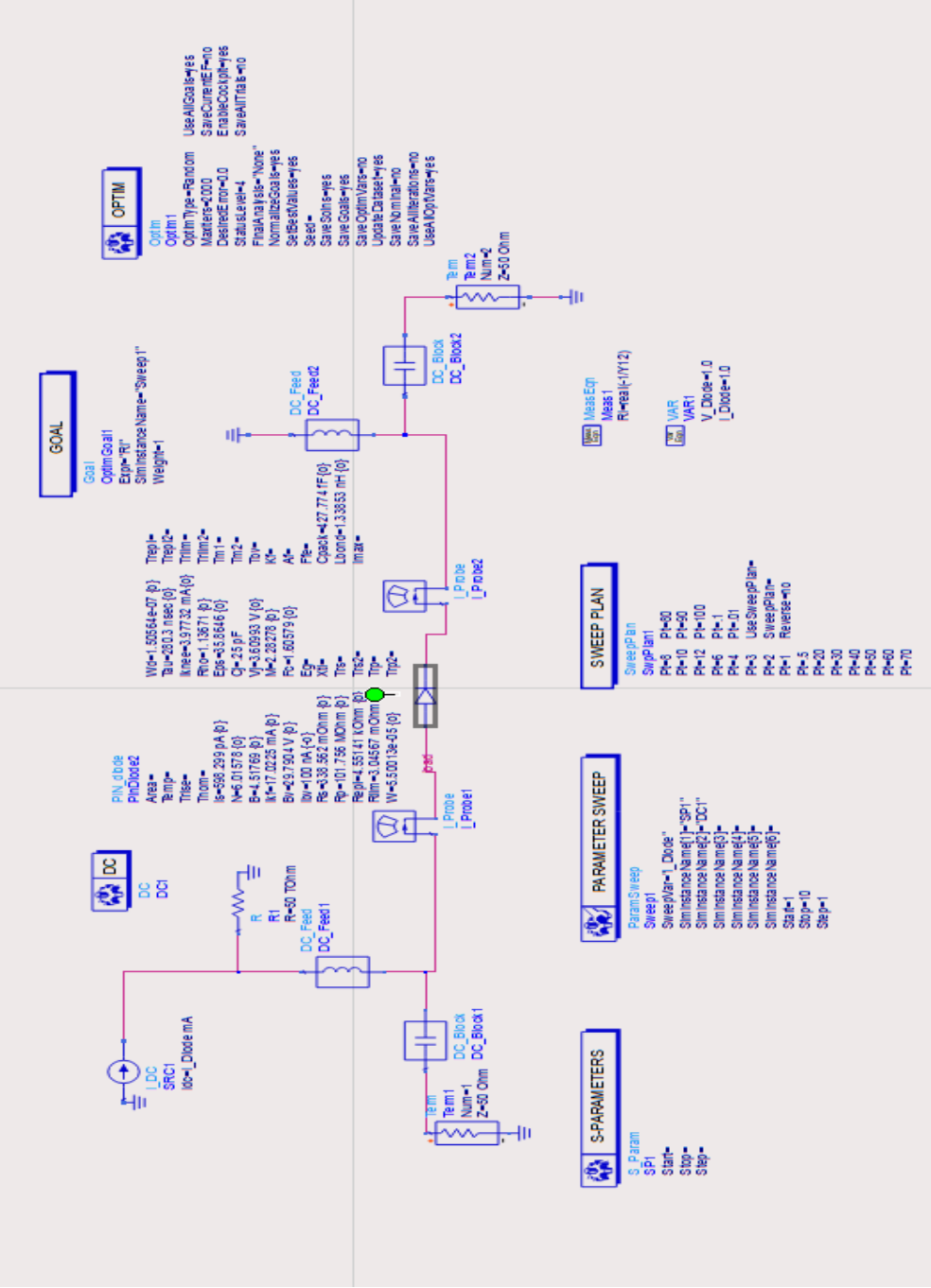

Figure 3.12: Forward Biased PIN Diode Optimization Schematic. Identical to the schematic for testing of the PIN diode resistance vs the forward bias current with a few added optimization blocks. Goal block sets the desired resistance values (taken from the data sheet); Optimization block sets the optimization parameters such as optimization type, number of iterations, etc.

The schematic for the reverse bias optimization is shown in Figure 3.13.

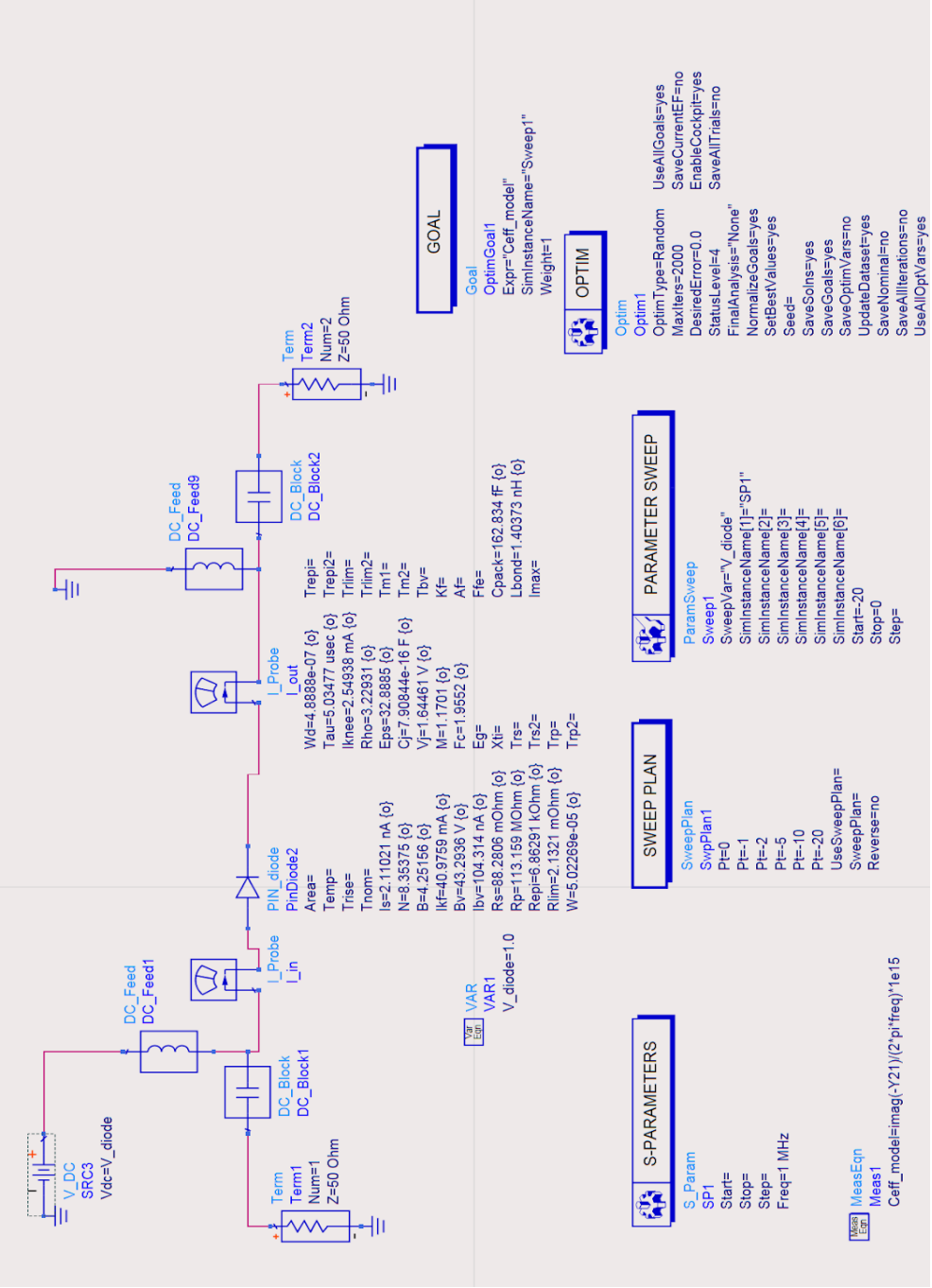

Figure 3.13: Reverse Biased PIN Diode Optimization Schematic. Identical to the schematic for testing of the PIN diode capacitance vs the reverse bias voltage with a few added optimization blocks. Goal block sets the desired capacitance values drawn from the data sheet; Optimization block sets the optimization parameters such as optimization type, number of iterations, etc.

The respective models are placed according to where there should be "ON" and "OFF" PIN diodes, resulting in an accurate simulation. For accurate switching and power handling simulations, other models are optimized specifically for those parameters. This is done similarly to the resistance and capacitance optimizations, simply by adding optimization and goal blocks to the respective schematics discussed in the model verification.

Note that in all these models, pad parasitics were assumed to be represented in the datasheet results.

3.3 Component Selection

A large contribution to the performance of the design is the selection of components, mainly the PIN diode as well as the bias tee.

3.3.1 PIN Diode Selection

As stated earlier, this design calls for capacitance below 1 nF to ensure an off state and an open circuit at the upper end of the 2-18 GHz bandwidth. A low resistance is also needed for impedance matching purposes to get a high impedance match at higher frequencies, which is explained more in detail in the Star Configuration section later in this chapter. Note also that this design uses a 0402 SMT PIN diode.

After some research, the Microsemi GC4271 PIN Diode was chosen. The datasheet, shown in Appendix B, states "The GC4200 series are high speed (cathode base) PIN diodes made with high resistivity epitaxial silicon material. These diodes are passivated with silicon dioxide for high stability and reliability and have been proven by thousands of device hours in high reliability systems." It is able to operate up

to 18 GHz with a low capacitance of 0.1 pF (at $V_R = 10$ V) as well as a low series resistance of 1.0 Ω (at $I_f = 20$ mA).

3.3.2 Bias Tee Selection

The bias tee includes a DC blocking capacitor and an RF choke to pass DC bias current while blocking RF signals. The DC bias voltage needed to control the PIN diode's mode is a function of the diode as well as the RF signal level, temperature range, and other factors. This bias voltage must be decoupled from the RF signal and be stable, as any noise or ripple will affect the diode's operating point.

Two options were considered. One was to construct a bias tee out of independent SMT components. However, due to its simplicity and strong performance, a vendor manufactured MACOM bias tee network (MABT-011000) is used, shown in Figure 3.14. See Appendix C for its datasheet.

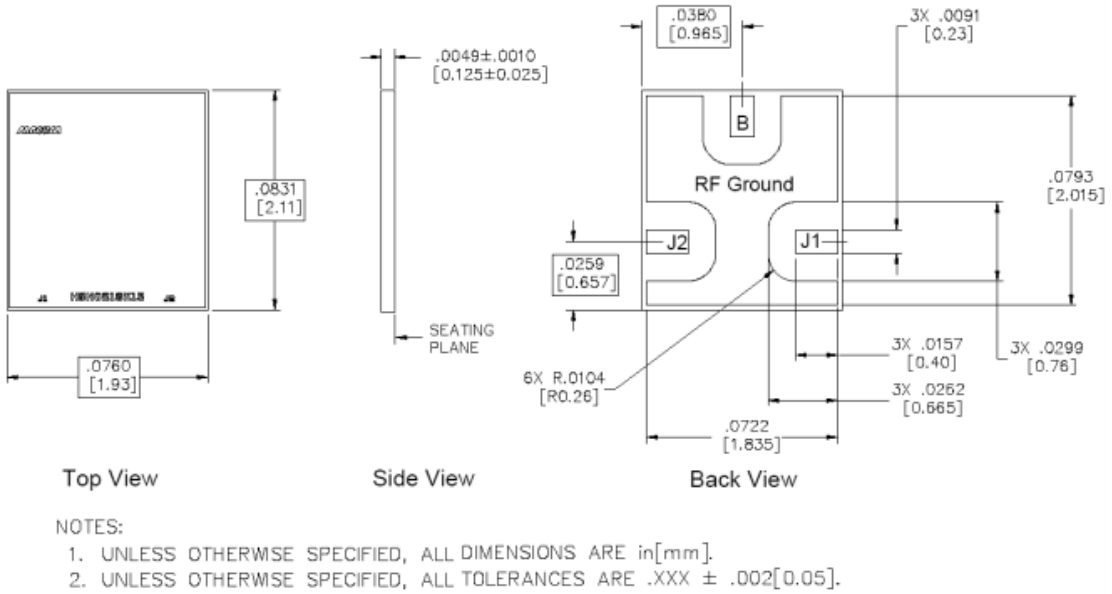

Figure 3.14: MABT-011000 Bias Tee Footprint Outline. Input J1, Output J2, Bias Voltage B.

The MABT-011000 datasheet states it is broadband, from 2 to 18 GHz. It also claims it is "suitable for the DC biasing of PIN diode control circuits. It functions as an RF-DC de-coupling network as well as the DC return and contains a series DC blocking capacitor." The functional schematic for this design is shown in Figure 3.15 and is exactly what this design calls for.

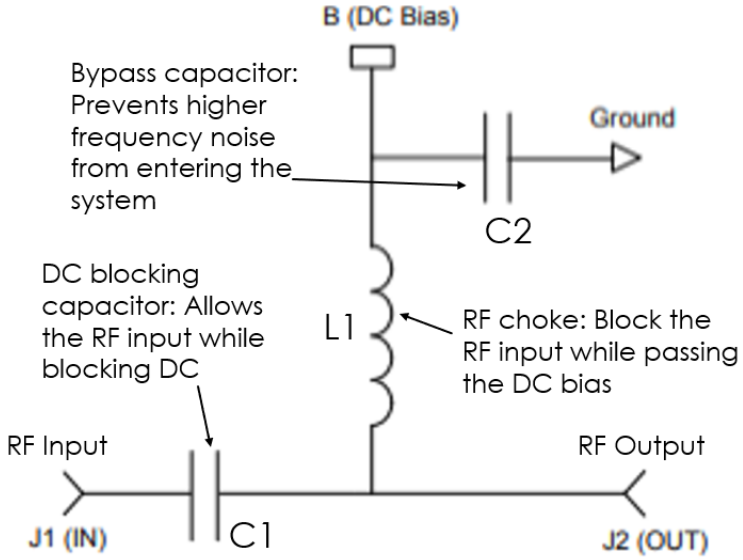

Figure 3.15: MABT-011000 Bias Tee Functional Schematic. DC Blocking Capacitor C1, RF Choke L1, Bypass Capacitor C2.

In order to simulate this part, the provided vendor .s3p file is used in the s3p block in ADS schematic.

3.4 Transmission Line Type

Two possible transmission lines were considered for this design, microstrip and coplanar. The design is a loose coplanar structure with adjacent ground plane. This transmission line was chosen for several reasons. First, this switch reaches high frequencies, up to 18 GHz, meaning it calls for the coplanar's lower loss tangent and dielectric constant stability through the GHz range. The gap between the transmis-

sion line and ground allows for a seamless path for the shunt diode, with its anode connected to the conducting wire and its cathode connected to ground. It also allows for the transmission line to be thinner than a standard microstrip, which leads to less coupling.

3.5 Substrate Selection and Transmission Line Dimensions

The first factor to consider when selecting a substrate is the mechanical 3D structure of the board. The substrate thickness must be sufficient to ensure a mechanically stable device, such that it does not snap easily. Second, this substrate thickness, as well as the dielectric constant and coplanar ground spacing, determine the width of the transmission lines on the board. This is of great importance since thinner lines minimize coupling.

Three different substrates were considered, RT Duroid 5880, RO4350B, and RO3006. Note that all three are Rogers substrates in contrast to the more common FR-4 material. Rogers substrates have lower loss tangent and less variation in dielectric constant with increase in frequency, allowing for use into the GHz range. A comparison of signal loss in FR4 and signal loss in a Rogers material RO4350B is seen in Figure 3.16.

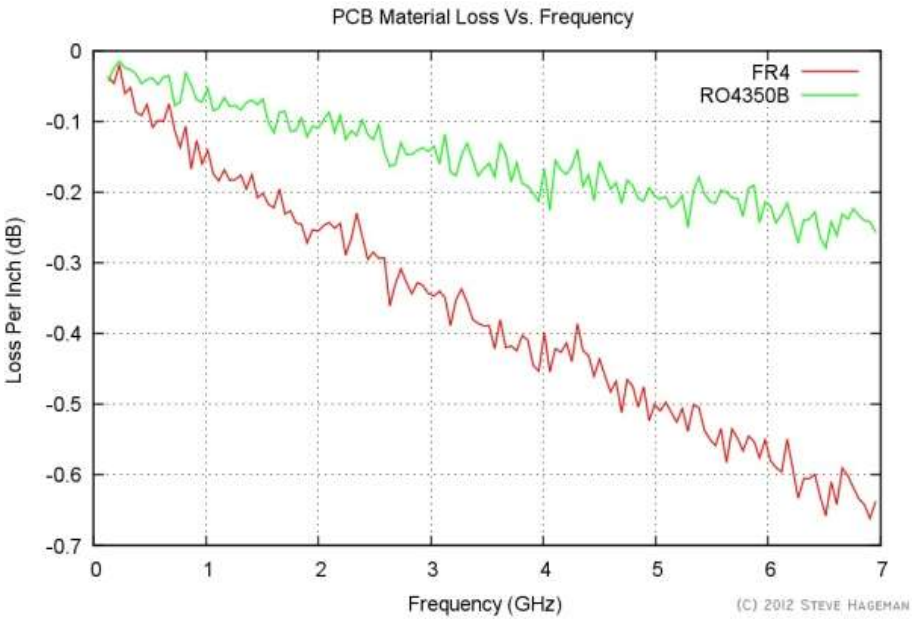

Figure 3.16: $|S21|$ Per Inch of Substrate Material (dB) vs. Frequency (GHz); FR4 substrate experiences more loss as frequency increases than Rogers 4350B substrate.

The material parameters, substrate thickness, line width, and desired characteristic impedance are all related through the following equation:

$$Z_o = \frac{60.0\pi}{\sqrt{\epsilon_{eff}}} \frac{1.0}{\frac{K(k))}{K(k')} + \frac{K(kl))}{K(kl')}} \tag{3.1}$$

where:

- K() is the elliptical integral function, where $K(k) = \frac{\pi}{2} \sum_{n=0}^{\infty} \left[\frac{(2n-1)!!}{(2n)!!} \right]^2 k^{2n}$
- $k = \frac{W}{W+2s}$
- $k' = \sqrt{1.0 - k^2}$
- $kl' = \sqrt{1.0 - kl^2}$
- $k1 = \frac{tanh(\frac{\pi W}{4.0h})}{tanh(\frac{\pi (W+2s)}{4.0h})}$

- $\varepsilon_{eff} = \frac{1.0+\varepsilon_r \frac{K(k')}{K(k)} \frac{K(kl))}{K(kl')}}{1.0+\frac{K(k')}{K(k)} \frac{K(kl))}{K(kl')}}$

Note that W is the width of the signal line, S is the spacing between the signal plane and adjacent ground plane, h is substrate height, and t is trace height, as shown in Figure 3.17.

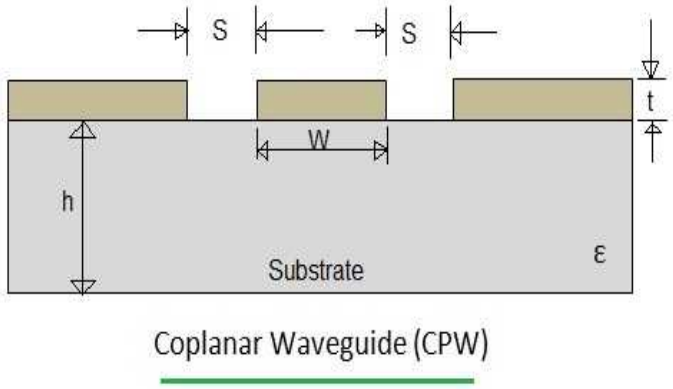

Figure 3.17: Cross-Sectional View of Coplanar Waveguide with Defined Lengths. *W* is the width of the signal line, *S* is the spacing signal plane and adjacent ground plane spacing, *h* is the substrate height, *t* is trace height.

While these equations prove to be quite complex and also allow for an infinite amount of solutions, the ADS Controlled Impedance Line Designer tool is used to streamline the process. A substrate thickness of 20 mil was chosen as a balance between sufficient thickness to maintain board integrity while still allowing for appropriate trace width to navigate and route on the board while maximizing spacing of the lines. The clearance, or spacing to the adjacent ground plane, was set to 10 mil to provide a seamless path for the shunt 0402 PIN diode to ground while also resulting in a reasonable line width. The resulting widths for the different substrates calculated in ADS Controlled Impedance Line Designer is shown below.

Figure 3.18 shows the resulting dimensions for the RT Duroid 5880.

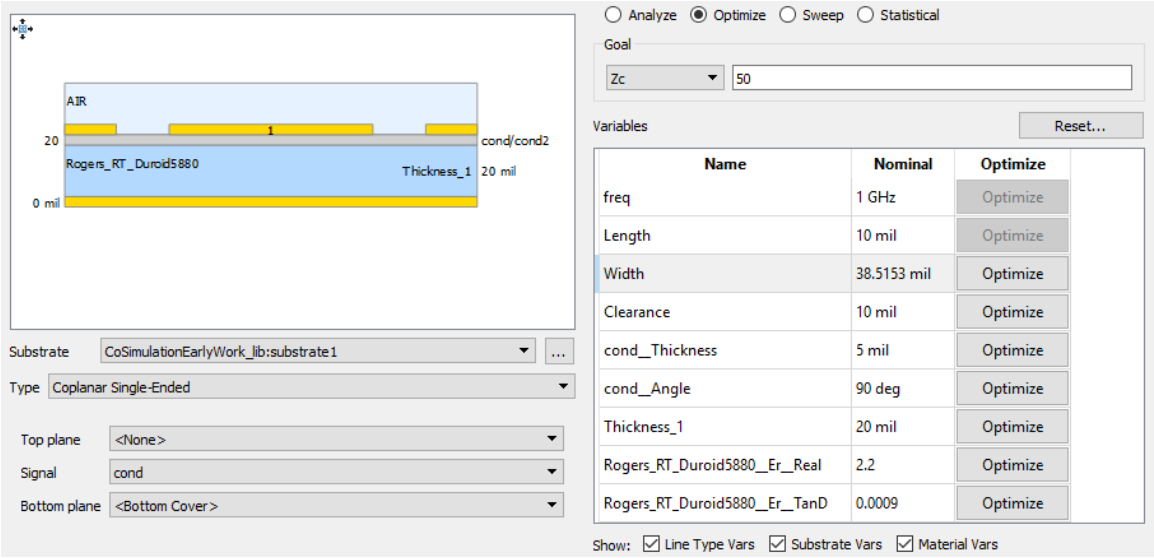

Figure 3.18: RT/Duroid 5880 Coplanar Waveguide Dimensions. Dielectric constant 2.2, maximizes line width: 38.5 mils.

Figure 3.19 shows the resulting dimensions for the RO3006.

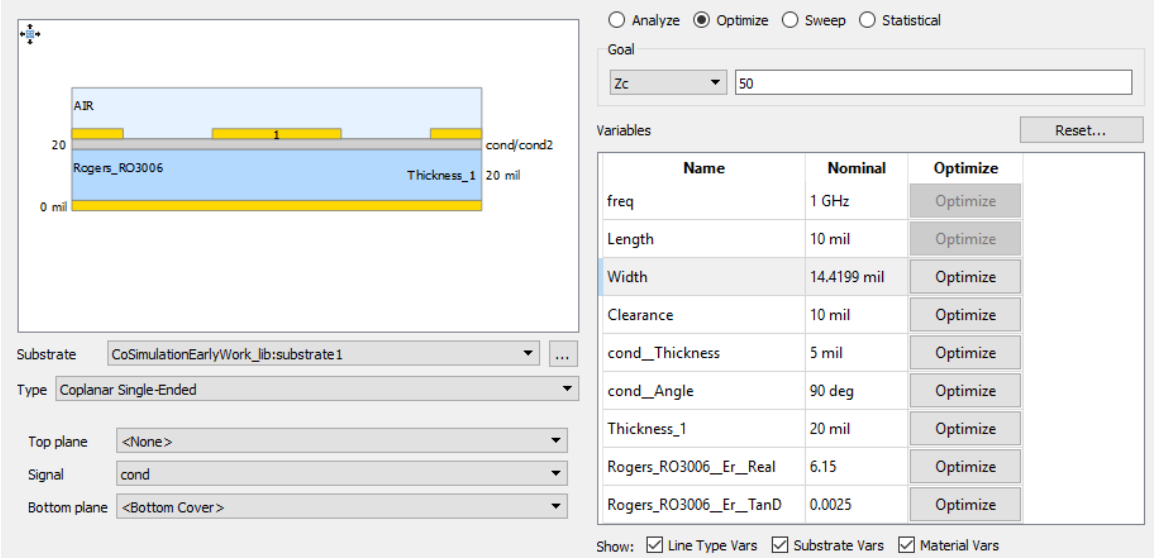

Figure 3.19: RO3006 Coplanar Waveguide Dimensions. Dielectric constant 6.15, minimizes line width: 14.42 mils.

Figure 3.20 shows the resulting dimensions for the RO4350B.

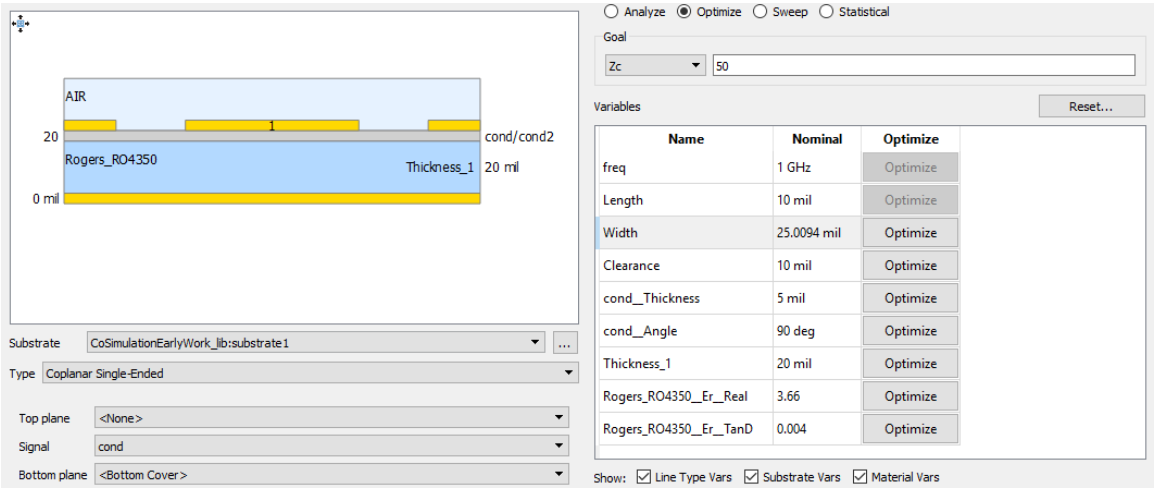

Figure 3.20: Rogers 4350B Coplanar Waveguide Dimensions. Dielectric constant 3.66, yields 25.01 mil line width.

The RO4350B material was used in this design (datasheet shown in Appendix D). This Rogers material has low signal loss and minimal dielectric variation up to 18 GHz and the dielectric constant of 3.66 (with a board thickness of 20 mil) yield a line width of 25.01 mil, thin enough to reduce coupling between the lines to reach the isolation specification of -30 dB.

Once the substrate material and thickness, as well at the transmission line type and dimensions are chosen, the transmission lines can be laid out and the star network configuration is designed.

3.6 Star Configuration

The star configuration is a type of switch architecture where the input and outputs all branch to one common node, with each branch consisting of a series diode and shunt diode. The switch based on PIN diodes needs a DC blocking capacitor to prevent the DC bias current from reaching the RF output and an RF choke to provide a path for the DC bias current to return while blocking the RF signal.

This configuration can vary with the number of branches, meaning the SP8T switch can be constructed with two four output star networks, one eight output star network, or another similar configuration. As the number of branches increases, the star network density increases coupling between transmission lines and outputs. This coupling is modeled in ADS by performing an FEM simulation. First the layout with the coplanar lines arranged in a star network is created.

The first design tried to incorporate all the branches into one node, meaning the input and all eight outputs are connected to the same star junction node. However, it became apparent very quickly that this caused too much crowding of the lines unless they were dropped to an unreasonably small width. Instead, the second approach of a one-to-two followed by a one-to-four switch was employed, as shown in Figure 3.21 below. The final size for this switch layout is 497x618 mil.

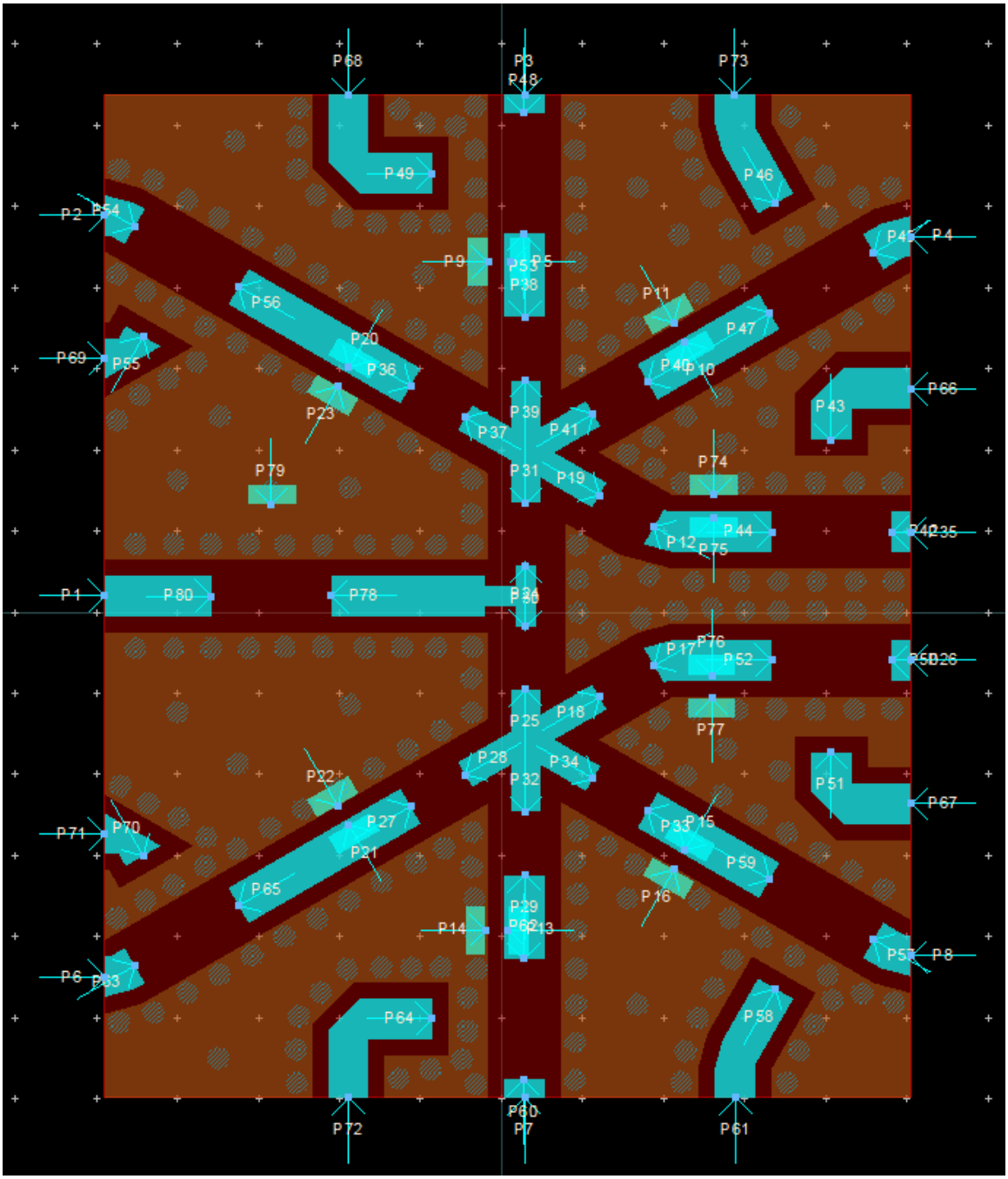

Figure 3.21: 8-way Star Network Layout. One input (middle left) to a 1x2 switch, each output to a 1x4 switch. Final size: 497 x 618 mils. PIN diodes and bias tee network connected at arrow ports in future simulations.

3.6.1 Transmission Line Spacing

The transmission lines in each 1x4 star are spread radially in an attempt to maximize spacing between the lines, as shown in Figure 3.22. Note that the space between the input and the adjacent outputs is larger than the two middle right outputs. This is due to the fact that there is always a signal going through the input line, while signal is only going through the two mentioned output lines if one of those outputs is ON. Therefore spacing between the input was valued more.

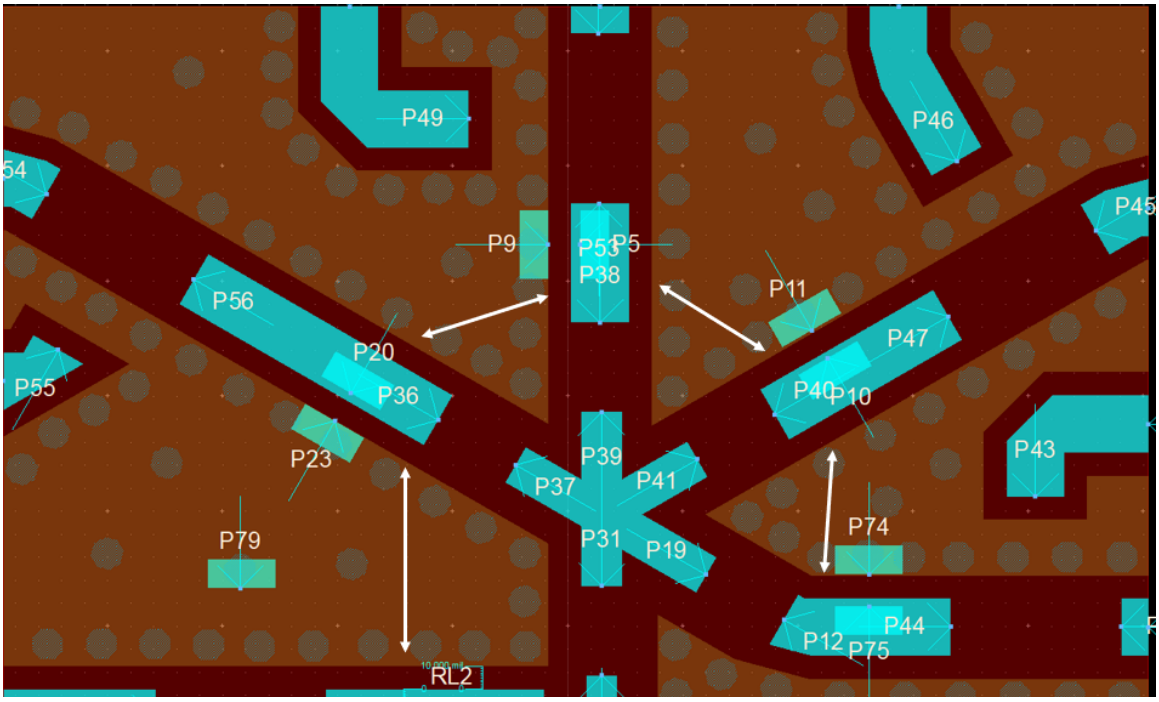

Figure 3.22: 1x4 Star Network Transmission Lines Spacing

3.6.2 Via Hole Spacing

Spacing of the via holes was also considered. If the ground vias are spaced at $\lambda/8$ or less, the ground plane will look like a solid ground. With the upper frequency limit of this device at 18 GHz, rounded up to 20 GHz, the maximum via spacing is 35 mil. Note that several are spaced closer together, as this is a maximum rating. For simulation purposes, the vias are drawn as octagons to save on simulation storage and time. Two vias and their spacing are shown in Figure 3.23.

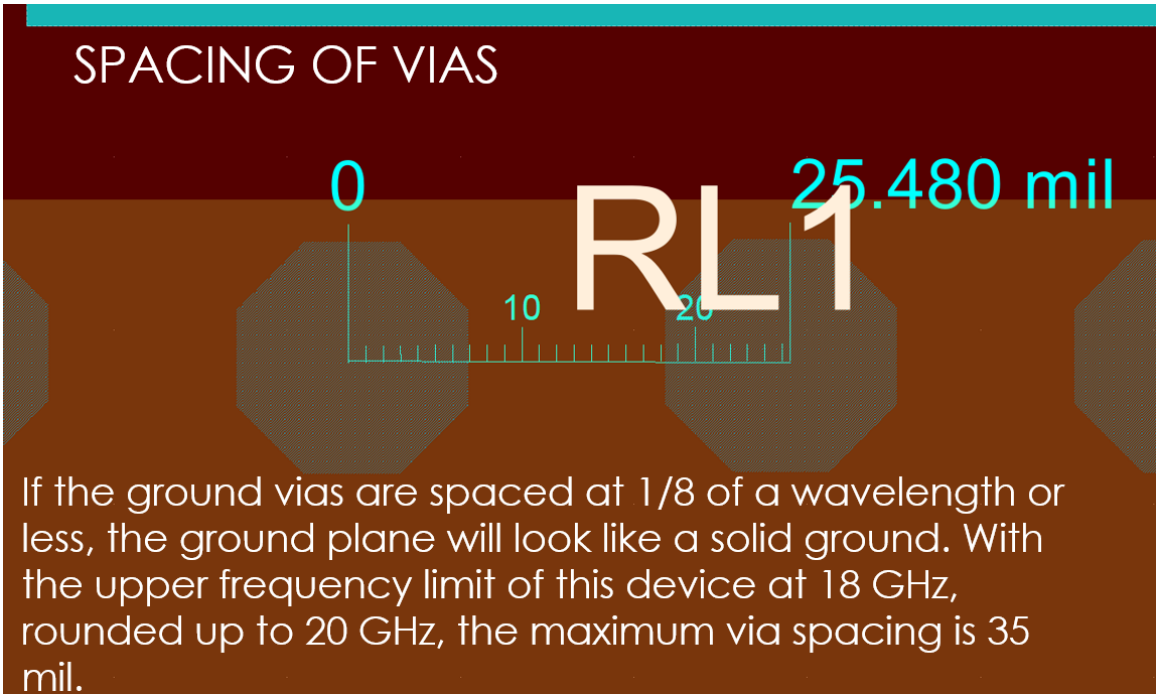

Figure 3.23: Via Hole Spacing. Set at ∼25.48 mil, significantly less than the maximum value of 35 mil.

3.6.3 Impedance Matching at Star Junction

Impedance matching was also a crucial design consideration. While the isolation is largely determined by the PIN diode capacitance, impedance matching at the center of the star to ensure the "OFF" outputs appear as open-circuits at the upper end of the bandwidth plays a large factor as well. This impedance matching was also considered at the 1x2 switch intersection. To analyze this, one output branch (assumed to be off) is shown in Figure 3.24 at 20 GHz, with an equivalent circuit shown in Figure 3.25. The corresponding impedances plotted on a Smith chart are shown in Figure 3.26.

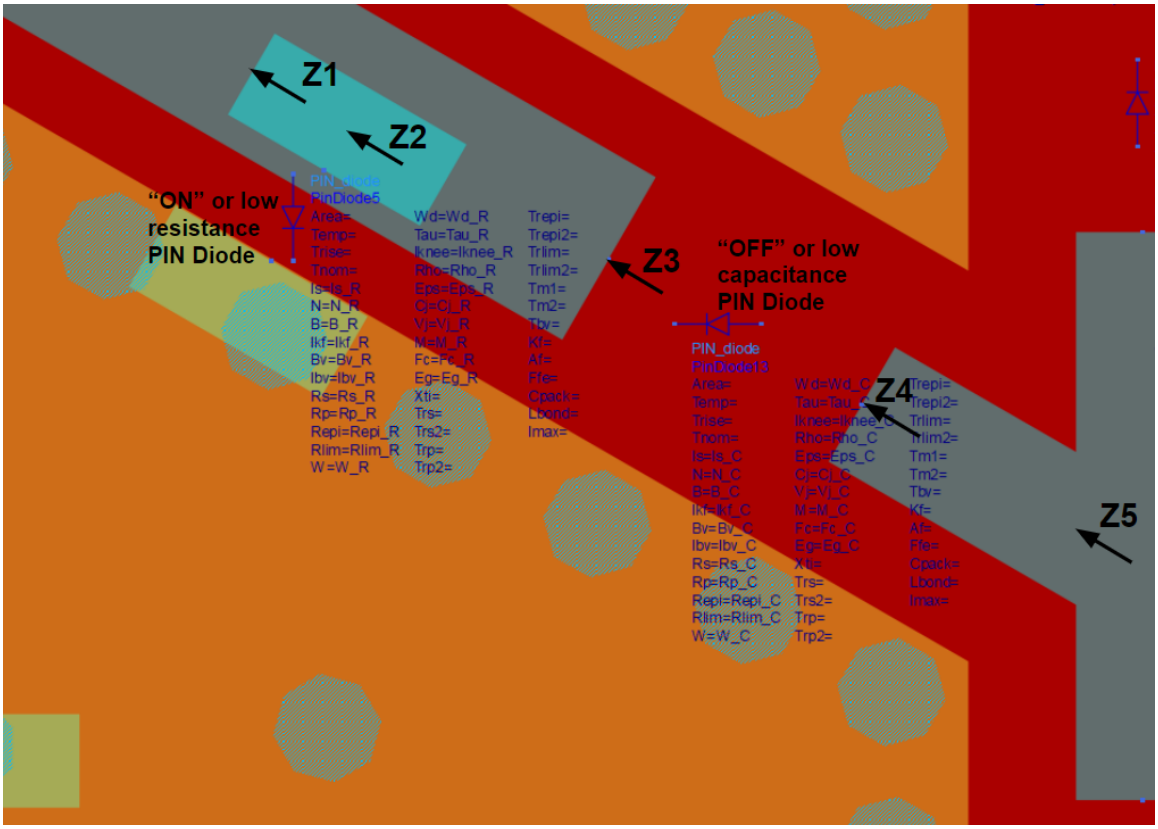

Figure 3.24: Equivalent Impedance across the Branch. Z1 equivalent impedance only the 50 Ohm line, Z2 adds the shunt PIN diode, Z3 adds extra transmission line length, Z4 adds the series PIN diode, Z5 adds extra transmission line length.

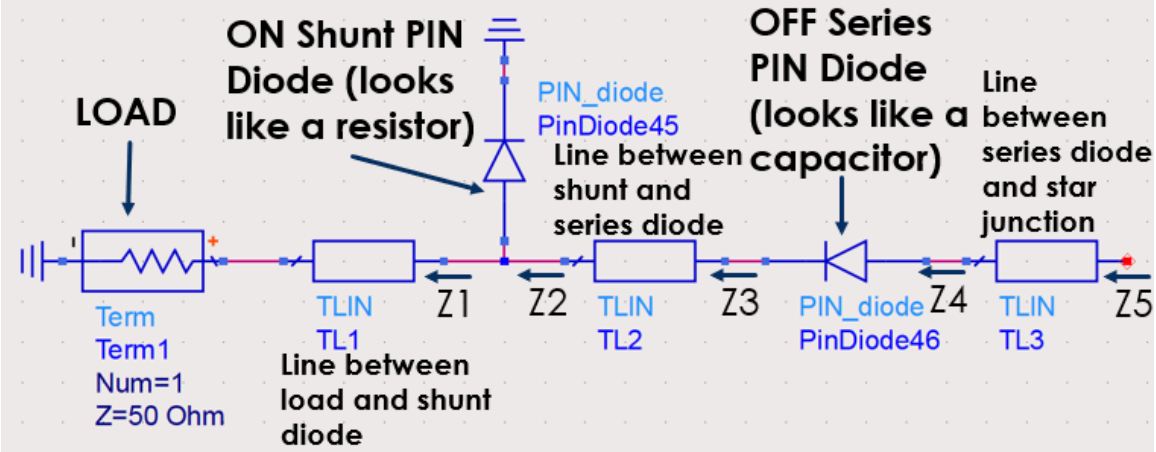

Figure 3.25: OFF Output Branch Equivalent Circuit

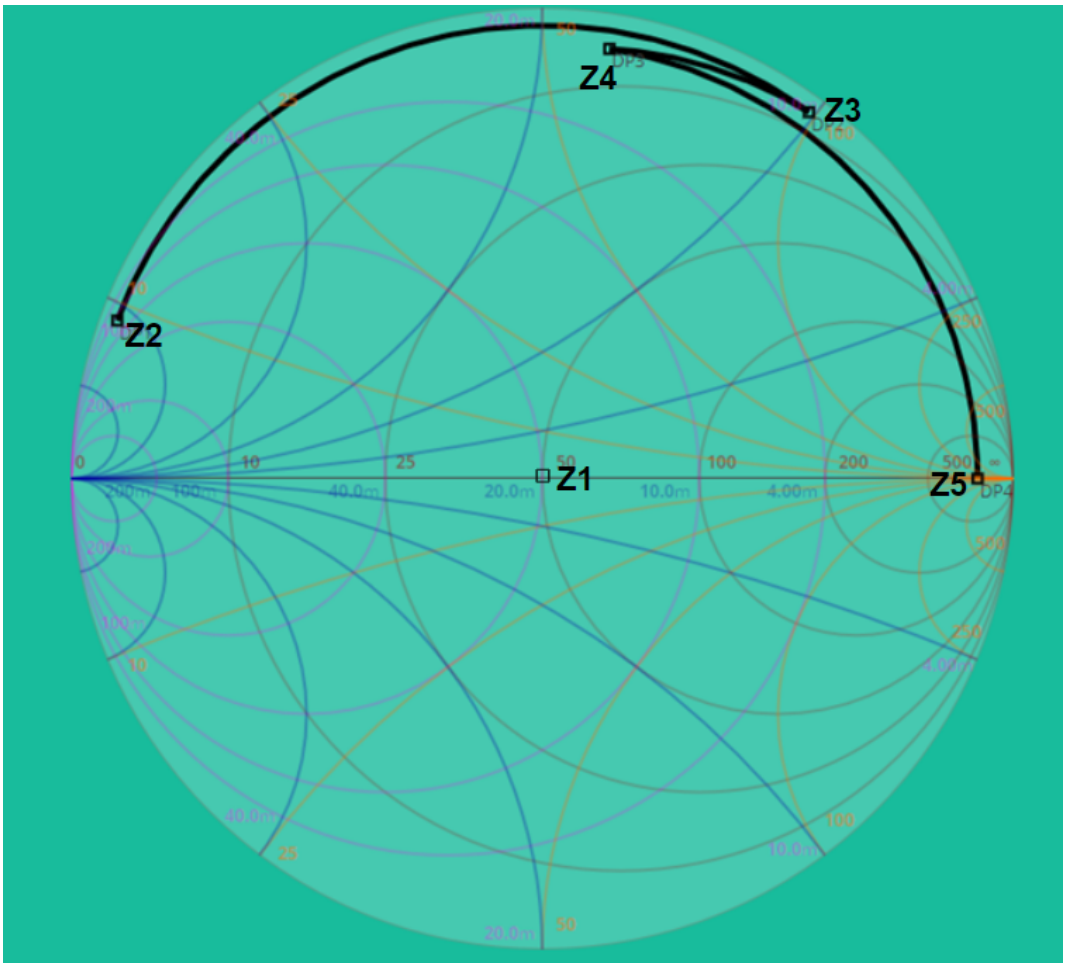

Figure 3.26: Equivalent Impedances Plotted on Smith Chart. Optimized such that Z5 resembles an open-circuit response, close to the right side of the Smith chart.

Z1 incorporates the transmission line with a characteristic impedance of 50 Ohms along with the bias tee. This point should be at the center of the Smith chart. Z2 then has the shunted "ON" PIN diode. This point should be at the left side of the Smith chart, a short to ground. Due to the series resistance as well as the parasitic capacitance and inductance of the PIN diode, this point has a resistance of approximately one Ohm and a reactance of approximately 10 Ohms. Z3 adds a small transmission line length, rotating the Z2 point clockwise with a constant radius/reflection coefficient. Z4 adds the series "OFF" PIN diode which works like a capacitor, rotating the Z3 point counterclockwise along the line of constant resistance. Finally, Z5 adds a small transmission line length, rotating the Z4 point clockwise.

The length between Z2 and Z3, between the series and shunt PIN diodes, along with the length of the star junction branch between Z4 and Z5, are both tuned with relation to the PIN diode parameter values to ensure Z5 is as far right on the Smith chart, as close to an open, as possible.

3.6.4 Transmission Line Width at Key Junctions

Another interesting design decision is seen with the widths of the transmission lines at both the 1x2 switch junction and the 1x4 switch junction. Note the smaller width at the end of the 1x2 switch. This is due to the characteristic impedance of the split. The input impedance sees this split and sees the equivalent as two parallel impedances. The width, and length to some degree, of this line was optimized to try to reduce this mismatch and maximize signal strength through this junction. The resulting layout at this junction is shown in Figure 3.27. The same applies for the 1x4 switch junction.

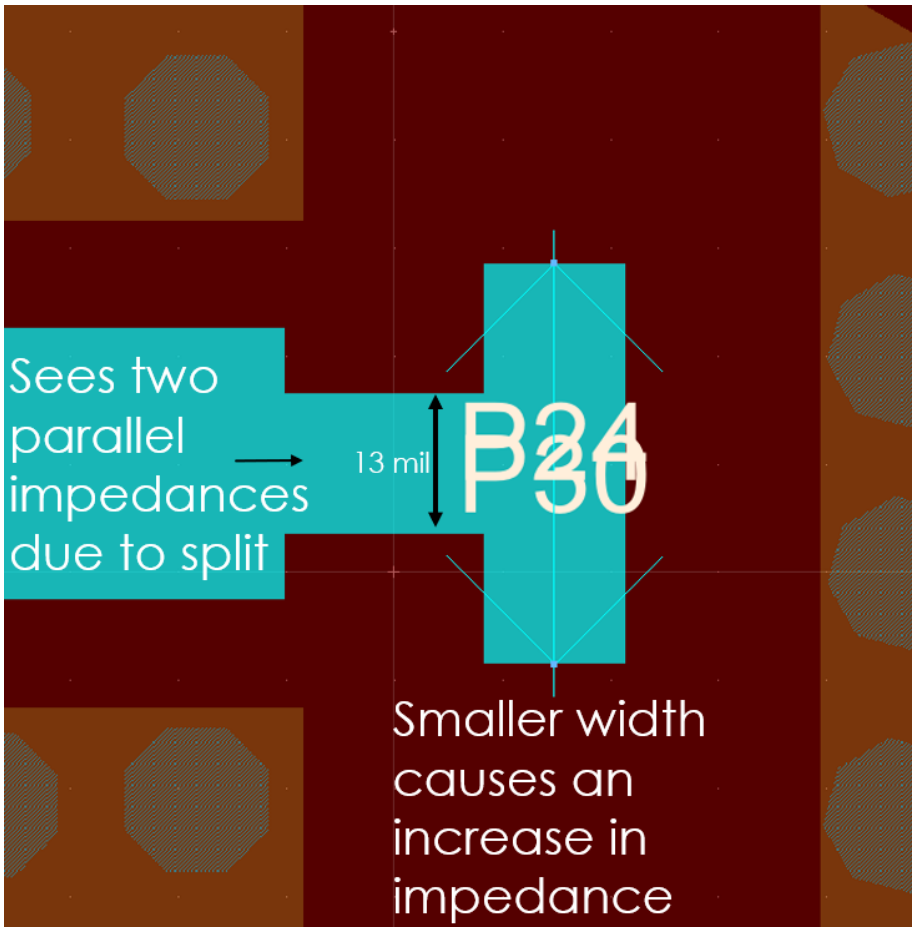

Figure 3.27: Transmission Line Width at 1x2 Switch Junction. Split causes a parallel impedance. Reduced width causes an increase in characteristic impedance.

3.7 Biasing Voltage Values

Another design consideration is the bias voltage. A higher positive voltage bias results in a lower series resistance, while a higher negative voltage bias results in a lower capacitance. All of the "OFF" outputs are given a positive voltage while the "ON" output is given a negative voltage. A negative voltage of -10V and a positive voltage of 5V is chosen. These values give the PIN diodes a low capacitance ($\sim$0.1pF) and resistance ($\sim$1 Ω), achieving the specifications.

The shunt diode, PIN1, on the "ON" output is forced into reverse bias with the negative voltage on the anode and ground on the cathode. The series diode, PIN2, on the "ON" output is forced into forward bias, causing a $\sim$1V drop across the diode, forcing -9V onto the middle 1x4 star junction. A similar analysis applies to the 1x2 ON PIN diode, PIN3, causing another $\sim$1V drop, forcing -8V onto the middle 1x2 junction. The positive voltages cause the shunt diode in the "OFF" outputs, such as PIN6 and PIN8, to be forward biased, grounding the signal and forcing $\sim$1V onto the node. With $\sim$1V on the cathode of the series PIN diode and -9V on the anode, the series PIN diodes on the "OFF" branches, such as PIN5, PIN7, and PIN9, are forced into reverse bias. Note that the other middle 1x4 star junction doesn't have any ON PIN diode to drive it to a certain voltage so it is a floating node that tends to stay at at a small voltage. An analysis of the voltages across the design are shown in Figure 3.28.

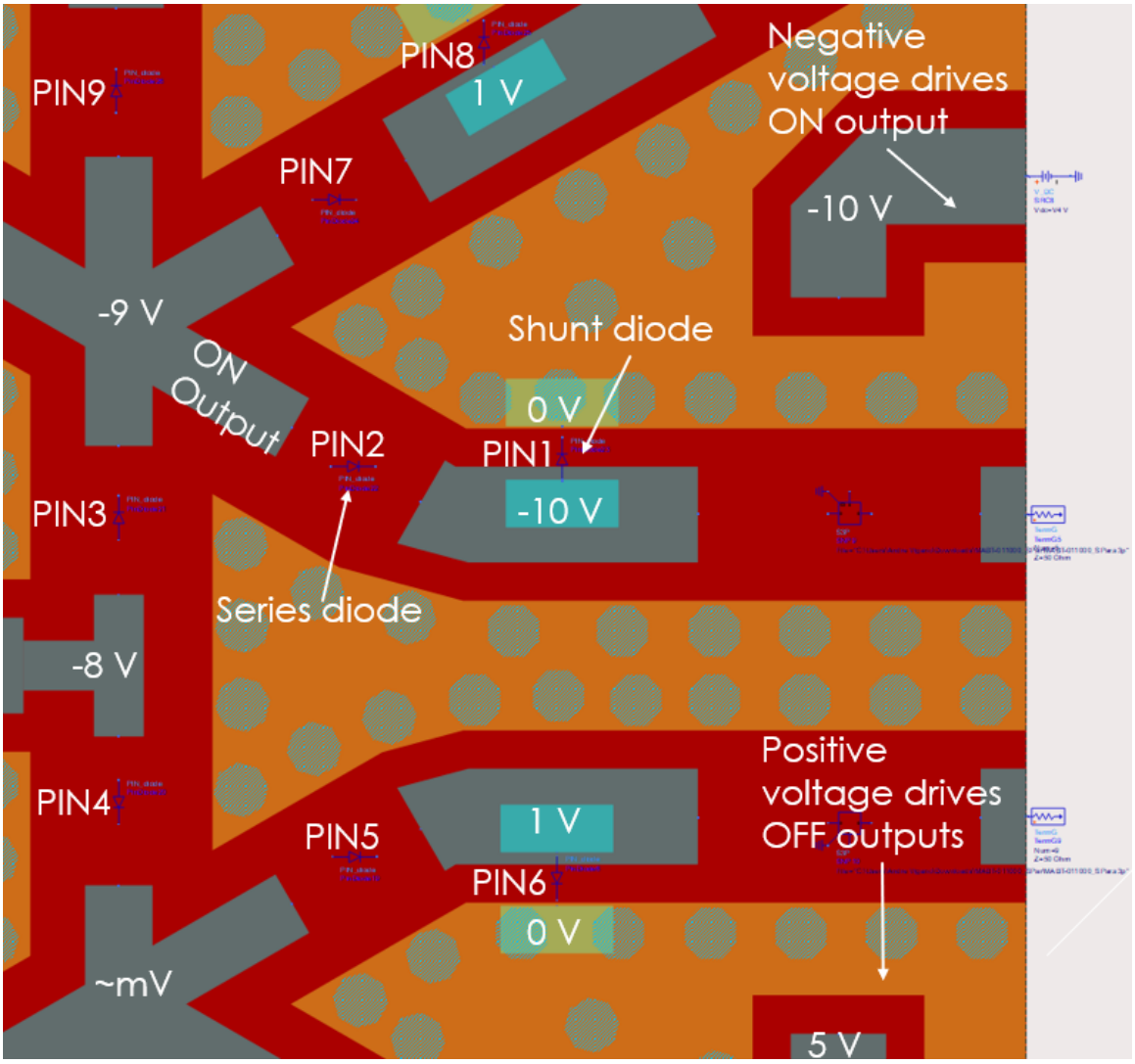

Figure 3.28: Voltages at Different Points in the Star Architecture. 1V drops across the ON PIN diodes (PIN2, PIN 3, PIN6, PIN8 seen in the figure), force all the PIN diodes into the desired modes of operation.

Now that the design is finished, including component selection, substrate dimensions and material selection, and geometry of the transmission lines and star network, a final EM simulation is ran in ADS layout to obtain the emData of the whole network.

Chapter 4

SIMULATION RESULTS

After the final layout design is simulated and the layout EM data is transferred to a models and input into a schematic, the PIN diode model and the bias tee are connected. A zoomed in view of the top star network is seen in Figure 4.1 while the full schematic is shown in Figure 4.2.

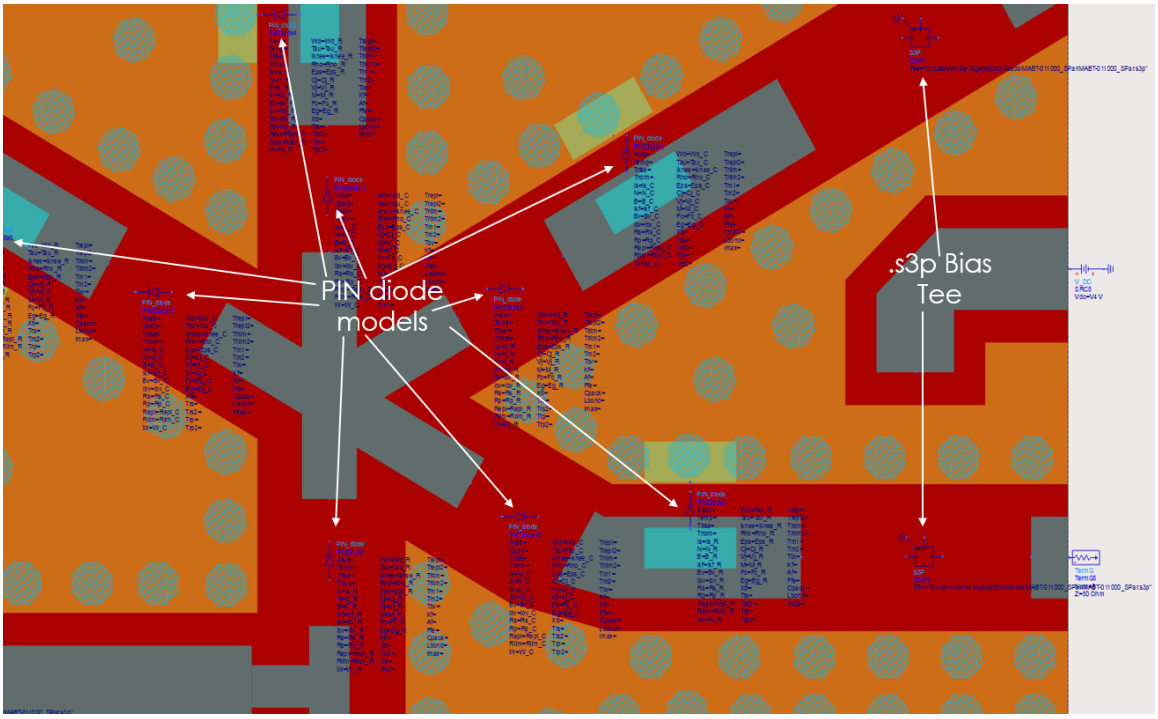

Figure 4.1: SP8T Switch, Zoomed In 2.5D EM Co-simulation. Includes PIN diode models and .s3p bias tee blocks.

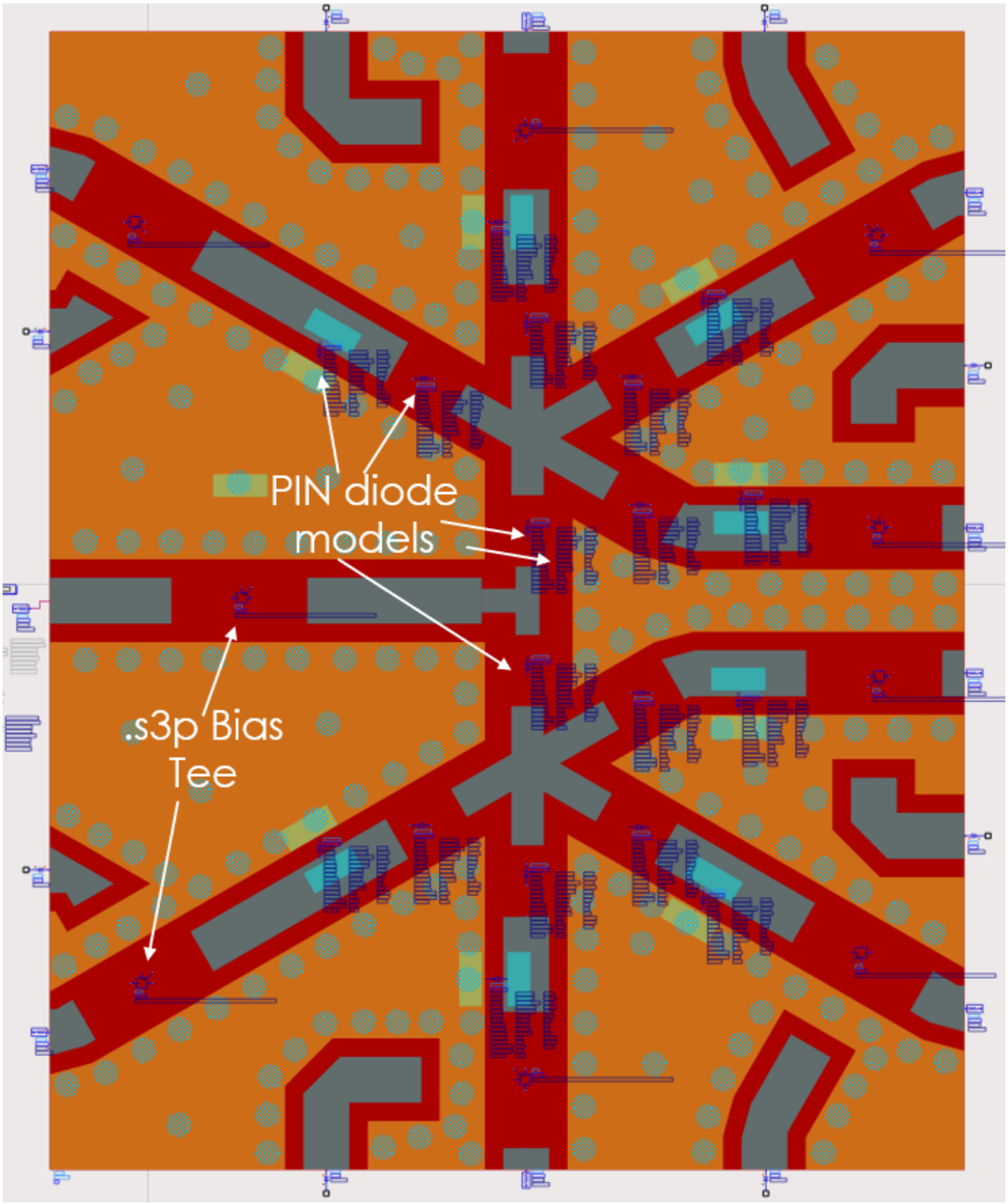

Figure 4.2: 2.5D EM Co-simulation of SP8T Switch. Includes PIN diode models and .s3p bias tee blocks.

This schematic was the baseline for several tests to determine the specifications of this switch in simulation, including insertion loss and isolation, power handling, and switching speed.

4.1 Insertion Loss and Isolation Results

Note that the PIN diode models for the forward bias and reverse bias modes are connected along the whole design such that the top right output, corresponding to term 4, is ON. The bias voltages are also set accordingly, with -10V on the ON output and 5V on all the OFF outputs. The simulation set up is shown in Figure 4.3. The insertion loss and isolation results of the final SP8T RF switch simulation are shown in Figure 4.4, with a zoomed in version of the insertion loss shown in Figure 4.5.

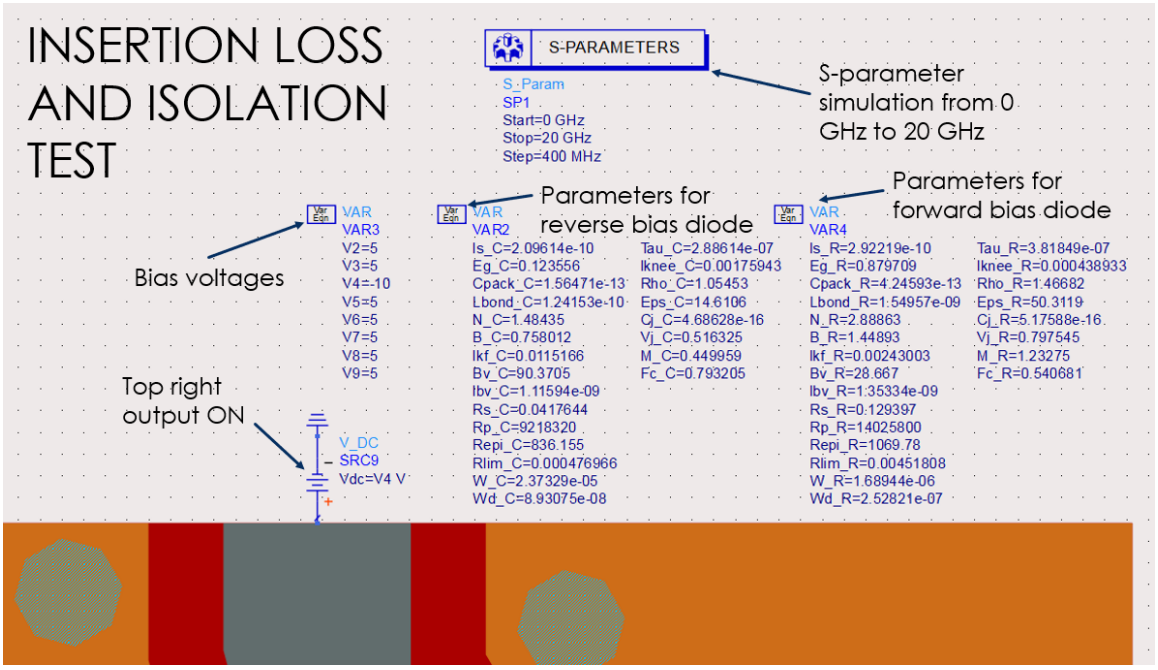

Figure 4.3: Insertion Loss and Isolation Test Set Up.

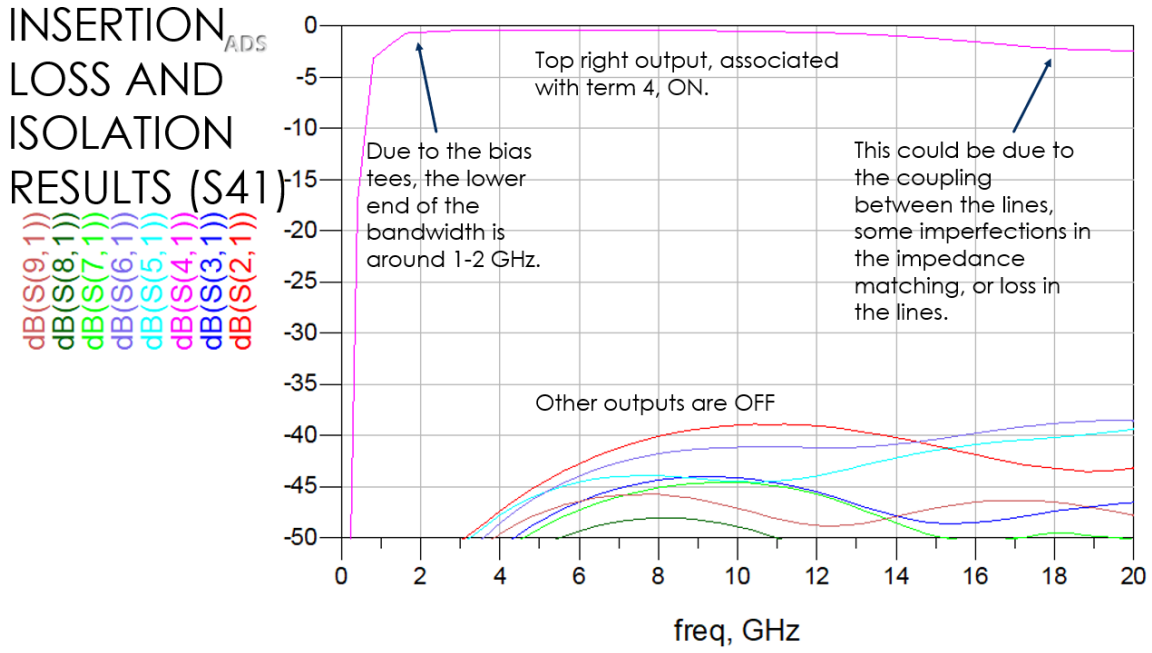

Figure 4.4: Insertion Loss and Isolation Results. S(4,1)Top right output, S(4,1), allows signal to pass while the rest are blocking the signal.

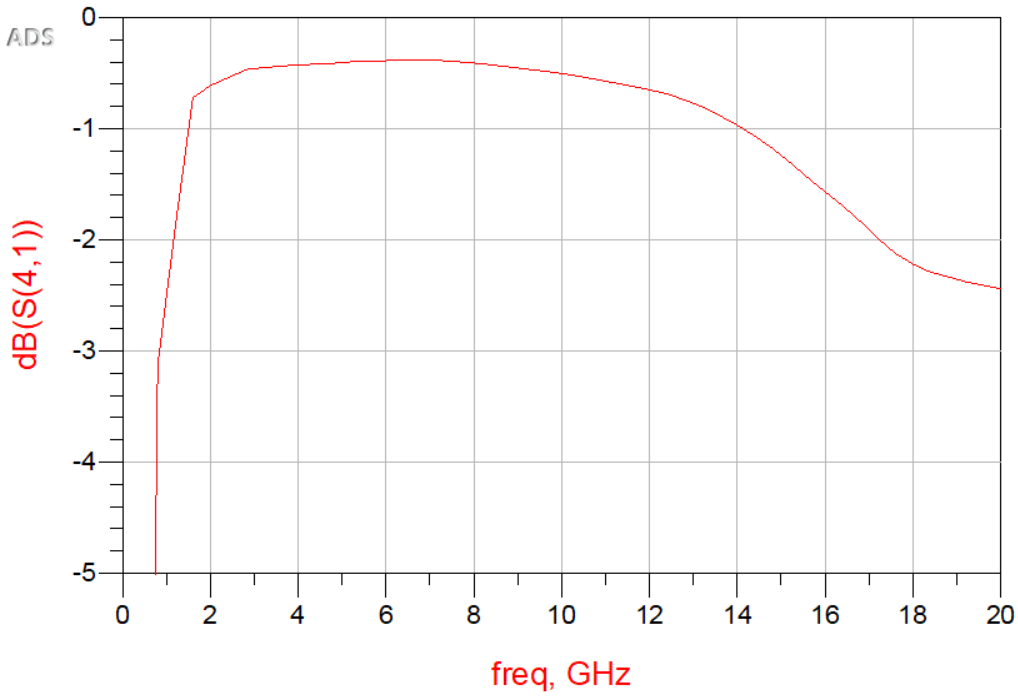

Figure 4.5: 2.5D EM Co-simulation S(4,1) Insertion Loss

The insertion loss for each output was observed. Figure 4.6 shows the results for the theoretical worst case scenario at the bottom right output of the top star network, corresponding to term 5, due to its proximity to the output branch below it, corresponding to term 6. The insertion loss at the upper end of the bandwidth is slightly worse in this case, approximately -4 dB, and it is clear the isolation from output 6, S(6,1) in the simulation, is the worst. However, it is still acceptable at approximately -35 dB. A zoomed in version of the insertion loss is shown in Figure 4.7.

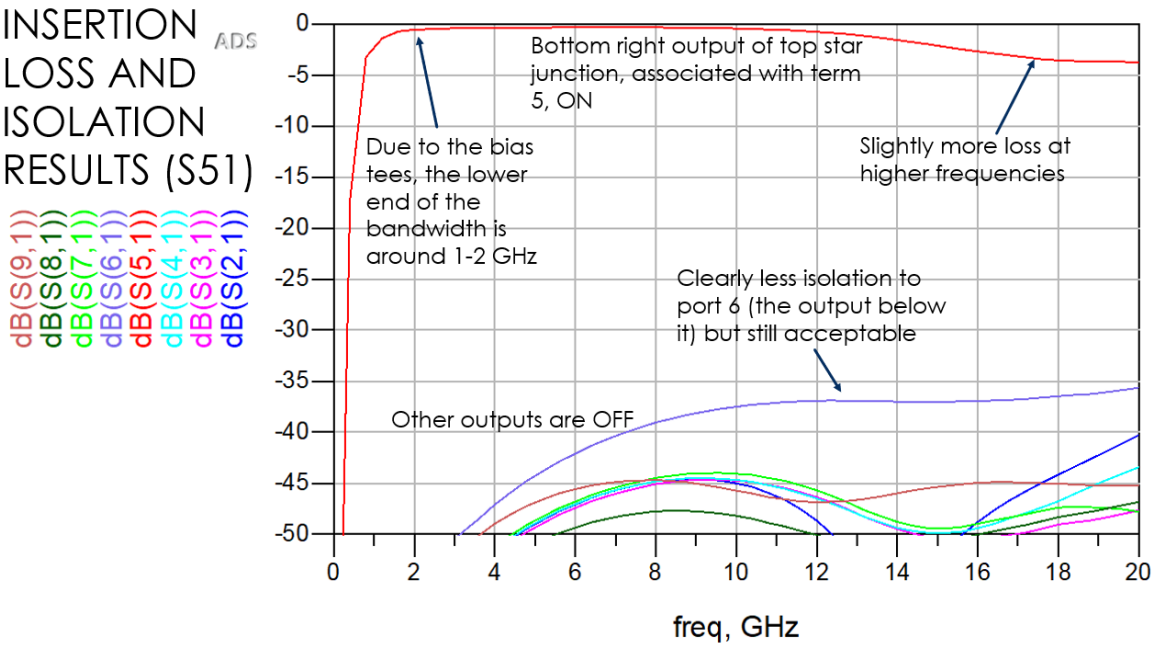

Figure 4.6: 2.5D EM Co-simulation Insertion Loss and Isolation. Note that S(5,1), which corresponds to the bottom right output of the top star network, is allowing signal to pass while the rest are blocking the signal.

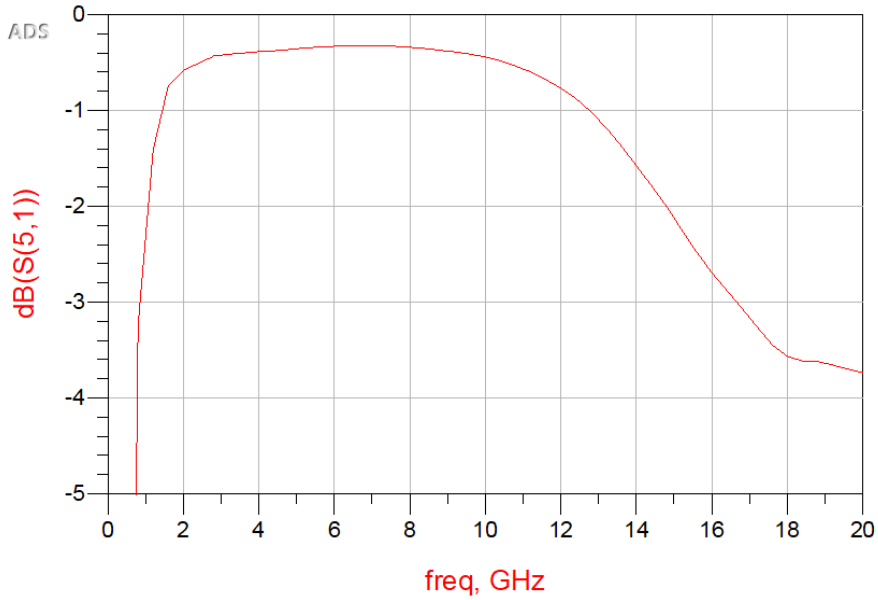

Figure 4.7: 2.5D EM Co-simulation Insertion Loss and Isolation. Bottom right output of the top star network, S(5,1), allows signal to pass while the rest are blocking the signal.

4.2 Power Handling Results

The power handling results were also promising. To obtain these results, an RF power source at 8 GHz was swept across various amplitudes at the input, with the resulting ON signal S(4,1) plotted versus the swept input power. Note that this does not incorporate temperature or overheating effects; it is only based on the bias current and the amplitude of the input signal. The simulation set up is shown in Figure 4.8. The resulting response is shown in Figure 4.9.

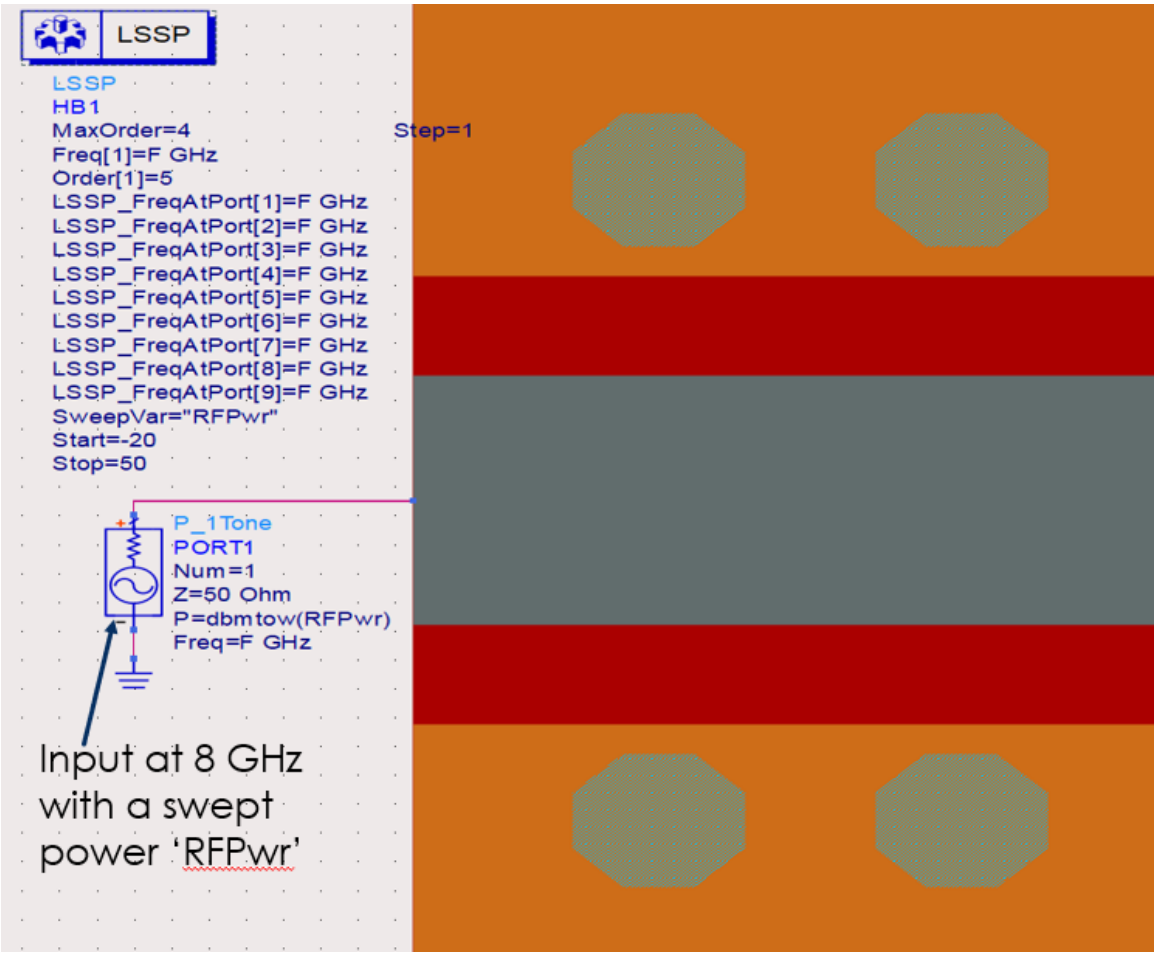

Figure 4.8: Power Handling Test Set Up. 8 GHz Input with Swept Amplitude.

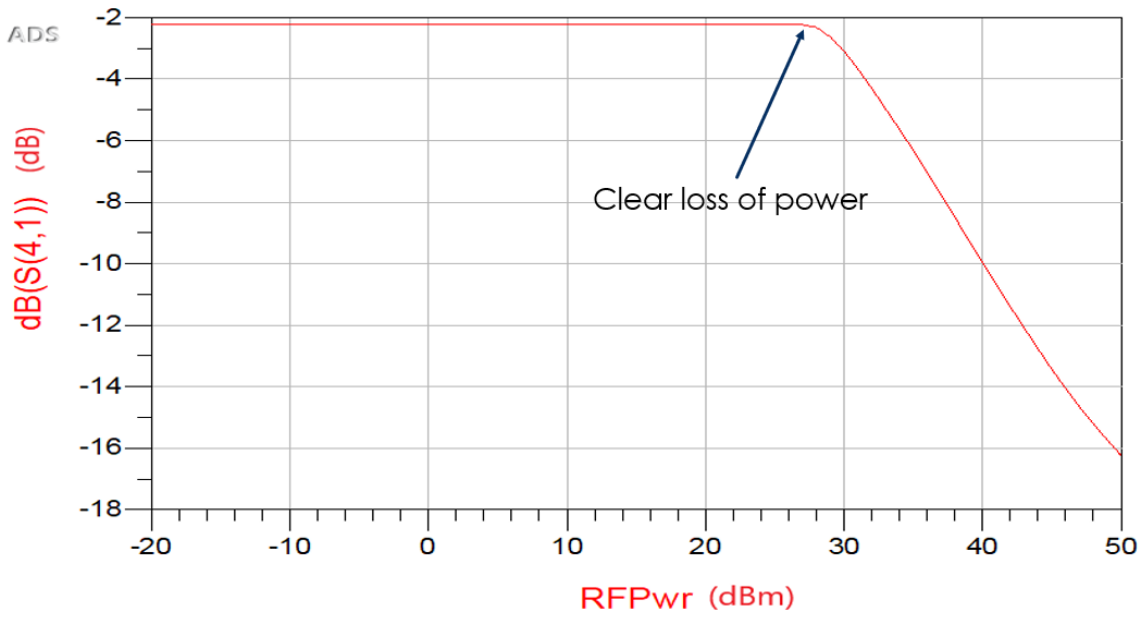

Figure 4.9: 2.5D EM Co-simulation Power Handling. S(4,1) holds a consistent value until the input RF power reaches 27 dBm, at which point the signal strength reduces. The current through the diode is estimated at 150 mA.

4.3 Switching Speed Results

The switching speed results were obtained by running a transient simulation with an input at 5 GHz and an amplitude of 1 V. A chosen output starts OFF, with a bias voltage of 5 V, and is then switched on by quickly switching the bias voltage to -10 V after 150 ns. The output signal is observed to see how long it take before it allows the signal through. The simulation set up is shown in Figure 4.10 with the results in Figure 4.11.

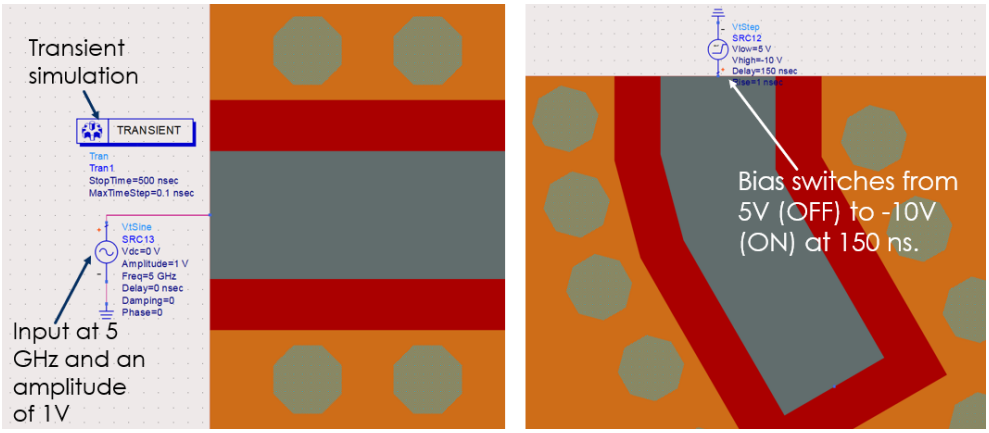

Figure 4.10: Switching Speed Test Set Up. 1V 5GHz Input Signal, Bias switches from 5V (OFF) to -10V (ON).

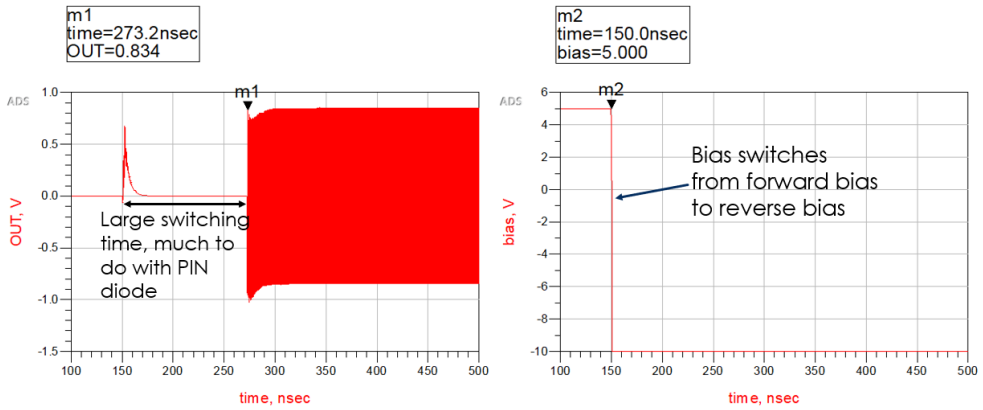

Figure 4.11: 2.5D EM Co-simulation Switching Speed. Right: Bias switching from 5V (OFF) to -10V (ON) at 150 ns, m1. Left: 5 GHz signal propagate through to output at 273.2 ns, m2, resulting in a 123.2 ns switching speed.

4.4 Final Simulation Results

The final results are shown in Table 4.1. These results show the insertion loss and isolation at different frequencies, the power handling, the switching speed, and the final size of the switch. The results are promising and resulted in an operating switch in simulation.

Table 4.1: SP8T Switch Simulation Results

PARAMETER	FREQ. BAND (GHz)	MIN	TYP	MAX
INSERTION LOSS (dB)	2 - 10	-	0.05	1
	10 - 14	-	1	1.5
	14 - 18	-	2	4
ISOLATION (dB)	2 - 10	38	42	-
	10 - 14	37	38	-
	14 - 18	35	39	-
POWER HANDLING (dBm)	-	-	27	-
SWITCHING SPEED (ns)	-	-	123.2	-

Chapter 5

CONCLUSIONS

Microwave/RF switches are one of the most widely used components in radar and communication systems with the main purpose of routing or blocking RF signals. While electromechanical switches were dominant many years ago, they have been superseded by solid-state solutions based on PIN diodes, FET switches, or a combination of components.

The PIN diode is a "simple" passive switching device with superior speed and isolation performance. Switch configuration (series, shunt, series-shunt) is selected to merge RF signals and DC bias. Detailed PIN diode models ensure accurate final circuit simulations.

This study simulates an 18 GHz SP8T RF Switch with eight series-shunt PIN diode switches configured in a star network. A comparison between simulations and required specifications are shown in Table 5.1 below.

Table 5.1: Simulation vs. Specifications Comparison

PARAMETER	FREQ. BAND (GHz)	MIN	TYP	MAX	REQUIRED
INSERTION LOSS (dB)	2 - 10	-	0.05	1	1
	10 - 14	-	1	1.5	1.5
	14 - 18	-	2	4	2
ISOLATION (dB)	2 - 10	38	42	-	30
	10 - 14	37	38	-	30
	14 - 18	35	39	-	30
POWER HANDLING (dBm)	-	-	27	-	23
SWITCHING SPEED (ns)	-	-	123.2	-	20
AC COUPLED	-	-	YES	-	YES
SIZE (mil)	-	-	497x618	-	500x500

The insertion loss at the upper end of the bandwidth drops below the specification by 2 dB. This could be due to the coupling between the lines, some imperfections in the impedance matching, or loss in the lines. Isolation and power handling met the initial goal. The switch ended up slightly larger than anticipated, at approximately 500 mil by 620 mil. While this is larger than the initial goal, it is still small enough to be acceptable. Power handling was above what was required, at 27 dBm in comparison to the specification of 23 dBm. Switching speed, 123.2 ns compared to the 20 ns goal, is due to the 100 ns switching time for the selected PIN diode. Hence, this discrepancy is considered acceptable.

Potentially the largest obstacle in this study was attempting to model the chosen vendor PIN diode in ADS. It is still an issue to effectively model PIN diodes in any simulation software. The function of a PIN diode is quite complex, with the large intrinsic region and the physics of the charges in that region, especially when changing the mode of operation. This issue was amplified due to limited datasheet information for equivalent model development. Resistance and capacitance accuracy was difficult;

thus, two models were created. However, diode charge carrier lifetime, voltage drop, and temperature did not match actual PIN diode performance. Vendor test conditions to achieve the datasheet specifications may deviate from the optimizing test circuit used to create the diode model, increasing potential model inaccuracies. Model inaccuracy could require layout modifications, most notably impedance matching network dimensions to ensure an open at the OFF outputs.

This study started with the ADS simulation of an SP8T 18 GHz RF switch, but there is much future work to be completed, described in the following chapter.

Chapter 6

FUTURE WORK

The switch requires improvements including wider bandwidth, 1 GHz to 20 GHz, and insertion loss reduction to 2 dB. Simulation accuracy can also be enhanced by PIN diode model improvements. PIN diode lab testing and parameter extraction can improve model accuracy.

While this study focused on simulation of the SP8T switch, either this exact design or an improved design will be manufactured in the future as well. This process will involve several steps. The first is adjusting the layout to manufactured switch form, as opposed to a simulation layout. This includes adding the pads for the components, converting the vias from octagons to circles, more accurately placing the vias throughout the design, and potentially more. Once the layout is finished, it is exported to a Gerber file. ADS layout has an export feature to help with this. Note that the final SP8T switch will not be the only layout manufactured. Test fixtures for series, shunt, and series-shunt PIN diodes are required. Also, bias tee, short open load calibration, TRL calibration, and microstrip and coplanar through lines could be useful. These are all used to better understand the diode as well as other parts of the design.

All test fixtures are combined into one panel (see Figure 6.1) and exported. The user then separates the fixtures. Note that this is just an example of what test fixtures could populate the panel and not the final layout of each.

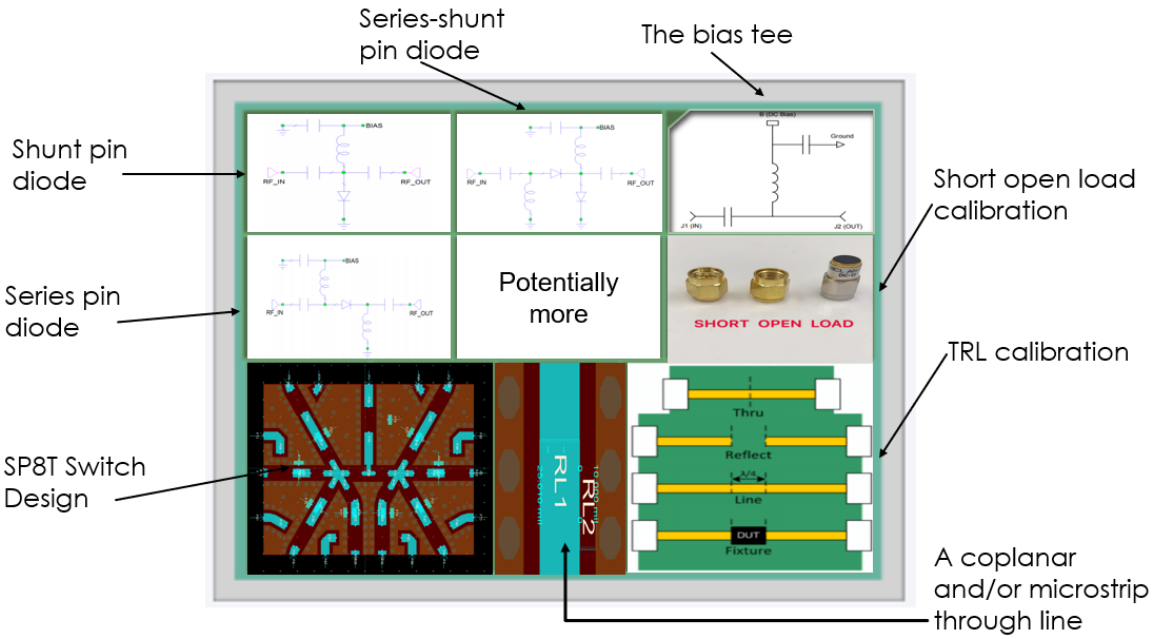

Figure 6.1: PCB Panel Layouts; SP8T design, Test Fixtures.

This Gerber file, along with a few definition files and readme files to clarify design and manufacturing processes, is sent to a PCB manufacturer such as Sunstone Circuits. Sunstone has the tools to manufacture this complex design; this includes the ability to manufacture such a small part as well as ability to manufacture with the desired high performance Rogers material.

One potential connector component used for testing is part 292-06A-6 made by Southwest Microwave (datasheet shown in Appendix E). It is essentially a clamp on SMA connector. This connector attaches to a 25 mil width trace. The specification states operation to 27 GHz, beyond the 18 GHz required switch bandwidth. The screw in/clamping allows for testing across the board with the same connector.

After testing the switch and its components, design improvements will be applied through simulations resulting in a new prototype.

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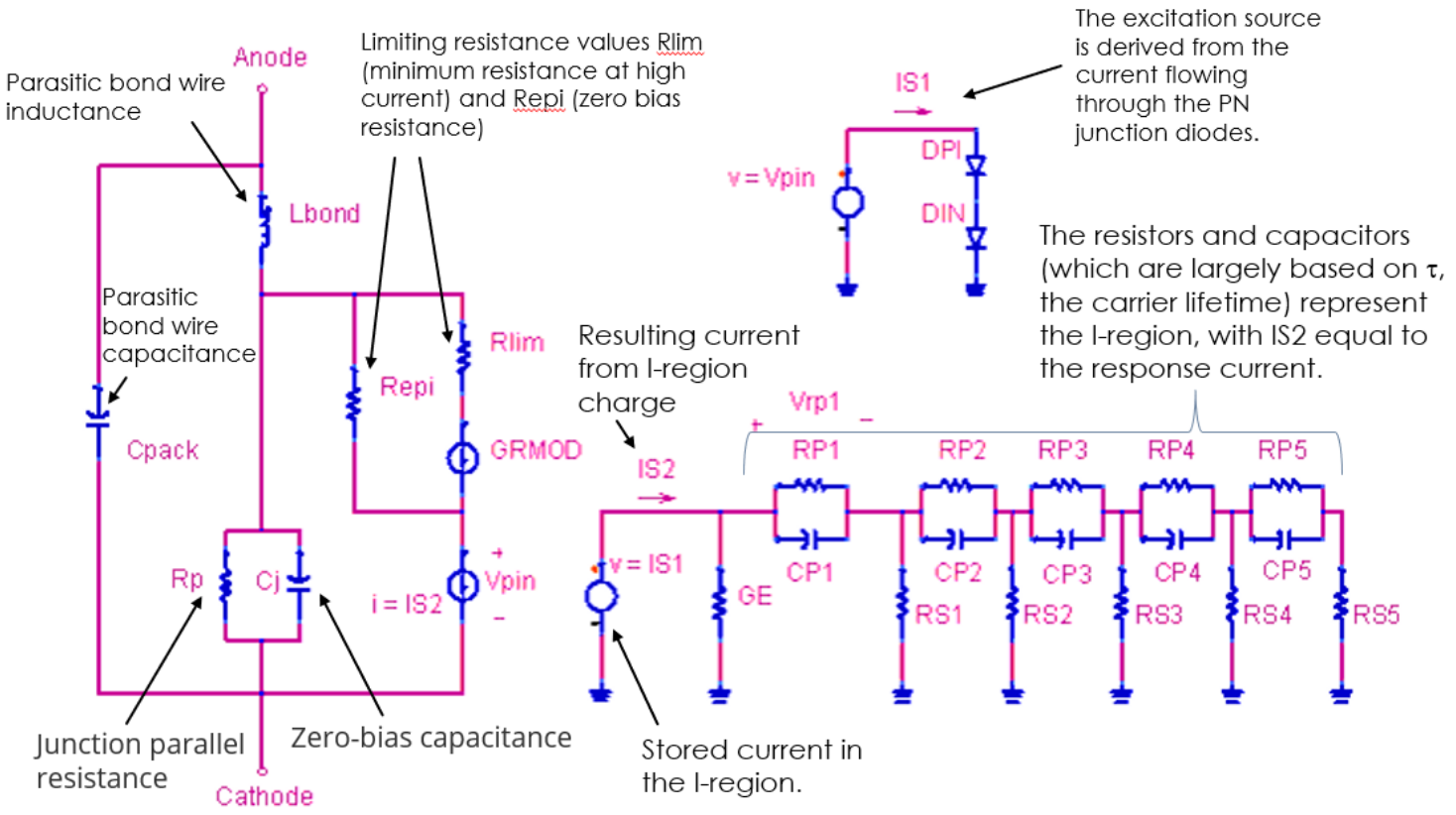
APPENDICES

Appendix A

ADS PIN DIODE MODEL

Appendix A shows the ADS PIN diode model and all its associated parameters, including name, description, units, and default value. These parameters drive the values of the equivalent circuit, determining the behavior of the PIN diode, and are optimized to model the behavior of a specific vendor PIN diode.

Equivalent Circuit



Parameters

Name	Description	Units	Default
Area	Area scaling factor	None	1.0
Temp	Device operating temperature	°C	25.0
Trise	Temperature rise above the circuit ambient (if Temp not specified)	°C	0.0
Tnom	Temperature at which device parameters were established	°C	25.0
Noise	Noise generation option: yes, no	None	yes
Model_level	Model level selector: 1=SPICE Cj model, 2=advanced Cj model	None	1
Is † , ††	Saturation Current	A	1.0e-14
N	Emission coefficient	None	1.0
B	PI-IN emission coefficient splitting factor	None	1.0
Ikf ††	High-injection knee current (0.0 means infinity)	A	infinity
Bv †	Reverse breakdown voltage (0.0 means infinity)	V	infinity
Ibv †	Current at reverse breakdown voltage	A	0.001
Rs † , †††	Diode ohmic resistance	Ohms	0.0
Rp † , †††	Junction parallel resistance	Ohms	1.0e9
Repi † , †††	Zero-bias resistance	Ohms	1.0e3
Rlim † , †††	Minimum series resistance	Ohms	1.0e-3
W	I-region width	m	1.0e-4
Wd	Depletion area width	m	1.0e-6
Tau	Ambipolar carrier lifetime	sec	1.0e-6
Iknee	Current dependent lifetime knee current (0.0 means infinity)	A	infinity
Rho	I-region resistivity	Ohm × m	0.0
Eps	I-region dielectric constant	None	11.9
Cj † , ††	Zero-bias capacitance	F	1.0e-15
Vj †	Junction potential	V	1.0
M †	Grading coefficient	None	0.0
Fc	Forward-bias depletion capacitance coefficient	None	0.5
Eg	Energy gap	eV	1.11
Xti	Temperature exponent for Is	None	3.0
Trs	Linear relative temperature coefficient for Rs	1/°C	0.0
Trs2	Quadratic relative temperature coefficient for Rs	$1/(°C)^2$	0.0
Trp	Linear relative temperature coefficient for Rp	1/°C	0.0
Trp2	Quadratic relative temperature coefficient for Rp	$1/(°C)^2$	0.0
Trepi	Linear relative temperature coefficient for Repi	1/°C	0.0
Trepi2	Quadratic relative temperature coefficient for Repi	$1/(°C)^2$	0.0
Trlim	Linear relative temperature coefficient for Rlim	1/°C	0.0
Trlim2	Quadratic relative temperature coefficient for Rlim	$1/(°C)^2$	0.0
Tm1	Linear relative temperature coefficient for M	1/°C	0.0
Tm2	Quadratic relative temperature coefficient for M	$1/(°C)^2$	0.0
Tbv	Temperature coefficient for Bv	V/°C	0.0
Kf	Flicker noise coefficient		0.0
Af	Flicker noise exponent	None	1.0
Ffe	Flicker noise frequency exponent	None	1.0
Cpack ††	Package parasitic capacitance	F	0.0
Lbond †††	Package parasitic inductance	H	0.0
Imax	Explosion current	A	1.0
_M	Number of devices in parallel	None	1

† Parameter value varies with the temperature based on Tnom and Temp. †† Parameter value scales with Area. ††† Parameter value scales inversely with Area.

Appendix B

MICROSEMI GC4271 PIN DIODE DATASHEET

Appendix B shows a few key pages from the chosen PIN diode (Microsemi GC4271) datasheet. They contain a general description of the diode, a few key features, the device electrical parameters, and a graph of the series resistance vs the forward bias current. This PIN diode is chosen due to its low capacitance and low resistance values. It is able to operate up to 18 GHz with a low capacitance of 0.1 pF (at $V_R = 10$ V) as well as a low series resistance of 1.0 Ω (at $I_f = 20$ mA).

GC4210 – GC4275

CONTROL DEVICES – HIGH SPEED PIN DIODES

RoHS Compliant e4

DESCRIPTION

The GC4200 series are high speed (cathode base) PIN diodes made with high resistivity epitaxial silicon material. These diodes are passivated with silicon dioxide for high stability and reliability and have been proven by thousands of device hours in high reliability systems.

These devices can withstand storage temperatures from -65°C to +200°C and will operate over the range from -55°C to +150°C. All devices meet or exceed military environmental specifications of MIL-PRF-19500. The GC4200 series will operate with as little as +10 mA forward bias.

This series of diodes meets RoHS requirements per EU Directive 2002/95/EC. The standard terminal finish is gold unless otherwise specified. Consult the factory if you have special requirements.

APPLICATIONS

The GC4200 series can be used in RF circuits as an on/off element, as a switch, or as a current controlled resistor in attenuators extending over the frequency range from UHF through Ku band.

Switch applications include high speed switches (ECM systems), TR switches, channel or antenna selection switches (telecommunications), duplexers (radar) and digital phase shifters (phased arrays).

The GC4200 series are also used as passive and active limiters for low to moderate RF power levels.

Attenuator type applications include amplitude modulators, AGC attenuators, power levelers and level set attenuators.

ABSOLUTE MAXIMUM RATINGS AT 25° C (UNLESS OTHERWISE SPECIFIED)

Rating	Symbol	Value	Unit
Maximum Leakage Current @80% of Minimum Rated V_B	I_R	0.5	uA
Storage Temperature	T_{STG}	-65 to +200	°C
Operating Temperature	T_{OP}	-55 to +150	°C

KEY FEATURES

- Available as packaged devices or as chips for hybrid applications
- Low Loss
- Suitable for application to 18Ghz
- High Speed
- Low Insertion Loss
- High Isolation
- RoHS Compliant [1]

[1] Most of our devices are supplied with Gold plated terminations. Other terminal finishes are available on request. Consult factory for details.

APPLICATIONS/BENEFITS

- RF / Microwave Switching
- Duplexers
- Digital Phase Shifting
- Phase Array Radar

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: www.MICROSEMI.com
Specifications are subject to change, consult factory for the latest information.

These devices are ESD sensitive and must be handled use using ESD precautions.

Rev.: 2009-02-19

Microsemi
Microwave Products
75 Technology Drive, Lowell, MA. 01851, 978-442-5600, Fax: 978-937-3748

RoHS Compliant e4

DEVICE ELECTRICAL PARAMETERS @ 25°C (unless otherwise specified)					
Model Number [1]	V_b(V) I_R=10µA (Min)	C_j (pF) [2] @V_R=10V (Max)	R_s(Ω) [3] @20 mA (Max)	T_L(nS) I_R=6mA/I_F=10mA (Typ)	Thermal Resistance θ (°C/W) (Max)
GC4270	70	0.06	1.5	100	80
GC4271	70	0.10	1.0	100	70
GC4272	70	0.20	0.8	100	70
GC4273	70	0.30	0.7	100	60
GC4274	70	0.40	0.6	100	50
GC4275	70	0.50	0.5	100	40
GC4210	100	0.06	1.5	200	80
GC4211	100	0.10	1.0	200	70
GC4212	100	0.20	0.75	200	70
GC4213	100	0.30	0.6	200	60
GC4214	100	0.40	0.5	200	50
GC4215	100	0.50	0.35	200	40
GC4220	250	0.06	2.5	500	80
GC4221	250	0.10	2.0	500	70
GC4222	250	0.20	1.5	500	70
GC4223	250	0.30	1.0	500	60
GC4224	250	0.40	0.8	500	50
GC4225	250	0.50	0.6	500	40

Notes:
1. This series of devices is available in standard case styles 00, 30, and 35. Many other styles are available on request.
2. Capacitance is measured at 1 MHz.
3. Resistance is measured AT 1 GHz using transmission loss techniques.

The junction capacitance specified is for a 00 (chip) package style. Standard wafer evaluation and characterization is completed using a style 30 package. Diodes are available in many case styles. Each type offers performance trade-offs. The proper choice of package style depends on the end application and operating environment. Consult factory for assistance. Reverse polarity diodes (NIP) and higher voltage PIN and NIP diodes are also available. (See data sheets for GC4300, GC4400, and GC4500 series respectively.)

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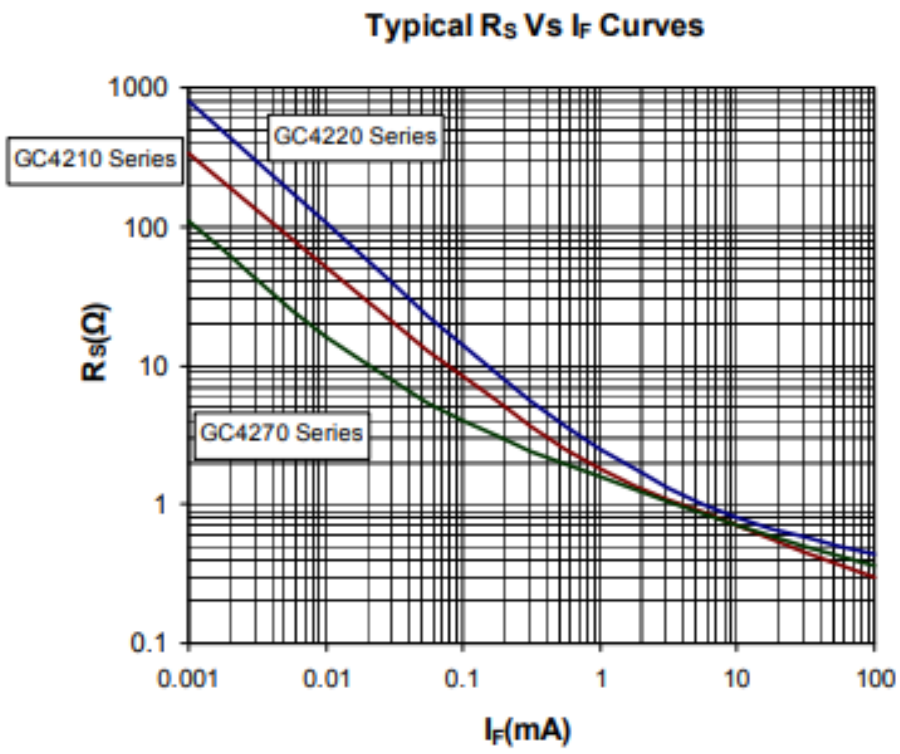
RS VS IF CURVES



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Appendix C

MACOM MABT-011000 BIAS NETWORK DATASHEET

Appendix C shows a few key pages from the chosen bias tee network (MABT-011000) datasheet. They contain a general description and a few key features, a functional schematic with labeled pins, electrical specifications, typical RF performance graphs, a few tips on how to use the device, and a die outline drawing. Its datasheet states it is broadband, from 2 to 18 GHz. It also claims it is "suitable for the DC biasing of PIN diode control circuits. It functions as an RF-DC de-coupling network as well as the DC return and contains a series DC blocking capacitor." This performance made this part ideal for this application.

MABT-011000

Integrated Bias Network
2 - 18 GHz

Rev. V1

Features

- Specified over Broad Bandwidth: 2 - 18 GHz
- Surface Mount
- Extremely Low Insertion Loss: < 0.3 dB
- High RF-DC Isolation: > 34 dB
- Rugged, Fully Monolithic Glass Encapsulation
- RoHS* Compliant and 260°C Reflow Compatible

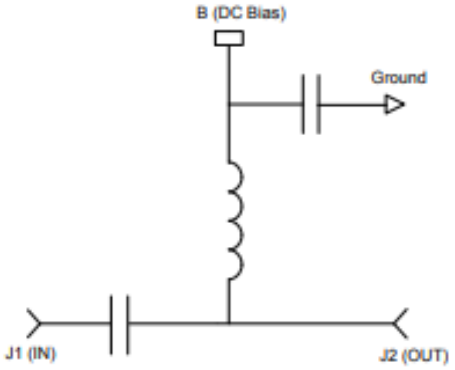
Description

The MABT-011000 is a fully monolithic broadband surface mount bias network utilizing MACOM's patented HMIC process. This process allows the formation of silicon vias by imbedding them in low loss, low dispersion glass along with high Q spiral inductors and MIM capacitors. The close proximity of elements and the combination of silicon and glass give this HMIC device low loss and high performance with exceptional repeatability through millimeter frequencies.

Large vias reduce inductance and allow part to be more easily soldered, while the gold backside metallization provides the RF and DC ground. This allows for manual or automatic die attach via electrically conductive silver epoxy or RoHS compliant solders.

The MABT-011000 bias network is suitable for the DC biasing of PIN diode control circuits. It functions as an RF-DC de-coupling network as well as the DC return and contains a series DC blocking capacitor. DC currents up to 60 mA and DC voltages up to 50 V may be used.

Functional Schematic



Pin Configuration

Pin	Function
J1	RF Input
J2	RF Output
B	DC Bias

Ordering Information[1]

Part Number	Package
MABT-011000-14230G	Gel pack
MABT-011000-14230W	Wafer Frame
MABT-011000-14230P	3000 piece reel
MABT-011000-14235P	500 piece reel

1. Die quantity varies.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications: T_A = 25°C

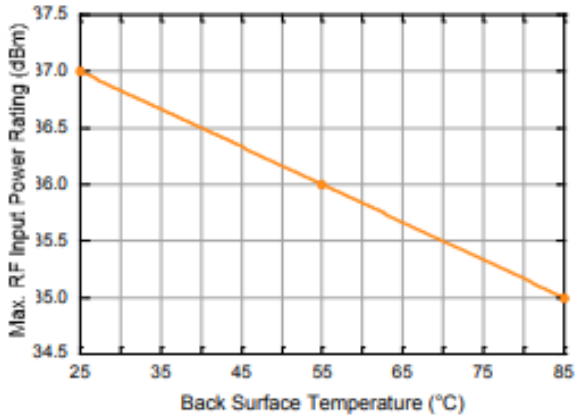
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss (J1-J2)	2 GHz 6 GHz 12 GHz 18 GHz	dB	—	0.25 0.10 0.15 0.25	0.50 0.30 0.40 0.50
RF - DC Isolation (J1-B, J2-B)	2 GHz 6 GHz 12 GHz 18 GHz	dB	30 50 50 40	34 60 60 47	—
Input Return Loss (J1)	2 GHz 6 GHz 12 GHz 18 GHz	dB	17 17 17 17	23 35 34 26	—
Output Return Loss (J2)	2 GHz 6 GHz 12 GHz 18 GHz	dB	17 17 17 17	22 44 37 26	—

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
DC Bias Voltage	±50 V
DC Bias Current	±60 mA
Operating Temperature	-65°C to +125°C
Storage Temperature	-65°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Maximum RF Input De-Rating Curve[4]



4. Based on testing done at 2.2 GHz.

Handling Procedures

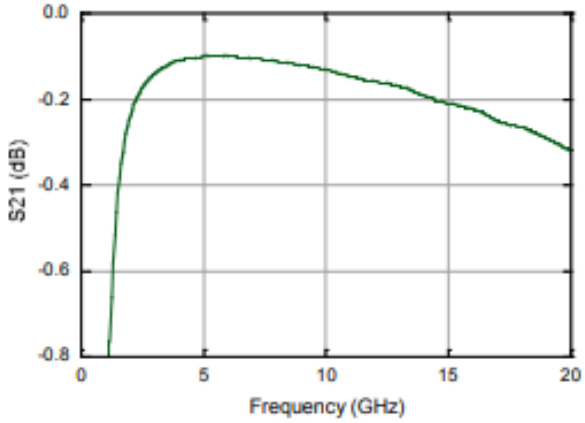
Please observe the following precautions to avoid damage:

Static Sensitivity

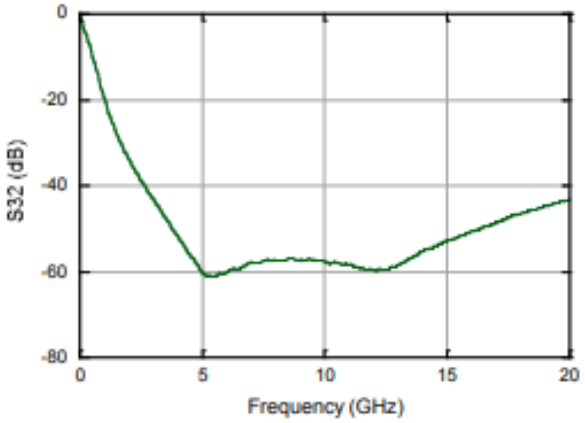
Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1B devices.

Typical RF Performance

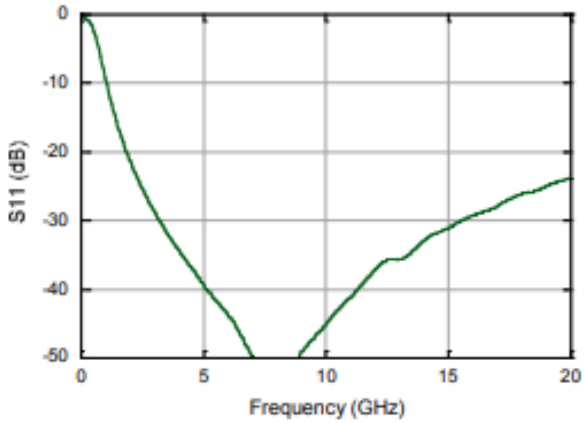
Insertion Loss



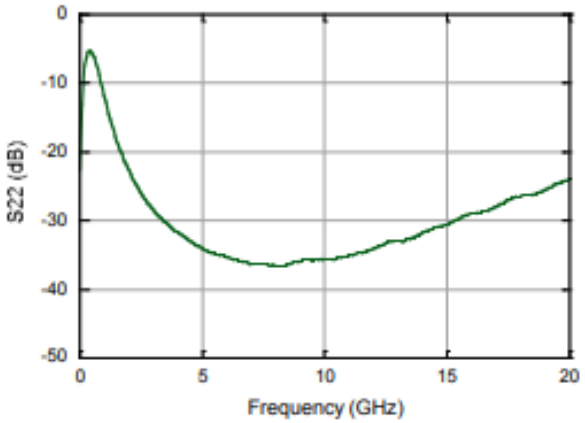
Isolation (RF to DC)



Input Return Loss



Output Return Loss



Integrated Bias Network
2 - 18 GHz

Operation

Operation of the MABT-011000 bias network is accomplished by applying DC bias to the DC port on the die. Port J2 provides the DC bias to the corresponding, connected, microwave device. Port J1 has a DC blocking capacitor, allowing current to only RF port J2, such as in a bias tee configuration. The MABT-011000 can also be used as a ground return when the DC Bias Port is attached to the RF and DC ground. The small DC resistance (≈ 7 Ω) of the DC Bias Port allows up to +/- 60 mA @ +/- 50 V to be delivered while still maintaining >35 dB RF-to-DC isolation.

Handling Procedures

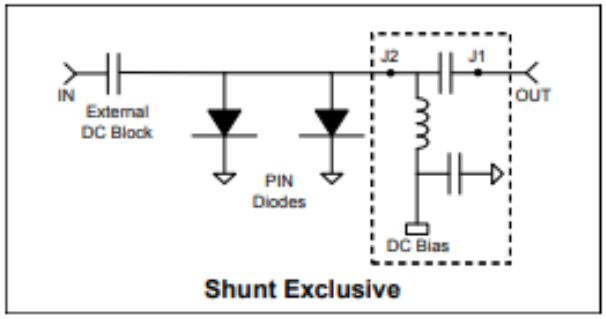
A vacuum pick up tool with a soft tip is recommended while placing the die. Attachment to a circuit board is made simple through the use of standard surface mount technology. Mounting pads are located on the back surface of the die. Position the die so that its mounting pads are aligned with the circuit board land pads. Since the HMIC glass is transparent, the edges of the mounting pads can be visually inspected through the die after attachment is completed.

Connections may be made onto hard or soft substrates using 80Au20Sn or other solder. When soldering these devices to a hard substrate, a solder re-flow method is preferred. When soldering to soft substrates, such as Duroid, it is recommended to choose a solder that minimizes stress due to any TCE mismatches.

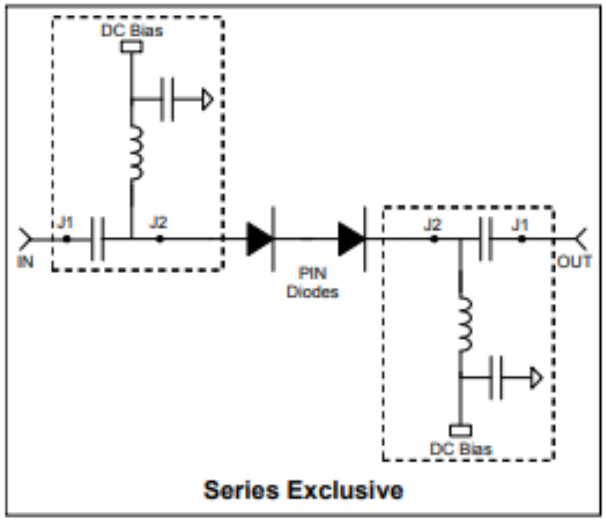
Typical re-flow profiles are provided in Application Note M538, Surface Mounting Instructions, available in the Technical Resources section of the MACOM website at www.macom.com. Solder reflow should not be performed by causing heat to flow through the top surface of the die to the back surface of the die.

For applications where the average power is ≤ 1 W, a thermally-conductive silver epoxy may be used. Cure per manufacturers recommended time and temperature, typically 1 hour at 150°C.

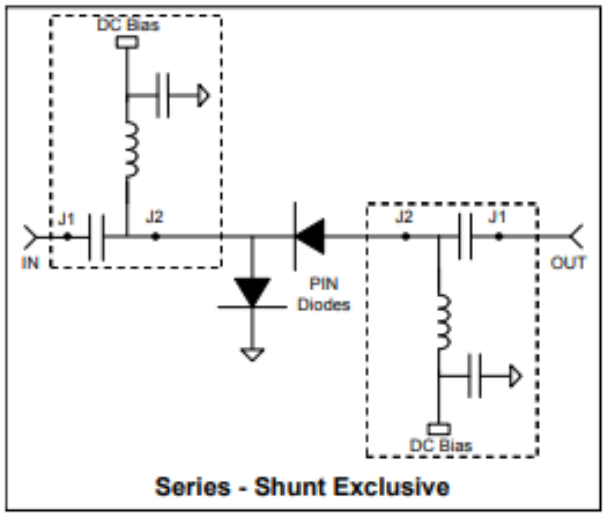
Bias Circuit for PIN Diode Switch



Shunt Exclusive

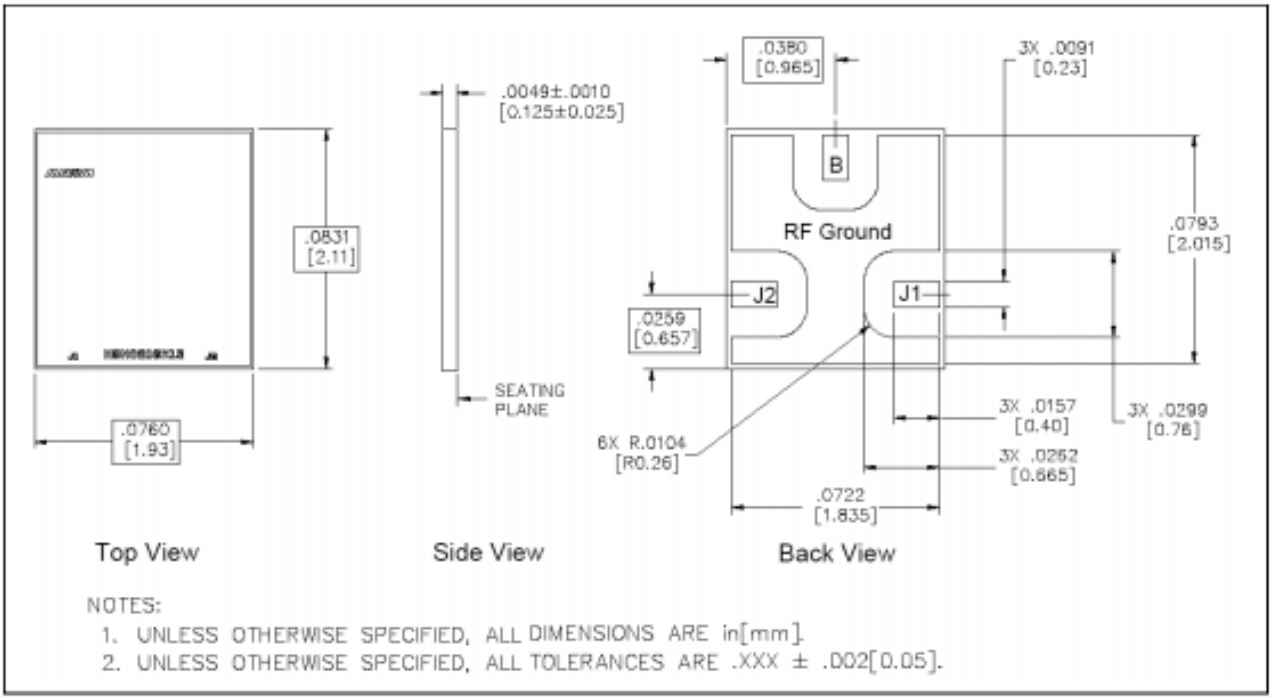


Series Exclusive



Series - Shunt Exclusive

Die Outline Drawing



Appendix D

ROGERS RO4350B DATASHEET

Appendix D shows a few key pages from the chosen Rogers substrate material (RO4350B) datasheet. They contain a general description of the RO4000 series, features and benefits of the material, the material parameters, and a few standard dimensions that are commonly used with the material. This Rogers material works very well up to high frequencies and the dielectric constant of 3.66 (with a board thickness of 20 mil) allowed the lines to be thin enough to fit the whole star network without too much coupling.

ROGERS CORPORATION

Data Sheet

RO4000® Series

High Frequency Circuit Materials

RO4000® hydrocarbon ceramic laminates are designed to offer superior high frequency performance and low cost circuit fabrication. The result is a low loss material which can be fabricated using standard epoxy/glass (FR-4) processes offered at competitive prices.

The selection of laminates typically available to designers is significantly reduced once operational frequencies increase to 500 MHz and above. RO4000 material possesses the properties needed by designers of RF microwave circuits and matching networks and controlled impedance transmission lines. Low dielectric loss allows RO4000 series material to be used in many applications where higher operating frequencies limit the use of conventional circuit board laminates. The temperature coefficient of dielectric constant is among the lowest of any circuit board material (Chart 1), and the dielectric constant is stable over a broad frequency range (Chart 2). For reduced insertion loss, LoPro® foil is available (Chart 3). This makes it an ideal substrate for broadband applications.

RO4000 material's thermal coefficient of expansion (CTE) provides several key benefits to the circuit designer. The expansion coefficient of RO4000 material is similar to that of copper which allows the material to exhibit excellent dimensional stability, a property needed for mixed dielectric multi-layer boards constructions. The low Z-axis CTE of RO4000 laminates provides reliable plated through-hole quality, even in severe thermal shock applications. RO4000 series material has a Tg of >280°C (536°F) so its expansion characteristics remain stable over the entire range of circuit processing temperatures.

RO4000 series laminates can easily be fabricated into printed circuit boards using standard FR-4 circuit board processing techniques. Unlike PTFE based high performance materials, RO4000 series laminates do not require specialized via preparation processes such as sodium etch. This material is a rigid, thermoset laminate that is capable of being processed by automated handling systems and scrubbing equipment used for copper surface preparation.

RO4003C™ laminates are currently offered in various configurations utilizing both 1080 and 1674 glass fabric styles, with all configurations meeting the same laminate electrical performance specification. Specifically designed as a drop-in replacement for the RO4003C™ material, RO4350B™ laminates utilize RoHS compliant flame-retardant technology for applications requiring UL 94V-0 certification. These materials conform to the requirements of IPC-4103, slash sheet /10 for RO4003C, see note #1 for RO4350B slash sheet determination.

Features and Benefits:

RO4000 materials are reinforced hydrocarbon/ceramic laminates - not PTFE
- Designed for performance sensitive, high volume applications

Low dielectric tolerance and low loss
- Excellent electrical performance
- Allows applications with higher operating frequencies
- Ideal for broadband applications

Stable electrical properties vs. frequency
- Controlled impedance transmission lines
- Repeatable design of filters

Low thermal coefficient of dielectric constant
- Excellent dimensional stability

Low Z-axis expansion
- Reliable plated through holes

Low in-plane expansion coefficient
- Remains stable over an entire range of circuit processing temperatures

Volume manufacturing process
- RO4000 laminates can be fabricated using standard glass epoxy processes
- Competitively priced

CAF resistant

Some Typical Applications:

- Cellular Base Station Antennas and Power Amplifiers
- RF Identification Tags
- Automotive Radar and Sensors
- LNB's for Direct Broadcast Satellites

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Chart 1: RO4000 Series Materials Dielectric Constant vs. Temperature

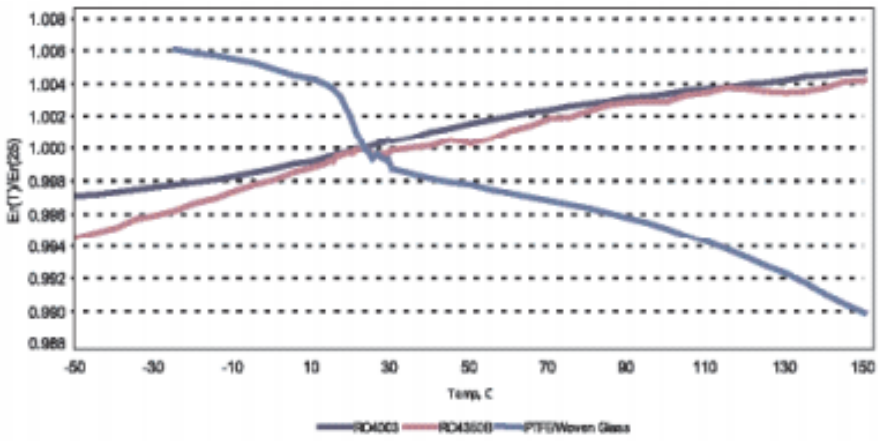


Chart 2: RO4000 Series Materials Dielectric Constant vs. Frequency

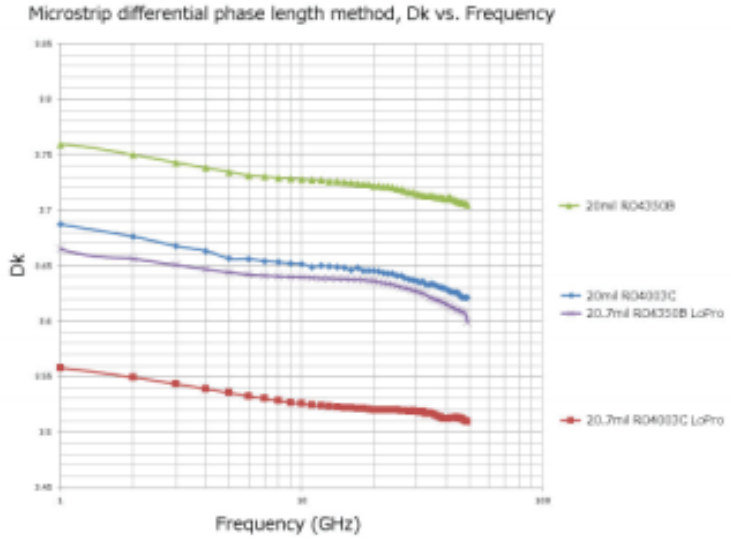
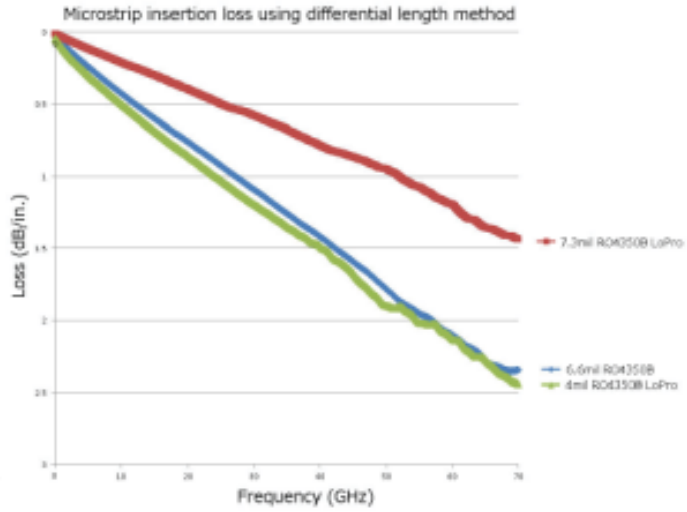


Chart 3: Microstrip Insertion Loss



Property	Typical Value		Direction	Units	Condition	Test Method
	RO4003C	RO4350B				
Dielectric Constant, ε_r Process	3.38 ± 0.05	[1] 3.48 ± 0.05	Z	--	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
[2] Dielectric Constant, ε_r Design	3.55	3.66	Z	--	8 to 40 GHz	Differential Phase Length Method
Dissipation Factor tan, δ	0.0027 0.0021	0.0037 0.0031	Z	--	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	+40	+50	Z	ppm/°C	-50°C to 150°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7 X 10^{10}	1.2 X 10^{10}		MΩ•cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2 X 10^{9}	5.7 X 10^{9}		MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	19,650 (2,850) 19,450 (2,821)	16,767 (2,432) 14,153, (2,053)	X Y	MPa (ksi)	RT	ASTM D638
Tensile Strength	139 (20.2) 100 (14.5)	203 (29.5) 130 (18.9)	X Y	MPa (ksi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)		MPa (kpsi)		IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°C	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	10 12 32	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.4.41
Tg	>280	>280		°C TMA	A	IPC-TM-650 2.4.24.3
Td	425	390		°C TGA		ASTM D3850
Thermal Conductivity	0.71	0.69		W/m/°K	80°C	ASTM C518
Moisture Absorption	0.06	0.06		%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86		gm/cm^3	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)		N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	[3] V-0				UL 94
Lead-Free Process Compatible	Yes	Yes				

NOTES:

(1) RO4350B 4 mil laminates have a process Dk of 3.33 ± 0.05 and are in conformance with IPC-4103A/240. All other RO4350B laminate thicknesses are /11 and /240 compliant.

(2) The design Dk is an average number from several different tested lots of material and on the most common thickness/s. If more detailed information is required, please contact Rogers Corporation or refer to Rogers' technical papers in the Rogers Technology Support Hub available at http://www.rogerscorp.com.

(3) RO4350B LoPro® laminates do not share the same UL designation as standard RO4350B laminates. A separate UL qualification may be necessary.

Typical values are a representation of an average value for the population of the property. For specification values contact Rogers Corporation.

RO4000 LoPro laminate uses a modified version of the RO4000 resin system to bond reverse treated foil. Values shown above are RO4000 laminates without the addition of the LoPro resin. For double-sided boards, the LoPro foil results in a thickness increase of approximately 0.0007" (18µm) and the Dk is approximately 2.4. The Dk decreases by about 0.1 as the core thickness decreases from 0.020" to 0.004.

Prolonged exposure in an oxidative environment may cause changes to the dielectric properties of hydrocarbon based materials. The rate of change increases at higher temperatures and is highly dependent on the circuit design. Although Rogers' high frequency materials have been used successfully in innumerable applications and reports of oxidation resulting in performance problems are extremely rare, Rogers recommends that the customer evaluate each material and design combination to determine fitness for use over the entire life of the end product.

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Standard Thickness	Standard Panel Size	Standard Copper Cladding
RO4003C: 0.008" (0.203mm), 0.012 (0.305mm), 0.016"(0.406mm), 0.020" (0.508mm) 0.032" (0.813mm), 0.060" (1.524mm) RO4350B: *0.004" (0.101mm), 0.0066" (0.168mm) 0.010" (0.254mm), 0.0133" (0.338mm), 0.0166" (0.422mm), 0.020"(0.508mm), 0.030" (0.762mm), 0.060"(1.524mm) Note: Material clad with LoPro foil add 0.0007" (0.018mm) to dielectric thickness	12" X 18" (305 X457 mm) 24" X 18" (610 X 457 mm) 24" X 36" (610 X 915 mm) 48" X 36" (1.224 m X 915 mm) *0. 004" (0.101mm) material is not available in panel sizes larger than 24"x18" (610 X 457mm)	½ oz. (17µm) electrodeposited copper foil (.5ED/.5ED) 1 oz. (35µm) electrodeposited copper foil (1ED/1ED) 2 oz. (70µm) electrodeposited copper foil (2ED/2ED) **PIM Sensitive Applications:** ½ oz (17µm) LoPro Reverse Treated EDC (.5TC/.5TC) 1 oz (35µm) LoPro Reverse Treated EDC (1TC/1TC)

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Appendix E

SOUTHWEST MICROWAVE 292-06A-6 CONNECTOR DATASHEET

Appendix E shows the suggested Southwest Microwave connector (292-06A-6) datasheet to use when the switch is manufactured. There are several key dimensions here that need to be considered. It is essentially a clamp on SMA connector. Several aspects about this connector make it ideal for this design. It is able to connect to a very small trace such as the width of 25 mil used in this design. The frequency specification states that it operates up to 27 GHz, well above the upper bandwidth of the switch. The screw in/clamping allows for testing across the board with the same connector.

DWG No.:

91Y60930

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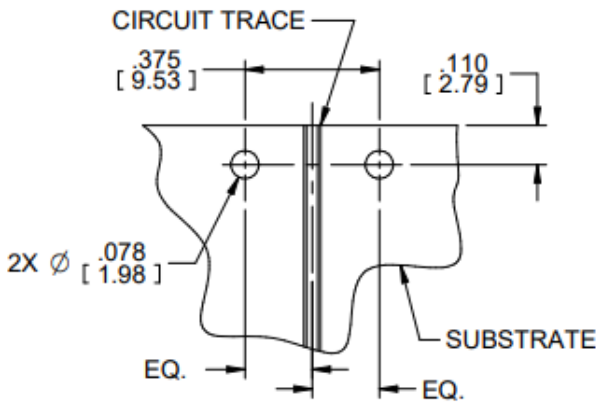
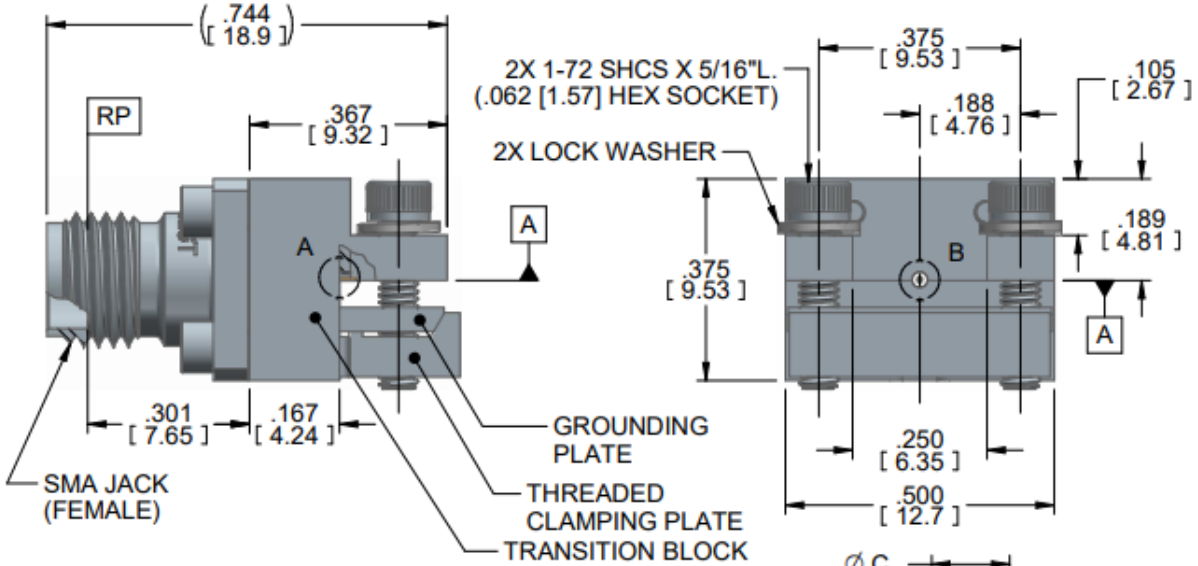


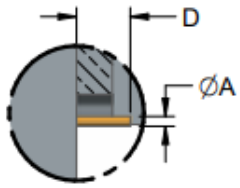
HOUSING:	STEEL, CRES ALLOY UNS-30300 PER ASTM A582 PASSIVATED PER ASTM A967-99
CONTACT:	BeCu UNS-C17300 PER ASTM B196 GOLD PLATE PER MIL-DTL-45204
DIELECTRIC:	VIRGIN PTFE FLUOROCARBON PER ASTM D1710 TYPE 1, GRADE 1, CLASS B
CAPTURE BEAD:	ULTEM 1000 PER ASTM D5205
ITEM	MATERIAL & FINISH
SMA CONNECTOR	

TRANSITION BLOCK, GROUNDING PLATE, THREADED CLAMPING PLATE	C360 BRASS ALLOY UNS-C36000 PER ASTM B16. NICKEL PLATE PER AMS 2404B
LAUNCH PIN:	BeCu UNS-C17300 PER ASTM B196 GOLD PLATE PER MIL-DTL-45204
TRANSITION BLOCK DIELECTRIC:	VIRGIN PTFE FLUOROCARBON PER ASTM D1710, TYPE 1 GRADE 1, CLASS B
ITEM	MATERIAL & FINISH
TRANSITION BLOCK	

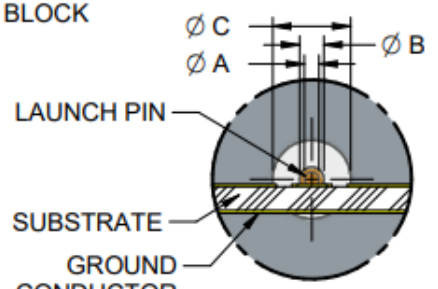
1. ALL DIMENSIONS ARE IN INCHES. ALL ANGLES ARE IN DEGREES. DIMENSIONS SHOWN IN BRACKETS [XXX] ARE IN MILLIMETERS.

NOTES: UNLESS OTHERWISE SPECIFIED.





DETAIL A



DETAIL B

Model	Ø A	Ø B	Ø C	D
292-04A-6	.010	.020	.0635	.050
292-05A-6	.007	.015	.0480	.030
292-06A-6	.007	.012	.0390	.030
292-07A-6	.005	.009	.0290	.030

REV		APRVD.	DATE:
A	RELEASE		

SOUTHWEST MICROWAVE

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Tempe, Arizona 85284-2946
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Fax (480) 783-0360

TITLE

SMA JACK (FEMALE)
END LAUNCH CONNECTOR
LOW PROFILE

DRN BY:	DATE:	DWG. NO.	REV.
EAG	09/26/12	91Y60930	A
SHEET: 1 OF 1			