CONTROLLER MODELING AND STABILITY ANALYSIS OF MULTIPLE INPUT SINGLE OUTPUT DC-DC CONVERTER

A Thesis

presented to

the Faculty of California Polytechnic State University,

San Luis Obispo

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

by

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January 2021

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ABSTRACT

Controller Modeling and Stability Analysis of Multiple Input Single Output DC-DC Converter

Astha Adhikari

This thesis entails the stability analysis of the Multiple Input Single Output (MISO) DC-DC converter developed for the DC House Project at Cal Poly. A frequency domain control system model of the MISO converter was designed and constructed using MATLAB Simulink. Transfer functions were derived and modeled for each stage of the converter to best fit the converter circuit system used in the original MISO circuit. Stability metrics such as overshoot, undershoot, rise time, phase margin and gain margin were measured to evaluate and analyze the stability of the converter. These metrics were measured with the original model including the current sharing network that allows load sharing between multiple MISO modules. The simulation results demonstrate that based on the existing model, the system is stable with a gain margin of infinity and phase margin of around 40 degrees at crossover frequency of 47kHz with nominal input voltage of 24V. Another compensator was proposed to overcome the shortcomings of the original compensator model with respect to the overshoot and phase margin. The new compensator model improved the phase margin at the same crossover frequency with a higher rise time and lowered percent overshoot. Additional improvements and tradeoffs are further discussed to help with the decision when designing a compensator for DC-DC converter that uses the current mode control technique.

ACKNOWLEDGMENTS

First, I would like to thank Dr. Taufik for his guidance in helping me complete this thesis during this unprecedented time. I would not be where I was without his knowledge and assistance. Thank you, professor, for always being readily available to guide me. I feel proud to say that I am fully prepared for my power electronics journey because of your classes and insights.

I would also like to thank my parents for supporting me and encouraging me. Thank you, mom, for listening to my complaints and achievements. I would also like to extend my gratitude to my cousins, Riya, and Raj for keeping me motivated while I took classes from home.

Lastly, I would like to thank my friends and family and one special furball that kept me company during my thesis endeavors.

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1. Introduction

With the globalization of technology and increase in world population, there has been a significant worldwide demand for electricity. Such phenomenon is the result of the fact that electricity is vital in enhancing economic growth and improving the standard of living. Electricity further increases the quality of healthcare along with productivity. In fact, electricity is needed for just about everything, from operating household appliances to running big factories. Something as simple as basic medical services are compromised without access to electricity. Electricity fuels the model lifestyle targeted towards improving the way of living and connecting people across the world. However, not everyone is fortunate enough to use modern technologies.

Approximately 940 million people still did not have access to electricity globally in 2016 [1]. While the number of people with access to electricity is increasing every year as shown in Figure 1.1, there are still millions living in the dark. Many reside in areas that pose big challenges in providing access to electricity via existing electric power grid [2]. Examples include people living in secluded islands, remote villages, and mountainous regions make it especially difficult to reach by any existing power grid. In particular, the high capital costs of building the necessary infrastructure and operating cost in maintaining it make it economically prohibitive to connect the existing power grid to these areas. Additional factors such as financial resources and local cultures further add to the complications in providing electricity to these remote areas. In such cases where it is challenging to connect to the grid, renewables offer a great solution [3].

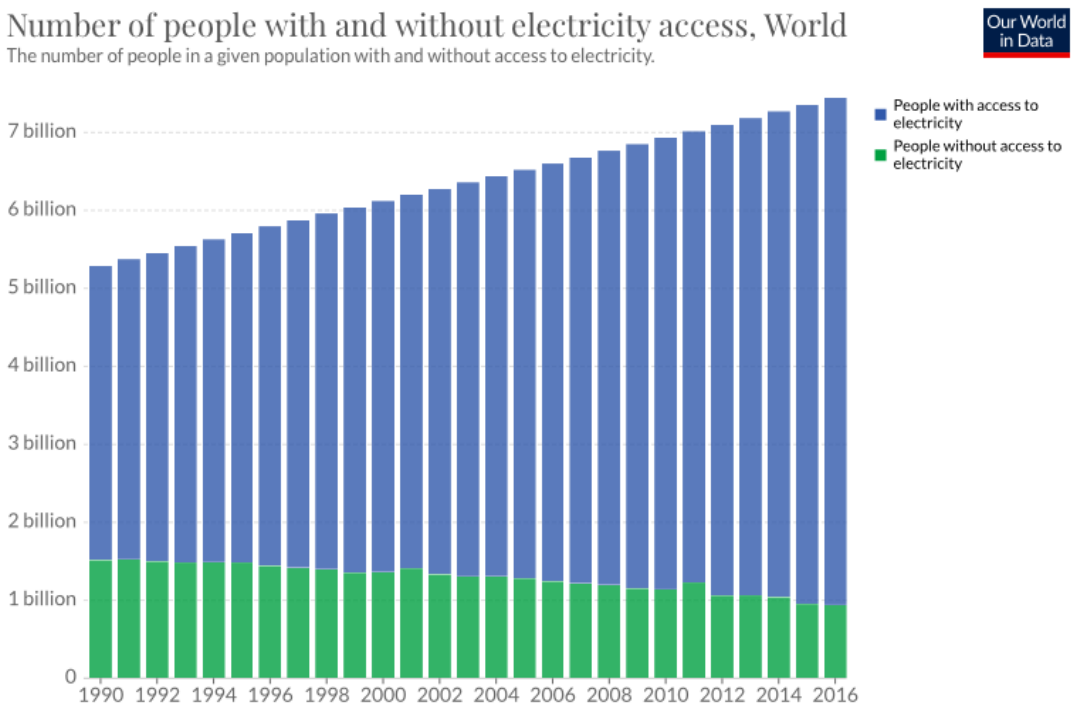


Figure 1-1: Number of people with and without access to electricity worldwide [1].

Renewable energy sources are sustainable and low in pollution as opposed to fossil fuels which are finite resources and cause pollution during combustion. They offer better environmental and economic benefits as they produce no greenhouse gases. They are one of the most effective tools to contribute towards meeting the Paris Agreement. The Paris Agreement is a landmark environmental accord adopted by over 186 nations in 2015 to address climate change and its negative impact [4]. The goal of the agreement is to limit global warming temperature increase to 1.5 degrees Celsius by 2030. In addition, renewables help to sustain the energy demands for a globalizing world where everyone is connected. This is feasible with the significant improvement in power electronic technology needed for renewable sources. Power electronics is the use of semiconductor devices as tools in increasing input to output power efficiency by using various isolated or non-isolated power converters [5].

The DC house project started at California Polytechnic State University, San Luis Obispo in 2010. The project is dedicated towards producing DC power from renewable energy sources for rural areas that are not connected to the grid. While most generation and transmission use AC power, many consumer products require DC power [6]. The DC house focuses on using only DC power generated from small renewable energy sources, thus eliminating the need to use AC to DC converters. This increases the overall system efficiency and reduces cost and size. The DC house aims to provide basic necessities needed to sustain a small off-grid house. In addition, the project also emphasizes the need for green energy and supports those looking for alternative energy sources. It serves as an example of how it is possible to survive solely on DC power fueled by renewables like solar, wind, hydro, etc.

The DC House includes four major blocks: renewable sources, converters, battery storage and DC loads as shown in Figure 1.2. Among these, the multiple input single output (MISO) converter is one of the critical components of the DC House system. The MISO converter is a DC-DC converter that takes multiple inputs from renewable energy sources and gives a single DC output voltage to a main DC bus of the DC house. A typical MISO converter uses isolated or non-isolated DC-DC converter topologies. Students at Cal Poly have studied several variations of MISO in the past. The initial study and prototype done by Wong in his thesis using a full bridge topology to achieve 600W [7]. However, this design lacked isolation and output power. Another design by Jong focused on fixing these shortcomings using the flyback converter topology [8]. Lastly, Gallardo's thesis developed the MISO modules constructed from a non-isolated four switch buck-boost topology [8].

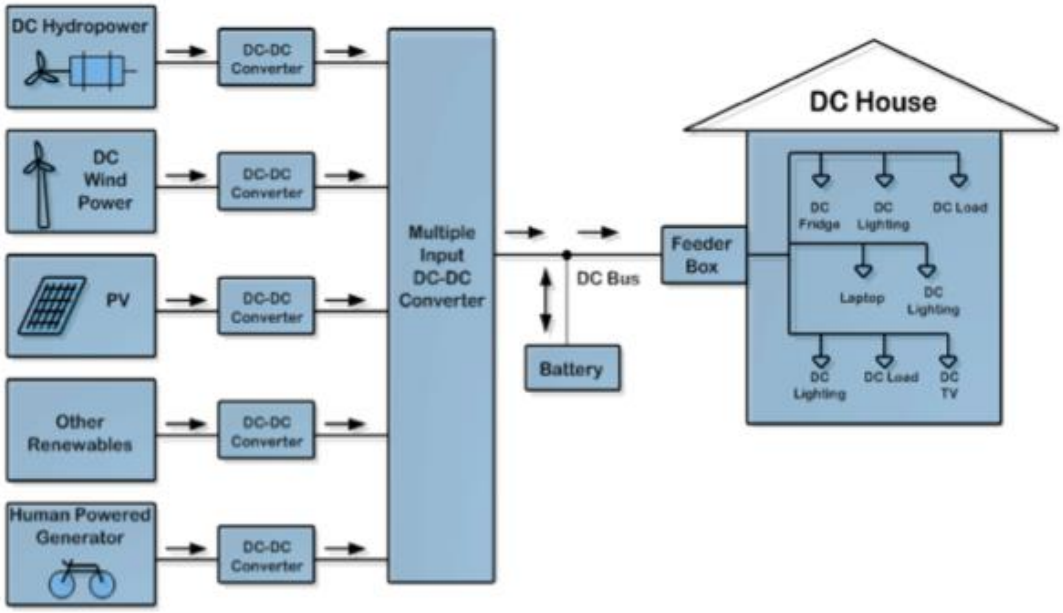


Figure 1-2: Simplified block diagram of the DC House project [6].

After choosing the suitable topology, the next phase in the MISO converter development includes investigation and study of the stability of the MISO converter. This is the aspect that has not been conducted yet for the current MISO prototype. More specifically, stability study of the MISO converter that is directly related to its steady-state and transient performances is needed to ensure proper operation of the MISO converter under various source, load, and environmental conditions. This thesis focuses on the stability analysis of the MISO converter developed by Gallardo.

2. Background

DC-DC converters maintain a constant value for the output voltage using control loop or feedback circuitry. In general, to obtain a regulated output voltage, the DC-DC converter employs an output voltage sensor which compares its voltage to a reference voltage whose difference translates into the required duty cycle of the switch used in the converter. There are four main control techniques to maintain the desired output voltage: voltage mode, current mode, hysteresis, and constant on time control. Each mode uses one or more feedback loop whose stability is central to the overall system design. Bode plot is a common tool used to determine the stability of a closed-loop system. It maps the frequency response of the system using two graphs: one showing the phase and one showing the magnitude. In order to perform stability analysis of a DC-DC converter using bode plots, the control technique employed in the DC-DC converter must first be investigated.

In voltage mode control, an error voltage is compared to a saw-tooth ramp of fixed frequency to generate a PWM signal to control the power switch as shown in Figure 2.1 [9]. The main characteristic of this technique is that it uses a single voltage feedback path or loop which is simple to design and analyze [10]. The error voltage is derived in the feedback system from the error amplifier that amplifies the difference between the output voltage and a reference voltage as shown in [10]. This reference voltage is typically a low DC voltage below 1.5 V and most commonly provided inside a controller chip; and thus, a user cannot change its value. If the error amplifier output voltage increases, then the duty cycle decreases. However, the correction process is longer when a disturbance occurs at its input stage such as a drop in input voltage. This is

because the disturbance signal will have to first travel through the converter and reach the output stage before it can be sensed by the feedback circuity. In inductor-based DC-DC converter, when the input voltage drops, the average inductor current
drops accordingly causing the output voltage to drop as well. The error amplifier voltage plus the compensation network
then increases to set the output voltage back to the desired value. This slower process of correcting the output voltage when the input voltage changes is one major drawback of voltage mode control.

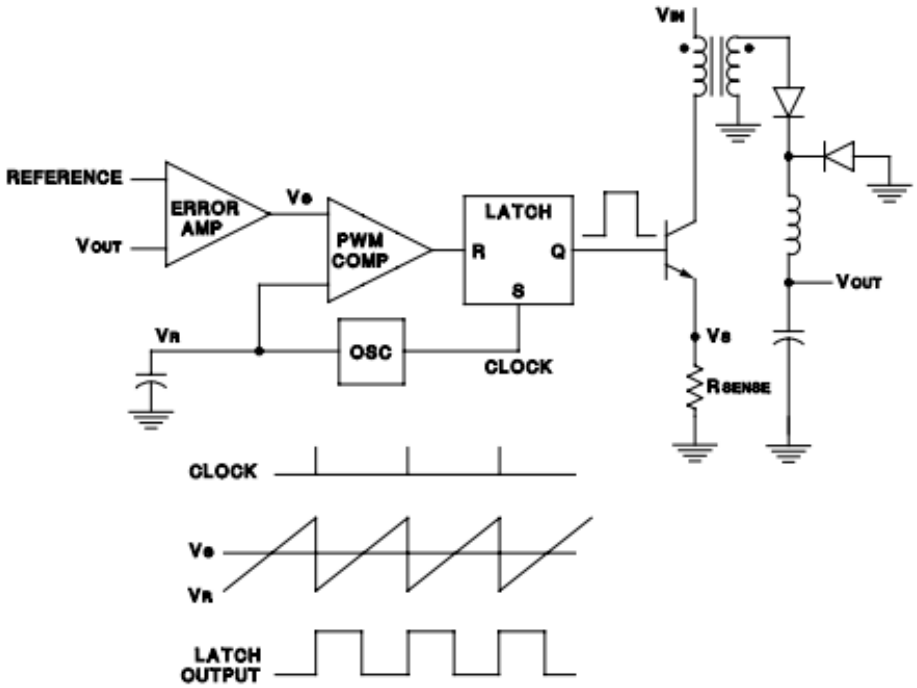


Figure 2-1: Voltage mode control block diagram [10].

Current mode control utilizes an additional inner current control loop. Similar to voltage mode control, an error voltage is generated by comparing the output voltage with the reference voltage as shown in Figure 2.2. This “outer” or bigger loop helps the

converter to react fast upon any disturbance occurring at the output stage of DC-DC converter. To overcome the shortcoming encountered in voltage mode control with the slow response upon disturbance at the input stage, the current mode control utilizes an additional sensor to monitor the peak of the inductor current. Whenever the peak current increases indicating an increase in load current which further corresponds to decreasing output voltage, the “inner” control loop reacts by increasing the duty cycle of the switch. In its practical implementation, the current mode senses the switch current instead of the inductor current for two major reasons. First, the peak switch current is the same as the peak inductor current. Secondly, the switch current is only a fraction of the inductor current making its more energy efficient to monitor switch current when a series sensing resistor is being used. Therefore, in current mode control the error voltage is directly used to control the peak of the switch current. If the error voltage increases, then the peak current increases causing the duty cycle to increase. This way, when a disturbance occurs at its input stage such as a drop in input voltage consequently changing the peak switch current, the inner loop works to correct the duty cycle without having to change the feedback voltage from the outer loop. This results in a faster response which covers both any disturbance at the input due a change in the source voltage and at the output due to the change in the load demand. This is a major advantage of current mode control.

In other words, with current mode control, there is an immediate response to change in line voltage which eliminates the delayed response and gain variation with changes in input voltage [10]. In addition, unlike voltage mode, current mode provides higher power stage efficiency in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [9]. The compensation is simpler and gives a

higher gain bandwidth for the error amplifier compared to voltage-mode circuits [10]. Furthermore, current mode makes load sharing easy when multiple power units are paralleled [10]. This is especially important in the context of the MISO converter which employs the current mode control. A drawback of current mode control is that slope compensation network is needed for duty cycle over 50% to keep the system stable [9]. The inductor current sensing also requires additional circuitry and power.

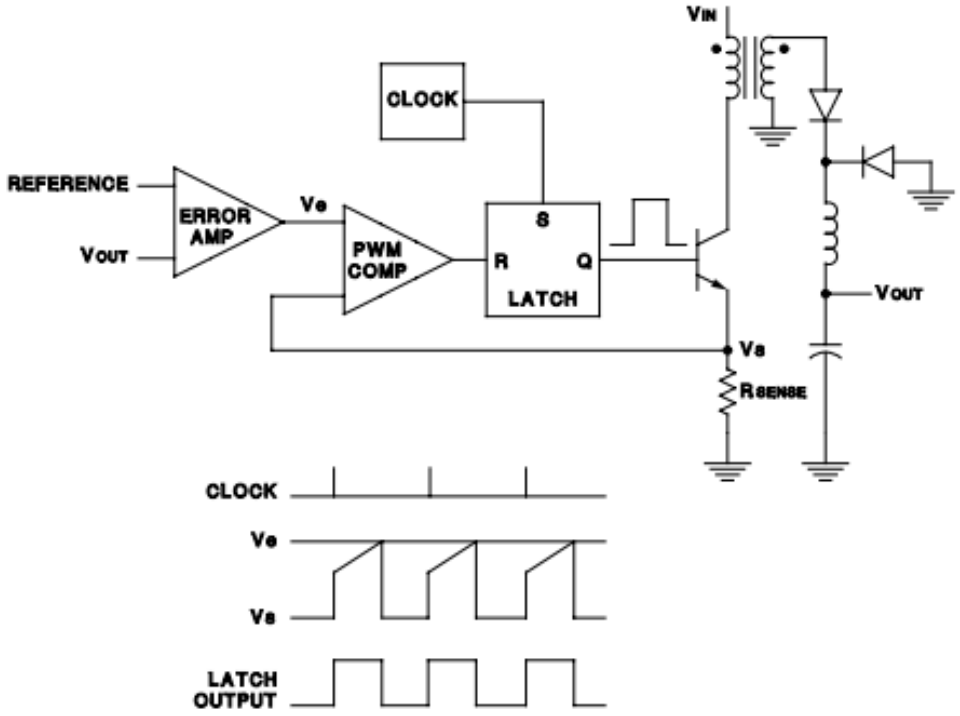


Figure 2-2: Current mode control block diagram [10].

Hysteretic control maintains the output voltage within hysteresis band centered about the internal reference voltage [11]. When the output voltage reaches or exceeds the reference of the hysteresis band, the switch turns on causing the output voltage to decrease. The switch turns off when the output voltage decreases from the upper limit as shown in Figure 2.3 [12]. The advantages of hysteretic control are it provides the fastest

response to load changes and does not require loop compensation. This topology is popular because it is inexpensive and simple to use. On the other hand, the drawback is that it has variable switching frequency and can be sensitive to output noise. It also requires output voltage ripple at feedback comparator to perform as a regulator [11]. The ripple is generated by output capacitor's equivalent series resistance (ESR). When using low ESR capacitor the topology may require additional feed forward capacitor to increase voltage ripple on the feedback pin.

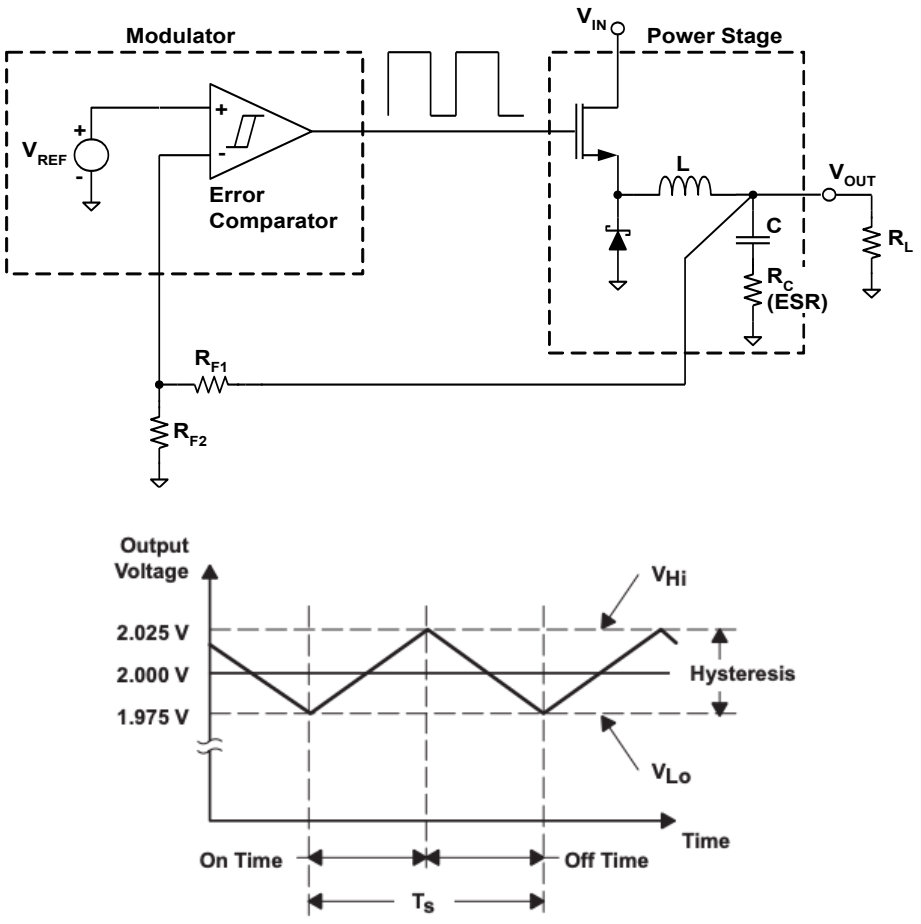


Figure 2-3: Hysteretic control block diagram [12].

Constant on time (COT) control solves the variable switching frequency problem of a hysteretic control. Similar to hysteretic control, COT control offers a simple controller technique in DC-DC converter. As illustrated in Figure 2.3, the controller utilizes a voltage divider network to sense the output voltage just like voltage mode and current mode control [13]. However, with the COT, it is the valley of the output ripple voltage that is being compared with the reference voltage to generate fixed on time pulses to turn on the high side switch (Q1 in Figure 2.3). Then, switch Q1 turns off after the on time, and the low side switch Q2 turns on. What makes COT different from hysteretic control is that it provides better frequency control. A constant on time generator or one-shot timer is added to keep the frequency as constant as possible [14]. Like hysteretic control, COT does not require loop compensation and provides fast transient response, almost two times faster than voltage and current mode [9]. Since it uses ESR to generate the output ripple voltage, it faces similar problems as hysteretic controller when it comes to adding intentional series resistance or needing higher ESR capacitors that make the design more complicated. There are modern COT technologies that can create a ripple voltage by sensing the current on the low side MOSFET (Q2) [14]. However, COT is still not widely popular in the industry as current mode control.

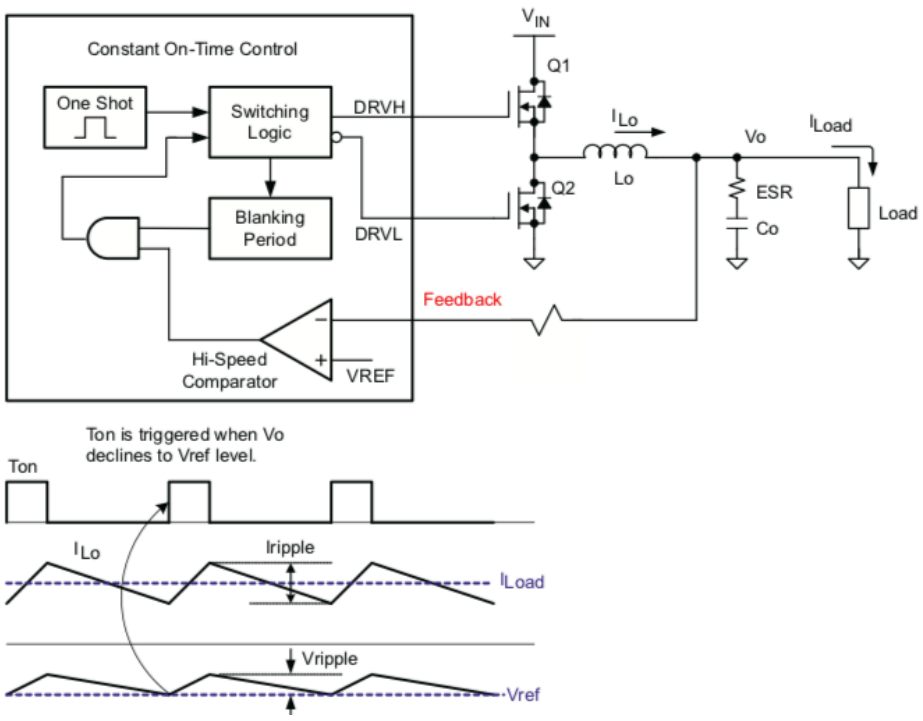


Figure 2-4: Constant on time control block diagram [13].

For the MISO converter used in the DC House project, the latest design utilizes the current mode control. This is because the commercially available controller used for the MISO converter design is already equipped with the current mode controller [8]. As previously stated, the latest version of the MISO converter utilizes the four-switch buck-boost topology which enables a wide input range operation needed for the DC House project. In the past, the converter has been tested for its steady-state operation and performances which include line and load regulations, peak to peak ripple at full load, and overall efficiency of the converter. However, the converter has never been tested under transient conditions such as a sudden change in its input voltage and/or output current. Such study will be critical to evaluate the overall performance of the converter under various operating conditions. This in turn will ensure the proper operation of the converter when it is used in the actual field implementation of the DC house system.

This thesis entails the stability analysis and study of the latest Cal Poly's MISO converter for DC house project. First, it will cover the study of the feedback controller technique and circuitry to understand how the current mode controller is used in conjunction with equal load sharing control implemented in the MISO converter. Following this, the controller function will be formulated, and its time and frequency domain analysis will be conducted to evaluate the overall stability performance of the converter under different input voltage and load conditions. In addition, the current sharing circuit network will be implemented to further analyze the stability metrics for the overall circuitry.

3. Performance Test Measurement Requirements

The stability of a system relates to its ability to respond to change in its inputs, outputs, and undesired inputs such as disturbances. One of the design requirements is choosing the correct analysis method to test the stability of the circuit. In step response method, time domain performance measurements such as percent overshoot, percent undershoot, and settling time quantify stability. A frequency response gives more information than step response as it allows for a quantitative measure of stability of a system by utilizing resonant frequencies, phase margin, and gain margin. The gain and phase margins are also known as the classical stability criteria.

Figure 3.1 shows the block diagram of the MISO converter using current mode control. As mentioned in the previous chapter, the outer loop is similar to voltage mode control while the inner loop is the extra loop needed for current mode control. Unlike traditional current mode control block diagrams, the outer loop has an additional current input on the feedback network. This additional circuitry block called the current share block enables the current sharing ability among different MISO converters. Without this block, a single module can be overloaded with power causing the module failure. The block compares the Imon current sensed by the current sensing block with the current of other blocks to set the largest one as the master. The load is then adjusted by pushing current in or out of the compensation block.

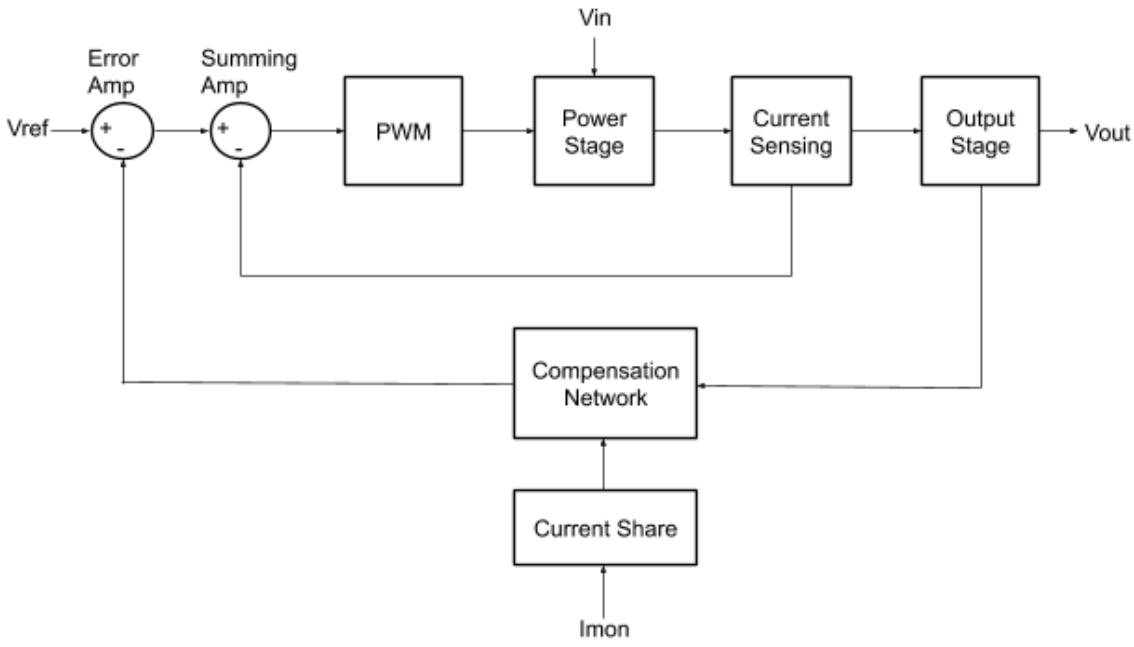


Figure 3-1: Level 0 block diagram for current mode control.

This thesis derives the transfer function for each block in Figure 3.1 and the entire system. After that, the thesis implements the blocks in MATLAB Simulink where frequency domain tests are performed under different load conditions and input voltages. The input voltage range is 10V-60V and the load conditions vary from light load around 0.1A up to 4.17A. The phase margin and gain margin of the overall system are measured and analyzed to see the stability of the overall system. The phase margin is measured at the crossover frequency where the gain crosses 0 dB. The greater the gain margin and phase margin, the greater the stability of the system. For a stable system, the minimum requirement for phase margin is 45° and the gain margin is 10 dB. In addition, the block diagram in Figure 3.1 will also be tested in time domain using step up and step-down inputs to look at the overshoot, undershoot, rise time and setting time. The load would step up from 10% to 90% of the load (0.42A to 3.75A) and step down from 3.75A to

0.42A at nominal input voltage of 24V. As for the input, the step response would be observed for a step-up change from 10V to 60 and step down from 60V to 10V. Table 3.1 summarizes the measurement requirements that will be conducted in this thesis.

Table 3-1: Performance test summary for MATLAB Simulink

Measurement	Domain	Justification
Phase Margin	Frequency	Shows the amount of change in open-loop phase needed to make a closed-loop system unstable, should be greater than 45°
Gain Margin	Frequency	Shows the amount of change in open-loop gain needed to make a closed-loop system unstable, must be greater than or equal to 10 dB
% Overshoot	Time	Shows the limit for excess output voltage allowed for a step change in the input, should not exceed 10% of the steady state value
% Undershoot	Time	Shows the amount by which the output voltage falls short of the desired value due to a step change in the input, should not exceed 10% of the steady state value
Rise time	Time	Shows the time it takes for the response to rise from 10% of final to 90% of the final value
Settling time	Time	Represents the time it takes for the step response to get with 2% of the steady state value

4. Controller Model Design

This chapter discusses the controller design for MISO converter in MATLAB Simulink in frequency domain. The first step in the controller model design is deriving the transfer functions for each block shown in Chapter 3. Since the converter uses a switching circuit, the converter is non-linear and needs linearization. A small signal model effectively models the linearized power stage. Note that the small signal model only applies to continuous conduction mode (CCM), thus the simulation will only look at the converter operating in CCM conditions. The MISO converter uses peak current mode (PCM) control which simplifies the internal current loop compared to average current mode control. It employs a current sampling ramp to compare with the output of the error amplifier to generate the regulated duty cycle [14]. Figure 4.2 shows a buck converter using PCM controller using small signal model where Vo is the output voltage. Appendix A shows additional models to linearize the system. The model shown in Figure 4.1 along with Figure 4.2 will be used in this chapter as guidance when deriving the transfer function for the power stage, output stage and compensation in the MISO converter.

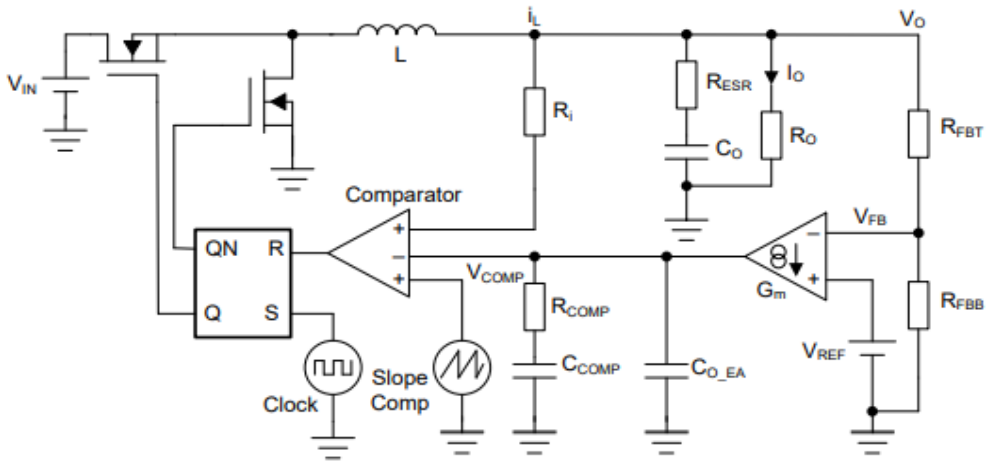


Figure 4-1: Simplified schematic for peak mode current buck converter [14].

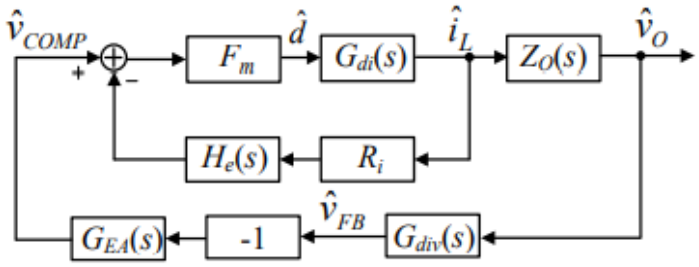


Figure 4-2: Small signal model for peak current mode buck converter [14].

4.1 Output Stage

In Figure 4.1, the Zo block is the output stage for the MISO converter which includes the output capacitor and the load resistor. The equivalent series resistance (ESR) for the output capacitor is also considered when deriving the transfer function since the ESR and the output capacitor adds another zero to the system which affects the compensation network. The leakage is not considered since DC-DC converters operate at high frequency. Figure 4.3 shows the circuit diagram for the output stage. Using this figure, the transfer function is derived as a function of output voltage to inductor current.

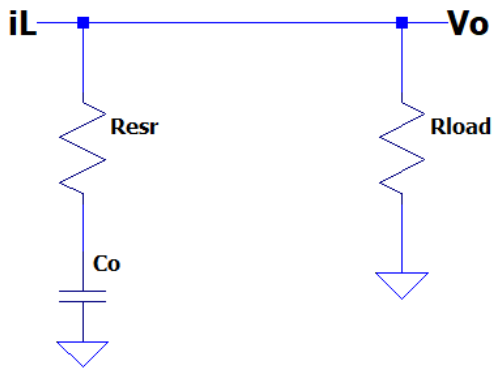


Figure 4-3: Output stage of the MISO circuit.

Using Kirchhoff's current law,

$$i_L = \frac{V_o}{\left(R_{ESR} + \frac{1}{sC_o}\right)} + \frac{V_o}{R_{load}}$$

$$i_L = V_o\left(\frac{sC_o}{sC_oR_{ESR} + 1} + \frac{1}{R_{load}}\right) = V_o\left(\frac{sC_oR_{load} + 1 + sR_{ESR}C_o}{R_{load}(1 + sR_{ESR}C_o)}\right)$$

Thus,

$$\frac{V_o}{i_L} = R_{load} \times \frac{1 + sR_{ESR}C_o}{1 + sC_o[R_{ESR} + R_{load}]} \qquad (4.1)$$

The thesis also requires changing the load to measure load transient. This can be done using a variable input transfer function block in Simulink.

4.2 Power Stage

The power stage includes the inductor with the transfer function from duty cycle to inductor current [14].

$$\frac{i_L}{D} = \frac{V_{in}(1 + sR_{load}C_o)}{s^2LR_{load}C_o + sL + R_{load}} \qquad (4.2)$$

The transfer function shown in equation 4.2 turns into equation 4.3 if the crossover frequency is much higher than the corner frequency [14].

$$\frac{i_L}{D} = \frac{V_{in}}{sL} \qquad (4.3)$$

4.3 Compensation Network

The next block for the MISO controller model is the compensator block. This block takes in the output voltage, compares it to the given reference and provides a

compensating gain value to maintain the output voltage to the desired value of 48V. The compensator model can be type 1, 2 or 3.

The type 2 compensation is commonly used with current mode control. For the LT8390 utilized by the MISO converter, an internal transconductance amplifier is used. Figure 4.4 shows the internal functional block diagram of the LT3890 switching controller [15]. Note that the internal reference voltage is 1V and EA1 is the internal transconductance amplifier compensated by Vc pin that uses external compensation network.

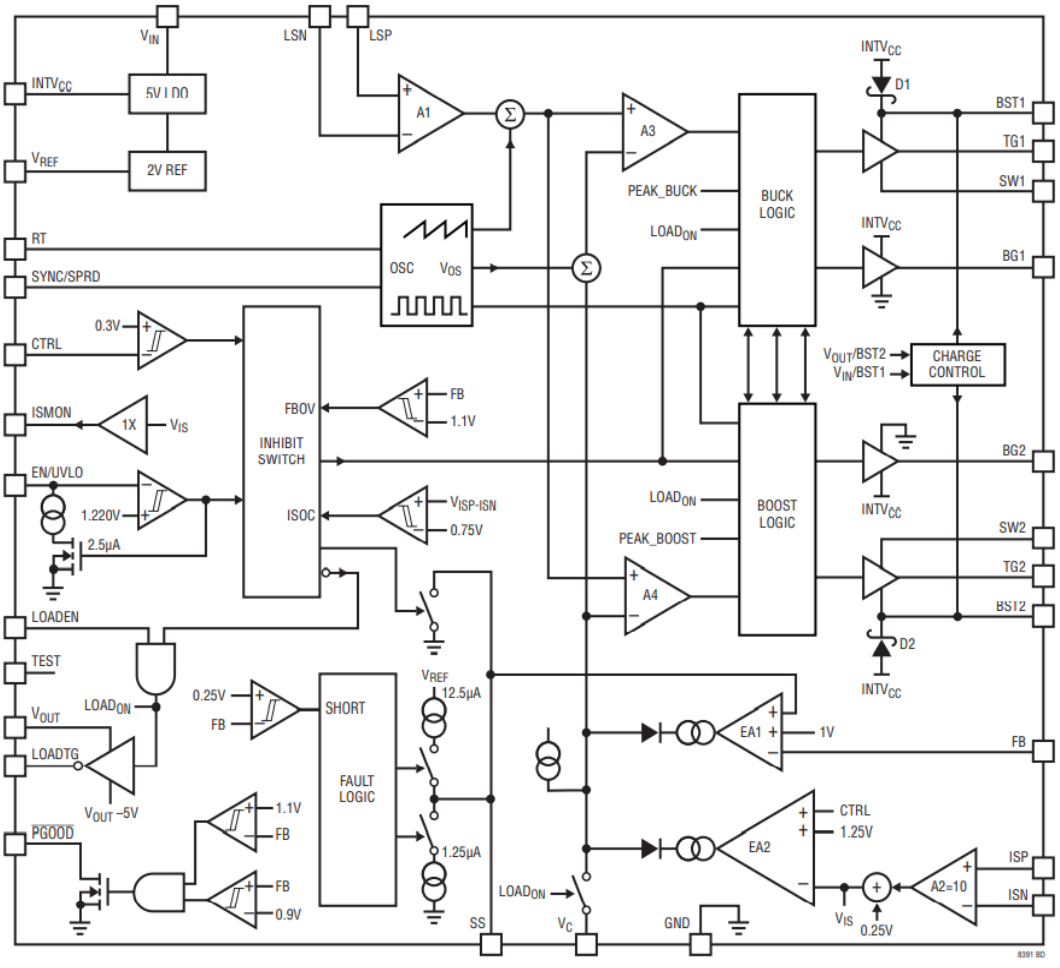


Figure 4-4: Internal circuitry for LT8390, converter used in the MISO circuit.

Figure 4.5 illustrates the type 2 compensator with the transconductance [16]. Current mode control has a single pole on the low frequency and the compensation needs only a single pole role off and a single zero phase lead [9]. C3 is not necessary but can be useful for noise attenuation at high frequencies.

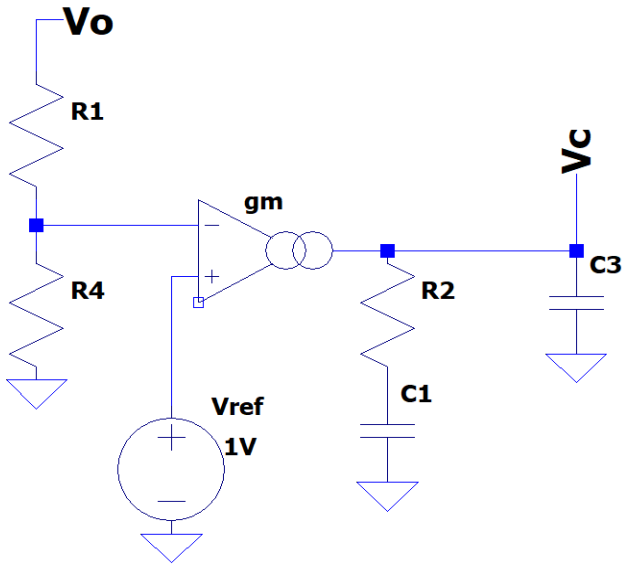


Figure 4-5: Type two transconductance operational amplifier schematic.

The output to input transfer function is:

$$\frac{V_c}{V_o} = -gm \times \frac{R_4}{R_1 + R_4} \times \frac{1 + sR_2C_1}{s(C_1 + C_3) + s^2R_2C_3C_1} \qquad (4.4)$$

Sometimes a type three amplifier is needed for additional phase boost. The type 3 compensator may also have the transconductance as depicted in Figure 4.6 [16].

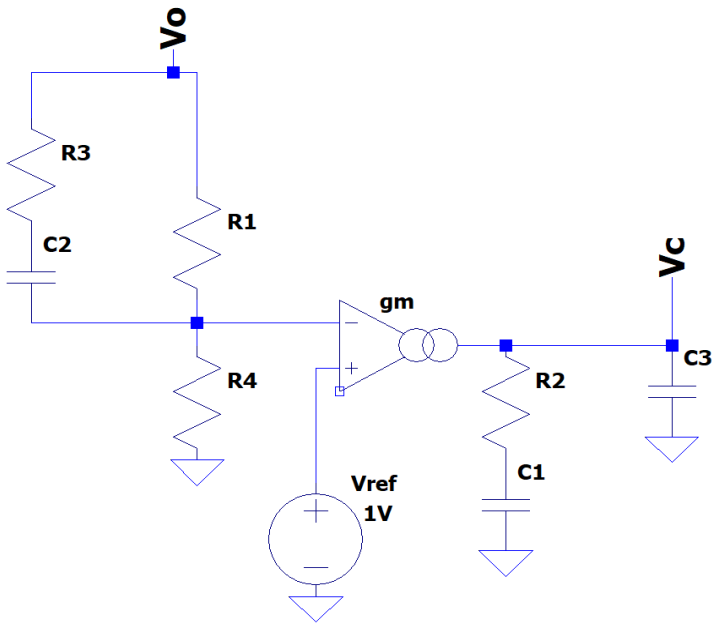


Figure 4-6: Type three transconductance operational amplifier schematic.

The transfer output to input transfer function is:

$$\frac{V_c}{V_o} = -gm \times \frac{R_4 + s(R_1 + R_3)C_2R_4}{R_1 + R_4 + s(R_4R_1 + R_3R_1 + R_3R_4)C_2} \times \frac{1 + sR_2C_1}{s(C_1 + C_3) + s^2R_2C_3C_1} \quad (4.5)$$

4.4 Inner Current Loop

The inner current loop with the He(s) and Ri(s) blocks in Figure 4.2 consists of the sample and hold inductor current value. This block takes the average of inductor current and feeds it to the comparator. Knowing that the system works in peak current mode, this block can be further simplified to get rid of the He(s) block that accounts for the inductor current sample and hold effect to generate average inductor current [17]. This reduces the inner loop transfer function to the following where A1 is the gain for block comparator A1 in Figure 4.4.

$$\frac{V_s}{i_L} = A1 \times R_{sense} \qquad (4.6)$$

4.5 PWM Gain

The gain block for the PWM considers the actual inductor changing slope in comparison with the fixed external ramp generated by the oscillator for slope compensation. Slope compensation is needed for a current mode converter to operate at duty cycle higher than 0.5 to dampen subharmonic oscillation.

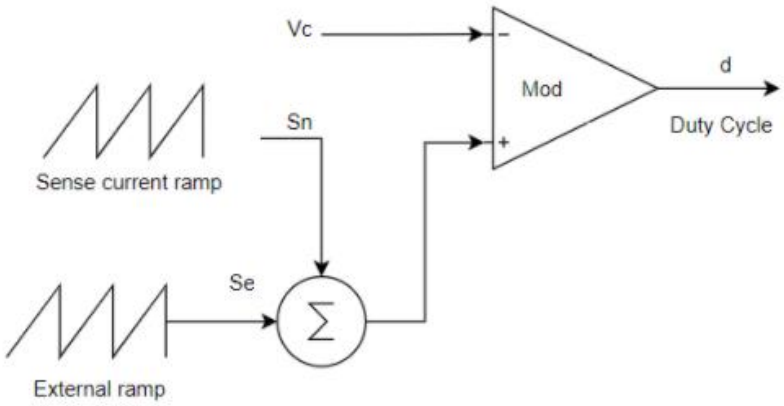


Figure 4-7: Slope compensation gain schematic.

Using [14] as the guidance, the gain block F_m is derived using Figure 4.7. This refers to the gain blocks A3 and A4 in Figure 4.4 that amplify the difference between the outer and inner compensator loop output.

$$F_m = \frac{f_{sw}}{S_e + S_n} \qquad (4.7)$$

In the above gain block equation, S_e is the slope compensation rising slope element generated by the internal oscillator whose equation is:

$$S_e = V_{oscpeak} \times f_{sw} \qquad (4.8)$$

S_n is the rising slope of the inductor current whose value depends on whether the MISO is in buck or boost mode. For the buck mode, the equation is

$$S_n = \frac{(V_{in} - V_o)R_{sense}}{L} \qquad (4.9)$$

While for the boost mode:

$$S_n = \frac{(V_{in})R_{sense}}{L} \qquad (4.10)$$

4.6 Current Share

The current sharing circuit is what allows the MISO converter to connect in parallel with other MISO modules and to share total output current equally among the parallel MISO converters. The MISO uses active current sharing technique which automatically assigns a master and slaves. The master's voltage is what compares with other slave modules to push or pull current from the feedback pin. In Figure 4.8 [8], ISMON_self represents the output voltage of a module and ISMON_all is the output voltage from another MISO module. The voltages are compared using a differential amplifier U02A which has a DC offset equivalent to V_{FB_self} voltage coming from the voltage follower circuit U02D. The transfer function for this module was made using the differential amplifier with an offset.

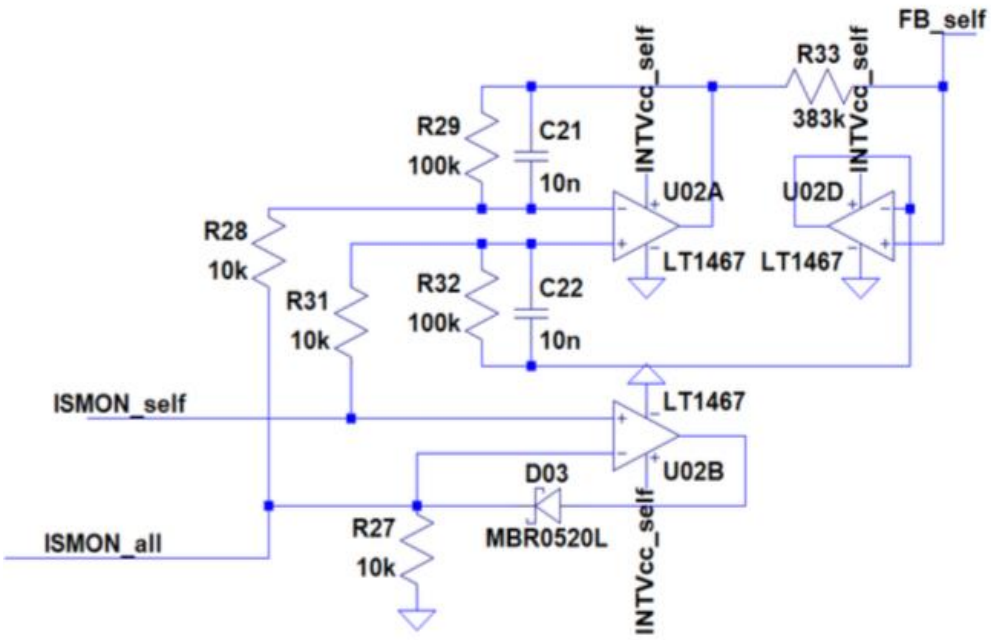


Figure 4-8: MISO current sharing circuit schematic [8].

For simplification, Figure 4.9 is redrawn as Figure 4.8 where Zf refers to the total feedback impedance network made of R29 and C21 or R32 and C22 pairs. Rin represents R28 and R31. In addition, ISMON_self is V2 and ISMON_all is V1. Vf is the FB_self.

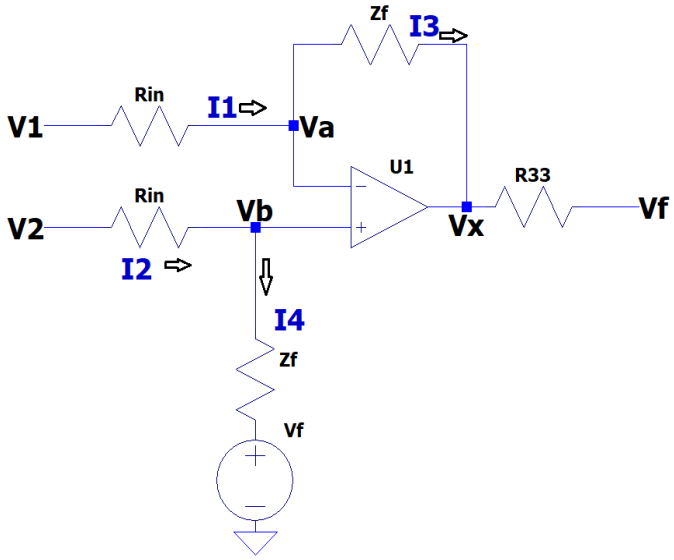


Figure 4-9: Simplified MISO current sharing circuit schematic.

The transfer function of the current sharing circuit as shown in Figure 4.9 is derived as follows. Starting with the feedback network total impedance where R32 and C22 are parallel,

$$Z_f = \frac{\frac{R_{32}}{sC_{22}}}{R_{32} + \frac{1}{sC_{22}}} \qquad (4.11)$$

Note that the above equation also applies to R29 and C21 pair. As mentioned before, Rin in Figure 4.9 refers to R28 and R31 in Figure 4.8. Based on Figure 4.9, the equations for each current are

$$I_1 = \frac{V_1 - V_a}{R_{in}}$$

$$I_2 = \frac{V_2 - V_b}{R_{in}}$$

$$I_3 = \frac{V_a - V_x}{Z_f}$$

$$I_4 = \frac{V_b - V_f}{Z_f}$$

Since there is zero current going into the positive node of the amplifier,

$$I_2 = I_4$$

Similarly,

$$I_1 = I_3$$

This further yield

$$I_4 = I_2$$

$$\frac{V_b - V_f}{Z_f} = \frac{V_2 - V_b}{R_{in}}$$

$$V_b(R_{in} + Z_f) = V_2 Z_f + V_f R_{in}$$

Since the voltage across the terminal nodes are always equal for an op amp,

$$V_a = V_b$$

Substituting V_a with V_b yields

$$V_a = V_b = \frac{V_2 Z_f + V_f R_{in}}{R_{in} + Z_f}$$

$$I_1 = I_3$$

$$(V_1 - V_a)Z_f = (V_a - V_x)R_{in}$$

$$\frac{Z_f}{R_{in}}(V_1 - V_a) = V_a - V_x$$

$$V_x = Va\left(1 + \frac{Z_f}{R_{in}}\right) - \frac{Z_f}{R_{in}}V_1$$

Substitute for V_a yields:

$$V_x = \frac{V_2 Z_f + V_f R_{in}}{R_{in} + Z_f}\left(\frac{Z_f + R_{in}}{R_{in}}\right) - \frac{Z_f}{R_{in}}V_1$$

$$V_x = \frac{V_2 Z_f + V_f R_{in}}{R_{in}} - \frac{Z_f}{R_{in}}V_1$$

$$V_x = (V_2 - V_1)\frac{Z_f}{R_{in}} + V_f$$

$$V_f = -(V_2 - V_1)\frac{Z_f}{R_{in}} + V_x \qquad (4.12)$$

I_{out} is the current going through R33 in Figure 4.9,

$$I_{out33} = \frac{V_x - V_f}{R_{33}}$$

Rewriting V_x in terms of Z_f and V_f,

$$I_{out33} = Z_f \frac{V_2 - V_1}{R_{in}R_{33}}$$

Using $R_{in} = R_{31}$ and equation 4.11,

$$I_{out33} = \frac{R_{32}}{sC_{22}R_{32} + 1} \times \frac{V_2 - V_1}{R_{31}R_{33}} \qquad (4.13)$$

I_{out33} is the current that gets pushed into or pulled from the feedback pin. Since the feedback network uses big resistor values, it can be assumed that the current going through R5, R13 and R6 is zero in Figure 4.10 [8].

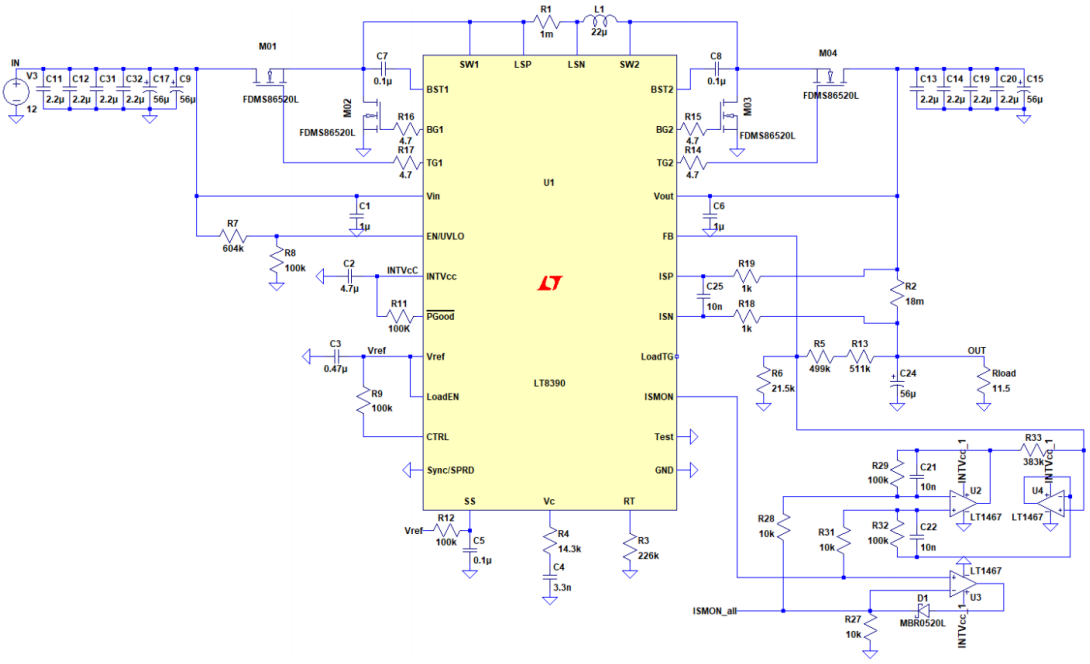


Figure 4-10: MISO schematic with current sharing network.

The ISP and ISN pin use a sense resistor to detect the current through each module and convert it to voltage for active current sharing comparison.

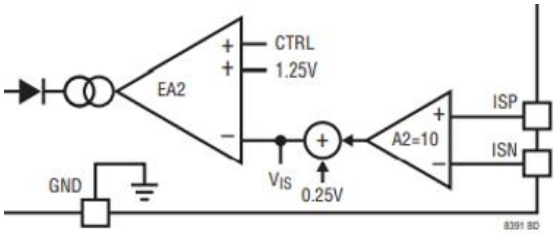


Figure 4-11: LT8390 internal current sharing circuit, note that Vis is the voltage that is compared between modules to set the master and slave.

Based on the datasheet portion for current sharing in Figure 4.11, the ISMON_self or V_{IS} or V_2 voltage equals

$$V_2 = A_2 V_{sense} + 0.25V$$

$$V_{sense} = I_{out} \times R_{sense} \text{ and } A_2 = 10$$

$$V_2 = 10 I_{out} \times R_{sense} + 0.25V \qquad (4.14)$$

The total FB voltage is the summation of the resistor divider voltage added with V_f from the current sharing circuit.

$$V_{FBtot} = V_{FB} + V_f$$

Using superposition,

$$V_{FB} = \frac{R_6}{R_6 + R_5 + R_{13}} V_{out} \qquad (4.15)$$

Since the output and the feedback pin nodes are both high impedances, the current coming from the current sharing network goes through R6 only,

$$V_f = R_6 I_{out33} \qquad (4.16)$$

Combining (4.12) and (4.15) gives

$$V_{FBtot} = \frac{R_6}{R_6 + R_5 + R_{13}} V_{out} + R_6 I_{out33}$$

$$V_{FBtot} = \frac{R_6}{R_6 + R_5 + R_{13}} V_{out} + R_6 \frac{R_{32}}{sC_{22}R_{32} + 1} \times \frac{V_2 - V_1}{R_{31}R_{33}} \qquad (4.17)$$

This voltage corresponds to the current that is added or taken from the feedback pin to enforce current sharing between multiple 200W MISO modules.

5. Simulation Results and Analysis

This chapter uses the component values from the MISO schematic [8] in the transfer functions derived in Chapter 4. Some assumptions are made to get as accurate response as possible. Similar to Chapter 4, this chapter is divided into subsections discussing each block.

5.1 Output Stage

Using the following component values from MISO schematic and equation 4.1, the overall transfer function for the output stage reduces to the following. The original model uses two output electrolytic capacitors with 30 mΩ ESR. There are also 4 ceramic capacitors use for filtering the output. Typical ESR for ceramic capacitors range from 0.01 to 0.1 Ω. The total calculated ESR using both extremes fall in the range between 3 mΩ -12.6 mΩ. The simulation model only works for continuous conduction mode. Hence, the load varied from 0.1 A to 4.12 A which correspond to 480 Ω and 11.5 Ω for a 200 W system. In addition, the inductor value used in the circuit is 22 µH. To summarize:

R_{load} = 11.5 Ω - 480 Ω

R_{ESR} = 3 mΩ - 12.6 mΩ

Co = 120.8 µF, L = 22 µH

Using these component values into the $\frac{V_o}{i_L}$ transfer function in the previous chapter yields:

$$\frac{V_o}{i_L} = 11.5 \times \frac{1 + 3.62 \times 10^{-7} s}{1 + 0.001389 s}$$

Figure 5.1 shows the Simulink model using this transfer function.

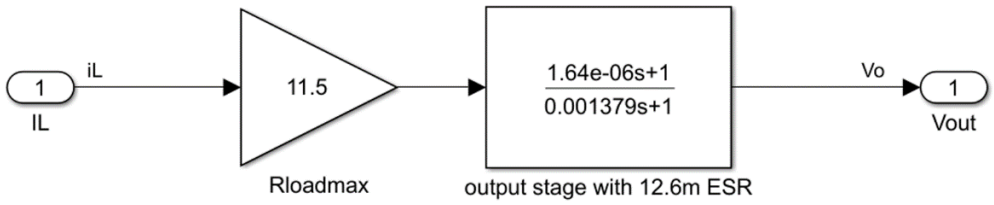


Figure 5-1: Output stage Simulink model at maximum load and ESR.

In control system performance test, step response helps analyze a system's stability by showing how the system reacts when its input or load suddenly changes. Since the setup will be tested on varying load conditions to evaluate system performance under the load transient, the variable input transfer function block is used as follows where a_0 is the summation of the load resistance and the equivalent series resistance.

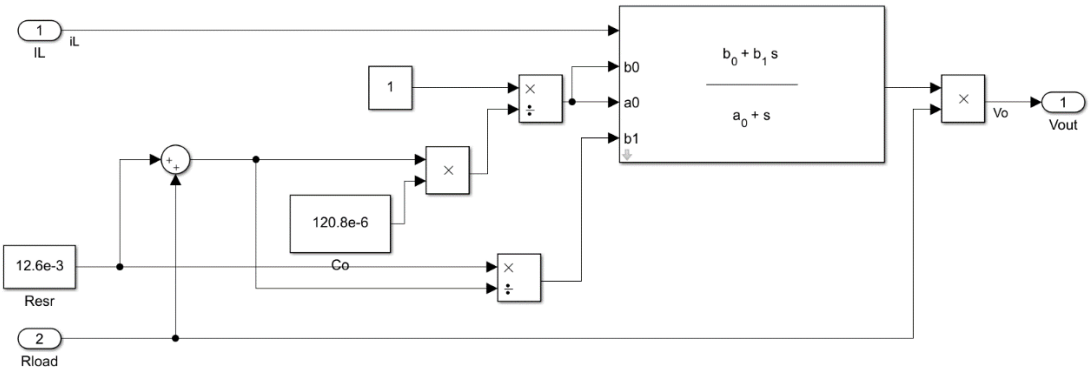


Figure 5-2: Output stage Simulink model with variable load and ESR.

5.2 Power Stage

Referring to the MISO schematic again, the component values for the power stage are as follows:

Inductor L = 22 µH, load resistor R_{load} = 11.5 Ω, Output capacitor's Equivalent Series Resistance R_{ESR} = 12.6 mΩ, and output capacitance Co=120.8 µF.

Putting these values into the transfer function $\frac{i_L}{D}$ as provided in equation 4.2 yields:

$$\frac{i_L}{D} = \frac{V_{in}(1 + 0.001389s)}{3 \times 10^{-8}s^2 + 22 \times 10^{-6}s + 11.5}$$

This is implemented in the Simulink block as shown in Figure 5.3.

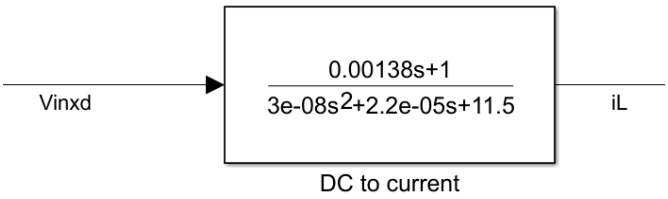


Figure 5-3: Non-simplified power stage Simulink model.

A simplification can be made to the above model if the crossover frequency is higher than the corner frequency. For this system, the corner frequency is 3.07 kHz. Cross-over frequency generally falls between 1/4 to 1/10 of the switching frequency. Keeping that in mind, the crossover frequency for MISO should be between 20 kHz-50 kHz. This is ten times larger than the corner frequency and therefore the system can be simplified. The thesis uses the following transfer function to find the inductor current based on input voltage and transfer function.

$$\frac{i_L}{D} = \frac{V_{in}}{22 \times 10^{-6}s}$$

5.3 Type 2 Compensation Amplifier

The original MISO compensation network as depicted in Figure 5.4 uses resistor R2 value of 14.3 kΩ and capacitor C1 of 3.3 nF. Capacitor C3 has no specified value in the original model. C3 is an additional capacitor to a type two amplifier that gives an additional pole to the system. The value for this capacitor as commonly done in practice is 0.1 pF to model a small capacitor such that its effect on the overall compensator response is negligible. After further evaluation and testing, this capacitor value is adjusted to obtain the desired system's stability performance.

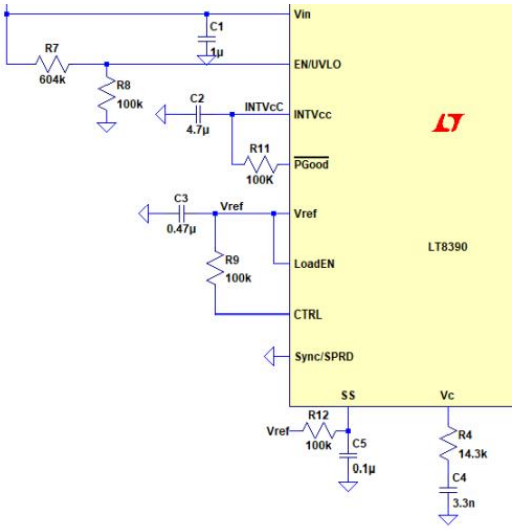


Figure 5-4: Original MISO converter showing compensation resistor and capacitor in Vc pin.

To summarize, the component values for the compensator are:

R1 = 1010 kΩ, R4 = 21.5 kΩ, R2 = 14.3 kΩ

C1 = 3.3 nF, C3 = 0.1 pF

gm = 660 µS from LT8390 datasheet [15]

Using the $\frac{V_c}{V_o}$ transfer function derived in Chapter 4, the above component numerical values give the following transfer function:

$$\frac{V_c}{V_o} = -660 \times 10^{-6} \times \frac{21.5k}{21.5k + 1010k} \times \frac{1 + 47.19 \times 10^{-6}s}{3.3 \times 10^{-9}s + 4.719 \times 10^{-18}s^2}$$

As before, the transfer function is then implemented as a Simulink block diagram as depicted in Figure 5.5.

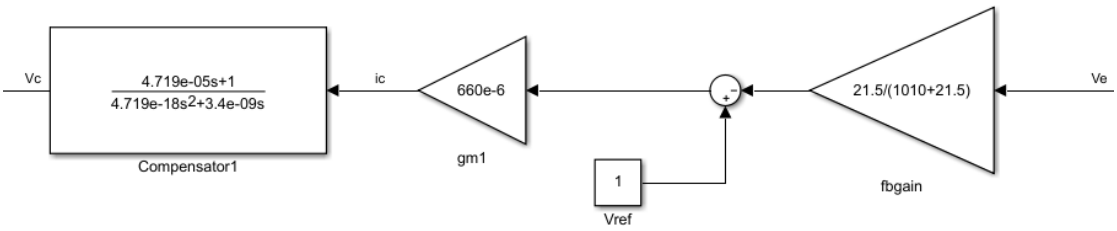


Figure 5-5: Type 2 compensation network Simulink model.

The inner compensation current loop is a simple model made of the current sense resistor amplified by a certain gain. If the inner loop is not stable the system shows subharmonic oscillations. Since the LT8390 converter [15] datasheet does not provide a value for A1, the Simulink model will use different gain to tune the system.

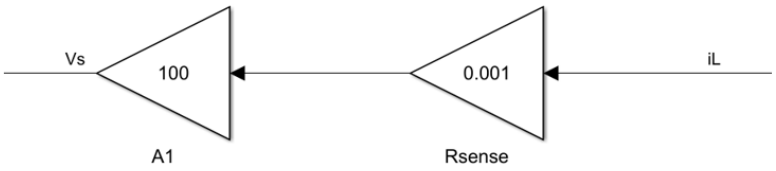


Figure 5-6: Inner loop current compensation network.

5.4 PWM Gain

The general assumption for Vosc, which is the internal oscillation voltage within the PWM block, is that it cannot exceed the reference voltage. Assuming that Vosc is equal to the reference voltage and using equations 4.6, 4.7 and 4.8, the transfer function for the gain block reduces to the following:

$$S_e = V_{oscpeak} \times f_{sw} = 0.2\frac{\text{V}}{\mu\text{s}}$$

Peak buck mode:

$$S_n = \frac{(V_{in} - V_o)1\ \text{m}\Omega}{22\ \mu H}$$

Peak boost mode:

$$S_n = \frac{(V_{in})\ 1\ \text{m}\Omega}{22\ \mu H}$$

Using the above definitions for Se and Sn, the gain function (F_m) block is shown below. Note that F_m is the value that the compensator output that multiplies with the error voltage to get the small signal duty cycle.

$$F_m = \frac{200kHz}{0.2\frac{\text{V}}{\mu\text{s}} + \frac{(V_{in} - V_o)1\text{m}\Omega}{22uH}}$$

The Simulink model for the PWM gain block uses a gain block that is manually changed based on the mode of operation as shown in Figure 5.7. With the initial block gain set to 0, the system works in the boost mode operation by making Vo to be zero. Alternately if the gain is set to 1, then it works on the buck mode of operation.

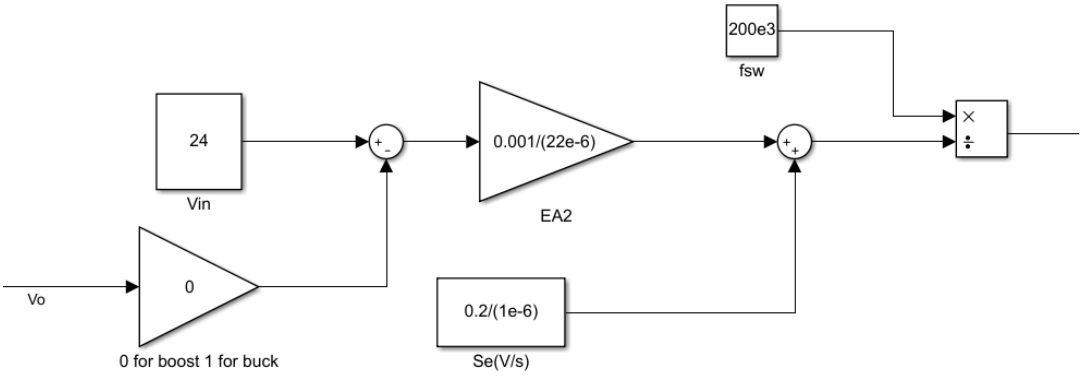


Figure 5-7: PWM gain Simulink model.

5.5 Current Share

Using superposition, the equation for total voltage to the feedback node in Chapter 4 is:

$$V_{FBtot} = \frac{R_6}{R_6 + R_5 + R_{13}} V_{out} + R_6 \frac{R_{32}}{sC_{22}R_{32} + 1} \times \frac{V_2 - V_1}{R_{31}R_{33}}$$

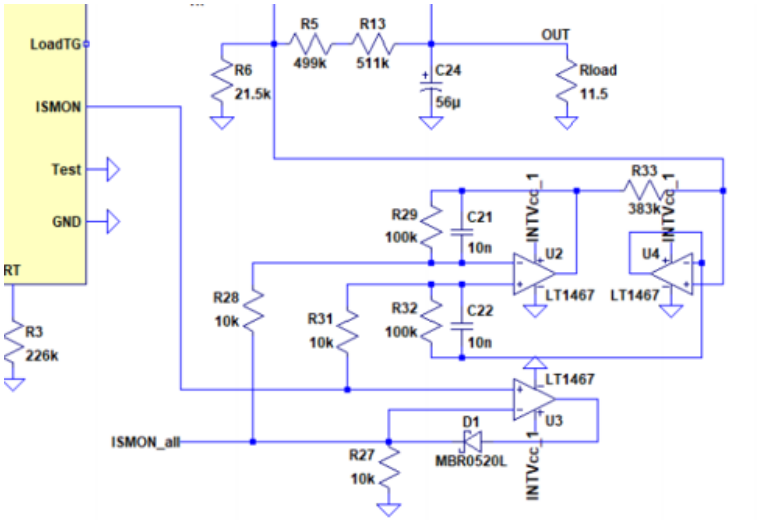


Figure 5-8: MISO module with current share network components.

Using values for resistors and capacitors in Figure 5.8,

$$V_{FBtot} = \frac{21.5}{21.5 + 1010} V_{out} + \frac{21.5 \times 100}{10 \times 383} \frac{V_2 - V_1}{0.001s + 1}$$

This total feedback voltage in Simulink is shown in Figure 5.9 where Vout is the output voltage for the master module and Vout2 is the output voltage from a slave module.

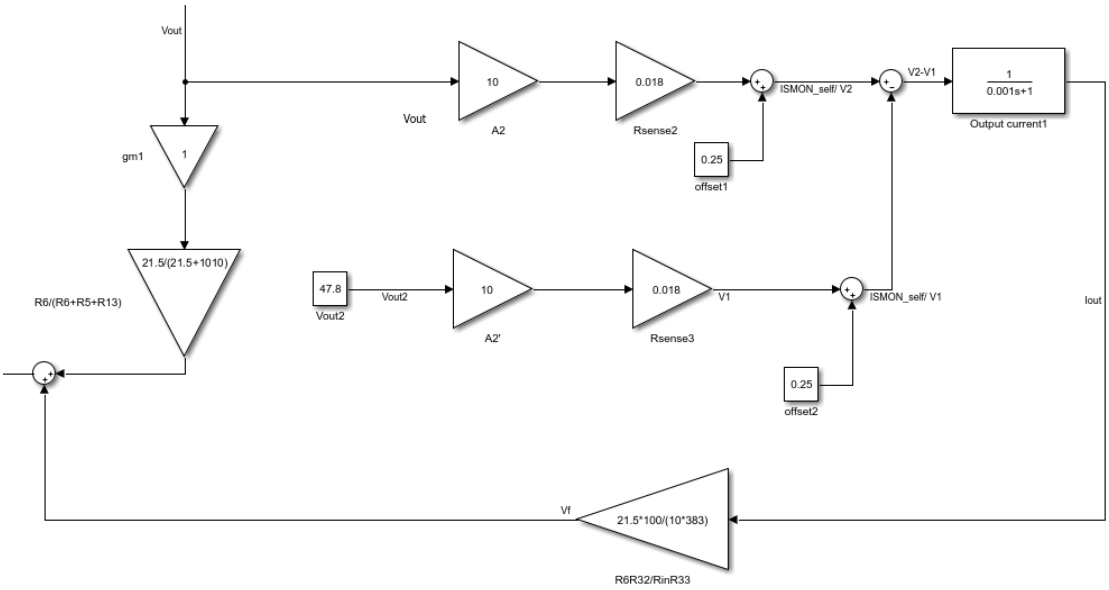


Figure 5-9: Current share circuit simulation model where Vout and Vout2 are the output voltages of two MISO modules.

5.6 Simulation Results

The simulation was first performed without the current sense network to tune the gain for the inner current compensator loop. The inner loop current gain values were changed from 1 to 100 to observe the frequency response. Figure 5.10 shows the Simulink model for a converter with Vin of 24V and maximum load. The bode plots were taken by injection method where a small sinusoidal signal was inserted after the feedback

network to the error amplifier and the output voltage was observed to see how that signal gets amplified.

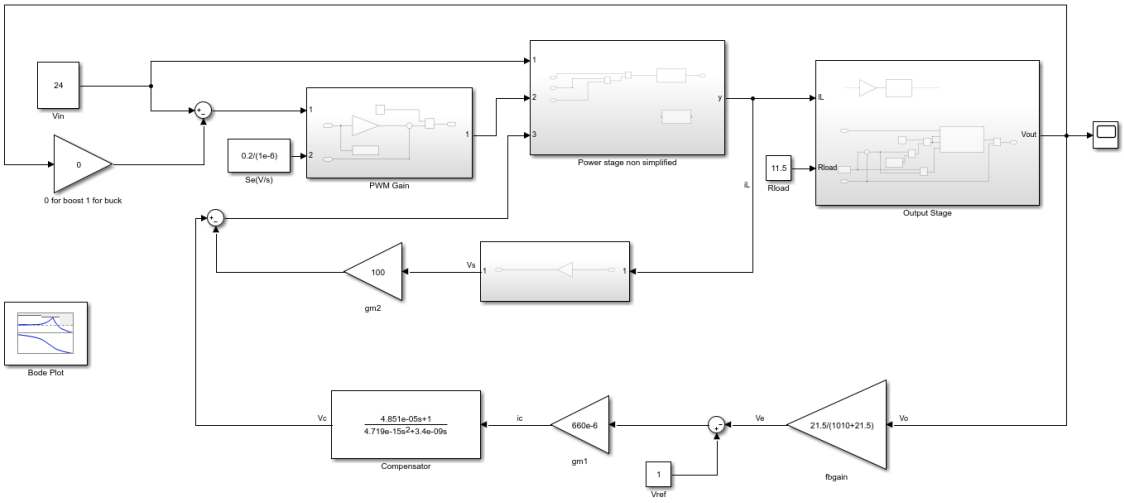


Figure 5-10: Overall model for converter with type 2 compensation.

The system behaves as depicted in Figure 5.11 when the unknown inner current loop gain (A1) is set to 1. There is some oscillation in the output and the system does not settle to expected value of 48V.

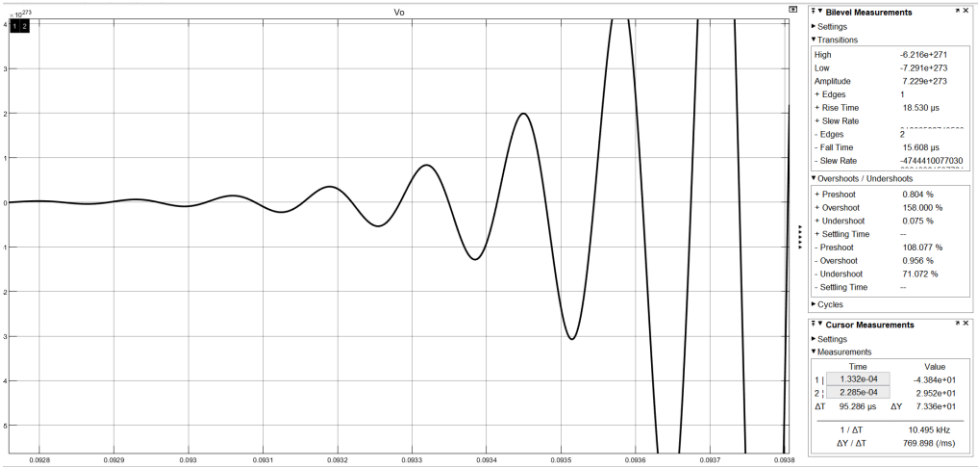


Figure 5-11: Transient output response with inner current loop gain (A1) set to 1 with 24V input and maximum load.

As expected, the system oscillates since the compensation from the inner loop is too small to affect the overall system's response. Any gain higher than 10 in the inner loop makes the system stable. A gain of 100 is chosen after making a model for an example circuit from LT8390 datasheet in Simulink and tuning it. Figure 5.12 shows the transient response for a gain of 100. Note that while the system is stable, the overshoot is higher than expected.

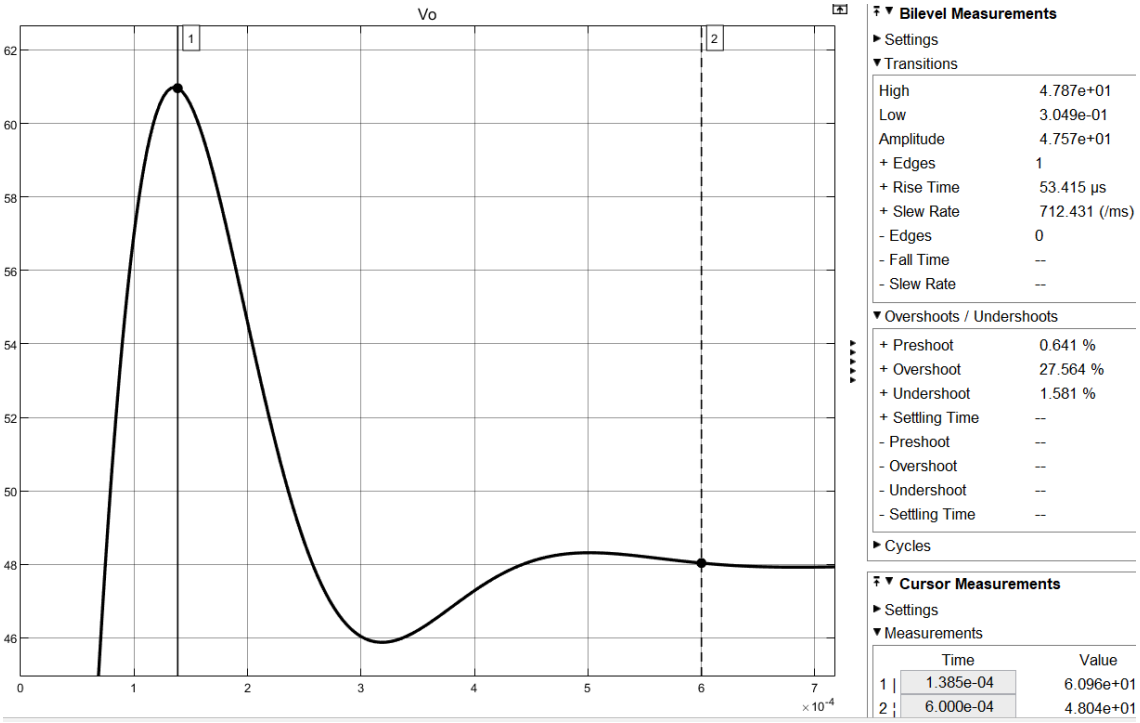


Figure 5-12: Transient response for inner current loop gain (A1) of 100 with 24V input and maximum load.

In Figure 5.13, the phase and gain margins are taken in terms of the system's output voltage and the input voltage to the compensator. The slope at the 0 dB crossing is around -30 dB/decade. Ideally a slope of -20 to -25 dB is preferred since anything over -40dB/decade implies that the gain changes drastically with change in the frequency

making the system unstable. As expected for a DC-DC converter, the gain is high at lower frequencies and reduced at higher frequencies. Based on the response, the closed-loop system is stable with a crossover frequency of 46.6 kHz at nominal input voltage. Additionally, the phase margin falls within the appropriate value of around 45° to ensure stability. Based on this response, the original MISO circuit is stable.

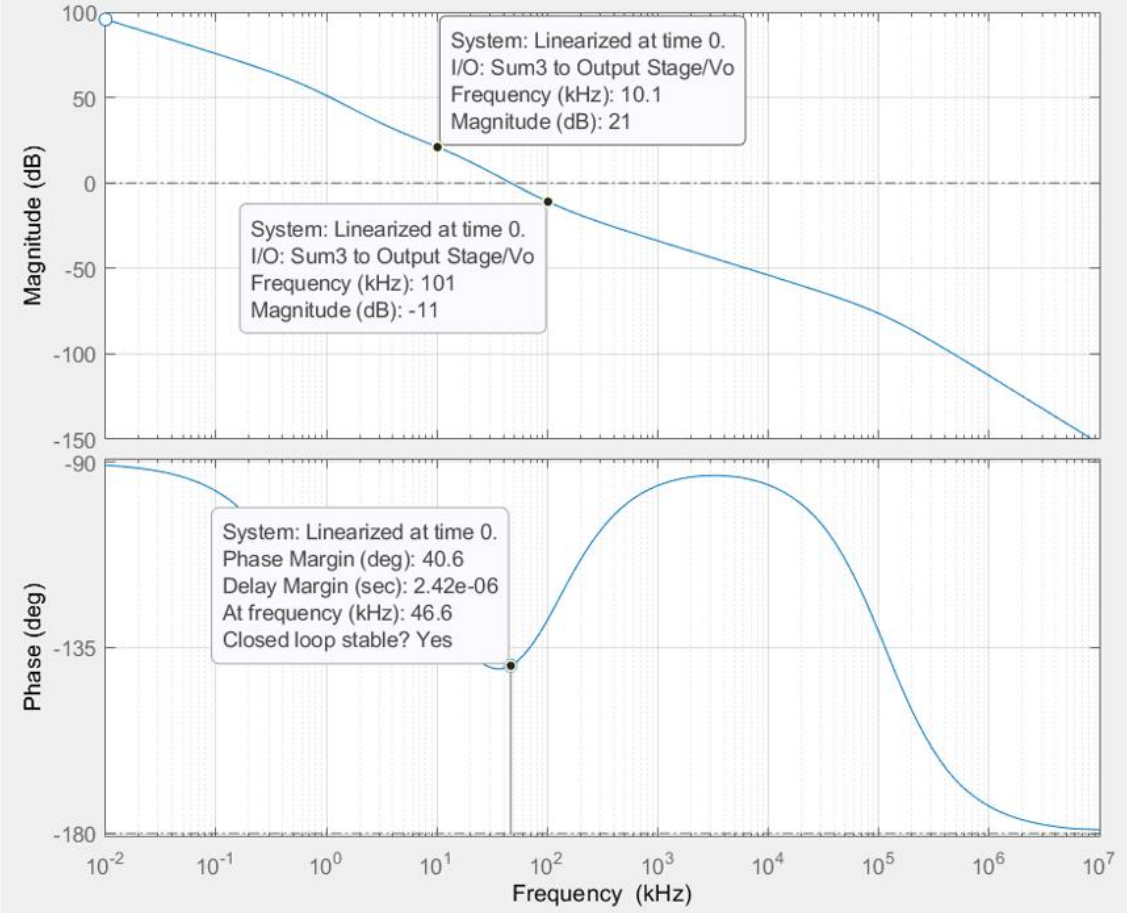


Figure 5-13: Open-loop response with A1 gain of 100 with 24V input and maximum load.

Table 5-1: Simulation summary for original MISO model with 3.3 nF compensator capacitor and 12.6 mΩ ESR

Step conditions	% Overshoot	Rise time(us)	Settling time (ms)	Phase margin (degree)	Gain Margin (dB)
24V Vin	27.56	54.4	0.6	40.6	Inf
90% to 10% load at Vin=24V	27.56	53.44	0.61	40.6	Inf
10% to 90% load at Vin=24V	29.2	52.8	1.46	40.5	Inf
Vin step up from 10V to 60V	29.2	54.0	0.6	63.2	Inf
Vin step down from 60V to 10V	25.5	58.5	0.5	23.7	Inf

5.7 New Design Using Higher C1

Table 5.1 summarizes the frequency response for the original MISO model [8]. The simulation results in a final voltage of 47.98 V and crossover frequency of 46.6 kHz with an input voltage of 24 V. The overshoot is higher than expected value of 10%.

Overshoot represents distortion in signal and one way to lower it is by changing the compensator capacitor C1 value. C1 is inversely proportional to the location of the left-hand plane (LHP) zero [18]. A LHP zero makes the system respond faster to a step change but with higher overshoot and lower rise time. Increasing C1 moves the zero away from the LHP which lowers the overshoot at the cost of increased rise time. The datasheet recommends C1 to be 15 nF. Increasing C1 to 10nF is enough to reach the less than 10% overshoot threshold. However, further increasing C1 also increases the phase

margin. Therefore, in order to achieve a higher phase margin and lower overshoot, C1 was raised to 15nF as advised by LT8390 datasheet. With new capacitor C1 value of 15 nF, the system still maintains the crossover frequency of 47 kHz at nominal input voltage with a lowered percent overshoot as shown in Figure 5.15 which shows the new transient response.

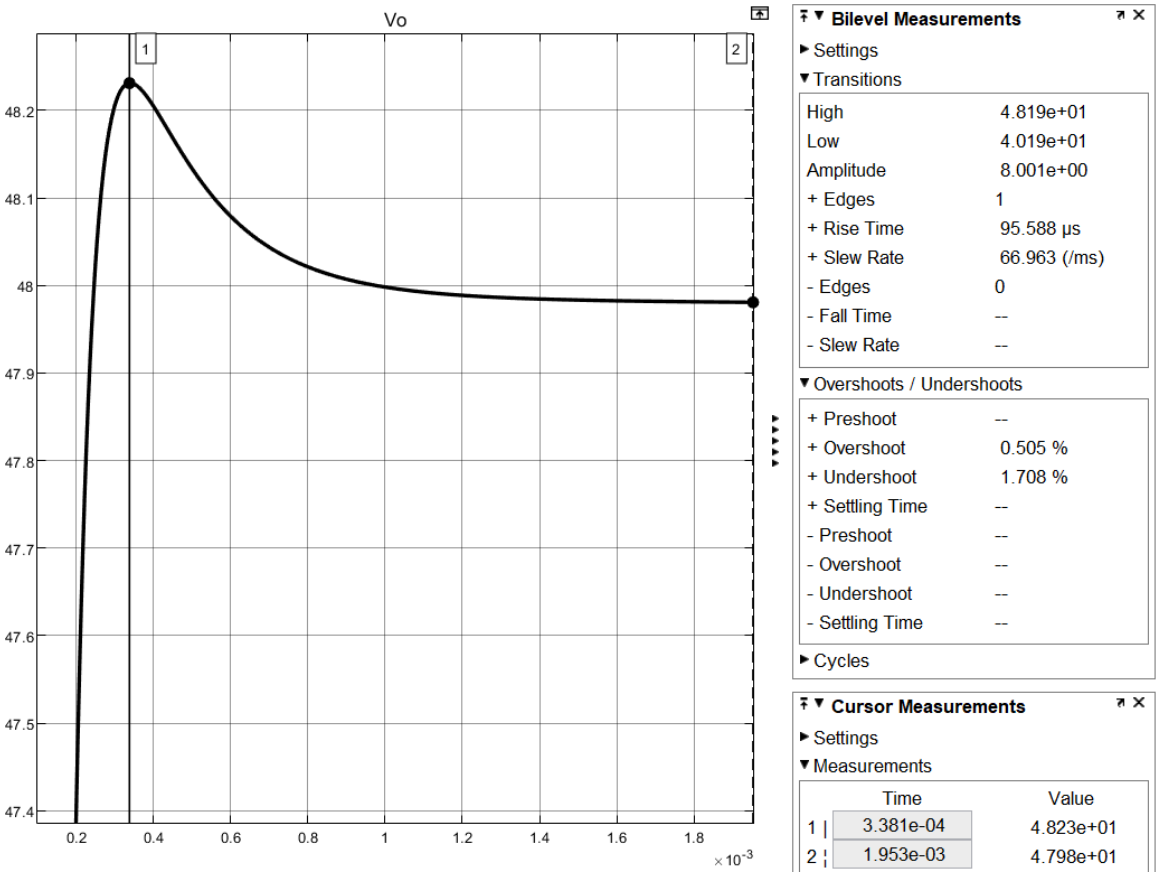
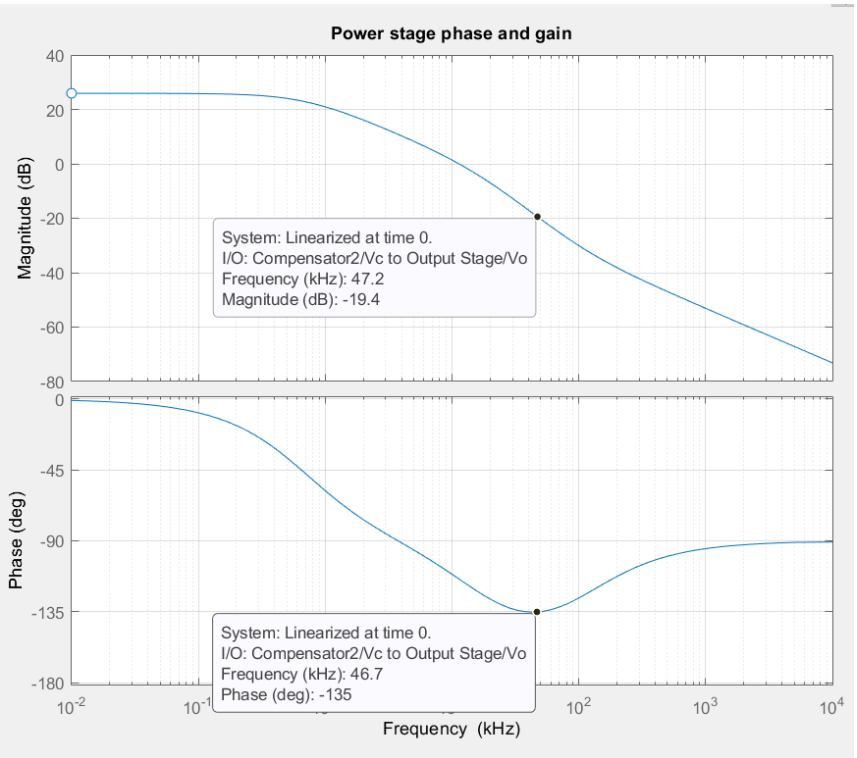


Figure 5-14: Transient output voltage response with C1 changed to 15nF, the percent overshoot is significantly lowered.



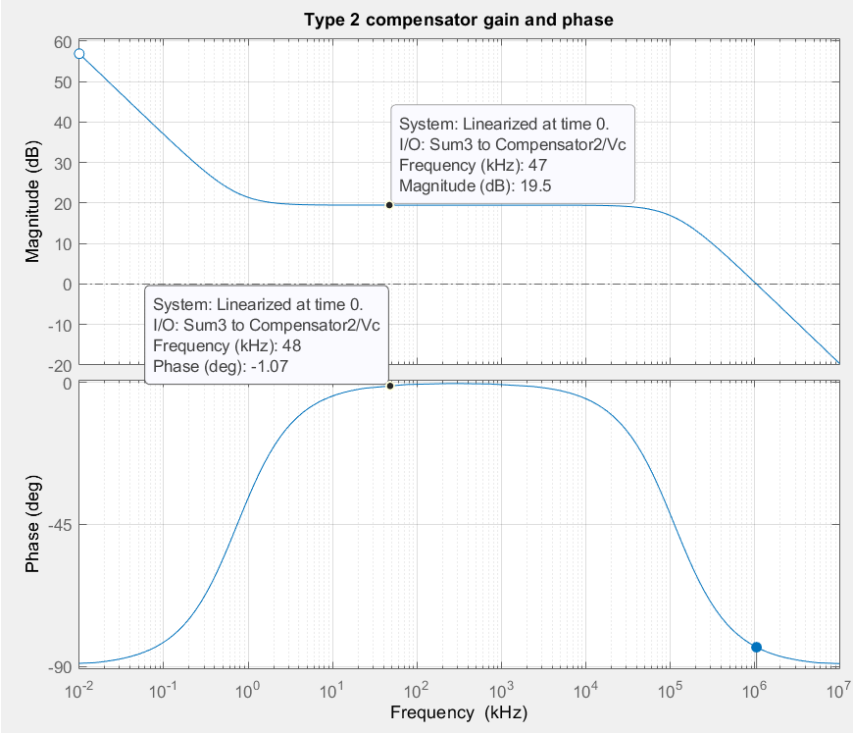


Figure 5-15: Power stage and type two compensator gain and phase.

The new compensator design boosts the targeted gain and phase for the power stage. In this case, the same crossover frequency of 47kHz is picked at nominal input voltage. Figure 5.16 shows the overall loop response which is the summation of the power stage and compensator stage shown in Figure 5.15. Note that the slope at the crossover frequency is within expected value of -25dB/decade.

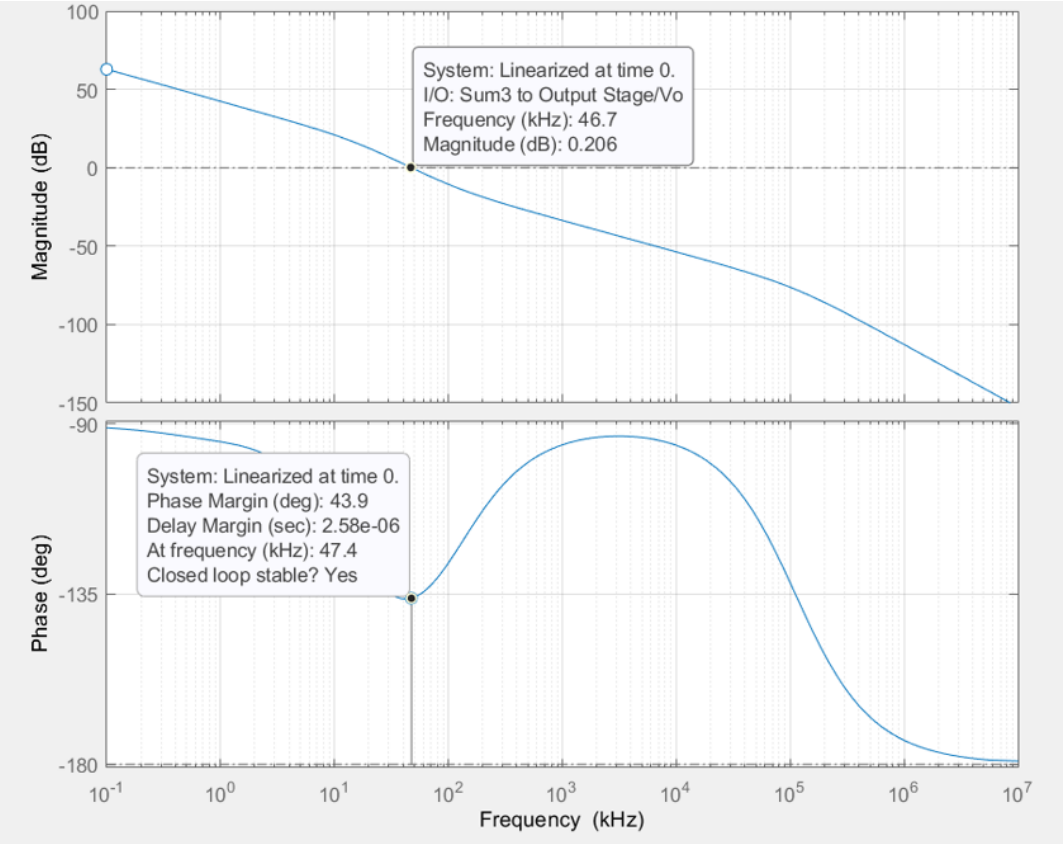


Figure 5-16: Overall loop gain and phase with test signals in the compensator input.

Table 5.2 summarizes the frequency and time measurements for MISO model with new compensator using a series capacitor of 15nF. This compensator enhanced the phase margin and lowered the overshoot. This can be seen when comparing Table 5.1

results with Table 5.2 where the percent overshoot is lowered significantly to achieve the less than 10% goal.

Table 5-2: Simulation summary for Simulink MISO model with 15 nF compensator capacitor and 12.6 mΩ ESR

Step conditions	% Overshoot	Rise time(us)	Settling time (ms)	Phase margin (degree)	Gain Margin (dB)
24V Vin	0.505	109	0.6	43.9	Inf
90% to 10% load at Vin = 24V	3.6	100	0.43	43.8	Inf
10% to 90% load at Vin = 24V	0.5	109	1.6	43.9	Inf
Vin step up from 10V to 60V	6.98	97	1.7	65.2	Inf
Vin step down from 60V to 10V	1.971*	299	1.5	28.7	Inf

*Undershoot

5.8 Analysis

Based on results in Tables 5.1, it is argued that the initial MISO design is stable with a phase margin around 40°. The gain margin of infinity ensures that the system will be stable no matter how much the gain increases. While the target goal for a typical DC-DC converter phase margin is above 45°, a phase margin of 40° is still stable and only affects the transient overshoot.

Some potential concerns with the initial MISO component values are higher overshoot and lower phase margin. While the initial values provide a faster response,

changing the capacitor value provides better stability metrics. The compensator series capacitor can be raised to increase the phase margin and lower the overshoot as shown in Table 5.2. The percent overshoot is lowered by 192% using the new capacitor value and phase margin is improved by 8% at nominal input voltage as shown in Table 5.3. However, this changes the rise time and increases the settling time for step changes in input. An ideal rise time for load transient is less than inverse of the loop bandwidth frequency [19] which equals

$$f_{BW} = \frac{G_{sense}R_4}{2\pi(R_5 + R_{13})C_o} = \frac{100 * 14.3k}{2\pi * 1010k * 120.8u} = 1.86kHz$$

$$1/f_{BW} = 0.54\text{ms}$$

As long as the transient rise time is much less than 0.54 milliseconds, the system will be fast enough to excite the loop for the compensator to work over a wide frequency range. This further shows that the increased rise time from the suggested compensator will not harm the overall load transient performance of the system. Another thing to note is that the crossover frequency increases with the increase in input voltage but remains below the threshold of half the switching frequency for the voltage range that MISO uses. Decreasing the series resistance is one way to lower the crossover frequency if required (see Appendix C). The higher crossover frequency implies a faster response or faster recovery for a step change in the load as shown in Table 5.1 and 5.2 where the rise time is lowered when the input steps from 10V to 60V.

Table 5-3: Percent difference calculation for time and frequency analysis metrics between initial compensator and proposed compensator values

Step conditions	%Overshoot	Rise time	Phase margin
24V Vin	192	67	7.8
90% to 10% load at Vin = 24V	154	61	7.5
10% to 90% load at Vin = 24V	193	69	8
Vin step up from 10V to 60V	123	57	3.1
Vin step down from 60V to 10V	171	135	19

5.9 Current Share Simulation and Analysis

The Simulink model combines the current sharing network to observe the stability metrics. Since the current sharing method uses active current sharing, the main module acts as the master and the slave module acts as a step voltage that corresponds to the follower module's output voltage. In this setting, the master always has the higher output voltage, while the follower modules increase their output voltage to take more current to lower the load burden from the master. This simulation observes the closed-loop response when the current share circuit was implemented as depicted in Figure 5.9. As expected, since the voltage added or taken from the feedback node is in the millivolts range, it does not affect the stability of the overall circuit as shown in Figure 5.17. The phase margin is still around 45° and the gain margin is infinite.

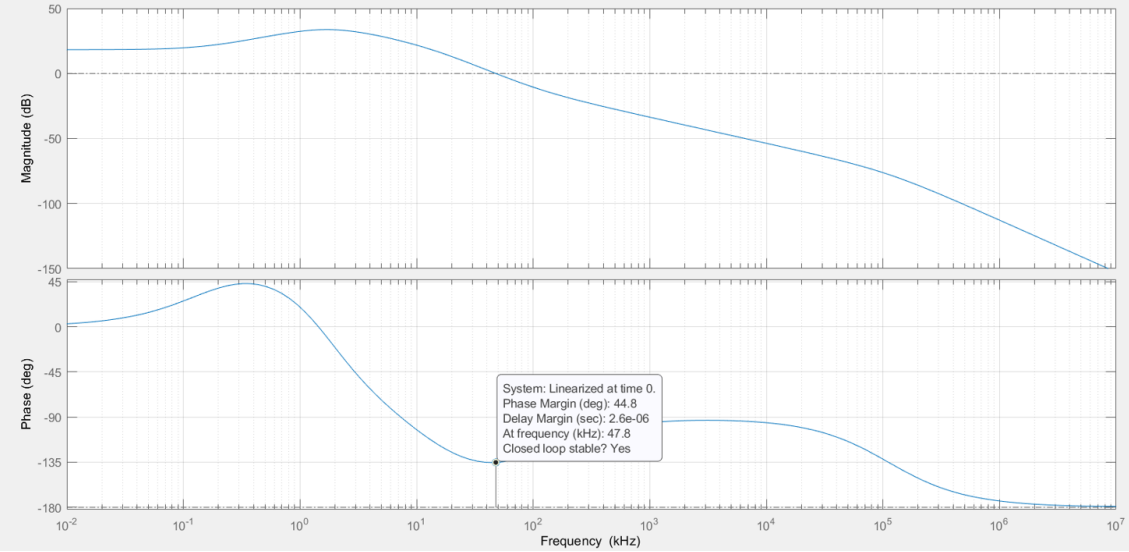


Figure 5-17: Closed-loop gain and phase with current share circuit implemented on main module.

While this is a basic test to look at the loop stability, improvements can be made in future model design. Incorporate the diode that allows automatic selection of the master and slave modules is one improvement for future work. In addition, a parallel module can be made in Simulink to show a better model of the overall current sharing between multiple modules.

6. Conclusion

This thesis developed the control system model of the Cal Poly's multiple input single output (MISO) converter in MATLAB Simulink in frequency domain. Transfer functions were developed for each system block such as power stage, compensation, current sharing, and output stage. The transfer functions were derived and modeled to best fit the converter design used in the original MISO circuit. The goal of the thesis was to gather the transient and frequency response metrics to analyze the stability for the main MISO circuit in conjunction with testing the current sharing network. The current sharing network is what allows multiple MISO modules to be placed in parallel to account for higher load condition. The results from the simulation testing showed that the original MISO circuit was stable with a phase margin of around 40°.

Since some blocks for the converter chip LT8390 were a black box, assumptions were made to make the Simulink model. The first assumption was that the inductor current was directly fed to the slope compensation network without sample and hold. This was done since Simulink does not allow transfer functions with numerators of higher order than denominator. The lack of sample and hold has a direct effect on phase margin. However, after some research it was found to be not significant enough to bring the whole system to instability. Another major assumption was made when picking the ESR for the output capacitors. The highest ESR was chosen to get the worst-case scenario. The compensation network was also designed to best fit the nominal input voltage. These assumptions, along with others mentioned in Chapter 4 could be the reason behind the lower phase margin and consecutive high overshoot observed when using the initial compensator design. An alternative compensator design was provided at

the end of Chapter 5 to overcome those challenges. In addition, the current share network was only tested using a single module with an additional input behaving as a parallel module.

The next step as a follow up for this thesis is to accurately model multiple parallel modules with current share network and check the simulation to assure that it remains stable throughout the current sharing process. Another major step is to use a frequency response analyzer to check the physical frequency response to analyze the stability of the MISO circuit and compare it to simulation. This method provides the best measure for stability since all other parasitic components are taken into consideration when testing the hardware itself. This step will also provide better explanation on how accurate the simulation model was compared to the original model and give insight on how close the assumptions were to the original values. This information can then be used to improve the Simulink model for future designs.

Overall, based on the simulation results in Chapter 5, the initial MISO schematic with a type 2 compensator is stable. The designed Simulink model successfully showed that while the initial design works as expected, changing the compensator gives better transient metrics such as lowered overshoot and higher phase margin. However, as mentioned in Chapter 5, tradeoffs should be taken into considerations when making such design decisions.

BIBLIOGRAPHY

[1] “Access to Energy.” in *Our World in Data*, Sept. 20, 2019. [Online]. Available: ourworldindata.org/energy-access. Accessed: June 15, 2020.

[2] T. Taufik and M. Taufik, "The DC House Project: Promoting the use of renewable energy for rural electrification," 2012 International Conference on Power Engineering and Renewable Energy (ICPERE), Bali, 2012, pp. 1-4, doi: 10.1109/ICPERE.2012.6287254.

[3] T. Taufik, "Research Experience on the DC House Project for Rural Electrification," 2017 International Conference on Computational Science and Computational Intelligence (CSCI), Las Vegas, NV, 2017, pp. 267-270, doi: 10.1109/CSCI.2017.44.

[4] M. Denchak, “Paris Climate Agreement: Everything You Need to Know.” *NRDC*, Dec 12, 2018. [Online]. Available: www.nrdc.org/stories/paris-climate-agreement-everything-you-need-know. Accessed: June 16, 2020.

[5] Taufik, *Introduction to Power Electronics, Lulu Publishing,* September 2020, ISBN 9781716695865.

[6] T. Taufik, "The DC House project: An alternate solution for rural electrification," IEEE Global Humanitarian Technology Conference (GHTC 2014), San Jose, CA, 2014, pp. 174-179, doi: 10.1109/GHTC.2014.6970278.

[7] O. Jong, "Multiple Input Single Output (MISO) DC-DC Converter for the DC House Project," Sr. Project Report, Elect. Eng. Dept., Cal Poly Univ., San Luis Obispo, CA, 2012.

[8] A. Gallardo, "Design and Construction of 1800W Modular Multiple Input Single Output Non-Isolated DC-DC Converters," M.S. thesis, Elect. Eng. Dept., Cal Poly Univ., San Luis Obispo, CA, 2017.

[9] Taufik, *Power Supply Components and Design*, *Lulu Publishing*, September 2020, ISBN 5800138847776.

[10] M. Robert, “Switching Power Supply Topology Voltage Mode vs. Current Mode.” 1999. [Online]. Available: https://www.ti.com/lit/an/slua119/slua119.pdf?ts=1597639783556&ref_url=https%253A%252%252Fwww.google.com%252F. Accessed: July 3, 2020.

[11] D. Briggs, “Designing Fast Response Synchronous Buck Regulators using the TPS5210.” March 1999. [Online]. Available: https://www.ti.com/lit/an/slva044/slva044.pdf. Accessed: July 10, 2020.

[12] “Buck Regulator Architectures - Hysteretic Buck Regulators.” TI Training, Jan. 3, 2019. [Online]. Available: https://training.ti.com/buck-regulator-architectures-hysteretic-buck-regulators. Accessed: July 13, 2020.

[13] “Adaptive Constant ON-Time(D-CAP) Control Study in Notebook Applications.” Dec. 2007. [Online]. Available: https://www.ti.com/lit/an/slva281b/slva281b.pdf. Accessed: July 13, 2020.

[14] “Loop Response Considerations in Peak Current Model Buck Converter Design.” April 2019. [Online]. Available: https://www.ti.com/lit/an/slvae09a/slvae09a.pdf?ts=1603926693707&ref_url=https%253A%252F%252Fwww.google.com%252F. Accessed: August 15, 2020.

[15] Linear Technology, “60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum,” LT8390 datasheet, 2016.

[16] S. Lee, “Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converters.” July 2014. [Online]. Available: https://www.ti.com/lit/an/slva662/slva662.pdf. Accessed: Sept. 1, 2020.

[17] R. Sheehan, “Emulated Current Model Control for Buck Regulators using Sample and Hold Technique.” Oct. 24, 2006. [Online]. Available: https://www.ti.com/lit/an/snva537/snva537.pdf. Accessed: Oct. 3, 2020.

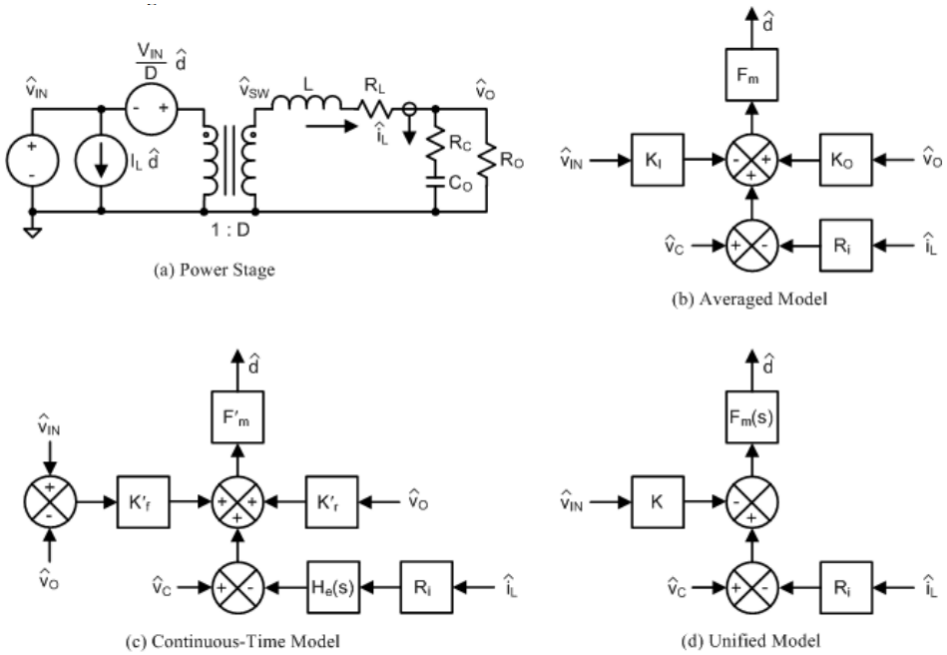
[18] “Effects of Zeros and Poles on Step Response.” 2008. [Online}. Available: https://courses.engr.illinois.edu/ece486/fa2017/documents/lecture_notes/effects_zero_pole.pdf. Accessed: Nov.27, 2020.

[19] Richtek Technology. “DC/DC Converter Testing with Fast Load Transient.” [Online]. Available:

https://www.richtek.com/Design%20Support/Technical%20Document/AN038. Accessed November 15, 2020.

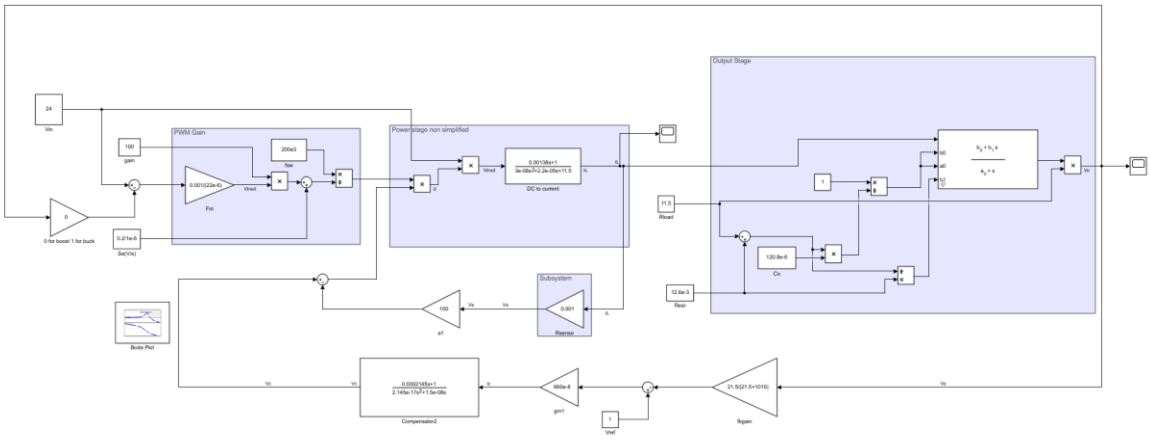
APPENDICES

A. Linear Models



Source: [17]

B. Simulink Model



C. Additional Simulation Results

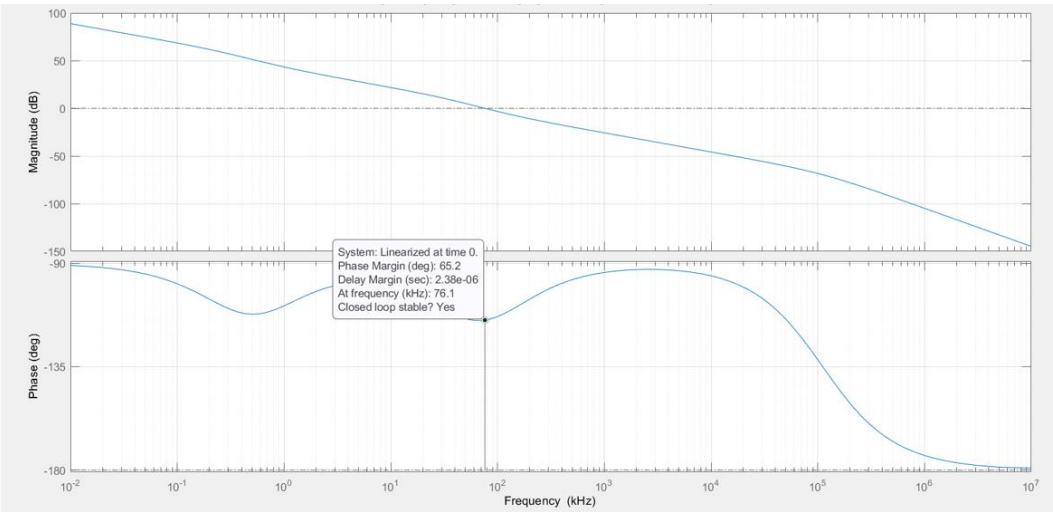


Figure C.1: Open-loop response with 60V input and increased compensation capacitor to show how cross-over frequency increases with increase in input voltage. To lower the crossover frequency, decrease type 2 compensator's series resistance value.

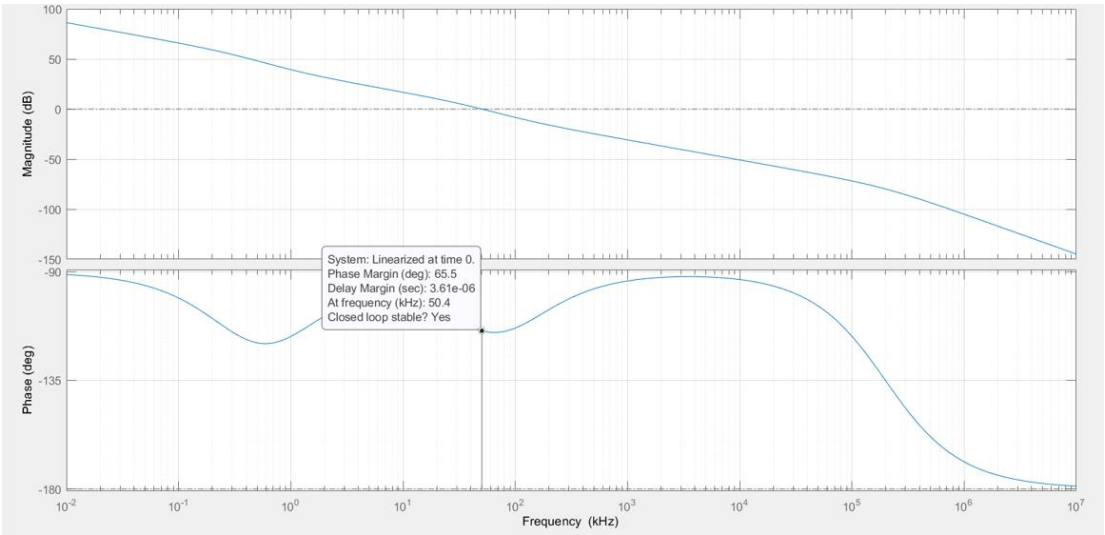


Figure C.2: Open-loop response with R compensation lowered to 10k from 14.3k to decrease the crossover frequency by 20kHz, with 60V input.