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Y. J. Huang
University of Maryland

Dimitris E. Ioannou
University of Maryland

A. Iliadis
University of Maryland

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SCANNING ELECTRON MICROSCOPY - ELECTRON BEAM INDUCED CURRENT AND DEEP LEVEL TRANSIENT SPECTROSCOPY STUDIES OF GaAs(In) LAYERS GROWN BY MOLECULAR BEAM EPITAXY

Y. J. Huang, D. E. Ioannou*, and A. Iliadis

Joint program for Advanced Electronic Materials,
Electrical Engineering Department, University of Maryland, College park, MD 20742
and Laboratory for Physical Sciences, College Park, Maryland 20742

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Abstract

Electrically active defects in indium-doped (0.6%) GaAs layers grown by Molecular Beam Epitaxy (MBE) on Si-doped ($\approx 1x10^{18}$ cm^{-3}) GaAs substrates have been studied by the combination of two techniques: Scanning Electron Microscope - Electron Beam Induced Current (SEM-EBIC) technique, and Deep Level Transient Spectroscopy (DLTS). The epilayers studied were three microns thick. No electrically active defects were revealed by the EBIC micrographs in the top one micron of the epilayers, whereas a large number of non-propagating misfit dislocations were observed at the epilayer/substrate interface. DLTS measurements made in the dislocation free top region of the epilayer showed the presence of three well known traps, which had previously been observed to also exist near the interface. It is concluded that these traps are not related to misfit dislocations.

Key Words: Electron Beam Induced Current, Deep Level Transient Spectroscopy, Molecular Beam Epitaxy, misfit dislocations.

*Address for correspondence:
Dimitris Ioannou,
Department of Electrical Engineering
University of Maryland
College Park, MD 20742
Phone No. : (301)-454-3214

Introduction

Isoelectronic doping has been used in the past to reduce the content of dislocations in GaAs layers grown by liquid phase epitaxy (LPE) [10,14,15] and metalorganic chemical vapor deposition (MOCVD) [1,2,3]. This reduction in dislocation density has been correlated to improvements in the electronic and optoelectronic quality of the layers, and the devices fabricated on them. The above improvements are observed, regardless of whether the dopant atomic radius is smaller, or larger than that of the substitutional atom.

The effects of isoelectronic doping on GaAs layers grown by molecular beam epitaxy (MBE) have only recently attracted substantial interest, and they have not yet been fully investigated [4,11,12,13]. Shinohara et al [11] applied SEM-EBIC to investigate the formation of misfit dislocations on MBE GaAs layers grown on In-doped LEC (i.e., Liquid Encapsulated Czochralski) GaAs substrates. For In doping level in the range 10^{19} - 10^{20} cm^{-3}, a large number of misfit dislocations were generated at the interface, for layer thickness larger than ≈ 1 μm. These dislocations were parallel to the interface, but some of them changed direction and propagated into the epilayer [12]. Takeuchi et al [13] studied In-doped MBE GaAs layers on In-doped GaAs substrates, where by using correct amounts of In they obtained epilayers completely free from misfit dislocations at the interface, and also from dislocations propagating into the epilayer from the substrate. Bhattacharya et al [4] have reported on the electronic quality of In-doped MBE GaAs layers on Si-doped dislocation free GaAs substrates. Their Deep Level Transient Spectroscopy (DLTS) results revealed the presence of several electron traps near the interface, the concentration of which decreased with increasing In content. They have not investigated the presence of misfit dislocations at the interface, but, based on photoluminescence spectra, they suggest that the traps are due to the native defects or complexes involving native defects.

In this paper, we also study the electronic properties of In-doped MBE GaAs layers on Si-doped GaAs

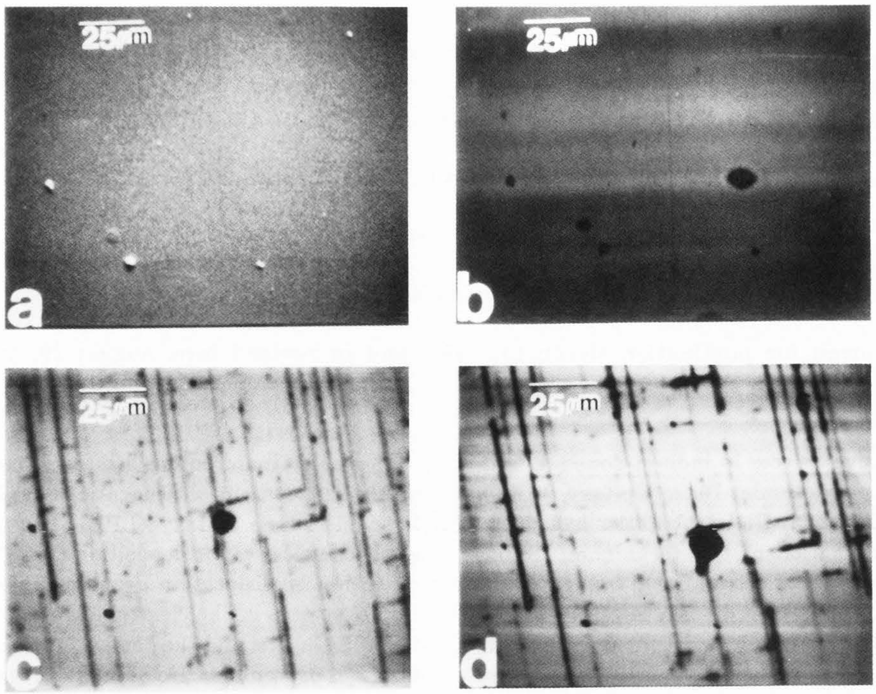

Fig. 1. SEM micrographs of the same sample area, showing the misfit dislocations present at the epilayer/substrate interface. (a) Emissive Mode (EM) micrograph obtained at beam energy 20 keV. (b), (c), and (d) EBIC micrographs obtained at beam energies 10, 20, and 30 keV, respectively.

substrates, by the combined application of SEM-EBIC [9] and DLTS [7]. Our results provide further evidence in support of the suggestion made by Bhattacharya et al [4].

Experimental

3 μm thick n-type GaAs layers with small amounts of In doping ($\approx$ 0.6%) were grown by MBE on Si-doped n^+ (100) GaAs substrates (n $\approx 10^{18}$ cm^{-3}) under As-stabilized conditions (As_4/Ga=16) with a substrate temperature 600 °C at a rate of $\approx$ 1 μm/hr. Al-Schottky barrier diodes for SEM-EBIC and DLTS examination were fabricated as follows: The sample was first thoroughly cleaned consecutively with trichlorethylene, acetone, and methanol using an ultrasonic bath. Following this, the sample was etched in diluted HF for 1 minute and washed in flowing deionized water, and finally stored in methanol until it was taken into the evaporation chamber. The evaporation was carried out resistively with a tungsten wire in a liquid-nitrogen-baffled oil-pumped vacuum system, the pressure being $\approx 10^{-6}$ Torr. The typical metal film thickness was $\approx$ 200 nm. After metal evaporation, conventional photolithography was used to define an array of Al dots of diameter $\approx$ 1 mm, by etching off annular rings of 40 microns width.

These Schottky diodes showed excellent I-V and C-V characteristics. The carrier concentration in the epilayer, deduced from the C-V measurements, was found to be pretty uniform up to a depth of $\approx$ 1 μm, its value being $\approx 5\text{x}10^{15}$ cm^{-3}. However, this carrier concentration increased for larger depth, presumably due to Si outdiffusion from the substrates.

The EBIC micrographs were obtained with an International Scientific Instruments ISI # 60 Scanning Electron Microscope (SEM) under three different accelerating voltage settings: 10, 20 and 30 keV. The DLTS measurements were performed with a BIO-RAD/POLARON # 4600 system, which uses a double box-car signal processor, and is capable of detecting traps with concentrations down to 10^{-4} N_d, where N_d is the background doping concentration.

Results and Discussion

EBIC micrographs of the same area of a typical sample, obtained at beam energies 10 keV, 20 keV, and 30 keV are shown in Figs. 1(b), 1(c), and 1(d), respectively. For comparison, the EM (Emissive Mode) micrograph of the same region is shown in Fig. 1(a). The range of electron penetration into the material is 0.79 μm for 10keV, 2.5 μm for 20keV and 4.9 μm for 30keV

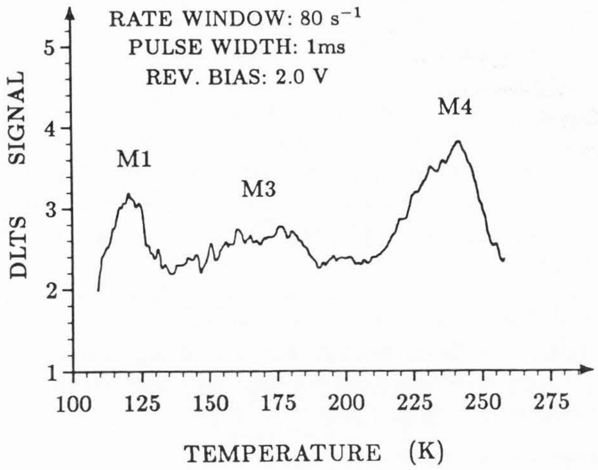

Fig. 2. A typical DLTS spectrum of electron traps obtained using the same diode as in Fig. 1.

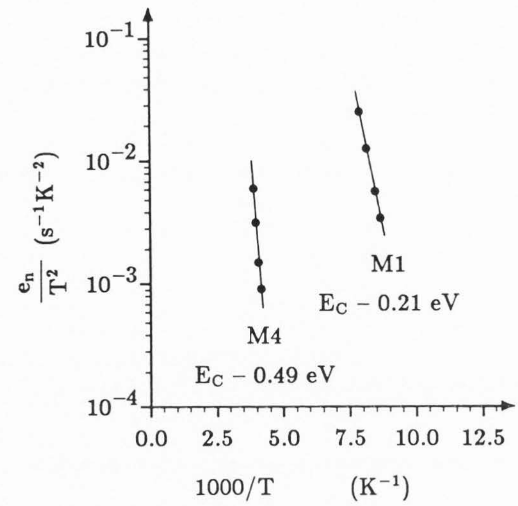

Fig. 3. Arrhenius plots for the peaks labeled M1, M4 in Fig. 2.

[6], whereas the depletion layer width of the Schottky diode is $\approx 0.4\ \mu m$ at present doping level. An examination of the above micrographs reveals the presence of a large number of misfit dislocations (Figs. 1(c) and 1(d)) close to the epi-layer/substrate interface, and an almost dislocation-free zone at the top one micron of the epilayer (Fig. 1(b)). Most of these dislocations appear to be parallel to the interface (cf. dark lines in the micrographs), although some of them appear to change direction and propagate into the epilayer (cf. black circular dots in the micrographs). The presence of these dislocations is in agreement with the results of previous investigators [11,12], where it was found that misfit dislocation formation occurs for layers thicker than about 1 micron.

A typical deep level spectrum for the same sample is shown in Fig. 2, where three well known traps, M1, M3, and M4 are found [8]. The Arrhenius plots of traps M1 and M4 are shown in Fig. 3, from which the trap energy levels are found to be 0.21 and 0.49 eV below the conduction band edge, and capture cross sections of 3.4×10^{-14} cm^2 and 1.8×10^{-13} cm^2, respectively. The Arrhenius plot of trap M3 could not be obtained, due to its complicated DLTS spectra. The above energy levels and capture cross sections are in agreement with the results of Lang et al [8] and Blood and Harris [5]. The trap concentrations were $\approx 2.5 \times 10^{13}$ cm^{-3}, again in good agreement with previous work [4,5].

Our results can in particular be compared to those by Bhattacharya et al [4], who studied very similar material. In their DLTS measurements they have studied the traps very close to the interface. They reported several traps, among which were traps M1, M3, and M4. It is argued in their paper that these traps are probably native defects or complexes involving native defects. They believe these defects to be Ga vacancies, based on the expected growth kinetics. We should note that by way of measurement their observations were made near the interface, and thus the observed traps were physically located in the same area as the misfit dislocations. By contrast, we observed these same traps near the top of the epilayers, physically away from the misfit dislocations. These observations appear to suggest that indeed the traps must not be directly related to the dislocations, and lend support to the hypothesis made by the previous authors [4], i.e., that the traps are due to defects related to Ga vacancies. The additional traps (M2, M6, M7) seen by the above authors are most probably due to the interface itself.

Conclusions

In conclusion, we have observed a substantial decrease in the density of deep traps (M1, M3, and M4) present in doped GaAs substrates, and produced evidence that these traps are probably not directly related to the misfit dislocations present at the interface.

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Discussion with Reviewers

D.Köhler: Can you give any information about the circular defects shown in the EBIC micrograph in Fig. 1?
Authors: The dark lines in the EBIC micrographs of Fig. 1 are images of misfit dislocations running parallel to the interface, whereas the dark circles may be images of epilayer misfit dislocations which changed directions and propagated into the epilayer, or substrate dislocations that propagated into the epilayer (text reference [12]).

M. Shinohara: When discussing the depth profile of defect density by using SEM-EBIC and DLTS, the depletion layer width must be taken into consideration. However the carrier concentration of the In-doped epilayer is not indicated. This value is essential to estimate the extension of the depletion region at -2V, and to assess your claim that the electron traps M1, M3, M4 observed in the DLTS measurement exist in the dislocation-free zone.
Authors: The carrier concentration in the In-doped epilayer deduced from C-V measurements is fairly uniform down to a depth of $\approx 1\mu m$, its value being $\approx 5x10^{15}$ cm^{-3}. At this doping level, the depletion layer width of the Schottky diode at -2V is $\approx 0.8\ \mu m$.

P.K. Bhattacharya: This reviewer is led to understand that the dislocations have nothing to do with In-doping. Is this true? This point should be clarified.
Authors: The misfit dislocations observed in Fig. 1 are a direct consequence of the lattice mismatch between the epilayer and the substrate, which is produced by the incorporation of Indium in the epilayer.