Scanning Microscopy

Volume 2 | Number 1 Article 10

10-25-1987

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Tompkins, Harland G. (1987) "Surface and Thin Film Analysis of Microelectronics Materials," *Scanning Microscopy*: Vol. 2 : No. 1 , Article 10.
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Scanning Microscopy, Vol. 2, No. 1, 1988 (Pages 107-112) 0891-7035/88$3.00+.00
Scanning Microscopy International, Chicago (AMF O'Hare), IL 60666 USA

SURFACE AND THIN FILM ANALYSIS OF MICROELECTRONICS MATERIALS

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(Received for publication March 22, 1987, and in revised form October 25, 1987)

Abstract

The use of probing techniques in the analysis of microelectronics materials is discussed in general and several examples are presented to illustrate the use of these techniques. The emphasis of this paper is for using electrons as the probing particles and both electrons and x-rays as the analyzed particles to deal with analysis of microelectronics materials. The first example involves the interaction of titanium and silicon dioxide. It is shown that when titanium is sputter deposited onto silicon dioxide, the titanium reduces a small amount of the oxide to elemental silicon at the interface. The second example shows how a thin oxide is converted to an oxynitride when silicon nitride is deposited on top of it. The last two examples involve failure analysis of microelectronics devices. We show that a simple ratio technique can be used to quickly estimate the thickness of a carbonaceous layer on aluminum bond pads.

KEY WORDS: Auger electron spectroscopy, x-ray energy spectroscopy, thin film analysis, bond pads microelectronics, titanium, silicon dioxide silicon nitride, carbonaceous, particle probe techniques

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Introduction

Microelectronics involves many aspects which include wafer fabrication and packaging. The packaging part involves problems in the classical areas of metal bonding, electroplating, electrical contact resistance when a lead is inserted into a socket, etc, and often the classical methods of materials analysis are appropriate. The wafer fabrication, on the other hand, involves analysis problems which are becoming increasingly complex because of **size**. The features on a microelectronic circuit on a silicon wafer vary in depth from a maximum of a micrometer or two down to a few tens of angstroms. The lateral dimensions of some features are being reduced to fractions of a micrometer. This places increasing demands on the ability of the analyst to determine topographical information, atomic concentrations, and chemical environment. We shall discuss the applicability of some of the analysis techniques and then give several examples of their use.

Perspective

Probes & Filters

We analyze microelectronics materials in a variety of ways. This includes simple observation by optical microscopy and SEM, electrical measurement and a variety of probing methods. This paper will deal with methods where a probe (e.g.,an electron beam) is directed at the sample and the resulting particles which come off of the sample are analyzed. Figure 1 illustrates some of the probing particles as well as the analyzed particles. Table 1 illustrates some of the techniques used routinely in the microelectronics industry in product development and manufacturing. This list is not intended to be all inclusive, but to illustrate some of the common techniques. If basic research were included, the list would be considerably longer.

Normally there is some filter for the ejected particles. We regard electrons with energies less than 50 eV as secondary electrons and electrons with energies near the incident energy as backscattered electrons. Auger electron spectroscopy and X-ray photoelectron spectroscopy filter the energy to a much greater extent (a few eV or a few tenths of an eV) and the quantity recorded is a spectrum of the number of electrons as a function of energy.

Flying Spots

Charged particles can be focused and rastered, so in the first three categories listed in Table 1 the "flying spot" is used to provide information as a function of position on the sample. Some of the techniques are inherently surface techniques (e.g., AES and XPS) and can be made to

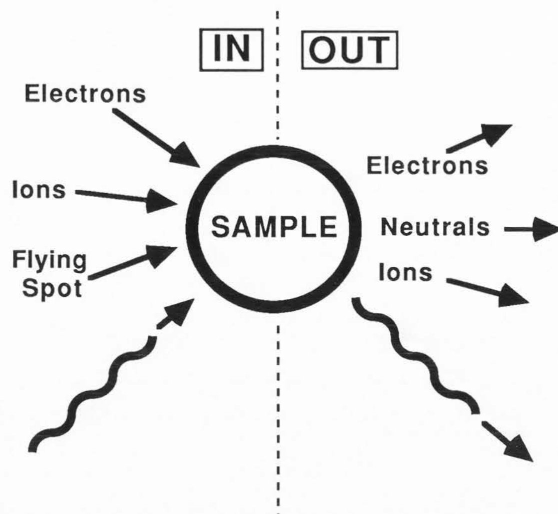


Figure 1. Probing particles and analyzed particles routinely used in materials analysis in the microelectronics industry.

analyze thin films (e.g., by sputter etching) and some are inherently thin film techniques (eg Ellipsometry and RBS). All of the techniques have some applicability in the film thickness range of zero to several thousand angstroms.

The flying spot techniques allow analysis with lateral resolution ranging from a few hundred angstroms to a few microns. The emphasis of this work will be on AES and EDS.

Thin Film XES

In many metallurgical applications, x-ray energy spectroscopy analyses are made using electron energies of 15 keV or greater. Lateral resolution of secondary electron images is better and many of the x-ray energy peaks of interest (eg iron, nickel, copper) are located in the 5 to 10 keV region. With energies above 15 keV, the electron penetration depth in most materials is several micrometers, and XES (EDS or WDS) might be considered a bulk technique.

In microelectronics, the depth of penetration is a key consideration. Few features of interest are greater in thickness than a couple of micrometers. In order to avoid penetration into the next lower layer, it is often convenient to operate at an electron energy of 5 keV or lower. Although elements such as iron, nickel, and copper are not accessible, elements such as silicon, aluminum, and phosphorus are readily measurable and if one has a windowless detector, peaks for oxygen and nitrogen can also be measured. Fortunately, these elements are the primary elements of interest in the silicon based semiconductor business. In this case, then, EDS becomes a thin film technique.

Examples

The Titanium/Silicon Dioxide Interface

In this example, we illustrate an interface phenomena which occurs when titanium is sputter-deposited onto silicon dioxide. About 25 nm of thermal oxide was grown on silicon <100> wafers and about 50 nm of titanium was then deposited by sputter deposition. Prior to the sputter deposition, about 15 nm of the oxide was removed by ion etching. Analysis of this interface was made with Auger electron spectroscopy along with argon ion etching. The ion gun was rastered in such a way that the sputtering rate for silicon dioxide was in the range of 4 to 6 nm per minute.

Table 1
Particle Probe Techniques routinely used in Microelectronics

Electrons in, Electrons out
Scanning Electron Microscopy (SEM)
Auger Electron Spectroscopy (AES)

Electrons in, Photons out
X-ray Energy Spectroscopy
(XES, EDS or WDS)

Ions in, Ions out
Rutherford Backscattering Spectroscopy (RBS)
Secondary Ion Mass Spectrometry (SIMS)

Photons in, Electrons out
X-ray Photoelectron Spectroscopy
(XPS or ESCA)

Photons in, Photons out
X-ray Diffraction/Fluorescence
(XRD/XRF)
Fourier Transform Infrared Spectroscopy
(FTIR)
Ellipsometry

Figure 2 shows spectra taken at equal sputter-time intervals as the etching proceeded from the titanium layer into the oxide and then into the wafer.

Spectrum A shows the titanium. As the oxide is approached, the oxygen and silicon signal begin to appear, as shown in spectrum B. Spectrum C shows that the first silicon to appear is actually elemental silicon rather than oxide silicon. In spectrum D, the oxide silicon is beginning to appear and the oxygen peak is in the process of shifting from titanium oxide to silicon oxide. Spectrum D and F represent mainly silicon dioxide. As the sputtering process proceeds through the oxide, the elemental silicon in the wafer appears, as shown in Spectrum G, H, and I.

This illustrates the fact that when the titanium is deposited onto the silicon dioxide, some of the oxide is reduced and some of the titanium is oxidized. Taubenblatt[2] discusses this phenomena. In addition, Yachi[5] shows spectra which illustrate this same point, but he does not mention in his discussion that the silicon peak represents elemental silicon and makes no interpretation of this facet of his data.

The Interaction of LPCVD Silicon Nitride with Silicon Dioxide

The deposition of silicon nitride on top of silicon dioxide is routinely done in microelectronics using a low pressure chemical vapor deposition (LPCVD). In the case of nitride passivation on top of a reasonably thick oxide, the layers have dimensions of thousands of angstroms and the interface between the two layers can be treated as if it were sharp.

Combinations of oxides and nitrides for very thin dielectric are being used more and more in the VLSI industry for capacitor dielectrics and interpoly dielectrics[1,3,4]. When the layers themselves are only a few nanometers thick, the

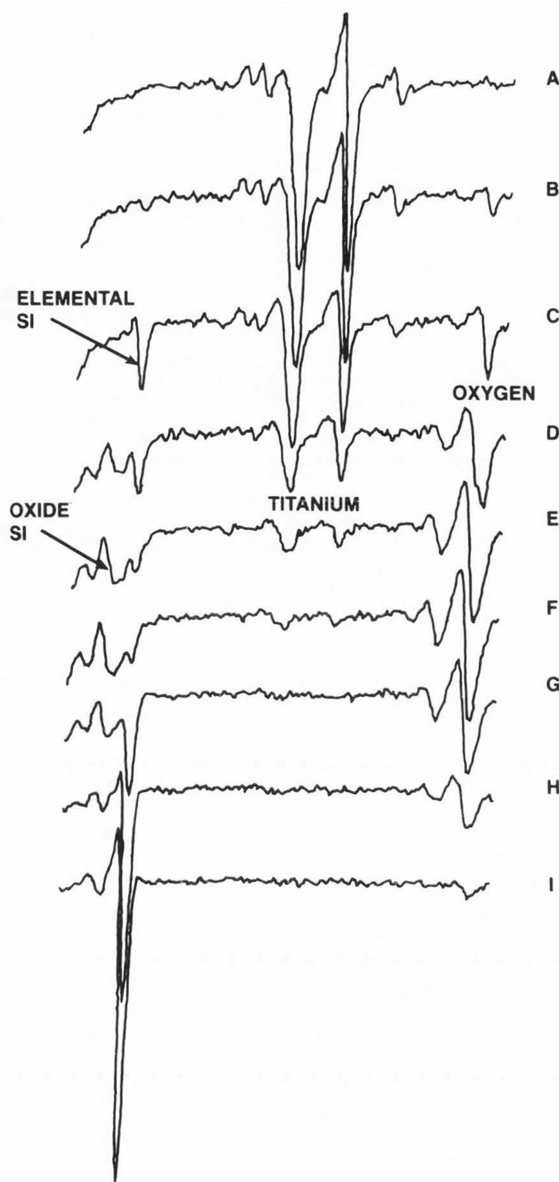


Figure 2. Spectra taken near the interface of titanium on silicon dioxide. The spectra were taken at equal sputtering time increments.

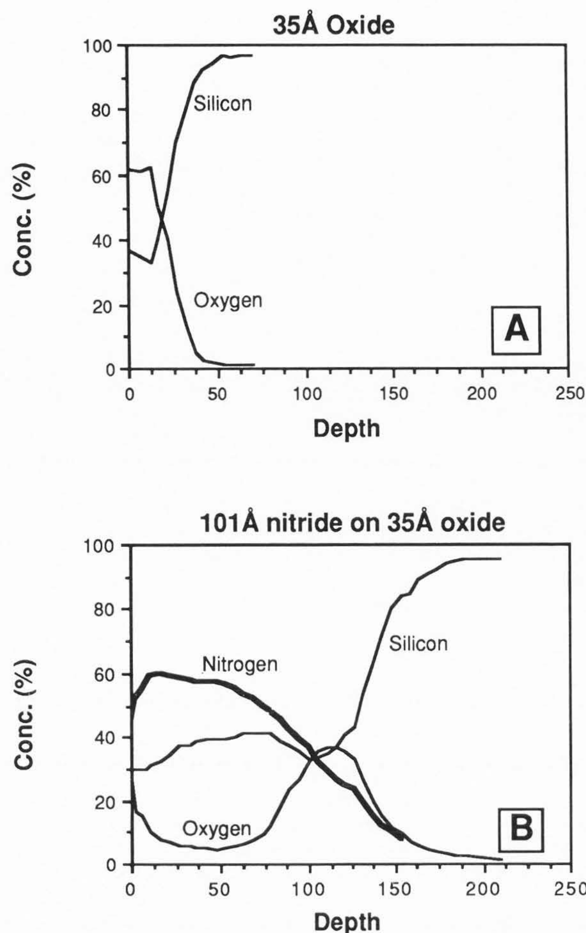


Figure 3. AES depth profiles of (A) Thermally grown silicon oxide measured with ellipsometry to be 35Å thick, and (B) oxide-nitride combination where the nitride was measured on a test wafer with ellipsometry to be 101Å thick.

transition between the oxide and the nitride is **not negligible**. In this study, the interaction between a very thin oxide and a subsequently deposited nitride is illustrated.

The processing sequence for this illustration is as follows. A very thin thermal oxide is grown on silicon <100> wafers in a dilute oxygen atmosphere. The oxide is measured with ellipsometry to have a thicknesses of 3.5 nm. Following this, an LPCVD nitride coating is deposited. The coating thickness on a test wafer processed at the same time is measured with ellipsometry to be 10.1 nm thick.

Figure 3 shows (A) the depth profile of the oxide film and (B) the profile obtained after the nitride deposition. In (B), the oxygen profile shows that the outside surface is slightly oxidized and the oxygen from the previously grown oxide can plainly be seen.

The nitrogen profile also shows that the outside surface is slightly oxidized. A rather notable observation is that the nitrogen peak decreases at about the same rate as the oxygen peak as the sputter etching proceeds through the film into the wafer.

The assumption made was that the nitride film was simply deposited on top of the oxide. Profile (B) is inconsistent with that model, however. While some mixing occurs due to the ion etching during the measuring process, the only model consistent with the oxygen and nitrogen decreasing at the same rate is that the material in contact with the wafer is an oxynitride. This implies that the original oxide has been consumed and no intact oxide exists. Other studies on thicker oxide films suggest that the amount of oxide which is consumed by the deposition of an LPCVD nitride is about 3.0 to 4.0 nm. Reference 4 argues that a native oxide with thickness less than 1.0 nm remains intact upon deposition of LPCVD nitride. This is inconsistent with our observations.

The implications of our studies are that the resulting structure from this process sequence is an intact nitride (with an oxidized surface) on top of an oxynitride on top of the wafer.

Bond Pad Failure Analysis

One of the last steps in the wafer fabrication is the covering of the IC with a passivation which is usually a form of silicon dioxide (or silicon nitride). Following this passivation, holes are cut in the passivation to expose the underlying metallization. This is usually a square area having typical dimensions of 100 micrometers on a side and this forms the bond pad for subsequent wire bonding for connection to the outside world.

One of the bonding failure modes is the incomplete removal of photoresist or photoresist-stripper from the bond pad area. AES can readily determine the presence of carbonaceous material in the bond pad region and this is the technique which should be used to identify this failure mode.

It is sometimes said of Auger spectroscopists that they find carbon on everything. Because of the extreme sensitivity of this technique and the all pervasiveness of carbonaceous contamination, there is a thread of truth in this accusation. Accordingly, the question occasionally comes up as to **how much** carbonaceous material is present. Usually a ball-park figure is all that is required. Depth profiling with ion etching is a possibility, but the presence of the glass passivation nearby sometimes causes difficulty because of charging. The following method is useful for estimating the thickness of a carbonaceous layer. The method uses X-ray Energy Spectroscopy (XES), and therefore can be used on an ordinary SEM-EDS (or WDS) even when AES is not available.

To obtain standards, silicon wafers were coated with aluminum metallization (aluminum concentration > 98%). The aluminum was about a micrometer thick. Photoresist films with different thicknesses were deposited onto these wafers. The thicknesses used were zero, 41 nm, 94 nm, and 239 nm, as determined by ellipsometry.

XES spectra were taken on all of these samples with electron energies of 3 keV, 5 keV, and 10 keV. For each individual electron energy, all of the samples were measured using **identical** electron beam parameters and a counting time of 120 seconds. The ratio of the number of counts obtained for the coated samples to the number of counts obtained for the bare aluminum sample are plotted in Figure 4.

To use the technique, one simply takes a spectrum of the bond pad in question and a spectrum of a clean bond pad **under identical conditions** and uses the ratio along with Figure 4 to obtain the thickness.

Several things might be pointed out about using this method. First, one should recognize that electron beams degrade organic or polymer films. In this case, we are measuring the residue pile left after our electron beam has done its damage on both the sample in question and the standards. It was observed that when the flying spot was stopped, the number of counts was about 10% smaller than if an area 100 micrometers on a side was analyzed. The success of this technique comes not from any first principle calculations, but from using standards which are very similar to the sample in question. The beam damage should not be significantly different from the sample to the standards.

One should recognize that the attenuation of the signal from one element by a layer of another element is not limited to carbon on aluminum. The only requirement is that the standards used to generate a curve such as shown in Figure 4 must be very similar to the sample in question. Another failure mode sometimes encountered is the failure to completely etch the glass off the metallization. Determining the thickness of a silicon dioxide layer on top of aluminum can be done in the same manner. Standards would have to be made where several thicknesses of silicon dioxide were deposited on top of the aluminum. Again, ellipsometry could be used to measure the thicknesses of the overlayers. A plot

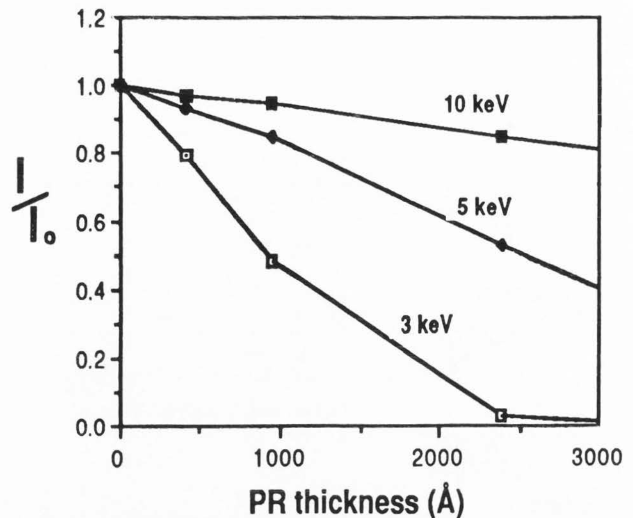


Figure 4. Ratio of intensity for a photoresist-coated aluminum surface to an uncoated aluminum surface as a function of film thickness and beam energy.

such as Figure 4 would then be made and subsequently used for determining oxide thicknesses on samples of interest.

General Failure Analysis

In some integrated circuits, more transisters and other devices are built on the chip than will actually be used. This redundancy is useful in product yield as well as allowing different uses for the same basic chip. The fabrication of this type of chip includes the following processing steps:

- fabrication and passivation deposited.
- bond pads and fuses exposed by cutting through the passivation
- electrical probing and decisions
- laser-burn appropriate fuses
- deposit passivation to cover all fuses
- open bond pads to connect to outside world
- electrical probing for quality control

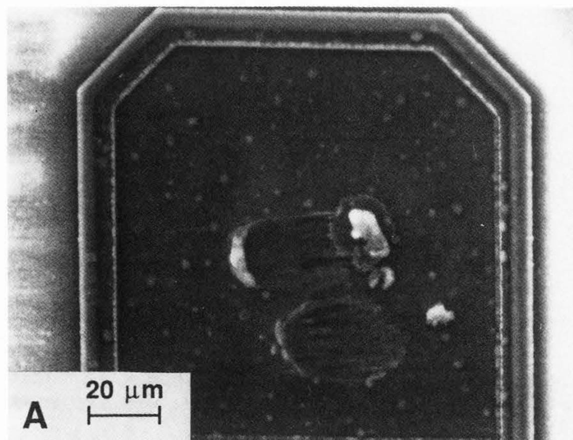
Note that electrical probing is done twice. This is done with a needle which has a tip with radius much smaller than the dimensions of the bond pads An interesting failure was observed on one product such as this and the bond pad is shown in Figure 5. Both probe marks can be seen. In addition, a particle which appears to be sitting on a "lily pad" can be observed. The particle is located at the end of the probe mark where the probe **first touches** the bond pad. The direction which the probe pushes can be determined by the presence of a "prow" where the probe stopped.

In some cases, the "lily pad" appears to overlay the probe mark, but was always under the particle. Another observation was that on occasion, the wafer had to be reprobed since the first probing appeared to miss the bond pad and strike the passivation.

Although better electron micrographs are obtained at 20 keV, it is important to do the x-ray analysis at 5 keV since the metallization is about a micron thick and the material under the metallization contains silicon. Figure 6 shows another secondary electron micrograph along with x-ray maps for silicon and aluminum. It is clear that the "lily pad" is made of silicon.

It is necessary to separate our observations from interpretations and conjectures. The above represents our observations. One interpretation of this failure is as follows:

- If during the first probing, the probe picked up particles, it would probably deposit them on subsequent bond pads.



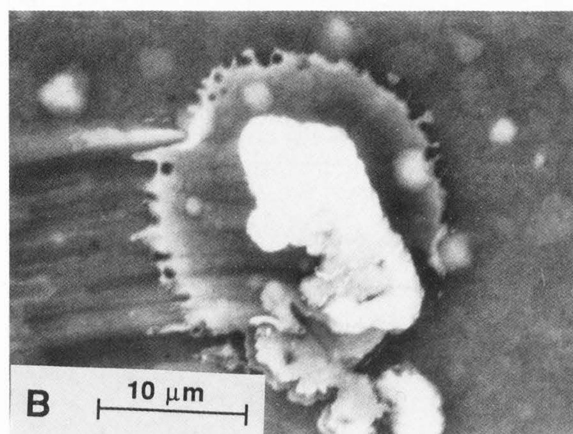
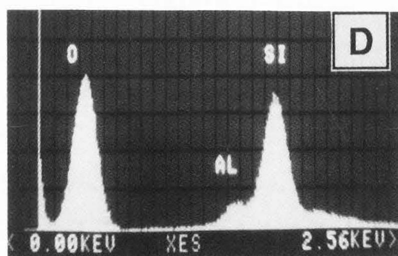
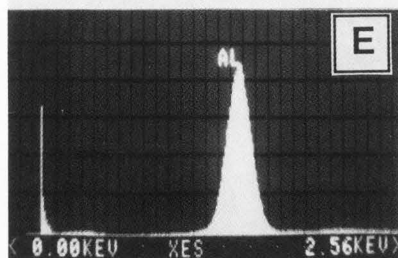
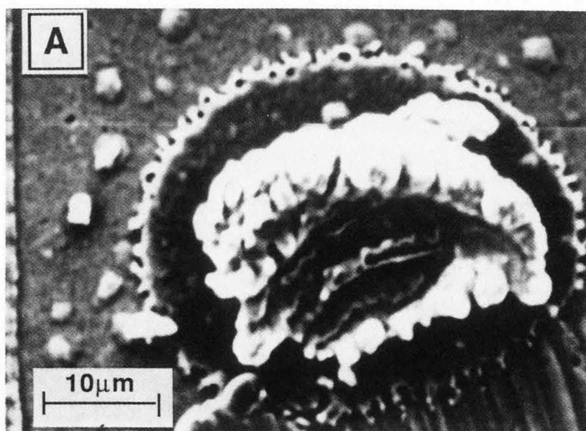
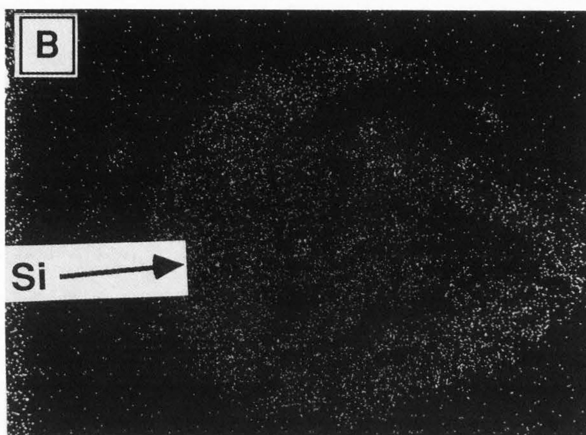


Figure 5. Secondary electron micrographs of particle on a "lily pad". (A) Low mag. (B) higher Mag. Both taken with 20 keV. Note that the "lily pad" appears to overlay one of the probe marks.









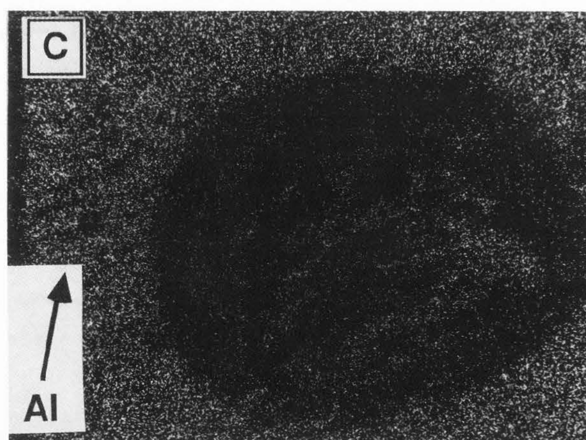


Figure 6. The particle and "lily pad". (A) Secondary electron micrograph, (B) Si x-ray map, and (C) Al x-ray maps. Also included are: (D) x-ray spectrum of the particle and (E) x-ray spectrum of the region on the bond pad away from the "lily pad".

- The deposition of passivation glass to coat the fuse openings would also coat the bond pad (and the particle). Since this is a CVD process, the bond pad would be coated under the particle in places where the particle is not actually touching the pad. Note that this would coat the first probe mark.
- During the Reactive Ion Etching (RIE) of the second passivation to cut the openings for the bond pads, the particle shown in the figure becomes charged. This repels the ions used for the etch and the "lily pad" under the particle is left unetched.

An alternate interpretation which does not involve repelling the ions is as follows:

- After the CVD passivation to coat the fuse opening, a photoresist is deposited, patterned, exposed, and developed, to allow the bond pads to be opened with an RIE. During the light-exposure to develop the photoresist, photoresist which was under an edge of the particle would be shaded and hence would not be subsequently removed. This would inhibit the removal of the passivation on the bond pad under the edges of the particle.

In any event, the solution to the problem was to avoid having the particles present. This involved paying more attention to the probing operation, to see that the probe lands on the bond pad rather than the passivation.

Summary

We have discussed methods of analyzing very small areas and very small depths by using electrons as a probing particle and electrons and x-rays as the analyzing particles. Several examples in the area of microelectronics are given as illustration.

Acknowledgements

The author would like to acknowledge Chang-Ou Lee, Bich-Yen Nguyen, M. Kottke, P. Tobin, and S. Thomas for useful discussions and sample preparation and P. Slovacek for SEM photography. Samples were also prepared or provided by R. Wright and P. Gupta, and their contribution is also gratefully acknowledged.

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