

# A HIGH-TECH RETRO SPECTRUM ANALYZER INCORPORATING WORLD WAR II DISPLAY TUBE

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By

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December 2020

## Abstract

With the discoveries and inventions of modern display and digital processing technologies, the contemporary paradigm of displaying and demonstrating information has shifted from those from just a few decades ago. Cold cathode display is one of the most widely used and superior display technologies from 50 years ago, which is also being called 'nixie tube'; however, with the semiconductor-based display development and cathode-ray tube-based monitor during the late 1900s, cold cathode displays rapidly disappeared from the market and ever since then, manufactures all over the world never paid attention back to the cold cathode display. In this thesis, the cold cathode display technology will be reexamined by exploring the ideas and works made possible by combining the cold cathode display with modern digital circuits and digital signal processing technology. This thesis will be concluded by designing a unique piece of visual art --- An audio spectrum visualizer based on IN-13 cold cathode display tubes from World War II manufactured in the USSR as a demonstration and investigation of modern utilization of cold cathode display technology.

Subject Keywords: Analog Circuit; Cold Cathode Display; Digital Arts; Digital Circuit; Audio DSP

## **Acknowledgments**

I want to recognize everyone who has encouraged me while writing this thesis, and I want to deliver my special thanks to Prof. Lippold Haken for his exceptional and gentle support, which lead to the final outcome of this project. I also want to thank my colleague Nickel Liang for his support and contributions to this project's firmware, industrial, and mechanical designs.

# Contents

- 1. Introduction ..... 1
- 2. Background Research..... 2
  - 2.1 History and Backgrounds of Cold Cathode Display Technology ..... 2
  - 2.2 Fundamental Mechanism of Cold Cathode Display ..... 4
  - 2.3 Contemporary Technology Derived from Cold Cathode Display ..... 7
  - 2.4 Motivation of Designing a Cold Cathode Display Based Device with Modern Digital Technology..... 7
- 3. Proof of Concept Design – Audio Spectrum Visualizer (Electrical) ..... 9
  - 3.1 Major revision on the electrical design..... 9
  - 3.2 First Revision of Electrical Design (MK1)..... 9
  - 3.3 Final Revision of Electrical Design (MK2) ..... 13
    - 3.3.1 Computing Core ..... 14
    - 3.3.2 USB-C Power Delivery ..... 15
    - 3.3.3 Battery Management and Charging System ..... 17
    - 3.3.4 Power Management ..... 20
    - 3.3.5 Digital to Analog Conversion..... 21
    - 3.3.6 Tube Drivers and High Voltage DC Supply ..... 22
  - 3.4 Final Revision of Mechanical Design (MK2) ..... 25
- 4. Firmware & System Logic..... 29
- 5. Conclusion ..... 31
- References ..... 32

## 1. Introduction

In this section, the history and the background theory of the cold cathode display technology will briefly discuss, with the discourse on the limitation of cold cathode display in its days, the forms and application of cold cathode display, and a few contemporary designs ideas and projects based on it. Also, the driving force of driving cold cathode display with a modern cutting-edge digital microprocessor, digital signal processing, and control technology, that reveals functions and possibility of the display that is impossible back to the time that it was being used which eventually leads to the invention of the cold cathode display-based audio spectrum visualizer in this thesis. Finally, there will be a brief discussion of the successor of cold cathode display in today's display and lighting system.

In Chapter II, this thesis will focus on the history and accomplishments of cold cathode display technology, its present-day successor, and the primary motivation of designing a device with the cold cathode display with improved technology. Chapter III will be mainly on electrical design, and chapter IV on the firmware design, of a project utilizing the cold cathode display tube. Chapter V will conclude the project of utilizing cold cathode display tubes as a display of audio spectrum, potential future developments, and how the cooperation of non-mainstream technology can be used in conjunction with the cutting-edge invention to open a new regime of digitally inspired art projects.

## 2. Background Research

### 2.1 History and Backgrounds of Cold Cathode Display Technology

There are two primary types of cold cathode displays, which are linear cold cathode display and discrete units cold cathode display; however, both types of cold cathode display utilizing the same operation principle of generating photons within visible light spectrum with gas discharge which is plasma with ionizing radiation by passing an electrical current through two electrodes, within a sealed glass chamber filled with certain types of gas. (Wikipedia\_contributors, 2020)

While the linear cold cathode display usually takes the shape of a long and thin tube, the glow length of the gas plasma can be controlled by controlling the current flow through the device as shown in Figure 1.

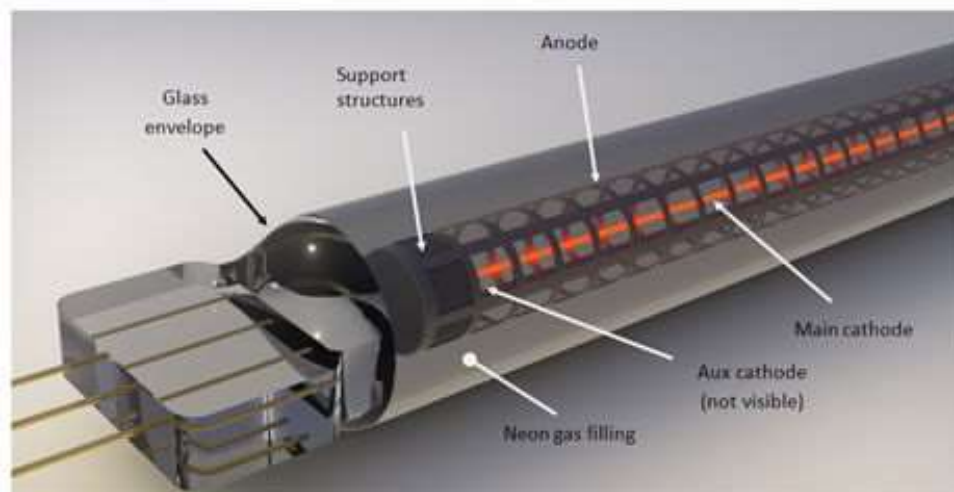


Figure 1 --- Internal construction of a typical linear CCD tube (Saltechips, 2020)

The more commonly used type of cold cathode display is the one has discrete anodes units. i.e., for each character/shape need to be displayed, there is a metal film with it shape lined up

inside a glass chamber, and each one of the shapes can be lit up by allowing an electrical current to flow through it, as demonstrated in Figure 2 and Figure 3; however, the shape of the thin metal cannot be partially lit up as one can in the linear cold cathode display by controlling the current through it, but the intensity of the light generated can be controlled via the current.

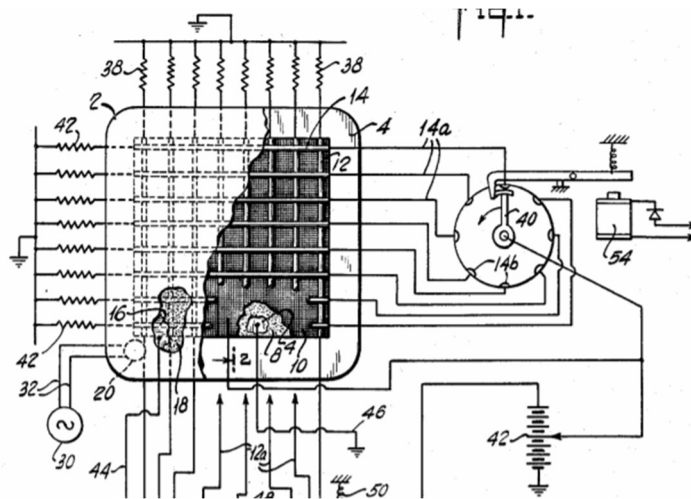


Figure 2 --- Internal construction of a typical discrete CCD tube (US Patent No. US2926286A, 1960)

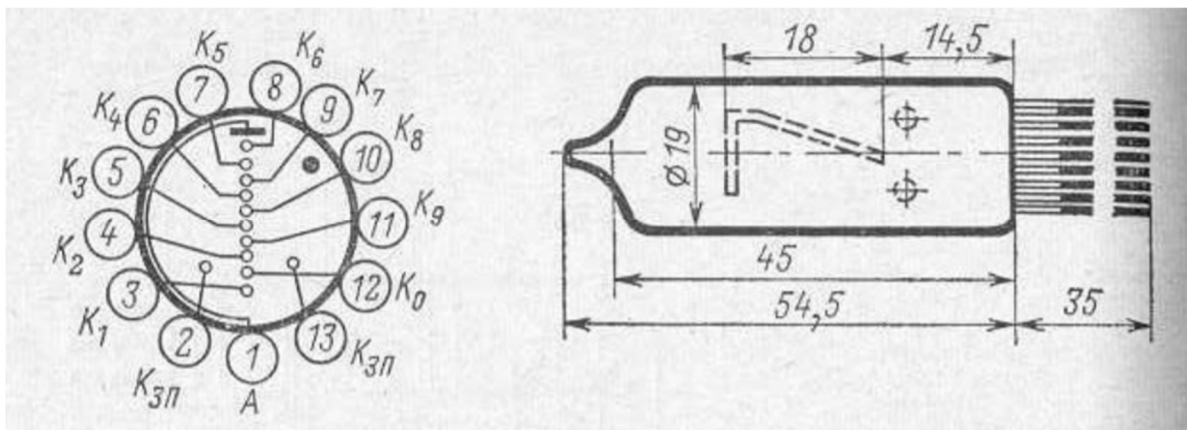


Figure 3 --- Internal construction of a typical discrete CCD tube 2 (USSR, 1950)

## 2.2 Fundamental Mechanism of Cold Cathode Display

A constant flowing charge carrier creates the plasma within the glass chamber within the chamber between two electrodes. The charge carrier can either be electrons or positively charged ions formed by the gas particles inside the chamber. The process leads to this continuous flow of the charge carrier within the chamber is called Townsend avalanche, that was discovered by John Sealy Townsend, who discovered the fundamentals of ionization mechanism in 1897. (Townsend discharge, 2019)

Townsend avalanche within the cold cathode display is achieved by applying a direct current (DC) bias between the two electrodes within the gas filled glass chamber, i.e., creating a large electric field between the anode and cathode of the display. The free electrons generated from the power supply get accelerated by the electric field between the electrodes to a critical velocity depending on the separation between the two electrodes and the gas's atomic composition within the chamber. While the electrons travel from the cathode to the anode, they create more negatively charged electrons and positively charged gas ions by a free additional electron from the gas particles; since the process can be continued by the electrons freed from the gas particles, a self-sustaining reaction can be formed with the plasma in between the two separated electrodes.

To start the operation of one of these gas discharge tubes, two conditions must be met. First of all, in order to create the chain reaction leads to the Townsend avalanche, the electrons generated from the cathode need to be accelerated to a velocity that is faster than the critical velocity; thus, a relatively high striking voltage is required to be supplied to the display



chamber, then the voltage can be lower after the reaction is partially self-sustained. The voltage required to start this reaction is then called the discharge breakdown voltage. Secondly, to initiate and sustain the reaction of Townsend avalanche, gas particles that can be relatively ionized by electrons must fill the glass chamber of the cold cathode display.

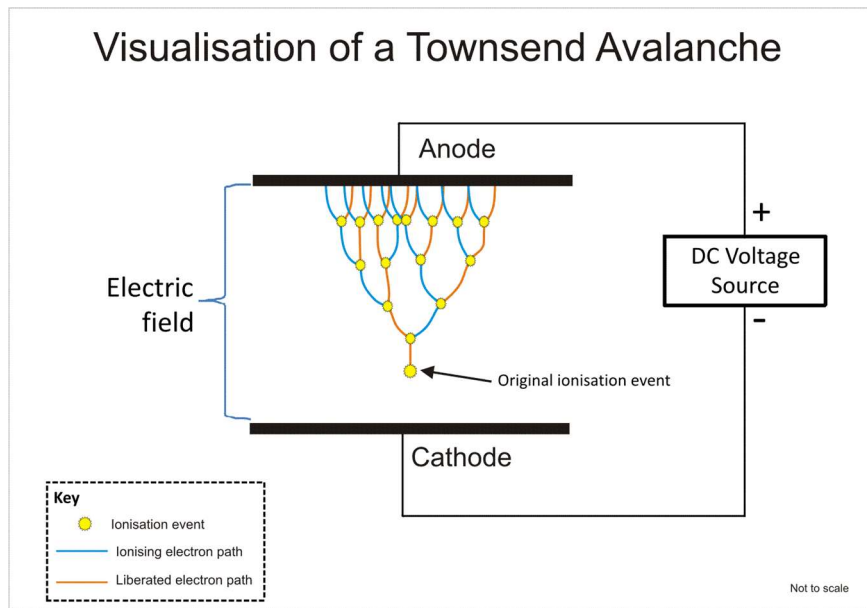


Figure 4 --- Townsend avalanche process (Wikipedia, 2019)

The electrical current flow can be used to calculate the photoelectric current generated at the cathode surface ( $I_0$ ) through the device's two electrodes ( $I$ ). The physical separation between the two electrodes ( $d$ ), and the primary and generalized Townsend ionization coefficients ( $\alpha$  and  $\frac{\alpha}{\omega}$ ) while the primary and generalized Townsend ionization coefficients are determined by the gas used inside the chamber. The physical separation of the electrodes depends on the design of the display device itself, and the electrical current flowing between the two electrodes can be controlled via the constant current source by the application circuitry described in Eq 2.1. (J. DUTTON, 1969)

$$I = \frac{C * I_c * e^{\alpha*d}}{1 - \left(\frac{\omega}{\alpha}\right) (e^{\alpha*d} - 1)}$$

Eq 2.1 --- Current Calculation for Cold Cathode Display (Linear)

Based on the desired of operating voltage and current, there are three major regions that the cold cathode display can operate in, and the application explored in this thesis falls within the "Glow Discharge" part of it. There are about three critical operating parameters of interests within the Glow Discharge operating region, as demonstrated in Figure 5: minimum voltage required to excite the gas in the chamber to start the pseudo-self-sustaining reaction **D**, critical voltage to transform the device into the Arc region, and the minimum maintaining voltage **G** to keep the device in regular glow operation. Combined with Eq 2.1, these give us the most critical operating and design parameters to use in the cold cathode display devices.

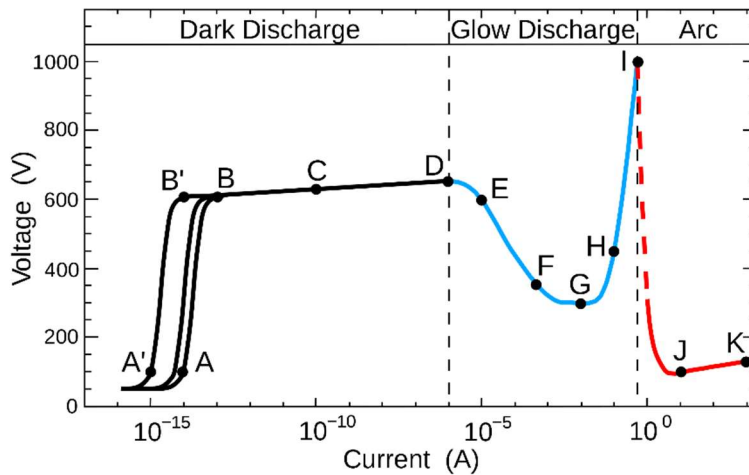


Figure 5 --- Townsend avalanche process (Wikipedia, 2019)

## **2.3 Contemporary Technology Derived from Cold Cathode Display**

One of the most successful and widely used technologies developed based on the cold cathode display technology today is the cold cathode fluorescent lamp (CCFL). Instead of using the generated light as a direct means of conveying information, CCFL is mostly used by transmissive liquid crystal display as the backlight illumination source for it to operate. (Lin, Ho, Shih, Chen, & Wu, 1998)

Since most of the cold cathode display devices are obsoleted and have limited access or resources to the datasheet and analysis model of the tubes, a model built by researchers from the University of Korea on CCFL is used in a proof of concept project (Cherl-Jin, Byeong-Kyu, Shin-Yong, & Soo-Hyun, 2005) which is used in this thesis to approximate the behavior of the cold cathode display. (IN-13 manufactured by USSR during World War II).

## **2.4 Motivation of Designing a Cold Cathode Display-Based Device with Modern Digital Technology**

Back to the 1940s and 1950s when the cold cathode displays were widely and massively used across the spectrum of commercial products, military operations, and almost every single aspects of human life, digital control and signal processing technology barely exist; thus, almost all applications build around the cold cathode displays are driven by pure analog circuits, which came at the cost of minimal functional flexibility, and immense power consumption combined with large device size that makes it unrealistic for uses in mobile devices. However, with all the

modern technological advancements in digital processing and control technology, there is an opportunity to explore what could be possible for these old cold cathode display devices.

Thus, from Chapter II of this thesis, it will focus on a proof of concept project to utilize one of the less-discussed bar graph linear cold cathode display IN-13, to build an audio spectrum visualizer to explore this potential.

### 3. Proof of Concept Design – Audio Spectrum Visualizer (Electrical)

#### 3.1 Major Revision on the Electrical Design

There are two major releases and more than a dozen smaller revisions of this audio spectrum visualizer's electrical designs. While the smaller revisions focused on stability and minor functional improvements, the two major releases are the main topic of this section.

#### 3.2 First Revision of the Electrical Design (MK1)

The first version of this project's electrical design is mainly a proof-of-concept system that focused on designing the driving circuit of the IN-13 display tubes and the feasibility using IN-13 with a digital microprocessor as an audio spectrum visualizer. To realize these potentials, the MK1 electrical design is highly modular, with lots of design overheads, and based on a very simple 8-bit ATMEGA MCU with well-developed libraries and design documents. To make this design easy to build and debug with, two simple 2-layer printed circuit boards (PCB) are designed with components size no smaller than 0805 package sizes (about 3mm x 1.5mm dimension), as shown in Figure 6 and 7.

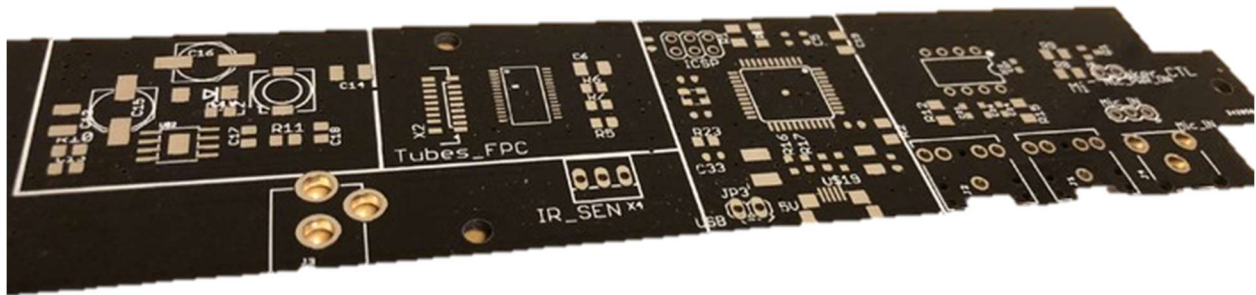


Figure 6 --- MK1 Audio Spectrum Visualizer PCB

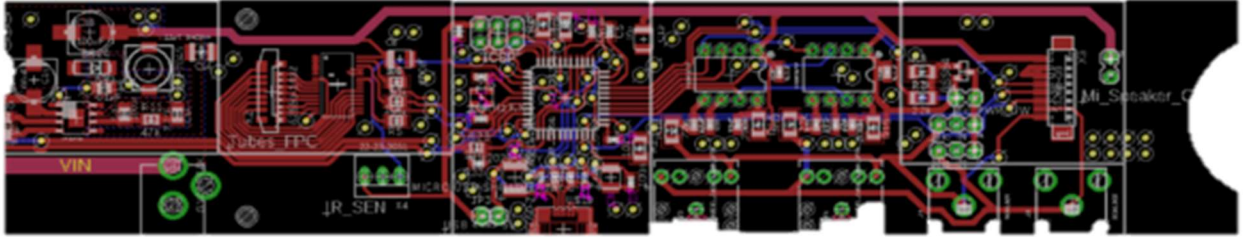


Figure 7 --- MK1 Audio Spectrum Visualizer PCB

The first PCB that contains all the necessary control logic runs on low digital voltage, while the second PCB contains all the tube driver circuits that runs on high voltage. This MK1 design works well as the bedrock and the initial platform for the project since it provides an outstanding modification possibility and debugs convenience; however, it also comes with the cost of the PCB's sizeable physical dimension, which is just the byproduct of relatively low complexity design.

For the Input/Output consideration of MK1's design, it is being powered by 12V DC via a traditional DC barrel jack, one USB micro-A port for programming and firmware update, two 3.5mm AUX audio jack for audio input and mirroring output, and finally two RCA coaxial audio input/output ports.

The central processor in Mk1 is an 8-bit Atmel ATMEGA 32U4 microcontroller. In order to display the spectrum information, there are two MSGEQ7 spectrum analyzer chips in this design to acquire the required information from the analog audio input, and lastly, an I2C PWM controller is used to generate all 14 channels of voltages need to be used to drive the 14 IN-13 tubes (7 tubes for each audio channel in stereo audio).

MSGEQ7 is a simple seven bandpass filters follows by peak detectors. The predefined bandwidth seven bandpass filters made the system easy to be used and programmed as shown in Figure 8; however, this also introduced a limitation of frequency resolution since there is no accurate way to produce an estimation of energy at a specific frequency band between the predefined bandpass range. It is possible to do mathematical estimation on the energy of these band since each predefined bandpass range of the MSGEQ7 has an overlay with each other; thus, a simple reverse 2/3 tap FIR filter should be able to make a rough approximation, but the system still needs to face physical limitation introduced by these fixed bandpass range. The built-in digital logic provides a simple and straightforward pulse/select/reset way to output the results from each peak detector's output onto one output pin and sweep across seven bandpass filters' peak detector based on the pulse signal input.

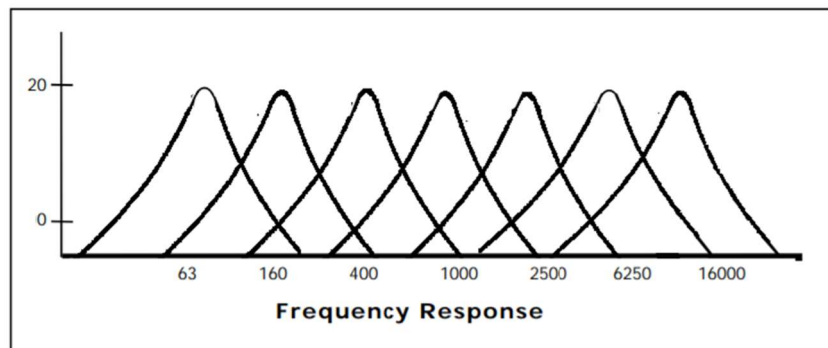


Figure 8 --- MSGEQ7 Bandpass Bin Arrangement (MSI, 2004)

The output of this design is based on a PWM controlled scheme. Since the cold cathode display tube used in this design (IN-13) is a current-controlled device, an LC lowpass filter with a 3dB cutoff frequency of 1kHz is used to mimic the switching output of the PWM driver into controlled pseudo-current sources to drive all the tubes. This design decision introduces both

advantages and disadvantages into the system: The LC lowpass filter prevents abrupt changes of the current passing through the tubes, and by avoiding abrupt current changes, the lifespan of the tubes can be improved. Nevertheless, in the meantime, this also limited the possible effects that can be displayed on the tubes by introducing the physical limitation of  $\frac{dI}{dt}$  by the LC lowpass filter.



### 3.3 Final Revision of the Electrical Design (MK2)

The second-generation design of this proof of concept project is an overhaul of the previous generation design, various improvements are made based on the discoveries from previous attempts, and various new functions are added to the final design. The significant shifts from the previous generation include the method of spectrum analysis, method of mimicking controlled current source, method of frequency band deinterlacing, and computing unit, et cetera, Table 1 contains a methods to methods comparison between MK1 and MK2 design of this proof of concept project.

Table 1 --- Side to side comparison between MK1 and MK2 design parameters

Subsystem	MK1	MK2
<b>Computing Unit</b>	ATMEGA 32U4 8bits MCU	STM32F427 Cortex M4
<b>Power Source</b>	12V DC Power Supply	USB-C 100W Power Delivery
<b>AUX Power Supply</b>	N/A	2x 18650 Lithium Ion Cells
<b>ADC for Audio Signal</b>	MSGEQ7 built-in ADC	STM32F427 Built-in ADC for low power operation
<b>AUX ADC</b>	N/A	External I2S 12bits
<b>DAC</b>	16 channels PWM Driver with LC-LP filter	Dedicated 12bits SPI DAC (DAC80508)

One of the most critical design decisions of MK2 from MK1 is to shift from the MSGEQ7's predefined analog bandpass filters to using fast Fourier transform and fast Hartley transform to reduce the power consumption, reduce the dimension of the design, and increase the overall flexibility.

### 3.3.1 Computing Core

STM32F427 ARM Cortex M4 based controller is used to provides higher computing power compared with the ATMEGA 32U4 8bit AVR controller used in the MK1 design, which enabled the possibility of replacing the MSGEQ7 from the system. Compared with ATMEGA32U4 (Atmel Corp, 2016), STM32F427 can provide at least 14 times more instructions per second performance (16MIPS vs. 225MIPS) while operating at higher primary clock frequency (16 MHz vs. 180 MHz), four times register width (8bits vs. 32bits). The power efficiency (i.e., mW/MHz rating) of STM32F427 is about two times better than the ATMEGA32U4. (ST Semiconductor, 2018) The schematic of this computing core is shown in Figure 9 and Figure 10.

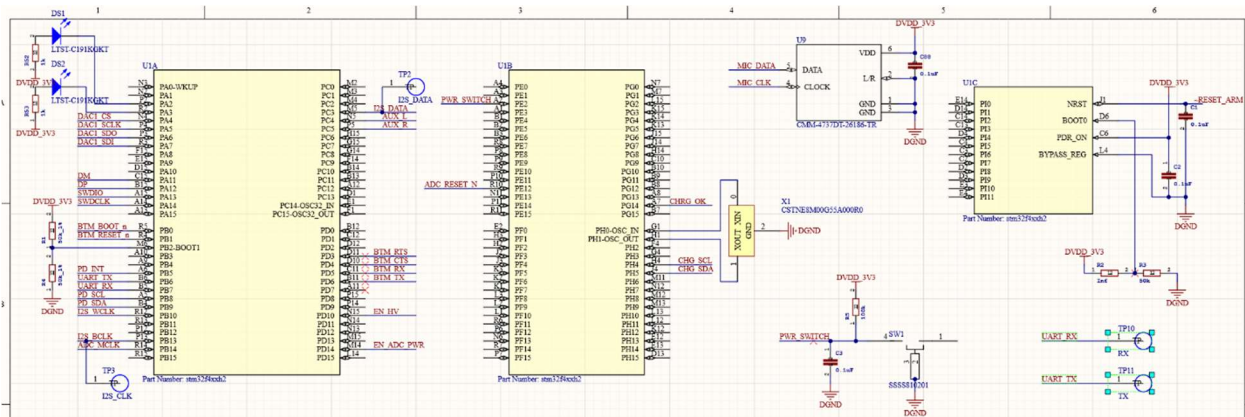


Figure 9 --- STM32F427 Cortex M4 Computing Core's Schematic

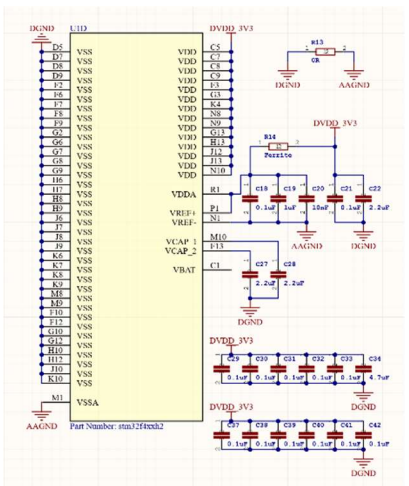


Figure 10 --- STM32F427 Cortex M4 Power Supply Schematic

### 3.3.2 USB-C Power Delivery

In order to archive both the convenience of being compatible with as many existing chargers in the market as possible and retain the possibility to enable the fast-charging capability of the two 18650 lithium-ion cells in the system, an integrated USB-C Power Delivery negotiator IC from Cypress is used to control the power source monitoring and negotiation, and the processes are shown in Figure 11. USB-C PD is a communication protocol between devices as power sources and devices as power sinks. Upon connection, the power source device will provide a table of power settings that it can; then, the power sink can let the power source know which voltage/current rating it wants from the power source device. If the power source device does not support the latest USB-C PD standard, i.e., it will not provide any power ratings

for the power sink device to select with. The VBUS power rail will then be held at default 5V standard USB operation, and the negotiator IC will tell the main microcontroller that the upstream power source device is a back compatible charger with a minimum potential power rating of 5V/500mA via an I2C interface. At the optimal condition, the charger will provide up to 100W to the application circuit at 20V/5A.

Packet	Direction	Source	Destination	Msg Type	DR	PR	Msg ID	Obj Cnt	Cmd	Cmd Type	Obj Pos	Vendor ID	Max Cur	Voltage	Dual Role	Max Cur	Voltage	Dual Role	Max Cur	Voltage	Dual Role	
4 Packets 32-35	→	CBL		Vendor Defined	DFP	UFP	0	1	Discover Identity	Initiator	0	PD SID										
Packet 36	Right	"82-EVM Src"	SRC	Source Cap	DFP	SRC	0	3	Fixed	3.00 A	5.00 V	0	Fixed	3.00 A	12.00 V	0	Fixed	3.00 A	20.00 V	0		
Packet 37	Left	"82-EVM Snk"	SNK	GoodCRC	UFP	SNK	0	0														
Packet 38	Left	"82-EVM Snk"	SNK	Request	UFP	SNK	0	1	Request	3.00A / 75.00W	3.00A / 75.00W	0	3									
Packet 39	Right	"82-EVM Src"	SRC	GoodCRC	DFP	SRC	0	0														
Packet 40	Right	"82-EVM Src"	SRC	Accept	DFP	SRC	1	0														
Packet 41	Left	"82-EVM Snk"	SNK	GoodCRC	UFP	SNK	1	0														
Packet 42	Right	"82-EVM Src"	SRC	PS Ready	DFP	SRC	2	0														
Packet 43	Left	"82-EVM Snk"	SNK	GoodCRC	UFP	SNK	2	0														

Figure 11 --- USB-C Power Delivery Communication Pipeline (Texas Instrument, 2016)

The physical endpoint of the power input system is a USB-C port from the JAE connector. In this system design, only USB2.0 ports, USB-PD communication, and power rails are used. Physically, two termination resistors are used to match the trace impedance to 90Ohm differential following the requirement from USB-IF. Also, an R-C network is used on the power rail to provide ESD protection and transient voltage surge when the cable is plugged into or unplugged from the system due to the combination of rapid current change and the parasitic inductance from the long cable length. The schematic of this USB PD negation circuit is shown in Figure 12.

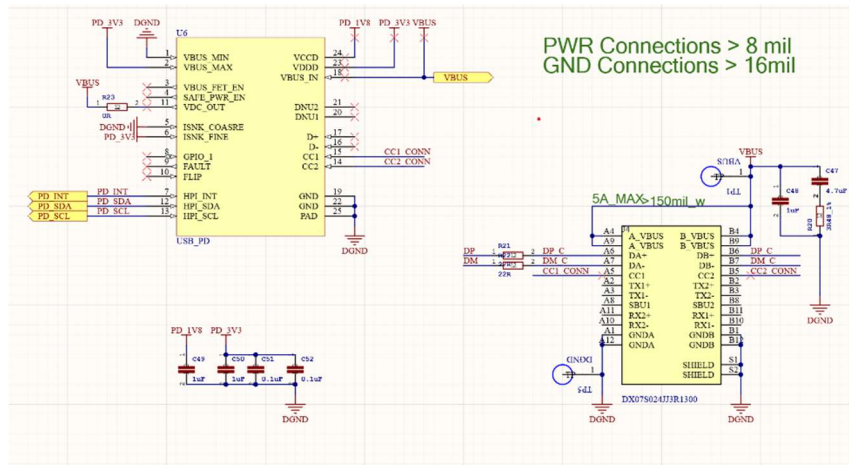


Figure 12 --- USB-C Power Delivery & PHY Schematic

### 3.3.3 Battery Management and Charging System

The battery management system (BMS) consists of supports for battery protection, charging, cell balancing, battery life monitoring, and power input and output monitoring. In this design, a BMS IC BQ25703 from Texas Instrument is used combined with two 18650 lithium-ion cells to accommodate all the required functions.

Five power MOSFETs (i.e., IC1, IC2, IC3, IC4, U7) are used to enable the BQ25703 controller to control the current flowing direction among battery, application circuit, and external USB-C PD power supply. Since the range of possible input voltages from the USB-C PD supply diversifies from 5V to 20V, and the two 18650 lithium cells in series' charging voltage demand also can vary from 3V (depleted) to 8.4V (fully charged), there is no manageable buck nor boost conversion charger topology can be used. A charger IC can handle broad input and output with buck and boost capability is used. The BMS IC's buck and boost capability allow the battery to

be charged following the required charging protocol. If the battery is completely depleted, upon power on, U7 is first enabled to operate in its linear region, which imitates the behavior of a Low Dropout power supply with a minimum current to activate the battery cells. During the second phase, the battery enters the constant current charging mode, and power input from the battery port reaches its maximum at this phase. For this design, 18650 cells with a capacity of 3200mAh are used with a charging coefficient of 2, which leads to the maximum current at a constant current charging phase of 6.4A calculated by Eq 3.1.

$$I_{CHG} = Capacity_{Cells} * \alpha_{charging}$$

Eq 3.1 --- Charging Current Calculation

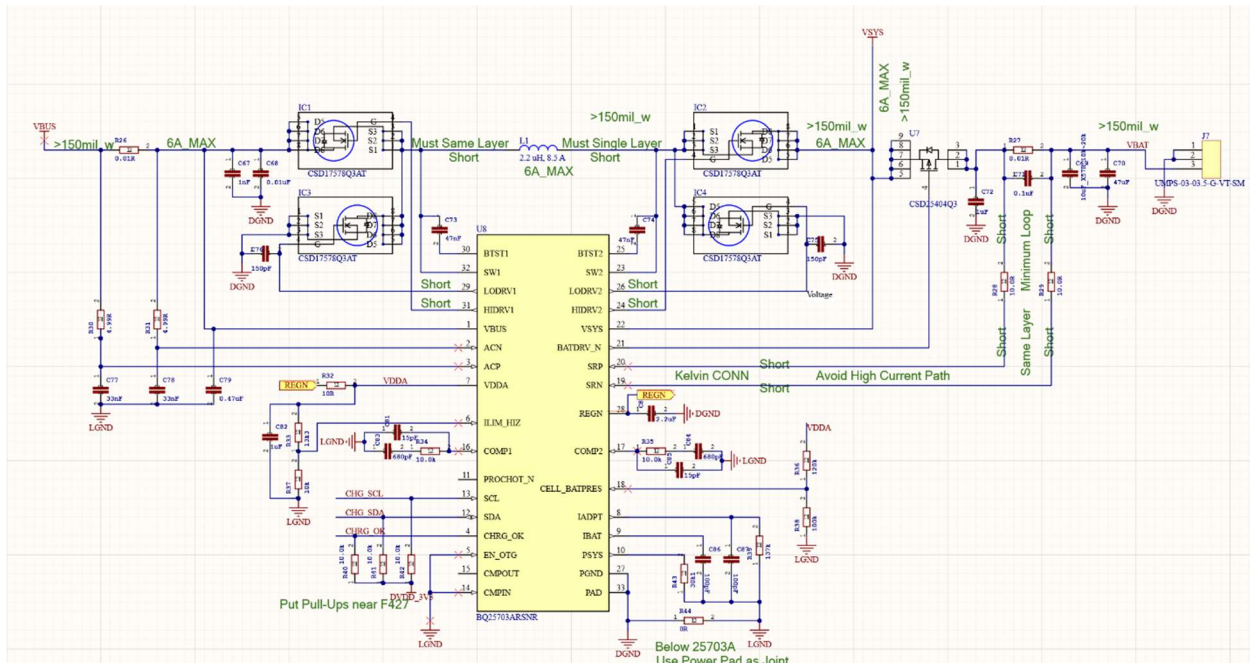


Figure 13 --- BMS Schematic

Since this design has multiple power sources (i.e., battery and external USB-C PD source), it is vital to implement a robust finite state machine to monitor, predict, and act on the power tree based on different operation conditions. Above all, the first parameter that needs to be calculated is the application circuit's maximum power requirement under routine operation. The decision tree is then built to distinguish different power input options and how and where to route the input power. The schematic of this BMS circuit is shown in Figure 13.

**Table 2 --- Power Tree Operation Conditions**

<b>Power Input from USB-C PD</b>	<b>Battery Remaining Capacity</b>	<b>Power Routing of Input Power</b>	<b>Battery Status</b>	<b>Application Status</b>
$> \max(P_{sys}) + \max(P_{chg})$	Don't Care	Both Battery and Application Circuit	Full Speed Charging or Idle	Normal Operation
$> \max(P_{sys})$ $< \max(P_{sys}) + \max(P_{chg})$	Low	Both Battery and Application Circuit	Limited Charging Current	Normal Operation
$> \max(P_{sys})$ $< \max(P_{sys}) + \max(P_{chg})$	Normal	Application Circuit only	Cutoff	Normal Operation
$< \max(P_{sys})$	Normal	Application Circuit only	Partial Support Application Circuit	Normal Operation
$< \max(P_{sys})$	Low	Battery	Full Speed or Limited Current Charging	Stopped

### 3.3.4 Power Management

Since this design incorporates a battery-powered system, investigation, and optimization to minimize power consumption are essential. To minimize power losses along the power tree, a high-efficiency wide input range, two independent outputs, buck only integrated switching power regulator from Linear Technology is selected to buck the bus voltage from the battery's output to 3.3V for microcontroller operation, and 5.5V for all other cold cathode display driving-related circuits. It can be deduced that the minimum cutoff voltage point for low battery condition in section 3.3.3 should be 5.0V (2.75V for each cell), which corresponds to the 100% duty cycle setting of the LTM4622 regulator's second output port.

In the meantime, after the cold cathode display tubes' driver circuit is turned off, the first output port of LTM4622 can still be enabled since the input voltage is still greater than 3.3V, and the power requirement for the microcontroller operates in the monitoring mode without running FFT/FHT is minimal. The microcontroller running in the background will continue monitoring the USB-C PD negotiator IC, BMS IC, and battery terminal voltages to ensure taking the whole system back on the operation after certain conditions are met.

Another low noise Low Dropout (LDO) regulator is used to provide a clean power supply to the Digital to Analog Converter (DAC) that is used to generate the reference voltages fed into the base of the high voltage transistors controlled the current flowing through the cold cathode display tubes. The reason that a separate 5.0V low dropout is used instead of lower the second output of LTM4622 is that the DAC requires stricter noise performance of its power supply,



which eventually directs to cleaner reference voltages and cleaner current outputs into the cold cathode display tubes. The schematic of this power supply circuit is shown in Figure 14.

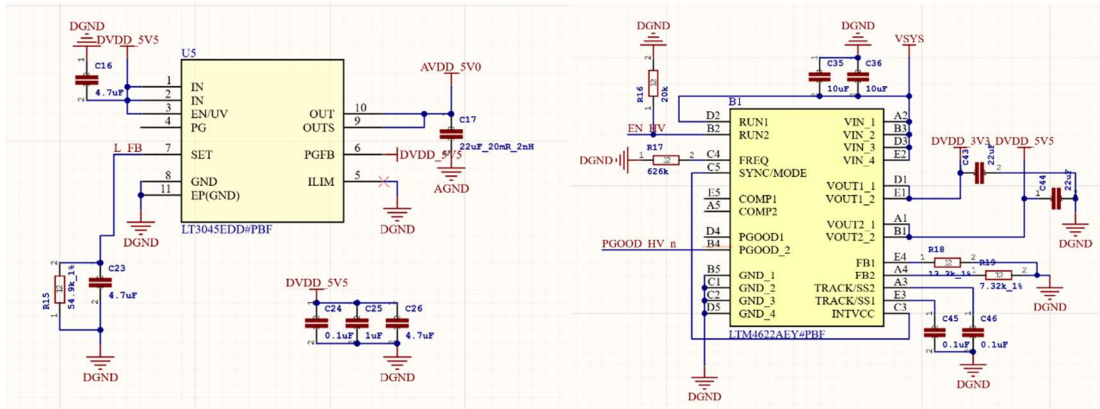


Figure 14 --- System Power Supplies Schematic

### 3.3.5 Digital to Analog Conversion

A 12bits dedicated DAC DAC80508 with a high drive capability of 20mA from Texas Instrument is used to render a reference voltage to generate the base current of the high voltage power transistors used to restrain the current flowing through the cold cathode display tubes. After matching with the base resistors for each power transistor, a span coverage of 90% usable range is reached. In combination with the DAC's 12bits resolution, one least significant bit (LSB) quantization resolution of 0.033mm on the actual cold cathode display tubes based on the tube's total electrically linear response region is at 120mm.

$$LSB_Q(mm) = \frac{120mm}{2^{12}} * 0.9$$

Eq-3.2 --- DAC Quantization Precision Calculation

Also, a Surface Mount Ferrite Bead (R9) with an impedance of 100Ohm@1MHz is used for GND isolation between DAC's dedicated analog ground and the rest digital ground for the system to ensure the noise performance of the. The schematic of this DAC circuit is shown in Figure 9.

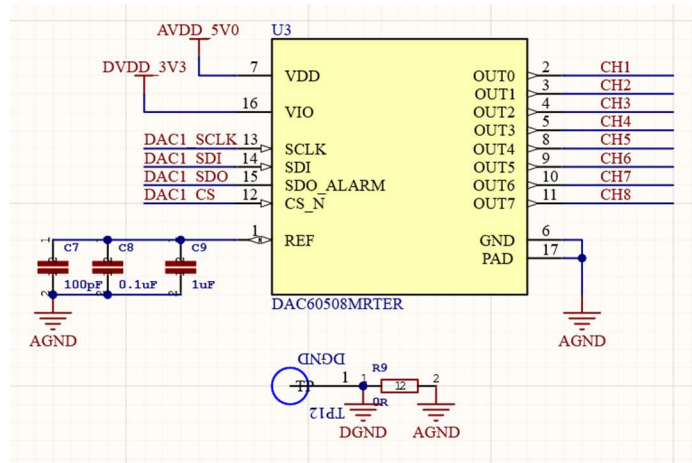


Figure 15 --- DAC Schematic

### 3.3.6 Tube Drivers and High Voltage DC Supply

The DC/DC flyback boost converters are in charge of boosting the raw battery output that could range from 5V to 8.4V DC up to 140V DC for the normal operation of the cold cathode display tubes. The maximum current consumption of each of the IN-13 cold cathode display tube is 7mA under overdrive condition, which leads to a maximum instantaneous power requirement of total  $7mA * 8 * 140V = 7.84W$

The DC/DC flyback boost converter is designed that each of them can handle long term continuous power output at the output side (i.e., effectual power output) at 8W and transient power output up to 12W at the output port without experiencing any noticeable voltage drop or overheating issue.

Two DC/DC flyback boost converters are used parallel and individually controlled by the control logic located on the lower PCB board. The resistor divider located at the internal regulator's output will provide a good power and operation status to the STM32F427 microcontroller on the lower board, then the microcontroller can decide which or both of the DC/DC flyback boost converters are going to be used to power the cold cathode display tubes. Under regular operation, both DC/DC flybacks are connected parallel to the voltage rails to load balance the power consumption by the cold cathode display tubes, thus prolonged the lifespan and lower the meantime before the error (MTBF) of the DC/DC flyback boost converter. Under exceptional circumstances such as regulator failure of one of the DC/DC flyback power supply, the system can still be powered and persist regular operation with only one active DC/DC flyback boost converter. The schematic of this tube driver circuit is shown in Figure 16.

The driver circuit of the cold cathode display tube is designed with the most straightforward implementation to ensure stability and a long-life span. Each of the driver circuits is powered by a high voltage up to 140V. Each of the eight IN-13 tubes has assigned with a single NPN high power transistor for current control propose. The R22 set the maximum current allowed to pass through each of the tubes, and C17 set the maximum slew rate of how fast the current can be altered.

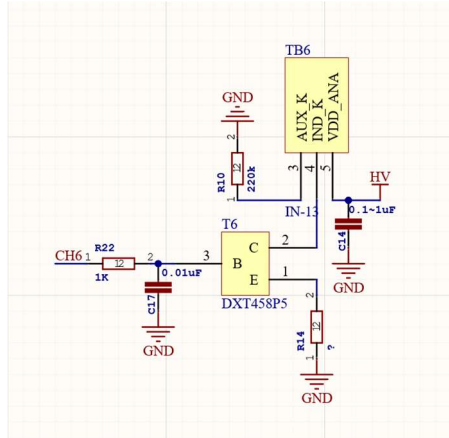


Figure 16 --- Tube Driver Schematic

### 3.4 Final Revision of Mechanical Design (MK2)

There are two different Printed Circuit Boards (PCB) in this design, which leads to a two layered stacked design. The primary reasons for the usage of layered design instead of a unibody design are to maximize usable PCB real estate area and potential routing area and to separate high-speed, low voltage digital circuits and the high voltage analog system for the cold cathode display tubes operates at more than 140V DC. This avoids or limits the damages caused by the potentiality of Electromagnetic Interference (EMI) from the high voltage analog system coupling into too low voltage digital system, which introduce the Electromagnetic Compatibility (EMC) of the control circuits.

#### **Low Voltage Board**

The low voltage board on the bottom of the stack consists following primary components/sub-systems: STM32F427 Digital Core, Digital to Analog Converter (DAC) for tube currents' reference voltages generation, Analog to Digital Converter (ADC) for the audio signal to digital signal conversion, Battery Management System (BMS) covered in section **3.3.3**, Wireless Communication Module for Wi-Fi and Bluetooth capability, power supplies and power distribution system, and connectors and I/O ports to the battery cells, the high voltage board, power supply, and audio inputs. The board is shown in Figure 17.



Figure 17 --- Low Voltage Controller Board

### Board cutouts on low voltage board

To minimize the thickness while providing the full protection of the fragile lower portion of the cold cathode display tubes maintains the potential of easy and straightforward tube replacement, reliable mechanical and electrical connections, and accurate vertical alignment during the assembly process, a customized 3D structure contains multiple 3D printed Nylon parts with a flexible injection-molded inner holder is designed as the tube holder as shown in Figure 18 and Figure 19. Mechanically, the more prolonged and more extensive the tube holder assembly, the better the final mechanical and electrical performance could be for the final assembly; thus, the tube holder's vertical dimension plays a crucial role in the system.

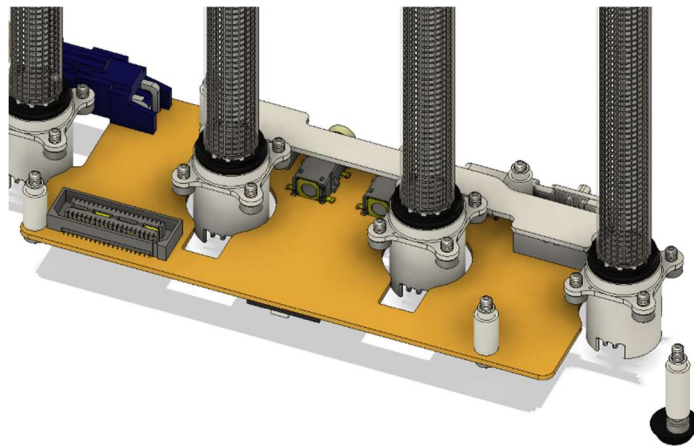


Figure 18 --- Low Voltage Board's Cutouts for Tube Assembly Clearances

To provide the spaces for the longed tube holder assemblies, two cutouts with the shape of the lower part of the tube assemblies are made on the low voltage board to accommodate the challenge of making the enclosure of this design as thin as possible in order to increase the aspect ratio of the actual cold cathode display tubes, and aesthetically improve the appearance of the design.



Figure 19 --- Tube Holder Assembly

Since the real estate of the low voltage board is very restricted due to the nature of the small form factor of the system combines with the unavoidable board cutouts, a six-layer board stack up PCB fabrication technology with the combination of cutting edge fabrication technology such as via-in-pad, blind-via, buried-via, Ball Grid Array (BGA), and High-Density Interconnect (HDI) are used to maximize usable routing area.

**High Voltage Board** The high voltage board consists two DC/DC flyback boost converter, eight cold cathode display tube driver circuits with electrical port for the tube connection, connector to the low voltage board, and eight board cutouts for tube holder assemblies. The high voltage PCB is shown in Figure 20.



Figure 20 --- High Voltage Board PCB & DC/DC Flyback Power Modules



## 4. Firmware & System Logic

Since STM32F427 Cortex M4 Microcontroller is chosen as the primary computing unit in this design, CMSIS-RTOS v1 is used as the underlying real-time operating system. The software of the system implemented with a layered design in a controlled manner, the most bottom layer is the STM32CubeMX's Hardware Abstraction Layer (HAL), which provides all the primary and essential I/O and internal hardware resources access, and the HAL is also used by CMSIS-RTOS for OS-level functionalities. The second bottom layer is the layer of Board Support Package files (BSP files). BSP packages provide all the necessary communication protocols required for communication with external devices such as I2C communication with the USB-C Power Delivery Subsystem and SPI communication with the Audio ADC for analog audio signal sampling. The BSP Layer is a combination of wrapped communication functions utilized by the HAL provided by ST Semiconductor.

(On top of the BSP layer is our library layer. All those library files have related APIs for different components in our system. In our implementation, each library usually has an initialization function, together with dozens of other stat monitor or debug functions that can fully utilize all the component's functionalities. On top of the library, the layer is our task layer. All these tasks are initialized and managed by CMSIS-RTOS. With our RTOS's help, we can easily schedule audio sampling tasks, FFT tasks, DAC tasks, and power management tasks.

In many cases, FFT will be a very time-consuming operation for MCUs. However, since we are using Cortex M4 series MCU, which has a hardware FPU, we adopted ARM's floating-point math

library, which gives us a considerable performance boost. All the code that we wrote is in the "Applications" folder in our code base.)

## 5. Conclusion

Based on the success of developing a proof-of-concept project utilizing the cold cathode display linear tube technology (IN-13), it is clear that even today, there is still great potential for visual art and digital art projects to explore the possibility of using cold cathode display technology. With the digital control and signal processing technological advancements during recent years, the full potential of cold cathode display can be re-explored. It is worth integrating cold cathode display into brand new design concepts to archive functions and effects that were considered physically impossible a few decades ago. In the meantime, the unique glowing characteristics of the cold cathode display have no contemporary counterparts that resemble it.



Figure 21 & 22 --- MK2 Audio Spectrum Visualizer

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