Improved MIMO Modelling and Enhanced Transient Performance of Phase Locked Loop During Grid Fault

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***Abstract*—In a grid-connected power converter, synchronizing with ac grid voltage is often realized by a phase-locked loop (PLL). A single input single output (SISO) linear model of PLL with the phase angle of the point of common coupling (PCC) voltage as input and the estimated phase angle as the output is generally used in the PLL analysis and design. However, an undesirable coupling between the magnitude and phase of the input voltage is present when a filtering stage is incorporated before the control loop, which cannot be captured by a SISO model, and could result in a large disturbance in the PLL estimated phase during grid faults To overcome this deficiency in SISO PLL modeling, this paper proposes a generalized multi-input multi-output (MIMO) linear model that captures the complete PLL dynamics during symmetrical faults for a PLL equipped with any prefilter. The proposed model captures this undesirable coupling between the magnitude and phase of the input voltage. Furthermore, a compensation method that decouples the magnitude dynamics of the input voltage from the phase dynamics is proposed in this paper. The proposed compensation improves the PLL's phase tracking performance by ensuring that the prefiltered PLL acts only on the PCC voltage phase changes. A vital application of the proposed compensation method for PLL is during a grid fault case, wherein the converters are expected to contribute to the fault current, which requires an accurate measurement of the PCC voltage phase. The compensation method's effectiveness is demonstrated using power hardware in the loop simulation of a hardware voltage source converter interfaced to a distribution system simulated in real-time.**

***Index Terms*—phase-locked loop (PLL),Power system faults**

I. Introduction

THE proliferation of power electronics (PE) based resources into the power system brings immense challenges and well-known benefits. Challenges arise, mainly because it is harder to describe the PE resources' response. It is driven by embedded control, unlike the synchronous machine, where physical parameters primarily drive their response. The difference in response is apparent in the case of fault current contribution, as the response from a synchronous machine is well described and predictable but it is not the same in the case of a PE based generation and compensation [1]–[3]. There are several different control strategies for PE-based generation proposed in the literature [4], which introduces diverse fault current characteristics and grid voltage support. An improper response current to grid fault from a converter could also result in currents from different converters to offset the reactive power contribution from rest of the components [5]. The grid codes expect that the PE resources quickly inject fast fault reactive current to the system to ensure the satisfactory protective relay system operation [6], [7]. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system.

Central to the requirement for a fast fault current contribution is accurate detection of the phase of the point of common coupling (PCC) voltage, typically achieved by a phase-locked loop (PLL) based synchronization unit [8]. During the fault event, both the magnitude and phase of the PCC voltage are disturbed, making it challenging to estimate the phase of PCC voltage using PLL. A comprehensive modeling of the PLL is necessary in the fault scenario to design the control parameters to meet the strict time-domain performance requirements, such as a rise time for reactive fault current injection in tens of milliseconds as specified in the grid codes. Several variations of PLL's for power converters were proposed over recent years [9], [10]. Despite the differences in their names, most of them are structurally similar and are derived from a conventional synchronous reference frame PLL (SRF-PLL) shown in Fig. 1. These differences between PLL types are mainly due to the different types of filtering incorporated in the PLL. These filtering of the PCC voltages are implemented in mainly three stages: digital filters in the stationary reference frame (prefilter,$PF2(s)$), the digital filters embedded in the PLL control loop (in loop filters,$IF(s)$), and the physical filtering ($PF1(s)$) present due to anti-aliasing filter, as well as transducers and its associated circuits as shown in Fig. 1, [9]. Both prefilter and in-loop filters are incorporated in the PLL structure to enhance the disturbance rejection capability of PLL during non-ideal grid voltage conditions, such as in the case of harmonics and unbalance in the PCC voltages. The classification of the most advanced PLL's is done based on the presence, absence, and types of prefilter and in-loop used in the PLL design. The PLL's with prefilter include, but not limited to, dual second-order generalized integrator based PLL (DSOGI-PLL) [8] multiple complex coefficient filters [8] based PLL both used to extract the positive sequence components of three-phase ac voltage before the PLL control loop. Further, even a simple lowpass or a bandpass filter implemented in the stationary reference frame

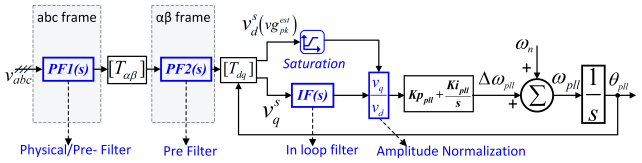

Fig. 1. Common structure of three Phase SRF-PLL with disturbance rejection capabilities

can also be considered a prefiltered type PLL. Several PLL's and frequency-locked loops (FLL) with prefiltering has been proposed in the literature to estimate the phase of distorted PCC voltages with unbalances in both amplitudes and phase angles [11], [12].

For PLL controller parameter design, most of the past work utilizes a linear time-invariant single input single output (SISO) PLL model with the phase angle ($\theta_g(t)$) of the PCC voltage as input and its estimated phase angle ($\theta_{pll}(t)$) as its output [13]. Extension of such a model is straightforward for the PLL's with in-loop filters [13], [14]. However, obtaining a SISO model is not a trivial task for a prefiltered PLL since the filtering takes place in a stationary frame with time-varying sinusoidal voltages. When analysis PLL's with sudden large disturbance in voltage magnitude it is important to consider the PCC voltage magnitude change as in input in PLL modelling. An extended SISO model that consider the harmonic components of the PCC voltage as a disturbance input is presented by [14]. While such a model is sufficient to capture PLL dynamics during small disturbances and control design, this paper shows that for PLL's equipped with additional filters for disturbances and harmonics elimination, the SISO modeling is inadequate. For studying large disturbances like power system faults, a multi-input multi-output (MIMO) dynamic model of the PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs is necessary to improve the modeling and control design. Such a MIMO model of the PLL could also improve synchronization stability assessment accuracy improvement during severe grid faults [15], [16]. Several recent studies have presented linear time-periodic (LTP) MIMO models of specific types of PLL's and frequency-locked loops (FLL). These MIMO models can account for the presence of harmonics and/or imbalance [17], [18]. In [12] modelling and an improvement in transient response and harmonic response for a second-order generalized integrator based FLL is presented. However, these MIMO models are specific to PLL/FLL types and cannot be generalized for prefiltered PLL types. In [19], a generalized method for converting the prefiltered section of the PLL's implemented in the stationary frame to a rotating reference frame is presented. Such a method could be used as the basis for establishing a generalized (MIMO) dynamic model of the prefiltered PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs.

In this paper, a generalized MIMO model for prefiltered PLL, which captures the complete dynamics of prefiltered PLL during faults, is proposed. From the developed nonlinear MIMO model, it is readily observable that unlike a PLL with in-loop filters, for the PLL's with prefilters implemented in the stationary frame (including physical filters), there exists a coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. Such a coupling is not a desirable attribute to a PLL as it is intended to only respond to the change in phase of the terminal ac voltage and could result in wrong estimates of frequency and phase during faults. Based on the derived nonlinear MIMO model, a linearized model is developed to aid the controller design. A supplementary control loop is proposed in the paper to reduce the coupling effect of the instantaneous peak of the ac voltage to the estimated phase. Overall the contributions of the paper are,

1) Develop a MIMO model of a prefiltered PLL which captures the complete dynamics of prefiltered PLL during faults. The model is useful in enforcing a strict time-domain requirement for converter response during fault cased. Further, the model can be used for converter control design as well as synchronization stability analysis;
2) A supplementary control loop is proposed for a prefiltered PLL, which not only reduces the transients in the estimated phase and frequency during fault but also eliminates the steady-state phase lag introduced by prefilters

The modeling and analysis in the paper is generalizable for all types of prefiltered PLL. However, for the sake of brevity, the analysis presented in the paper is restricted to three of the commonly used types of prefilters, (i) PLL with first-order lowpass filter as prefilter (LPF-PLL), (ii) PLL with bandpass filter as prefilter (BPF-PLL), (iii)PLL with DSOGI as prefilter (DSOGI-PLL). Additionally, to show the effectiveness of the proposed model and supplementary control on a cascaded prefilter as an example application of a PLL with both physical filter and a prefilter, a PLL with DSOGI as prefilter and a first-order lowpass filter as a physical filter (LPF-DSOGI-PLL) is also studied in this paper.

II. Overview of PLL operations and motivation

In SRF-PLL with prefilter is as shown in Fig. 1. The three phase instantaneous PCC voltages (v_{abc}) are first filtered and transformed into a rotating reference frame (dq frame) using estimated phase angle θ_{pll}. The q-axis voltage (v_q^s) of the the transformed voltages is then driven to zero in steady-state by a Proportional Integral (PI) controller with a proportional gain Kp_{pll}, and integral gain Ki_{pll}. In steady state, the magnitude of the d-axis voltage (v_d^s) is equal to the magnitude of the input PCC voltage (vg_{pk}), hence the v_d^s is also termed as estimated peak voltage of the PCC voltage (vg_{pk}^{est}). The PLL estimated frequency ω_{pll} is the sum of the nominal frequency (ω_n) and output of the PI controller ($\Delta\omega_{pll}$). A dynamic amplitude normalization is implemented in all the PLL's considered to ensure the loop gain of the PLL remain the same for all magnitude of the grid voltages. The $[T_{\alpha\beta}]$ and $[T_{dq}]$ in Fig. 1 are the Clarke (abc to $\alpha\beta$) and park ($\alpha\beta$ to dq) transformation matrices.

$$[T_{\alpha\beta}] = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{1}$$

TABLE I
TRANSFER FUNCTIONS AND PARAMETERS OF THE FILTERS USED

Prefilter type	Transfer Function	Parameters
Bandpass prefilter	$H1(s) = \frac{2\,\omega_n\, s\,\zeta}{s^2+2\,\omega_n\,\zeta\, s+\omega_n}$	$\zeta = 0.707$
	$H2(s) = 0$	$\omega_n = 2\pi 50\ rad/\sec$
Lowpass prefilter	$H1(s) = \frac{\tau}{s+\tau}$	$\tau = 0.0005$
	$H2(s) = 0$	
DSOGI prefilter	$H1(s) = \frac{k\,s}{\omega_n{}^2+s^2+2\,\omega_p\,s}$	$\omega_n = 2\pi 50\ rad/\sec$
	$H2(s) = \frac{\omega_n\, k}{\omega_n{}^2+s^2+2\,\omega_p\,s}$	$k = \sqrt{2}$
Lowpass Inloop	$IF(s) = \frac{\tau}{s+\tau}$	$\tau = 0.0005$

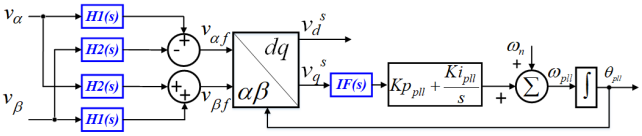

Fig. 2. Generalized representation of prefiltered SRF PLL

$$[T_{dq}] = \begin{bmatrix} \cos(\theta_{pll}(t)) & \sin(\theta_{pll}(t)) \\ -\sin(\theta_{pll}(t)) & \cos(\theta_{pll}(t)) \end{bmatrix} \quad (2)$$

In a PLL, the physical filtering stage ($PF1(s)$) and prefilter stage ($PF2(s)$) could be present in abc frame or $\alpha\beta$ frame. However, most filtering action in the abc frame can also be represented in an equivalent $\alpha\beta$ frame model. For instance, a low pass filter or a bandpass filter implemented in abc frame is similar to the same filters implemented in $\alpha\beta$ frame [19]. Hence the PLL's with a filtering stage (both $PF1(s)$,$PF2(s)$) present in the stationary reference frame (abc and $\alpha\beta$), can be represented in a convenient generalized form as shown in Fig. 2 with no distinction between a prefilter or physical filter. The transfer functions $H1(s), H2(2)$ shown in Fig. 2, acts on the $\alpha\beta$ frame value of the terminal voltages (v_α, v_β) to give the filtered $\alpha\beta$ frame terminal voltages $(v_{\alpha f}, v_{\beta f})$. The transfer functions $H1(s), H2(2)$ could include

1) The 2×2 MIMO transfer function of a prefilter implemented in $\alpha\beta$ frame, which could include a DSOGI [14], a standard complex coefficient filter (SCCF) [20], or any other prefilter implemented in $\alpha\beta$ frame.
2) $\alpha\beta$ frame equivalent of the filtering action caused due to physical filter or anti-aliasing filter in abc frame.
3) A cascaded combination of the physical filter and prefilter in $\alpha\beta$ frame.

In order to emphasize the main motivation of the paper, the four types of prefiltered PLL's under consideration; LPF-PLL, BPF-PLL, DSOGI-PLL,LPF-DSOGI-PLL along with a PLL with no prefilter but a low pass filter placed inside the control loop (LPF-Inloop-PLL), are subjected to symmetrical grid voltage sag to about 0.1 p.u and recovery. The parameters for the prefilters are typical to 50 Hz supply and is shown in Table I. The PLL control parameters Kp_{pll} and Ki_{pll} are designed such that all the PLL's time-domain performances are equal for a change in the terminal voltage phase. The response of the considered PLL's to the sudden dip in PCC voltage is depicted in Fig. 3. The symmetrical voltage sag is of magnitude 0.1 p.u lasting for 0.1 seconds and a subsequent

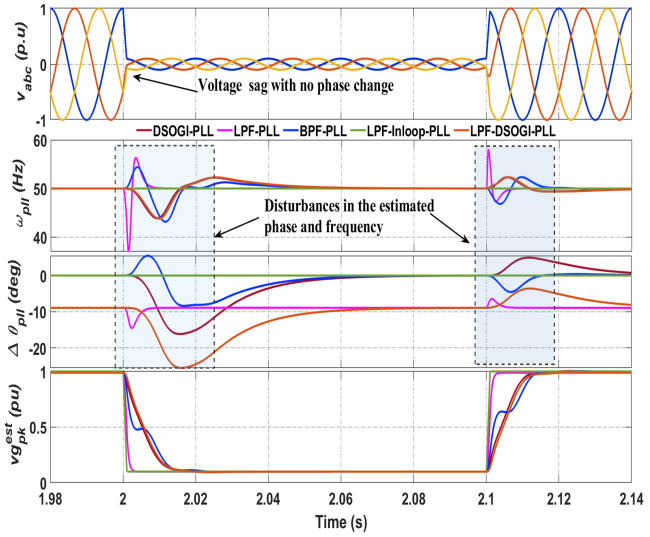

Fig. 3. Comparative simulation results of different prefiltered and inloop filtered PLL under grid voltage magnitude change while keeping the phase constant

recovery to 1 pu, the terminal voltages' phases unchanged for the whole duration.

Ideally, as the name suggests, a PLL is only supposed to respond to a change in the terminal voltage phase. However, as seen from Fig. 3, except for the PLL with a filter placed inside the control loop (LPF-inloop-PLL), all the other three PLL's with prefilters show disturbances in the estimated phase ($\Delta\theta_{pll}$) and frequency (ω_{pll}), with varying degree of differences in performance. Moreover, for the case of a low pass filter in the prefilter stage as in LPF-DSOGI-PLL and LPF-PLL, there is also a steady-state phase error of approximately 10° as seen in Fig. 3. Such responses of the prefiltered PLL during grid faults cannot be explained or accounted for by a conventional linear SISO model. Therefore, to design the PLL's with prefilters and to capture and subsequently reduce the coupling effect of the instantaneous peak voltages and the estimated phase, an improved PLL model has to be developed.

III. PHASE LOCKED LOOP MODELLING

A small signal model of a basic SRF-PLL without filters is well explained in literature [9], [14]. All the variable in the PLL is transformed to rotating refernce frame for ease of analysis due to existence of DC steady state. One must note that the inverter system has two rotating reference frames; a controller d-q frame (dq frame) which is defined by PLL angular velocity ω_{pll} and a system d-q frame (DQ frame) defined by ω_{ref}, which in this paper is the nominal system frequency ω_n. At steady-state condition, both frames rotate in synchronization, but during small-signal perturbations the frames can rotate at different speeds depending on the PLL's tracked angle and speed. The phasor relationship between the variables defined in DQ and dq domain are depicted in Fig. 4. Assuming the voltages are balanced, the PCC voltage can be represented as a vector $\overrightarrow{v}_{abc}$ with a magnitude Vg_{pk} and phase of $\Delta\theta_g$ in DQ frame. The $\Delta\theta_{\text{pll}}$ is the difference in phase of the PLL dq frame and system DQ frame. Henceforth

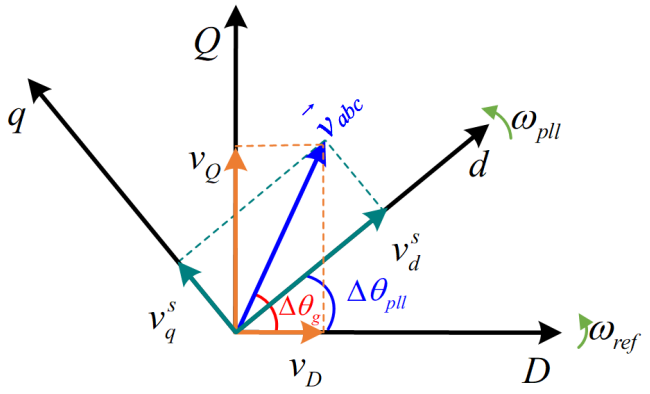

Fig. 4. Phasor relationship between the variables for SRF-PLL without prefilter

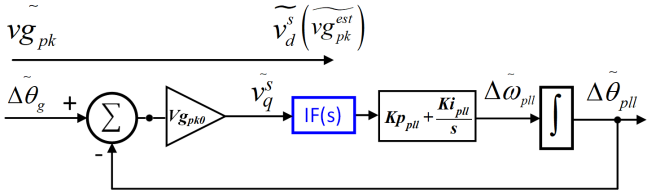

Fig. 5. Linear model of SRF PLL with an in loop filter

in the paper, variables with the symbol $\sim$ represents small perturbed form of the respective variables, also variable with appended 0 represents its steady-state value.

A. PLL's with only inloop filter (IF(s))

The PLL with only inloop filter without a prefilter does not technically exist because there is almost always a physical prefilter present for signal processing $(PF1(s))$, however if the bandwidth of the prefilters is very high, the dynamics of these can be neglected and approximated as a unity gain. Therefore, among the three possible filtering positions in Fig. 1 only $IF(s)$ needs to be considered. Using the phasor diagram shown in Fig. 4 and the Fig. 1, the linearized model of the three phase PLL with an inloop filter around an operating point Vg_{pk0}, $\Delta\theta_{g0}$ can be derived and is shown in Fig. 5. The inputs of this model are $\tilde{vg}_{pk}$ and $\Delta\tilde{\theta}_g$, and outputs are the estimated phase of the terminal voltage $(\Delta\tilde{\theta}_{\text{pll}})$ and $\tilde{vg}_{pk}^{est}$.

As seen from Fig. 5 the linear small signal model of a SRF-PLL with an in loop filter is decoupled for the dynamics of $\tilde{vg}_{pk}$ and $\Delta\tilde{\theta}_g$. The model is simply an extension of the conventional SISO SRF-PLL linear model. The important point to note is that any disturbance in the instantaneous peak voltage will not have an impact on the estimated phase θ_{pll}, this conclusion is also confirmed from the simulation results shown in Fig. 3.

B. PLL's with prefilters (PF1(s) and PF2(s))

In the generalized model of prefiltered SRF-PLL is depicted in Fig. 2. The major challenge in modelling the prefilter PLL is that the control/filter action on the voltages occurs in stationary reference frame as well as synchronous reference frame. This imposes challenges on developing a linear time invariant model, as there is no dc steady-state in the stationary reference frame which is required for modelling the equations in dq reference frame. The methods shown in [21], [22] is used to transform the prefilters represented in frequency domain $(H1(s), H2(s))$ shown in Fig. 2 to its equivalent transfer function $(H1_{DQ}(s), H2_{DQ}(s))$ in the system synchronous rotating reference frame (DQ frame). The synchronous frame equivalent (SFE) transfer function matrix of the prefilter is given by $H_{DQ}(s)$

TABLE II
SYNCHRONOUS FRAME EQUIVALENT TRANSFER FUNCTIONS OF $H1(s)$ AND $H2(s)$

Synchronous frame equivalent transfer function	
Band pass	
$H1_{DQ}(s)$	$\frac{2\,\omega_n\,\zeta\,(2\,\zeta\,{\omega_n}^3+2\,{\omega_n}^2\,s+2\,\zeta\,\omega_n\,s^2+s^3)}{4\,{\omega_n}^4\,\zeta^2+8\,{\omega_n}^3\,s\,\zeta+4\,{\omega_n}^2\,s^2\zeta^2+4\,{\omega_n}^2\,s^2+4\,\omega_n\,s^3\,\zeta+s^4}$
$H2_{DQ}(s)$	$-\frac{2\,{\omega_n}^2\,s^2\,\zeta}{4\,{\omega_n}^4\,\zeta^2+8\,{\omega_n}^3\,s\,\zeta+4\,{\omega_n}^2\,s^2\,\zeta^2+4\,{\omega_n}^2\,s^2+4\,\omega_n\,s^3\,\zeta+s^4}$
Lowpass	
$H1_{DQ}(s)$	$\frac{\tau\,(s+\tau)}{{\omega_n}^2+s^2+2\,s\,\tau+\tau^2}$
$H2_{DQ}(s)$	$\frac{-\omega_n\,\tau}{{\omega_n}^2+s^2+2\,s\,\tau+\tau^2}$
DSOGI	
$H1_{DQ}(s)$	$\frac{k\,\omega_n\,(2\,k\,{\omega_n}^3+4\,{\omega_n}^2\,s+k\,\omega_n\,s^2+s^3)}{2\,k^2\,{\omega_n}^4+2\,k^2\,{\omega_n}^2\,s^2+8\,k\,{\omega_n}^3\,s+4\,k\,\omega_n\,s^3+8\,{\omega_n}^2\,s^2+2\,s^4}$
$H2_{DQ}(s)$	$\frac{k^2\,{\omega_n}^3\,s}{2\,k^2\,{\omega_n}^4+2\,k^2\,{\omega_n}^2\,s^2+8\,k\,{\omega_n}^3\,s+4\,k\,\omega_n\,s^3+8\,{\omega_n}^2\,s^2+2\,s^4}$

$$[H_{DQ}(s)] = \begin{bmatrix} H1_{DQ}(s) & -H2_{DQ}(s) \\ H2_{DQ}(s) & H1_{DQ}(s) \end{bmatrix} \tag{3}$$

where

$$H1_{DQ}(s) = \frac{H1(s-j\omega_{ref})}{2} + \frac{H1(s+j\omega_{ref})}{2} - j\frac{H2(s-j\omega_{ref})}{2} + j\frac{H2(s+j\omega_{ref})}{2} \tag{4}$$

$$H2_{DQ}(s) = j\frac{H1(s-j\omega_{ref})}{2} - j\frac{H1(s+j\omega_{ref})}{2} + \frac{H2(s-j\omega_{ref})}{2} + \frac{H2(s+j\omega_{ref})}{2} \tag{5}$$

The elements of SFE transfer funtion matrix of the prefilters considered in the paper is given in Table. II. For cascaded prefilters such as the LPF-DSOGI-PLL considered in this paper, the synchronous frame equivalent can be found by first obtaining the individual SFE transfer function matrix for each prefilter separately and then multiplying to get the final SFE transfer funtion matrix.

The variables defined in system DQ frame can be rotated to the control frame (dq frame) using transformation matrix $[T_{\Delta dq}]$, for instance

$$[v_{dq}] = [T_{\Delta dq}][v_{DQ}] \tag{6}$$

where

$$[T_{\Delta dq}] = \begin{bmatrix} \cos(\Delta\theta_{pll}(t)) & \sin(\Delta\theta_{pll}(t)) \\ -\sin(\Delta\theta_{pll}(t)) & \cos(\Delta\theta_{pll}(t)) \end{bmatrix} \tag{7}$$

The nonlinear model of prefiltered PLL in rotating reference frame by utilizing the SFE transfer funtion matrix is shown in Fig. 6, the DQ frame voltage of terminal voltages (v_{DQ}) v_D, v_Q are given as input signals to the DQ frame transfer

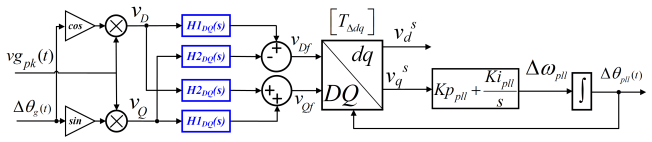

Fig. 6. Non linear model of a general prefiltered PLL in rotating reference frame

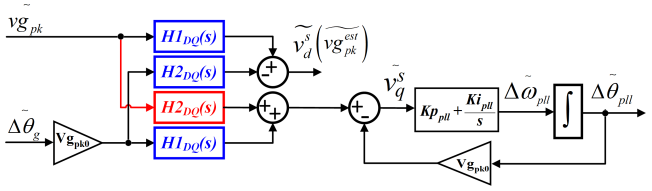

Fig. 7. Linear model of SRF PLL with pre filter

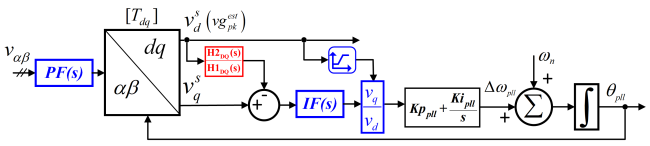

Fig. 8. The general implementation of compensator for a prefiltered PLL

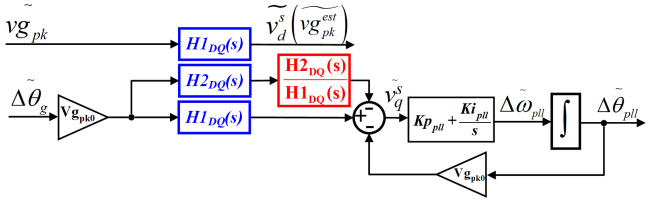

Fig. 9. The simplified linear model of prefiltered PLL including the proposed compensator

function of the prefilter. The non linear model has the inputs as terminal voltage phase $\Delta\theta_{\rm g}$ and instantaneous peak $vg_{pk}(t)$, and outputs are the estimated phase of the terminal voltage $\Delta\theta_{\rm pll}$ and estimated magnitude vg_{pk}^{est}. This non linear model can also be used to extend the loss of synchronization study power converter dominated power systems [15], [23], [24].

The time domain equation of $v_{DQ}(t)$ and subsequently of $v_{dq}(t)$ (vector of v_d^s, v_q^s) can be written as

$$[v_{DQ}(t)]= \begin{bmatrix} vg_{pk}(t)\cos\left(\Delta\theta_{\rm g}(t)\right) \\ vg_{pk}(t)\sin\left(\Delta\theta_{\rm g}(t)\right) \end{bmatrix} \tag{8}$$

$$[v_{dq}^s(t)] = [T_{\Delta dq}]\cdot[[H_{DQ}(t)]*[v_{DQ}(t)]] \tag{9}$$

where the asterisk $*$ denotes the convolution operation, and dot $\cdot$ denotes multiplication. The linearized model can be derived by finding the first order approximation of Eq. (9) around an operating point Vg_{pk0}, $\Delta\theta_{g0}$, $\Delta\theta_{pll0}$.

$$\begin{bmatrix} \tilde{v}_d^s & \tilde{v}_q^s \end{bmatrix}^T = [Cl(s)]\begin{bmatrix} \tilde{v}g_{pk} & \Delta\tilde{\theta}_g & \Delta\tilde{\theta}_{pll} \end{bmatrix}^T \tag{10}$$

where

$$Cl(s) = \begin{bmatrix} H1_{DQ}(s) & -Vg_{pk0}H2_{DQ}(s) & 0 \\ H1_{DQ}(s) & Vg_{pk0}H2_{DQ}(s) & Vg_{pk0} \end{bmatrix} \tag{11}$$

Using (10) and the non linear model shown in Fig. 6 the linearized model of the prefiltered PLL as shown in Fig. 7 can be derived. Unlike a PLL with only inloop filter where $\tilde{v_q}$ was decoupled from $\tilde{vg_{pk}}$, in prefiltered PLL, $\tilde{vg_{pk}}$ is coupled to $\tilde{v_q^s}(s)$ via $(H2_{DQ}(s))$ as shown in 7. This coupling effect can be significant during the large disturbances in PCC voltage for some PLL's with prefilter, but it is usually ignored in the existing PLL models. It is also important for controller design as the underlying couplings is evident as opposed to a SISO model of the PLL. The MIMO model helps us in designing an efficient controller and thus ensures a better time domain performance, especially when there is a simultaneous large disturbances in both terminal voltage magnitude and phase as in the case of power system faults. The MIMO model also allow us to capture the disturbances in estimated phase of prefiltered PLL's for a symmetrical disturbance in the PCC voltage.

IV. Proposed Control to Reduce Coupling

In this section a supplementary control structure is proposed to reduce the coupling between the phase and instantaneous peak of the terminal voltage. The coupling effect is highlighted in Fig. 7, the obvious choice for a perfect decoupling would be to include a inverse based controller which inverts the plant dynamics, which in this case is the transfer function matrix $H_{DQ}(s)$. However, the computational burden associated with such a controller can be extremely high as it involves inverting the MIMO transfer function matrix. Moreover, such controls will also overturn the advantages of using a prefilter such as harmonic. Hence, for practical purpose, a pure inverse based controller may not be desirable in this case.

Based on the insights derived from the linearized model and also from the characteristics of DQ equivalent frequency response of the common prefilters, a compensator of the same order as the respective prefilter transfer functions shown in Table. I is proposed. The approach followed is to make the forward path gain from $\tilde{v}g_{pk}$ to the input of the PI control to zero, which is achieved with the addition of a compensator $(\frac{H2_{DQ}(s)}{H1_{DQ}(s)})$ as shown in Fig. 8. The compensator is realizable for any filter type as long as the filter types have no non minimum phase behaviour. The decoupling effect of the addition of compensator can be cleary seen from Fig. 9, which depicts the linearized model of the PLL with prefilter. The compensator types for the prefilters considered in this paper is shown in Table. III. To test the effectiveness of the compensator, the study shown in Fig. 3 is repeated with added compensator, the parameters of the prefilter remained the same as in Table. I. As anticipated, the disturbance in peak voltage did not have any effect on the estimated phase and frequency of the PLL with prefilter as shown in Fig. 10. Furthermore, the steady-state phase offset caused due to a first order low pass filter as the prefilter is also eliminated by the use of compensator.

The paper's focus is on PLL response and compensation for balanced voltage dips and phase jump. Nevertheless, the feasibility of the proposed compensator is also investigated in an unbalanced sag case. Among the considered PLL, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the

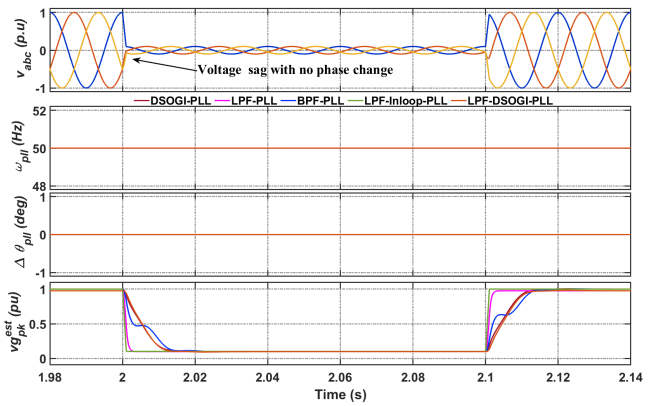

Fig. 10. Simulation results of prefiltered PLL's with the proposed supplimentay compensator for grid voltage magnitude change while keeping the phase constant

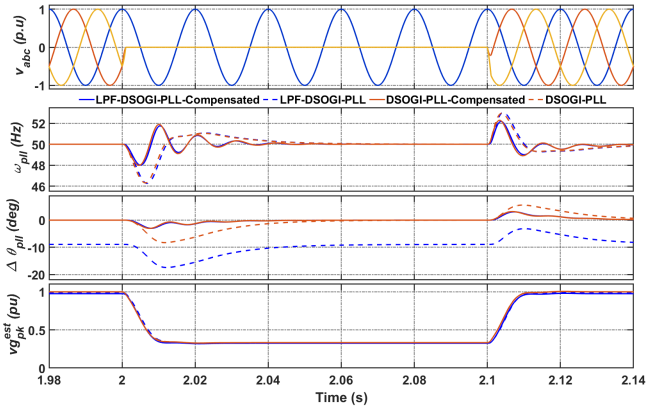

Fig. 11. Simulation results of DSOGI-PLL and LPF-DSOGI-PLL with and without compensation for unbalanced grid voltage sag while keeping the phase constant

negative sequence voltage generated by unbalanced sag [9]. Therefore the results for unbalanced cases are only demonstrated on those two PLL's against PCC volage sag typical for Double line to ground fault while keeping the phase constant. The results of the unbalanced sag study is shown in Fig. 11. It can be seen that the compensation reduces the disturbance in estimated phase and frequency of the PLL as well as it removes any steady state error caused due to low pass filter in LPF-DSOGI-PLL.

The procedure for obtaining the compensator for any prefiltered PLL is summarized below for readers convenience

1) Convert to generalized representation as in Fig. 2 and obtain transfer functions $H1(s), H2(s)$.
2) Obtain the (SFE) transfer function matrix components $H1_{DQ}(s), H2_{DQ}(s)$ using algebraic combination of frequency shifted $H1(s), H2(s)$ as shown in eqn (4) and (5)
3) The compensator is $\frac{H2_{DQ}(s)}{H1_{DQ}(s)}$ and its generalized implementation is shown in Fig. 8.

V. SIMULATION RESULTS

A simulation study of the three prefilter types and its compensation was carried out to verify the advantages of

TABLE III
THE TRANSFER FUNCTIONS OF THE PROPOSED COMPENSATORS

$\mathrm{Pr}\,efilter\mathrm{Type}$	$Compensator$
$Bandpass$	$-\frac{\omega_n\, s^2}{2\,\zeta\,\omega_n{}^3+2\,\omega_n{}^2\, s+2\,\zeta\,\omega_n\, s^2+s^3}$
$Lowpass$	$-\frac{\omega_n}{s+\tau}$
$DSOGI$	$\frac{k\,\omega_n{}^2\, s}{2\,k\,\omega_n{}^3+4\,\omega_n{}^2\, s+k\,\omega_n\, s^2+s^3}$

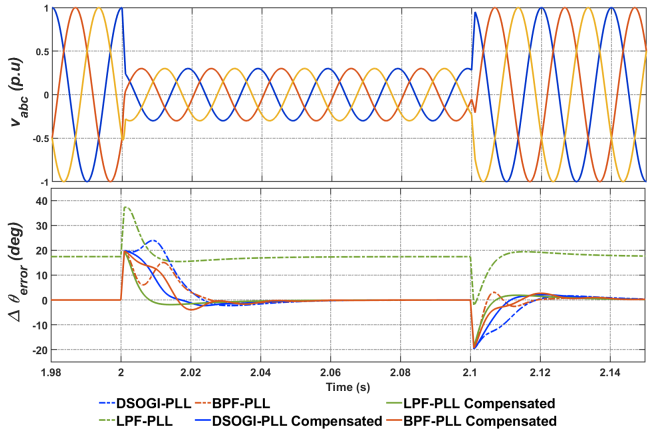

Fig. 12. Simulation results for a dip in positive sequence voltage magnitude for 100 ms duration accompanied by a positive phase jump of 15°

the proposed compensation. To ensure a fair design, all the three PLL's were designed to have 2 cycle settling time while limiting the overshoot to 10%. The design was carried out using the linear model derived in the previous section. The control parameters of a PLL type was retained when compensation was added. It should be noted that, as the PLLs as the PLL input voltage magnitude coupling is eliminated with the proposed compensator, control performance can be improved. To simulate symmetrical fault, we considered a positive sequence voltage sag to 0.3 p.u for 100 ms duration accompanied by a positive phase jump of 15°. The positive effects of compensation is evident from the results shown in Fig. 12. The net error in estimated angle of the PLL and the actual angle ($\Delta\theta_{error}$=$\theta_{pll} - \theta_g$) is reduced. To further quantify the impact of compensation, a normalized root mean square (NRMS) of $\Delta\theta_{error}$ is computed for all the PLL types considered with varying level of voltage dip and phase jump. The NRMS of $\Delta\theta_{error}$ for a PLL under a input phase jump of θ_{fault} during the period of fault related dynamics is defined by

$$NRMS\Delta\theta_{error} = \frac{\sqrt{\frac{1}{T2-T1}\int_{T1}^{T2}\Delta\theta_{error}(t)^2}}{\overline{\theta_{fault}}} \qquad (12)$$

where T1 is the fault initiation time and T2 is two cycles after the fault clearing time when all dynamics of induced by the fault is settled. The NRMS of $\Delta\theta_{error}$ is computed by running the time domain simulation for a dip in positive sequence voltages for a period of 100 ms, a phase jump is

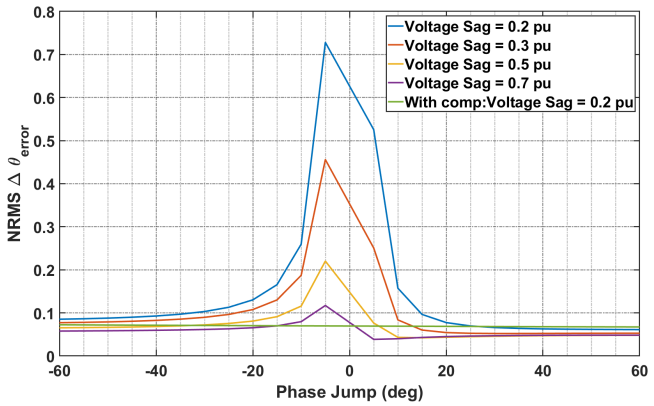

Fig. 13. NRMS of $\Delta\theta_{error}(deg)$ during variable voltage sag and simultaneos phase jump for 100 ms period for BPF PLL

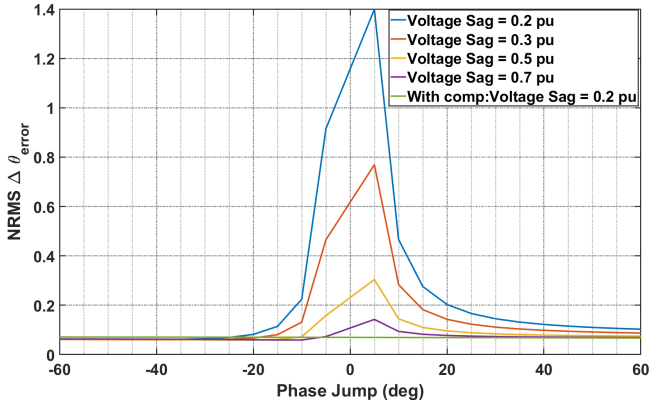

Fig. 14. NRMS of $\Delta\theta_{error}(deg)$d during variable voltage sag and simultaneous phase jump for 100 ms period for DSOGI PLL

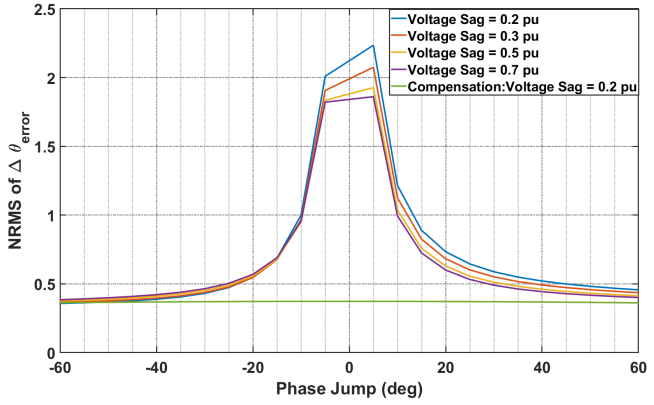

Fig. 15. NRMS of $\Delta\theta_{error}(deg)$d during variable voltage sag and simultaneous phase jump for 100 ms period for LPF-DSOGI-PLL

also accompanied with this dip. It can be seen from Fig. 13-15 that the net error in estimated phase for all uncompensated PLL's is dependent on the magnitude of dip in voltage where as a compensation makes NRMS of $\Delta\theta_{error}$ independent of the voltage dip. The NRMS is not relevant for LPF prefilter as the phase shift introduced is constant regardless of the dip in voltage.

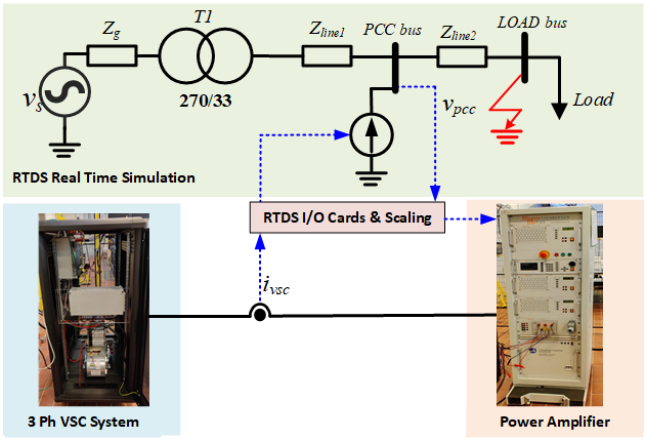

Fig. 16. Power hardware in the loop test

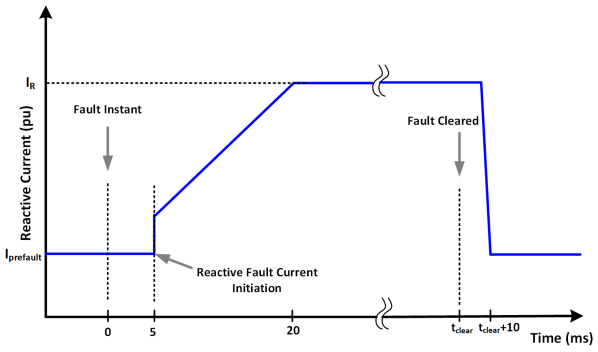

Fig. 17. The positive sequence fault current reference

VI. Power Hardware In The Loop Results

The proposed compensation and MIMO modeling can be applied in any grid-connected converter system which employs a prefiltered PLL for grid frequency and phase detection for protection and control. One of the applications where the advantage of the PLL compensation is inherently visible is to enable fast fault current injection effectively. The grid codes expect that the PE resources quickly inject as much reactive current to the system to ensure the satisfactory protective relay system operation [6], [7]. The protection system in the high voltage grid requires a sufficient amplitude of fault current in the first 20-30 ms after the fault to operate correctly. Further, the fault level contribution from PEIPS (PE connected equipment) mitigates the severity of maximum voltage depression seen by other assets (especially more distant from the fault). It can prevent tripping due to under-voltage protection and help keep the power system stable. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system.

The advantages of using proposed compensation for pre-filtered PLL is confirmed through power hardware in the loop (PHIL) simulation. The PHIL test setup is shown in Fig. 16. The setup includes a simplified power system model implemented in Real-Time Digital Simulator (RTDS), RTDS I/O cards, two-level VSC hardware which is a SEMIKRON SkiiP stack with inductive filter, and current and voltage

TABLE IV
PHIL SCALING FOR THE VSC HARDWARE

Symbol	Description	Physical Value	Scaled to Simulation
V_{vsc}	Amplifier voltage	100 V	33kV
I_{vsc}	VSC Current	7A	150 A
P_{vsc}	VSC power	2 kVA	5 MVA

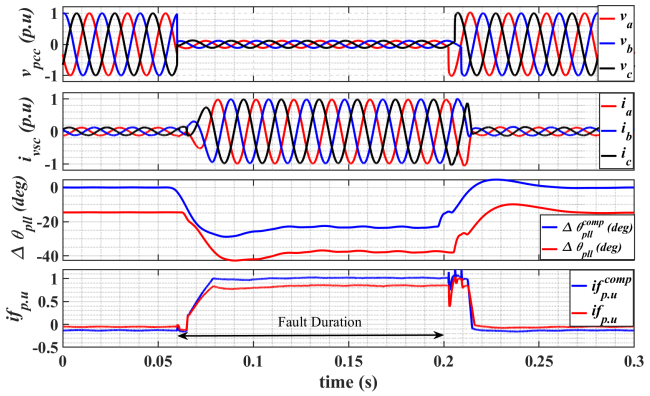

Fig. 18. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a low pass filter as prefilter and its compensation

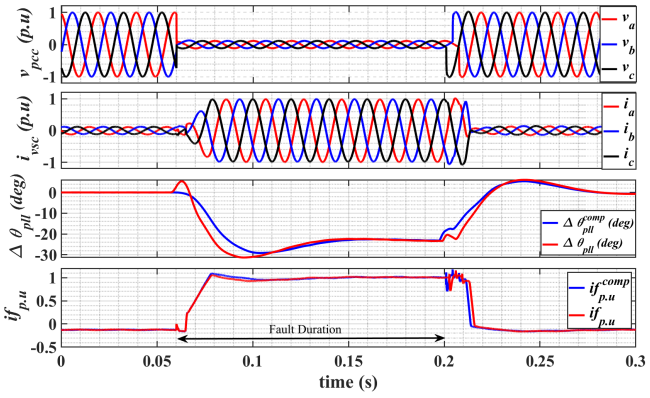

Fig. 19. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a 50 Hz BPF prefilter and compensation

sensors, a 2.5 kVA SPITZENBERGER SPIES PAS 2500 linear amplifier. The VSC switching frequency is set to 10 kHz, and the inductive filter for the VSC stack is 8 mH. The I/O cards exchange the PCC voltage from RTDS and current coming into the RTDS between the amplifier and the PCC. This exchange ensures that the VSC is part of the power system network. The voltage and current signal between the RTDS and the hardware is scaled, and the scaling is shown in Table. IV. The current feedback signal is conditioned with a first order low pass filter with a time constant of 250 μs to eliminate noise and ensure the PHIL simulation's stability.

The VSC control system, including the current control and the PLL's discussed in the paper and their compensation strategies, are implemented on a FPGA based digital controller from National Instruments (NI). The PLL's are set to track the amplifier voltage phase, which is the simulated PCC bus's

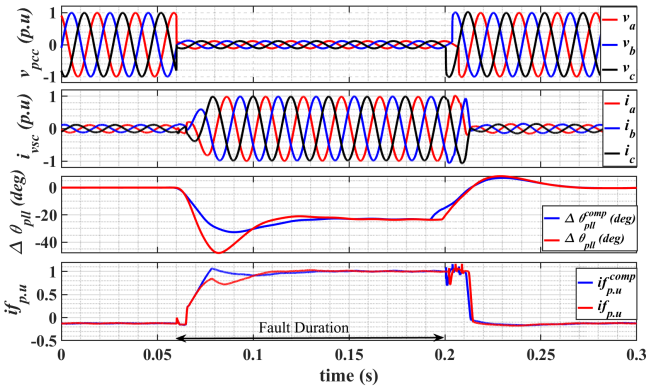

Fig. 20. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a DSOGI prefilter and compensation

scaled voltage. The sampling time for the control loop is 40 μs. The controller is discretized using the trapezoidal method. The fault reactive current reference is as shown in Fig. 17. The reactive reference fault current is initiated 5 ms after the fault instant. The reference rate is limited to 1 pu in a cycle during the fault current initiation stage. The PLL compensation performance is then evaluated first for a symmetrical fault with a fault impedance of 0.2 ohm at the load bus. The VSC performance with and without compensation for balanced fault is shown in Fig. 18-20. All the plots captured in the NI controller and RTDS interface is exported to MATLAB and replotted for enhanced clarity. The plots for three-phase PCC voltage and the injected three-phase current is shown only for compensated case. The fault reactive current at the PCC without compensator($if_{p.u}$) and with compensator ($if_{p.u}^{comp}$) are found by scaling the reactive power measured at the PCC with the PCC voltage and dividing by base current (150 A) in real-time simulation. The PLL estimated phase of the terminal voltage with and without compensator $\Delta\theta_{pll}, \Delta\theta_{pll}^{comp}$ are captured in NI controller.

Fig. 18, shows the VSC's response for balanced fault equipped with a fist order low pass filter, with a time constant of 1 ms. The first order low pass filter, albeit with a low time constant, introduces a phase delay of $17.4\,\mathrm{deg}$ at the fundamental frequency. This open-loop delay also results in a difference in the required reactive current injected and the measured reactive current at the PCC bus, as depicted in Fig. 18. The open-loop delay and the resulting difference in fault current are eliminated using the proposed PLL compensation. Fig. 19 and Fig. 20 depicts VSC's balanced fault response with BPF and DSOGI prefilter as well as the response with proposed compensation. The reactive current injected in the prefilter compensated cases are closer to the reference reactive current because the compensation decouples the dynamics of voltage magnitude from the measured phase.

Among the PLL's considered in the paper, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the negative sequence voltage generated by unbalanced sag [9]. Therefore the results for unbalanced sag cases are only demonstrated on those two PLL's against Double line to ground fault at the load bus. During unbalanced fault, a balanced reactive current

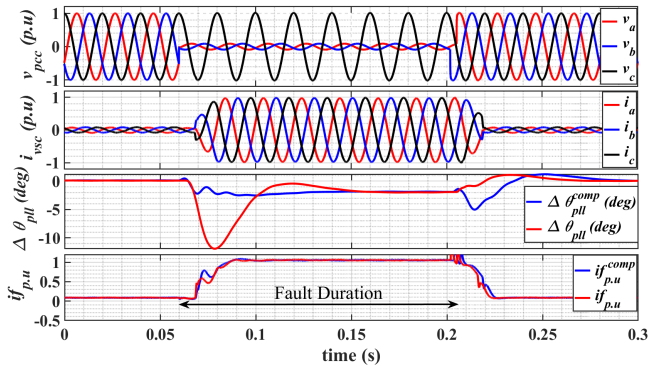

Fig. 21. Results from PHIL study of the VSC under under double line to ground fault case, for a PLL with a DSOGI prefilter and compensation

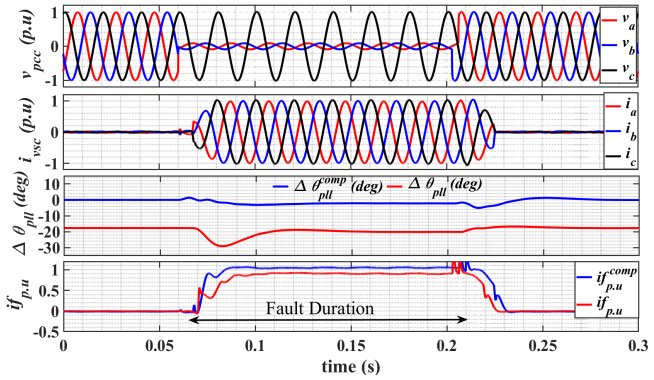

Fig. 22. Results from PHIL study of the VSC under double line to ground fault case, for a PLL with a cascaded LPF and DSOGI prefilter and compensation

injection strategy is utilized in this paper, the positive sequence reactive fault current reference is as shown in Fig. 17. Fig. 21 shows the VSC's output with DSOGI-PLL during double line to ground fault. It can be seen that the compensation reduces the disturbance in the estimated PLL phase (θ_{pll}). However, the difference between the estimated phases for compensated and uncompensated case is not significant in this case. Therefore the injected reactive current during compensated and uncompensated cases are similar. Fig. 22 depicts the results of the VSC with LPF-DSOGI-PLL under double line to ground fault. The low pass filter in the LPF-DSOGI-PLL introduces a phase delay, which is compensated with the use of the proposed compensator. Therefore the reactive current injected in the prefilter compensated cases are closer to the reactive reference current and better cater to the grid requirements.

This application example of reactive fault current injection by VSC demonstrates the advantage of the proposed compensation.

VII. Conclusion

The fast detection of the PCC voltage phase is necessary for power electronic-based resources to comply with reactive current injection requirements during a fault. It is well known that the three-phase balanced ac voltages can be represented by two instantaneous quantities, namely, the peak of the voltages and its phase angle. During symmetrical fault, there is a large disturbance in both these quantities. In this paper, it is shown that during a fault in the power system, the traditionally used SISO model cannot capture the complete dynamics of the PLL with a prefiltering stage. The paper proposes a non-linear MIMO model of a general prefiltered PLL, which during a power system fault more accurately captures the transients of prefiltered PLL. The developed non-linear model of the prefiltered PLL depicts the undesirable coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. The paper proposes a compensator to reduce this coupling, and the prefiltered PLL is made to act only on changes in the phase of PCC voltage. The proposed compensator is demonstrated with three commonly used prefiltered PLL's and on a cascaded prefilter case to show the effectiveness. The proposed control ensures an accurate current phase control and injection during faults to fulfill fault ride-through requirements.

Appendix

A. Test power system parameters

$Zg = 0.054 + j0.54; Z_{line1} = 1.691 + j3.3929; Z_{line2} = .1691 + j.34$; Load=5 MW; Transformer T1 leakage reactance=10% at 100 MVA base

Acknowledgment

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References

[1] X. Tian, Y. Chi, W. Wang, G. Li, H. Tang, and Z. Wang, "Transient characteristics and adaptive fault ride through control strategy of DFIGs considering voltage phase angle jump," *Journal of Modern Power Systems and Clean Energy*, DOI 10.1007/s40565-016-0251-2, 2017.

[2] M. H. H. Musa, L. Fu, Z. He, and Y. Lei, "Faulty phase identification for transmission line with metal oxide varistor-protected series compensator," *Journal of Modern Power Systems and Clean Energy*, 2020.

[3] B. Wang and L. Jing, "A protection method for inverter-based microgrid using current-only polarity comparison," *Journal of Modern Power Systems and Clean Energy*, vol. 8, no. 3, pp. 446–453, 2019.

[4] J. Jia, G. Yang, and A. H. Nielsen, "A Review on Grid-Connected Converter Control for Short-Circuit Power Provision under Grid Unbalanced Faults," *IEEE Trans. Power Deliv.*, DOI 10.1109/TPWRD.2017.2682164, 2018.

[5] J. Jia, G. Yang, A. H. Nielsen, and V. Gevorgian, "Investigation on the Combined Effect of VSC-Based Sources and Synchronous Condensers under Grid Unbalanced Faults," *IEEE Trans. Power Deliv.*, DOI 10.1109/TPWRD.2019.2914342, 2019.

[6] NERC, "Reliability guideline: Bps-connected inverterbased resource performance," Atlanta, GA,, Tech. Rep., Sept 2018.

[7] *ENTSO-E Connection Codes Implementation Guidance Documents, ENTSO-E*, Nov. 2016. [Online]. Available: https://consultations.entsoe.eu/system-development/entso-e-connection-codes-implementationguidance-d-3/

[8] "Performance improvement of a prefiltered synchronous-reference-frame PLL by using a PID-type loop filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3469–3479, 2014.

[9] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase plls: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.

[10] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 434–452, 2018.

[11] M. S. Reza, F. Sadeque, M. M. Hossain, A. M. Ghias, and V. G. Agelidis, "Three-phase pll for grid-connected power converters under both amplitude and phase unbalanced conditions," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8881–8891, 2019.

[12] J. Matas, M. Castilla, J. Miret, L. G. de Vicuña, and R. Guzman, "An adaptive prefiltering method to improve the speed/accuracy tradeoff of voltage sequence detection methods under adverse grid conditions," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2139–2151, 2013.

[13] X. Quan and A. Q. Huang, "Pi-based synchronous reference frame frequency-locked loop," *IEEE Trans. Ind. Electron.*, 2020.

[14] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, 2013.

[15] S. Ma, H. Geng, L. Liu, G. Yang, and B. C. Pal, "Grid-Synchronization Stability Improvement of Large Scale Wind Farm During Severe Grid Fault," *IEEE Trans. Power Syst.*, vol. 33, no. 1, pp. 216–226, 2017.

[16] J. Zhao, M. Huang, H. Yan, C. K. Tse, and X. Zha, "Nonlinear and Transient Stability Analysis of Phase-Locked Loops in Grid-Connected Converters," *IEEE Trans. Power Electron.*, vol. 36, DOI 10.1109/TPEL.2020.3000516, no. 1, pp. 1018–1029, 2021.

[17] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "Linear Time-Periodic Modeling, Examination, and Performance Enhancement of Grid Synchronization Systems with DC Component Rejection/Estimation Capability," *IEEE Trans. Power Electron.*, vol. 36, DOI 10.1109/TPEL.2020.3018584, no. 4, pp. 4237–4253, 2021.

[18] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "All-pass-filter-based pll systems: linear modeling, analysis, and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3558–3572, 2019.

[19] S. Golestan, E. Ebrahimzadeh, B. Wen, J. M. Guerrero, and J. C. Vasquez, "Dq-Frame Impedance Modeling of Three-Phase Grid-Tied Voltage Source Converters Equipped with Advanced PLLs," *IEEE Trans. Power Electron.*, vol. 36, DOI 10.1109/TPEL.2020.3017387, no. 3, pp. 3524–3539, 2021.

[20] M. Ramezani, S. Golestan, S. Li, and J. M. Guerrero, "A Simple Approach to Enhance the Performance of Complex-Coefficient Filter-Based PLL in Grid-Connected Applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5081–5085, 2018.

[21] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 601–610, 2001.

[22] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2239–2248, 2007.

[23] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2014.2334665, no. 1, pp. 310–321, 2015.

[24] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "An Overview of Assessment Methods for Synchronization Stability of Grid-Connected Converters under Severe Symmetrical Grid Faults," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9655–9670, 2019.

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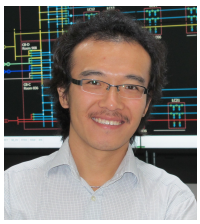

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