Harmonic Voltage Control in Distributed Generation Systems Using Optimal Switching Vector Strategy

Lakshmi Srinivas Vedantham, *Member, IEEE*, Bhim Singh, *Fellow, IEEE*, Sukumar Mishra, *Senior Member, IEEE* and Lie Xu, *Senior Member, IEEE*

***Abstract*- With increased penetration of renewable power and the nonlinear loads in the distributed generation (DG) systems, increased power quality concerns are exhibited, especially the challenges associated with the current and voltage harmonics in the system. Various conventional harmonic compensation techniques are developed for *voltage-controlled* DG inverters in past, majority involve either multiple proportional-integral (PI) or proportional-resonant (PR) controllers in eliminating grid current harmonics. The *current-controlled* inverters, on the other hand, are not preferred in industrial applications, accounting to their wide variations in the switching frequency. A novel and adaptive harmonic-voltage control is developed here, for *voltage-controlled* DG inverters, which neither uses any PI regulators, nor imposes stability issues associated with non-ideal implementation of infinite gains of PR controllers. Interestingly, the developed control logic can be used for DG inverters, both in grid connected and off-grid operational modes. Furthermore, this strategy allows network operator to be used as an additional supplement that can be enabled/disabled as per the network requirement. The control logic exploits the property of optimal-switching-vector (OSV) controller i.e. accurate output voltage tracking. Simulations results demonstrate the effectiveness of the controller, to suppress grid current harmonics and load voltage harmonics in grid-interfaced and off-grid modes respectively, ultimately satisfying the mandatory IEEE standard-1547. Experimental results verify the viability of the controller for practical applications.**

***Index Terms*- Distributed generation, harmonics, power quality, OSV Control and voltage source inverter (VSI).**

I. INTRODUCTION

An increased dissemination of distributed energy resources (DERs) has led to shift in paradigm toward the decentralized generation of electricity. The energy industry is moving into a new era of smart grids, which encourage distributed generation systems with reliable, resilient and responsive control structure [1]. The smart grid concept encourages decentralized network structure that enhances reliability and performance of the grid, reduces undesirable environmental impacts by incorporating renewable energy sources and facilitates customer-operator-power producer real time interactions [2]. To promote future resilient power grids with flexible control structure, different power quality standards are formulated. In many practical applications, the distributed power network contains a substantial number of harmonics when nonlinear loads located in the network. These background harmonics make the output current of grid-connected inverter distorted, which imposes difficulty in satisfying the stringent grid standards, such as IEEE 519 and IEEE 1547-2018 [3].

Different research work are reported in the past decade for power quality improvement in grid interfaced DERs, both for single-phase and three-phase DERs. These are broadly classified into two categories- selective methods for harmonic mitigation [4-7] and non-selective methods [8-12]. The selective harmonic mitigation techniques generally use multiple proportional-integral (PI) regulators in rotating frame, individually for each harmonic, thereby involving dq-transformations. Some methods like [4], [7] use multiple resonant controllers at fundamental frequency and harmonic frequencies, either in stationary or rotating frame. In the selective harmonic compensation control for harmonic current rejection, the reference currents are modified to provide information about the prominent harmonics present in the load current. These methods are computationally more intensive and are sensitive to variations in system fundamental frequency. Moreover, commonly used proportional-resonant (PR) controllers or PI controllers are based on harmonic compensators to eliminate the steady-state error and compensate selective grid harmonics. In such cases, the current loop needs a wide enough bandwidth to cover the resonant frequencies of controller. Otherwise, the system may become unstable [12]. Moreover, these resonant filters designed for a particular frequency, can accurately compensate harmonics only with a known utility grid frequency. In the case of varying the grid frequency, the tracking performance of the current is degraded. Thus, variable grid frequency can contribute to significant performance degradation of the harmonic mitigation for grid interactive systems.

The non-selective approaches generally use hysteresis controllers [8-10], dead-beat controllers [11] and the repetitive controllers [12-13]. The power quality improvement in the distribution system using the hysteresis current control techniques are widely reported, which have used indirect current control technique, where the grid current is controlled by feeding only the fundamental component of local load currents. For instance, in [8-10], the local load currents are sensed and the fundamental component of the load current is extracted, and accordingly the reference grid currents are generated. The reference grid currents are compared with the grid currents and passed through hysteresis current controller. These algorithms are successful in achieving harmonic current elimination; however, the PCC load current measurements are not readily available all the time. Moreover, the use of hysteresis indirect current control is undesirable accounting to its variable switching frequency. A comprehensive review of different harmonic mitigation techniques, is reported in [14].

In majority, industrial applications, therefore, hysteresis current controllers are avoided, and prefer reference voltage based pulse width modulated inverters [9], [15]. However, in

voltage-controlled inverters, in order to modify the inverter reference voltages to include harmonic reference voltages, the conventional methods employ multiple PR controllers. For example, He *et. al.* [16] have used the cascaded voltage and current control schemes for harmonic output voltage control in DG based systems with multiple proportional resonant (PR) controllers for different harmonics, to establish harmonic output voltage control, which is computationally intensive. The system performance with PR-controllers is degraded under variation of the system frequency as it provides infinite gain at selected harmonic frequencies. The non-ideal implementation of infinite gains could cause series of instability issues for grid interfaced DG systems [17].

To overcome these issues, in this paper, a harmonic controller for three phase voltage-controlled inverter is contemplated. Contrast to the conventional harmonic current control techniques, this new strategy is capable of being appended in any voltage-controlled inverter system, without causing stability issues. It means that the harmonic compensation algorithm becomes a subset of any voltage-reference driven inverter systems, and it is possible to be switched-on or switched-off at the convenience of the operator. This controller facilitates direct harmonic voltage control, where it neither uses cascaded voltage/current control loops nor PI/PR regulators. It uses OSV controller [18], which is based on finite future samples of input. It explicitly uses the system model to produce control action that describes the desired system behaviour. Thus, the OSV controller for power electronic device, facilitates easier practical implementation. Here, the system identification is performed in a certain way by modelling the system through state-space equations, thereafter, transforming the continuous state space model to discrete domain. Model identification serves in estimating the future control samples. Out of the future samples thus computed, only the first prediction is applied to the plant. After predicting the future control samples, a minimization criterion is used to generate the control signal. Different minimization criteria for OSV controller are described in [19] and this paper uses quadratic cost function minimization to compute the future control samples. The OSV controller for voltage-controlled inverters, has been used in the past research work [20-22], where the output voltages of an inverter, are strictly governed by the minimization criterion, however, this property is not fully explored for reference harmonic voltage injection. This work explores this property to formulate a generalized algorithm, which voluntarily injects harmonic grid voltages, to improve power quality in the grid connected and off-grid distributed generation systems.

Effectiveness of this new strategy is demonstrated through various simulation results, in both grid connected and off-grid modes of operation. The experimental validation is then performed through dSPACE-1202 micro-lab-box controller interface. The total harmonic distortion (THD) in the grid currents in grid-interfaced operation are well within the limits prescribed by the IEEE standard-1547 grid code.

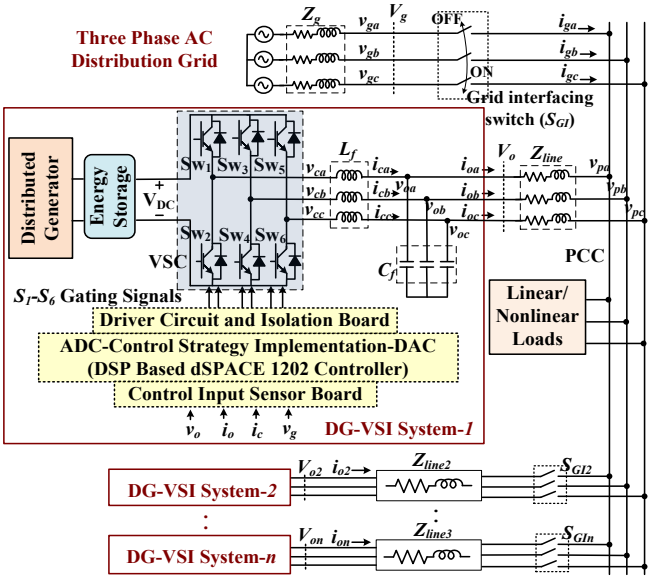


Fig. 1 System Configuration

II. System Description and Modelling

The system configuration is as shown in Fig. 1. The system simulation and experimental parameter specifications are reported in Appendix-A and Appendix-B, respectively. The DG output filter ('L_f' and 'C_f' in Fig. 1) design procedure is described in Appendix-C. The dynamic equations relating to the filter inductance and capacitance, are expressed as follows,

$$L_f \frac{d}{dt}\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} = \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} - \begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix}; \quad C_f \frac{d}{dt}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} - \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \quad (1)$$

In (1), 'L_f' represents the filter inductance and 'C_f' represents the filter capacitance, as indicated in Fig. 1. The dynamics in (1) are expressed in terms of inverter voltages (v_{ca}, v_{cb}, v_{cc}), filter inductor currents (i_{ca}, i_{cb}, i_{cc}), filter output voltages (v_{oa}, v_{ob}, v_{oc}) and filter output currents(i_{oa},i_{ob}, i_{oc}). These dynamics are further expressed in $\alpha\beta$ reference frame by means of Clarke's transformation depicted as,

$$\mathbf{u}_{\alpha\beta} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\mathbf{u}_{abc} \quad (2)$$

where, $\mathbf{u}_{\alpha\beta}$ is vector in $\alpha\beta$ reference frame and $\mathbf{u}_{abc}$ is vector in *abc* reference frame. Transformed dynamic equations are identified as follows,

$$L_f \frac{d\mathbf{i}_c}{dt} = \mathbf{v}_c - \mathbf{v}_o; \; C_f \frac{d\mathbf{v}_o}{dt} = \mathbf{i}_c - \mathbf{i}_o \quad (3)$$

The vectors '$\mathbf{i}_c$', '$\mathbf{v}_c$', '$\mathbf{i}_o$' and '$\mathbf{v}_o$' in (3) are as follows,

$$\mathbf{v}_c = \begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix}, \mathbf{i}_c = \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix}, \mathbf{v}_o = \begin{bmatrix} v_{o\alpha} \\ v_{o\beta} \end{bmatrix} \text{ and } \mathbf{i}_o = \begin{bmatrix} i_{o\alpha} \\ i_{o\beta} \end{bmatrix} \quad (4)$$

The formulation in (3) is represented as state-space model,

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}_v\bar{\mathbf{v}}_c + \mathbf{B}_i\bar{\mathbf{i}}_o \quad (5)$$

The '$\mathbf{x}$', '$\bar{\mathbf{v}}_c$' and '$\bar{\mathbf{i}}_o$' are the vectors expressed in terms of '$\mathbf{i}_c$', '$\mathbf{v}_c$', '$\mathbf{i}_o$' and '$\mathbf{v}_o$' as,

$$\mathbf{x}=\begin{bmatrix}\mathbf{i}_c\\ \mathbf{v}_o\end{bmatrix};\ \bar{\mathbf{v}}_c=\begin{bmatrix}\mathbf{v}_c\\ \mathbf{0}_{2\times1}\end{bmatrix};\ \bar{\mathbf{i}}_o=\begin{bmatrix}\mathbf{0}_{2\times1}\\ \mathbf{i}_o\end{bmatrix} \tag{6}$$

Moreover, the matrices '**A**', '$\mathbf{B}_v$' and '$\mathbf{B}_i$' in (5) are as follows,

$$\mathbf{A}=\begin{bmatrix}\mathbf{0}_{2\times2} & -\left(1/L_f\right)\mathbf{I}_2\\ \left(1/C_f\right)\mathbf{I}_2 & \mathbf{0}_{2\times2}\end{bmatrix};$$
$$\mathbf{B}_{\mathbf{v}}=\begin{bmatrix}-\left(1/L_f\right)\mathbf{I}_2 & \mathbf{0}_{2\times2}\\ \mathbf{0}_{2\times2} & \mathbf{0}_{2\times2}\end{bmatrix};\ \mathbf{B}_{\mathbf{i}}=\begin{bmatrix}\mathbf{0}_{2\times2} & \mathbf{0}_{2\times2}\\ \mathbf{0}_{2\times2} & \left(1/C_f\right)\mathbf{I}_2\end{bmatrix} \tag{7}$$

It may be noted in (6) and (7), that the matrix '$\mathbf{0}_{m\times n}$' represents a zero matrix with 'm' rows and 'n' columns, while '$\mathbf{I}_m$' represents an identity matrix of size 'm'.

III. CONTROL APPROACH

The control algorithm for the voltage source inverter is described here. The OSV controller takes the reference values of filter output voltages as its inputs and outputs the required switching sequence for VSI switches to produce desired filter output voltages.

A. OSV Controller

Consider a system shown in Fig. 1, the dynamic behavior of filter inductor and filter capacitor is identified from (1). The corresponding state-space representation is given by (4). The discrete time model of (4), is identified as follows,

$$\mathbf{x}(k+1)=\mathbf{A}_z\mathbf{x}(k)+\mathbf{B}_{vz}\bar{\mathbf{v}}_c(k)+\mathbf{B}_{iz}\bar{\mathbf{i}}_o(k) \tag{8}$$

where, 'k' represents the sampling instant, and the matrices '$\mathbf{A}_z$', '$\mathbf{B}_{vz}$' and '$\mathbf{B}_{iz}$' are discretized form of the matrices '**A**', '$\mathbf{B}_v$' and '$\mathbf{B}_i$' respectively, given by,

$$\mathbf{A}_z=e^{\mathbf{A}T_s},\ \ \mathbf{B}_{vz}=\int_0^{T_s}e^{\mathbf{A}\tau}\mathbf{B}_v d\tau,\ \ \mathbf{B}_{iz}=\int_0^{T_s}e^{\mathbf{A}\tau}\mathbf{B}_i d\tau \tag{9}$$

Here, 'T_s' is the sampling time. In this context, $e^{\mathbf{A}T_s}\approx1+\mathbf{A}T_s$ approximation holds true as 'T_s' is a small quantity (of the order of *micro seconds*). Thus, are predicted values of currents and voltages can be written as,

$$\mathbf{i}_c(k+1)=\mathbf{i}_c(k)+\left(T_s/L_f\right)\left(\mathbf{v}_c(k)-\mathbf{v}_o(k)\right) \tag{10}$$

$$\mathbf{v}_o(k+1)=\mathbf{v}_o(k)+\left(T_s/C_f\right)\left(\mathbf{i}_c(k)-\mathbf{i}_o(k)\right) \tag{11}$$

The filter output current '$\mathbf{i}_o$' depends on load connected at the filter output. The capacitor voltages- (11) is expressed for $(k+2)^{th}$ instant as,

$$\mathbf{v}_o(k+2)=\mathbf{v}_o(k+1)+\left(T_s/C_f\right)\left(\mathbf{i}_c(k+1)-\mathbf{i}_o(k)\right) \tag{12}$$

This is also represented as follows,

$$\mathbf{v}_o(k+1)\equiv E\left(z^{-1}\right)\mathbf{v}_o(k)+F\left(z^{-1}\right)\mathbf{v}_c(k)+H\left(z^{-1}\right)\mathbf{i}_c(k)+G\left(z^{-1}\right)\mathbf{i}_o(k) \tag{13}$$

In (13), 'z^{-1}' represents a backward time-shift operator. The polynomials '$E(z^{-1})$', '$F(z^{-1})$', '$G(z^{-1})$', '$H(z^{-1})$' in (13) are as,

$$E\left(z^{-1}\right)=1-\left(T_s^2/L_fC_f\right)z^{-1};\ \ F\left(z^{-1}\right)=\left(T_s^2/L_fC_f\right)z^{-1}$$
$$G\left(z^{-1}\right)=\left(-T_s/C_f\right)z^{-1}\ \ ;\ \ H\left(z^{-1}\right)=\left(T_s/C_f\right)z^{-1} \tag{14}$$

The set of future finite control samples is then estimated by extending (13). The estimates of the output voltages are thus obtained as,

$$\mathbf{v}_o(k+n)=A\left(z^{-1}\right)\mathbf{v}_o(k)+N_p.B\left(z^{-1}\right)\mathbf{v}_c(k)+H\left(z^{-1}\right)\left[\sum_{j=1}^{n}\mathbf{i}_c(k+j-1)\right]+N_p.G\left(z^{-1}\right)\mathbf{i}_o(k) \tag{15}$$

Here, (15) is computed for $n=1,2,...N_p$, where 'N_p' is the prediction horizon. Depending on how far ahead the model needs to be predicted, accordingly the prediction horizon is chosen (three prediction samples are considered here). Thus, the vector of future estimates of filter output voltages can be represented as,

$$\hat{\mathbf{V}}_o=\begin{bmatrix}\mathbf{v}_o(k+1) & \mathbf{v}_o(k+2) & . & . & \mathbf{v}_o(k+N_p)\end{bmatrix}^T \tag{16}$$

The future control samples of capacitor current i.e. $\mathbf{i_c}(k)$, $\mathbf{i_c}(k+1)$,..$\mathbf{i_c}(k+N_p-1)$, are computed in parallel to the future estimates of output voltages. From (15), the future estimates (16) are expressed as,

$$\hat{\mathbf{V}}_o=\mathbf{E}.\mathbf{v}_o(k)+\mathbf{F}.\mathbf{v}_c(k)+\mathbf{H}.\mathbf{I}_c+\mathbf{G}.\mathbf{i}_o(k) \tag{17}$$

Here, '**E**' is a matrix of size '$N_p\times1$' with all entries as '$E(z^{-1})$' and '**H**' is a lower triangular matrix with elements '$H(z^{-1})$'. The rest of vectors, '**F**', '**G**' and '$\mathbf{I_c}$' in (17) are as,

$$\mathbf{F}=\begin{bmatrix}F\left(z^{-1}\right) & 2F\left(z^{-1}\right) & . & . & N_pF\left(z^{-1}\right)\end{bmatrix}^T$$
$$\mathbf{G}=\begin{bmatrix}G\left(z^{-1}\right) & 2G\left(z^{-1}\right) & . & . & N_pG\left(z^{-1}\right)\end{bmatrix}^T \tag{18}$$
$$\mathbf{I}_c=\begin{bmatrix}\mathbf{i}_c(k) & \mathbf{i}_c(k+1) & . & . & \mathbf{i}_c(k+N_p-1)\end{bmatrix}^T$$

The objective of OSV control is to force future samples to track the reference output voltages (v_{oa}^{ref}, v_{ob}^{ref}, v_{oc}^{ref}) depicted in Fig. 2. The reference output voltages (v_{oa}^{ref}, v_{ob}^{ref}, v_{oc}^{ref}), are considered as a sum of primary reference voltages (v_{oa}^{p}, v_{ob}^{p}, v_{oc}^{p}), and the harmonic-compensating reference voltages (v_{oa}^{c}, v_{ob}^{c}, v_{oc}^{c}), as shown in Fig. 2. The primary reference voltages are fundamental reference-voltage components, which are obtained in state-of-art control techniques for DG systems, and these are reported rich in literature. This is not the focus of present work; and the grid-interfaced and off-grid control strategy for obtaining primary reference voltages depicted in [23] is directly employed in this work for obtaining the primary reference voltages. The procedure for obtaining primary reference voltages, is therefore reported in [23] in both grid-connected and off-grid systems. The generation of harmonic reference voltages and the capability of OSV controller in tracking the harmonic reference voltages are illustrated in later subsections. The succeeding stage following evaluation of the future samples, is the predictive control, which generates optimal switching sequences resulting in the minimum error between predicted voltages (17) and the voltage references, as depicted in Fig. 2. A minimization function using quadratic minimization criterion, is used to minimize the error between the both, which takes the following general form,

$$M_{GPC}=\mathbf{e}^T(k)R_1(k)\mathbf{e}(k) \tag{19}$$

Here, 'M_{GPC}' is the minimization function, 'R_1' is a square matrix signifying the weights of individual vector elements, and '**e**(k)' is the error vector given by,

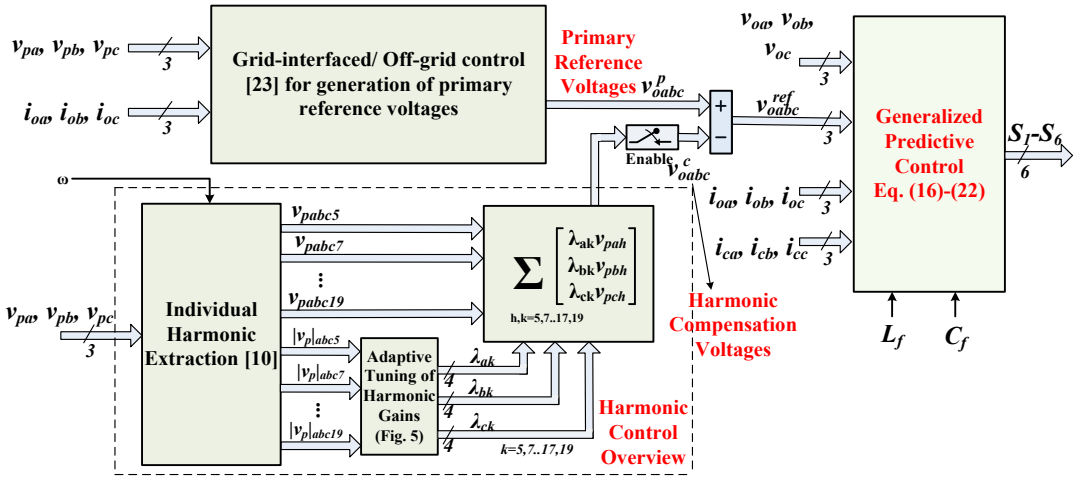


Fig. 2 Control schematic of harmonic-voltage controller

$$\mathbf{e}(k)=[v_{o\alpha}^{ref}(k+1)-v_{o\alpha}(k+1),v_{o\beta}^{ref}(k+1)-v_{o\beta}(k+1),$$
$$v_{o\alpha}^{ref}(k+2)-v_{o\alpha}(k+2),v_{o\beta}^{ref}(k+2)-v_{o\beta}(k+2), \quad (20)$$
$$\ldots v_{o\alpha}^{ref}(k+N_p)-v_{o\alpha}(k+N_p),v_{o\beta}^{ref}(k+N_p)-v_{o\beta}(k+N_p)]^T$$

where, $v_{o\alpha}^{ref}$ and $v_{o\beta}^{ref}$ are the $\alpha\beta$-components of the reference output voltages (v_{oa}^{ref}, v_{ob}^{ref}, v_{oc}^{ref}). For simplicity, the weights of individual vector elements in 'R_1' are considered unity and thus the minimization criterion can be re-written as,

$$M_{GPC}=\sum_{i=1}^{N_p}e_\alpha^2(k+i)+\sum_{i=1}^{N_p}e_\beta^2(k+i) \quad (21)$$

where,

$$e_\alpha(k+i)=v_{o\alpha}^{ref}(k+i)-v_{o\alpha}(k+i)$$
$$e_\beta(k+i)=v_{o\beta}^{ref}(k+i)-v_{o\beta}(k+i) \quad (22)$$

A limit on converter over-currents is imposed by incorporating an additional constraint in (21) in terms of change in VSI output currents and assigning appropriate weights to them. However, more reliable method for limiting the over currents during abnormal conditions, is by incorporating a nonlinear function (w_{oc}) in the minimization criterion as below [18],

$$M_{GPC}=\sum_{j=1}^{N_p}\left[e_\alpha^2(k+j)+e_\beta^2(k+j)\right]+w_{oc}(k)$$
$$w_{oc}(k)=\begin{cases}0 & \text{if } |i_{c\alpha}(k+j)|,\ |i_{c\beta}(k+j)|\Big|_{for\ j=1\ to\ N_f}<i_{max}\\ \infty & \text{Otherwise}\end{cases} \quad (23)$$

In (23), 'i_{max}' is the maximum limit of the VSI currents and 'N_f' is the total number of future inductor current samples of attention. By imposing this maximum limit, the voltage vectors ($\mathbf{v}_c$), which produce a current magnitude greater than 'i_{max}' add large penalty to the minimization criterion and thus they are not selected. On other hand, zero-penalty is imposed as long as the current magnitude is lesser than its maximum limit. The overall OSV control schematic is depicted in Fig. 3. Subsequent to this, the seven possible VSI output voltages ($\mathbf{v}_c$) are then identified as,

$$\mathbf{v}_c=(2V_{DC}/3)\left(S_a+S_b\mathbf{a}+S_c\mathbf{a}^2\right);\ \mathbf{a}=e^{i(2\pi/3)} \quad (24)$$

where S_a, S_b and S_c are the gating signals for VSI. From Fig.1, the state 'S_a=1' can be understood as a state where 'Switch-Sw_1 is ON and the Switch-Sw_2 is OFF' corresponding the first leg of VSI, and vice-versa when 'S_a=0'. Similarly 'S_b=1' implies 'Sw_3 is ON and Sw_4 is OFF' and 'S_c=1' implies 'Sw_5 is ON and Sw_6 is OFF'. Table-I highlights the seven possible voltage vectors generated by (24), corresponding to seven switching states (SS_1-SS_6 and SS_0). Out of these voltage vectors, the gating sequence with least minimization function (23) is applied to VSI, to ensure perfect track references v_{oa}^{ref}, v_{ob}^{ref}, v_{oc}^{ref} tracking.

TABLE I
POSSIBLE SWITCHING VECTORS WITH (24)

Switching State	$\mathbf{v}_{c\alpha}$ (Real part of (24))	$\mathbf{v}_{c\beta}$ (Imaginary part of (24))
SS_1	$-V_{DC}/3$	$-V_{DC}/\sqrt{3}$
SS_2	$-V_{DC}/3$	$V_{DC}/\sqrt{3}$
SS_3	$-2V_{DC}/3$	0
SS_4	$2V_{DC}/3$	0
SS_5	$V_{DC}/3$	$-V_{DC}/\sqrt{3}$
SS_6	$V_{DC}/3$	$V_{DC}/\sqrt{3}$
SS_0	0	0

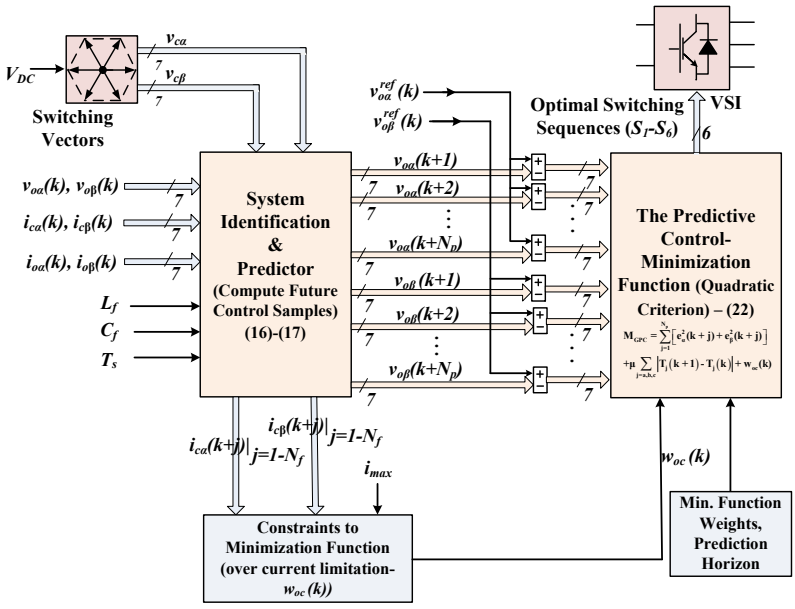
B. Harmonic Voltage Control Strategy

The aforementioned OSV controller formulation serves two purposes. Firstly, it eliminates the rigorous tuning of PI regulator parameters. Secondly, it provides a way to directly control the DG output voltages. It directly monitors and adjusts the reference output voltages (v_{oa}^{ref}, v_{ob}^{ref}, v_{oc}^{ref}), by including harmonic output voltages. The harmonics are intentionally injected in DG output voltages to control DG harmonic currents. The harmonic voltage tracking capability of OSV control and its advantages, are illustrated in this sub-section.

Consider the system operation in GI-mode shown in Fig. 4. To eliminate the harmonics in load, the DG harmonic voltages are controlled as per PCC harmonic voltages ('v_{pah}') as,

$$v_{oah}=-\lambda_a v_{pah};\ v_{obh}=-\lambda_b v_{pbh};\ v_{och}=-\lambda_c v_{pch} \quad (25)$$

where, 'λ_a', 'λ_b' and 'λ_c' are gains corresponding to harmonics of individual phases. The harmonic currents are identified as,



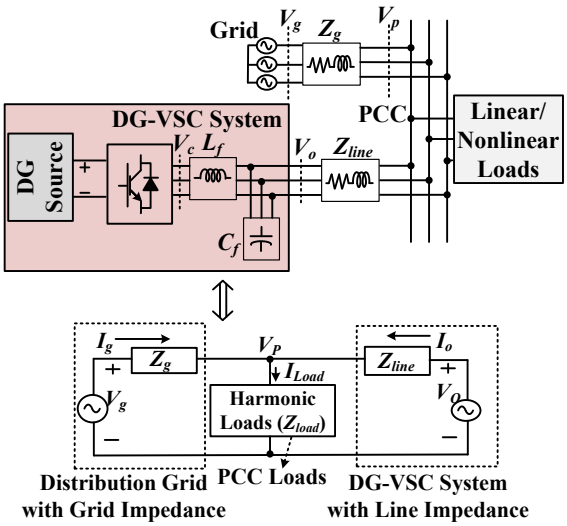


Fig. 3 (Left) The OSV control schematic; Fig. 4 (Right) Equivalent circuit of single DG-VSI system in grid-interfaced mode

$$i_{oah} = \left(v_{pah} - v_{Oah}\right)/Z_{lineh} \tag{26}$$

From (25) and (26),

$$i_{oah} = \left(1+\lambda_a\right)v_{pah}/Z_{lineh} \tag{27}$$

From (27), it can be noticed that, by altering 'λ_a', the harmonic impedance (i.e. 'v_{pah}/i_{oah}') is significantly changed. Therefore, 'λ_a', 'λ_b' and 'λ_c' can be controlled to vary harmonic impedances of phases 'a', 'b' and 'c', respectively. Raising 'λ' value implies less harmonic impedance by DG than the grid. In this way, the grid harmonic currents can be substantially minimized. This harmonic voltage control is accommodated in by including 'harmonic voltage control' block in Fig. 2. The 'harmonic compensation' block produces the compensation harmonic voltages (v^c_{oabc}), when added to the (v^p_{oabc}), form the reference voltages (23) for OSV. The adaptive observer based harmonic cancellation technique [10] is used here in the 'individual harmonic extraction' block in Fig. 2, employs this algorithm. This is briefly depicted here, as follows. For individual harmonics extraction, the voltage (v_{pa}) at PCC and nonlinear load currents (i_L), are written as,

$$\begin{aligned} v_{pa} &= V_{pa1c}\sin(\omega_1 t) + V_{pa1s}\cos(\omega_1 t) + \\ &\quad ... + V_{pakc}\sin(\omega_k t) + V_{paks}\sin(\omega_k t) \end{aligned} \tag{28}$$

where,

$$V_{pa1c} = V_{pa1}\cos(\delta_1), V_{pa2c} = V_{pa2}\cos(\delta_2), ..., V_{pakc} = V_{pak}\cos(\delta_k)$$
$$V_{pa1s} = V_{pa1}\sin(\delta_1), V_{pa2s} = V_{pa2}\sin(\delta_2), ..., V_{paks} = V_{pak}\sin(\delta_k)$$

The harmonic order is represented by 'k'. The quantities V_{pak}, ω_k and δ_k denote amplitude of the k^{th} harmonic, its angular frequency and the corresponding phase shift, respectively. Following the procedure outlined in [10], the harmonic voltages are estimated as,

$$\begin{aligned} &\dot{\hat{V}}_{pa1c} = \Upsilon_{1c}\tilde{E}_{pa}\sin(\omega_1 t), \dot{\hat{V}}_{pa1s} = \Upsilon_{1s}\tilde{E}_{pa}\cos(\omega_1 t), ... \\ &..., \dot{\hat{V}}_{pakc} = \Upsilon_{kc}\tilde{E}_{pa}\sin(\omega_1 t), \dot{\hat{V}}_{pa1s} = \Upsilon_{ks}\tilde{E}_{pa}\cos(\omega_1 t) \end{aligned} \tag{29}$$

where, $\Upsilon_{1c}, \Upsilon_{1s}, \Upsilon_{2c}, \Upsilon_{2s}, \ldots, \Upsilon_{kc}, \Upsilon_{ks}$ are the adaptive weights [10] and $\hat{V}_{pa1c}, \hat{V}_{pa1s}, \ldots \hat{V}_{pakc}, \hat{V}_{paks}$ are the estimates of fundamental and harmonic voltages, and $\tilde{E}_{pa}$ is difference between measured and estimated voltages. Then, the PCC voltage harmonics are computed as [10],

$$\begin{aligned} V_{pak} &= \hat{V}_{pakc}\sin(\omega_k t) + \hat{V}_{paks}\cos(\omega_k t) \\ \left|V_{pak}\right| &= \sqrt{\hat{V}^2_{pakc} + \hat{V}^2_{paks}} \end{aligned} \tag{30}$$

The phase signals of each of the individual harmonic components are then amplified by harmonic gain (Fig. 2). The harmonic compensation also involves harmonic gains tuning. The flowchart for tuning harmonic gains is as in Fig. 5. The step values (μ_a, μ_b, μ_c) are adaptively varied whenever the grid harmonic content increases, especially when it exceeds the

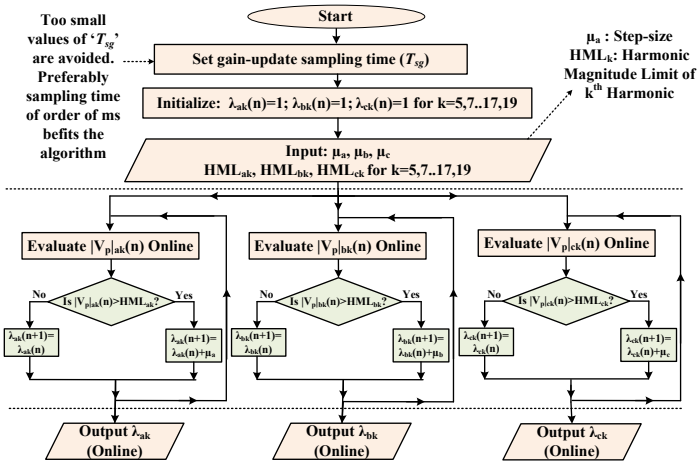


Fig. 5 Algorithm for online tuning of harmonic gains - λ_{ak}, λ_{bk} and λ_{ck}

harmonic magnitude limit (HML). The HML is set as per the IEEE standard 1547-2018 (with maximum 8% THD). the gain-update sampling time (T_{sg}) is preferably much larger than the control sampling time. The critical step size, above which the harmonic-gain update algorithm diverges, can be derived as $|i_{Lah}||Z_{lineh}|/|v_{pah}|$. All these parameters are depicted in Appendix-A. The same control strategy is employed in stand-alone mode of operation to suppress the load harmonic voltages. These features are demonstrated in detailed in the simulation results.

IV. Simulation and Experimental Results

The modeling and simulation of the system are executed in MATLAB/Simulink using sim-scape toolbox. A three legged IGBT based VSI is considered herein. A three phase 208V, 50Hz distribution grid is considered for interfacing purpose. The system is depicted in Fig.1, with R=1 for single DG-VSI based system and R=2 for double DG-VSI based system. The system specification and the parameters of the controller used for simulation purpose, are stated in Appendix-A.

A. Controller Tracking Performance of Output Voltages

This subsection highlights the output voltage tracking efficiency of the controller. The reference voltage tracking capability of the OSV controller is shown in Fig. 6. A grid interfaced single DG-VSI system supplying a nonlinear load (≈3kVA) is considered. Initially, the grid current THD is considerably high, accounting to the nonlinear loads in the system. The harmonic control switch (depicted in Fig. 2) is enabled at 0.9s. The DG output voltage of 'a'-phase (v_{oa}), its corresponding reference value (v_{oa}^{ref}) and the tracking error between both, are highlighted in Fig. 6. Fig. 6(a) depicts the main simulation window with salient control signals of v_{oa}^{ref}, v_{oa}, tracking error (v_{oa}^{ref}-v_{oa}), THD of v_{oa} and the THD of i_{ga}. Fig. 6(b) depicts the tracking performance of the controller before enabling the harmonic control switch, while Fig. 6(c) depicts the tracking performance after enabling the harmonic control switch. Both before and after enabling harmonic voltage control, perfect tracking of v_{oa} is observed exactly as per v_{oa}^{ref} as seen in Fig. 6(b) and Fig. 6(c). The tracking error is maintained well below 5%, as observed in the third panel of Fig. 6(a). The OSV controller, therefore, accommodates the filter dynamics within itself, to provide precise output voltage tracking capability. Further reduction in tracking error is possible through an increase in prediction horizon (N_p) of the controller, however, at the cost of increased computational burden. It can be observed that, upon enabling the harmonic voltage control block, the DG output voltages are adjusted to minimize the harmonic currents (caused due to nonlinear loads) entering the grid, by voluntarily injecting the DG output voltage harmonics to the primary DG output voltages references (v_{oabc}^{p}). Consequently, the DG output harmonic voltages are increased from 2.2% to 8.3%, while the harmonic currents entering the grid are reduced to 3.2% to satisfy the IEEE Std. 1547. Moreover, the effectiveness of the OSV controller in controlling harmonic output voltages and harmonic grid currents can be observed from last two panels of Fig. 6(a).

Upon enabling the harmonic control switch, the dynamics in the internal signals of the harmonic voltage controller are reported in Fig. 7. The salient internal signals are reported in a sequence, corresponding to the 'harmonic compensation' block in Fig. 2. Fig. 7(a) and Fig. 7(b) highlight the individual harmonic components derived from 'individual harmonic extraction' block of Fig. 2. For the sake of simplicity, only the harmonic components corresponding to 5th, 7th, 11th and 13th

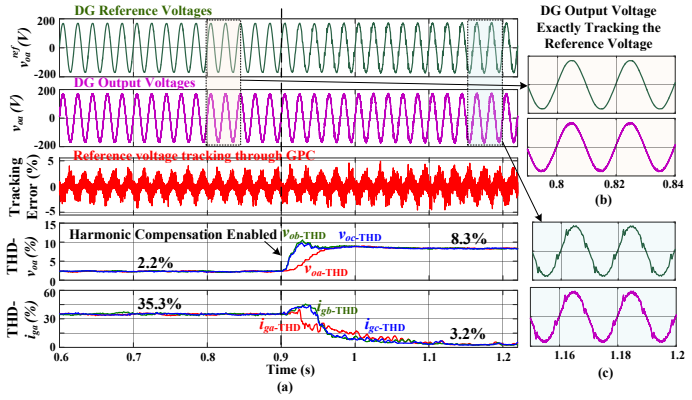


Fig. 6 (a) Output voltage tracking capability of OSV controller; (b-c) DG reference and output voltages (zoomed view), before and after enabling the harmonic compensation algorithm

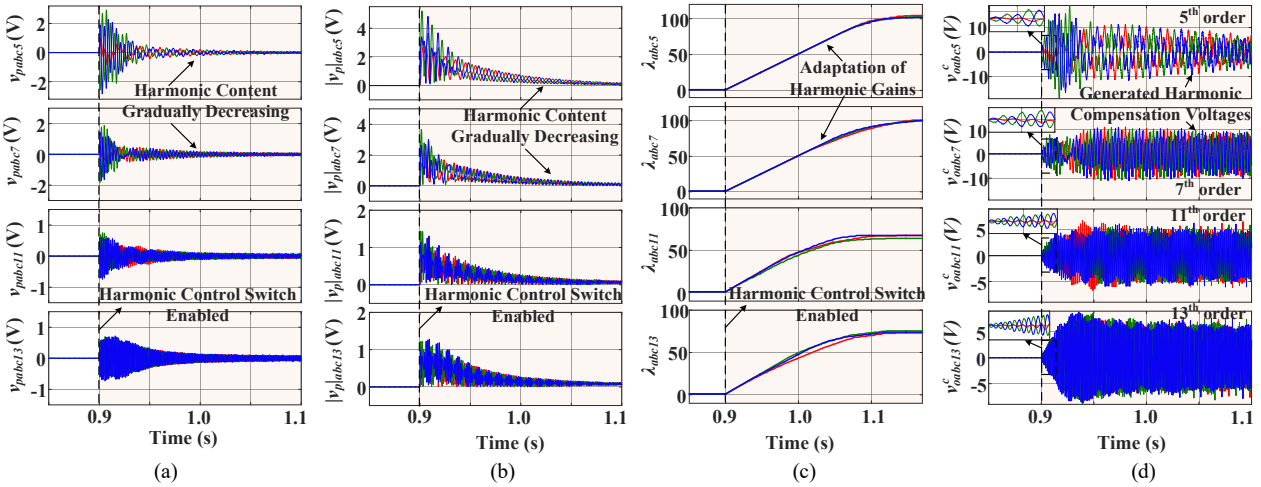


Fig. 7 Salient internal signals of the harmonic voltage controller upon enabling the harmonic control switch (a) v_{pabc5}, v_{pabc7}, v_{pabc11} and v_{pabc13}; (b) $|v_p|_{abc5}$, $|v_p|_{abc7}$, $|v_p|_{abc11}$ and $|v_p|_{abc13}$; (c) λ_{pabc5}, λ_{pabc7}, λ_{pabc11} and λ_{pabc13}; (d) v^c_{abc5}, v^c_{abc7}, v^c_{abc11} and v^c_{abc13}

harmonics are reported, where the signals v_{pabc5}, v_{pabc7}, v_{pabc11} and v_{pabc13} are highlighted in Fig 7(a) with their corresponding magnitudes in Fig. 7(b). Upon enabling the harmonic control switch at 0.9s, it is observed that the harmonic content in the PCC voltages gradually decreases with time as observed in Fig. 7(a) and Fig. 7(b). This is due to the adaptation of the harmonic gains (i.e. λ_{abc5}, λ_{abc7}, λ_{abc11} and λ_{abc13}) in the controller, as depicted in Fig. 7(c). It can be seen that, as the adaptation process of the harmonic gains saturates, the harmonic content of the PCC voltage harmonics are diminished gradually within the prescribed HML. The individual harmonic compensation voltages generated in this process are reported in Fig. 7(d). The sum of these individual harmonic compensation voltages is the reference harmonic compensation voltage (i.e. v^{c}_{oabc}), as reported in the first panel of Fig. 8. The generated primary reference voltage (i.e. v^{p}_{abc}) are highlighted in the second panel of Fig. 8. Finally, the net reference voltages (i.e. v^{ref}_{oabc}) are shown in the third panel of Fig. 8. Thus, upon enabling the harmonic control switch, the net reference voltages are successfully adapted in accordance with the harmonic content in PCC voltage, as observed from the zoomed panels in Fig. 8. The reference voltages, thus produced, are the inputs to the generalized predictive control based OSV controller (as seen in Fig. 2).

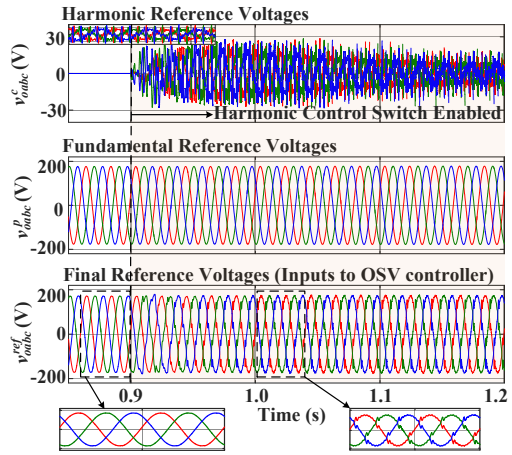


Fig. 8 Reference voltages generated by the harmonic voltage controller

The salient internal signals of the OSV controller are reported in Fig. 9, with the harmonic control switch enabled at 0.9s. Fig. 9(a) highlights the salient signals of '$v_{o\alpha\beta}$', '$i_{o\alpha\beta}$', '$v_{c\alpha\beta}$' corresponding to the switching vector 'SS_1' and also the '$v_{o\alpha\beta}$' of the immediate next sampling instant generated with switching vector 'SS_1'. The error ('e_α') corresponding to the '$v_{o\alpha\beta}$' of the next sampling instant with the switching vector 'SS_1' is depicted in the first panel of Fig. 9(b). The corresponding values of minimization functions with the 'SS_1', are highlighted in the second panel of Fig. 9(b). The minimization functions with other switching vectors 'SS_2-SS_6' and 'SS_0' are also shown in Fig. 9(b) and Fig. 9(c). The minimum of all these minimization function values, is the optimal minimization function value ($M_{GPC|Opt}$), which is reported in Fig. 10. The optimal switching sequences (*i.e.* gating pulses) thus generated, are also highlighted in Fig. 10.

B. Harmonic Control in Grid Connected and Off-Grid Modes

Fig. 11 depicts the performance of the single DG-VSI system with a nonlinear load (≈3kVA). The performance with the conventional control [23], without harmonic voltage control, is reported in Fig. 11(a),while Fig. 11((b) highlights the system performance with the presented harmonic voltage control. The performance is shown in terms of DG output voltages (v_o), PCC voltages (v_p), load currents (i_L), grid currents (i_g) and VSI currents (i_o).The grid impedance (Z_g) and DG impedance (Z_{line}) are set to '0.2+0.5j Ω'. As it can be seen in Fig. 11(a), without the harmonic voltage control the grid current is contaminated with significant harmonics. However, these harmonics are eliminated with the harmonic control, since the DG output harmonic voltages are automatically adjusted as observed in the first panel of Fig. 11(b). The corresponding THD values in bar-graph representation are reported in Fig. 12. The PCC voltage and grid current THD values are observed as high as 6.2% and 35.3%, respectively, without presented harmonic

compensation strategy. However, these values are regulated to 2.94% and 3.17%, respectively, with harmonic voltage control. Since the DG output voltages are controlled rigidly by the OSV controller through the action of the minimization function (22), the harmonics in DG output voltage are precisely controlled to compensate for the harmonic currents

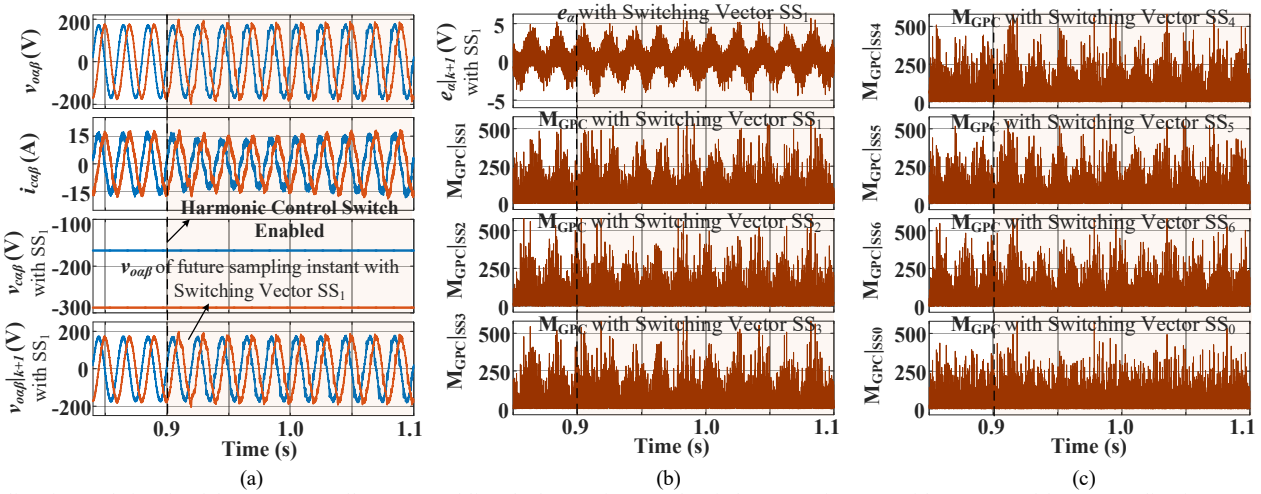


Fig. 9 Salient internal signals of the OSV controller upon enabling the harmonic control switch (a) $v_{o\alpha\beta}$, $i_{o\alpha\beta}$, $v_{c\alpha\beta}$ with SS_1, $v_{o\alpha\beta}$ of future sampling instant with SS_1; (b) 'e_α' of future sampling instant with SS_1, M_{GPC} with SS_1, SS_2 and SS_3; (c) M_{GPC} with SS_4, SS_5, SS_6 and SS_0

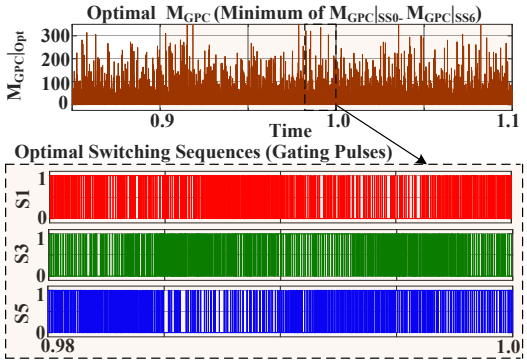


Fig. 10 Optimal minimization function and the corresponding switching sequences generated by the OSV controller

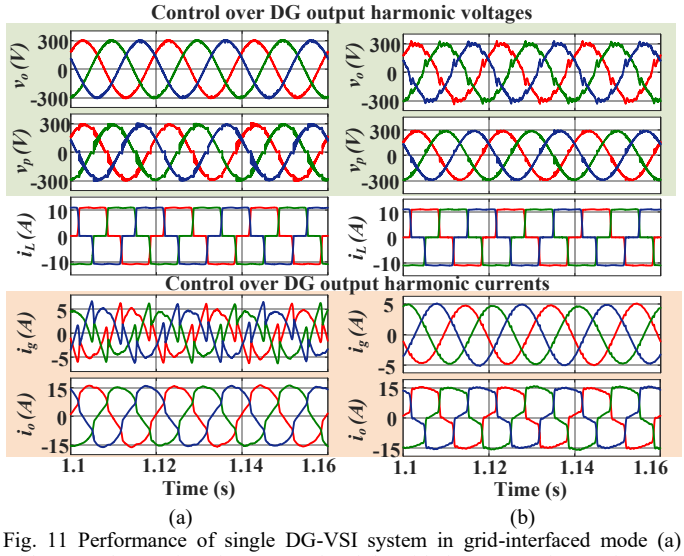


Fig. 11 Performance of single DG-VSI system in grid-interfaced mode (a) without any harmonic voltage control and (b) with the presented control

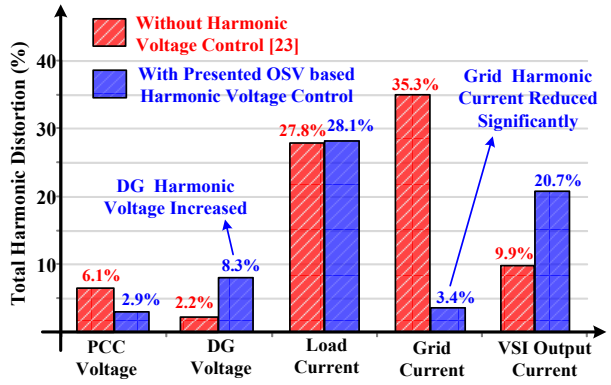


Fig. 12 THD Values of Grid-Interfaced DG-VSI System with and without Harmonic Control

entering the grid. For the same reason, higher DG output voltage THD (8.31%) is observed high with harmonic voltage control, and the PCC voltage harmonics are thus reduced considerably. Thus, both the grid currents and PCC voltages comply to IEEE-519 standard. The complete harmonic spectra of the grid currents and PCC voltages up to 50th harmonic order, with the presented control strategy, is reported in Appendix-D. Moreover, the effect of step-sizes (μ_a, μ_b, μ_c) on convergence of the harmonic gains is reported in Fig. 13. The grid-interfaced DG-VSI system is operating without harmonic voltage control. The harmonic voltage control is enabled at 0.5s and the performances of output harmonic gains for 5th, 7th and 11th harmonics under for different step-sizes (0.1, 0.5, 2.5 and 10) are reported in Fig. 13. The harmonic gains converge faster at large step-size values. However, as remarked earlier, too high step-sizes (greater than the critical step size, $|i_{Lah}||Z_{lineh}|/|v_{pah}|$), diverge the harmonic-gain update algorithm.

Fig. 14 depicts the performance of the *islanded* microgrid system with two DG sources under nonlinear loads. Fig. 14(a) shows the performance without the harmonic voltage control, while Fig. 14(b) shows the system performance with presented harmonic voltage control. Two equally rated DG-VSIs (5kVA) are considered for this purpose, supplying a nonlinear load (3kVA) and a linear load (4kW and 1kVar). The harmonic voltage control is applied to 2nd DG-VSI. Upon invoking the harmonic voltage control, the DG output harmonic voltage is increased as seen in Fig. 14(b). Thus DG2 output harmonic voltages are controlled to allow all the harmonic load currents to flow through 2nd DG-VSI system, leaving the currents in first DG-VSI completely harmonics-free. This is observed in the fourth panel of Fig. 14(b). Moreover, the PCC voltage harmonics are reduced. In this context, the THD values of DG voltages (v_{oa},v_{oa2}) and DG currents (i_{oa}, i_{oa2}) in bar-graph representation are reported in Fig. 15. The harmonic distortion in PCC voltages, is improved from 5.18% to 3.41%. The DG-VSI1 currents are improved, while DG-VSI2 absorbs all the harmonic currents. The harmonic voltage control, therefore, facilitates harmonic current sharing in islanded microgrid system. The overall comparative performance of the presented strategy with both the conventional control [23] and harmonic control [16], is systematically evaluated and presented in Table-II.

Besides verification of presented strategy in simulation, an experimental validation of results is performed, using a develop laboratory prototype. Hall-Effect current sensors (LA-55p) and voltage sensors (LV-25) are used to sense the currents and voltages. A real time controller- DSP (Digital Signal Processor) dSPACE1202 Microlab-box, is used to realize the presented control strategy, where, different inverter gating pulses are the outputs of micro-lab box controller. The results depict the grid voltages (v_{gab}, v_{gbc}, v_{gca}), output voltages (v_{oab}, v_{obc}, v_{oca}), filter currents (i_{ca}, i_{cb}, i_{cc}) and output currents (i_{oa}, i_{ob}, i_{oc}). The optical isolation between VSI and digital signal processor (DSP) is ensured through opto-couplers.The results under steady-state are captured using power analyser (Fluke-43B). The dynamic performance is captured using a four channel digital storage oscilloscope. A photograph of experimental test rig with different components highlighted, is shown in Fig. 16. The parameters considered in the experimental prototype are stated in Appendix-B.

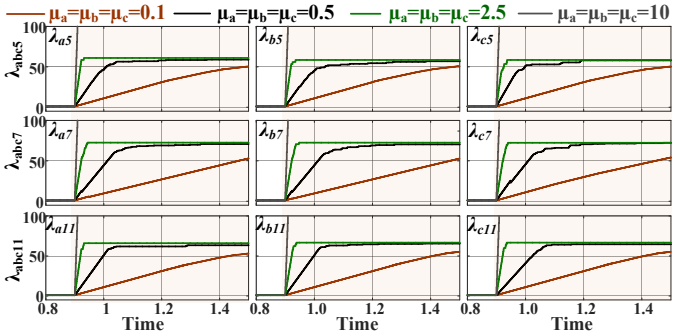


Fig. 13 Effect of step-sizes (μ_a, μ_b, μ_c) on convergence of harmonic gain

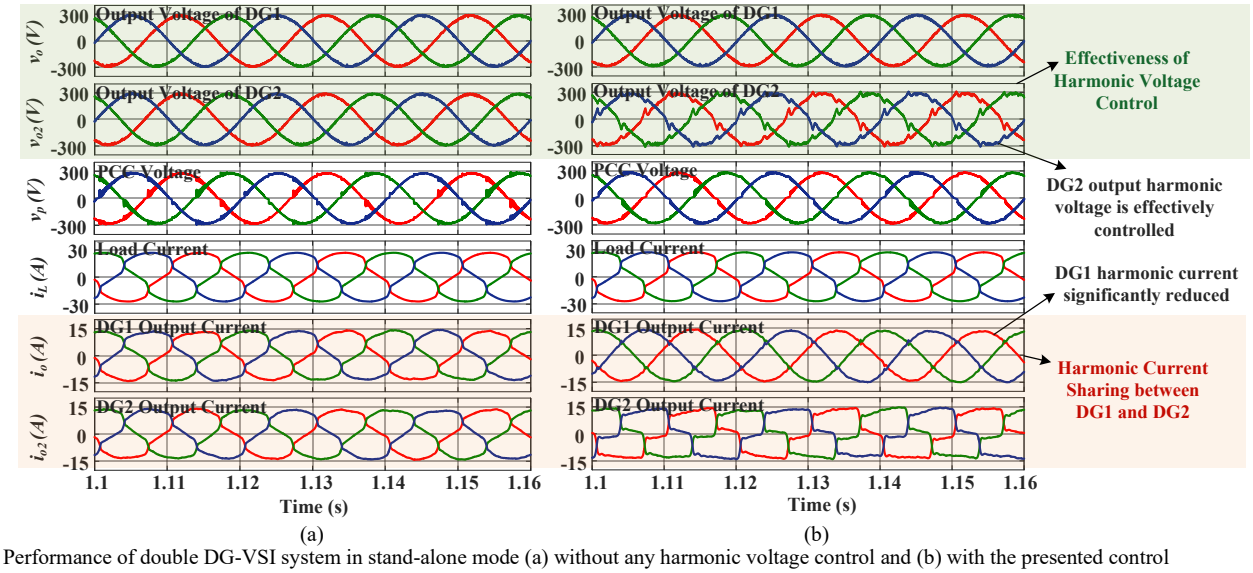


Fig. 14 Performance of double DG-VSI system in stand-alone mode (a) without any harmonic voltage control and (b) with the presented control

TABLE II
COMPARATIVE ANALYSIS WITH STATE-OF-ART CONTROL STRATEGIES

Parameter	Conventional VSI control strategy [23]	State-of-art control [16] (PR based harmonic control)	State-of-art control [18] (OSV based control)	Presented OSV based Harmonic Voltage Control
Type of controller	PWM control	PWM control	Switching Vector Control	Switching Vector Control
Selective harmonic compensation	No	Yes	No	Yes
Flexibility in Harmonic Control	No	Yes	No	Yes
Adaptive HML	Not facilitated	Not facilitated	Not facilitated	Facilitated
VSI overcurrent protection	No	No	Yes, Inherent within the control	Yes, Inherent within the control
Computational burden	15e-6 s	15e-6 s	20e-6 s	20e-6 s
Memory burden	High	Low	High	High
Rigorous tuning of PI/PR regulators	Not required	Mandatory	Not required	Not required
Performance during system frequency fluctuations	Unaffected	Degraded (Due to harmonic resonance frequency change)	Unaffected	Unaffected
System stability	Stable	Prone to stability issues caused by non-ideal PR regulators	Stable	Stable (Output voltages directly governed by GPC)
THD of grid currents in grid-tied mode	35.3% (High)	4.3% (Low/Regulated)	NA	3.2% (Low/Regulated)
THD of PCC voltages in islanded mode	5.3% (Higher)	4.1% (Low/Regulated)	5.2% (Higher)	3.4% (Low/Regulated)
IEEE-519 standard*	Violates	Follows	Violates	Follows
IEC-61727 standard*	Violates	Follows	Violates	Follows

*Tested under the presence of non-linear loads at the point of common coupling

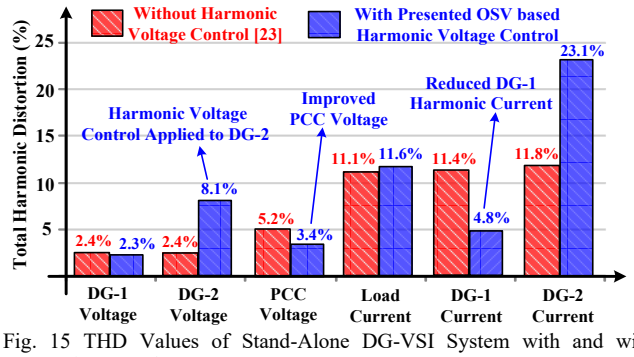


Fig. 15 THD Values of Stand-Alone DG-VSI System with and without Harmonic Control

Fig. 17 depicts the performance of single DG-VSI system supplying a nonlinear load, with harmonic voltage control enabled. The grid impedance and DG impedance are set to

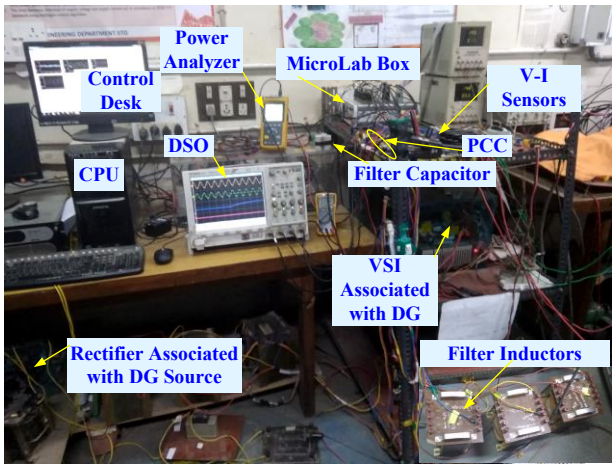


Fig. 16 Photograph of experimental test-rig

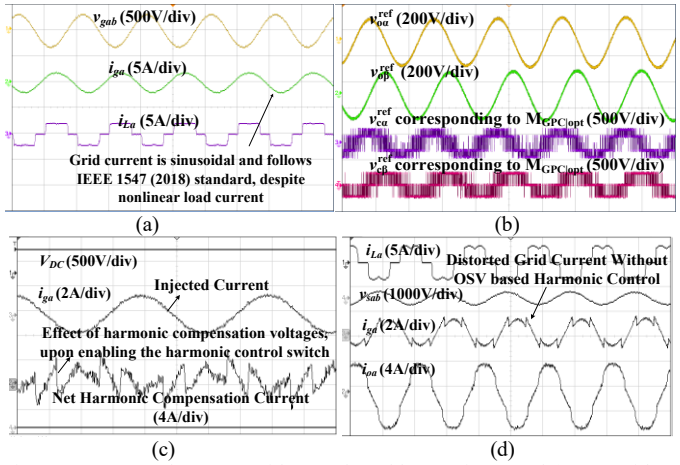


Fig. 17 System performance with OSV based harmonic control (a) v_{gab} with i_{ga} and i_{La}; (b) Salient internal signals of the OSV controller- reference voltages corresponding to gating pulses; (c) V_{DC}, i_{ga} and harmonic currents absorbed by the DG; (d) Performance without any harmonic control- i_{La}, v_{gab}, i_{ga} and i_{oa}

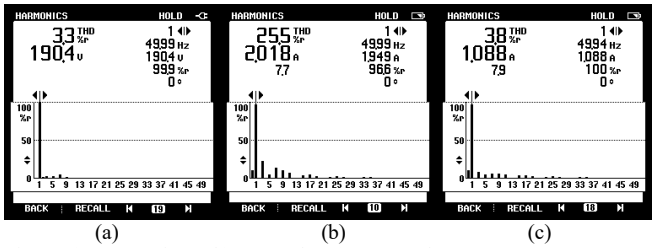


Fig. 18 (a) THD of v_{gab} (b) THD of i_{La} (c) THD of i_{ga}

'0.5+1.25j Ω'. Fig. 17(a) shows the grid voltage (v_{gab}), load current (i_{La}) and grid current (i_{ga}). The salient internal signals of the controller, are depicted in Fig. 17(b), which include $v_{o\alpha}^{ref}$, $v_{o\beta}^{ref}$, $v_{c\alpha}^{ref}$ and $v_{c\beta}^{ref}$, where, $v_{c\alpha}^{ref}$ and $v_{c\beta}^{ref}$ are the references of $v_{c\alpha}$ and $v_{c\beta}$ corresponding to the optimal switching sequences obtained from OSV controller. Since the harmonic control switch is enabled, the harmonic compensation voltages are produced by the controller, which absorb the grid current harmonics. Consequently, the net harmonic currents absorbed by the DG are shown in Fig. 17(c), leaving the grid current perfectly sinusoidal. However, without the OSV based harmonic control, the grid current is contaminated with significant harmonics, as observed in Fig 17(d), with the same load current.

As noticed in Fig. 17(a), the grid current is maintained sinusoidal throughout the operation, where the THD is maintained with the limits in accordance with the IEEE 1547 standard. This is reported in Fig. 18, where the THD of grid current is observed as 4.7% (as in Fig. 18(c)) with a highly nonlinear load current THD of 27% (as in Fig. 18(b)). This is the effect of enabling the harmonic control switch. Since the DG output voltages are rigidly controlled by OSV controller through the action of minimization function (22), the harmonics in DG output voltage, are regulated to compensate for the harmonic currents entering the distribution grid.

The controller performance under change in the reference active power of the DG is also recorded. This is shown in Fig. 19, where the DG reference active power is gradually reduced by 50% and then restored back. Fig. 19(a) shows the system performance under decrease in the DG reference power, while Fig. 19(b) depicts the performance under increase in the DG reference power. Accordingly, the current injected into the grid is decreased and increased, as pointed out in Fig. 19(a) and

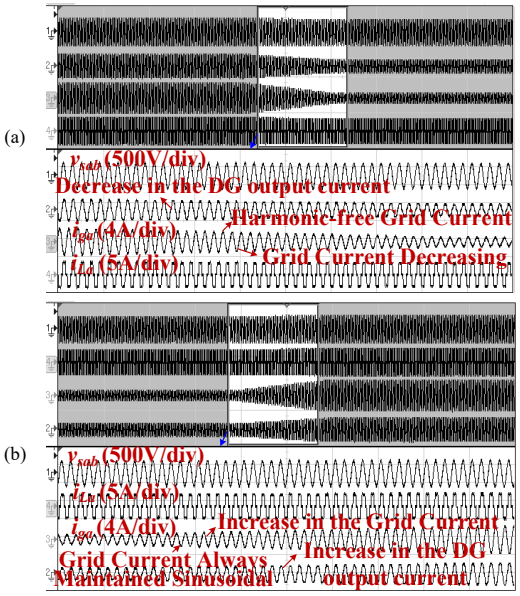


Fig. 19 Dynamic performance of the system under- (a) Decrease in DG reference active power, (b) Increase in DG reference active power

Fig. 19(b), respectively. The dynamic operation is observed smooth, and the grid currents are maintained sinusoidal throughout the operation, despite the nonlinear load current, as observed in Fig. 19(a) and Fig. 19(b). Thus the harmonic control strategy properly adapts to the dynamic perturbations in the DG-VSI system.

V. Conclusion

A harmonic voltage control strategy using optimal switching vector controller has been explored for three-phase grid connected and off-grid distributed generation system. A minimization criterion is used in OSV controller to achieve accurate output voltage tracking performance and flexibly control the DG output harmonic voltage. In this way, the harmonic currents entering the grid, are precisely regulated in the grid connected mode of operation. In stand-alone mode of operation, the power quality is improved by elimination of PCC voltage harmonics, caused by nonlinear load in the system. The controller eliminates the usage multiple proportional-resonant controllers, proportional-integral regulators, cascaded feedback loops or phase locked loops in the system. The simulation and experimental performances are evaluated to confirm the viability of the algorithm. The modern DG systems employ increased renewables and are subject to rapidly increasing nonlinear loads, and the presented control strategy is a possible solution for voltage-controlled distributed generation inverters. As this controller is possible to be appended in existing DG inverter controls, it can be easily enabled or disabled flexibly, as per the system operator need.

Acknowledgements

The authors acknowledge the feedback and contributions of Prof. Bikash Pal (Imperial College London) that have helped to improve the quality of the work. This work is supported by the Department of Science and Technology (DST), Government of India, J. C. Bose fellowship and the projects, UK-India Clean Energy Research Institute (UK-I CERI, Grant Number RP03391) and Fund for Improvement of Science and Technology (FIST, Grant Number RP03195G).

APPENDICES

A. Simulation and Control Parameters

Grid Voltage: 208V; Grid Frequency: 50 Hz; DC Bus Voltage: 400 V; Filter Parameters: 3 *m*H and 15 μF; Grid Inductor: 4 mH; OSV Control Parameters: N_p=3, N_f=2; Sampling Time (T_s): 30 µs; Sampling Time: 30 μs; Step-size for harmonic gain update algorithm: 0.5; Gain Update Sampling Time (T_{sg}): 1 *m*s; VSI Switching Frequency: 10 kHz.

B. Experimental Parameters

Grid Voltage: 190V; Grid Frequency: 50Hz; DC Bus Voltage: 400 V; Grid Inductor: 4mH; Filter Parameters: 3 *m*H and 15 μF; VSI Rating: 15 kVA; VSI Switching Frequency: 10 kHz; DSP Sampling Time: 33 μs.

C. Design of LC Filter Parameters

In this GPC based approach, the filter dynamics are incorporated in the GPC controller using state-space representation and then directly generating the VSC gating pulses. This is in contrast to the conventional controllers which generally use multiple PI/PR regulators [16], which are sensitive to grid stability. However, the GPC based controller directly governs the output voltages, by incorporating the LC filter dynamics within itself. Since the LC filter dynamics are incorporated within the GPC controller, the variations in the LC filter parameters hardly affect the stability of the system (Since the DG output voltages are governed directly by the minimization function (21)). Yet, the design procedure adopted to determine the filter parameters is as shown here.

The LC filter is connected in series with VSI to filter out the higher-order harmonics from the pole voltages. The associated DG module cannot be connected to the PCC unless the high frequency components are attenuated from the output voltage. The output voltage (v_{oa}) varies slowly relatively to switching frequency. Then the voltage across the inductor (V_L) is,

$$V_L = V_{ca} - V_{oa} \tag{31}$$

To determine the maximum inductor ripple current, the values of v_{ca} and v_{oa} are as [25],

$$V_{ca} = (2/3)V_{DC}, V_{oa} = (1/2)V_{DC}, V_L = (1/6)V_{DC} \tag{32}$$

The ripple current depends on the DC link voltage, inductance, and the switching frequency. The DC link voltage and switching frequency are constant, thus the inductance is obtained from (32) as,

$$V_L = L\Delta\hat{I}_L / 0.75T_s, \Delta\hat{I}_L = 0.75V_L / 6f_s L \tag{33}$$

$$L = V_{DC} / 8\Delta\hat{I}_L f_s \tag{34}$$

where, V_L is the inductor voltage, f_s is the switching frequency. For the system considered here (V_{DC}= 400 V; T_s= 30µs), the typical range of LC filter parameters are obtained as follows. The rated current of voltage source converter is $5\times10^3/\sqrt{3}\times208$, which is approximately 14A. Hence,

$$L = V_{DC} / 8\Delta\hat{I}_L f_s \approx 5 \text{ mH} \tag{35}$$

The capacitance must be selected to produce low reactance at the switching frequency. The typical resonant frequency is lower than one third of switching frequency of the voltage source converter [26]. Therefore, the typical value of resonant frequency of VSI is around 0.5-2 kHz. Hence, the typical value of capacitance is obtained as,

$$C = 1/\left(4L\pi^2 f_{resonance}^2\right) \approx 2 \text{ µF to } 20 \text{ µF} \tag{36}$$

D. Detailed Analysis of Grid Current and PCC Voltage Harmonics

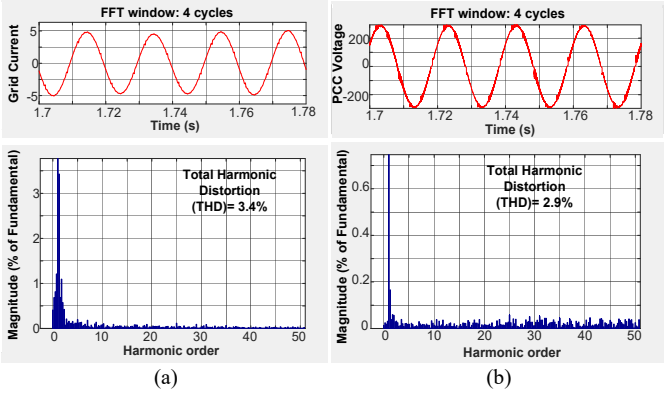
The detailed analysis of grid current and PCC voltage harmonics are reported here, in Table-III and Table-IV, respectively. The corresponding harmonic spectra of grid current and PCC voltage is shown in Fig. 20(a) and Fig. 20(b), respectively, through fast Fourier transform (FFT) analysis.

TABLE III
DETAILED ANALYSIS OF GRID CURRENT HARMONICS

No.	%	No.	%	No.	%	No.	%	No.	%
DC	0.2								
1	100	11	0.1	21	0.05	31	0.66	41	0.33
2	0.1	12	0.06	22	0.04	32	0.02	42	0.03
3	0.12	13	0.11	23	0.07	33	0.06	43	0.29
4	0.11	14	0.04	24	0.03	34	0.03	44	0
5	0.08	15	0.01	25	0.9	35	0.48	45	0.04
6	0.07	16	0.04	26	0.02	36	0.03	46	0.01
7	0.12	17	0.04	27	0.03	37	0.48	47	0.21
8	0.08	18	0.02	28	0.02	38	0.03	48	0.01
9	0.08	19	0.03	29	0.68	39	0	49	0.21
10	0.03	20	0.04	30	0.01	40	0	50	0.01

TABLE IV
DETAILED ANALYSIS OF PCC VOLTAGE HARMONICS

No.	%	No.	%	No.	%	No.	%	No.	%
DC	0								
1	100	11	0.02	21	0.02	31	0.63	41	0.44
2	0.02	12	0.01	22	0.02	32	0.02	42	0.04
3	0.01	13	0.05	23	0.03	33	0.06	43	0.37
4	0.01	14	0.01	24	0.03	34	0.02	44	0.01
5	0	15	0.02	25	0.68	35	0.53	45	0.05
6	0.01	16	0.01	26	0.02	36	0.02	46	0.02
7	0.03	17	0.04	27	0.04	37	0.52	47	0.32
8	0	18	0.03	28	0.01	38	0.03	48	0.01
9	0.02	19	0.04	29	0.65	39	0.03	49	0.27
10	0.01	20	0.03	30	0.03	40	0.03	50	0.03



(a) (b)

Fig. 20 Harmonic spectra (FFT analysis) of (a) Grid current, (b) PCC voltage

The harmonic order and its corresponding harmonic percentage value with respect to fundamental component, are highlighted up to 50th harmonic. The color code in the tables depict the closeness to the safe values, within the prescribed limits as per IEEE-519 standard [24]. The red color gradients represent the violated harmonic values, while the yellow and green color gradients represent the safe values.

REFERENCES

[1] D. E. Olivares, A. M. Sani, A. H. Etemadi *et. al.*, "Trends in microgrid control," *IEEE Trans. Smart Grid*, vol. 5, no. 4, pp. 1905–1919, 2014.

[2] H. R. Baghaee, M. Mirsalim, G. B. Gharehpetian and H. A. Talebi, "Decentralized Sliding Mode Control of WG/PV/FC Microgrids Under Unbalanced and Nonlinear Load Conditions for On- and Off-Grid Modes," *IEEE Systems Journal*, vol. 12, no. 4, pp. 3108-3119, 2018.

[3] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," in *IEEE Std 1547-2018*, pp.1-138, 2018.

[4] H. R. Baghaee, M. Mirsalim, G. B. Gharehpetan and H. A. Talebi, "Nonlinear Load Sharing and Voltage Compensation of Microgrids Based on Harmonic Power-Flow Calculations Using Radial Basis Function Neural Networks," *IEEE Systems Journal*, vol. 12, no. 3, pp. 2749-2759, Sept. 2018..

[5] S. Priyank and B. Singh, "Leakage Current Suppression in Double Stage SECS Enabling Harmonics Suppression Capabilities," *IEEE Trans. Energy Conv*., Early Access, 2020.

[6] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "High performance current controller for selective harmonic compensation in active power filters," *IEEE Trans. Pow. Electr.*, vol. 22, no. 5, pp. 1826–1835, 2007.

[7] J. He, Y. W. Li, and M. Munir, "A flexible harmonic control approach through voltage-controlled DG-grid interfacing converters," *IEEE Trans. Ind. Electron*., vol. 59, no. 1, pp. 444–455, Jan. 2012.

[8] P. Shah, I. Hussain, B. Singh, A. Chandra and K. Al-Haddad, "GI-Based Control Scheme for Single-Stage Grid Interfaced SECS for Power Quality Improvement," *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 869-881, 2019.

[9] N. Babu P, J. M. Guerrero, P. Siano, R. Peesapati and G. Panda, "An Improved Adaptive Control Strategy in Grid-Tied PV System With Active Power Filter for Power Quality Enhancement," *IEEE Systems Journal,* Early Access, 2020.

[10] L. S. Vedantham, K. Shailendra, S. Bhim and M. Sukumar, "A Multifunctional GPV System Using Adaptive Observer Based Harmonic Cancellation Technique," in *IEEE Transactions on Industrial Electronics*, pp. 1347-1357, vol. 65, no. 2, , 2018.

[11] J. R. Fischer, S. A. Gonzlez, I. Carugati, M. A. Herrn, M. G. Judewicz, and D. O. Carrica, "Robust predictive control of grid-tied converters based on direct power control," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5634–5643, Oct. 2014.

[12] G. Escobar, P. G. Hernandez-Briones, P. R. Martinez, M. Hernandez Gomez, and R. E. Torres-Olguin, "A repetitive-based controller for the compensation of 6ζ± 1 harmonic components," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3150–3158, Aug. 2008.

[13] Y. Yang, K. Zhou, H. Wang and F. Blaabjerg, "Analysis and Mitigation of Dead-Time Harmonics in the Single-Phase Full-Bridge PWM Converter With Repetitive Controllers," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5343-5354, Sept.-Oct. 2018.

[14] X. Liang and C. Andalib -Bin- Karim, "Harmonics and Mitigation Techniques Through Advanced Control in Grid-Connected Renewable Energy Sources: A Review," *IEEE Trans. Industry Applications*, vol. 54, no. 4, pp. 3100-3111, July-Aug. 2018.

[15] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," in *IEEE Transactions on Industrial Electronics*, vol. 45, no. 5, pp. 691-703, 1998.

[16] J. He, Y. W. Li and F. Blaabjerg, "Flexible Microgrid Power Quality Enhancement Using Adaptive Hybrid Voltage and Current Controller," *IEEE Trans Industrial Electronics*, vol. 61, no. 6, pp. 2784-2794, June 2014.

[17] N. Zhang, H. Tang, and C. Yao, " A systematic method for designing a PR controller and active damping of the LCL filter for single-phase grid-connected PV inverters", *Energies*, Vol.7, no. 6, pp.3934-3954, 2014.

[18] V. Srinivas, B. Singh and S. Mishra, "Predictive Optimal Switching Vector Controller based Microgrid Enabling Switching Frequency Constraint," in Proc., *IEEE International Conference on Power Electron, Drives and Energy Systems (PEDES),* Chennai, pp. 1-6, 2018.

[19] S. Kouro, P. Cortes, R. Vargas, U. Ammann and J. Rodriguez, "Model Predictive Control—A Simple and Powerful Method to Control Power Converters," *IEEE Tran. Ind. Elecr.*, vol. 56, no. 6, pp. 1826-1838, 2009.

[20] V. Srinivas, B. Singh and S. Mishra, "A Self-Synchronizing VSM with Seamless Operation during Unintentional Islanding Events," *IEEE Trans. Ind. Inform*., Early Access.

[21] A. J. Babqi and A. H. Etemadi, "MPC-based microgrid control with supplementary fault current limitation and smooth transition mechanisms," *IET GTD*, vol. 11, no. 9, pp. 2164-2172, 2017.

[22] J. Hu, J. Zhu and D. G. Dorrell, "Model-predictive control of grid-connected inverters for PV systems with flexible power regulation and switching frequency reduction,", in Proc., *IEEE Energy Conversion Congress and Exposition*, Denver, CO, pp. 540-546, 2013.

[23] M. G. Karimi, A. S. Khajehoddin, P. Piya and M. Ebrahimi, "Universal Controller for Three-Phase Inverters in a Microgrid," *IEEE Journ. Emer. Sel. Topics in Pow. Electron.*, vol. 4, no. 4, pp. 1342-1353, Dec. 2016.

[24] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, in *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)* , vol., no., pp.1-29, 11 June 2014

[25] K. H. Ahmed, S. J. Finney and B. W. Williams, "Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation,", *in Proc., IEEE Compatibility in Power Electronics*, Gdansk, pp. 1-9, 2007.

[26] K. Hatua, A. K. Jain, D. Banerjee and V. T. Ranganathan, "Active Damping of Output LC Filter Resonance for Vector-Controlled VSI-Fed AC Motor Drives," *in IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 334-342, Jan. 2012.

Vedantham Lakshmi Srinivas (M' 17) was born in East Godavari, India on 30 October 1994. He received his B. Tech. degree in electrical engineering from Indian Institute of Technology (BHU), Varanasi, India in 2015, after which he joined Indian Institute of Technology Delhi for M. Tech. degree in the field of power systems and power electronics. He has received his Ph.D. degree in the field of distributed power control and integration, with the department of electrical engineering at the Indian Institute of Technology Delhi, New Delhi, India.

Dr. Lakshmi Srinivas is the recipient of POSOCO Power System National Award as a recognition for his research work, from Power Grid Corporation of India Limited in 2021, while he is also the recipient of research excellence travel award and international research grant from the government of India. Currently, he is working as a postdoctoral research associate at the Cardiff University, where he is with the Centre for Integrated Renewable Energy Generation and Supply (CIREGS) of the School of Engineering. His research interests include renewable energy, energy storage systems, power electronic converters, power system optimization, adaptive controllers, Kalman filtering state-estimation methods and machine learning algorithms.

Bhim Singh (SM'99-F'10) was born in Rahamapur, Bijnor (UP), India, in 1956. He has received his B.E. (Electrical) from the University of Roorkee (Now IIT Roorkee), India, in 1977 and his M.Tech. (Power Apparatus & Systems) and Ph.D. from the Indian Institute of Technology Delhi, India, in 1979 and 1983, respectively.

In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a Lecturer. He became a Reader there in 1988. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, India, as an Assistant Professor, where he has become an Associate Professor in 1994 and a Professor in 1997. He has been ABB Chair Professor from Sept. 2007 to Sept. 2012. He has also been CEA Chair Professor from Oct. 2012 to September 2017. He has been Head of the Department of Electrical Engineering at IIT Delhi from Jul. 2014 to Aug. 2016. He has been the Dean, Academics at IIT Delhi from Aug. 2016 to Aug. 2019. He is JC Bose Fellow of DST, Government of India since December 2015. Prof. Singh is the Chairman of Board of Governors (BOG), Maulana Azad National Institute of Technology, Bhopal, since 3rd Jul. 2018 for 3 Years and Non-official Independent Director, NTPC Limited, since Jul. 2018 for 3 years. He is Central Electricity Authority (CEA) Chair Professor since 2019.

Prof. Singh has guided 95 Ph.D. dissertations, and 168 M.E./M.Tech./M.S.(R) theses. He has been filed 64 patents. He has executed more than eighty sponsored and consultancy projects. He has co-authored a text book on power quality: Power Quality Problems and Mitigation Techniques published by John Wiley & Sons Ltd. 2015. His areas of interest include solar PV grid interface systems, microgrids, power quality monitoring and mitigation, solar PV water pumping systems, improved power quality AC-DC converters.

Sukumar Mishra (M'97–SM'04) received his M.Tech and PhD in Electrical Engineering from National Institute of Technology, Rourkela in 1992 and 2000 respectively. After spending nine years as a lecturer at Sambalpur University (Orissa), Prof. Mishra joined BPUT (Orissa) as a Reader at the Electrical Department and served there for two years. Presently, Prof. Mishra is a Professor at Indian Institute of Technology Delhi and has been its part for the past 17 years, and presently, he has been functioning as Associate Dean R&D of IIT Delhi from March 2020.

Prof. Mishra has won many accolades throughout his academic tenure of 27 years. He has been a recipient of Young Scientist award (1999), INSA medal for young scientist (2002), INAE young engineer award (2002), INAE silver jubilee young engineer award (2012), The Samanta Chandra Shekhar award (2016), Bimal Bose award (2019) and NASI-Reliance Platinum Jubilee award (2019). He has been selected as the Mission Innovation National Champion (2019) under the Mission innovation initiative to accelerate clean energy in India. He has been granted fellowships from many prestigious technical societies like IET (UK), NASI (India), INAE (India), IETE (India), and IE (India) and is also recognized as the INAE Industry-Academic Distinguish Professor. Prof. Mishra is currently acting as ABB Chair professor and has previously delegated as the NTPC, INAE and Power Grid Chair professor. Prof. Mishra has also carried out many important industrial consultations with TATA Power, Microtek and others.

Prof. Mishra's research expertise lies in the field of Power Systems, Power Quality Studies, Renewable Energy and Smart Grid. He has supervised 33 PhD students (18 ongoing), 40 Master students (2 ongoing). Prof. Mishra has also authored five book chapters so far and has 13 patents to his credit. Prof. Mishra has been working in close association with IEEE Delhi Section Executive Committee for past few years and is currently serving as an Editor for the IEEE Transactions on Smart Grid, IEEE Transactions on Sustainable Energy and was an Area Editor for the IET Generation, Transmission & Distribution journal.

Lie Xu (M'03–SM'06) received the B.Sc. degree in mechatronics from Zhejiang University, Hangzhou, China, in 1993, and the Ph.D. degree in electrical engineering from the University of Sheffield, Sheffield, U.K., in 2000.

He is currently a Professor with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, U.K. He was with the Queen's University of Belfast and ALSTOM T&D, Stafford, U.K. His research interests include power electronics, wind energy generation and grid integration, and application of power electronics to power systems.

Dr. Xu is an Editor for the IEEE Transactions on Power Delivery and IEEE Transactions on Energy Conversion.