Novel Developments in Scientific EMCCDs

Thesis

Novel Developments in Scientific EMCCDs

Alice Georgina Fleur Dunford

Centre for Electronic Imaging
Faculty of Science, Technology, Engineering and Mathematics
The Open University

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Abstract

This thesis presents a complete characterisation and an assessment of the technology readiness of a new Electron Multiplying Charge Coupled Devices (EMCCD) technology. Several factors of interest are studied here including, charge transfer efficiency, gain ageing and radiation effects from protons. Many light-starved and high-speed image applications (e.g. observation from space and automated visual inspection) can benefit from Time Delay Integration (TDI) as it allows photoelectrons from multiple exposures to be summed in the charge domain with no added noise. Electron multiplication (EM) can be used to further increase the signal to noise ratio for extremely faint light signals. There is a growing demand for Complementary metal–oxide–semiconductor (CMOS) sensors with the same or greater functionality and even better performance. The research presented here analyses the functionality of a recently designed EMCCD in a CMOS process. This device (EMTC1) incorporates two novel EM pixel structures which enable high gain at relatively low voltages. The theory and architecture of Charge Coupled Devices (CCDs) and EMCCDs are discussed, providing a technical background for the results. Furthermore, the practical methods, including experimental techniques developed for this device's testing, are presented here. Ageing within the device is a primary focus within this thesis, as is the effect of proton irradiation. The effects of the radiation damage on parameters such as dark current, and Charge Transfer Inefficiency (CTI) have been documented along with its effect on EM gain. These results have been corroborated with simulations of device operation in TCAD.

Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other University as part of the requirement for a higher degree. The work described herein was conducted solely by the undersigned except for those colleagues and other workers acknowledged in the text.

Alice Dunford
March 2020

This thesis is dedicated to
my friends and family for their unconditional support
and who continue to inspire me
and to Lucy the cat, superior laptop warmer
who has failed to delete my thesis despite repeated attempts.

Acknowledgements

I would like to acknowledge the following people as without them, the work detailed in this thesis could not have been accomplished. I would like to thank my supervisors Konstantin Stefanov, Andrew Holland and Douglas Jordan, for their continued support and guidance. Thanks to all members past and present of the centre for electronic imaging, including; Andrew Clarke, Ben Dryer, David Hall, Edgar Allanwood, Jason Gow, Matthew Soman, Philippa Smith and Ross Burgon. Thanks to all members of the School of Physical Sciences. Thanks to all members of Teledyne e2v who have provided guidance, insight and support. I would like to acknowledge the financial support from STFC, The Open University and Teledyne e2v. Special thanks to David Burt whose knowledge and assistance over the last few years has been invaluable. Finally, I must thank my family and friends, thank you for putting up with me.

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Acronyms

AIMO Advanced Inversion mode.

ASCA Advanced Satellite for Cosmology and Astronomy.

CCD Charge Coupled Device.

CDS Correlated Doubling Sampling.

CHEI Channel Hot Electron Injection.

CIC Clock Induced Charge.

CIS CMOS Image Sensor.

CME Coronal Mass Ejections.

CMOS Complementary Metal Oxide Semiconductor.

CTE Charge Transfer Efficiency.

CTI Charge Transfer Inefficiency.

DAHC Drain Avalanche Hot Carrier.

EMCCD Electron Multiplication Charge Coupled Device.

EMTC1 Electron Multiplication Test Chip 1.

ENF Excess Noise Factor.

EPC ESPROS Photonic Corporation.

EPER Extended Pixel Edge Response.

FPGA Field-Programmable Gate Array.

FPN Fixed Pattern Noise.

FWC Full Well Capacity.

LED Light Emitting Diode.

LPCVD Low Pressure Chemical Vapour Deposition.

MOS Metal Oxide Semiconductor.

NIMO Non-Inverted Mode.

P2HV P2 High Voltage.

PCB Printed Circuit Board.

PTC Photon Transfer Curve.

RG Reset Gate.

ROI Region of Interest.

RTD Resistance Temperature Detector.

SEU Single Event Upsets.

SGHE Secondary Generated Hot Electron Injection.

SHE Substrate Hot Electron.

SNR Signal to Noise Ratio.

TDI Time Delay and Integration.

TEC Thermoelectric Cooler.

Chapter 1

Introduction

1.1 Context

From the Chauvet cave paintings in France to Van Gogh's The Starry Night, humans have endeavoured to capture both their terrestrial and celestial surroundings. The invention of cameras simplified the process considerably. The first camera, the camera obscura, was based on the principle that an inverted image is produced when a scene is projected through a small hole on a screen. The inclusion of lenses in the 16th century enabled the camera obscura to be used as an aid to drawing.

From the early 1800s, cameras developed rapidly, as it had been known for several centuries that certain materials are photosensitive such as a silver nitrate-based solution. The Daguerreotype camera utilised a silver-plated sheet of copper, which was treated with iodine vapour producing a highly photosensitive layer of silver vapour. The dry plates were made from gelatin which drastically reduced the exposure time.

The advent of the Kodak camera developed by George Easterman, which utilised celluloid film for the first time in 1889 enabled the average consumer to capture everyday life.

Astrophotography evolved concurrently with the camera and was pioneered by amateur astronomers and 'Gentlemen Scientists'. The first attempt at astronomical photography was made by L.J.M. Daguerre in 1839, the inventor of the Daguerreotype camera to photograph the Moon. These early cameras required long exposures and led to an indistinct fuzzy image of the Moon. The

first successful image of the Moon was taken a year later in 1840 using a 20 minute long exposure Daguerreotype camera mounted on a 13 cm reflecting telescope [71]. The introduction of dry plates led to astrophotography being utilised as a research tool. By 1887 multiple observatories were working on the first all-sky photographic astronomy project, the Astrographic Catalogue and Carte du Ciel in 1887.

The mid-twentieth century saw a revolution in astrophotography with the development of the Charge Coupled Device (CCD), a semiconductor image sensor. By 1970, the CCD had been proposed by Boyle and Smith, becoming highly popular due to its relatively simple structure yet high performance. With the advent of the CCD, the 1970s saw the transition from photographic plates to electronic imaging in both amateur and research observatories due to increased light sensitivity, and an increased ability to respond to a far wider spectral range and store large quantities of data.

Image sensor technology developed rapidly and helped to revolutionise astronomical imaging among other fields. Expeditions by the Jet Propulsion Lab (JPL) team to major astronomical observatories using a portable CCD camera system, captured the first professional high-resolution astronomical images [56].

CCDs are also successful in high energy physics experiments due to their high spatial resolution and thin, sensitive layers enabling the study of short lived particles. This has been particularly demonstrated in linear colliders, which study flavour identification using CCDs.

Semiconductor imaging devices such as the CCD have developed significantly since the initial development of operating p-n junctions in a "photon flux integrating mode" first described by G. Welker in 1967 [132]. This early design structure now forms the basis of the active pixel sensor. The Active Pixel Sensor (APS), developed from the early p-n junction proposed by G. Welker, was initially overtaken by the CCD. Several attempts were made during the 1970s, and 80s to compete with CCDs, as integrated circuit (IC) technology continued to develop but were ultimately unsuccessful.

It was not until the late 1990's that the APS became a viable option, enabled by the development of the high density, reduced power and low-cost Complementary Metal Oxide Sensors (CMOS) manufacturing process. These CMOS image sensors have developed rapidly over the last twenty years, but are yet to reach their full potential.

Light starved and high speed applications, such as Earth observation, can benefit from the implementation of several different techniques which increase the sensitivity of the device. In recent years, CMOS devices have become increasingly relevant within the industry, with ever evolving technological developments enabling far greater performances to be achieved.

Certain techniques have been employed within CCD technology to improve the performance of image sensors. In low light conditions and high speed image capture, the implementation of Time Delay Integration (TDI) can greatly improve the signal-to-noise-ratio (SNR) of the image. TDI allows for photoelectrons to be summed from multiple exposures without additional noise. The performance of CCD image sensors can be further improved by the addition of Electron Multiplication (EM). EM gain has become increasingly important within scientific detection, from astronomical imaging to automated visual inspection. Traditional CCDs have long been popular within astronomical imaging; however, they do suffer from several major disadvantages, namely the slow readout speed and read noise, which limit the observation of faint objects. EMCCDs have been shown to have very low read noise, close to 100% quantum efficiency (QE), and linear response. The QE and linear response are similar to modern CCDs. However, due to the more complex design, greater care is required to ensure the device is operated under the correct conditions.

Traditionally EM has been implemented only in CCDs, with only limited examples in CMOS technology; however interest in EM-in-CMOS is growing. The sensitivity of CMOS devices has previously been restricted by the readout noise when exposed to low level light conditions [34] however, and demand is growing for CMOS sensors with a similar if not greater functionality and performance than established CCD sensors. To date, the implementation of techniques such as TDI or EM within CMOS design have been limited due to restrictions, including the size of the inter-gate gaps and low operating voltage. With the possible benefits of on-chip functionality and high tolerance to saturation and radiation damage, implementing EM and TDI within a CMOS sensor could produce a highly sensitive image sensor.

This project focuses on implementing a CCD-style buried channel within a CMOS process, namely, the ESPROS process [28]. Newly patented EM gate structures have been integrated into the design, with the hope that these gates will greatly improve the EM gain and the overall performance of EM within CMOS devices. Research has been completed studying EM within the CMOS

imaging technology and has been found to provide a solution for low light applications.

1.2 Aims

The main aim of this study is to investigate new image sensors for space applications, specifically in Earth observation and low light level imaging, including industrial applications. Over the past decade, Teledyne e2v has successfully produced a range of EMCCDs and CMOS sensors which have been employed within scientific and industrial applications. The CEI, in conjunction with Teledyne e2v and ESPROS, have designed a new sensor that implements Electron Multiplication in an advanced CMOS process with the aim of achieving similar or superior functionality to CCDs and/or EMCCDs. This project studies the characterisation and device simulation of charge transfer efficiency in CCD-style buried channel when implemented in a CMOS process and provides a detailed study of the electron multiplication process under the constraints of low voltage. This characterisation aims to increase the technology readiness level for space applications and provide assistance in the design of new CMOS devices implementing TDI and EM.

This project also aims to test the potential of the newly developed technology and provide insight into the possibility of implementing it in the astronomical imaging. It is hoped that this research will lead to further developments within the field, with the potential for a new generation of devices implementing these unique design features.

1.3 Thesis Organisation

The work is presented in 8 further chapters. Chapter 2 provide a theoretical and technical background to CCDs, EMCCDs and CMOS active pixel image sensors. An outline of device architecture, operation and characteristics of the sensors are provided. An overview of the recently patented device that is studied is covered in Chapter 3 before a complete description of the experimental technique in Chapter 4. An initial characterisation of the device is provided in Chapter 5. This chapter covers the results of dark current, photon transfer curves and the charge transfer within the device when run at normal

operating conditions. Chapter 6 discusses the implication of the design on the charge transfer process; furthermore, the implementation of the new EM Gate designs is discussed. Research chapters 7 and 8 provide insight into the results of ageing, and proton irradiation within the device along with thorough simulations analysing potential the damage these mechanisms induce within this novel device. The final chapter concludes the work within this thesis and describes possible progression of any future work.

1.4 Publications arising from this study

1.4.1 First author conference proceedings

Dunford, A.G.F, Stefanov, K., Holland, A.D. "Low Voltage EMCCD in a CMOS process." Proc. SPIE 9915, High Energy, Optical, and Infrared Detectors for Astronomy VII, 99152Y, (2016).
Dunford, A.G.F, Stefanov, K., Holland, A.D. "The Operational Characteristics and Potential Applications of a Low Voltage EMCCD in a CMOS Process", Proc. SPIE 10709, High Energy, Optical, and Infrared Detectors for Astronomy VIII, 10709-84, (2018).

1.4.2 First author peer reviewed publications

Dunford, A.G.F, Stefanov, K., Holland, A.D., "Ageing and proton irradiation damage of a low voltage EMCCD in a CMOS process", Journal of Instrumentation, 13, (2018)

1.4.3 Contributing author peer reviewed publications

Stefanov, K., Dunford, A.G.F, Holland, A.D. "Electron Multiplying Low-Voltage CCD with Increased Gain", IEEE Transactions on Electron Devices, 65(7), (2018), pp. 2990-2996.

Chapter 2

Introduction to CCD and EMCCD Image Sensors

Charge Coupled Devices have been the detector of choice for many imaging needs. CCDs have been extensively studied in terms of characterisation and response to radiation damage. That research has required a working knowledge of CCD structure and operation. Presented here is a brief introduction to semiconductor principles which dictate CCD operation followed by a discussion of the operation of CCDs, EMCCDs and CMOS image sensors. The overview will be sufficient for the purpose of this work, and the reader will be directed to other literature sources if a complete review is required.

2.1 Image sensors

A range of different sensors have been developed over the last 100 years to detect unique events or changes within the detector's surroundings, but all are required to have certain features including an ability to respond to incident photons with good sensitivity, large dynamic range and good Signal-to-Noise-Ratio (SNR). These sensors are traditionally divided into two groups: scanned systems which contain a sensor detecting different energies that are scanned across the focal plane and static systems where an array detects the position at which the photon interacts.

Typical image sensors are the Charge Coupled Device (CCD) and many different types of CMOS images sensors (CIS). This thesis will focus on the theory of CCDs and their offshoot Electron Multiplication CCDs (EMCCDs) while also probing the theory of CIS sensors.

2.2 The Development of the Charge Coupled Device

The Charge Coupled Device (CCD) was invented at AT&T Bell Labs by William Boyle, and George E. Smith in 1969 [7], an innovation for which they were later awarded the Nobel Prize for physics in 2009. The device developed from earlier work focused on the construction of the magnetic-bubble memory where they discovered a "charge-bubble" could be transferred through both linear and area registers by manipulating electrode potentials.

CCDs are used to capture an image by converting incident light into an electrical signal. A simple analogy for CCD operation describes the pixel structure as buckets placed on top of a series of parallel conveyor belts. The parallel conveyor belts are distributed across a field akin to the focal plane of a telescope forming a square array of buckets (pixels). The belts are initially stationary and collect falling rain (photons). The buckets are temporarily covered by a large tarpaulin (the camera shutter closes) and the conveyor belts start to move, transferring the contents of each bucket of rain to another conveyor belt (serial or readout register) that runs perpendicular to the rest of the array. Once all of the buckets on the first row have been emptied into the serial array, the serial conveyor belt starts to move towards a special measuring cylinder. The first bucket on the belt is emptied into the measuring cylinder and the amount of water recorded. The serial conveyor belt shifts again and the process is repeated until all the buckets have been measured. The buckets on the serial conveyor belt are now empty, and the main conveyor belt shifts the second row of buckets into the serial conveyor belt and the contents measured. This process continues until the contents of all of the buckets in the array have been emptied into the measuring cylinder and measured. The tarpaulin is then removed, and rain (photons) can once again fill the buckets, and a new image is captured.

The three-phase device was rapidly fabricated and underwent testing with early experimental data presented in a paper by Amelio, Tompsett and Smith after the initial design [1]. Fairchild produced the first commercially available devices by 1974, consisting of a 100 by 100 2D pixel array and a 500 element linear device. Fairchild had also developed a CCD for use in the KH-11 Kennan reconnaissance satellite, launched in 1978, to be used for optical imaging [8]. By the 1980s CCDs were mass-produced for commercial electronic devices, such as camcorders and in 1993, the Advanced Satellite for Cosmology and Astronomy (ASCA) became the first satellite to utilise CCDs for X-ray imaging [126]. Recent decades have seen further developments in the image sensor field, with interest in implementing CCDs within astronomical study only growing. Furthermore, the CCD has driven developments in photography, and high-resolution imaging in medical [17] and scientific applications. Examples include using CCDs for use in dental X-rays [2], use in optical microscopy of biological structures [46] and nuclear power plant inspection [83].

2.3 The Semiconductor

To fully understand the mechanics of the image sensors described in this thesis, an understanding of the science of the semiconductor is required. The following section introduces semiconductor theory which governs CCD operation. CCDs have primarily been developed on a silicon substrate but have also been developed in other materials including graphene [37] and Mercury Cadmium Telluride (HgCdTe) [16]. This thesis will focus primarily on the operation of silicon CCDs, EMCCDs and CISs.

An isolated atom has discrete energy states. If two atoms are brought together, the atomic interactions energy levels can split. For solids, this results in atoms that have either energy bands or an energy state continuum. Where there are no available states, the regions are called band gaps. At any temperature, the band gaps can either be filled or empty. Partially filled energy levels provide the majority contribution to the conductivity as the electrons have high mobility.

The valence and conduction bands are those closest to the Fermi level. Here, the Fermi level can be considered a hypothetical energy level of an electron with a 50% probability of being occupied when at thermal equilibrium.

The Fermi level position in relation to the band energy levels determines the electrical characteristics of the semiconductor. The valence band consists of the highest occupied electronic states for a system at 0 K while the conduction band contains the lowest vacant electronic states. The gap between these is called the band gap. Insulators have a large band gap compared to kT (k is the Boltzmann constant and T is temperature). In conductors, there is no band gap resulting in band gap states being constantly occupied. Comparatively, semiconductors have a small band gap that an electron can cross when promoted from the valence to the conduction band. For silicon the band gap is $\sim$1.12 eV at room temperature [41].

The addition of certain impurities to a semiconductor lattice (doping), such as silicon, results in additional band gap states which can greatly enhance conductivity. In silicon doping with group V and VI elements (donor dopants) results in an additional carrier in the conduction band. Examples of donor dopants include phosphorus and arsenic. The addition of donor dopants results in mid-band gap states close to the conduction band and raise the Fermi level. In silicon, this doping results in n-type silicon. Comparatively doping with group II or III elements (acceptor dopants), such as boron or aluminium, introduces mid-band states close to the valence band lowering the Fermi-level. In silicon, this doping results in p-type silicon.

This doping results in n-type and p-type containing an excess of electrons and holes respectively. However, due to the now ionised atoms, both n and p-type silicon remain electrical neutral and in equilibrium. When these two materials are brought into contact, in the presence of no external fields, free carriers will diffuse across the junction and recombine. However, the ions are no longer in equilibrium and charge builds on either side of the junction; positive in the n-type and negative in the p-type silicon. An electric field results, which repels further charge diffusion resulting in a new equilibrium. The area on either side of the junction is called the depletion region as it has been depleted of free carriers (see Fig.2.1). The p-n junction described here refers directly to the boundary between the two semiconductor regions. It is this region that is fundamental in CCD operation to separate electron-hole pairs produced by photon interactions.

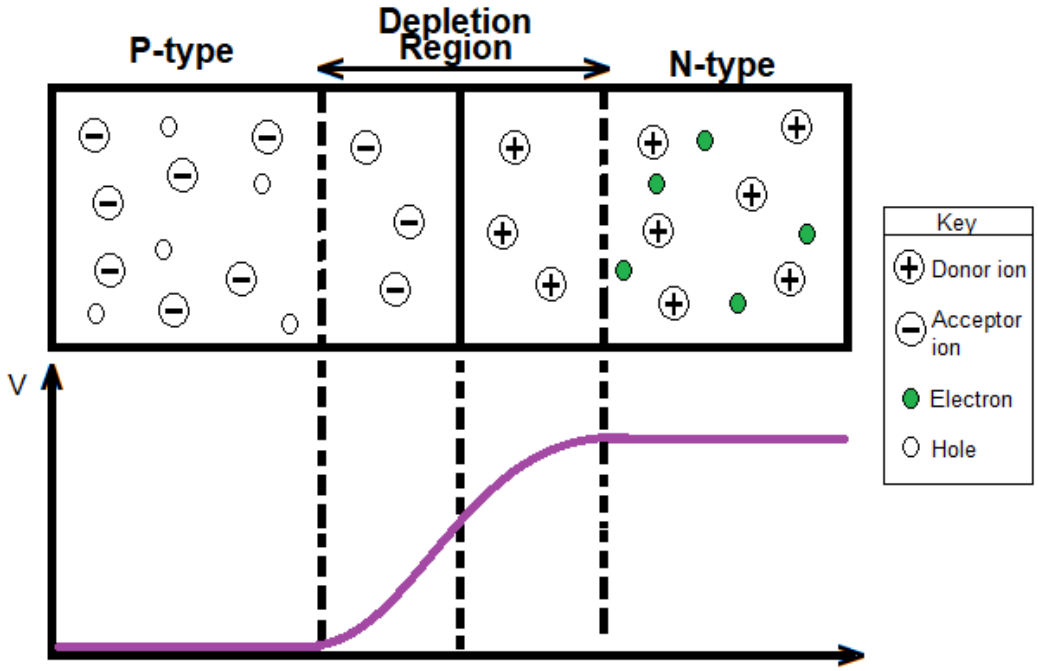

Figure 2.1: Diagram of a pn junction showing the depletion region and charge location. The graph denotes the potential step across the junction.

The application of different potentials further alters the bias regimes and modes of operation of the device. The application of a negative potential across the junction causes the semiconductor to leave its electrically neutral equilibrium and excess charge to accumulate that forms when a relatively lightly doped p-type epitaxial film is grown upon a highly doped substrate forming on the surface of the silicon. Oxidation of the silicon results in a layer of silicon oxide. By removing small sections of this layer, donor impurities can diffuse into the silicon. Multiple junctions can be formed simultaneously on a silicon wafer during this process. These are separated by scribing, contacts are added to the diffused portion of each diode, and the bottom side and these diodes are then inserted into the packaging.

The p-n junctions can be operated under several different conditions. When the regions are connected, some holes within the p-type region have sufficient energy to overcome the potential barrier. The movement of the charge majority can be described as a Forward Current. Likewise, the minority carriers within the n-type region can move across the junction in the opposite direction, known as Reverse Current. While the potential barrier limits the diffusion of majority

carriers across the junction, it aids in diffusing the minority carriers (a few free holes in the n-region and electrons from the p-region).

As such, when there is a zero net flux of holes, the Fermi level is constant when passing through the junction from the n region to the p. To enable further calculation of the characteristics of the depletion region, it is assumed that the concentrations of the carriers within the two regions are negligible in comparison to the ionised acceptors and donors within the depleted region.

When a positive voltage (V_r) is applied to the n-type region and a negative to the p region, a reverse bias condition is induced. Electrons are attracted to the positive electrode and holes towards the negative, both carriers moving away from the junction. This results in an increase in the depletion layer due to the lack of charge carriers producing a high impedance path, resulting in a high potential barrier preventing current from owing through the semiconductor material. It is important to note that a small leakage current can flow through the junction.

When the reverse bias is small, the depletion width remains mostly constant, however when the applied voltage increases such that a positive voltage (V_r) very large, the depletion region also increases with V_r. In comparison, when a negative voltage (V_f) is applied to the n-type region, a diode operates in forward bias. The variation within the electrostatic potential is reduced when compared to an equilibrium leading to a reduction in the depletion region. Large currents, many orders of magnitude higher than those seen in the reverse-bias case, flow through the p-n junction.

2.3.1 Metal-Oxide-Semiconductor (MOS)

The properties of the semiconductor can be further altered by the addition of capacitors such as the Metal-Oxide-Semiconductor (MOS) capacitor. Metal-Oxide-Semiconductors (MOS) are fundamental to many modern technologies. In essence, the electrical characteristics of a semiconductor can be controlled by biasing a metal gate. This biasing as a function of the voltage results in several different charge distributions. MOS capacitors form the foundation of CCDs, acting as light-sensitive "pixels". The MOS capacitor applies a potential to the gate electrode.

The MOSFET is a 4 terminal device consisting of a gate, body and source and drain terminals (see Fig.2.2). Ion implantations form these terminals

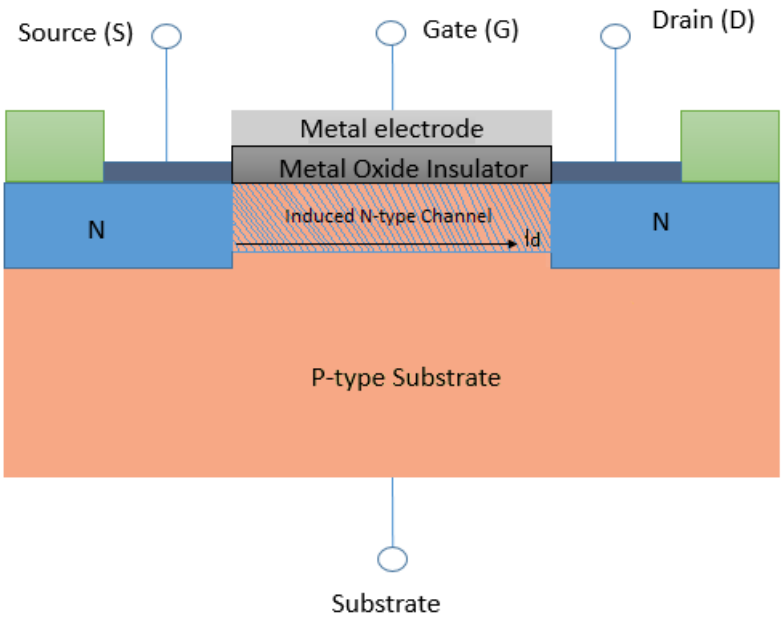

Figure 2.2: Labelled cross-section of Metal-Oxide-Semiconductor Field-Effect-Transistor.

or gates in regions where voltages are applied to the MOSFET. In modern CCDs, highly doped polysilicon is deposited by chemical vapour deposition. The gates are electrically insulated from the semiconductor channel by a thin layer of material, traditionally silicon dioxide. The application of different bias modes further alters the bias regimes and modes of operation of the device. The application of a negative potential to the gate electrode causes the semiconductor to leave its electrically neutral equilibrium and excess charge to accumulate. The gate's negative charge attracts the holes from the substrate to the silicon, silicon oxide interface (Si-SiO_2). A positive bias repels holes from the semiconductor-oxide interface, inducing a depletion layer in the silicon. A negative charge is left due to the ionised acceptor ions. Conduction occurs in the channel, and the gate potential controls the current flow by altering the charge carrier concentration. When the gate is positive with reference to the source, holes are repelled, producing a narrow n-type channel. This inversion layer acts as a highly conductive path from source to drain. Electrons flow from the source to the drain, and the magnitude of the current I_d is dependent on potential applied to the gate, and the mode of operation [50].

2.4 The Charge Coupled Device

The CCD is an integrated circuit on a semiconductor structure composed of an array of light-sensitive elements called pixels (see Figure 2.3). CCD's are based on a Metal-Oxide-Semiconductor capacitor (MOS) structure, which is light sensitive and can store charge. When photons are incident on the device, photoelectrons are generated, and charge is stored in the potential wells under the electrodes. By altering the biasing applied to the electrodes, this potential well can be moved through the device, and the charge collected and measured, producing a recorded image. The basic CCD structure consists of an array of closely spaced MOS capacitors on an oxide layer (insulator) that covers the semiconductor substrate. Silicon epitaxial-grown wafers are used for the majority of CCD image sensors due to the epitaxial layer achieving good doping uniformity and high purity.

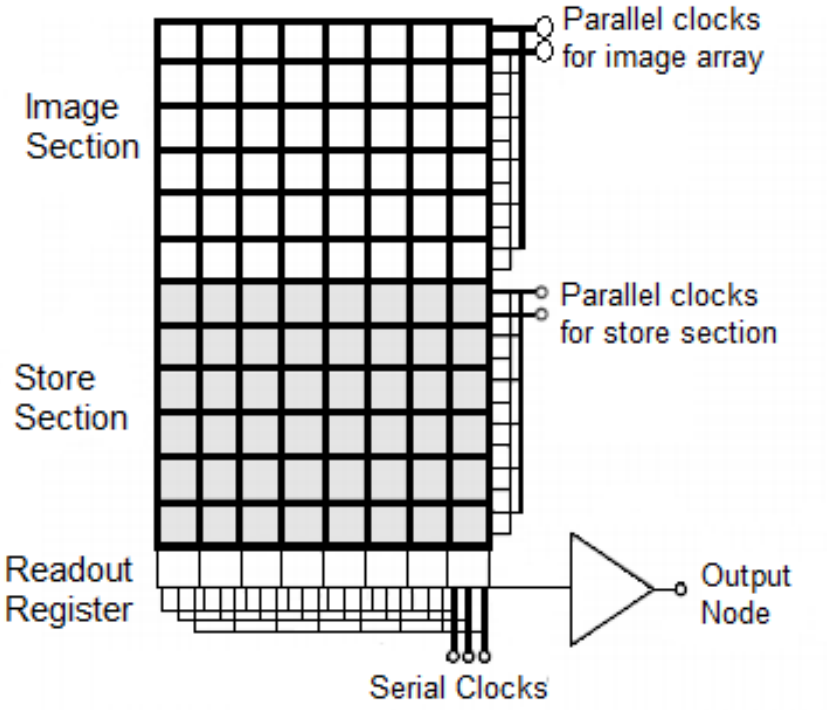

Figure 2.3: Schematic of a frame transfer CCD. Each square in the image and store section represents a pixel; the number of horizontal and vertical pixel differ depending on CCD architecture

2.4.1 Fabrication Process

The fabrication process of CCDs happens in several stages. The p-epitaxial silicon layer is grown on p-type silicon substrate. The next step in the formation of the n-type buried channel by the implantation and thermal annealing. The p+ stops are implanted prior to the formation of the gate electrodes and act to confine the extent of the buried channel. Polysilicon is then deposited on the gate oxide and doped. After oxidation of the first polysilicon, up to three more polysilicon layers are deposited, patterned and doped to form the gate electrodes. N-type implants are then used to define the output transis-

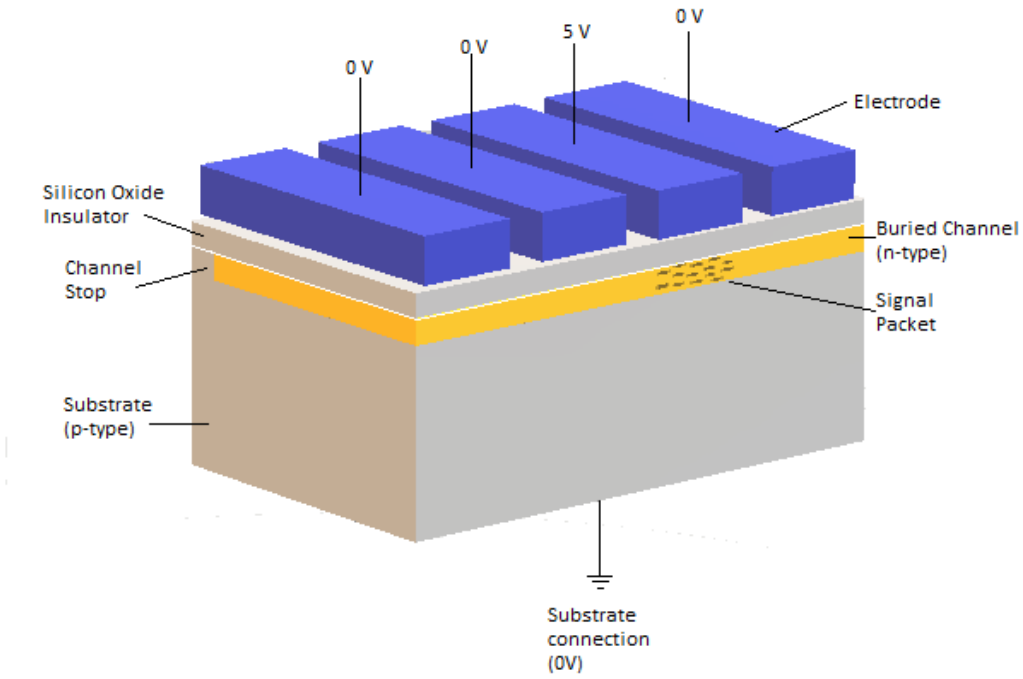

Figure 2.4: Section of a buried channel CCD with 4-phases adapted from [11] with the major components labelled.

tors. Finally, aluminium is deposited by sputtering to form the connections. The wafer is annealed in a hydrogen environment at a temperature of 400 ^{o}C to passivate the interface traps.

CCDs can have several different architectures including full-frame, frame transfer and interline transfer. The electrodes define the pixel rows while the gaps in the buried channel act as channel stops and define the columns within the pixel matrix. Furthermore, they prevent the spread of charge between the columns. In a simple CCD structure, demonstrated in Figure 2.4, a single

pixel is formed from three electrodes connected to three separate clock drivers, called phase-1 (P1), phase-2 (P2), and phase-3 clocks (P4). An array of these pixels form the imaging area of the device. By utilising at least three phases (4-phase devices as seen in Fig.2.4 and 2-phase are also possible) on the device, it is possible to isolate the pixels during the operation of the device by applying a set of similar but time-shifted pulses (clock pulses). Buried channels employ a depletion region to separate e-h pairs formed via photogeneration and allows for the potential under the gate to be controlled, however the width of the depletion region that forms naturally with a pn junction increases with the application of a positive gate substrate voltage forming a buried channel. The mobile electrons are attracted to the gate electrode, and holes pushed towards the substrate.

The buried channel was developed as it offered several advantages over the original surface channel; it is not affected by surface trapping, thus increasing the charge transfer efficiency, offers an increase in the operating frequency and results in an increase in the bulk mobility compared to that of the surface charge mobility [13]. Subsequently, buried channel devices have replaced the surface channel as the industry standard.

This moves the collection point of the photoelectrons from the interface to just below the interface (within the buried channel), away from any trapping centres at an approximate distance of $\sim$0.5 μm from the surface. The potential gradient of the buried channel structure (see Fig.2.5) can be calculated as a function of the electric field through the oxide and buried channel. Figure 2.5 denotes three major regions of the CCD: the silicon oxide layer, the buried channel and substrate. The one-dimensional potential distribution is found by solving Poisson's differential equations, assuming depletion approximation, for each of the three regions

$$\frac{\delta^2 V}{\delta x^2} = 0 \text{ for } d < x < 0 \tag{2.1}$$

$$\frac{\delta^2 V}{\delta x^2} = \frac{-qN_d}{\epsilon_{Si}} \text{ for } 0 < x < t \tag{2.2}$$

$$\frac{\delta^2 V}{\delta x^2} = \frac{qN_a}{\epsilon_{Si}} \text{ for } t < x < t + x_p \tag{2.3}$$

where t is the n-channel depth, x_p is the depletion depth, V is the potential, x is the distance through the cross-section from the surface, d is the depth of the oxide layer, ϵ_{Si} is the relative permittivity of silicon, N_a is the acceptor

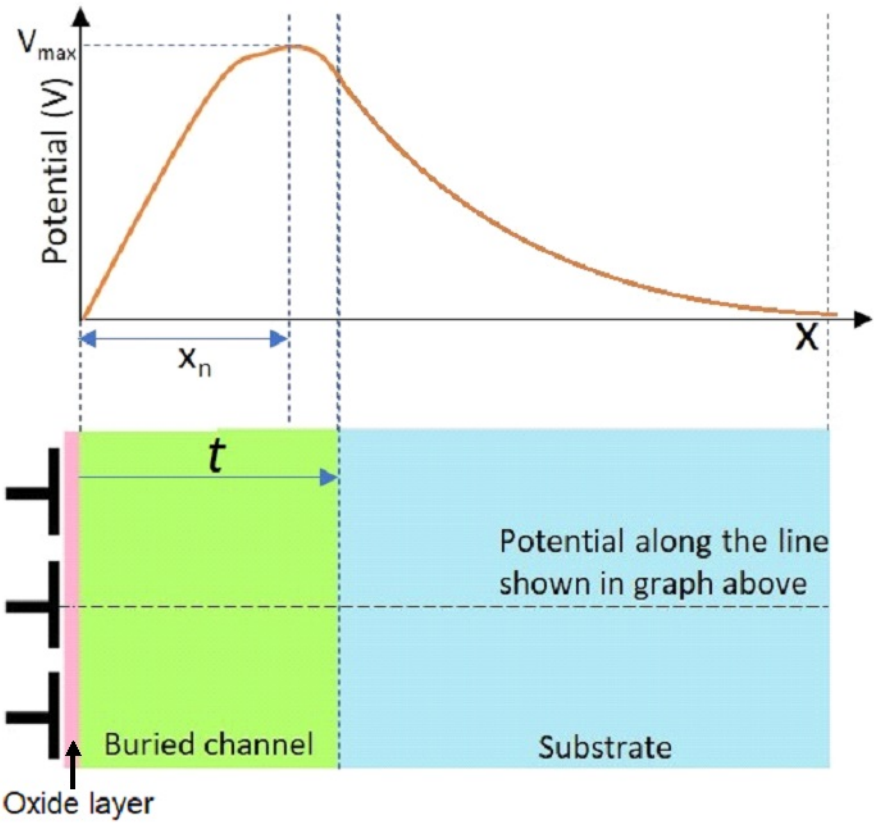

Figure 2.5: The potential through the cross-section of the thickness of CCD.

doping concentration and N_d is the donor doping concentration. For the oxide region of the device ($d < x < 0$), the solution to the differential equation is given by

$$V_{OX} = V_G - V_{FB} - E_{OX}(x + x_{OX}) \tag{2.4}$$

where V_G is the applied voltage at the gate electrode, V_{FB} is the flatband voltage, E_{OX} is the electric field through the oxide and x_{OX} is the distance through the oxide. For $0 < x < t$ the solution is

$$V_t = V_{max} - \frac{qN_d}{2\epsilon_{Si}}(x - x_n)2 \tag{2.5}$$

where V_{max} is the potential maximum of the channel and x_n is the distance to the potential maximum from the p-n junction.

Subsequently, the channel potential maximum is given by

$$V_{max} = V_J\left(1 + \frac{N_a}{N_d}\right) \tag{2.6}$$

where V_J is the junction potential. Its location with the channel is given by [56]

$$x_n = t - x_p\left(\frac{N_a}{N_d}\right) \tag{2.7}$$

where x_p is the p-region depletion depth given by

$$x_p = \sqrt{\frac{2V_J\epsilon_{Si}}{qN_A}} \tag{2.8}$$

Subsequently, the maximum depletion depth under the gates (V_G) is given by

$$x_p = \sqrt{\frac{2\varepsilon_{SI}(V_G - V_{SS})}{qN_a}} \tag{2.9}$$

where V_{SS} is the voltage at the substrate. The depletion depth is an important consideration as the depletion region is devoid of electrons; subsequently, any electrons that then appear in the potential well can be assumed to be photoelectrons. A thicker depletion region also minimises the risk that the penetration depth of the radiant energy is greater than the depletion depth generating charges in a neutral region of the substrate. These charges can then spread out due to diffusion effects and result in the degradation of the resolution of the image.

2.4.2 Front and Back Illumination

Image sensors can be illuminated from either the front or backside of the device. A front-illuminated device requires incident photons to pass through the electrode structure before interaction with the active silicon. The penetration depth is dependent on the material through which the photon is passing and the energy of the incident photon. Highly energetic photons can travel further through the sensor, with the potential for photons to pass directly through the device without interacting.

Back-illuminated CCDs are manufactured by reversing and thinning the silicon wafer, such that photons are directly incident on the photosensitive layer and do not have to pass through the electrodes. Back-illuminated sensors can improve the quantum efficiency (QE), which is the ratio of the quantity of charge carrier collected compared to the number of incident photons.

2.4.3 Device Operation

The operation of the charge-coupled device can be separated into four stages: charge generation, charge collection, charge transfer and the detection of the charge.

2.4.3.1 Charge Generation and Photoelectric Effect

During the charge generation stage, the external stimulus or input signal is converted to an internal electric charge that can be detected as an electric signal via the photoelectric effect. The photoelectric effect is the interaction of an incident photon with an electron within the valence band (see Fig.2.6). The electron gains sufficient energy to be liberated to the conduction band and generating an electron-hole pair.

This process requires an energy greater than the band gap of silicon, 1.12 eV at 300 K [61]. While the band gap of silicon is 1.12 eV, 3.6 eV is actually required to ionise an atom, as crystalline silicon has an indirect band gap. An indirect band gap requires higher energy for charge excitation because energy and momentum must be conserved. Electron-hold pairs which are generated by a photon energy greater than 3.6 eV are described as directly ionised [6]. Photons with an energy lower than 3.6 eV can still liberate an electron by using energy within the lattice in a process called indirect ionisation. Photons with an energy greater than 4.5 eV are capable of creating more than one electron-hole pair [95].

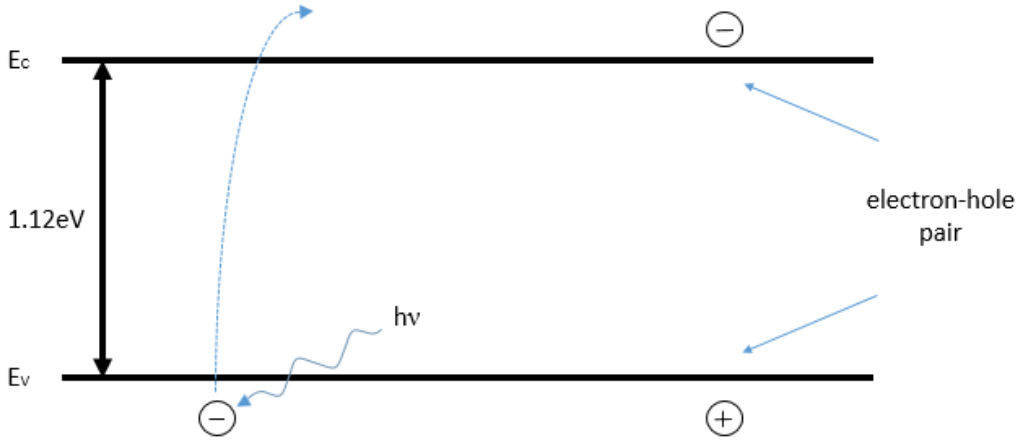

Figure 2.6: The photoelectric effect where an electron is excited from the valence band to the conduction band after interacting with an incident photon.

The reverse of this process, involving annihilation of electron-hole pairs, is recombination. As silicon is an indirect semiconductor, the dominant recombination process occurs via localised states in the band gap. This process is known as the Shockley-Read-Hall recombination [98].
There are four basic SRH processes:

- An occupied trap emitting an electron to the conduction band
- An occupied trap capturing a hole from the valence band
- A neutral trap captures an electron from the conduction band
- A neutral trap captures an electron from the valence band, leaving a hole.

It is possible to determine the change in level occupation or defect energy level and subsequently, the rate of electron capture. For further information pertaining to trap recombination please refer to [98, 55, 19]. It is sufficient to say that the capture and emission time constants are the inverse of the capture rates and that emission time constants are highly temperature sensitive.

When an electron is liberated, a hole is formed which has lower mobility than the electron but can still move within the lattice. The work function ϕ, the energy required to remove an electron to infinity from the atom, is given by

$$\phi = hf - E_k \tag{2.10}$$

where h is Planck's constant, f is the frequency of the incident light and E_k is the maximum kinetic energy of the ejected photons. The energy of the incident photon (E_p) is given by

$$E_p = \frac{hc}{\lambda} \tag{2.11}$$

where c is the speed of light and λ is the wavelength. For photon energies above 50 eV the mean electron number (η) excited to the conduction band can be calculated from

$$\eta = \frac{E_p}{E_e} \tag{2.12}$$

where E_e is the ionisation energy equal to 3.6 eV at room temperature. Due to this ionisation process, it is possible for an X-ray source of photons with energies of the magnitude of ∼keV to generate a mean number of electron-hole pairs in the order of 10^2 to 10^3 according to equation 2.12. The path of the electrons is random due to the interaction of the electron with acoustic phonons. When an electric field E is present, there is an additional drift velocity component u_d to the random motion

$$u_d = \mu_n E \tag{2.13}$$

where μ_n is the mobility of electrons. The electrons increase their kinetic energy while passing through the field. At high electric fields, the drift velocity saturates.

To produce an image, the photoelectrons are captured within a potential well after their generation. The number of generated photoelectrons is proportional to the number of absorbed photons [133]. The attenuation of incident photons follows the Beer-Lambert law

$$I(z) = I_0 \exp(-\alpha(\lambda)z) \tag{2.14}$$

where I is the remaining photon intensity at depth z, α is the absorption coefficient and I_0 is the original intensity. Thus, it follows that the probability of a given photon being absorbed (P) is dependent on the thickness z of the material through which it is travelling.

$$P(z) = 1 - \exp(-\alpha(\lambda)z) \tag{2.15}$$

With this knowledge, it is possible to model electron generation. At high energies, the absorption of photons is dependent on nuclear processes. The

absorption probability of high energy photons is also dependent on a number of other factors, including the Fano effect [33]. When a high energy photon releases a high energy electron, it may have sufficient energy to ionise further atoms resulting in a cascade process.

2.4.3.2 Charge Collection

Charge collection is determined by the potential structure of the pixel. The majority of modern scientific CCDs are based on n-channel structure, which results in the electrons being collected (in a p-channel device, holes are collected) in a potential well beneath one or more gates within a pixel. Initially, each pixel in the sensor array functions as a potential well, storing the charge during collection. Both negatively charged electrons or positively charged holes can be accumulated (depending on the CCD design), the charge carriers generated by incident light are usually referred to as photoelectrons.

At least one gate is biased to act as a barrier between the pixels to ensure that electrons only collect within one pixel. The channel-stops prevent charge spill-over between columns.

2.4.3.3 Charge Transfer

Once the charge has been collected under a gate, the charge is transferred towards the output node for measurement (see Fig.2.3).

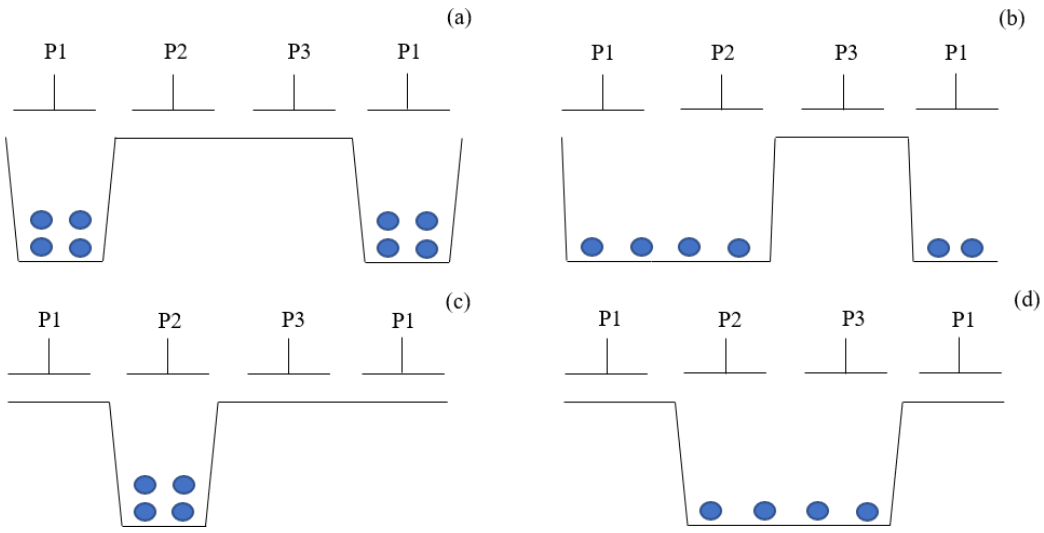

Figure 2.7: A classic clocking scheme utilised for a 3-phase CCD.

This is achieved by transferring the charge from one phase to the next within a pixel. A common clocking scheme for a 3-phase device is demonstrated in Figure 2.7. One phase within the pixel is held at a high potential (Fig.2.7 (a)), typically +10 V. The adjacent phase is then biased to the same value and the charge spreads across both phases (Fig.2.7 (b)). The potential of the first phase is then reduced, and the charge is fully transferred to the second phase (Fig.2.7 (c)). This process is then repeated for the third phase and all subsequent pixels (Fig.2.7 (d)). The holes within the device are attracted to the substrate and are not collected in an n-channel device.

Once the charge has been moved through the device, it must be readout. It is possible to reverse the passage of the signal charges by altering the clocking of the phases, and the phases can be arranged differently, with 2 [118] and 4 phase [113] devices possible.

Parallel clocking describes the process of moving charge through the pixel area. The charge packet from each row reaches the bottom of the image area where it is transferred into the serial register. This serial register consists of a 1D array of gates and moves the charge towards the output node. The serial register must be read out in its entirety for a single parallel transfer. The speed of readout for this process determines the total readout speed of the CCD.

There are several common CCD architectures utilised in modern scientific CCD technology, Figure 2.8 shows three of these structures.

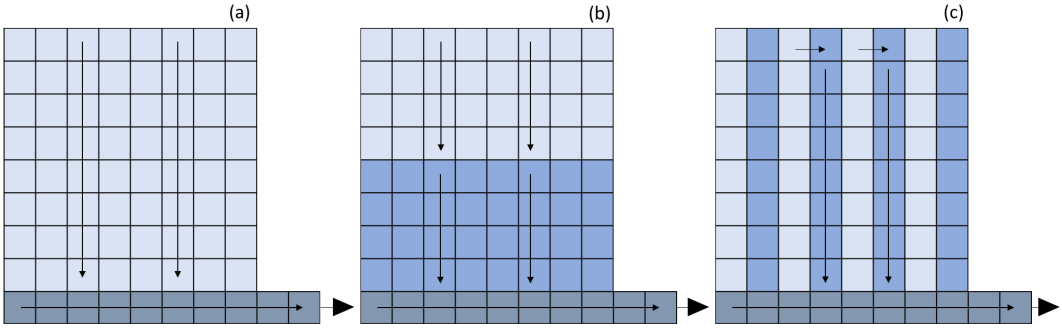

Figure 2.8: Three common CCD architectures: (a) Full Frame Transfer, (b) Frame Transfer and (c) Interline Transfer

The simplest of these is the Full Frame Transfer (see Fig.2.8 (a)). The entire image area is photosensitive, and after each integration, the charge is

transferred vertically along the columns, through the parallel register to the serial register. Smearing is a major disadvantage of this structure, due to further light falling on the sensor during readout. This can be overcome by implementing a mechanical shutter which covers the sensor during the readout. These shutters can be slow and become unreliable after extended periods of operation.
In a frame transfer structure, a store region is implemented below the image area (see Fig.2.8 (b)). After each integration period, the charge from the image area is transferred into the store region, allowing the device to integrate while the image is readout. The charge is then held in the storage region where no further signal is produced. This then allows the image section to accumulate a new measurement while the stored section is read out limiting smearing [128]. These devices often have faster frame rates that full-frame devices and have the advantage of almost constantly collecting light. However, to achieve the sensitivity of full frame transfer sensors, the device must often be larger to achieve equivalent image areas.

Interline CCDs are similar to the frame transfer structure in that a store region is utilised to increase the frame rate (see Fig.2.8 (c)). However, the charge is shifted horizontally into shielded parallel registers and vertically to the serial register demonstrated in Figure 2.8. The rapid image capture considerably reduces the image smearing. However, the interline masks lead to a significant reduction in the size of the light-sensitive area of the device.

2.4.4 Charge Measurement

Once the charge has reached the sense node, the charge stored within the potential wells must be measured. This almost exclusively involves converting the signal into a current or voltage. This is normally achieved with a floating diffusion output with reset but can be implemented without the reset [121]. Both utilise source followers to buffer between the floating diffusion and outside world.
The floating diffusion with reset is demonstrated in Figure 2.9 with DC-biased output gate (OG) (see Fig2.3) and n^+ floating diffusion. Using a reset transistor as a switch, the n^+ floating diffusion is connected to the positive supply voltage (V_{DD}) and is controlled by the reset pulse to Reset Gate (RG). A charge packet is initially stored beneath phase 3 (P3) while RG is held high

and a barrier phase (V_{DC}) to separate charge from the floating diffusion. At this point in time, the floating diffusion is connected to V_{DD} and is at its reset voltage. The reset switch then opens, and the diffusion 'floats'. Due to a small amount of clock feedback, the voltage on the FD decreases slightly.

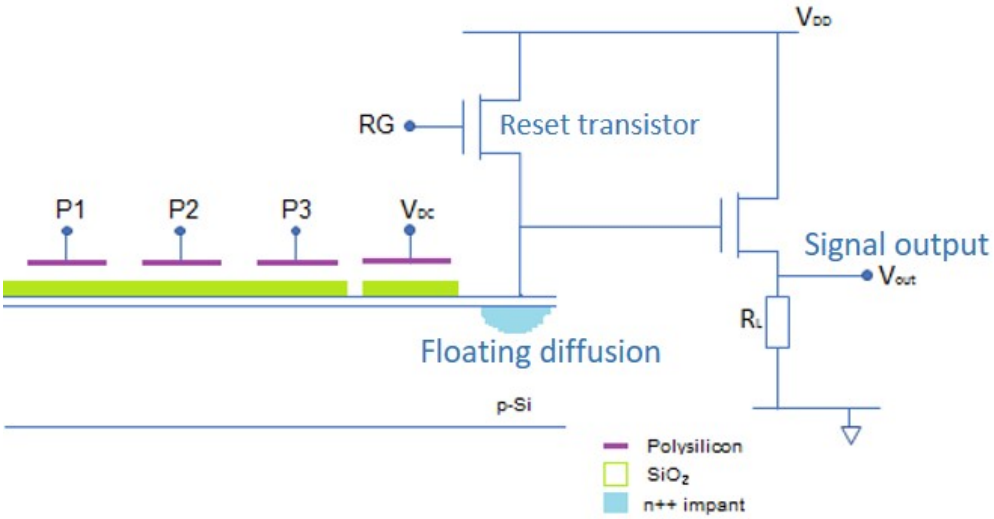

Figure 2.9: Circuit schematic showing the readout register and floating diffusion with reset of a CCD.

P3 is then lowered, and the charge is transferred over the OG to the floating diffusion. The voltage on the floating diffusion is then sensed by a single stage source follower. The increased number of electrons on the floating diffusion capacitance further lowers its potential. This change is mirrored by a proportional change in the V_{out} voltage equal to

$$V_{out} = \frac{qn}{C} \tag{2.16}$$

where q is the charge, n is the charge density, and C is the capacitance. The reset clock is then utilised to clear the floating diffusion of charge once the change in the voltage has been recorded. The reset transistor is switched on, sweeping the charge from the sense node (same as floating diffusion) to the drain and resetting the node to the drain voltage. When the reset clock is 'switched-off' the sense node stabilises, and it is then possible for the next charge packet to be transferred to the sense node.

2.5 Electron Multiplying Charge-Coupled Device

Electron multiplying charge-coupled devices described by e2v technologies [57] and Texas Instruments in 2001 and first proposed in 1983 [74], aim to increase the signal above the amplifier noise. The EMCCD is similar in design to a conventional CCD but with the addition of a multiplication gain register between the readout register and the output node (labelled in Figure 2.10). This gain register implements impact ionisation increasing the number of electrons within each charge packet [57] and hence produces a signal gain and an increased signal to noise ratio.

The multiplication register contains a gate that can be operated at a high voltage, traditionally in the range of ∼40-50 V, which is called a high voltage phase (P2HV), and an additional phase, P2DC which acts as a barrier phase sitting between P1 and P2HV (see Fig.2.11).

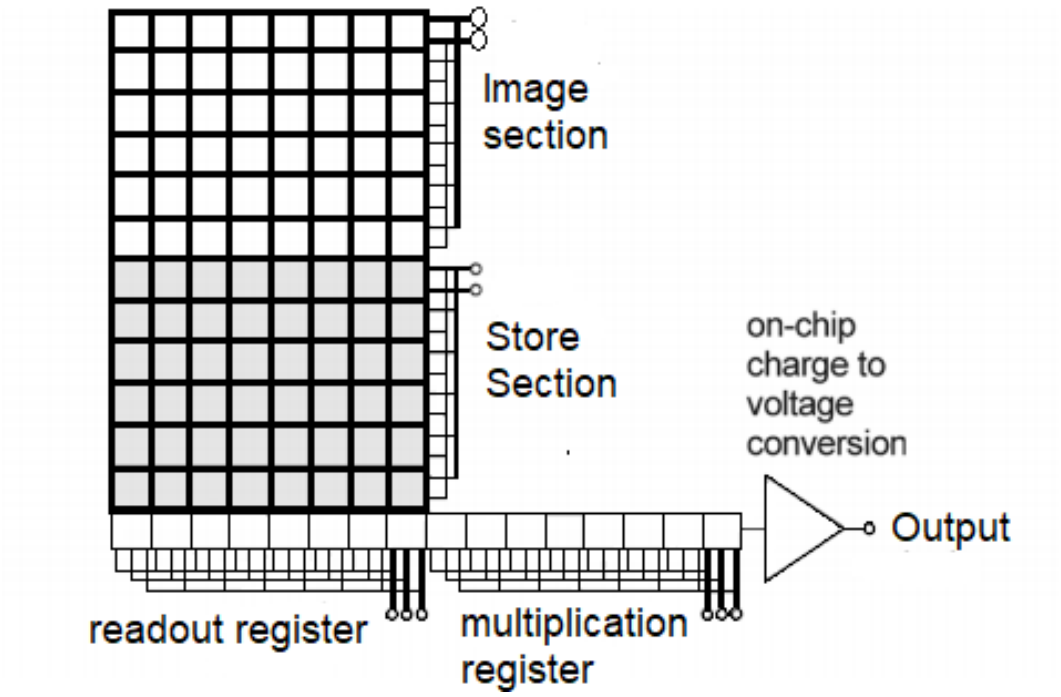

Figure 2.10: Schematic of a traditional Electron Multiplying Charge-Coupled Device adapted [reprinted] from [92].

Electrons enter a high electric field region between the P2DC and P2HV

and are accelerated. Some of these accelerated electrons have sufficient energy to generate electron-hole pairs in the silicon lattice. The process of increasing the number of e-h pairs through lattice collisions is called avalanche multiplication [36]. The impact ionisation coefficients for holes and electrons depend on the electric field. Different models for the impact ionisation parameters, including the rate of impact ionisation can be found in literature [89].

The multiplication register (gain register) contains four phases. Two of these phases are identical to the ordinary register (P1 and P3). The charge packet is initially collected beneath P1 while the potential of P2HV increases to full potential. P2DC is held at a constant low potential in relation to the substrate ($\sim$ 3 V) and acts as a barrier phase preventing charge flowing into P2HV before a maximum potential has been reached. The P1 gate potential is subsequently reduced to 0 V, and charge can flow into the potential well beneath the P2HV gate, experiencing impact ionisation in the high field region between P2DC and P2HV. The region of high electric field between P2DC and P2HV is a result of the potential gradient between the two gates. The charge packet is then clocked into P3, and the process repeats for each stage in the gain register, normally $\sim$ 500 stages [116].

The total gain (G) is dependent on the potential difference between P2DC and P2HV and number of elements (stages) in the gain register (n). The total gain can be calculated from [57]

$$G = (1 + g)^n \tag{2.17}$$

where g is the mean gain per element. The probability that an e-h pair is generated is small, and the mean gain per element is of the order of 10^{-2}; however, there are many elements in a gain register enabling high gains to be reached.

The gain in the signal occurs before the device readout and the readout noise is independent of the signal size, effectively improving the signal-to-noise-ratio (SNR).

2.5.1 Factors affecting EM Gain and SNR

The EM gain is known to be affected by a number of factors including the device clocking, temperature range and a decrease in gain with time, called ageing, among others.

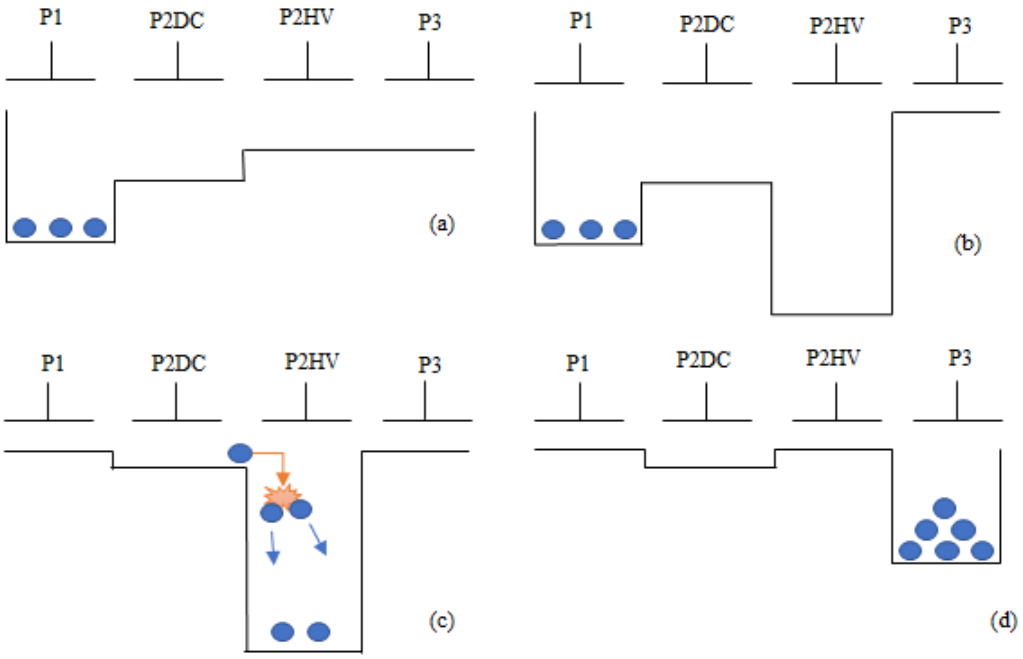

Figure 2.11: EMCCD operation. The charge is initially held under the P1 gate (a). A region of high field is established (b). Impact ionisation occurs as the charge is transferred between P2DC and P2HV (c) before the signal is then moved out to the next multiplication element (d) adapted from [26].

2.5.1.1 Effect of photon energy and EM gain on SNR ratio

The gain produced by an EMCCD is stochastic, and as such, the achieved gain is an average of the true gain. The probability distribution of the output signal for an input signal of n is given by

$$p(x) = \frac{x^{n-1} exp(-x/g)}{g^n (n-1)!} \tag{2.18}$$

where g is the mean gain and when the photon input is small with a large gain. This distribution trends towards Gaussian at high signals and produces a mean of ng and a variance of ng^2. As such, the noise is independent of the energy of the input photon. When the number of input electrons is large enough, the gain distribution can be considered Gaussian, and as such, the shot noise can be defined as

$$\sigma_{shot} = \sqrt{\frac{E}{E_e}} \tag{2.19}$$

where σ_{shot} is the shot noise, E_e is the ionisation energy, and E is the magnitude of the input signal packet. The total noise can then be acquired if it is assumed that the only noise sources are from the readout amplifier (σ_{out}), the shot noise on the initial photon interaction (σ_{shot}) (see Eq.2.19) and the gain noise. It is of interest to note that due to the photon Poisson distribution, the shot and gain noise are proportional to $\sqrt{n_e}$ where n_e is the signal collected by the device in electrons, for optical photons [1]. It is possible to obtain the SNR (S/N) by combining the noise from the multiplication process and the noise due to the Poisson nature of light,

$$\frac{S}{N} = \frac{n_e}{\sqrt{\alpha n_e + \beta n_e + (\frac{\sigma_{read}}{G})^2}} \tag{2.20}$$

For large gain values the read noise (σ_{read}), can be considered to be suppressed and as such the SNR ratio can be simplified to

$$\frac{S}{N} = \frac{\sqrt{n_e}}{\sqrt{\alpha + \beta}} \tag{2.21}$$

In the EMCCD, there is an additional noise contribution called Excess Noise Factor (ENF) discussed by Hynecek [51]. This is due to the stochastic nature of EM gain and has been calculated by Robbins [92]

$$ENF = \frac{1}{g}\left(\frac{2g + P - 1}{P + 1}\right) \tag{2.22}$$

where P is the probability that a multiplication event will occur. This result essentially replicates those found by Hollenhorst [47], and Matsuo [75] who analysed the noise for cascaded multiplication devices and a staircase avalanche photodiode, respectively. It has been shown theoretically that the ENF tends to 2 as the gain increases [92]. It is possible to rewrite the total noise of an EMCCD in the form of

$$\sigma_{tot}^2 = \frac{\sigma_{read}^2}{G} + ENF\sigma_{dark}^2 + ENF\frac{E}{E_e} \tag{2.23}$$

when G is large, the ENF tends to 2.

As EM gain increases, the SNR improves. However, Equation 2.23 demonstrates that there is an increase in the noise due to ENF. Furthermore, the ENF acts on not only the multiplied electrons but also the dark signal that has accumulated before multiplication.

[1] This thesis focuses on optical photons however X-rays were used to characterise the device

2.5.1.2 Temperature Dependence

Cooling an EMCCD not only reduces the dark current but also increases the EM gain (see Figure 2.12). This is due to the impact ionisation coefficient increasing as the temperature decreases, a result of reduced phonon scattering [24]. The magnitude of the energy of the phonon is dependent on the temper-

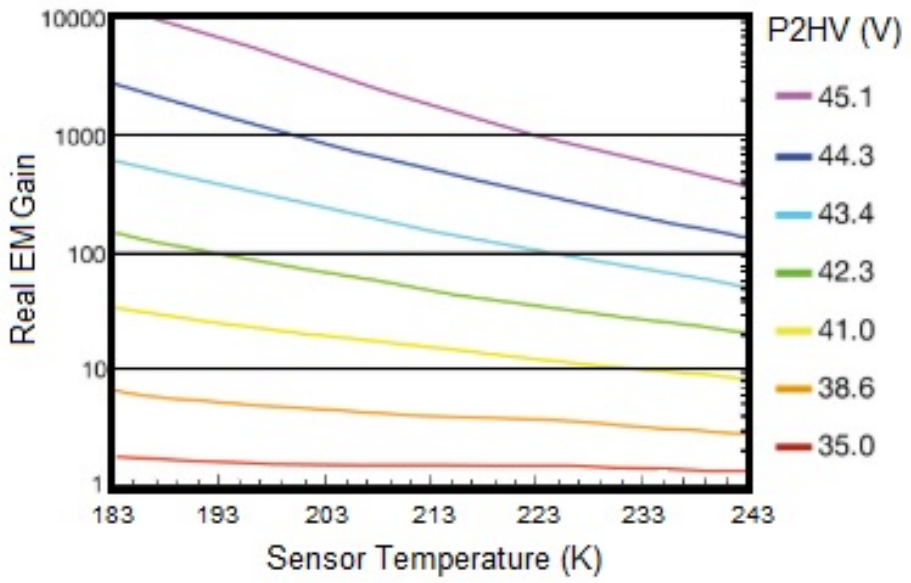

Figure 2.12: The EM gain as a function of temperature for several EM clock voltages for Andor EMCCD camera. Adapted [reprinted] from [84]

ature; at higher temperatures, the magnitude of the phonon's energy is higher. Subsequently, the larger the phonon energy, the higher the probability of electron scattering, reducing the energy available for impact ionisation [123, 108]. The average phonon number is temperature (T) and frequency (ω) dependent and given by

$$< n >= \frac{1}{exp\left(-\frac{\hbar\omega}{k_B T} - 1 \right)} \tag{2.24}$$

where $\hbar$ is the reduced Planck's constant and k_B is Boltzmann's constant. The effect of temperature is small; however, cooling results in reduced phonon scattering and a reduced phonon number. As discussed previously in this thesis, cooling also results in a reduction of dark current, enabling the optimisation of EM gain for photon counting.

2.5.1.3 Ageing Process

EMCCDs experience a decrease in the gain during the operational lifetime of the device. This is most notable during the initial operating period of the device (the first few hours) before the rate of reduction of the EM gain decreases with time. Teledyne e2v, among other companies, 'burn-in' the device to provide customers with a more stable EM gain. The physical processes behind this ageing have been examined [31] but not fully understood. An in-depth discussion into the processes of ageing in an EMCCD, specifically an EMCCD in a CMOS process is provided in Chapter 8.

2.6 CMOS Image Sensors

The CMOS sensor was initially developed concurrently with the CCD, and in many ways, the active pixel technology predates the more commercially successful CCD. However, the CMOS image sensor only became commercially viable with the development of the thin gate CMOS process in the 1990s. Since then the interest in CMOS images sensors has grown considerably, spurred on by the low fabrication and new technological developments. CMOS image sensors are now fabricated by a number of large foundries. Each process differs depending on the foundry, but it does follow the basic outline demonstrated in 2.13.

Both CCD and CMOS image sensors convert light into electric charge measuring the electric signal that they have processed. In CMOS sensor each pixel completes its own charge-to-voltage conversion and often also includes amplifiers, noise-correction and digitisation circuits. The circuits output digital bits. These functions increase the design complexity and often result in a smaller photosensitive region. However, the addition of backside illumination and microlenses, which can focus light counteract the smaller photosensitive region leading to increased efficiency. The device can also have the ability for pixel signals to be accessed directly and sequentially.

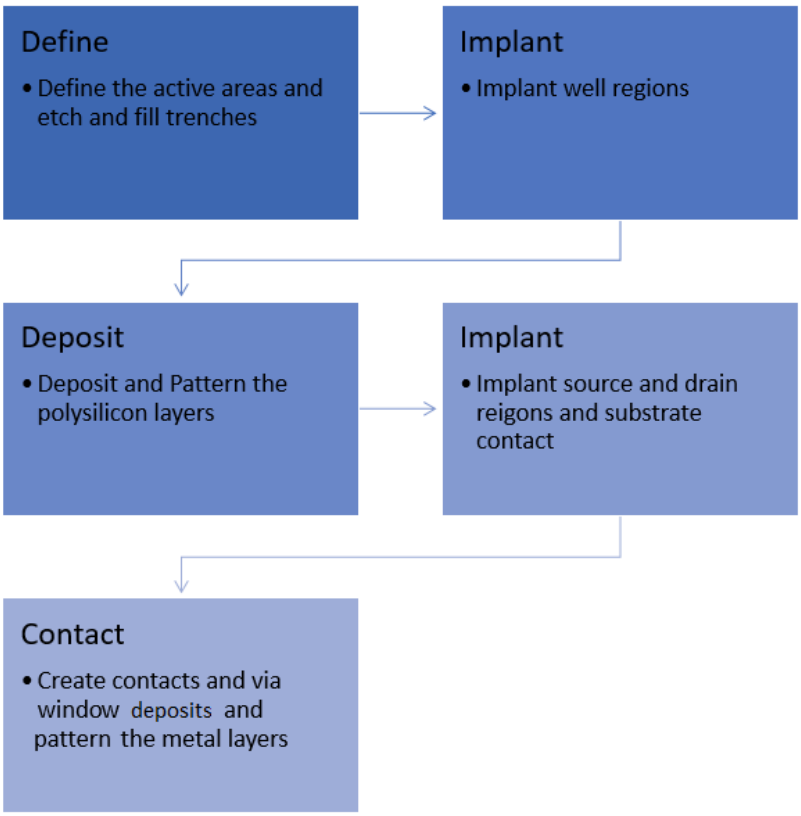

Figure 2.13: An overview of the CMOS fabrication process

Generally, CMOS image sensors have a number of advantages over the CCD image sensors:

- Able to read out different regions of interest independently
- A higher tolerance to pixel saturation
- Faster readout due to on-chip electronics
- A higher tolerance to radiation-induced damage due to the very thin oxide layer, the thinner the oxide, the lower the trapped charge, resulting in reduced surface damage. The bulk damage remains unchanged.

Furthermore, CMOS image sensors operate using a far lower power consumption, and they are generally less expensive to manufacture due to standard semiconductor fabrication. Lower power consumption is incredibility important when considering implementing image sensors in a restricted power environment such as Earth observation or Solar System missions.

2.7 EM in CMOS Devices

Recent developments in CMOS sensors have led to sensors with ultrahigh conversion gain and sub-electron noise; however, EMCCDs are still superior in many photon counting applications, including molecular imaging [67, 14]. The EM process is traditionally implemented in CCDs, though several devices with similar functionality have been implemented in the CMOS process [34, 97]. These devices benefit from smaller feature size possible due to the manufacturing process and allowing the introduction of additional features such as pinned photodiodes and reciprocating charge transfer [105]. Establishing the necessary high electric fields in CMOS devices is difficult due to the small operating voltages. Furthermore, simply increasing the electric field does not result in increased EM gain due to several secondary effects, including edge losses, blooming and voltage breakdown. Reducing the intergate gap can also result in an increase in the EM gain. To achieve the target EM gain, it is essential that a balance is achieved between the EM gain and the secondary effects.

EMCCDs suffer from several side effects of high gain, including clock-induced charge (CIC) and gain ageing [31]. CIC occurs due to parasitic impact ionisation in the multiplication register and the imaging area where high voltages are not implemented. Holes are accelerated towards the channel stops by the high electric field after they have been released from interface traps and undergo impact ionisation producing electrons as a parasitic charge. This effect can be reduced if the standard practice is utilised of enclosing the HV gate within the CCD buried channel (see Figure 2.14), well away from the channel stops.

Ageing, another detrimental side effect of EM gain has previously been attributed to hot carriers injected into the gate dielectric [31] (discussed in subsequent chapters) also affects the gain produced by the EMCCD. Both CIC and ageing are exacerbated by high electric fields due to the increased impact ionisation.

The high electric field traditionally requires high voltages limiting EM application to the CCD image sensor. However, in recent years EM has been implemented in CMOS imaging technology, a technology that traditionally utilises far lower voltages. This has been approached by several different research groups independently. One structure utilises a multi-gated pixel such

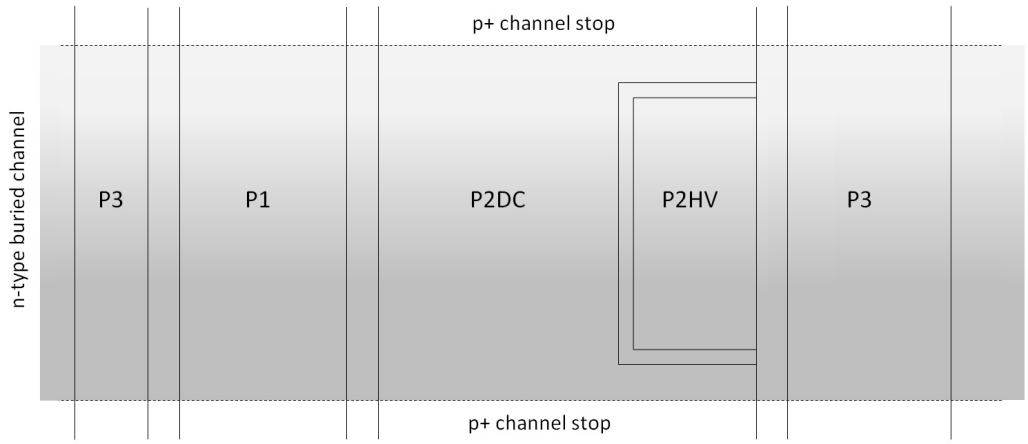

Figure 2.14: Cross section of EMCCD demonstrating the HV gate enclosed by the buried channel.

that charge is transferred between three electrodes removed from the photosensitive element [120], in another the charge circulates the photosensitive element in the pixel array such that the charge passes through at least one EM stage per loop [125]. The number of EMCMOS (or closely related) devices that have been reported is small and have limited details pertaining to device performance.

2.8 Chapter Summary

The main concepts behind signal generation, collection, transport and measurement have been described. The theories presented here form the basis of the design and characterisation of the device studied in this thesis. Subsequent sections of this thesis will provide insight into device properties and characteristics. The detector design of the EMTC1 is detailed in the next chapter.

Chapter 3

The Electron Multiplying CCD Test Chip 1

3.1 Introduction

This thesis focuses heavily on a novel technology that was developed to enable far superior gain at a lower gate voltage. This chapter focuses on the reasoning behind the design and main features of the Electron Multiplying Test Chip 1 (EMTC1), implemented in a CMOS process. The novel structures of several EM pixels are described, and the potential implications of these structures are discussed.

3.1.1 The ESPROS CMOS Process

The industrial standard CMOS manufacturing process has been discussed in Chapter 2; however, each foundry adapts the process dependent on their client's needs. The device studied in this thesis was produced at the ESPROS foundry. The EPC CMOS process is a 150 nm CMOS process with both 1.8 V and 5.0 V devices [29], and the process can be adapted for new optical detectors. It is possible to adapt 5.0 V devices for high voltage switching by utilising a 12.0 V class drain devices. The device can be developed to include back illumination and at its core is the ability to incorporate CCD modules in a CMOS process flow without limiting the device parameters. As such, it

is possible for advanced low voltage digital devices to be developed and the integration of digital processing, Analogue to Digital (A/D) conversion and voltage regulation over several voltage domains.

3.1.2 Electron Multiplication in EMTC1

The device studied in this thesis was developed with the aim of providing a high level of gain at a lower voltage. In a region with an ionisation rate of α_n, the increase of carrier concentration $n(x)$ over distance x is defined as

$$\frac{\delta n(x)}{\delta x} = \alpha_n(x)n(x) \tag{3.1}$$

The solution where $g(d)$ is the multiplication factor as a function of the distance d, $n(0)$ is the number of electrons injected at $x = 0$ and $n(x)$ is the number of electrons at x is given by

$$g(d) = \frac{n(d)}{n_0} = \exp\left(\int_0^d \alpha_n(x)dx \right) \tag{3.2}$$

where $\alpha_n(x)$ is ionisation rate (i.e. the number of pairs generated per distance travelled by an electron), which can be expressed as [74]

$$\alpha_n = A_n \exp(-b_n/E) \tag{3.3}$$

The parameters A_n and b_n are obtained empirically, and E is the electric field. The multiplication gain is exponentially dependent on the length of the EM region x.

When considering the region of the electric field, it can be assumed that the maximum of the electric field lies directly between the DC and HV electrodes at the shortest distance between the two gates. The field decreases towards the edges of the gate. As such, if the effective volume of the EM region, the density of the charge or the strength of the electric field are increased, the total gain increases too. If a number of these factors can be increased simultaneously, then the gain can be further increased.

3.1.2.1 Increasing the strength of the electric field

It is apparent from Equations 3.2 and 3.3 that the multiplication gain strongly depends on the strength of the electric field. The electric field is proportional

to the difference between the voltages of DC and HV gates. Subsequently, to increase the electric field, ever higher voltages are required which can be problematic in CMOS processes. As such, there are limitations on how high the electric field can be achieved by increasing the voltage. However, it is possible to increase the strength of the field in a small region or increase the overall volume where the electric field is highest.

3.1.2.2 Increasing the volume of the high field region

It is possible to increase the gain by increasing the volume of the high field region. This can be achieved by increasing the perimeter of the boundary between the HV and the DC electrodes. This leading-edge is orientated such that it runs along the maximum width of the HV electrode through which the charge carriers pass undergoing EM as they are transferred along the channel.

If the HV edge length is increased the electron path across the boundary between the electrodes is also increased, effectively increasing the volume of the high field region.

As described above, increasing the length of the boundary between the HV and the DC electrode can increase the length of the electron path. Normally this would mean simply increasing the width of the HV gate; however, it is possible to increase the length of the boundary by altering the shape of the gate.

3.1.2.3 Increasing the electron density

It is known, as discussed in Chapter 2, that the EM gain process is stochastic in nature, however the probability of impact ionisation events occurring increases with the magnitude of the electric field and electron current density according to Equation 3.4.

$$G_r = \frac{\alpha_n J_n}{q} \tag{3.4}$$

where G_r is the generation rate, J_n is the current density and q is the elementary charge. By altering the shape of the electrodes, the shape of the electric field will also be altered, and the charge can be directed to the centre of HV electrode, thus increasing its current density. A higher electron density leads to an increased electron-hole generation rate.

3.1.3 The EMTC1

The EMTC1 was developed to test the capabilities of EM technology in a CMOS process and to study several new EM pixel structures. The device was divided into 8 blocks, each consisting of 32 columns. The first two blocks utilise a normal 4-phase CCD structure without EM and serve as a reference. Four of the EM blocks utilise a traditional rectangular EM structure that varies in length and width. The size of each the pixel structures in each block can be found in Table 3.1. Blocks 7 and 8 contain pixel structures which differ in shape from the traditional HV electrode structure. These structures were patented along with several other novel gate structures which have yet to be tested experimentally [119].

Pixel Parameters			
Block	HV gate type	HV gate length (μm)	HV gate width (μm)
Block 1	4-phase CCD (No EM)		
Block 2	4-phase CCD (No EM)		
Block 3	Rectangular	3.0	6.0
Block 4	Rectangular	2.5	6.0
Block 5	Rectangular	3.0	5.0
Block 6	Rectangular	2.5	5.0
Block 7	Staircase	2.5-3.5	5.0
Block 8	Spike	1.6-2.6	5.0

Table 3.1: Table denoting each pixel shape and size for the EMTC1.Blocks 1 and 2 provide a reference.

3.1.4 Rectangular pixel structure

The rectangular pixel structure is the traditional EM gate structure utilised in many modern EMCCD devices. The leading edge in the rectangular HV gate is orientated such that it extends across the maximum width of the buried channel. It is across this boundary that the charge carriers undergo EM.

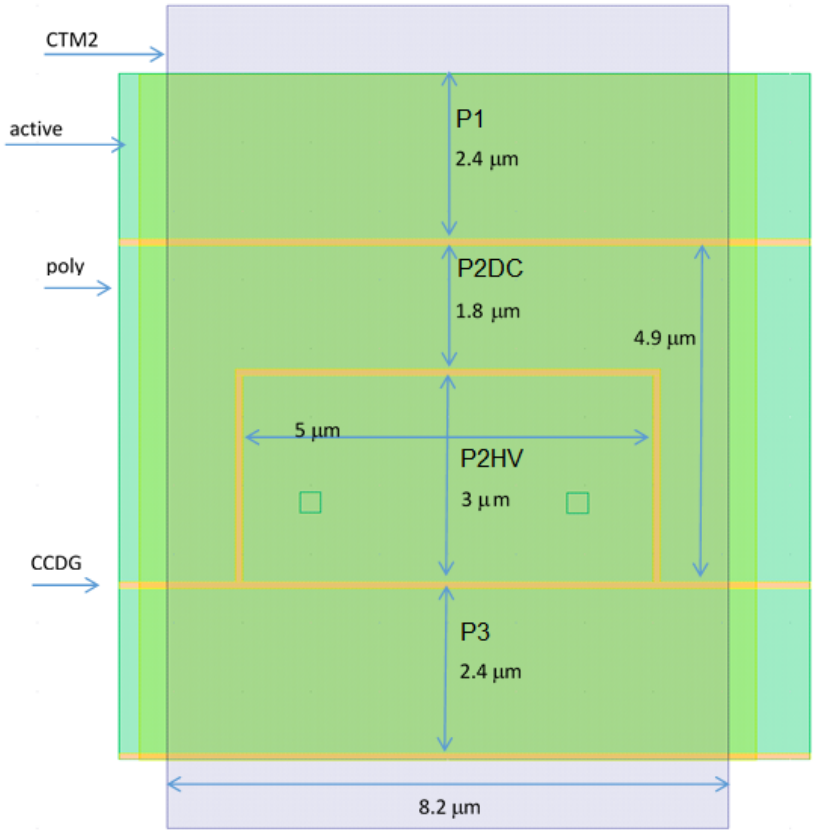

Figure 3.1: Top view showing EMCCD pixel variant 3 (Block 5) geometry where selected layers are shown. The CCDG defines the gap in the polysilicon, and the CTM2 defines the buried channel. The rectangular structure is similar to Blocks 3, 4 and 6 but these differ in length and width according to Table 3.1.

The P2DC electrode encloses the P2HV electrode above the channel stops. The dimensions of the electrode are normally dictated by the need to reduce high electric fields near the channels stops. Simulations have demonstrated

that the path taken by the electrons is nearly as wide as the leading edge of the P2HV gate [105]. Furthermore, the majority of the electron multiplication occurs at the centre of the leading edge of the P2HV gate.

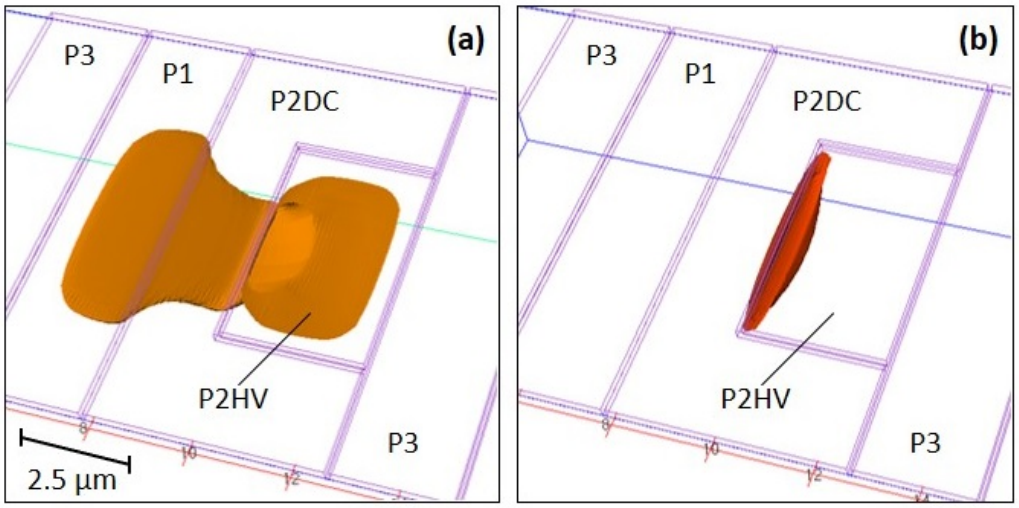

Figure 3.2: Simulation results for Block 5 (EM pixel variant 3). (a) Isosurfaces of electron concentration at 10^{12} cm^{-3} and (b) Impact ionisation rate at 10^{21} cm^{-3}s^{-1} with a signal of 900 $e-$ and at a moment of time when 50% of the charge has been transferred. The image denotes the location of the charge but assumes that the concentration is largely uniform across the EM gate. Image produced by a collaborator adapted [reprinted] from [105].

Figure 3.2 shows the simulations results for Block 5 for the electron concentration and impact ionisation when 50 % of the charge has been transferred. The charge and impact ionisation are spread along the leading edge; however, the pixel suffers from gain losses at the edge of the P2HV gate. Furthermore, the maximum of the impact ionisation region is focused at the midpoint of the leading edge.

3.1.4.1 Staircase pixel structure

The staircase arrangement demonstrated in Figure 3.3 is a castellated arrangement such that the leading edge of the HV gate is shaped with two protrusions mirrored on both sides of the electrode, with a stepped profile. The central

portion of the HV electrode is recessed. The electrode protrudes in a direction following the flow of the electrons when charge is transferred through the channel.

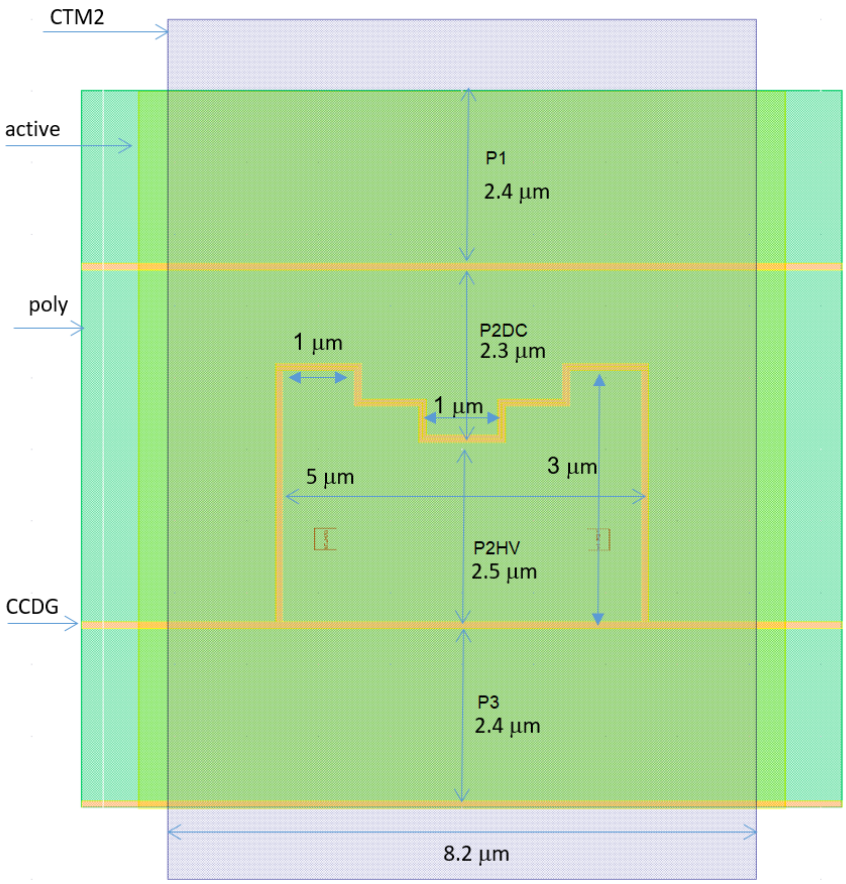

Figure 3.3: Top view of EMCCD pixel variant 5 (Block 7) also known as the staircase pixel structure. Selected layers are shown.

In this design arrangement, the leading edge of the HV electrode is considerably longer than in the rectangular HV electrode. Therefore, the ratio of the leading-edge length over the electrode area is much larger than in the rectangular structure. Simulations show that impact ionisation occurs along the entire leading edge [105].

Furthermore, when analysing the simulated path of the charge carriers in Figure 3.4, it is apparent that the area through which the electrons pass is far larger than that seen in the rectangular structure. Furthermore, any sharp changes in the direction of the leading edge can lead to an increase in the electric field strength. Combining these factors can lead to an increase in the

EM gain when compared to the rectangular gate structure. There are edge gain losses, but a high concentration leads to a large region of high impact ionisation.

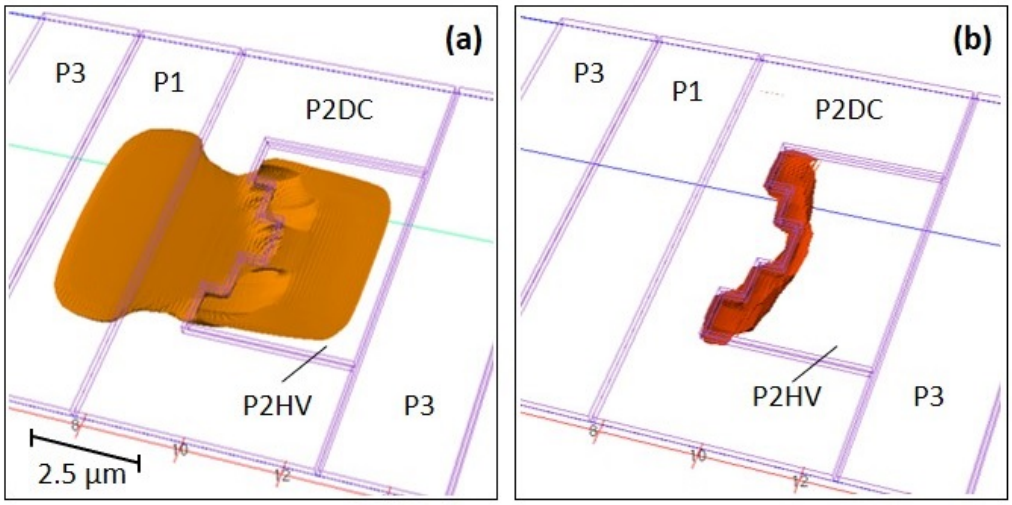

Figure 3.4: Simulation results for Block 7. (a) Isosurfaces of electron concentration at 10^{12} cm^{-3} and (b) Impact ionisation rate at 10^{21} cm^{-3}s^{-1} with a signal of 900 $e-$ and at a moment of time when 50% of the charge has been transferred. The image denotes the location of the charge but assumes that the concentration is largely uniform across the EM gate. Image produced by a collaborator adapted [reprinted] from [105].

3.1.4.2 Spike pixel structure

Block 8 contains an EM pixel structure which contains a single stepped protrusion that reaches across the channel from the HV gate and is mirrored across the channel with a similar protrusion extending from the DC gate. These protrusions extend such that the distance between the edge of the first clocked electrode and the edge of the HV electrode is reduced (see Fig. 3.5). Furthermore, the central protrusions from both gate structures align such that the gap between the clocked electrode and the high voltage electrode is at its narrowest along the central line that passes through the middle of the HV and clocked electrode.

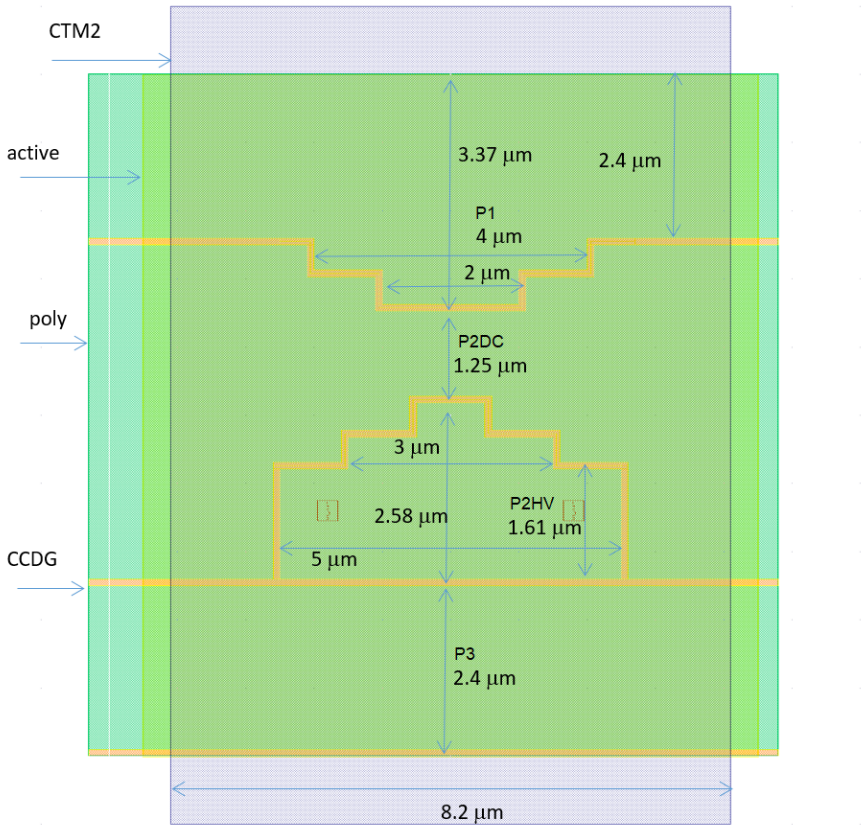

Figure 3.5: EM pixel variant 6 (Block 8). This is described as the spike pixel structure.

The progressive narrowing leads to a corralling of the charge through the funnel created between the two electrodes and the thinned DC gate. Subsequently, there is a substantial increase in the charge carrier density within this region demonstrated by the concentration of electrons in the centre of protrusion in Figure 3.6. Simulations demonstrating this electron density during the transfer process were published in [105].

Early simulations, before the fabrication of the EMTC1, demonstrated that the EM gain produced by these two novel pixel structures is significantly higher than that produced by a simulated rectangular structure.

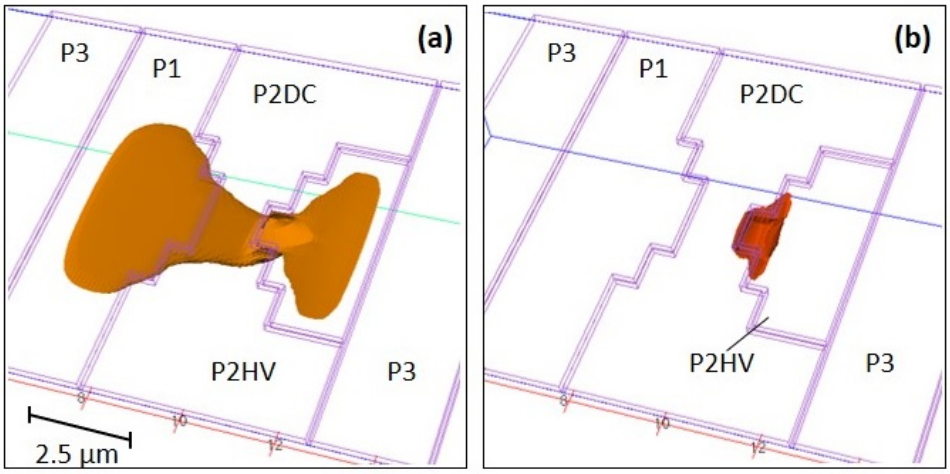

Figure 3.6: Simulation results for EM pixel variant 6 (Block 8). (a) Isosurfaces of electron concentration at 10^{12} cm^{-3} and (b) Impact ionisation rate at 10^{21} cm^{-3}s^{-1} with a signal of 900 $e-$ and at a moment of time when 50% of the charge has been transferred. The image denotes the location of the charge but assumes that the concentration is largely uniform across the EM gate. Image produced by a collaborator adapted [reprinted] from [105].

Due to an accumulated increase in the signal packet from each stage within the device, the increase in gain achieved by each novel electrode structure can lead to a substantially larger increase in the total gain.

These novel structures were selected from several other structures details of which can be found within a patent filed by Stefanov et al. 2017 [119]. These other designs have yet to be tested experimentally. The novel gate structures utilised in EMTC1 were simulated; however, it is not possible to obtain reliable quantitative data when simulating impact ionisation. As such, these two-pixel structures were tested experimentally in conjunction with previously described CMOS process technology. It was hypothesised that the predicted increase in EM gain would be large enough to ensure that the EM gain would be significant even at the lower voltages than those used in modern scientific EMCCDs.

3.2 Features of the EMTC1

The EMTC1 (see Figure 3.7) was fabricated using a 0.15 μm, 6-level metal, 1.8/5.0 V CMOS process by EPC, prior to commencement of the research presented in this thesis. It is a 4-phase buried channel CCD on 50 μm thick, high resistivity bulk silicon substrate ($\sim$ 10 kΩ.cm) which is fully depleted.

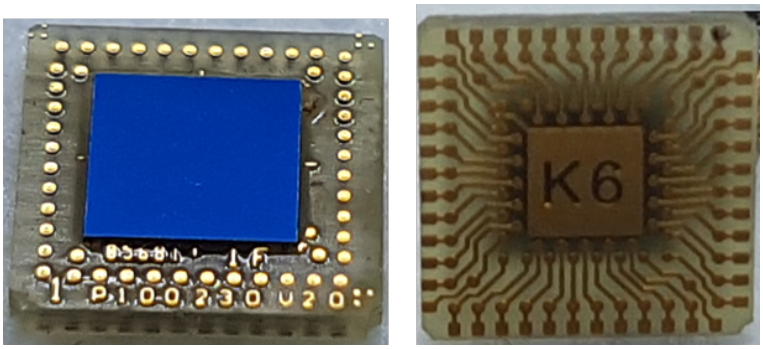

Figure 3.7: The front and back side of the EMTC1

The image sensor contains parallel columns on 10 μm pitch. The EPC 150 nm image sensor CMOS process utilises n-type buried channel CCDs in a p-type high resistivity substrate. The CCD gates are single-level polysilicon, and the interelectrode gaps are only 90 nm wide enabling high electric fields to be obtained at low operating voltages. Due to the low CCD channel potential ($\sim$ 1.5 V), it is only possible to use low voltage gate clock amplitudes (2-5 V).

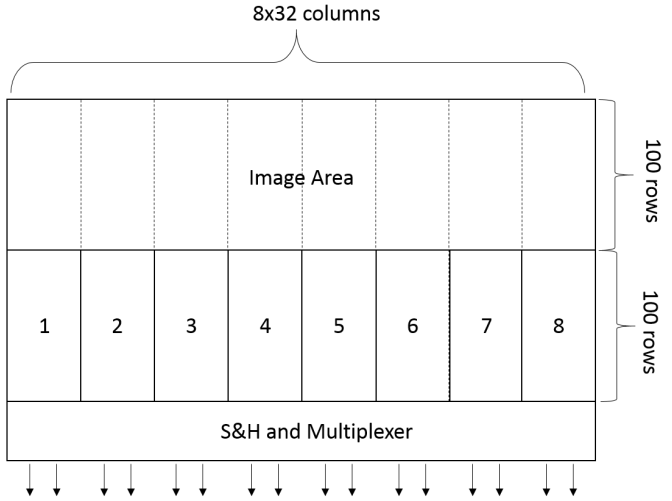

Figure 3.8: Simplified EMTC1 block diagram with each pixel variant numbered and the cross-section along the charge direction.

As described previously, the chip architecture enables direct comparison between different EM elements when operated simultaneously and under the same conditions (e.g. temperature, integration time biasing and clock times). The layout of the sensors can be found in Figure 3.8. The image area and the pixel variants in blocks 1 and 2 (see Table 3.1) have a four-phase CCD structure without EM elements, and the gates have a 2.5 μm pitch. Blocks 3 to 8 contain EM elements which vary in size and shape (see Table 3.1).

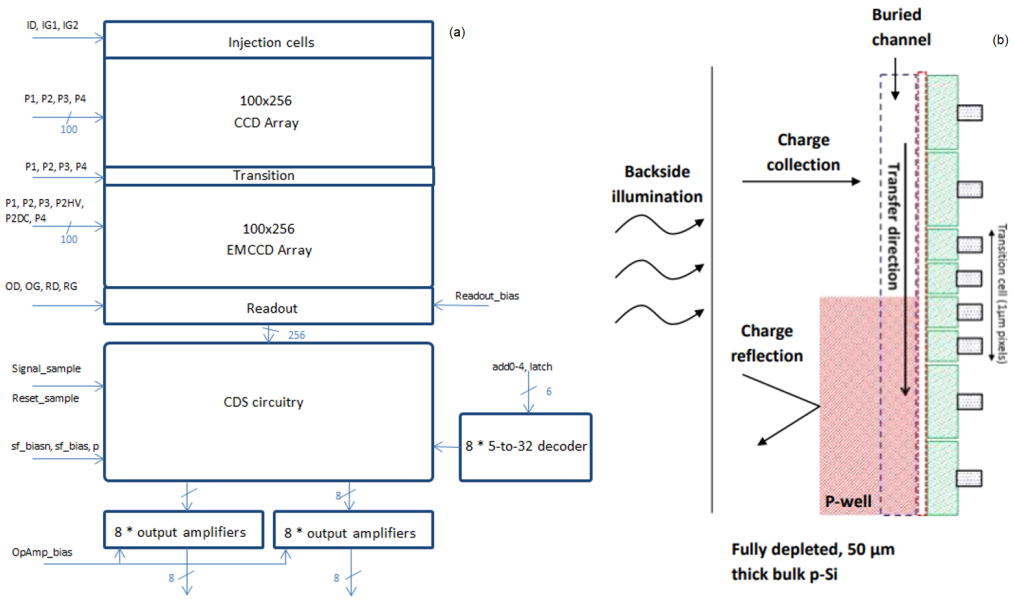

Figure 3.9: Simplified block diagram of EMTC1 from (a) front view and (b) side view.

The pixel matrix where each pixel is 10 μm square, is subdivided into 200 rows by 256 columns in 8 blocks of 32 columns. Each block has a differential output with Correlated Double Sampling (CDS).

The device is backside illuminated, and the bottom 100 rows of the pixel matrix are placed within a p-well which shields from direct charge collection. The deep p-well shields the other wells from the collection electrode from the epi-layer, preventing the collection of signal charge. As such, it is only possible for charge to enter the EM region from the image area above, as demonstrated in Figure 3.9(b). The device has the ability to attain up to 1 MHz column-parallel clock rate, with 32 Mpix/s from each output. The CCD array is 2.60 mm by 2.00 mm, and the overall chip area is 3.69 mm^2. Figure 3.10 denotes the top layer of the chip, and the array, CDS circuitry output amplifiers and

decoders are labelled. It is also possible to discern the power lines which are surrounded by the pads. The chip is flip-chip bonded to a QFN48 ceramic carrier the assembly of which was also completed at ESPROS.

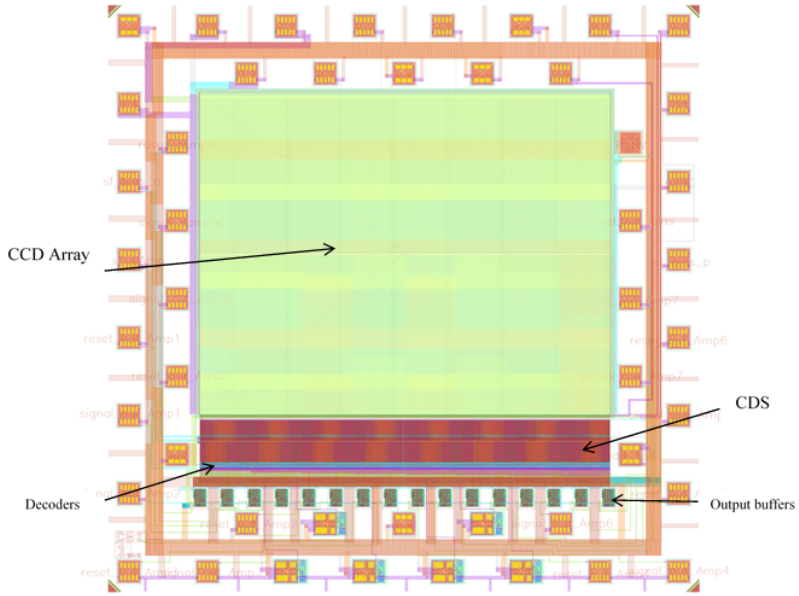

Figure 3.10: EMTC1 layout with the array, circuitry, decoders and amplifiers labelled. The power supply rails are visible, and the pads can be seen to surround the array.

The device also has a fill and spill charge injection. The fill and spill technique utilises the two input gates and an input diode limiting the noise and non-linearity customarily produced by the diode cut-off method. A small empty well is initially held beneath the input gate, isolated from the rest of the CCD buried channel by a blocking gate and the source of the electrons (input gates, see Figure 3.11) [121]. The diode voltage is then lowered, and the potential well fills with electrons, excess electrons spill back into the diode, which is rapidly pulsed high. The charges can then be transported in the desired direction mimicking photoelectric charge.

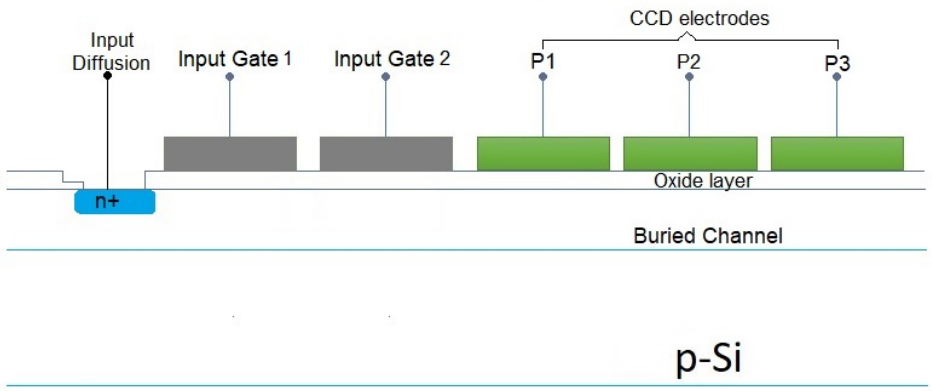

Figure 3.11: Basic input configuration of a CCD. The input diode is the source of electrons, and the input gate controls the quantity of injected charge [121].

3.2.1 Correlated Double Sampling Circuitry

Each column has the ability to store the reset and signal levels enabling the Correlated Double Sampling (CDS) to be completed off-chip. CDS is used to measure an electrical value such as a voltage and removal an undesired offset. This is achieved by measuring the sensor output twice, once under a known condition and once again with an unknown condition. The known condition is then subtracted from an unknown condition resulting in a value with a known relation to what was being measured. This can be used in an image sensor as a noise reduction technique. A reference voltage in a CCD is subtracted from the signal voltage of the pixel resulting in a reduced noise level. The CDS circuit consists of two transmission gates and two 1 pF metal-insulator-metal capacitors pictured in Figure 3.12.

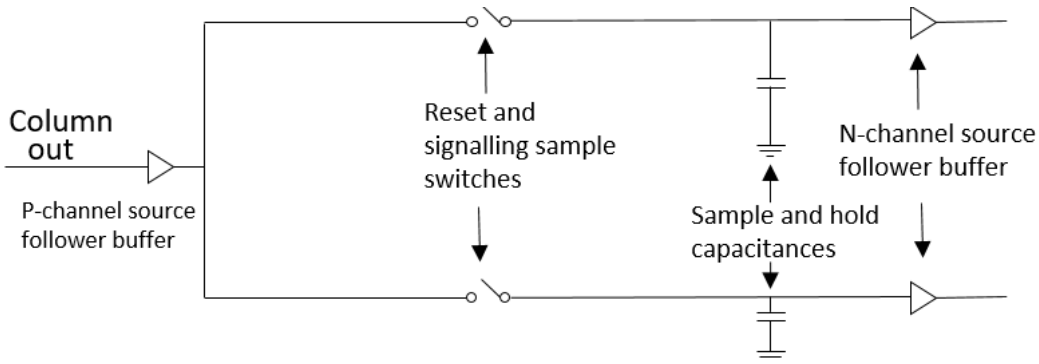

Figure 3.12: Functional diagram of the CDS circuitry.

The P-channel source follower buffer has a bias of 10 μA which provides an increased drive to charge the capacitances of the CDS circuit and raises the DC signal level by the approximately the same amount as the decrease caused by the readout source follower. The reset and signal sampling switches have a transmission gate architecture which has been sized to ensure minimal charge injection and are utilised as logic switches (high closes and low opens it). The transmission gates offer a good performance option as they work well at both high and low signal levels. The sample and hold capacitances are metal-insulator-metal capacitors with a capacitance of 1 pF and size of 8 μm by 130 μm. Finally, the n-channel source follower provides a buffer to the capacitances and provides a drive to the inputs of the output amplifier. This source follower also has a bias of 10 μA. The n-type source follower can achieve near unity gain.

3.2.2 Readout circuitry

The schematic of the readout circuit is shown in Figure 3.13, which consists of a p-channel reset transistor and an n-channel follower. This transistor sits in an isolated p-well which eliminates the body effect leading to near unity gain.

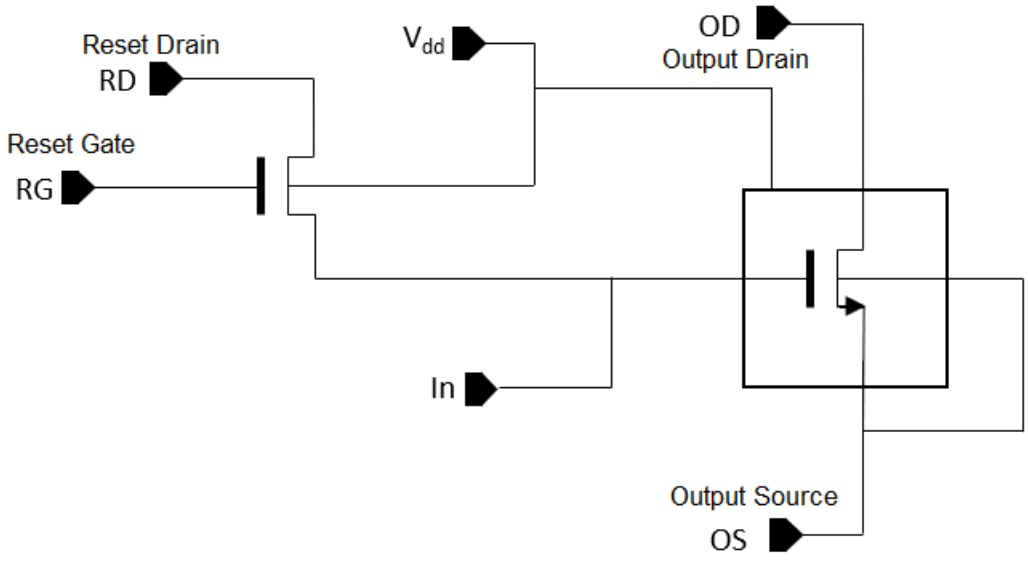

Figure 3.13: Reset transistor and source follower schematic.

Simulated data provided some insight into the performance characteristics of the readout stage including a typical gain of 0.9938, Charge to voltage

conversion factor (CVF) of 50.1 $\mu V/e-$, a bias current of 2 μA and linearity of 0.0092 %. The sense node capacitance was simulated at 28 fF.

3.2.2.1 Output Amplifier

An output amplifier is utilised as a unity gain follower. The buffer is a two-stage operational amplifier where the output is connected to the inverting input. The bandwidth is 119 MHz with the bias current set at 5 mA and 10 pF load. The simulated white noise density is 6.6 nV/Hz$^{1/2}$.

3.2.2.2 Address Decoders

An address decoder is a binary decoder with 5 inputs with only one output which is active high when the required address is selected. The address decoder is constructed by combinational logic gates.

3.3 Chapter Summary

This chapter has provided insight into the mechanical and electrical structure of the EMTC1. Early simulation data indicated (see Figures 3.4 and 3.6), completed by collaborators that the EMTC1 would provide considerably higher gain than traditional EMCCDs, due to several novel features; however, further insight from experimental data was required to gauge the impact of the new design. As such, the proposed EM structures and new process were implemented experimentally to further the understanding of the device and the physics behind the two novel EM gates. Explicit details pertaining to the foundry process are not available for this thesis; however, the impact of the structure is discussed in subsequent chapters.

Chapter 4

Experimental Setup and Method

4.1 Introduction

This section of the thesis presents the setup implemented throughout the recording of experimental results. An overview of the experimental setup is provided in this chapter but details pertaining to specific testing requirements, e.g. proton irradiation, can be found in following chapters.

Two iterations of the experimental setup were implemented due to several issues with insufficient thermal contact between the cold plate and the image sensor. The schematics of the two iterations are shown in Figure 4.1.

4.2 Experimental Setup

A description of each component of the experimental process follows and a discussion of why certain components were chosen. Results detailing the thermal responses for both setups are also provided giving insight into why two iterations were used.

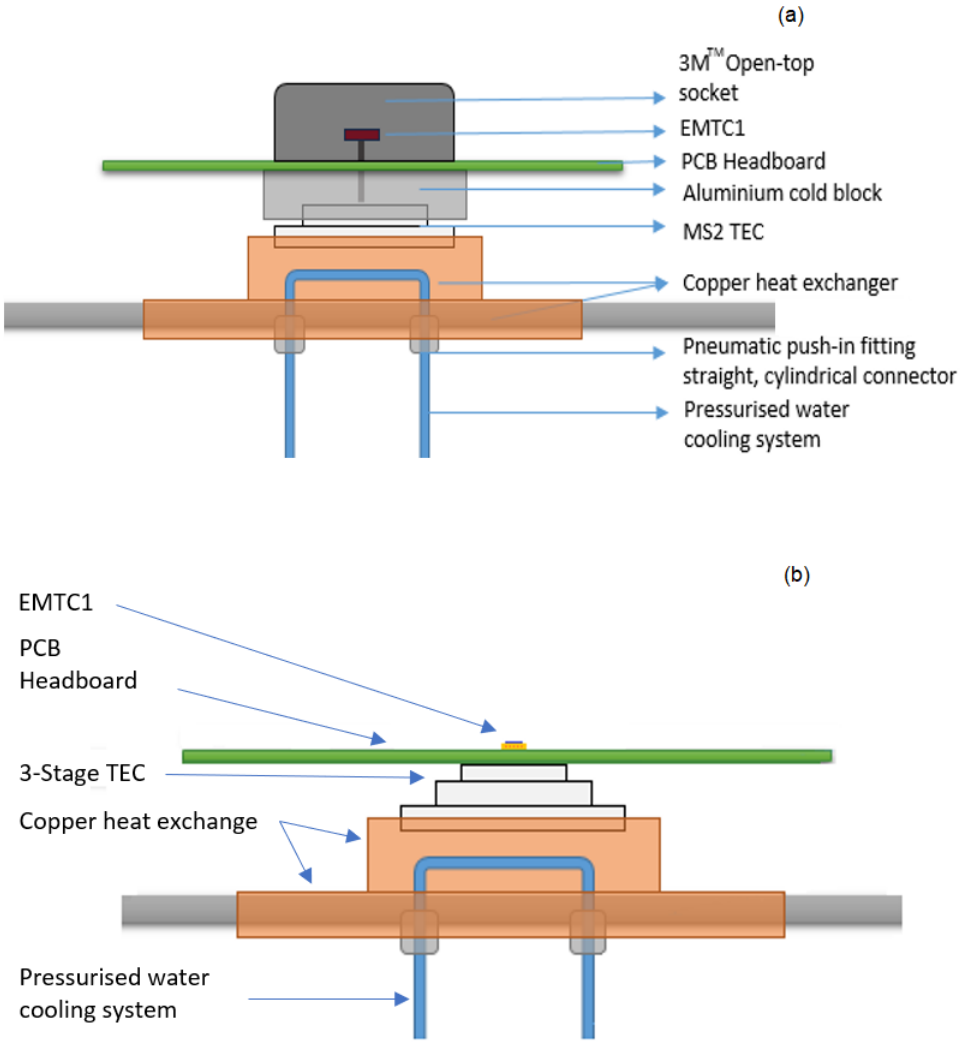

Figure 4.1: Experimental setups utilised during the characterisation and testing of EMTC1. a) The original experimental setup utilised a 2-stage TEC and an aluminium cold block which provided thermal contact to the PCB headboard. The EMTC1 was held in a socket soldered to the PCB. b) In the second iteration a 3-stage TEC was used and the EMTC1 was directly soldered to the PCB removing the need for the cold block.

4.2.1 Vacuum System

The fundamental component of the experimental system is the vacuum chamber. While several tests can be completed at room temperature, multiple facets of the device characterisation process require sub-zero temperatures. At such temperatures, any water within the atmosphere condenses on cold surfaces in accordance to the Arden-Buck theory [9]. It is essential to ensure that no condensation can form on either the electronics or the device or permanent damage can occur.

To achieve this vacuum, a Pfeiffer Turbo-Drag Pump was used. This setup is a highly economical bench-top station that can achieve a pressure of 10^{-8} mbar and the average pressure of the system after sufficiently long settling was 8.6×10^{-6} mbar.

The vacuum chamber utilised is a 200 mm stainless steel 304 cylinder shaped (see Figure 4.2) chamber with two detachable flanges and three smaller feed-throughs, two with a diameter of 25 mm and one of 16 mm. These additional feed-throughs allow for the adaptions dependent on the experiment requirements.

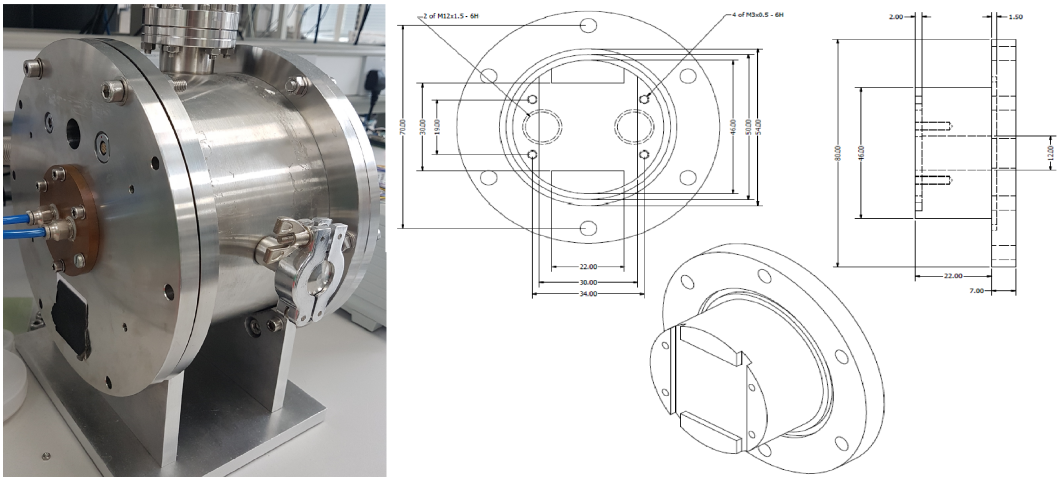

Figure 4.2: (Left) The vacuum chamber utilised during the experimental process. The blue water cooling system piping can be seen as can the flanges. (Right) The vacuum chamber schematics for the front plate and heat exchanger.

These include attaching an electrical feed-through for an LED to provide flat-field illumination or for additional temperature sensors to enable a thor-

ough analysis of the device cooling. Atop the chamber is a Conflat flange which allows for the mounting of X-ray fluorescence targets or an iron-55 source. The chamber also includes three vacuum electrical feed-throughs to allow for the control of the temperature and camera inputs and outputs. One detachable flange was replaced with an electrical feed-through enabling the addition of another temperature sensor and an LED. A heat exchanger was connected to the front flange so that a water cooling system could be used to reduce the temperature of the system further.

4.2.2 Thermoelectric Cooling

The Thermoelectric Cooler (TEC) utilises the Peltier effect first discovered in 1834. The Peltier Effect induces a thermal gradient across the junction of two materials by passing a current across the junction [91]. It is possible to achieve a temperature differential of up to 70 degrees utilising a standard single stage TEC. It is only possible to cool effectively if the heat is removed from the hot side, otherwise overheating can cause permanent damage to the device.

The easy controllability that the TEC offers enables a high level of flexibility especially for a setup that does not require the temperature range that the Cryotiger or Stirling cooler offers. However, the incorrect operation of a TEC can lead to catastrophic consequences. By increasing the current beyond the limits of the device, it is possible for the cold side of the device to rapidly heat. This, in turn, can lead to not only a broken TEC but can also damage the PCB and the image sensor. High temperatures can lead to the damage to the elements and cracking of the ceramic. The thermoelectric cooler is small and compact in design, and the vacuum chamber employed in this system required minimal adaption.

There are several different types of TECs are available, and it was important to consider the size of the heat exchange recess to ensure a good fit and strong heat exchange.

The initial TEC used in the system was the Laird MS2 1147, to test experimental setup for faults and initial device characterisation. Several measurements presented in this thesis were made utilising 2-stage cooling with an EMTC1 sensor in a socket, including ageing of Chip 5 (Chapter 8) and some initial characterisation of the chips (Chapter 5). The MS2 1147 can achieve a ΔT_{max} of 80 degrees with a maximum current of 5.70 A. The dimensions of the

TEC were 30.0 by 30.0 by 10.9 mm, matching the size of the heat exchanger in the chamber. The maximum voltage for the TEC is 3.5 V.

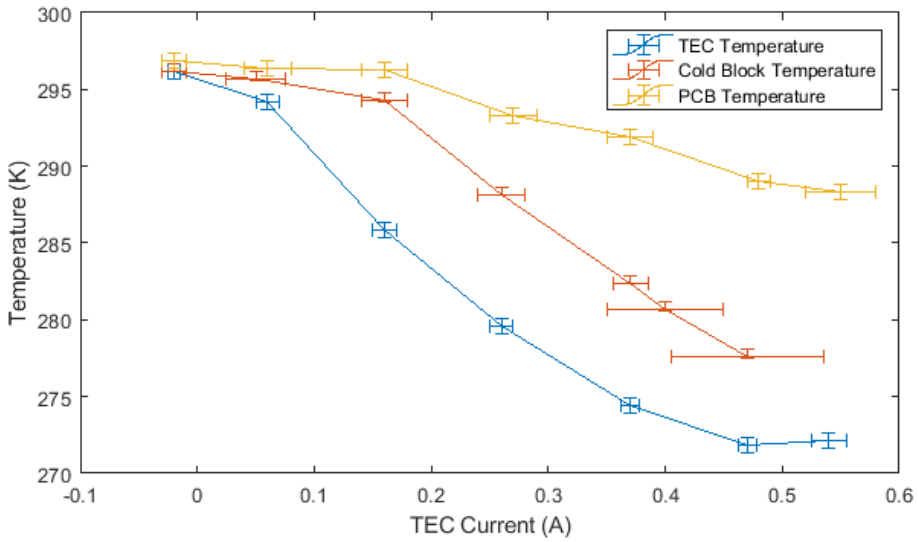

Figure 4.3: A comparison of the temperature measured using an RTD attached to the MS2 1147 TEC, Al cold block and PCB as a function of the current applied to the TEC.

Figure 4.3 compares the simultaneous temperature measurements for the MS2 1147 TEC, cold block and Resistance Temperature Detector (RTD) attached to the PCB adjacent to the device. While the TEC was able to reach 272 K at a current of 0.5 A the temperature on the PCB and ultimately the socket was $\sim$ 20 degrees warmer. Furthermore, the PCB temperature did not consider the additional insulating properties of the socket which would result in the image sensor operating at an even warmer temperature. It was apparent from these results that there was poor thermal conductivity from the TEC through to the socket. This was then compared with an RTD sensor attached to the board such that for future tests the temperature of any device studied could be determined from the comparison with the temperature from an RTD attached to the headboard within the vacuum chamber. To effectively analyse the conduction of heat through both the board and the socket to the EMTC1 chip an RTD was glued to a spare chip and placed in the socket and the temperature measured.

Figure 4.3 demonstrates the temperature achieved on-chip as a function of the TEC current. Exceeding the maximum current resulted in the rapid warming of the cold side of the TEC. Subsequently, the TEC was operated using a current of 1.20 A. This can be attributed to deficiencies in the water cooling system resulting in heat not being removed at a fast enough rate. The temperature controller used to control the TEC is the LDT-5525 ILX-Lightwave. It provides an output of 4 A, 24 W with a temperature range from 372.15 to 473.05 K [52]. The controller uses thermistor resistance and voltage related through Ohms Law. As the thermistor resistance changes, a changing voltage signal is available to the thermistor inputs of the LDT-5500B Series. The controller works in conjunction with the LM335 sensor which is a linear thermal sensor that acts as a constant voltage source.

The experimental setup experienced an overhaul to enable a far lower temperature to be reached (see Fig. 4.1 from (a) to (b)). As demonstrated by Figure 4.3, the minimal temperature that the TEC could achieve was 0°C. As such, it became necessary to find a better solution to cooling the device. A new headboard was designed to enable the EMTC1 to be soldered directly to the PCB, thus removing the need for a cold block and significantly improving the heat transfer to the device. The Laird MS3 (see Figure 4.4) can reach a maximum temperature difference (ΔT_{max}) of 87°C working with a maximum current I_{max} of 4 A and V_{max} of 8.2 V, with a size of 30 by 30 by 9 mm.

Figure 4.4: Laird MS3 TEC utilised for the majority of the characterisation of the EMTC1, original image adapted [reprinted] from [66]

The TEC was cooled under vacuum conditions with the new headboard

placed in contact with the TEC, separated only by a square of indium foil to increase the thermal contact. This was cooled at a rate of 1 K per minute, then allowed to stabilise.

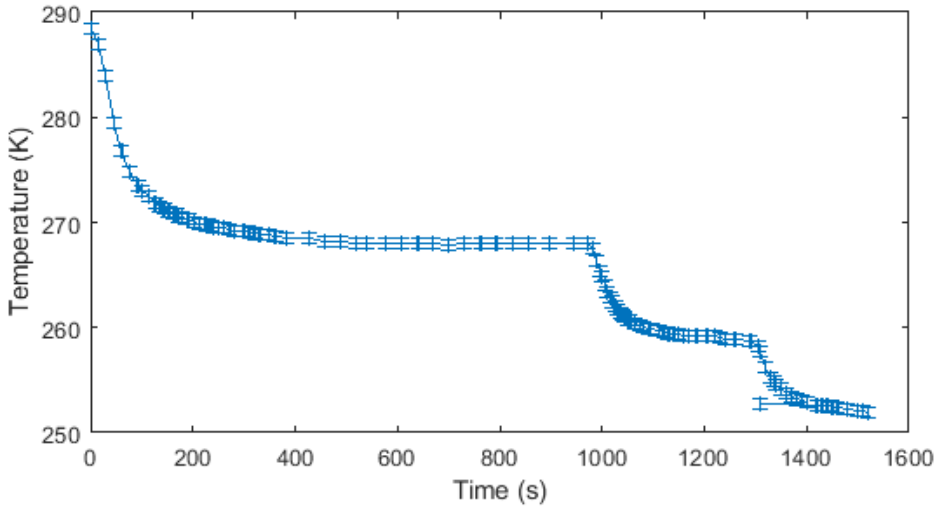

Figure 4.5: The cooling curve of the EMTC1 with the TEC cooling as a function of time. The sudden decrease in temperature signifies an increase in the current of the TEC. The temperature was measured from using an RTD attached to the PCB close to but not in contact with the EMTC1 device.

Figure 4.5 demonstrates the cooling curve of the Laird MS3-119-14-15-00-W8 thermoelectric cooler. The current was increased incrementally at the end of each plateau until the minimum temperature was reached. Insulating the water cooling system enabled an increase in heat removal, resulting in a minimum temperature achieved by this system of 245 K.

The stability of the temperature was then tested over 15 minutes. The temperature was initially set to 253.5 K. However, biasing the EMTC1 increased the power dissipation which lead to a temperature increase of 0.5 K. Figure 4.6 demonstrates the stability over this period with cooling and warming demonstrating the TEC attempting to stabilise the temperature. It is important to note that this setup had been allowed to settle for several hours before device operation.

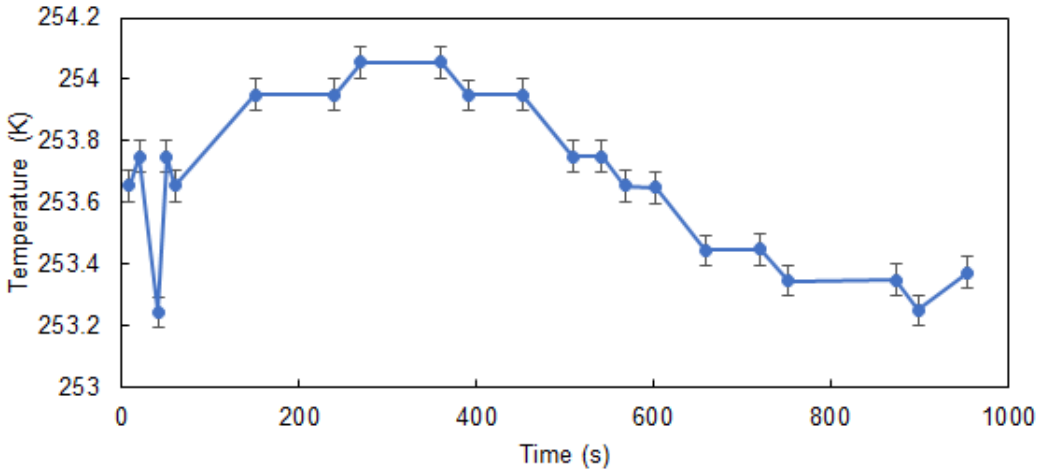

Figure 4.6: The stability of the temperature at a set temperature of 253.5 K. The temperature was measured using an RTD attached the internal PCB headboard next to the EMTC1 chip soldered directly to the PCB.

To control the device, the internal board was wired to the external board via the electric feed-throughs. The external board, connected to the internal headboard via the electrical feed-though, was controlled via a National Instruments NI PXI-7852R R-Series FPGA card. The board was powered by ±5 V and +20 V supplies.

As described previously; the cooling was aided by the addition of a water cooling system. It was attached to the heat exchange block on the vacuum chamber. Pneumatic quick push fit 6 mm plugs were attached to the heat exchange block, to allow for the flow of pressurised water to remove the heat and allow for a much lower temperature to be reached. Insulation of this system led to a 5 degree decrease in the minimum temperature. The water cistern was kept outside in a sheltered location but was susceptible to fluctuations in the ambient temperature. As such, the lowest temperatures were achieved on a seasonal basis.

4.3 Electronics

The EMTC1 was driven via a controller board which connected to the computer via a National Instruments NI 7852R FPGA card.

The EMTC1 was plugged into a headboard inside the chamber which connects to the controller board via two hermetically sealed Fischer connectors visible in Figure 4.7. The controller board provided all the necessary signals for EMTC1 operation.

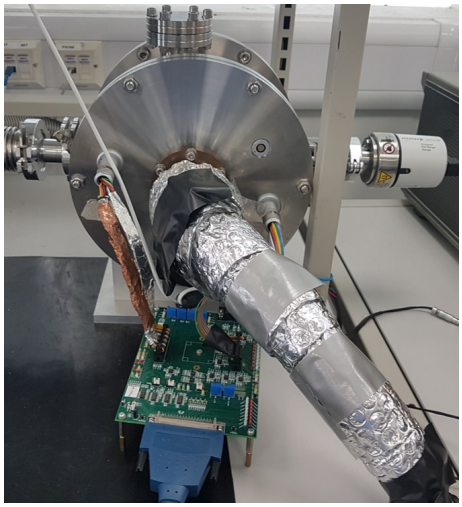

Figure 4.7: The completed vacuum chamber showing the insulated water cooling system, the Pfeiffer Vacuum compact full range gauge, and the controller board connected to the vacuum chamber via hermetically sealed Fischer connectors.

In addition, the controller board also powers and triggers the timings of the internal LED. This LED was calibrated using this controller board. It went through two iterations during this research reducing noise seen in early test results. The majority of the results presented in this thesis used the latter headboard.

4.4 LabVIEW

A pre-existing LabVIEW programme was adapted to suit the clocking and biasing required by the EMTC1. The majority of the changes involved the automation of the programme. During this thesis the programme was adapted to enable automated data collection including the automated initial characterisation completed on all devices such as the PTC and dark current. The programme was further adapted to enable automated testing for ageing (which

will be discussed in a subsequent chapter). The ageing programme enabled the operated the EMTC1 at high voltage for days with intermittent automated device characterisation.

The EMTC1 DAQ V2 LabVIEW script enabled the sequencer to be altered within the GUI. A flow chart describing the processes of the software can be seen in Figure 4.8. The original sequencer timing used can be seen in Figure 4.9 which details the start of and end of the EMTC1 clock sequence. By increasing the time that the LED is switched on, the incident light that illuminates the devices increases proportionally. The LED is triggered near the end of the sequence during the integration period as seen in Figure 4.9. Figure 4.9 initiates with the reset gate pulsed high to clear charge. P1 is then biased during the charge collection phase before P2, P2HV, P3 and P4 are pulsed in turn as charge is moved through array. The sequencer also controls the signal sample and hold (SSH) used sample and hold the light and dark reference pixels.

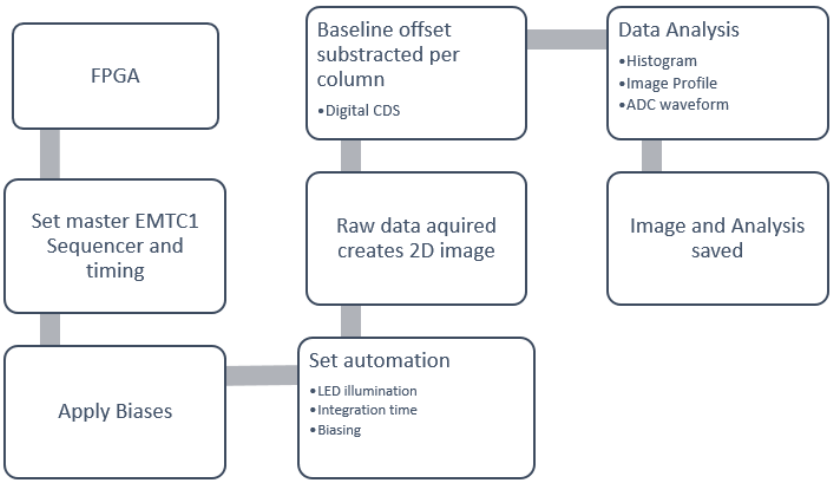

Figure 4.8: Flowchart describing the data flow in the EMTC1 LabVIEW program

The sequencer shown in 4.9 does not trigger the Input Drain (ID) clock. When pulsed this controls the charge injection via a 'fill and spill' technique. As the input diode is lowered, the channel beneath the input gate 'fills'. Once filled the input gate is brought high and the charge spills back into the diode until an equilibrium with the channel potential is reached. The charge is then transferred through the serial register and the amount of charge that has been

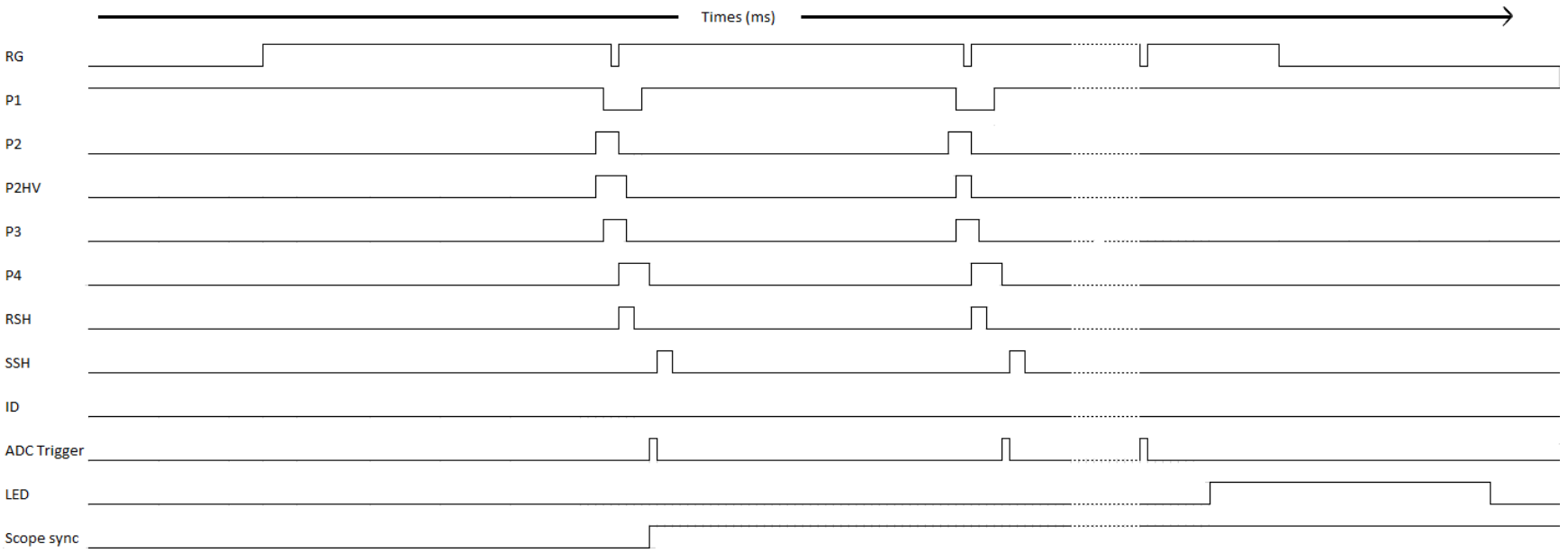

Figure 4.9: The start and end of the EMTC1 EM 500 30 inj CDS 32 sequencer in detail. This sequence was the main sequence implemented in the for most characterisation test unless otherwise stated.

injected can be determined by calculating the difference between the voltages applied to the collecting well and the input gate and as such, by varying these voltages it is possible to alter the quantity of input charge. The dotted line demonstrates an extended period of time between the start of the sequence (0 ms) and the end of the sequence (50 ms).

The GUI also enabled the control of the column readout. The column address sequence controls the address decoder by biasing the address bits. The sequencer was developed prior to commencement of the research presented in this thesis by K. Stefanov and remained unchanged during the research presented in this thesis. The LabVIEW program also sets biases of the EMTC1 device which can easily be changed by the user. These biases were altered to optimise the device performance.

4.5 Experimental Procedure

To ensure a high level of repeatability, it was important that the experimental procedure remained consistent. The device was placed within a clean chamber, secured and a temperature sensor attached. For the original setup, the device was placed in a spring-loaded socket soldered to the internal headboard, which in turn was then attached to the aluminium cold block and then attached to the heat exchange as detailed in Figure 4.1. The internal headboard provides direct power to the EMTC1 in the vacuum chamber via the electric feed-throughs. The connections from the headboard to the vacuum chamber were made using nylon screws which limited the risk of electrical shorting; however, they undergo considerable outgassing.

Once the chamber has been sealed the air was evacuated from the vacuum chamber until a pressure of 10^{-6} mbar was reached. Subsequently, the device was cooled at a rate of 1 K per minute, to avoid thermal shock, until the desired temperature was reached for each experiment.

Once the experiment had been completed and the device needed to be removed, the EMTC1 was slowly warmed and the temperature allowed to stabilise. Once room temperature had been reached the vacuum was switched off and the pressure equalised with atmospheric pressure. Uninterrupted Power Supplys (UPS) were used to protect the device should power failure occurs

which would result in loss of vacuum at a faster rate than the device would warm.

4.5.1 Handling and Cleanliness

It was important throughout the testing process that devices were not exposed to electrostatic or particle damage. During the experimental system development, the entire vacuum chamber was thoroughly cleaned, and all components installed within the chamber were bathed in a sonic bath and cleaned with isopropanol. A Class 100 Laminar Flow bench was utilised to minimise contamination during assembly. When the devices were not in use, they were stored in labelled plastic containers within antistatic zipped bags. All handling of the devices was completed using powder-free Nitrile gloves, and an antistatic wrist strap was worn at all times. The length of time that the device was out of chamber was recorded with the aim of minimising exposure to dust particles. Furthermore, the chamber was not left open for extended periods of time and regularly cleaned when the system had been opened.

4.6 Chapter Summary

This chapter focuses on the experimental setup implemented throughout the thesis. Some changes have been made for specific tests; however, these will be detailed in subsequent chapters. It is important to note that the experimental setup has evolved during this work. Furthermore, the work establishing the test camera for the EMTC1 provides a good platform for other camera systems to be developed and the system has now been adapted into other projects.

Chapter 5

Characterisation and Device Screening

5.1 Introduction

Several devices, newly fabricated from the same wafer, can differ from each other due to slight variations in the size and thicknesses of each layer. As such, it is essential to characterise each device post-fabrication fully. Through device characterisation, several device metrics can be calculated and enable an evaluation of different devices for specific applications.

For a new technological process, this characterisation is essential in providing a comparison with existing devices and established manufacturing procedures. This chapter discusses the characterisation process of the low voltage EMCCD in a CMOS process, split into several sections including the optimisation of voltages, the characterisation of the test devices and a preliminary analysis of the potential of each of the EM pixel variants. The work was conducted to investigate device performance, to identify trends in the device behaviour and to identify the suitability for using a low voltage EMCCD in a CMOS process in low light imaging. This section details the experimental procedures followed by the results, discussion and conclusions.

5.2 Experimental Procedure

Chapter 4 described the experimental setup and many of the experimental procedures utilised during this experimental process. Here it is sufficient to describe the operational biasing used (see Table 5.1) and that the experimental setup remains unchanged from that described in Chapter 4. Initial testing demonstrated that the device was functional at these voltages when operated without EM gain.

Parameter	Notation	Voltage (V)
Input Drain	ID	4.0
Reset Drain	RD	4.5
Output Gate	OG	2.0
DC Gate	P2DC	2.0
Clocking voltage	P1234	0.0 to 4.0
High Voltage gate	P2HV	0.0 to 15.0

Table 5.1: The initial voltages used for the device characterisation and testing.

The vacuum chamber was cooled slowly once the air was evacuated from the chamber. The device was able to reach a temperature of 243 $\pm$0.5 K. A settling period of 30 minutes was initiated prior to each new experimental run to allow for the temperature to stabilise once the device had been powered. The initial operating voltages tested are given in Table 5.1. The sequence used to control the voltages and timings was designed to read out the whole device. Figure 5.1 shows the readout for the EMTC1 denoting the floating diffusion, reset gate and differential ADC. The Non-EM and EM regions both readout to the same diffusion circuitry. As such, any noise contributions after the floating diffusion should be independent of the device region.

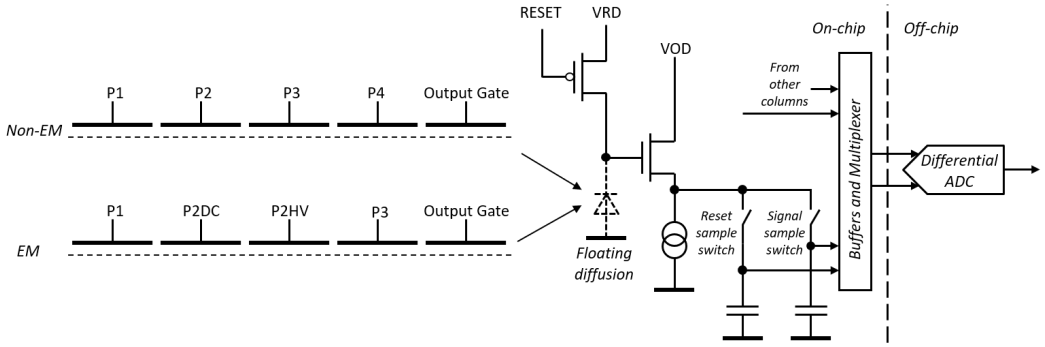

Figure 5.1: Simplified readout circuitry of the test chip. Correlated double sampling (CDS) is performed by the differential ADC which subtracts the reset sample from the signal sample. Adapted [reprinted] from [105].

5.3 Device Characterisation

The testing completed for each device is divided into several sections;

- Functionality
- Performance and Image Quality

The work was conducted to calculate and understand basic device behaviour and enable certain recommendations for the operation of the EMTC1 and opportunities for the development of this technology. Table 5.2 provides a list of the devices tested during this thesis, the setup for each and the experimental testing each device underwent.

5.3.1 Error Calculation

During this and subsequent chapters, errors were calculated from the combined error of the standard error and measurement errors calculated from the accuracy of the system unless otherwise stated. The standard error was calculated from the standard deviation of multiple images captured under the same conditions. Combination of errors was completed using the following equation

$$\frac{\delta_x}{x} = \sqrt{\left(\frac{\delta_a}{a}\right)^2 + \left(\frac{\delta_b}{b}\right)^2 + ...\left(\frac{\delta_n}{n}\right)^2} \tag{5.1}$$

where δ_x is the total error, x is the final value, δ_a, δ_b and δ_n are the error the values a, b and n. Any other error methods used in subsequent chapters will be described in detail.

Device	Experimental Setup	Testing
EMTC1_C1	Device in socket	Experimental setup Device characterisation
EMTC1_C2	Device in socket	Device characterisation
EMTC1_C3	Device in socket	Device characterisation
EMTC1_C4	Device in socket	Device characterisation
EMTC1_C5	Device in socket	Device Characterisation EM Ageing
EMTC1_B1	Chip on PCB	Device Characterisation Irradiation Control
EMTC1_B2	Chip on PCB	Device Characterisation Proton Irradiation
EMTC1_B3	Chip on PCB	Device Characterisation EM Ageing
EMTC1_B4	Chip on PCB	Device Characterisation
EMTC1_B5	Chip on PCB	Device Characterisation Charge Transfer

Table 5.2: The EMTC1 devices used during the collection of experimental data for this thesis.

5.3.2 Photon Transfer Curve

The Photon Transfer Curve (PTC) is an effective tool to characterise CCD performance. The primary purpose of the PTC is to determine the conversion factor between the number of electrons collected and the digital readout. It is

then possible to determine several other performance parameters such as the readout noise, non-linearity and the Full Well Capacity (FWC).

5.3.3 Derivation of the Photon Transfer Curve

The photon transfer curve is generated by plotting the noise as a function of the signal of different light levels using a uniform light source. It is possible to discern four distinct regions of the PTC. The initial region is dominated by read noise which gives way to photon shot noise, as the signal increases. When the PTC is plotted on a log-log scale, the shot noise region is characterised by a gradient of 1/2. As the light intensity increases, the third regime is dominated by the fixed pattern noise (FPN) which scales with the signal such that the gradient of this region is unity. The final section of the PTC denotes the device's full well region during which, the noise modulation decreases as the image sensor nears saturation.

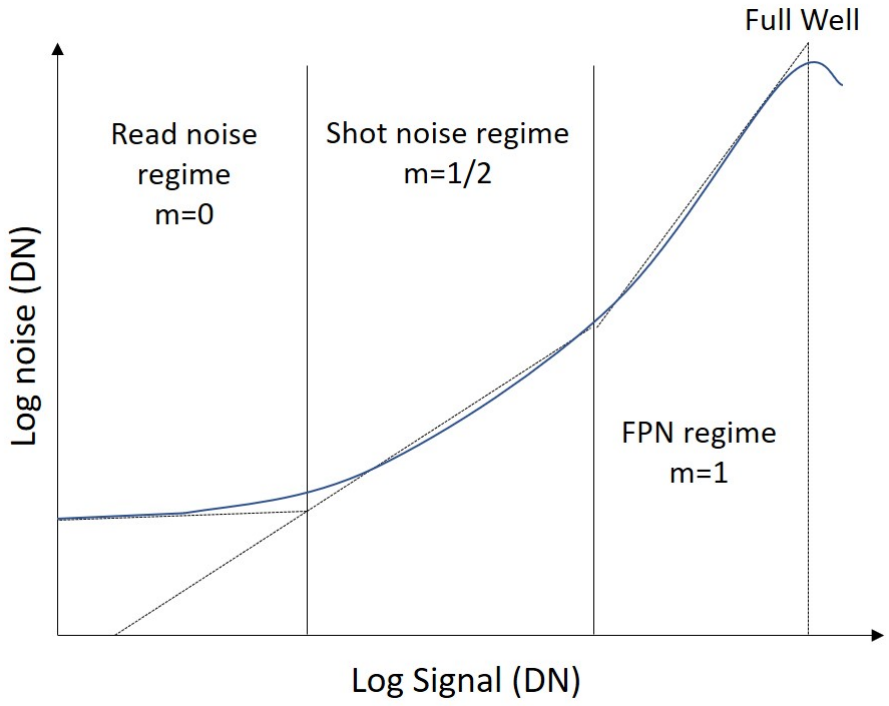

Figure 5.2: Example of Photon Transfer Curve with the regions of the curve labelled where DN is the Data Numbers which refers to raw data also known as analog-to-digital units (ADU). Image taken from [54]

5.3.3.1 The Mean-Variance Curve

The Mean-Variance Curve is a type of PTC used to characterise solid-state image sensors and has been used to derive the device characteristics of CCDs, EMCCDs and CMOS image sensors [54]. The mean-variance curve utilises the shot noise associated with photons incident on the photo-sensitive region of the image sensor. The noise is described by the Poisson statistical distribution such that the variance is equal to the average number of photons which is incident on a pixel during a given time period.

The variance can be acquired from the square of the standard deviation of a Region of Interest (ROI) of a frame. By subtracting the mean from the signal frame, it is possible to remove the DC offset and the bias caused by amplifier drift between subsequent exposures. By subtracting one image frame from another taken under the same conditions, the fixed pattern noise can be removed. Subsequently, the remaining noise is the photon shot noise and the readout noise. These noise sources are stochastic and independent such that the total noise (σ_{tot}) can be calculated from

$$\sigma_{tot}^2 = \sigma_{ph}^2 + \sigma_{read}^2 \tag{5.2}$$

where σ_{ph} is the photon noise and σ_{read} is the read noise. The signal from the sensor (S) in Analogue-to-Digital Units (ADU) can be expressed as

$$S_{ADU} = \frac{1}{G_s} N_e \tag{5.3}$$

where N_e is the average number of electrons collected and G_s is the system gain expressed in units of e-/ADU. The signal variance (σ_S) can be calculated using the propagation of errors

$$\sigma_S^2 = \left(\frac{\partial S_{ADU}}{\partial N_e}\right)^2 \sigma_{N_e}^2 + \left(\frac{\partial S_{ADU}}{\partial G_s}\right)^2 \sigma_{G_s}^2 + \sigma_{read}^2 \tag{5.4}$$

Since G_s is a constant, $\sigma_{Gs} = 0$ and from Poisson statistics $\sigma_{N_e}^2 = N_e$ it is possible to rewrite Equation 5.4 and by using Equation as 5.3 as

$$\sigma_S^2 = \frac{S_{ADU}}{G_s} + \sigma_{read}^2 \tag{5.5}$$

From here the system gain is

$$G_s = \frac{S_{ADU}}{\sigma_S^2 - \sigma_{read}^2} \tag{5.6}$$

If we plot the signal variance vs the signal (mean-variance plot) the system gain can be obtained as the inverse gradient of the straight-line fit to the variance. The responsivity of the device R, measured in units of V/e-, can then be obtained from the system gain as

$$R = \frac{V_{ADU}}{G_e G_s} \tag{5.7}$$

where G_e is the electronic gain and V_{ADU} is the size of one 1 ADU in volts.

5.3.4 Results

The majority of the results in this section were acquired from mean-variance curves. The results presented here were acquired at 273±0.5 K unless otherwise stated. However, mean-variance curves were also completed for each characterised test chip at a range of temperatures (see Fig. 5.3).

5.3.4.1 System and Conversion Gain

The PTC was utilised to attain several important device characteristics discussed in this section. It is important to note that when a PTC is discussed, a Mean-Variance method is utilised unless otherwise stated.

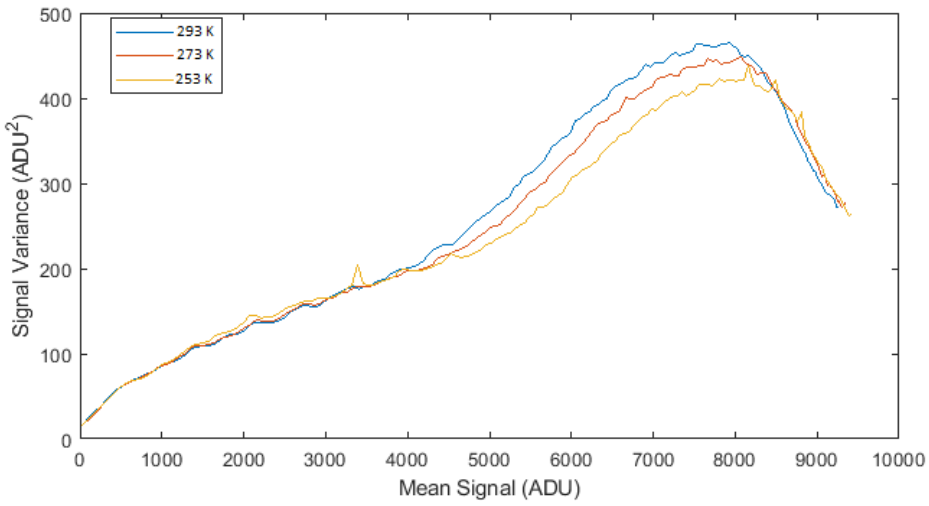

Figure 5.3: Mean-variance graph acquired from EMTC1_B3 at three temperatures. The integration time was kept constant at 100 ms.

Figure 5.3 demonstrates a Mean-Variance curve for the EMTC1. As discussed, early, a PTC requires flat field illumination. For illuminated experiments in this thesis, calibrated LED was installed at the rear of the vacuum chamber. Due to the size of the device and distance from the light, the device was uniformly illuminated. This corresponded with flat field illuminations taken demonstrating that the standard deviation with the image area corresponds to the variation expected from the different structures within the EMTC1. The temperature dependence of the signal variance can be attributed to a decrease of the full well capacity at higher temperatures.

One of the primary uses of the mean-variance curve is to acquire the conversion gain of a device. The conversion gain was extracted for each block using a large number of frames at a constant temperature. The gains recorded here were acquired at 273 K. The fit from which the system and conversion gains were acquired was plotted in the range of 4500 to 6000 ADU. This range was more susceptible to variations in the temperature; however, experienced only negligible non-linearity. The R^2 value for each of these fits exceeded 96%. The errors calculated for the gains (seen in Table 5.3) were calculated from the standard error from the standard deviation of the region of interest and the coefficient of determination. The system and conversion gain were acquired for each device and averaged over the optically sensitive region of the device. The conversion and system gain were uniform across the image sensor within an average non-uniformity of 4.5% across the devices.

Sensor	System gain (e-/ADU)	Conversion gain ($\mu V/e-$)
EMTC1_B1	11.56 ± 0.60	26.38 ± 0.61
EMTC1_B2	12.41 ± 0.65	24.58 ± 0.65
EMTC1_B3	10.75 ± 0.54	28.37 ± 0.53
EMTC1_B5	13.57 ± 0.62	22.48 ± 0.60

Table 5.3: The system gain and subsequent conversion gain for four EMCT1 sensors. The system gain was averaged across the image area. the conversion gain was calculated from the system gain.

It was also possible to determine the read noise from y-intercept of the mean-variance curve of a linear fit in the read-noise regime. The fit from which

the system and conversion gains were acquired was plotted in the range of 500 to 3000 ADU. This range was found to be largely temperature independent with the three fits seen in Figure 5.3 falling within the error. The R^2 value for each of these fits exceeded 96%. The errors calculated for the read noise (seen in Table 5.4) were calculated from the error standard area from the region of interest and the coefficient of determination. Table 5.4 shows the read noise for each region of the device for EMTC1_B3 ∼250 K with a pixel readout frequency of 10 kHz. The read noise was largely uniform across the device with only Block 8 experience a read noise higher than the average. This could be attributed to stochastic noise or from unknown noise contributions from the EM register. The read noise was considerably higher than many modern devices. A reduction in the read noise results in an improved dynamic range of the device. Operating at a lower readout frequency would result in a lower readout noise.

Device region	Readout noise (e-)
Block 1	70.81 ± 0.36
Block 2	73.85 ± 0.38
Block 3	73.87 ± 0.49
Block 4	73.88 ± 0.61
Block 5	73.95 ± 0.78
Block 6	73.95 ± 0.57
Block 7	75.94 ± 0.42
Block 8	80.00 ± 0.45

Table 5.4: Readout noise for each block of the EMTC1_B3 when operated using the biasing in Table 5.1 at ∼250 K with a pixel readout frequency of 10 kHz.

5.3.4.2 Linearity

It can be assumed that the charge generated by the photoelectric effect collected within each pixel, transferred to the sense node and then readout is

directly proportional to the number of the photons absorbed by the silicon. The conversion of the charge to voltage is nearly linear, and it is possible for a number of factors to limit the linearity including incorrect bias voltages, which in turn affect the charge transfer to the sense node and the linearity of the source follower. Only an idealised CCD is strictly linear; however, the non-linearity for many modern CCDs can be modelled using the dependence of the conversion gain on the collected electrons per second and the exposure time.

The linearity curves were attained by plotting the sensor response against input illumination on a scale to acquire a curve as demonstrated in Figure 5.4. These fits were selected to cover the entire range of the mean-variance graph to highlight the non-linearity at higher signals. The non-linearity is then normally represented as a percentage based on the deviation of the data from the line of best fit.

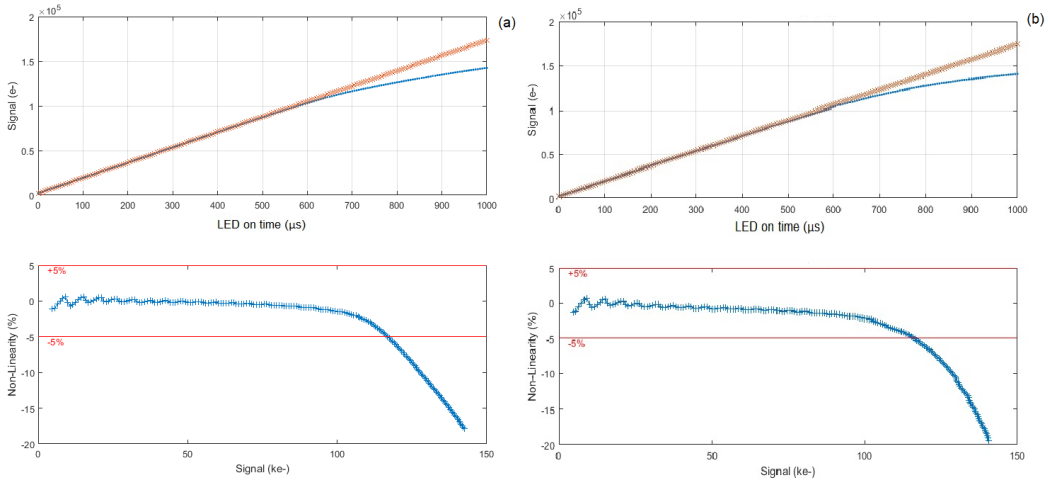

Figure 5.4: Illumination and linearity curves using flat fields at 302.5 K for (a) Block 1 and (b) Block 6. The device was clocked using the biases described in Table 5.1 using a readout frequency of 10 kHz.

Linearity measurements were performed across the whole device, but results were taken from regions of homogeneous subsections within each block. Figure 5.4 demonstrates the device linearity for two blocks of the image area as a function of the photon irradiance. As can be seen from the graphs, non-linearity sharply increases above the 100k electron signal level. The small fluctuations in the linearity at the start of the curve can be attributed to read

out noise. Figure 5.5 shows the linearity as a function of signal for 5 different

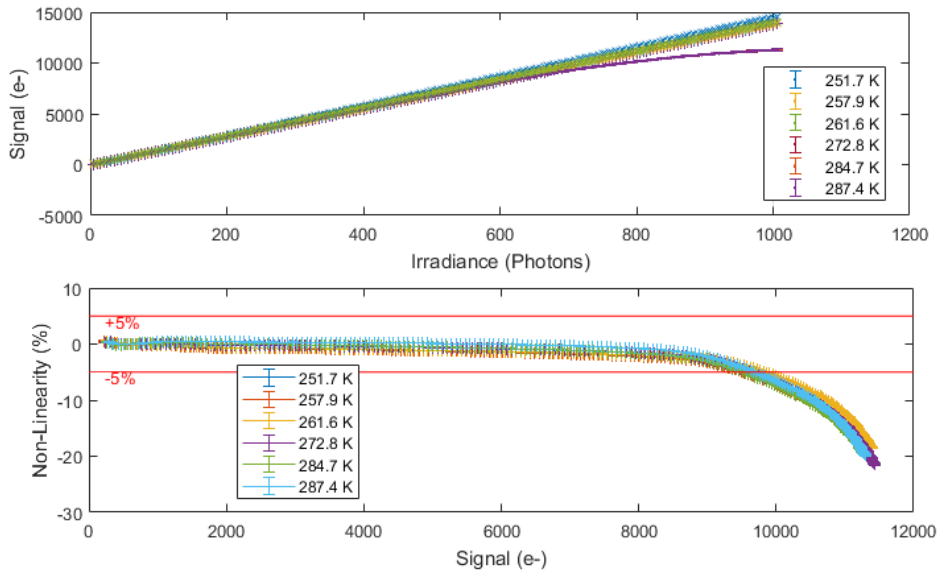

Figure 5.5: Illumination and linearity curves using flat fields at 302.5 K for Block 6 when the device was operated at 6 separate temperatures in the range of 250 - 290 K. The device was clocked using the biases described in Table 5.1 using a readout frequency of 10 kHz.

temperatures. It was apparent that dark current correction was unnecessary, as increases in the temperature did not affect the linearity. There was only a fractional change in the linearity at higher temperatures that largely fall within the error calculated from the standard error.

Though it will be covered again in subsequent chapters, it is of interest to note that the device was found to have a poor charge transfer efficiency, especially at high and low signal levels.

5.3.4.3 Full Well Capacity

The full well capacity, which can be obtained from the PTC and linearity curves, describes the quantity of charge that can be held within a pixel based on the individual collection pixels. If the charge within a pixel exceeds the full well capacity, the pixel will begin to experience "blooming" where charge can spill into adjacent pixels. These full well capacities were calculated using the biasing found in Table 5.1.

Device	FWC (e-/pixel)	FWC (e-/μm^2)
Block 1	1.17×10^5 $\pm0.3k$	1170 $\pm$3.43
Block 2	1.19×10^5 $\pm0.3k$	1190 $\pm$3.24
Block 3	1.21×10^5 $\pm0.5k$	1210 $\pm$5.42
Block 4	1.21×10^5 $\pm0.5k$	1160 $\pm$5.41
Block 5	1.16×10^5 $\pm0.5k$	1160 $\pm$5.12
Block 6	1.17×10^5 $\pm0.5k$	1110 $\pm$5.44
Block 7	1.15×10^5 $\pm0.3k$	1150 $\pm$2.92
Block 8	1.08×10^5 $\pm0.4k$	1080 $\pm$3.83
CCD97-00	1.30×10^5	508
CCD220	3.0×10^5	521
CCD60	8.0×10^5	1390

Table 5.5: Full well capacity for each region of the device compared with modern commercially available devices measured when the non-linearity exceed 5%. These measurements were taken at 273 $\pm$0.5 K when the device was flat field illuminated. The error here were calculated from non-linearity measurement of the full-well capacity and the standard error of multiple image frames.

Linearity curves demonstrated in Figure 5.4 were used to calculate the full well capacity for each block. It is assumed that full well capacity is reached when the non-linearity exceeds 5%. However, blooming was not observed until 10% non-linearity was exceeded. Table 5.5 shows the full well capacity for each block of the device and provides a comparison with several Teledyne EMCCDs. There is little disparity in the results between the device regions. However, it is interesting to note that Blocks 7 and 8 have a slightly smaller full well capacity when compared to other regions of the device. The FWC per pixel area of the EMTC1 is either higher or comparable to modern EMCCDs, especially when the size of the pixel is considered.

5.3.5 Dark Current

The dark current is an intrinsic characteristic of image sensors and is a fundamental limitation of an image sensor. When an ideal device has 100% quantum efficiency, one photon incident on the device will produce a signal of a single electron. It is defined as the ratio of the number of electron-hole pairs created and successfully read out for each incoming photon. However, in all devices, there is an additional thermally dependent signal in the sensor that is attributed to the dark current. One of the main focuses of the scientific research and manufacture of image sensors is reducing the dark current and noise to enable more detailed images to be acquired at warmer temperatures.

5.3.5.1 Integration Time and Delays

The integration time of an image sensor is defined as the time during which charge is accumulated within each pixel. Increasing the integration time allows for a greater quantity of charge to collect, including dark signal. The rate of dark current generation limits the integration time over which useful signal can be collected. To minimise dark current the shortest integration time, which results in sufficient photon collection is selected.

Increases in thermal energy can lead to the excitation of electrons into the conduction band without any photoelectric input. The level of dark current is an intrinsic limit on the device performance, and its reduction is desirable. Impurities and imperfections in the semiconductor at the interface introduce additional energy levels into the forbidden band gap.

Most dark current sources are a product of pre-processing, fabrication and post-processing. It is possible to reduce the dark current by reducing the operating temperature according to the general dark current equation:

$$DC \simeq T^3 \exp\left(- \frac{E_g}{2kT} \right) \tag{5.8}$$

Where DC is the dark current, T is the temperature (in Kelvin), and E_g is the band gap in silicon. If a CCD is operated in multi-pinned phase mode, where a device is fully operated in an inverted mode during integration and readout, the interface is inverted resulting in a higher hole concentration [133] effectively suppressing the surface dark current.

As described previously; dark current is the generation of electron-hole pairs through thermal excitation. This is possible by either direct band-to-band exchanges or via intermediate states. In a pure silicon lattice, the generation/recombination of charge carriers is only possible by the band-to-band process. This process requires sufficient energy to directly elevate electron-hole pairs to the conduction band. Impurities can lead to the disruption of the silicon lattice and introduce additional energy levels into the band gap. Some impurities can be added unintentionally during the fabrication process; however, intentional doping can alter lattice structure. Unintended defects can also alter the silicon lattice results in additional energy levels that can act as intermediate centres for trapping charge carriers. These can subsequently act as additional sources of dark current. The net generation and recombination through these intermediate centres is calculated using the Shockley-Hall-Read equation [98]

$$U = \frac{\sigma_p \sigma_n v_{th}(np - n_i^2)N_t}{\sigma_n[n + n_i exp(\frac{E_t - E_i}{kT})] + \sigma_p[p + n_i exp(\frac{E_i - E_t}{kT})]} \tag{5.9}$$

where U is the generation/recombination rate, σ_n and σ_p are the electron and hole cross-sections, N_t is the concentration of the traps at energy level E_t, v_{th} is the thermal velocity and n and p are the electron and hole concentrations. The intrinsic Fermi level is given by E_i and the intrinsic carrier concentration is given by

$$n_i = \sqrt{N_v N_c}\exp\left(-\frac{E_g}{2kT}\right) \tag{5.10}$$

When the system is in thermal equilibrium then the generation/recombination rate is equal to zero. When U is negative, electron-hole pairs are generated; when positive, a recombination of electron-hole pairs occurs. If the cross-section for electron and hole trapping are assumed to be equal such that, $\sigma = \sigma_n = \sigma_p$, the net generation rate can then be given by

$$U = \frac{\sigma v_{th}(np - n_i^2)N_t}{n + p + 2n_i \cosh(\frac{E_t - E_i}{kT})} \tag{5.11}$$

There are three main regions within a CCD which contribute to the total dark current (see Fig. 5.6); a) the neutral bulk material beneath the potential well, b) at the Si-SiO_2 interface and c) the depleted material of the potential well [133].

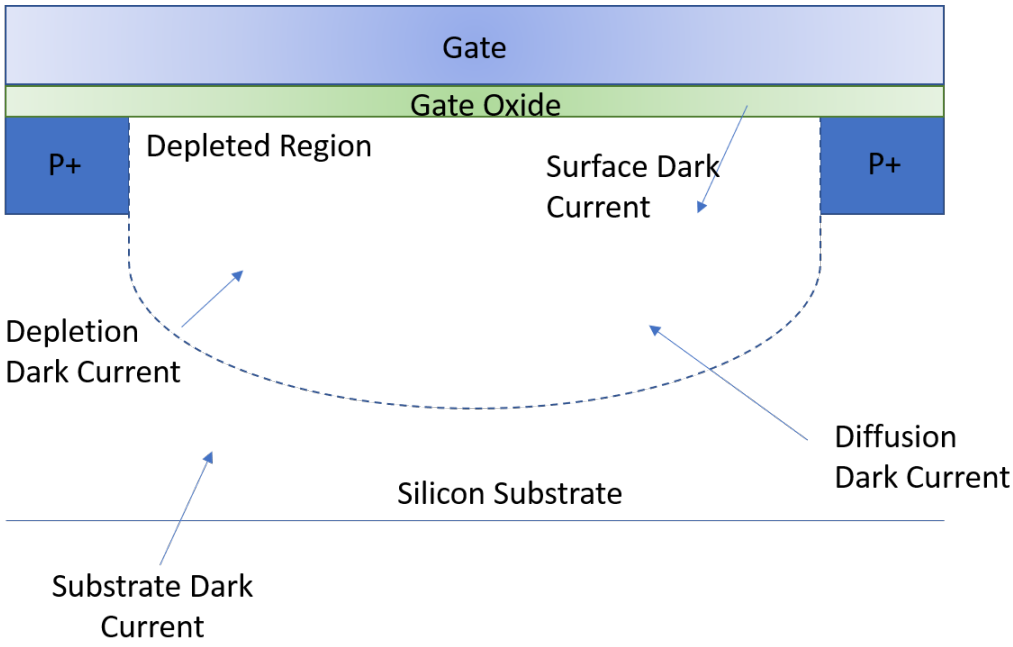

Figure 5.6: The sources of dark current within a photodiode, adapted from [56].

One of the main source of dark current is the Si-SiO_2 interface (surface) of the device. The difference in the number of available bonds between the silicon and the silicon oxide results in free 'dangling' bonds. Fabrication processes aim to passivate these bonds via the subjecting the silicon to a high-temperature hydrogen atmosphere. Hydrogen atoms bond with the dangling bonds, passivating them [103]. Any bonds not passivated, can act as interface states and can enable an electron to be excited to the midband level if there is sufficient thermal energy. If the device is exposed to radiation, the passivated bonds can be broken, and diatomic hydrogen can be liberated. Hydrogen will leak from the surface of the device, and the dangling bonds are recreated.

The depletion region is another source of dark current due to bulk traps. The area that surrounds the pn junction boundary is depleted of charge carriers, and any generated charge is swept away due to the electric field. It is possible for carriers to be excited thermally into the conduction band, a feat made easier if traps exist within the band gap providing bulk states. These traps can exist naturally within silicon; however, they can also be generated by displacement damage due to irradiation (discussed in Chapter 7).

5.3.5.2 Dark Current Measurements

Dark signal measurements were made at increasing integration times at several different temperatures. The statistical variations of the signal normally attributed to Poisson's distribution were minimised by averaging over several frames. The dark current could then be acquired from the gradient of the dark signal against the integration time and plotted as a function of temperature as plotted in Figure 5.7. Dark current is shown to increase temperature. Figure 5.7 was derived by measuring the average across the region of interest for each block. The errors were calculated from the standard deviation of the mean.

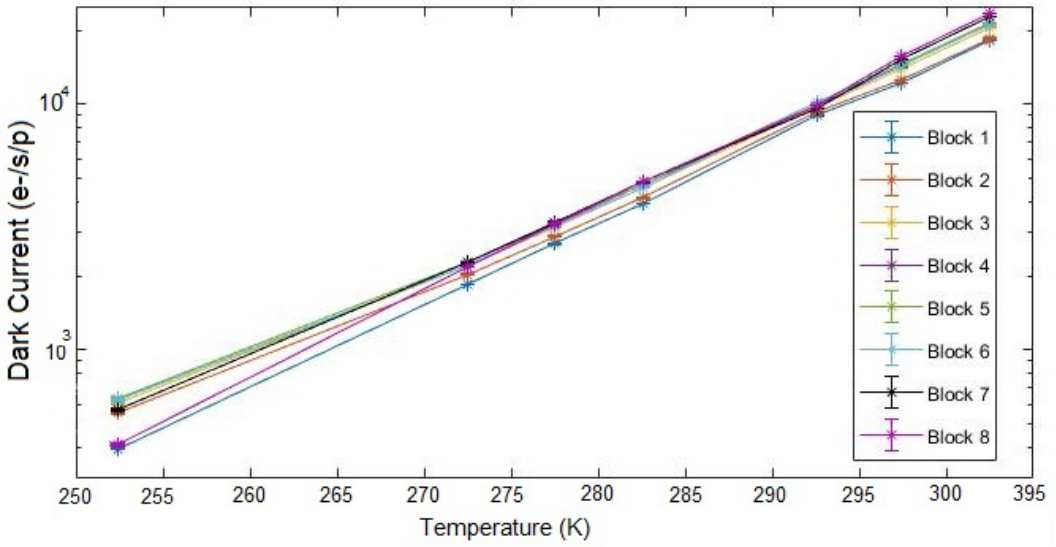

Figure 5.7: The dark current as a function of temperature for each of the optically sensitive blocks in EMTC1_B3.

It is important to note that the integration times were limited to 5 seconds due to system restrictions. However, full well capacity was not reached by dark current alone at room temperature and the measured non-linearity was low. To fully understand the impact of dark current on the imaging capabilities of the EMTC1, it is important to provide a comparison with modern commercially available image sensors.

The dark current results were converted into nA/cm^2, enabling a direct comparison of thermal signal generation independent of the size of the pixel.

Device	Pixel size (μm)	Dark current (e-/s/p)	Dark current (nA/cm^2)
Block 1	10	$8.99\times10^3 \pm 7.87$	$1.44 \pm 1.26\times10^{-}3$
Block 2	10	$9.26\times10^3 \pm 10.16$	$1.48 \pm 1.63\times10^{-}3$
Block 3	10	$9.79\times10^3 \pm 10.52$	$1.57 \pm 1.69\times10^{-}3$
Block 4	10	$9.87\times10^3 \pm 10.42$	$1.58 \pm 1.67\times10^{-}3$
Block 5	10	$1.01\times10^4 \pm 10.12$	$1.62 \pm 1.62\times10^{-}3$
Block 6	10	$1.02\times10^4 \pm 9.99$	$1.63 \pm 1.60 \times 10^{-}3$
Block 7	10	$9.60\times10^3 \pm 8.21$	$1.54\pm 1.32\times10^{-}3$
Block 8	10	$9.88\times10^3 \pm 5.72$	$1.58\pm 9.16\times10^{-}4$
CCD 30-11	26	6.86×10^4	0.247

Table 5.6: The dark current of the optical regions across each region of the EMTC1 and across three devices and the dark current for Teledyne e2v CCD30-11 in non-inverted mode, taken at 293 K. The error in this table was calculated from the standard error.

Table 5.6 demonstrates the dark current of each region of the EMTC1 and Teledyne e2v CCD30-11. It is apparent from both Table 5.6 and Figure 5.7 that the EMTC1 has high dark current. The dark current was largely uniform across the optical sensitive regions of the device and independent of the EM structure however the dark current of the non-EM regions (Blocks 1 and 2) are only slightly lower than the EM regions.

Figure 5.8 demonstrates dark current histograms for each region of the device at 3 different temperatures. The standard deviation of the dark current increased with temperature and the disparity of dark current between the EM and non-EM regions became more distinct at higher temperatures. It is of interest to note that there are a number of high dark current pixels in both the shielded and optically sensitive regions of the device. These can be attributed to a high local defect density on the device, likely a result of the fabrication process.

This was noted across all devices and the results presented above have been averaged over 5 testing runs and compared with several different test chips,

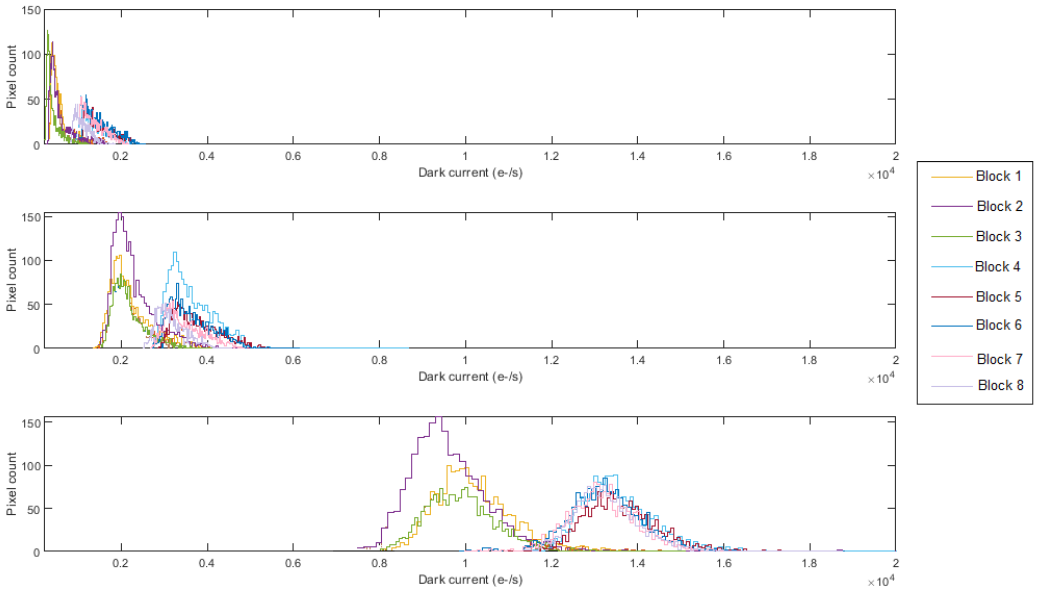

Figure 5.8: Histograms comparing the dark current for each device region when operated without illumination. The EMTC1_B3 was operated in darkness at (a) 253 K (b) 273 K and (c) 293 K.

and all were found to produce similar results. Further information pertaining to dark current will be discussed in subsequent chapters.

5.4 Image Quality

The cosmetic quality of each test chip was evaluated initially by taking a dark image at room temperature. An initial comparison of the dark frames provided insight into anomalies of the device. It is important to note that these devices were experimental and were not screened at the foundry.

Several devices had noticeable defects. This can be most clearly demonstrated in Figure 5.9(d), (f), (g) and (h) where there is a high concentration of hot pixels in centre of the image area. Of the chips shown in Figures 5.9 only EMTC1 (b) and EMTC1 (c) were characterised for testing, the other chips remained uncharacterised due to the large number of defects present. Figure 5.9 (d) demonstrates a semi-circle of hot pixels around the central point of the image. The location and shape of these defects imply a level of stress to the silicon surface during either the manufacturing process or during transport.

The majority of hot pixels in all the devices tested are centred around the bright line within the device.

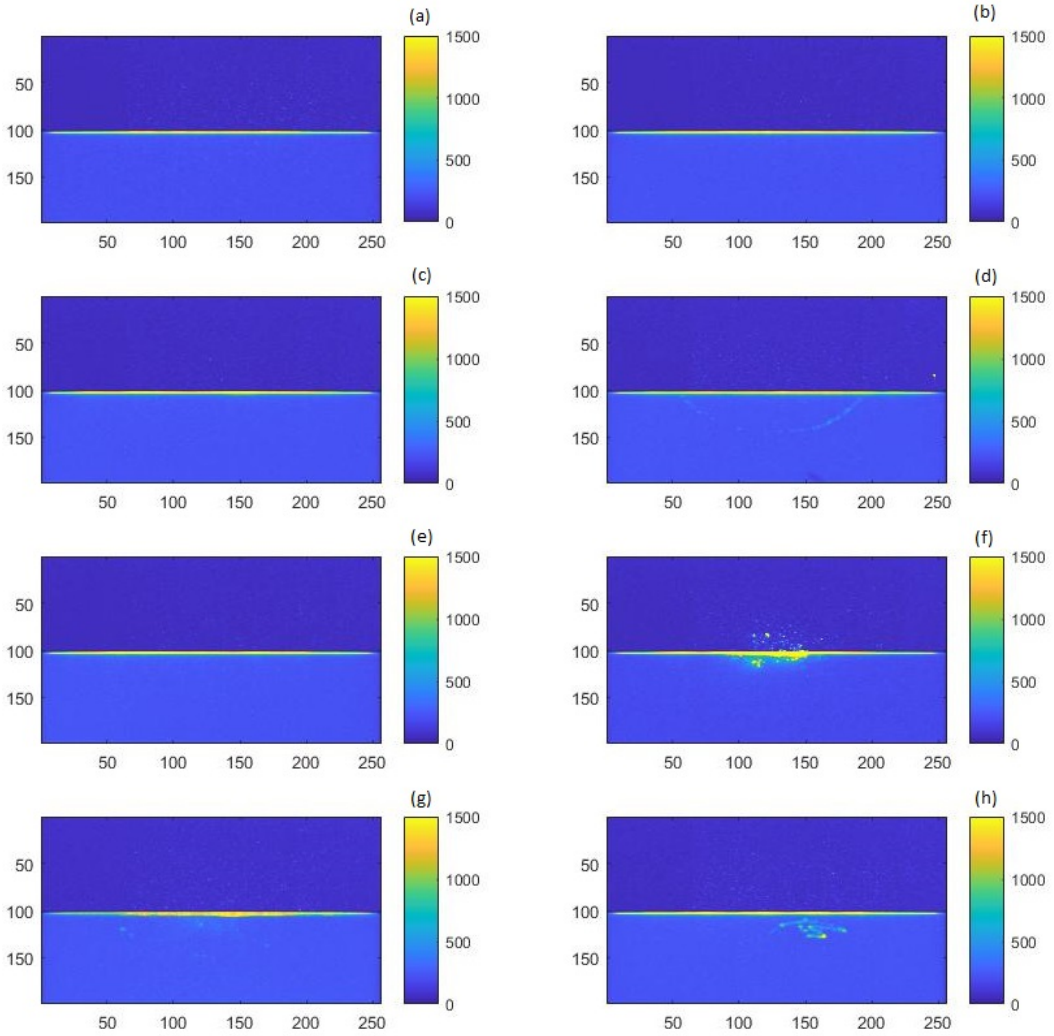

Figure 5.9: Dark frames at ≃293 K for a number of devices utilising the original experimental setup with the chip held in the socket. (a) EMTC1_C2, (b) EMTC1_C3, (c) EMTC1_C5, (d) EMTC1_C6, (e)EMTC1_C8, (f) EMTC1_C10, (g) EMTC1_C14, (h) EMTC1_17. These frames were taken when the device was operated with low P2HV voltage (i.e. without EM gain).

The bright feature in the centre of the device is due to the p-well (see Fig. 3.9) which captures the electron over-spill. The p-well blocks charge from entering the subsequent pixels. The charge is reflected to the pixels sitting outside the p-well which collect much larger charge than pixels in the middle of the imaging array. As a consequence, a bright band appears horizontally across the image splitting the image and the shielded regions.

As discussed previously; the experimental setup was altered to ensure a more efficient cooling from the TEC to the sensor. This was achieved by replacing the socket with a headboard onto which the sensor was directly soldered. To verify that no damage occurred during this process, a dark frame was then retaken at room temperature and compared. This can be seen in Figure 5.10 where the dark frames for EMTC1_B1, EMTC1_B2 and EMTC1_B3 pre and post soldering are shown. It is of interest to note that the dark frames pre soldering were significantly brighter than those from the chips directly soldered to the PCBs. This could be attributed to a slightly increased temperature when first tested or due to a light leak that was not experienced in the updated setup.

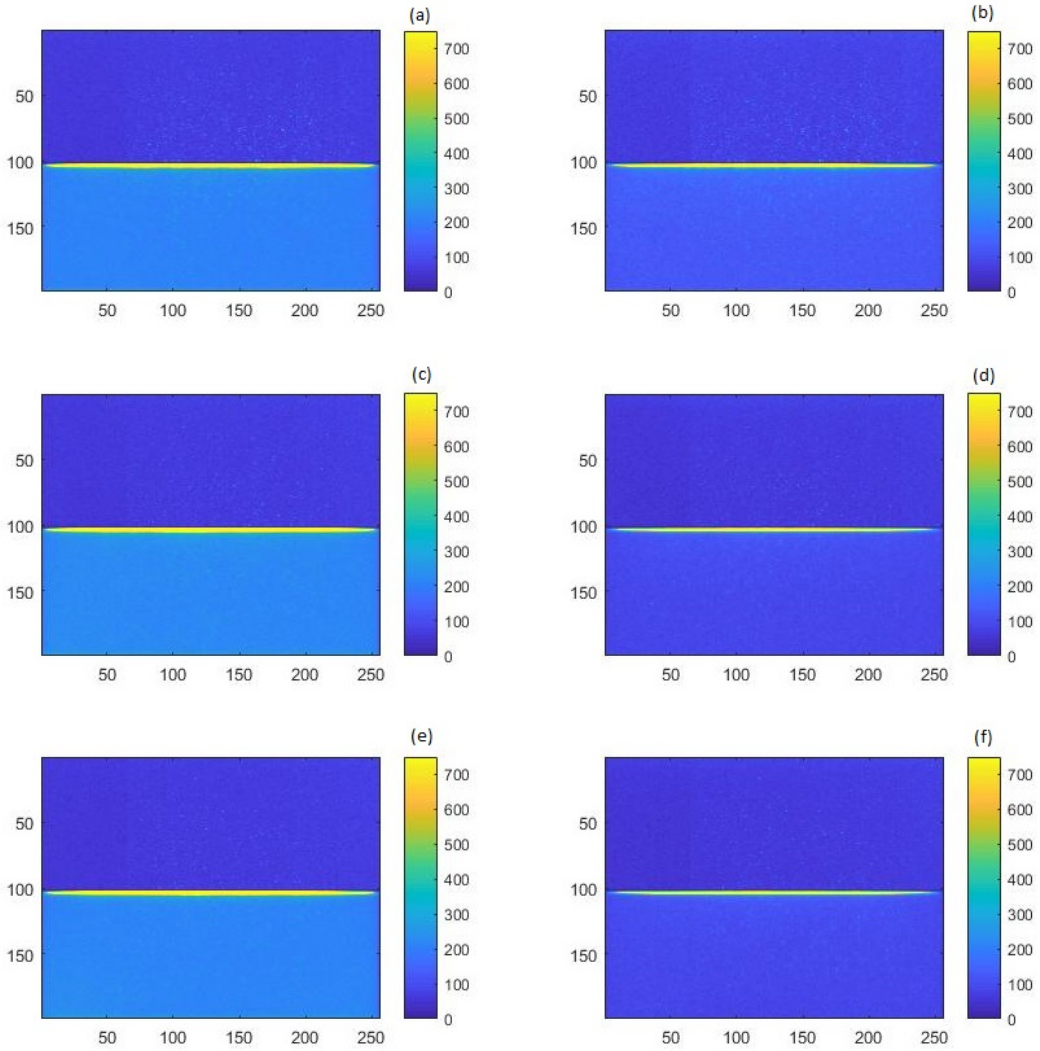

Figure 5.10: (a) EMTC1_B1, (c) EMTC1_B2 and (e) EMTC1_B3 before and after soldering to the headboard resulting in images (b), (d) and (f).

5.4.1 EM Gain

The operating principles of the EMCCD were discussed in Chapter 2. The novel structure of the EMTC1 was developed with the aim of increasing the EM gain achievable at low operating voltages.

Figure 5.11 demonstrates EM gain as a function of P2HV voltage with the P2DC voltage remaining constant at 3.0 V. The EM gain of pixel variants 5 and 6 (Blocks 7 and 8) increased to peaks of 118 and 116 total EM gain respectively as the device reaches saturation. The other pixels also experience an increase in gain in correlation with the increasing potential difference.

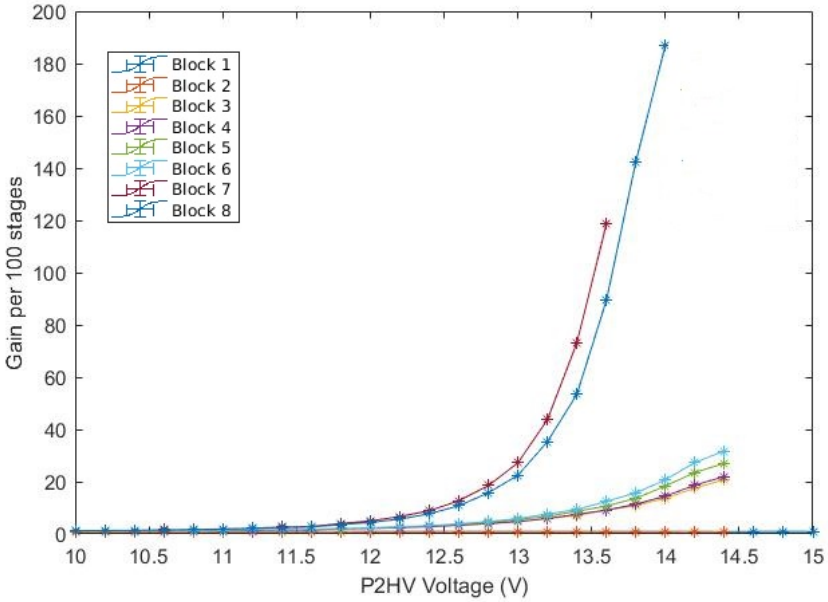

Figure 5.11: The EM gain for EMTC1_B3 as a function of P2HV for each EM pixel variant when illuminated with 1000 e- at 243 K. P2DC was held at 3.0 V.

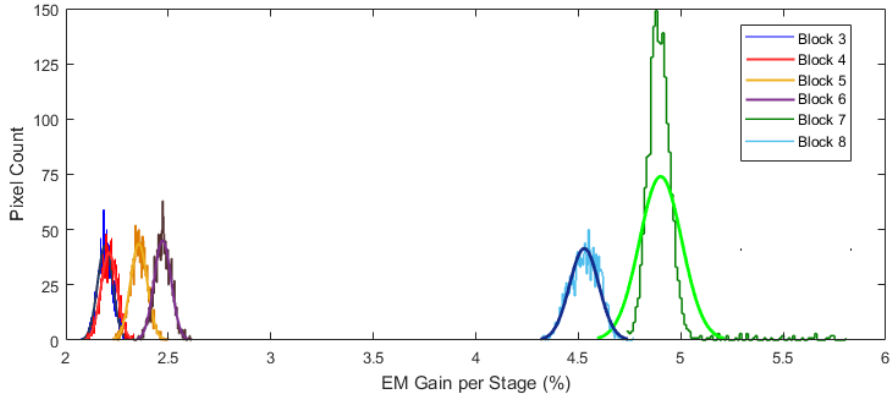

Figure 5.12: Histogram with Gaussian fits for each EMCCD region of the device of the EMTC1_B3 with a signal of 1000 electrons and operated with a P2HV voltage of 13.0V at a temperature of 273 ± 0.5 K.

Figure 5.12 shows the gain per stage distribution for each block at a high voltage allowing the operation of each EM pixel variant below saturation and normal distribution fit (detailed in Table 5.7). It can be noted here that the gain per stage was calculated using Equation 2.17 from the total EM gain. It is assumed that statistically, the gain at each stage is equal. Subsequently, the EM gain per stage can be assumed to be an averaged across all stages in the EM register. It is apparent that the novel design EM gain structures

Block	Standard deviation	Range	Skewness
3	0.037	0.241	0.167
4	0.039	0.236	0.050
5	0.041	0.271	0.009
6	0.042	0.285	0.009
7	0.103	1.072	4.761
8	0.071	0.449	-0.102

Table 5.7: The spread of gain for the EM gain for each EMCCD region of the device of the EMTC1_B3 with a signal of 1000 electrons when operated with a P2HV of 13.0 V at a temperature of 273 ± 0.5 K.

have higher gain spread than the rectangular EM gate structures. In addition, Blocks 7 and 8 experience a considerably higher skewness than other regions of the device. This can be attributed to a non -uniformity in the EM gain across the columns resulting in a number of 'hot columns' where the EM gain greatly exceeds the standard deviation. The exact cause of this is unknown; however, it is likely due to non-uniformity in the manufacturing process. The large spread in EM gain seen in Blocks 7 and 8 was experienced by all devices.

Measurements were made over a temperature range of 243 K to 303 K at intervals of 5 K, to understand the effect of temperature on the EM gain. It is important to note that the EMTC1 has only 100 EM stages. Many commercial devices often have several times this number, with the typical number of stages in a Teledyne e2v EMCCD around 500 stages [118, 112]. Thus, while the EM gain per stage in the EMTC1 would likely be considerably larger, the total EM gain in commercial devices may be much higher due to the larger number of stages.

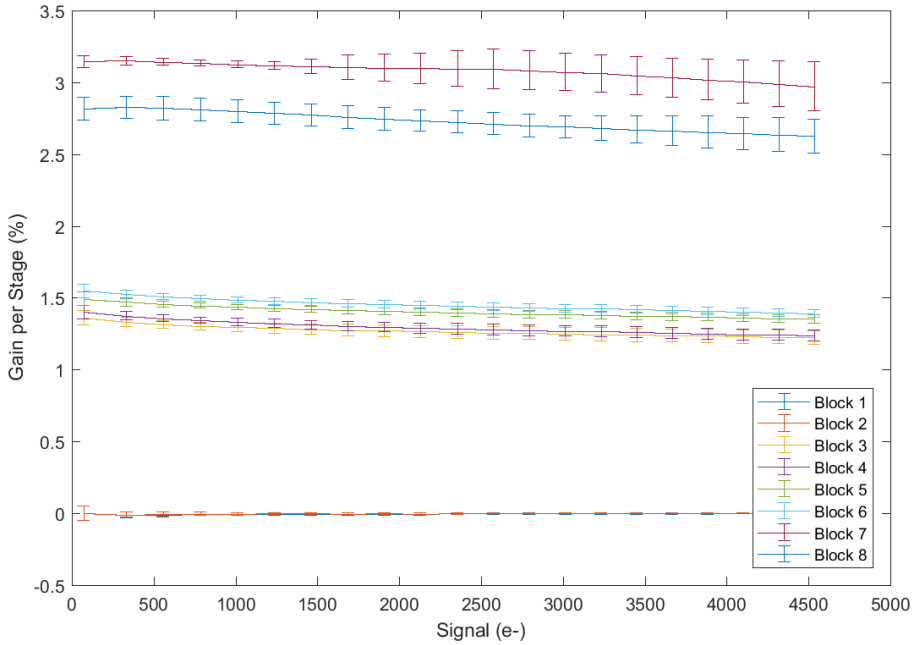

Figure 5.13: The EM gain per stage as a function of the signal at 273 K. The device was operated using the bias voltages found in Table 5.1 with P2DC and P2HV at 2.00 V and 13.00 V respectively.

Figure 5.13 demonstrates the EM gain as a function of the signal when the device was operated with a P2HV bias of 13.00 V with increasing illumination intensity. As the signal increases towards full well and ultimately saturation the EM gain decreases linearly. The coefficients of the fits for each region of the device can be found in Table 5.8. Subsequently, the functional input signal when EM is utilised falls below the full well capacity measured under non-EM conditions.

Block	a	b
Block 3	-4E-05	1.48
Block 4	-5E-05	1.55
Block 5	-4E-05	1.69
Block 6	-5E-05	1.78
Block 7	-6E-05	4.34
Block 8	-7E-05	3.75

Table 5.8: The coefficients for the fits of the linear decrease of gain with signal when the device was operated with a P2HV bias of 13.00 V and P2DC of 2.00 V at a temperature of 273.0 $\pm$0.5 K. The input signal was increase incrementally. The fit equation is in the form of y=ax+b. Data from Figure 5.13.

The EM gain was measured as a function of P2HV voltage for each region of the device. The gain increases rapidly at voltages between 12.5 and 13.5 V for Blocks 7 and 8.

As the EM gain increases, there is an increase in gain non-uniformity across each region of the device. This in part, can be attributed to the stochastic nature of the EM gain process. EM Blocks 7 and 8 experience considerably higher EM than other regions of the device and even at relatively low signal experience saturation.

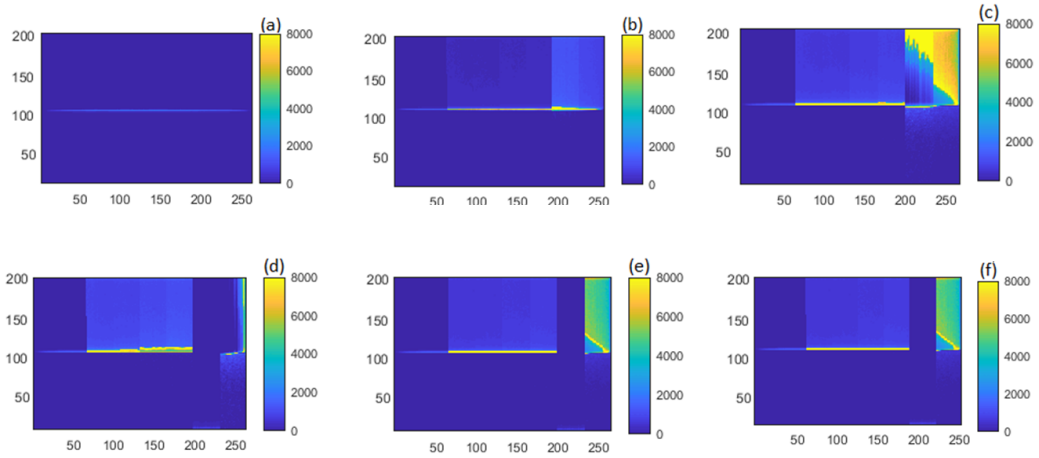

Figure 5.14: The image area response with an optical signal of 1000 e- at room temperature. The device was operated at different P2HV voltages to measure the signal. (a) EMTC1 operated with no EM gain (P2HV biased at 3.00 V), (b) P2HV = 11.00 V, (c) P2HV = 12.50 V, (d) P2HV = 13.00 V, (e) P2HV = 14.00 V, (f) P2HV = 15.00 V. The colour-bar denotes the signal level in ADU after an integration period of 100 ms. The axis denotes the rows and columns of pixels.

Figure 5.14 demonstrates the image area response when the device was illuminated with a signal equivalent to 1000 electrons at increasing P2HV voltages. The numbered axes denote the rows and columns of the pixel array. The different pixel regions can be seen distinctly as the HV gate voltage increases. As the HV bias is increased the gain increases until the device begins to reach saturation. Figure 5.14 (a) demonstrates that when the device is operated without gain, the image area is uniform. As the P2HV voltage increases the different regions become more defined until saturation begins to occur. At higher voltages blocks 7 and 8 experience blooming across the image area, this saturation is most apparent in Figures 5.14 (c) and (d).

The gain for the novel pixels can be compared to EMCCDs and the voltages required. The EM gain for each region of the device and several commercial Teledyne e2v EMCCDs can be found in Table 5.9. EM blocks 7 and 8 were designed with the aim of increasing the EM gain achievable in an EMCCD. Commercially available devices often (e.g. CCD97) have $\geq$ 400 stages in comparison to the EMTC1's 100 stages. The EMTC1 is able to achieve a maximum

Device	P2HV (V)	Gain per stage (%)
Block 3	15.0	2.57 ± 0.20
Block 4	15.0	2.65 ± 0.06
Block 5	15.0	2.84 ± 0.05
Block 6	15.0	2.94 ± 0.06
Block 7	13.6	4.81± 0.08
Block 8	13.8	5.92± 0.09
CCD201-20	45	1.08
CCD60	45	1.06
CCD97	45	1.07

Table 5.9: Average EM for each region of the device compared to several Teledyne e2v EMCCDs at 273 K. The device was illuminated with signal generating 1000 electrons. The errors here were calculated from the standard error.

EM gain of 5% per stage at 13.8 V compared to CCD201-20's 1.5 % at 45 V. It is apparent that the EMTC1 is able to achieve at least double the EM gain per stage at a third of the voltage. Blocks 7 and 8 are able to exceed the EM gain of commercial EMCCDs by 400% at less than a third of the voltage. This increased EM was largely predicted by simulations completed by Stefanov et al. [105] seen in Figures 3.4 and 3.6. In a traditional EMCCD gate structure, the charge and impact ionisation are spread along the length of the leading edge. This results in a loss of charge at the edges of the high voltage gate and a reduction in the number of electrons that can induce ionisation. Block 7 (the staircase pixel) increases the leading edge length and area through which electrons pass is much larger than in traditional rectangular structure. The spike structure was also simulated and demonstrated that the reduction in the distance between the HV and DC gate was reduced as the gate structure is progressively narrowed corralling the charge into an area of high charge carrier density. Subsequently, for both EM pixels an increase in EM line comparable to the increase in electron density and the leading edge length was expected.

However, the increase in EM gain achieved by the rectangular gate structures in the EMTC1 (Blocks 3-6) was not simulated before the EMTC1's fabrication. This increase in gain can be attributed to the thin gate structure achieved in the CMOS process. This effect will also contribute to the increased gain achieved by blocks 7 and 8.

Further description of the charge transfer process, which occurs in these new pixels will be discussed in subsequent chapters providing insight into the effect of the charge transfer on the EM gain.

5.5 Conclusion

This chapter provides a summary of the initial characterisation of the EMTC1 and a comparison with several commercially available EMCCDs. The results have demonstrated that the EM gain in EMTC1 is superior to traditional EMCCDs.

Several of these characterisations will be repeated in subsequent chapters testing the lifespan of the device. This chapter focuses on the optimisation of the device operating conditions. A description of the optimisation of the device in relation to the charge transfer, the signal to noise ratio and achieving the maximum gain will be provided in the next chapter which focuses on the charge transfer process in the EMTC1.

Chapter 6

Charge Transfer in the EMTC1

6.1 Introduction

Integral to the function of a CCD is the ability to successfully transfer charge between electrodes and pixels through to readout. Charge transfer is often characterised in terms of Charge Transfer Efficiency (CTE) or Charge Transfer Inefficiency (CTI). The relationship between CTE and CTI is such that CTI=1-CTE.

This chapter discusses the charge transfer process within CCDs, EMCCDs and then focuses on charge transfer in the EMTC1. The effect of altering the device biasing and the EM gain is discussed. This is achieved in the form of device simulation and experimental analysis. An in-depth study into the effect of the size and shape of the high voltage gate on charge transfer in the EMTC1 has been conducted, providing a direct comparison between the different factors that may affect the charge transfer process.

6.2 Charge Transfer and the Trapping Model

The modern CCD has been developed to ensure that there is minimal loss of charge between each transfer. The charge is 'lost' when it becomes trapped in defects. The introduction of the buried channel aimed to move charge away from the surface where it is prone to becoming trapped in surface defects at

the Si- SiO_2 interface, such that the interaction of the signal packet with traps within the bulk region is the only interaction that needs consideration.

6.2.1 Factors affecting the CTI

As previously stated, the charge transfer process does not result in a complete transfer of charge; it is also not an instantaneous transfer. CTI provides a quantitative analysis of the charge lost during a transfer. The effectiveness of the transfer process (or the CTE) is dependent on several factors:

- The temperature of the device directly affects the charge transfer inefficiency. The CTI will decrease at low temperature because the trap emission time constant is very long, keeping the traps nearly permanently occupied. At high temperatures, the CTI also decreases due to rapid emission of trapped charge into the same signal packet.
- The CTI is inversely proportional to the signal packet density.
- Background charge which can fill the bulk traps leading to a reduction of the CTI.
- The type of defect which determines the emission and capture time constants.
- The CTI is proportional to the trap concentration.
- The timing of the transfer, which is selected considering the emission time constant.

The efficiency of the charge transfer is often dependent on the nature and number of traps within the sensor. As described in Chapter 2 traps can capture charge in a number of different ways. Furthermore, a defect can capture charge carriers and emit this charge after a time delay. If a defect has an energy E_t below the conduction band, the Shockley-Read-Hall theory can give the capture time constant (τ_c)

$$\tau_c = \frac{1}{\sigma_n \nu_{th} n_s} \tag{6.1}$$

and the emission time constant (τ_e)

$$\tau_e = \frac{1}{\sigma_n X_n \nu_{th} N_c} \exp(\frac{E_t}{kT}) \tag{6.2}$$

Where σ_n is the electron capture cross-section, X_n is the entropy factor due to electron emission, ν_{th} is the thermal velocity, N_c is the density of states in the conduction band, and n_s is the density of the signal packet. If the emission time constant is larger than the transfer time, then the released charge does not re-join the signal packet from which it originated. The remaining charge is then merged with the charge in a subsequent signal packet. The dependence of the emission time constant on temperature is apparent in Equation 6.2 where at low temperatures, the emission time constant can be of considerable magnitude ($\simeq ms$). Even though the dark signal is small at low temperatures, the traps can be filled with charge so that they cannot trap any additional charge and the CTI is low.

6.3 Charge Transfer Modelling in CCDs

The transfer of charge through an EMCCD has been described briefly in Chapter 2. This section will focus on charge transfer models for both CCDs and EMCCDs.

6.3.1 Charge Trapping

Figure 6.1 demonstrates simulation data of a Teledyne e2V CCD 97-00, a back-illuminated 2-Phase IMO Series EMCCD. This device was simulated by construction the CCD97-00 image area and standard register pixels within a commercial TCAD software package (Silvaco©) to enable the measurement of the potential profiles of the pixels when clocking at different stages. The models were 2D in nature. The profile was symmetrical and flat towards the centre of the pixels such that the functional form of the potential profile within this simulation was representative of the whole pixel. Parameters relating to the manufacturing of the pixel was simulated, including the implantation, dopant diffusion and polysilicon deposition process. In addition, the geometry of the pixels was set in accordance with standard Teledyne e2V design parameters, including the width of the dielectric layers. The device was simulated with an initial signal packet of 1000 electrons at room temperature and biased with P1 = 6.5 V and P2HV = 46.0 V. These values and the clocking conditions of

the simulated results are consistent with the operational settings of the CCD 97-00 [118].

This simulation was completed at high gain requiring the modelling of the impact ionisation process. Appropriate physical models were chosen to simulate the device physics, including the Lombardi mobility model [69] which has been shown to have a range of applications in MOS devices. The impact ionisation process was imperially modelled through a modified method originally proposed by Lackner [65, 80]. One of the most accepted models, it is based on Chynoweth's law [18] which proposes that the impact-ionisation rate is expressed as the inverse of the electric field and was later validated by Van Overstaeten and De Man [131]. The Lackner model built on the work from Chynoweth's mode and proposed an analytical change to the model adapting for field correction. This method was modified to tailor the parameters specifically for the case of the EMCCD by comparison with measured values [118]. The transfer was performed with an initial signal of 300 electrons and clocked using timings for clock pulses consistent with a device operated at 10 MHz.

The movement of charge within the simulated structure started with the lowering of the P1 clock such that the signal packet moves to beneath the DC phase. Subsequently, the signal packet is accelerated towards the interface region before collecting beneath the high voltage phase.

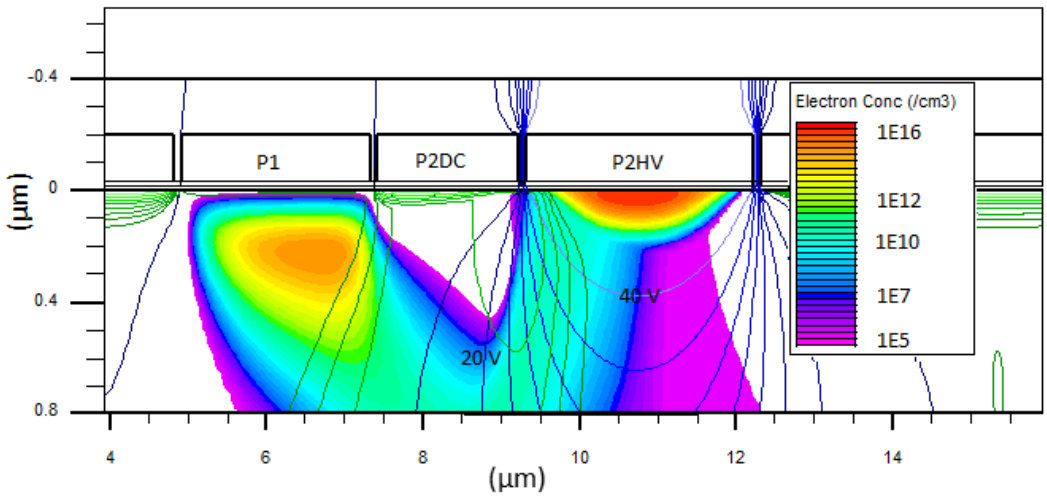

Figure 6.1: Electron concentration at a point during the charge transfer process of an EMCCD when the P2HV = 40 V. The contour lines are at 5 V space.

The simulation data, shown in Figure 6.1 demonstrates that the charge

packet can come into contact with the surface , even when a buried channel is implemented if the P2HV is sufficiently high.

Figure 6.1 demonstrates the carrier concentration and potential when 50% charge had been transferred. The high field region is located between the DC and HV gate. It is here that the energy is gained by carriers due to successive collisions. The energy gained exceeds that lost to scattering processes (dominated by phonon scattering). The carriers can be seen to extend close to the interface. It is here that they may become trapped.

Some interface traps are created during the fabrication process, but many are due to damage the device undergoes via hot carriers. The traps lead to a decrease in the signal packet for each transfer as the charge carriers are removed from the electron cloud and trapped for a trap-dependent time period. An increase in the number of traps leads to a decrease in the charge transfer efficiency and a subsequent increase in the image smearing and device noise.

6.4 Charge Transfer in the EMTC1

As described previously, the EMTC1 has several different P2HV gate structures, which vary in size (width and length). The charge transfer process was simulated for several pixel geometries. The following section provides a description of charge transfer for each EM gate structure and a simulation.

The EM gate structure have been thoroughly discussed earlier in this thesis (see Tables 3.1 and 6.1), however, to provide an understanding of the charge transfer, the device was simulated as it enabled several parameters to be quantified, such as the carrier concentration and the impact ionisation regions.

Pixel Parameters			
Block	HV Gate Type	Length (μm)	Width (μm)
Block 3	Rectangular	3.0	6.0
Block 4	Rectangular	2.5	6.0
Block 5	Rectangular	3.0	5.0
Block 6	Rectangular	2.5	5.0
Block 7	Staircase	2.5-3.5	5.0
Block 8	Spike	1.6-2.6	5.0

Table 6.1: EM pixel sizes in EMTC1.

The simulations were completed using Atlas, a commercial software provided by Silvaco similar to the simulation completed for the CCD 97-00. The models were 2D in nature which did limit the simulation of blocks 7 and 8. Many of the parameters relating to the manufacture of the pixel were simulated including the width of the dielectric layers and the dimensions of the phases. However, the exact details of the fabrication process remain the intellectual property of the ESPROS company. Subsequently, some details of the simulation including the doping were based on the Teledyne e2v CCD 97-00. The simulation parameters were selected to ensure that the simulation matched the device physics and normal operating conditions for the EMTC1. The biases are shown in Table 6.2 and matched those used in the initial experimental characterisation. This was in part to confirm that the EM gain can be correlated to the used voltages and the shape and size of the HV gate. An input signal of approximately 1000 electrons was simulated to perform the transport.

Electrode	Bias (V)
RD	4.0
OG	2.5
P2DC	1.5
P1234 Low	0.0
P1234 High	4.5

Table 6.2: The values for the optimised bias conditions. Due to the number of different electrodes altered this is called Bias 5.

A mobility model was selected, based on a Lombardi model proposed in [70] and an impact ionisation model which was based on one proposed by Selberherr [96]. The simulation was completed at 293 K. Furthermore, the simulated device was clocked using timings for 10 kHz line rate. The simulation was time-stepped to enable the output of the device parameters in a format that allows for a visualisation of the impact ionisation regions, carrier concentration and the current density.

The device model was illuminated, and charge allowed to collect within an empty potential well under P1. As the P1 clock was subsequently lowered, the signal packet which has been collected moves beneath the P2HV gate undergoing impact ionisation during this transfer.

6.4.1 Two-dimensional Simulation of the EMTC1

For the two-dimensional simulation, it was not possible to model the shape of the HV electrode. As such, the focus of this section is on the effect of the length of the electrode. The device was simulated for P2HV gate lengths 1.6, 2.5, 3.0 and 3.5 μm.

The P2DC gate length was kept at a constant length of 1.9 μm, independent of the P2HV gate length. The voltages P2DC and P2HV were set at 3.0 V and 15.0 V respectively.

Figures 6.2 and 6.3 shows the simulated results for each P2HV gate length. As the P1 clock is lowered, the signal packet moves from beneath the DC gate and accelerates towards the interface before collecting beneath the HV gate.

The highest field is found at the midpoint between the DC and HV gates, and it is here that the majority of impact ionisation occurs. The primary region of impact ionisation shown in Figure 6.3 extends close to the device interface. Beyond the field midpoint, the carriers are no longer in thermal equilibrium with the silicon lattice. The charge was transferred through the device as described above for several gate widths.

In the region which extends towards the interface, it can be assumed that some of these carriers are of high energy. As such, it is possible to assume that the carriers interact with the interface and are injected into the gate stack. It is also possible to see an additional region of impact ionisation that sits beneath the DC gate. It is interesting to note that this mirrors simulations completed for a traditional EMCCD [80] however, the EMTC1 simulation does not extend as deeply beneath P2DC. The impact region can be a source of both energetic holes and electrons, both of which may have sufficient energy to interact with interface states.

Increasing the length of the P2HV changes the location and shape of the impact ionisation, as shown in Figure 6.3. As the gate length increases the position of the peak electric field shifts along the channel in the direction of the charge transfer (left to right) [58]. This shift moves the centre of the electric field towards the P2HV, strengthening the electric field and causing the potential to extend deeper beneath the high voltage gate. It could be assumed that by moving the impact ionisation region further away from the interface that less interaction would occur however the impact region beneath the DC gate is a source of holes [80] which can have sufficient energy to interact with the interface leading to further trapping. Furthermore, as the gate length increases the impact generation region also extends further into the substrate, moving the region away from the interface. By moving the impact generation region away from the interface, the signal packet is less likely to interact with the interface reducing the charge trapping. This result would hypothesise that there would be an increased CTE for the longer gate lengths and potentially higher EM gain. The impact of this will be seen in the ageing process. Furthermore, it is apparent from Figure 6.2 that as the gate length increases from 1.6 μm to 3.0 μm the electron cloud shifts further away from the interface beneath the P1 and P2DC interface. This coincides with the second ionisation region seen beneath the P2DC gate.

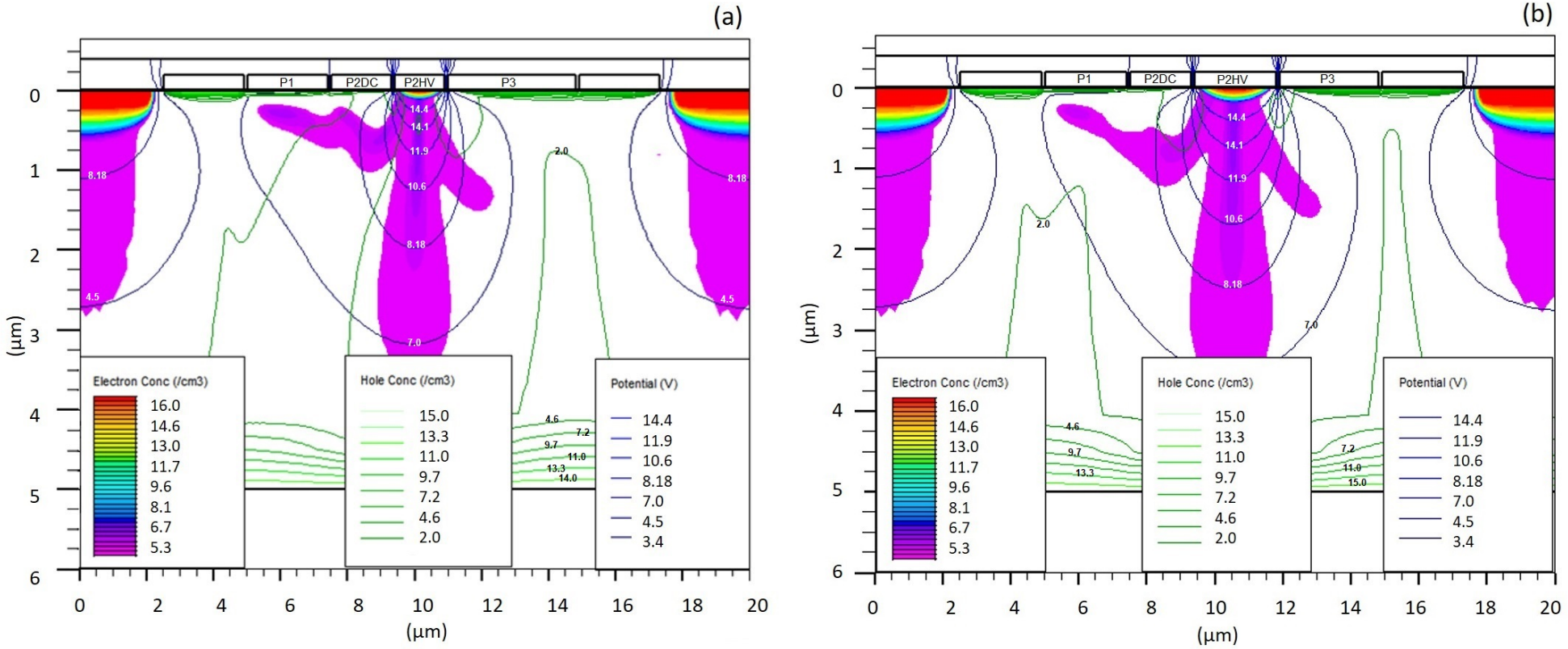

Figure 6.2: Simulation data for the EMTC1 at 273 K for increasing lengths of P2HV gate showing the electron concentration, hole concentration and the potential after an initial ramp period of 4×10^{-9} ns. P2DC was biased at 3.0 V while P2HV was clocked at 15.0 V. (a) P2HV gate width 1.6 μm and (b) 3.0 μm.

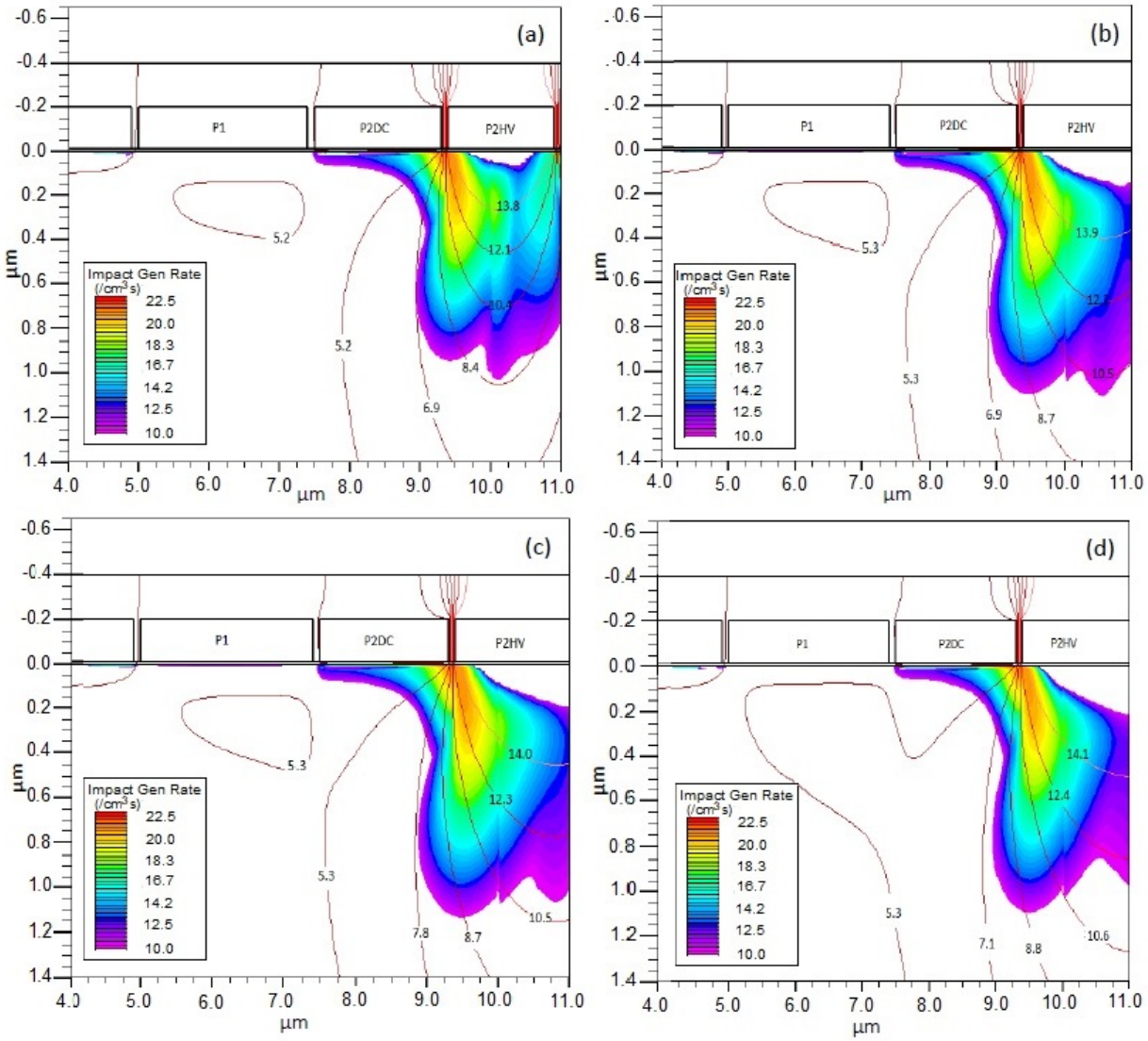

Figure 6.3: Simulation data for the EMTC1 at 273 K for increasing lengths of P2HV gate demonstrating the regions of impact ionisation. (a) 1.6 μm, (b) 2.5 μm (c) 3.0 μm and (d) 3.5 μm when 50 % of the charge has been transferred from P1 to P2HV. P2DC was biased at 3.0 V while P2HV was clocked at 15.0 V. The contours denote the potential in volts [27].

At the longer P2HV lengths the potential extends much further beneath the P2DC gate. For the 1.6 μm length this potential extends to beneath the P1-P2DC interface. As such, it is apparent that the location of the charge cloud (for both electrons and holes) shifts dependent on the gate length. As the gate length decreases, the charge packet extends deeper from the Si-SiO_2 interface due to its smaller size in the direction of transfer.

As discussed previously increasing the length of the gates results in the central field distribution shift along the channel away from the P2DC gate. This leads to an increase in the electric strength in the impact generation region and increases the size of the impact generation region. At longer gate lengths, the length of time for complete transfer is reduced. As the gate increases in size, the potential under it in the buried channel also increases. Therefore, the electric field contributing to EM also increases, and so does the volume where EM takes places.

Figure 6.3 demonstrates this increase in impact ionisation and the shift in the potential lines. Subsequently, we can expect the EM gain to increase with gate length as a function of gate size and subsequently, the length of the leading edge. Furthermore, it is important to note that as the length of the leading edge increases, the potential lines and charge cloud moves further away from the interface and into the bulk of the device.

6.4.2 Effect of the potential difference between P2DC and P2HV

Early experimental results indicated that the EM gain changed considerably with the P2DC bias despite the P2HV-P2DC potential difference remaining constant. It was hoped that by simulating the transfer, a greater understanding of the charge transfer process could be attained. Previously it had been assumed that the strength of the field is dependent on the potential difference between the two gates, not the voltage of the independent gates. As such, any variation in the field and subsequently the EM gain, should not be affected by altering the voltages of the gates as the same potential difference is maintained.

6.4.2.1 Simulation Results

The simulation mirrored the operation of the device during the collection of the experimental data. The device was simulated with a signal of 1000 electrons at 273 K.

The bias voltages utilised were set as those seen in Table 6.3 such that the potential difference between the P2DC and the P2HV gate was kept constant at 11.8 V.

P2DC (V)	P2HV (V)
1.6	13.4
2.0	13.8
2.4	14.2
2.8	14.6

Table 6.3: The simulation bias voltages during the EM transfer of charge.

It is known that by altering the potential difference, there is a direct effect on the electric field and subsequently EM gain. It was apparent from Figure 6.4 that by increasing the P2DC voltage, the EM gain not only increases with the P2DC voltage but also demonstrates that the transfer time dramatically decreases at higher voltages.

From Figure 6.5 it is apparent that increasing the P2DC voltage results in a shift of the electron cloud closer to the interface. As the P2DC voltage increases, the percentage of charge transferred from the P1 gate to beneath the P2DC gate not only dramatically increases, it also alters in shape, moving closer to the gate and entering a region of stronger electric field. As such, it can be concluded that the increase in the EM gain at higher P2DC can be attributed to an increase in the transfer efficiency between the two gates preceding the avalanche gate. A discussion of the experimental results pertaining to the effect of the potential difference can be found later in the chapter.

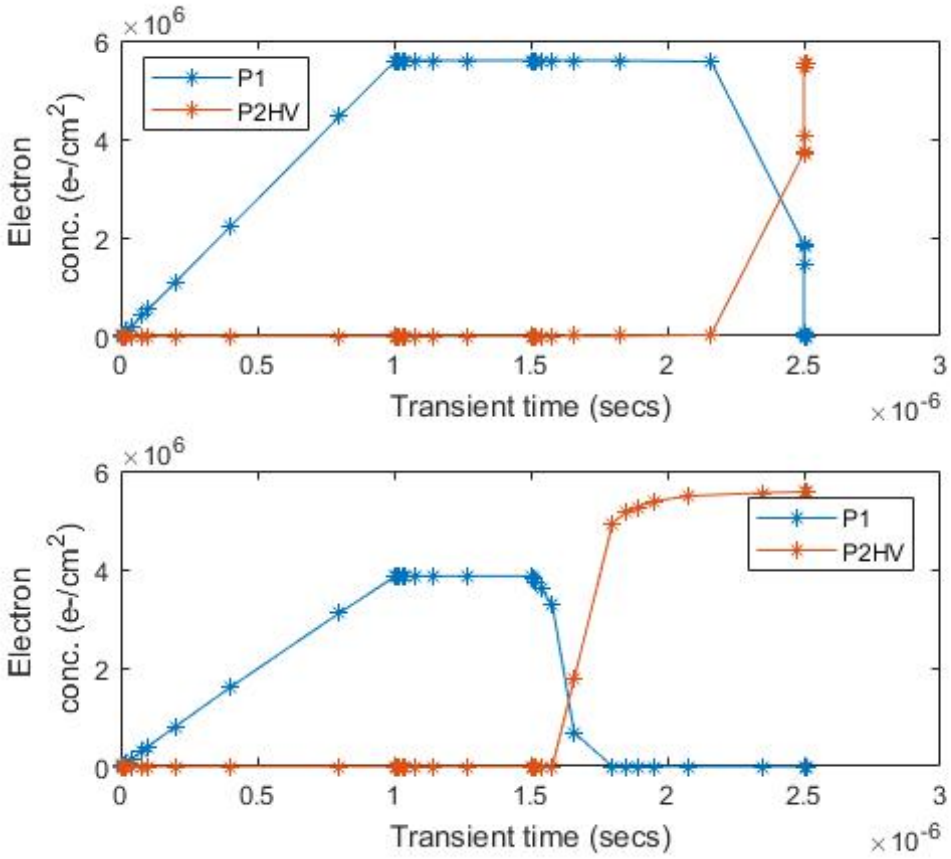

Figure 6.4: The simulation results for the electron concentration beneath the P1 and P2HV gate during impact ionisation as a function of the transient time using a rectangular gate structure. The device was simulated at 293 K and a signal of 1000 electrons. The P2HV gate length was kept constant at 2.5 μm. (Top) P2DC=1.0 V and P2HV=13.0 V (Bottom) P2DC=2.0 V and P2HV=14.5V.

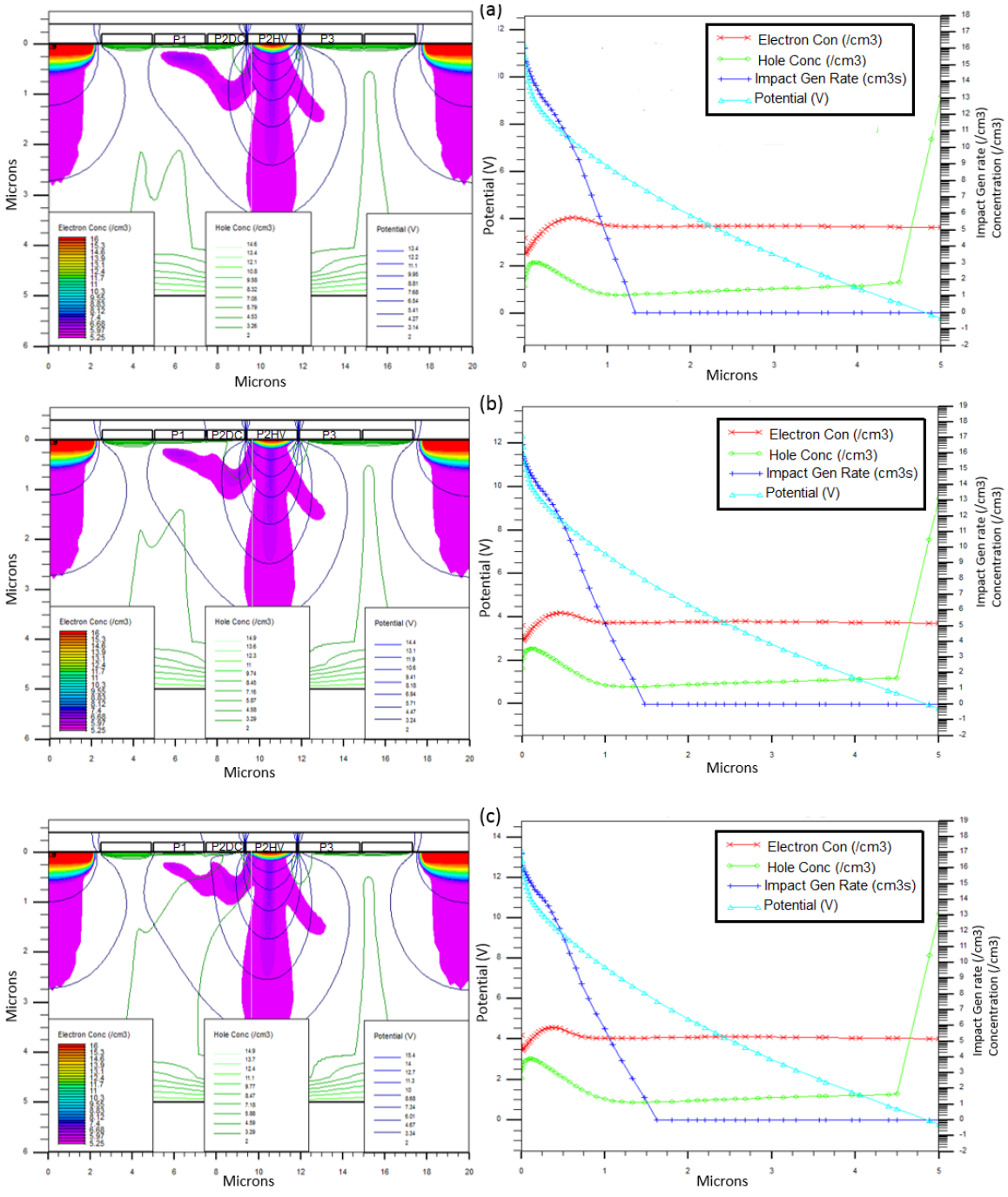

Figure 6.5: Simulation data for the EMTC1 at 273K a gate width of 2.5 μm demonstrating the electron concentration, hole concentration and the potential after an initial ramp period. (a) The visual interpretation and the data is along the grey cutline (9.4,0) to (9.4,5.0) μm when P2DC=1.0 V and P2HV = 12.8 V (b) P2DC=2.0 V and P2HV = 13.8 V and (c) P2DC=3.0 V and P2HV = 14.8 V.

6.4.3 Experimental Results

These results were then compared to experimental data for the EMTC1_B3. The device was operated at 273 K and illuminated with a signal of 1000 electrons. The device was biased using the conditions found in Table 6.2. However, the biasing of P2DC and P2HV were altered such that the potential difference remained constant at 11.8 V. This voltage was selected due to its ability to get a range of P2HV values without reaching saturation.

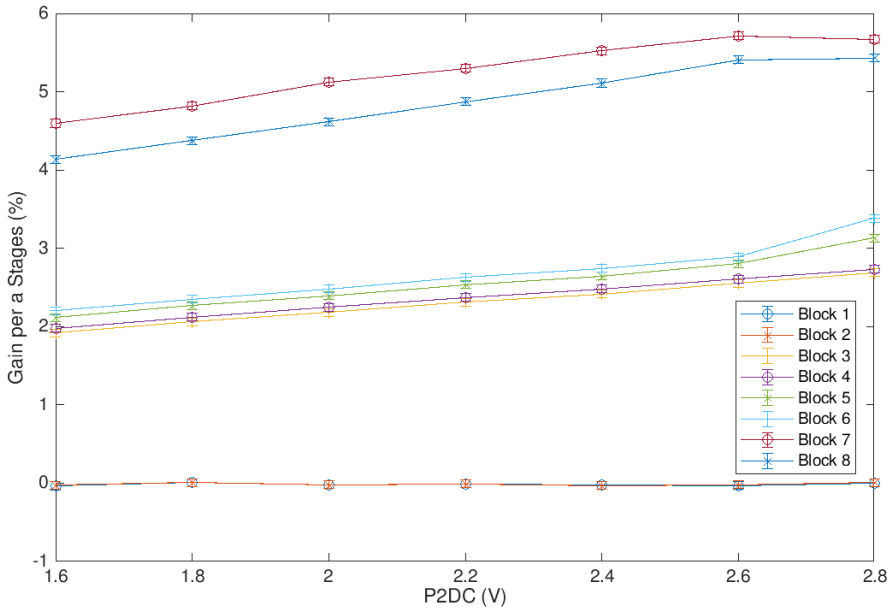

Figure 6.6: The EM gain per stage as a function of the DC gate bias for each region of the device at 273 K with a signal of 1000 electrons. The potential difference between the DC and HV gate was kept constant at 11.8 V.

The EM gain increased linearly with the P2DC voltage with Blocks 7 and 8 able to exceed 5 % as shown in Figure 6.6. Insight into this process can be seen in Figure 6.5. As the potential on both gates increases, the electric field potential peaks closer to the gate. The electron concentration extends closer to the DC gate. As such, by comparing with the impact ionisation regions seen in Figure 6.3 it is possible to see that the impact ionisation region will extend deep beneath the P2DC gate. Subsequently, a higher percentage of charge carriers will enter the impact ionisation region. It is interesting to note that at the higher voltages, the holes also extend to beneath the DC gate and are more

likely to interact with the interface. This would likely lead to an increase in the ageing process, as discussed in Chapter 8. As described previously, the DC gate often acts as a barrier to charge spill back. By increasing the P2DC gate voltage, the potential well increases, 'raising the barrier' reducing accelerated charge spill-back.

Furthermore, while the potential difference remains constant, the increased voltage leads to a greater percentage of the charge being pulled through the impact ionisation region from P1 to P2HV. If there is less loss to charge trapping and spill back, the signal charge packet is larger before it undergoes impact ionisation. Subsequently, there is an increase in EM gain per stage that is demonstrated in Figure 6.6.

6.5 Charge Transfer Inefficiency in the EMTC1

The CTI was measured using the Extended Pixel Edge Response (EPER) technique. This is achieved by flat-field illuminating the image area and measuring the quantity of deferred charge in the extended pixel region [56].

Figure 6.7 demonstrates the last row (the second smaller peak) followed by a 'tail' of deferred charge until the average background signal value is reached.

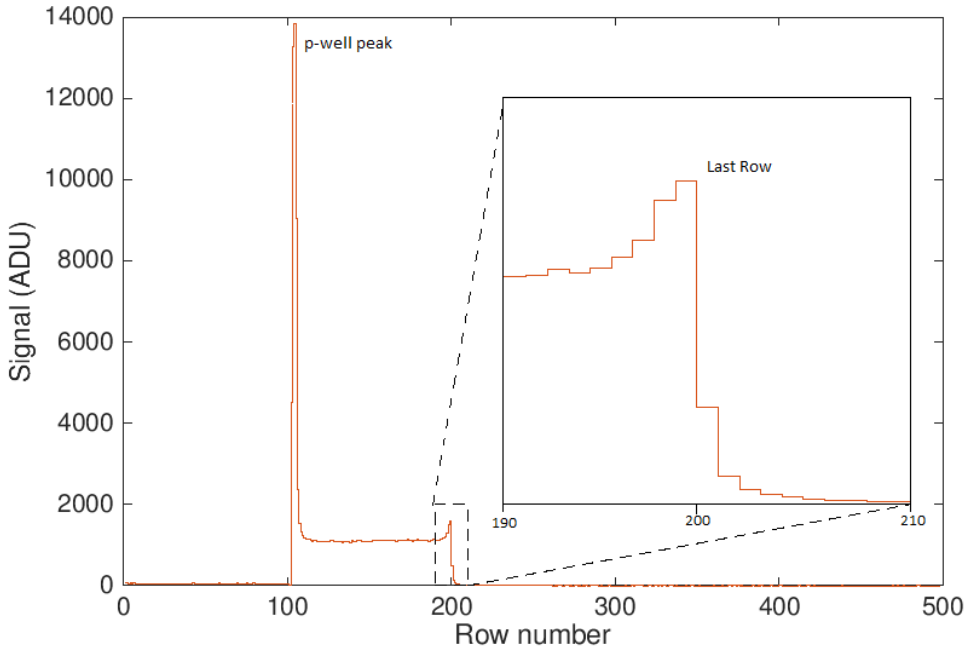

Figure 6.7: The charge in each pixel along column number 100. The enlarged region focuses on the last row of the image area and the overscan region. The tail represents the charge deferred in each subsequent pixel.

The CTI is calculated using

$$CTI_{EPER} = 1 - \frac{S_{def}}{S_{LC} N_{pt}} \tag{6.3}$$

here S_{def} is the sum of the deferred charge in the extended pixel region in electrons, S_{LC} is the signal in the last column in electrons, and N_{pt} is the number of pixel transfers within the CCD register. The last column appears as a peak as it can contain a larger quantity of charge than other columns or rows. This is attributed to the diffusion of charge from neutral regions outside of the array into the last column when flat-field illuminated.

The charge transfer inefficiency could then be measured when the device is operated without EM gain using the initial biases described in Table 5.1 at incremental input signal from 0 to beyond full well capacity.

6.5.1 Charge Transfer Efficiency as a Function of Clock Amplitude

As described previously, the CTI is dependent on several factors, including clocking speed and clock amplitude. This section looks at the effect of altering the clock amplitudes on the charge transfer inefficiency. It can be assumed that by optimising the biasing of each electrode and operating the device using the optimised voltages, the CTI should be reduced.

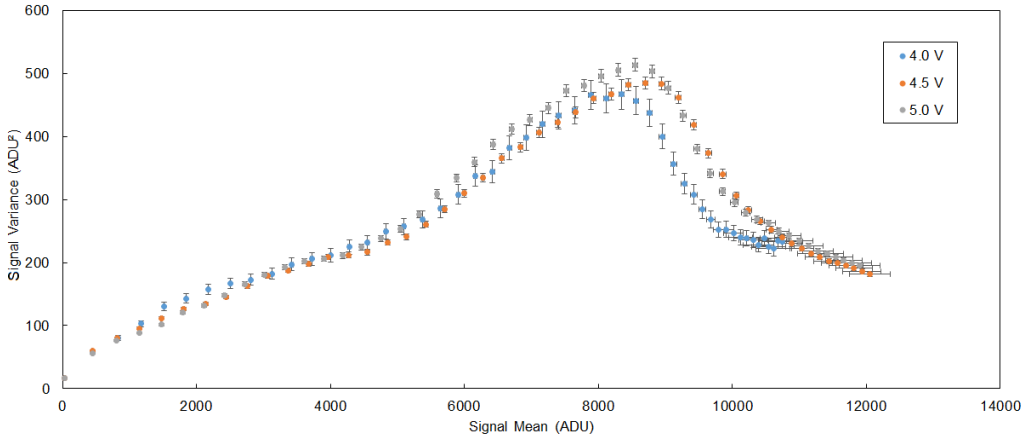

Figure 6.8: The mean-variance curves for EMTC1_B3 at 273 K for when the P1234 was clocked at several voltages. The remaining biases can be seen in Table 5.1.

The clock amplitude (P1234 setting) controls the voltages of the P1, P2, P3 and P4 gates, providing the same voltages to each gate. When the device is operated without EM gain, the P2HV bias and clocking voltages are kept at the same level. As such, when P2HV was biased at 4.0 V and P2DC gate was biased to 3.0 V, a sufficient potential difference formed for a high CTE but insufficient for impact ionisation to occur. It is possible to demonstrate the effect of altering the P1234 clocking voltage by looking at the photoelectric response. As shown in Figure 6.8, there is a small variation in the PTC shape and peak. Subsequently, the CTI was measured as a function of the input signal when the device was cooled to approximately 253 K.

The voltages were incremented in steps of 0.5 V from 0.5 V to 5.0 V. Figure 6.9 demonstrates the charge transfer efficiency as a function of the signal when the device was operated at 253 $\pm 0.5K$ when the voltages for bias electrodes

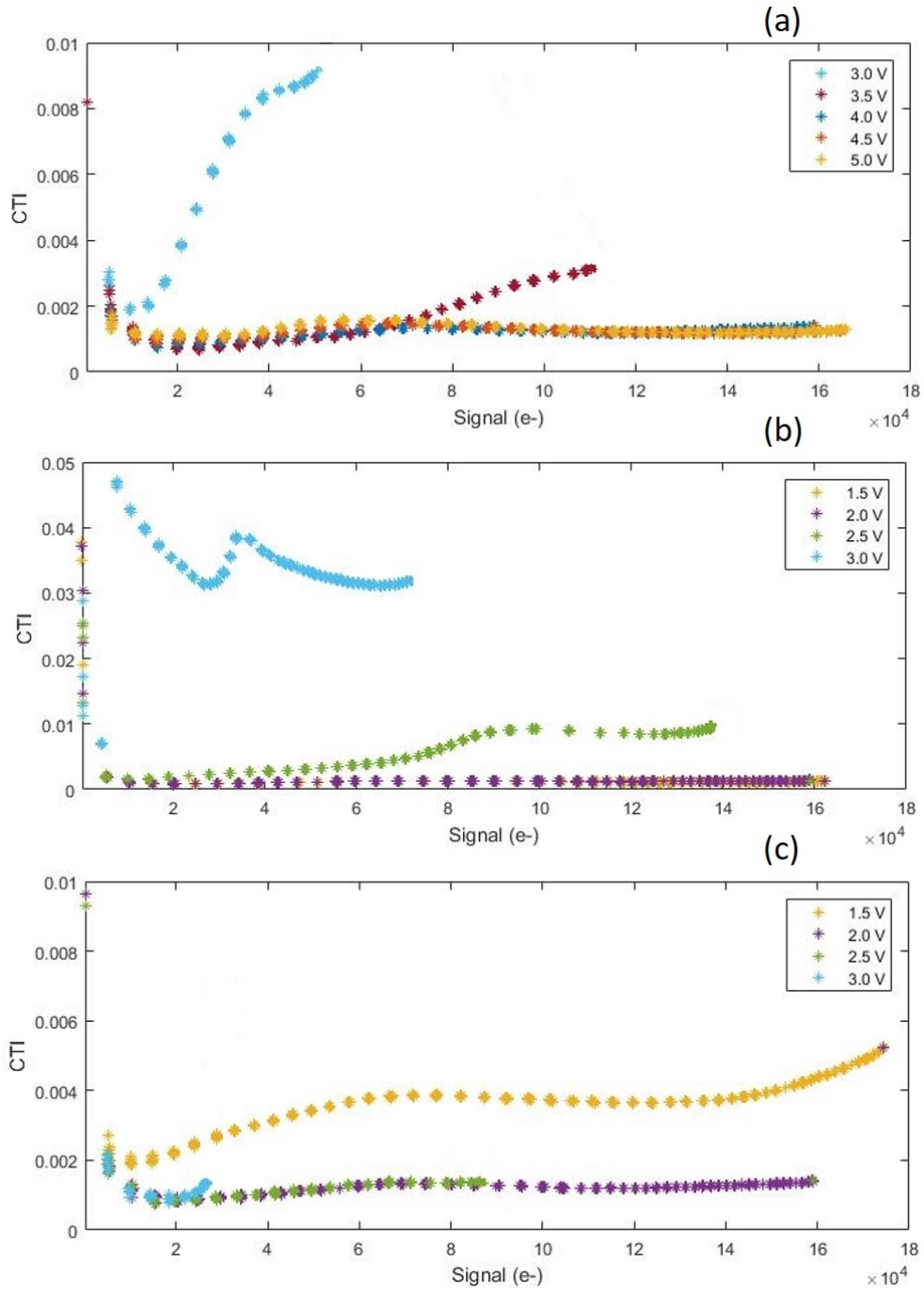

Figure 6.9: The CTI of Block 6 as a function of signal at 253 K. (a) varying P1234, (b) varying P2DC and (c) varying OG. The remaining biases were operated at the voltages described in Table 5.1 without EM gain.

clocking gate, output gate, and DC gate were increased incrementally from 0.5 to 5.0 V. This graph however only shows the curves for the voltages when an image was successfully produced. This graph focuses on Block 6 however, the graphs are largely uniform across the different regions of the device.

It is apparent that altering the bias voltage on each electrode has a direct effect on the charge transfer inefficiency in line with simulation results. When the biasing of the output gate is increased above 3.00 V, the CTI increases significantly above the CTI at 2.0 V, and a successful transfer is not completed. It is also apparent that low voltages, less than 1.50 V, results not only in a significantly higher than the optimum CTI but also results in the failure to read out an image. The potential difference between the gates too small, resulting in the charge not passing on to the sense node efficiency and the potential is insignificant for charge to be stored beneath the output gate.

6.5.1.1 EM Gain and Charge Transfer Inefficiency

When considering the dependence of the EM gain on the EM field, it is important to consider the CTI, as the size of the charge packet that has been transferred will be affected by the magnitude of the EM gain. When a device is operated with gain, it can become difficult to determine the functional CTI of an EMCCD. As such, it is important to operate an EMCCD without gain to calculate the effective CTI of a device. However, operating with a high voltage across P2HV gate results in the development of a high field that shifts the signal packet, as seen in Figure 6.5. This can cause the signal packet to interact with new trap sites. By operating with a small P2HV voltage, an electric field can be induced that is insufficient to cause significant impact ionisation. This results in the signal packet moving into other regions of the device and can directly affect the CTI. As described previously, the field strength is a function of the potential difference between the HV and DC gates. By altering the DC voltage, the electric field strength can be increased or decreased, moving the charge across different regions of the device. Blocks 7 and 8 experienced an increased gain when compared to rectangular gain gate structures due to the shape of the gate corralling charge to the areas of highest electric field and countering edge losses traditionally experienced by rectangular gate structures. Figure 6.10) plots the CTI as a function of the P2DC voltage for each region while the HV voltage remained constant at 8.0 V. As described earlier in this

thesis (see Figures 6.3 and 6.5) the electric field is higher closer to the gate resulting in a stronger electric field. This means that even at low field strengths, it is sufficiently close to the impact ionisation region for measurable gain to occur, even at a small potential difference. However, a low P2DC and P2HV voltage can cause insufficient movement of charge through the device resulting in charge lagging into subsequent charge packets. Subsequently, as the P2DC voltage is increased, the CTI decreases as sufficient charge is moved through the device. As expected, due to the lack of EM register, Blocks 1 and 2 the CTI remains constant, independent of the P2DC voltage.

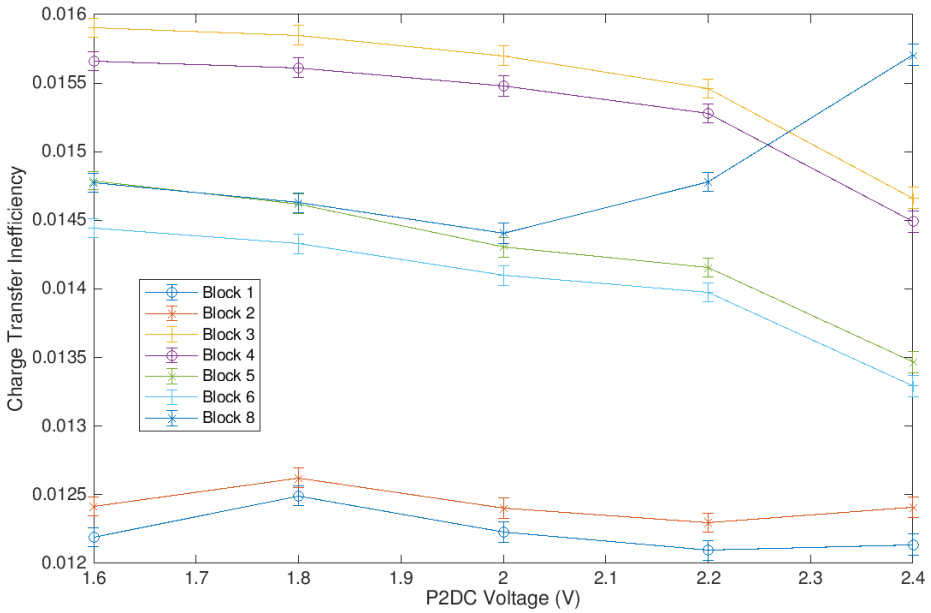

Figure 6.10: The CTI as a function of P2DC voltage while the potential difference between P2DC and P2HV remained constant at 8.0 V. The device was biased using the values in Table 5.1 and operated at 253 K with a signal of 1000 electrons.

In Figure 6.10 Block 7 is omitted as this region of the device experiences saturation due to the high gain achieved at these voltages and input signal. A similar process can be seen for Block 8, which sees considerably higher gain than the average gain of the rectangular gate structure. Block 8 experiences an increase in the CTI as the P2DC exceeds 2.0 V, implying that the charge packet is experiencing a higher number of trap sites as the charge packet moves

closer to the interface. It is possible that this increase in CTI is caused by hot carriers interacting with the interface leading to trapped charge. This is a process that is discussed in Chapter 8 as it directly correlates to ageing damage. Further analysis of the CTI at higher P2DC voltages would give additional insight into the location of the traps causing increases in the CTI. Subsequently, it is possible to state that increasing the voltages of the P2DC and P2HV while the potential difference remains constant results in a reduction of the CTI. Furthermore, changing the gate voltage moves the location of the impact region and increases the density of the electron cloud close to the impact region.

6.6 Conclusion

The chapter looks at the charge transfer in the EMTC1 with a focus on the effect of the HV gate on the transfer process. It is apparent that the length of the gate impacts the transfer of charge and subsequently, the EM gain. By increasing the length of the gate, the charge cloud and potential are altered in size and density. As the gate length increases the potential under it in the buried channel also increases, increasing the electric field. The location of the charge packet impacts both the charge transfer efficiency and the EM gain. This is expected to impact the ageing discussed in a subsequent chapter.

Chapter 7

Radiation Damage in the EMTC1

7.1 Introduction

When utilised in space, image sensors are exposed to an environment consisting of pervasive radiation. The radiation is composed of a mixture of particles with concentrations that can change by many orders of magnitude in a short time. For the successful operation of the device, it is necessary to have a complete understanding of the environment in which the device will operate. This chapter initially discusses the natural space radiation environment and radiation damage mechanisms, such as ionisation and displacement damage. This will be explored in relation to the effects experienced by CCDs in terms of physical damage and operation, and methods that have previously been employed to reduce radiation damage.
The second half of this chapter will focus on the proton irradiation effects on the operational characteristics of the EMTC1 to assess the potential applications in space.

7.2 Radiation Environment

The space radiation environment has a broad range of conditions. Even within the Earth orbits, the radiation environment differs significantly with location and time in terms of intensity, dominant particle types and their energies. In space, image sensors are subjected to irradiation by protons, electrons, heavy ions and gamma rays. These particle types interact with the silicon lattice and oxides and can cause bulk and ionisation damage.

The remainder of this section will focus on the following categories of radiation

- Trapped Radiation (around the Earth)
- Galactic Cosmic Rays (GCRs)
- Solar particle events

The first two sources are relatively constant or vary on time scales from a day to years. The third source is highly variable in response to solar events. These can be on a scale of minutes to several days.

7.2.1 Radiation Belts

The radiation belts that surround the Earth were first discovered in 1958 and named Van Allen belts after the man who confirmed their existence using Explorers 1 and 3 [127].
The Van Allen belts contain highly energetic charged particles trapped at high altitudes by the Earth's magnetic field. The inner belt typically extends from 1 to 3 Earth radii (R_{Earth}) [35]. It is largely stable, dominated by protons with a mean particle energy of 50 MeV. At the belt's maximum intensity, the belt contains several thousand protons/cm^2/s which have an energy exceeding 100 MeV. The flux of the protons can greatly exceed that of the electrons within this belt.

In comparison, the outer belt is much more dynamic, extending from 4 to 7 R_{Earth} [23] demonstrating variations in space and time due to the competing source and loss processes. These are driven by solar dynamics, and as such, this belt can be profoundly affected during periods of high solar activity.

The flux maximum occurs at approximately $4\mathrm{R}_{Earth}$ for electrons which have an energy greater than 1 MeV. The particles in the outer belt are subject to injection events during geomagnetic storms and the acceleration of particles from the magnetosphere tail. Furthermore, the electrons undergo periods of energisation and inward diffusion due to the disturbances in the magnetic field [21].

At the South Atlantic Anomaly (SAA) the Earth's inner Van Allen radiation belt dips closer to the surface of the Earth reaching an altitude of 200 km. Within this region, there is an increased flux of energetic protons. The shape and particle density of the SAA change daily, and it is drifting at a rate estimated to be $0.28 \pm 0.03^{\circ}$ west and $0.08 \pm 0.03^{\circ}$ north each year [3].

7.2.2 Galactic Radiation

Galactic Cosmic Rays (GCR) originate outside of the solar system and primarily consists of protons and energetic nuclei. The rays are characterised by an omnidirectional flux and composition of $\sim 85\%$ protons, $\sim 14\%$ alpha particles and $\sim 1\%$ heavy ions [32]. When considering effects on spacecraft the particles with energies in the range 10^6 eV to 10^9 eV are of the most concern. Furthermore, some GCRs have very low flux but energies that exceed 10^{12} eV. At these high energies, spacecraft shielding becomes ineffective, and GCRs can produce Single Event Upsets (SEU) damaging electronic memory and logic components.

7.2.3 Solar Radiation

Solar flares and Coronal Mass Ejections (CMEs) are eruptive solar events due to magneto-hydrodynamic instabilities. These events correlate to the sunspot cycle, which lasts 11 years. After approximately the initial two years, sunspot activity rises to a maximum; a year is spent at maximum before a four-year decline to a minimum which usually lasts a further four years.
CMEs are most likely to occur two years pre and post the solar maximum. Solar flare particles can be of very high energy and have been known to trigger single event upsets in electronics and some electronic failures on Earth [72, 94]. The protons, electrons and high-energy nuclei have an energy that ranges from several keV to many MeV.

7.2.4 Shielding

It is important to note that some protection can be provided to instrumentation. This can take two forms: the Earth's magnetic field and physical shielding protecting sensors.
Physical shielding can be utilised to limit damage to onboard sensors. Most onboard instrumentation is offered a level of innate shielding due to the structure of the spacecraft. However, the effective mass can be limited by the requirement to minimise spacecraft mass. It is also possible for secondary charge particles to be generated due to spacecraft and instrument shielding. The secondaries have been known to cause high levels of low energy photons and can lead to damage to onboard sensors. The secondary particles can provide a large contribution to the total dose of a mission. Studies have demonstrated that materials with a low Z provide shielding that can dramatically reduce the number of secondary particles [5, 87]. No shielding can eliminate the damage to radiation-sensitive components, so the focus of limiting radiation damage is to reduce the dose to a reasonable level. It is possible to achieve an understanding of the effect of the shielding using computer models, which allow for the calculation of the dose.

7.3 Radiation Damage in Image Sensors

Exposing a semiconductor to high energy radiation, such as electrons, protons and gamma rays, allows energy levels to be introduced into the band gap. An atom within the silicon lattice can be knocked out of place by a high-energy particle producing an interstitial atom and vacancy. Complex lattice deformations rapidly form with energy levels within the band gap. These can act as acceptors, donors or recombination centres. It is possible for these centres to anneal over time at both low [39] and high temperatures [20].

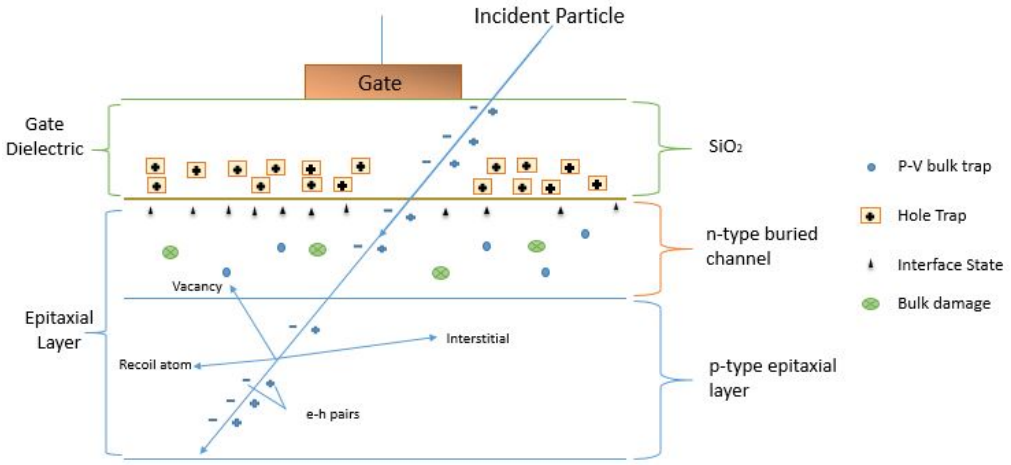

Figure 7.1: The gate dielectric and epitaxial layer in CCD in which different types of radiation damage can occur producing different types of traps.

Extensive research has been conducted into the effect of radiation on silicon devices. The two main mechanisms of damage are ionisation and displacement, details pertaining to the damage induced by these mechanisms can be found in Table 7.1. The radiation damage mechanism and the location of the damage induced are detailed in Figure 7.1. This image is based on an n-type buried channel CCD.

Damage Mechanism	Location	Damage
Ionisation	SiO_2	Flat band voltage shift
Ionisation	Si-SiO_2 interface	Traps generated at surface, increasing flatband voltage shift and surface generated dark current
Ionisation	Region of charge generation and collection	Transient effects
Displacement	Charge generation, collection and transfer site in silicon	Increased CTI, increased dark current, dark current non-uniformity, an increased number of hot pixels and RTS

Table 7.1: Radiation damage mechanisms and location of interaction resulting in damage in silicon image sensors.

7.3.1 Ionisation Damage

Ionising damage is primarily caused by charged particles, x-rays and γ-rays resulting in a charge build-up at the gate electrode and interface states. Electron-hole pairs are generated within the gate dielectric between the electrodes and the underlying silicon. When a gate is positively biased, the highly mobile electrons pass through the gate. The less mobile holes become trapped close to the Si-SiO_2 interface. When operated under negative bias, the electrons move towards the silicon and are lost from the system. The holes become trapped at the gate-interface. It is common for CCD manufacturers to utilise a layer of silicon nitride on top of the oxide to aid in the manufacturing process. The electron and hole mobilities are reduced, and the charge is more likely to recombine in the nitride layer.

Surface or interface traps occur due to the lattice mismatch between silicon and silicon oxide resulting in unpaired bonds called 'dangling bonds'. These bonds have lower binding energies when compared to that of the lattice. These locations act as traps with energy levels that span the band-gap. During normal operation, the silicon surface is depleted, and these traps generate dark current. Passivation, in the form of annealing in a hydrogen-rich environment at $\sim 400°C$, completed during device manufacturing, is known to reduce the surface dark current considerably. The hydrogen dissociates and bonds to the dangling bonds. Ionising radiation breaks these bonds, reversing the passivation process producing a surface with a higher density of states than

pre-passivation.

7.3.2 Displacement Damage

When a high energy particle or a photon is incident on a silicon lattice displacement damage can be induced. Initially, vacancies (absence of atoms) and interstitials (movement of a displaced atom to a non-lattice position) are created. When these combine, a Frenkel pair is formed shown in Figure 7.2. Two adjacent vacancies form a defect described as a divacancy. It is also possible for larger defect clusters to form. The primary displaced atom can dislodge numerous atoms locally creating a disordered region. Within this region, the defect density is much higher than that of the other areas of the device. Incident particles can produce a mixture of clustered and isolated defects.
It is possible for these defects to reorder, forming more stable configurations such as divacancies and vacancy-impurity complexes. This process is described as annealing and is temperature dependent. Annealing occurs in several stages: short term thermal annealing that happens in seconds and minutes directly following the initial defect creation and long term annealing that occurs over the following years. The stable combinations form in the presence of oxygen or phosphorus atoms [11] producing electron or hole traps. The lattice defects create energy levels within the silicon band-gap. The energy levels (activation energy) can be used to characterise the trap type; the O-V or A-centre has an energy level of E_c-0.17 eV while the P-V or E-centre has an energy level of E_c-0.44 eV. These energy levels cause the following processes:

- **Generation:** e-h pairs are generated thermally at a mid-gap energy level resulting in an increase in the dark current within the depletion region.
- **Recombination:** A trap can capture a hole or electron resulting in a reduction in the minority carrier lifetime. The rate of recombination is dependent on the free carrier concentration and electron-hole capture cross-section.

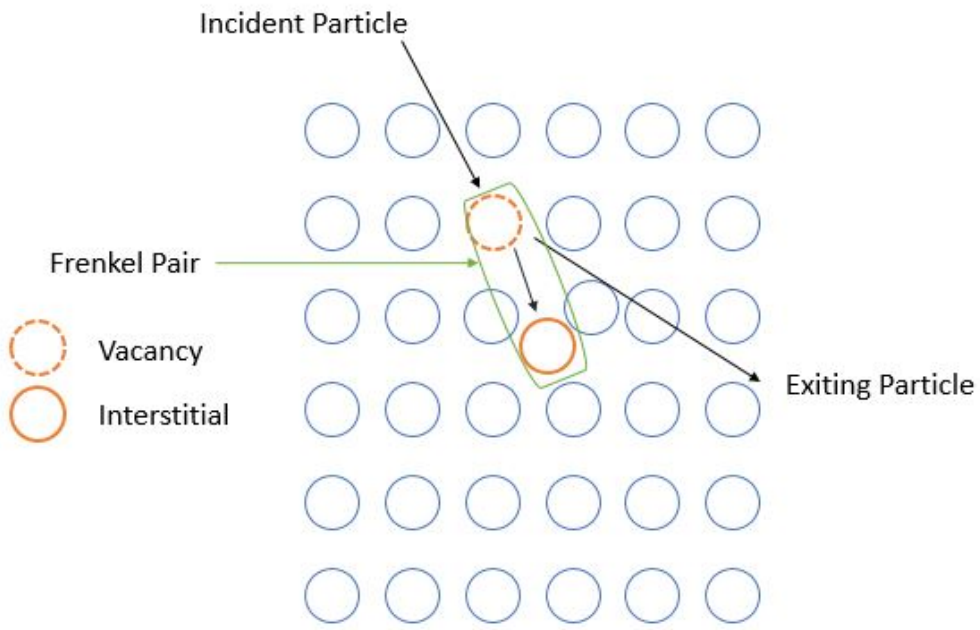

Figure 7.2: Displacement damage within silicon lattice structure producing Frenkel pair.

- **Trapping:** A shallow trap captures a charge carrier. If recombination does not occur, the free carrier is released after a time dependent on the type of the defect centre. This process can result in an increase in CTI.
- **Tunnelling:** Carriers can tunnel through the potential barrier from the valence band to the conduction with the assistance of the defect. This process results in an increase in the device current.
- **Compensation:** Defect centres compensate donors or acceptors, resulting in a reduction in the majority carrier concentration.
- **Scattering:** Defects can act as scattering centres, which can lead to a reduction in the carrier mobility at increased trap concentration. Below 300 K this effect is dominant over lattice scattering [104].

Not all displaced atoms will remain an interstitial [78] if the interstitial has an energy less than the lattice binding energy after the interaction. For silicon, this value is 2.3 eV. Any energy less than this will result in the silicon interstitial annealing.

7.4 Experimental Procedure

7.4.1 Pre-irradiation testing

The cosmetic quality and functionality of several devices were tested in the temperature range between 243 K to 303 K using an integration period of 100 ms. Two devices were selected, one to be irradiated, and one kept as a control. The EMTC1 was irradiated unbiased due to experimental setup restrictions at the Proton Irradiation Facility (PIF) [86]. EMTC1_B2 was selected to be irradiated due to the uniformity of dark current and hot pixel density. This device was selected as it was representative of the devices and lacked manufacturing defects. The devices were characterised by the noise, dark current and EM gain to enable comparison post irradiation.

7.4.2 Proton Irradiation of the EMTC1

Irradiation of the EMTC1 was undertaken at PIF at the Paul Scherrer Institut (PSI) in Switzerland. PIF can recreate realistic proton spectra encountered at any orbit in space. PIF delivers an initial proton beam from the PROSCAN accelerator employing a primary energy degrader, reducing the initial beam from 230 MeV to 74 MeV [86].

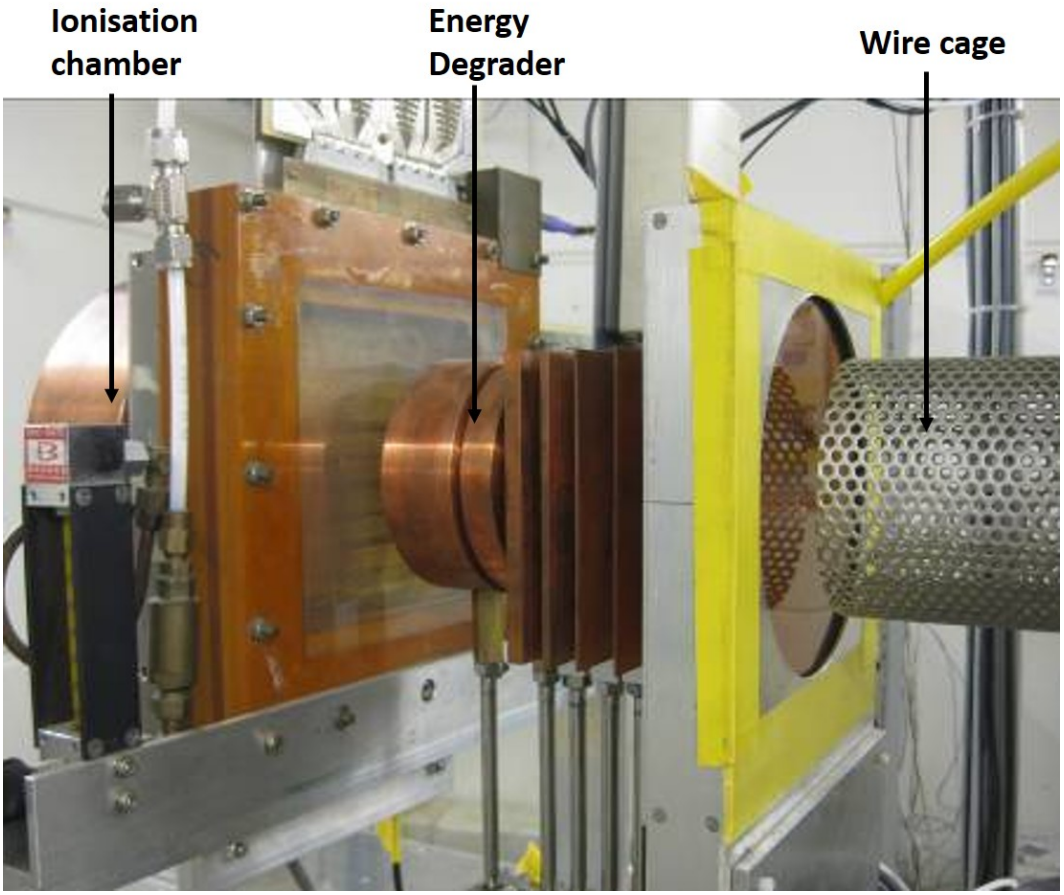

Figure 7.3: The ionisation chamber within the PIF setup container, the energy degrader and the wire chamber [86].

By reducing the energy of the beam, the beam intensity is reduced on the target. As demonstrated in Figure 7.3, the experimental setup consists of a localised energy degrader, beam collimator, wire chamber and monitor devices. The test device can then be mounted onto a movable XY table with a sample holder, as seen in Figures 7.3 and 7.4.

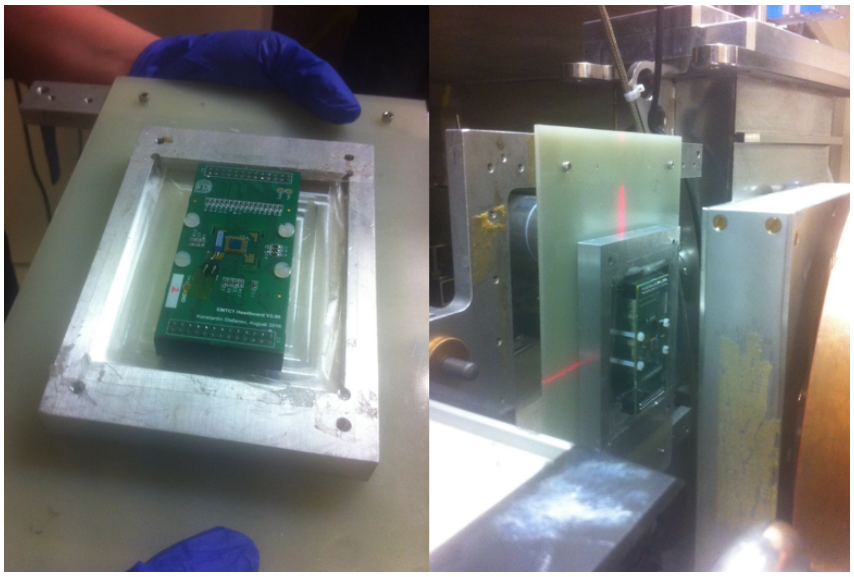

Figure 7.4: The EMTC1 was securely attached to the mounting plane. The board was then mounted onto the face of the irradiation plate aligned with the proton beam.

EMTC1_B2 was irradiated on 12^{th} February 2017 at ambient temperature while the device was grounded. The dosimetry had an accuracy better than 10%. PIF provided 10 MeV protons utilising a 74.3 MeV beam which was degraded using 0.4 mm aluminium and 7.5 mm copper blocks. The beam flux was approximately $2 \times 10^7\ cm^{-2}s^{-1}$.

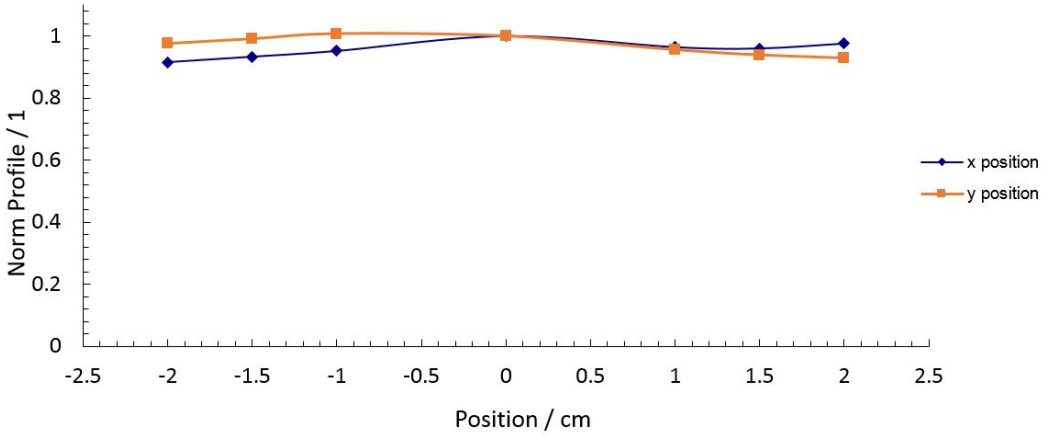

Figure 7.5: The beam intensity profile as measured by PSI staff immediately prior to irradiation.

The orientation of the beam profile in the horizontal (x) and vertical (y) direction during setup prior to the irradiations is shown in Figure 7.5 and show uniformity better than 10%. Due to NIEL (non-ionising energy loss) scaling it is possible for any particle fluence to be reduced to an equivalent 1 MeV neutron fluence which would produce the same amount of bulk damage in a specific semiconductor [129, 59]. It is often useful to talk about total proton fluence values in terms of equivalent 10 MeV fluence to enable the comparison of irradiation experiments when irradiated at different proton energies. This scaling is based on the assumption that bulk damage generation is caused by non-ionising energy transfers to the lattice, enabling them to be compared. NIEL scaling has been described in detail for silicon device by Burke (1986) [10], Van Lint (1987) [130] and specifically for CCDs by Srour et al. (2003) [104].

EMTC1_B2 was irradiated for 1920±10 seconds at the 10 MeV equivalent fluence, $1.038 \times 10^{10}\ p/cm^2$. In comparison the end of life of the JUICE mission is $2.077 \times 10^{10}\ p/cm^2$ [102] and the Hubble telescope experiences a 10 MeV equivalent fluence of $1 \times 10^{10}\ p/cm^2$ per year [99]. The non-uniformity of the radiation was insignificant due to the small size of the EMTC1, compared to the size of the beam. The device was then irradiated for a total run time

of 525 seconds. The device was irradiated in ambient air, and the temperature prior and post irradiation was 298 K however, the temperature during irradiation was not measured.

7.4.3 Post-Irradiation Characterisation

The same measurements completed prior to the irradiation were then repeated. During the retesting of the device, it was discovered that EMTC1_B1 had suffered a failure. Block 7 had experienced a catastrophic failure likely due to a broken connection in transit. This resulted in a significantly reduced signal that had considerable noise. As such testing on this device post-irradiation was limited, and a full comparison between the devices could not be completed.

7.5 Performance Degradation

When a dark image was taken several days after the irradiation a significant increase in the dark signal, CTI and noise of the device were observed (see Figure 7.6). It is of interest to note that while the dark current and CTI increased, the increase was largely independent of the individual pixel structures. Furthermore, the EM gain also experienced a change post irradiation.

7.5.1 Dark Current

Prior to the irradiation, the dark current was calculated by measuring the gradient of the sensor output against the integration time. This was completed for both the irradiated and control devices, and the average dark current was found to be 3.12 nA/cm^2. This was a slightly higher than the average dark current of several other devices which was found to be 1.49 nA/cm^2 averaged across the two commercial devices noted in the bottom of Table 7.2.

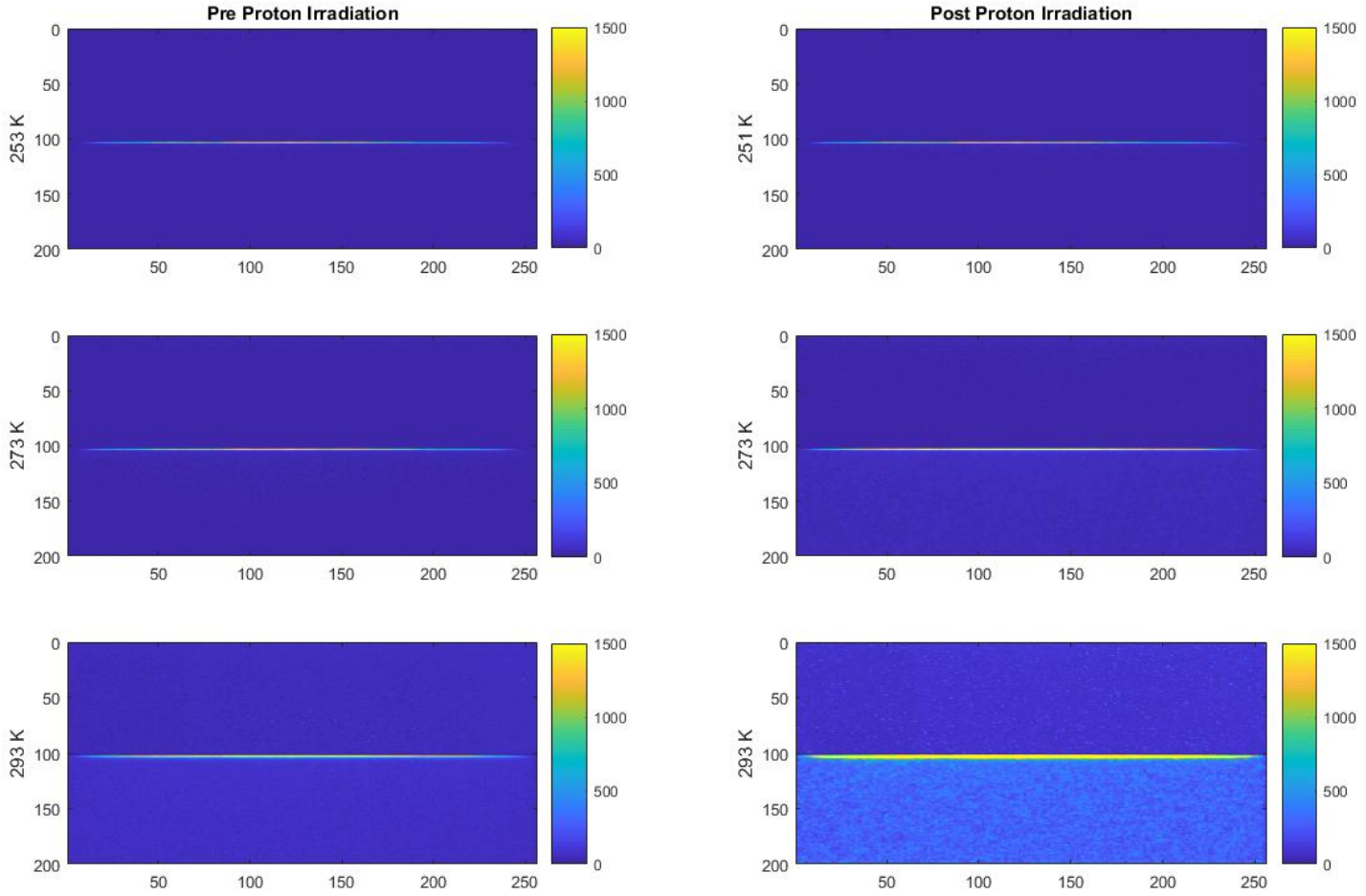

Figure 7.6: Dark signal image frames at 100 ms integration time pre and post proton irradiation at temperatures ≃253 K, ≃273 K and 293 K. Post proton irradiation an increase in dark signal at ≃293 K.

Device	Dark Current (nA/cm^2)	After Irradiation (nA/cm^2)
EMTC1_B1	1.46	1.39
EMTC1_B2	3.13	4.64
CCD97-00	2.5	-
CCD30-11	1.18	-

Table 7.2: Average Dark Current of several image sensors representative of the design prior to exposure to proton irradiation when operated at 293 K. All of the EMTC1 devices in this table demonstrate a representative range for the devices available for testing.

Table 7.2 lists the dark current averaged over multiple dark frames when the selected devices were operated at room temperature without EM gain. The table compares the results of two modern EMCCDs with the EMTC1 chips that were representative of the EMTC1. In addition, this table demonstrates the dark current after EMTC1$_C$3 had been irradiated. Both EMTC1$_C$3 and EMTC1$_C$1 (the control) were retested five days after the initial irradiation.

After the proton irradiation, the device was left to 'cool' for a week before characterisation. Results demonstrated that the dark current had increased by an average of 108% for all regions of the device. Dark current histograms for each block at a 10 MeV equivalent proton fluence of 4.15×10^{10} proton/cm^2 are shown in Figure 7.7. [1]

[1] A comparison of the mean dark current for each region of the device can be found in Table 7.3

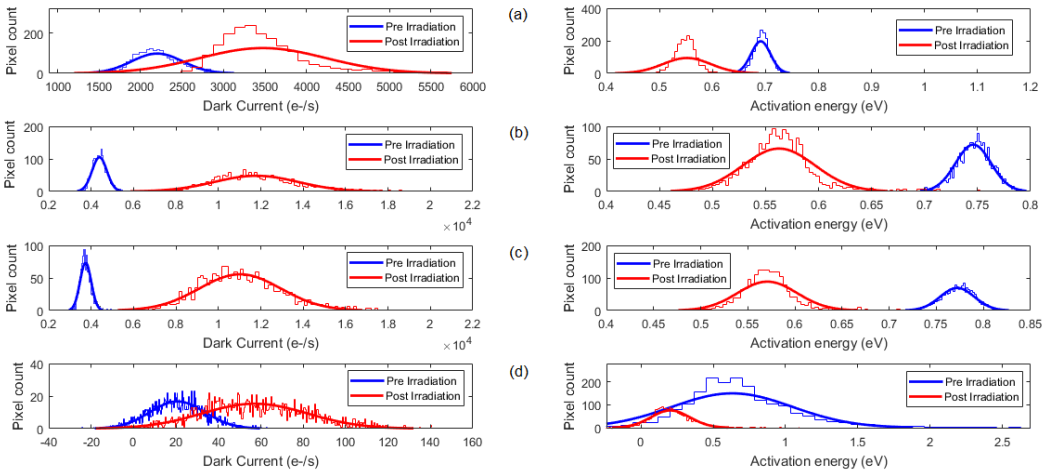

Figure 7.7: The dark current and activation energy pre and post proton irradiation with Gaussian fits (a) Block 2, (b) Block 5, (c) Block 6 and (d) Block 8.

It is important to compare the new technology with non-inverted mode CCDs. Initially, the EMTC1 was compared to a CCD 47-20 Advanced Inverted Mode (AIMO) device which had been irradiated to 10 MeV equivalent fluence of 5×10^9 protons/cm^2. A CCD47 operated in AIMO has experienced a considerably lower dark current than devices run in Non-inverted Mode (NIMO). The dark current pre irradiation was measured to be 17 e/s/p increasing to 130 e/s/p after irradiation. Dark current uniformity decreased slightly after the irradiation. The initial Dark Signal Non-Uniformity (DSNU) pre irradiation was measured to be 1.22%, rising to 3.4% post irradiation for the image area. This can be attributed to the increase in the number of bright pixels.

7.5.1.1 Bright Pixels

A bright pixel can be defined as a non-uniformity of the dark current spatial distribution, resulting in certain pixels having a dark current far greater than the mean dark current. They are often called hot pixels. Bright pixels can occur during the manufacturing process and as a result of high electric fields

in the device; however, the number of hot pixels can be increased by damage caused by incident radiation. The energy levels near the midgap are mostly responsible for the increase in the dark current. Protons with the same initial energy may result in considerably different amounts of displacement damage dependent on the initial collision cascade. In addition, if these defects occur in a region of high electric field, it is possible for high dark current to appear as a result of field-enhanced emission [100]. As the proton induced damage increases, the mean dark current (peak of the histogram) and the hot pixel population (histogram tail) also increases. As shown in Figure 7.7, the dark current increases after irradiation and can be attributed to the increase in dark current generation rates for a number of pixels. This increase in the dark current is linked to ionisation damage caused by the depassivation of surface states and bulk defects. Furthermore, the tail of the histogram rises significantly and lengthens considerably, indicating a large increase in the number of hot pixels. This increase can be linked to displacement damage events that have led to the overall increase in dark current. In this thesis, a hot pixel has been defined by two measures:

- a pixel with a dark signal with 3 times the standard deviation (3σ) of the region of interest.
- a pixel with a dark signal with 5 times the standard deviation (5σ) of the region of interest.

This differentiation was made to determine the pixels with the most dramatic increase in dark signal after irradiation and determine if these very high pixels were newly formed during the irradiation or were pre-existing and experienced an overall increase in the dark current. Populations were tracked to identify whether a hot pixel encountered at any step in the process was a new hot pixel or an existing one.

Figure 7.8 plots the number of hot pixels which have a signal 3σ greater than the average signal as a function of the pixel signal. There are a number of hot pixels measured prior to the irradiation. The average magnitude of the hot pixel prior to the irradiation was 407.8 $\pm$ 0.94 electrons with a spread of 27 rising to 912.0 $\pm$ 2.44 electrons with a spread of 78.20 after the proton irradiation. This increase in the number of hot pixels indicates that

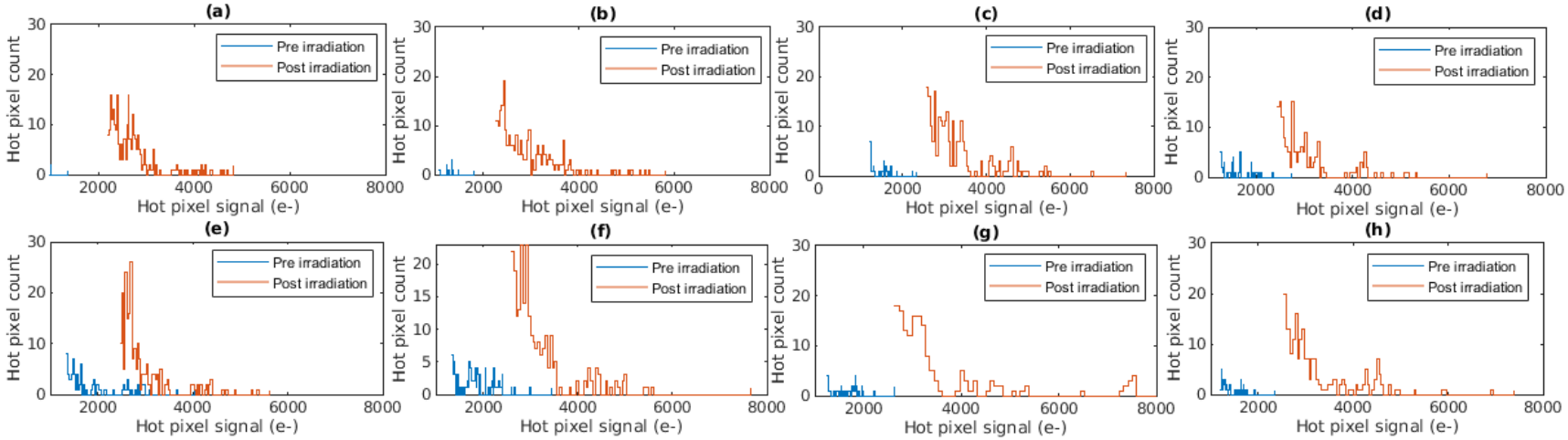

Figure 7.8: Histograms for each block of the image area of the hot pixel count which exceed the average signal by 3σ as a function of the signal of the hot pixel. The device was operated with an integration period of 100 ms at a temperature of 273. Each figure. (a) Block 1, (b) Block 2, (c) Block 3, (d) Block 4, (e) Block 5 (f) Block 6, (g) Block 7 and (h) Block 8.

new hot pixels form due to the irradiation. In addition, the total number of hot pixels within the image area rose from 821 to 1026. In addition to these new hot pixels, there were changes to the original hot pixels measured prior to irradiation. After irradiation, only 12% of the original hot pixels were measured again after irradiation. These pixels saw an average increase of 53.95 % comparable to the total average increase in signal of all hot pixels of 55.29 %. All radiation types lead to an increase in the average dark current. Subsequently, a hot pixel prior to being irradiated may look less and less like a hot pixel. This process then masks a proportion of the hot pixels that existed prior to exposure to radiation damage.

These results could then be compared to the hot pixels with a signal greater than 5σ. This hot pixel population saw a reduction in the total number of pixels with no new hot pixels formed when tested at 273 K. Once again the original signal of these pixels fell beneath the average signal after irradiation. The hot pixels that remained saw an increase of 78.5 % from 261.2 $\pm$4.4 to 1212.3 $\pm$21.9 electrons. The average activation after irradiation was 0.57 eV however some hot pixels show a much stronger reduction in their activation energy (see Fig.7.7 (b)). It is these spikes that are likely caused by defects in or near the Si-SiO_2 interface in areas of high field.

7.5.2 EM Gain

To determine the effect of the proton irradiation on the EM gain of the EMTC1, a set of 100 flat field illuminated frames were taken with an initial input signal of 300 electrons 253 K. The frames were repeated at increasing P2HV voltages. The EM gain pre and post irradiation in shown Figure 7.9 for four regions of the device. The errors calculated in this figure were calculated from the combined error of the standard deviation of the region of interest and multiple image frames captured under the same conditions. The increased errors at seen at high EM gains can be attributed to the non-uniformity experienced by the device at high EM gains.

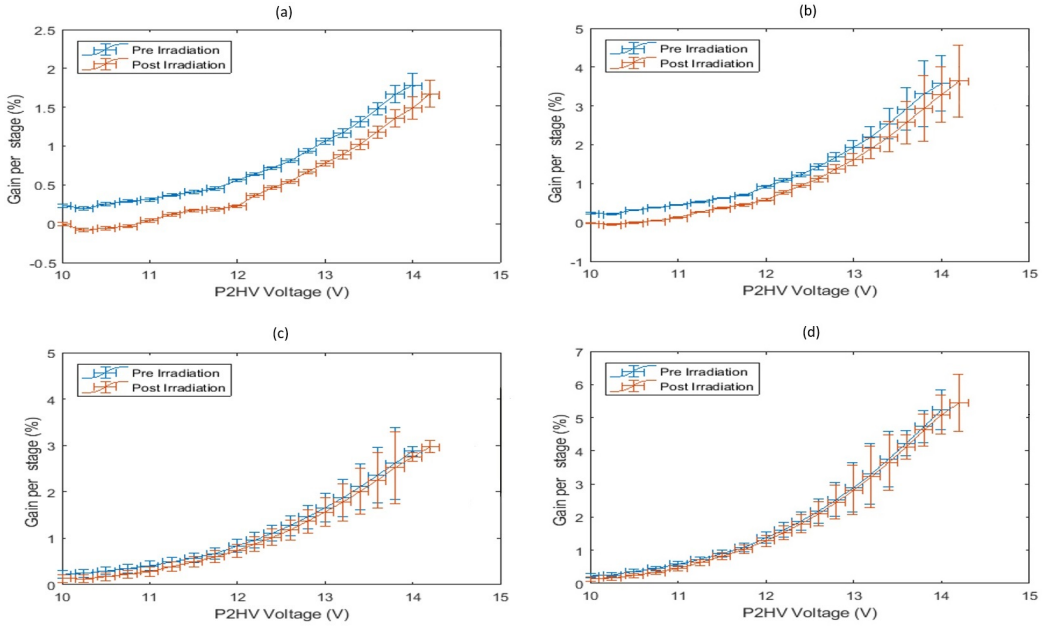

Figure 7.9: The EM gain per stage pre and post irradiation as a function of P2HV voltages at 253 K. (a)Block 5 (b) Block 6(c) Block 7(d) Block 8. The errors calculated in this figure were calculated from the combined error of the standard deviation of the region of interest and multiple image frames captured under the same conditions.

The shape of the post-irradiation EM curve is comparable to the device pre-irradiation, indicating that the gain structure and process have not been significantly affected by the proton irradiation. However, all regions shown demonstrate a constant off-set. As discussed in the subsequent chapter, the ageing process decreases the voltage at each P2HV voltage. While the loss in EM can be recovered to a certain extent by increasing EM register clock voltage, this is only possible to a certain point. It could be assumed that this decrease is due to ageing after repeated device characterisation. However, blocks 7 and 8 experience minimal variation in the EM gain after irradiation. As discussed later in the thesis, due to their high initial gain and structure blocks 7 and 8 experience the greatest decrease in gain. Subsequently, it can be assumed that any gain reduction would be most significant for blocks 7 and 8. Instead, it is blocks 5 and 6 that see a reduction in the gain. Due to the localised effect on the EM regions on the sensor, this change in the EM gain could be attributed to the formation of radiation induced positive charge. It is possible that that proton damage in the region of the high electric field between the DC and HV gates could produce a damage site leading to charge injection when exposed to the high field. Hot carriers could migrate under the influence of the electric field and trap in the interface in a process similar to ageing. However, there is no known injection site as it is likely that it could only be observed within the gain register. However, as noted previously, there was an expected increase in the dark current and hot pixel population due to the proton induced damage. This results in register saturation being reached at a lower level of gain. Figure 7.10 demonstrates the EM gain per stage as a function of temperature for Block 5. A reduction in the gain is noted after irradiation, including a non-linear decrease at high temperatures. When the gain measurements were taken at a higher temperature, the EM gain reduces due to the device reaching register saturation at a lower gain. At lower temperatures the Figure 7.10 after irradiation shows the same shape but shifted to a lower gain due to the same offset seen in Figure 7.9.

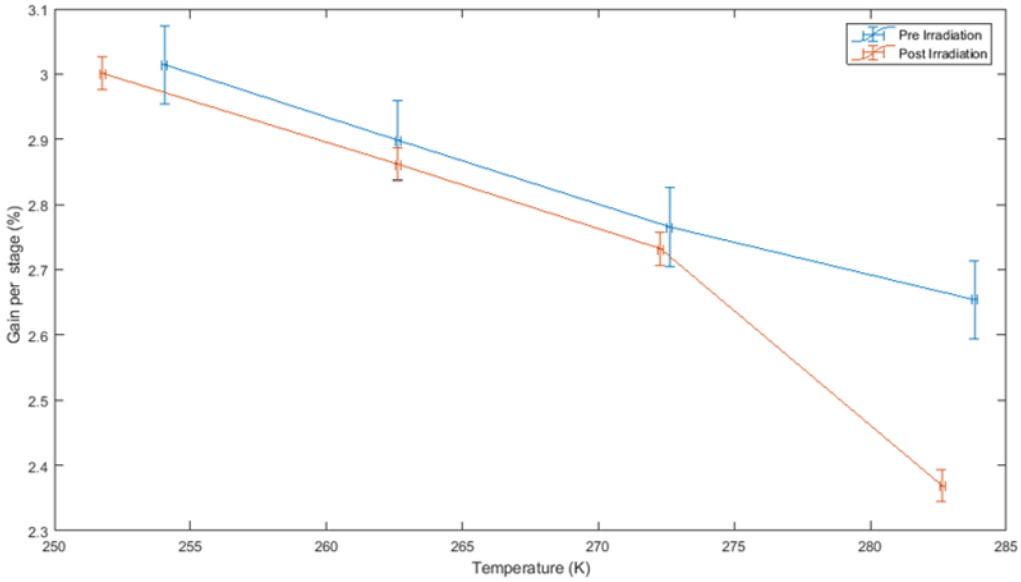

Figure 7.10: The EM gain per stage as a function of temperature for Block 5 with a signal of 1000 electrons.

7.6 Room Temperature Anneal

The traps that form are often not permanent and can anneal with time. Research has demonstrated that it is possible to anneal thermally. For annealing to be successful, it is important that the trap energies are understood to ensure that the correct temperature is used to anneal the trap. Annealing can, in turn, provide insight into the nature of the traps.

7.6.1 Dark Current and Activation Energy Post Anneal

Dark current measurements were repeated after a 10-month room temperature anneal. These were completed under the same conditions that were utilised for the pre and post irradiation results. It is possible to measure the increase in trap concentration induced by irradiation in charge coupled devices, even at low trap concentrations. This is due to the discrete nature of the distribution of the radiation-induced traps within each pixel [77]. Using Dark Current

Spectroscopy, it is possible to observe the traps on a pixel level directly; subsequently, the correlations between the dark current peaks and defects can be understood. However, no distinct quantisation of the dark current was noted in any of the regions at this proton energy.

Charge pumping could also provide more insight into the nature of these traps [43]. However, due to time and setup restrictions this thesis has analysed the nature of the traps by calculating the activation energy. The activation energy here describes the energy required to overcome the potential energy of the trap. The activation energy is a characteristic of each trap and can be used to determine the dominant type of trap within the device. It is possible to determine the activation energy of these traps from the temperature dependence and Arrhenius equation [133]

$$DC = DC_0 exp\left[\frac{\Delta AE}{kT}\right] \tag{7.1}$$

where DC is the dark current, DC_0 is a pre-exponential factor, AE is the activation energy, k is the Boltzmann constant, and T is constant. According to the Arrhenius plot, plotting the logarithm of the dark current versus the inverse temperature produces a straight-line plot. Subsequently, the activation energy is the absolute value of the gradient. It should be noted that studies completed by Widenhorm et al. (2002) [133] determined that analysing dark current via the Arrhenius plot leads to spread in the activation energy which is predicted by the Meyer-Neldel rule (MNR). This method for calculating the activation energy was used throughout this thesis.

Retesting the device after the anneal demonstrated a decrease in the dark current and an increase in the activation energy seen in Figures 7.11 and 7.12. Table 7.3 presents the average dark current for each region of interest when the device was operated at 293 K. It is apparent from the table that there was a largely uniform increase in the dark current barring Block 7 which saw a larger increase in dark current than the other regions of the device. After irradiation, block 7 on both the irradiated and control devices experienced anomalous increases in the dark current and CTI. As the control also experienced the damage, it can be assumed that the damage was caused by a mechanical fault that occurred during transport. After irradiation, there was an average percentage increase of 76.9%. After the anneal, there was an

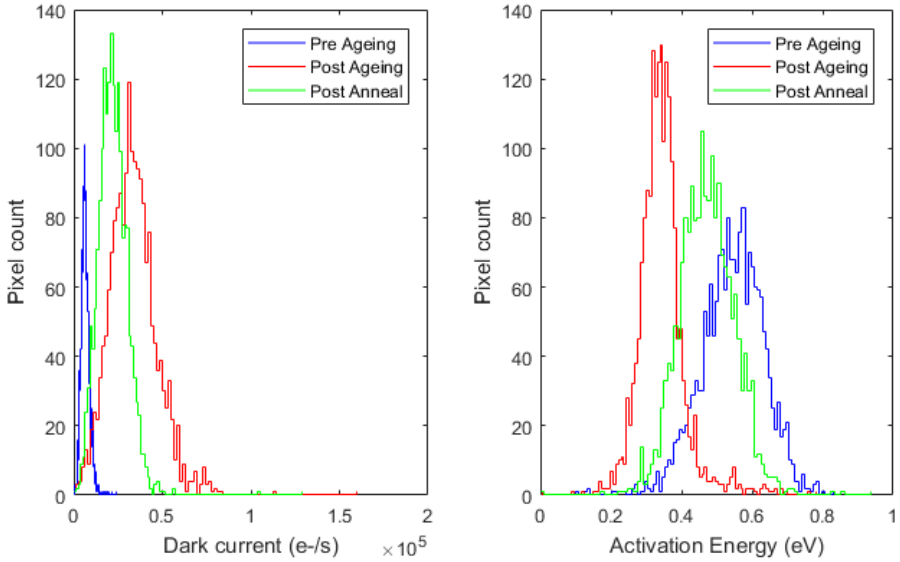

Figure 7.11: (a) Histogram comparing the dark current pre and post irradiation and post anneal at 253 K for Block 6 ;(b) Activation energy for the same block.

average reduction of the dark current of 7.97%. This decrease in the dark current can be attributed to the anneal of hot pixels with set trap energies. Further study into the activation energy would provide a greater understanding of the traps that lead to the increase in dark current, number of hot pixels and subsequent annealing of the pixels.

With the largely uniform increase in dark current, it is sufficient in this chapter to state that traps form post irradiation, with an energy of E_c 0.36 eV annealing to 0.45 eV. This was largely uniform across the device and can be attributed to traps forming in the bulk region of the device.

Block	Pre DC (e-/s/p)	Post DC (e-/s/p)	Anneal DC (e-/s/p)
1	$1.33\times10^4 \pm 39.5$	$2.27\times10^4 \pm 139.9$	$1.94\times10^4 \pm 75.1$
2	$1.21\times10^4 \pm 42.30$	$2.09\times10^4 \pm 102.6$	$1.78\times10^4 \pm 65.6$
3	$1.22\times10^4 \pm 60.79$	$2.09\times10^4 \pm 93.9$	$1.76\times10^4 \pm 68.9$
4	$3.64\times10^4 \pm 108.2$	$6\ .80\times10^4 \pm 113.8$	$7.01\times10^4 \pm 192.7$
5	$1.75\times10^4 \pm 30.93$	$3.01\times10^4 \pm 262.1$	$6.85\times10^4 \pm 116.8$
6	$1.69\times10^4 \pm 24.83$	$3.70\times10^4 \pm 241.7$	$6.67\times10^4 \pm 105.8$
7	$4.52\times10^4 \pm 168.92$	$1.96\times10^4 \pm 703.7$	$1.91\times10^4 \pm 695.4$
8	$8.10\times10^3 \pm 184.75$	$1.32\times10^4 \pm 643.2$	$1.11\times10^4 \pm 432.1$

Table 7.3: The average dark current (DC) for each region of the device when operated at 293 K before and after the proton irradiation and after the 10 month anneal. The errors were calculated from the standard deviation of the region of interest and multiple image frames.

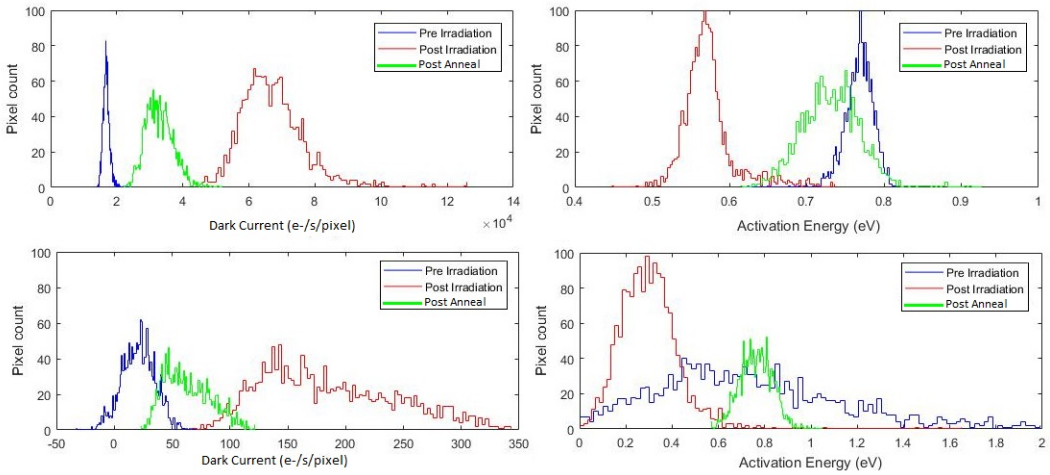

Figure 7.12: Histograms comparing the pre and post irradiation and post anneal for the dark current and activation energy at 253 K. (Top) The dark current and activation energy for Block 7 and (Bottom) The dark current and activation energy for Block 8.

7.6.1.1 Charge Transfer Inefficiency

The Charge Transfer Inefficiency (CTI) post anneal was compared with the results pre and post-irradiation. As stated previously the CTI of the EMTC1 was higher than average, typical CTI for a conventional CCD is of the magnitude $\times 10^{-}6$ [38]. The device was flat-field illuminated with an LED for incremental time periods at a series of temperatures. Figure 7.13 compares the CTI for Block 6. The data is fitted with an exponential fit.

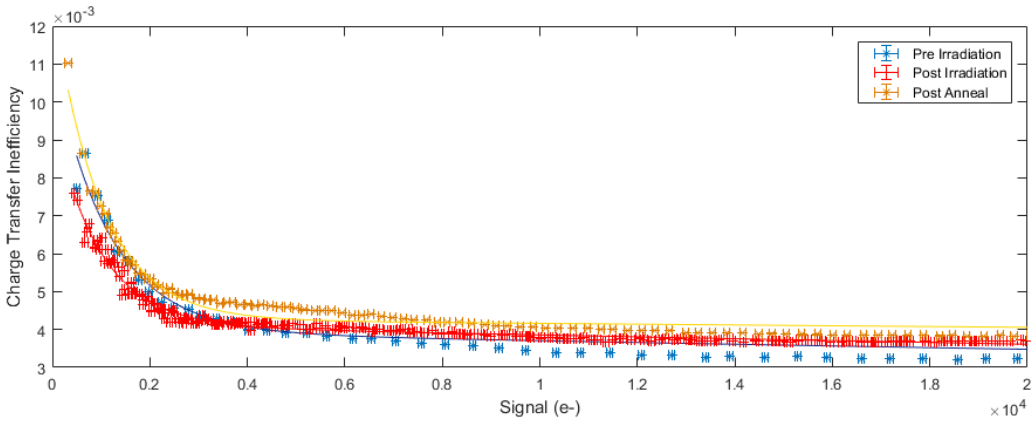

Figure 7.13: Average CTI for Block 6 pre and post irradiation, and post anneal.

The fits themselves found in Table 7.4 demonstrate the similarity in fits between the irradiated and annealed device. The shape of the curves for both post-irradiation and post anneal are largely comparable; however, there is an average fractional increase in the CTI after the eight-month anneal of 2.64 $\pm$0.02%. This fractional change is small compared with total average change in the CTI from before irradiation to after irradiation of 38.08 $\pm$0.03%. The impact of annealing on CTI in terms of defect mobility has been investigated in detail by the Chandra X-ray observatory team [4, 40]. After warming the Chandra test CCD to $\sim$ 293-303 K for 8 hours, a 35% increase in the CTI was measured [4, 40]. Figure 7.14 demonstrates the CTI for each region of the device at 273 K. When irradiated or operated cold both silicon interstitials and vacancies are highly mobile (below 173 K) enabling stable defects within the silicon lattice to form. For example, the carbon interstitials formed during irradiation when an Si atom changes location with a carbon atom is stable

Period	a	b	c	d
Pre	3.90E-3	-6.30E-06	7.22E-3	-9.00E-04
Post	5.60E-03	-1.06E-03	4.12E-03	-6.58E-6
Anneal	8.41E-03	-1.01E-03	4.27E-03	-2.53E-06

Table 7.4: Variable information for the best fit for the CTI when fitted with an exponential equation (x) = a*exp(b*x) + c*exp(d*x). The R square for all three fits exceed 0.96.

when cooled [38]. However, when operated at 303 k they are once again mobile and able to form metastable defects with phosphorus and carbon. Such defects could have impacted the CTI of the EMTC1 after annealing. The device was annealed at room temperature ($\sim$ 295 K) however, it was annealed in an environment where the temperature was prone to fluctuations. Subsequently, it can be assumed the fractional decrease can be attributed to defects becoming mobile as the device was annealed. These traps are currently unknown, with the activation energy currently the only source of identification for the traps. Further studies into proton damage in the EMCT1 would provide insight into the traps that formed and the potential effect annealing effect.

After annealing a clear "relaxation" in CTI is noted after 10 months at 295 K. This process was largely uniform across the device. However, Block 1 (see Fig. 7.14 (a)) differs slightly. Block 1 experiences a larger increase in the CTI at a signal of 4000 electrons at all testing points before irradiation and after annealing. This can be attributed to defect in this block. The fractional increase in CTI after the anneal is largely consistent with the rest of the device and the fit corresponds to a constant off-set. The anneal was only completed at one temperature. Different traps are known to anneal at different energies and annealing at a temperature about 303 K could further anneal the CTI. This temperature was selected as a number of studies into annealing of image sensors have been completed at room temperature [38, 60]. Modern annealing is often completed warm at temperatures exceeding $\sim$ 300 K. However, studies have demonstrated that some populations of bright defect concentrations could be annealed at room temperature for both CCD and CIS

image sensors [48, 49]. Subsequently, room temperature was chosen to anneal both the irradiated and aged devices described in this thesis.

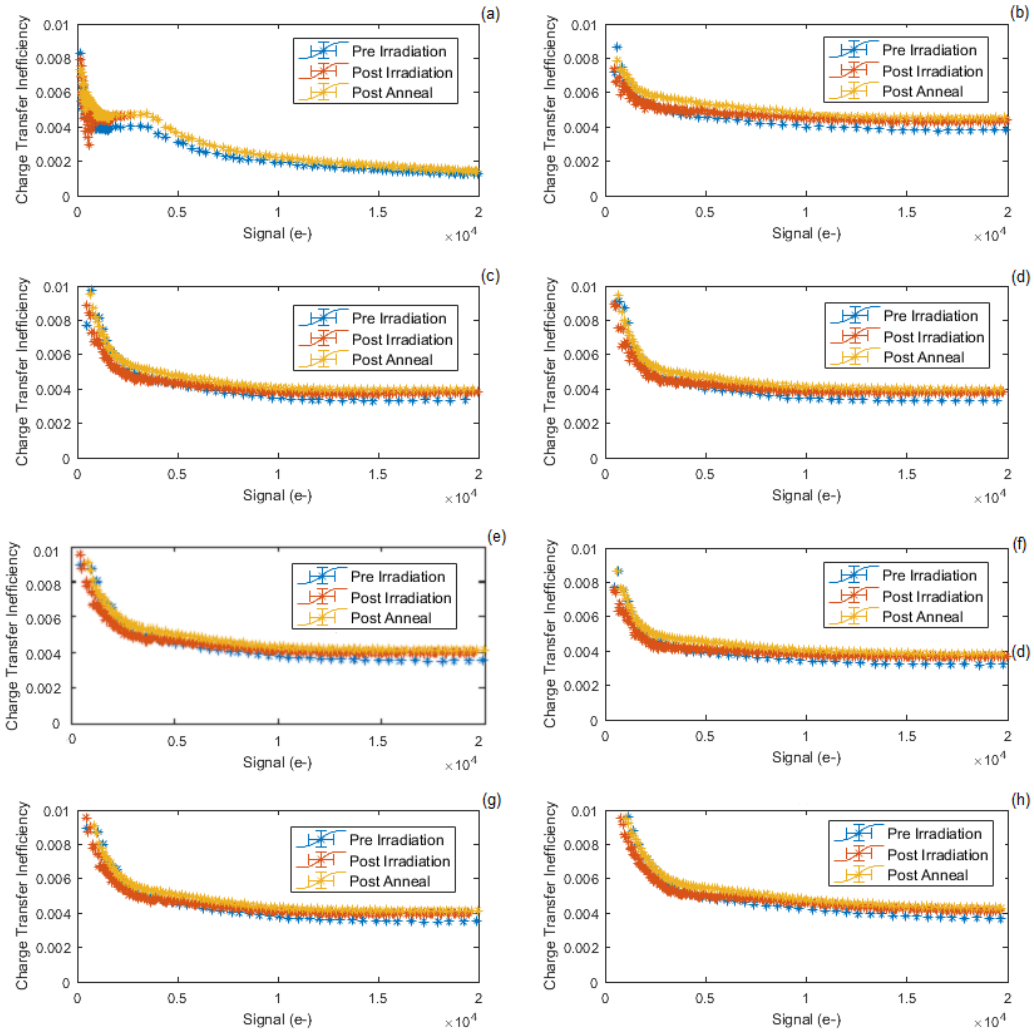

Figure 7.14: Averaged charge transfer inefficiencies across each region of the device at 273 K for pre and post irradiation and post anneal. (a) Block 1, (b) Block 2, (c) Block 3, (d) Block 4, (e) Block 5, (f) Block 6, (g) Block 7, (h) Block 8.

7.6.2 EM Gain

The EM gain was remeasured after the 10-month room temperature anneals at a range of temperatures. Figure 7.15 demonstrates the EM gain per stage as a function of temperature for Block 5. The decrease post irradiation in gain at high temperatures can likely be attributed to the high dark current which leads to saturation.

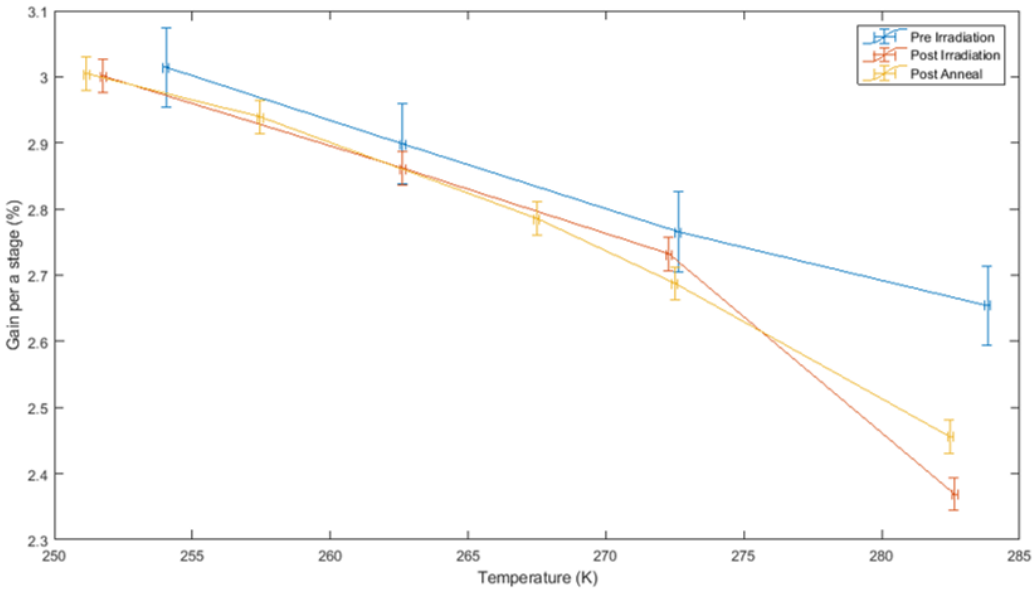

Figure 7.15: The EM gain per stage as a function of temperature comparing the pre and post EM gain for Block 5 region of the device against the EM gain after the eight-month room temperature anneal. The errors were calculated using standard errors calculated from the combined errors of the standard deviation of the regions of interest and from multiple image frames captured under the same conditions.

Other EMCCDs irradiated have also seen decreases in EM gain; however, this has largely attributed to the EM ageing process [101]. It has been demonstrated that when a CCD is irradiated biased, there is an increase in the ionisation damage [14]. This has been attributed to the increased electric field within the dielectric layers leading to a reduction in the probability that any photo-generated electrons can recombine due to forces pulling charge in the

opposite directions. As such, generally fields beneath P2HV generated within the EMCCD have a higher in magnitude than those experienced in a CCD due to the P2HV gate. High electric fields can lead to greater levels of ionisation damage, either in the form of transient or total dose effects. Transient events are where electron-hole pairs are separated by high electric fields and the recombination is negligible. It is possible for the holes to collect at the Si-SiO_2 interface, leading to a decrease in the EM gain. As holes collect at the Si-SiO_2 interface the potential difference to the buried channel is gradually decreased leading to a reduction in the EM gain. This would imply similar damage to that experienced during ageing and a lack of annealing here would insinuate that an aged device would also not undergo annealing. Research by Robbins *et al.* [93] has shown that once annealing has stabilised the differences between the biased and non-biased devices experience negligible differences in damage. A large percentage of the CTI can be considered a product of bulk damage as the capture of signal electrons by bulk defects induced by high energy protons in the bulk region leads to an increase in the charge transfer inefficiency [106]. Ionisation damage can lead to an increase in the CTI at high energies and temperature, but minimal impact is seen at lower temperatures. The number of ionisation traps can be affected by the bias regime which would result in an increase in the CTI [68]. It can be assumed here that the majority of the damage induced CTI here is bulk due to the energy at which the device was irradiated [22, 44].

7.7 Conclusions

The proton damage results demonstrate that the EMTC1 responds in a manner similar to other EMCCDs, CCDs and some CMOS image sensors when irradiated with similar fluences. The device also experiences a small decrease in EM gain that is not recovered after the anneal. A thermal anneal at a higher temperature may be sufficient to effectively anneal the damage from both proton damage and EM ageing.

7.8 Further Work

This work has only been completed at one fluence at room temperature. The device was not biased, as proton damage largely results in displacement damage. However, irradiation under a different bias regime would enable an investigation into the influences of the different trap species on device characteristics, especially CTI. To provide a thorough comparison of the device with other scientific image sensors when utilised in a radiation environment, it would be necessary to conduct this experiment under cryogenic conditions. This is because the majority of image sensors operated in space are cooled cryogenically to decrease the effects of dark current and CTI.

Proton damage largely results in displacement damage. Further irradiations, such as gamma or electron, would provide data on ionisation damage within the EMTC1, which would likely result in increases in dark current and a flatband voltage shift.

A considerable focus in this thesis has been on a comparison between the operational characteristics of each of the regions of the device. Further optimisation of the clock timing could improve the performance of the device post-irradiation. The proton irradiation and the majority of the testing in both this chapter and the next were completed with the same bias voltages used for initial testing limiting potential optimisation of the different regions of the device.

Chapter 8

Gain Ageing in the EMTC1

8.1 Introduction

An EMCCD can also suffer from an additional source of damage not traditionally seen in other image sensors, called ageing. There has not yet been a comprehensive study into the effect of ageing in CMOS devices using EM. This chapter studies ageing in the EMTC1 and provides a comparison with traditional EMCCD.

8.2 EMCCD Ageing

Ageing occurs when large signals pass through the EM gain elements. EMCCDs are designed such that they can withstand the high voltages required to produce gain; however, the high electric fields can lead to irreversible damage, seen as a decrease in gain, over the lifespan of the device.

The rate at which ageing occurs depends on several factors, including signal, gate voltage, and temperature [31]. Previous studies have demonstrated that the ageing can occur in two stages [73, 31, 53]. An initial drop in the gain slows to a gradual decrease in EM gain over the lifespan of the device. Many

manufacturers condition EMCCD sensors before distribution to ensure that most degradation has already happened. Research has demonstrated that it is possible to counter the loss of gain by increasing the high voltage applied to the P2HV gate [73], an example of this can be seen in Figure 8.1.

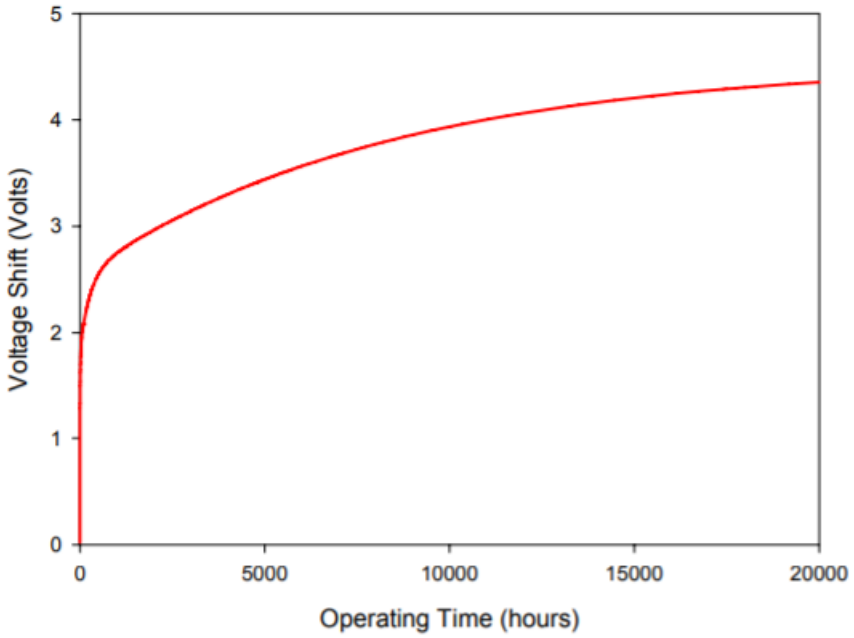

Figure 8.1: The voltage shift required to maintain the gain of CCD65 when operated at 11 MHz pixel rate as a function of operating time with output signal of 300 ke-. The normal operating voltage of the CCD65 is $\sim$ 41 V. Original figure found in [115].

The factors affecting the ageing process were probed in a study completed by Teledyne e2v on its L3Vision CCD [115, 114]. The L3Vision range are EMCCDs developed for ultra-low light applications with photon counting capabilities at high frame rates [117]. The decrease in gain was presented as the required shift in the high voltage gate to maintain the original gain. This voltage shift was shown to have an exponential dependence on time [115]

$$\Delta V = A(1 - exp(-t/\tau)) \tag{8.1}$$

where τ is the time constant, t is the operation time, and A is the proportionality constant.

In addition, the research demonstrated that ageing rapidly accelerates at large signals. Limiting high potentials and high input signals have been used in practice to reduce ageing.

Previous studies [31, 30] have shown that the ageing process can be attributed to hot carrier damage in the nitride layer. A silicon nitride layer is deposited onto the EMCCD using a Low-Pressure Chemical Vapour Deposition (LPCVD) process. In combination, the stack of silicon oxide and silicon nitride constitutes the gate dielectric in Teledyne e2v's process. For a device without a nitride layer, it was expected that there would be no ageing. Other causes were also proposed which could be linked to increases in CTI, including damage to the interface. The following section discusses the effect of hot carrier damage, which has been strongly linked to the ageing process.

8.3 Hot Carrier Damage: The cause of EM Ageing?

Impact ionisation occurs when charged carriers are accelerated through regions of high electric field to high velocities. These energetic carriers are called hot carriers and can be either electrons or holes. The carriers must have sufficiently high energies and momenta to be injected into dielectric films including the oxide and the gate. For charge carriers to be injected into the gate oxide, the carriers require a high kinetic energy to reach the conduction or valence band in the oxide (3.2 eV for electrons and 4.6 eV for holes) [90]. Mobile carriers in the oxides can trigger various physical processes which can alter the device characteristics over prolonged periods of time and can result in device failure. The change in device behaviour is described as "hot carrier degradation". It has been demonstrated that large electric fields can directly influence the long term operation of modern devices. Hot carrier device degradation has been the subject of a number of studies and has been observed in a number of device structures [122, 85, 88].

Hot carrier damage is closely related to the damage that can be induced during irradiation. Several hot carrier damage mechanisms are com-

monly encountered in MOSFETs, as described below.

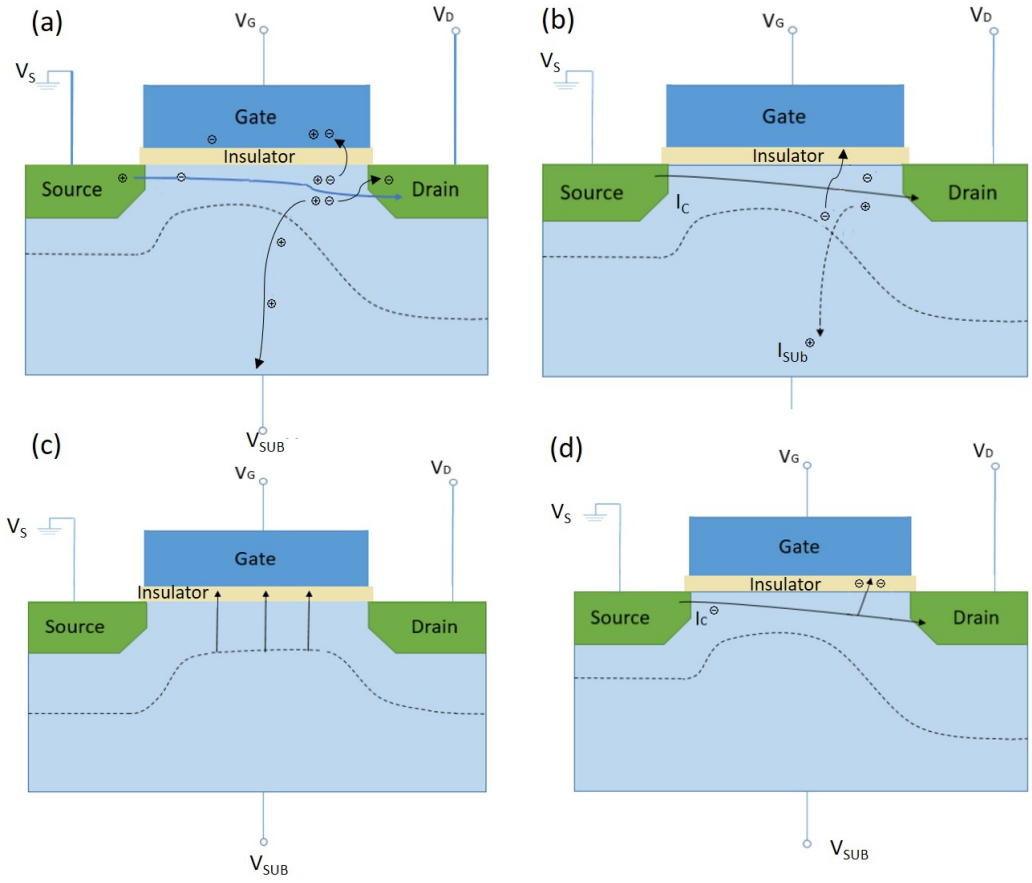

Figure 8.2: Hot Carrier Mechanisms (a) DAHC ($V_d = 2V_g$) (b) SGHE (c) SHE ($|V_{sub} > 0|$) (d) CHEI ($V_d = V_g$).

8.3.1 The drain avalanche hot carrier

Drain Avalanche Hot Carrier (DAHC) [110, 109] occurs due to the generation of electron-hole pairs due to impact ionisation (see Fig. 8.2 (a)). A high voltage near the drain results in a high electric field and an acceleration of electrons into the drain's depletion region. Electrons resulting from impact ionisation are attracted towards the gate while the holes drain towards the substrate. Damage can occur when the hot electrons become trapped at the silicon-silicon dioxide interface or the oxide layer. If the charge does not become trapped, it contributes to the charge packet. Measurements of DAHC can prove difficult

as both carrier types undergo injection simultaneously and generated carriers can contribute to the bulk current.

8.3.2 Secondary Generated Hot Electron Injection (SGHE)

When under similar conditions to DAHC (when the drain voltage is higher than the gate voltage) it is possible that a secondary carrier is created from an earlier incident of impact ionisation [82, 62]. This is known as Secondary Generated Hot Electron Injection (SGHE). Photogenerated electron-hole pairs undergo avalanche impact ionisation near the drain region leading to the injection of holes and electrons into the dielectric (see Fig. 8.2 (b)). The substrate bias induces a field driving the hot carries towards the surface region.

8.3.3 Substrate Hot Electron (SHE)

When the substrate bias is high (either very positive or negative), carriers may be driven into the silicon-silicon dioxide interface by the substrate field (see Fig. 8.2 (c)). The high field within the surface depletion region further increases the kinetic energy of the carrier. In Substrate Hot Electron (SHE) the high energy of the carriers is sufficient to overcome the surface energy barrier and are injected into the gate oxide. Within this oxide, the carriers can become trapped.

8.3.4 Channel Hot Electron Injection (CHEI)

If the gate and drain voltage are of similar value and are significantly higher than the source voltage, charge can be driven into the gate oxide as they pass from the source to the drain due to the high gate voltage (see Fig. 8.2 (d)). Channel Hot Electron Injection (CHEI) can result in the degradation of device performance due to the development of interface traps and electron traps in the gate oxide [63, 111].

These stress conditions are inherent for CMOS devices as the main source of hot carriers is from the heating within the MOSFET channel. Impact ionisation triggered by the energised electrons within the substrate generates electrons or holes which can produce defects at the interface or in the bulk oxide.

8.3.5 Common Characteristics of Hot Carrier Injection

Hot carrier injection is dependent on a number of factors that can be utilised to understand further the nature of the damage. Several studies have found that the majority of oxide degradation is due to interface traps. In deuterium-passivated devices, smaller interface trap concentration have been observed when compared with hydrogen-passivated devices [64]. This strongly indicates that the Si-H bond breaking causes the interface trapping. A power law time dependence was also observed, reflecting the hole trapping induced shift within the degradation region. Hot carrier injection is also known to be temperature dependent. Previous studies of hot electron injection at room temperature have demonstrated that the device lifetime is determined by the maximum channel electric field and the substrate current [110]. At low temperatures a reduction in the phonon scattering leads to an increase in the average kinetic energy of the electrons, increasing the impact ionisation rate. A higher voltage leads to a higher field strength increasing the kinetic energy of the carriers, leading to an increase in degradation.

8.4 Ageing Characterisation

The characterisation was carried out by systematically ageing the device over extensive time periods. The device was run at the highest possible P2HV voltage and with the light-generated signal above saturation. This was achieved by illuminating the device for 800 μs during the integration period generating a signal of 20k electrons. The EM gain was measured prior to and post ageing. The device was aged for incremental periods of time starting at 1 minute, increasing to 5, 10, 30 minutes and several hours. After each ageing interval,

the EM gain was measured at 4 P2HV voltages: 12.0, 12.5, 13.0 and 14.0 V. The complete ageing characterisation of one device took seven days. During this time, the dark signal was also measured to compare the values pre and post ageing to allow for insight into the ageing mechanism.

Due to limitations in the thermal conduction, the ageing test of EMTC1_C5 was completed at 282 K. The device was operated for 150 hours at a P2HV voltage of 15.0 V. The device was then retested at incremental voltages and device illuminations at regular time periods. After ageing, the device then underwent a complete characterisation. The second ageing test was completed using device EMTC1_B3, which utilised the new experimental setup and allowed the device to be aged when cooled. The device was fully characterised prior to the ageing process at temperatures in the range of 250 to 300 K using the same characterisation techniques described in Chapter 3.

The ageing of EMTC1_B3 was then carried out at 250 K under vacuum conditions. The ageing was induced in several steps; the device was initially tested at each P2HV voltage at increasing illumination times from 0 to 1000 μs generating an input signal from 0 to 100k electrons. The device was then held at a P2HV voltage of 15.0 V, and the device was illuminated with an input signal of 5000 electrons for 30 minutes before the measurement of the EM gain. This process was repeated for a total of 157.6 hours, not including the time taken to re-characterise the EM gain after each ageing period. Each EM gain characterisation would take an average of 2.5 minutes, giving a total operational period of approximately 170 hours. The device underwent EM gain characterisation every $\simeq$30 minutes for the first 140 hours; however, once it was apparent that the device had entered the second stage of ageing, this interval period was increased to $\simeq$60 minutes. The device was retested after annealing at room temperature for approximately 5.5 months to enable a comparison with the proton irradiation. This retesting process was automated, and the Labview was adapted as part of this thesis.

It is common practice to quantify the ageing by compensating for the decrease in the EM gain by increasing the P2HV voltage. The change in the voltage can then be quantified as the voltage shift required to maintain a constant gain, as shown in Figure 8.1. Due to complications in the required

experimental setup, it was decided that in this work, the decrease in the EM gain would be measured directly.

8.5 Experimental Results on Ageing

The following section describes the results of the EM gain ageing of the EMTC1 at a P2HV voltage of 15.0 V and a device illumination producing a signal of 20 ke-. This illumination was sufficient for all regions of the device to reach saturation. The sensor was initially aged at 283±0.5 K.

To create an effective comparison between the annealing seen in the EMTC1 after proton irradiation and that after ageing, the aged devices were also annealed for eight months at room temperature. The device was retested, and the results were compared. As described in Chapter 7 annealing is a common tool used when devices have been exposed to radiation due to silicon lattice damage. This results in induced hot pixels, which can be annealed when warmed to room temperature. An eight month room temperature anneal was in part selected to enable a direct comparison with the proton irradiation anneal described in Chapter 7. However, due to time constraints, this anneal was limited to 8 months.

8.5.1 Photoelectric Response

The photoelectric responses of the aged devices were analysed using the mean-variance method. The noise measurements were taken before and after ageing. The reduction in dark current and CTI after annealing of the irradiated device has previously been noted, as was the effect on the EM gain. As such, it was hypothesised that a room temperature anneal could lead to a recovery of the dark current and provide insight into ageing mechanisms.

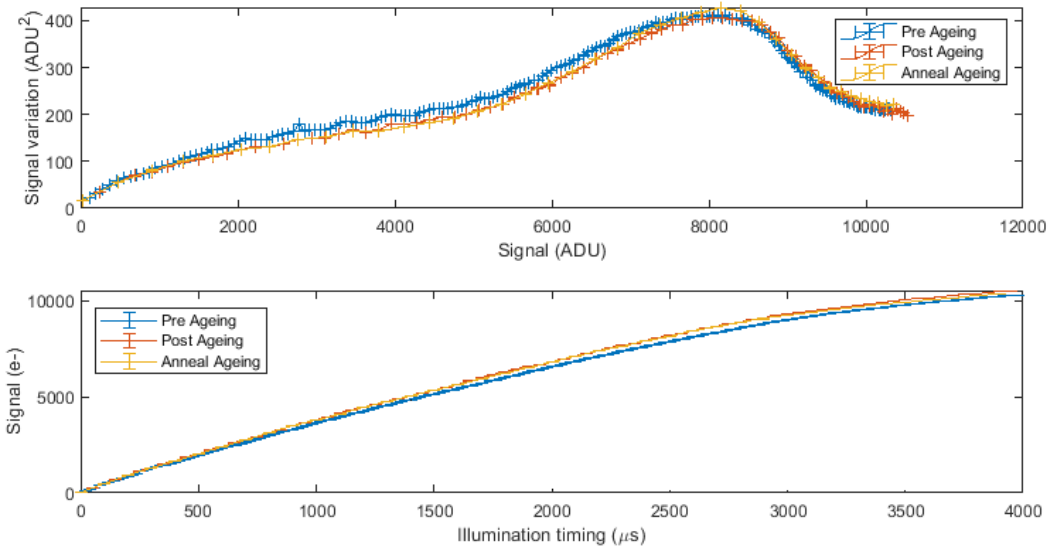

Figure 8.3: The linearity and mean-variance for Block 5 at 253 ±0.5 K comparing pre and post ageing and after an eight month anneal. the errors were calculated from the standard deviation of the mean of 100 measurements for each point.

The PTC could be used to determine the full well capacity and to analyse any loss of linearity post ageing. Figure 8.3 plots the mean-variance curve and linearity pre and post ageing and after the anneal. The figure demonstrates a small decrease in the full well capacity with no loss of linearity. Table 8.1 presents the parameters acquired from the mean-variance curve, including the full well capacity and non-linearity.

Parameter	Pre Ageing	Post Ageing	Post Anneal
Full well capacity	$8.31\times10^4 \pm 8.2 \times 10^2$	$8.02\times10^4 \pm 4.3 \times 10^2$	$8.11\times10^4 \pm 6.4 \times 10^2$
Non-linearity at 50k e-	2.20±0.002%	2.72±0.004%	2.48±0.004%
Non-linearity at 100k e-	5.88±0.008%	5.64±0.01%	6.04±0.01%

Table 8.1: Parameters acquired from the mean-variance linearity curve for Block 5 when operated at $\sim$ 253 ±0.5 K comparing the results from pre and post ageing and post anneal.

No significant changes in the EMCCD linearity or full well capacity were observed. With no significant change in the full well capacity, it can be assumed that there has not been a threshold voltage shift induced by the ageing process. While all values vary slightly outside of the errors, these variations can be attributed to small changes in the temperature.

8.5.2 EM Gain

The main focus of the study was to analyse the effect of the ageing process on the EM gain over an extended period of operation. Once the temperature had stabilised, the temperature fluctuations were ±0.5 K and had negligible influence on the gain measurement. These results could then be compared with preexisting data that on a Teledyne e2v CCD65 by Evagora [31] where the ageing had been carried out ∼ 301 K.

Region	a	b	c
Block 3	-1.18E-4	0.65	1.63
Block 4	-1.29E-4	0.68	1.62
Block 5	-1.45-E-4	0.67	1.64
Block 6	-1.11-E-4	0.70	1.62
Block 7	-8.16E-3	0.34	1.64
Block 8	-6.9E-3	0.30	1.64

Table 8.2: Variable information for the power best fit of $y = ax^b + c$ for EMTC1_C5 for each region of the device when P2HV = 12.0 V after ageing with a signal of 10k electrons.

The initial ageing was completed at 283 ±0.5 K and aged over 10260 minutes with an input signal of 10000 electrons. Figure 8.4 shows the decrease in EM gain per stage as a function of the time for several P2HV voltages. The fit information for the initial ageing period can be found in Table 8.2 using a polynomial fitting. Block 8, which experienced the greatest ageing, aged at a rate equivalent to a loss of gain of 0.0097% per hour.

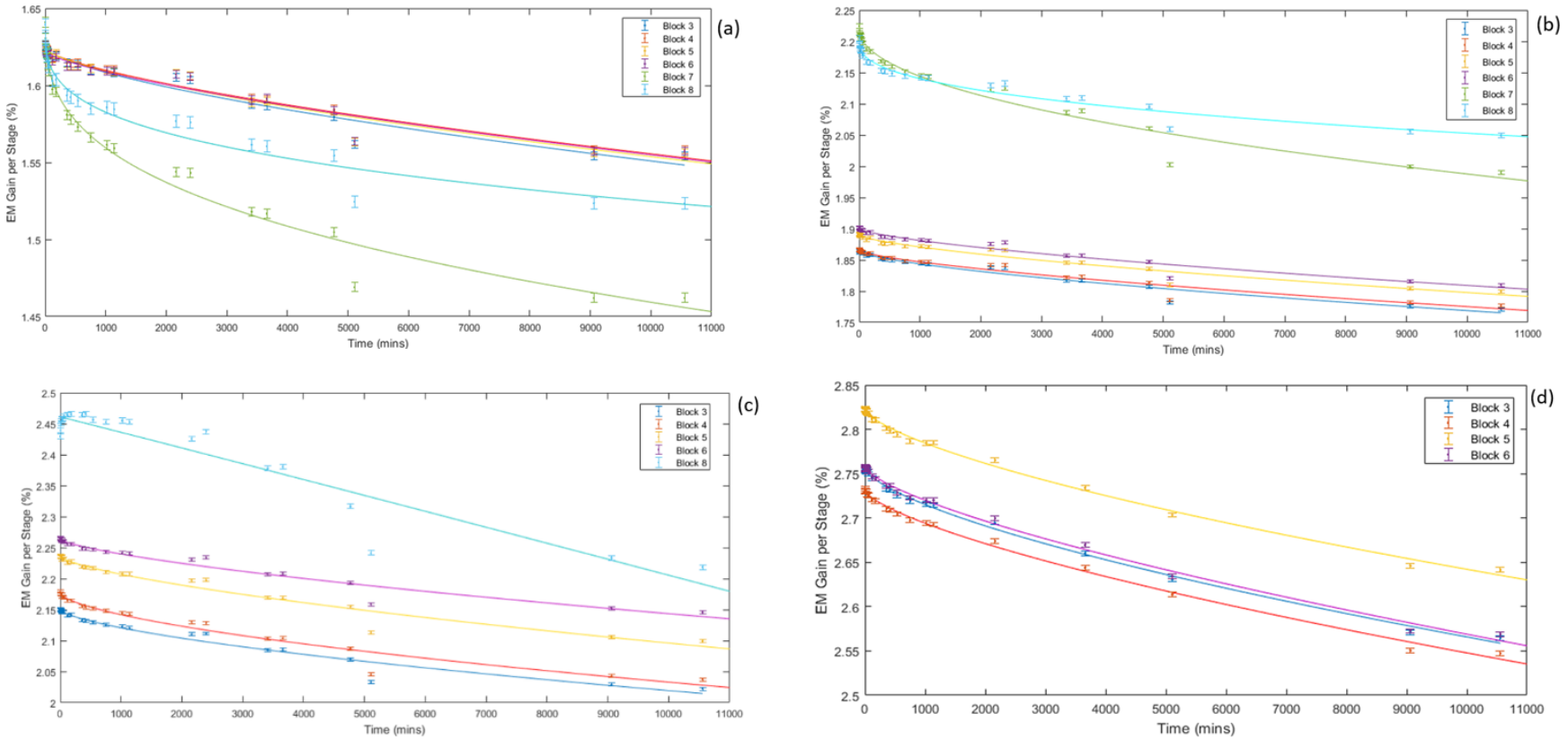

Figure 8.4: The EM gain per stage as a function of operation time at 283±0.5 K with a signal of 1000 electrons. (a) P2HV = 12.00 V, (b) P2HV = 12.50 V, (c) P2HV = 13.00V and (d) P2HV 14.00 V. (c) and (d) do not include all blocks due to these regions experiencing saturation.

The rate of loss of gain can be found in Table 8.3 for each EM pixel. The errors in the table here were calculated from the mean of the raw data. The rate of loss in Table 8.3 is calculated as the percentage loss per hour. The initial gain of each block prior to ageing can be found in Table 5.9. The rate of loss was found to decrease non linearly as a power function with the variables in Table 8.2. The rate of decrease in gain was not uniform across the regions of the device, with Blocks 7 and 8 experiencing percentage decreases of $6.19\times10^{-3}\pm$ and $9.67\times10^{-3}\pm$ per an hour compared with the average decrease of blocks 3-6 of $6.19\times10^{-4}\pm4.03E-06$. Blocks 7 and 8 experience a loss of gain a factor of 10 higher than the rest of the device; however, their gain prior to ageing was only a factor of ~ 2 larger. The regions which experience the higher gain contain larger signal packets and subsequently induced a greater quantity of damage as each subsequent charge packet passes through the device. As each signal packet passes through the next stage, the packet size increases and there are a higher number of hot carriers able to induce damage. With each subsequent charge transfer, the risk of damage increases. With a higher initial gain, there is a larger signal packet resulting in a greater reduction in gain. Furthermore, with the novel gate shape and structure, the shape of the electric field is stronger nearer the interface leading to a higher probability of hot carrier interaction with the interface and subsequent decrease in the EM gain. At this stage, it is difficult to differentiate the impact of the high gain versus the increased ageing due to the location of the electric field. Blocks 3 to 6 have a largely consistent rate of loss of gain. The loss of gain could then be compared to the ageing experienced by modern commercial EMCCDs. Research completed by A. Evagora et al (2012) [31] demonstrated that the e2V CCD97-00 undergoes ageing when operated at a working P2HV voltage of 40 V (the normal working voltage of the CCD97-00) when aged at 301 K. The rate of loss of gain per hour when aged for 25 hours was 0.33 %, over fifty times larger than the highest rate seen in the EMTC1. It is also of interest to note that the initial ageing process of the CCD97-00 was linear experiencing a rate of of 2% an hour when aged for 17.5 hours at a voltage 40.5 V. The reasoning for this difference is explored later in this thesis however it is apparent that novel structure of the CMOS has led to a dramatic reduction in the total ageing process.

The second device was aged in several stages. It was initially operated

Block	Voltage	Loss of Gain per hour
3	15.00 V	$6.44\times10^{-4}\pm 1.2\times10^{-6}$
4	15.00 V	$4.11\times10^{-4}\pm 3.2\times10^{-6}$
5	15.00 V	$7.69\times10^{-4}\pm 6.4\times10^{-5}$
6	15.00 V	$6.53\times10^{-4}\pm 5.3\times10^{-6}$
7	15.00 V	$6.19\times10^{-3}\pm 2.4\times10^{-5}$
8	15.00 V	$9.67\times10^{-3}\pm 5.6\times10^{-5}$

Table 8.3: The rate of loss of gain per hour after the device was aged for 12608 ± 4 minutes at 15.0 V when illuminated with input signal of 10000 electrons at 283 K.

without an external input signal at P2HV = 15.0V for 107 hours (Test 1). The ageing was retested, and no decrease in gain was measured. The second ageing period was operated with a charge input of 1000 electrons over 377 hours (Test 2) shown in Figure 8.5.

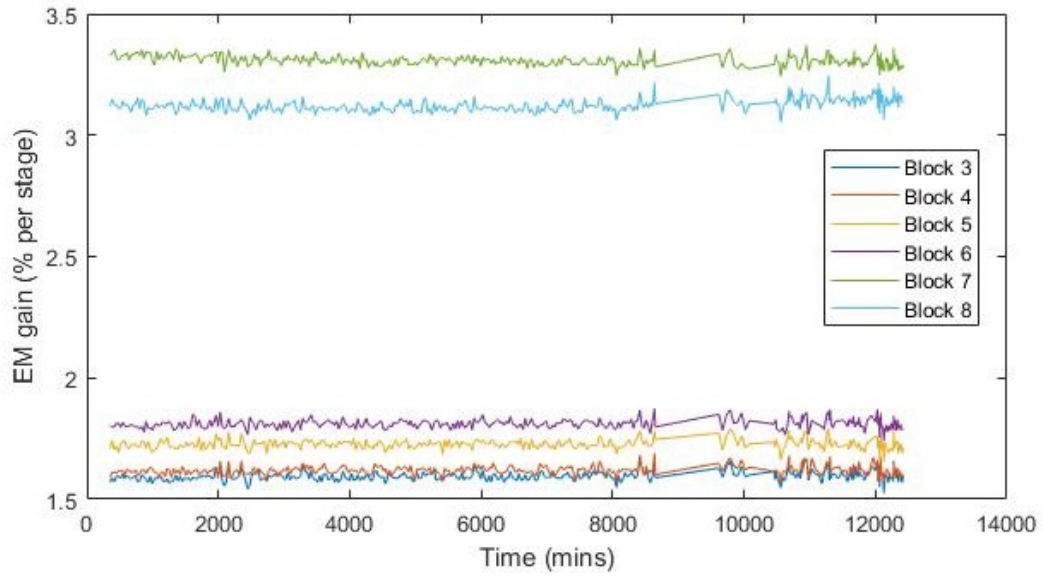

Figure 8.5: The EM gain as a function of the ageing time when the sensor has been illuminated with a signal of 1000 electrons at 243 ±0.5 K. Operated at P2HV = 13.0 V.

EM ageing was noted with a linear decrease in the gain (see Figure 8.5) and a small increase in the dark current.

Finally, EMTC1_B3 was aged for an additional 75 hours with an input signal of 10000 electrons (Test 3). The fit for Block 8 of EMTC1_B3 can be found in Table 8.4.

Fit	Test 2	Test 3
a	-6E-7	-1.11E-3
b	-	0.46
c	3.12	1.28

Table 8.4: Variable information for best fit for both ageing tests of the EMTC1_B3 Block 8 at 243 K. Test 2 was a linear fit of y=ax+c while Test 3 was fitted with y = ax^b+c. The R square for both fits exceed 0.98.

From Table 8.4 it is clear to see that the ageing is dependent not only on the avalanche potential but also the signal size. If the simulations shown in Chapter 6 are considered, it is possible to see that the charge packet's location changed depending on the length of the gate and avalanche potential. By increasing the signal packet size, it extends more closely to the interface, increasing the probability of hot carriers interacting with the surface leading to surface trapping. Furthermore, due to the cumulative nature of the EM gain register, the signal packet will increase in size and subsequently increase ageing through the following registers. Finally, while the EM gain is still considerably higher for Blocks 7 and 8 than the rest of the blocks, the decrease in gain was largely uniform across the device when illuminated with a small signal. It is only at high signal input that the ageing process becomes significant. It has been demonstrated in previous chapters that the length of the gate can directly affect the location of the charge and impact ionisation region; however, the exact impact on the ageing process is unknown. It can be assumed that the high level of EM gain results in a large signal packet which has been demonstrated to have a direct impact on the ageing process. Further simulations could provide insight into the effect of the novel pixel structures on

the ageing process. However, while percentage decrease in ageing is dependent on the pixel structure (in part due to the higher initial gain), it can be assumed that should the charge be interacting with the same regions of the device, the traps should remain the same independent of the device region.

8.5.3 Charge Transfer Efficiency in Aged Devices

As described in previous chapters, the charge transfer efficiency is an important device parameter. Changes in the CTI provide insight into the damage mechanisms causing the ageing process. One cause proposed for the decrease in gain can be attributed to an increased density of trapped charge, reducing potential at the P2HV gate and the strength of the electric field. It can be proposed that a device which has undergone such ageing will exhibit an increase in CTI. The CTI was measured using the EPER method as described in chapter 6. It can be seen from Figures 8.6 and 8.7 that there is no increase in the CTI either as a function of temperature or signal. Furthermore, this result is uniform across the device independent of the device's region or the temperature at which the device is aged.

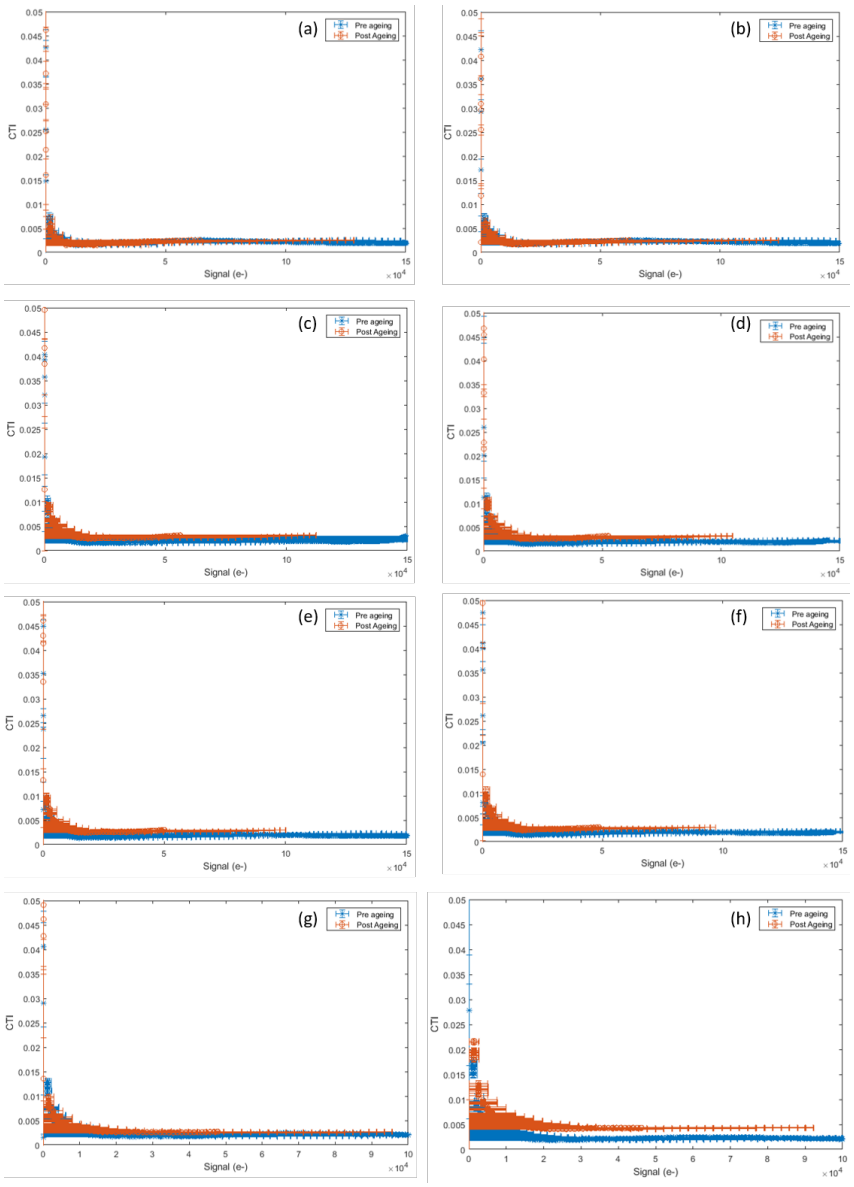

Figure 8.6: The CTI as a function of signal at 243.0±0.5 K for each region of the device. (a) Block 1, (b) Block 2, (c) Block 3, (d) Block 4, (e) Block 5, (f) Block 6, (g) Block 7 and (h) Block 8.

Figure 8.6 demonstrates the CTI for each region of the device after ageing for $\sim$ 175 hours at 243.0$\pm$ 0.5 K. It is of interest to note that there has been a small increase in the CTI as a function of signal for Blocks 7 and 8. The increase in CTI is most notable at mid to high illuminations, which can be attributed to the aged device suffering from a reduction in the full well

capacity leading to device saturation. Figure 8.7 compares the CTI before and after ageing and there is a notable increase in the CTI once aged. In addition to an increase in the average CTI, there is also a notable increase in the standard deviation of the CTI from 0.0101 to 0.0307. This indicates that after the ageing period not only is there an average increase in the CTI but there are also a number of columns that experience an above average increase in the CTI.

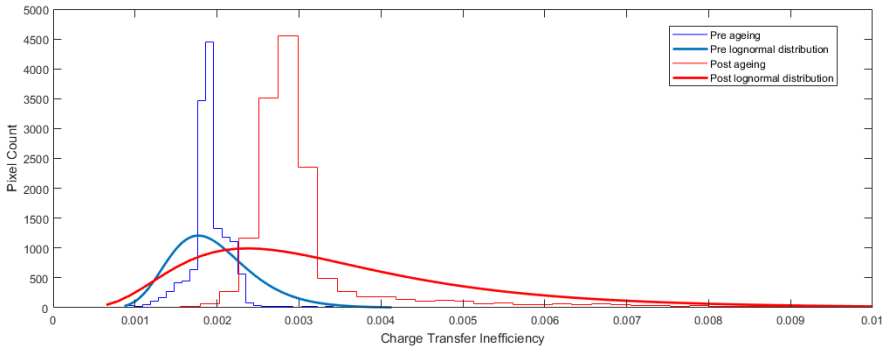

Figure 8.7: Fitted histogram comparing the CTI pre and post ageing for EMTC1_C5 block 6 at 243 K.

This result provides insight into the nature of the damage induced during the ageing process. As discussed earlier in this thesis, an increase in the CTI after irradiation is normally dominated by trapping by bulk states [44]. The EPER method is flawed because it is a relative test tool and does not provide an absolute measurement of the charge. As such, a device may experience an increase in the CTI, but the deferred charge may not be measured due to the location of the trap and the clocking speed. Furthermore, EPER does not detect surface traps only bulk. As such, it would be expected that there would be no increase in the CTI if the ageing is attributed to surface traps. An explanation for this increase is not provided in this thesis, but further analysis should provide greater insight into the cause for the increase in CTI.

8.5.4 Dark Current

Damage to the silicon induced by radiation damage has been demonstrated to increase the dark current due to displacement or surface damage. Utilising the activation energy derived from Arrhenius plot it is possible to determine trap types contributing to the dark current, and subsequently, an increase in dark current can provide insight into the ageing process. In an aged device, there has been a demonstrable increase in dark current.

8.5.4.1 Dark Signal Through the Device

As the signal passes through the device, it transfers from electrode to electrode within the buried channel. When EM is used, electrodes nearer the readout experience a larger quantity of signal passing through them as each signal packet gains charge.

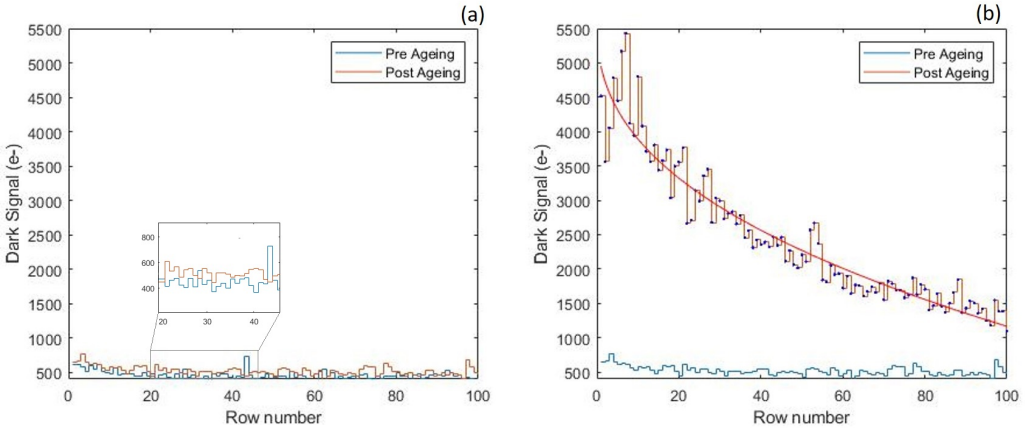

Figure 8.8: Dark signal along column 14 pre and post ageing at 293.0 K: (a) Block 2(non-EM) and (b) Block 4 (EM). The device readouts from high row number to low row number (i.e. from right to left in the above figures). The original figures were published in [25].

Figure 8.8 (a) demonstrates the dark signal pre and post ageing for Block 2, a non-EM region which does not experience gain and was not expected to experience ageing. The results show a fractional uniform increase in the

dark current. In comparison, Figure 8.8 (b) shows a large non-uniform dark current increase for EM block 4. The dark current increases in the direction of the readout as the cumulative signal increases. Increases in the dark current imply an increase in the number of traps proportional to the quantity of signal passing through. Fitting a power law curve to Figure 8.8 (b) resulted in the following equation:

$$y = -672.7x^{0.41} + 5624 \tag{8.2}$$

where y is the dark signal and x is the pixel number.

The dark current was measured pre and post ageing as a function of temperature, enabling the activation energy to be calculated from the Arrhenius plot [133].

The dark current was shown to increase across all EM regions of the device for both ageing temperatures. Figure 8.9 demonstrates the dark current and subsequent activation energies for Block 3. The dark current pre ageing had a small spread and a small number of hot pixels. After ageing the average dark current increased by over a factor of 10 from 7.51×10^3 $\pm$12.3 to 9.12×10^4 $\pm$12.3 e-/s/p when operated at 273 K. Mostly notably the increase in dark current led to an increase in the spread of the dark current from 520.6 to 2.86×10^4. This large spread is indicative of an increase in the number of hot pixels created either due to either damage or due to the high field phenomenon. Further study of the hot pixel would provide additional insight into not only the ageing process but also the formation of hot pixels as a result of hot carrier induced damage.

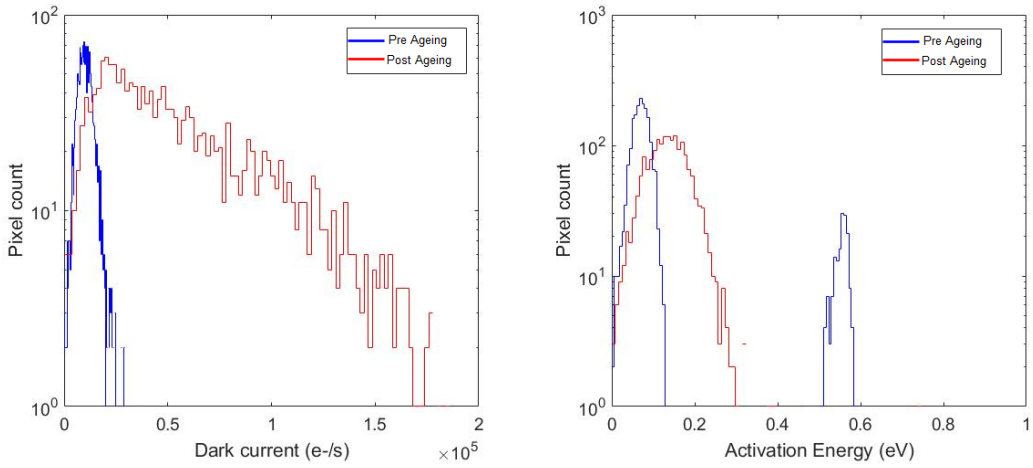

Figure 8.9: A comparison of the dark current and the activation energy for Block 3 of EMTC1_C5 after the device has been aged for a total of 10750 minutes 3 at 273 ±0.5 K.

The dark current and subsequent activation energies were then measured after the device had been annealed. Figure 8.10 demonstrates dark current for each of the EM regions of the device before and after ageing and after the annealing process. At 273 K the increase in dark current did not result in an additional peak but a shift in the total dark current and an increase in the spread of the dark current. This increase in the spread can be attributed to the formation of new hot pixels.

The traps formed in these hot pixels are then annealed over the 8 months. All regions of the device experienced an increase in dark current after ageing and subsequent decrease in dark current after annealing. Table 8.5 compares the dark current after each stage. It is apparent from the table that there was a lack of uniformity across the device. The regions which experienced the highest EM gain and subsequently ageing also experienced a larger increase in the dark current. Averaging across the entire EM region of the device results in a percentage increase of the dark current of 177%, with block 7 experiencing a 348% increase in the dark current. This is an increase in dark current over a factor of 2 higher than that experienced by the irradiated device. Again the annealing process was not uniform across the device, with device that experienced the least amount of ageing experiencing the greatest

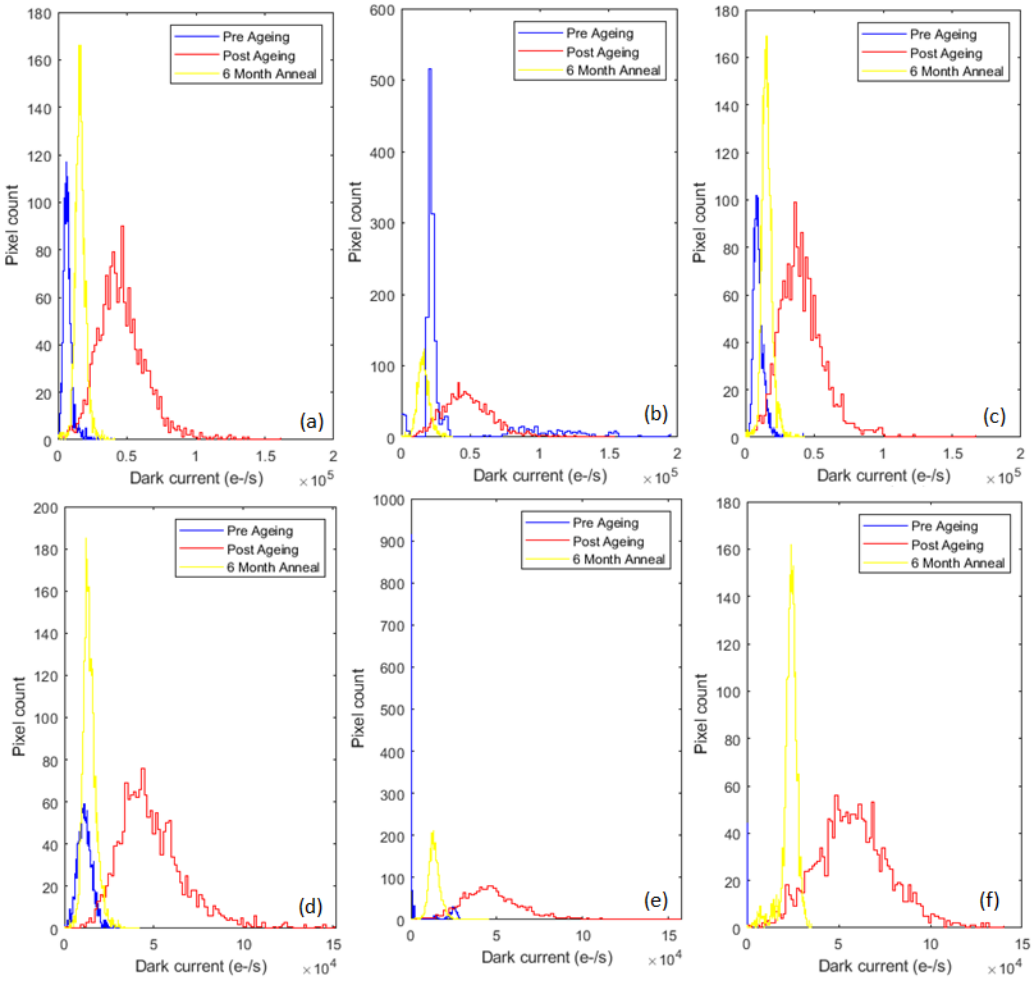

Figure 8.10: A comparison of the dark current for EMTC1_C5 after ageing for a total of 10750 minutes at 273 ±0.5 K. (a) Block 3, (b) Block 4, (c) Block 5, (d) Block 6, (e) Block 7 and (f) Block 8

decrease in the dark current. Once again comparing the aged dark current results to those seen in Table 7.3, the average decrease in dark current after annealing for the aged device was 169% compared with the 7.9 % decrease seen after the irradiated device was annealed. By comparing the results of the aged and irradiated sensors, it is possible to determine that there was a far greater increase in dark current after the ageing and then a greater anneal than seen in the irradiated devices. This implies that the initial damage induced by the ageing exceeded that of the irradiation; however, the annealing process had a more significant impact over a shorter period of time. In conjunction with the CTI results, this implies that not only was the damage (trap formation) in

Block	Pre DC (e-/s/p)	Post DC (e-/s/p)	Anneal DC (e-/s/p)
3	$1.00\times10^4\pm2.48\times10^2$	$3.43\times10^4\pm 2.19\times10^2$	$1.88\times10^4\pm2.19\times10^2$
4	$2.96\times10^4\pm7.31\times10^2$	$3.45\times10^4\pm 5.97\times10^2$	$2.41\times10^4\pm5.97\times10^2$
5	$1.41\times10^4\pm3.48\times10^2$	$3.44\times10^4\pm 1.86\times10^2$	$7.54\times10^3\pm1.87\times10^2$
6	$1.33\times10^4\pm3.29\times10^2$	$3.52\times10^4\pm 8.71\times10^2$	$6.74\times10^3\pm1.67\times10^2$
7	$5.38\times10^3\pm8.48\times10^1$	$2.41\times10^4\pm 8.51\times10^2$	$1.76\times10^4\pm4.36\times10^2$
8	$1.39\times10^4\pm3.43\times10^2$	$3.42\times10^4\pm 8.46\times10^2$	$1.94\times10^4\pm4.80\times10^2$

Table 8.5: The dark current for each EM region of the device when test before and after ageing and after the 8 month anneal. The errors were calculated from the standard error from multiple images taken under the same conditions. This dark current was measured when the device was operated at 293 K.

another location, the traps themselves differed in their nature. However, due to both devices experiencing a decrease in dark current after the anneal and the dependence of the trap coefficients on temperature, it can be postulated that there is a partial overlap in the nature of the traps formed after both types of damage.

This annealing regime was utilised to give a comparison to the damage documented after the proton irradiation. Prior to the start of the ageing process, it was not known if a device without a silicon-nitride layer would undergo ageing, let alone the processes that would lead to ageing. To understand the damage mechanisms within this novel structure, comparisons with the known damage mechanisms triggered by proton irradiation were made to better understand if the same traps were formed. Annealing traps are known to be temperature dependent. By annealing at a set temperature, it is possible to determine the type of trap. The annealing temperature, 293 K was chosen to anneal in part due to the experimental setup. Also, the time frame was chosen to maximise the effect of the anneal and to once again compare to the anneal process experienced by the irradiated device. It has been noted that the higher the annealing temperature, the shorter the period of time. However, studies have demonstrated that at any temperature there is a saturation

effect at long annealing times [12]. As such, the long time period should result in all any traps that can anneal at that temperature.

Annealing the aged device at only one temperature limited the type of trap that could be annealed. By annealing, at several temperatures, a greater understanding of the type of traps could be gain and the traps' location.

8.5.4.2 Dark Current Spectroscopy

As discussed in the previous chapter, it is possible to determine the type of trap formed in silicon. There have been many theories proposed concerning the source of damage resulting in the decrease in the EM gain; however, it has yet to be fully understood. By analysing the changes in the dark current, it can be possible to determine the type of trap developed and subsequently, it may be possible to understand where these traps are formed. When the dark current is measured at a sufficiently high temperature and integration time, it is possible for the pixel-to-pixel difference to be amplified and quantisation can be observed. The quantisation was noted in other blocks post ageing as demonstrated in Figures 8.11 and 8.12, where distinct regions in the dark current as a function of temperature can be noted. However, the highest level of quantisation was noted in Block 8. This can be attributed to the high level of ageing experienced in Block 8 due to the far higher gain achieved in this region. It was theorised that the type of trap would be independent of the shape of the HV gate structure, even though the location of the damage may differ. Once the device had been aged, the relationship between the dark current and the inverse of temperature becomes more linear. This can be attributed to the overall increase in dark current. Furthermore, those regions which experience higher EM gains and subsequently higher ageing experienced a greater level of dark current quantisation. The dark current for Block 7 is an order of magnitude lower than the other regions post ageing.

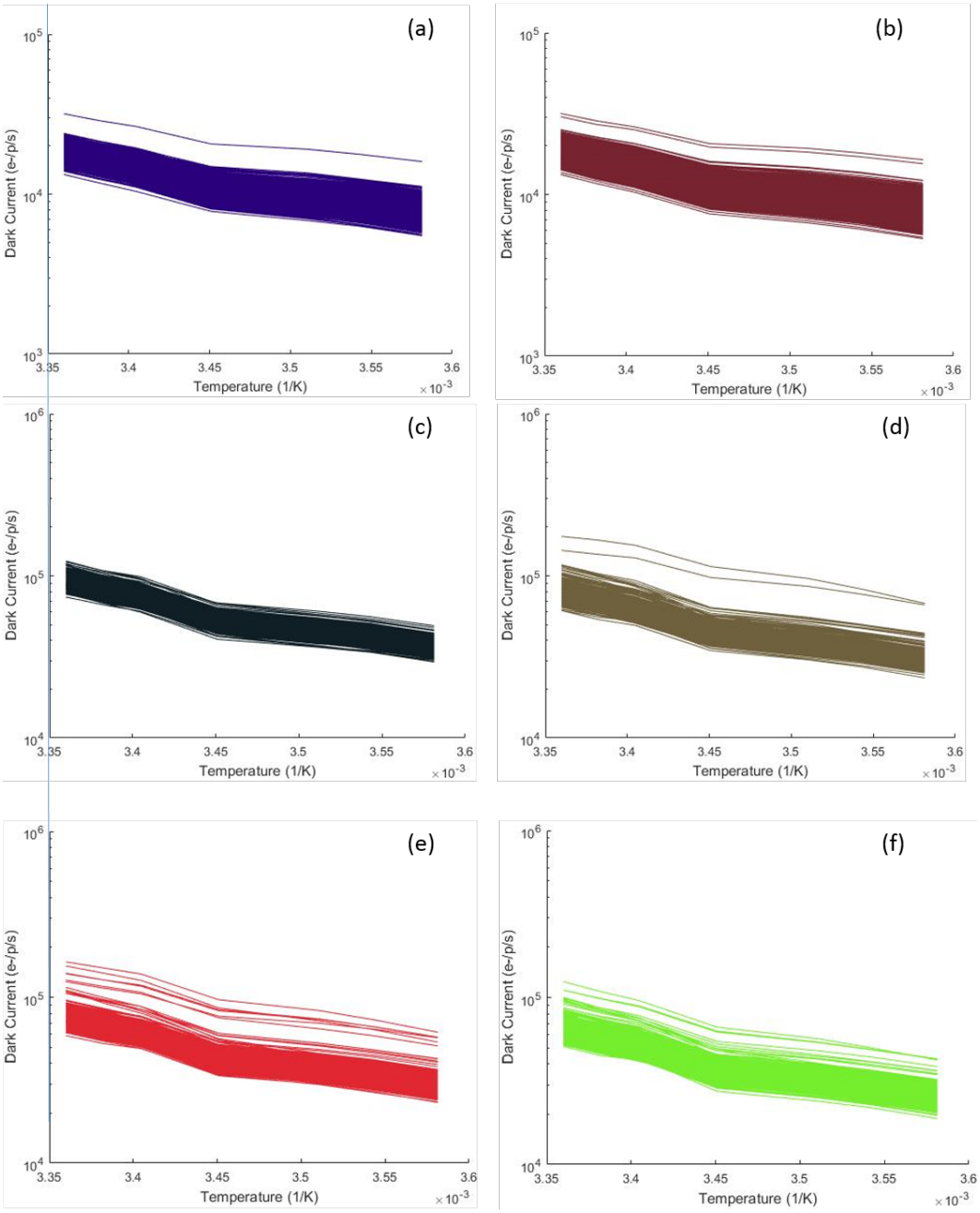

Figure 8.11: Arrhenius plot for each pixel as a function in the inverse temperature after ageing for 175 hours at 283±0.5 K: (a) Block 1, (b) Block 2, (c) Block 3, (d) Block 4, (e) Block 5 and (f) Block 6.

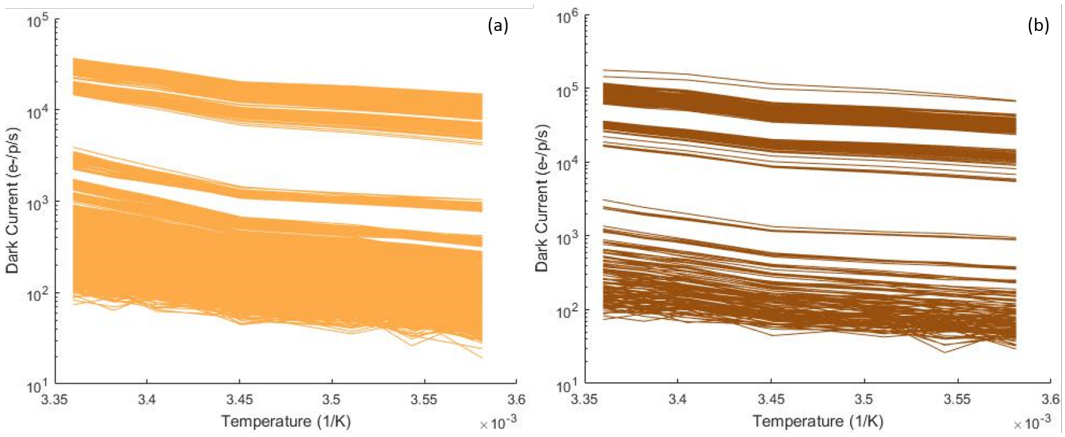

Figure 8.12: Arrhenius plot for each pixel for 175 hours at 283±0.5 K: (a) Block 7 and (b) Block 8.

Figures 8.11 (e) and (f) start to demonstrate the dark current becoming quantised. This quantisation becomes more exaggerated for Blocks 7 and 8, as demonstrated in Figure 8.12. Block 8 experiences the highest level of ageing, as described previously.

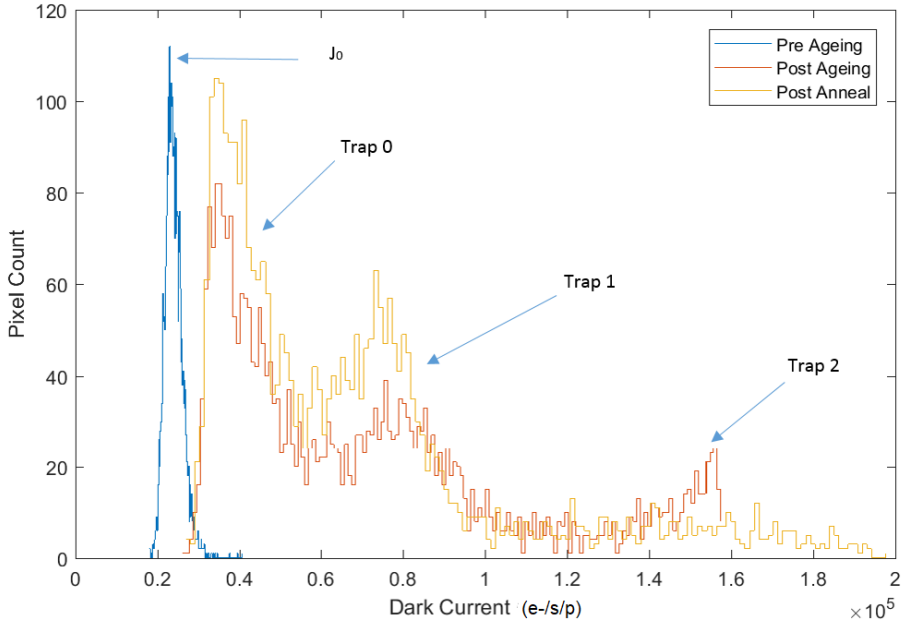

Figure 8.13: Histogram demonstrating the dark current pre and post ageing and post anneal for Block 8 at 283±0.5 K.

Figure 8.13 demonstrates the dark current before and after ageing and after the annealing of the EMTC1_C5 for Block 8. The histograms were taken at 303 K and 0.1 s integration time. Under these conditions, the pre ageing histogram appears narrow, whereas the histograms post ageing and anneal have a long tail similar to that seen in the proton irradiated device in Chapter 7 and previously reported after other irradiations. By plotting the dark current as a histogram at a higher temperature, it is possible to determine the quantised dark current. Each peak can be attributed to a trap or trap cluster. Figure 8.13 demonstrates the dark current after ageing and has three distinct peaks, labelled Trap 0, Trap 1 and Trap 2. J_0 refers to the dark current pre-irradiation. These peaks only appear after the device had been aged at a high potential, and considerable ageing is discernible. Figures 8.11 and 8.12 show the dark current for each block. The different blocks experienced increased ageing that can be attributed to the magnitude of their initial gain. For example, Blocks 5 and 6 experienced a maximum 2.84% and 2.94% gain per stage compared to the 2.57% experienced by Block 3. It is apparent that at higher gains, the dark current becomes more quantised. This is most apparent in Figure 8.12 where the dark current quantisation is shown to increase further. Traps 0, 1 and 2 appear only after ageing. Each of these peaks contains pixels which have a particular dark current value which results from the generation of a specific trap. Figure 8.8 demonstrates that the dark current increases as a power law towards the output. It can be hypothesised that those pixels with quantised dark current contain traps with higher activation energies, as a result of prolonged ageing. It is possible that these peaks can be attributed to pixels which contain multiple traps, either the same trap type or a combination of several different trap types, such that the dark current of pixels is a sum of the dark current from the multiple traps. The Arrhenius plot for the dark current for these traps can be seen in Figures 8.11 and 8.12. The activation energy was calculated using Equation 7.1. This equation was used in conjunction with the dark current.

It is also possible to determine the activation energy and capture cross-section, (σ), of these traps from the temperature dependence and equation [124]

$$\kappa(T) = \frac{n_i v \sigma}{\cosh((E_a - E_i)/kT)} \tag{8.3}$$

where κ(T) is the temperature dependent carrier generation rate, E_a is the activation energy, E_i is the silicon band-gap energy, v is the thermal velocity, and n_i is the intrinsic carrier concentration. Ultimately, the capture cross-section was not captured during this thesis due to inaccuracies in measuring the carrier generation rate.

Dark current spectroscopy studies the DC generation rate. The generation rates increase as the activation energy approach the mid-gap. Integration over a number of frames and statistical analysis of the pixels enables the observation of quantised dark current. Traps closest to E_i (8.3) produce the highest level of dark current; therefore it is possible to probe mostly deep level traps. This method can have a detection sensitivity below 10^9 traps/cm^3 [76].

Peak No.	Activation Energy (eV)
0	0.45±0.05
1	0.42±0.05
2	0.34±0.05

Table 8.6: Properties of the traps for the EMTC1_C5 aged at 283±0.5 K.

The energies denoted in Table 8.6 do align well with several deep level traps however due to the structure of the device (buried channel) and the charge transfer process it is unlikely that these deep level traps would be formed. Instead, due to the simulations completed in Chapter 6, it is possible to postulate the potential trap site location. As the impact ionisation region comes into contact with the interface traps can form from incident hot carriers. Subsequently, it is possible to hypothesise that the traps form in the interface and surface regions of the device. The exact nature of these traps is unknown. Charge pumping could provide further insight into cross-section and exact nature of the traps.

However, there are a number of possible traps that could align with these energies. Surface damage introduces oxide charges at the Si-SiO_2 interface. Defects have been reported at these energy levels; however, without the known cross-sections, it can be difficult to know the explicit nature of the

trap. Consensus exists for traps existing at these energy levels [135, 79, 45], including evidence for a hole trap in the Si-SiO_2 interface at 0.36 eV [135]. MOS devices are known to have dominant trappings centres at P_{b0} and P_{b1} centres [81]. While many sources claim these have correlation energies in the range of 0.6-0.7 eV [81, 15], several have now concluded that the P_b1 could have a lower energy level than previously thought. The energy level could be in the range of 0.3-0.4 eV [81]. This could correlate to the trap centres seen in Figure 8.13. These interface defects are known to be dependent upon several factors, including manufacture conditions and device history. However, they are not yet known to be induced by ageing. Furthermore, several sources have simulated the impact of these traps on CTI and shown that these traps remain populated after the original signal packet has been transferred [80]. Subsequently, it can be concluded that if P_b1 was a dominate ageing induced trap, an effect would have been seen in Figure 8.7.

While the exact nature of the traps is not known, it is possible to see that the traps anneal. The device was room temperature annealed to gain further insight into the nature of these traps. EMTC1_C5 was annealed in ambient room pressure and temperature for ten months. The effect of this anneal is also seen in Figure 8.13. Trap 2 anneals at room temperature; however, the populations of Traps 0 and 1 can be seen to increase in size, and there is a small decrease in the dark current. The nature of these traps is still not understood; however, this demonstrates that it is possible to anneal EM ageing.

8.6 Causes of Ageing

The processes described in Chapter 8.3 concerning hot carrier charge injection focus on the impact of ageing in MOSFET devices; however, the processes are comparative. It has long been proposed that the ageing phenomenon could be attributed to hot electrons entering the oxide after acceleration through the electric fields in a manner similar to CHE and SHE. In both cases, the high electric field is sufficient to drive the electrons into the gate oxide where traps can form. However, this hypothesis does not consider where in the gate oxide

the charge is becoming trapped nor considers the excited holes also produced in the impact ionisation process. As shown in Figure 6.2, the charge shifts towards the interface and the point of maximum potential moves closer towards surface and increases in magnitude. Furthermore, holes can also undergo hot carrier injection, and several models have been developed by Teledyne e2v studying the impact of hot holes in the ageing process [30]. Holes also increase in density beneath the DC gate, which could also lead to traps forming. It is important to note that a high electric field can lead to a saturation of the drift velocity as the charge density increases resulting in a distortion of the electric field [42] closest to the positive electrode and a reduction in the field nearest to the negative electrode. However, this reduction would likely result in a temporary decrease in the EM gain and not the prolonged damage that results in ageing. In an EMCCD, the DC gate is negative relative to the far more positive HV gate. The region close to the DC gate can be an abundant source of holes which undergo a backward acceleration towards the gate interface and oxide. These holes are accelerated at high energies but have relatively low mobilities when compared to electrons. The energetic holes can enter the Si-SiO_2 interface. In a traditional EMCCD, this could also include the interface between the silicon-oxide and silicon-nitride (SiO_2-Si_3Ni_4). There is considerable work that has demonstrated that holes and electrons can directly interact with the oxide [136]. Furthermore, holes can be trapped via a two-stage process in the oxide and the interface before recombining to form interface states [134, 137].

For these holes or electrons to become trapped in either location, the charge traps must either already exist due to traps induced during the fabrication process or due to damage inflicted on the device, such as radiation or hot carrier damage. Some insight into the type of damage induced by the ageing process has been provided by the dark current spectroscopy. It is apparent that a number of traps are developing during the ageing process, and through dark current spectroscopy, it has been possible to identify a number of these traps and their concentrations. However, the exact nature of these traps remains unknown. Due to the energy levels, several traps have been proposed. However, this subject requires more time to explore the nature of these traps and determine if these traps would be seen in normal CCDs. It is possible

for these traps to be annealed over time and further study into the annealing process should provide further insight into the lifespan of EMCCDs.

It is possible to gain insight into the ageing process by comparing with the results gained from the proton irradiation. Post irradiation a significant increase in the CTI was noted which was not mirrored in the aged devices. Subsequently, it is possible to see that proton induced damage leads to bulk damage, while the ageing process leads to an increase in surface trapping. Finally, it is important to discuss the structure of the EMCCD pixel. Though it is apparent that Blocks 7 and 8 experience a higher level of ageing at high signals, low signals showed limited variation between the blocks. However, simulations have demonstrated that changing the gate length can shift the location of the impact region and charge carrier concentration resulting in the charge interacting with the interface. Further study into the impact of the new gate structure is required, however it important to remember that the EM gain seen in EMTC1 is significantly lower than that seen in many commercial EMCCDs [25, 31].

8.7 Conclusion

The structure of the EMTC1 is unique, lacking a Si_3N_4 layer commonly seen in EMCCDs and has a very thin gate oxide. Many papers including those referenced in this thesis have hypothesised that the ageing process can be attributed to traps formed in the Si_3N_4 layer and a traditionally thicker gate oxide [107]. Damage within these regions has been attributed to the hot charge carriers produced by the impact ionisation process. Without these characteristics, it was hypothesised that there would be negligible ageing in the EMTC1, which has a gate oxide only 10 nm thick. This chapter has demonstrated that the EMTC1 not only ages but experiences ageing dependent on a number of different factors.

These results have then been compared with the ageing experienced by Te2v EMCCDs [31, 115]. Due to the thin gate oxide, the P2HV voltage cannot exceed 15.0 V. Most traditional EMCCD devices require a voltage exceeding 40 V to achieve a detectable EM gain due to the gate dielectric

being $\sim$ 20 times thicker. It has been demonstrated in this chapter that the damaging impact which can occur increases as a function of the measurement P2HV voltage. The increased ageing experienced by EMCCDs can be partially attributed to high potential leading to high gain, large charge packets and subsequent device saturation. During a period of high potential there is an increase in the concentration of hot charge carriers, to which the majority of the traps can be attributed. Even considering these factors, it is apparent that the EMTC1 does not suffer ageing to the same magnitude seen in other EMCCD sensors ageing with a maximum rate equivalent to a loss of gain of 0.0097% per hour.

Ageing is minimised when the device is operated at low EM potentials and low signal resulting in smaller charge packets. Furthermore, it has been demonstrated that the damage can be partially annealed at room temperature. This annealing provides insight into the lifespan of an EMCCD and the traps formed during the ageing process. Thermal annealing (at 373 K) may further anneal traps which have not yet been annealed at room temperature.

Chapter 9

Future Work and Conclusions

9.1 Future Work

This thesis has focused on the testing and modelling of a recently invented EM image sensor. This new technology has been thoroughly examined; however, there is still a substantial amount of work to be completed in this area.

9.1.1 EM-in-CMOS Technology

Firstly, it is important to consider that the EMTC1 device considered here is engineering grade and consists of 8 different pixel designs. It would be beneficial for full devices of each EM gate structure to be produced as this would improve the statistics of characterisation.

9.1.2 Novel EMCCD Pixel Structures

Among the two novel EM gate structures presented in this thesis, a number of other pixel designs were also patented [119]. While several of the proposed designs would be difficult to fabricate, some provide further insight into the

charge transfer process. This testing could be beneficial not only for EMCMOS devices but also for traditional EMCCDs.

Furthermore, it would provide an interesting contrast if a device was developed in a traditional CCD process as well as in CMOS. A comparison could be made between the impact of the CMOS process on the EM pixel structure and the subsequent charge transfer process and EM gain.

9.1.3 Damage Effects in the EMTC1

This thesis has presented the study of the effects of high energy protons on device operation and lifespan; however, due to time and budget restraints, this was limited to one proton energy, and it was not possible to show the effects of increasing proton energy. Furthermore, it is important to remember that the radiation environment is not limited to high energy protons but can include neutrons, gammas and high energy electrons, some of which can be produced as secondary particles due to interactions with the spacecraft. Irradiating the device with gammas and electrons would enable a complete comparison with other EMCCDs and CMOS image sensors.

As discussed in chapter 8, the EMCCD is affected by damage induced by high energy particles and experiences gain ageing attributed to hot carrier damage. This thesis has proposed several ideas concerning the ageing process in the EMTC1 pertaining to the cause and nature of the traps produced from hot carriers. While a number of theories pertaining to the effect of the new gates in the ageing process have been discussed, it is difficult to separate the impact of the novel gate structures from the effect of the operating an EMCCD in a CMOS process, e.g. at a lower voltage and without a nitride layer. As such, to provide a clearer understanding of the physical processes, implementing the novel EM gate structures in a traditional EMCCD process could provide more data and potential insight into the effect of the CMOS process.

9.2 Conclusions

9.2.1 Device Characterisation

The thorough initial characterisation of the Electron Multiplying Test Chip 1 has demonstrated that the new chip can achieve an EM gain that exceeds many modern image sensors by at least 100 %. The results derived from experimental characterisation demonstrate that there is considerably higher dark current and charge transfer inefficiency than in many CCDs. The high CTI can, in part, be attributed to a large number of defects within each sensor. These defects have been determined to be sources of dark current and CTI and accredited to the fabrication process. Future iterations of these devices would ideally be manufactured such that the number of defects is reduced. Furthermore, an improved cooling system would allow for the device to be cooled sufficiently for dark current to be suppressed.

9.2.2 Device Damage

The focus of the two major areas in this research has been the radiation damage effects from proton irradiation and from prolonged operation at high voltages leading to gain ageing. It is apparent from the results that the EMTC1 experienced damage in a manner similar to other devices. It had been hoped that there would be no ageing due to the absence of the nitride layer in the EMTC1. However, the results demonstrated that though the effect of ageing is greatly reduced, it is not eliminated. This indicates that though there is a certain amount of ageing in EMCCDs that can be attributed to hot carriers trapping in the nitride layer, a large quantity can be attributed to other sources. It has been determined through experimental testing that the ageing within the EMTC1 can largely be attributed to trapping of hot carriers accelerated beneath the DC gate result in a gradual decrease in storage capacity and subsequently size of the charge packet and a reduction in the strength of the electric field. It can thus be theorised that the source of ageing in EMCCDs cannot solely be attributed to the nitride layer. However, as ageing does still occur within the EMTC1, there are other sources of ageing.

It is also important to note that it has been determined that by annealing the device after it has experienced ageing it is possible to partially recover the EM gain. The device was tested repeatedly over a long time period, and the EM gain and dark current were shown to improve gradually under room temperature annealing.

9.2.3 EMCMOS: A viable option?

This device is a prototype to demonstrate the potential of two newly designed gate structures and provide a comparison of an EMCCD in a CMOS process with commercial EMCCDs. Results and simulations have demonstrated that the novel EM structures have produced an EM gain at least double (at room temperature) the gain per stage seen in modern scientific EMCCDs at a third of the applied high voltage. Optimisation and cryogenic operation further improve the gain and decreases the noise. Furthermore, the device has been demonstrated to have considerably reduced EM ageing and comparable radiation damage response. It is hoped that this device and the research presented in this thesis will be a stepping stone for the future development of this technology such that it will become a viable option for scientific low light imaging from Earth observation to industrial imaging.

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