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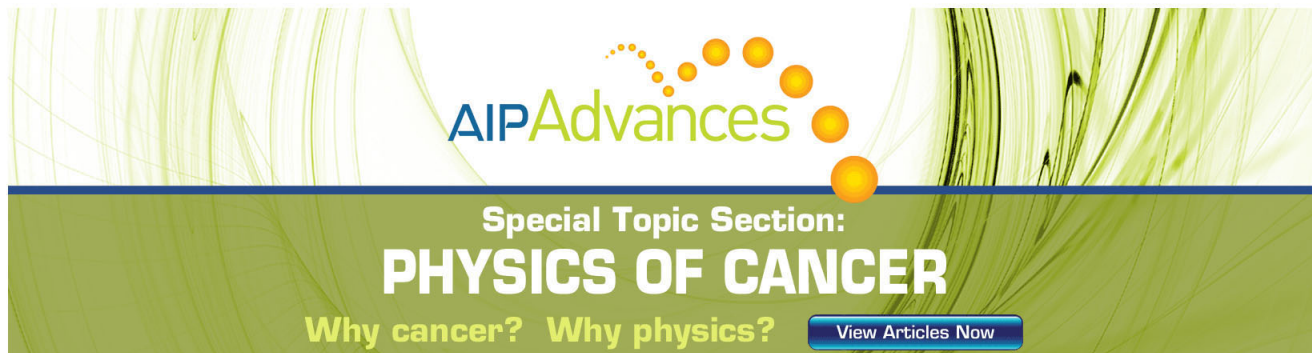
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Impacts of reduction of deep levels and surface passivation on carrier lifetimes in *p*-type 4H-SiC epilayers

T. Hayashi,[1,2,a)] K. Asano,[2] J. Suda,[1] and T. Kimoto[1]

[1]*Department of Electronic Science and Engineering, Kyoto University, Kyotodaigaku-katsura, Nishikyo, Kyoto 615-8510, Japan*

[2]*Power Engineering R&D Center, Kansai Electric Power Co., Inc. 3-11-20 Nakoji, Amagasaki, 661-0974, Japan*

Impacts of reduction of deep levels and surface passivation on carrier lifetimes in *p*-type 4H-SiC epilayers are investigated. The authors reported that the carrier lifetime in *n*-type epilayers increased by reduction of deep levels through thermal oxidation and thermal annealing. However, the carrier lifetimes in *p*-type epilayers were not significantly enhanced. In this study, in order to investigate the influence of surface passivation on the carrier lifetimes, the epilayer surface was passivated by different oxidation techniques. While the improvement of the carrier lifetime in *n*-type epilayers was small, the carrier lifetime in *p*-type epilayers were remarkably improved by appropriate surface passivation. For instance, the carrier lifetime was improved from 1.4 μs to 2.6 μs by passivation with deposited SiO_2 annealed in NO. From these results, it was revealed that surface recombination is a limiting factor of carrier lifetimes in *p*-type 4H-SiC epilayers. © *2011 American Institute of Physics*. [doi:10.1063/1.3583657]

I. INTRODUCTION

Silicon carbide (SiC) is an important material for development of high-power, high-temperature, and high-frequency devices, owing to its outstanding physical properties such as superior thermal stability, high breakdown field, and superior thermal conductivity.[1,2] High-voltage SiC devices, especially bipolar power devices, are suitable for high-power electrical conversion systems, where the material properties of SiC provide a significant advantage over those of conventional Si devices. In the case of high-voltage bipolar devices, a long carrier lifetime is required to modulate the conductivity of very thick voltage-blocking layers. If the carrier lifetime is short, however, conductivity modulation does not work effectively and low on-resistance cannot be attained.

The carrier lifetimes usually observed in SiC are still short, approximately 1 μs, in spite of the indirect band structure. Bergman *et al*. have shown that the small grain boundaries strongly affect the carrier lifetimes in SiC.[3] After the crystalline quality was improved, however, it turned out that there are other lifetime-killing defects besides the macro-structural defects. Tawara *et al*. have shown that the $Z_{1/2}$ and $EH_{6/7}$ centers influence the carrier lifetimes of 4H-SiC epilayers.[4] Klein *et al*. have reported that in the case of *n*-type 4H-SiC epilayers, there exists a relationship between the inverse of the carrier lifetimes and the concentration of $Z_{1/2}$ center (although the plotting range is within one order of magnitude).[5] Danno *et al*. have revealed the clear relation between the carrier lifetime and the $Z_{1/2}$ and/or $EH_{6/7}$ centers in the wide range of the trap concentration. They clarified that the carrier lifetimes are limited by the $Z_{1/2}$ and/or $EH_{6/7}$ centers. They also found that the carrier lifetimes are limited by other factors such as surface recombination when the $Z_{1/2}$ concentration is low enough.[6] Klein *et al*. and Reshanov *et al*. concluded that $EH_{6/7}$ cannot be a lifetime killer by comparing the DLTS spectra of a *pn* junction with and without minority-carrier injection.[5,7] More recently, a few groups attempted reduction of these deep levels and successfully improved carrier lifetimes. Storasta *et al*. have shown dramatic reduction of the concentration of the $Z_{1/2}$ center using carbon ion implantation combined with subsequent diffusion by high-temperature annealing.[8] Hiyoshi *et al*. have also shown elimination of these centers by thermal oxidation.[9] Thus far, the lifetime killers of *n*-type SiC have been analyzed systematically,[10,11] and long lifetimes of 9–18 μs have been achieved.[12,13]

However, these beneficial results have mainly addressed *n*-type 4H-SiC, and there have been very few reports on the carrier lifetimes in thick and lightly doped *p*-type SiC, which is often employed as the voltage-blocking region of high-voltage SiC switching devices such as thyristors[14] and IGBTs.[15] Therefore, the authors have investigated the factors affecting the carrier lifetimes in both *p*-type and *n*-type 4H-SiC epilayers, for example, the dependence of carrier lifetime on temperature and injection level.[16] As for the deep centers, the $Z_{1/2}$ center has been identified as the lifetime killer in *n*-type SiC, as mentioned above. On the other hand, the lifetime killer in *p*-type SiC has not yet been clarified. In an attempt to clarify the lifetime killer in *p*-type SiC, the authors investigate the impacts of reduction of deep levels and surface passivation in both *p*-type and *n*-type 4H-SiC epilayers. As a result, it turned out that the carrier lifetime in *p*-type SiC is severely affected by surface passivation. The authors succeeded in the lifetime enhancement in *p*-type 4H-SiC by improved surface passivation.
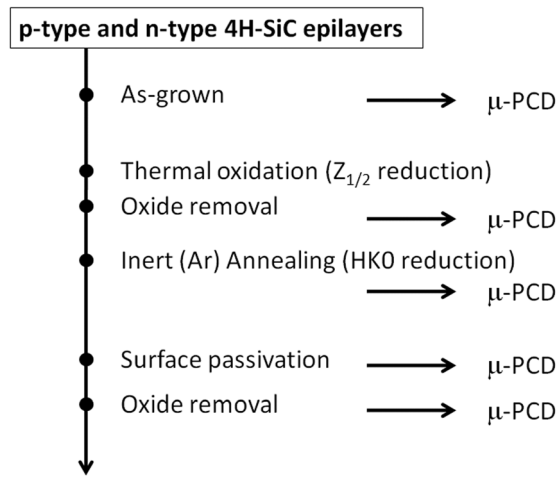
a)Electronic mail: hayashi@semicon.kuee.kyoto-u.ac.jp.

p-type and n-type 4H-SiC epilayers

As-grown ⟶ μ-PCD

Thermal oxidation ($Z_{1/2}$ reduction)
Oxide removal ⟶ μ-PCD

Inert (Ar) Annealing (HK0 reduction) ⟶ μ-PCD

Surface passivation ⟶ μ-PCD
Oxide removal ⟶ μ-PCD

FIG. 1. Experimental procedure to investigate impacts of various treatments on carrier lifetimes in 4H-SiC.

II. EXPERIMENT

In this study, the carrier lifetimes of *p*-type and *n*-type 4H-SiC epilayers were estimated by employing a microwave photoconductance decay (μ-PCD) method. The samples used in this study were nitrogen-doped *n*-type and aluminum-doped *p*-type epilayers grown on 8° off-axis 4H-SiC (0001) substrates by chemical vapor deposition (CVD). The thickness of both epilayers was 50 μm, and the doping concentration was 9×10^{14} cm^{-3} for the *p*-type epilayer and 1.2×10^{15} cm^{-3} for the *n*-type epilayer.

The μ-PCD method used in this study allows for contactless estimation of carrier lifetime, and the lifetimes of the whole wafer (mapping) can be easily measured. In this measurement, excess carriers were generated by a pulsed YLF (yttrium lithium fluoride)-3HG laser of 349 nm wavelength. Decay of electrical conductivity (which is proportional to the excess carrier concentration) was monitored with microwave reflectivity at a frequency of 26 GHz. This method has been employed as a standard technique for measurement of the lifetimes of Si.[17] In order to increase the signal-to-noise ratio of μ-PCD signals, a differential μ-PCD method was used in this study; this method relies on the mechanism of a difference in microwave reflectivity from areas with and without laser illumination.
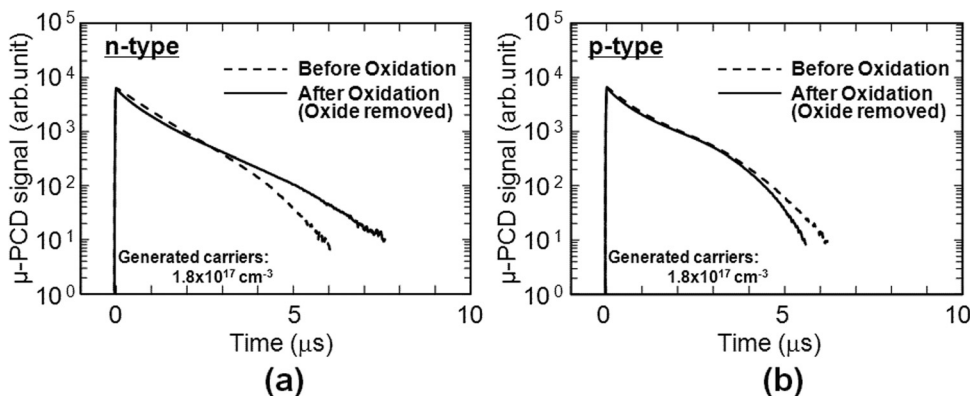
Effects of decrease in deep levels and surface passivation on carrier lifetimes were compared, including the as-grown epitaxial wafers, by applying this differential μ-PCD method. The experimental procedure is illustrated in Fig. 1. A thermal oxidation treatment processed at 1300°C for 5 h aimed at reduction of deep levels.[9] After this thermal oxidation, the surface oxide film was removed by hydrofluoric acid, and then the carrier lifetime was measured. High-temperature annealing was performed in Ar atmosphere at 1550 °C for 30 mins after forming a carbon cap on the substrate surface to reduce the HK0 center, which is generated by thermal oxidation.[18] Dry oxide, N$_2$O-grown oxide,[19,20] and deposited SiO$_2$ followed by NO annealing[21,22] were used as surface passivation.

III. RESULTS

A. Impact of deep-level reduction

At first, the authors evaluated the influence of the $Z_{1/2}$ center reduction by thermal oxidation processing on carrier lifetimes of 4H-SiC. The $Z_{1/2}$ center, which is energetically located at 0.65 eV below the conduction bandedge,[23] is a prime lifetime killer in *n*-type 4H-SiC epilayers. The authors' group reported that the $Z_{1/2}$ center of *n*-type 4H-SiC is eliminated by thermal oxidation as described above.[9] Carrier lifetimes at the same location on the same wafer and at the same excitation intensity were measured before and after the thermal oxidation process where the surface oxide was removed after the oxidation by hydrofluoric acid. Comparison of the μ-PCD decay curves at RT before and after thermal oxidation is shown in Fig. 2 for (a) *n*-type and (b) *p*-type epilayers. In each figure, the dashed line shows the decay curve before the thermal oxidation, and the solid line after the oxidation process including oxide removal. For these decay curves, the generated carrier density by the excitation laser is both 1.8×10^{17} cm^{-3}. From these figures, the improvement of a carrier lifetime was confirmed in *n*-type SiC as expected. However, obvious improvement of a carrier lifetime was not found in the *p*-type epilayer. Although no direct evidence has been given, it may be reasonable to assume that the $Z_{1/2}$ center also exists in p-type SiC. The charge state of the defect will be different because the Fermi level is different between *p*-type and *n*-type SiC. Given that the $Z_{1/2}$ center in *p*-type 4H-SiC is reduced by thermal
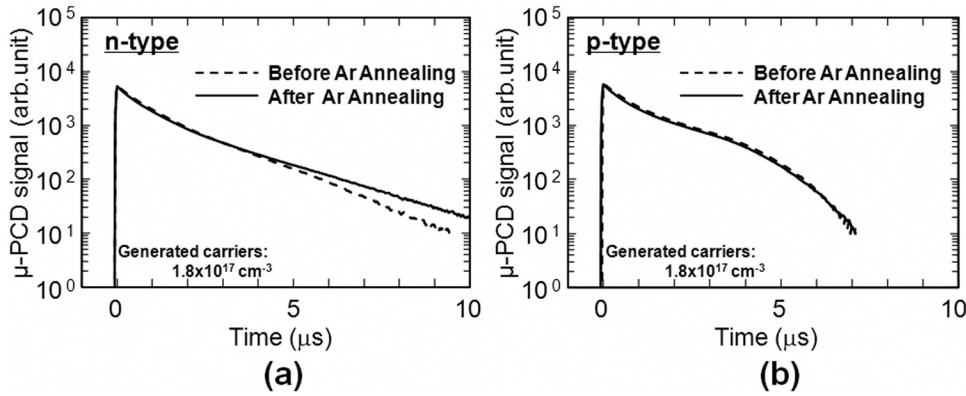
FIG. 2. μ-PCD decay curves before and after thermal oxidation process (at 1300 °C for 5 h followed by oxide removal) for 50-μm-thick (a) *n*-type and (b) *p*-type 4H-SiC epilayers. The generated carrier density is 1.8×10^{17} cm^{-3}.

FIG. 3. μ-PCD decay curves before and after high-temperature Ar annealing (at 1550 °C for 30 min) for 50-μm-thick (a) *n*-type and (b) *p*-type 4H-SiC epilayers. The generated carrier density is 1.8×10^{17} cm^{-3}.

oxidation, the present result suggests that a lifetime killer other than the $Z_{1/2}$ center works for *p*-type 4H-SiC.

While the $Z_{1/2}$ center can be reduced by thermal oxidation, the HK0 center, which is energetically located at 0.78 eV above the valence bandedge,[24] is generated at the same time. The authors' group reported the HK0 annihilation by inert (Ar) annealing at high temperature.[18] To investigate the impact of the HK0 center on carrier lifetimes, the authors performed the μ-PCD measurements before and after this high-temperature annealing. Figure 3 depicts the comparison of the μ-PCD decay curves at RT for (a) *n*-type and (b) *p*-type 4H-SiC epilayers before and after this high-temperature annealing. In each figure, the dashed line shows the decay curve before the annealing, and the solid line after the annealing. For these decay curves, the generated carrier density is also 1.8×10^{17} cm^{-3}. From these figures (as with the case of the $Z_{1/2}$ center reduction) the carrier lifetime in *n*-type SiC became longer, while the lifetime in *p*-type SiC hardly changed. Therefore, it also seems that a lifetime killer other than the HK0 center works in *p*-type 4H-SiC.

B. Impact of surface passivation

In spite of reduction of the $Z_{1/2}$ and HK0 centers, the carrier lifetime in the *p*-type epilayer was not improved. Thus, the influence of surface passivation on carrier lifetimes was investigated for both types of epilayers. Various surface passivations are tried on the same samples. The detailed conditions of surface passivations employed in this study are summarized in Table I. Comparison of the μ-PCD decay curves for various surface passivations are shown in Fig. 4 for (a) *n*-type and (b) *p*-type 4H-SiC epilayers. In each figure, the dashed line shows the μ-PCD decay curve before surface passivation, the solid line shows that for the sample passivated with a dry oxide, and the dashed-dotted line

TABLE I. Employed surface passivation and its experimental conditions.

Surface Passivation	Experimental Conditions
Dry O_2-Grown Oxide	100% O_2 @ 1150°C-5min
N_2O-Grown Oxide	10% N_2O (diluted by N_2) @ 1300°C-10min
Deposited SiO_2 Annealed in NO	PECVD @ 400°C-7 min $\rightarrow$ 10% NO (diluted by N_2) @ 1300°C-30 min

shows that with deposited SiO_2 annealed in NO, respectively. For these decay curves, the generated carrier density is also 1.8×10^{17} cm^{-3}. From these figures, unlike the case of the deep-level reduction, a remarkable change was confirmed for the *p*-type epilayer while the change of the *n*-type epilayer was small. In the case of dry oxidation as the passivation, the carrier lifetime for the *p*-type epilayer decreased drastically. Therefore, the dry oxide may give a high surface recombination velocity for the *p*-type 4H-SiC. On the other hand, in the case of deposited SiO_2 with NO annealing, the carrier lifetime for *p*-type epilayer was significantly enhanced, indicating that the surface recombination may be suppressed. From these results, it seems that the carrier lifetimes in *p*-type SiC are strongly influenced by surface passivation.

IV. DISCUSSION

In order to clarify the effect of surface passivation, an influence of oxide removal on the carrier lifetime in the *p*-type epilayer was investigated. After the carrier lifetime measurement for each passivation process described above, the surface passivation layer (oxide) was removed by acid etching, and a carrier lifetime was measured again on the same region of the epilayer. Comparison of the μ-PCD decay curves before passivation, after passivation, and after oxide removal for the *p*-type epilayer are shown in Fig. 5. In this figure, the dashed line shows the decay curve before the passivation, the solid line shows that with deposited SiO_2 annealed in NO, and the dashed-dotted line shows that after oxide removal. The decay curves for a generated carrier density of 1.6×10^{15} cm^{-3} and 1.8×10^{17} cm^{-3} are shown. As shown earlier, the carrier lifetime increased by surface passivation with the deposited SiO_2. When this oxide was removed, the carrier lifetime of the *p*-type epilayer decreased back to that before the surface passivation, as shown in this figure. In the case of dry oxide, the decay curve was also recovered to that before the passivation by oxide removal (not shown). Consequently, it can be concluded that these lifetime changes arise from effect of surface passivation.

In order to discuss the influence of the surface passivation for *p*-type SiC in more detail, the interface state density of the SiO_2/SiC structures for each oxidation is compared with the carrier lifetimes. Figure 6 shows the interface state
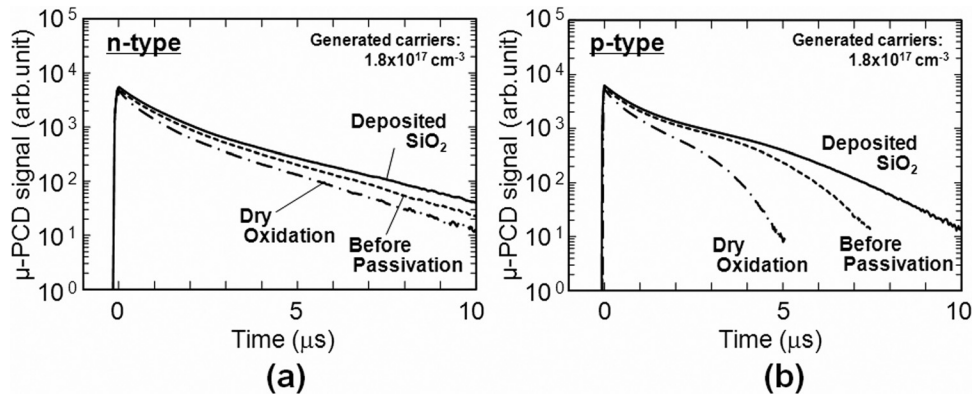
FIG. 4. Comparison of the μ-PCD decay curves for various surface passivations for 50-μm-thick (a) *n*-type and (b) *p*-type 4H-SiC epilayers. The generated carrier density is 1.8×10^{17} cm^{-3}.

density (D_{it}) near the conduction and valence band edges for each oxidation.[22,25] The interface state density was investigated by preparing metal–oxide–semiconductor (MOS) capacitors on both *n*-type and *p*-type 4H-SiC(0001) epilayers. Simultaneous high-frequency (100 kHz) and quasi-static capacitance–voltage measurements were performed on MOS capacitors, and the interface state density was extracted by the high-low method. The interface state density near the band edges strongly depends on the oxide formation process. For example, the D_{it} value at $E_C - 0.2$ eV is 4×10^{12} cm^{-2}eV^{-1} for dry oxide, 2×10^{12} cm^{-2}eV^{-1} for N$_2$O-grown oxide, and 2×10^{11} cm^{-2}eV^{-1} for deposited SiO$_2$ annealed in NO. The carrier lifetime of the *p*-type epilayer changed in the following process order: as-grown (1.5 μs), passivation with dry oxide (1.4 μs), N$_2$O-grown oxide (2.1 μs), and deposited SiO$_2$ annealed in NO (2.6 μs) at the generated carrier density of 4×10^{15} cm^{-3}. This comparison is summarized in Table II. From this result, a tendency of carrier lifetimes for each surface passivation is consistent with the change of interface state density for different passivation techniques. This may be the reason why the surface recombination was reduced, and thereby the longer lifetime was achieved, when the surface was passivated with the deposited oxide annealed in NO.
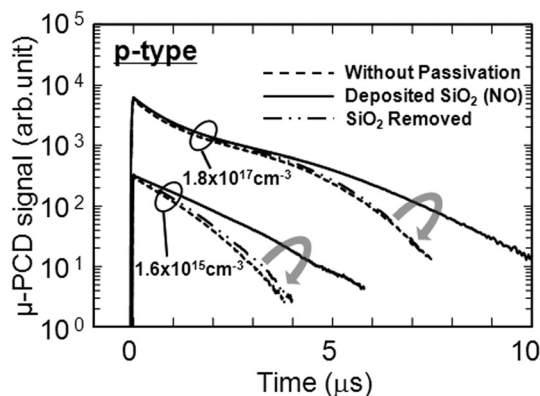
In the case of the present *p*-type 50 μm-thick epilayer, the carrier lifetime has not been improved very much after the two-step thermal treatment, by which the $Z_{1/2}$ center and HK0 center are almost eliminated. However, the carrier lifetime has been enhanced by surface passivation. From the result, deep levels eliminated by two-step thermal treatment are not major lifetime killers, and the surface recombination is a major limiting factor of the lifetime in the *p*-type epilayer. In the case of *n*-type 4H-SiC epilayer, the maximum carrier lifetime is limited at about 2–3 μs even after the two-step thermal treatment, as far as the epilayer thickness is 50 μm.[12] The measured carrier lifetime increases with increasing the epilayer thickness, when the deep level concentrations are low. The authors reported that recombination in the substrate or near the epilayer/substrate interface severely limits the measured carrier lifetime when the epilayer are not thick enough.[12,26] Miyazawa *et al.* experimentally demonstrated the impacts of substrate recombination by repeating the backside polishing and lifetime measutrements.[13] In the present 50 μm-thick *p*-type epilayer, it may be reasonable that the obtained lifetimes of about 2 μs is also limited by significant influence of recombination in a substrate. At
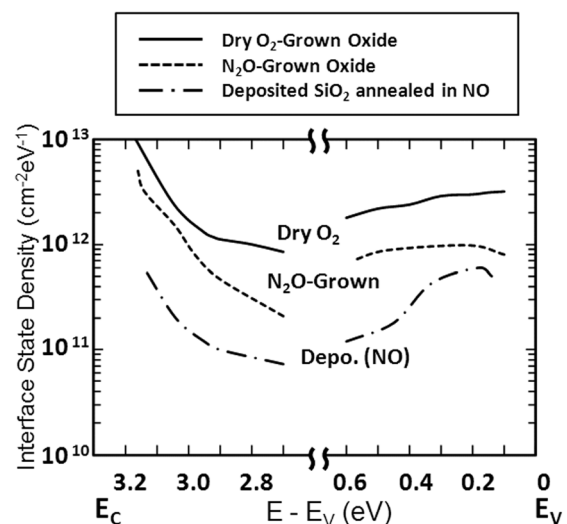

FIG. 5. μ-PCD decay curves before and after surface passivation, and after removing the passivation layer for a 50 μm-thick *p*-type 4H-SiC epilayer. The surface was passivated with deposited SiO$_2$ annealed in NO. The decay curves for generated carrier density of 1.6×10^{15} cm^{-3} and 1.8×10^{17} cm^{-3} are shown.

FIG. 6. Interface state densities of SiO$_2$/4H-SiC(0001) near the valence and conduction band edges. The solid line refers to dry O$_2$-grown oxides, the dashed line refers to N$_2$O-grown oxide, the chain dashed line refers to deposited SiO$_2$ annealed in NO as Refs. 22 and 25.

TABLE II. Comparison of carrier lifetimes in 50μm-thick p-type epilayers and the interface state density (D_{it}) at $E_V + 0.2$ eV and $E_C - 0.2$ eV, for various surface passivations on the 4H-SiC (0001).

Surface Passivation	τ (p-type) (μs)	D_{it} at $E_C - 0.2$ eV[a] (cm^{-2}eV^{-1})	D_{it} at $E_V + 0.2$ eV[a] (cm^{-2} eV^{-1})
(As-Grown)	1.5	−	−
Dry O$_2$-Grown Oxide	1.4	4×10^{12}	3×10^{12}
N$_2$O-Grown Oxide	2.1	2×10^{12}	9×10^{11}
Deposited SiO$_2$ Annealed in NO	2.6	2×10^{11}	6×10^{11}

[a]D_{it} values were adopted from Refs. 22 and 25.

present, it is not very clear why the surface recombination is more sever for p-type epilayers. Even if the distribution of surface state density is identical for n- and p-type epilayers, the direction of surface band bending is opposite, and the position of surface Fermi level must be different for n- and p-type epilayers. The quantitative evaluation of the surface recombination velocity is a subject of future study.

The decay curve in the high injection region seems to show a less effect of the surface passivation. The dependency of carrier lifetimes on the injection level for an as-grown epilayer and an epilayer passivated with the deposited SiO$_2$ annealed in NO is shown in Fig. 7. This figure clearly shows that improvement of carrier lifetimes became small in the high injection region. This phenomenon may be ascribed to the influence of carrier recombination in the substrate and the change in the recombination path at high carrier density. The epilayer thickness of 50 μm is thinner than the sum of penetration length of excited laser[27] ($\sim$30 μm) and the diffusion length of the generated carrier (more than 40 μm). The excess carriers generated in substrate naturally recombine well inside the substrate due to the very short lifetime in the substrate, and carriers may diffuse from the epilayer into the substrate through the interface, and disappear by recombination in the substrate.[12] In the high injection region, in particular, the carrier recombination in the substrate may be relatively pronounced, because of enhanced carrier diffusion to the substrate by increase of the carrier concentration gradient. Another reason is the change in recombination path at high carrier density. The maximum injection level near the epilayer surface reaches over 3×10^{17} cm^{-3}. At the extremely high-injection level, the carrier recombination

paths by the radiative recombination and the Auger recombination should be considered. The carrier lifetime limited by the radiative recombination and the Auger recombination at this injection level can be estimated to be about 3 μs and 30 μs, respectively, by using the radiative recombination coefficient of 1.5×10^{-12} cm^3/s[28] and Auger recombination coefficients of Cn as 5.0×10^{-31} cm^6/s and Cp as 2.0×10^{-31} cm^6/s.[29] Thus, the carrier lifetime at this high-injection level should be also influenced by radiative recombination significantly.

V. CONCLUSION

Impacts of reduction in deep levels and surface passivation on carrier lifetimes in 50 μm-thick p-type 4H-SiC epilayers have been investigated. Though the carrier lifetime in n-type epilayers has increased by reduction in deep levels through thermal oxidation and thermal annealing, the carrier lifetime in the p-type epilayer has not changed significantly. Several surface passivation processes have been performed on both p-type and n-type epilayers in order to investigate the influence of surface passivation on the carrier lifetime. Measurements have revealed that surface passivation results in a significant change in the carrier lifetime of p-type 4H-SiC. By using deposited SiO$_2$ annealed in NO, for instance, the carrier lifetime was improved from 1.4 μs to 2.6 μs. A tendency of carrier lifetimes for each surface passivation was consistent with the change in interface state density for different passivation techniques. Surface recombination is a limiting factor of carrier lifetimes for p-type 4H-SiC.

FIG. 7. Injection level dependencies of carrier lifetimes for 50-μm-thick p-type 4H-SiC epilayers before (as-grown) and after surface passivation with deposited SiO$_2$ annealed in NO.

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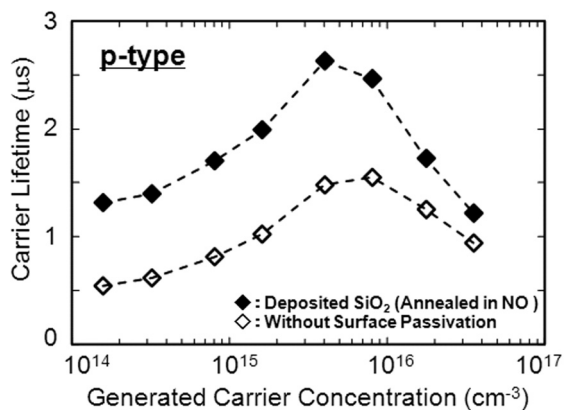
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