Title	Modeling of plasma-induced damage and its impacts on parameter variations in advanced electronic devices
Author(s)	Eriguchi, Koji; Takao, Yoshinori; Ono, Kouichi
Citation	Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (2011), 29(4)
Issue Date	2011-06
URL	http://hdl.handle.net/2433/141939
Right	© 2011 American Vacuum Society
Type	Journal Article
Textversion	publisher

Modeling of plasma-induced damage and its impacts on parameter variations in advanced electronic devices

Koji Eriguchi,[a] Yoshinori Takao, and Kouichi Ono
Department of Aeronautics and Astronautics, Graduate School of Engineering, Kyoto University, Yoshida-Honmachi, Sakyo-ku, Kyoto 606-8501, Japan

(Received 31 December 2010; accepted 6 May 2011; published 23 June 2011)

A comprehensive model predicting the effects of plasma-induced damage (PID) on parameter variations in advanced metal–oxide–semiconductor field-effect transistors (MOSFETs) is proposed. The model focuses on the silicon recess structure (Si loss) in the source/drain extension region formed by high-energy ion bombardment during plasma etching. The model includes the following mechanisms: (1) damaged layer formation by ion impact and penetration, (2) Si recess structure formation by a subsequent wet etch, (3) MOSFET performance degradation, and (4) MOSFET parameter variation. Based on a range theory for plasma-etch damage, the thickness of the damaged layer exhibits a power-law dependence on the energy of the ion incident on the surface of Si substrate. Assuming that the damaged layer was formed during a gate or an offset spacer etch process, the depth of Si recess (d_R) is a function of the depth profile of the created defect site (n_{dam}), the wet-etch stripping time (t_w), and the energy of the incident ion. It was found that d_R also showed a power-law dependence on the average ion energy $\bar{E}_{ion}$ estimated from applied self-dc-bias voltage for various t_w. As for MOSFET performance degradation, the threshold voltage (V_{th}) shifted and the shift (ΔV_{th}) increased with an increase in $\bar{E}_{ion}$ and a decrease in gate length. This induces an increase in subthreshold leakage current (I_{off}) for MOSFET. Technology computer-aided-design simulations were performed to confirm these results. By integrating the presented PID models, parameter variations could be predicted: Using a Monte Carlo method, it was demonstrated that PID increases parameter variations such as V_{th} and I_{off}. It also was found that the variation in $\bar{E}_{ion}$ induces V_{th} and I_{off} variations, comparable to that induced by other process parameter fluctuations such as dopant fluctuation and gate length. In summary, considering the effects of PID on parameter variations is vital for designing future ultralarge-scale-integrated circuits with billions of built-in MOSFETs.
 [DOI: 10.1116/1.3598382]

I. INTRODUCTION

Recently, plasma-induced damage (PID)[1] has been a crucial problem for controlling threshold voltage (V_{th})—a key parameter for operation of metal–oxide–semiconductor field-effect transistors (MOSFETs).[2–4] During plasma etching, ions are accelerated in the sheath between the plasma bulk and the device surface, and impacted on the material surface. This damage mechanism is usually referred to as physical damage. During a gate or an offset spacer etching, the ion-bombardment damage form a Si damaged layer in the source/drain extension (SDE) region of the MOSFET.[5–7] Various analyses have shown that the damaged layer was composed of displaced Si atoms, Si vacancy, and the interstitial atoms. On the basis of a range theory for PID,[8] the thickness of the damaged layer (d_{dam}) shows a power-law dependence on the average energy of ions from plasma ($\bar{E}_{ion}$), estimated from applied self-dc-bias voltage (V_{dc}) between a plasma and a device surface.[8,9] In practical device manufacturing processes, this damaged layer is removed by a subsequent wet-etch process, and the removed thickness defines the depth of Si loss (or Si recess) d_R.[5,6,9,10] This Si loss is a critical concern for future devices and should be suppressed to less than a nanometer thick,[7] because the resultant "Si recess structure" induces a device performance change such as a shift in V_{th} (ΔV_{th}).[4,9] An analytical expression was proposed for the relationship between the Si recess depth (d_R) and ΔV_{th} caused by PID,[11] suggesting a considerable increase in $|\Delta V_{th}|$ with the shrinkage of gate length (L_g). In terms of device performance, it is widely accepted that V_{th} is a key parameter which determines subthreshold leakage current.[12,13] Therefore, the ΔV_{th} by PID is thought to change subthreshold leakage current[12,13] (denoted as I_{off} in this paper), i.e., power consumption of a chip. The relationship between I_{off} and d_R ($\bar{E}_{ion}$) was predicted on the basis of the range theory for PID and ΔV_{th} by PID.[14] However, there have been few discussions clarifying the quantitative relationship between $\bar{E}_{ion}$ and ΔV_{th} (or I_{off}) for the wet-etch stripping process being considered.

Parameter variation has become a key concern in designing ultralarge-scale-integrated (ULSI) circuits where billions of MOSFETs are built in.[7,15–17] From a device technology perspective, the short-channel effect (SCE) induced by the shrinkage of L_g is regarded as one of the critical phenomena determining I_{off}.[12,18] Much effort has been devoted to suppressing the SCE in MOSFET design.[7] From a process technology perspective, in addition to dopant fluctuation in the channel region,[15,16,19] critical dimension control of L_g during gate patterning has been a crucial challenge in developing plasma etch processes. The fluctuation in L_g (σ_{Lg}) is found to

[a]Electronic mail: eriguchi@kuaero.kyoto-u.ac.jp

enhance V_{th} variation,[7] leading to a wider statistical distribution of I_{off}.[20–24] The V_{th} variation is crucial for designing low-operation-voltage devices in particular,[7] and >10 mV V_{th} variations have been reported for various process technologies.[17,19,21,22] Aggressively scaled MOSFETs beyond 32 nm node require the V_{th} variation to be suppressed to less than 10 mV.[7] Due to this requirement, there have been extensive studies on suppression of σ_{Lg},[7] line-edge roughness (LER),[19,25–27] and line-width roughness (LWR),[7,19,28] during gate-etch processes. These studies focused on controlling the reactions on material surfaces governed by plasma chemistry.

Based on the above-presented discussions on PID and parameter variations in MOSFETs, it also may be considered that PID enhances the V_{th} and I_{off} variations.[14] To estimate the effect of PID on these variations, it is crucial to structure a comprehensive (analytical) PID model combining the parameters $\bar{E}_{ion}$, d_R, L_g, ΔV_{th}, and I_{off}. Furthermore, correlating the plasma parameter $\bar{E}_{ion}$ to the device parameter I_{off} is quite useful. However, there have been few reports clarifying the direct relationship between the $\bar{E}_{ion}$ variation and the I_{off} variation. In this paper, we focus on Si recess formation by PID and a wet-etch process, and clarify the effects of PID on the device parameter variations. The relationship between $\bar{E}_{ion}$ and ΔV_{th} is investigated in detail in the context of a wet-etch removal of the damaged layer. Based on obtained analytical relationships and the probability density distribution functions of the parameters ($\bar{E}_{ion}$, ΔV_{th}, and I_{off}), we propose a new methodology predicting V_{th} and I_{off} variations directly from $\bar{E}_{ion}$ variation. Findings indicate that PID considerably increases V_{th} and I_{off} variations.

This paper is organized as follows: In Sec. II, we briefly review the PID mechanism (Si recess structure formation) and present a relationship between d_R and $\bar{E}_{ion}$. In Sec. III, we propose a model correlating $\bar{E}_{ion}$-variation to ΔV_{th} variation. In Sec. IV, we demonstrate how $\bar{E}_{ion}$ variation impacts V_{th} and I_{off} variations for various technology nodes. Section V contains closing remarks.

II. DAMAGED LAYER FORMATION MODELING

A. Si recess formation and PID parameters

Figures 1(a)–1(c) illustrate the PID mechanism for Si recess structure formation in the SDE region of a MOSFET during an offset spacer etch and a subsequent wet-etch process. Ion impacts on the Si surface with energy E_{ion} leasing the energy by a series of collisions, it creates the defect sites under the exposed surface, forming the damaged layer (Fig. 1(a)). In general, defect sites are referred to as displaced Si atoms, vacancies, and interstitials.[8,29,30] The profile of a defect site $n_{dam}(x)$ (x: distance from the surface) is dominantly determined by E_{ion} and the potential between Si and ion in the system.[31,32] After the plasma exposure, a portion of the damaged layer is stripped off by the wet-etch process. As a consequence, the Si recess structure is formed (Fig. 1(b)). The residual $n_{dam}(x)$ (not removed by the wet etch) increases the resistance in the SDE,[30] whereas MOSFETs with the Si recess structure suffer from a threshold voltage

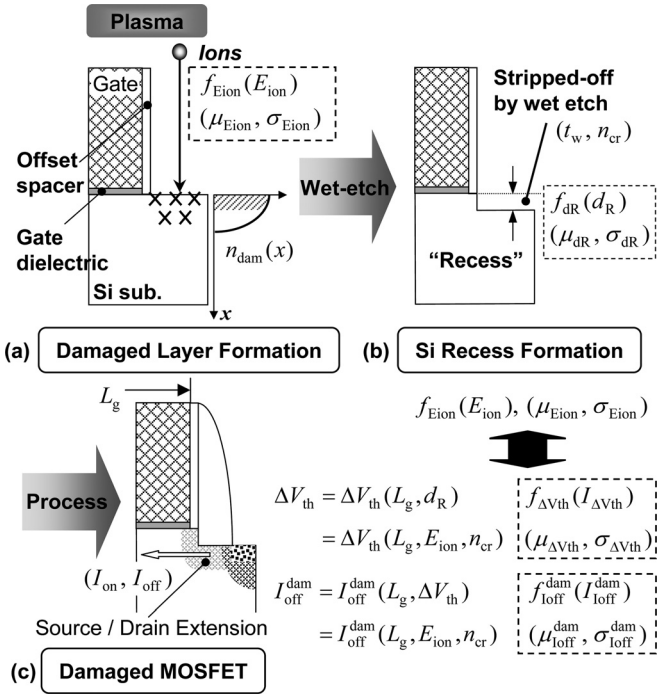

FIG. 1. Mechanisms of plasma-induced physical damage to Si substrate, Si recess structure formation, and the resultant device performance degradation. (a) High-energy ion bombardment on Si surface during plasma processing. This process creates a damaged layer underneath the Si surface. (b) A portion of the damaged layer is stripped off during a subsequent wet-etch process, resulting in Si recess structure. (c) MOSFETs with the Si recess structure suffer from the changes in threshold voltage (V_{th}), subthreshold leakage current (I_{off}), and drain current (I_{on}). (f_i is the probability density distribution function, where i stands for a parameter under consideration. The mean value and the variance of f_i are denoted as μ_i and $(\sigma_i)^2$, respectively. See the text for details.)

shift (ΔV_{th}) due to structural change in the region (Fig. 1(c)). In the case of n-channel (n-ch) MOSFETs, the I_d–V_g curves of damaged MOSFETs shift in the negative direction,[11] resulting in a decrease in V_{th} (ΔV_{th}), i.e., $V_{th}^{dam} = V_{th}^0 + \Delta V_{th}$, where V_{th}^{dam} and V_{th}^0 are the threshold voltages of the damaged and the control devices, respectively. The decrease in V_{th} induces an increase in an off-state leakage current I_{off}, usually referred to as subthreshold leakage current.[12]

In estimating the above-mentioned parameter variations, we define probability density distribution function (p.d.f.) and cumulative density distribution function (c.d.f.) as f_i and F_i, respectively,[33] where i stands for a parameter under consideration. The mean value and the variance (the squared standard deviation)[33] of f_i are denoted as μ_i and $(\sigma_i)^2$, respectively. For example, for d_R, we define f_{dR} and F_{dR} as the p.d.f. and the c.d.f, and μ_{dR} and $(\sigma_{dR})^2$, as the mean value and the variance, respectively (see Figs. 1(a)–1(c)). Details are discussed in the following sections.

B. Comparison between model and experiment

Based on a range theory for high-energy ion injection,[31] the projected range of ion (R_p) is determined from stopping power dependent on the energy of the incident ion (E_{ion}).[31,34,35] In a relatively low ion energy case (<1 keV),

the stopping power can be described by a universal form corresponding to a nuclear stopping mechanism.[36] In the case of the plasma etch process where E_{ion} is generally smaller than 1 keV, the stopping power is considered to exhibit a power-law dependence on E_{ion}. Based on a range theory for PID,[8] the damaged layer thickness (d_{dam}) is determined from E_{ion} as

$$d_{dam} = A(E_{ion})^{\alpha}, \quad (1)$$

where A and α are material- and process-dependent constants, which are functions of the masses and atomic numbers of the incident ion and target atom.[32,36] Damaged layer thickness is typically characterized by optical techniques such as spectroscopic ellipsometry,[6,37,38] as mentioned later in this paper. Note that d_{dam} depends on the detection limit of the analysis technique employed.[8] When Ar ion is projected to the Si substrate, a Moliere-type potential[36,39] is used, and A and α are calculated as 0.21 nm and 0.32, respectively.[8] Note also that based on discussion of the reduced energy and range,[32,34–36,40] parameter differences between substrates with Ar and other ions can be estimated with respect to the potential model. Moreover, it is worthy to note that the typical estimated projection range (R_p) is within approximately 10% between a silicon substrate and an amorphous SiO_2 layer usually formed on the Si substrate during manufacturing processes.[34,41] Therefore, parameters are deterministically characterized for a process under consideration. Details are described elsewhere.[8] For the purpose of simplicity, an Ar–plasma exposure is investigated in this study.

In conventional plasma etch equipment, an rf bias is applied to a wafer stage and the energy of the incident ion obeys an ion energy distribution function (IEDF) in response to a waveform of the applied bias voltage.[42–44] In general, an analytically derived IEDF is broad and bimodal,[42–47] i.e., it has two singular peaks (E_{min}, E_{max}) with a mean value of $(E_{min}+E_{max})/2$. In the case of low bias frequency when the ion transit time across the sheath is much shorter than the rf period (i.e., the ions cross the sheath in a small fraction of an rf cycle and respond to the instantaneous sheath voltage), the IEDF has a mean value of $\bar{E}_{ion}$ and a spectrum width of ΔE $(=(E_{max}-E_{min}))$, where E_{max} and E_{min} correspond to the maximum and minimum sheath voltage drop, accelerating ions from the plasma by assuming a collisionless sheath.[43,44,48] Thus, the incident ion energy ranges from 0 to $2\bar{E}_{ion}$ by eliminating a plasma potential. Typically, from PIC (particle-in-cell) simulations, this regime corresponds to a bias frequency of less than ~1 MHz, depending on various plasma parameters.[43] Alternatively, in the case of high bias frequency, the ions take many rf cycles to cross the sheath and can no longer respond to the instantaneous sheath voltage. Thus, the ions respond only to an average sheath voltage with a smaller spectrum width than observed at low bias frequencies. In the upper limits of bias frequency, the incident ion energy is $\bar{E}_{ion}$ for all ions (approximately monochromatic E_{ion}). This study focuses on the IEDF impacting the damaged layer formation, and therefore the transition (intermediate) frequency range is not in the scope of this paper. In the following, we discuss the effects of IEDF on d_{dam} or d_R for two extreme IEDF cases, i.e., low and high bias frequency limits.

First, we treated n-type (100) Si with 0.02 Ω cm by inductively coupled plasma (ICP) reactor.[9,38,49] Samples were exposed to an Ar plasma for 30 s. The source ICP power was 300 W and the pressure was 2.7 Pa. To fully understand the effects of IEDF on formation of the damaged layer, rf biases of 400 kHz and 13.56 MHz were applied to the wafer stage with power ranging from 0 to 150 W. (Although the 13.56-MHz case does not correspond to a high bias-frequency limit, one can investigate the effects of IEDF on formation of damaged layer.) These bias frequencies are related to high and low bias frequencies, respectively.[43] Plasma diagnostics were performed using a Langmuir probe and an oscilloscope. The V_{dc} and plasma potential (V_p) were determined to be <0 and ~11.0 V, respectively. The average ion energy $\bar{E}_{ion}$ is defined as $q(V_p - V_{dc})$, where q is the electronic charge. Note that this plasma configuration results in a constant ion flux (Γ_{ion}) to the Si substrate for all conditions ($\Gamma_{ion} \sim 5.0 \times 10^{16}$ cm^{-2} s^{-1}). After the plasma exposures, the surface damaged structures were analyzed by using spectroscopic ellipsometry with an optimized optical model proposed recently[50] (d_{dam} was identified using this technique). A three-layer model (surface SiO_2 layer/interfacial layer/Si substrate) was employed. Bruggeman Effective Medium Approximation was used to identify the thickness and the volume fraction of the interfacial layer.[51] The interfacial layer was assumed to be composed of c-Si and SiO_2.[11,37] Details for this analysis technique are published elsewhere.[50,52]

Figure 2 shows experimental results for the relationship between d_{dam} and $\bar{E}_{ion}$. The d_{dam} value was identified by spectroscopic ellipsometry and $\bar{E}_{ion}$ was estimated based on plasma diagnostics. From Fig. 2, the difference in d_{dam} at different bias frequencies is relatively small compared to the

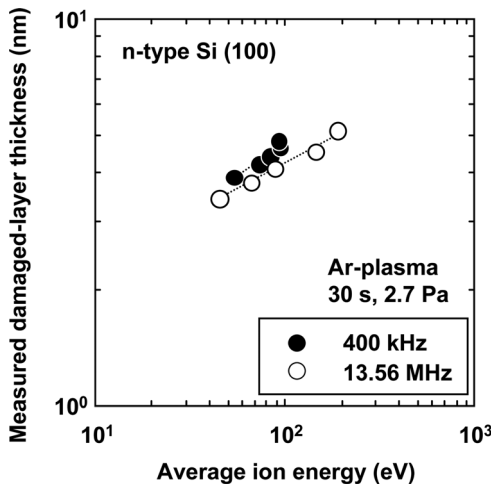

FIG. 2. Damaged layer thickness as a function of average ion energy determined from the average sheath voltage drop $q(V_p–V_{dc})$. The thickness was estimated by spectroscopic ellipsometry with an optimized optical model. Closed and open circles correspond to the applied bias frequencies of 400 kHz and 13.56 MHz, respectively.

E_{ion} effect. This indicates that the average ion energy $\bar{E}_{ion}$ is a useful measure for predicting PID under various rf-biases. Unless otherwise stated, $\bar{E}_{ion}$ is used as the primal measure in the following discussion. In Fig. 2, a power-law relationship is evident between d_{dam} and $\bar{E}_{ion}$ for both bias frequencies. Calculated power-law constants are 0.36 and 0.27 for 400 kHz and 13.56 MHz, respectively. The observed dependence agrees well with the range theory for PID (Ref. 8) and the model proposed previously.[14] Therefore, it may be assumed that the Si recess depth d_R exhibits a similar dependence on $\bar{E}_{ion}$ to d_{dam} for various bias frequencies, because d_R is considered to be strongly dependent on the resultant d_{dam}.

The effect of wet-etch removal on d_R has not been clearly discussed in previous reports.[8,11,14] Now we perform a model prediction for estimating d_R on the basis of the range theory for PID.[8] In order to identify the d_R in MOSFETs, we take into account the removal step of the damaged layer as illustrated in Figs. 1(a) and 1(b).

In general, a wet-etch process is utilized to remove surface contaminants after plasma etching. In a conventional wet-etch treatment, a highly selective process condition (Si, SiO_2, other contaminants) is employed. Thus, the wet-etch process removes the damaged layer, including defects whose concentrations are larger than a critical threshold. In this study we introduce n_{cr} (normalized by the total ion dosage from plasma) to define how much the defects are removed by the wet etch. For example, the criterion $n_{cr} = 10^{-2}$ means that the damaged layer including the region with more than 1% defect-site density is stripped off. Figure 3(a) displays the calculated depth profiles of $n_{dam}(x)dx$ for two extreme bias-frequency cases. The employed IEDFs (low and high bias-frequency limits) are determined in accordance with analytical expressions.[8] For a constant ion dose, d_R is a function of $\bar{E}_{ion}$ and n_{cr}. As observed, when n_{cr} is defined (the wet-etch depth is defined), the recess depth (d_R) can be estimated with respect to the bias frequency and $\bar{E}_{ion}$. Figure 3(b) shows the simulated d_R for critical values of $n_{cr} = 10^{-4}$ and 10^{-2}, a similar power-law dependence of d_R on $\bar{E}_{ion}$ to that seen in Fig. 2. Thus, the power-law relationship between d_R and $\bar{E}_{ion}$ may be expected as

$$d_R = B(\bar{E}_{ion})^{\beta}, \tag{2}$$

where B and β are process- and material-dependent constants. In Table I, these calculated constants are listed for various n_{cr} and bias frequencies. The absolute value of d_R depends strongly on n_{cr} as indicated in Table I.

Figure 4 shows the calculated d_R as a function of wet-etch criterion ($= n_{cr}$). The horizontal axis corresponds to the wet-etch time t_w. The decrease in n_{cr} corresponds to an increase in t_w. Since the low bias-frequency case has more high-energy ions than the high bias-frequency case,[43,44] $n_{dam}(x)dx$ extends deeper (wider in depth) in the Si substrate, resulting in larger d_R, as expected based on Figs. 2 and 3(a). Next, the obtained relationship in Eq. (2) is applied to a model prediction of device performance degradation as well as the parameter variations for the case of $n_{cr} = 10^{-4}$.

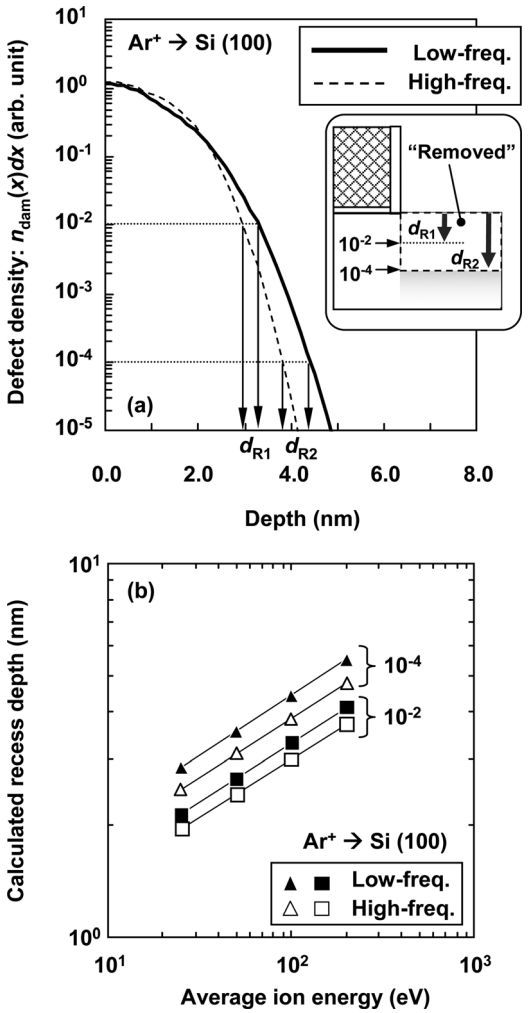

FIG. 3. (a) Calculated depth profiles of $n_{dam}(x)dx$ for two extreme bias-frequency cases. Once n_{cr} (approximately wet-etch criterion) is defined, d_R is determined as illustrated here. (b) Calculated d_R as a function of average ion energy under different IEDF configurations; low bias-frequency limit ("low-freq.," closed symbols) corresponds to a double-peak IEDF case, while high bias-frequency limit ("high-freq.," open symbols) corresponds to a monochromatic incident ion-energy case. Two different wet-etch criteria are compared: $n_{cr} = 10^{-4}$ (triangles) and 10^{-2} (squares). For details, see the text.

III. PARAMETER VARIATION MODELING

A. Threshold voltage shift and off-state leakage current

Threshold voltage (V_{th}) is a key parameter determining "on-state" and "off-state" of MOSFETs.[12,13] Owing to Si recess formation by PID, V_{th} shifts in accordance with d_R.[11]

TABLE I. Summary of the parameters B and β in Eq. (2) calculated from the present defect generation model.

	Low frequency limit		High frequency limit	
Wet-etch criterion	B	β	B	β
10^{-2}	0.77	0.32	0.72	0.31
10^{-3}	0.91	0.31	0.83	0.31
10^{-4}	1.0	0.32	0.92	0.32

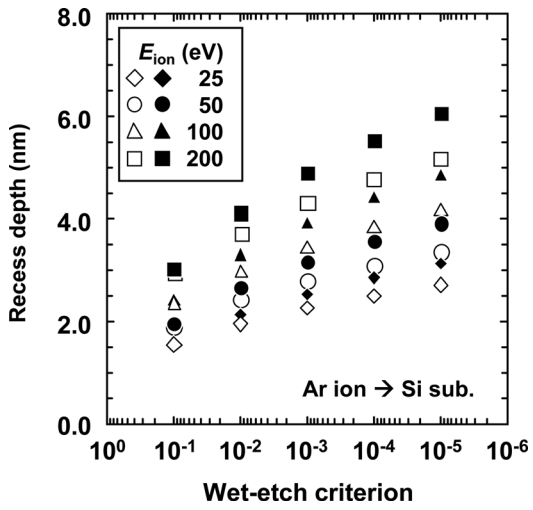

FIG. 4. Relationship between d_R and wet-etch criterion for various $\bar{E}_{ion}$ and the bias-frequency configurations (low- and high-frequency limit cases). As shown, as the wet-etch criterion (n_{cr}) decreases (equivalent to an increase in the wet-etch time), d_R increases. Closed symbols: low bias-frequency limit, open symbols: high bias-frequency limit.

ΔV_{th} by PID was found to depend linearly on d_R as described by[11]

$$\Delta V_{th} \approx -\frac{qN_A W^2}{C_{ox}\sqrt{X_j^2 + 2WX_j}}\left(\frac{d_R}{L_g}\right), \tag{3}$$

where N_A is the substrate doping concentration, X_j is the source/drain junction depth, C_{ox} is the gate oxide capacitance, and W is the depletion-layer width. Based on Eqs. (2) and (3) and Figs. 2 and 3(b), the relationship between ΔV_{th} and $\bar{E}_{ion}$ may be expressed as

$$\Delta V_{th} = C\left(\frac{(\bar{E}_{ion})^{\beta}}{L_g}\right), \tag{4}$$

where C is a constant. Note that ΔV_{th} is negative for n-ch MOSFETs. Thus, the decrease in V_{th} increases the subthreshold leakage current (I_{off}) as expressed by

$$I_{off}^{dam} = I_{off}^{0} \times \exp\left(D\frac{d_R}{L_g}\right) = I_{off}^{0} \times \exp\left(D\frac{B(\bar{E}_{ion})^{\beta}}{L_g}\right), \tag{5}$$

where D is a device-structure-dependent constant. This expression was preliminarily predicted,[14] and is confirmed to be valid from the above-presented discussions in this study.

To determine the parameters C and D, we performed 2D technology computer-aided-design (TCAD) simulations[9] for the present-day n-ch MOSFETs with various d_R. For the simulations, the substrate doping was set to be 5×10^{17} cm^{-3} and the peak concentrations of SDE, source/drain (SD), and halo implant (Halo) regions[7] were 1×10^{19}, 1×10^{20}, and 1×10^{18} cm^{-3}, respectively. The junction depths of SDE, SD, and Halo were set to be 26, 120, and 70 nm, respectively. Gate dielectric thickness was 2 nm. Only the geometrical structure change in the damaged devices was taken into account. Details are described elsewhere.[11,30] Based on Eqs. (4) and (5), one can estimate degradation of MOSFET performance by using plasma parameter $\bar{E}_{ion}$.

B. MOSFET parameter variations

Once analytical expressions for the relationship between plasma and device parameters ($\bar{E}_{ion}$, ΔV_{th}, and I_{off}) are obtained as in Eqs. (4) and (5), MOSFET parameter variations can be calculated with a mathematical approach.[14] As shown in Fig. 1, we define the probability density distribution functions[33] of ΔV_{th} ($=z$), $\bar{E}_{ion}$ ($=E_{ion}=x$), L_g($=y$), and d_R($=w$), as $f_{\Delta Vth}(z)$, $f_{Eion}(x)$, $f_{Lg}(y)$, and $f_{dR}(w)$, respectively. Note that $z=g(x,y)$, or $z=h(w,y)$, as deduced from Eqs. (4) and (3), respectively. The $f_{\Delta Vth}(z)$ value is the joint density distribution function[33] of $f_{Eion}(x)$ and $f_{Lg}(y)$. In general, the cumulative distribution functions of $f_{\Delta Vth}(z)$, $F_{\Delta Vth}(z)$, are calculated from[33]

$$F_{\Delta Vth}(z) = \iint_{x,y\in D_z} f_{xy}(x,y)dx\,dy, \tag{6}$$

where $f_{xy}(x,y)$ is the joint p.d.f. and D_z in the x–y plane represents the region where the inequality $g(x,y) \le z$ is satisfied. Since x ($=E_{ion}$) and y ($=L_g$) are considered to be independent random variables for an offset space etching, Eq. (6) can be rewritten by the convolution of the functions as

$$F_{\Delta Vth}(z) = \iint_{x,y\in D_z} f_{Eion}(x)f_{Lg}(y)dx\,dy. \tag{7}$$

The expected value or the mean of x is defined by

$$\mu_{Eion} = \int_{-\infty}^{\infty} x f_{Eion}(x)dx \tag{8}$$

and the variance[33,53] is defined by

$$(\sigma_{Eion})^2 = \int_{-\infty}^{\infty} (x-\mu_{Eion})^2 f_{Eion}(x)dx. \tag{9}$$

Note that the same procedure can be applied to the other parameters such as L_g, d_R, and I_{off}. The main purpose of this paper is to derive $f_{\Delta Vth}(z)$, $\mu_{\Delta Vth}$ (the mean value of ΔV_{th} by PID), and $\sigma_{\Delta Vth}$ (the standard deviation) from $f_{Eion}(x)$ and $f_{Lg}(y)$ by using PID models presented previously. In this calculation, we employed a Monte Carlo method for more than 10^6 MOSFETs.

IV. RESULTS AND DISCUSSION

A. Threshold voltage versus $\bar{E}_{ion}$

Based on Eqs. (3)–(5) and TCAD simulations, the effects of $\bar{E}_{ion}$ on ΔV_{th} and I_{off} are calculated for various technology nodes.[7] Figure 5(a) shows calculated $|\Delta V_{th}|$ as a function of $\bar{E}_{ion}$ for two bias configurations. In this figure, the average ion energies were calculated from the recess depths assumed. Figure 5(b) shows I_{off} determined from Eq. (5). As seen in these figures, as $\bar{E}_{ion}$ increases, both $|\Delta V_{th}|$ and I_{off} increase. Since d_R exhibits a power-law dependence on $\bar{E}_{ion}$, $|\Delta V_{th}|$ obeys a similar power-law dependence, while I_{off} exponentially increases with increased $\bar{E}_{ion}$ as Eq. (5) suggests.

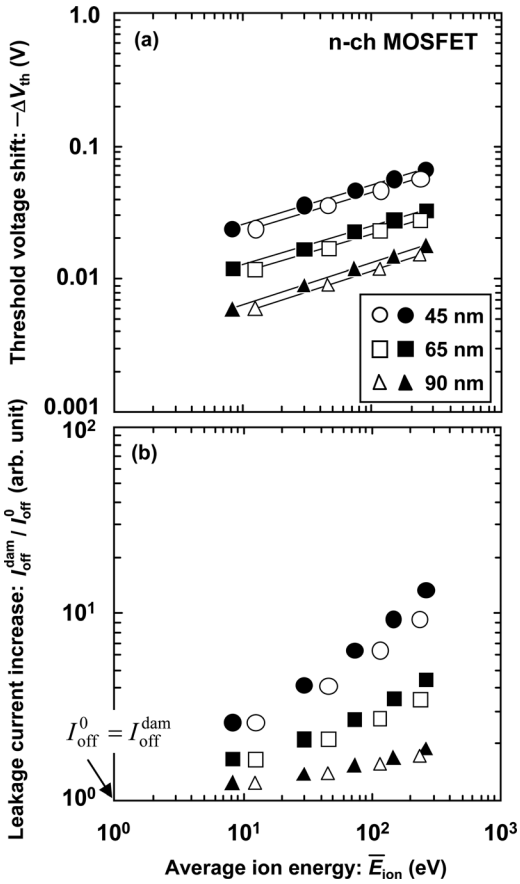

FIG. 5. Calculated (a) ΔV_{th} and (b) I_{off} changes of damaged MOSFETs with recess structure as a function of $\bar{E}_{ion}$ for various technology nodes. (a) A power-law dependence of $|\Delta V_{th}|$ on $\bar{E}_{ion}$ is seen. (b) I_{off}^{dam} is normalized by I_{off}^{0} for easy comparison. (I_{off}^{dam} is the subthreshold leakage current of the damaged MOSFET and I_{off}^{0} is that of the control device.) Closed symbols: low bias-frequency limit, open symbols: high bias-frequency limit.

Regarding bias-frequency effects, the low bias frequency indicates larger changes of $|\Delta V_{th}|$ and I_{off}. However, as reported previously,[8,54] the bias-frequency effect is comparatively smaller than the $\bar{E}_{ion}$ effect as seen in these figures.

B. V_{th} and I_{off} variations induced by $\bar{E}_{ion}$ variation

Figure 6(a) shows an example of $f_{Eion}(x)$ when values are assumed as $\mu_{Eion} = 100$ eV and $\sigma_{Eion} = 3$ eV. (The energy of each ion defined by an IEDF is assumed to obey the distribution $f_{Eion}(x)$.) This assumption is based on a speculated variation of resultant V_{dc} determined from that of absorbed power by plasma (or applied and reflected powers) supplied by an rf system during plasma etching—approximately 10% stability in $3\sigma_{Eion}$. Since there are many factors influencing the energy of the ion impacting on the Si surface during an offset spacer etch process (applied bias powers, collisions in the plasma bulk and sheath, etc.), we assume that $f_{Eion}(x)$ obeys a Gaussian distribution as shown in Fig. 6(a). Thus, $f_{Eion}(x)$ is expressed as

$$f_{Eion}(x) = \frac{1}{\sqrt{2\pi}\sigma_{Eion}} \exp\left[\frac{-(x-\mu_{Eion})^2}{2\sigma_{Eion}^2}\right], \tag{10}$$

where μ_{Eion} and σ_{Eion} represent the mean value and the standard deviation, respectively. In this figure, the variation in x ($\bar{E}_{ion}$) was estimated by a Monte Carlo method for more than 10^6 MOSFETs. From Eq. (2), we can describe $f_{dR}(w)$ as

$$f_{dR}(w) = \frac{f_{Eion}(h^{-1}(w))}{|h'(x)|}, \tag{11}$$

where $w = h(x) = B(x)^{\beta}$. The value $h^{-1}(w)$ $(=x)$ is its inverse function and $h'(x)$ is the derivative of $h(x)$.[20,33] Figure 6(b) shows the cumulative probability plots of calculated $f_{dR}(w)$ for the case of $f_{Eion}(x)$ under low bias frequency. Although

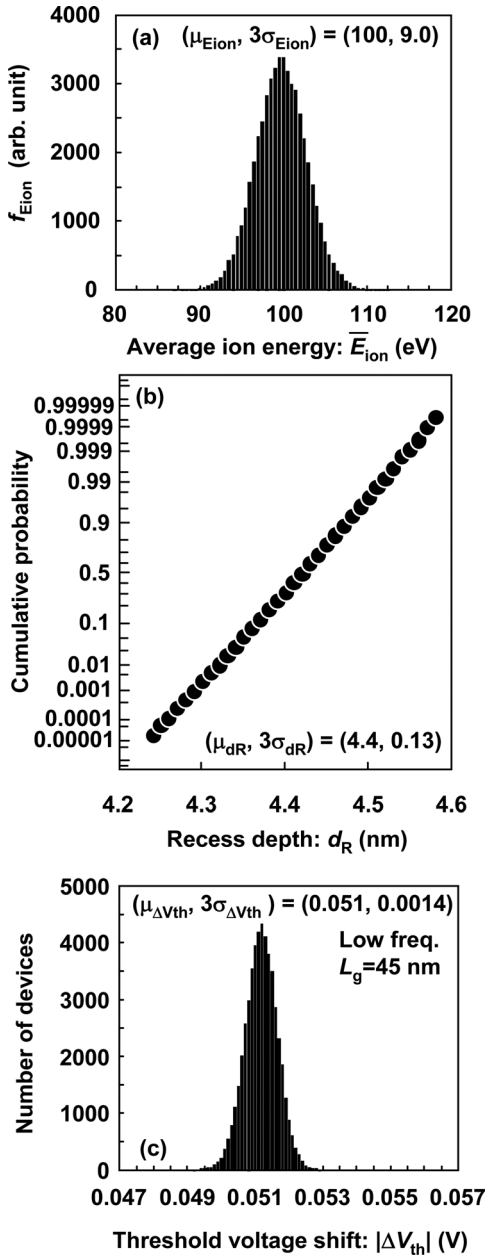

FIG. 6. (a) Example of distribution function f_{Eion} for $>10^6$ MOSFETs employed in this simulation. $\mu_{Eion} = 100$ eV and $\sigma_{Eion} = 3$ eV are assumed. Increment in f_{Eion} is 0.5 eV. (b) Cumulative probability plot of the resultant d_R distribution calculated from f_{Eion}. (c) Calculated $|\Delta V_{th}|$ distribution for $>10^6$ MOSFETs with $L_g = 45$ nm and damaged by the low bias-frequency configuration. Increment in $f_{\Delta Vth}$ is 0.1 mV.

d_R exhibits a power-law dependence on $\bar{E}_{\mathrm{ion}}$ (as in Eq. (2)), the calculated d_R distribution $f_{dR}(w)$ shows an approximately normal distribution, confirmed from the linear relationship between cumulative probability and d_R in the displayed plot. In this case, μ_{dR} (the mean value) and $3\sigma_{dR}$ (σ_{dR}: the standard deviation) are 4.4 and 0.13 nm, respectively. This normal distribution is attributed to the power-law constant $\beta = 0.32$ (<1) and small $\sigma_{E\mathrm{ion}} = 3$ eV.

From the results in Figs. 6(a) and 6(b), $f_{\Delta V\mathrm{th}}(z)$ can be calculated for the present simulation, and the result is shown in Fig. 6(c). For the purpose of simplicity, the variation in L_g is disregarded, i.e., $f_{Lg}(y) = \delta(y - \mu_{Lg})$, where $\delta(x) = 1$ at $x = 0$ and $\delta(x) = 0$ at $x \neq 0$, and $\mu_{Lg} = 45$ nm.

Given L_g, one can write, from Eq. (4),

$$f_{\Delta V\mathrm{th}}(z) = \frac{f_{E\mathrm{ion}}(g^{-1}(z))}{|g'(x)|}, \tag{12}$$

where $z = g(x, y = L_g) = g(x) = (C/L_g)(x)^{\beta}$ and $g^{-1}(z)$ is its inverse function. The value $g'(x)$ is the derivative of $g(x)$. In Fig. 6(c), calculated $\mu_{\Delta V\mathrm{th}}$ and $3\ \sigma_{\Delta V\mathrm{th}}$ are shown. In this case, $6\sigma_{\Delta V\mathrm{th}}$ is ~3 mV, in a comparable range to the reported parameter variations induced by doping fluctuation,[15,16,19] LER,[27] and LWR.[22] This is a significant amount considering that the present-day ULSIs require V_{th} variability of less than 10 mV.[7,16–19,26,28]

Finally, we summarize simulated results of ΔV_{th} and I_{off} variations for two $f_{E\mathrm{ion}}(x)$ cases in Figs. 7 and 8, respectively. In both figures, the variation in L_g is disregarded. Figure 7(a) shows the $\bar{E}_{\mathrm{ion}}$ dependence of $\sigma_{\Delta V\mathrm{th}}$ for the case when $\sigma_{E\mathrm{ion}}$ is set to 3% of $\mu_{E\mathrm{ion}}$, as a case study of a constant uniformity in the resultant V_{dc} by an rf system. Figure 7(b) shows the case of constant $\sigma_{E\mathrm{ion}}$ (= 3 eV) regardless of $\bar{E}_{\mathrm{ion}}$ as a case study of constant fluctuation range in the resultant V_{dc}. Although the present model prediction is based on ideal scenarios, results provide better understanding of the effects of plasma process parameters on MOSFET performance variations than previously available. Figures 8(a) and 8(b) show these corresponding results for I_{off} variations ($3\sigma_{I\mathrm{off}}^{\mathrm{dam}}$ normalized by $\mu_{I\mathrm{off}}^{\mathrm{dam}}$). In both cases, σ_{Lg} is disregarded to clarify the effect of $\sigma_{E\mathrm{ion}}$ or $\bar{E}_{\mathrm{ion}}$ without other parameter-variation impacts.

Note that because the variables x ($= \bar{E}_{\mathrm{ion}}$) and y ($= L_g$) are independent random variables in terms of $f_{V\mathrm{th}}(z)$ as indicated in Eq. (7), the other parameter variations can be incorporated into the results here, if necessary, by using

$$\left(\sigma_{V\mathrm{th}}^{\mathrm{dam}}\right)^2 = \left(\sigma_{V\mathrm{th}}^{Lg}\right)^2 + \left(\sigma_{\Delta V\mathrm{th}}\right)^2, \tag{13}$$

where $\left(\sigma_{V\mathrm{th}}^{\mathrm{dam}}\right)^2$ is the variance of V_{th} of the damaged MOSFETs and $\left(\sigma_{V\mathrm{th}}^{Lg}\right)^2$ is the variance of V_{th} induced by L_g variation.

As seen in Figs. 7(a) and 7(b), the shrinkage of L_g increases ΔV_{th} variations drastically. In the worst case, 3 $\sigma_{\Delta V\mathrm{th}}$ increases to more than 2 mV. When L_g is less than 45 nm, the effect of bias frequency on $\sigma_{V\mathrm{th}}^{\mathrm{dam}}$ is considerable in Figs. 8(a) and 8(b). The same $\bar{E}_{\mathrm{ion}}$ dependence of $\sigma_{I\mathrm{off}}^{\mathrm{dam}}$ is observable. As seen, $3\sigma_{I\mathrm{off}}^{\mathrm{dam}}$ becomes ~8% for 32-nm-L_g

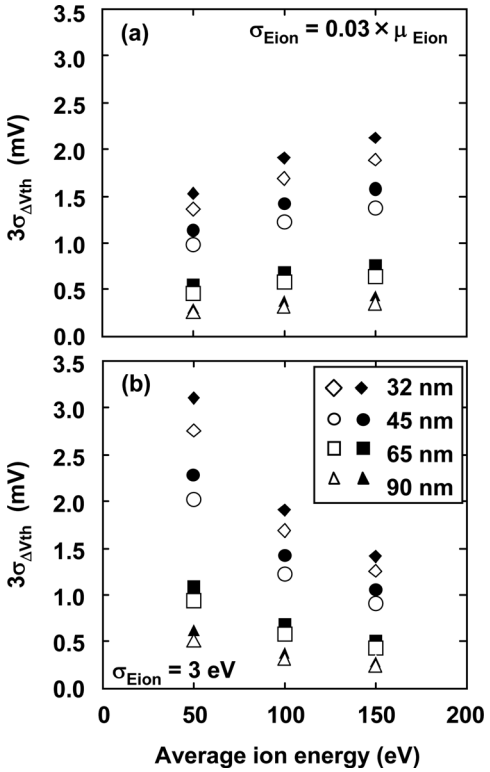

FIG. 7. Calculated $3\sigma_{\Delta V\mathrm{th}}$ of $f_{\Delta V\mathrm{th}}$ for (a) $\sigma_{E\mathrm{ion}} = 3\%$ of $\bar{E}_{\mathrm{ion}}$ and (b) $\sigma_{E\mathrm{ion}} = 3$ eV for various technology nodes with two different bias frequency cases. Closed symbols: low bias-frequency limit, open symbols: high bias-frequency limit.

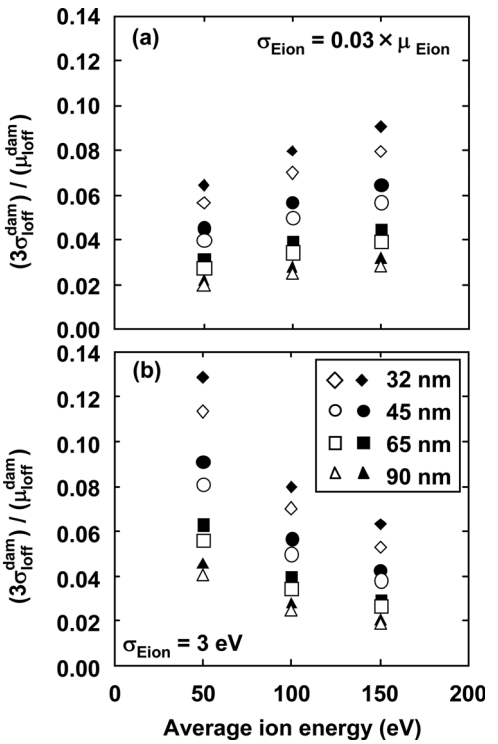

FIG. 8. Calculated $3\sigma_{I\mathrm{off}}^{\mathrm{dam}}/\mu_{I\mathrm{off}}^{\mathrm{dam}}$ of $f_{I\mathrm{off}}^{\mathrm{dam}}$ for (a) $\sigma_{E\mathrm{ion}} = 3\%$ of $\bar{E}_{\mathrm{ion}}$ and (b) $\sigma_{E\mathrm{ion}} = 3$ eV for various technology nodes with two different bias frequency cases. Closed symbols: low bias-frequency limit, open symbols: high bias-frequency limit.

MOSFETs, indicating an increase in stand-by power consumption of ULSIs. Therefore, it should be noted that, in addition to L_g variation or impurity fluctuation,[15] plasma-parameter variation such as $\sigma_{E\mathrm{ion}}$ in $\bar{E}_{\mathrm{ion}}$ also enhances V_{th} and I_{off} variations considerably.

V. SUMMARY AND CONCLUSIONS

The effects of plasma-induced damage on the MOSFET parameter variations were modeled. Si recess structure was found to enhance ΔV_{th} with the shrinkage of L_g. The quantitative relationships among $\bar{E}_{\mathrm{ion}}$, d_R, ΔV_{th}, and I_{off} were investigated by taking into account the wet-etch process and the analytical expressions for the model prediction were proposed. Due to the variation of $\bar{E}_{\mathrm{ion}}$, the damaged MOSFET suffers from considerable increases in V_{th} and I_{off} variations. This is significant for present-day ULSI development, which requires comparatively low variations. The present model has potential to be integrated with other variation models such as LER, LWR, and dopant fluctuation for future advanced ULSI designs.

ACKNOWLEDGMENTS

The authors greatly thank M. Yoshimaru, H. Hayashi, S. Hayashi, H. Kokura, and T. Tatsumi at STARC (Semiconductor Technology Academic Research Center) for their helpful discussion, and Y. Nakakubo and A. Matsuda of Kyoto University for their support. This work was financially supported in part by STARC and a Grant-in-Aid for Scientific Research (B), 20360329, from the Japan Society for the Promotion of Science.

[1]K. Eriguchi and K. Ono, J. Phys. D: Appl. Phys. **41**, 024002 (2008).
[2]S. Krishnan and A. Amerasekera, *Proceedings of the International Reliability Physics Symposium*, Reno, NV, 1998 (IEEE, 1998), p. 302.
[3]K. Eriguchi, M. Kamei, K. Okada, H. Ohta, and K. Ono, *Proceedings of the International Conference on Integrated Circuit Design & Technology*, Grenoble, France, 2008 (IEEE, 2008), p. 97.
[4]K. Eriguchi, M. Kamei, D. Hamada, K. Okada, and K. Ono, Jpn. J. Appl. Phys. **47**, 2369 (2008).
[5]S. A. Vitale and B. A. Smith, J. Vac. Sci. Technol. B **21**, 2205 (2003).
[6]T. Ohchi, S. Kobayashi, M. Fukasawa, K. Kugimiya, T. Kinoshita, T. Takizawa, S. Hamaguchi, Y. Kamide, and T. Tatsumi, Jpn. J. Appl. Phys. **47**, 5324 (2008).
[7]Semiconductor Industry Association, *The International Technology Roadmap for Semiconductors*, 2009 ed. (2009).
[8]K. Eriguchi, Y. Nakakubo, A. Matsuda, Y. Takao, and K. Ono, Jpn. J. Appl. Phys. **49**, 056203 (2010).
[9]K. Eriguchi *et al.*, Tech. Dig. – Int. Electron Devices Meet. **2008**, 443 (2008).
[10]N. Yasui, K. Kuwahara, M. Sakaguchi, and S. Watanabe, *Proceedings of the Symposium on Dry Process*, Tokyo, Japan, 2007 (The Japan Society of Applied Physics, 2007), p. 195.
[11]K. Eriguchi, A. Matsuda, Y. Nakakubo, M. Kamei, H. Ohta, and K. Ono, IEEE Electron Device Lett. **30**, 712 (2009).
[12]Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. (Cambridge University Press, New York, 2009).
[13]S. M. Sze, *Physics of Semiconductor Devices* 2nd ed. (Wiley-Interscience, New York, 1981).
[14]K. Eriguchi, M. Kamei, Y. Takao, and K. Ono, *Proceedings of the International Conference on Integrated Circuit Design & Technology*, Grenoble, France, 2010 (IEEE, 2010), p. 94.
[15]K. Takeuchi, T. Tatsumi, and A. Furukawa, Tech. Dig. – Int. Electron Devices Meet. **1997**, 841 (1997).
[16]M. Kanno *et al.*, VLSI Symposium on Technology, Kyoto, Japan, 2007 (IEEE 2007), p. 88.
[17]K. J. Kuhn, Tech. Dig. – Int. Electron Devices Meet. **2007**, 471 (2007).
[18]K. A. Bowman, A. R. Alameldeen, S. T. Srinivasan, and C. B. Wilkerson, IEEE Trans. Very Large Scale Integr. (VLSI) Systems **17**, 1679 (2009).
[19]O. Weber *et al.*, Tech. Dig. – Int. Electron Devices Meet. **2008**, 245 (2008).
[20]C. D'Agostino, P. Flatresse, E. Beigne, and M. Belleville, *Proceedings of the International Conference on Integrated Circuit Design & Technology*, Grenoble, France, 2008 (IEEE, 2008), p. 301.
[21]S. Narendra, V. De, S. Borkar, D. A. Antoniadis, and A. P. Chandrakasan, IEEE J. Solid-State Circuits **39**, 501 (2004).
[22]H.-W. Kim, J.-Y. Lee, J. Shin, S.-G. Woo, H.-K. Cho, and J.-T. Moon, IEEE Trans. Electron Devices **51**, 1984 (2004).
[23]G.-H. Kim, Y.-R. Kang, W.-J. Kim, S.-Y. Kim, and C.-I. Kim, Thin Solid Films **515**, 4892 (2007).
[24]R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **12**, 131 (2004).
[25]A. Yamaguchi, H. Kawada, and T. Izumi, *Proceedings of the Symposium on Dry Process*, Tokyo, Japan, 2007 (The Japan Society of Applied Physics, 2007), p. 277.
[26]A. T. Putra, A. Nishida, S. Kamohara, and T. Hiramoto, Appl. Phys. Express **2**, 024501 (2009).
[27]H. Fukutome, Y. Momiyama, T. Kubo, Y. Tagawa, T. Aoyama, and H. Arimoto, IEEE Trans. Electron Devices **53**, 2755 (2006).
[28]H. Fukutome, E. Yoshida, K. Hosaka, M. Tajima, Y. Momiyama, and S. Satoh, IEEE Electron Device Lett. **31**, 240 (2010).
[29]G. H. Kinchin and R. S. Pease, Rep. Prog. Phys. **18**, 1 (1955).
[30]K. Eriguchi, Y. Nakakubo, A. Matsuda, Y. Takao, and K. Ono, IEEE Electron Device Lett. **30**, 1275 (2009).
[31]J. Lindhard, M. Scharff, and H. E. Schiott, Mat. Fys. Medd. K. Dan. Vidensk. Selsk. **33**, 1 (1963).
[32]J. F. Gibbons, Proc. IEEE **56**, 295 (1968).
[33]A. Papoulis and S. Pillai, *Probability, Random Variables, and Stochastic Processes* (McGraw-Hill, New York, 2002).
[34]S. M. Sze, *VLSI Technology*, 2nd ed. (McGraw-Hill, New York, 1988).
[35]C. Y. Chang and S. M. Sze, *ULSI Technology* (McGraw-Hill, New York, 1996).
[36]W. D. Wilson, L. G. Haggmark, and J. P. Biersack, Phys. Rev. B **15**, 2458 (1977).
[37]A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, Thin Solid Films **518**, 3481 (2010).
[38]Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, K. Eriguchi, and K. Ono, *Proceedings of the International Conference on Integrated Circuit Design & Technology*, Grenoble, France, 2008 (IEEE, 2008), p. 101.
[39]G. Moliere, Z. Naturforsch. A **2**, 133 (1947).
[40]J. D. Plummer, M. Deal, and P. B. Griffin, *Silicon VLSI Technology, Fundamentals, Practice and Modeling* (Prentice Hall, Englewood Cliffs, NJ, 2000).
[41]M. Posselt, B. Schmidt, C. S. Murthy, T. Feudel, and K. Suzuki, J. Electrochem. Soc. **144**, 1495 (1997).
[42]P. Benoit-Cattin and L.-C. Bernard, J. Appl. Phys. **39**, 5723 (1968).
[43]E. Kawamura, V. Vahedi, M. A. Lieberman, and C. K. Birdsall, Plasma Sources Sci. Technol. **8**, R45 (1999).
[44]M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*, 2nd ed. (Wiley-Interscience, New York, 2005).
[45]J. W. Coburn and K. Eric, J. Appl. Phys. **43**, 4965 (1972).
[46]A. Manenschijn, G. C. A. M. Janssen, E. v. d. Drift, and S. Radelaar, J. Appl. Phys. **69**, 1253 (1991).
[47]J. Liu, G. L. Huppert, and H. H. Sawin, J. Appl. Phys. **68**, 3916 (1990).
[48]A. Metze, D. W. Ernie, and H. J. Oskam, J. Appl. Phys. **65**, 993 (1989).
[49]Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, K. Eriguchi, and K. Ono, in *Emerging Technologies and Circuits*, edited by A. Amara, M. Belleville, and T. Ea (Springer, London, 2010), Vol. 66, p. 107.
[50]A. Matsuda, Y. Nakakubo, Y. Ueda, H. Ohta, K. Eriguchi, and K. Ono, Ext. Abs. Solid State Dev. Mat., 358 (2008).
[51]D. E. Aspnes, J. B. Theeten, and F. Hottier, Phys. Rev. B **20**, 3292 (1979).
[52]Y. Nakakubo, A. Matsuda, M. Fukasawa, Y. Takao, T. Tatsumi, K. Eriguchi, and K. Ono, Jpn. J. Appl. Phys. **49**, 08JD02 (2010).
[53]H. F. Dadgour, L. Sheng-Chih, and K. Banerjee, IEEE Trans. Electron Devices **54**, 2930 (2007).
[54]Y. Nakakubo, Y. Ueda, M. Yoshida, D. Hamada, M. Kamei, K. Eriguchi, and K. Ono, *Proceedings of the Symposium on Dry Process*, Tokyo, Japan, 2007 (The Japan Society of Applied Physics, 2007), p. 287.