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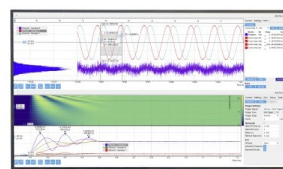
Heterogeneously structured phase-change materials and memory

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ABSTRACT

Phase-change memory (PCM), a non-volatile memory technology, is considered the most promising candidate for storage class memory and neuro-inspired devices. It is generally fabricated based on GeTe–Sb_2Te_3 pseudo-binary alloys. However, natively, it has technical limitations, such as noise and drift in electrical resistance and high current in operation for real-world device applications. Recently, heterogeneously structured PCMs (HET-PCMs), where phase-change materials are hetero-assembled with functional (barrier) materials in a memory cell, have shown a dramatic enhancement in device performance by reducing such inherent limitations. In this Perspective, we introduce recent developments in HET-PCMs and relevant mechanisms of operation in comparison with those of conventional alloy-type PCMs. We also highlight corresponding device enhancements, particularly their thermal stability, endurance, RESET current density, SET speed, and resistance drift. Last, we provide an outlook on promising research directions for HET-PCMs including PCM-based neuromorphic computing.

I. INTRODUCTION

The emergence of data-driven technologies demands ultrahigh density and fast-access memories. Traditionally, in the von Neumann architecture, the basic concept of classical computing has a memory hierarchy that ranges from processor cache and dynamic random-access memory (DRAM) to solid-state drives (SSDs). There is a mismatch in operating speed and bandwidth between such memories, which fundamentally limits computing speed and efficiency. In particular, a new element is required to fill the gap between DRAM and SSD. Storage class memory (SCM)[1] was first proposed by IBM as the next-generation class of memory in 2008. Phase-change memory (PCM), which is a random-access memory based on phase-change chalcogenides, has emerged as a leading non-volatile SCM candidate, largely owing to its relatively good scalability, fast operating speed, and multi-level storage ability.[2,3] In addition, PCM is potentially well-suited to the future neuro-inspired computing systems toward non-von Neumann computing architectures.[4–8]

Phase-change materials, of which GeTe–Sb_2Te_3 (GST) pseudo-binary alloys are representative, experience a reversible transformation between the amorphous and crystalline phases, accompanied by a recognizable contrast in electrical resistivity and optical

reflectivity. The RESET operation activated by the melt-quenched amorphization process requires a mA-level current, resulting in high power consumption, while the SET programming pulse limits the operating speeds of memories. In addition, conventional alloy-based PCMs suffer from inhomogeneity in their phase and chemical compositions, both spatially and temporally, upon repetitive cycling. This leads to large fluctuations in the electrical resistance of both the SET and RESET states. Owing to the considerable volume difference between the amorphous and crystalline phases, structural relaxation also occurs in the volume-expanded amorphous GST. In short, the high energy consumption and inherent cell variation of PCMs are critical issues that must be addressed for future technological applications of PCM, such as SCM and neuromorphic computing.

To date, a number of attempts have been made to reduce energy consumption and improve the reliability of PCMs. For the former, the RESET current needs to be substantially reduced. One material-based solution is to simply increase the resistance of the crystalline phase with substitutional dopants in alloy-based PCMs. Various dopants have been investigated for GST pseudo-binary alloys, which has successfully led to a 30%–60% reduction in the

RESET current. However, this approach causes poor long-term device stability due to phase segregation. Alternatively, new device structures, such as (i) edge-contact structure,[9] (ii) μ-trench,[10,11] (iii) confined structure,[12,13] and (iv) ring-shape,[14] have been proposed to minimize the effective contact area between the PCM layer and the bottom electrode. As expected, the RESET current is dramatically reduced to a few-μA, but the resultant high current density ($\sim$40 MA/cm^2) still causes a tolerance issue for metal connecting wires in the circuitry.

More recently, heterogeneously structured PCMs (HET-PCMs) were introduced to represent the best compromise between device performance and consistency. For instance, an interlayer functioning as a thermal barrier can be inserted between the PCM and bottom electrode to effectively localize heating by blocking heat dissipation.[15] This particular type of heterostructured PCM exhibits the desired low operation energy while unexpectedly improving stability-related properties. Another major class of HET-PCMs is based on superlattice-like (SLL) heterostructures; one example is interfacial PCM (iPCM), first proposed by the Tominaga group in 2011.[16] It showed excellent switching responsiveness and consumed substantially less energy during the SET process, possibly due to the confined local atomic switching of Ge atoms. To date, there have been many debates over its novel mechanism of interfacial atomic switching, but it is generally accepted that the increasing number of interfaces introduces a series of thermal boundary resistances, thus potentially enhancing their performance significantly.[17–19] There have been recent attempts to more actively explore the role of such confinement layers. Ding et al. reported the best device characteristics in their heterostructured PCMs of Sb$_2$Te$_3$/TiTe$_2$ in 2019, underlining a selection rule of the confinement layer.[20]

The aim of this article is to review such impactful results from heterogeneously structured PCMs, mostly in chronological order. In this Perspective article, the development of HET-PCMs is introduced first, followed by a comprehensive comparison of the operating mechanisms of conventional homogeneous PCMs with those of HET-PCMs. Fabrication and device enhancements in HET-PCMs are summarized thoroughly. Last, our perspective on the further optimization required for HET-PCM-based devices and their potential application in neuromorphics is provided.

II. DEVELOPMENT OF HETEROGENEOUS PCMs

One fundamental limitation in implementing PCM as an emerging non-volatile memory (NVM) element originates from the melt-quenching process because it requires high power and introduces a significant amount of stress caused by a volume change of up to 7%. Such Joule-heating-induced phase transitions suffer from critical issues hindering the reliable operation of scaled devices, including thermal instability and resistance drift. Early on, designing a new class of homogeneous alloys was reported as an efficient way to overcome energy consumption and reliability challenges, with pseudo-binary GST, doped GST, and doped Sb$_2$Te$_3$ being representative examples. However, device performance is still limited when compared with that of other NVM technologies. More recently, heterogeneously structured PCMs, either using interfacing dissimilar components or adopting SLL multi-stacks, have resulted in marked improvements in device performance in terms of speed,

energy efficiency, and reliability. Here, we present a progress report for heterogeneously structured PCMs with superior performance, following a brief review of homogeneous phase-change alloys.

A. Homogeneous phase-change alloys

1. Materials perspective

The first reported electrical switching phenomenon in phase-change materials was by Ovshinsky in 1968, but the applied pulse was too long for immediate use as NVM.[21,22] A few decades later, phase-change materials based on GST and Ag- and In-doped Sb$_2$Te (AIST) were tested for use in memory and optical devices, but such conventional phase-change memory still exhibited low SET speed ($\sim$50 ns),[23] poor data retention ($\sim$85 °C for 10 years),[24] high-resistance drift (drift exponent: $\sim$0.101),[25] and high RESET energy. To function as main memory, lower RESET energy and higher endurance are commonly required. More specifically, faster switching speeds are required to replace DRAM, while other technical challenges, such as scalability, manufacturing cost, and data retention, must be addressed to substitute flash memory. To enhance the device performance of PCMs for use as main memory, doped phase-change materials based on GST and GeTe were actively investigated by doping with various elements, such as C,[26–29] N,[30,31] O,[32] Cu,[33–35] Ni,[36] Sc,[37,38] and SiC.[39] Thanks to the incorporated dopants, the increased resistivity and crystallization temperature resulted in lower RESET currents and improved retention temperatures in the range of 119–183 °C. Theoretically estimated from the first-principles calculation, the local order of the amorphous matrix could show enhanced thermal stability in amorphous doped GST. However, the lack of ABAB-type squared rings, caused by increasing the tetrahedral Ge atoms, limits the extremely fast crystallization speed. Recently, carbon-doped GST with 40 nm nodes was successfully fabricated on an industrial level with a >10^2 resistance ratio, a high crystallization speed potential of 20 ns, a retention temperature of 128 °C, and a high endurance of $\sim$10^8 cycles.[28] Although doped GST shows advanced device performance in terms of retention temperature and SET speed, there are still limitations stemming from the trade-off between amorphous stability and SET speed, while the RESET current and endurance properties limit the use of PCM as main memory.

Under the limited material selection of PCMs with the FCC structure of the GST pseudo-binary line,[40] a novel study of Ti$_{0.4}$Sb$_2$Te$_3$ (TST) by Zhu et al. reported simultaneous improvements in the SET speed and stability by doping the hexagonally structured Sb$_2$Te$_3$, widely known to possess very fast switching speed.[41] Indeed, TST-based devices showed ten times faster SET speed ($\sim$6 ns at 1.3 V) than GST ($\sim$75 ns at 1.6 V), and the endurance was as high as $\sim$10^7 cycles, but its thermal stability still remained inferior to doped GST or GeTe with the reported retention temperatures of 92–141 °C. The RESET energy of TST (0.95×10^{-9} J) for an 80 nm bottom electrode contact (BEC) was much lower than that of conventional GST (4.20×10^{-9} J).[41] Although the Ti–Te–Ti–Te "extrinsic bond" supported fast nucleation in the hexagonal lattice of TST, the segregated TiTe$_2$ nano-lamella structures prevented a further reduction of the crystallization time to sub-nanoseconds.[42] Subsequently, various elements, such as Ti,[41,43–46] Al,[47] and Sc,[48,49] were implemented in
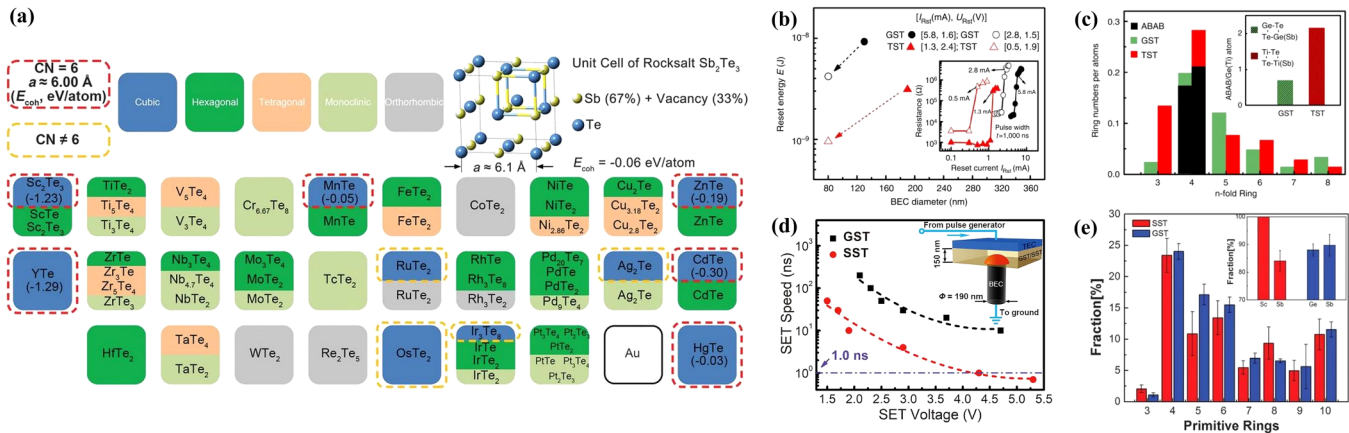
FIG. 1. (a) Materials screening for transition metal doped Sb$_2$Te$_3$. Reproduced with permission from Rao *et al.*, Science **358**, 1423 (2017). Copyright 2017 AAAS. (b) Reset performance comparison for Ge$_2$Sb$_2$Te$_5$ and Ti$_{0.4}$Sb$_2$Te$_3$ phase-change memory cells. (c) Nucleation-dominated crystallization mechanism of Ti$_{0.4}$Sb$_2$Te$_3$. Adapted from Zhu *et al.*, Nat. Commun. **5**, 4086 (2014). Copyright 2014 Springer Nature. (d) PCM switching properties for SET operation of SST and GST PCRAM devices. (e) Primitive ring analysis of amorphous SST and GST using DFMD simulations. Reproduced with permission from Rao *et al.*, Science **358**, 1423 (2017). Copyright 2017 AAAS.

Sb$_2$Te, Sb$_4$Te, and Sb$_2$Te$_3$. Rao *et al.* introduced Sc-doped Sb$_2$Te$_3$ (SST) with a high device performance, such as an ultra-fast crystallization speed of 0.7 ns compared with GST, as shown in Fig. 1(d).[49] Figure 1(a) shows their selection of dopants, transition metals with a cubic lattice structure, high melting temperature over 900 K, and high cohesive energy with Te. They suggested the mechanism of SST, which showed dominant four-membered rings in amorphous SST in a density functional theory (DFT)-based molecular dynamics (MD) simulation. In Fig. 1(e), every Sc atom has one fourfold ABAB ring, and ~80%–90% of Sb atoms form ABAB rings, which indicates a high nucleation rate. In contrast, the Sc dopant in Sb$_2$Te$_3$ introduced strong Sc–Te–Sc–Te "extrinsic bonds" with a dominant ABAB ring environment in the amorphous states. These "extrinsic bonds" might act as crystallization nuclei, supporting nucleus growth dominance.[41,49,50] Accordingly, SST-based devices possess endurance as high as 10^5 for 0.8 ns pulse width and 4 × 10^7 for 50 ns pulse width, respectively. Although Sc-doped Sb$_2$Te$_3$ has a benefit of fast SET speed, its thermal stability of 87 °C indicates a trade-off in device performance. In order to address the lack of thermal stability, aluminum[47] and scandium[48] have been doped into Sb$_2$Te to enhance device performance while maintaining high crystallization speeds. We note that SST phase-change materials have a great potential to achieve a longer cyclability under fast operating speed <10 ns when the device geometry of SST is further shrunk.

In later studies, Sc-doped GST was introduced to further enhance the retention temperature. In 2018, Sc-doped GST was presented by Wang *et al.* with thermal stability up to 119 °C, which is higher than those of Sc-doped Sb$_2$Te$_3$ families.[37] In addition, it had a SET speed of ~6 ns at 2.5 V, endurance of ~5 × 10^5 cycles, and RESET energies of 3.37 nJ for 190 nm and 0.96 nJ for 80 nm BEC, respectively, which are similar to those of TST. Considering these superior device properties, Sc-doped GST is potentially

expected to show the best performance among homogeneous alloys. Therefore, although doping can effectively enhance the retention temperature, a fast crystallization speed of <10 ns has not been reported simultaneously with a high endurance level of over 10^8 cycles in homogeneous PCMs.

2. Device architecture perspective

We discussed above various ways to increase the efficiency of PCM devices via material design, especially by introducing dopants to conventional phase-change materials. Research studies on improving device efficiency through cell design have also been actively conducted.[3] Since the BEC area and RESET current (thus, energy) are linearly proportional to each other as shown in Fig. 2(a), the strategy to minimize the contact size was primarily considered from a device architectural perspective. Five types of cell structures are introduced including cross-bar array and mushroom, edge-contact, ring, and confined structures, as presented in Figs. 2(b)–2(f).

Basically, a PCM device consists of PCM and an ovonic threshold switching (OTS) selector with an array structure, called a cross-bar array. The OTS selector selects a specific cell for operation, and then the PCM operates with the aid of the imposed electro-thermal energy. As a relatively simple design, the mushroom structure has been widely adopted as a PCM cell structure; therefore, early research efforts have been focused on reducing the BEC area of the mushroom-shaped PCMs. In 2003, Pirovano *et al.* fabricated a mushroom-structured GST with a 180 nm device,[51] while Sasago *et al.* implemented a cross-bar array of PCM with poly-Si selectors. The technology node was then reduced to 80 nm and the cell size was minimized to 4 F^2 (where F represents the technology node) in the PCM;[52] the RESET current was gradually reduced to 160 μA.
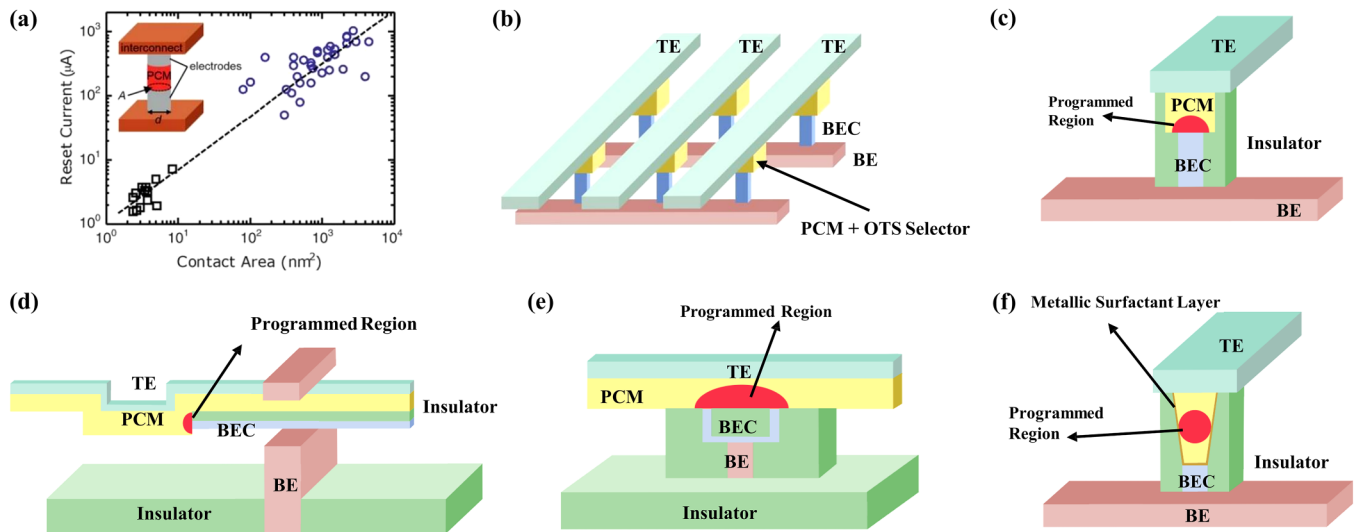
FIG. 2. Various device structures of phase change memory (PCM). (a) Reset current vs an electrode contact area in PCM devices. The inset shows a schematic of a typical PCM cell, where A is the contact area and d is the contact diameter. Reproduced with permission from Raoux *et al.*, MRS Bull. **39**, 708 (2014). Copyright 2014 Cambridge University Press. (b)–(f) Schematic of PCM cell architecture designs. (b) Cross-bar array. (c) Mushroom type. (d) Edge-contact type. (e) Ring type. (f) Confined type.

Another structure is the edge-contact structure. The thin bottom electrode can contact the stair-like GST structure and confine a phase-change region around the edge, which can further reduce the RESET current.[9] Similar to the edge-contact structure, the ring structure and the μ-trench structure were demonstrated to minimize the BEC area.[11,53] As an effort to reduce the BEC area, other research groups also suggested confined-structure PCMs. Hwang *et al.* reported the first confined PCM, shrinking the BEC area from 75 nm to 40 nm. A reduction of the writing current was also reported, but it suffered from an abnormal resistance distribution, presumably caused by the poor uniformity of the BEC.[12] A sub-50 nm BEC area was achieved by Lee *et al.*, and the corresponding simulation results supported the finding of low thermal disturbance among adjacent PCM cells.[13]

By further developing the confined structure, a dash-type confined PCM was first realized with a 7.5 nm wide dash-contact, effectively minimizing the technology node to 20 nm by chemical vapor deposition (CVD).[54] Most dash-type confined PCM devices are fabricated utilizing CVD or atomic layer deposition (ALD) to completely fill the high aspect ratio, with its small pore size. Brightsky and co-workers first proposed a dash-confined GST with a metallic nitride surfactant layer for low-resistance drift and multi-level cells (MLCs). Later, other results using various deposition techniques were also reported.[55–57] In all cases, the metallic surfactant layer could provide a conductive path, making time- and temperature-dependent properties less sensitive for read operations. Specifically, as the current barely affected the partial amorphous region, the drift characteristic was improved. Moreover, due to its catalytic behavior, it also promoted growth near the contact area without any void formation. Recently, Kim *et al.* suggested the potential for a neuromorphic device with low-resistance drift and

1000 programmable states.[58] Considering the excellent performance of dash-type confined PCM and the need for a device with a smaller pole area, ALD is the most promising method for manufacturing high-density PCM devices, as has been actively studied by Hwang and co-workers[59,60] and Adinolfi *et al.*[61] for GST and OTS materials, respectively.

B. Heterogeneously structured PCMs

Prior to the introduction of iPCM, the main objective of developing heterogeneously structured PCM alloys was MLC implementation despite there being relatively little interest in improving endurance and retention characteristics.[62,63] On the other hand, there have been many attempts to use heterogeneous structures in thin-film thermoelectric technology through the reduction of thermal conductivity, and $Sb_2Te_3/TiTe_2$ is a good example of such a heterostructure.[64] Similarly, this concept has been applied to the recent $TiTe_2/Sb_2Te_3$ HET-PCM application, which is currently attracting enormous interest in the field. Among many device metrics, the most decisive properties of PCMs for SCM or neuromorphic applications are endurance, drift, and MLCs, as stated in the International Roadmap for Devices and Systems (IRDS) 2020 edition. Since the above properties can be much improved in a heterogeneously structured PCM, we present the main research trends in this new group of phase-change materials.

1. Heterogeneous PCM with a single interfacial layer

Generally speaking, Joule heating dominantly occurs near the interface between the PCM and the bottom electrode. Owing to the high thermal conductivity of the metallic electrodes (which is proportional to the electrical conductivity at the given temperature

according to the Wiedemann–Franz law), generated heat tends to be dissipated into the environment. In addition to the melt-quenching process, considerable heat dissipation is also closely related to inefficient phase-change characteristics. To optimize and design the thermal properties, the development of a heterogeneously structured PCM was suggested, with an additional layer with low thermal conductivity inserted between the PCM and bottom electrode. However, such an interfacial layer can potentially add extra electrical resistances in series, possibly resulting in higher power consumption in operation. Numerous studies have demonstrated heterogeneously structured PCMs by inserting varied (atomically) thin layers, such as fullerene, tungsten oxide, graphene, and MoS_2. These adlayers could act as confined layers, with the characteristics of a thermal barrier or diffusion barrier, to enhance the switching energy efficiency and endurance of the device. Fullerene (C_{60}),[65] tungsten trioxide (WO_3),[66] and titanium dioxide (TiO_2)[67–69] have been used as thermal confinement layers with low thermal conductivities compared with a tungsten electrode. In

those reports, the reduction of the RESET voltage and the increase of SET resistance resulted in an efficient Joule heating process. In particular, Choi et al.[70] suggested an ultrathin (4 nm) interfacial layer of TiO_2, suggesting the possibility of optimizing thermal conductivity and resistance by controlling the film thickness.[65,66,71,72]

Atomic intermixing between such a 3D thermal barrier layer (which has interfacial defects associated with non-saturated bonds on its surface) and the bottom electrode limits the endurance, usually to less than 10^5 cycles.[71,72] Ahn et al.[73] reported the effect of a graphene layer, known to be a mechanically, chemically, and thermally stable 2D diffusion barrier. In their work, a graphene layer was located between the GST and W plug as displayed in Fig. 3(a). Although the graphene was just a few atoms thick, its desired properties, such as high thermal boundary resistance (TBR) and minimal electrical contact resistance, resulted in a 40% lower RESET current while maintaining 10^5 cycles. As shown in Fig. 3(b), when the graphene layer was larger than the dimension of the bottom electrode (control sample), the current level required
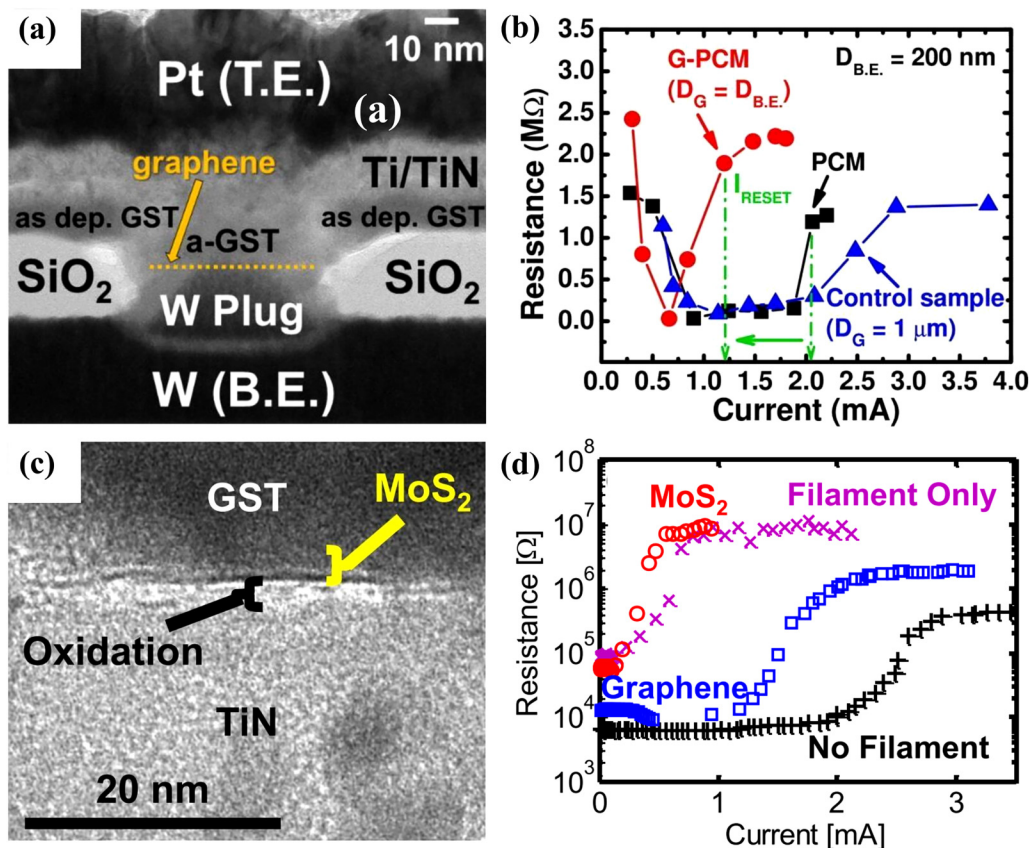

FIG. 3. (a) Cross-sectional HR-TEM image of a graphene-PCM device. (b) RESET current reduction (∼40%) in the G-PCM device (with patterned graphene), compared with control samples without the graphene and with a graphene layer, which points to the enhanced confinement of heat by the inserted graphene layer at the interface. Reproduced with permission from Ahn et al., Nano Lett. **15**, 6809 (2015). Copyright 2015 American Chemical Society. (c) Cross-sectional HR-TEM image of the MoS_2-PCM device. (d) DC read resistance vs current during RESET for the MoS_2-PCM device. The MoS_2-PCM device shows more than 30% reduction in switching current and power. Reproduced with permission from Neumann et al., Appl. Phys. Lett. **114**, 082103 (2019). Copyright 2019 AIP Publishing.

for the RESET operation was higher than in the case of GST without graphene. By contrast, when the graphene layer had dimensions comparable to the bottom electrode (G-PCM), it had fast switching time with a lower current value. This is because the graphene adlayer in G-PCM supports increasing RESET resistance, which makes switching possible even with a lower RESET current. Similarly, Zhu et al. also reported a GST-graphene–GST heterogeneous structure where the active region in the PCM was confined to under the graphene layer, thus significantly decreasing both the RESET current and energy.[74] However, such a small active region could result in only one order of an on/off ratio, which would be a critical issue when determining high- and low-resistance levels. Like graphene, MoS_2 could achieve a reduced effective volume of phase-change materials by acting as a thermal confinement layer. In their recent research, Neumann et al. introduced a thermal confinement layer using a monolayer of MoS_2 and fabricated a heterogeneous structure with a conventional GST material.[15] As shown in Figs. 3(c) and 3(d), owing to relatively low in-plane thermal conductivity and high TBR of MoS_2 compared with graphene, a PCM device inserted with a three-atom-thick monolayer of MoS_2 (~6 Å) between GST and BEC (TiN) showed a 30% reduction in switching current and power.

2. SLL phase-change materials

Among the various attempts to lower the switching energy, one of the most notable results was achieved by lowering the dimension of entropic energy loss. As shown in Fig. 4(a), it was possible to reduce the entropic loss by confining the movement of Ge to 1D, and the supporting results also indicate a crystal–crystal phase transition. iPCM, which was first introduced by the Tominaga group, had a sensational impact on stagnant PCM research. With an ultra-delicate fabrication methodology and material design using layer-by-layer composition, many groups have demonstrated improved device performance compared with

conventional GST. In this section, we discuss various SLL-PCMs, mainly containing GeTe and Sb_2Te_3 layers.

The first SLL structure of PCM was reported by Chong et al. who prepared GeTe/Sb_2Te_3 (where / represents a van der Waals gap) SLL-PCMs exhibiting lower RESET current (6 mA) compared with a bulk alloy (16 mA) under an identical current pulse width (70 ns) and an endurance of ~10^5 cycles. It is noticeable that van der Waals gaps between two adjacent layers still existed even after 10^6 cycles, suggesting that the lower thermal conductivity of the SLL-PCM could be a reason for the reduced RESET and SET currents.[75] In 2011, Simpson et al. introduced iPCM, which has a layer thickness between 5 Å and 40 Å, made up of GeTe and Sb_2Te_3 layers using physical vapor deposition (PVD). Using a laser static tester, iPCM could be transformed to the SET phase at high power (16.5 mW) in ~25 ns, but continuous heating resulted in melting and subsequent ablation. In addition to superior properties including the SET and RESET currents and endurance, iPCM had a SET speed four times faster than a GST alloy at low power (9.5 mW). iPCM showed not only a prompted SET operation but also lower power consumption for the SET operation of 11 pJ for iPCM compared to 90 pJ for GST. Moreover, the RESET operation required 0.73 mA at 3.5 V for iPCM, compared with 1.25 mA at 6 V for a GST alloy at the same pulse width of 50 ns, and the endurance was >1×10^{10} cycles regardless of film thickness. In this study, thermal conductivity was estimated to be 0.33 W m^{-1} K^{-1} for iPCM and 0.21 W m^{-1} K^{-1} for a GST thin film, differing from previous reports. They explained the above phenomenon in terms of reducing the change in configurational entropy between SET and RESET states by controlling the local atomic switching of Ge atoms.[16]

Many studies of GeTe/Sb_2Te_3 SLL-PCM were carried out by industrial[76,77] and academic research groups.[17,78–82] Ohyanagi et al. fabricated a 50 nm diameter GeTe/Sb_2Te_3 superlattice, consisting of [GeTe (1 nm)/Sb_2Te_3 (4 nm)]$_8$, onto the bottom electrode. The GeTe/Sb_2Te_3 had a low RESET current of 70 μA and a high endurance of ~10^8 cycles with a fast SET speed of 10 ns.[76] From the same group, Takaura et al. introduced a novel topological switching
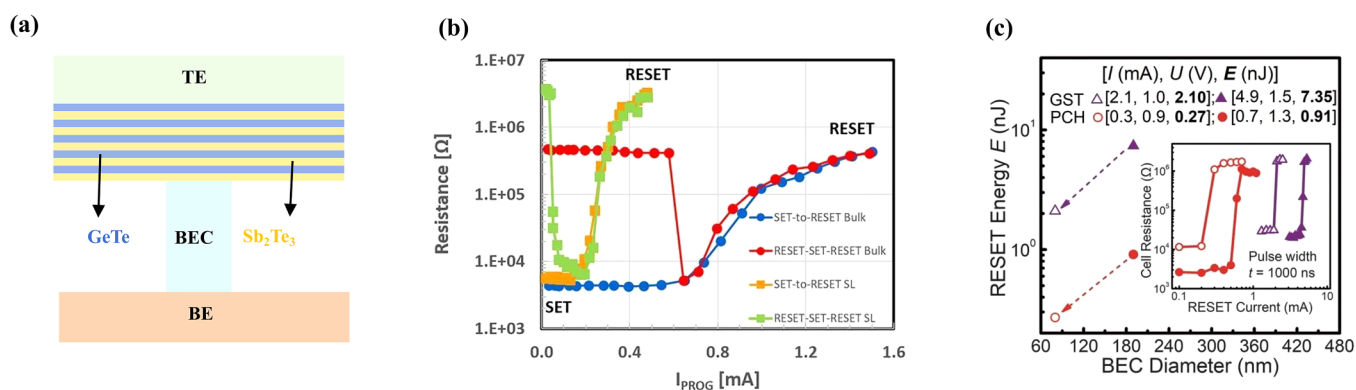

FIG. 4. Device performance of iPCM and HET-PCM. (a) Schematic of iPCM device. (b) Resistance as a function of an increasing programming current, starting from the SET state and from the RESET state for bulk GST and SL. Reproduced with permission from Boniardi et al., Phys. Status Solidi RRL **13**, 1970021 (2019). Copyright 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (c) Improved RESET energy, SET speed, and cycling endurance. RESET energy as a function of BEC diameter for the GST and HET-PCM devices. Reproduced with permission from Ding et al., Science **366**, 210 (2019). Copyright 2019 AAAS.

RAM (TRAM) with a low RESET voltage (0.6 V) compared with that of GST (1 V). The group also studied the switching mechanism of the GeTe/Sb_2Te_3 superlattice and revealed that the region around the top GeTe layer in the SLL-PCM was responsible for switching.[77] Additionally, they demonstrated a modified SLL-PCM structure consisting of Sb_2Te_3 (10 nm)/[GeTe (1 nm)/Sb_2Te_3 (1 nm)]$_5$/$Ge_{30}Te_{70}$ (3 nm), which had an even lower RESET current of under 60 μA.[78] In more recent studies, Mitrofanov et al. presented the temperature-dependent resistance change of [(GeTe)$_2$/(Sb_2Te_3)$_4$]$_8$ iPCM on a 3 nm Sb_2Te_3 seed layer. The iPCM showed a ~10^3 RESET/SET resistance ratio and over 10^7 cycles of endurance. During aging above 150 °C, resistance changed to a new resistance state with 400 times higher SET resistance. Therefore, they concluded that there were originally more than two atomic arrangements of iPCM related to the electrical properties.[79] Okabe et al. studied iPCM by preparing [GeTe (1 nm)/Sb_2Te_3 (4 nm)]$_{10}$ with Sb_2Te_3 as a starting layer on a TiN bottom electrode with a diameter of 80 nm. Varied thicknesses of the GeTe/Sb_2Te_3 basis showed a proportional relationship with thermal conductivity. They reported the TBR of GeTe/Sb_2Te_3 as ~3.4 m^2 K GW^{-1}, seven times lower than those of the GST/TiN and GST/SiO_2 interfaces. Moreover, thermal conductivity was measured as 0.4 W m^{-1} K^{-1}, which is lower than that of GST (~0.5 W m^{-1} K^{-1}). However, lower thermal conductivity could not fully explain the reduced RESET current; therefore, they supported it with void formation on the bottom electrode by atomic diffusion, which potentially makes Joule heating more effective.[17] Other groups investigated iPCM with the molecular beam epitaxy (MBE) technique. Boniardi et al.[83] showed that the GeTe/Sb_2Te_3 iPCM is indeed made up of GST and Sb_2Te_3 due to the intermixing across the interface between GeTe and Sb_2Te_3 layers. As shown in Fig. 4(b), such MBE-deposited iPCM showed a higher RESET resistance state compared with bulk GST. From the results, the RESET current of iPCM corresponds to 0.4–0.5 mA (1–1.5 mA for the bulk counterpart), and SET speed and operation energy were also reduced substantially. They suggested that increasing thermal resistance with the existence of van der Waals gaps is a key parameter for such high performance of the device. In these studies, the performance of the iPCM supported the melt-quenching process, which is different from other reports,[16,76,77] and the exact mechanism of the iPCM is still under debate in this regard.[84] The SLL structure could also reduce resistance drift, which is critical for operating MLCs.[85] In recent work, Zhou et al. showed a resistance drift of SLL-PCM of 0.02 for GeTe (4 nm)/Sb_2Te_3 (2 nm) and a further reduction of 0.006 for GeTe (2 nm)/Sb_2Te_3 (2 nm) compared with that for a GST alloy of 0.16.[81]

3. Stacking confinement layers between phase-change materials

Despite collective efforts to find evidence for order-to-order transition in SLL-PCMs, a convincing experimental observation for a non-melting phase transition has not yet been made. From DFT calculations and sophisticated TEM studies, there is some evidence for thermal-based transitions only. These studies considered that the low operating energy of SLL-PCMs is caused by the increase in thermal confinement due to multiple interfaces. Since then,

attempts have been made to optimize the properties of SLL-PCMs using different thermal confinement layers. There have also been many reports about a combination of two different PCMs or a combination of one PCM and one blocking layer, such as GaSb/Sb_4Te,[86] GeTe/Sb,[87] $TiTe_2$/Sb_2Te_3,[20,88] and V_2O_5/Sb,[89] with other SLL PCMs.[90–94] Most of the results reported enhanced thermal stability, reasonably good endurance over 10^7 cycles, and a higher on–off ratio.

Among them, Ding et al. reported the most remarkable device performance using a delicately designed multilayer HET-PCM with confinement layers. They chose a confinement layer under a well-defined selection rule: higher melting temperature, smaller in-plane lattice parameter, chemical stability, octahedral local atomic arrangement, high thermal resistivity, similar electrical resistance, and a compatible complementary metal–oxide–semiconductor process. Under these criteria, the confinement layers performed many functional duties, such as effective diffusion and thermal barriers, interface protection, promoting crystallization, and controlling the resistance window. $TiTe_2$, a transition metal dichalcogenide (MX$_2$), was employed as a confinement layer to simultaneously satisfy all of the properties (a T$_m$ of ~1470 K, a thermal conductivity of ~0.12 W m^{-1} K^{-1}, and a lattice constant of ~3.78 Å) and stacked with Sb_2Te_3 as the phase-change material (~900 K, ~0.78 W m^{-1} K^{-1}, and ~4.26 Å). The HET-PCM consisted of $TiTe_2$ (~3 nm)/Sb_2Te_3 (~5 nm) with a total thickness of ~69 nm. Owing to the diffusion barrier characteristics, the device showed reduced fluctuations in electrical resistance for both RESET and SET states compared with those of the GST-based device. In addition, thanks to the simple composition (binary) of quasi-2D Sb_2Te_3 blocks, the stochastic property was markedly reduced, leading to far more consistent conductance. The HET-PCM device also showed extremely low drift in the RESET state due to the diminishing content of Ge-related structural defects and nano-sized effects that suppress atomic diffusion dynamics near $TiTe_2$ walls. In addition, the low-resistance drift of ~0.005 was 50 times lower than that of the GST alloy (~0.11) by suppressing the through-plane heat loss during programming.[20] In Fig. 4(c), RESET energy was calculated as 0.91 and 7.35 nJ for the HET-PCM and GST alloy, respectively, at the bottom electrode with a diameter of 190 nm. When the diameter was reduced to 80 nm, the RESET energy was also reduced to 0.27 nJ and 2.10 nJ, respectively, via effective Joule heating. The power consumption of the HET-PCM was then reduced by more than 87% due to enhanced thermal barrier resistance and diminished melting region. Furthermore, the device showed ~8 ns SET speed at ~1.5 V, whereas the Sb_2Te_3 film required ~4 V for change at ~8 ns. Also, the endurance of ~2 × 10^9 was 3 orders greater than that of the GST alloy (~10^6 cycles).

In addition to such greatly enhanced performance, the HET-PCM device also showed a continuum of electrical resistance values, which can potentially be used for neuro-inspired computing. The continuous conductance change can be achieved by either the iterative RESET operation or the cumulative SET operation. More interestingly, owing to the high accuracy of the cumulative SET operation, it seems to offer more than 5 bits of distinctive MLCs. These memory cells already showed high accuracy vector–matrix multiplications and pattern classifications. Shen et al. also studied a [$TiTe_2$ (2.6 nm)/Sb_2Te_3 (8 nm)] SLL-PCM in comparison

with Ti-doped Sb_2Te_3 and $GeTe/Sb_2Te_3$ iPCM. Since this HET-PCM structure was not fabricated by delicate van der Waals epitaxy, both the Sb_2Te_3 and $TiTe_2$ layers suffered from intermixing of cations ($Sb_2Te_3 \sim 15$ at. %, $TiTe_2 \sim 10$ at. %). Considering the GeTe layer contained less than 30% of Ge atoms even in the center of the GeTe block in the SLL $GeTe/Sb_2Te_3$, and only 22 at. % of Sb atoms were visible in the Sb_2Te_3 block, the $TiTe_2/Sb_2Te_3$ multilayer did not show strong intermixing, which is possibly responsible for the long endurance property ($\sim 2 \times 10^7$ cycles). In addition, the RESET current density of the $TiTe_2/Sb_2Te_3$ was around 1.8 MA/cm^2, which is an order lower than the iPCM (~ 19 MA/cm^2), and it exhibited a much faster SET speed of 10 ns comparable to the cases of iPCM and GST alloys at the same required voltage.[88]

III. PHASE TRANSITION MECHANISM IN PCMs

A. Conventional PCMs

Earlier studies of phase-change materials using x-ray absorption spectroscopy showed evidence of different local structures between the crystalline and amorphous phases. In the crystalline phase, Ge atoms were octahedrally coordinated, and in the amorphous phase, they had a tetrahedral coordinated structure. To explain the fast reversible phase transition in GST, which has distinct local structures, the umbrella-flip model suggested an atomic flip transition of Ge atoms from octahedral to tetrahedral sites, triggered when the strain relaxation energy was sufficient, as illustrated in Fig. 5(a).[95] Both the amorphous and crystalline phases have many local structures, such as defective octahedral and pyramidal

local structures, especially in the case of amorphous GST, where only ~30% of Ge atoms exist on tetrahedral symmetry sites. Subsequent *ab initio* studies based on DFT showed inconsistent results with the umbrella-flip model.[96] Nevertheless, as will be seen in Sec. III B, the idea of the umbrella-flip model provided an important concept for iPCM.

Because all phases of GST within a PCM cell consist of various local structures and the resistance level is affected by the relative volume ratio, it is more difficult to describe the entire system with a simple phase transition model. Therefore, to describe the phase transition characteristics more statistically, a ring statistics analogy using *ab initio* simulations has been applied. Many studies reported that ABAB square fragments (A: Ge, Sb and B: Te) dominated the structure of amorphous GST,[97] and the crystallization process could be explained by ordering of the pre-existing disordered ABAB building blocks. In fact, the roles of vacancies are also important: the vacancies in amorphous GST provide the requisite space for crystallization to occur. ABAB blocks exist even at high temperatures (>1000 K). Because the concentration of ABAB blocks, which varies with temperature, determines the maximum cluster size of the connected square rings, it provides important information about the behavior of the crystallization characteristics of the PCM. As illustrated in Fig. 5(b), Kohara *et al.* claimed that even folded rings, especially dominant ABAB building blocks in melt-quenched amorphous GST, support fast crystallization speed. Owing to the reorientation of disordered ABAB squares, phase transition could be achieved without any broken bonds, as supported by *ab initio* molecular dynamics (AIMD) and reverse
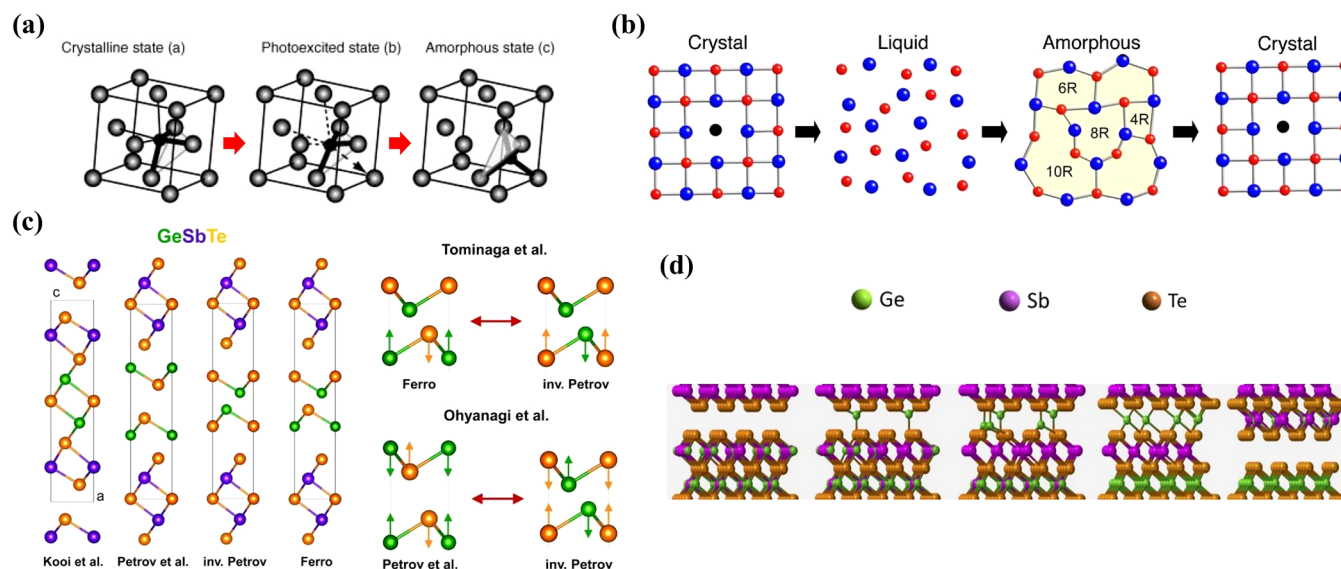

FIG. 5. (a) Schematic representation of the local structure in the crystalline, photoexcited, and amorphous states where a Ge atom (black circle) is shown within the Te fcc lattice (shaded circles). Reproduced with permission from Kolobov *et al.*, J. Non-Cryst. Solids **352**, 1612 (2006). Copyright 2006 Elsevier.[147] (b) The possible ring size transformation in a crystal-liquid-amorphous phase change (record) and an amorphous-crystal phase change (erase) operation in $Ge_2Sb_2Te_5$ and GeTe. Reproduced with permission from Kohara *et al.*, Appl. Phys. Lett. **89**, 201910 (2006). Copyright 2006 AIP Publishing LLC. (c) Structural and switching model of $GeTe$–Sb_2Te_3 superlattices. Adapted from Momand *et al.*, Nanoscale **7**, 19136 (2015). Copyright 2015 Royal Society of Chemistry. (d) Schematic representation of bi-layer switching triggered by Ge atom switching. Reproduced with permission from Saito *et al.*, Appl. Phys. Lett. **114**, 132102 (2019). Copyright 2019 AIP Publishing LLC.

Monte Carlo simulation.[98] In contrast, as-deposited amorphous GST showed that homo-polar (Ge–Ge, Sb–Sb) and Ge–Sb bonding were dominant and acted as crystallization nuclei.[99] Amorphization can be understood as a process in which a specific long bond (>bond cut-off distance) is broken and the central Ge atom changes from a symmetrical three-center Te–Ge–Te to an asymmetrical three-center Te–Ge–Te. This process can be viewed as ordered ABAB blocks being destroyed, resulting in disordered ABAB blocks. In addition, because these asymmetric Te–Ge–Te arrangements have lone-pair electrons at partially hybridized Ge, the amorphous phase can be stabilized by forming Ge–Ge bonds with other asymmetric Te–Ge–Te.

In the case of AIST, there was a broad distribution of numbered rings in the amorphous state, indicating a lack of crystallization nuclei and ABAB squared rings. Moreover, the local environments of Sb atoms showed similar distorted octahedral sites in both a- and c-AIST. Because of these results, crystallization in AIST was suggested as alignment of octahedral Sb bonds along the crystalline c-axis with small displacements of bond-interchange. The bond-interchange model indicated a growth-dominated recrystallization in AIST compared with GST.[99] Although the ring structure model is widely used to explain the phase transition of doped PCM, it is still difficult to fully explain the changes in various operating characteristics, such as thermal stability and SET speeds. In addition, because the phase transition mechanism changes from nucleation-dominant to growth-dominant in nano-sized PCMs, further improvements are required when using the ring structure to explain the phase transition mechanism of PCMs for various interface architectures.

B. HET-PCMs

A typical heterogeneous structure in PCMs is the SLL layer-by-layer design. It consists of alternating layers of 2D Sb_2Te_3 and 3D GeTe, separated by van der Waals gaps. In the earlier study of such SLL PCMs, the reduced thermal conductance across the interface could act as a thermal barrier; therefore, a more effective Joule heating process might be the main reason for phase transition, as in conventional GST.[75] However, iPCM showed higher thermal conductivity in the $GeTe/Sb_2Te_3$ SLL structure.[16] Its device endurance was less sensitive to different film thicknesses, and no atomic migration was observed via x-ray spectroscopy. These results might be in contrast with the atomic diffusion behavior of the GST alloy. Furthermore, the sub-2 nm thickness of the GeTe layers could reduce entropic loss. Kolobov et al. suggested local atomic switching of Ge atoms at the interface of two distinct PCMs, which caused efficient reduction of the configurational entropic loss.

Studies by Ohyanagi et al. and Takaura et al.[76,77] showed similar results to previous research. Hence, the phase change mechanism of the $GeTe/Sb_2Te_3$ SLL structure (GST-superlattice or GST-SL) was suggested by order-to-order transition. Generally, order-to-order transition was explained with four types of atomic structures: Kooi (with no quintuple layers, known as the most stable phase by DFT simulation at lower temperatures[100]), Petrov, inverted Petrov, and Ferro models, as shown in Fig. 5(c).[101] Note that vacancies and adjacent atoms could swap with each other and be replaced by van der Waals gaps in the GST-SL. The most

popular order-to-order transition models are the Ferro-to-inverted Petrov and Petrov-to-inverted Petrov models. The Ferro-to-inverted Petrov model suggests that the inverted Petrov structure (high-resistance state) is obtained by only one Ge atom flipping in the Ge–Te layers of the Ferro structure (low-resistance state),[102] while the Petrov-to-inverted Petrov model is represented by two Ge atoms flipping in the Ge–Te layers of the Petrov model.[82] Furthermore, atomic transition in the GST-SL was suggested by two steps of lateral motion of Ge, not in the vertical direction, to present the most stable atomic structure of GST-SL.[103] All of these mechanisms focus on Ge atomic transition with formation of van der Waals gaps, which is a similar concept to that of the umbrella-flip model.

However, cross-sectional high-angle annular dark-field imaging–scanning transmission electron microscopy (HAADF-STEM) of GST-SL showed the Kooi group[101] but no Petrov, inverted Petrov, or Ferro structures. Bang et al. suggested that a mechanism of iPCM should be modified because of the strong dependency of GeTe layers and lack of z-contrast in TEM images of iPCM.[102] In current studies, the evidence for GST/Sb_2Te_3 intermixing in the GST-SL structure is shown as Ge-enriched GST,[19] nine blocks of GST,[104] or hexagonal $GeSb_2Te_4$ layers.[105] Lotnyk et al. showed chemically driven intermixing between $GeTe/Sb_2Te_3$ with the fabrication of Ge-rich GST/Sb_2Te_3 structures at a low deposition temperature. Therefore, intermixed Ge and Sb atoms toward the van der Waals gaps could be one possible switching mechanism in iPCM.[19] Thanks to TEM studies on iPCM, there are new trials under way to determine the mechanism of $GeTe/Sb_2Te_3$, focused on the intermixing atoms between van der Waals gaps, which include ab initio DFT or MD simulations.

Basically, van der Waals gaps consist of vacancy sites; several types of vacancy-supported phase transition models for understanding iPCM can also be applied. As a modified form of the umbrella-flip model called Ge/Sb intermixing, Sb atoms should be interacted with vacancies besides the atomic transition of Ge atoms in iPCM. Saito et al. introduced Ge/Sb intermixing on the cation layer, which is crucial for phase transition in iPCM.[18] In the SET operation, long and low-intensity pulses suggest that pseudo-binary composition ($GeTe–Sb_2Te_3$) blocks, such as $Ge_1Sb_2Te_4$ or $Ge_2Sb_2Te_5$ blocks, are formed with a van der Waals gap at the center. This is supported by a previous TEM study on iPCM. In contrast, short and high-intensity pulses for the RESET operation would form non-pseudo-binary composition blocks, which would be quenched at the end of the programmed current. As shown in Fig. 5(d), the mechanism is explained by bi-layer switching across the nearest van der Waals gap, resulting in the resistance change. Starting from the hexagonal structure at the SET state, Te atoms near a van der Waals gap form numerous tetrahedral vacancies in the van der Waals gap. In that region, there are two asymmetric compositions of GST blocks, which are separated by the van der Waals gap. When the RESET pulse injects, Ge atoms in the Ge-rich GST block with enough thermal energy switch to the tetrahedral vacancy sites. After a critical quantity of Ge atom switch, Te layers slide across the van der Waals gaps, and energetically more favorable octahedral Ge atoms are automatically formed. This layer sliding results in the transformation of tetrahedral vacancy sites into octahedral vacancy sites. Sb atoms switch to the octahedral vacancy sites, leading to new van der Waals gaps with two

non-pseudo-binary GST blocks. As non-pseudo-binary composition breaks the electronic balance in GST blocks, it forms p-type and n-type GST blocks, resulting in the resistance change. In contrast to the above mechanism, Wang et al. argued that the role of Ge atoms for the switching mechanism in iPCM was not clarified. They fabricated Sb_2Te_3 with bilayer defects using magnetron sputtering and post-annealing to closely analyze Sb–Te intermixing. The Sb_2Te_3 thin film consisted of Te layers, each terminated with bilayer defects. Without Ge atoms in this sample, a swapped bilayer formed by Sb–Te intermixing. DFT calculations supported the idea that the intermixed structure had a relatively low energy cost compared with the non-intermixed structure. Therefore, they concluded that Ge atoms were not crucial, but Sb–Te intermixing showed a more essential role in stabilizing swapped bilayers.[106]

Subsequently, Han et al.[107] investigated Ge/Sb intermixing in iPCM using the four interfacial intermixing models, Kooi, Ferro, Petrov, and inverted Petrov, with different Ge/Sb intermixing ratios (25:75, 50:50, and 75:25). Different values of the intermixing ratio were chosen based on the results of TEM observations by different groups.[19,108] As the Ferro-based structure is known as the most favorable structure for iPCM at high temperatures,[103,109] that was the structure they chose for MD simulations. Interestingly, the results claimed that the first switching atom was dependent on the Ge/Sb intermixing ratio. For the 25:75 ratio, the Sb atom would first be switched in the phase transition mechanism. In contrast, for the 50:50 and 75:25 ratios, the Ge atom would take the role of the Sb atom. To elucidate this mechanism, the electron localization function of the relaxed intermixing models near the van der Waal gap suggested that the weakest bond in each structure may change Sb–Te to Ge–Te. From these simulation results, a discussion of switched atom priority in various iPCM operating situations is introduced.

Based on the device performance results of recent iPCMs, in 2019, Okabe et al. suggested that effective Joule heating was the main reason for the lower thermal conductivity in iPCM and void formation above the bottom electrode at high deposition temperatures.[17] In their study, the iPCM performance supported the melt-quenching process, which is similar to results from the Kooi group. Given the varying views, the phase transition mechanism in iPCM needs further debate.[84] In the case of order-to-order transition

models, they could be applied to designing a broad variety of engineered 2D van der Waals solids.[110]

Recently, the interfacially induced epitaxial growth of $GeSb_2Te_4$ on Sb_2Te_3 templates was introduced with $[(GST)_1/(Sb_2Te_3)_3]_{13}$. As the melting temperatures of GST and Sb_2Te_3 were 862 K and 998 K, respectively, the Sb_2Te_3 layer existed after the SET operation. AIMD results showed that the Sb_2Te_3 template GST could fully crystallize in 80 ps, while the GST template amorphous state could not. Thanks to more unpaired electrons with less anti-bonding on Sb_2Te_3 surfaces, a faster growth-dominant switching mechanism was suggested in GST/Sb_2Te_3 SLL.[111]

IV. FABRICATION AND DEVICE PERFORMANCE

A. Deposition and fabrication processing

Following the introduction of the $GeTe/Sb_2Te_3$ PCM in 2007, such superlattice PCM devices (SL-PCM) have been extensively studied for realizing high-performance, multi-level, low-power emerging NVM technologies.[16] Another simple HET-PCM structure can be realized by inserting atomically thin films, such as graphene[74] or transition metal dichalcogenides,[15] between the phase change materials and bottom electrode heater, forming a single hetero-interface with atomic sharpness. A major role of such 2D material-based interlayers in HET-PCMs is as a thermal diffusion barrier and a charge injector. Most recently, atomically sharp hetero-interfaces in $Sb_2Te_3/TiTe_2$ HET-PCM reportedly improved noise and drift characteristics.[20] Here, we focus on how to realize such HET-PCMs, mainly with complicated SLL structures, with deposition methods including the widely adopted PVD techniques, such as sputtering, molecular beam epitaxy (MBE), and pulsed laser deposition (PLD), as well as ALD.

The most widely investigated SL-PCM, $GeTe/Sb_2Te_3$, which has excellent phase transition memory characteristics, is fabricated by sputtering onto various substrates, e.g., Si (100) and (111), SiO_X, amorphous Si, WSi, TiN, Al_2O_3, and polymer substrates.[16,104,112–117] Sputtering produces highly oriented thin films on most substrates, even a polymer. As shown in Fig. 6(a), an out-of-plane XRD pattern shows highly (001) textured GST-SL films on Si (100).[112] In the Tominaga group's work,[116] sputtering deposition for SL-PCM
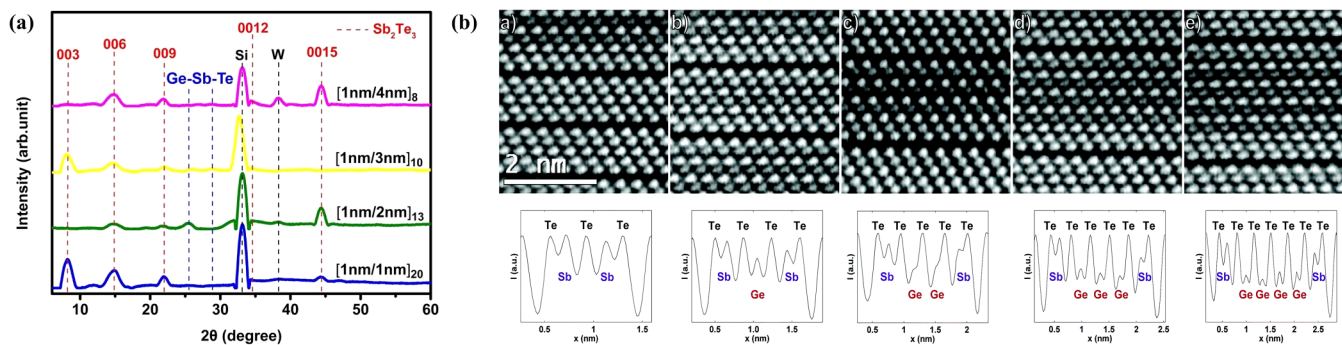

FIG. 6. (a) Highly (0 0 l) textured GST-SL films: out-of-plane XRD pattern. Reproduced with permission from Huang et al., Appl. Surf. Sci. **493**, 904 (2019). Copyright 2019 Elsevier. (b) Variety of vdW layers formed in the as-deposited superlattice. Several atomic columns already show evidence of Ge/Sb intermixing. Adapted from Momand et al., Nanoscale **7**, 19136 (2015). Copyright 2015 Royal Society of Chemistry.

generally consists of three steps. The first step is surface treatment. For example, Ar plasma treatment is used to remove the native oxide of the Si substrate surface or surface oxide of the electrode surface. The surface of the Si substrate becomes amorphous Si after the Ar plasma process. The second step is to form a seed layer. After depositing an as-grown amorphous Sb_2Te_3 film of $\sim$3 nm, heat treatment at $\sim$250 °C is performed. Due to differences in selective reactivity between Sb–Si and Te–Si, Te is the dominant chemical bond with the amorphous Si. As a result, an exclusive Te quasi-monolayer[117] is formed on an amorphous Si layer that supports the following growth of highly oriented chalcogenide films. In this case, thanks to the van der Waals nature of Sb_2Te_3, a highly crystalline thin film with >100 nm in-plane grain size and textured along [0001] can be acquired regardless of the substrates used for growth. When the seed layer is GeTe, it is reportedly known to obtain alloys, not superlattice structures, whereas a Sb_2Te_3 seed layer prior to SL-PCM improves the quality of textured crystalline films. As the third step, alternative deposition (GeTe/Sb_2Te_3) is conducted at the same temperature ($\sim$200–250 °C) with various units and total layer thicknesses. Optimal growth temperatures reported in the literature are in the range of 230–250 °C. Below 200 °C, amorphous or polycrystalline Sb_2Te_3 films are obtained, and above 250 °C, Te desorption impedes stoichiometric deposition. However, the GeTe layer is known to be thermodynamically unstable between Sb_2Te_3 slabs at a temperature of $\sim$250 °C, and most of the GeTe layers start to intermix with the Sb_2Te_3 slabs. As shown in Fig. 6(b), during the GeTe deposition sequence, some of the Ge atoms are replaced with the outermost Sb cation site in the Sb_2Te_3 block, and the Ge atoms gradually permeate into the center of the Sb_2Te_3 block because the central Sb cation site is energetically favored by the Ge atom, resulting in the formation of a GeTe layer in the Sb_2Te_3. Despite such intermixing, the sputtering method described above is considered to have the most advantages for making SLL structures compared to other deposition methods.

In addition, when Sb_2Te_3 is used as a single target, a thin film with Te deficiency often appears. A Te deficiency of greater than 4% leads to misorientation of the atomic planes of the superlattice by a few degrees with respect to the substrate. This can be beneficial for synthesizing stoichiometric superlattices under a Te-rich deposition environment by co-sputtering the Te target with Sb_2Te_3. Saito et al. recently described this approach as the most important strategy for preparing stoichiometric, well-oriented SL-PCM films. They demonstrated that stoichiometric films can be successfully obtained from an $Sb_{33}Te_{67}$ target with much increased x-ray diffraction peak intensity. Recently, Hippert et al. succeeded in depositing highly textured Sb_2Te_3 thin films on WSi, TiN, amorphous Si, and native and thermal silicon oxide layers. Because native oxide layers and polyimide substrates can also lead to the formation of a surface layer containing a few Te terminated planes, it is essential in the future to investigate the different principles behind the formation of a Te terminated layer on different substrates.

MBE growth requires a more delicate surface treatment; therefore, there are more restrictions on the choice of the substrate than with sputtering.[101,108,118–121] Of course, in the case of an amorphous substrate such as SiO_2, textured SL-GST can be synthesized if a substrate surface treatment, such as Ar^+ sputtering or exposure to a 20 keV electron beam, is performed. However, for most other cases, SL-PCM synthesis is performed using a $Si(111) - \left(\sqrt{3} \times \sqrt{3}\right)R30° -$Sb passivated substrate. Because the close-packed planes of Si and Sb_2Te_3 have lattice mismatches as large as $\sim$11%, GST-SL is typically grown on Sb-passivated Si(111). For example, in-plane twisted domains are observed in GST-SL films on a Si(111) substrate, while they are suppressed in GST-SL films on an Sb-passivated Si(111) substrate.[120] Using MBE, growth can be initiated with GeTe as well as with Sb_2Te_3, but lower interface roughness and narrower peaks are obtained when starting with Sb_2Te_3. In addition, many studies have been published directly showing that GeTe–Sb_2Te_3 superlattices reconfigure into alternating GST and Sb_2Te_3 when grown at the usual temperature of 230 °C and completely reconfigure into the trigonal structure of GST when annealed at 400 °C. This originates from the thermodynamic tendency of Ge atoms to diffuse into an Sb_2Te_3 slab.

For the PLD technique, the detailed process is described elsewhere,[19,122,123] and only a few points will be considered here. With PLD technology, prior to the growth of GeTe thin layers, a high-quality seeding layer of Sb_2Te_3 ($\sim$250 °C) is required on a Si(111) substrate. In the subsequent processes, there are also problems similar to those encountered by sputtering and MBE, such that, instead of GeTe/Sb_2Te_3 sequential layers, a GST/Sb_2Te_3 structure appears. To address this, a deposition method to minimize intermixing was attempted by reducing the temperature to $\sim$140 °C after forming the seed layer. GeSbTe building blocks were still observed, and intermixed GeSb also appeared in the outermost cation layer. Thus, despite various improved deposition methodologies, there are few convincing ways to make SL GeTe/Sb_2Te_3 without Ge–Sb intermixing in the cation layer. Considering that the most problematic part of PCM originates from the melt-quenching process of GST alloys, research on SL-PCM synthesis, which is essential for implementing the flipping process of a Ge–Te layer or TRAM, is very meaningful. Ding et al. reported recently the results of optimizing the thermal barrier layer properties of SL-Sb_2Te_3/$TiTe_2$, resulting in improved drift performance.[20] This study originated from a method to recognize and effectively utilize melt-quenched processes in SL-PCM. The synthesis method proceeds as that for SL-GeTe/Sb_2Te_3 except for the high temperature of $\sim$300 °C. The development of CVD or ALD[60,124] for SL-PCM formation is still in its early stages. The main targets of development for ALD-grown PCM thin films are the +2 oxidation state of the Ge precursor, the Te precursor with higher reactivity, the precursor for high density, and the development of process methods for stoichiometric as-deposited films. That is, the main goal is to synthesize an improved thin film alloy of GeTe–Sb_2Te_3 tie-line, and recently, attempts have been made to prevent phase separation with GST124, Sb_2Te_3, etc., even after the subsequent heat treatment. From the superlattice point of view, the chemical adsorption capacity of elements is insufficient compared to those of other thin films; therefore, the intermixing and alloying problems appear to be more serious than in any other PVD-based as-grown thin films. At the current level, following the quality of sputtering, a GST alloy is a realistic goal, and the development of a superlattice thin film is not expected in the near future.[60,124]

B. Device performance

In Sec. II, we discussed the device performance of various phase-change materials, such as doped PCM and SLL-PCM. For

device applications based on PCMs, a few key performance parameters, including (1) thermal stability and SET speed and (2) resistance drift and RESET current density, should be considered.

1. Thermal stability and SET speed

Thermal stability is a fundamentally important parameter for memory devices to retain their information under dynamic thermal cycles.[125] For phase-change materials, thermal stability is generally considered for the amorphous phase. When a sufficient amount of heat is supplied either during a read operation or from adjacent cells, the amorphous phase tends to be reconstructed by local crystallization. As a result, the RESET resistance becomes reduced, and the data recorded in the phase-change material can be unintentionally perturbed. In a memory device, one major parameter for gauging thermal stability is the retention temperature ($T_{10years}$), which is defined as the available data retention temperature for 10 years. The retention temperature can be determined from the Arrhenius equation, $t = \tau \exp(-E_a/k_B T_{10years})$, where τ is a proportional time constant and E_a is the activation energy of crystallization. The failure time (t) is defined as the time taken for the initial resistance value to drop by half, which is usually 10 years.

The superior thermal stability observed in HET-PCMs recently has drawn much attention.[126,127] Basically, as the surface-to-volume ratio increases, the interfacial energy plays an important role for various material properties including the phase transformation characteristics. Recently, Wang et al.[127] showed enhanced phase-change properties in terms of size and interfacial effects. In their work, the crystallization temperature T_c of the Sb_2Se increases as the film thickness decreases, especially below 10 nm. The increase of the surface area-to-volume ratio leads to an increase in the activation energy, which is in good agreement with the model based on the Gibbs free energy calculation.[128] In addition, the VO_2-covered Sb_2Se film has a higher T_c than the uncovered film, which is due to the fact that additional interface energy generated by the interface layer enhances the nucleation barriers.[129] Typically, the crystallization temperatures are closely related to thermal stability of the material. According to the Arrhenius equation, the 10-year data retention temperature increases with decreasing thickness and the VO_2-covered films have slightly longer data retention than the uncovered ones. In addition, the crystallization behavior can be obtained from temperature and thickness dependent resistance data. The kinetic exponent (n) determined from the Johnson–Mehl–Avrami (JMA) model[130] reduces to around 1.5 as the film thickness decreases from 50 nm to 2 nm. The kinetic exponent value seems to decrease monotonically with increasing temperature, which means that the crystallization process changes gradually from the nucleation-dominated mode into a nucleation-grain-growth hybrid mode.[131] Specifically, the crystallization behavior of an ultrathin film (2–5 nm) can be characterized as the 1D growth-dominated mode with a high crystallization rate.[132] In addition, as the film thickness increases from 2 nm to 50 nm, the average kinetic exponent initially increases and then decreases. This slope variation is due to the size effect of the film.[133] This also supports the notion that the crystallization behavior can change from a 1D growth-dominated mode for 2 nm and 5 nm thin films to a nucleation-grain-growth hybrid mode for

thicker films. This mechanism change leads to a reduction in critical crystalline cluster size, which is associated with the energy barrier between amorphous (amor) and crystalline (cry) states. Consequently, the reduced surface of the related crystalline-amorphous boundary leads to a decrease in the energy barrier for crystallization E_B.[134] The crystallization rate typically enhances with decreasing E_B, and therefore, scaling the thickness diminishes the crystallization time of PCM. The influence of an interfacial layer (IFL) on the crystallization time of PCMs can be explicated by the formation energy of a crystalline cluster of size. A threshold size of the crystalline cluster exists at which the IFL/cry-PCM interface energies are comparable to the IFL/amor-PCM interface energies. This means that the IFL/amor-PCM interface energy dominates the change in total free energy when the film thickness is larger than the threshold size of the crystalline cluster. Consequently, the energy barrier for crystallization will be reduced owing to the decreasing IFL/cry-PCM interface, providing an acceleration of the crystallization rate. For those reasons, both the PCM thickness decrease and the coverage of IFL can lead to a reduced crystallization time.

2. Resistance drift and RESET current density

In Sec. IV B1, the improvement of SET speed and thermal stability of heterogeneously structured PCM was described from the viewpoint of crystallization kinetics. Of course, the SET operation can be further explained in terms of thermal efficiency, but this section focuses on reset current density and drift, describing the functional aspects of the thermal barrier of IRF and atomic-level chemical aspects.

Resistance drift is the phenomenon of increasing resistance as the structure relaxes, arising from volume expansion of amorphous states in PCM. This phenomenon can be described based on the power law dependence equation $R(t) = R_0 \left(\frac{t}{t_0}\right)^\nu$, where ν represents the resistance drift coefficient.[3,135] The time-dependent changeable resistance can interrupt and destroy the MLC system, as determined by individual resistance levels. Resistance drift is thus very important in implementing stable MLC devices.[136] The resistance drift of various PCM devices is compared in Figs. 7(a)–7(c). The resistance drift coefficient of amorphous GST (a-GST) is known to be 0.101.[25] For a closer look at the doped PCM cases, carbon- and nitrogen-doped PCM are shown. C-doped GST had good device performance, but its resistance drift was much higher than that of GST.[27] In contrast, N-doped GST had a low-resistance drift of 0.023 similar to that of TST.[136] The other two binary alloys, a-$Ge_{15}Te_{85}$[137,138] and a-Sb_2Te_3,[20] showed low-resistance drift in the range of ~0.05–0.07. Further reduction occurred by TST, which had a resistance drift of 0.02.[139] In contrast, heterogeneous structures, such as iPCM and HET-PCM, have much lower resistance drifts compared to homogeneous PCM. GeTe/Sb_2Te_3 iPCM had a value of 0.006, as mentioned in Sec. II.[81] The most effective resistance drift was improved by $TiTe_2$/Sb_2Te_3 devices with the remarkably low value of 0.002.[20] Ding et al. suggested two reasons for the low drift in a HET-PCM device. First, the HET-PCM presents simplified chemical bonding and structural motifs in amorphous Sb_2Te_3 compared with other PCMs. Considering sheet resistance
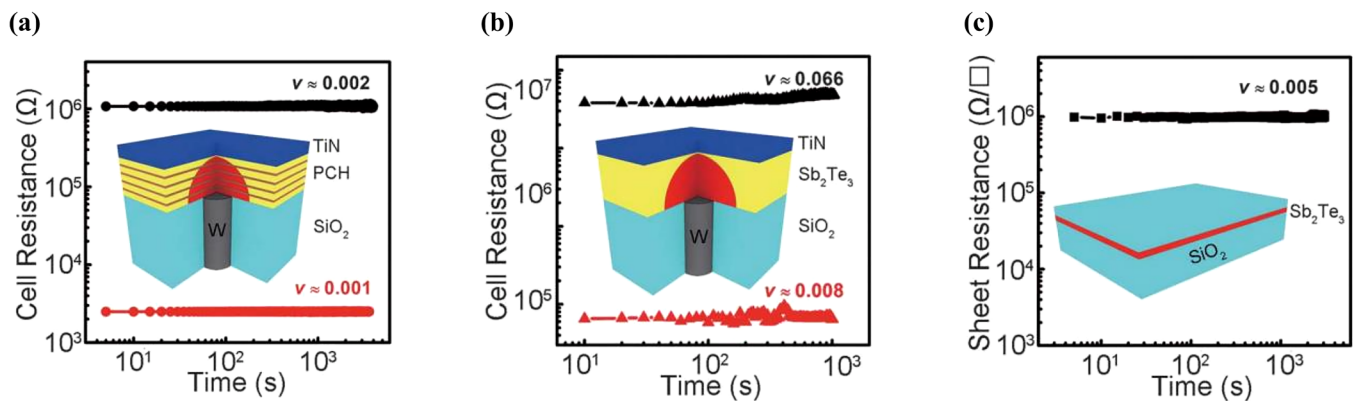
FIG. 7. (a) Cell resistance as a function of time for the RESET and SET states of the PCH device. (b) Cell resistance as a function of time for the RESET and SET states of a ~150 nm-thick Sb_2Te_3 device. (c) Sheet resistance as a function of time for a ~5 nm-thick amorphous Sb_2Te_3 thin film sandwiched between SiO_2 layers. Reproduced with permission from Ding *et al.*, Science **366**, 210 (2019). Copyright 2019 AAAS.

data in Fig. 7(c) where only an ~5 nm Sb_2Te_3 thin film is sandwiched by SiO_2 layers, regardless of the optimized thermal barrier layer, the sheet resistance can be considered to be due to the characteristics of Sb_2Te_3 itself. In addition, in the case of Sb_2Te_3, this does not apply at all since the resistance drift in GeTe and GST alloys is caused mainly by the diminishing content of Ge-related structural defects such as tetrahedral Ge motifs and the reinforcement of structural distortion of octahedral motifs.[140] Second, the nanosize effects can change the structural relaxation dynamics.[141] Specifically, from the DFT calculation, the Te–Te antibonding interaction between the wall and the nearby Te–Sb–Te bonding pairs of Sb_2Te_3 hindered the reinforcement of structural distortion toward the walls. This also resulted in quenching of atomic diffusion dynamics of supercooled Sb_2Te_3 liquids and restricting structural relaxation. Interestingly, Ding *et al.* also showed a dramatic reduction in power consumption for the RESET operation.[20] As earlier shown in Fig. 4(c), they experimented with various electric current pulses of 1000 ns (t). The RESET energy (E) was calculated as $E = I \times U \times t$ (where I is the RESET current and U the RESET voltage). The RESET energy was 0.91 nJ and 7.35 nJ for the HET-PCM and GST devices, respectively. Decreasing the diameter of the BEC from 190 nm to 80 nm, the RESET energy reduced to 0.27 nJ and 2.10 nJ, respectively. They partly attributed the dramatic enhancement in power consumption to partial melting in the Sb_2Te_3 and unchanged $TiTe_2$. The $TiTe_2$ confinement layers show also enhanced TBR properties, suppressing the through-plane heat loss during programming.

C. Perspective for future device performance

In this section, device performance of various phase change materials has been discussed, including thermal stability, endurance, RESET current density, SET speed, and resistance drift. Discussion of the material design aspect suggested both SLL structures and doped SbTe families have potential for good device performance, though there are still some trade-off issues, such as SET speed and thermal stability. In contrast, HEP-PCM with a

confinement layer or a thermal barrier has the potential to enhance device performance effectively with the SLL structure. Therefore, a HET-PCM based on Sb_2Te_3 is expected to result in remarkable PCM devices. Introducing a fast operation speed and a lower drift coefficient might be beneficial for neuromorphic devices. However, there is still a lack of research on the thermal stability issues of both iPCM and HET-PCM, and further study is required. Nevertheless, heterogeneous phase change materials, especially those introducing various van der Waals gaps with a thermal stability layer, are suggested for future studies.

In contrast, the cell design discussion in Sec. II A 2 included a dash-type confined structure for implementing high-density devices on a limited chip area for 3D stacking. Normally, both homogeneous and heterogeneous PCMs, as discussed in Sec. II, are fabricated by PVD, especially sputtering, limiting the BEC area. However, Zhu *et al.* claimed that the lower contact size of conventional PCMs leads to a high RESET current density, which is not desirable for use with OTS materials.[142] The reported OTS materials commonly operate at under 10 MA/cm². As heterogeneous PCM has the potential to reduce the RESET current density compared with GST, future study of the fabrication of heterogeneous PCMs with CVD or ALD is required.

V. EMERGING APPLICATIONS: PCM IN NEUROMORPHIC DEVICES

Various emerging memory devices have been tested recently for their suitability in neuromorphic devices. As shown in Fig. 8(a), a cross-bar array is a prototypical synapse network in neuromorphic chips to facilitate the simultaneous integration of multiple presynaptic neuron signals passing through each synapse for generating post-synaptic neuron signal. Because "learning" is represented as a formation process of specific synaptic weight patterns in the network, a rule of changing synapses (i.e., learning rule) has to be provided explicitly. One of frequently demonstrated learning rules is STDP (spike-timing dependent plasticity), indicating a synaptic weight change (Δw) depending on the temporal difference
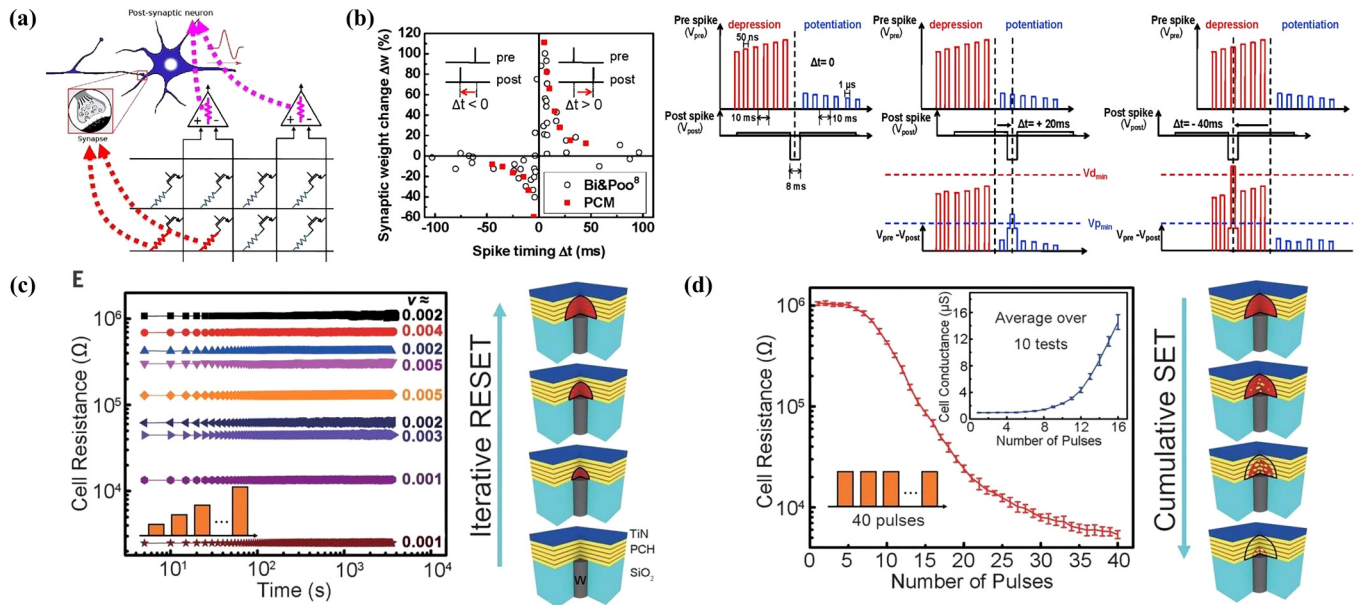
FIG. 8. (a) Schematic image of biological neuron and neuromorphic chip arrays. Excitatory and inhibitory postsynaptic potentials are delivered from one neuron to the next through chemical and electrical messaging at synapses, driving the generation of new action potentials. Adapted from Burr *et al.*, Adv. Phys. X **2**, 89 (2016). Copyright 2016 Informa UK Ltd. (b) Implementation of STDP with a two-NVM-per-synapse scheme. Reproduced with permission from Kuzum *et al.*, Nano Lett. **12**, 2179–2186 (2012). Copyright 2012 American Chemical Society. (c) Iterative RESET operations of HET-PCM. (d) Cumulative SET operations of HET-PCM. Reproduced with permission from Ding *et al.*, Science **366**, 210 (2019). Copyright 2019 AAAS.

(Δt = post-synaptic spiking − pre-synaptic spiking) as shown in Fig. 8(b) (left). STDP can be implemented in PCM when presynaptic and post-synaptic spikes are represented as amplitude-modulated pulse train with positive voltages and a single pulse with a negative voltage. According to the timing of both spikes, an effective voltage can cross the threshold voltages Vp_{min} or Vd_{min} for potentiation ($\Delta w > 0$) or depression ($\Delta w < 0$), respectively, in Fig. 8(b) (right). Some device characteristics are summarized in Table I,[143] including device performance, reliability, and suitability

for neuromorphic devices. PCM is essentially different from other NVMs in that it has a high on/off ratio and good retention. Its endurance is inferior to that of MRAM but slightly better than that of resistive random-access memory (RRAM). In particular, PCM has been found to be suitable for a deep neural network (DNN) inference. The reason for its good on/off ratio and retention is that the basic switching mechanism is a first-order phase transition process between two defined states. In addition, even with a large on/off difference, the on-state resistance is high. Thus, the reading

TABLE I. Summary and comparison of neuromorphic device technologies in terms of performance, reliability, and their suitability for DNN training, DNN inference, and SNNs. [Ielmini and Ambrogio, Nanotechnology **31**, 092001 (2019). Copyright 2019 Author(s), licensed under a Creative Commons Attribution (CC BY) license.]

	RRAM	PCM	MRAM	FeRAM	Li-ion
ON/OFF ratio	20–50	10^2–10^4	1.5–2	10^2–10^3	40–10^3
Endurance	10^5–10^8	10^6–10^9	$>10^{12}$	10^{10}	$>10^5$
Retention	Medium	Large	Medium	Large	…
Drift	Weak	Yes	No	No	No
Linearity	Low	Low	None	None	High
Integration density	High	High	High	Low	Low
Energy efficiency	0.1–1 pJ/bit	10 pJ/bit	100 fJ/bit	100 fJ/bit	100 fJ/bit
Switching speed	<10 ns	10–100 ns	<10 ns	30 ns	<10 ns
Suitability for DNN training	No	No	No	No	Yes
Suitability for DNN inference	Moderate	Yes	No	No	Yes
Suitability for DNN algorithms	Yes	Yes	Moderate	Yes	Moderate

operation energy is low; therefore, it is considered to be highly advantageous for DNN inference, which requires a large number of read operations for highly integrated PCM.

On the contrary, the two definite states of PCM increase the switching energy and reduce the switching speed. Moreover, the amorphous state is strongly affected by resistance drift. The reason for the high write energy is that it is required to reach the melting point of the phase transition material in the melt-quenching process, which is RESET switching; and the glass transition process, which is SET switching, requires sufficient time for atomic ordering.[3] Because the PCM switching process uses thermal energy as the driving force of the phase transition, it can be explained as structural relaxation due to latent heat after phase transition. Device imperfections are a common problem that must be addressed for applications in neuromorphic devices, although they vary slightly by memory devices.

A large on/off resistance difference can increase the amount of information that can be processed at once by a crossbar array, which is popular in neuromorphic computing architectures. For example, if there is a 100-fold difference between two states in resistance, the number of PCMs in on and off states can be determined easily from the accumulated resistance of ten PCMs. However, it is not easy to distinguish between 100 PCMs being off and 1 PCM being on due to the small difference in resistance. Although PCM shows a much larger on/off ratio than RRAM or MRAM, it is difficult to maintain a high on/off ratio while implementing the multi-level analog behavior required in a neuromorphic system. To solve this problem, multi-cell methods have been used. However, in superlattice structures, stacked PCM layers can be switched sequentially with less interference from each other, similar to the multi-cell method. Thus, although the possibility of large on/off and multi-level operations in superlattice structures has been confirmed, it is still approximately 5-bit (32 levels), and symmetrically reversible operation remains a major challenge.

In terms of retention, PCM is rated to have better retention characteristics than RRAM or MRAM. However, neuromorphic devices require a high-temperature environment due to the heat generated by the high-density array. Retention is an indicator of neuromorphic device performance for inference. When learning is complete and the information recorded in the PCM begins to deteriorate because of temperature, it is fatal because a neuromorphic computing system can lead to false inference. As described in Sec. IV, we could see improvements in thermal stability in doped systems and superlattice structures, but because of the presence of tradeoffs such as endurance degradation, a comprehensive assessment of thermal stability is urgently required in various material groups with heterogeneous structures.

Neuromorphic computing systems require a high-density synaptic device array with a large number of write operations. The devices proposed to date are not suitable for training yet because of their lack of endurance. When operating as a conventional memory device, even if the endurance is slightly lowered, the resistance state could be corrected through various methods, such as write-and-verify. However, in the case of a neuromorphic system, because high-density arrays are required, interference between many cells cannot be avoided, making it difficult to use conventional methods. In particular, because such systems operate as

multi-level or analog-like, endurance is a more difficult problem to address. Nevertheless, we have seen endurance improvements to $\sim 10^9$ cycles in iPCM and HET-PCM.[16,20] As the interface acts as a thermal barrier, heat is well confined, and the crystallization and metal-quench processes can proceed stably. Thus, adequate heat control is a shortcut to making neuromorphic devices suitable for training by improving their endurance.

The synapses that make up the human brain work at a time-scale of several milliseconds and are known to consume ~ 10 fJ per synaptic event.[144] On the surface, neuromorphic devices operate at a higher speed than biological synapses, but they also consume incomparably higher energy and so are much less efficient. Some studies have focused on reduction of the energy consumed per synaptic event.[145] Organic field-effect transistors have also been used for artificial synapses operating at very low energies (~ 1 fJ), and it has been reported that up to 1 aJ is possible in magnetic Josephson junction devices. In contrast, PCM requires a relatively high RESET current compared to RRAM and MRAM, and the SET speed is low. As a result, both RESET and SET require high operating energy. Compared to conventional GST, $TiTe_2/Sb_2Te_3$ systems have low RESET currents and high SET speeds while preserving endurance and the on/off ratio. Therefore, although there has been some improvement in the heterostructure, there is a need to further improve the RESET current and SET speed through fusion with other technologies as well as using other materials and structures.

Resistance drift is much higher in PCM than in other memory devices. In the amorphous state, resistance increases with time; this is not considered a major disadvantage in conventional memory devices due to two resistance states becoming more distinguishable. In a multilevel operation, resistance drift is a fatal problem in PCM devices.[146] Because the resistance state originally recorded may be read differently over time, some techniques to combat this problem have been studied. For example, even when resistance drift occurs, the order of resistance values does not change; therefore, a method such as introducing a reference resistance for resistance value comparison can be used. However, because neuromorphic devices require much higher levels than 2-bit and are expected to accelerate computation through vector–matrix multiplication, it is still difficult to use conventional methods. In addition, because the resistance drift coefficient is known to have a dependence on the initial resistance value and temperature, many studies have been conducted to suppress the drift phenomenon rather than using a complementary method. Among them, the reduction of the drift coefficient observed from binary alloys Ge–Te and Sb–Te, TST, $GeTe/Sb_2Te_3$ iPCM, and $TiTe_2/Sb_2Te_3$, compared to conventional GST, shows the possibility of controlling the resistance drift through material design and device structure. Particularly, $TiTe_2/Sb_2Te_3$ performed stable states at iterative RESET operation and high linearity at cumulative SET operation as shown in Figs. 8(c) and 8(d). In particular, because resistance drift is understood as a structural relaxation process, heterogeneity as an atomic confinement barrier as well as a thermal barrier plays a key role in the utilization of PCM in neuromorphic devices.[20]

Thus far, only the intrinsic characteristics of PCM devices and their potential in neuromorphic devices have been discussed. Heterogeneity overcomes the limitations of existing PCM to a great extent, but there are still some technical challenges that need to be

addressed. Based on the advantages of PCM, such as definite resistance states, we hope to achieve innovative research results in RESET current and SET speed related to minimizing operation energy for use in future neuromorphic devices.

AUTHORS' CONTRIBUTIONS

W.Y. and N.H. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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