Doctoral Thesis

Strained Silicon Fin-Based High Electron Mobility Transistor for Optimal Device Design of Performance and Reliability

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Approved by

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Abstract

I present the predictions of scaling and process variation for a strained-silicon (s-Si) fin-based high electron mobility transistor (FinHEMT) with well-tempered, short-channel characteristics. The operation principle of FinHEMT, which the SiGe behaves as an additional insulator forming quantum well (QW) channel in s-Si with the conduction band off-set improving the effective electron mobility, is clearly shown. By calibrating with experimental data, the high electron mobility (~1100 cm^2/Vs) and enhanced effective mobility (up to 2×) of the FinHEMT is predicted by suppressing the surface roughness scattering effect in the s-Si QW channel.

An extensive simulation is performed to find the optimized structure. The Si capping layer is replaced as high-κ dielectric insulator to prevent the gate leakage current, and undoped SiGe layer is eliminated because the conduction band off-set (ΔE_C) is enough to confine the electrons in s-Si QW channel. The parameter analysis is performed for both long and short channel regime of FinHEMT. Eventually, suppressed OFF-current (I_{OFF}) and improved ON-current (I_{ON}) with enhanced mobility can be achieved by fabrication process optimization and 10^{19} cm^{-3} of doping concentration and 2 nm thick of SiGe. Especially in short channel regime, maximized I_{ON} and gate controllability clarify the FinHEMT optimization.

With enhanced effective mobility, excellent scalability of the FinHEMT I_{ON} > 1.1 mA/μm at L_G= 10 nm is predicted because the high channel mobility can reduce the series resistivity in the scaled device. Owing to this low series resistivity, The FinHEMT has little effect on the process variation. Moreover, the unique operation principle of FinHEMT, which the part of doped SiGe layer behaves as an additional high-κ dielectric insulator, enhances the hot carrier reliability of FinHEMT by suppressing gate leakage current.

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Nomenclature

FET	Field-effect transistor
Si	Silicon
HEMT	High electron mobility transistor
FinHEMT	Fin-based high electron mobility transistor
FinFET	Fin-based field-effect transistor
SRS	Surface roughness scattering
s-Si	Strained-silicon
HK	High-κ
QW	Quantum well
sSOI	strained silicon-on-insulator
HCI	Hot carrier injection
RD	Reaction-diffusion

1. Introduction

1.1 Transistor scaling technology

1.1.1 Mobility degradation

Multi-gate transistors such as Fin-based field effect transistor (FinFET) and tri-gate field effect transistor are adopted as a mainstream technology to sub-10 nm due to its good gate controllability [1]-[4]. FinFET has been successfully scaled down to the state-of-the-art 5 nm technology node [5] using metal gate and high-κ dielectric material. It is possible to make thick gate oxide with scaled down gate capacitance (C_G) preventing gate dielectric tunneling and more aggressive gate oxide thickness scaling satisfies the device's target performance such as ON-current (I_{ON}), OFF-current (I_{OFF}) and ON/OFF current ratio (I_{ON}/I_{OFF}). While scaling in sub-5 nm node, however, the I_{ON} of FinFET is saturated around at or below 1 mA/μm [6]-[8] because of the universal effective mobility (μ_{eff}) degradation dominated by surface roughness scattering (SRS) [9][10] and the increased series resistance by the gate underlap structure [11]-[13] between the source and drain to suppress the short channel effects such as drain induced barrier lowering (DIBL), threshold voltage roll-off ($V_{T,roll\text{-}off}$), and gate induced drain leakage (GIDL) (underlap length X_{ud} is where the physical gate length L_g is less than the effective gate length L_{eff}, i.e. X_{ud} is negative).

1.1.2 Reliability degradation by hot carrier injection

Although the aggressive scaling of gate oxide thickness achieves the target performance of devices, it causes the gate leakage current by hot carrier injection (HCI) from channel to insulator. HCI can be occurred by high electric field at drain side in short channel regime as shown in **Figure 1.2**. The injected hot carrier breaks off the hydrogen bond in the insulator and channel interface and the interface trap is formed by this hydrogen ion. Recently, interface trap formation is explained with reaction-diffusion (RD) theory [14] with fitting parameter of reaction constant (v) by electric field and HCI [15]. And the gate leakage current generation can be calculated by multiplication of hot carrier injection probability (P_{ins}) as a function of the mean-free path in insulator (λ_{ins}) to the drain current.

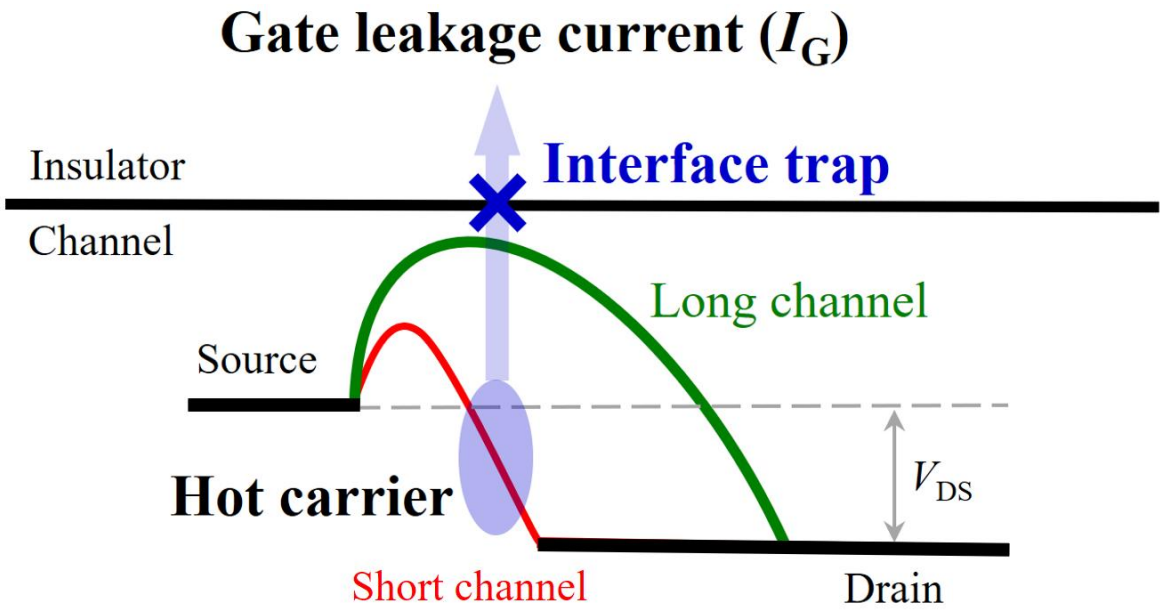

Figure 1-1. Interface trap formation and gate leakage current mechanism by hot carrier injection.

The mean-free path in insulator does not considered as a variable in Sentaurus TCAD, while it is reported as a function of inversion charge and lattice temperature [16]. In section 4.4, the effects of λ_{ins} on FinFET and FinHEMT is shown. Also, the device lifetime (τ_D), gate leakage current variation (ΔI_G), drain current variation ($\Delta I_{D,}$) substrate current variation (ΔI_{sub}) and interface charge trap density (N_{it}) are extensively verified with Sentaurus TCAD simulation comparing experimental data.

1.2 Boost-up the channel mobility

1.2.1 Compound/Ge MOSFET

Recently, new channel materials such as III-V compound semiconductor with high electron mobility for *n*-channel [17]-[19] and Ge with high hole mobility for *p*-channel [20]-[23] have been introduced on Si platform to boost-up channel mobility for high-performance CMOS but, the experimental values of μ_{eff} on III-V/Ge inversion channel are significantly degraded from their intrinsically high bulk mobility values [24]-[26]. The expected manufacturing cost increase would be additional burden in economic aspects.

1.2.2 High electron mobility Transistor (HEMT)

To overcome the limitations in compound semiconductor MOSFETs, strained-silicon (s-Si)-based high electron mobility transistor (HEMT) minimized gate field effect by quantum-well (QW) channel is reported [27]-[29]. The electrons in channel can be accumulated by the lower conduction band energy of Si than that of SiGe. Eventually, the electrons in channel transferred from doped SiGe layer can flow from source to drain, thus, there is less gate electric field degrading the electron mobility. Even though the channel mobility is enhanced, however, the gate off-leakage current is significantly increased through a Si capping layer with a relatively low bandgap [30]. Figure 1.1 shows the schematic structure explaining the operation principle of s-Si HEMT.

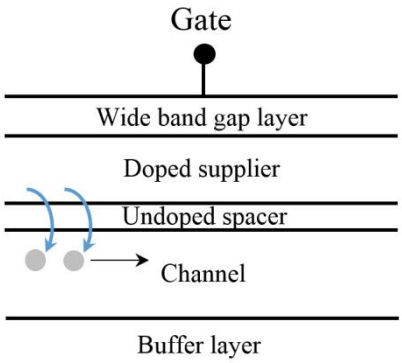

Figure 1-2. Operation principle of HEMT.

1.2 Motivation

To adopt the advantages that excellent gate electrostatic of FinFET and high electron mobility of HEMT, a novel s-Si FinHEMT is proposed. FinHEMT is feasible by introducing a SiGe layer between the high-κ (HK) gate dielectric insulator and s-Si channel of FinFET. The inserted SiGe layer forms the conduction band offset (ΔE_C) to separate the channel from the gate dielectric/channel interface by confining the electrons in the s-Si quantum well (QW) channel, resulting in effective suppression of the SRS effect. Enhanced effective mobility can break through the ON-current limitation of FinFET degrading the series resistance.

In this paper, we present a careful study on the device performance and hot carrier reliability of FinHEMT with optimized device structure. Our simulation reveals that the proposed FinHEMT can achieve enhanced mobility close to the Si bulk mobility. To analyze the variability and scalability of FinHEMT, the effects of various device parameters were extensively investigated. Moreover, the reliability of FinHEMT is improved compared with FinFET considering exact modeling of mean-free path and thickness of insulator.

2. Fabrication process

Fabrication process and its optimization

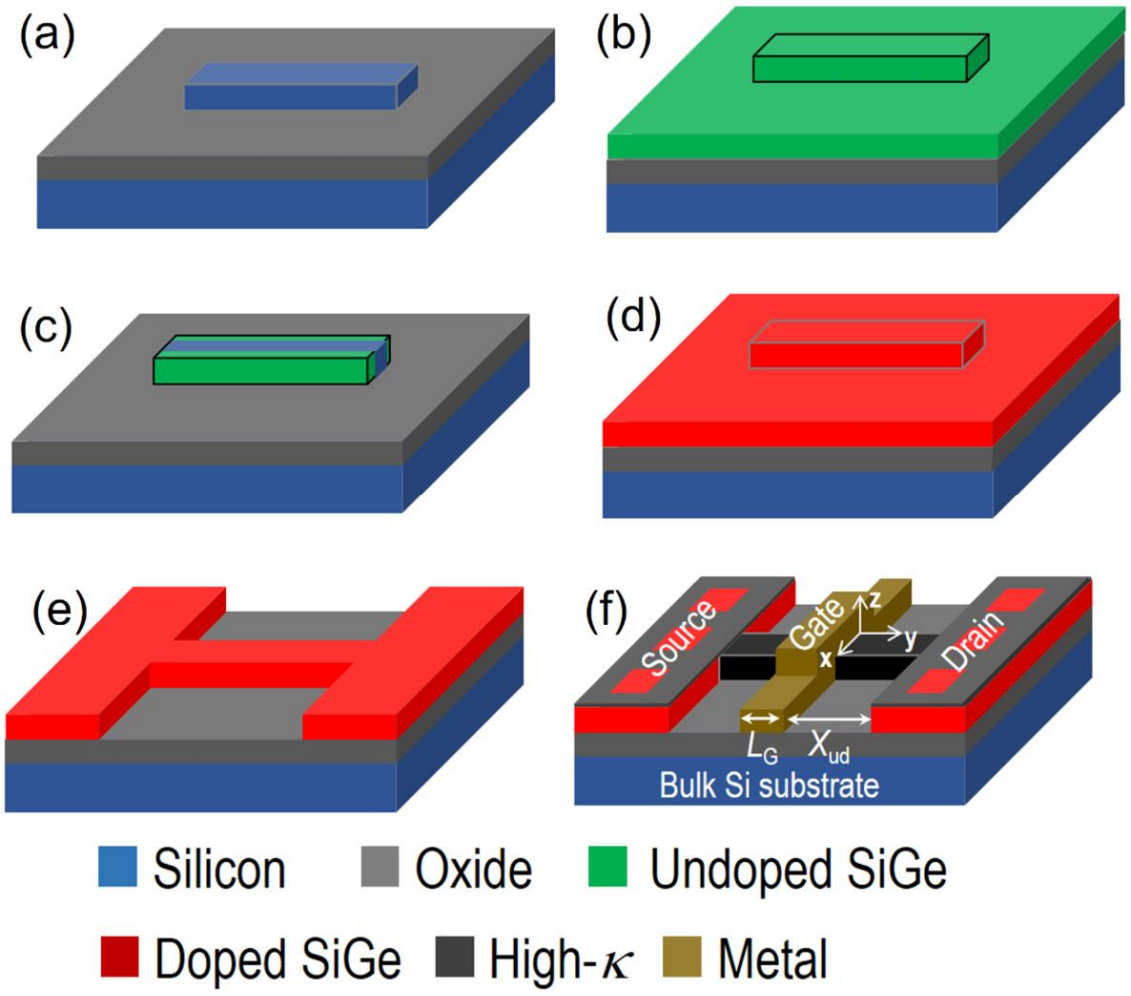

Figure 2-1. Fabrication process (a) Fin-first, (b) undoped SiGe deposition, (c) undoped SiGe etch, (c) doped SiGe deposition, (d) etching the doped SiGe layer as Source/Drain reservoir, and (f) final structure of proposed FinHEMT with device dimension parameters.

Figure 2-1 shows the proposed novel FinHEMT fabrication process [31] for advantages combination of both FinFET and HEMT which are good gate controllability and high electron mobility respectively. Basic platform of FinHEMT is s-Si on insulator (sSOI) substrate. Firstly, the fin shape of top s-Si layer is etched for the channel and then, thin undoped SiGe layer, which is used as undoped spacer between channel and doped supply layer, is deposited on fin- sSOI layer. This undoped SiGe layer is etched to form the sidewalls of s-Si fin channel. Subsequently, deposited n-doped SiGe supply layer is etched

with a lithographical mask for the simultaneous formation of Source/Drain reservoirs and the sidewalls around s-Si fin channel. This point is distinguished from the conventional HEMT or FinFET process. It can be expected that doped SiGe layer for Source/Drain contacts can be placed close to the fin-channel and thus, reduce parasitic resistance which are usually exist in conventional HEMT structure for ohmic contact. Finally, nanoscale high-κ dielectric such as hafnium oxide (HfO_2) and metal-gate is formed to achieve high gate controllability and low gate-leakage mob. Based on this device structure, TCAD double gate HEMT device simulation is performed to analyze the electrical characteristics of the proposed FinHEMT.

Figure 2-2 shows TCAD device simulation of double gate HEMT that is composed of 5-nm-thick 1×10^{19} cm^{-3} doped SiGe, 3 nm undoped SiGe and 10 nm undoped s-Si channel. Gate length is 60 nm, HfO_2 thickness is 8 nm, and distance between gate and Source/Drain is 40 nm. Conduction band offset (ΔE_C) between SiGe and s-Si is 0.2 eV which is enough to accumulate electrons transferred from doped SiGe layer to undoped s-Si channel with 1.02 eV band gap [32][33]. Drain currents as a function of gate voltage are shown in **Figure 2-2** comparing (a) Si cap single-gate planar s-Si HEMT [28] with (b) HfO_2 cap double-gate FinHEMT. High OFF-current which is main weakness of conventional s-Si HEMT with Si cap is shown since relatively small Si bandgap results in high gate leakage current when it is at OFF-state. Also, **Figure 2-2(c)** shows the FinHEMT structure eliminated the undoped SiGe layer for improving the performance of the device. The subthreshold swing, ON-current, and OFF-current are improved because the ΔE_C can prevent the electrons transferred to doped SiGe layer from QW channel.

Therefore, in case of FinHEMT with gate oxide (e.g. HfO_2), on-current has been enhanced by the double-gate structural effect on fin channel and OFF-current has been reduced by the suppressed gate leakage and, simply doubled electron density and channel controllability. Through TCAD device simulation of FinHEMT as double-gate HEMT, on-current of 1.65 mA/μm and off-current of 11 pA/μm with the extremely high ON-OFF current ratio (= 1.5×10^{8}) have been achieved on Si-compatible device platform. Moreover, good subthreshold swing (SSW) is observed as 63 mV/dec. Maximum depletion width of $1x10^{19}$ cm^{-3} doped SiGe can be estimated 7.85 nm which is larger than the thickness (5 nm) of doped SiGe layer. Thus, FinHEMT gates can control whole of doped SiGe, undoped SiGe, and undoped s-Si channel which results in good SSW.

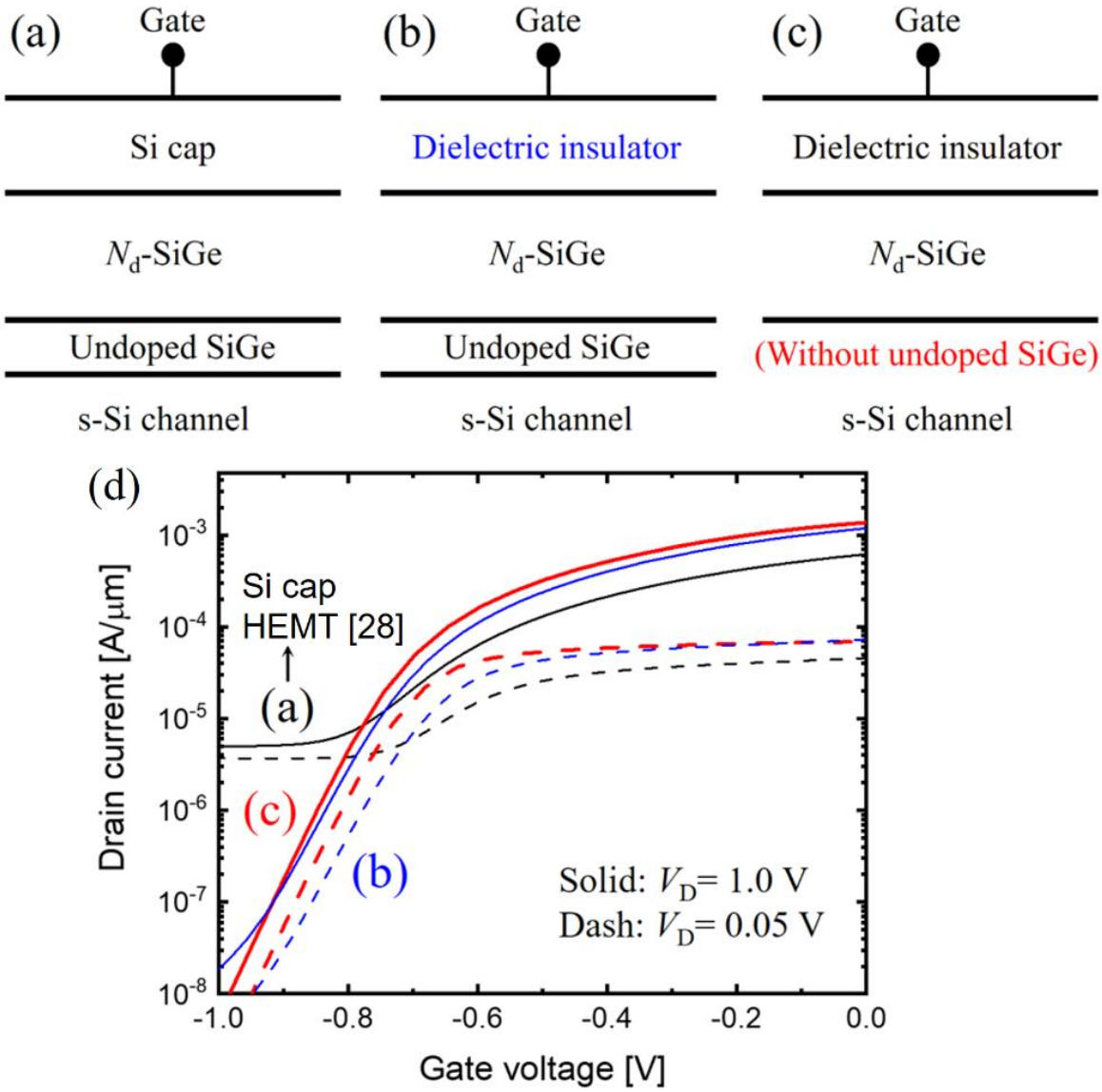

Figure 2-2. Structure optimization process from (a) Si cap HEMT [28], (b) replacing Si cap as dielectric insulator, and (c) without undoped SiGe layer.

2.2 Simulation models

To form the ΔE_C, electron affinity (X) of s-Si is set as 4.295 eV rather than 4.05 eV for Si. And the bulk mobility value of 2600 cm^2/Vs is used to match the experimental low-field mobility of s-Si FinFET [9]. Moreover, "eQuantumPotential" model is used to clarify s-Si QW channel. The general transport equation "Hydrodynamic(eTemperature)" is used to confirm the current density and electron velocity in short channel regime. To verify the mobility improvement in FinHEMT, "DopingDependence" "Enormal" and "HighFieldSaturation" are used with equivalent parameters set for both FinHEMT and FinFET. The mole fraction of Ge is 0.3 is used to realize biaxial tensile stress on Si and to form the ΔE_C [34]. The parameters set is calculated as linear interpolation of Si and Ge with the mole fraction.

3. Operation principle of FinHEMT (Long channel)

3.1 Device parameter analysis

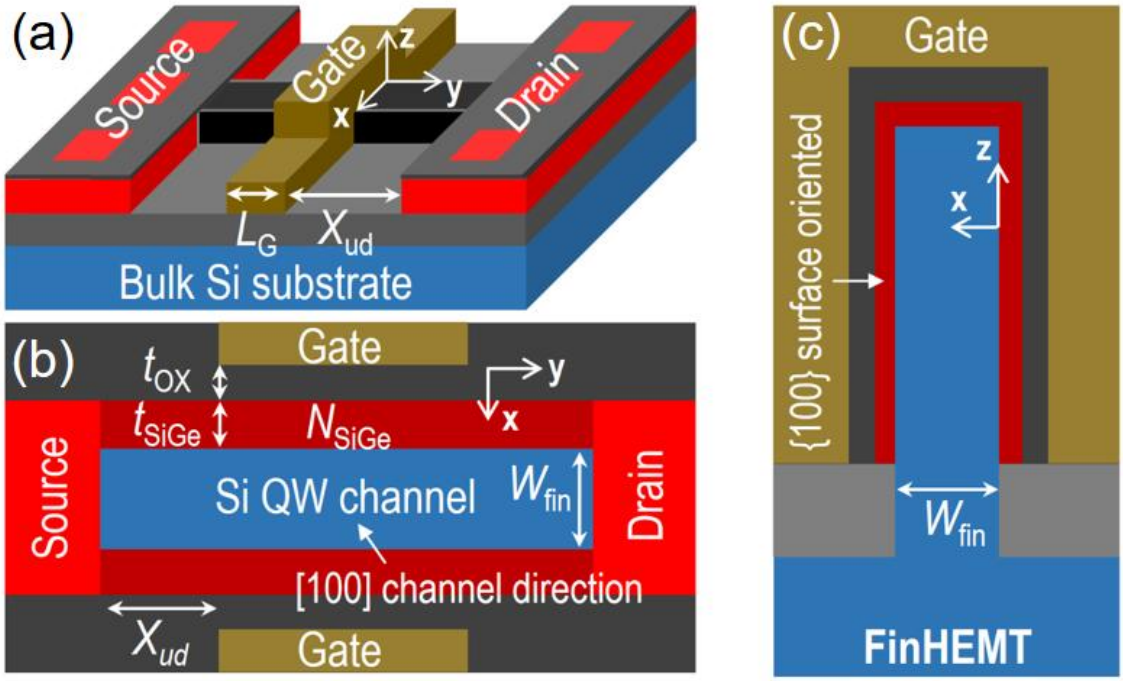

Figure 3-1. FinHEMT structure of (a) three dimensional schematic, (b) (x-y plane cut) cross-sectional schematic in channel and (c) (z–x plane cut) gate [100] direction with additional SiGe layer parameters (t_{SiGe}, N_{SiGe}) from FinFET.

The three dimensional and cross-sectional schematics of FinHEMT are presented in **Figure 3-1(a)** to **(c)**, respectively. The relaxed $Si_{0.7}Ge_{0.3}$ layer [32], [34] between the s-Si QW channel and HK gate dielectric, which the biaxial tensile stress is enable to applied on s-Si channel, distinguishes FinHEMT from FinFET. This unique $Si_{0.7}Ge_{0.3}$ layer has two design parameters which are the thickness (t_{SiGe}= 2 nm) and doping concentration (N_{SiGe}= 1×10^{19} cm^{-3}) of the SiGe layer. And 6 nm-thick width of s-Si fin (W_{fin}) and 6 nm-thick HK (= $23\varepsilon_0$) gate dielectric, which has effective oxide thickness EOT is 1 nm, are used as a reference from the 14 nm technology node [35] for both FinFET and FinHEMT. Moreover, the [100] channel direction and {100} surface orientation s-Si is adopted for bulk mobility of 2600 cm^2/Vs [36] and minimized interface trap density [37].

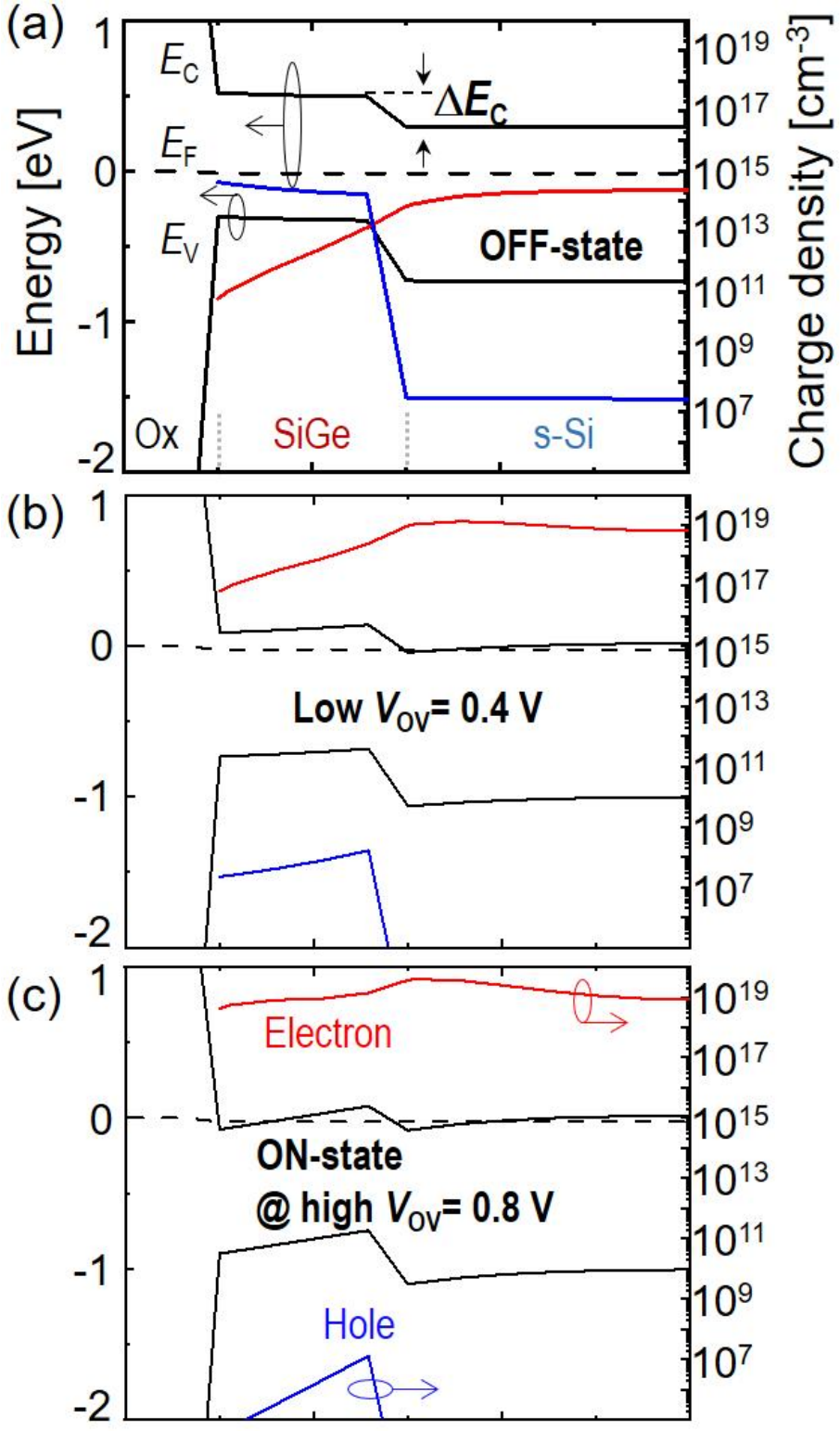

Figure 3-2. FinHEMT's electron/hole density profiles and corresponding conduction/valence band diagram (center of the gate) of (a) OFF-state at V_{OV}= -0.2 V, (b) ON-state at relatively low V_{OV}= 0.4 V and (c) high V_{OV}= 0.8 V for L_G= 1 μm, HK EOT = 1 nm, t_{SiGe}= 2 nm, N_{SiGe}= 1×10^{19} cm^{-3}, $t_{s\text{-}Si}$=W_{fin} = 6 nm, and ΔE_C= 0.2 eV.

The ON/OFF-state conduction/valence band diagrams and corresponding charge density (red line for electron and blue line for hole) plots using the quantum-corrected potential model and Fermi–Dirac statistics [38] are presented in **Figure 3-2(a)** to **(c)**. The conduction band offset ΔE_C of 0.2 eV formed at the $Si_{0.7}Ge_{0.3}$ and s-Si interface is clearly shown [27], [39]. At the OFF-state with $V_{OV}= V_{GS}-V_T= -0.2$ V (**Figure 3-2(a)**), where $V_T= 0.2$ V, both the SiGe and s-Si are fully depleted with the charge density below 10^{14} cm^{-2}, resulting in low OFF-current (I_{OFF}). At low gate overdrive voltage with $V_{OV} = 0.4$ V (**Figure 3-2(b)**), the s-Si QW channel confined the most electrons owing to the lower conduction band than that of SiGe [27], [39]. In the ON-state at high $V_{OV}= 0.8$ V, the e-density in the SiGe layer also increases by band bending of the SiGe forming surface channel, but only up to 10 % of that in the s-Si QW channel (**Figure 3-2(c)**). Therefore, the electrons in the s-Si QW channel separated from the gate dielectric interface are expected to dominate the ON-current (I_{ON}). For all V_{OV}, as the hole density is significantly low and, due to the Source/Drain are n-type doped, there is no effects of holes in the FinHEMT operation.

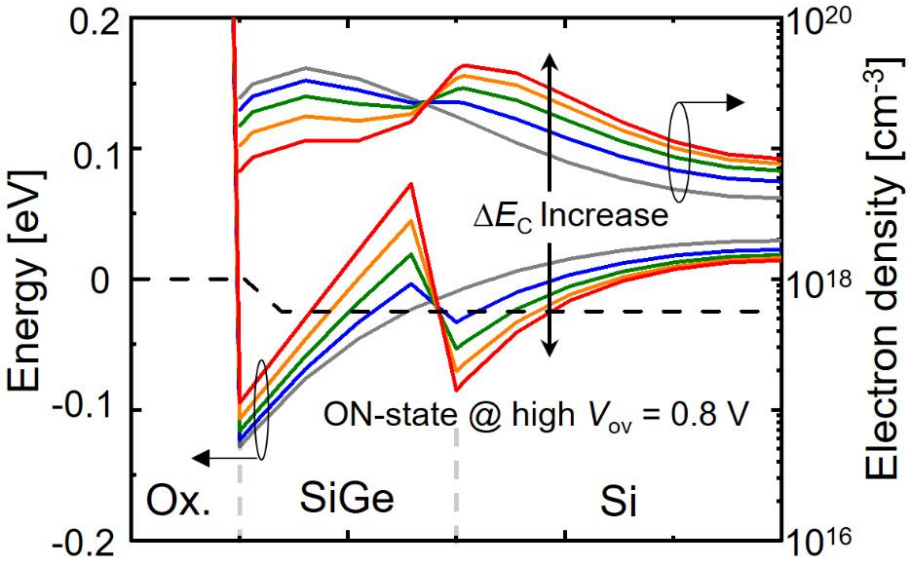

Figure 3-3. Conduction band energy and electron density with ΔE_C variation at V_{OV}= 0.8 V. As the ΔE_C increases, electron density in s-Si channel increases, while decreases in SiGe layer.

The ΔE_C can be changed by the mole fraction of SiGe [32]. **Figure 3-3** shows the conduction band energy and corresponding electron density with ΔE_C variation at V_{OV}= 0.8 V. ΔE_C varies from well-known value of 0.2 eV (red line) to 0 eV (gray line) with 0.05 eV step. If there is no ΔE_C, the operation principle of FinHEMT is equivalent with FinFET. Therefore, it should be noted that s-Si QW channel can be formed with the ΔE_C, which the lower gate capacitance (C_G) and surface roughness scattering than FinFET is expected.

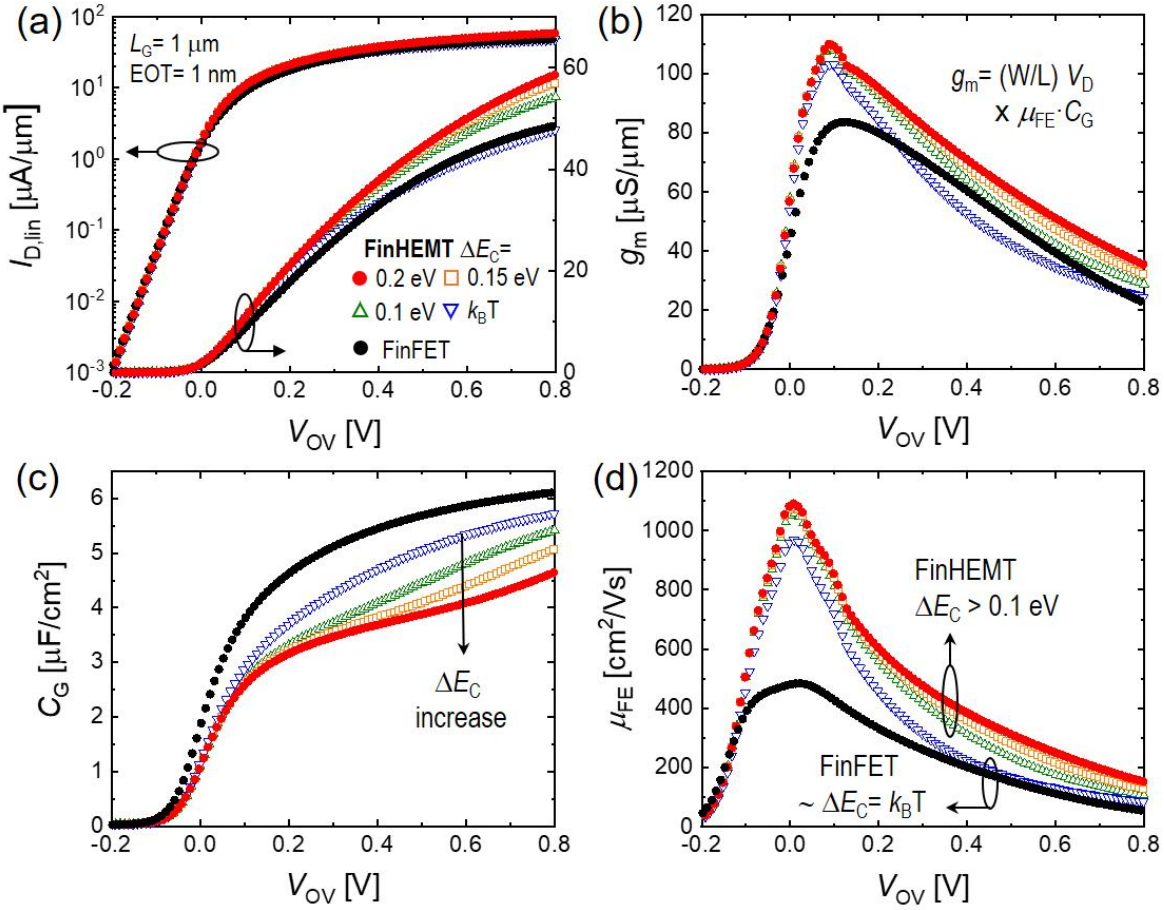

Figure 3-4. The calculated dataset of field-effect mobility (μ_{FE}) extraction: (a) transfer *I-V* curves (b) transconductance g_m (c) gate capacitance and (d) the extracted μ_{FE} from g_m= (W/L) $\mu_{FE}C_GV_D$ for the long-channel FinFET and FinHEMT with different ΔE_C= 0.2 [27][39], 0.15, 0.1 and 0.026 eV(= k_BT), t_{SiGe}= 2 nm, and N_{SiGe}= 1x10^{19} cm^{-3}.

Figure 3-4 shows the typical extraction dataset of field-effect mobility (μ_{FE}) based on the transconductance equation g_m= (W/L) $\mu_{FE}C_GV_D$, where W=L= 1 μm and V_D= 0.05 V. To investigate the effect of ΔE_C, we consider various ΔE_C in the simulation of FinHEMT with the 2-nm-thick SiGe layer. Clear current and g_m gain are obtained in FinHEMT, (**Figure 3-4(a)** and **(b)**) as long as ΔE_C > 0.1 eV. Even with the reduced gate capacitance (C_G) by the additional gate dielectric coming from the depleted SiGe layer (**Figure 3-4(c)**), the dramatic mobility improvement in the well-confined QW channel formed by ΔE_C enables the overall gain (**Figure 3-4(d)**). In **Figure 3-4(c)**, the gate capacitance decreases as the ΔE_C increases, because the s-Si channel can be confined away from the gate with ΔE_C. And 25 % lower gate capacitance indicates that additional EOT of SiGe is 0.36 nm which is 1.2 nm

thick SiGe with relative permittivity ε_r= 13. If ΔE_C is too small (e.g. ~k_BT), FinHEMT only suffers from the C_G reduction without any mobility improvement since QW is not well defined, thus resulting in the degraded current. The known value of ΔE_C ~0.2 eV [27][39] is more than enough to guarantee the overall current and g_m gain in our FinHEMT operation.

This doped and thin SiGe layer has two specific design parameters, which are thickness (t_{SiGe}) and doping concentration (N_{SiGe}) of the SiGe layer. As in **Figure 3-5(a)**, the enhanced current by SiGe layer remains same even with t_{SiGe}= 1~ 3 nm variation. From a simple guess, we may expect that the thicker SiGe layer results in the higher mobility and the lower C_G, which is valid at low V_{OV} (**Figure 3-5(b)**). In high V_{OV} regime, however, due to the electron density increase in SiGe (**Figure 3-2(c)**), the dependency of C_G and mobility on t_{SiGe} becomes weak for t_{SiGe}= 1~ 3 nm (**Figure 3-5(c)**). The effect of N_{SiGe} is not significant when t_{SiGe} is less than or equal to 2 nm since maximum depletion width W_{dm}= =~ 11 nm for high N_{SiGe}~ 10^{19} cm^{-3} is larger than t_{SiGe}, but it becomes effective in short-channel regime that will be discussed in the section 4.1.

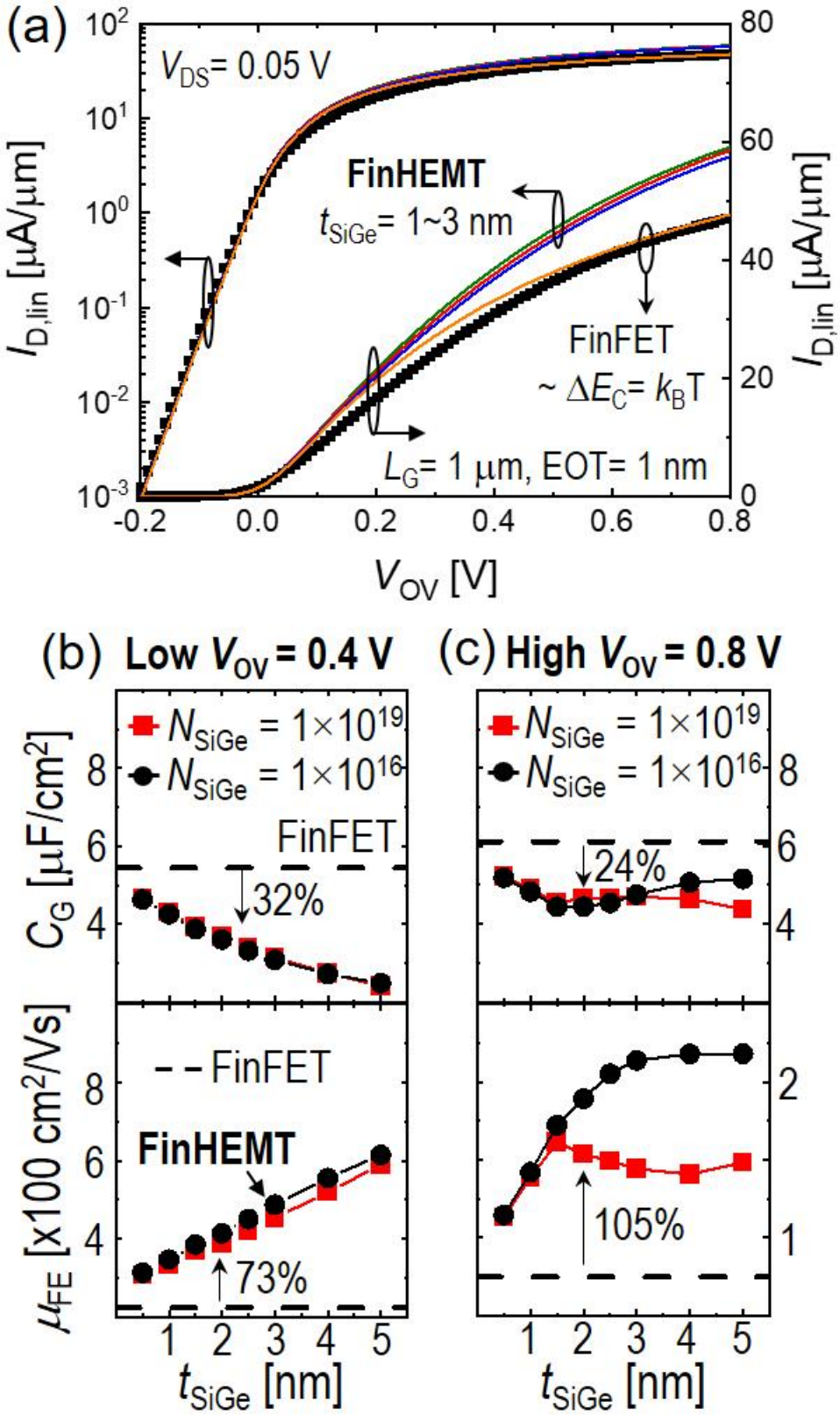

Figure 3-5. (a) Transfer *I-V* curves of FinHEMT and FinFET for different t_{SiGe} with ΔE_C= 0.2 eV. Gate capacitance (C_G) and calculated field effect mobility (μ_{FE}) at (b) low V_{OV}= 0.4 V and (c) high V_{OV}= 0.8 V for various t_{SiGe} and N_{SiGe} of FinHEMT benchmarking with FinFET.

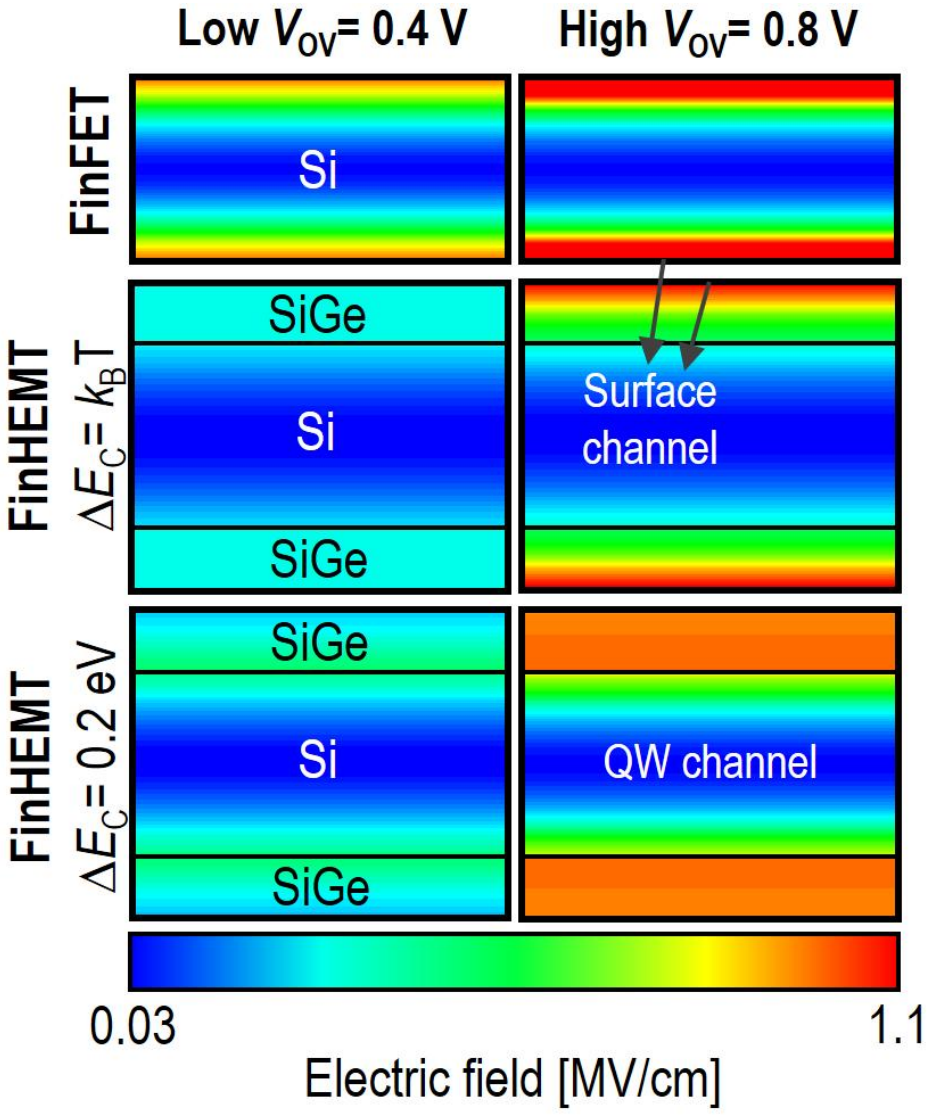

Figure 3-6. E_{norm} contour plot at low V_{OV}= 0.4 V and high V_{OV}= 0.8 V in FinHEMT with ΔE_C= 0.2 eV and FinFET (~$\Delta E_C = k_B T$).

The increased electron density in SiGe layer at high V_{OV} blocks the normal electric field (E_{norm}) and hence suppress the further E_{norm} increase in QW channel (ΔE_C = 0.2 eV), thereby reducing SRS effect (**Figure 3-6**). However, the SiGe surface channel is activated when the ΔE_C= ~$k_b T$ because there is no QW channel in FinHEMT. There is effective mobility degradation owing to high surface E_{norm} which is equivalent with FinFET operation.

3.2 Enhanced effective mobility

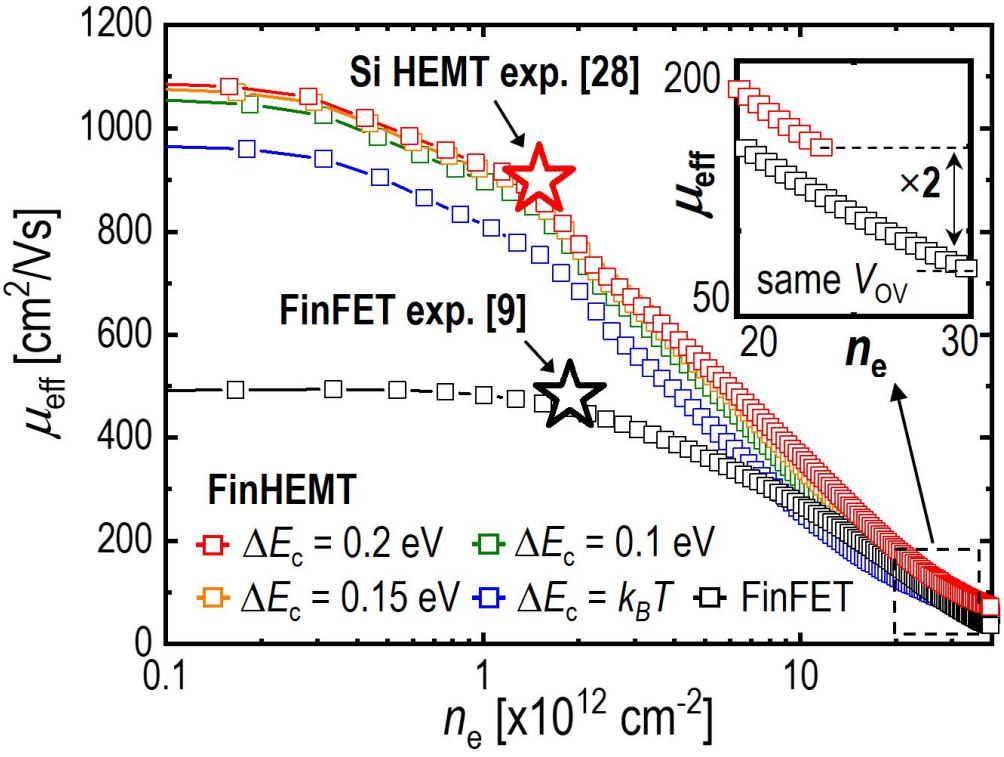

Figure 3-7. Universal μ_{eff} vs. e-density ($qn_e = C_G V_{OV}$) of FinFET and FinHEMT with experimental data [9], [28]. Inset: 2 times enhanced μ_{eff} in s-Si channel in FinHEMT at same $V_{OV} = 0.8$ V.

Comparing with FinFET as a reference, the extracted μ_{eff} of FinHEMT for different ΔE_C values is summarized in **Figure 3-7**. Based on our simulation platform, well-calibrated with the available experimental record mobility of s-Si on insulator (sSOI) FinFET ~500 cm^2/Vs [9] and Si HEMT ~950 cm^2/Vs [28], the proposed FinHEMT shows record-high low-field mobility ~1100 cm^2/Vs and 2 times enhanced μ_{eff} by SRS suppression in s-Si QW channel than in FinFET (inset), while keeping the same gate controllability with FinFET.

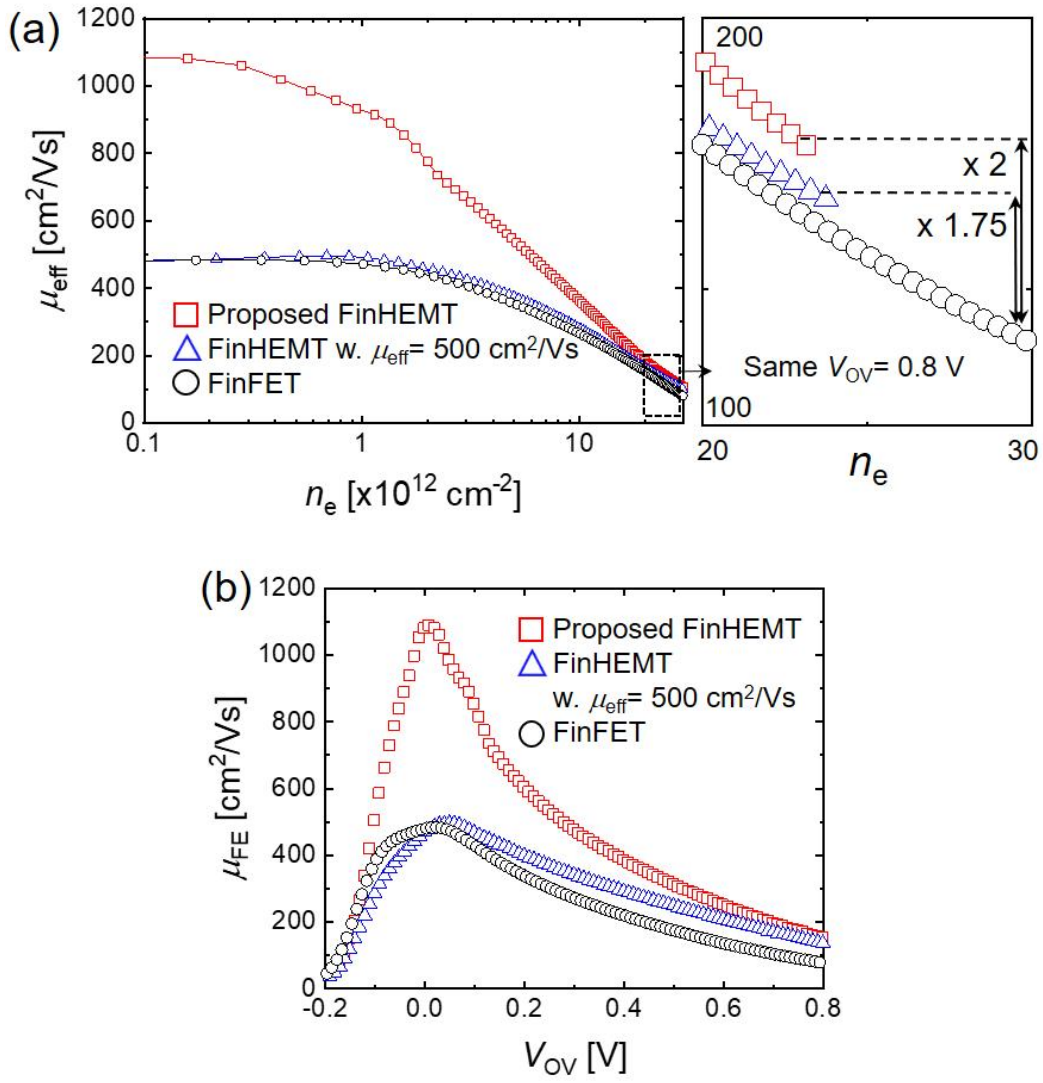

Figure 3-8. (a) Effective mobility and (b) field-effect mobility with 500 cm^2/Vs low-field mobility of FinHEMT.

As shown in the left of **Figure 3-8(a)**, we intentionally lower the mobility of FinHEMT down to 500 cm^2/Vs at low electron density by adjusting ionized impurity scattering parameters and run the FinHEMT simulation with the other scattering parameters remaining the same. Although the mobilities of FinHEMT and FinFET are matched at low electron density, FinHEMT could still have 1.75× higher mobility than FinFET in the high electron density regime at the same gate overdrive voltage (V_{OV}= 0.8 V) because of the reduced SRS (**Figure 3-8(a)** right and **(b)**). However, as shown in **Figure 3-4(c)**, an additional EOT from the SiGe layer in FinHEMT leads to the lower capacitance, and hence we cannot achieve higher current in FinHEMT even with the improved mobility. If EOT of FinHEMT is scaled down further and matched to FinFET, we can expect higher current in FinHEMT.

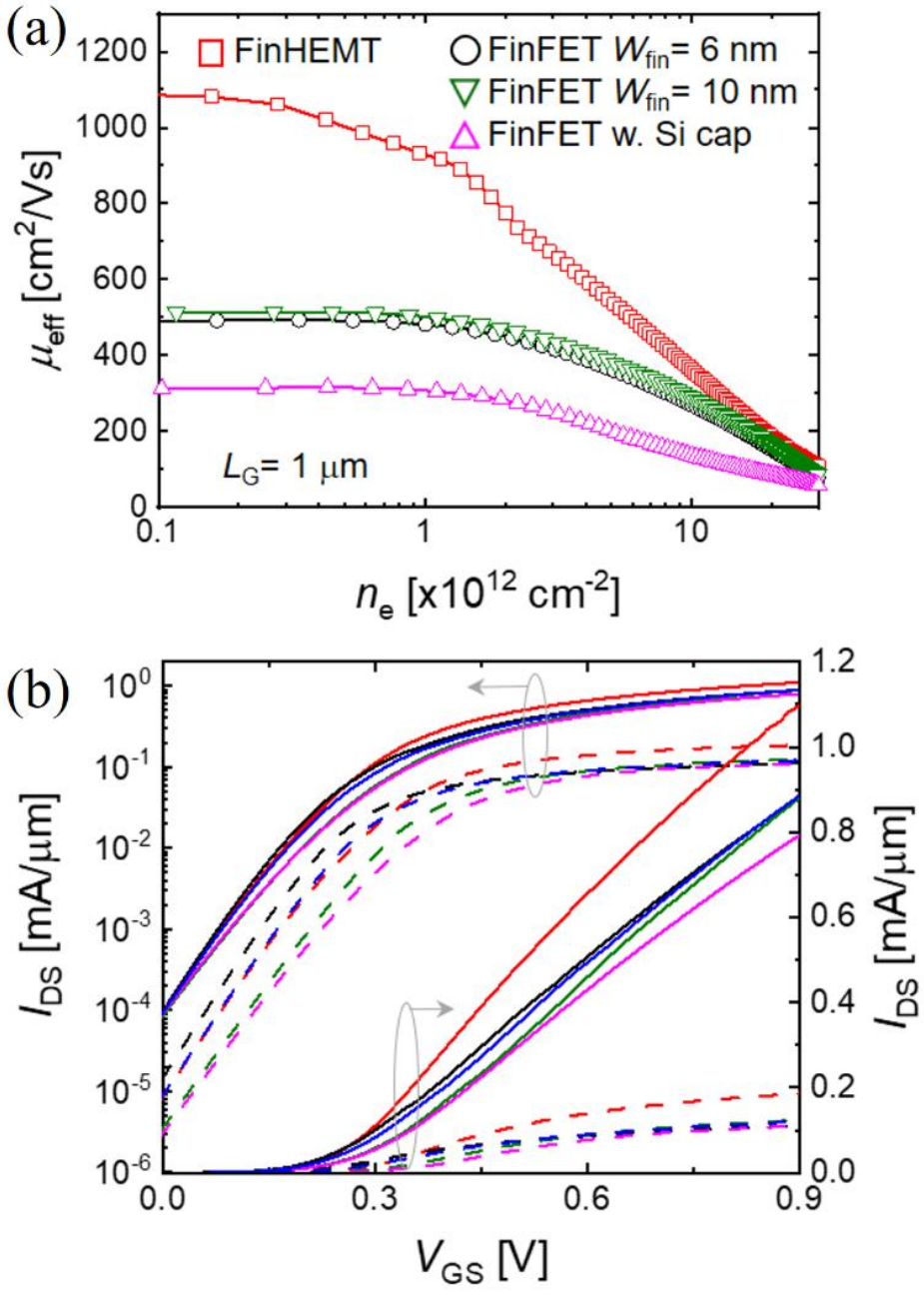

Figure 3-9. (a) Effective mobility versus electron density and (b) transfer I_{DS}-V_{GS} curves compared with 1x10^{19} cm^{-3} doped Si cap and W_{fin}= 6, 7.6, 10 nm of FinFET.

If we use $1x10^{19}$ cm^{-3} doped Si cap instead of SiGe, the electron channel is formed at the interface between gate oxide and doped Si because there is no band offset to separate the electron from the interface. Therefore, as we expect, the effect of SRS and ionized impurity scattering severely degrade the mobility as shown in **Figure 3-9(a)**. If we just increase the Si channel thickness to 10 nm without doping, the mobility is recovered and becomes similar to the 6-nm-thick s-Si channel in **Figure 3-9(a)**. As a result, from the transfer characteristics in **Figure 3-9(b)**, $1x10^{19}$ cm^{-3} doped Si cap exhibits lower current than FinFET and 10-nm-thick channel FinFET shows almost similar current with the original 6-nm-thick FinFET.

Additionally, we examine the validity of comparing FinHEMT and FinFET with the same 6-nm-thick Si Channel. In FinHEMT, if we consider the spreading of electron into the SiGe layer, the effective Si Fin width could be roughly estimated to 7.6 nm, suggesting that benchmarking our FinHEMT to 7.6-nm-thick channel FinFET is more reasonable. In **Figure 3-7(b)**, we show the transfer characteristics of 7.6-nm-thick channel FinFET and confirm that current is almost same with our original 6-nm-thick FinFET. Therefore, we believe that the comparison between FinHEMT and FinFET having the same 6 nm-thick s-Si channel could be valid in terms of the on-current and short channel effects (SCEs).

4.Short channel characteristics

4.1 Performance optimization

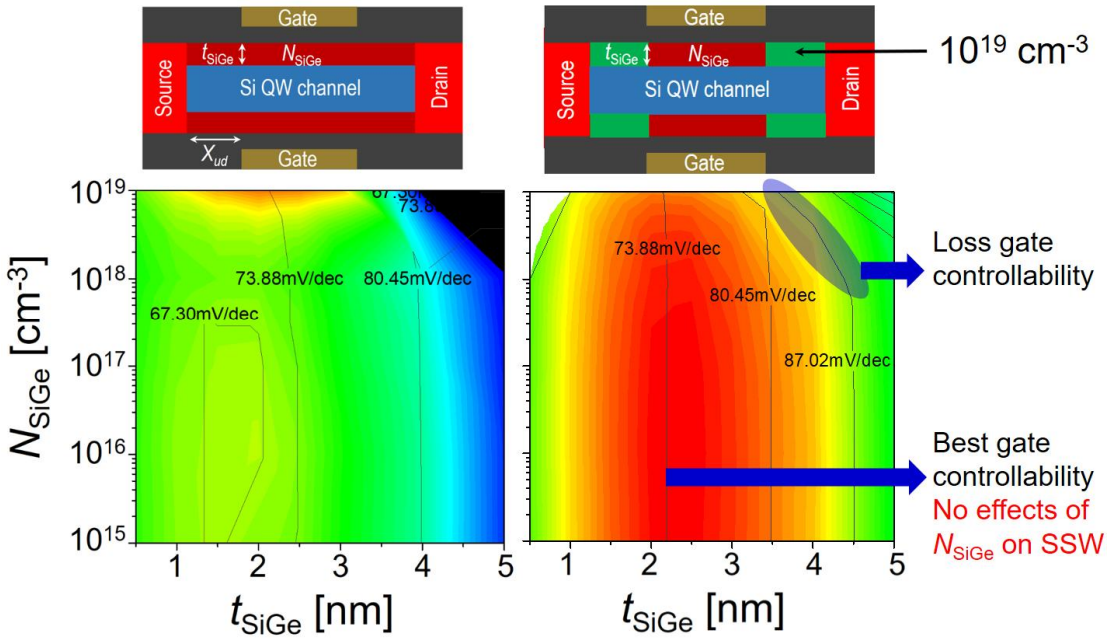

Figure 4-1. I_{ON} contour plots for (a) FinHEMT, and (b) considering diffusion process through the SiGe layer from source/drain to under the gate region. Optimized t_{SiGe} and N_{SiGe} following scaling rule. With t_{SiGe}= 2 nm and N_{SiGe}= 10^{19} cm^{-3}, the I_{ON} is maximized with 73.88 mV/dec of SS.

In short channel regime, ON-current is determined by the Source/Drain series resistance $\rho_s = \rho_{source} + \rho_{channel} + \rho_{Drain}$. Our proposed FinHEMT with gate undelap region (X_{ud}) can achieve low Source/Drain resistance due to quantum well with high electron density transferred from high N_{SiGe} layer. **Figure 4-1** shows ON-current contour plot according to the N_{SiGe} and t_{SiGe} variation. Maximized ON-current can be achieved at t_{SiGe}= 2 nm and N_{SiGe}= 1×10^{19} cm^{-3} and subthreshold swing is 73.88 mV/dec. If we consider the diffusion from Source/Drain to SiGe layer, the SiGe layer under the channel can be lower than the gate underlap region as shown in **Figure 4-1(b)**. The simulation result shows that there is subthreshold variation at higher t_{SiGe} > 3.5 nm and N_{SiGe} > 10^{18} cm^{-3}. However, at t_{SiGe}= 2 nm, there is no subthreshold swing variation which means that the best gate controllability regime. Therefore, optimized device parameters are t_{SiGe}= 2 nm, and N_{SiGe} < 5x10^{18} cm^{-3}.

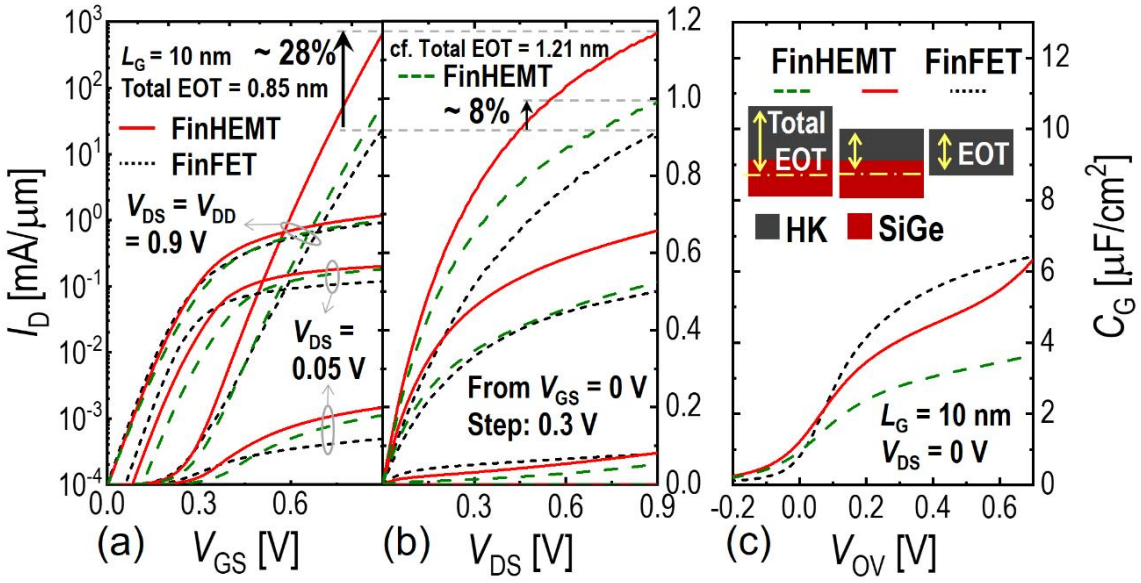

Figure 4-2. (a) Transfer I_D–V_{GS}, (b) output I_D–V_{DS}, and (c) C–V curves for FinHEMT with N_{SiGe}= 1 × 10^{19} cm^{-3} and t_{SiGe} = 2 nm, gate HK dielectric EOT = 0.85 nm (green, total EOT= 1.21 nm), and 0.49 nm (red, total EOT= 0.85 nm) and FinFET (black) with total EOT = 0.85 nm, and gate workfunction WF= 4.95, 4.83, and 4.65 eV respectively. Inset in (c): schematic for total EOT of FinHEMT with SiGe layer compared to only HK EOT of FinFET.

Benchmarked with FinFET based on the technology node device parameters of the gate length L_G= 10 nm, W_{fin}= 6 nm, EOT= 0.85 nm, and the underlap length X_{ud}= (L_G-L_{eff})/2= -5 nm, **Figure 4-2** shows the dc characteristics of the short-channel FinHEMT. The I_{ON} is normalized with $2H_{fin}$ + W_{eff}, where we use 50 nm for H_{fin}, and 6 and 7.6 nm for W_{eff} for FinFET and FinHEMT respectively. For FinHEMT, the additional SiGe thickness operating as the channel (**Figure 4-2(c)**, inset) is included in W_{eff}. FinHEMT shows 28% enhanced driving on-current I_{ON}= 1.176 mA/μm at V_{DD}=V_{GS}=V_{DS}= 0.9 V (**Figure 4-2 (a)(b)**) for the same total EOT= 0.85 nm of FinFET composed of gate HK dielectric EOT= 0.49 nm and SiGe EOT= 0.36 nm by the additional t_{SiGe}= 2 nm with N_{SiGe}= 1x10^{19} cm^{-3} (**Figure 4.2(c)**). Even in FinHEMT with thicker total EOT= 1.36 nm (HK EOT= 0.85 nm + SiGe EOT= 0.51 nm), I_{ON} is still enhanced by 8 %. This additional I_{ON} gain in the short-channel FinHEMT can be explained by the reduction of the series resistance composed of the channel and gate underlap region by the doped SiGe layer.

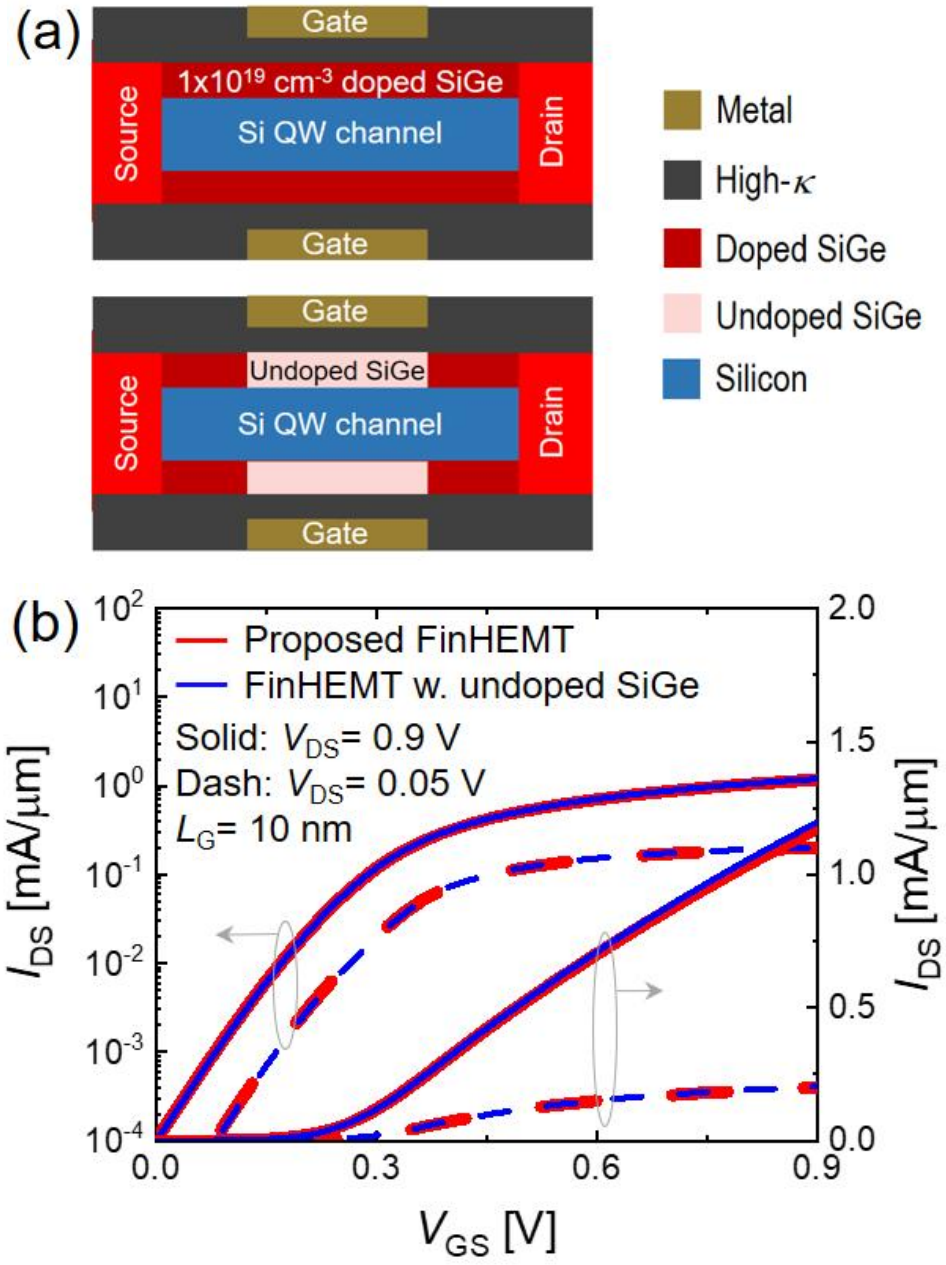

Figure 4-3. (a) Schematic structure of proposed FinHEMT and FinHEMT with undoped SiGe layer under the gate. (b) Those transfer I_{DS}-V_{GS} curves at L_G= 10 nm.

If we consider 10 nm gate length, 50 nm fin height and 2-nm-thick SiGe layer, there are 10 impurities in 2-nm-thick SiGe layer. One may think that the impact of random discrete dopant (RDD) is significant, however, this SiGe layer behaves as additional high-κ (ε_r= 13) dielectric insulator rather than channel. So, the effect of RDD should be limited. Moreover, we can also consider undoped SiGe layer to avoid

any concerns about RDD. As presented in **Figure 4-3(a)** bottom, we consider FinHEMT with the undoped SiGe layer and run the FinHEMT simulation again. From the transfer I_{DS}-V_{GS} curves at the matched I_{OFF} in **Figure 4-3(b)**, FinHEMT with and without doping in the SiGe layer result in the almost identical transfer characteristics. Therefore, we can completely avoid RDD concern if the undoped SiGe layer is employed in FinHEMT.

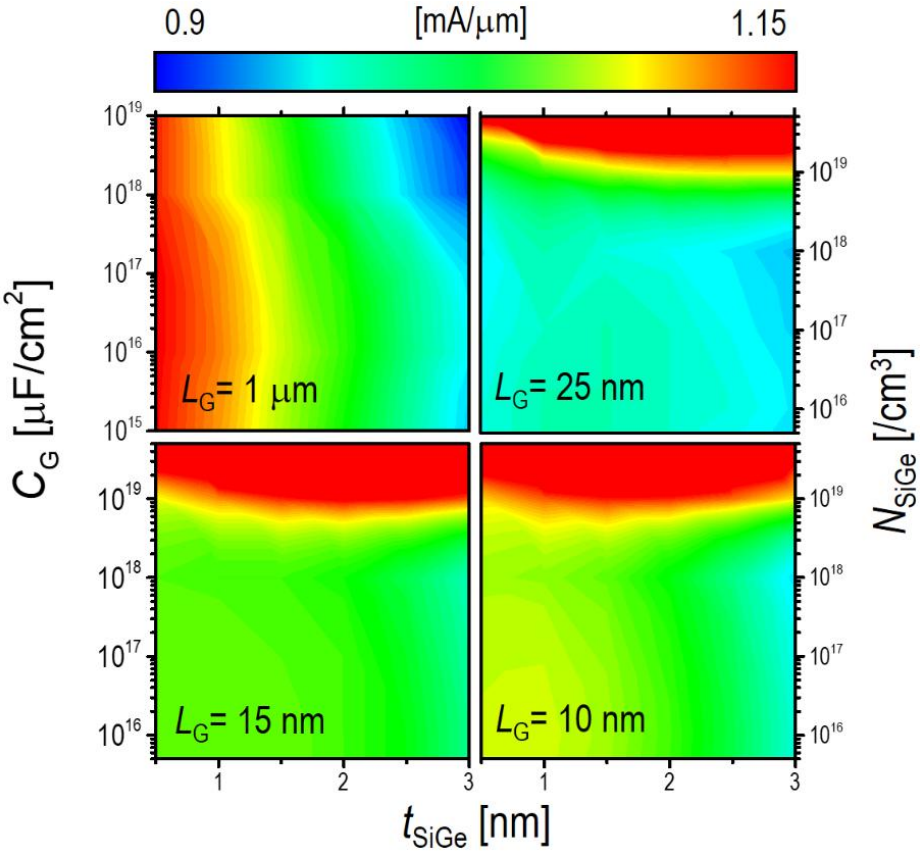

Figure 4-4. I_{ON} contour plots as functions of t_{SiGe} and N_{SiGe} for various L_G= 1 μm, 25 nm, 15 nm, and 10 nm.

As shown in the I_{ON} contour plots as functions of t_{SiGe} and N_{SiGe} (**Figure 4-4**), I_{ON} is improved as N_{SiGe} increases in short-channel regime upon scaling down to sub-30 nm where the underlap series resistance dominates while no I_{ON} dependence on N_{SiGe} (mainly on t_{SiGe}, i.e. EOT) in long-channel regime. In short channel regime, the length of channel is comparable with the gate underlap region X_{ud} and therefore, the resistivity of X_{ud} become significant to I_{ON}.

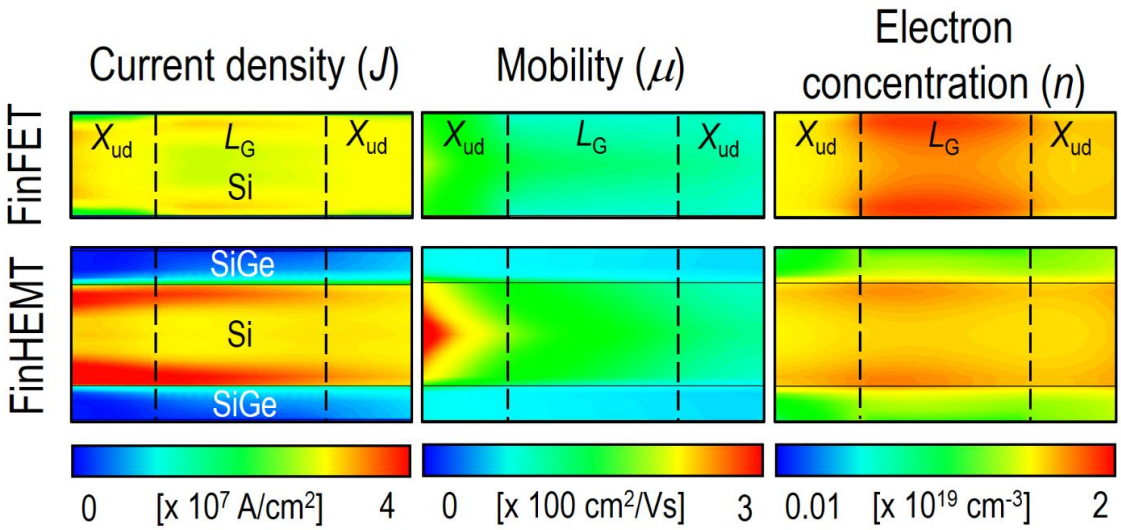

Figure 4-5. Contour plots of current density (J), mobility (μ) and electron concentration (n) in 2D cross-sectional channel with underlap region (X_{ud}) at V_{GS}=V_{DS}= 0.9 V for both FinHEMT and FinFET (L_G= 10 nm, L_{UN}= 5 nm, and same total EOT= 0.85 nm).

L_G= 10 nm Total EOT= 0.85 nm	FinFET	FinHEMT (N_{SiGe}) Undoped 10^{16} cm^{-3}	 Doped 10^{19} cm^{-3}
J [10^7 A/cm^2]	3.3	3.7 (x 1.11)	4.0 (x 1.21)
μ [cm^2/Vs]	175	249 (x 1.42)	259 (x 1.48)
n [10^{18} /cm^2]	6.7	6.2 (x 0.93)	8.4 (x 1.27)
ρ_{Xud} [10^{-3} Ω·cm]	5.4	4.1 (x 0.76)	2.9 (x 0.53)

Table I. The extracted current density (J), mobility (μ), e-density (n), and calculated resistivity ρ_{Xud} for the gate underlap region.

Figure 4-5 provides the contour plots of the current density (J), electron concentration (n), and mobility (μ) in 2D cross-sectional channel with the gate underlap region at V_{DD}=V_{GS}=V_{DS}= 0.9 V for both FinHEMT and FinFET. As compared with FinFET, s-Si QW channel under the gate of FinHEMT has lower n, but improved μ by SRS suppression as explained in the long-channel regime (Section 2). Especially in the gate underlap region, however, both higher μ and n can be achieved by the doped SiGe layer (N_{SiGe}= 1x10^{19} cm^{-3}) with ΔE_C= 0.2 eV as in HEMT [40], which results in the lower underlap resistivity (ρ_{Xud}) than that of FinFET. The quantitative analysis is summarized in **Table I** resulting the 47% reduction of $\rho_{Xud} = 1/(q\mu n)$ in FinHEMT with N_{SiGe}= 1x10^{19} cm^{-3}. In the case of FinHEMT with the undoped SiGe layer (N_{SiGe}= 1x10^{16} cm^{-3}), it should be noted that there is still 24% reduction of ρ_{Xud} from FinFET by highly improved μ (1.42 times higher than FinFET) even with lower n than those of FinFET.

4.2 Variability and Scalability predictions

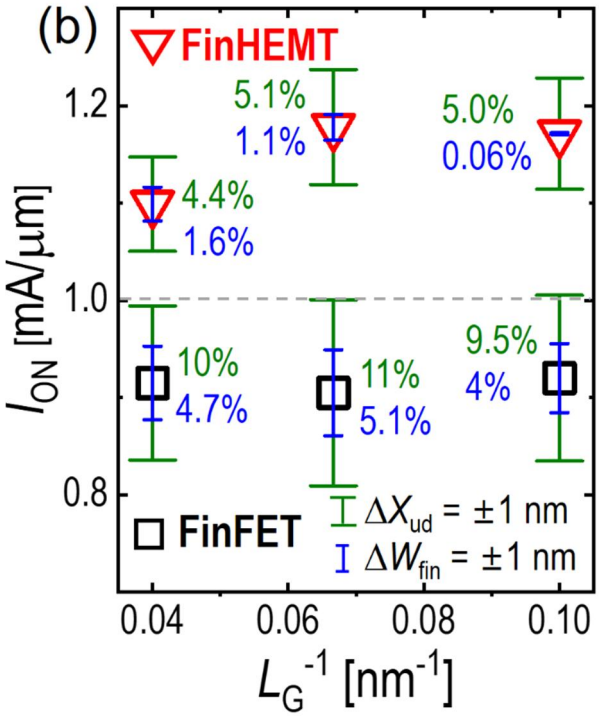

Figure 4-6. I_{ON} variability with process variation of X_{ud} and W_{fin} (±1 nm) when scaling L_G = 25, 15, 10 nm at V_{DD} = 1, 0.93, 0.9 V with total EOT= 1.36 (1), 0.9 (0.9), 0.85 (0.85) nm of FinHEMT (FinFET).

Ascribed to this low ρ_{Xud} in FinHEMT, a better immunity in I_{ON} to the process variation [41][42] of X_{ud} and W_{fin} is expected in FinHEMT than in FinFET. **Figure 4-6** shows only 5% change in I_{ON} from the X_{ud} variation (±1 nm) in FinHEMT with L_G= 10 nm, while 9.5% in FinFET. The change of I_{ON} owing to the W_{fin} variation (±1 nm) is reduced to 0.06% in FinHEMT from 4% in FinFET. Observed excellent immunity to the process variation in FinHEMT is due to the both low underlap series resistance and low s-Si channel resistance since the main current path is the s-Si QW channel in FinHEMT (**Figure 4-5**). Furthermore, this uniformity to variability becomes more significant in the further scaling

Moreover, we analyze the variabilities of the DC characteristics such as $V_{T,sat}$, DIBL, SS, and I_{OFF} as summarized in **Figure 4-7**. Since FinHEMT has W_{eff}= 7.6 nm, the variability is the same as that of the 7.6 nm-thick FinFET for these parameters. Although comparing with W_{eff}= 6 nm of FinFET, there is little difference between FinHEMT and FinFET.

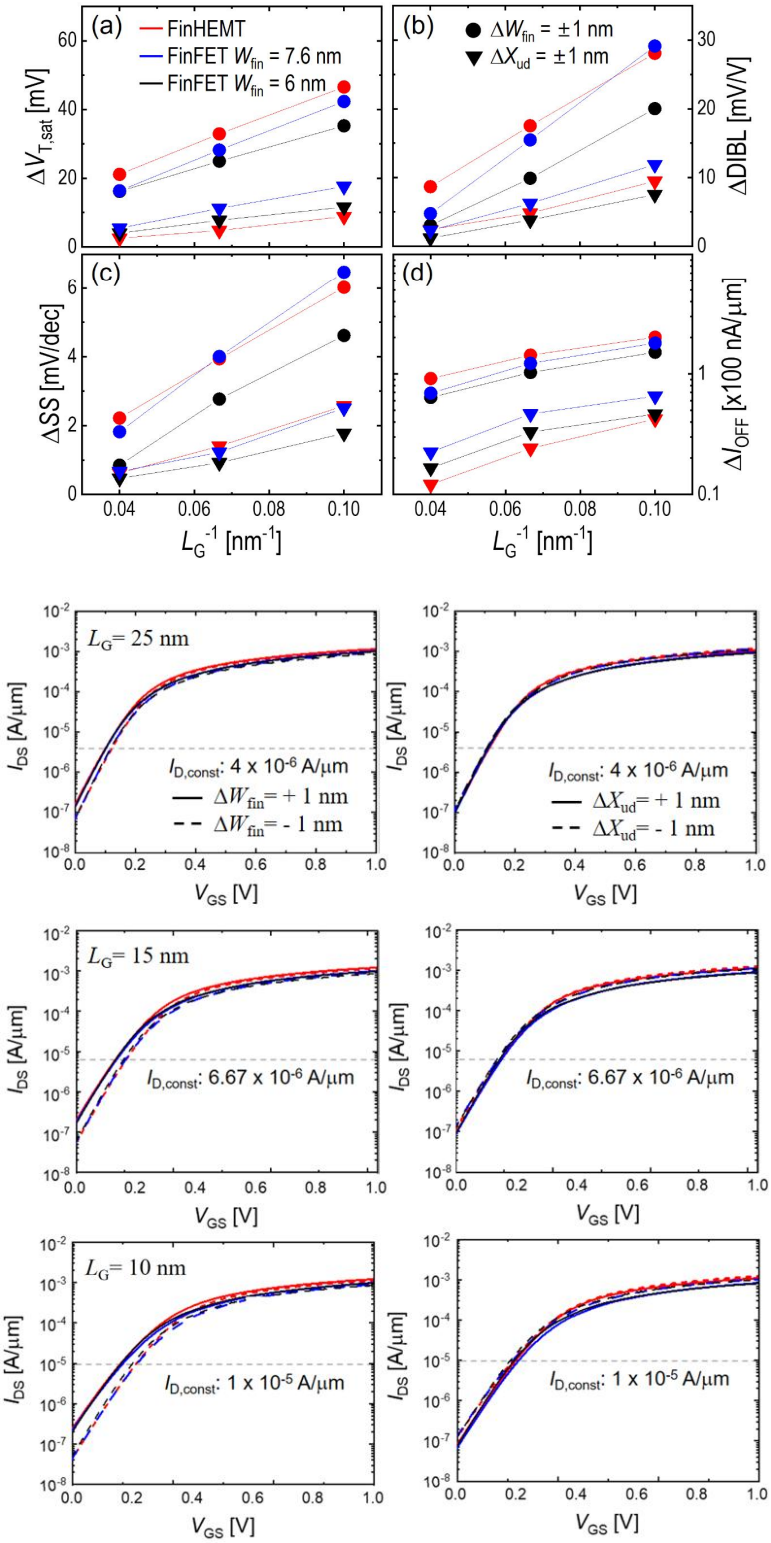

Figure 4-7. (a) $V_{T,sat}$ considering the gate length scaling effects on V_T, (b) calculated DIBL, (c) extracted SS, and (d) I_{OFF} variabilities on X_{ud} and W_{fin} variations of FinHEMT and FinFET with W_{Fin} = 7.6, 6 nm. $V_{T,sat}$ is extracted at I_D= 4, 6.67, 10 μA/μm at L_G = 25, 15, 10 nm, respectively ($V_{D,sat}$ = 1.0, 0.93, 0.9 V, and $V_{D,lin}$ = 0.05 V). Below figures are corresponding transfer I_{DS}-V_{GS} curves of each points.

We run the FinHEMT simulation with reducing the SiGe layer thickness from 2.2 to 1.8 nm as shown in **Figure 4-8** for the high-κ EOT thicknesses of 0.49 and 0.2 nm, respectively. From the transfer I_{DS}-V_{GS} curves in **Figure 4-8**, ΔV_T and σ_{VT} are estimated to 49.0 and 28.2 mV, respectively, for the high-κ EOT 0.49 nm. If the high-κ EOT is reduced to 0.2 nm, we can obtain smaller values of ΔV_T and σ_{VT} (35.7 and 25.6 mV, respectively). To check whether these amounts of variation are acceptable or not, we use A_{VT} defined as $A_{VT} = \sigma\Delta V_T\sqrt{WL} = \sqrt{2}\sigma V_T\sqrt{WL}$ in Ref. [43]. For the stable operation of 6T-SRAM, A_{VT} less than 1.5 mVμm is required [43]. We roughly calculate A_{VT} values of FinHEMT considering σ_{VT} of FinHEMT originating the SiGe layer thickness variation and $\sigma_{VT,FinFET}$ of 6-nm-thick FinFET separately. As shown in Ref. [44], $\sigma_{VT,FinFET}$ due to the metal gate granularity (MGG), fin width roughness (FWR) and fin height roughness (FHR) is estimated to ~22.3 mV for the fin height of 50 nm. Then, using the total σ_{VT} defined as total $\sigma_{VT} = \sqrt{{\sigma_{VT}}^2 + {\sigma_{VT,FinFET}}^2}$ where σ_{VT} is from the SiGe layer thickness variation and $\sigma_{VT,FinFET}$ is from FinFET, the total σ_{VT} values are estimated to 28.16 and 25.6 mV, resulting in the A_{VT} values of 1.31 and 1.19 mVμm for the high-κ EOT thicknesses of 0.49 and 0.2 nm, respectively. Since those values are less than the require value of A_{VT} for the stable 6T-SRAM operation, we expect that the effect of the SiGe thickness variation is limited.

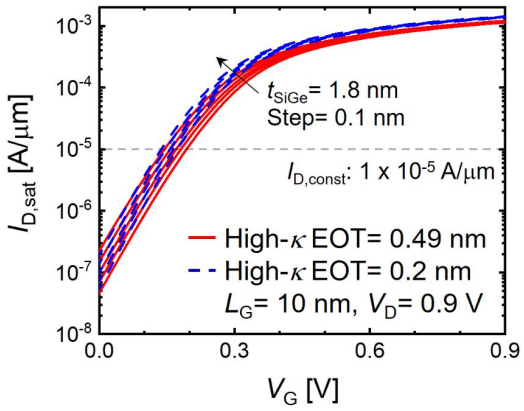

Figure 4-8. Transfer I_D-V_G curves with the SiGe thickness variation for the high-κ EOT= 0.49 (proposed FinHEMT) and 0.2 nm. σ_{VT} and A_{VT} values extracted from the transfer I_{DS}-V_{GS} curves are summarized in Table II.

FinHEMT	HK EOT=	
	0.49 nm	0.2 nm
$\sigma_{VT,FinFET}$ [mV] (Ref. [43])	22.3	
σ_{VT} [mV]	17.19	12.57
Total σ_{VT}	28.16	25.6
A_{VT} [mVμm]	1.31	1.19

Table II. Calculated σ_{VT} and A_{VT} of FinHEMT with conventional σ_{VT} of FinFET.

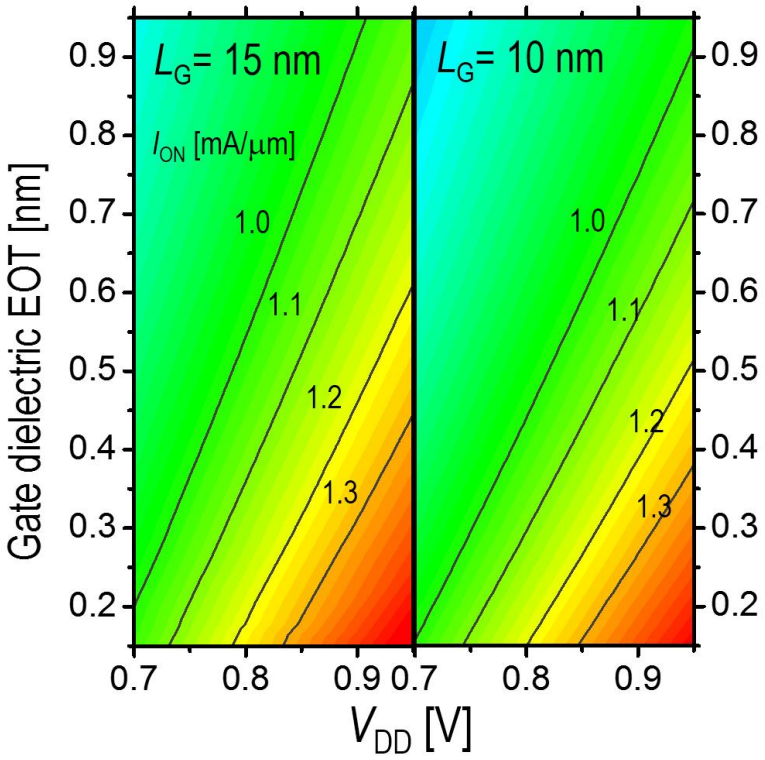

Figure 4-9. Contour plots of I_{ON} in FinHEMT to the gate dielectric EOT and V_{DD} scaling for L_G= 15 nm and 10 nm.

Figure 4-9 shows the I_{ON} contours to the EOT and V_{DD} scaling for L_G= 15 nm and 10 nm. While scaling V_{DD} from 0.95 V to 0.75 V, FinHEMT shows I_{ON} > 1 mA/μm by the gate dielectric EOT scaling from 0.7 to 0.2 nm.

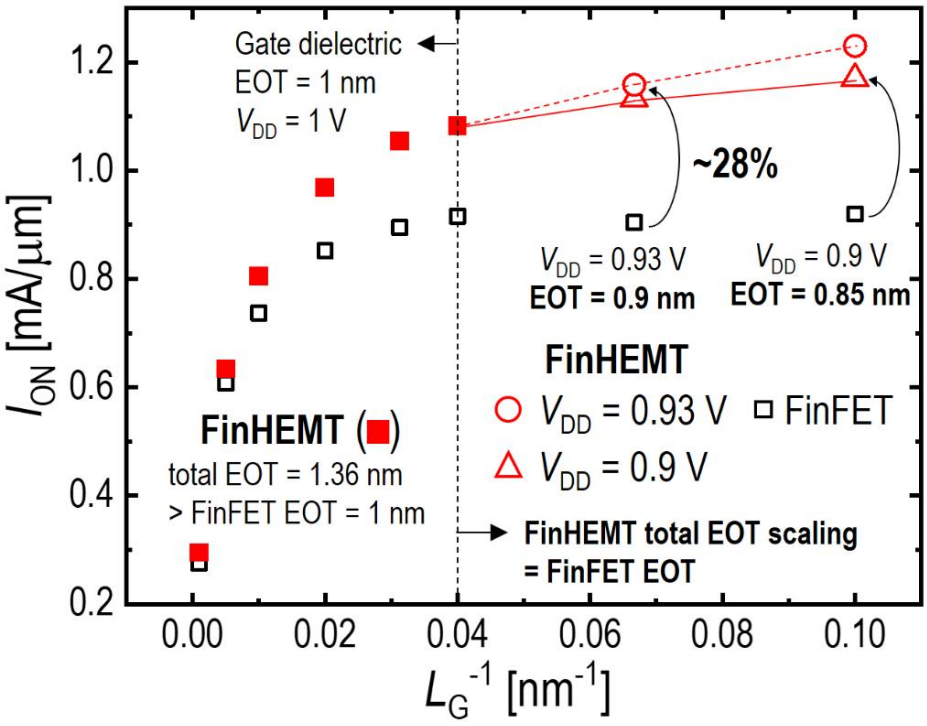

Figure 4-10. FinHEMT scalability over FinFET by plot of I_{ON} as a function of $1/L_G$. For sub-10 nm scaling, FinHEMT I_{ON} keeps increasing by 28% from FinFET at the same total EOT and V_{DD} scaling.

Figure 4-10 shows the overall scalability evaluation of the proposed FinHEMT. For sub-10 nm scaling with the equivalent total EOT with FinFET, 28% enhanced I_{ON} can be achieved for FinHEMT mainly due to higher electron mobility in QW channel while having lower capacitance. In technology aspects, more aggressive gate dielectric EOT scaling would be possible in FinHEMT since the additional SiGe layer can suppress the gate leakage current more effectively than in FinFET. If this ultimate gate dielectric EOT scaling is considered for FinHEMT, I_{ON} can be enhanced further.

4.3 RF characteristics: cutoff/maximum frequency

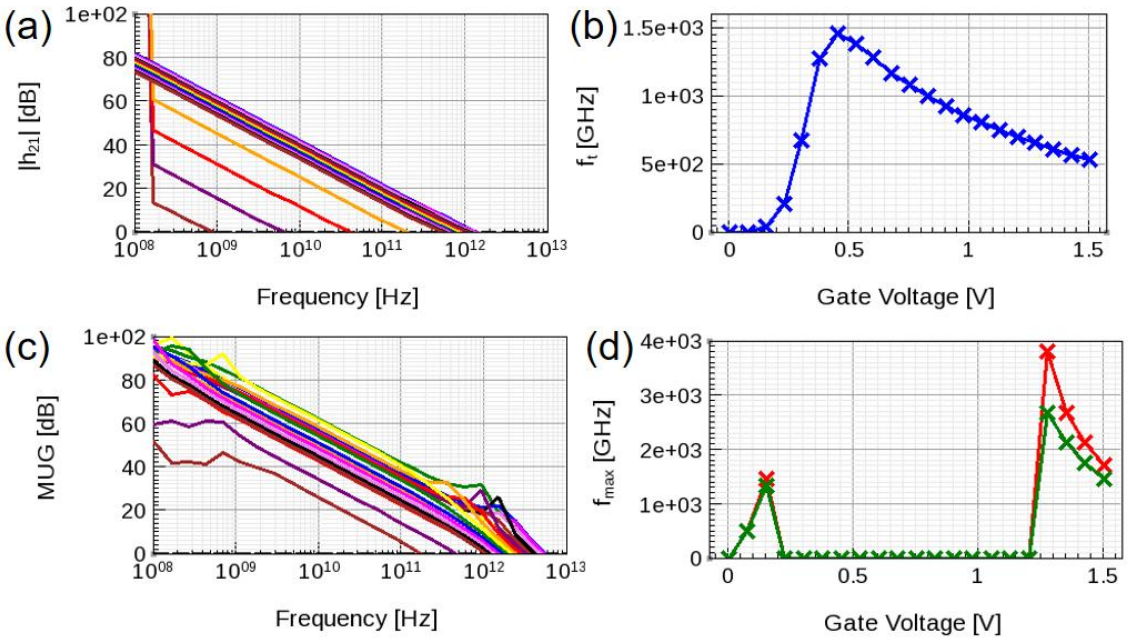

Figure 4-11. (a) $|h_{21}|$ (b) cut-off frequency f_T using unit gain method (c) MUG, and (d) maximum frequency f_{max} using unit gain method and extrapolation method for FinHEMT.

Cut-off frequency is calculated with unit gain method searching for $|h_{21}|= 1$. Here, $|h_{21}|$ is calculated as follow:

$$h_{21} = \frac{y_{21}}{y_{11}} \tag{3.1}$$

The subscript number 1 and 2 indicate the gate and drain node respectively. And Y-matrix can be converted from 2x2 conductance (A) and capacitance (C) matrix:

$$Y = A + j\omega C \tag{3.2}$$

Where j is the imaginary unit, and $\omega= 2\pi f$. Thus, the unit gain method is when $y_{21}= y_{11}$. Also, the maximum frequency f_{max} can be calculated when Mason's Unilateral Gain (MUG) is equal to 1 [45].

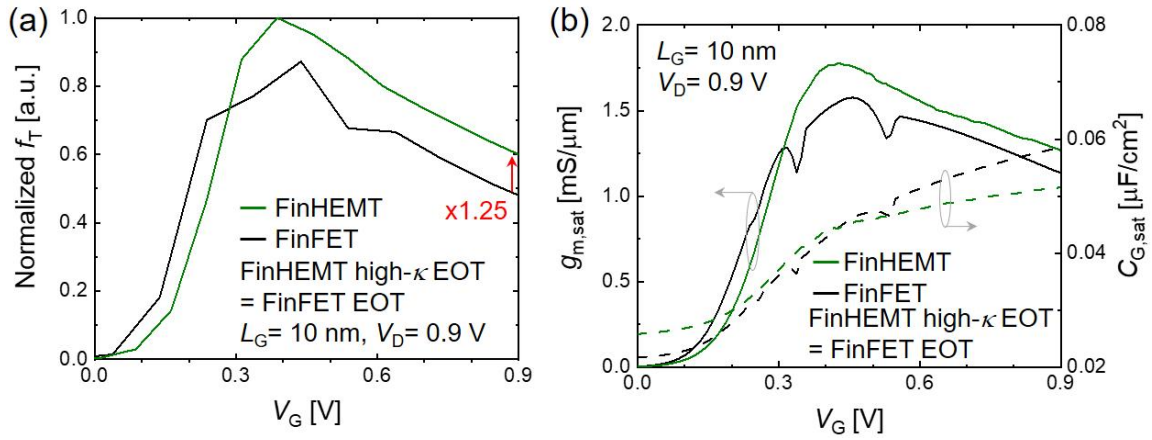

Figure 4-12. (a) Normalized cut-off frequency f_T of FinFET and FinHEMT with equivalent high-κ EOT. (b) Transconductance $g_{m,sat}$ and gate capacitance $C_{G,sat}$ at V_D= 0.9 V.

As well as better DC performance, a higher cutoff/maximum frequency (f_T/f_{max}) than conventional FET can be expected due to the lower capacitance in FinHEMT. In long channel regime, 2 times enhanced mobility (**Figure 3-7**) can be revealed as cutoff frequency enhancement from the following equation: $f_T = \frac{g_m}{2\pi C_G} = \frac{1}{2\pi}\frac{WV_D}{L}\mu$. Moreover, in short channel regime, we confirmed this expectation using TCAD f_T simulation with unity gain method for FinHEMT (8% I_{ON} increment) and FinFET as shown in **Figure 4-12**. The simulation results of $g_{m,sat}$ and $C_{G,sat}$ at V_D= 0.9 V in **Figure 4-12(b)** and the extracted values at V_{DD}=V_G=V_D= 0.9 V are $g_{m,sat}$= 1.25 mS/μm, $C_{G,sat}$= 5.15x10^{-2} μF/cm^2 for FinHEMT and $g_{m,sat}$= 1.14 mS/μm, $C_{G,sat}$= 5.85x10^{-2} μF/cm^2 for FinFET respectively. Therefore, there is 1.25 times enhancement even with the lower capacitance (thicker EOT) in FinHEMT than in FinFET as shown in **Figure 4-2(b)** $f_{T,FinHEMT} = \frac{1.10 \times g_{msat,FinFET}}{0.88 \times 2\pi C_{G,sat,FinFET}} = 1.25 f_{T,FinFET}$.

4.4 Improved reliability

As the gate length get shorter, the electric field between source and drain become higher causing hot carrier injection (HCI) in insulator from channel. The Fiegna model explains this phenomenon simply by multiplying the gate leakage probability to drain current as shown below [46]:

$$I_g = q\int P_{ins}\left(\int_{E_{B0}}^{\infty} v_{\perp}(\varepsilon)f(\varepsilon)g(\varepsilon)d\varepsilon\right)ds \tag{4.1}$$

Here, $v(\varepsilon)$ is velocity, $f(\varepsilon)$ is fermi-dirac distribution function, and $g(\varepsilon)$ is density-of-state as a function of energy ε. And injection probability P_{ins} from the channel to insulator is:

$$P_{ins} = \begin{cases} \exp\left(-\dfrac{x_0}{\lambda_{ins}}\right) & E_{ins} < 0 \\ \exp\left(-\dfrac{t_{ins}-x_0}{\lambda_{ins}}\right) & E_{ins} > 0 \end{cases} \tag{4.2}$$

where x_0 is the distance from the interface to maximum position of barrier, and λ_{ins} is the mean-free path in insulator. λ_{ins} is highly affected by the temperature and inversion charge density [16]

$$x_0 = \min\left(\sqrt{\frac{q}{16\pi\tilde{\varepsilon}_{ins}|E_{ins}|}}, \frac{t_{ins}}{2}\right) \tag{4.3}$$

where $\tilde{\varepsilon}_{ins}$ is average permittivity of insulator as follow:

$$\tilde{\varepsilon}_{ins} = \varepsilon_{ins}(\varepsilon_{sem}+\varepsilon_{ins})/(\varepsilon_{sem}-\varepsilon_{ins}) \tag{4.4}$$

Here, ε_{ins} and ε_{sem} is permittivity of insulator and semiconductor.

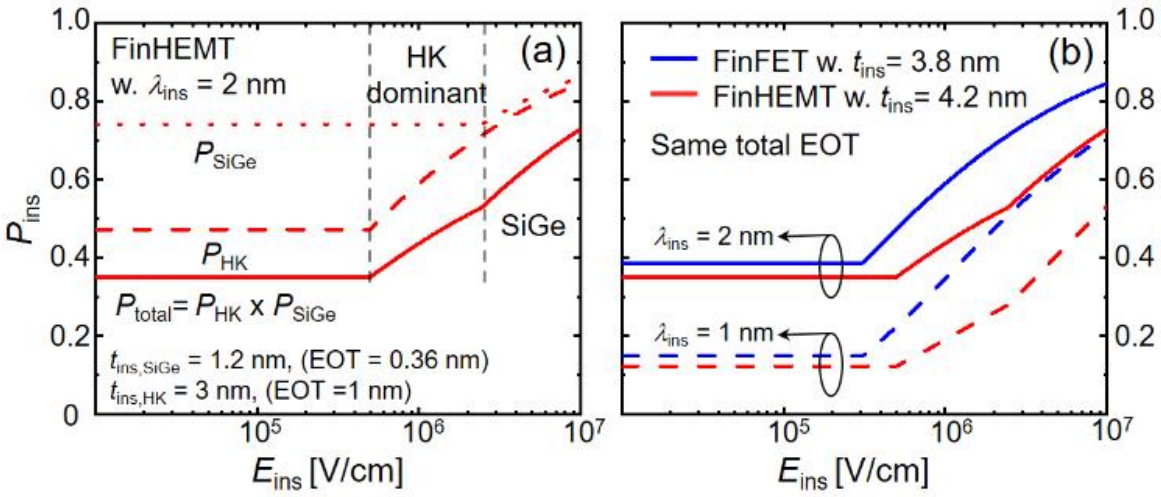

Figure 4-13. (a) Injection probability component effects for FinHEMT (b) Injection probability with λ_{ins}= 1, 2.

Figure 4-14(a) presents the injection probability for FinHEMT considering HK dielectric and SiGe layer injection from the channel. For the calculation, we consider that the thickness of SiGe behaving as an additional EOT is 1.2 nm (detailed in Section 4.1.) and thickness of HK is 3 nm with $\varepsilon_{r,HK}$= 9.75 (EOT= 1 nm). Therefore, total injection probability is P_{total}= P_{HK}×P_{SiGe}. Although the total EOT is equivalent for FinHEMT and FinFET, there is physical thickness difference 0.4 nm only owing to the permittivity of SiGe ($\varepsilon_{r,SiGe}$= 13) is greater than HK. Moreover, 10% of P_{ins} difference is shown in **Figure 4-14(b)** for λ_{ins}= 1 and 2 nm even 0.4 nm of physical thickness of insulator.

The kinetic equation of hydrogen bond at the interface is follow [47]:

$$\begin{aligned}
&\frac{dN_{hb}}{dt} = -\nu N_{hb} + \gamma\left(N - N_{hb}\right) \\
&\gamma = \gamma_0\left[N_H / N_H^0 + \Omega\left(N_{hb}^0 - N_{hb}\right)\right] \\
&\gamma_0 = \frac{N_{hb}^0}{N - N_{hb}^0}\nu_0
\end{aligned} \tag{4.5}$$

$$\begin{aligned}
&\nu = \nu_0 \exp\left(\frac{\varepsilon_A^0}{kT_0} - \frac{\varepsilon_A^0 - \Delta\varepsilon_A}{\varepsilon_T}\right) k_{FN} k_{HC} \\
&\varepsilon_T = k_b T + \delta_{\|}\left|E_{\|}\right|^{\rho_{\|}} \\
&k_{FN} = 1 + \delta_{Tun}\left|I_{Tun}\right|^{\rho_{Tun}} \\
&k_{HC} = 1 + \delta_{HC}\left|I_{HC}\right|^{\rho_{HC}} \\
&\Delta\varepsilon_A = -\delta_{\perp}\left|E_{\perp}\right|^{\rho_{\perp}} + (1+\beta)\varepsilon_T \ln\left(\frac{N - N_{hb}}{N - N_{hb}^0}\right)
\end{aligned} \tag{4.6}$$

Here, ν is reaction constant, ν_0 is depassivation constant, ε_T is threshold energy, k_{FN} and k_{HC} is a constant suppling the effects of tunneling, and hot carrier injection respectively, and $\Delta\varepsilon_A$ is the change of activation energy by vertical electric field.

Considering Spherical Harmonic Expansion (SHE) method [48], there is additional constant k_{SHE}:

$$k_{SHE} = 1 + \delta_{SHE}\frac{qg_v}{2}\int_{\varepsilon_{th}}^{\infty}\left(\min\left[\exp\left(\frac{\varepsilon - \varepsilon_a}{kT}\right), 1\right] g(\varepsilon) f(\varepsilon) v(\varepsilon)\right) d\varepsilon \tag{4.7}$$

Where, δ_{SHE} is a prefactor, ε_{th} is a threshold energy, ε_a is an activation energy to break the passivated hydrogen bond, g_v is the valley degeneracy, and $g(\varepsilon)$, $f(\varepsilon)$, and $v(\varepsilon)$ are the density of states, electron energy distribution and magnitude of the electron velocity respectively.

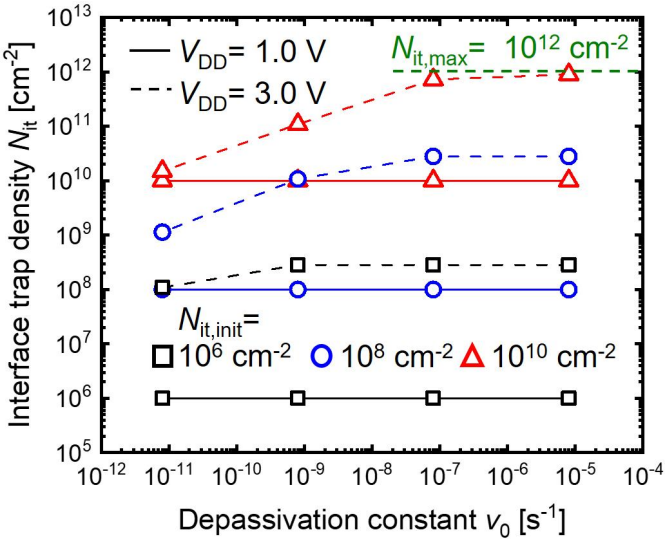

Figure 4-14. Interface trap density as a function of depassivation constant with initial N_{it}= 10^6, 10^8, 10^{10} cm^{-2} and V_{DD}= 1.0, and 3.0 V

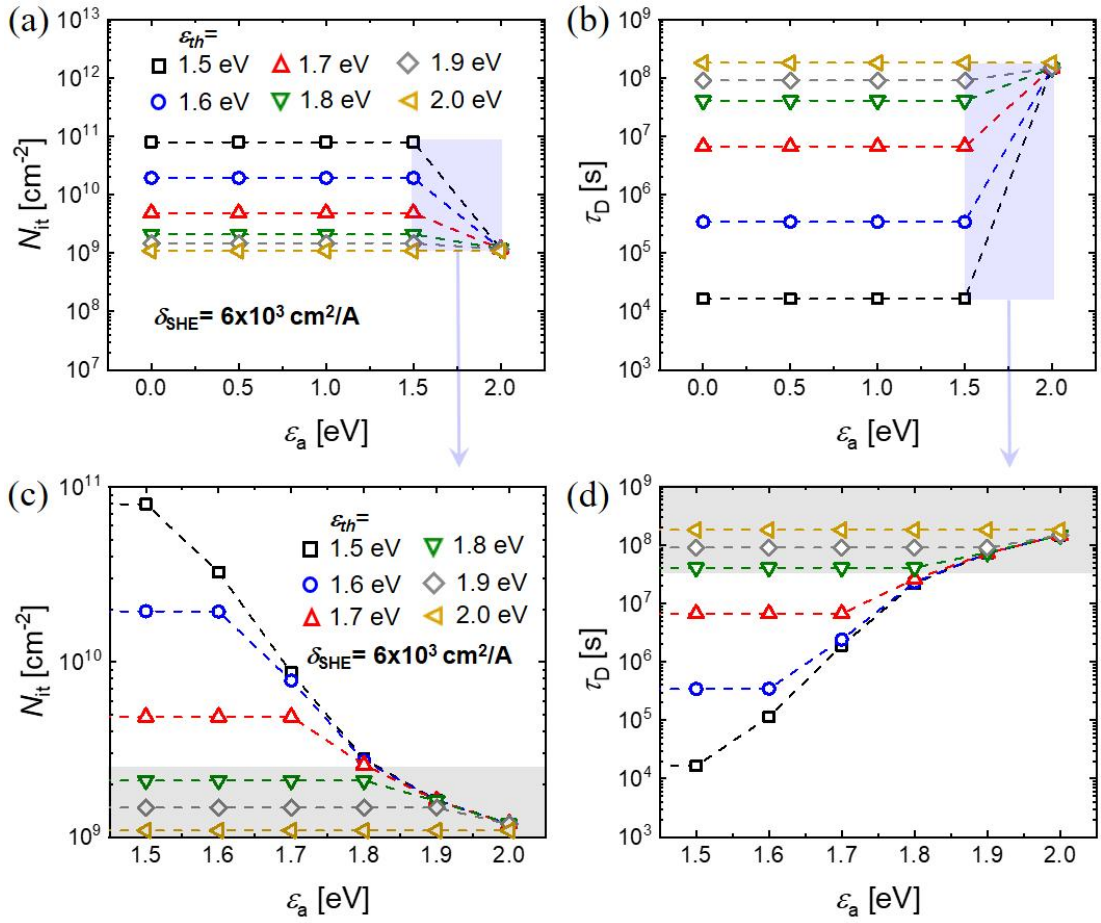

Figure 4-15. ε_{th}, ε_a sensitivity analysis on (a),(c) N_{it} and (b),(d) τ_D

A rigorous simulation is performed to find the interface trap density N_{it} range for the device lifetime (= degradation time τ_D, $\tau_D = \left(\frac{v^{stress}}{v}\right) \times \tau_D^{stress}$) over 1 year. **Figure 4-14** shows the results of changing the depassivation constant, and the initial N_{it} are 10^6, 10^8, and 10^{10} cm^{-2} with maximum N_{it} is 10^{12} cm^{-2}, V_{DD}= 1.0 and 3.0 V. And we change the ε_a and ε_{th} considering standard deviation $\sigma_{\varepsilon a}$= 0.35 eV [49] as shown in **Figure 4-15**. Therefore, $N_{it} < 2.5\times10^9$ cm^{-2} is necessary for over 1 year of device lifetime (gray area in **Figure 4-15(c)(d)**).

The physical thickness of SiGe layer behaving as a HK dielectric insulator is 1.2 nm. Although the mean-free path increases to 2 nm, it is shorter than total insulator thickness resulting no change in drain current with stress time. Therefore, the proposed FinHEMT has improved reliability than FinFET.

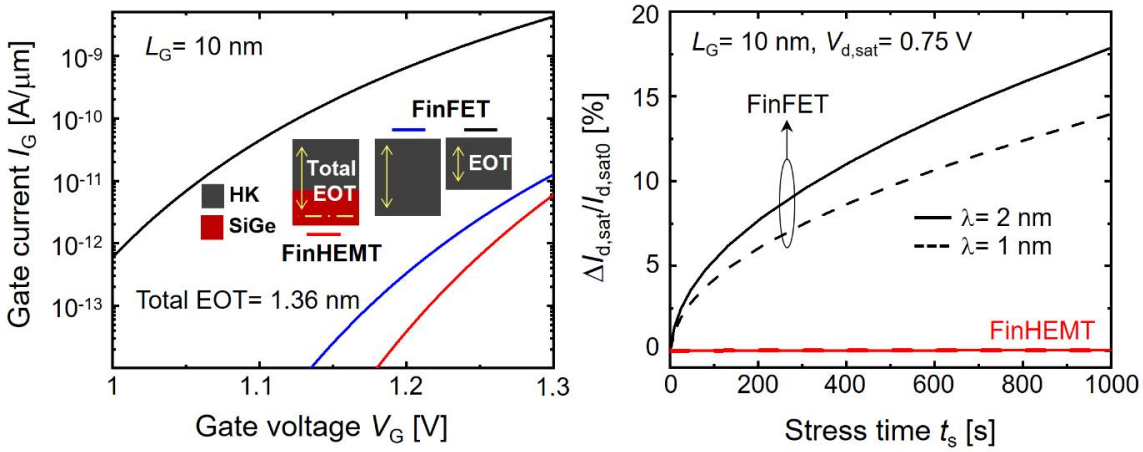

Figure 4-16. (a) Gate leakage current (b) drain current variation.

5. Conclusion

Highly scalable and variability-immune Si FinHEMT has been demonstrated with “well-tempered” 10 nm gate length characteristics. Highly enhanced electron mobility ~ 1100 cm^2/Vs close to bulk-Si value and doubly enhanced effective mobility are achieved in FinHEMT by degrading SRS in s-Si QW channel, which results in highly improved mA-level on-current than that of FinFET with the same gate controllability. FinHEMT also shows an excellent uniformity to the underlap length and fin width variations owing to the low resistivity in the gate underlap and channel region. The FinHEMT is predicted to exhibit excellent scalability and sturdiness to process variability, and may be a promising device platform in mainstream Si technology scaling. Moreover, the operation principle of SiGe layer which behaves as an additional HK insulator improve the reliability of FinHEMT suppressing the gate leakage current.

6. Remaining work to be done

- Theoretical modeling of FinHEMT operation

  Atomistic modeling and experiments of channel mobility by SRS.

  Analytical modeling of VT and ID based on the unique band structure.

- Reliability evaluation window development

  Analyze the effect of device parameters on reliability.

  Comparing with experimental data, enhance the effectiveness of the evaluation window.

  Extend it to circuit level.

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