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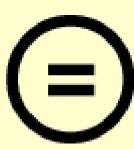

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Doctoral Thesis

Multi-Functional Optoelectronic Heterostructure Devices Based on Transfer Printing of Nanomaterials

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School of Energy and Chemical Engineering
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Ulsan National Institute of Science and Technology

2021

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Multi-Functional Optoelectronic Heterostructure Devices Based on Transfer Printing of Nanomaterials

A thesis/dissertation submitted to
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in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

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Multi-Functional Optoelectronic Heterostructure Devices Based on Transfer Printing of Nanomaterials

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Abstract

Heterostructure devices, combining different electronic properties of semiconductors, offer novel electronic functionalities, which are critically required in emerging applications in high performance and multi-functional electronics. Previously, heterostructure devices have attracted a great attention due to the enhancing performances, adding functionalities and broadening absorption range, through components modulation, resulting in many applications in high electron mobility transistors, non-volatile memory, light emitting diodes, and broadband photodetectors. However, traditional semiconductor heterostructures present significant challenges due to the lattice constant mismatch with other substrates and generation of defects during the direct growth and deposition processes. To address these challenges, a transfer printing was introduced to heterogeneously integrate various nanomaterials onto arbitrary substrates, whereby the bonding at heterointerfaces with a large lattice mismatch is facilitated by van der Waals forces during the transfer printing processes. The transfer printing can provide a freedom of material choice, from zero to three dimensional materials, in the formation of heterostructures without the restriction from lattice mismatch, which enabled various heterostructure devices with unique physical properties.

In this thesis, we demonstrate multi-functional optoelectronic heterostructure devices based on transfer printing of nanomaterials. First, in chapter 1, we briefly introduce the research trends in electronic devices and basic concept of transfer printing methods and multi-functional heterostructure devices. In chapter 2, we demonstrate a new type of heterostructure device based on black phosphorus and n-InGaAs nanomembrane semiconductors. The device offers gate-tunable rectification and switching behaviors. In addition, the proposed heterojunction diode can be programed by the modulation of forward current due to the capacitive gating effect. Furthermore, the device is photoresponsive in a spectral range spanning the ultraviolet to near infrared. In chapter 3, we describe the fine patterning technique of silver nanowires on various substrates using vacuum filtration and transfer printing process. This technique provides very simple and cost-effective fabrication for fine patterning of AgNWs electrode for optically transparent and mechanically flexible optoelectronic device applications. This patterning technique can be applied to other nanomaterials such as CNT and graphene and combination of nanomaterials to realize highly flexible and transparent optoelectronic devices. In chapter 4, the large-area MoS_2 film and pattering process is demonstrated by shadow mask assisted transfer printing process. The liquid exfoliated MoS_2 flakes can be easily patterned by vacuum filtration with polyimide shadow mask. Patterned film is transferred to arbitrary substrate by using transfer printing process for high performance and flexible electronic applications. Therefore, the heterostructure devices made by transfer printing are advantageous in scalability and avoids complicated fabrication process for multi-functional applications.

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Nomenclature

0D	Zero-dimensional
1D	One-dimensional
2D	Two-dimensional
AAO	Anodic aluminum oxide
AC	Alternation current
AFM	Atomic force microscopy
AgNW	Silver nanowire
BJT	Bipolar junction transistor
BP	Black phosphorus
CNT	Carbon nanotube
CVD	Chemical vapor deposition
DCM	Dichloromethane
DI	Deionized
DMF	Dimethylformamide
DRAM	Dynamic random access memory
EDS	Energy dispersion X-ray spectroscopy
FE-SEM	Field emission scanning electron microscopy
FET	Field-effect transistor
FG	Function generator
FTE	Flexible and transparent electrode
h-BN	Hexagonal boron nitride
HEMT	High-electron-mobility transistors
HRTEM	High-resolution transmission electron microscopy
IC	Integrated circuit
IoT	Internet of Things
IPA	Isopropyl alcohol
ITO	Indium tin oxide
KPFM	Kelvin probe force microscope
LD	Laser diode
LED	Laser emitting diode
MOSFET	Metal-oxide-semiconductor field-effect transistor

MRAM	Magnetic random access memory
MSM	Metal–Semiconductor–Metal
NIR	Near infrared
NOA	Norland Optical Adhesives
NW	Nanowire
OM	Optical microscopy
PC	Pulsating current
PDDA	Poly(diallyldimethylammonium chloride)
PDMS	Polydimethylsiloxane
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
PLLA	Poly-L-lactide
PMMA	Poly(methyl methacrylate)
PVA	Polyvinyl alcohol
PVP	Polyvinylpyrrolidone
RF	Radio frequency
rGO	Reduced graphene oxide
RIE	Reactive ion etching
RMS	Root-mean-square
RRAM	Resistive random access memory
SEM	Scanning electron microscopy
SRAM	Static random access memory
SWNT	Single-walled carbon nanotube
TFSI	Bis(trifluoromethane)sulfonimide
TFT	Thin film transistor
THAB	Tetraheptylammonium bromide
TMDC	Transition-metal dichalcogenides
UV	Ultraviolet
XRD	X-ray diffractometer

Chapter 1. Introduction

1.1 Research background

In the past century, electronic devices have been continuously developed from huge and simple single devices to tiny and complicate integrated devices.[1] In this progress, the processing capability and scaling down of devices were intensely focused for high performance and low fabrication cost. However, these trends were changed because the innovation of technology has been accelerated with the Fourth Industrial Revolution. Recently, electronic devices become human friendly with various functionalities such as transparency, wearability and accessibility for improving human convenience (Figure 1.1).[2] Furthermore, the development of Internet of Things (IoT) derives the enhanced human-machine interface which makes humans easily to manage the functionalities of devices.[3] Following these trends, the next-generation electronic devices will much be related with human compatibility and multi-functionalities such as wearable electronics, augmented reality and neuromorphic system.[4] But, the multi-functional electronics with conventional semiconductor materials (e.g. Si, Ge) and device structures face a challenge due to the limitation of performance and functionality, resulting in demands for new materials and structures.

To securing multi-functionalities in electronic devices, various nanomaterials, including quantum dot, metallic nanowires and two-dimensional (2D) materials, have been intensively researched. Especially, 2D materials with mechanical stability, novel electrical properties, high mobility and atomic sharp surface were spotlighted as the next-generation materials.[5] Also, the metallic nanowires were frequently used as a substitute of metal electrode because of good mechanical strength, conductivity, transparency and flexibility, which are proper for multi-functional device applications. These various nanomaterials were conjugated as the heterostructure devices which enable fabricating multi-functional electronic devices for applications in junction field-effect-transistors, memory devices and flexible photodetectors.[6] As a result, it is essential that various nanomaterials are liberated from the choice of materials in fabricating heterostructures for next-generation electronic devices with exceptional functionalities (Figure 1.2).[7]

However, the traditional fabrication process for the heterostructure devices was suffered from lattice mismatch during the direct growth and thermal deformation caused by high temperature during fabrication process, resulting in limitation in the choice of materials (Figure 1.3). To address these challenges, a transfer printing technique was introduced to heterogeneously integrate various nanomaterials onto arbitrary substrates by easy control of adhesion between stamp, material and substrate.[8] The transfer printing enabled various heterostructure devices to be formed without limitations in material choice, which have been utilized in multi-functional and high-performance

applications (Figure 1.4).[9] Furthermore, recently developed nanomaterials also efficiently exploit their unique properties by association with other materials and substrates through the transfer printing process.

1.2 Multi-functional heterostructure devices

With the rapid development of technology, the multi-function of electronic devices is becoming general trend. By achieving multi-functionality in a single device, the electronic devices can be improved in scalability and processing capability as well as broadened applications, such as advanced logic circuit, wearable electronics, flexible display and neuromorphic memory.[10-12] However, the homogenous structures have several limitations in terms of functionality due to restricted electrical and mechanical properties of conventional semiconductor materials. Therefore, many researchers have investigated new emerging materials and effective device structures to develop functional devices. Especially, nanomaterials including 2D materials, quantum dots and nanowires have been utilized as combined active layers or stacked on polymeric substrates, called as heterostructure devices (Figure 1.5).[13] Recently, the heterostructure devices based on nanomaterials, which can simultaneously act as diode, transistor and photodetector[14] or diode, memory and photovoltaic[15] were reported with novel multi-functionalities. In this section, we will briefly describe various research fields, which used heterostructures with nanomaterials for employing complementary features of each materials

1.2.1 Heterostructure for diode

Diodes are essential building blocks for modern electronics and optoelectronics, which have the characteristic of passing current in one direction only.[16] The diode commonly has been used as the platform to develop novel semiconductor devices, such as clipper circuit, laser emitting diode (LED), solar cell, laser diode (LD) and photo diode.[17] Traditionally, it was fabricated by p-type and n-type doping on homogenous semiconductor materials, resulting in the formation of p-n junction. However, it is now possible to realize various heterostructures for p-n junctions with development of nanomaterials.[13] Especially, the lack of dangling bonds on the surface of 2D materials enables the improvement of quality in heterointerface and device performance.[18] By using diverse 2D materials with different band gaps and work functions, bandgap engineering of heterojunction is allowed for tunneling diode[19] and negative differential resistance device.[20] Moreover, the tunability in carrier densities and band alignments of nanomaterials offer novel designs of functional heterostructures.[21] For example, heterojunction diode based on the integration of p-type single-walled carbon nanotubes (SWNTs) and MoS_2 showed gate tunable rectifying behaviors because of electrostatic inversion of SWNT (Figure 1.6a).[22] In addition, $SnSe_2/MoTe_2$ heterostructures can exhibit both Esaki diode and backward diode as the applied gate voltages, caused by large difference in electron affinities (Figure

1.6b).[23] As a result, the heterostructure with nanomaterials can provide a platform for future multi-functional applications in diode devices. Here, we also briefly explain about the knowledge of basic parameters for the evaluation of diode performances.

***Rectification ratio*:** Rectification ratio is a figure of merit for comparing the effectiveness of rectification. Generally, it is defined as the ratio of reverse (I_R) and forward (I_F) currents at the same source–drain bias magnitude. Therefore, it can be expressed by $|I_F/I_R|$.

***Ideality factor (η)*:** The ideality factor of a diode is a measure of how closely the diode follows the ideal diode equation. It can be estimated by fitting the Shockley diode equation ($I = I_0\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right]$), which can be defined as $\eta = \frac{q}{kT}\left(\frac{\partial V}{\partial \ln I}\right)$, where I_0 is the reverse bias saturation current, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. Here, the ideality factor has to be a value of 1 in an ideal state. If it is higher than 1, the diode is considered to be influenced by the trap states and the resistance of the heterojunction in the interface.

1.2.2 Heterostructure for transistor

Transistor is one of widely used semiconductor devices in modern industry, which can control the current flow between two other terminals by applying voltage or current to another terminal.[24] It has been mainly used in digital circuit for switching or amplifying of electric signals. By integration with other devices such as diode, resistor, capacitor and inductor, transistor becomes a basic unit in integrated circuit (IC) which has calculating ability in computer. Therefore, the advance in transistor is significantly important for the development of information processing technology. Previously, the transistor was investigated for scaling down and low power consumption with efficient device structures, like bipolar junction transistor (BJT) and field-effect transistor (FET). Nowadays, the heterostructure with nanomaterials has been applied in transistors for its own purposes, such as scalability,[25] efficient architecture[26] and high performance (Figure 1.7).[27] In addition, nanomaterials in transistor induce novel device structures such as a hot electron transistor by using ultrashort channel less than the mean-free-path of carriers.[28] Furthermore, combination of nanomaterials with ferroelectric materials[29] or organic semiconductors[30] can lead to improved performance and flexibility, respectively. In summary, the adoption of nanomaterials in transistor devices can provide new opportunities for novel applications in future electronics. In the following parts, figures of merit for transistors are introduced for comparison of performances.

***Mobility(μ)*:** Mobility indicates the speed of carrier movement in channel layer under the electric field, which can be defined as $\mu = \frac{\partial I_{DS}}{\partial V_G}\left(\frac{L}{W C_i V_{DS}}\right)$, where L, W, and C_i denote channel length, channel width, and specific capacitance between the channel and the gate per unit area. The specific capacitance

can be obtained using the parallel-plate capacitor equation $C_\mathrm{i} = \varepsilon_0\varepsilon_\mathrm{r}/d$, where ε_0, ε_r, and d are the vacuum dielectric constant (8.85×10^{-12} F/m), dielectric constant of dielectric material, and thickness of dielectric material, respectively.

On/off ratio**:** On/off ratio is the ratio of on-current (I_on) and off-current (I_off), which is controlled by the applied gate voltage at the same drain–source voltage. In other words, it's the ratio of the current in accumulation mode over the current in depletion mode. Therefore, it is defined as $I_\mathrm{on}/ I_\mathrm{off}$.

Subthreshold swing (SS)**:** Subthreshold swing is the change in gate voltage needed to increase the drain current by one order of magnitude, which is defined as $SS = \mathrm{d}V_\mathrm{g}/\mathrm{d}(\log I_\mathrm{ds})$, where V_g and I_ds denote gate voltage and drain−source current, respectively. It is closely related with power-consumption of devices.

1.2.3 Heterostructure for memory

Memory has become the basis of information storage system, which is central importance for data processing and computing devices in modern industry.[31] Memory devices have been continuously developed into various device structures such as static random access memory (SRAM), dynamic RAM (DRAM), magnetic RAM (MRAM), resistive RAM (RRAM) and ferroelectric RAM (FeRAM).[32] However, the innovation of memory devices are necessary to follow the demands for fast speed, scaling down, low power and fabrication cost with the Fourth Industrial Revolution. Therefore, many researchers have intensively studied to realize superior memory devices with nanomaterials in heterostructure. Recently, heterostructure memory devices which can be operated by both applied voltage and incident light from artificial trap site[33] and photogate effect,[34] was reported for low-power consumption. In addition, high performance memory devices with large memory window and stable retention were developed by using 2D materials[35, 36] and nanoparticles[37] as floating gate materials. Furthermore, tremendous efforts have been dedicated for synaptic memory devices, mimicking the energy-efficient neurons in the human brain.[38] Especially, phase-engineered 2D heterostructure can offer considerable power-saving benefits by emulating synaptic functionality, such a short- and long-term plasticity (Figure 1.8).[39] Consequently, the heterostructure with nanomaterials improve the performance and extend application field of memory devices. The detail parameters which are important in memory device are briefly introduced in following part.

Program/erase ratio**:** It is the ratio of the current at programed state (I_P) and at erased state (I_E), which is described as $I_\mathrm{P}/I_\mathrm{E}$.

Retention time**:** Retention time refers to the ability of a memory to retain its data state over periods of time regardless of whether the device is powered off.

1.2.4 Heterostructure for photodetector

Photodetectors are devices used for the detection of light, which can convert light signals to electrical signals.[40] So far, the photodetector technologies have been developed for practical use in human life and covered broad applications such as digital camera, night vision, optical communication, biomedical imaging and flame detection.[41] Conventional photodetectors based on silicon, germanium and indium gallium arsenide (InGaAs) have limitations in terms of spectral range, flexibility, transparency, resolution and compatibility with other devices. However, recently investigated nanomaterials can overcome these challenges benefitting from mechanical flexibility and excellent optoelectrical properties.[42] Photodetector based on heterostructures of 2D materials offer high responsivity[43] and broadband detection range.[44] Moreover, the efficient detection in photodetector with 2D material is possible in combination with perovskite[45] and quantum dot.[46] In addition, by adjusting the substrate, stretchable photodetector was realized for potential applications in wearable electronics.[47] Furthermore, vertical point heterostructure, in which 2D material is sandwiched by two cross-stacked nanowires, was demonstrated for nanoscale resolution imaging ability.[48] As a result, the facile integration of various nanomaterials in photodetectors paves the way for high performance, broadband detection and wearable applications.[49] Here, the key figure of merits in photodetectors are described for standard comparison.

***Photoresponsivity (R_{ph})*:** Photoresponsivity is the ratio of generated photocurrent over the incident optical power, which can be expressed by $R_{\mathrm{ph}} = \frac{J_{\mathrm{ph}}}{P_{\mathrm{light}}}$, where J_{ph} is photocurrent density, P_{light} is optical power of incident light.

***Detectivity (D*)*:** Detectivity represents the ability to distinguish a signal from noise, which is defined as $D^{*} = \frac{\sqrt{A}}{NEP} \cong \frac{R_{\mathrm{ph}}}{\sqrt{2qJ_{\mathrm{d}}}}$, where A is the effective area of detector, *NEP* is noise-equivalent power, q is the electron charge, and J_d is dark current density and R_{ph} is photoresponsivity.

***Response time*:** It is the time required for changes of photocurrent from 10% to 90% or 90% to 10% of its peak value.

***On/Off ratio*:** On/off ratio is the ratio of photocurrent (I_{ph}) and dark current (I_d) at same anode voltage. So, it is defined as I_{ph}/ I_d.

***Spectral responsivity range*:** Spectral responsivity range is the range of optical wavelengths in which the photodetector has a significant responsivity. Generally, it is strongly related with the band gap of active semiconductor materials.

1.3 Transfer printing

According to the emergence of multi-functional electronics with nanomaterials, the assembly technology has been spotlighted for adoption of novel features in each material without critical damages.

Especially, much interest of human compatible devices, such as bio-integrated electronics,[50] curvilinear electronics,[51] human–machine interface[52] and wearable electronics,[53] require the conformal attachment of active layer to various polymeric substrates. However, the difference of thermal and mechanical properties, such as thermal tolerance and crystallinity between nanomaterials and polymeric substrates was pointed out as a critical limitation of directly manufacturing nanomaterial onto polymeric substrate. In recent years, a novel strategy, transfer printing, which transfers completely solid objects from a donor substrate to a receiver substrate was proposed for advance in the assembly technology.[8] This method can separate the fabrication process from integration of substrate, avoiding incompatibility of polymeric substrate with the extreme processing conditions such as high temperature and chemical etching.[54] Therefore, transfer printing method enables various kinds of materials form bulk semiconductor to quantum dot to be liberated from restriction of substrate choice, resulting in further broadening its applicable scope.

1.3.1 Strategies for transfer printing

Basically, the transfer printing is enacted by the control of adhesion when the target material on donor substrate is attached to receiver substrate.[55] In natural, this method is dominantly depending on the kinds of materials which are used as donor, receiver substrates and target materials because the adhesion is related with the surface energy of each material. However, in this case, the transfer printing method is hardly limited in the material choice. For efficient transfer printing, several strategies have been successfully developed using different techniques with planar or structure-modified elastomeric stamps, adhesive layers and polymeric thin film (Figure 1.9). In this section, we briefly discuss about these developed strategies for transfer printing.

***Transfer printing using planar elastomeric stamp*:** Generally, the simple transfer printing method utilizes planar elastomeric stamp, such as Ecoflex, polydimethylsiloxane (PDMS), and polyurethane. To transfer the target material from donor substrate to receiver substrate with mediated stamp, the adhesion between target material and stamp has to be higher than that between target material and donor substrate. On the other hand, the adhesion must be lower than that between target material and receiver substrate. If the above two conditions cannot be satisfied at the same time, the yield of transfer will be exceedingly low. To solve this difficulty, kinetically controlled transfer printing methods have been introduced.[56] Due to the viscoelastic motion of the elastomeric stamp, the adhesion process during transfer printing process depends on the separation kinetics, the peeling speed of the stamp (Figure 1.10). The separation of two different substances is resulted from the propagation of the failure of their interface. In the case of the elastomer–object interface, the failure of their interface propagates via the deformation of the elastomer. Owing to its viscoelastic movement, high peeling speed of the elastomer does not provide enough time to make a deformation of the viscoelastic elastomer. In this result, the

propagation of the failure of the elastomer–object interface is interrupted, and eventually the printable object is attached to the elastomer. In slow peel off process, elastomer has enough time to deform, and the separation between those two substances consequently occurs as the interface failure propagates more easily. In conclusion, the printable object can be more easily grabbed off from donor substrate by quickly peeling back the stamp and the transfer of object onto receiver substrate from the stamp is achieved by slowly peeling back the stamp.

Transfer printing with an aid of adhesive layer**:** Where donor and receiver substrate have similar surface energy or the receiver substrate has poor interface, the support of an adhesive layer can enable high yield of transfer printing.[57, 58] Here, the uncured adhesive layers such as SU–8, NOA, and poly(methyl methacrylate) (PMMA), are coated onto the receiver substrates. Then, the uncured can flow around and cover all revealed area of target material including even its edge when the target material is attached to the receiver substrate. Thus, more fine and large-area contact is possible, and after curing process the strong bonding force between those adhesive layers and the target material is generated (Figure 1.11). Because of artificially made strong adhesion, this method is not restricted by the kinds of target materials and receiver substrates. Therefore, this method is commonly used for transfer of nanowire type materials which has small contact area and very thin film as receiver substrate.

Transfer printing using structure-modified elastomeric stamp**:** Structure-modified elastomeric stamp has been intensively studied for switchable adhesion in response to stimuli such as temperature and pressure. It is very promising method because the adhesion of stamp can be differently controlled when the target materials are detaching from the donor substrate or attaching to the receiver substrate without any damage or contamination of materials. One of used structure is microtip structure for change of contact area (Figure 1.12a).[59] The adhesive strength based on van der Waals interaction between the stamp and the target material can be controlled as the contact area between them. Here, the contact area between microtip-structured stamp and target object is controlled by the amount of preload during approach of the stamp. In other studies, microcavity structure was demonstrated by mimicking octopus-suckers which can control cavity-pressure-induced adhesion through the muscle actuation (Figure 1.12b).[60] The adhesion is switchable in response to the temperature because thermal responsive hydrogel is coated on microcavity structure of elastomeric stamp, inducing controllable cavity pressure by volume change in microcavity. Transfer printing by using structure-modified elastomeric stamp can efficiently transfer various materials from nano- to macroscale regardless damages or contaminations, providing potential use in commercial industry.

Transfer printing mediated by polymer thin film**:** In transfer printing process, polymeric film such as PMMA, cellulose acetate butyrate, poly-L-lactide (PLLA), and poly(diallyldimethylammonium chloride) (PDDA) is occasionally used as a carrier during transfer printing process instead of elastomeric stamp.[61, 62] These polymers can be simply coated by spin-coating, dip-coating, drop-casting

with thin layer and easily removed by rinsing with or immersing in solvents such as acetone, dichloromethane (DCM), and water. Therefore, this method can completely grab the target materials by coating of polymer and successfully transfer them to desired substrate by rinsing of polymer (Figure 1.13). Through this transfer printing strategy, the clean transfers of zero-dimensional (0D) Au nanoparticles, one-dimensional (1D) Ag nanowires, 2D nanosheets such as graphene, molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), and even their composites were achieved successfully.[63] Accordingly, this method facilitates the fabrication of various nanomaterials and functional architecture, which can be used for multi-functional applications.

1.4 Challenges of previous works

As we mentioned earlier, multi-functional devices based on heterostructure of nanomaterials have been vigorously researched for future electronics. Although various types of heterostructure have been realized by using transfer printing technique, there are still challenges for further development of performance, functionality and fabrication process. At first, the kinds of semiconductor materials which was commonly used for multi-functional applications are limited. In formation of heterostructure, the choice of materials is mostly important because the properties of heterostructure are partly influenced by characteristics of used materials. Therefore, many factors such as environmental stability, electrical conductivity, processability, band gap and gate tunability, are considered when the materials are chosen for fabrication of heterostructure. In this regard, only restricted semiconductor materials, including graphene, hexagonal boron nitride (h-BN), transition-metal dichalcogenides (TMDCs), silicon and germanium, have been actively conjugated due to its well-known and good properties.[64] To find novel functionalities and properties in heterostructure, it is necessary to expand the scope of applicable materials, like Xenes and compound semiconductors.[65, 66]

Second, only use of transfer printing in the formation of heterostructure couldn't fully solve processing problems. Through transfer printing technique, various nanomaterials have been adopted on polymeric substrates without lattice mismatch problem and thermal deformation. However, further processes are essential for completely fabricating devices. Especially, patterning process is surely necessary for integration and enhancing device performance in modern industry. During patterning process, the heterostructure again faces the extreme conditions such as high temperature and etching process. Even though entirely fabricated devices are transferred to polymeric substrate, the active materials must undergo harsh conditions. Therefore, additory methods have to support the transfer printing technique for freely manufacturing heterostructure devices with novel functionalities and characteristics.

To address these issues, this thesis suggests multi-functional heterostructure devices with diverse nanomaterials and vacuum filtration-assisted transfer printing for future electronics (Figure 1.14). In

chapter 1, we briefly introduce the research background of heterostructure devices and transfer printing methods. In chapter 2, we demonstrate a multifunctional heterostructure device based on 2D black phosphorus and n-InGaAs nanomembrane semiconductors that exhibit gate tunable, photoresponsive, and programmable diode characteristics. This gate-tunable diode properties enable the device to offer both rectifying and switching behaviors with a maximum rectifying ratio of 2,500 and on/off ratio exceeding 10^5 for diode and transistor devices, respectively. The device also exhibits non-volatile memory properties including large hysteresis and stable retention of storage charges due to the native phosphorus oxide (PO_x). By combining the memory and gate tunable rectifying behaviors, the rectifying ratio of the device can be controlled and memorized from 0.06 to 400 by the application of gate pulse. Moreover, the device could generate three different electrical signals by combination with photoresponsivity of 0.704 A W^{-1} and gate tunable electrical property, which has a potential application in multiple logic operator. In chapter 3, we introduce a simple technique for high-resolution solution patterning of AgNW networks, based on simple filtration of AgNW solution on a patterned polyimide (PI) shadow mask. This solution process allows the smallest pattern size of AgNW electrodes down to a width of 3.5 μm. In addition, we have demonstrated the potential of these patterned AgNW electrodes for applications in flexible optoelectronic devices, such as photodetectors. Specifically, for flexible and semi-transparent UV photodetectors, AgNW electrodes are embedded in sputtered ZnO films to enhance the photocurrent by light scattering and trapping, resulting in a significantly enhanced photocurrent (up to 800%) compared to devices based on AgNW electrodes mounted on top of ZnO films. In addition, our photodetector could be operated well under extremely bent conditions (bending radius of approximately 770 μm) and provide excellent durability even after 500 bending cycles. In chapter 4, the large area MoS_2 array is demonstrated by using ion-intercalated liquid exfoliation and water-assisted transfer printing method. Here, the MoS_2 film can be easily patterned through PI shadow mask and vacuum filtration. After filtration, water-assisted transfer printing enables the patterned MoS_2 array to be transferred to desired substrates such as Si, PEN, PI film. The fabricated device exhibits mobility up to 2.8 $cm^2 V^{-1} s^{-1}$ and high photoresponsivity of 24 A W^{-1} owing to the efficient exfoliation. This simple method can derive heterostructure devices for high performance and flexible electronic applications, which are advantageous in scalability and avoids complicate fabrication process for multi-functional device applications. Finally, this thesis is summarized and future perspective of multi-functional heterostructure devices is described in chapter 5.

1.5 References

(1) Pearson, G. L.; Brattain, W. H., History of Semiconductor Research. *Proceedings of the Institute of Radio Engineers* **1955,** *43*, 1794-1806.

(2) Gu, Y.; Zhang, T.; Chen, H.; Wang, F.; Pu, Y.; Gao, C.; Li, S., Mini Review on Flexible and

Wearable Electronics for Monitoring Human Health Information. *Nanoscale Res. Lett.* **2019,** *14*, 263.

(3) Kumar, S.; Tiwari, P.; Zymbler, M., Internet of Things Is a Revolutionary Approach for Future Technology Enhancement: A Review. *Journal of Big Data* **2019,** *6*, 111.

(4) Lee, G. H.; Moon, H.; Kim, H.; Lee, G. H.; Kwon, W.; Yoo, S.; Myung, D.; Yun, S. H.; Bao, Z.; Hahn, S. K., Multifunctional Materials for Implantable and Wearable Photonic Healthcare Devices. *Nat. Rev. Mater.* **2020,** *5*, 149-165.

(5) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L., Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014,** *9*, 768-779.

(6) Jariwala, D.; Marks, T. J.; Hersam, M. C., Mixed-Dimensional van der Waals Heterostructures. *Nat. Mater.* **2017,** *16*, 170-181.

(7) Geim, A. K.; Grigorieva, I. V., Van Der Waals Heterostructures. *Nature* **2013,** *499*, 419-425.

(8) Linghu, C.; Zhang, S.; Wang, C.; Song, J., Transfer Printing Techniques for Flexible and Stretchable Inorganic Electronics. *npj Flexible Electron.* **2018,** *2*, 26.

(9) Park, J.; Lee, Y.; Lee, H.; Ko, H., Transfer Printing of Electronic Functions on Arbitrary Complex Surfaces. *ACS Nano* **2020,** *14*, 12-20.

(10) Xu, K.; Lu, Y.; Takei, K., Multifunctional Skin-Inspired Flexible Sensor Systems for Wearable Electronics. *Adv. Mater.Technol.* **2019,** *4*, 1800628.

(11) Zhu, J.; Dexheimer, M.; Cheng, H., Reconfigurable Systems for Multifunctional Electronics. *npj Flexible Electron.* **2017,** *1*, 8.

(12) Mao, J.-Y.; Hu, L.; Zhang, S.-R.; Ren, Y.; Yang, J.-Q.; Zhou, L.; Zeng, Y.-J.; Zhou, Y.; Han, S.-T., Artificial Synapses Emulated through a Light Mediated Organic–Inorganic Hybrid Transistor. *J. of Mater. Chem. C* **2019,** *7*, 48-59.

(13) Liu, Y.; Weiss, N. O.; Duan, X.; Cheng, H.-C.; Huang, Y.; Duan, X., Van Der Waals Heterostructures and Devices. *Nat. Rev. Mater.* **2016,** *1*, 16042.

(14) Huo, N.; Kang, J.; Wei, Z.; Li, S.-S.; Li, J.; Wei, S.-H., Novel and Enhanced Optoelectronic Performances of Multilayer MoS_2-WS_2 Heterostructure Transistors. *Adv. Funct. Mater.* **2014,** *24*, 7025-7031.

(15) Li, D.; Chen, M.; Sun, Z.; Yu, P.; Liu, Z.; Ajayan, P. M.; Zhang, Z., Two-Dimensional Non-Volatile Programmable P–N Junctions. *Nat. Nanotechnol.* **2017,** *12*, 901-906.

(16) Sze, M. S.; Ng, K. K., P–N Junctions. In *Physics of Semiconductor Devices*, 2006; pp 77-133.

(17) Kim, D. M., P–N Junction Diode: Applications. *Introductory Quantum Mechanics for Applied Nanotechnology*, 2015; pp 231-243.

(18) Lee, C. H.; Lee, G. H.; van der Zande, A. M.; Chen, W.; Li, Y.; Han, M.; Cui, X.; Arefe, G.; Nuckolls, C.; Heinz, T. F.; Guo, J.; Hone, J.; Kim, P., Atomically Thin P–N Junctions with Van

Der Waals Heterointerfaces. *Nat. Nanotechnol.* **2014,** *9*, 676-681.

(19) Zhou, X.; Hu, X.; Zhou, S.; Song, H.; Zhang, Q.; Pi, L.; Li, L.; Li, H.; Lu, J.; Zhai, T., Tunneling Diode Based on WSe_2/SnS_2 Heterostructure Incorporating High Detectivity and Responsivity. *Adv. Mater.* **2018,** *30*, 1703286.

(20) Shim, J.; Oh, S.; Kang, D. H.; Jo, S. H.; Ali, M. H.; Choi, W. Y.; Heo, K.; Jeon, J.; Lee, S.; Kim, M.; Song, Y. J.; Park, J. H., Phosphorene/Rhenium Disulfide Heterojunction-Based Negative Differential Resistance Device for Multi-Valued Logic. *Nat. Commun.* **2016,** *7*, 13413.

(21) Sangwan, V. K.; Hersam, M. C., Electronic Transport in Two-Dimensional Materials. *Annu. Rev. Phys. Chem.* **2018,** *69*, 299-325.

(22) Jariwala, D.; Sangwan, V. K.; Wu, C. C.; Prabhumirashi, P. L.; Geier, M. L.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C., Gate-Tunable Carbon Nanotube-MoS_2 Heterojunction P–N Diode. *Proc. Natl. Acad. Sci. U. S. A.* **2013,** *110*, 18076-18080.

(23) Lee, J.; Duong, N. T.; Bang, S.; Park, C.; Nguyen, D. A.; Jeon, H.; Jang, J.; Oh, H. M.; Jeong, M. S., Modulation of Junction Modes in $SnSe_2/MoTe_2$ Broken-Gap van der Waals Heterostructure for Multifunctional Devices. *Nano Lett.* **2020,** *20*, 2370-2377.

(24) Angelov, G. V.; Nikolov, D. N.; Hristov, M. H., Technology and Modeling of Nonclassical Transistor Devices. *Journal of Electrical and Computer Engineering* **2019,** *2019*, 1-18.

(25) Yeh, C. H.; Liang, Z. Y.; Lin, Y. C.; Chen, H. C.; Fan, T.; Ma, C. H.; Chu, Y. H.; Suenaga, K.; Chiu, P. W., Graphene-Transition Metal Dichalcogenide Heterojunctions for Scalable and Low-Power Complementary Integrated Circuits. *ACS Nano* **2020,** *14*, 985-992.

(26) Yu, W. J.; Li, Z.; Zhou, H.; Chen, Y.; Wang, Y.; Huang, Y.; Duan, X., Vertically Stacked Multi-Heterostructures of Layered Materials for Logic Transistors and Complementary Inverters. *Nat. Mater.* **2013,** *12*, 246-252.

(27) Guo, J.; Wang, L.; Yu, Y.; Wang, P.; Huang, Y.; Duan, X., $SnSe/MoS_2$ Van Der Waals Heterostructure Junction Field-Effect Transistors with Nearly Ideal Subthreshold Slope. *Adv. Mater.* **2019,** *31*, 1902962.

(28) Liu, W.; Li, L.; Guo, H.; Qadir, A.; Bodepudi, S. C.; Shehzad, K.; Chen, W.; Xie, Y. H.; Wang, X.; Yu, B.; Xu, Y., Approaching the Collection Limit in Hot Electron Transistors with Ambipolar Hot Carrier Transport. *ACS Nano* **2019,** *13*, 14191-14197.

(29) Yuan, S.; Yang, Z.; Xie, C.; Yan, F.; Dai, J.; Lau, S. P.; Chan, H. L.; Hao, J., Ferroelectric-Driven Performance Enhancement of Graphene Field-Effect Transistors Based on Vertical Tunneling Heterostructures. *Adv. Mater.* **2016,** *28*, 10048-10054.

(30) Oh, G.; Kim, J. S.; Jeon, J. H.; Won, E.; Son, J. W.; Lee, D. H.; Kim, C. K.; Jang, J.; Lee, T.; Park, B. H., Graphene/Pentacene Barristor with Ion-Gel Gate Dielectric: Flexible Ambipolar Transistor with High Mobility and On/Off Ratio. *ACS Nano* **2015,** 9, 7515-7522.

(31) Wong, H. S.; Salahuddin, S., Memory Leads the Way to Better Computing. *Nat. Nanotechnol.*

2015, *10*, 191-194.

(32) Lankhorst, M. H.; Ketelaars, B. W.; Wolters, R. A., Low-Cost and Nanoscale Non-Volatile Memory Concept for Future Silicon Chips. *Nat. Mater.* **2005,** *4*, 347-352.

(33) Lee, J.; Pak, S.; Lee, Y. W.; Cho, Y.; Hong, J.; Giraud, P.; Shin, H. S.; Morris, S. M.; Sohn, J. I.; Cha, S.; Kim, J. M., Monolayer Optical Memory Cells Based on Artificial Trap-Mediated Charge Storage and Release. *Nat. Commun.* **2017,** *8*, 14734.

(34) Wang, Q.; Wen, Y.; Cai, K.; Cheng, R.; Yin, L.; Zhang, Y.; Li, J.; Wang, Z.; Wang, F.; Wang, F.; Shifa, T. A.; Jiang, C.; Yang, H.; He, J., Nonvolatile Infrared Memory in MoS_2/Pbs van der Waals Heterostructures. *Sci. Adv.* **2018,** *4*, eaap7916.

(35) Choi, M. S.; Lee, G. H.; Yu, Y. J.; Lee, D. Y.; Lee, S. H.; Kim, P.; Hone, J.; Yoo, W. J., Controlled Charge Trapping by Molybdenum Disulphide and Graphene in Ultrathin Heterostructured Memory Devices. *Nat. Commun.* **2013,** *4*, 1624.

(36) Li, D.; Wang, X.; Zhang, Q.; Zou, L.; Xu, X.; Zhang, Z., Nonvolatile Floating-Gate Memories Based on Stacked Black Phosphorus-Boron Nitride-MoS_2 Heterostructures. *Adv. Funct. Mater.* **2015,** *25*, 7360-7365.

(37) Lee, D.; Choi, Y.; Hwang, E.; Kang, M. S.; Lee, S.; Cho, J. H., Black Phosphorus Nonvolatile Transistor Memory. *Nanoscale* **2016,** *8*, 9107-9112.

(38) Zhou, F.; Zhou, Z.; Chen, J.; Choy, T. H.; Wang, J.; Zhang, N.; Lin, Z.; Yu, S.; Kang, J.; Wong, H. P.; Chai, Y., Optoelectronic Resistive Random Access Memory for Neuromorphic Vision Sensors. *Nat. Nanotechnol.* **2019,** *14*, 776-782.

(39) Huh, W.; Jang, S.; Lee, J. Y.; Lee, D.; Lee, D.; Lee, J. M.; Park, H. G.; Kim, J. C.; Jeong, H. Y.; Wang, G.; Lee, C. H., Synaptic Barristor Based on Phase-Engineered 2D Heterostructures. *Adv. Mater.* **2018,** *30*, 1801447.

(40) Cai, S.; Xu, X.; Yang, W.; Chen, J.; Fang, X., Materials and Designs for Wearable Photodetectors. *Adv. Mater.* **2019,** *31*, 1808138.

(41) Xie, C.; Yan, F., Flexible Photodetectors Based on Novel Functional Materials. *Small* **2017,** *13*.

(42) Xia, F.; Wang, H.; Xiao, D.; Dubey, M.; Ramasubramaniam, A., Two-Dimensional Material Nanophotonics. *Nat. Photon.* **2014,** *8*, 899-907.

(43) Choi, W.; Akhtar, I.; Kang, D.; Lee, Y. J.; Jung, J.; Kim, Y. H.; Lee, C. H.; Hwang, D. J.; Seo, Y., Optoelectronics of Multijunction Heterostructures of Transition Metal Dichalcogenides. *Nano Lett.* **2020,** *20*, 1934-1943.

(44) Long, M.; Liu, E.; Wang, P.; Gao, A.; Xia, H.; Luo, W.; Wang, B.; Zeng, J.; Fu, Y.; Xu, K.; Zhou, W.; Lv, Y.; Yao, S.; Lu, M.; Chen, Y.; Ni, Z.; You, Y.; Zhang, X.; Qin, S.; Shi, Y.; Hu, W.; Xing, D.; Miao, F., Broadband Photovoltaic Detectors Based on an Atomically Thin Heterostructure. *Nano Lett.* **2016**, *16*, 2254-2259.

(45) Kang, D. H.; Pae, S. R.; Shim, J.; Yoo, G.; Jeon, J.; Leem, J. W.; Yu, J. S.; Lee, S.; Shin, B.;

Park, J. H., An Ultrahigh-Performance Photodetector Based on a Perovskite-Transition-Metal-Dichalcogenide Hybrid Structure. *Adv. Mater.* **2016,** *28*, 7799-7806.

(46) Huo, N.; Gupta, S.; Konstantatos, G., MoS_2-HgTe Quantum Dot Hybrid Photodetectors Beyond 2 μm. *Adv. Mater.* **2017,** *29*, 1606576.

(47) Kang, P.; Wang, M. C.; Knapp, P. M.; Nam, S., Crumpled Graphene Photodetector with Enhanced, Strain-Tunable, and Wavelength-Selective Photoresponsivity. *Adv. Mater.* **2016,** *28*, 4639-4645.

(48) Zhang, J.; Wei, Y.; Yao, F.; Li, D.; Ma, H.; Lei, P.; Fang, H.; Xiao, X.; Lu, Z.; Yang, J.; Li, J.; Jiao, L.; Hu, W.; Liu, K.; Liu, K.; Liu, P.; Li, Q.; Lu, W.; Fan, S.; Jiang, K., SWCNT-MoS_2-SWCNT Vertical Point Heterostructures. *Adv. Mater.* **2017,** *29*.

(49) Huo, N.; Konstantatos, G., Recent Progress and Future Prospects of 2D-Based Photodetectors. *Adv. Mater.* **2018,** *30*, e1801164.

(50) Choi, S.; Han, S. I.; Jung, D.; Hwang, H. J.; Lim, C.; Bae, S.; Park, O. K.; Tschabrunn, C. M.; Lee, M.; Bae, S. Y.; Yu, J. W.; Ryu, J. H.; Lee, S. W.; Park, K.; Kang, P. M.; Lee, W. B.; Nezafat, R.; Hyeon, T.; Kim, D. H., Highly Conductive, Stretchable and Biocompatible Ag-Au Core-Sheath Nanowire Composite for Wearable and Implantable Bioelectronics. *Nat. Nanotechnol.* **2018,** *13*, 1048-1056.

(51) Song, Y. M.; Xie, Y.; Malyarchuk, V.; Xiao, J.; Jung, I.; Choi, K. J.; Liu, Z.; Park, H.; Lu, C.; Kim, R. H.; Li, R.; Crozier, K. B.; Huang, Y.; Rogers, J. A., Digital Cameras with Designs Inspired by the Arthropod Eye. *Nature* **2013,** *497*, 95-99.

(52) Liu, Y.; Norton, J. J.; Qazi, R.; Zou, Z.; Ammann, K. R.; Liu, H.; Yan, L.; Tran, P. L.; Jang, K. I.; Lee, J. W.; Zhang, D.; Kilian, K. A.; Jung, S. H.; Bretl, T.; Xiao, J.; Slepian, M. J.; Huang, Y.; Jeong, J. W.; Rogers, J. A., Epidermal Mechano-Acoustic Sensing Electronics for Cardiovascular Diagnostics and Human-Machine Interfaces. *Sci. Adv.* **2016,** *2*, e1601185.

(53) Zhu, Z.; Li, R.; Pan, T., Imperceptible Epidermal-Iontronic Interface for Wearable Sensing. *Adv. Mater.* **2018,** *30*, 1705122.

(54) Ko, H.; Takei, K.; Kapadia, R.; Chuang, S.; Fang, H.; Leu, P. W.; Ganapathi, K.; Plis, E.; Kim, H. S.; Chen, S. Y.; Madsen, M.; Ford, A. C.; Chueh, Y. L.; Krishna, S.; Salahuddin, S.; Javey, A., Ultrathin Compound Semiconductor on Insulator Layers for High-Performance Nanoscale Transistors. *Nature* **2010,** *468*, 286-289.

(55) Hsia, K. J.; Huang, Y.; Menard, E.; Park, J. U.; Zhou, W.; Rogers, J.; Fulton, J. M., Collapse of Stamps for Soft Lithography Due to Interfacial Adhesion. *Appl. Phys. Lett.* **2005,** *86*, 154106.

(56) Meitl, M. A.; Zhu, Z.-T.; Kumar, V.; Lee, K. J.; Feng, X.; Huang, Y. Y.; Adesida, I.; Nuzzo, R. G.; Rogers, J. A., Transfer Printing by Kinetic Control of Adhesion to an Elastomeric Stamp. *Nat. Mater.* **2005,** *5*, 33-38.

(57) Seo, J.; Lee, H.; Lee, S.; Lee, T. I.; Myoung, J. M.; Lee, T., Direct Gravure Printing of Silicon

Nanowires Using Entropic Attraction Forces. *Small* **2012,** *8*, 1614-1621.

(58) Lee, S. K.; Jang, H.; Hasan, M.; Koo, J. B.; Ahn, J. H., Mechanically Flexible Thin Film Transistors and Logic Gates on Plastic Substrates by Use of Single-Crystal Silicon Wires from Bulk Wafers. *Appl. Phys. Lett.* **2010,** *96*, 173501.

(59) Kim, S.; Wu, J. A.; Carlson, A.; Jin, S. H.; Kovalsky, A.; Glass, P.; Liu, Z. J.; Ahmed, N.; Elgan, S. L.; Chen, W. Q.; Ferreira, P. M.; Sitti, M.; Huang, Y. G.; Rogers, J. A., Microstructured Elastomeric Surfaces with Reversible Adhesion and Examples of Their Use in Deterministic Assembly by Transfer Printing. *Proc. Natl. Acad. Sci. U. S. A.* **2010,** *107*, 17095-17100.

(60) Lee, H.; Um, D. S.; Lee, Y.; Lim, S.; Kim, H. J.; Ko, H., Octopus-Inspired Smart Adhesive Pads for Transfer Printing of Semiconducting Nanomembranes. *Adv. Mater.* **2016,** *28*, 7457-7465.

(61) He, Y.; Li, D.; Li, T.; Lin, X.; Zhang, J.; Wei, Y.; Liu, P.; Zhang, L.; Wang, J.; Li, Q.; Fan, S.; Jiang, K., Metal-Film-Assisted Ultra-Clean Transfer of Single-Walled Carbon Nanotubes. *Nano Res.* **2014,** *7*, 981-989.

(62) Thanh, Q. N.; Jeong, H.; Kim, J.; Kevek, J. W.; Ahn, Y. H.; Lee, S.; Minot, E. D.; Park, J. Y., Transfer-Printing of as-Fabricated Carbon Nanotube Devices onto Various Substrates. *Adv. Mater.* **2012,** *24*, 4499-4504.

(63) Li, H.; Wu, J. M. T.; Huang, X.; Yin, Z. Y.; Liu, J. Q.; Zhang, H., A Universal, Rapid Method for Clean Transfer of Nanostructures onto Various Substrates. *ACS Nano* **2014,** *8*, 6563-6570.

(64) Manzeli, S.; Ovchinnikov, D.; Pasquier, D.; Yazyev, O. V.; Kis, A., 2D Transition Metal Dichalcogenides. *Nat. Rev. Mater.* **2017,** *2*, 17033.

(65) Chuang, S.; Kapadia, R.; Fang, H.; Chia Chang, T.; Yen, W.-C.; Chueh, Y.-L.; Javey, A., Near-Ideal Electrical Properties of InAs/WSe_2 van der Waals Heterojunction Diodes. *Appl. Phys. Lett.* **2013,** *102*, 242101.

(66) Wang, T.; Wang, H.; Kou, Z.; Liang, W.; Luo, X.; Verpoort, F.; Zeng, Y. J.; Zhang, H., Xenes as an Emerging 2D Monoelemental Family: Fundamental Electrochemistry and Energy Applications. *Adv. Funct. Mater.* **2020,** *30*, 2002885.

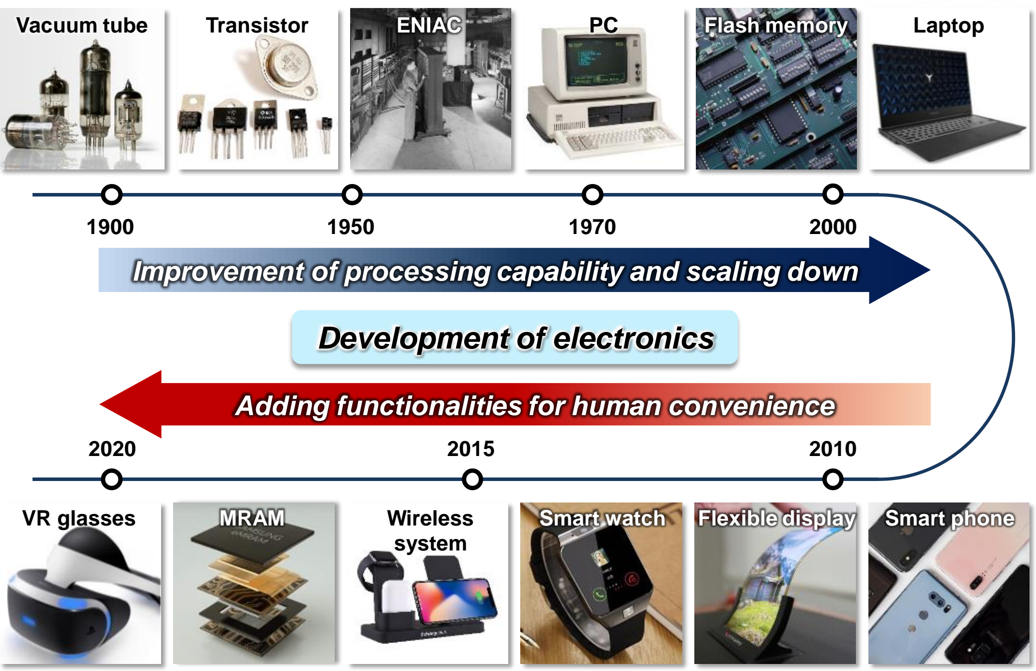

Figure 1.1. Development of electronic devices over the course of time.

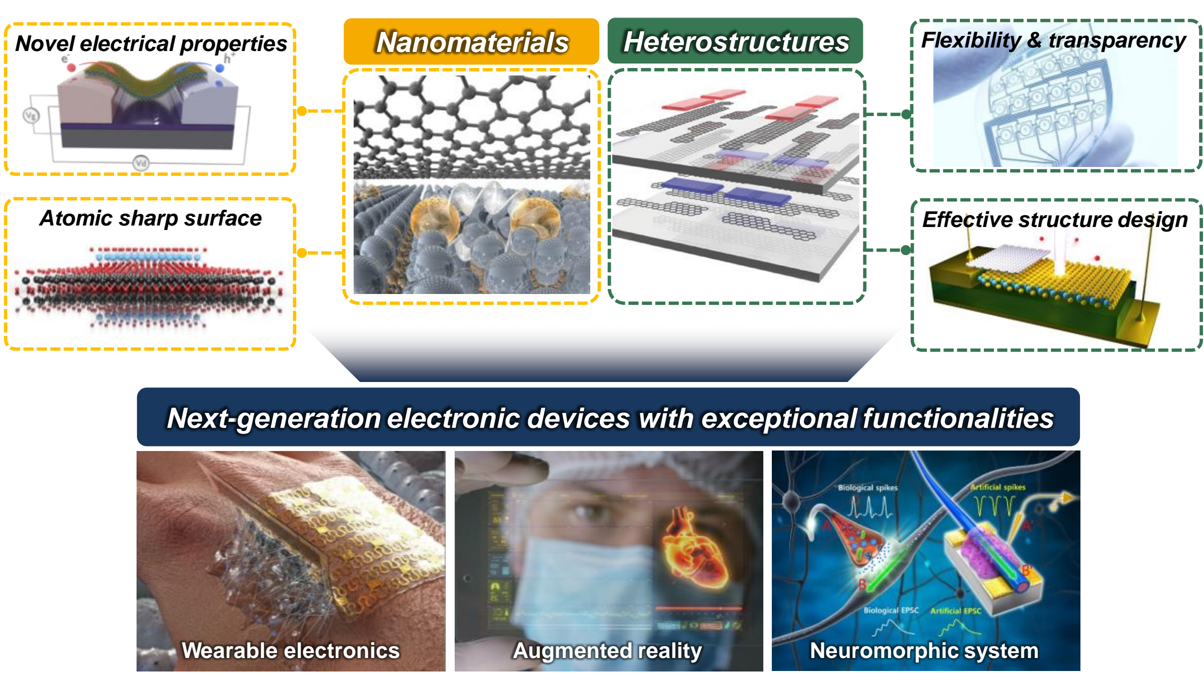

Figure 1.2. Necessity of nanomaterials and heterostructures for next-generation electronic devices.

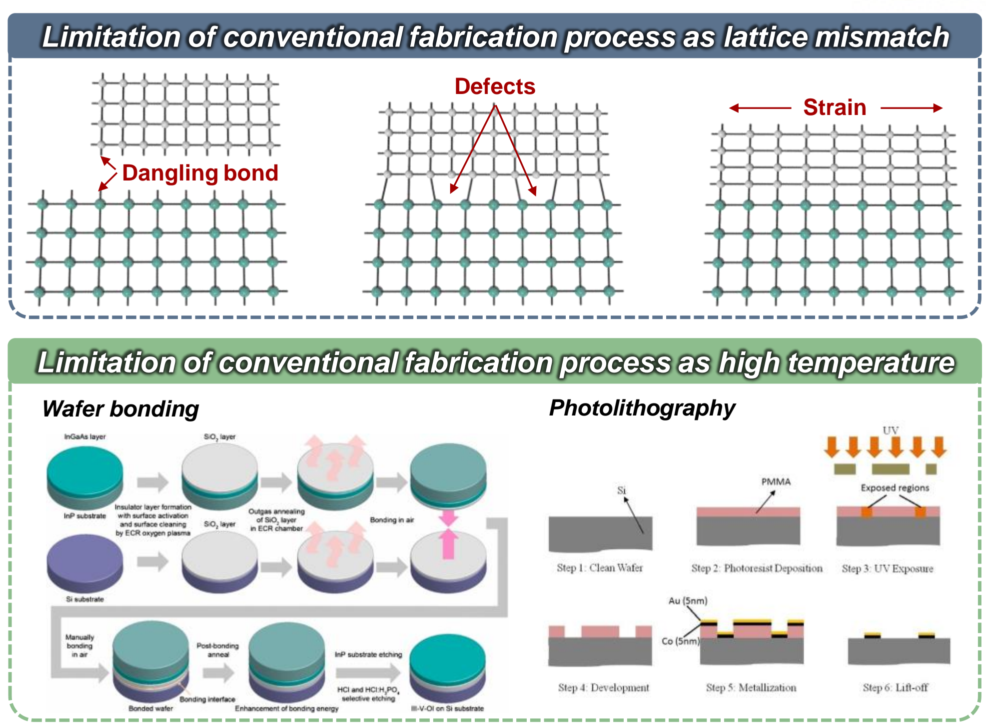

Figure 1.3. Limitations of convention fabrication technology for formation of heterostructure.

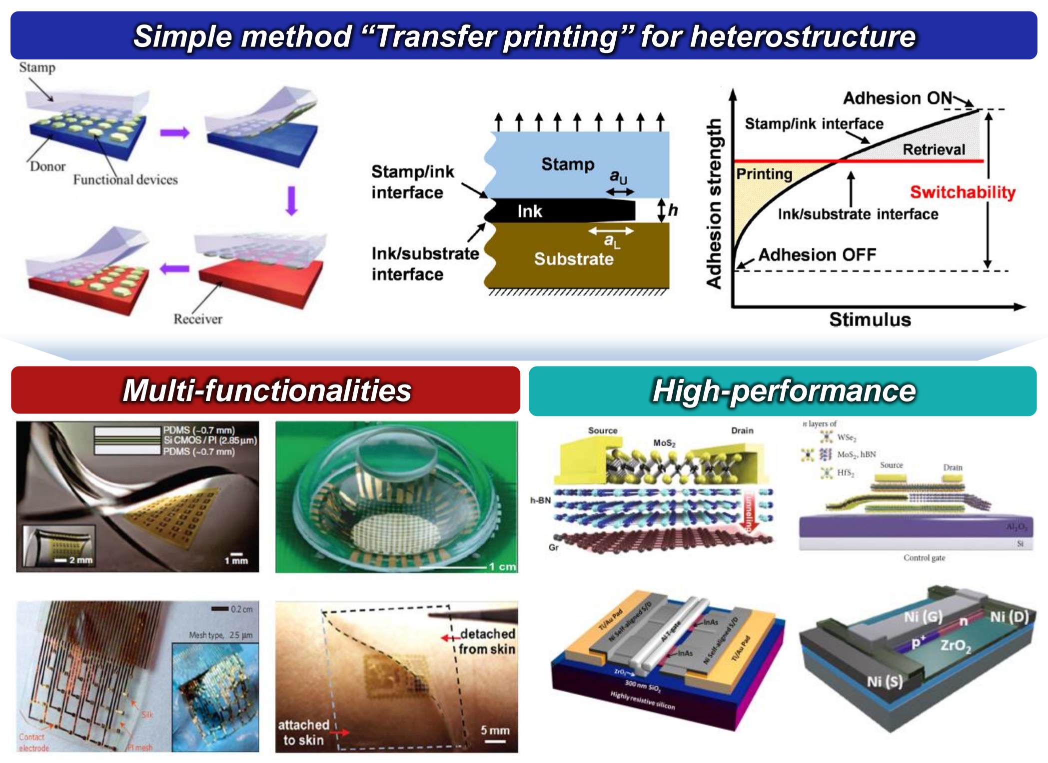

Figure 1.4. Transfer printing technique for multi-functional and high-performance applications.

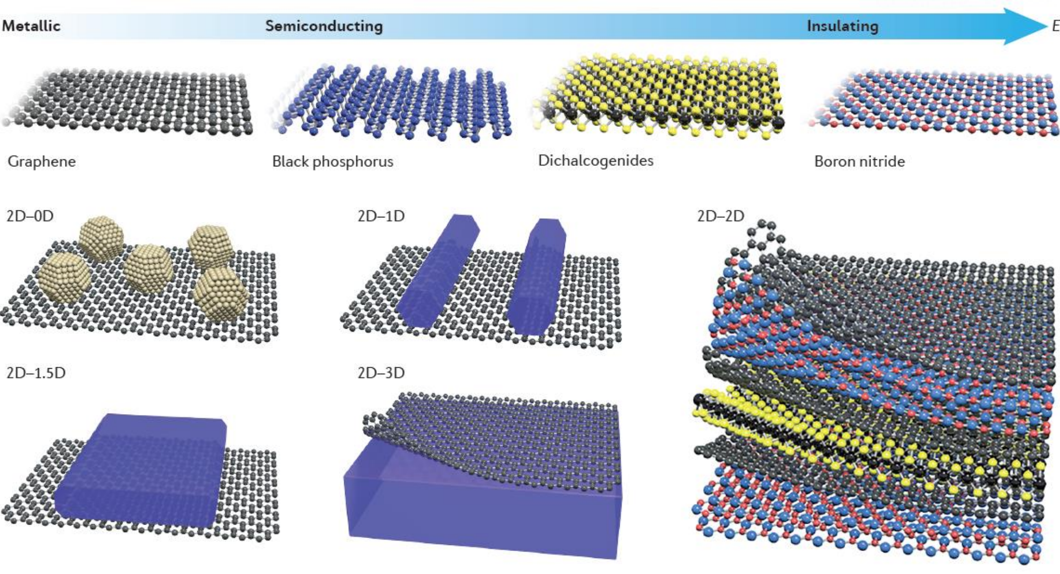

Figure 1.5. Various heterostructure devices based on nanomaterials.

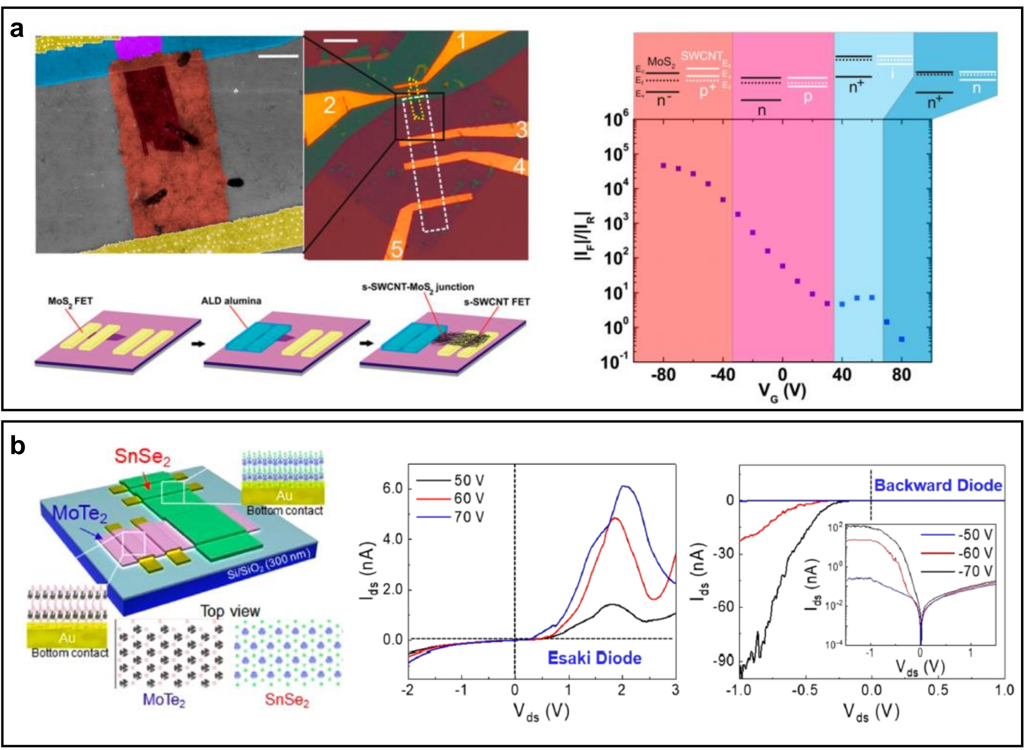

Figure 1.6. Functional heterojunction diodes. (a) Gate tunable SWNT/MoS_2 heterojunction diode. (b) $SnSe_2$/$MoTe_2$ heterojunction diode for modulation of junction modes.

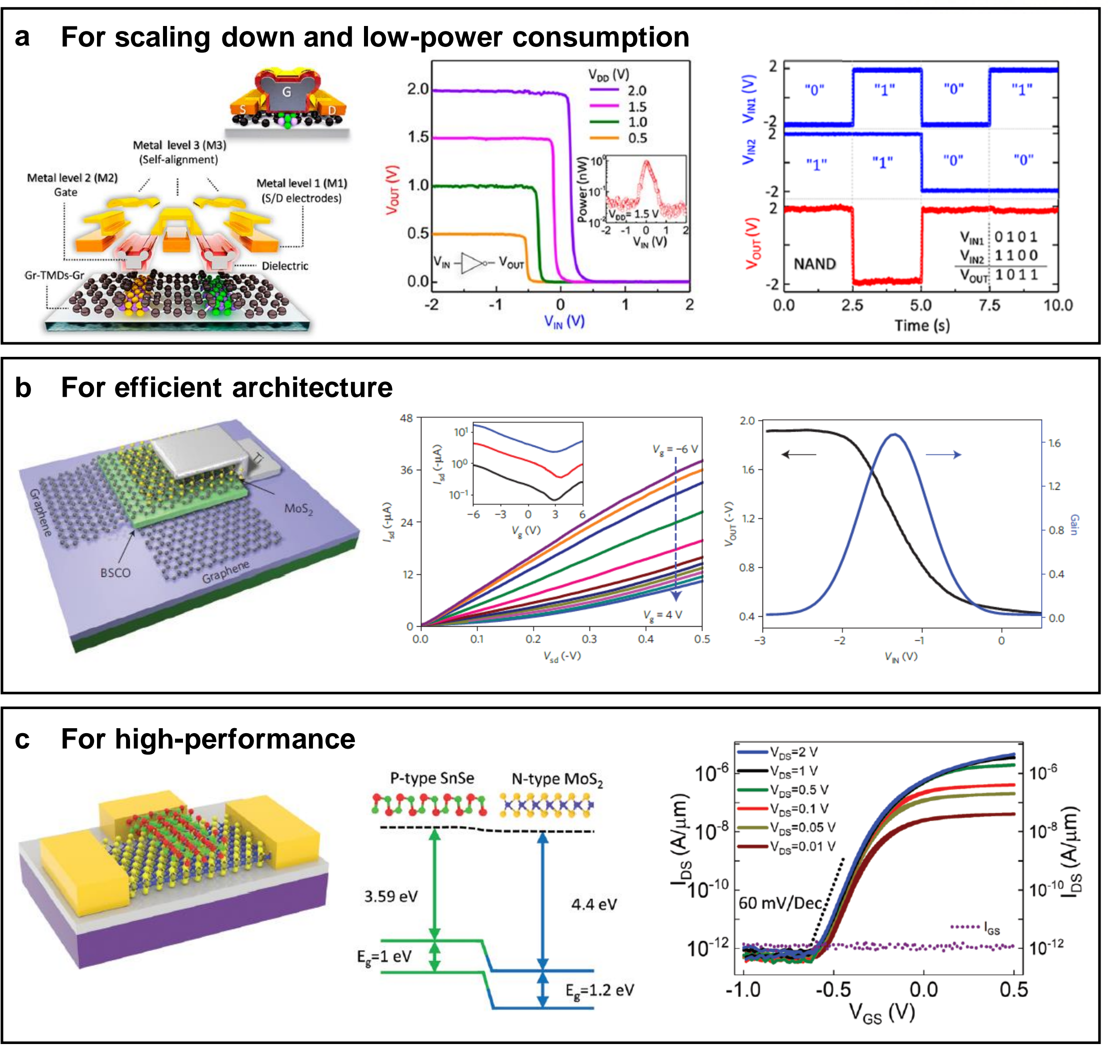

Figure 1.7. Multi-functional transistors based on heterostructure of nanomaterials for (a) scaling down and low-power consumption, (b) efficient architecture, (c) high-performance.

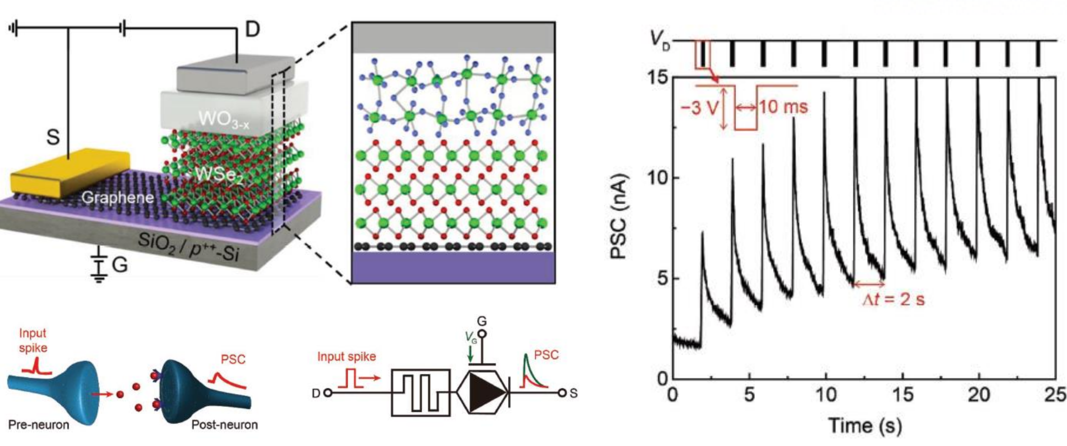

Figure 1.8. Memory device based on heterostructure with nanomaterials for neuromorphic applications.

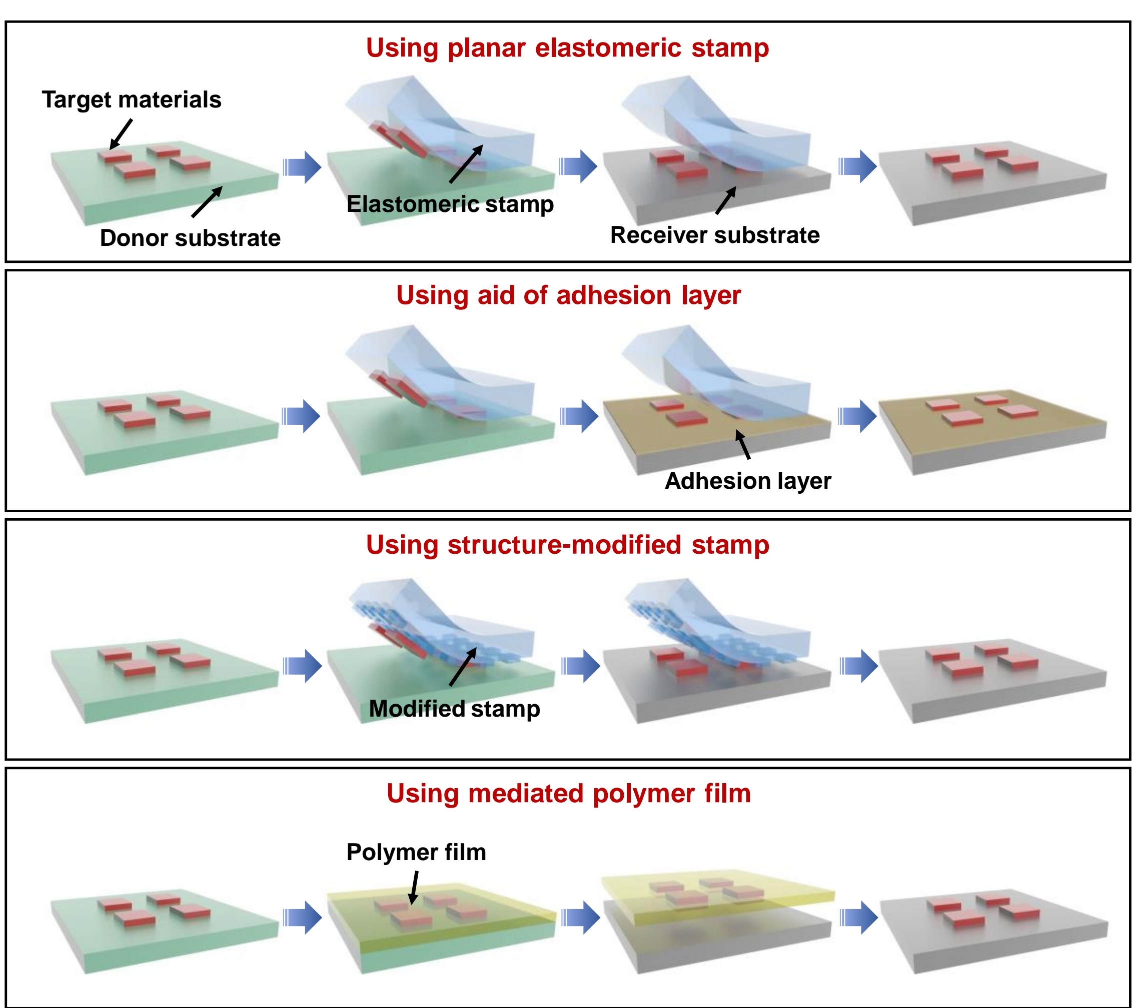

Figure1.9. Schematic illustrations of four different strategies of transfer printing technique for efficient transfer.

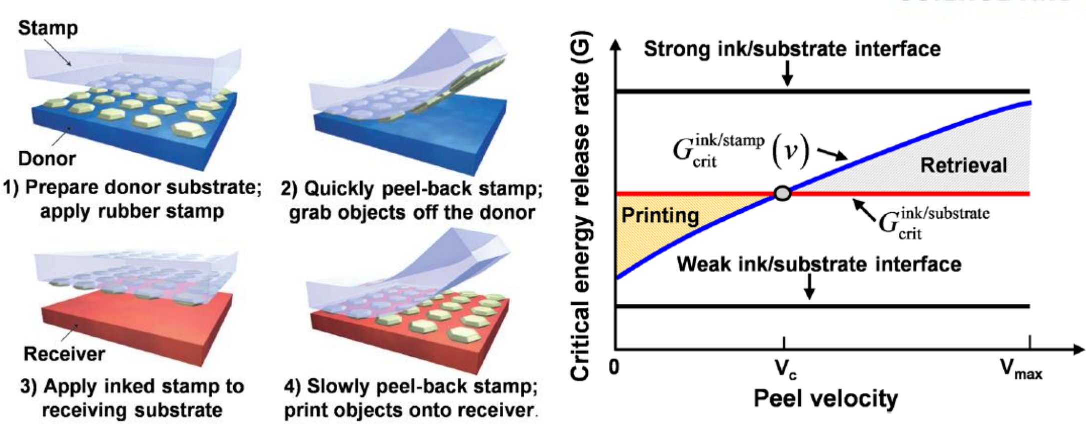

Figure 1.10. Kinetically controlled transfer printing process.

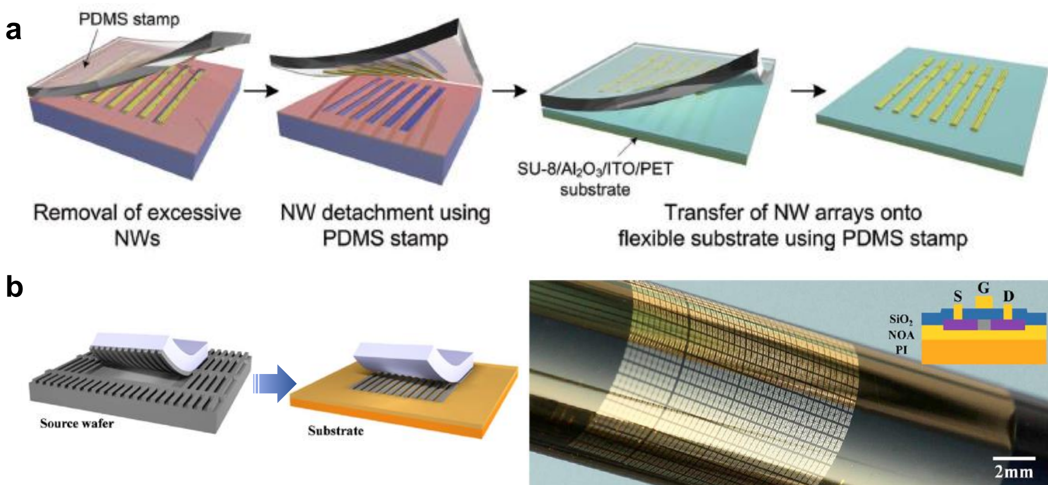

Figure 1.11. Transfer printing methods by using adhesive layer, (a) SU-8 and (b) NOA.

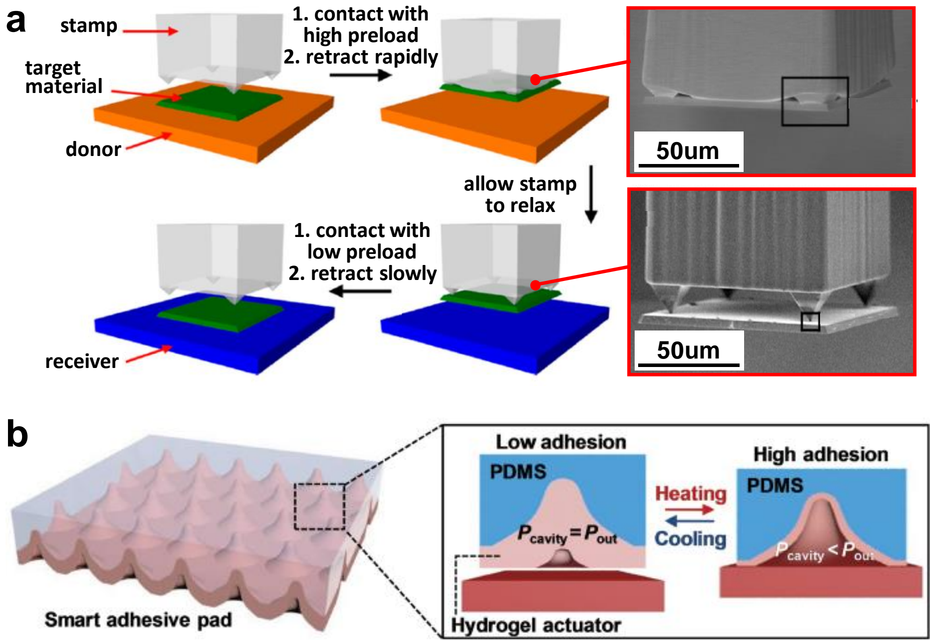

Figure 1.12. Transfer printing with supports of structure-modified elastomeric stamp. (a) The adhesion of stamp controlled by microtip structure with change of contact area. (b) Bio-inspired smart adhesive pad with microcavity structure inducing controllable cavity pressure.

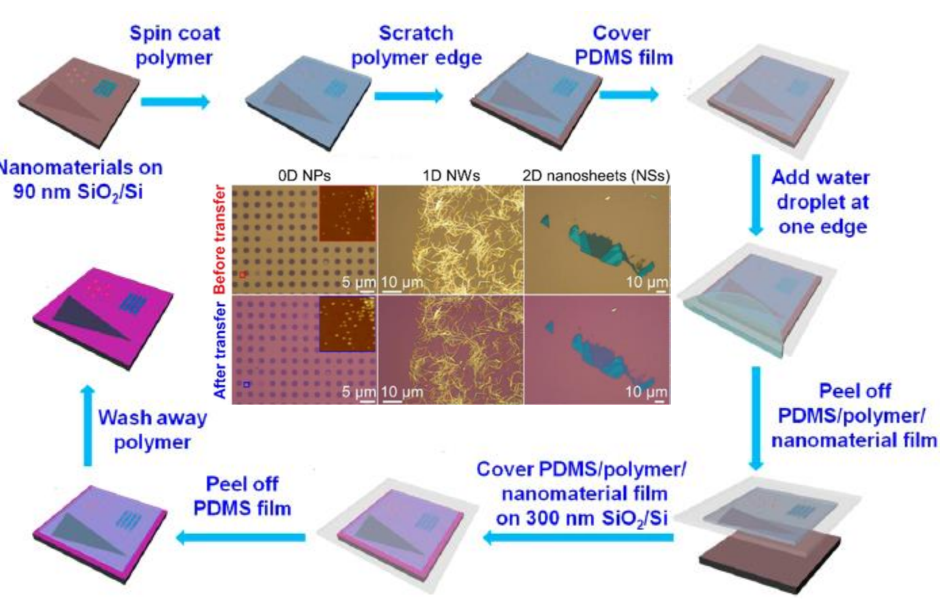

Figure 1.13. Transfer printing method with mediated polymer thin film.

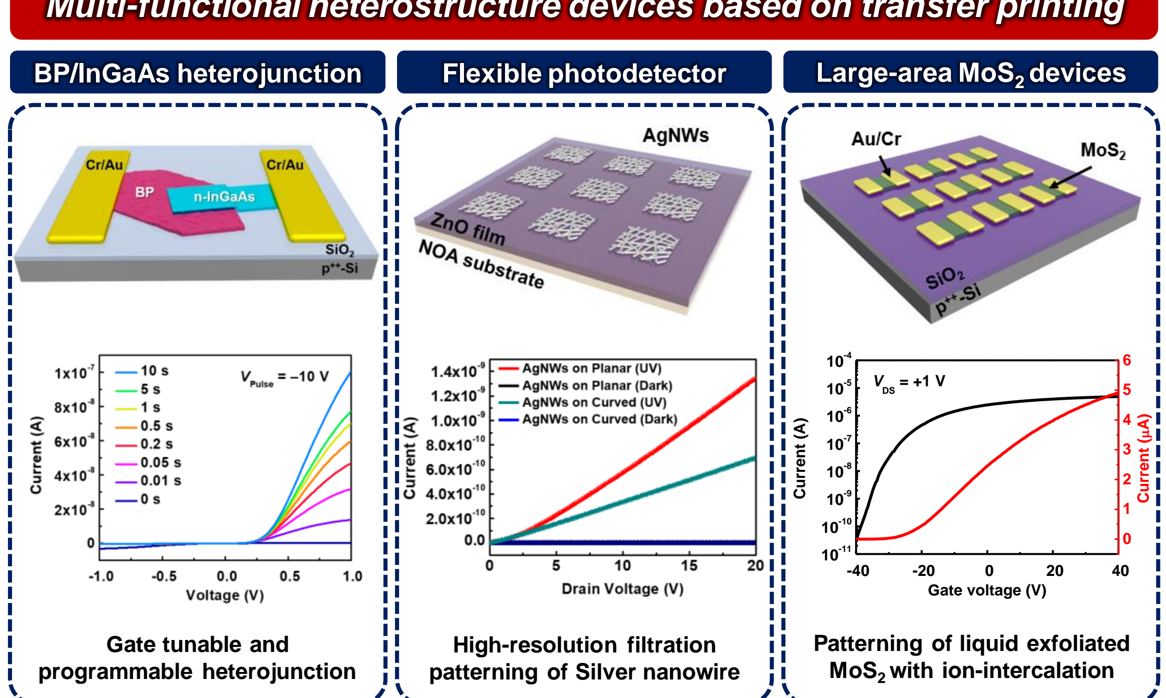

Figure 1.14. Contents of this thesis.

Chapter 2. Gate-Tunable and Programmable n-InGaAs/Black Phosphorus Heterojunction Diodes

2.1 Introduction

Heterostructure devices based on III-V compound semiconductors have attracted great attention because of the high mobility and low effective mass of the carriers, the direct band gap, and the tunability of the band gap by modulating components, which combine to enable many applications such as high-electron-mobility transistors (HEMTs),[1, 2] quantum-well laser diodes,[3, 4] light-emitting diodes (LEDs),[5, 6] and photodetectors.[7-9] However, traditional fabrication of III–V semiconductor heterostructures present significant technological challenges because of the lattice-constant mismatch with other substrates and the generation of defects during the processes of direct growth and wafer bonding.[10-12] To address these challenges, an epitaxial layer transfer technique was introduced to heterogeneously integrate III-V semiconductor nanomembranes onto arbitrary substrates,[13] whereby the bonding at heterointerfaces with a large lattice mismatch is facilitated by van der Waals forces during the transfer printing processes. This technique has enabled the fabrication of various III–V heterostructure devices on Si and flexible substrates, including complimentary metal-oxide-semiconductor field-effect transistors (MOSFETs) based on InGaSb and InAs on Si substrates,[14] flexible MOSFETs with InAs on polyimide substrates,[15] spin-FETs with InAs HEMT structures on Si substrates,[16] and broadband photodetectors based on InGaAs and Si heterojunctions.[17] However, III–V heterostructures still have limitation in securing multi-functionality in a unit device because of the lack of III-V materials with diverse electronic properties. Programmable multifunction in a single device is advantageous in scalability and avoids complicated fabrication process for multi-functional applications.

As opposed to III–V semiconductors, the atomically sharp interface of two-dimensional (2D) layered materials can liberate the choice of materials for fabricating heterostructures without the restriction of lattice mismatch, which allows fabricating heterostructure devices with unique physical properties.[18-22] Various heterostructure combinations between 2D and other dimensionalities with new functionalities have recently been introduced, for example, gate-tunable p–n diodes,[23-26] tunneling transistors,[27] photoresponsive memory devices,[28, 29] and broadband photovoltaic devices.[30] Among the possible 2D materials for heterostructure devices, black phosphorus (BP) has attracted significant interest because of its high mobility, tunablility and direct band gap (0.3–1.5 eV). More interestingly, the Fermi level of BP could be tuned by the gate voltage,[31-33] which plays an important role for the gate-tunable multi-functionalities and enhancement of performance in the heterostructure through the control of energy band offset.[34] Thus, the heterostructure based on BP can expand the device functionalities and enhance the performances in multi-functional device applications, which can function as a diode and transistor,[35]

a photodiode and phototransistor,[36] and a diode, transistor and logic system.[34] Furthermore, the oxide layer (PO_x) that forms naturally on BP provides charge-trapping and -releasing sites as a function of the gate pulse, which allows the development of memory devices without additional structures, such as floating gates or ferroelectric layers.[37, 38] Combining these unique electronic and physical features of BP with the III-V semiconductor may allow us to fabricate heterostructure devices with clean heterointerfaces, no lattice mismatch, and multiple electronic functionalities.[19, 20, 39]

This study demonstrates programmable, gate-tunable, and photoresponsive heterojunction diodes based on heterostructures comprising few-layer BP and an n-InGaAs nanomembrane. The heterojunction diode with clean hetero-interface was fabricated by the epitaxial layer transfer printing of n-InGaAs nanomembrane on the mechanically exfoliated BP layer. These heterojunction diodes clearly exhibit gate-controlled rectification and switching with the maximum rectification ratio of 4600, mobility value of 84.6 $cm^2 V^{-1} s^{-1}$, and on/off ratio exceeding 10^5 for diode and transistor devices because of the electrostatic inversion of the BP. In addition, the device offers nonvolatile-memory properties through charge trapping in the native phosphorus oxide, enabling the fabrication of gate-controllable and programmable diodes. By combining gate-tunable rectification with the nonvolatile-memory property, the rectification ratio of the device can be controlled and memorized from 0.06 to 400 by applying a gate pulse. Furthermore, the photoresponsive properties of heterostructure diodes (photoresponsivity value of 0.704 A/W) enable the generation of various electrical signals in response to specific stimuli, which can find applications in multiple logic operators. These multi-functional properties of the proposed heterostructure architecture offer potential applications in novel advanced logic circuits, controllable electric transformers and neuromorphic applications.

2.2 Experimental details

***Growth of III–V compound semiconductor film*:** InAs/n-InGaAs/InAlAs stacked layers were grown on a InP (001) substrate using a molecular beam epitaxy (Riber Compact 21T, France). Here, a 200-nm-thick $In_{0.52}Al_{0.48}As$ layer was used as a buffer layer to lattice match to the InGaAs layer. The n-$In_{0.53}Ga_{0.47}As$ layer was doped with Si at a concentration of 1.5×10^{18} cm^3 at 440 °C. A 2-nm-thick InAs layer was grown on the InGaAs layer to prevent the surface oxidation of the n-InGaAs layer at atmospheric pressure.

***Fabrication of n-InGaAs–BP heterojunction diode*:** BP nanosheets were mechanically exfoliated from the bulk BP crystal (99.998%, smart elements) using a scotch tape. The exfoliated BP nanosheets were transferred onto the elastomeric PDMS (10:1) using a stamping method. Next, the exfoliated BP nanosheets were transfer-printed onto the SiO_2 (100 nm)/p^{++}-Si substrate. Before epitaxial transfer printing, the n-InGaAs layer on the growth substrate was patterned using a standard photolithography technique (MA-6, SUSS MicroTec, Germany) with AZ 5214E photoresist and etched by dilute citric

acid (citric acid monohydrate:H_2O:H_2O_2 = 1:1:2) into micropattern arrays (10 × 200 μm^2). After the removal of photoresist by acetone, the patterned n-InGaAs side of the III-V multi-stacked layer was attached onto the PDMS stamp. The InAlAs/InP layer was etched by dilute HCl solution (37% HCl; HCl:H_2O = 2.3:1 volume ratio) with small amounts of sodium dodecyl sulfate to prevent bubble trapping during etching. Next, the remaining n-InGaAs layer on the PDMS stamp was transfer-printed at room temperature. Finally, Cr/Au (3/100 nm) electrode contacts were formed via e-beam lithography (nB3, NanoBeam Ltd., UK) and thermal evaporation. All samples were sequentially cleaned using deionized water, acetone, and 2-propanol to remove the residue and then stored in nitrogen after rapid thermal annealing (MILA-5000, ULVAC, US) at 200 °C.

***Characterization*:** The images of n-InGaAs and BP heterojunction diodes were obtained by an optical microscopy (BX-53, Olympus, Japan). The thickness of n-InGaAs and BP layers was measured using the AFM (DI-3100, Vecco, US). The crystalline quality of transferred nanomembranes was verified via a confocal Raman microscopy (Alpha300R, WITec, Germany) with a 532 nm excitation laser (laser power: 1 mW) at an integration time of 1 s with 5 times accumulations. The contact the interface of heterostructure was investigated using a HR TEM (JEM-3000F, JEOL, Germany) at an acceleration bias of 80 kV. The difference in contact potential was analyzed using a multimode AFM (Multimode V, Veeco, US) system with Pt/Ir-coated silicon tips (tip radius 25 nm; force constant 3 N/m; resonance frequency 75 kHz).

***Electrical and optical measurements*:** The basic electrical properties of the heterojunction diode were investigated using a semiconductor characterization system (4200-SCS, Keithley, US) and a vacuum probe station (M6VC, MS Tech, Korea) at room temperature in a vacuum chamber of ~10^{-3} Torr. The applied voltages with ac and PC waveforms were generated using a function generator (AFG3011C, Tektronix, US). The rectified output voltages were analyzed using an oscilloscope (DPO 2022B, Tektronix, US). Various LEDs (Skycares, Korea) were used to measure the photocurrent of the device while being illuminated at different wavelengths. The intensity of the illumination at the various wavelengths was verified using a calibrated optical power meter (1916-R, Newport, US), incorporating a Si photodetector (818-UV, Newport, US) and a Ge photodetector (818-IR, Newport, US).

2.3 Results and discussion

Figure 2.1 illustrates the fabrication process for n-InGaAs–BP heterojunction diodes. First, a BP nanosheet was mechanically exfoliated from a synthetic bulk BP crystal using the scotch-tape method. Next, the exfoliated BP nanosheet was transferred onto a SiO_2 (100 nm)/p^{++}-Si substrate via polydimethylsiloxane (PDMS) stamping, which efficiently transfers the BP nanosheet without introducing significant contamination onto the transferred BP.[40] To efficiently transfer a n-InGaAs nanomembrane and form a heterojunction with the BP nanosheet, we used an epitaxial transfer printing

technique.[17, 41, 42] For the epitaxial transfer printing of a n-InGaAs nanomembrane, a single-crystalline n-InGaAs thin film (15 nm) was grown epitaxially on an InAlAs buffer layer on an InP (001) growth substrate. Next, the n-InGaAs film on the growth substrate was patterned using standard photolithography, etched by dilute citric acid into micropattern arrays (10 × 200 μm^2), and transferred onto the BP nanosheet via PDMS stamping (Figure 2.1b). Finally, Cr/Au (3/100 nm) electrodes were formed using e-beam lithography and thermal evaporation, resulting in the n-InGaAs–BP heterojunction diode. Figure 2.2a shows a schematic and an optical-microscope image of the fabricated n-InGaAs–BP heterojunction diode. The thicknesses of BP and n-InGaAs nanomembrane are 32 and 15 nm, respectively (Figure 2.2b). Figure 2.3 shows the surface morphology of n-InGaAs and BP by using an atomic force microscopy (AFM) analysis, indicating negligible change of the root-mean-square (RMS) roughness of n-InGaAs and BP during the transfer process. Figure 2.2c shows the Raman spectra of a few-layer BP nanosheet, n-InGaAs nanomembrane, and n-InGaAs–BP heterojunction. The Raman peaks at 361, 438, and 466 cm^{-1} are attributed to the $A^1{}_g$, B_{2g}, and $A^2{}_g$ vibrational modes of BP,[43-45] respectively, and the broad peak at 266 cm^{-1} is the longitudinal optical phonon peak of InGaAs.[10] The Raman spectrum from the n-InGaAs–BP heterojunction contains typical Raman peaks of both the BP nanosheet and of the n-InGaAs nanomembrane, indicating that the mechanical exfoliation and epitaxial transfer printing processes successfully transferred the BP and InGaAs onto the Si wafer without introducing critical defects. The formation of n-InGaAs–BP heterojunction was confirmed by the energy dispersion X-ray spectroscopy (EDS) elemental mappings of phosphorus (P), indium (In), gallium (Ga), and arsenic (As) in the interface (Figures 2.4a and b). Furthermore, the cross-sectional high-resolution transmission electron microscopy (HRTEM) images of the interface between InGaAs/BP and BP/SiO_2, as shown in Figures 2.4c and d, indicate a sharp and tight-bonding interface at the n-InGaAs–BP heterojunction.

The heterojunction diode exhibits strong gate-tunable rectification. Figure 2.5a shows the drain-source current (I_{DS}) as a function of drain–source voltage (V_{DS}) on a semi-logarithmic scale for gate voltages (V_G) of −40, 0, and 40 V for a representative n-InGaAs–BP heterojunction diode. This figure clearly shows that the forward current (I_F) depends strongly on the gate voltage. Figure 2.6 shows in more detail the I_{DS}-V_{DS} curves for several applied gate voltages. These results show that by applying gate voltages between 0 and 40 V, the forward current at V_{DS} = 1 V can be modulated from 31 pA to 8.43 μA with an on/off ratio exceeding 10^5. Conversely, the reverse current (I_R) depends only weakly on the gate voltage and can be modulated only from 23 to 341 pA at V_{DS} = −1 V. Thus, depending on the gate-voltage, the heterojunction diode has poor rectification at V_G = 0 V but has good rectification at V_G = 40 V. For gate voltages from 0 to −40 V, the reverse current at V_{DS} = −1 V increases from 23 to 251 pA and the forward current at V_{DS} = 1 V decreases from 31 to 16 pA, resulting in a reverse rectification behavior at V_G = −40 V. The rectification ratio ($|I_F/I_R|$) can be modulated from ~0.1 to 4600 as the applied gate voltage increases from −40 to 40 V (Figure 2.5b). The ideality factor (η) is a figure

of merit for heterojunction diodes and can be estimated by fitting the Shockley diode equation

$$I = I_0\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right], \quad (1)$$

$$\eta = \frac{q}{kT}\left(\frac{\partial V}{\partial \ln I}\right), \quad (2)$$

where I_0 is the reverse bias saturation current, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. From the semi-logarithmic I_{DS}–V_{DS} curve in Figure 2.5a and Figure 2.6, the ideality factor for the n-InGaAs–BP heterojunction diode is estimated to be ~3.6 at V_G = 0 V, which decreases to ~2.5 at V_G = −40 V and to ~1.6 at V_G = 40 V (Figure 2.7). This gate-tunability of ideality factors indicates that the resistance or barrier height of the heterojunction in the interface can be modulated by adjusting the applied gate voltage. Achieved values for the ideality factor in the n-InGaAs–BP heterojunction diode are higher than that of an ideal diode (η = 1), which is attributed to mainly the trap state and the resistance of the heterojunction in the interface.[32] The ideality factor of ~1.6 at V_G = 40 V for the n-InGaAs–BP heterojunction diode is comparable to the ideality factors of previously reported heterojunction diodes comprising WSe_2–$MoSe_2$ (η = ~1.5),[46] BP–WS_2 (η = ~1.7),[47] and BP–MoS_2 (η = ~2.7).[32]

The gate-tunable rectifying behavior of n-InGaAs–BP heterojunction diodes is caused by the electrostatic inversion of the BP (Figure 2.8c), where the Fermi level of BP is modulated by the gate voltage.[31, 33, 38, 48] This modulation of the Fermi level is attributed to the weak Fermi-level pinning and screening effects of 2D materials.[49, 50] On the other hand, the Fermi level of n-InGaAs is pinned near the conduction band and has negligible change with the gate voltage.[51] This behavior is illustrated in the energy-band diagram shown in Figures 2.9 and 2.10. In this band diagram, the electron affinity and band gap of BP (InGaAs) are estimated to be 4.2 eV (4.5 eV) and 0.4 eV (0.75 eV), respectively, based on previously reported band properties.[52, 53] A small barrier forms at the n-InGaAs–BP heterojunction because of the small difference in work function of the two materials, as can be seen by the band alignment between BP and n-InGaAs shown in Figure 2.9a. Changing the gate voltage from negative to positive gate induces an electrostatic inversion of the BP nanosheets from p-type to n-type, altering the band structure of the heterostructure device from p^+–n to n^-–n junctions and decreasing the barrier height (Figures 2.9b and c), resulting in an increase of the forward current. Thus, the n-InGaAs–BP heterojunction diode exhibits strong rectification under the positive gate voltage and its rectification depends strongly on the applied gate voltage.

The gate tunability of n-InGaAs–BP heterojunction diodes enables both rectifying and switching behaviors when operated as diode and transistor modes, respectively. The mobility μ of the transistor can be calculated using

$$\mu = \frac{\partial I_{DS}}{\partial V_G}\left(\frac{L}{W C_i V_{DS}}\right), \quad (3)$$

where L, W, and C_i denote channel length, channel width, and specific capacitance between the channel and the back gate silicon per unit area.[54] The specific capacitance can be obtained using the parallel-plate capacitor equation $C_i = \varepsilon_0 \varepsilon_r / d$, where ε_0, ε_r, and d are the vacuum dielectric constant (8.85×10^{-12} F/m), dielectric constant of silicon (3.9), and silicon thickness (100 nm), respectively. From the transfer characteristics shown in Figure 2.11a, the mobility of the n-InGaAs–BP heterojunction diode is determined to be ~84.6 cm^2 V^{-1} s^{-1}, which is significantly greater than that of other p–n heterojunction diodes, such as MoS_2–WSe_2 (~14 cm^2 V^{-1} s^{-1}),[54] $ReSe_2$–MoS_2 (~4 cm^2 V^{-1} s^{-1}),[55] and MoS_2–rubrene (~8 cm^2 V^{-1} s^{-1}).[56] The mobilities of individual BP and n-InGaAs FETs are calculated to be ~145.1 and ~9.39 cm^2 V^{-1} s^{-1}, respectively, based on the transfer characteristics shown in Figures 2.8c and f.

For the use of a diode in electrical switch or rectifier applications, dynamic properties of the diode are required. For further investigation of the dynamic gate-tunable rectifying behavior of n-InGaAs–BP heterojunction diodes, we used a function generator (FG) to apply various voltages with alternating current (ac) waveforms. Figure 2.12a shows a schematic of the n-InGaAs–BP heterojunction diode with a corresponding circuit diagram for investigation of the dynamic rectifying behavior. Figure 2.12b shows the dynamic rectification with different amplitudes (0.2, 0.5, 1 V) of sinusoidal input drain-source voltage (V_{Input}) under a positive gate voltage (V_G = 40 V). The sinusoidal input drain-source voltage creates a clear sinusoidal waveform in the rectified current, whose amplitude increases with the amplitude of the input drain–source voltage. Figure 2.13a shows the dynamic rectification with the input voltage amplitude of 0.2 V and for different gate voltages V_G = −40, 0, 40 V. Similar to the results shown in Figure 2.5, the forward current of the device (V_{DS} = 0.2 V) under positive gate voltage (V_G = 40 V) increases significantly compared with the reverse current (V_{DS} = −0.2 V), resulting in a clear rectified output current. For negative gate voltage, the n-InGaAs–BP heterojunction diode also exhibits reverse rectification (Figure 2.13b). Figure 2.14 shows the rectifying behavior of the n-InGaAs–BP heterojunction diode with a 0.1 kHz ac voltage waveform for input drain–source voltage under a positive gate voltage (V_G = 40 V). These results indicate that n-InGaAs–BP heterojunction diodes offer dynamic rectification that can be modulated by the gate voltage, which is useful for applications that require gate-tunable switching devices.

To investigate the dynamic switching behavior of n-InGaAs–BP heterojunction diodes, we applied rectangular pulsating current (PC) voltage to the back gate electrode. Figure 2.12c shows a schematic of the n-InGaAs–BP heterojunction diode with corresponding circuit diagram for investigation of the switching behavior. Figure 2.12d shows the dynamic switching behavior for various amplitudes of the applied gate voltage (V_G = 2, 5, and 10 V) under a bias voltage of V_{DS} = +1. Figure 2.15a displays the dynamic switching behavior for different bias voltages (V_{DS} = 0.2, 0.5, and 1 V) under the positive gate voltage (V_G = 10 V). The device exhibits a clear switching behavior, which is enhanced by increasing the bias voltage and the applied gate voltage. This switching behavior results in a maximum on/off ratio exceeding 10^5 (Figure 2.11a). For comparison, the switching behavior of the device under a negative

bias voltage (V_{DS} = −1 V) was also investigated with various gate voltages (V_G = −2, −5, and −10 V); see Figure 2.15b. The on/off ratio is low, which differs markedly from the case with positive bias voltage (V_{DS} = 1 V). These results are consistent with the results shown in Figure 2.5a, which exhibits strongly gate-dependent current under the forward bias (V_{DS} > 0V) and weakly gate-dependent current under the reverse bias (V_{DS} < 0V).

Figure 2.16a shows a schematic of the n-InGaAs–BP heterojunction diode as a memory device. Here, the charge trapping in the native phosphorus oxide under the applied gate voltage induces memory properties. Figure 2.16b displays the transfer characteristics of the heterojunction diode with a large hysteresis, which is a basic requirement for the memory device application. The potential for use as the memory device was investigated by applying a retention test and studying the memory-switching behavior (see Figures 2.16c and d). The retention characteristics of the device were measured at a forward bias of 1 V under ±10 V gate-voltage pulses (V_{Pulse}) with 100-ms duration (Figure 2.16c). Here, the current level increases (programmed state) upon applying a −10 V gate-voltage pulse, whereas the current level decreases (erased state) upon applying a +10 V gate-voltage pulse. The two distinguishable current levels can be retained for over 1000 s. Figure 2.16d shows the periodic cycles of programmed and erased states of the device. This result demonstrates that the device operates well and has stable switching under the applied gate pulses. We attribute the memory properties in the heterojunction diode to the native phosphorus oxide (PO_x) on the surface of the BP nanosheets. Because of the PO_x, BP FETs exhibit memory properties with large hysteresis in the transfer characteristics and retention test (Figure 2.17). Figure 2.18 explains the operating mechanism of the heterojunction diode to serve as a memory device. When a gate voltage is applied to the device, charges are populated in the BP channel because the Fermi level changes. These charges can be trapped in the native phosphorus oxide.[37] The trapped charges in the oxide layer can induce the accumulation of opposite charges in the channel layer due to the capacitive gating effect,[37, 38] which induces an electric field, similar to the applied gate voltage and results in the modulation of the Fermi level of the BP.

To confirm the charge trapping in the oxide layer, we used a Kelvin probe force microscope (KPFM) to measure the contact potential difference (V_{CPD}) (Figure 2.19). Here, the V_{CPD} between the KPFM tip and the surface of the BP changes significantly (V_{CPD} of 1.06 V) under the programmed and erased states. This large difference in V_{CPD} indicates that opposite charges are trapped in the oxide layer in each state because V_{CPD} is related to the electrostatic interaction between the KPFM tip and the charges on the surface.[57, 58] Under reverse bias, however, the heterojunction diode shows a lower program/erase ratio than in forward bias because the modulation of Fermi level of the BP only weakly affects the current level under reverse bias (Figure 2.20). These results indicate that the proposed heterojunction diode has controllable memory properties that depend on the direction of the drain-source voltage in contrast with a typical memory device which shows the similar program/erase ratio at both forward and reverse biases because the whole channel is affected by the floating gate or by the ferroelectric

structures.[58-60]

The rectification ratio depends on the duration of the voltage pulse applied to the gate. As shown in Figure 2.16e, in the programmed state, increasing the pulse time results in a significant increase in the forward current, which is due to the electrostatic inversion of the BP layer. Here, depending on the pulse duration, the rectification ratio increases from 0.06 to 400 for the pulse duration time from 0 to 10 s. In addition, we show in Figure 2.21 the rectification with gate-voltage pulses of various amplitudes. Here, the n-InGaAs–BP heterojunction diode exhibits clear rectification under the programmed state. Furthermore, the amplitude of rectified current increase as gate-voltage pulse decreases from 0 V to −70 V because the amount of trapping charges could be controlled by gate-voltage pulses. Note that the naturally grown PO_x enables the simple fabrication of a memory device without requiring additional floating gate and ferroelectric structures. Given these memory properties, the proposed device can be used as a programmable diode, which has potential applications in neuromorphic systems[37, 38, 61] and in controllable electric transformers.[62, 63]

The proposed heterojunction diode is also photoresponsive due to its p-n heterojunction structure. This photoresponsivity broadens the potential device applications to the realm of optical fiber communications,[64] image sensors,[65] and pulse oximeters.[66] In addition, when the photosensitivity is combined with its tunable electrical properties (memory and gate), the heterojunction diode can provide a multi-functionality for artificial retinas[67] and multiple-state logic devices.[68] Figure 2.22a shows the I_{DS}-V_{DS} curves of the heterojunction diode in the dark state and under illumination (460 nm; 2.2 mW/cm^2). The generated photocurrent increases for not only reverse but also forward biases because the drift current at the forward bias can be blocked by the barrier at the interface between BP and n-InGaAs, which reduces carrier recombination (Figure 2.23).[69] Figure 2.24 shows the photoinduced current and responsivity as a function of gate voltage. Herein, the responsivity under reverse bias increases six fold as the gate voltage decreases from 0 to −40 V because of the increase in built-in potential, which can promote the electron-hole separation (Figure 2.25).[70] Conversely, the responsivity under forward bias depends weakly on the gate voltage. Figure 2.22 shows the spectral responsivity of the device with a bias voltage V_{DS} = +1.0 V. The spectral responsivity ranges from the ultraviolet (UV) to the near infrared (NIR) with a maximum responsivity of 704 mA/W. The spectral responsivity of this photoresponsive device depends on the band gap of the materials from which it is fabricated;[17, 71] however, the proposed n-InGaAs–BP heterojunction diode can detect the UV light, which does not coincide with the band gaps of either BP (~0.4 eV) or InGaAs (~0.75 eV). This UV absorption is due to electron excitations between the nested valance and conduction bands of the BP, which is called "band nesting".[72] In the spectra response, the heterojunction diode shows the different photoresponsivity at the wavelengths under 460 nm due to the differences in the light intensity of used LEDs for measuring the photocurrent and the trap sites at the interface of the heterojunction, which also influences the relatively low photocurrent of the device.[73] In this configuration, the current of the

heterojunction diode can be controlled by two independent stimuli: the applied gate voltage and the incident light (Figure 2.22c). As shown in Figure 2.22d, the device generates three different current states (0, 1, and 2) depending on the applied gate voltage and the optical illumination of the device at a forward bias of 1 V. This capacity to manipulate output signals by optical and electrical inputs can be used in a multiple logic operator, where the incident light and applied gate voltage can be used as two input signals to manipulate output current for multiple output signals. This multiple logic operator can find potential applications in mixed optoelectronic logic devices and digital-to-analog converters.[68, 74] The multi-functional n-InGaAs–BP heterojunction diode provides a versatile platform for applications requiring rectifying, switching, memory, photoresponsivity, and multiple signal-generation capabilities. In terms of the multiple functionalities, the device has results comparable to those of other multi-functional devices (Table 2.1). Especially, our device shows a much simple structure and an easy fabrication process, compared to other 2D based multi-functional heterostructure with a floating gate. These results demonstrate the great potential of the n-InGaAs–BP heterojunction diode for future multi-functional electronics.

2.4 Conclusion

In conclusion, we developed a new type of heterostructure device based on BP and n-InGaAs nanomembrane semiconductors. The device is gate tunable and photoresponsive, has programmable diode characteristics, and offers gate-tunable rectification with a maximum rectification ratio of 4600 and switching with an on/off ratio exceeding 10^5. In addition, the proposed heterojunction diode can be programed by the modulation of forward current because of the capacitive gating effect. Furthermore, the device is photoresponsive with a maximum responsivity of 0.704 A/W in a spectral range spanning the UV to NIR. By combining the gate tunability and photoresponsivity, the device can generate multiple signals. These properties make n-InGaAs–BP heterojunction diodes very attractive for the development of multi-functional devices and future electronics, such as the neuromorphic system.

2.5 References

(1) Di Cioccio, L.; Jalaguier, E.; Letertre, F. III-V Layer Transfer onto Silicon and Applications. *phys. stat. sol. (a)* **2005,** *202*, 509-515.

(2) Datta, S.; Dewey, G.; Fastenau, J. M.; Hudait, M. K.; Loubychev, D.; Liu, W. K.; Radosavljevic, M.; Rachmady, W.; Chau, R. Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate. *Ieee Electron Device Lett.* **2007,** *28*, 685-687.

(3) Justice, J.; Bower, C.; Meitl, M.; Mooney, M. B.; Gubbins, M. A.; Corbett, B. Wafer-Scale Integration of Group III-V Lasers on Silicon Using Transfer Printing of Epitaxial Layers. *Nat.*

Photonics **2012,** *6*, 610-614.

(4) Wada, H.; Kamijoh, T. 1.3-μm InP-InGaAsP Lasers Fabricated on Si Substrates by Wafer Bonding. *Ieee J. Sel. Top. Quantum Electron.* **1997,** *3*, 937-942.

(5) Chilukuri, K.; Mori, M. J.; Dohrman, C. L.; Fitzgerald, E. A. Monolithic CMOS-Compatible AlGaInP Visible LED Arrays on Silicon on Lattice-Engineered Substrates (SOLES). *Semicond. Sci. Technol.* **2007,** *22*, 29-34.

(6) Horng, R. H.; Wuu, D. S.; Wei, S. C.; Tseng, C. Y.; Huang, M. F.; Chang, K. H.; Liu, P. H.; Lin, K. C. AlGaInP Light-Emitting Diodes with Mirror Substrates Fabricated by Wafer Bonding. *Appl.Phys. Lett.* **1999,** *75*, 3054-3056.

(7) Gity, F.; Daly, A.; Snyder, B.; Peters, F. H.; Hayes, J.; Colinge, C.; Morrison, A. P.; Corbett, B. Ge/Si Heterojunction Photodiodes Fabricated by Low Temperature Wafer Bonding. *Opt. Express* **2013,** *21*, 17309-17314.

(8) Levine, B. F.; Pinzone, C. J.; Hui, S.; King, C. A.; Leibenguth, R. E.; Zolnowski, D. R.; Lang, D. V.; Krautter, H. W.; Geva, M. Ultralow-Dark-Current Wafer-Bonded Si/InGaAs Photodetectors. *Appl.Phys. Lett.* **1999,** *75*, 2141-2143.

(9) Li, D.; Lan, C.; Manikandan, A.; Yip, S.; Zhou, Z.; Liang, X.; Shu, L.; Chueh, Y.-L.; Han, N.; Ho, J. C., Ultra-Fast Photodetectors Based on High-Mobility Indium Gallium Antimonide Nanowires. *Nat. Commun.* **2019**, *10*, 1664.

(10) Yokoyama, M.; Iida, R.; Ikku, Y.; Kim, S.; Takagi, H.; Yasuda, T.; Yamada, H.; Ichikawa, O.; Fukuhara, N.; Hata, M.; Takenaka, M.; Takagi, S. Formation of III–V-on-Insulator Structures on Si by Direct Wafer Bonding. *Semicond. Sci. Technol.* **2013,** *28*, 094009.

(11) Zhang, X. X.; Raskin, J. P. Low-Temperature Wafer Bonding: A Study of Void Formation and Influence on Bonding Strength. *J. Microelectromech. Syst.* **2005,** *14*, 368-382.

(12) Tan, Y. H.; Chong, G. Y.; Tan, C. S. Direct Bonding of Ge-Ge Using Epitaxially Grown Ge-on-Si Wafers. *ECS J. Solid State Sci. Technol.* **2012,** *1*, P18-P22.

(13) Ko, H.; Takei, K.; Kapadia, R.; Chuang, S.; Fang, H.; Leu, P. W.; Ganapathi, K.; Plis, E.; Kim, H. S.; Chen, S.-Y.; Madsen, M.; Ford, A. C.; Chueh, Y.-L.; Krishna, S.; Salahuddin, S.; Javey, A. Ultrathin Compound Semiconductor on Insulator Layers for High-Performance Nanoscale Transistors. *Nature* **2010,** *468*, 286-289.

(14) Nah, J.; Fang, H.; Wang, C.; Takei, K.; Lee, M. H.; Plis, E.; Krishna, S.; Javey, A. III-V Complementary Metal-Oxide-Semiconductor Electronics on Silicon Substrates. *Nano Lett.* **2012,** *12*, 3592-3595.

(15) Wang, C.; Chien, J.-C.; Fang, H.; Takei, K.; Nah, J.; Plis, E.; Krishna, S.; Niknejad, A. M.; Javey, A. Self-Aligned, Extremely High Frequency III-V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates. *Nano Lett.* **2012,** *12*, 4140-4145.

(16) Kim, K.-H.; Um, D. S.; Lee, H.; Lim, S.; Chang, J.; Koo, H. C.; Oh, M.-W.; Ko, H.; Kim, H.-j.

Gate-Controlled Spin-Orbit Interaction in InAs High-Electron Mobility Transistor Layers Epitaxially Transferred onto Si Substrates. *ACS Nano* **2013,** *7*, 9106-9114.

(17) Um, D. S.; Lee, Y.; Lim, S.; Park, J.; Yen, W.-C.; Chueh, Y.-L.; Kim, H.-j.; Ko, H. InGaAs Nanomembrane/Si van der Waals Heterojunction Photodiodes with Broadband and High Photoresponsivity. *ACS Appl. Mater. Interfaces* **2016,** *8*, 26105-26111.

(18) Geim, A. K.; Grigorieva, I. V. van der Waals Heterostructures. *Nature* **2013,** *499*, 419-425.

(19) Jariwala, D.; Marks, T. J.; Hersam, M. C. Mixed-Dimensional van der Waals Heterostructures. *Nat. Mater.* **2017,** *16*, 170-181.

(20) Liu, Y.; Weiss, N. O.; Duan, X. D.; Cheng, H.-C.; Huang, Y.; Duan, X. F. van der Waals Heterostructures and Devices. *Nat. Rev. Mater.* **2016,** *1*, 16042.

(21) AlAmri, A. M.; Leung, S.-F.; Vaseem, M.; Shamim, A.; He, J.-H. Fully Inkjet-Printed Photodetector Using a Graphene/Perovskite/Graphene Heterostructure. *IEEE Trans. Electron Devices* **2019**, *66*, 2657-2661.

(22) Yang, W.; Chen, J.; Zhang, Y.; Zhang, Y.; He, J.-H.; Fang, X., Silicon-Compatible Photodetectors: Trends to Monolithically Integrate Photosensors with Chip Technology. *Adv. Funct. Mater.* **2019**, *29*, 1808182.

(23) Jariwala, D.; Sangwan, V. K.; Wu, C.-C.; Prabhumirashi, P. L.; Geier, M. L.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. Gate-Tunable Carbon Nanotube-MoS_2 Heterojunction p-n Diode. *Proc. Natl. Acad. Sci. U. S. A.* **2013,** *110*, 18076-18080.

(24) Rathi, S.; Lee, I.; Lim, D.; Wang, J.; Ochiai, Y.; Aoki, N.; Watanabe, K.; Taniguchi, T.; Lee, G.-H.; Yu, Y.-J.; Kim, P.; Kim, G. H. Tunable Electrical and Optical Characteristics in Monolayer Graphene and Few-Layer MoS_2 Heterostructure Devices. *Nano Lett.* **2015,** *15*, 5017-5024.

(25) Jariwala, D.; Howell, S. L.; Chen, K. S.; Kang, J.; Sangwan, V. K.; Filippone, S. A.; Turrisi, R.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. Hybrid, Gate-Tunable, van der Waals p-n Heterojunctions from Pentacene and MoS_2. *Nano Lett.* **2016,** *16*, 497-503.

(26) Kim, W.; Li, C.; Chaves, F. A.; Jimenez, D.; Rodriguez, R. D.; Susoma, J.; Fenner, M. A.; Lipsanen, H.; Riikonen, J. Tunable Graphene-GaSe Dual Heterojunction Device. *Adv. Mater.* **2016,** *28*, 1845-1852.

(27) Roy, T.; Tosun, M.; Cao, X.; Fang, H.; Lien, D.-H.; Zhao, P.; Chen, Y.-Z.; Chueh, Y.-L.; Guo, J.; Javey, A. Dual-Gated MoS_2/WSe_2 van der Waals Tunnel Diodes and Transistors. *ACS Nano* **2015,** *9*, 2071-2079.

(28) Roy, K.; Padmanabhan, M.; Goswami, S.; Sai, T. P.; Ramalingam, G.; Raghavan, S.; Ghosh, A. Graphene-MoS_2 Hybrid Structures for Multifunctional Photoresponsive Memory Devices. *Nat. Nanotechnol.* **2013,** *8*, 826-830.

(29) Lei, S.; Wen, F.; Li, B.; Wang, Q.; Huang, Y.; Gong, Y.; He, Y.; Dong, P.; Bellah, J.; George, A.; Ge, L.; Lou, J.; Halas, N. J.; Vajtai, R.; Ajayan, P. M. Optoelectronic Memory Using Two-

Dimensional Materials. *Nano Lett.* **2015,** *15*, 259-265.

(30) Long, M.; Liu, E.; Wang, P.; Gao, A.; Xia, H.; Luo, W.; Wang, B.; Zeng, J.; Fu, Y.; Xu, K.; Zhou, W.; Lv, Y.; Yao, S.; Lu, M.; Chen, Y.; Ni, Z.; You, Y.; Zhang, X.; Qin, S.; Shi, Y.; Hu, W.; Xing, D.; Miao, F. Broadband Photovoltaic Detectors Based on an Atomically Thin Heterostructure. *Nano Lett.* **2016,** *16*, 2254-2259.

(31) Chen, P.; Xiang, J.; Yu, H.; zhang, J.; Xie, G.; Wu, S.; Lu, X.; Wang, G.; Zhao, J.; Wen, F.; Liu, Z.; Yang, R.; Shi, D.; Zhang, G. Gate Tunable MoS_2–Black Phosphorus Heterojunction Devices. *2D Mater.* **2015,** *2*, 034009.

(32) Deng, Y.; Luo, Z.; Conrad, N. J.; Liu, H.; Gong, Y.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Xu, X.; Ye, P. D. Black Phosphorus-Monolayer MoS_2 van der Waals Heterojunction p-n Diode. *ACS Nano* **2014,** *8*, 8292-8299.

(33) Buscema, M.; Groenendijk, D. J.; Steele, G. A.; van der Zant, H. S.; Castellanos-Gomez, A. Photovoltaic Effect in Few-Layer Black Phosphorus PN Junctions Defined by Local Electrostatic Gating. *Nat. Commun.* **2014,** *5*, 4651.

(34) Huang, M.; Li, S.; Zhang, Z.; Xiong, X.; Li, X.; Wu, Y. Multifunctional High-Performance van der Waals Heterostructures. *Nat. Nanotechnol.* **2017,** *12*, 1148-1154.

(35) Jeon, P. J.; Lee, Y. T.; Lim, J. Y.; Kim, J. S.; Hwang do, K.; Im, S. Black Phosphorus-Zinc Oxide Nanomaterial Heterojunction for p-n Diode and Junction Field-Effect Transistor. *Nano Lett.* **2016,** *16*, 1293-1298.

(36) Wang, L.; Huang, L.; Tan, W. C.; Feng, X.; Chen, L.; Ang, K.-W. Tunable Black Phosphorus Heterojunction Transistors for Multifunctional Optoelectronics. *Nanoscale* **2018,** *10*, 14359-14367.

(37) Tian, H.; Guo, Q.; Xie, Y.; Zhao, H.; Li, C.; Cha, J. J.; Xia, F.; Wang, H. Anisotropic Black Phosphorus Synaptic Device for Neuromorphic Applications. *Adv. Mater.* **2016,** *28*, 4991-4997.

(38) Tian, H.; Cao, X.; Xie, Y.; Yan, X.; Kostelec, A.; DiMarzio, D.; Chang, C.; Zhao, L.-D.; Wu, W.; Tice, J.; Cha, J. J.; Guo, J.; Wang, H. Emulating Bilingual Synaptic Response Using a Junction-Based Artificial Synaptic Device. *ACS Nano* **2017,** *11*, 7156-7163.

(39) Ruzmetov, D.; Zhang, K.; Stan, G.; Kalanyan, B.; Bhimanapati, G. R.; Eichfeld, S. M.; Burke, R. A.; Shah, P. B.; O'Regan, T. P.; Crowne, F. J.; Birdwell, A. G.; Robinson, J. A.; Davydov, A. V.; Ivanov, T. G. Vertical 2D/3D Semiconductor Heterostructures Based on Epitaxial Molybdenum Disulfide and Gallium Nitride. *ACS Nano* **2016,** *10*, 3580-3588.

(40) Castellanos-Gomez, A.; Vicarelli, L.; Prada, E.; Island, J. O.; Narasimha-Acharya, K. L.; Blanter, S. I.; Groenendijk, D. J.; Buscema, M.; Steele, G. A.; Alvarez, J. V.; Zandbergen, H. W.; Palacios, J. J.; van der Zant, H. S. J. Isolation and Characterization of Few-Layer Black Phosphorus. *2D Mater.* **2014,** *1*, 025001.

(41) Yang, Y. S.; Um, D. S.; Lee, Y.; Shin, J.; Chang, J.; Koo, H. C.; Ko, H.; Kim, H.-j. Spin Injection

and Detection in $In_{0.53}Ga_{0.47}As$ Nanomembrane Channels Transferred onto Si Substrates. *Appl. Phys. Express* **2014,** *7*, 093004.

(42) Das, S.; Gulotty, R.; Sumant, A. V.; Roelofs, A. All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor. *Nano Lett.* **2014,** *14*, 2861-2866.

(43) Lu, J.; Carvalho, A.; Wu, J.; Liu, H.; Tok, E. S.; Neto, A. H.; Ozyilmaz, B.; Sow, C. H. Enhanced Photoresponse from Phosphorene-Phosphorene-Suboxide Junction Fashioned by Focused Laser Micromachining. *Adv. Mater.* **2016,** *28*, 4090-4096.

(44) Liu, H.; Neal, A. T.; Zhu, Z.; Luo, Z.; Xu, X.; Tomanek, D.; Ye, P. D. Phosphorene: an Unexplored 2D Semiconductor with a High Hole Mobility. *ACS Nano* **2014,** *8*, 4033-4041.

(45) Du, Y.; Liu, H.; Deng, Y.; Ye, P. D. Device Perspective for Black Phosphorus Field-Effect Transistors: Contact Resistance, Ambipolar Behavior, and Scaling. *ACS Nano* **2014,** *8*, 10035-10042.

(46) Liu, H.; Hussain, S.; Ali, A.; Naqvi, B. A.; Vikraman, D.; Jeong, W.; Song, W.; An, K.-S.; Jung, J. A Vertical WSe_2–$MoSe_2$ p–n Heterostructure with Tunable Gate Rectification. *RSC Adv.* **2018,** *8*, 25514-25518.

(47) Dastgeer, G.; Khan, M. F.; Nazir, G.; Afzal, A. M.; Aftab, S.; Naqvi, B. A.; Cha, J.; Min, K. A.; Jamil, Y.; Jung, J.; Hong, S.; Eom, J. Temperature-Dependent and Gate-Tunable Rectification in a Black Phosphorus/WS_2 van der Waals Heterojunction Diode. *ACS Appl. Mater. Interfaces* **2018,** *10*, 13150-13157.

(48) Li, L.; Yu, Y.; Ye, G. J.; Ge, Q.; Ou, X.; Wu, H.; Feng, D.; Chen, X. H.; Zhang, Y. Black Phosphorus Field-Effect Transistors. *Nat. Nanotechnol.* **2014,** *9*, 372-377.

(49) Wang, Z.; Li, Q.; Chen, Y.; Cui, B.; Li, Y.; Besenbacher, F.; Dong, M. The Ambipolar Transport Behavior of WSe_2 Transistors and It's a Analogue Circuits. *NPG Asia Mater.* **2018,** *10*, 703-712.

(50) Sangwan, V. K.; Hersam, M. C. Electronic Transport in Two-Dimensional Materials. *Annu. Rev. Phys. Chem.* **2018,** *69*, 299-325.

(51) Taoka, N.; Yokoyama, M.; Kim, S. H.; Suzuki, R.; Lee, S.; Iida, R.; Hoshii, T.; Jevasuwan, W.; Maeda, T.; Yasuda, T.; Ichikawa, O.; Fukuhara, N.; Hata, M.; Takenaka, M.; Takagi, S. Impact of Fermi Level Pinning Inside Conduction Band on Electron Mobility in InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors. *Appl.Phys. Lett.* **2013,** *103*, 143509.

(52) Livani, A. M.; Kaatuzian, H. Design and Simulation of an Electrically Pumped Schottky-Junction-Based Plasmonic Amplifier. *Appl. Opt.* **2015,** *54*, 2164-2173.

(53) Shim, J.; Oh, S.; Kang, D.-H.; Jo, S.-H.; Ali, M. H.; Choi, W.-Y.; Heo, K.; Jeon, J.; Lee, S.; Kim, M.; Song, Y. J.; Park, J.-H. Phosphorene/Rhenium Disulfide Heterojunction-Based Negative Differential Resistance Device for Multi-Valued Logic. *Nat. Commun.* **2016,** *7*, 13413.

(54) Huo, N.; Kang, J.; Wei, Z.; Li, S.-S.; Li, J.; Wei, S.-H. Novel and Enhanced Optoelectronic Performances of Multilayer MoS_2-WS_2 Heterostructure Transistors. *Adv. Funct. Mater.* **2014,** *24*,

7025-7031.

(55) Wang, X.; Huang, L.; Peng, Y.; Huo, N.; Wu, K.; Xia, C.; Wei, Z.; Tongay, S.; Li, J. Enhanced Rectification, Transport Property and Photocurrent Generation of Multilayer $ReSe_2/MoS_2$ p–n Heterojunctions. *Nano Res.* **2015,** *9*, 507-516.

(56) Liu, F. C.; Chow, W. L.; He, X. X.; Hu, P.; Zheng, S. J.; Wang, X. L.; Zhou, J. D.; Fu, Q. D.; Fu, W.; Yu, P.; Zeng, Q. S.; Fan, H. J.; Tay, B. K.; Kloc, C.; Liu, Z. van der Waals p-n Junction Based on an Organic-Inorganic Heterostructure. *Adv. Funct. Mater.* **2015,** *25*, 5865-5871.

(57) Kumar, P.; Khosla, R.; Sharma, S. K. Nanoscale Investigations: Surface Potential of Rare-Earth Oxide (Re_2O_3) Thin Films by Kelvin Probe Force Microscopy for Next Generation CMOS Technology. *Surf. Interfaces* **2016,** *4*, 69-76.

(58) Chen, M. K.; Nam, H.; Wi, S.; Priessnitz, G.; Gunawan, I. M.; Liang, X. G. Multibit Data Storage States Formed in Plasma-Treated MoS_2 Transistors. *ACS Nano* **2014,** *8*, 4023-4032.

(59) Lee, Y. T.; Kwon, H.; Kim, J. S.; Kim, H.-H.; Lee, Y. J.; Lim, J. A.; Song, Y.-W.; Yi, Y.; Choi, W.-K.; Hwang, D. K.; Im, S. Nonvolatile Ferroelectric Memory Circuit Using Black Phosphorus Nanosheet-Based Field-Effect Transistors with P(VDF-TrFE) Polymer. *ACS Nano* **2015,** *9*, 10394-10401.

(60) Lee, D.; Choi, Y.; Hwang, E.; Kang, M. S.; Lee, S.; Cho, J. H. Black Phosphorus Nonvolatile Transistor Memory. *Nanoscale* **2016,** *8*, 9107-9112.

(61) Arnold, A. J.; Razavieh, A.; Nasr, J. R.; Schulman, D. S.; Eichfeld, C. M.; Das, S. Mimicking Neurotransmitter Release in Chemical Synapses via Hysteresis Engineering in MoS_2 Transistors. *ACS Nano* **2017,** *11*, 3110-3118.

(62) Li, D.; Chen, M.; Sun, Z.; Yu, P.; Liu, Z.; Ajayan, P. M.; Zhang, Z. Two-Dimensional Non-Volatile Programmable p-n Junctions. *Nat. Nanotechnol.* **2017,** *12*, 901-906.

(63) Li, D.; Chen, M.; Zong, Q.; Zhang, Z. Floating-Gate Manipulated Graphene-Black Phosphorus Heterojunction for Nonvolatile Ambipolar Schottky Junction Memories, Memory Inverter Circuits, and Logic Rectifiers. *Nano Lett.* **2017,** *17*, 6353-6359.

(64) Binda, M.; Natali, D.; Iacchetti, A.; Sampietro, M. Integration of an Organic Photodetector onto a Plastic Optical Fiber by Means of Spray Coating Technique. *Adv. Mater.* **2013,** *25*, 4335-4339.

(65) Song, Y. M.; Xie, Y.; Malyarchuk, V.; Xiao, J.; Jung, I.; Choi, K.-J.; Liu, Z.; Park, H.; Lu, C.; Kim, R.-H.; Li, R.; Crozier, K. B.; Huang, Y.; Rogers, J. A. Digital Cameras with Designs Inspired by the Arthropod Eye. *Nature* **2013,** *497*, 95-99.

(66) Lochner, C. M.; Khan, Y.; Pierre, A.; Arias, A. C. All-Organic Optoelectronic Sensor for Pulse Oximetry. *Nat. Commun.* **2014,** *5*, 5745.

(67) Wang, H.; Liu, H.; Zhao, Q.; Ni, Z.; Zou, Y.; Yang, J.; Wang, L.; Sun, Y.; Guo, Y.; Hu, W.; Liu, Y. A Retina-Like Dual Band Organic Photosensor Array for Filter-Free Near-Infrared-to-Memory Operations. *Adv. Mater.* **2017,** *29*, 1701772.

(68) Bie, Y. Q.; Liao, Z. M.; Zhang, H.-Z.; Li, G. R.; Ye, Y.; Zhou, Y.-B.; Xu, J.; Qin, Z. X.; Dai, L.; Yu, D. P. Self-Powered, Ultrafast, Visible-Blind UV Detection and Optical Logical Operation Based on ZnO/GaN Nanoscale p-n Junctions. *Adv. Mater.* **2011,** *23*, 649-653.

(69) Khan, W.; Kim, S.-D. Ultra-Violet Photo-Response Characteristics of *p*-Si/*i*-SiO_2/*n*-ZnO Heterojunctions Based on Hydrothermal ZnO Nanorods. *Mater. Sci. Semicond. Process.* **2017,** *66*, 232-240.

(70) Yu, W. J.; Liu, Y.; Zhou, H.; Yin, A.; Li, Z.; Huang, Y.; Duan, X. Highly Efficient Gate-Tunable Photocurrent Generation in Vertical Heterostructures of Layered Materials. *Nat. Nanotechnol.* **2013,** *8*, 952-958.

(71) Lim, S.; Um, D.-S.; Ha, M.; Zhang, Q.; Lee, Y.; Lin, Y.; Fan, Z.; Ko, H. Broadband Omnidirectional Light Detection in Flexible and Hierarchical ZnO/Si Heterojunction Photodiodes. *Nano Res.* **2016,** *10*, 22-36.

(72) Wu, J.; Koon, G. K.; Xiang, D.; Han, C.; Toh, C. T.; Kulkarni, E. S.; Verzhbitskiy, I.; Carvalho, A.; Rodin, A. S.; Koenig, S. P.; Eda, G.; Chen, W.; Neto, A. H.; Ozyilmaz, B. Colossal Ultraviolet Photoresponsivity of Few-Layer Black Phosphorus. *ACS Nano* **2015,** *9*, 8070-8077.

(73) Lopez-Sanchez, O.; Lembke, D.; Kayci, M.; Radenovic, A.; Kis, A. Ultrasensitive Photodetectors Based on Monolayer MoS_2. *Nat. Nanotechnol.* **2013**, *8*, 497-501.

(74) Kim, Y. L.; Jung, H. Y.; Park, S.; Li, B.; Liu, F.; Hao, J.; Kwon, Y.-K.; Jung, Y. J.; Kar, S. Voltage-Switchable Photocurrents in Single-Walled Carbon Nanotube–Silicon Junctions for Analog and Digital Optoelectronics. *Nat. Photonics* **2014,** *8*, 239-243.

(75) Yang, Z.; Liao, L.; Gong, F.; Wang, F.; Wang, Z.; Liu, X.; Xiao, X.; Hu, W.; He, J.; Duan, X. WSe_2/GeSe Heterojunction Photodiode with Giant Gate Tunability. *Nano Energy* **2018,** *49*, 103-108.

(76) Kim, C.; Moon, I.; Lee, D.; Choi, M. S.; Ahmed, F.; Nam, S.; Cho, Y.; Shin, H. J.; Park, S.; Yoo, W. J. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS nano* **2017,** *11*, 1588-1596.

(77) Cheng, R.; Wang, F.; Yin, L.; Wang, Z.; Wen, Y.; Shifa, T. A.; He, J. High-Performance, Multifunctional Devices Based on Asymmetric van der Waals Heterostructures. *Nat. Electron.* **2018,** *1*, 356-361.

(78) Sun, M.; Xie, D.; Sun, Y.; Li, W.; Teng, C.; Xu, J. Lateral Multilayer/Monolayer MoS_2 Heterojunction for High Performance Photodetector Applications. *Sci. Rep.* **2017,** *7*, 4505.

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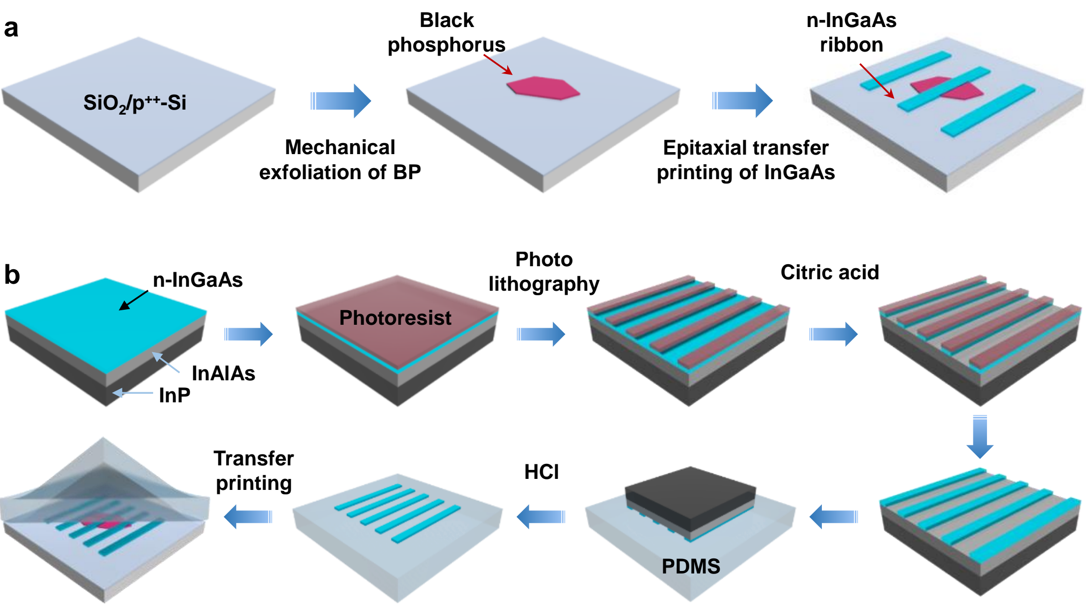

Figure 2.1. (a) Schematic of the fabrication process of n-InGaAs–BP heterojunction diode. (b) Schematic illustration of details of patterning and transfer printing process of n-InGaAs nanomembrane.

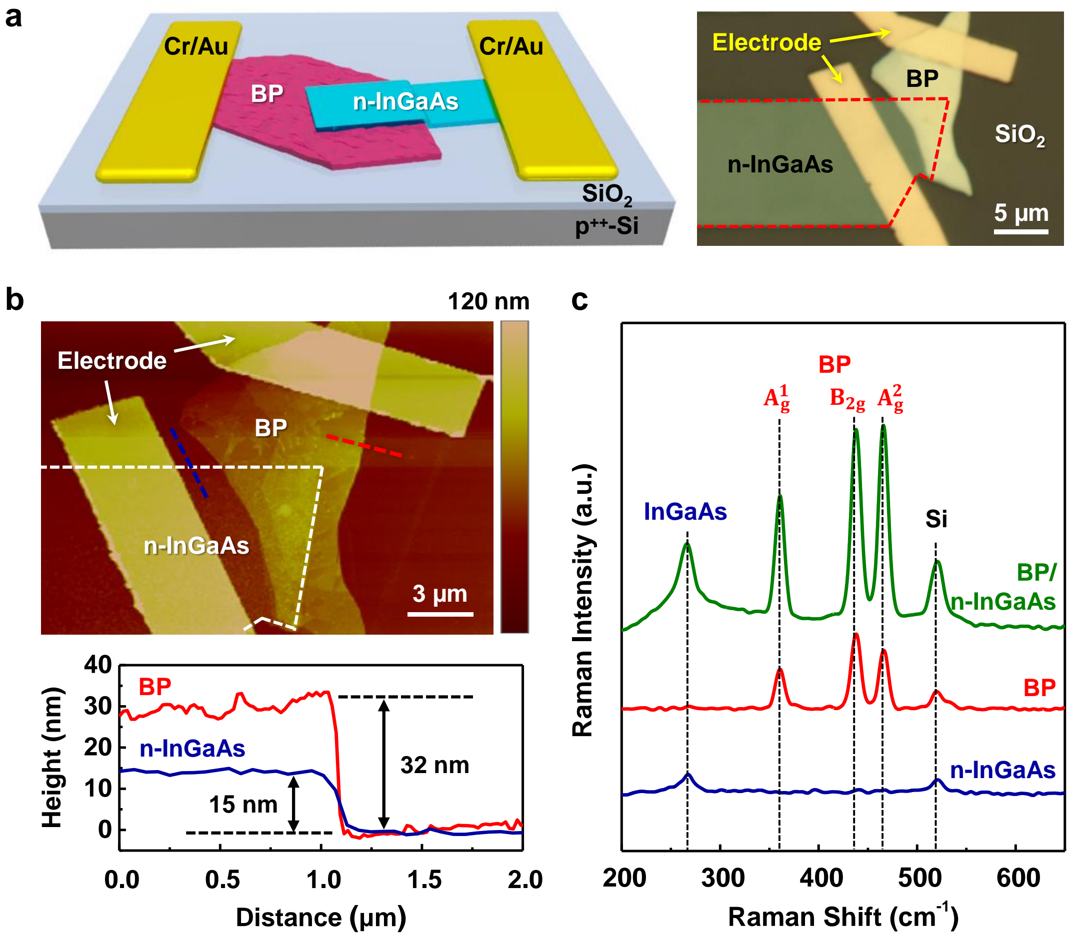

Figure 2.2. Design of heterojunction diode based on n-InGaAs and BP. (a) Schematic and optical-microscope image of n-InGaAs–BP heterojunction diode. (b) AFM image and height analysis of n-InGaAs–BP heterojunction diode and height profile of BP (red line) and n-InGaAs (blue line). (c) Raman spectra of n-InGaAs, BP, and the junction of n-InGaAs and BP layers.

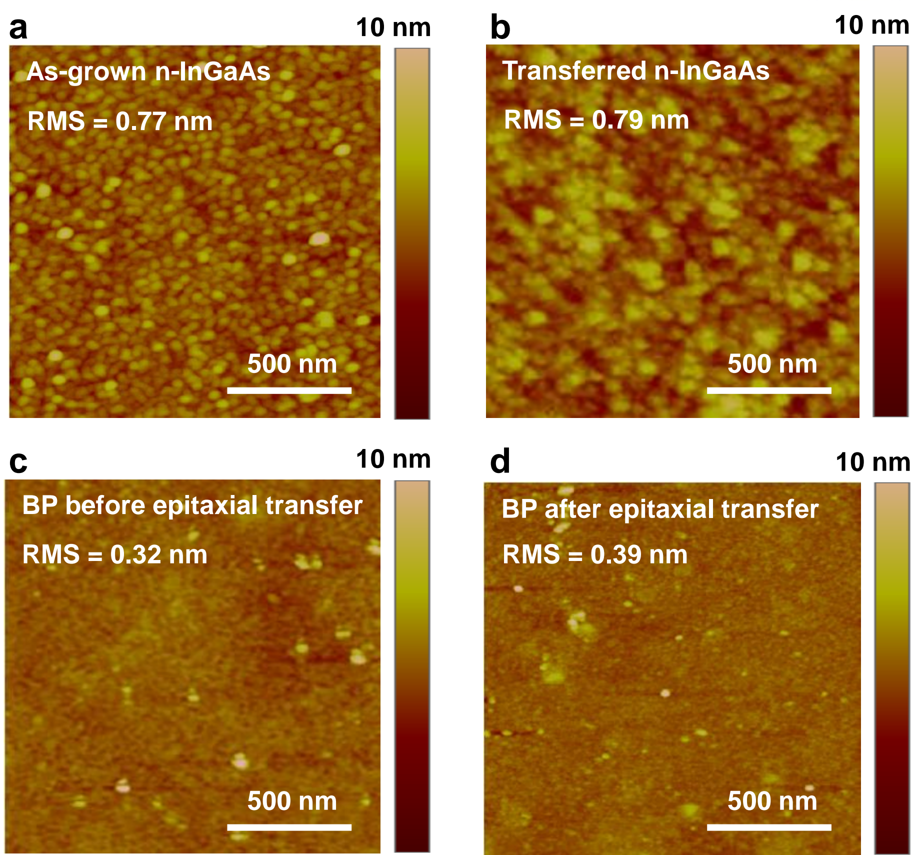

Figure 2.3. AFM images for the surface roughness of (a) as-grown n-InGaAs and (b) transferred n-InGaAs. AFM images for the surface roughness of BP (a) before the epitaxial transfer printing process of n-InGaAs and (d) after the epitaxial transfer printing process of n-InGaAs.

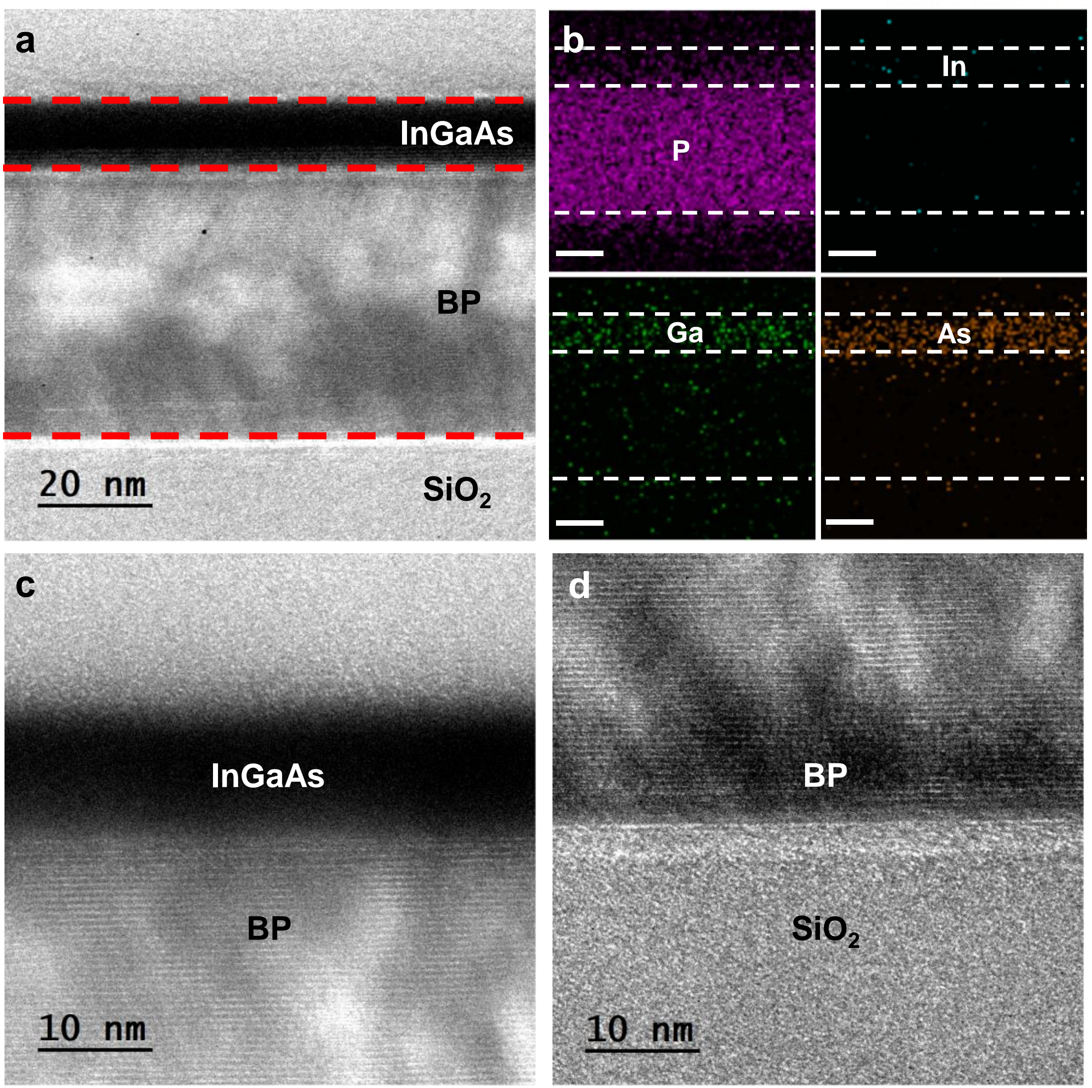

Figure 2.4. (a) Cross-sectional HRTEM image of n-InGaAs and BP heterojunction. (b) EDS elemental mappings of phosphorus (P), Indium (In), Gallium (Ga), and Arsenic (As) of n-InGaAs and BP heterojunction. Scale bar is 10 nm. Cross-sectional HRTEM images of the interface of (c) InGaAs/BP and (d) BP/SiO_2.

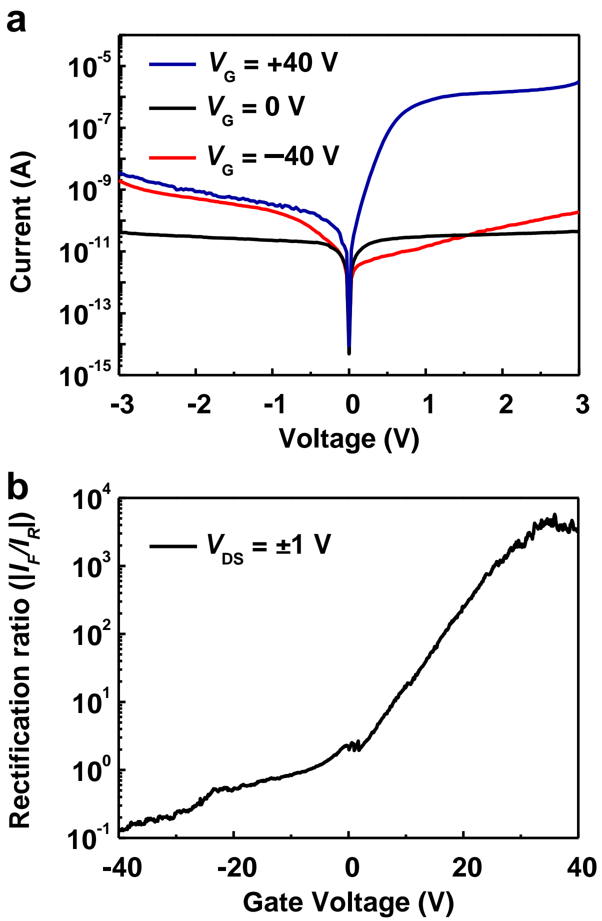

Figure 2.5. Gate-tunable electrical properties of heterojunction diode. (a) *I*–*V* characteristics of n-InGaAs and BP heterojunction diode under different gate voltages of −40, 0, 40 V. (b) Forward-to-reverse current ratio at bias of ±1 V as a function of applied gate voltage.

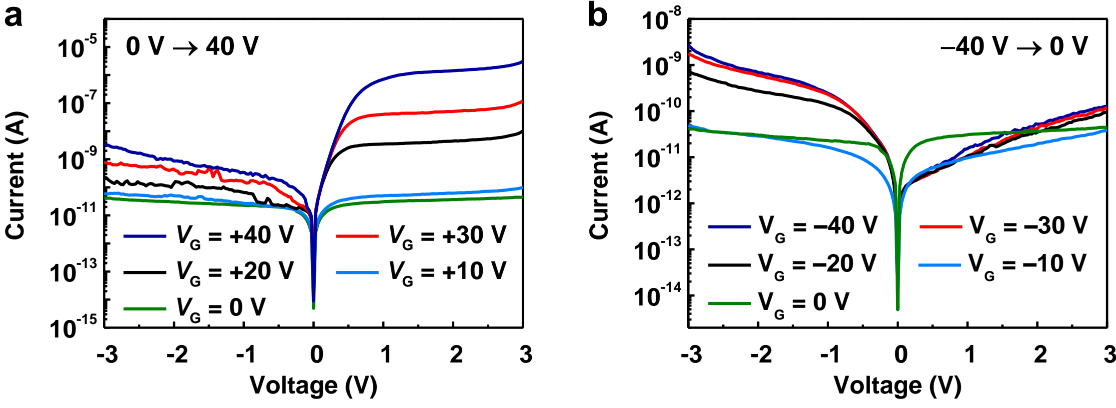

Figure 2.6. *I*–*V* characteristics of n-InGaAs–BP heterojunction diode under different gate voltages (a) from 0 to 40 V and (b) from −40 to 0 V.

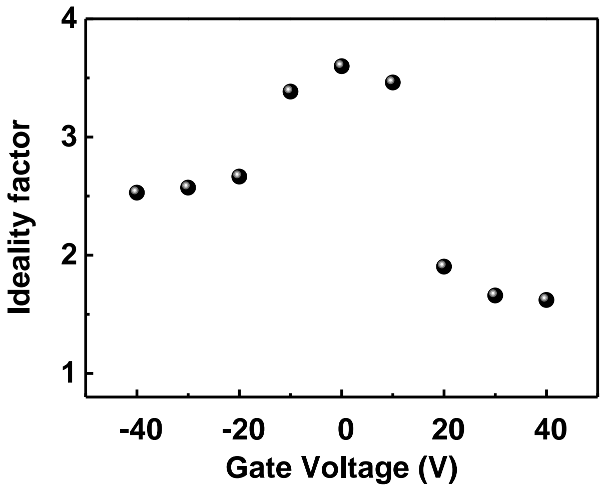

Figure 2.7. Estimated ideality factor as a function of gate voltages.

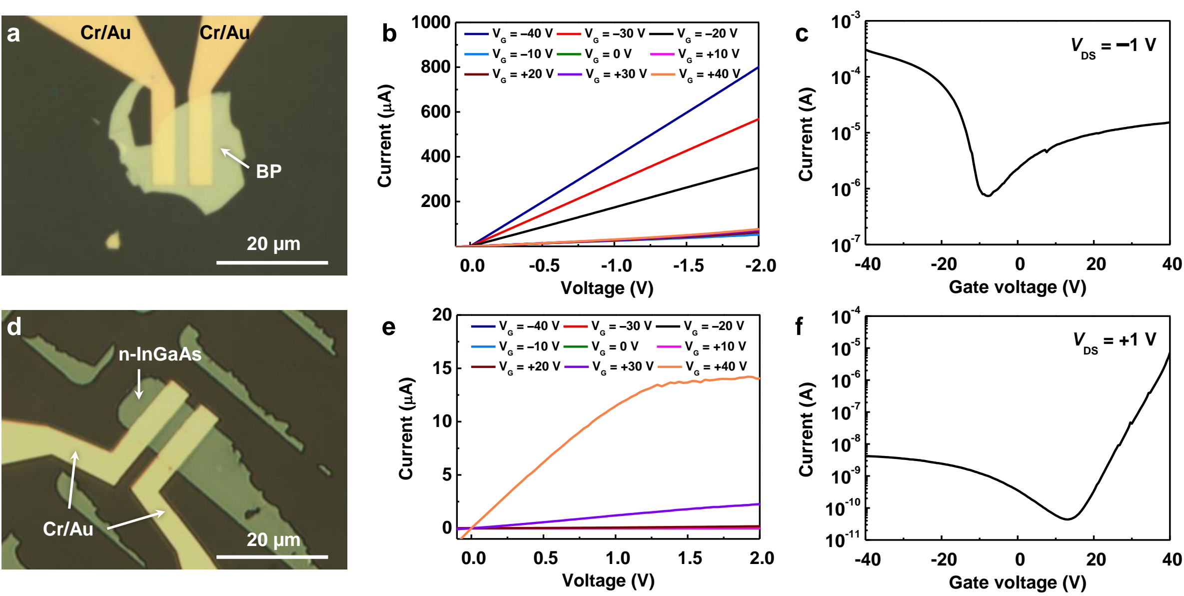

Figure 2.8. (a) Optical-microscope image and (b) output characteristics of BP FET. (c) Transfer characteristics of BP FET at V_{DS} = −1 V. (d) Optical image and (e) output characteristics of n-InGaAs FET. (f) Transfer characteristics of n-InGaAs FET at V_{DS} = 1 V.

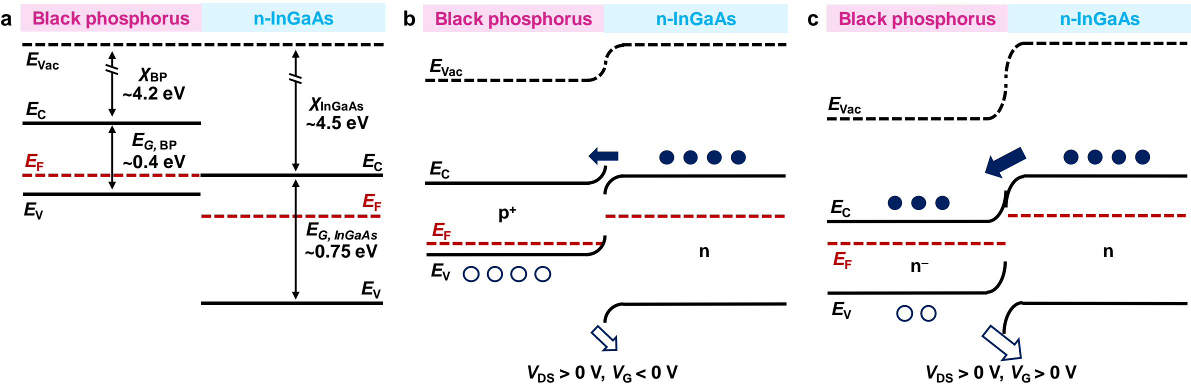

Figure 2.9. (a) Schematic illustration of estimated band alignment between BP and n-InGaAs. Schematic energy-band diagrams of heterojunction diode under forward bias with (b) negative gate voltage and (c) positive gate voltage. E_{Vac}, E_C, E_V, E_F, E_G and χ are the vacuum level, lowest energy level of the conduction band, the highest energy level of the valence band, the Fermi level, the band gap and the electron affinity of the semiconductors, respectively.

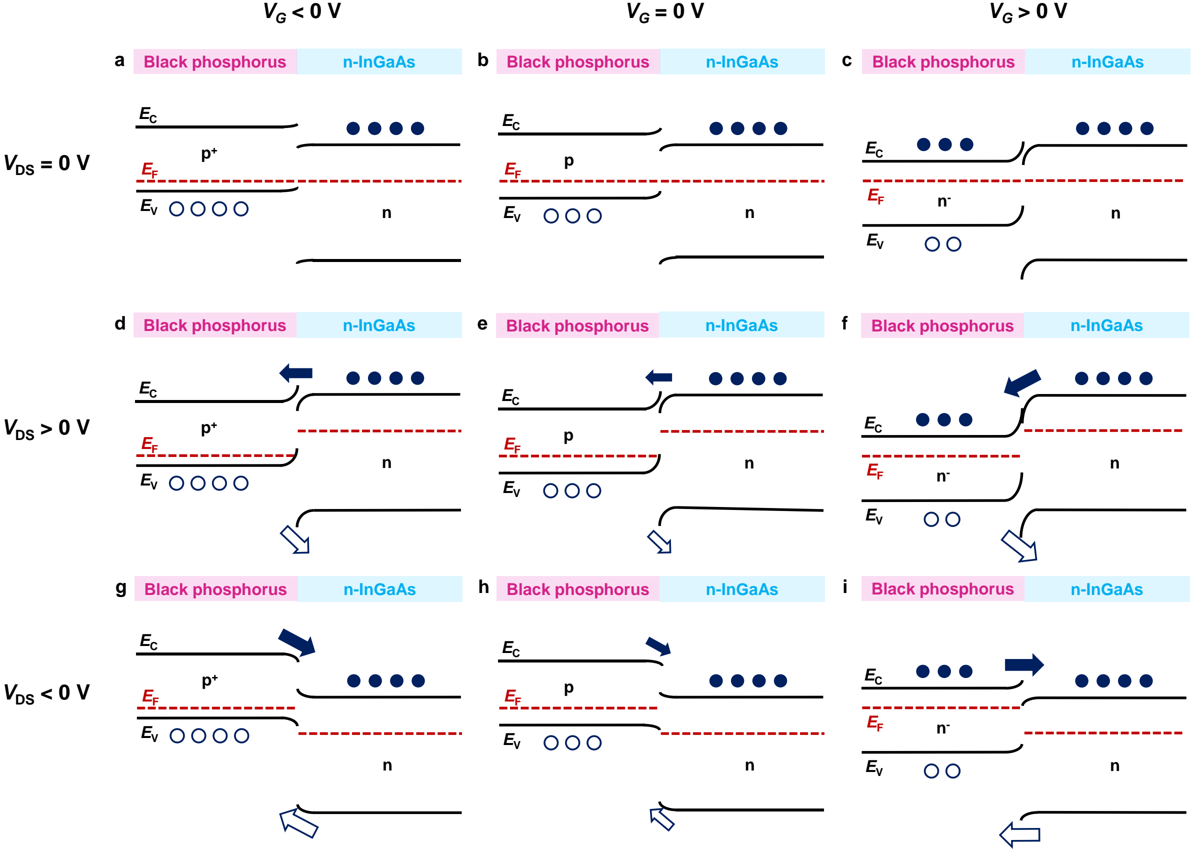

Figure 2.10. Schematic energy-band diagrams of heterojunction diode under zero bias with (a) negative gate voltage, (b) zero gate voltage and (c) positive gate voltage, under forward bias with (d) negative gate voltage, (e) zero gate voltage and (f) positive gate voltage and under reverse bias with (g) negative gate voltage, (h) zero gate voltage and (i) positive gate voltage.

Change of the energy-band diagrams of n-InGaAs–BP heterojunction diode depending on the bias and gate voltages is shown in Figure 2.10 Here, the electrostatic inversion of BP nanosheets from p-type to n-type as the gate voltage change from negative to positive induces the modulation of the Fermi level of BP, whereas the Fermi level of n-InGaAs remains stationary due to the Fermi-level pinning effect. These behaviors induce the change of the band structure and electrical transport in the heterojunction diode (Figures 2.10a–c).[75] Here, the band bending of BP at the interface occurs due to the weak Fermi-level pinning which is caused by the defect and vacancy of molecules in the surface.[76] Due to the modulation of the band structure, the current flow of the heterojunction diode depends on the gate and applied bias voltages. Especially, under the forward bias, the current of device increases at the positive gate voltage due to the decreased barrier height. On the other hand, the flow of holes from BP to InGaAs is dominantly blocked by the barrier at the negative gate voltage, resulting in low current levels as shown in Figures 2.10d–f. While under reverse bias, the change of current in the device is much smaller

than under forward bias because the current flow is blocked by the barrier at positive gate voltage and depends on minority carriers at the negative gate voltage (Figures 2.10g–i).

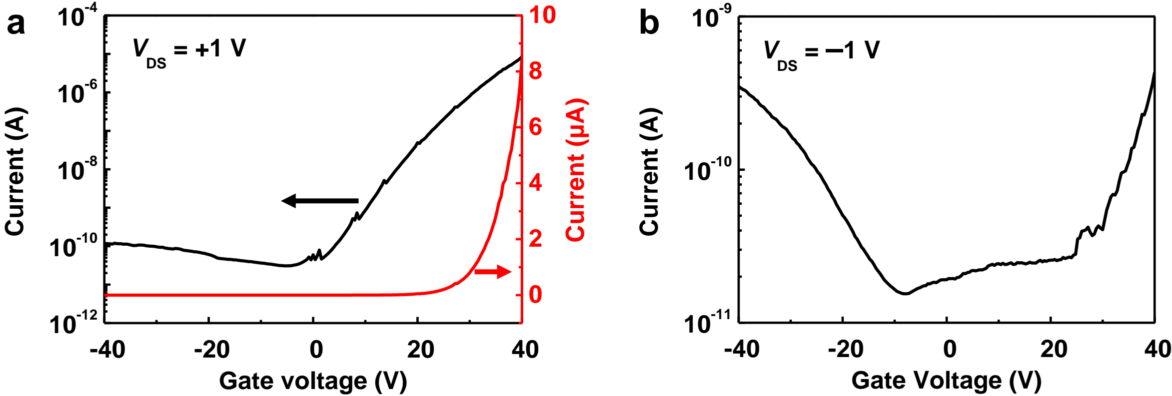

Figure 2.11. (a) Transfer characteristics of n-InGaAs–BP heterojunction diode at V_{DS} = 1 V on a linear scale (red) and on a semi-logarithmic scale (black). (b) Transfer characteristics of n-InGaAs–BP heterojunction diode at V_{DS} = −1 V on a semi-logarithmic scale.

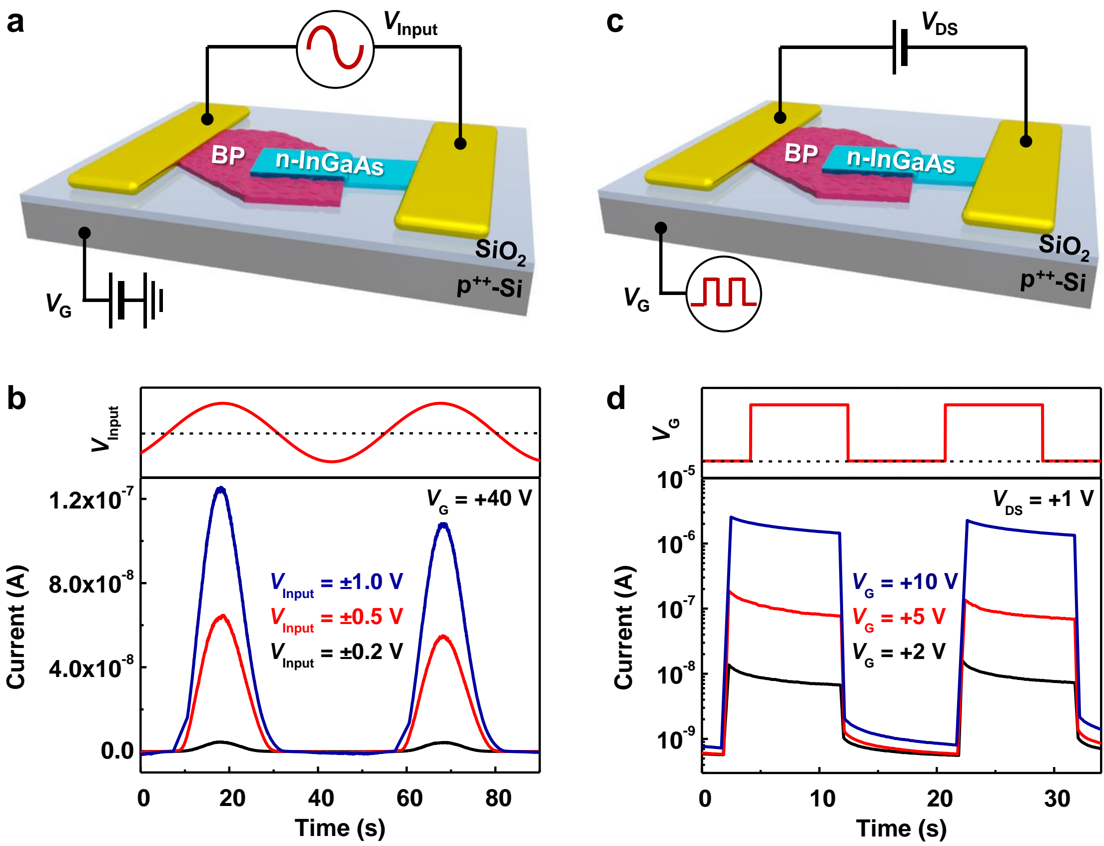

Figure 2.12. Rectifying and switching behaviors of heterojunction diode. (a) Schematic of device structure with corresponding circuit diagram for rectifying measurement. (b) Output current of heterojunction diode at applied gate voltage of 40 V under different intensities of input drain-source voltage of sine waveform (V_{Input} = −1 to +1 V, −0.5 to +0.5 V, −0.2 to +0.2 V). (c) Schematic of device structure with corresponding circuit diagram for switching measurement. (d) Output current of heterojunction diode at forward bias of 1 V under different maximum intensities of applied gate voltage of rectangle waveform (V_G = 2, 5, 10 V).

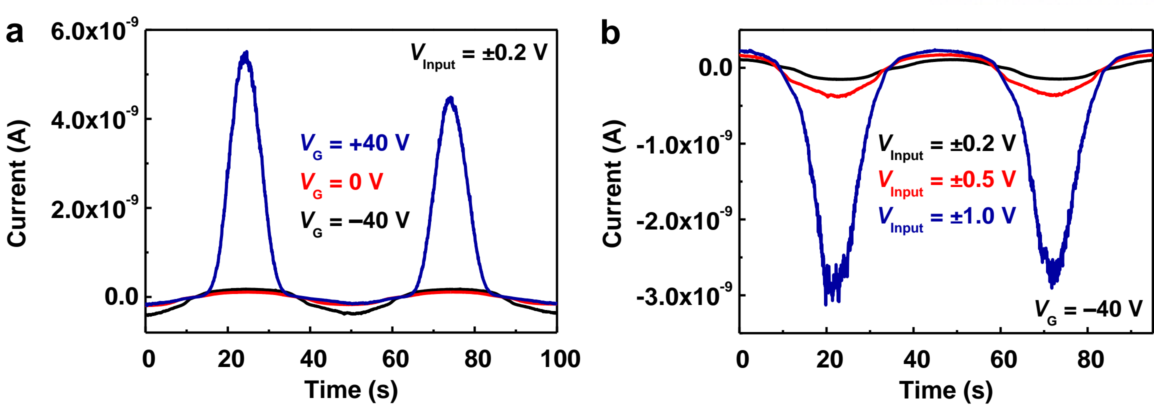

Figure 2.13. (a) Output current of heterojunction diode with sinusoidal input drain-source voltage (V_{Input} = −0.2 to +0.2 V) and under applied gate voltages of −40, 0, 40 V. (b) Output current of heterojunction diode under applied gate voltage of −40 V and with sinusoidal input drain-source voltages of various magnitudes (V_{Input} = −1 to +1, −0.5 to +0.5, and −0.2 to +0.2 V).

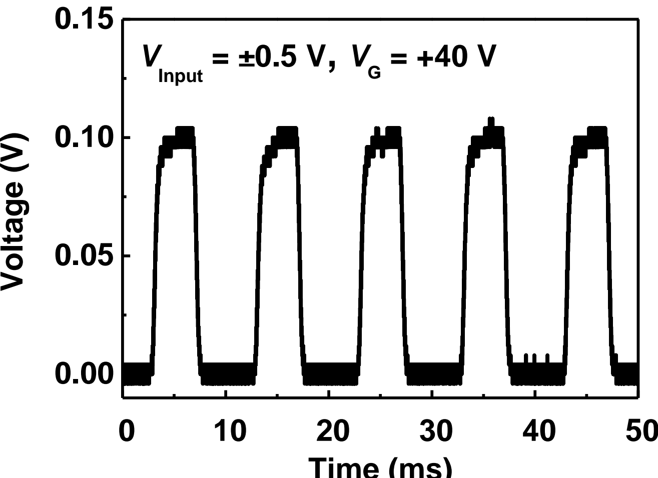

Figure 2.14. Output voltage of n-InGaAs–BP heterojunction diode with external resistor (R = 1 MΩ) under applied gate voltage of 40 V and sinusoidal input drain-source voltage (V_{Input} = −0.5 to 0.5 V; 0.1 kHz).

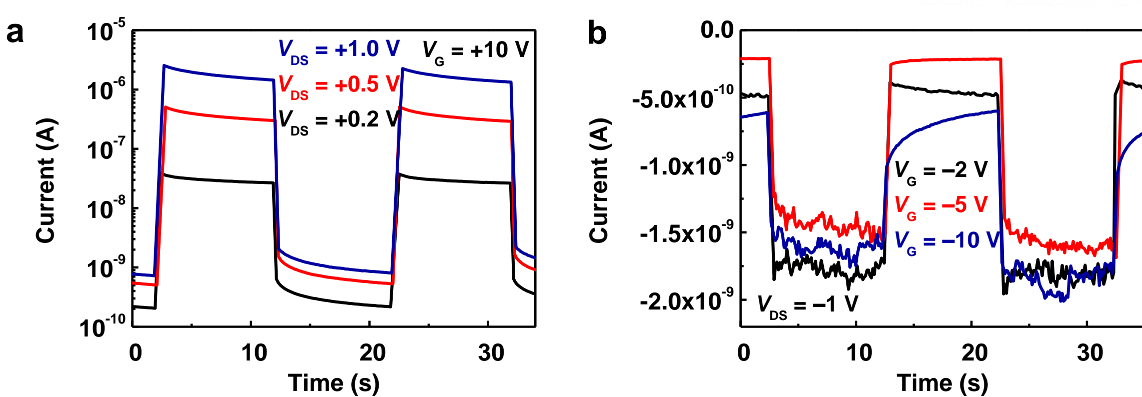

Figure 2.15. (a) Output current of heterojunction diode with rectangular voltage pulse applied to gate (V_G = 10 V) under forward biases of 0.2, 0.5, and 1 V. (b) Output current of heterojunction diode under reverse bias of −1 V and with rectangular voltage waveform of various magnitudes applied to gate (V_G = 2, 5, and 10 V).

Figure 2.16. Non-volatile memory and programmable diode properties of heterojunction diode. (a) Schematic of the heterojunction diode as a memory device. (b) Transfer characteristics at forward bias of 1 V with gate voltage sweep from −40 V to +40 V in positive direction and +40 V to −40 V in negative direction. (c) Retention test at forward bias of 1 V with ±10 V applied gate voltage pulses for 100 ms. (d) Switching behavior between programmed and erased state with applied alternating gate voltages of ±60 V for 1 s at forward bias of 1 V. (e) *I*–*V* characteristics at programmed state (V_{Pulse} = −10 V) with different applied pulse times from 0 to 10 s.

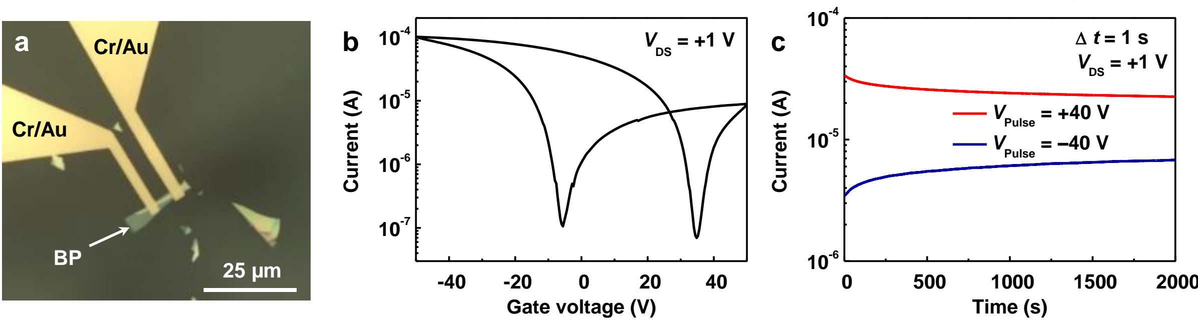

Figure 2.17. (a) Optical-microscope image of BP FET. (b) Transfer characteristics of BP FET under forward bias of 1 V with gate voltage sweep from −50 V to 50 V in positive direction and 50 V to −50 V in negative direction. (c) Retention test of BP FET under forward bias of 1 V with ±40 V applied gate voltage pulses for 1s.

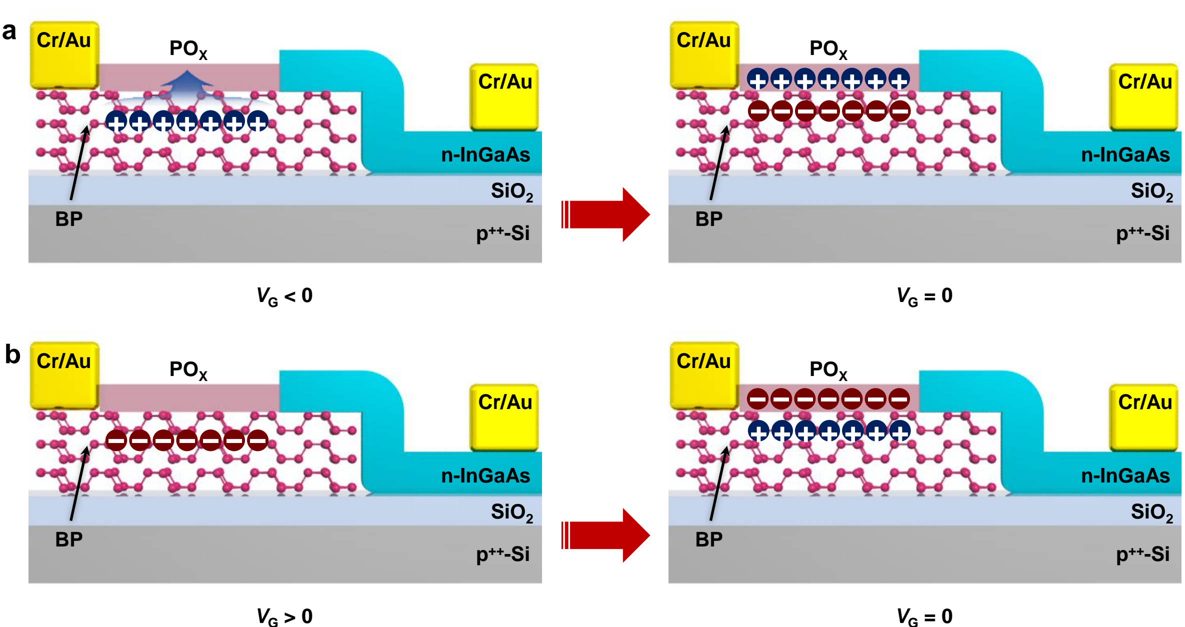

Figure 2.18. Schematics of programmable heterojunction diode in (a) programmed state and (b) erased state.

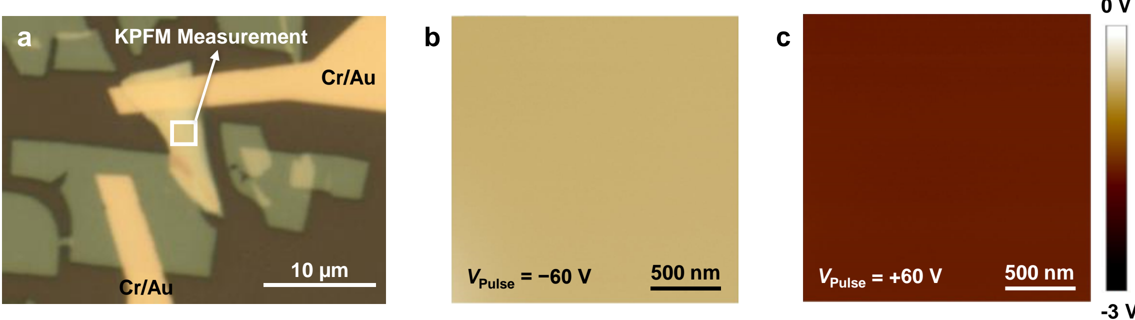

Figure 2.19. (a) Optical-microscope image of n-InGaAs–BP heterojunction diode used for Kelvin probe force scope measurement (KPFM). (b) KPFM image on BP with V_{CPD} ~ −0.59 V after the device is programmed by −60 V applied gate voltage pulses for 1s. (c) KPFM image of BP with V_{CPD} ~−1.65 V after device is erased by 60 V applied gate voltage pulses for 1s.

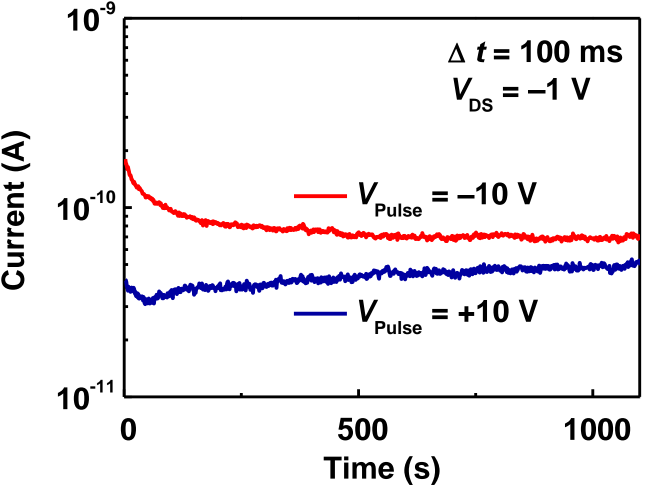

Figure 2.20. Retention test of n-InGaAs–BP heterojunction diode under reverse bias of −1 V with ±10 V applied gate voltage pulses for 100 ms.

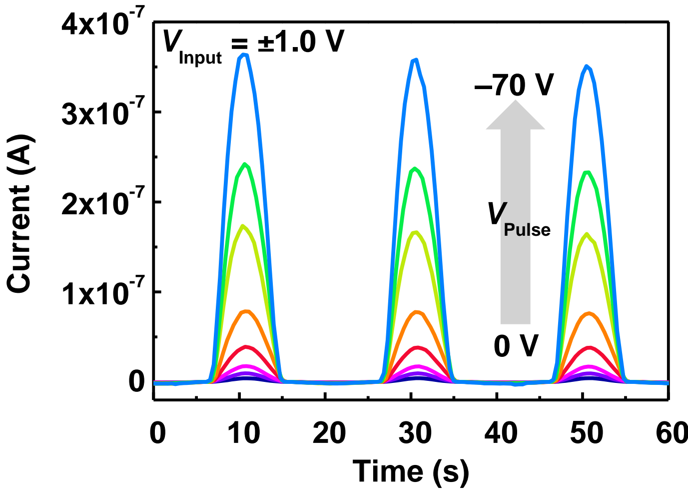

Figure 2.21. Output current of n-InGaAs–BP heterojunction diode with sinusoidal input drain-source voltage (V_{Input} = −1 to +1 V) and 10 s gate voltage pules ranging from 0 to −70 V.

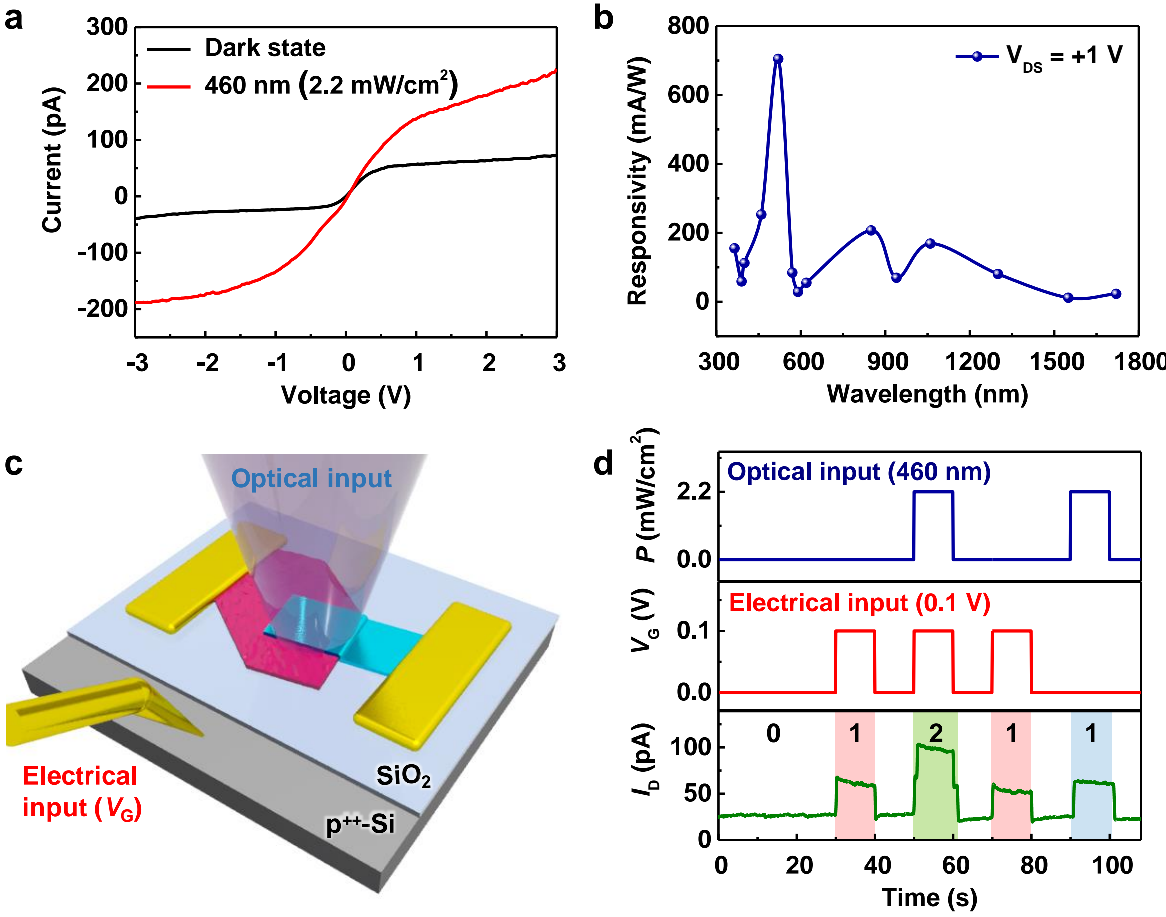

Figure 2.22. Optoelectrical properties of heterojunction diode. (a) *I*–*V* characteristics of n-InGaAs–BP heterojunction diode under dark and 460 nm light illumination. (b) Spectral response under forward bias of 1 V. (c) Schematic illustration of multiple signal generation. (d) Output current under forward bias of 1 V and different input signals (applied gate voltage and illuminated 460 nm laser states).

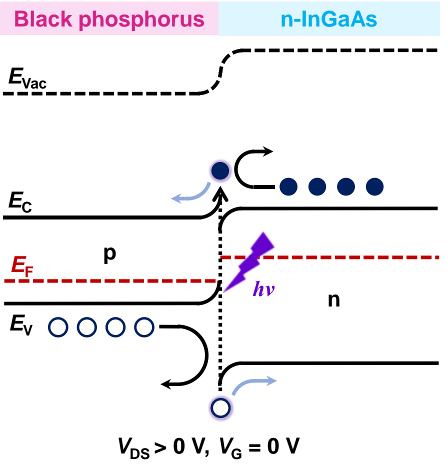

Figure 2.23. Schematic of energy-band diagram of heterojunction diode under forward bias and zero gate voltage.

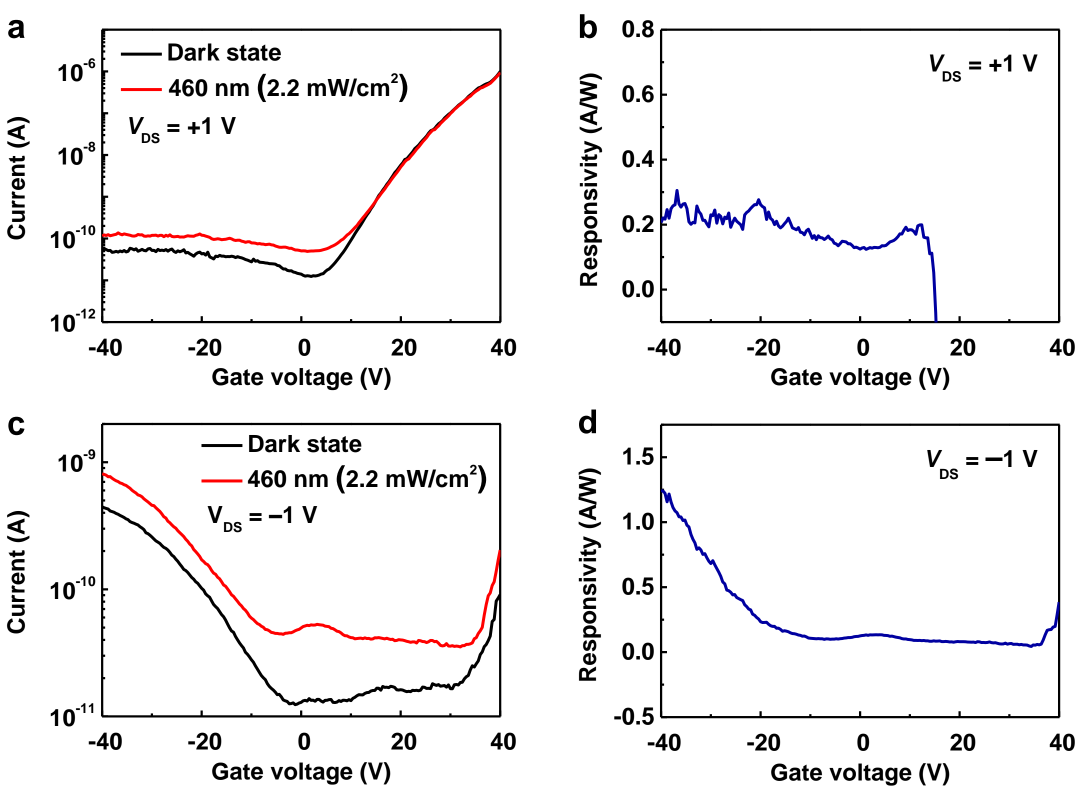

Figure 2.24. (a) Transfer characteristics of n-InGaAs–BP heterojunction diode under forward bias of 1 V in dark and 460 nm light illumination. (b) Responsivity of n-InGaAs–BP heterojunction diode under forward bias of 1 V as a function of gate voltage. (c) Transfer characteristics of n-InGaAs–BP heterojunction diode under reverse bias of −1 V in dark and 460 nm light illumination. (d) Responsivity of n-InGaAs–BP heterojunction diode under reverse bias of −1 V as a function of gate voltage.

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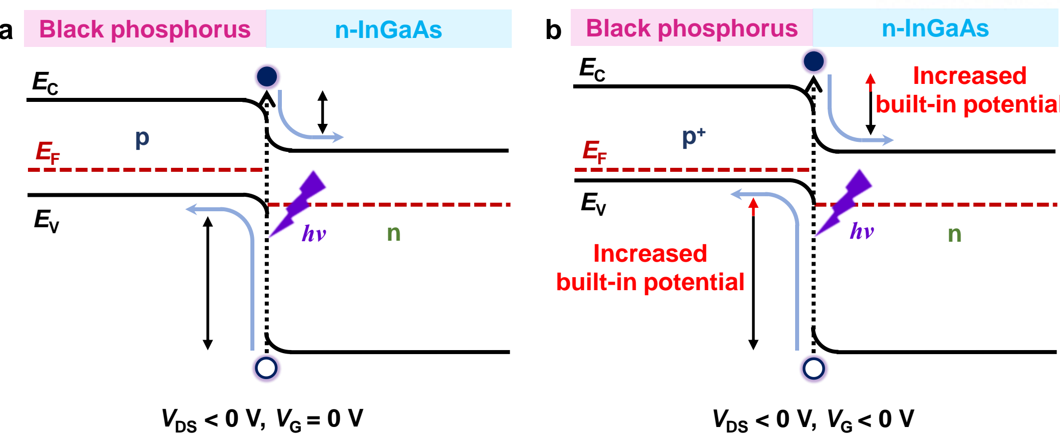

Figure 2.25. Schematic illustration of energy-band diagrams of heterojunction diode under reverse bias with light illumination under (a) zero gate voltage and (b) negative gate voltage states.

Table 2.1. Comparison of possible functionalities of various multi-functional devices.

Structure	Diode	Transistor	Memory	Photodetector	Logic system	Ref.
BP/InGaAs heterojunction	R_{rec}: 4600	M: 84.6 cm^2 V^{-1} s^{-1}; On/Off ratio: ~10^5	T_r: 1000 s	R_{ph}: 0.704 A/W	ADDER	This work
Si/SWNT heterojunction	–	On/Off ratio: ~10^5	–	R_{ph}: ~1 A/W	AND; OR; ADDER	74
BP-MoS_2 heterostructure	R_{rec}: ~4 ×10^5	On/Off ratio: ~10^7	–	–	Inverter	34
MoS_2-$MoTe_2$ heterostructure	R_{rec}: ~10^7	On/Off ratio: ~10^8	R_{pr}: ~10^9	R_{ph}: ~28.6 A/W	–	77
Graphene-MoS_2 heterostructure	–	M: ~10^4 cm^2 V^{-1} s^{-1}	T_r: ~4 × 10^4 s	R_{ph}: ~5 × 10^8 A/W	–	28
Multilayer /Monolayer MoS_2 heterojunction	R_{rec}: ~10^3	M: 0.1–10 cm^2 V^{-1} s^{-1}; On/Off ratio: ~10^7	–	R_{ph}: ~10^3 A/W	–	78
Layer-controlled BP heterojunction	–	M: 100 cm^2 V^{-1} s^{-1}; On/Off ratio: ~10^6	–	R_{ph}: 383 A/W	–	36

R_{rec}: Rectifying ratio, M: Mobility, T_r: Retention time, R_{ph}: Photo-responsivity, R_{pr}: Program/erase ratio

Chapter 3. High-Resolution Filtration Patterning of Silver Nanowire Electrodes for Flexible and Transparent Optoelectronic Devices

3.1 Introduction

The development of low-cost, flexible and transparent electrodes (FTEs) is continuously attracting significant interest owing to the huge demand for wearable optoelectronic devices, such as solar cells,[1] light emitting diodes (LEDs),[2] photodetectors[3] and thin film transistors (TFTs).[4] Various conductive materials, such as indium tin oxide (ITO), carbon nanotubes (CNTs), graphene, and metal nanowires (NWs) have led to the development of FTEs.[5] ITO as a typical transparent conductive electrode material has excellent electrical conductivity and high optical transparency; however, it has poor characteristics in terms of durability and flexibility. Furthermore, it is a high-cost material as indium is a rare metal.[5-7] CNTs and graphene are strong candidates for FTEs; however, they have a drawback in terms of low electrical conductivity.[6] Silver NW (AgNW) is the most promising candidate in view of its excellent mechanical flexibility, optical transparency, and electrical conductivity.[8, 9] Moreover, AgNWs provide additional advantages, such as economy and low-temperature processing.[7] For enhanced performance of AgNW electrodes, various methods have been developed, for example, plasmonic welding technique,[10] AgNW–CNT or AgNW–graphene composites,[11-13] synthesis of thin/long AgNWs,[14] Ag–Pt alloy-walled hollow NWs,[15] and cross aligning technique[16] to reduce the electrical resistivity, and increase the optical transparency, mechanical strength, and thermal and chemical stability of AgNWs. Their excellent mechanical flexibility (even stretchability), electrical conductivity, optical transparency, cost-effectiveness and large-area processing facilitate their use in various flexible (or stretchable) optoelectronic devices, such as solar cells, photodetectors and LEDs.[16, 17]

To utilize AgNW electrodes in image sensors, bioelectric devices, TFTs, and LEDs, fine patterning of AgNW electrodes is essential.[8, 18, 19] Various methods for patterning of AgNWs, for example, photolithography,[19] laser ablation,[20] stamp contact printing,[21] and shadow mask printing method[22] have been investigated. Although photolithography has been established as the most widely used patterning process for device fabrication, it has various drawbacks for patterning of AgNW electrodes. First, this process has a limitation in the selection of the substrate owing to the high baking temperature (> 100 °C) and post-processing methods, such as wet or dry etching processes.[23, 24] In addition, conductive AgNW networks can be damaged during the process of photoresist removal, and it is difficult to completely remove the photoresist residue from the substrate or AgNW network.[24] Although the laser ablation technique is capable of high-resolution AgNW patterning, it can damage the substrate; in addition it suffers from high cost and poor throughput.[25] Stamp contact printing, on the other hand is suitable as a low cost and high throughput process; however, its pattern resolution is very poor.[24] The patterning of

AgNWs using a shadow mask is advantageous in terms of cost effectiveness and it is also free from the substrate selection owing to the low-temperature process and reusability of the mask. However, it is challenging to reduce the pattern resolution because of the limited resolution of the shadow mask.[19, 24] When the thickness of the shadow mask increases, it is difficult to fabricate fine patterns owing to the difficulties involved in the anisotropic etching process. To increase the resolution of the shadow mask, the mask should be thin. However, when the mask becomes very thin, it can be easily broken or torn during the process. In addition, for sharp pattern edge resolution, the mask must be conformably and strongly attached to the substrate to prevent the penetration of the solution by capillary forces between the mask and the substrate. As a result, a new approach is needed to easily control the thin shadow mask for fine-patterning and conformal contact.

In this study, we have developed a fine-patterning method for AgNW networks for high-resolution FTEs based on vacuum filtration on the shadow mask, and transfer printing using a polydimethylsiloxane (PDMS) stamp. Vacuum filtration enables the use of a very thin polyimide (PI) shadow mask with high-resolution patterns because of the vacuum-induced conformal attachment of the mask on an anodic aluminum oxide (AAO) template. In addition, it is economical compared to spin or spray coating processes because there is no wastage of AgNW solution. Moreover, the vacuum filtration process could remove small size-impurities in the AgNW solution as it passes through the pores of the AAO template, resulting in an enhanced optical transparency and electrical conductivity.[26, 27] For a proof of concept of the patterned AgNW electrodes, we have demonstrated their application in flexible optoelectronic devices. A silicon (Si) photodetector based on the AgNW electrodes exhibited an extremely low dark current (3.24×10^{-10} A at 5 V) and an excellent optical on/off ratio (1.86×10^{3}) compared to a device using Ag film electrodes. A ZnO-based flexible and semi-transparent UV photodetector with embedded AgNW electrodes developed in this study exhibited a highly enhanced photocurrent (up to 800%) compared to a device based on the top-mounted AgNW electrodes; furthermore, it operated well under extreme bending conditions (bending radius of approximately 770 μm) and 500 bending cycles.

3.2 Experimental details

***Patterning process*:** The Si substrate was sonicated in isopropyl alcohol (IPA) solution for 30 min for cleaning and sequentially rinsed in IPA and DI water. The Si substrate was treated with an O_2 plasma (18 W, for 5 min). A polyimide (PICOMAX, Korea) solution for the shadow mask was spin coated on the Si substrate at 4000 rpm for 60 s and cured at 120 °C on a hot plate for 3 h. The patterns of PI film were fabricated by standard photolithography (MA-6, SUSS MicroTec, Germany) and reactive ion etching (Lab Star, TTL, Korea) process (20 sccm of SF_6, 60 sccm of Ar; 10 mTorr; 300 W of RF power). The patterned PI film was floated on DI water for separation for 20 min after scratching the edge of the

film. An AAO template (Whatman, UK) of 0.2 μm pore size was used as the pattering substrate. Used AgNW ink (0.05 wt.%) was diluted with an ethanol solution and AgNW ink (Nanopyxis Corp., Korea) containing 0.5 wt.% of AgNWs in ethanol. (for characterization of AgNW)

***Device fabrication for Si-photodetectors*:** The n-type Si substrate was treated with a 4% HF solution for 30 min to remove the oxide layer. The substrate was then rinsed in IPA and DI water. For transferring the patterned AgNW networks from the AAO template after the filtration process onto the PDMS stamp, the AAO template with the patterned AgNW networks were first attached to the PDMS stamp. Next, a small quantity of DI water was dropped on the backside of the AAO template. Then, the AAO template was carefully removed from the PDMS stamp. The patterned AgNW networks on the PDMS stamp were transferred onto the Si substrate by a wet-transfer technique using EtOH.

***Device fabrication for the AgNW electrode embedded UV photodetector*:** A PVA solution (5% in DI water) was spin coated on a clean Si substrate at 4000 rpm for 60 s and annealed at 120 °C on a hot plate for 1 h. Through the same transfer process of AgNWs as mentioned above, patterned AgNW networks were formed on the PVA/Si substrate. A 200-nm-thick ZnO layer was deposited onto the AgNW/PVA/Si substrate by an RF sputtering system (SRN-120D, SORONA, Korea) (20 sccm of O_2; 10 mTorr; 500 W of RF power). Then, an NOA solution (Norland Products Inc., USA) was spin coated on this sample at 4000 rpm for 60 s and exposed to UV radiation (365 nm, 6 W) for 10 min. Finally, this sample was floated on DI water. Next, the PVA layer was removed and simultaneously the NOA film with the UV photodetector arrays was separated from the Si substrate.

3.3 Results and discussion

Figure 3.1 shows the patterning and transfer printing processes for high-resolution patterning of AgNW networks, which include (i) vacuum filtration of AgNW solution on a thin PI shadow mask and (ii) transfer printing of the patterned AgNWs from the AAO template onto target substrates, such as Si, glass, and polyethylene terephthalate (PET). Here, we used 0.05 wt% AgNW solution with an average length of 25 ± 5 μm and an average diameter of 32 ± 5 nm (for more detail structural characteristic of AgNW, please refer to the experimental section and Figure 3.2). For the fabrication of the patterned PI shadow mask, a PI solution was spin-coated on a Si substrate and cured at 120 °C for 3 h. Subsequently, the PI film was patterned by standard photolithography and reactive ion etching (RIE) processes (Figure 3.3). To separate the PI shadow mask from the Si substrate, we utilized the water assisted peeling-off method, which would effectively protect the shadow mask from any external damage (Figure 3.4a).[28, 29] Next, the PI shadow mask was picked up by the AAO template from the surface of the water for conformal attachment (Figure 3.4b). After the AAO template with the PI shadow mask was placed on the filtration plate, the PI shadow mask was strongly attached to the AAO template using the vacuum process (Figure 3.4c). A few drops of AgNW solution was added after filling the funnel with deionized

(DI) water (Figure 3.4d). The AgNWs would be easily stacked inside the patterns of the shadow mask by the strong water flow during the vacuum filtration process. Figures 3.1b–d show the stacked AgNWs inside the pattern of the shadow mask after the filtration process. Most of the AgNWs were assembled within the pattern area, except for a very few AgNWs at the edge of the pattern. Between the patterned windows, no AgNWs could be found (Figure 3.5b). As the PI shadow mask was removed, the patterned AgNWs would remain on the AAO template (Figure 3.1e). This strategy could provide a very cost-effective and efficient way of patterning of AgNWs as the shadow mask and AAO template could be reused. Furthermore, the number of fabrication steps was reduced and no AgNW solution was wasted. Figure 3.6 shows the optical microscopy (OM) image of the PI shadow mask after the filtration process and the scanning electron microscopy (SEM) image of the AAO template after the transfer printing of the AgNW networks.

To demonstrate the application of the above developed patterned AgNW networks as electrodes of optoelectronic devices, we transferred the AgNW networks onto arbitrary substrates (e.g., Si, glass, and PET). In the transfer printing process, after the AgNW networks were dried on the AAO template, the patterned AgNW networks were attached on the PDMS stamp. Next, a small amount of DI water was sprayed on the back side of the AAO template to separate the AgNW networks from the AAO template. The water, thus sprayed was passed through the hole to the front side; it would penetrate between the AgNW networks and the AAO template.[29-31] Then, the resultant buoyant force of the water would act on the AgNW networks on the PDMS stamp, thus causing the AgNW networks to be detached from the AAO template and attached on the PDMS stamp (Figures 3.1 and 3.4g).[31, 32] The AgNW networks on the PDMS stamp could be easily transferred onto Si (Figure 3.1g) or PET (Figure 3.4h) substrates using the liquid bridge method.[33, 34] Figure 3.1e–g shows the OM and SEM images for each step of transfer printing of the patterned AgNW networks. It should be noted that the AgNW networks were maintained well during the transfer printing processes from the AAO template to the Si or PET substrate. Figure 3.7 shows the surface morphology of transferred AgNW networks on the Si substrate using atomic force microscopy (AFM) analysis, indicating similar value (33.25 nm) of the root-mean-square roughness compared to spin-coated AgNWs networks.[16] Moreover, our method was also able to fabricate a variety of sophisticated patterns of AgNWs, such as a butterfly, numbers, and letters on the Si substrate (Figures 3.8a–e). While patterning AgNWs *via* conventional photolithography is limited in achieving reduced pattern sizes owing to the scattering of light by the AgNW networks,[19, 35] in our method, the high-resolution assembly of AgNWs along the pattern edge of the shadow mask could remain clear because of the total removal of the AgNWs from the shadow mask (Figure 3.5c, d). Therefore, our method could facilitate a sharp AgNW pattern with approximately 3.5 μm line width (Figures 3.8f and 3.9). Moreover, our strategy possesses additional advantages, such as easy thickness control of the AgNW electrodes, ability to accommodate various flexible substrates, as well as patterning and combination of various low dimensional materials. Figures 3.10 and 3.11 show the density and optical transmittance of the

AgNW networks based on the amounts of AgNW solutions. Figure 3.12 showed AFM images and height analysis of AgNW networks, indicating that the thickness of the AgNW networks could be simply controlled by controlling the amount of AgNW solutions. Here, the sheet resistance of AgNW networks with 10 and 40 μL solution are 2.615 and 0.746 Ω/sq, respectively. Figure 3.13 shows the sheet resistance changes depend on the post-annealing temperature, which indicates the AgNW network is thermally stable up to 150 °C. Figure 3.14 shows the transferred AgNW networks on glass, PDMS and PET substrates, thus demonstrating their potential applications in the fabrication of various optoelectronic devices, such as flexible and/or transparent TFTs, photodetectors, and LEDs.

Previously, combined assembly of different low-dimensional conductive materials, for example, AgNWs, CNT, and graphene has been investigated to improve the electrical properties and prevent the conductive materials from oxidation through capping with air-stable materials, such as reduced graphene oxide (rGO).[36, 37] Our method allows the combined assembly of AgNWs and CNTs and stacking of rGO sheets on top of the AgNW networks through sequential filtration of each solution and transfer printing processes. Figure 3.15a, b shows patterned graphene on a Si substrate fabricated using our method, which demonstrates its capability to pattern various low-dimensional materials. Figure 3.15c shows an AgNW network covered with rGO sheets after the sequential filtration of AgNWs and rGO solutions, which demonstrates that the AgNW/rGO film retained sharp pattern edges (Figure 3.15c). Figure 3.15d shows the Raman mapping image for the G-band of rGO at the edge of the AgNW/rGO film. Similarly, Figure 3.15e shows the Raman shift of the AgNW/rGO film with D, G, and 2D peaks at 1349, 1590, and 2688 cm^{-1}, respectively. Furthermore, Figure 3.15f shows the SEM image of the AgNW/rGO film, indicating a uniform coverage of the rGO sheets on the AgNW network. In addition, we confirmed that a combination network of AgNW and CNT was also possible through sequential filtration (Figure 3.16 and 3.17). Hence, the combination and stacking of different low-dimensional materials are possible through a sequential filtration process, which can be applied to various device structures.

Next, to demonstrate the potential applications of our technique in optical devices, we compared the characteristics of the Ag film and AgNW electrodes for planar Metal–Semiconductor–Metal (MSM) Si photodetectors. For fabricating the former, a 200 nm thick Ag film for the anode and cathode, deposited by thermal evaporation on top of the Si substrate, was patterned using the standard photolithography and lift-off process. The insets in Figure 3.18a, b show the Ag film and the AgNW electrodes, wherein the channel length and width were 50 and 200 μm, respectively. Figure 3.18a, b shows the dark current and photocurrent characteristics under a specific light illumination (λ = 850 nm; P_{light} = 2.2 mW/cm^2). The dark current of the Si photodetector with the Ag film electrode was 3.2×10^{-5} A at a bias voltage of 5 V, which was considerably higher than that of the Si photodetector with the AgNW electrode (3.24×10^{-10} A). Similarly, the photocurrent of the photodetector with the Ag film was 3.3×10^{-5} A at the same bias voltage of 5 V, which was again higher than that of the photodetector based on the AgNW

electrode (6.0×10^{-7} A). Although the photocurrent of the Si photodetector with the AgNW electrode was lower than that of the photodetector with the Ag film, the on/off ratio of the former was 1.86×10^{3}, which was much higher than that of the latter with a ratio of 1.04. Figure 3.18c, d shows the photo-switching behaviors of these two photodetectors. The AgNW electrode exhibited a superior and stable photo-switching behavior compared to the Ag film electrode (Figure 3.18c). The superior photo-switching and low dark current behavior of AgNW electrodes could be mainly attributed to the following three factors. Firstly, polyvinylpyrrolidone (PVP) coating around the AgNW acted as the barrier between the Si substrate and AgNW (Figure 3.19a).[38] Therefore, under the bias condition, electrons (and holes) are mostly blocked by the PVP barrier in the dark state (Figure 3.19b). But when light illuminated, electrons (and holes) accumulated by the photo-generated electrons-hole pair are tunneled through the PVP barrier under the illumination of light (Figure 3.19c). Secondly, the actual contact area between the AgNW electrode and the Si substrate was lower than that in the Ag film electrode owing to the round shape of the AgNWs and vacant area in the conductive AgNW network. These two factors resulted a low dark current. Finally, as the AgNW network was semi-transparent, the effective photocurrent-generated area was wider than that of the Ag film electrode, thus causing an increase in the photocurrent, resulting in a high optical on/off ratio. Figure 3.18e, f shows the photocurrent mapping data of these two photodetectors, which were measured by scanning a 532 nm laser from drain to source at zero-bias voltage. The photocurrent was not generated when the laser was on top of the Ag film electrode (Figure 3.18e); however, high photocurrent was generated on the top of the AgNW electrode. Interestingly, the photocurrent in the AgNW area was even higher than that in the Si semiconductor area (Figure 3.18f). This result could be attributed to the small electron-hole recombination in the area of the AgNW electrode owing to the short current path at the interface between the AgNW electrode and the semiconductor interface. Therefore, the AgNW networks were very useful as electrodes for high performance photodetectors with low-power consumption.

Furthermore, the AgNW networks exhibited excellent optical transparency and mechanical flexibility. We fabricated a planar MSM ZnO photodetector with AgNW electrodes on the Norland Optical Adhesives (NOA) substrate (Figure 3.20a). Figure 3.20b shows the optical transmittance spectra of AgNW and Ag film electrodes on the ZnO film (200 nm)/glass substrates. Compared to the AgNW electrode, the Ag film electrode significantly decreased the optical transmittance of the ZnO film. As mentioned earlier, the AgNW electrode had a low photocurrent owing to a low contact area between the AgNW electrode and the active layer. To address this problem, the AgNW electrodes were embedded in the active layer to increase the contact area and path length of the incident light by scattering, and trapping the events for enhanced photocurrent.[9, 39] For incorporating this embedded AgNW electrode into the active layer, the AgNW electrodes were transferred onto a silicon substrate coated with polyvinyl alcohol (PVA) (Figure 3.21). Then, ZnO and NOA films were sequentially coated by radio frequency (RF) sputtering and spin coater, respectively. Finally, the UV photodetector and the Si

substrate were separated by removing the sacrificial PVA layer with DI water after UV-polymerization of the NOA film (Figure 3.22). The UV photodetector with the embedded AgNW electrode on the NOA substrate was semi-transparent (Figure 3.20c). To verify the effect of embedding the AgNW electrode into the active layer, we compared the performances of two types of photodetectors based on embedded and on the top-mounted AgNW electrodes on ZnO films. The band diagram of both structures is the same, and its band diagram and photodetection mechanism are similar to the AgNW based Si-photodetector (Figure 3.23). Figure 3.20d shows the *I–V* curve of the UV photodetectors under dark and illuminated conditions of the UV light (365 nm, 1.56 mW). The UV photodetector with the embedded AgNW electrode showed improved photocurrent performance (approximately 800%) compared to the top AgNW electrode, whereas the dark current performance exhibited similar extremely low values under 60 fA for both the devices. This significant increase in the photocurrent for the embedded AgNW electrode was due to an increased contact area of the AgNW electrodes and light scattering and trapping events. When the AgNWs were embedded in the ZnO film, the contact area between the AgNW electrodes and the ZnO film increased, which increased the photocurrent in the device. In addition, the incident light was scattered on the surface of the AgNW electrode and was trapped in the stacked AgNWs inside the ZnO film, resulting in a significantly enhanced light absorption. The key figure of merit, photo-responsivity (R_λ), and detectivity (D^*), in two types of the photodetector, was used for the standard of comparison. Responsivity is defined as the photocurrent according to the power of the incident light in the unit area, and detectivity represents the ability to distinguish a signal from noise and facilitates comparison with other devices. The responsivity and detectivity are calculated by the following equations[40, 41]

$$R(\lambda) = \frac{J_{\mathrm{ph}}}{P_{\mathrm{light}}}\ [\mathrm{A/W}] \qquad (1)$$

$$D^* = \frac{\sqrt{A}}{NEP} \cong \frac{R(\lambda)}{\sqrt{2qJ_{\mathrm{d}}}}\ [\mathrm{cm\ Hz^{1/2}/W}] \qquad (2)$$

where λ is the wavelength, J_{ph} is photocurrent density, P_{light} is optical power, A is the effective area of detector, NEP is noise-equivalent power, q is the electron charge, and J_{d} is dark current density. The responsivity and detectivity of the UV photodetector with the embedded AgNW electrode were 1.05×10^{-2} A/W and 7.53×10^{11} cm Hz$^{1/2}$/W at a bias voltage of 20 V, respectively. It shows superior performance than the UV photodetector with the top AgNW electrode, which is responsivity of 1.31×10^{-3} A/W and detectivity of 9.40×10^{10} cm Hz$^{1/2}$/W .) (Here, we calculated by considering only the shot noise for the detectivity.) The photo-responsive on/off ratio of the UV photodetectors with the embedded AgNW electrode showed a very high value of 3.93×10^4 at a bias voltage of 20 V. Figures 3.20e and 3.24 show the photo-switching behavior and photo-response speed under UV light at a bias voltage of 2 V for the embedded AgNW electrode. The repeated switching behavior was well-retained with a stable and reproducible current and fast photo-response time

(approximately 9.1 ms of rise time and 18.3 ms of decay time). In general, ZnO-based photodetectors have a slow response speed and unstable reproducibility because charge carriers by the adsorption and desorption of O_2 and/or H_2O on the ZnO surface contributes to the operation of the device.[42] But, in our device, the affection of charge carriers by the adsorption and desorption processes do not significantly contribute to the operation of the device because the low-density charge carriers are blocked by the PVP barrier layer. Thus, the tunneling mechanism with the PVP barrier layer leads to fast photo-response time.[43] Moreover, our UV photodetector could be operated well even under severe bending conditions. Figure 3.25a, b shows the UV photodetector array on the tip of a glass pipette with a radius of approximately 770 μm. The AgNWs were properly embedded in the ZnO film even under a highly bent condition (Figures 3.25b and 3.26). The highly bent UV photodetector exhibited a photocurrent approximately two times lower than that in the flat state (green dots, as shown in Figure 3.25c). This could be attributed to the multiple factors, such as reduced light collection area on the curved surface and increased reflection of light at the surface due to strongly bent geometry of the photodetector. Figure 3.25d shows the photocurrent variation after the device was bent repeatedly with a radius of 0.5 cm. The photocurrent after 500 bending cycles did not show any noticeable change compared to the initial value. In terms of the performances, our device has results comparable to those of other flexible UV photodetectors (Table 3.1). Especially, the PVP layer around AgNWs acts as the barrier at the interface and embedded structure increased the contact area, resulting in high on/off ratio and fast response time with a tunneling mechanism. In addition, our photodetector could be transferred to various substrates, such as leaf and safety glasses (Figures 3.20c and 3.27), which could find diverse applications in wearable sensors and augmented reality.

3.4 Conclusion

We have developed a fine-patterning technique of AgNWs on various substrates using simple vacuum filtration and transfer printing processes. This technique has provided a very simple and cost-effective fabrication method for fine patterning of AgNW electrodes for applications in transparent and flexible optoelectronic devices. This patterning technique could be applied to other nanomaterials, such as CNTs, graphene, and a combination of nanomaterials to realize highly flexible and transparent optoelectronic devices. As a proof-of-concept demonstration, we fabricated a Si-based photodetector and a ZnO-based UV photodetector. The Si-based photodetector with the AgNW electrode exhibited an excellent on/off ratio and a low dark current compared to the Ag film electrode. The UV photodetector with an embedded AgNW electrode under an active semiconductor showed an enhanced photocurrent that was 800 % higher than that of the top AgNW electrode. The proposed patterning technique of AgNWs has a significant potential for applications in the development of flexible and transparent optoelectronic devices.

3.5 References

(1) Yoon, J.; Baca, A. J.; Park, S. I.; Elvikis, P.; Geddes, J. B.; Li, L. F.; Kim, R. H.; Xiao, J. L.; Wang, S. D.; Kim, T.-H.; Motala, M. J.; Ahn, B. Y.; Duoss, E. B.; Lewis, J. A.; Nuzzo, R. G.; Ferreira, P. M.; Huang, Y. G.; Rockett, A.; Rogers, J. A., Ultrathin Silicon Solar Microcells for Semitransparent, Mechanically Flexible and Microconcentrator Module Designs. *Nat. Mater.* **2008,** *7*, 907-915.

(2) Liang, J.; Li, L.; Niu, X.; Yu, Z.; Pei, Q., Elastomeric Polymer Light-Emitting Devices and Displays. *Nat. Photonics* **2013,** *7*, 817-824.

(3) Hossain, M.; Kumar, G. S.; Barimar Prabhava, S. N.; Sheerin, E. D.; McCloskey, D.; Acharya, S.; Rao, K. D. M.; Boland, J. J., Transparent, Flexible Silicon Nanostructured Wire Networks with Seamless Junctions for High-Performance Photodetector Applications. *ACS Nano* **2018,** *12*, 4727-4735.

(4) Hoffman, R. L.; Norris, B. J.; Wager, J. F., ZnO-Based Transparent Thin-Film Transistors. *Appl. Phys. Lett.* **2003,** *82*, 733-735.

(5) Kumar, A.; Zhou, C., The Race To Replace Tin-Doped Indium Oxide: Which Material Will Win? *ACS Nano* **2010,** *4*, 11-14.

(6) Lee, J. Y.; Connor, S. T.; Cui, Y.; Peumans, P., Solution-Processed Metal Nanowire Mesh Transparent Electrodes. *Nano Lett.* **2008,** *8*, 689-692.

(7) Chen, Y. T.; Carmichael, R. S.; Carmichaele, T. B., Patterned, Flexible, and Stretchable Silver Nanowire/Polymer Composite Films as Transparent Conductive Electrodes. *ACS Appl. Mater. Interfaces* **2019,** *11*, 31210-31219.

(8) Ahn, Y.; Lee, H.; Lee, D.; Lee, Y., Highly Conductive and Flexible Silver Nanowire-Based Microelectrodes on Biocompatible Hydrogel. *ACS Appl. Mater. Interfaces* **2014,** *6*, 18401-18407.

(9) Wang, B.-Y.; Yoo, T.-H.; Lim, J. W.; Sang, B.-I.; Lim, D.-S.; Choi, W. K.; Hwang, D. K.; Oh, Y.-J., Enhanced Light Scattering and Trapping Effect of Ag Nanowire Mesh Electrode for High Efficient Flexible Organic Solar Cell. *Small* **2015,** *11*, 1905-1911.

(10) Garnett, E. C.; Cai, W.; Cha, J. J.; Mahmood, F.; Connor, S. T.; Greyson Christoforo, M.; Cui, Y.; McGehee, M. D.; Brongersma, M. L., Self-Limited Plasmonic Welding of Silver Nanowire Junctions. *Nat. Mater.* **2012,** *11*, 241-249.

(11) Lee, P.; Ham, J.; Lee, J.; Hong, S.; Han, S.; Suh, Y. D.; Lee, S. E.; Yeo, J.; Lee, S. S.; Lee, D.; Ko, S. H., Highly Stretchable or Transparent Conductor Fabrication by a Hierarchical Multiscale Hybrid Nanocomposite. *Adv. Funct. Mater.* **2014,** *24*, 5671-5678.

(12) Deng, B.; Hsu, P. C.; Chen, G.; Chandrashekar, B. N.; Liao, L.; Ayitimuda, Z.; Wu, J.; Guo, Y.; Lin, L.; Zhou, Y.; Aisijiang, M.; Xie, Q.; Cui, Y.; Liu, Z.; Peng, H., Roll-to-Roll Encapsulation of Metal Nanowires between Graphene and Plastic Substrate for High-Performance Flexible

Transparent Electrodes. *Nano Lett.* **2015,** *15*, 4206-4213.

(13) Lai, Y.-T.; Tai, N. H., One-Step Process for High-Performance, Adhesive, Flexible Transparent Conductive Films Based on p-Type Reduced Graphene Oxides and Silver Nanowires. *ACS Appl. Mater. Interfaces* **2015,** *7*, 18553-18559.

(14) Hu, L.; Kim, H. S.; Lee, J.-Y.; Peumans, P.; Cui, Y., Scalable Coating and Properties of Transparent, Flexible, Silver Nanowire Electrodes. *ACS Nano* **2010,** *4*, 2955-2963.

(15) Zhou, K. L.; Han, C. B.; Li, C. F.; Jiu, J.; Yang, Y.; Li, L.; Wang, H.; Liu, J. B.; Liu, Z. Q.; Yan, H.; Suganuma, K., Highly Stable Transparent Conductive Electrodes Based on Silver-Platinum Alloy-Walled Hollow Nanowires for Optoelectronic Devices. *ACS Appl. Mater. Interfaces* **2018,** *10*, 36128-36135.

(16) Kang, S.; Kim, T.; Cho, S.; Lee, Y.; Choe, A.; Walker, B.; Ko, S.-J.; Kim, J. Y.; Ko, H., Capillary Printing of Highly Aligned Silver Nanowire Transparent Electrodes for High-Performance Optoelectronic Devices. *Nano Lett.* **2015,** *15*, 7933-7942.

(17) Yang, L. Q.; Zhang, T.; Zhou, H. X.; Price, S. C.; Wiley, B. J.; You, W., Solution-Processed Flexible Polymer Solar Cells with Silver Nanowire Electrodes. *ACS Appl. Mater. Interfaces* **2011,** *3*, 4075-4084.

(18) Liu, S. Y.; Ho, S. H.; So, F., Novel Patterning Method for Silver Nanowire Electrodes for Thermal-Evaporated Organic Light Emitting Diodes. *ACS Appl. Mater. Interfaces* **2016,** *8*, 9268-9274.

(19) Martinez, V.; Stauffer, F.; Adagunodo, M. O.; Forro, C.; Voros, J.; Larmagnac, A., Stretchable Silver Nanowire-Elastomer Composite Microelectrodes with Tailored Electrical Properties. *ACS Appl Mater Interfaces* **2015,** *7*, 13467-13475.

(20) Cann, M.; Large, M. J.; Henley, S. J.; Milne, D.; Sato, T.; Chan, H.; Jurewicz, I.; Dalton, A. B., High Performance Transparent Multi-Touch Sensors Based on Silver Nanowires. *Mater. Today Commun.* **2016,** *7*, 42-50.

(21) Madaria, A. R.; Kumar, A.; Ishikawa, F. N.; Zhou, C., Uniform, Highly Conductive, and Patterned Transparent Films of a Percolating Silver Nanowire Network on Rigid and Flexible Substrates Using a Dry Transfer Technique. *Nano Res.* **2010,** *3*, 564-573.

(22) Kim, J.; Lee, S. H.; Kim, H.; Kim, S. H.; Park, C. E., 3D Hollow Framework Silver Nanowire Electrodes for High-Performance Bottom-Contact Organic Transistors. *ACS Appl. Mater. Interfaces* **2015,** *7*, 14272-14278.

(23) Ko, Y.; Kim, J.; Kim, D.; Yamauchi, Y.; Kim, J. H.; You, J., A Simple Silver Nanowire Patterning Method Based on Poly(Ethylene Glycol) Photolithography and Its Application for Soft Electronics. *Sci. Rep.* **2017,** *7*, 2282.

(24) Yang, B.-R.; Cao, W.; Liu, G.-S.; Chen, H.-J.; Noh, Y.-Y.; Minari, T.; Hsiao, H.-C.; Lee, C.-Y.; Shieh, H.-P.; Liu, C., Microchannel Wetting for Controllable Patterning and Alignment of Silver

Nanowire with High Resolution. *ACS Appl. Mater. Interfaces* **2015,** *7*, 21433-21441.

(25) Choo, D. C.; Bae, S. K.; Kim, T. W., Flexible, Transparent Patterned Electrodes Based on Graphene Oxide/Silver Nanowire Nanocomposites Fabricated Utilizing an Accelerated Ultraviolet/Ozone Process to Control Silver Nanowire Degradation. *Sci. Rep.* **2019,** *9*, 5527.

(26) Langley, D.; Giusti, G.; Mayousse, C.; Celle, C.; Bellet, D.; Simonato, J.-P., Flexible Transparent Conductive Materials Based on Silver Nanowire Networks: a Review. *Nanotechnology* **2013,** *24*, 452001.

(27) Pradel, K. C.; Sohn, K.; Huang, J., Cross-Flow Purification of Nanowires. *Angew. Chem. Int. Ed.* **2011,** *50*, 3412-3416.

(28) Li, H.; Wu, J. M. T.; Huang, X.; Yin, Z. Y.; Liu, J. Q.; Zhang, H., A Universal, Rapid Method for Clean Transfer of Nanostructures onto Various Substrates. *ACS Nano* **2014,** *8*, 6563-6570.

(29) Gurarslan, A.; Yu, Y. F.; Su, L. Q.; Yu, Y. L.; Suarez, F.; Yao, S.; Zhu, Y.; Ozturk, M.; Zhang, Y.; Cao, L. Y., Surface-Energy-Assisted Perfect Transfer of Centimeter-Scale Mono layer and Few-Layer MoS_2 Films onto Arbitrary Substrates. *ACS Nano* **2014,** *8*, 11522-11528.

(30) Xiong, W. W.; Liu, H. L.; Chen, Y. Z.; Zheng, M. L.; Zhao, Y. Y.; Kong, X. B.; Wang, Y.; Zhang, X. Q.; Kong, X. Y.; Wang, P. F.; Jiang, L., Highly Conductive, Air-Stable Silver Nanowire@Iongel Composite Films toward Flexible Transparent Electrodes. *Adv. Mater.* **2016,** *28*, 7167-7172.

(31) Kim, B. S.; Pyo, J. B.; Son, J. G.; Zi, G.; Lee, S.-S.; Park, J. H.; Lee, J., Biaxial Stretchability and Transparency of Ag Nanowire 2D Mass-Spring Networks Prepared by Floating Compression. *ACS Appl. Mater. Interfaces* **2017,** *9*, 10865-10873.

(32) Lai, S.; Jeon, J.; Song, Y.-J.; Lee, S., Water-Penetration-Assisted Mechanical Transfer of Large-Scale Molybdenum Disulfide onto Arbitrary Substrates. *RSC Adv.* **2016,** *6*, 57497-57501.

(33) Um, D.-S.; Lee, Y.; Lim, S.; Park, S.; Lee, H.; Ko, H., High-Performance MoS_2/CuO Nanosheet-on-One-Dimensional Heterojunction Photodetectors. *ACS Appl. Mater. Interfaces* **2016,** *8*, 33955-33962.

(34) Hwang, J. K.; Cho, S.; Dang, J. M.; Kwak, E. B.; Song, K.; Moon, J.; Sung, M. M., Direct Nanoprinting by Liquid-Bridge-Mediated Nanotransfer Moulding. *Nat. Nanotechnol.* **2010,** *5*, 742-748.

(35) Shin, K.; Park, J. S.; Han, J. H.; Choi, Y.; Chung, D. S.; Kim, S. H., Patterned Transparent Electrode with a Continuous Distribution of Silver Nanowires Produced by an Etching-Free Patterning Method. *Sci. Rep.* **2017,** *7*, 40087.

(36) Liang, J.; Li, L.; Tong, K.; Ren, Z.; Hu, W.; Niu, X.; Chen, Y.; Pei, Q., Silver Nanowire Percolation Network Soldered with Graphene Oxide at Room Temperature and Its Application for Fully Stretchable Polymer Light-Emitting Diodes. *ACS Nano* **2014,** *8*, 1590-1600.

(37) Meenakshi, P.; Karthick, R.; Selvaraj, M.; Ramu, S., Investigations on Reduced Graphene Oxide

Film Embedded with Silver Nanowire as A Transparent Conducting Electrode. *Sol. Energ Mat. Sol. Cells* **2014,** *128*, 264-269.

(38) Wang, Y.; Zhang, X. W.; Jiang, Q.; Liu, H.; Wang, D. G.; Meng, J. H.; You, J. B.; Yin, Z. G., Interface Engineering of High-Performance Perovskite Photodetectors Based on PVP/SnO_2 Electron Transport Layer. *ACS Appl. Mater. Interfaces* **2018,** *10*, 6505-6512.

(39) Preston, C.; Xu, Y. L.; Han, X. G.; Munday, J. N.; Hu, L. B., Optical Haze of Transparent and Conductive Silver Nanowire Films. *Nano Res.* **2013,** *6*, 461-468.

(40) Das, K.; Mukherjee, S.; Manna, S.; Ray, S. K.; Raychaudhuri, A. K., Single Si Nanowire (Diameter ≤ 100 nm) Based Polarization Sensitive Near-Infrared Photodetector with Ultra-High Responsivity. *Nanoscale* **2014,** *6*, 11232-11239.

(41) Ji, C. H.; Kim, K. T.; Oh, S. Y., High-Detectivity Perovskite-Based Photodetector Using a Zr-Doped TiO_x Cathode Interlayer. *RSC Adv.* **2019,** *9*, 40023-40023.

(42) Chen, Q.; Ding, H. Y.; Wu, Y. K.; Sui, M. Q.; Lu, W.; Wang, B.; Su, W. M.; Cui, Z.; Chen, L. W., Passivation of Surface States in the ZnO Nanowire with Thermally Evaporated Copper Phthalocyanine for Hybrid Photodetectors. *Nanoscale* **2013,** *5*, 4162-4165.

(43) Kim, D. C.; Jung, B. O.; Lee, J. H.; Cho, H. K.; Lee, J. Y.; Lee, J. H., Dramatically Enhanced Ultraviolet Photosensing Mechanism in a n-ZnO Nanowires/i-MgO/n-Si Structure with Highly Dense Nanowires and Ultrathin MgO Layers. *Nanotechnology* **2011,** *22*, 265506.

(44) Zhang, W.; Jiang, D. Y.; Zhao, M.; Duan, Y. H.; Zhou, X.; Yang, X. J.; Shan, C. C.; Qin, J. M.; Gao, S.; Liang, Q. C.; Hou, J. H., Piezo-Phototronic Effect for Enhanced Sensitivity and Response Range of ZnO Thin Film Flexible UV Photodetectors. *J. Appl. Phys.* **2019***, 125,* 024502.

(45) Dong, Y.; Zou, Y.; Song, J.; Li, J.; Han, B.; Shan, Q.; Xu, L.; Xue, J.; Zeng, H., An All-Inkjet-Printed Flexible UV Photodetector. *Nanoscale* **2017,** *9*, 8580-8585.

(46) Lien, D.-H.; Wang, H.-P.; Chen, S.-B.; Chi, Y.-C.; Wu, C.-L.; Lin, G.-R.; Liao, Y.-C.; He, J.-H., 360° Omnidirectional, Printable and Transparent Photodetectors for Flexible Optoelectronics. *npj Flexible Electron.* **2018***, 2,* 19.

(47) Lim, S.; Um, D.-S.; Ha, M.; Zhang, Q.; Lee, Y.; Lin, Y.; Fan, Z.; Ko, H., Broadband Omnidirectional Light Detection in Flexible and Hierarchical Zno/Si Heterojunction Photodiodes. *Nano Res.* **2017,** *10*, 22-36.

(48) Duan, Y.; Cong, M.; Jiang, D.; Zhang, W.; Yang, X.; Shan, C.; Zhou, X.; li, M.; Li, Q., Zno Thin Film Flexible Uv Photodetectors: Regulation on the Zno/Au Interface by Piezo-Phototronic Effect and Performance Outcomes. *Adv. Mater. Interfaces* **2019**, *6*, 1900470.

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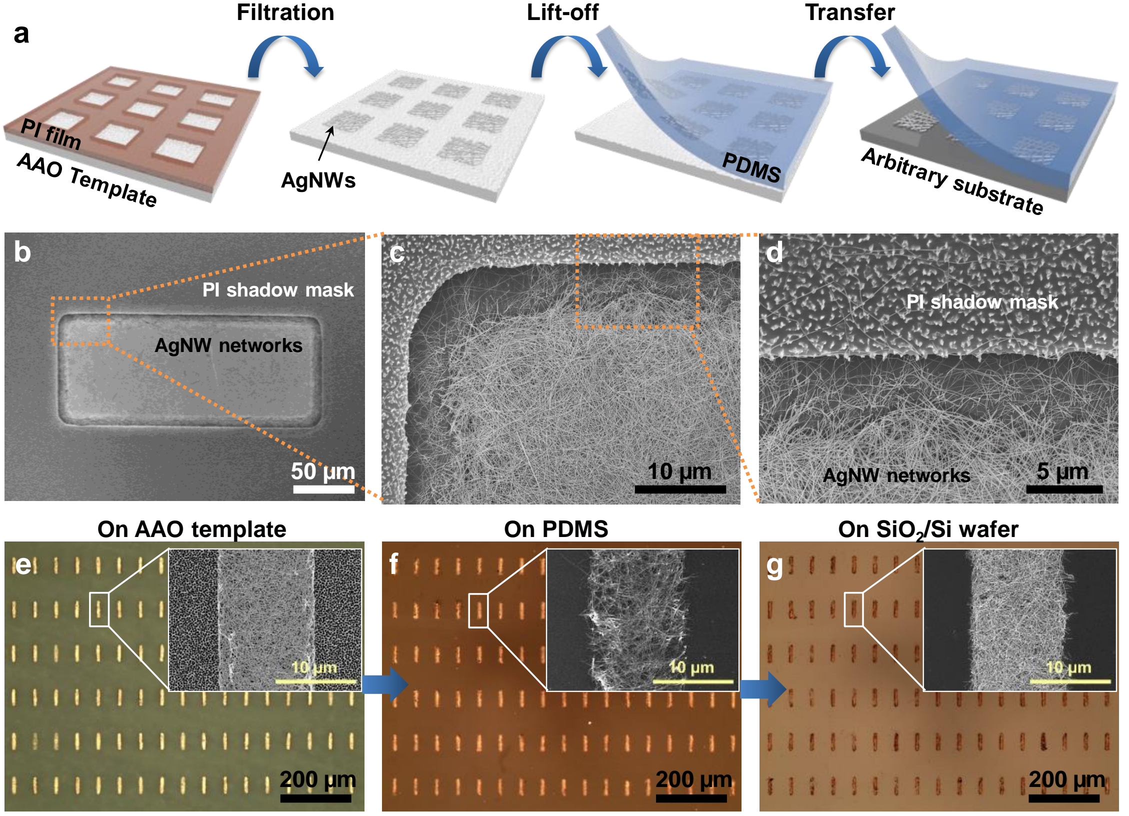

Figure 3.1. (a) Schematic illustration of the AgNW pattering process through vacuum filtration with a PI shadow mask. (b–d) SEM images of patterned AgNW network on AAO template before peeling the PI shadow mask off: (b) whole area, (c) edge part, and (d) magnified image of the edge part of the patterned AgNW network. (e–g) Sequential images of the transfer process of patterned AgNW networks in terms of a series of OM images: (e) on AAO template, (f) on PDMS stamp, and (g) on Si wafer. Insets: SEM images of each step.

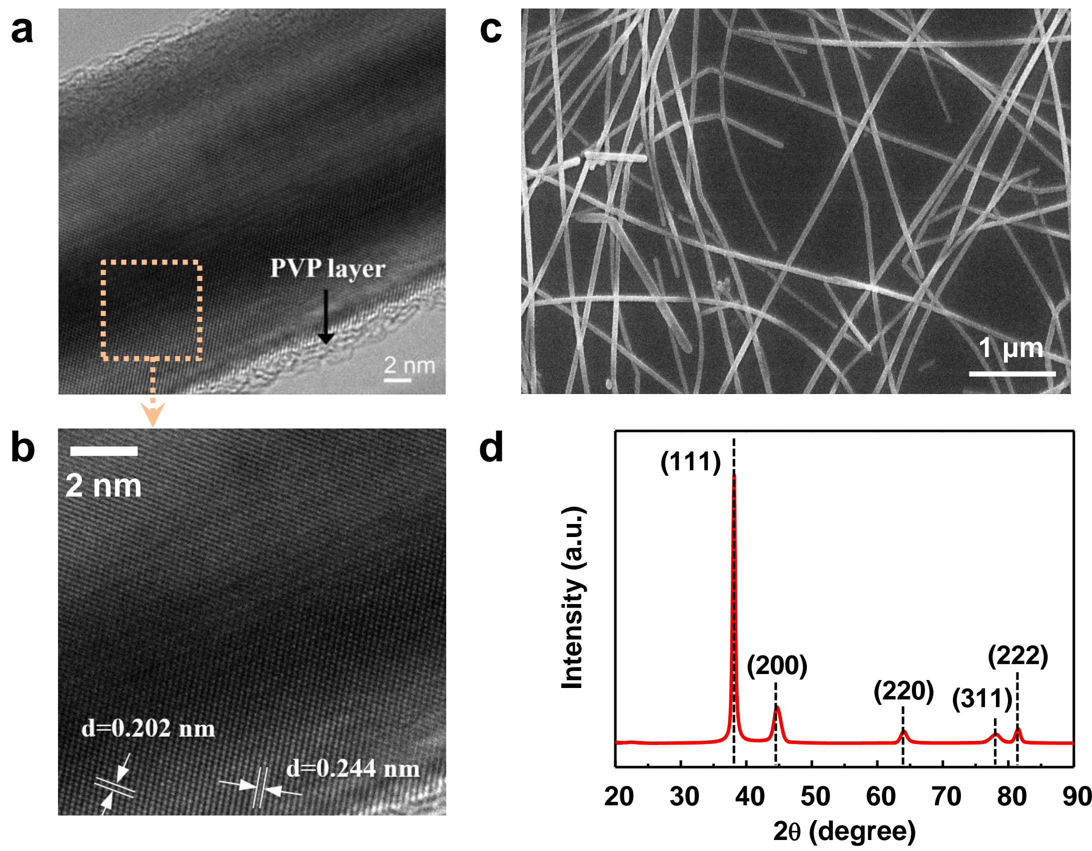

Figure 3.2. (a, b) TEM and (c) HRSEM image of AgNWs. (d) XRD pattern of AgNWs.

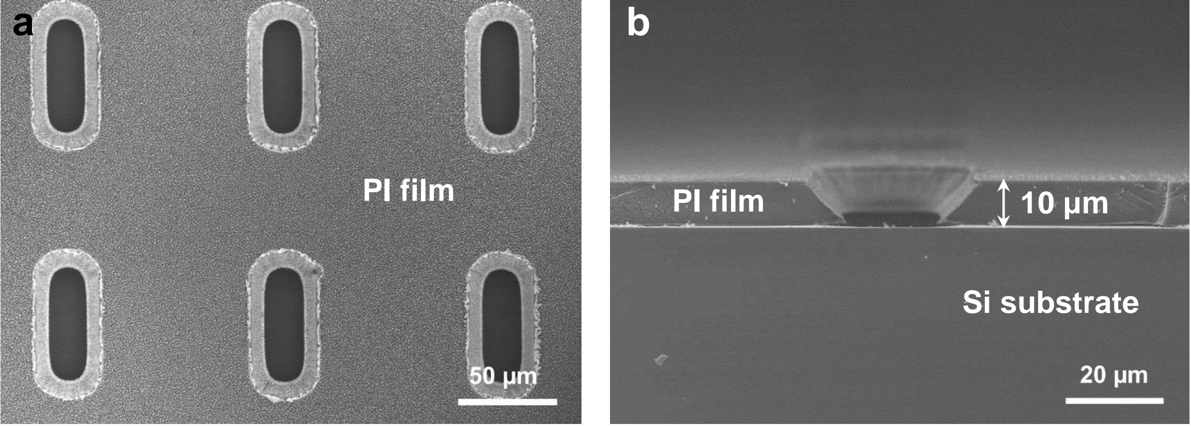

Figure 3.3. SEM images of patterned Polyimide (PI) film after photolithography and dry etching process: (a) top view and (b) side view.

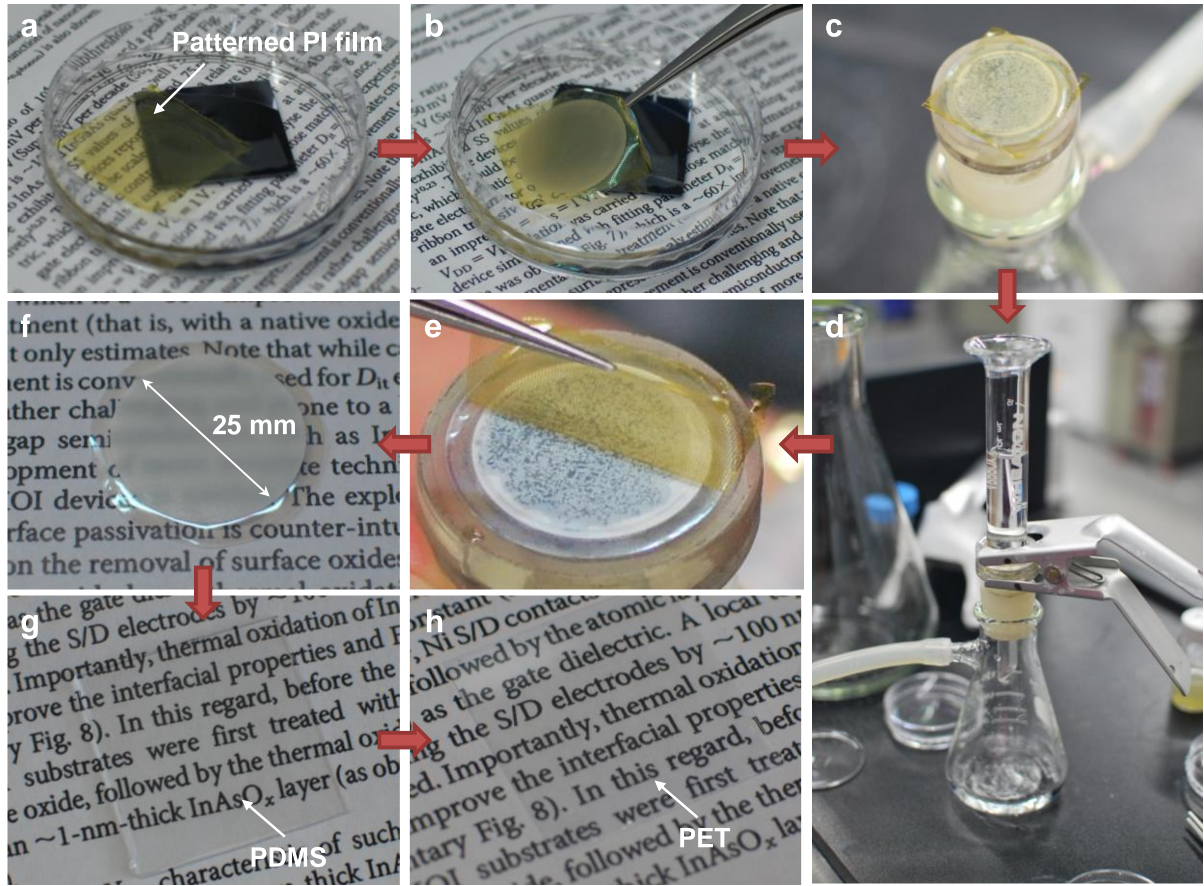

Figure 3.4. A series of optical images of filtration and transfer processes for AgNW patterning: (a) PI shadow mask on the water detached from source substrate. (b) PI shadow mask put on the AAO template. (c) AAO template with PI shadow mask placed on porous plate. (d) AgNW solution added into water filled cylinder filter system. (e) PI shadow mask peeled off from the AAO template. (f) Patterned AgNW networks on AAO template. (g) AgNW networks transferred onto PDMS substrate by stamping process. (h) AgNW networks transferred onto PET substrate by liquid bridge transfer printing.

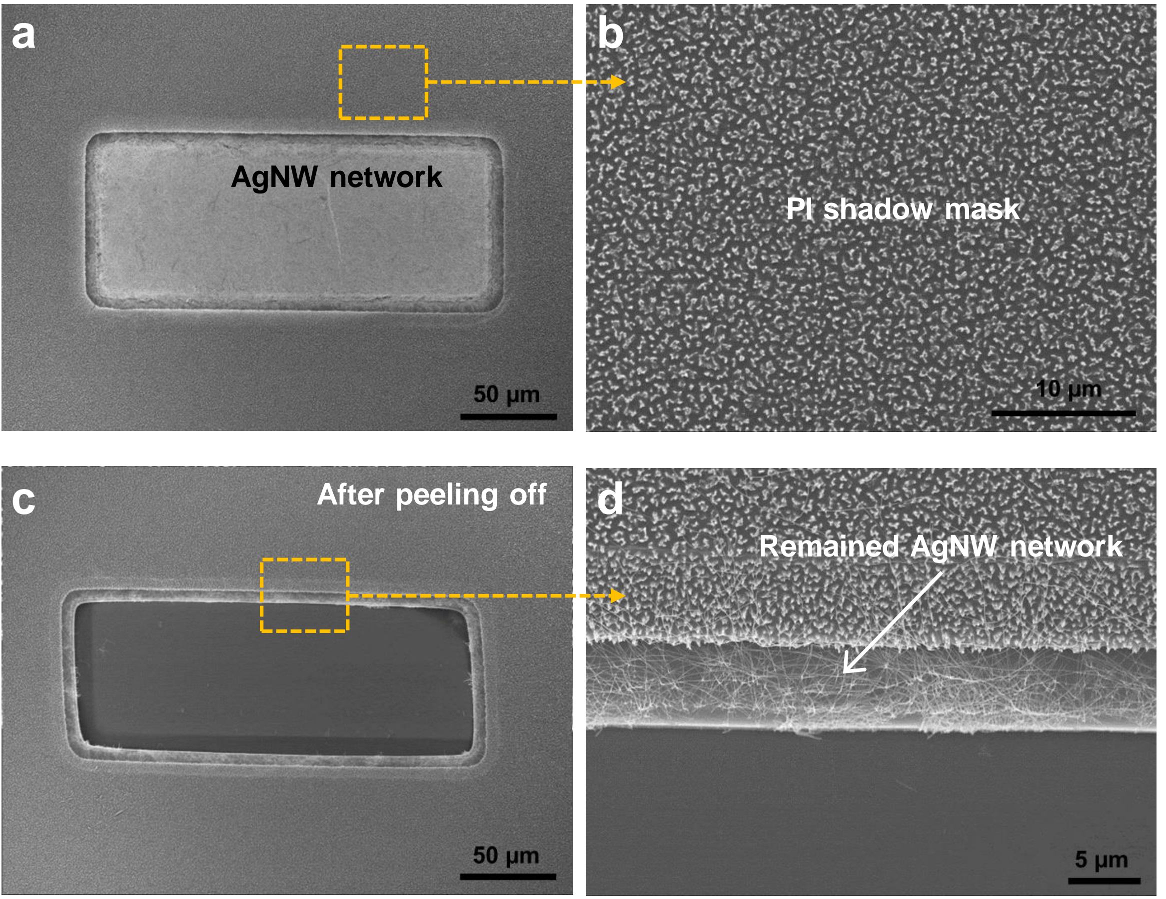

Figure 3.5. (a, b) Scanning electron microscope (SEM) images of patterned AgNW networks on AAO template before peeling the PI shadow mask off: (a) whole area and (b) area between hole patterns of PI shadow mask. (c, d) SEM images of PI shadow mask after peeling off process: (c) whole area and (d) edge part.

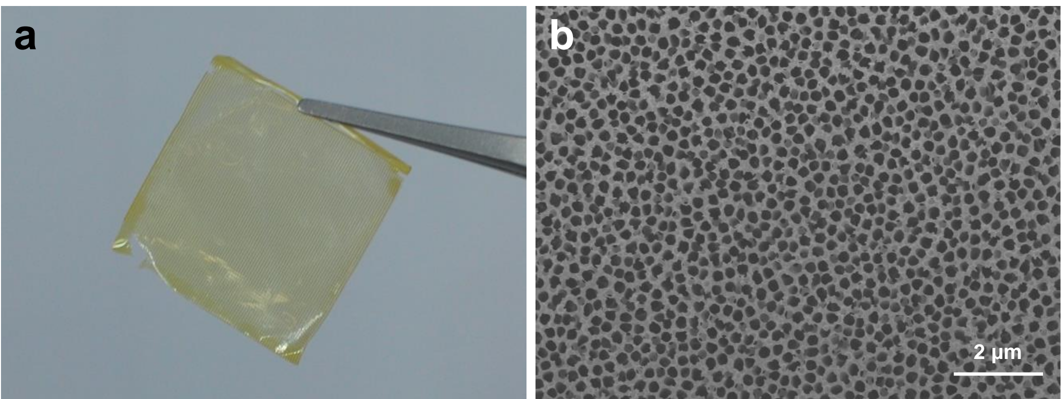

Figure 3.6. (a) Optical image of PI shadow mask after filtration of AgNW solution. (b) SEM image of AAO template after transferring AgNW network onto the other substrate.

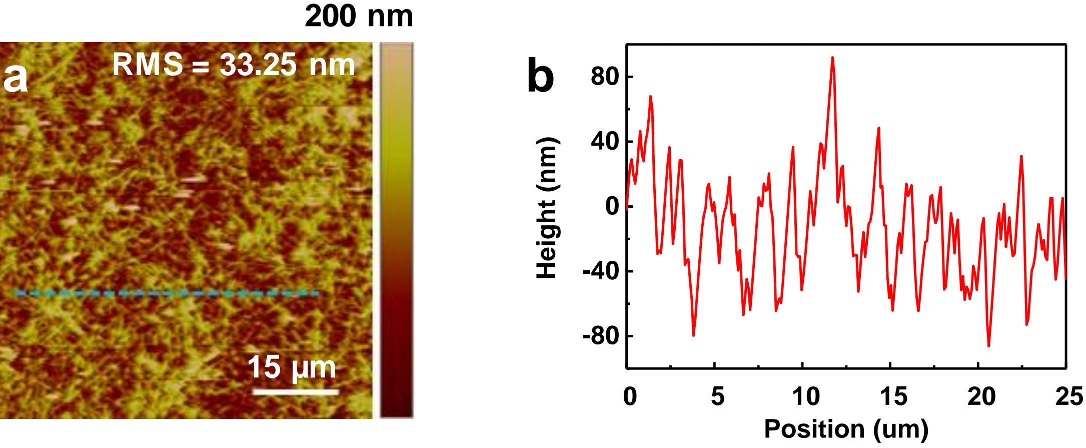

Figure 3.7. (a) AFM image for surface roughness of transferred AgNWs on Si wafer and (b) height analysis of transferred AgNWs on Si wafer.

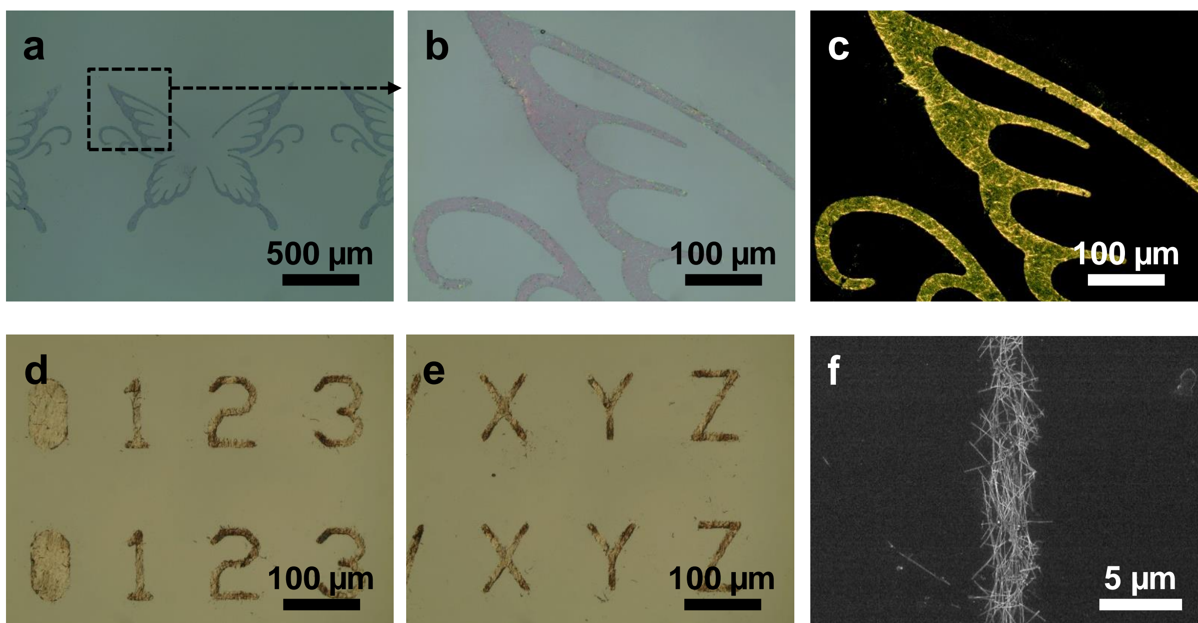

Figure 3.8. OM images of AgNW patterned as (a–c) butterfly shapes, (d) numbers, and (e) letters on the Si substrate. (f) SEM image of patterned AgNW networks on Si substrate with 3.5 μm line width.

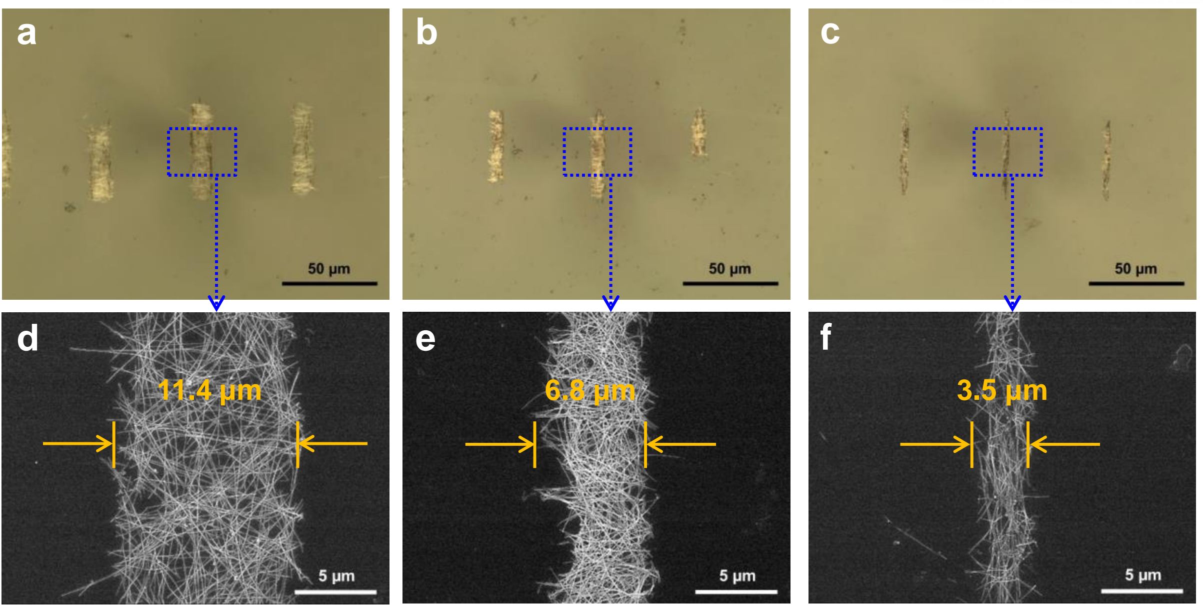

Figure 3.9. (a–c) OM images and (d–f) SEM images of patterned Ag NW networks on Si substrate with different line widths.

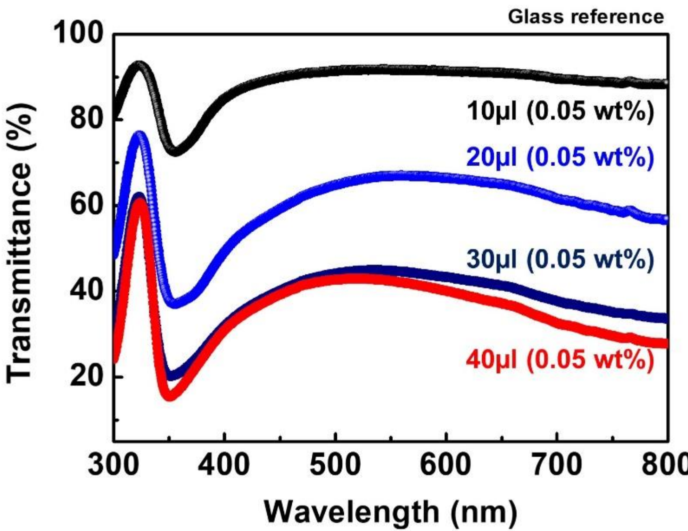

Figure 3.10. Transmittance of patterned AgNW networks on glass for different nanowire densities.

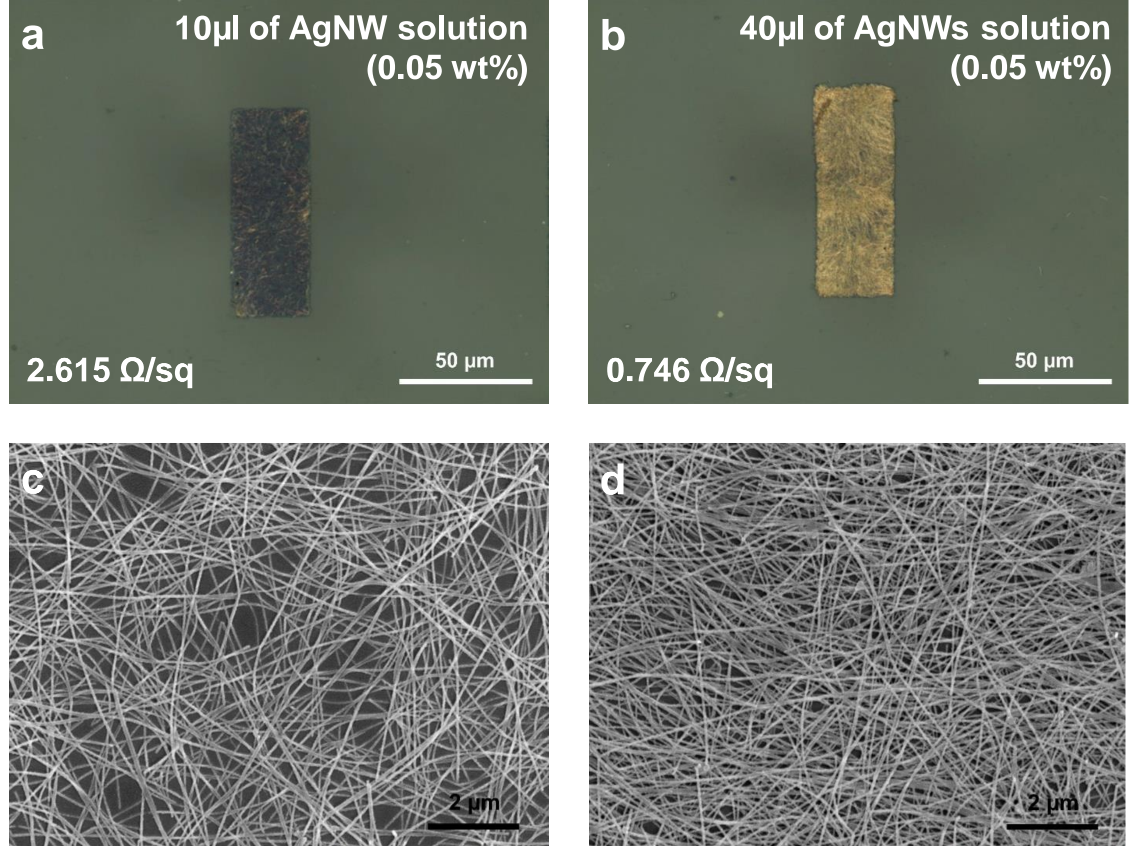

Figure 3.11. (a, b) OM images of patterned AgNW network: (a) 10 µl injection of Ag NW solution and (b) 40 µl injection of Ag NW solution. (c, d) SEM images of patterned AgNW network: (c) 10 µl injection of Ag NW solution and (d) 40 µl injection of AgNW solution.

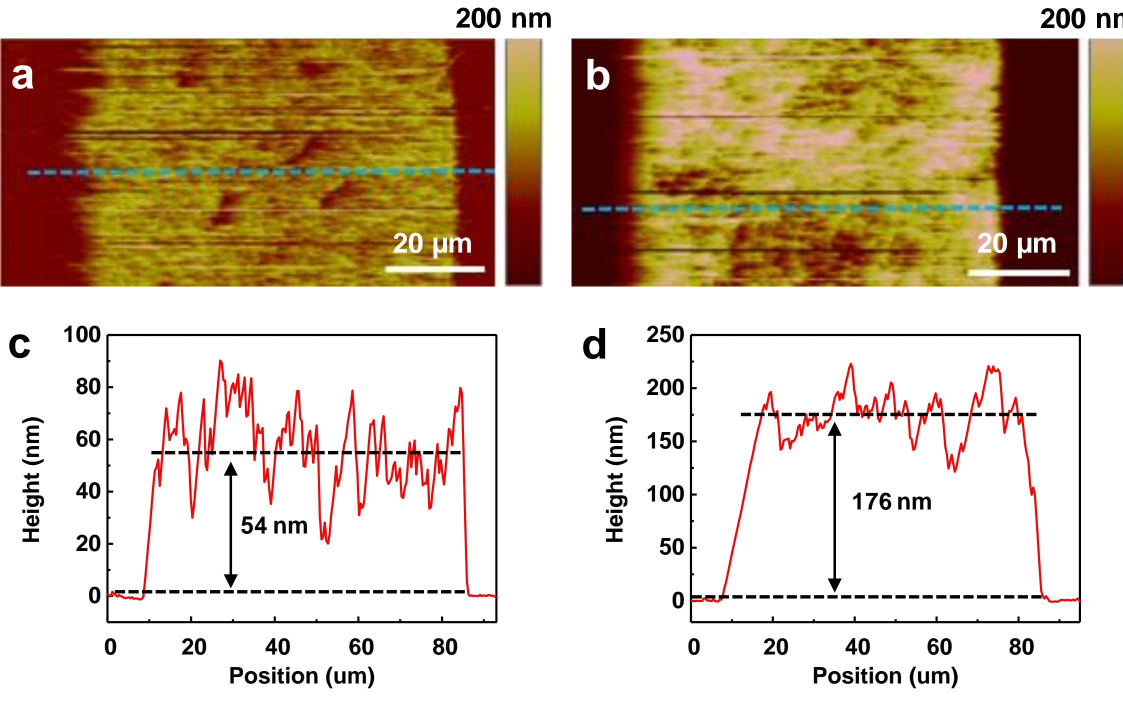

Figure 3.12. (a, b) AFM images of patterned AgNWs network: (a) 10 μl injection case, and (b) 40 μl injection case of Ag NWs solution. (c, d) Height analysis of patterned AgNWs network: (c) 10 μl injection case, and (d) 40 μl injection case of AgNWs solution.

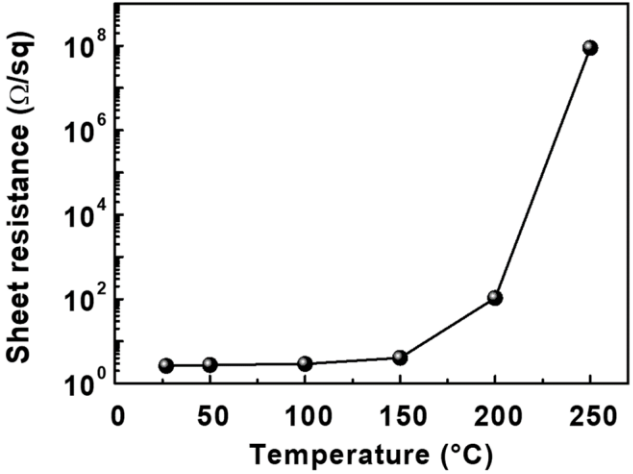

Figure 3.13. Temperature dependent sheet resistance of AgNW networks.

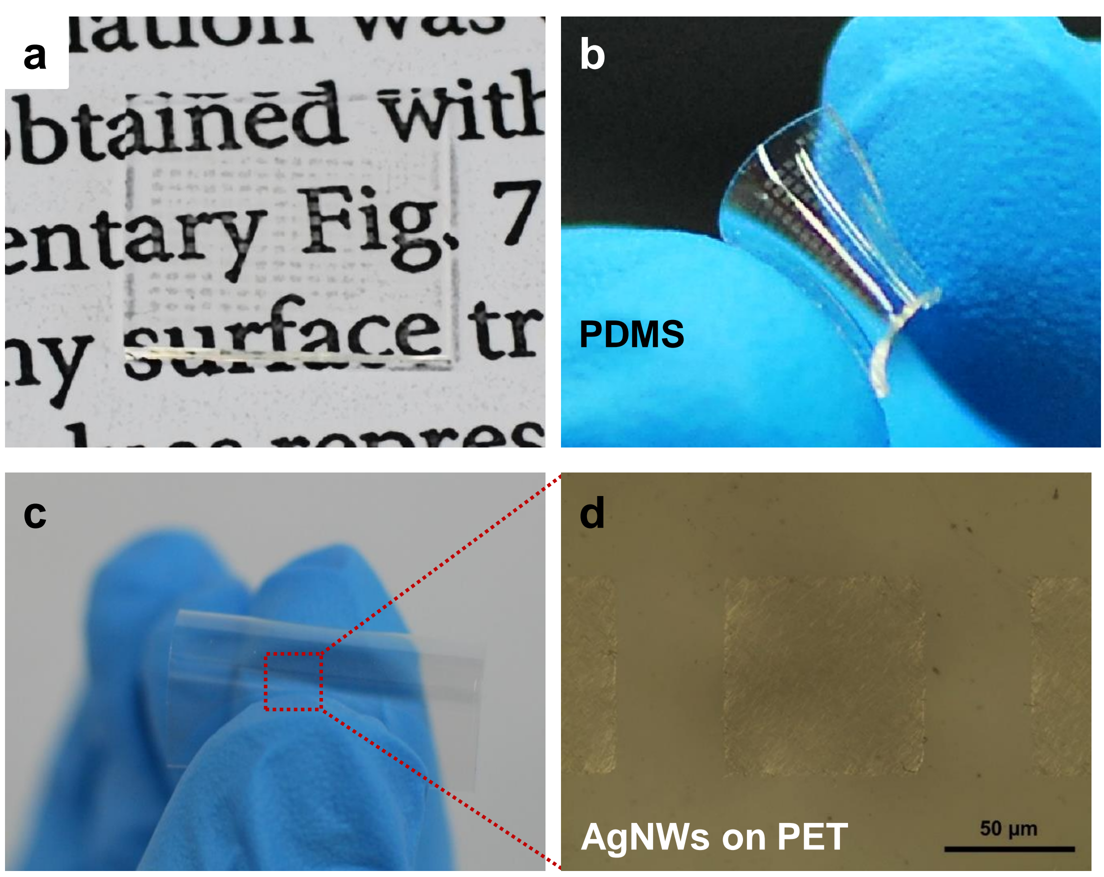

Figure 3.14. (a, b) Optical images and (c, d) OM images of patterned AgNW networks on PET substrate.

Figure 3.15. (a, b) Images of patterned graphene sheets on the Si substrate: (a) OM image and (b) SEM image. (c) SEM image of patterned hybrid structures of AgNW network and rGO through sequential filtration. (d) Raman mapping image of the edge part of patterned hybrid structure. (e) Raman shift of the hybrid structure. (f) SEM image of the AgNW network and rGO hybrid structure enlarged image of the central region of (c).

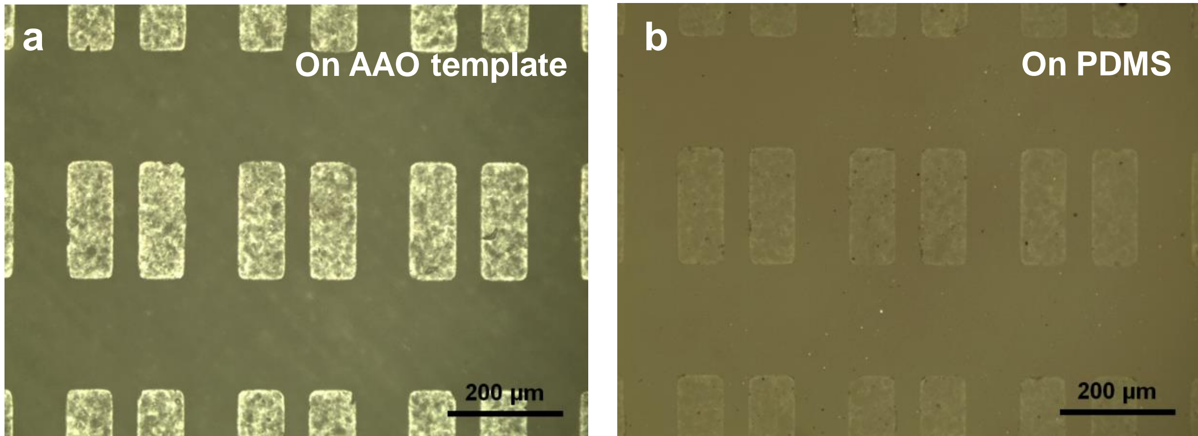

Figure 3.16. (a, b) OM images of patterned graphene sheets on AAO template and PDMS stamp.

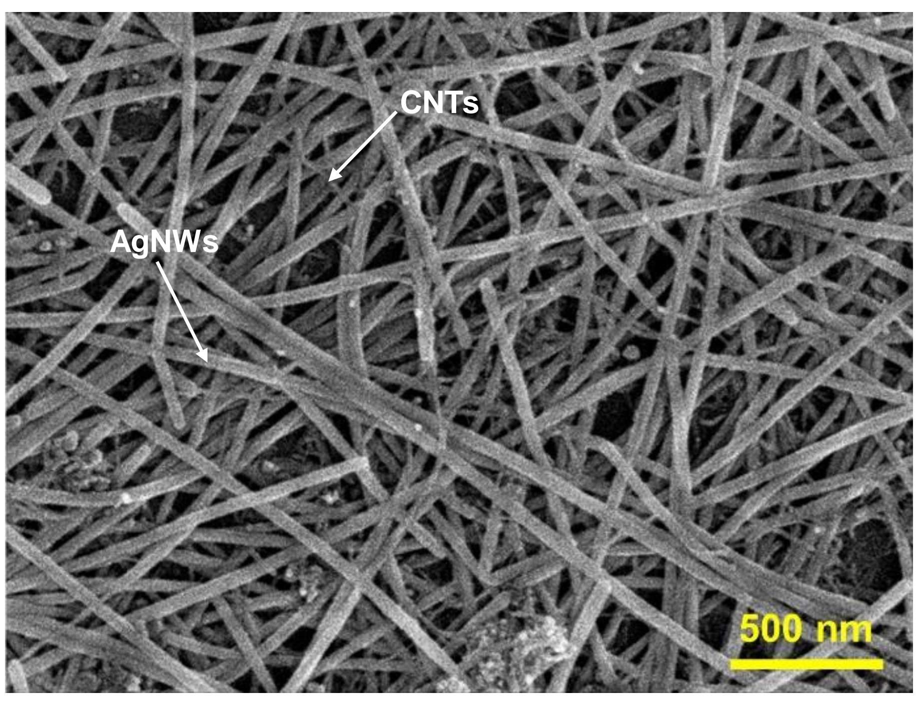

Figure 3.17. SEM image of patterned hybrid structure of AgNW network and carbon nanotubes (CNTs) through sequential filtration.

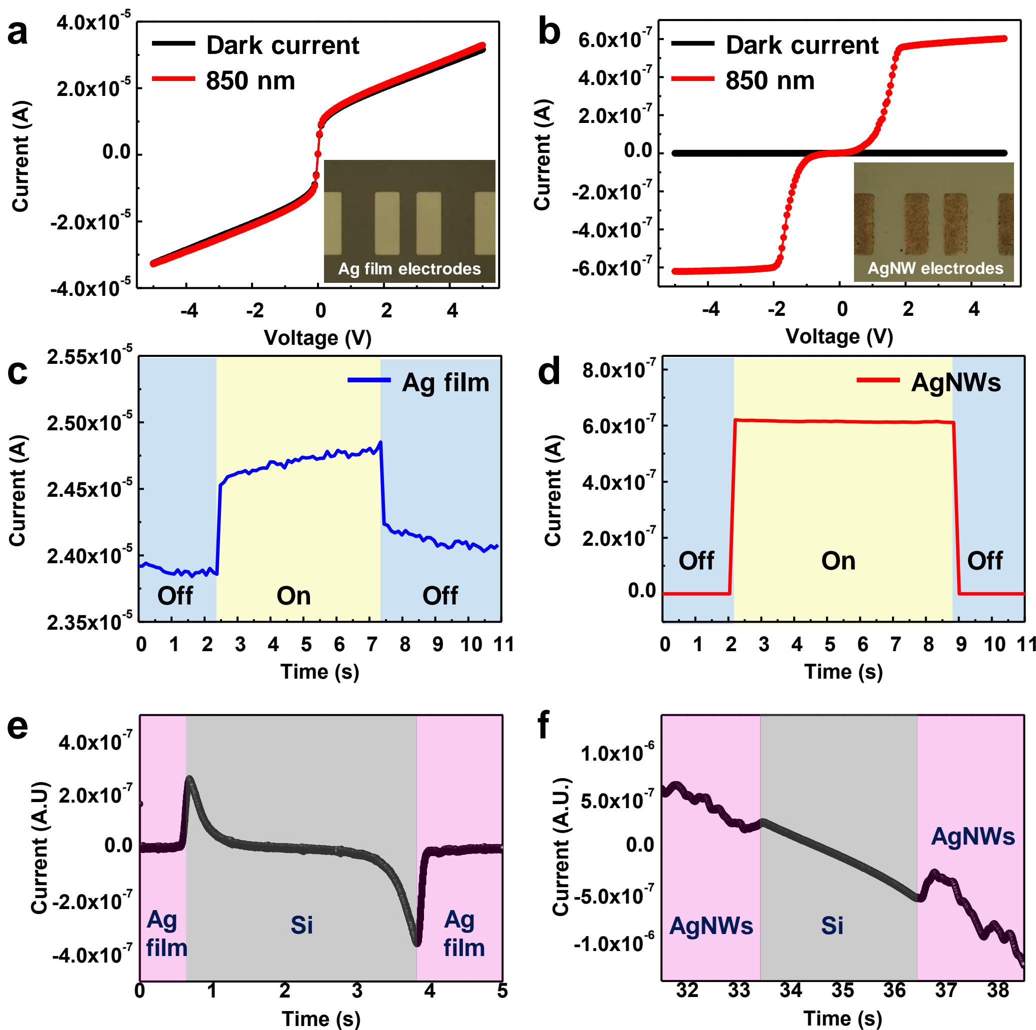

Figure 3.18. (a–b) Photo-response characteristics of the Si-photodetector with (a) Ag film electrode and (b) AgNW electrode under 850 nm LED light. (c, d) Photo-switching behavior of Si-photodetector with (c) Ag film electrode and (d) AgNW electrode under 850 nm LED light. (e, f) Photocurrent mapping data of the Si-photodetector with (e) Ag film electrode and (f) AgNW electrode under 532 nm laser.

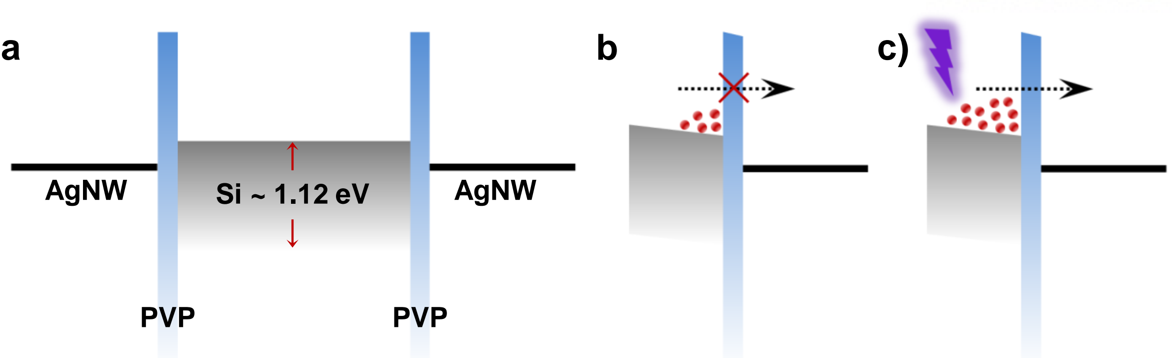

Figure 3.19. (a) Schematic illustration of estimated band alignment between Si and AgNWs. Schematic energy-band diagrams of Si photodetector (b) in dark state and (c) under the illumination of light.

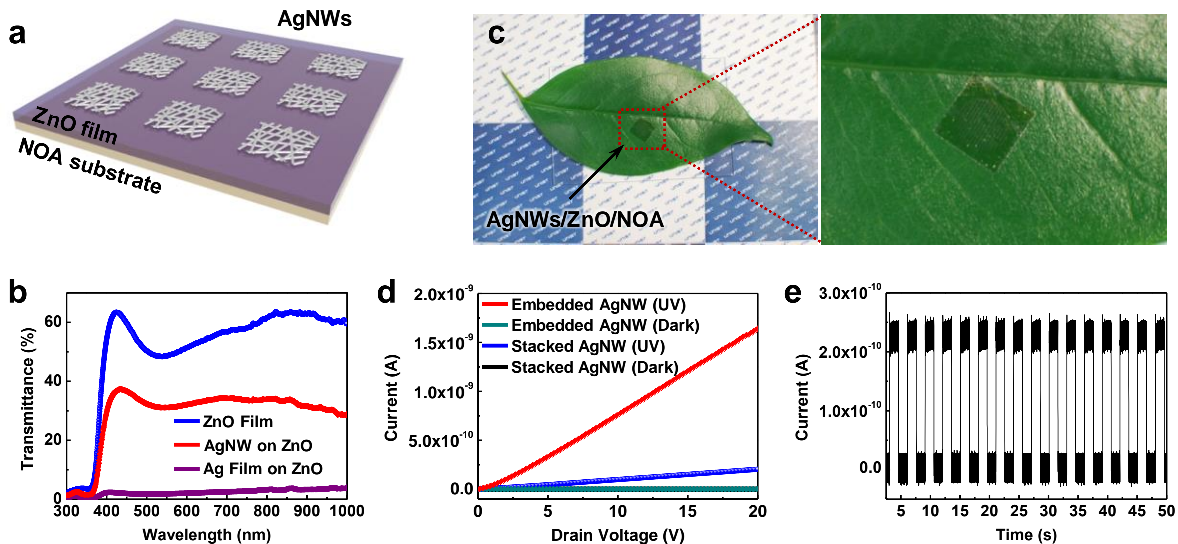

Figure 3.20. (a) Device scheme of the ZnO-based UV photodetector with AgNW network electrodes on the NOA substrate. (b) Transmittance of the AgNW electrode and Ag film electrode on a 200 nm ZnO thin film. (c) Optical images of UV photodetector arrays on the surface of leaf. (d) Photocurrent characteristics of UV photodetectors with AgNW electrodes stacked on and embedded in the ZnO active layer. (e) On/off stability of photo-switching behavior of UV photodetectors with embedded AgNW electrodes.

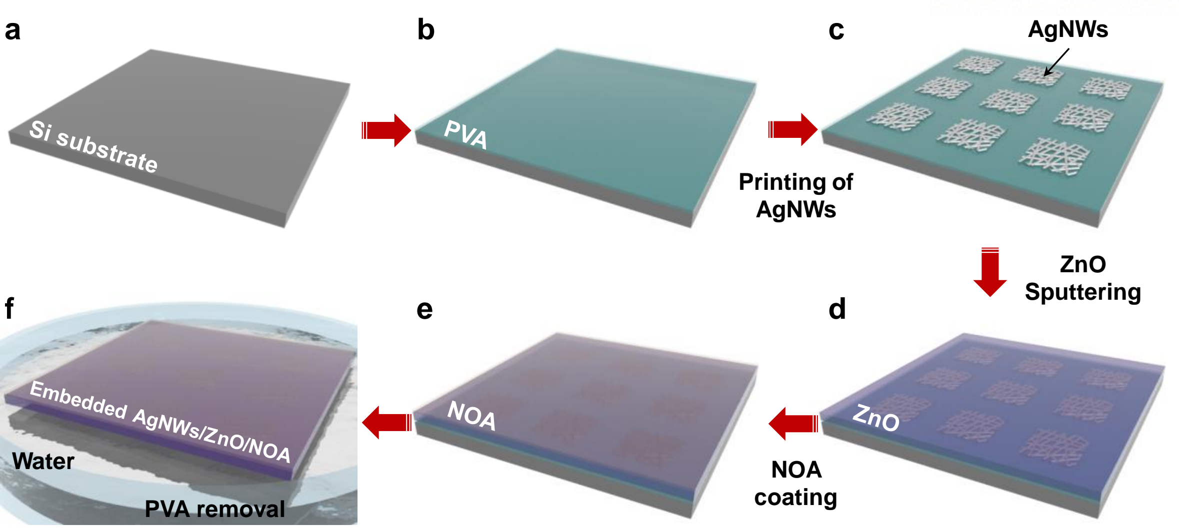

Figure 3.21. Fabrication scheme for flexible and transparent UV photodetector arrays with embedded AgNW electrodes.

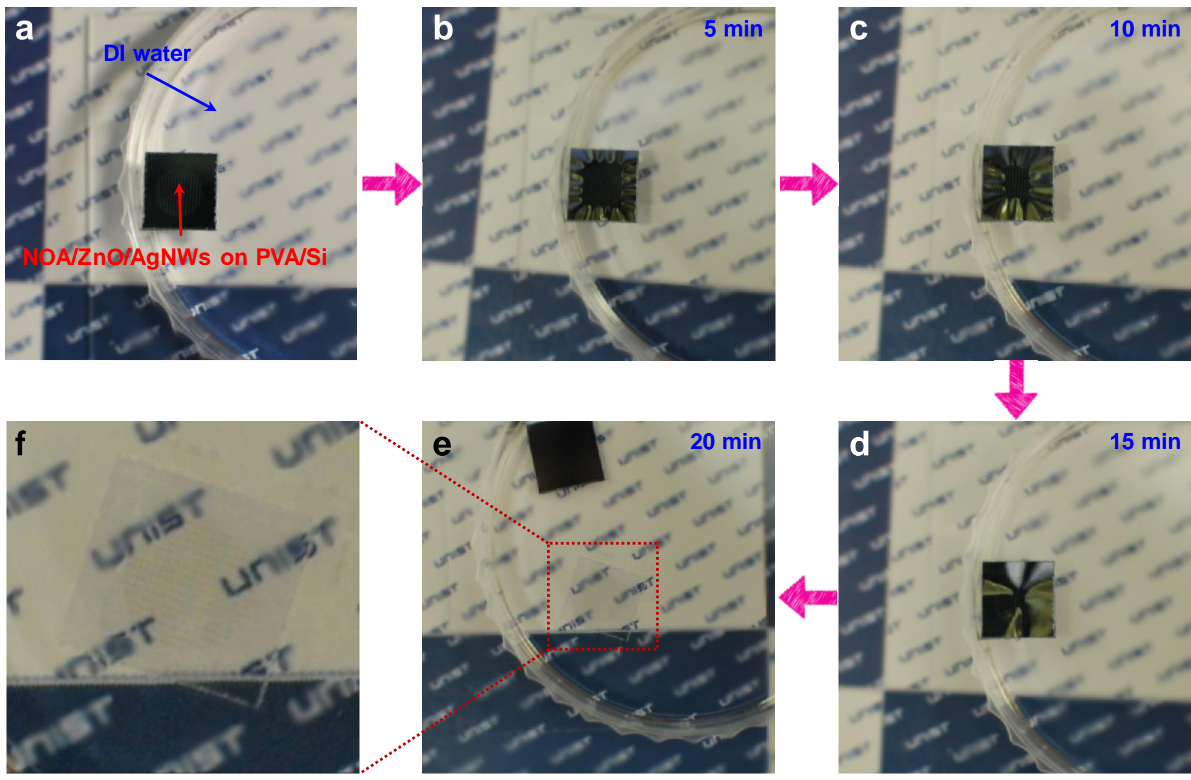

Figure 3.22. (a–e) Sequential optical images of the process of separation from source substrate for flexible and transparent UV photodetector arrays with embedded AgNW electrode: (a) immediately after floating on water, (b) after 5 min, (c) after 10 min, (d) after 15 min, and (e) after 20 min. (f) Close-up view of separated UV photodetector.

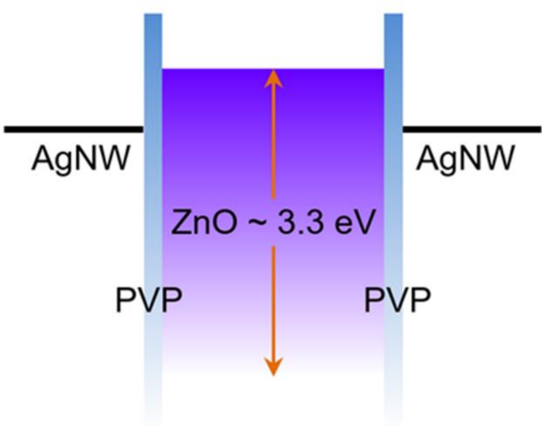

Figure 3.23. Schematic illustration of estimated band alignment between ZnO and AgNWs.

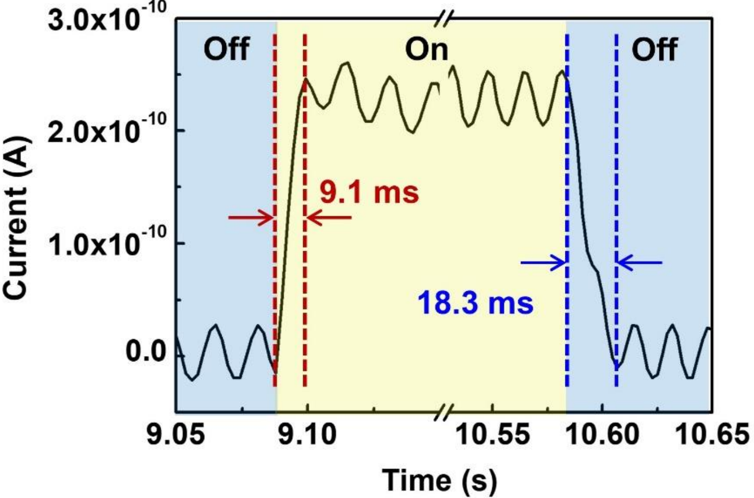

Figure 3.24. Photo-responsive rise and decay times of a UV photodetector with embedded AgNW electrode under illumination of λ = 365 nm and bias voltage of 5 V.

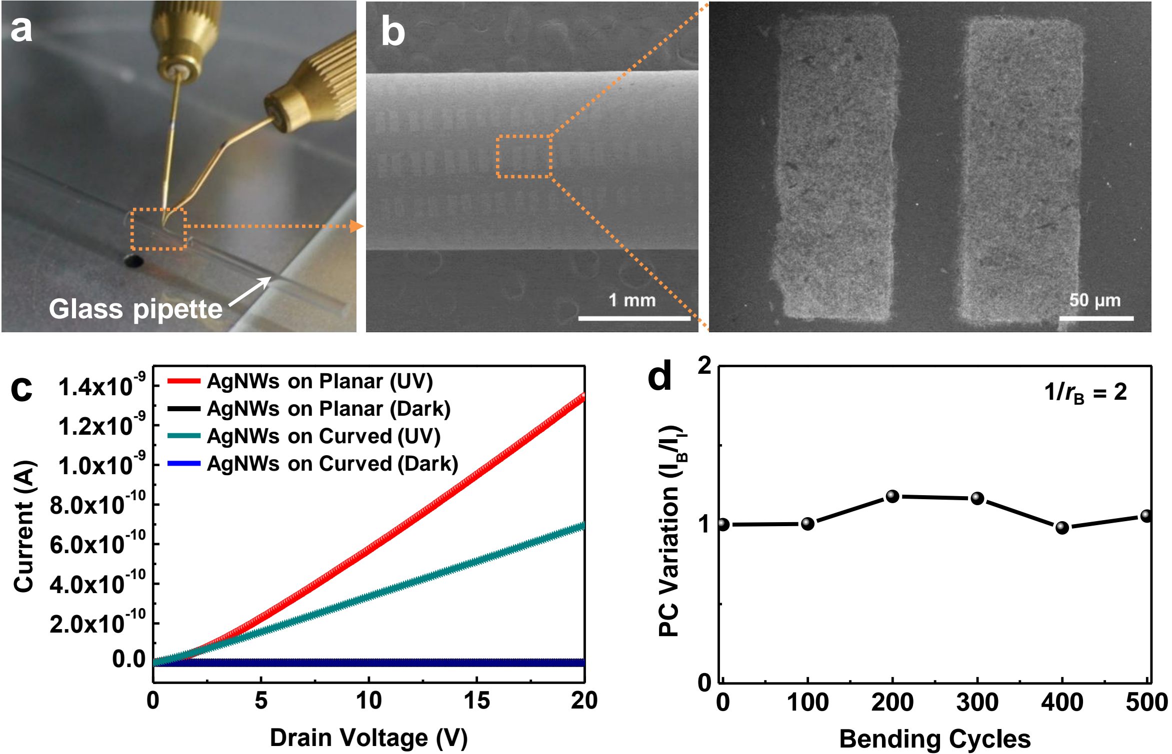

Figure 3.25. (a) Optical image and (b) SEM image of highly curved UV photodetector arrays on narrow glass pipette. (c) Photocurrent characteristics of the AgNW electrode-embedded UV photodetectors in flat and bent states. (d) Photocurrent retention as a function of bending cycles with bending radius of 0.5 cm.

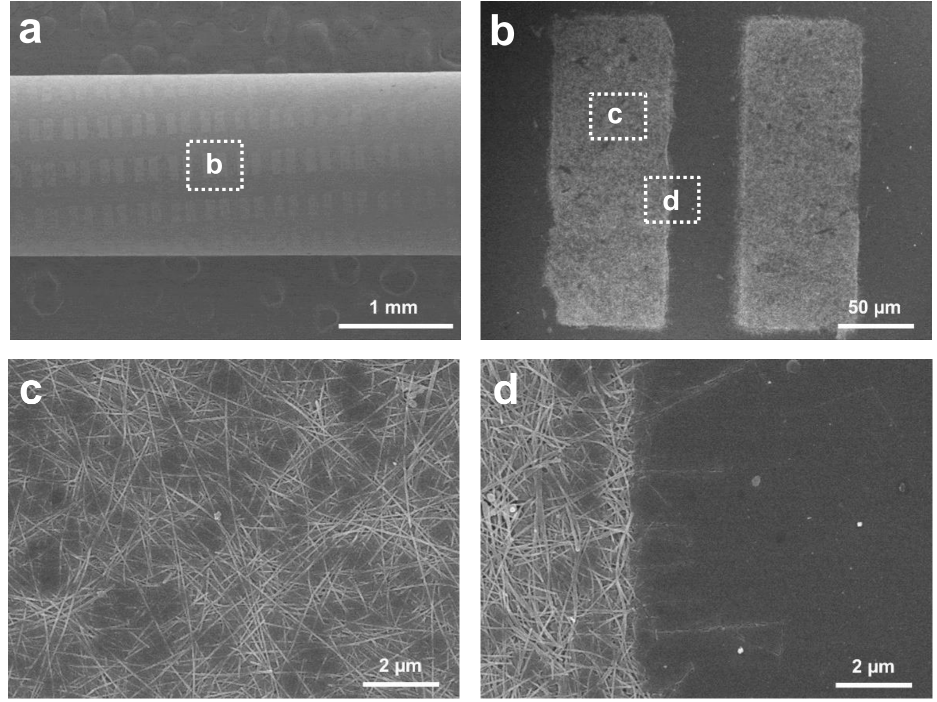

Figure 3.26. (a-d) SEM images of highly curved UV photodetector: (a) wide view, (b) the top part of UV photodetector arrays, (c) embedded AgNWs networks of top part device, and (d) the boundary area between channel layer and Ag NWs electrodes.

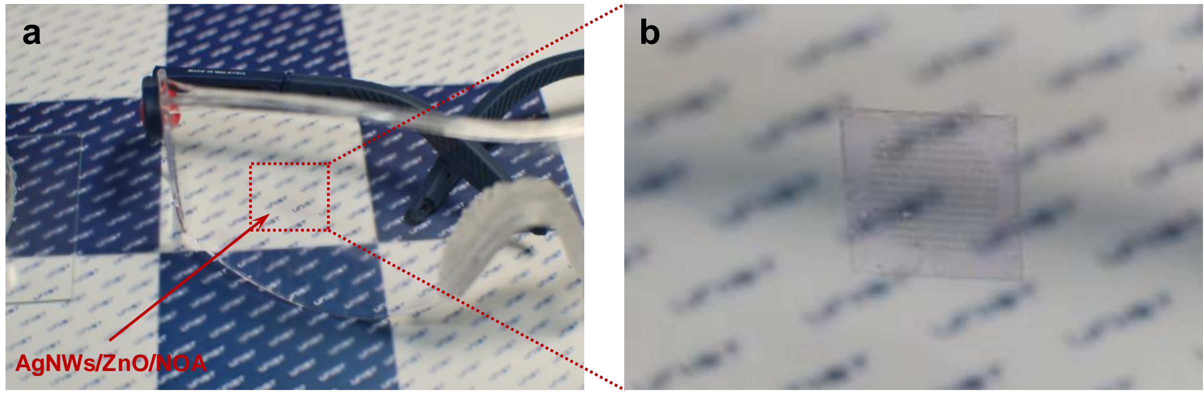

Figure 3.27. Optical images of UV photodetector arrays on safety glasses.

Table 3.1. Comparison of the performance of various flexible UV photodetectors.

Structure	Responsivity (A/W)	On/Off ratio	Response time (ms)	Flexibility	Reference
ZnO film/AgNWs	0.01	4×10^4	R_T/D_T: 9.1/18.3	r_B = 0.5 cm	This work
ZnO film/Au	2.2	10^2	R_T/D_T: 200/300	–	44
ZnO nanocrystal/Ag	0.14	10^3	R_T/D_T: 300/290	r_B = 3.0 cm	45
ZnO NWs/AgNWs	6.4	–	R_T/D_T: 800/1600	r_B = 0.5 cm	46
Al/ZnO NWs−Si/Au	0.4	32	R_T/D_T: 11/12	r_B = 1.0 cm	47
ZnO film/Au	0.36	–	–	–	48

R_T: rise time, D_T: decay time, r_B: bending radius

Chapter 4. Filtration Patterning of Liquid Exfoliated MoS_2 for High-Performance Large-Area Electronics

4.1 Introduction

The exploration of two-dimensional (2D) layered materials such as graphene, hexagonal boron nitride (h-BN), black phosphorus and transition-metal dichalcogenides (TMDCs) has led to extensive progress in research fields of electronics, energy storages and sensors due to their novel characteristics inherited from the 2D confined molecular structures.[1-3] In particular, the absence of dangling bond in the surface of 2D materials and tunable band gap enable to have potential applications in high-performance, multi-functional and flexible electronics.[4-6] Among 2D materials, molybdenum disulfide (MoS_2) is a promising candidate for new generation electronics, optoelectronics and sensors due to its environmental stability, mechanical flexibility, suitable band gap (1.0−2.0 eV) and high carrier mobility.[7-9] However, the practical applications of MoS_2 have been hindered from the lack of mass production, which requires efficient, low cost and eco-friendly exfoliation methods in large quantities. To address these issues, several synthetic methods have been introduced, including mechanical cleavage,[10] chemical vapor deposition (CVD)[11] and liquid exfoliation.[12, 13] But the mechanical cleavage is suffered from very limited scalability. The CVD method also needs more developments to resolve the issues of complicate fabrication process and requirement of harsh conditions.[14]

Liquid exfoliation is an alternative synthetic method for the mass production of MoS_2 by using ultrasonication in liquid phase for exfoliation. Thus, thin flake of MoS_2 can be prepared in solution-processable conditions, resulting in large-area films by spin coating or inkjet printing.[15-17] However, the vigorous ultrasonication triggers lots of surface defect and reduces the size of flakes, degrading the performance of devices. To reduce the time for ultrasonication, chemical intercalation method based on commonly used *tert*-butylithium-mediated intercalation supports the liquid exfoliation.[18-20] During lithium intercalation, however, insertion of Li^+ ions accompanies the injection of electrons into the MoS_2, inducing phase transition from semiconducting 2H phase to metallic 1T phase. Recently, a method of intercalating large cations such as tetraheptylammonium$^+$ (THA^+) by electrochemical reaction was introduced for preventing phase transition, whereby the number of injected electrons is decreased by reducing the number of intercalated ions.[21-23] This technique has enabled the efficient exfoliation with the large size of 2H−MoS_2 flakes and possible applications in large area transistors, biosensors and photodetectors. Although solution-processable MoS_2 can provide great opportunities for practical applications and commercialization, there are still challenges in the patterning process, which requires high baking temperature and chemical or dry etching, resulting in damages in MoS_2.

In this study, we demonstrated the large-area MoS_2 array, which is prepared by using ion-intercalation

in liquid exfoliation and vacuum filtration with a shadow mask. The bulk MoS_2 crystal was exfoliated in liquid phase through the intercalation of TBA^+ cations, resulting in reduced ultrasonication time and high quality of 2H−MoS_2 flakes in isopropyl alcohol (IPA). The MoS_2 flakes were easily patterned by vacuum filtration with the thin polyimide (PI) shadow mask without etching processes. Then, the patterned MoS_2 array was transferred by water-assisted transfer printing method from an anodic aluminum oxide (AAO) template to arbitrary substrates such as silicon, polyethylene naphthalate (PEN) and PI film. The large-area MoS_2 array exhibited an electron mobility value of 1.5 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio of 10^5. Moreover, our method allows the combined assembly of MoS_2 and single-walled carbon nanotube (SWNT) for the improvement of performance, resulting in mobility of 2.8 $cm^2\ V^{-1}\ s^{-1}$. This simple method enables heterostructure devices for high-performance and flexible electronic applications, which are advantageous in scalability and avoids complicate fabrication process for multi-functional applications.

4.2 Experimental details

***Liquid exfoliation with ion-intercalation*:** Tetraheptylammonium bromide (THAB) (99%, Sigma–Aldrich) was dissolved in acetonitrile with concentration of 5 mg ml^{-1}, which was acted as electrolyte. Then, small piece of MoS_2 crystal (SPI Supplies) and graphite rod were placed in THAB solution as the working electrode and counter electrode, respectively. A voltage of −6 V was applied to MoS_2 crystal for 1 h to insert THA^+ cations into the crystal. After electrochemical reaction, the intercalated MoS_2 crystal was rinsed by ethanol. The crystal was exfoliated by ultrasonication for 30 min in the solution of 0.2 M polyvinylpyrrolidone (PVP; Molecular weight of 40,000, Sigma–Aldrich) in dimethylformamide (DMF). To remove large cluster of non-exfoliated MoS_2 and impurities, the exfoliated solution was centrifuged at 2,000 rpm for 5 min and precipitate were discarded. The solution was centrifuged at 13,000 rpm for 1 h and the solvent was replaced from DMF to IPA for 3 times in order to wash the excessive PVP. Finally, the MoS_2 solvent was obtained after removal of residual MoS_2 flakes by centrifugation at 3,000 rpm for 3 min.

***Patterning by vacuum filtration*:** A piece of silicon was cleaned by ultrasonication for 30 min in acetone, deionized (DI) water and IPA, sequentially. The PI solution (PICOMAX, Korea) was spin coated on the Si substrate at 4,000 rpm for 60 s after O_2 plasma treatment (15 W for 5 min). The PI film on Si substrate was cured at 70 °C for 1 h and 130 °C for 3 h. The patterning process of PI film was done by using standard photolithography (MA–6, SUSS MicroTec, Germany) and reactive ion etching (RIE; Lab Star, TTL, Korea) process (20 sccm of SF_6, 60 sccm of Ar; 10 mTorr; 300 W of RF power). The PI shadow mask was loaded on AAO template (Whatman, UK) of 0.02 μm pore size through floating on DI water. Then, patterning process was finished by vacuum filtration of 1 mg ml^{-1} MoS_2 solution onto PI shadow mask with AAO template.

***Fabrication of MoS_2 array device*:** The substrates, such as PEN, PI and Si, was washed by DI water and ethanol. The patterned MoS_2 array on AAO template was attached to the polydimethylsiloxane (PDMS) stamp. Next, PDMS attached AAO template was immersed into DI water. Then, the patterned MoS_2 array was successfully transferred to PDMS stamp after removal of AAO templated from the PDMS stamp. The MoS_2 array was placed on desired substrate by wet-transfer printing technique with ethanol. For reducing surface defects on MoS_2, the array was treated with 10 mg ml^{-1} bis(trifluoromethane)sulfonimide (TFSI; 95.0%, Sigma–Aldrich) in 1,2-dichloroethane at 80 °C for 1h. Finally, Cr/Au (3/100 nm) electrode contacts were formed via e-beam lithography (nB3, Nanobeam LTD, UK) and thermal evaporation. In case of composite device with SWNT, the composite array was fabricated by adding 0.1 mg ml^{-1} SWNT in toluene (nanoWearable, Korea) during vacuum filtration process of MoS_2 solution.

***Characterization*:** The thickness of the single flake and stacked flakes of MoS_2 were measured by using atomic force microscopy (AFM; DI–3100, Vecco, US). The morphologies of MoS_2 array was analyzed through field emission scanning electron microscopy (FE-SEM; S–4800, Hitachi, Japan) images. The electrical properties of MoS_2 array were investigated by a semiconductor characterization system (4200–SCS, Keithley, US) and a vacuum probe station (M6VC, MS Tech, Korea). A monochromator (Cornerstone™ 130 1/8 m Monochromators, Newport, USA) and a Xe arc lamp (300 W) was employed to analyze the optoelectrical properties with various wavelengths of light. The intensity of light at various wavelengths was confirmed by using a calibrated optical power meter (1916-R, Newport, US), incorporating a Si photodetector (818-UV, Newport, US) and a Ge photodetector (818-IR, Newport, US).

4.3 Results and discussion

The ion-intercalation into MoS_2 crystal by electrochemical reaction is illustrated in Figure 4.1a, where bulk MoS_2 crystal, graphite rod, THAB in acetonitrile were used as working electrode, counter electrode and electrolyte, respectively. Here, the large size of THA^+ cations (about 0.85 nm) was inserted into MoS_2 crystal, driven by negative electrochemical potential on MoS_2.[21] Because the size of THA^+ cation is greater than the interlayer spacing of MoS_2 layers (about 0.615 nm),[24] the volume of MoS_2 crystal was dramatically expanded by ion-intercalation (Figure 4.1b). The intercalated MoS_2 crystal was immediately exfoliated in 0.2 M PVP/DMF solution by ultrasonication for 30 min, where PVP was used for stable dispersion of exfoliated MoS_2 flakes. After exfoliation of MoS_2, the DMF solvent was replaced to IPA solvent and excessive PVP was removed by typical centrifuge and re-dispersion processes (Figure 4.2). As a result, the exfoliated MoS_2 flakes were collected in IPA solution with concentration of 1 mg ml^{-1} (Figure 4.1c). The morphology of exfoliated MoS_2 flakes was elucidated by AFM and SEM images (Figure 4.1d and Figure 4.3), which indicate narrow thickness

distribution and lateral dimensions of 0.5–2.0 μm. Figure 4.4 shows that the thicknesses of MoS_2 flakes are about 2.0–3.3 nm.

The patterning and transfer printing processes of exfoliated MoS_2 flakes is illustrated in Figure 4.5a, including vacuum filtration with PI shadow mask and transfer printing via PDMS stamp. At first, the PI shadow mask was fabricated by spin-coating of PI solution on Si wafer with curing at 130 °C for 3 h and patterned by standard photolithography and RIE processes. The PI shadow mask was successfully separated from Si wafer without any external damage through water-assisted detaching method.[25] Then, the PI shadow mask was loaded onto the AAO template by scooping floated PI shadow mask on DI water with AAO template. Next, the PI shadow mask was conformally attached to AAO template by the vacuum pressure. During the vacuum filtration, DI water was firstly filled up to the funnel and then few drops of MoS_2 solution were added to DI water. After vacuum filtration, the PI shadow mask was removed by drying in the oven. As a result, the patterned MoS_2 array was remained on the AAO template as shown in Figure 4.5b. For the transfer of MoS_2 array from AAO template onto PDMS stamp, PDMS was attached onto the MoS_2/AAO template and immersed into DI water. In this process, the water can penetrate between hydrophilic AAO template and hydrophobic MoS_2 array with PDMS stamp, resulting in easy separation of MoS_2 array from AAO template.[26, 27] Successful transfer of MoS_2 array from AAO template to PDMS was confirmed by Figure 4.5c. Finally, MoS_2 array on PDMS stamp was easily transferred onto Si/SiO_2 wafer via wet-transfer printing, which is supported by liquid bridge of ethanol solution (Figure 4.5d).[28-30] The morphology of transferred MoS_2 array on Si wafer was analyzed by SEM and AFM images, as shown in Figure 4.6 and Figure 4.7. It is noted that the MoS_2 array was well transferred from AAO template onto Si wafer without introducing external damage. Moreover, the morphology and thickness of MoS_2 array could be tuned by the control of amount of MoS_2 solution during the vacuum filtration process (Figure 4.8). In addition, this method enables patterning of MoS_2 array with various sizes because the size of pattern is dependent on the PI shadow mask. Figure 4.9 shows the patterned MoS_2 array on Si wafer with different widths (150 μm, 50 μm, 10 μm). Because our method doesn't require extreme conditions such as high temperature or pressure, the MoS_2 array can be easily patterned on polymeric substrates, e.g., PEN, PI film. (Figure 4.10). As a result, our method enables simple and cost-effective patterning of MoS_2 on arbitrary substrates, thus demonstrating potential applications in the fabrication of large-area thin film transistors (TFTs), flexible electronics and transparent photodetectors.

To explore the potential of patterned MoS_2 array for electronic and optoelectronic applications, we fabricated a back-gate MoS_2 transistor on SiO_2 (100 nm)/heavily p-doped Si (Figure 4.11a). The transfer (Figure 4.11b) and output characteristics (Figure 4.11c) of fabricated MoS_2 array transistors indicate that our transistor shows properties of a typical n-type transistor. The mobility μ of the MoS_2 array transistor could be calculated by using

$$\mu = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{G}}}\left(\frac{L}{W C_{\mathrm{i}} V_{\mathrm{DS}}}\right), \quad (1)$$

where L, W, and C_i denote channel length, channel width, and specific capacitance between the channel and the back-gate silicon per unit area.[31] The specific capacitance can be obtained using the parallel-plate capacitor equation, $C_{\mathrm{i}} = \varepsilon_0 \varepsilon_{\mathrm{r}} / d$, where ε_0, ε_{r}, and d are the vacuum dielectric constant (8.85×10^{-12} F/m), dielectric constant of silicon oxide (3.9), and silicon oxide thickness (100 nm), respectively. On the basis of transfer characteristic shown in Figure 4.11c, the mobility and on/off ratio of our transistor is determined to be around 1.5 $cm^2\ V^{-1}\ s^{-1}$ and 10^5, respectively. The mobility and on/off ratio of MoS_2 array transistors according to the channel lengths, widths and amount of MoS_2 solution were analyzed in Figure 4.12. Our device exhibited the mobility of around 1.2–1.6 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio of around 10^4–10^5. The mobility values obtained in MoS_2 array transistor are lower than that obtained in a single MoS_2 flake transistor (about 10 $cm^2\ V^{-1}\ s^{-1}$), which is derived from Figure 4.13. It is mainly attributed to the contact resistances and trap sites in grain boundaries of stacked MoS_2 flakes.[32] Furthermore, MoS_2 array transistor exhibits photo-response properties due to photoconductive effect of MoS_2. As shown in Figure 4.11d, the spectral responsivity of the device ranges from ultraviolet (UV) to visible wavelengths with a maximum responsivity of 24 A W^{-1}, which corresponds to the typical band gap of MoS_2. These excellent responsivities of device are induced by large size MoS_2 flakes and low dangling bonds which are caused by efficient liquid exfoliation with ion-intercalation.[23]

One of novel features in our patterning method is the easy processability for the combined assembly of various nanomaterials through filtration of each solutions and transfer printing technique. Here, we fabricated the composite array of MoS_2 and SWNT by adding 20 µl of 0.1 mg ml^{-1} SWNT solution during filtration of MoS_2 solution (Figure 4.14a). The electrical properties of fabricated composite array were analyzed by transfer characteristics in Figure 4.14b. The current variation as applied gate voltages is much higher in the composite array than that in MoS_2 array, inducing improved electron mobility of 2.8 $cm^2\ V^{-1}\ s^{-1}$, whereby the on/off ratio is slightly degraded. The enhanced mobility in composite array transistor is attributed to the high conductivity of SWNT, where the SWNT acts as the conductive pass, achieving efficient electron transportation in channel layer.[33] This capability of patterning composites with various nanomaterials induces further improvement in performances and multi-functionality in large-area electronics. A comprehensive comparison is provided in Table 4.1. Our device showed comparable results to those of other large-area MoS_2 electronics and optoelectronics. Especially, our method can provide high quality patterning of MoS_2 with easy processability and broad choice of nanomaterials, demonstrating the great potential for large-area MoS_2 arrays for future multi-functional electronics with combinations with quantum dots, conductive nanowires and polymeric substates.

4.4 Conclusion

In summary, a large-area MoS_2 array was successfully demonstrated via a simple and cost-effective patterning method with liquid exfoliation and vacuum filtration with a PI shadow mask. Because of effective exfoliation of large size MoS_2 by ion-intercalation with TBA^+ cations, the MoS_2 array transistor possesses electron mobility of 1.5 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of 10^5 and high photoresponsivity of 24 A W^{-1}. In addition, the MoS_2 array can be fabricated on flexible substrates such as PEN and PI films by the water-assisted transfer printing method after filtration process. Furthermore, the electron mobility of MoS_2 array transistor could be enhanced up to 2.8 $cm^2\ V^{-1}\ s^{-1}$ through the composite formation with highly conductive SWNT during filtration process. These simple processability and diverse material capability of our method for large-area MoS_2 devices can offer potential applications in the development of high-performance, flexible and multi-functional electronics.

4.5 References

(1) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L., Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014,** *9*, 768-779.

(2) Huh, W.; Jang, S.; Lee, J. Y.; Lee, D.; Lee, D.; Lee, J. M.; Park, H. G.; Kim, J. C.; Jeong, H. Y.; Wang, G.; Lee, C. H., Synaptic Barristor Based on Phase-Engineered 2D Heterostructures. *Adv. Mater.* **2018,** *30*, e1801447.

(3) Huo, N.; Konstantatos, G., Recent Progress and Future Prospects of 2D-Based Photodetectors. *Adv. Mater.* **2018,** *30*, e1801164.

(4) Liu, Y.; Weiss, N. O.; Duan, X.; Cheng, H.-C.; Huang, Y.; Duan, X., van der Waals Heterostructures and Devices. *Nat. Rev. Mater.* **2016,** *1*, 16042.

(5) Geim, A. K.; Grigorieva, I. V., van der Waals Heterostructures. *Nature* **2013,** *499*, 419-425.

(6) Jariwala, D.; Marks, T. J.; Hersam, M. C., Mixed-Dimensional van der Waals Heterostructures. *Nat. Mater.* **2017,** *16*, 170-181.

(7) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S., Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012,** *7*, 699-712.

(8) Wang, H.; Li, C.; Fang, P.; Zhang, Z.; Zhang, J. Z., Synthesis, Properties, and Optoelectronic Applications of Two-Dimensional MoS_2 and MoS_2-Based Heterostructures. *Chem. Soc. Rev.* **2018,** *47*, 6101-6127.

(9) Yu, W. J.; Liu, Y.; Zhou, H.; Yin, A.; Li, Z.; Huang, Y.; Duan, X., Highly Efficient Gate-Tunable Photocurrent Generation in Vertical Heterostructures of Layered Materials. *Nat. Nanotechnol.* **2013,** *8*, 952-958.

(10) Huang, Y.; Pan, Y. H.; Yang, R.; Bao, L. H.; Meng, L.; Luo, H. L.; Cai, Y. Q.; Liu, G. D.; Zhao,

W. J.; Zhou, Z.; Wu, L. M.; Zhu, Z. L.; Huang, M.; Liu, L. W.; Liu, L.; Cheng, P.; Wu, K. H.; Tian, S. B.; Gu, C. Z.; Shi, Y. G.; Guo, Y. F.; Cheng, Z. G.; Hu, J. P.; Zhao, L.; Yang, G. H.; Sutter, E.; Sutter, P.; Wang, Y. L.; Ji, W.; Zhou, X. J.; Gao, H. J., Universal Mechanical Exfoliation of Large-Area 2D Crystals. *Nat. Commun.* **2020,** *11*, 2453.

(11) Jeon, J.; Jang, S. K.; Jeon, S. M.; Yoo, G.; Jang, Y. H.; Park, J. H.; Lee, S., Layer-Controlled CVD Growth of Large-Area Two-Dimensional MoS_2 Films. *Nanoscale* **2015,** *7*, 1688-1695.

(12) Hu, G.; Kang, J.; Ng, L. W. T.; Zhu, X.; Howe, R. C. T.; Jones, C. G.; Hersam, M. C.; Hasan, T., Functional Inks and Printing of Two-Dimensional Materials. *Chem. Soc. Rev.* **2018,** *47*, 3265-3300.

(13) Coleman, J. N.; Lotya, M.; O'Neill, A.; Bergin, S. D.; King, P. J.; Khan, U.; Young, K.; Gaucher, A.; De, S.; Smith, R. J.; Shvets, I. V.; Arora, S. K.; Stanton, G.; Kim, H. Y.; Lee, K.; Kim, G. T.; Duesberg, G. S.; Hallam, T.; Boland, J. J.; Wang, J. J.; Donegan, J. F.; Grunlan, J. C.; Moriarty, G.; Shmeliov, A.; Nicholls, R. J.; Perkins, J. M.; Grieveson, E. M.; Theuwissen, K.; McComb, D. W.; Nellist, P. D.; Nicolosi, V., Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* **2011,** *331*, 568-571.

(14) Das, P.; Fu, Q.; Bao, X.; Wu, Z.-S., Recent Advances in the Preparation, Characterization, and Applications of Two-Dimensional Heterostructures for Energy Storage and Conversion. *J. Mater. Chem. A* **2018,** *6*, 21747-21784.

(15) Qiao, W.; Yan, S.; He, X.; Song, X.; Li, Z.; Zhang, X.; Zhong, W.; Du, Y., Effects of Ultrasonic Cavitation Intensity on the Efficient Liquid-Exfoliation of MoS_2 Nanosheets. *RSC Adv.* **2014,** *4*, 50981-50987.

(16) McManus, D.; Vranic, S.; Withers, F.; Sanchez-Romaguera, V.; Macucci, M.; Yang, H.; Sorrentino, R.; Parvez, K.; Son, S. K.; Iannaccone, G.; Kostarelos, K.; Fiori, G.; Casiraghi, C., Water-Based and Biocompatible 2D Crystal Inks for All-Inkjet-Printed Heterostructures. *Nat. Nanotechnol.* **2017,** *12*, 343-350.

(17) Li, J.; Naiini, M. M.; Vaziri, S.; Lemme, M. C.; Östling, M., Inkjet Printing of MoS_2. *Adv. Funct. Mater.* **2014,** *24*, 6524-6531.

(18) Kappera, R.; Voiry, D.; Yalcin, S. E.; Branch, B.; Gupta, G.; Mohite, A. D.; Chhowalla, M., Phase-Engineered Low-Resistance Contacts for Ultrathin MoS_2 Transistors. *Nat. Mater.* **2014,** *13*, 1128-1134.

(19) Eda, G.; Yamaguchi, H.; Voiry, D.; Fujita, T.; Chen, M.; Chhowalla, M., Photoluminescence from Chemically Exfoliated MoS_2. *Nano Lett.* **2011,** *11*, 5111-5116.

(20) Ambrosi, A.; Sofer, Z.; Pumera, M., Lithium Intercalation Compound Dramatically Influences the Electrochemical Properties of Exfoliated MoS_2. *Small* **2015,** *11*, 605-612.

(21) Zhang, P.; Yang, S.; Pineda-Gomez, R.; Ibarlucea, B.; Ma, J.; Lohe, M. R.; Akbar, T. F.; Baraban, L.; Cuniberti, G.; Feng, X., Electrochemically Exfoliated High-Quality 2H-MoS_2 for Multiflake

Thin Film Flexible Biosensors. *Small* **2019,** *15*, e1901265.

(22) Lin, Z.; Liu, Y.; Halim, U.; Ding, M.; Liu, Y.; Wang, Y.; Jia, C.; Chen, P.; Duan, X.; Wang, C.; Song, F.; Li, M.; Wan, C.; Huang, Y.; Duan, X., Solution-Processable 2D Semiconductors for High-Performance Large-Area Electronics. *Nature* **2018,** *562*, 254-258.

(23) Shi, H.; Li, M.; Shaygan Nia, A.; Wang, M.; Park, S.; Zhang, Z.; Lohe, M. R.; Yang, S.; Feng, X., Ultrafast Electrochemical Synthesis of Defect-Free In_2Se_3 Flakes for Large-Area Optoelectronics. *Adv. Mater.* **2020,** *32*, 1907244.

(24) Hirsch, A.; Hauke, F., Post-Graphene 2D Chemistry: The Emerging Field of Molybdenum Disulfide and Black Phosphorus Functionalization. *Angew. Chem. Int. Ed. Engl.* **2018,** *57*, 4338-4354.

(25) Um, D. S.; Lee, Y.; Kim, T.; Lim, S.; Lee, H.; Ha, M.; Khan, Z.; Kang, S.; Kim, M. P.; Kim, J. Y.; Ko, H., High-Resolution Filtration Patterning of Silver Nanowire Electrodes for Flexible and Transparent Optoelectronic Devices. *ACS Appl. Mater. Interfaces* **2020,** *12*, 32154-32162.

(26) Lai, S.; Jeon, J.; Song, Y.-J.; Lee, S., Water-Penetration-Assisted Mechanical Transfer of Large-Scale Molybdenum Disulfide onto Arbitrary Substrates. *RSC Adv.* **2016,** *6*, 57497-57501.

(27) Li, H.; Wu, J. M. T.; Huang, X.; Yin, Z. Y.; Liu, J. Q.; Zhang, H., A Universal, Rapid Method for Clean Transfer of Nanostructures onto Various Substrates. *ACS Nano* **2014,** *8*, 6563-6570.

(28) Hwang, J. K.; Cho, S.; Dang, J. M.; Kwak, E. B.; Song, K.; Moon, J.; Sung, M. M., Direct Nanoprinting by Liquid-Bridge-Mediated Nanotransfer Moulding. *Nat. Nanotechnol.* **2010,** *5*, 742-748.

(29) Um, D. S.; Lee, Y.; Lim, S.; Park, S.; Lee, H.; Ko, H., High-Performance MoS_2/CuO Nanosheet-on-One-Dimensional Heterojunction Photodetectors. *ACS Appl. Mater. Interfaces* **2016,** *8*, 33955-33962.

(30) Ma, X.; Liu, Q.; Xu, D.; Zhu, Y.; Kim, S.; Cui, Y.; Zhong, L.; Liu, M., Capillary-Force-Assisted Clean-Stamp Transfer of Two-Dimensional Materials. *Nano Lett.* **2017,** *17*, 6961-6967.

(31) Huo, N.; Kang, J.; Wei, Z.; Li, S.-S.; Li, J.; Wei, S.-H., Novel and Enhanced Optoelectronic Performances of Multilayer MoS_2-WS_2 Heterostructure Transistors. *Adv. Funct. Mater.* **2014,** *24*, 7025-7031.

(32) Lin, Z.; Chen, Y.; Yin, A.; He, Q.; Huang, X.; Xu, Y.; Liu, Y.; Zhong, X.; Huang, Y.; Duan, X., Solution Processable Colloidal Nanoplates as Building Blocks for High-Performance Electronic Thin Films on Flexible Substrates. *Nano Lett* **2014,** *14*, 6547-6553.

(33) Xiao, P.; Mao, J.; Ding, K.; Luo, W.; Hu, W.; Zhang, X.; Zhang, X.; Jie, J., Solution-Processed 3D rGO-MoS_2/Pyramid Si Heterojunction for Ultrahigh Detectivity and Ultra-Broadband Photodetection. *Adv. Mater.* **2018,** *30*, 1801729.

(34) Yang, P.; Zou, X.; Zhang, Z.; Hong, M.; Shi, J.; Chen, S.; Shu, J.; Zhao, L.; Jiang, S.; Zhou, X.; Huan, Y.; Xie, C.; Gao, P.; Chen, Q.; Zhang, Q.; Liu, Z.; Zhang, Y., Batch Production of 6-Inch

Uniform Monolayer Molybdenum Disulfide Catalyzed by Sodium in Glass. *Nat. Commun.* **2018,** *9*, 979.

(35) Lim, Y. R.; Song, W.; Han, J. K.; Lee, Y. B.; Kim, S. J.; Myung, S.; Lee, S. S.; An, K. S.; Choi, C. J.; Lim, J., Wafer-Scale, Homogeneous MoS_2 Layers on Plastic Substrates for Flexible Visible-Light Photodetectors. *Adv. Mater.* **2016,** *28*, 5025-5030.

(36) Lee, Y.; Yang, J.; Lee, D.; Kim, Y. H.; Park, J. H.; Kim, H.; Cho, J. H., Trap-Induced Photoresponse of Solution-Synthesized MoS_2. *Nanoscale* **2016,** *8*, 9193-9200.

(37) Velusamy, D. B.; Haque, M. A.; Parida, M. R.; Zhang, F.; Wu, T.; Mohammed, O. F.; Alshareef, H. N., 2d Organic-Inorganic Hybrid Thin Films for Flexible UV-Visible Photodetectors. *Adv. Funct. Mater.* **2017,** *27*, 1605554.

(38) Xie, Y.; Zhang, B.; Wang, S.; Wang, D.; Wang, A.; Wang, Z.; Yu, H.; Zhang, H.; Chen, Y.; Zhao, M.; Huang, B.; Mei, L.; Wang, J., Ultrabroadband MoS_2 Photodetector with Spectral Response from 445 to 2717 nm. *Adv. Mater.* **2017,** *29*, 1605972.

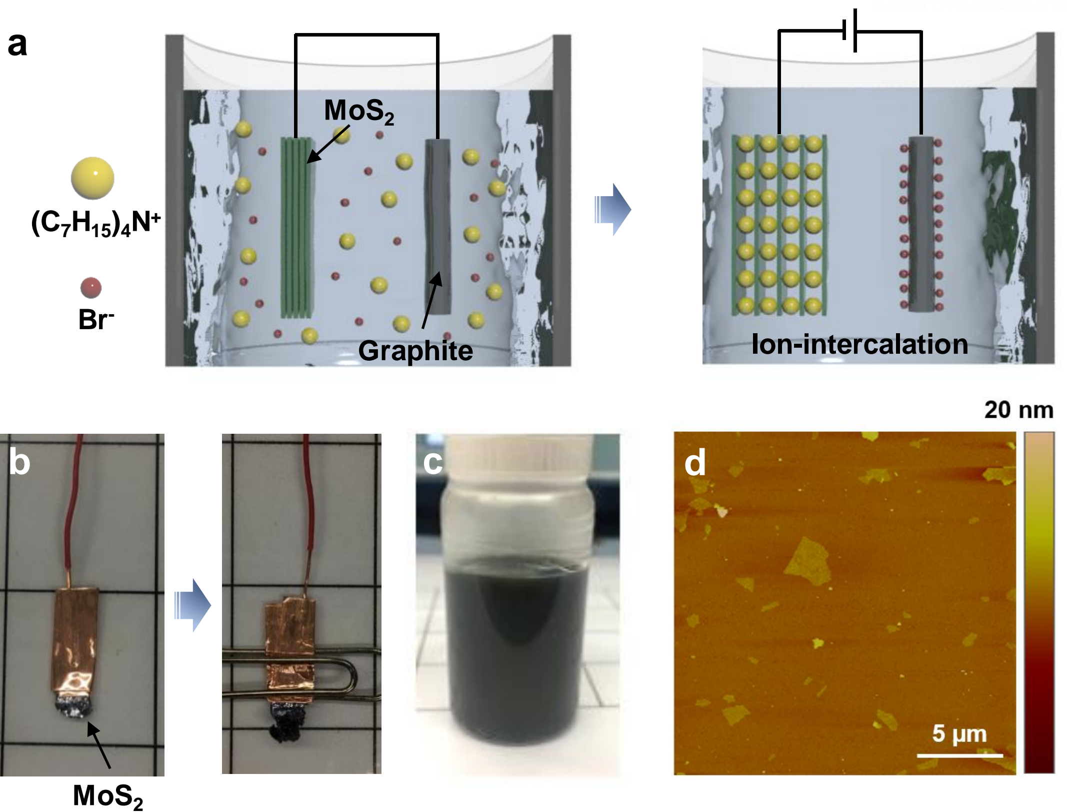

Figure 4.1. Liquid exfoliation of MoS_2 with ion-intercalation. (a) Schematic illustrations for mechanism of ion-intercalation by electrochemical reaction. (b) Photographs of natural MoS_2 crystal (left) and intercalated MoS_2 crystal (right). (c) Photograph of dispersion of MoS_2 flakes in IPA solution after exfoliation. (d) AFM image of MoS_2 flakes with a narrow thickness distribution.

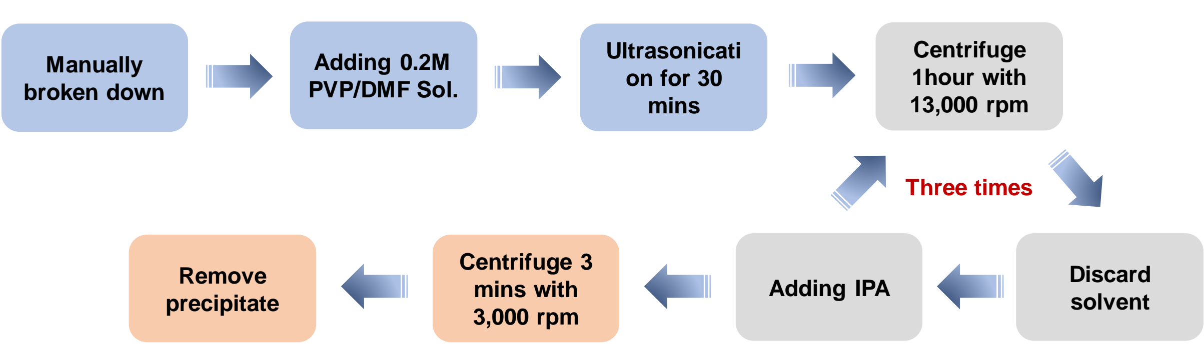

Figure 4.2. Schematics of the liquid exfoliation, centrifuge and re-dispersion steps for MoS_2 solution.

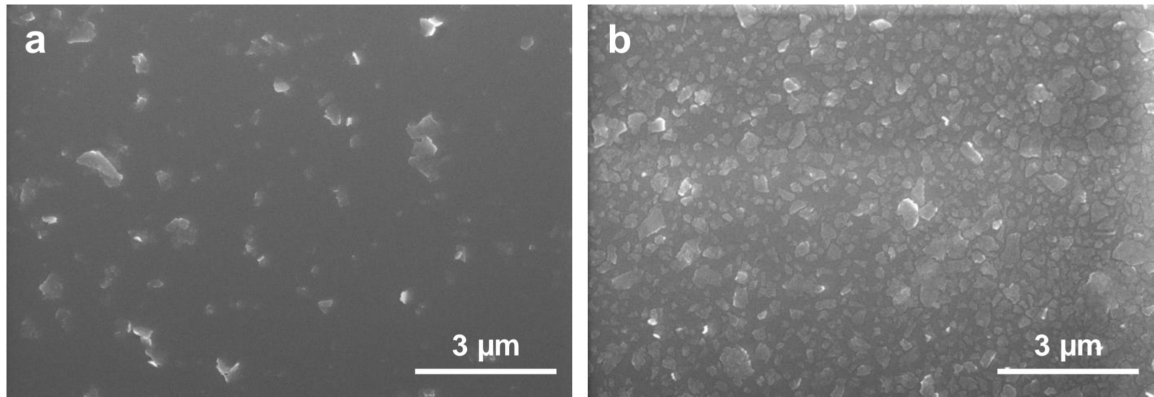

Figure 4.3. SEM images of exfoliated MoS_2 flakes on Si/SiO_2 wafer which is fabricated by spin coating for (a) 1 time and (b) 5 times.

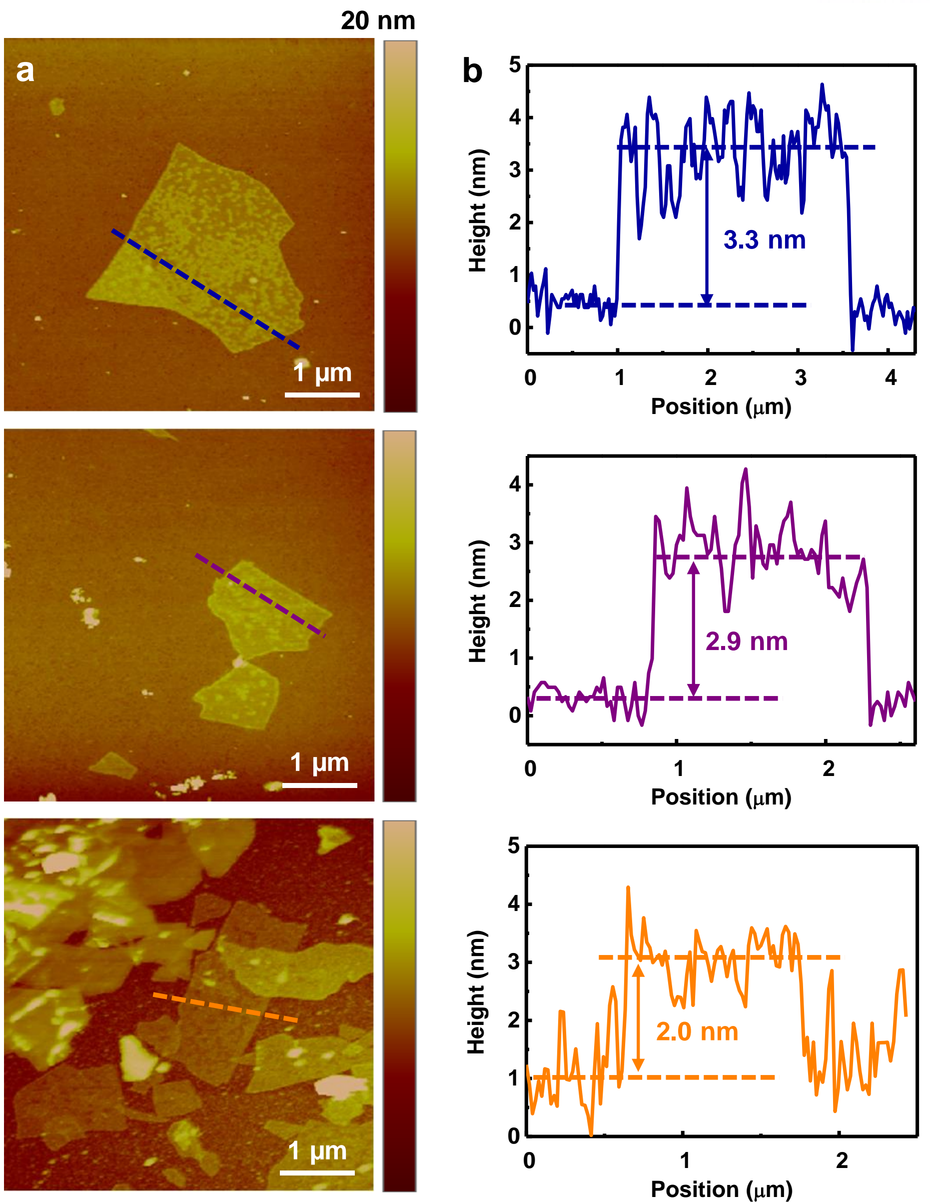

Figure 4.4. (a) AFM images of exfoliated MoS_2 flakes on Si/SiO_2 wafer. (b) Height profiles of each flakes.

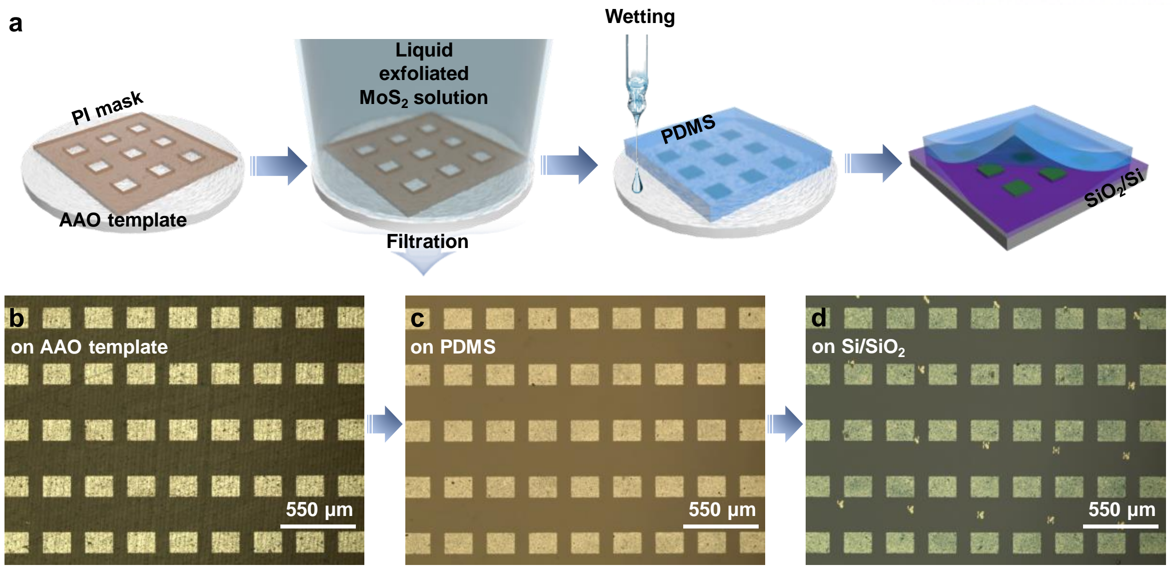

Figure 4.5. Patterning and transfer printing processes of MoS_2 array (a) Schematic illustration of vacuum filtration with PI shadow mask for patterning of MoS_2 array. Sequential images of transfer printing process of patterned MoS_2 array from (b) AAO template to (c) PDMS stamp and from PDMS stamp to (d) Si/SiO_2 wafer.

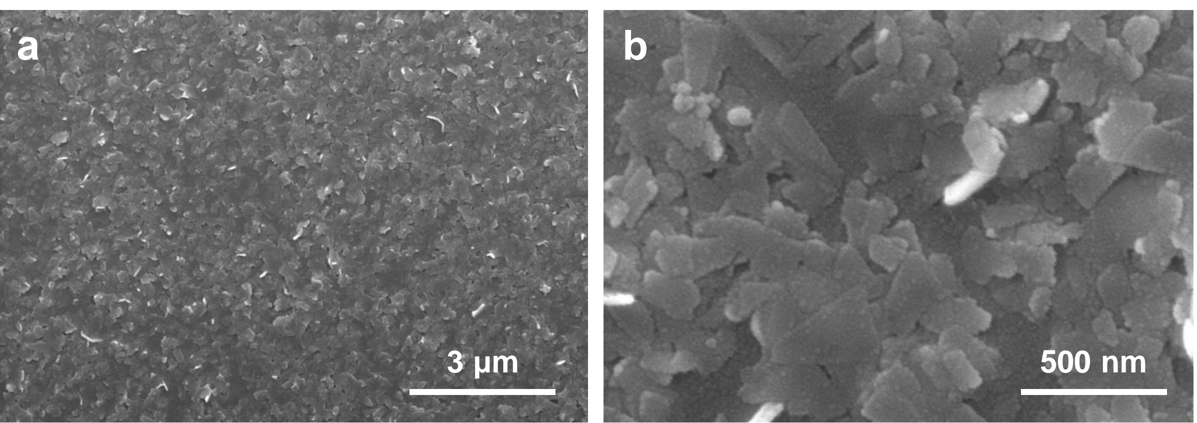

Figure 4.6. (a) SEM images of transferred MoS_2 array on Si/SiO_2 after vacuum filtration. (b) Enlarged SEM image of (a).

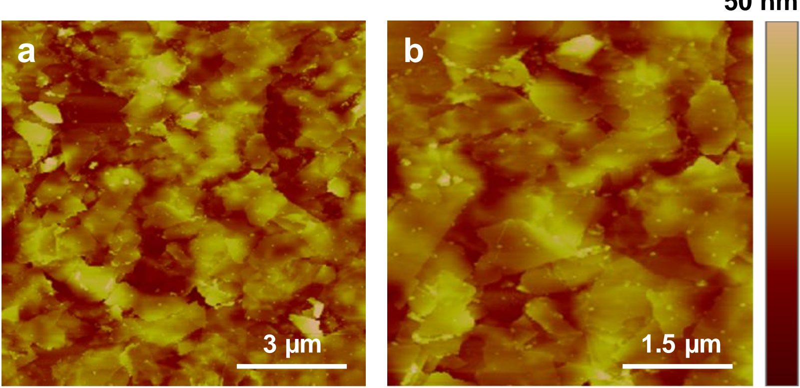

Figure 4.7. (a) AFM images of transferred MoS_2 array on Si/SiO_2 after vacuum filtration. (b) Enlarged AFM image of (a).

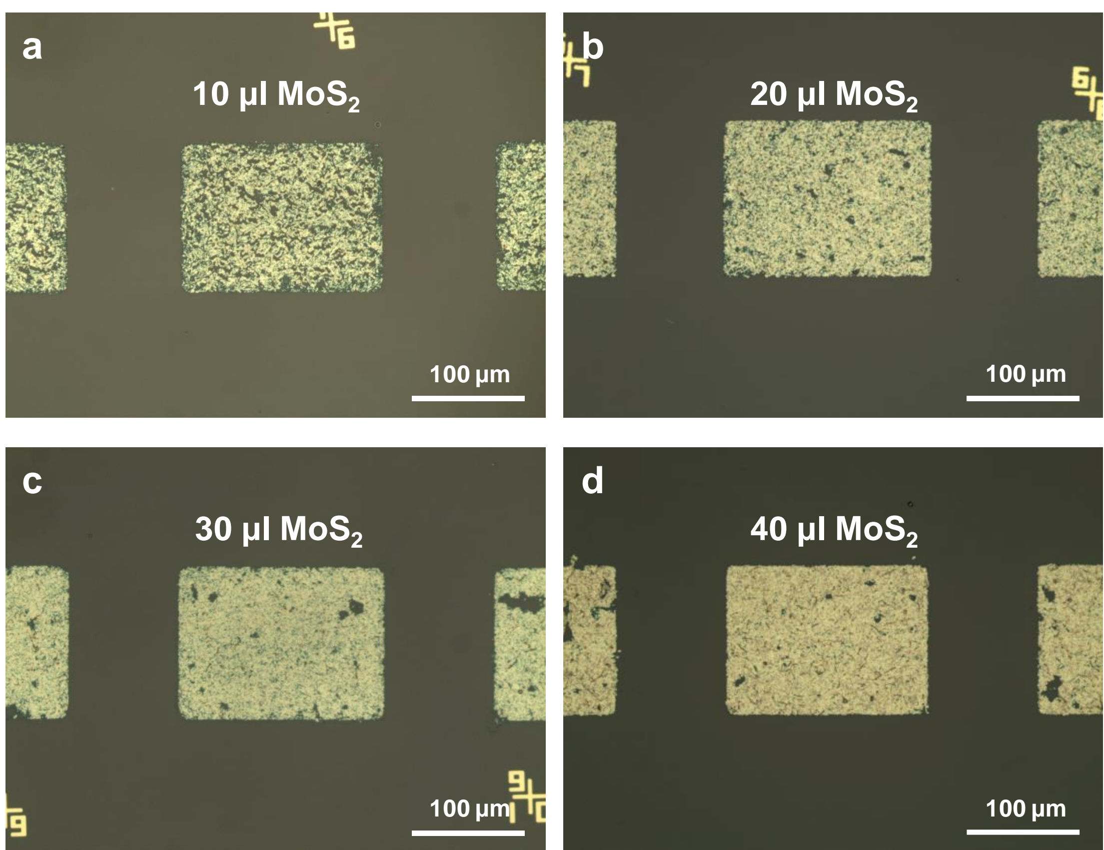

Figure 4.8. Optical microscope images of MoS_2 array on Si/SiO_2 as the amount of used MoS_2 solution. (a) Using 10 μl of MoS_2 solution. (b) Using 20 μl of MoS_2 solution. (c) Using 30 μl of MoS_2 solution. (d) Using 40 μl of MoS_2 solution.

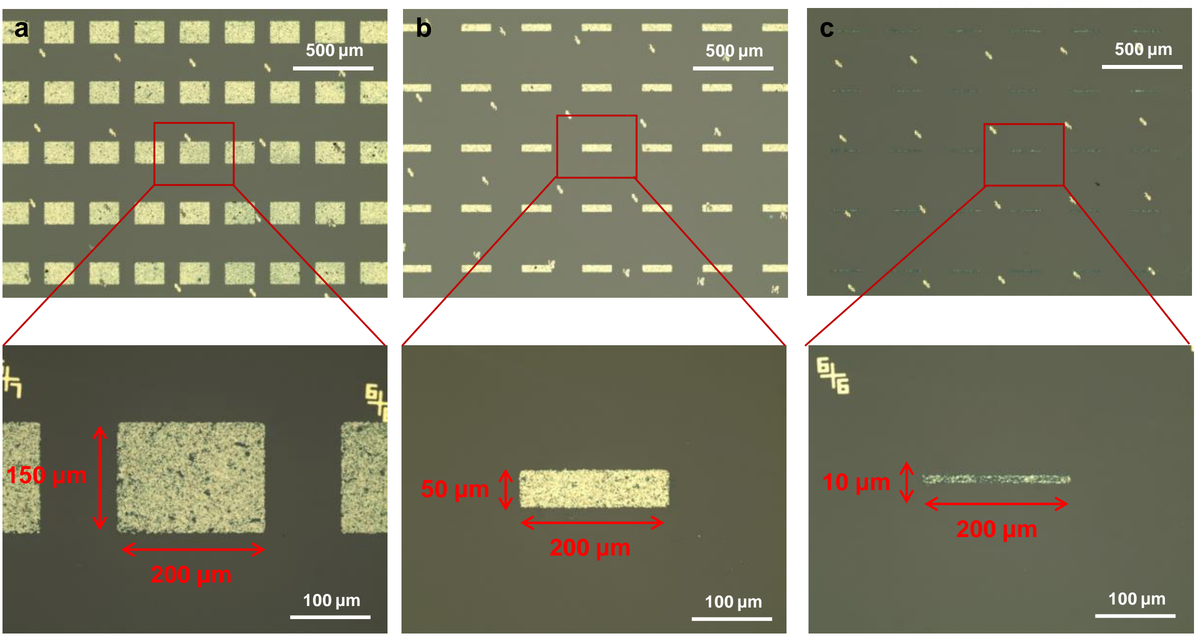

Figure 4.9. Optical microscope images of MoS_2 array on Si/SiO_2 with different widths. (a) Width of 150 µm pattern. (b) Width of 50 µm pattern. (c) Width of 10 µm pattern.

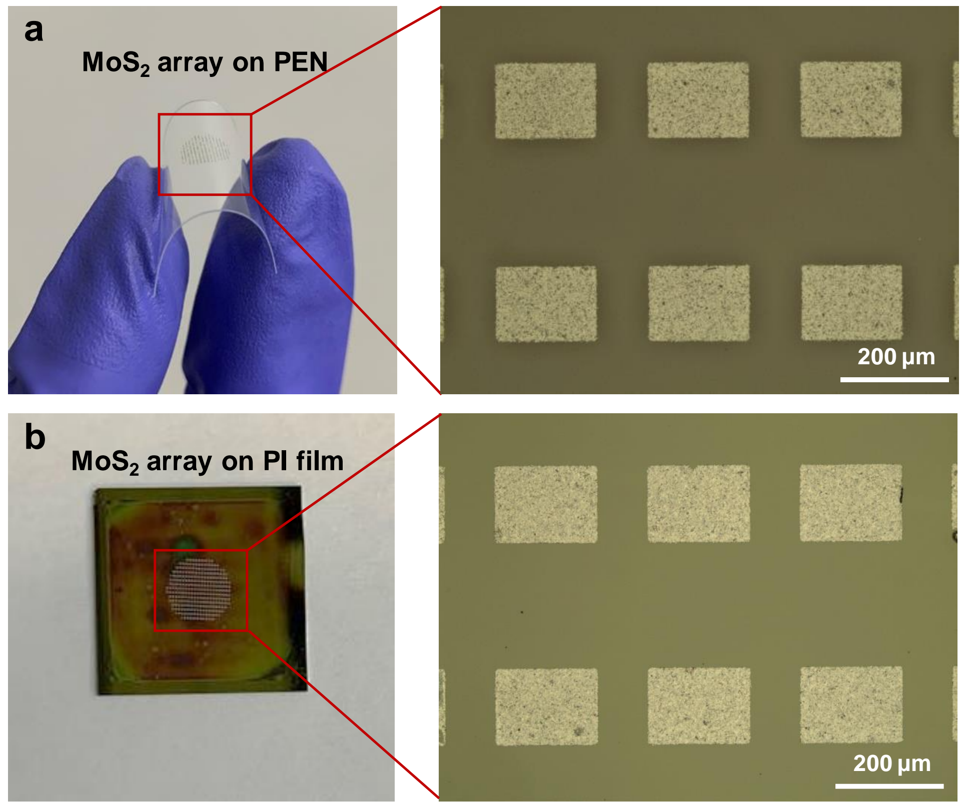

Figure 4.10. Photographs and optical microscope images of patterned MoS_2 array on (a) PEN and (b) PI substrates.

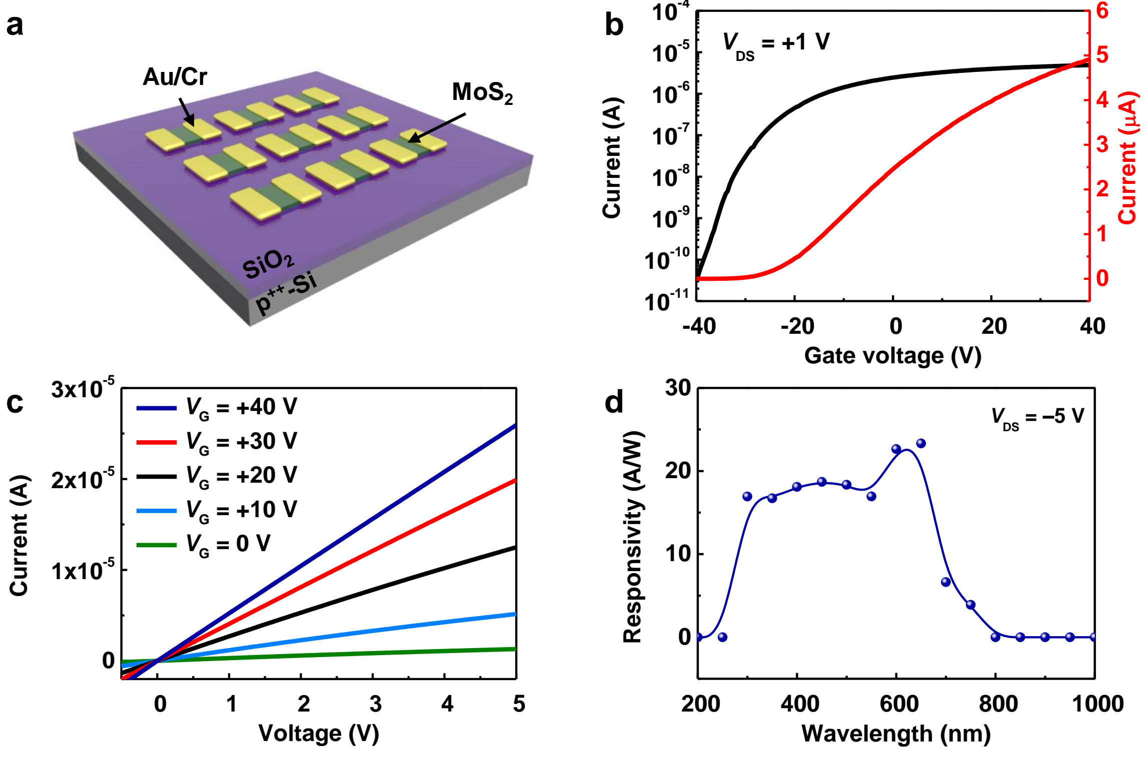

Figure 4.11. Electrical and optoelectrical properties of MoS_2 array transistor. (a) Schematics of MoS_2 array transistor. (b) Transfer characteristics of MoS_2 array transistor with V_{DS} = 1 V. (c) Output characteristics MoS_2 array transistor. (d) Spectral response of MoS_2 array transistor V_{DS} = −1 V.

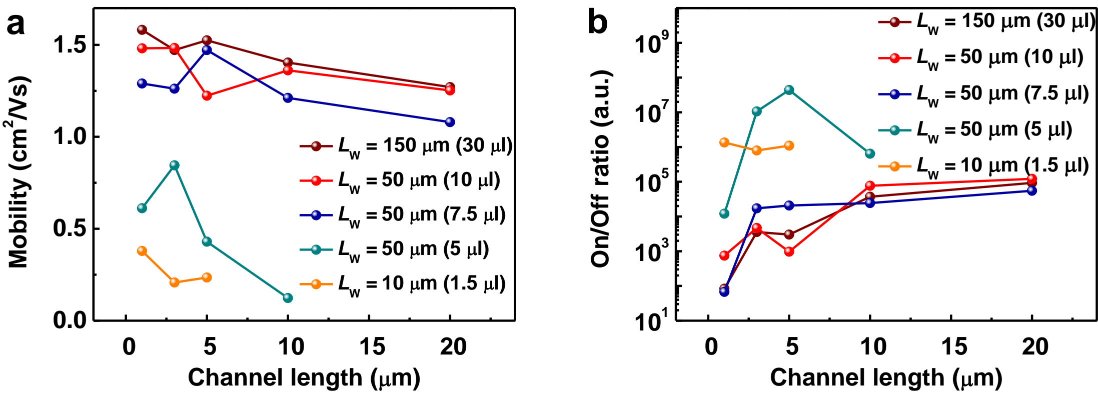

Figure 4.12. (a) The mobility values of MoS_2 array transistors as channel lengths, widths and amount of MoS_2 solutions. (b) The on/off ratio of MoS_2 array transistors as channel lengths, widths and amount of MoS_2 solutions.

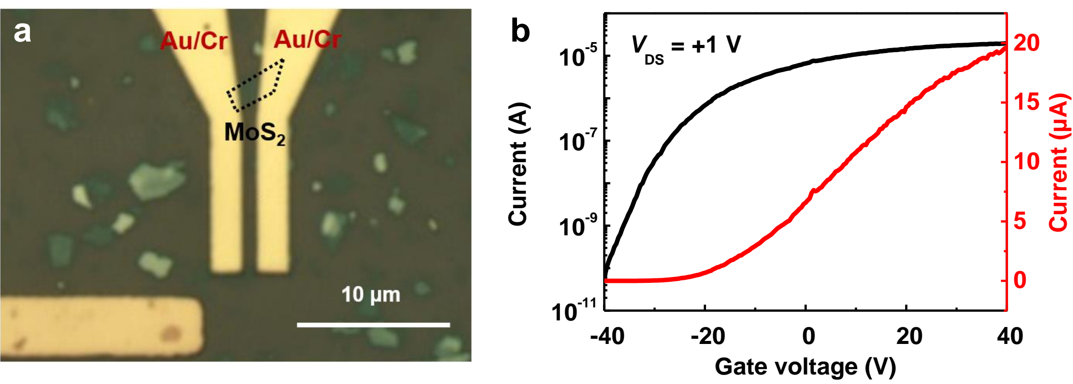

Figure 4.13. (a) Optical microscope image and (b) transfer characteristics of single MoS_2 flake transistor at V_{DS} = +1 V.

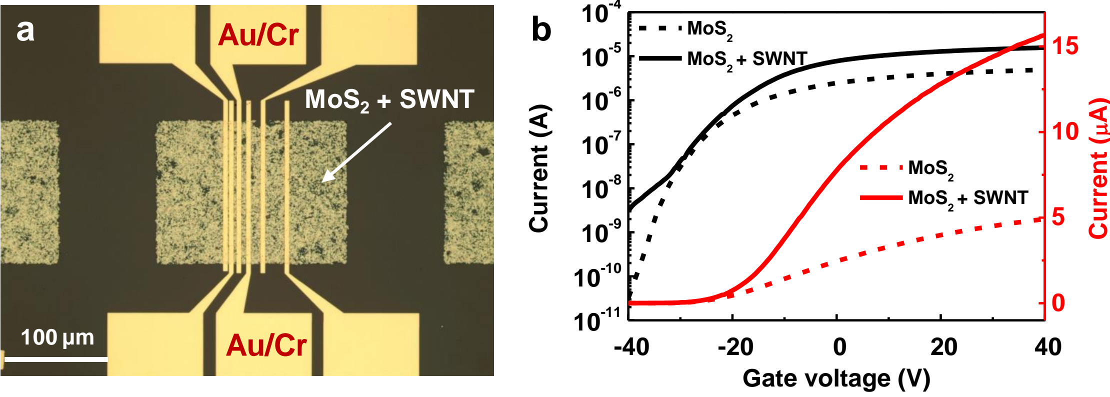

Figure 4.14. (a) Optical microscope image and (b) transfer characteristics of composite of MoS_2 and SWNT transistor at V_{DS} = +1 V.

Table 4.1. Comparison of device performance for large-area MoS_2 devices.

Synthesis	Mobility ($cm^2/V \cdot s$)	On/Off ratio	Photoresponsivity (A/W)	Reference
Liquid exfoliation	1.2 – 2.8	$10^4 – 10^6$	20 – 30	This work
Liquid exfoliation	7 – 11	10^6	–	22
CVD growth	6 – 11	10^6	–	34
Solution process	14	10^2	–	35
Solution process	0.01	10^2	10^{-6}	36
Liquid exfoliation	–	–	4	37
PLD growth	–	–	10^{-2}	38
Solution process	–	–	21.8	33

Chapter 5. Summary and Future Perspective

In this thesis, we demonstrated multi-functional devices based on the heterostructure of nanomaterials by using transfer printing technique for future electronics. Especially, diverse nanomaterials such as compound semiconductor, 2D materials and nanowires are employed in heterostructure for adoption of novel features of each material. For efficient assembly of nanomaterials, we conjugated the transfer printing technique, resulting in successful fabrication of multi-functional heterostructures without restriction of material choice. Based on these concepts, the heterojunction diode which can act as diode, transistor, memory device and photodetector was developed by assembly of compound semiconductor and 2D material. Moreover, flexible photodetector was embodied by patterning of AgNWs with vacuum filtration and transfer printing. For practical applications of 2D materials, we also introduced large-area MoS_2 devices on arbitrary substrate through efficient liquid exfoliation and water-assisted transfer printing technique. These demonstrations of multi-functional devices and fabrication methods have facilitated further development and understanding for potential applications of heterostructure.

In chapter 1, we briefly introduced the research background and promising perspective of electronics. In addition, we explained various types of heterostructure, including diodes, transistors, memory devices and photodetectors, for multi-functionalities with figures of merit in performance. Furthermore, the concept of transfer printing with several strategies for efficient transfer was discussed for the realization of heterostructures.

In chapter 2, a new type of heterojunction diode based on BP and n-InGaAs nanomembrane semiconductors was demonstrated for multi-functional applications. Here, the heterojunction was fabricated by epitaxial layer transfer printing of n-InGaAs nanomembrane on the mechanically exfoliated BP layer. The fabricated device exhibited programmable, gate-tunable, and photoresponsive properties, which has multi-functionalities in one device. In detail, the heterojunction diodes possessed gate-controlled rectification with the maximum rectification ratio of 4600, mobility value of 84.6 $cm^2 V^{-1} s^{-1}$, on/off ratio exceeding 10^5 and photoresponsivity value of 0.704 $A W^{-1}$ in a spectral range spanning the UV to NIR. Moreover, charge trapping in the native phosphorus oxide enables to the operation as programmable diode where the rectifying ratio could be tuned and memorized from 0.06 to 400, simultaneously. Furthermore, the heterojunction diode generated various electrical signals in response to specific stimuli such as applied gate voltage and illuminated light. The proposed heterostructure provides an efficient platform for the development of multi-functional future electronics such as advanced logic circuits, controllable electric transformers and neuromorphic applications.

In chapter 3, we demonstrated flexible and semi-transparent UV photodetector based on novel

patterning method for AgNWs and transfer printing. For cost-effective patterning, vacuum filtration with PI shadow mask was employed because of no wastage of AgNW solution, compared spin or spray coating processes. This patterning technique enables patterned AgNWs to be loaded on desired substrates, such as Si wafer, PET, and glass, without critical damages on AgNWs. By using this method, UV photodetector based on ZnO film with embedded AgNWs pattern was fabricated, resulting in highly enhanced photocurrent (up to 800%) compared to the AgNWs film electrodes due to increased contact area. In addition, our UV photodetector showed excellent flexibility (well operating in bending radius of approximately 770 μm) and durability (minimal change in photocurrent over 500 bending cycles). We anticipate the demonstrated patterning method for AgNWs can be used to develop flexible and transparent optoelectronic devices.

In chapter 4, we introduced the large-area devices based on MoS_2 for high-performance optoelectronics. The MoS_2 array could be produced by liquid exfoliation with the intercalation of TBA^+ cations and vacuum filtration. Finally, MoS_2 array was transferred to arbitrary substrates such as Si wafer, PEN and PI film through water-assisted transfer printing technique. The fabricated MoS_2 array transistor possessed electron mobility value of 1.5 $cm^2 V^{-1} s^{-1}$, on/off ratio of 10^5 and photoresponsivity of 24 A W^{-1} owing to the efficient exfoliation with reduced time for ultrasonication. Moreover, the solution-processable MoS_2 enables the assembly with high conductive SWNT, resulting in improved mobility up to 2.8 $cm^2 V^{-1} s^{-1}$. The proposed method and large-area MoS_2 devices show probability of MoS_2 for potential applications in high-performance, flexible and multi-functional electronics.

Overall, this thesis covers various heterostructures comprising nanomaterials for multi-functional applications. These novel design and fabrication method allow to utilize the unique properties of each materials for reserving functionalities and enhancing performance. To following trends with the development of technology, the electronic devices must secure high-performance as well as multi-functionalities for human convenience. Furthermore, the next-generation electronic devices will require human compatibility, derived from the progress of IoT, which is hard to be achieved by conventional semiconductor materials. In terms of these points, the suggested heterostructures and fabrication methods in this thesis can contribute to develop novel design of multi-functional electronics with diverse architectures and nanomaterials such as wearable electronics, flexible display and neuromorphic memory devices.

Appendix: List of Achievements

Research publications related with this dissertation (†: Equal contribution)

1. Doo-Seung Um†, **Youngsu Lee**†, Taehyo Kim, Seongdong Lim, Hochan Lee, minjeong Ha, Ziyauddin Khan, Saewon Kang, Minsoo P Kim, Jin Young Kim*, and Hyunhyub Ko*, "High-Resolution Filtration Patterning of Silver Nanowire Electrodes for Flexible and Transparent Optoelectronic Devices", *ACS Appl. Mater. Interfaces*, **2020**, *12*, 32154.

2. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, Hochan Lee, Minsoo P. Kim, Tzu-Yi Yang, Yu-Lun Chueh, Hyung-jun Kim, and Hyunhyub Ko*, "Gate-Tunable and Programmable n-InGaAs/Black Phosphorus Heterojunction Diodes", *ACS Appl. Mater. Interfaces*, **2019**, *11*, 23382.

Research publications related with the others (†: Equal contribution)

1. Yoojeong Park, Young-Eun Shin, Jonghwa Park, **Youngsu Lee**, Minsoo P. Kim, Young-Ryul Kim, Sangyun Na, Sujoy Kumar Ghosh, and Hyunhyub Ko*, "Ferroelectric Multilayer Nanocomposites with Polarization and Stress Concentration Structures for Enhanced Triboelectric Performances", *ACS Nano*, **2020**, *14*, 7101.

2. Jeonghee Yeom, Ayoung Choe, Seongdong Lim, **Youngsu Lee**, Sangyun Na, and Hyunhyub Ko*, "Soft and ion-conducting hydrogel artificial tongue for astringency perception", *Sci. Adv.*, **2020**, *6*, eaba5785.

3. Jonghwa Park†, **Youngsu Lee**†, Hochan Lee†, and Hyunhyub Ko*, "Transfer Printing of Electronic Functions on Arbitrary Complex Surfaces", *ACS Nano*, **2020**, *14*, 12.

4. Seongdong Lim, Minjeong Ha, **Youngsu Lee**, Hyunhyub Ko*, "Large-Area, Solution-Processed, Hierarchical $MAPbI_3$ Nanoribbon Arrays for Self-Powered Flexible Photodetectors", *Adv. Optical Mater.*, **2018**, *6*, 1800615.

5. Minsoo P. Kim, Youngoh Lee, Yoon Hyung Hur, Jonghwa Park, Jinyoung Kim, **Youngsu Lee**, Chang Won Ahn, Seung Won Song, Yeon Sik Jung*, and Hyunhyub Ko*, "Molecular structure engineering of dielectric fluorinated polymers for enhanced performances of triboelectric nanogenerators", *Nano Energy*, **2018**, *53*, 37.

6. Seungse Cho, Saewon Kang, Ashish Pandya, Ravi Shanker, Ziyauddin Khan, **Youngsu Lee**, Jonghwa Park, Stephen L. Craig, and Hyunhyub Ko*, "Large-Area Cross-Aligned Silver Nanowire Electrodes for Flexible, Transparent, and Force-Sensitive Mechanochromic Touch Screens", *ACS*

Nano, **2017**, *11*, 4346.

7. Seongdong Lim, Doo-Seung Um, Minjeong Ha, Qianpeng Zhang, **Youngsu Lee**, Yuanjing Lin, Zhiyong Fan, and Hyunhyub Ko*, "Broadband omnidirectional light detection in flexible and hierarchical ZnO/Si heterojunction photodiodes", *Nano Res.*, **2017**, *10*, 22.

8. Ziyauddin Khan, Seungyoung Park, Soo Min Hwang, Juchan Yang, **Youngsu Lee**, Hyun-Kon Song, Youngsik Kim, and Hyunhyub Ko*, "Hierarchical urchin-shaped α–MnO_2 on graphene-coated carbon microfibers: a binder-free electrode for rechargeable aqueous Na-air battery", *NPG Asia Mater.*, **2016**, *8*, e294.

9. Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, Seungyoung Park, Hochan Lee, and Hyunhyub Ko*, "High-Performance MoS_2/CuO Nanosheet-on-One-Dimensional Heterojunction Photodetectors", *ACS Appl. Mater. Interfaces*, **2016**, *8*, 33955.

10. Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, Jonghwa Park, Wen-Chun Yen, Yu-Lun Chueh, Hyung-jun Kim, and Hyunhyub Ko*, "InGaAs Nanomembrane/Si van der Waals Heterojunction Photodiodes with Broadband and High Photoresponsivity", *ACS Appl. Mater. Interfaces*, **2016**, *8*, 26105.

11. Hochan Lee, Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, Hyung-jun Kim and Hyunhyub Ko*, "Octopus-Inspired Smart Adhesive Pads for Transfer Printing of Semiconducting Nanomembranes", *Adv. Mater.*, **2016**, *28*, 7457.

12. Jonghwa Park, Youngoh Lee, Jaehyung Hong, **Youngsu Lee**, Minjeong Ha, Youngdo Jung, Hyuneui Lim, Sung Youb Kim, and Hyunhyub Ko*, "Tactile-Direction-Sensitive and Stretchable Electronic Skins Based on Human-Skin-Inspired Interlocked Microstructures", *ACS Nano*, **2014**, *8*, 12020.

13. Jonghwa Park, Youngoh Lee, Seongdong Lim, **Youngsu Lee**, Youngdo Jung, Hyuneui Lim, Hyunhyub Ko*, "Ultrasensitive piezoresistive pressure sensors based on interlocked micropillar arrays", *BioNanoScience*, **2014**, *4*, 349.

14. Yun-Suk Yang, Doo-Seung Um, **Youngsu Lee**, JaeKyun Shin, Joonyeon Chang, Hyun Cheol Koo, Hyunhyub Ko*,and Hyung-jun Kim*, "Spin injection and detection in $In_{0.53}Ga_{0.47}As$ nanomembrane channels transferred onto Si substrates", *Appl. Phys. Express*, **2014**, *7*, 093004.

15. Doo-Seung Um, Seongdong Lim, **Youngsu Lee**, Hochan Lee, Hyung-jun Kim, Wen-Chun Yen, Yu-Lun Chueh, and Hyunhyub Ko*, "Vacuum-Induced Wrinkle Arrays of InGaAs Semiconductor Nanomembranes on Polydimethylsiloxane Microwell Arrays", *ACS Nano*, **2014**, *8*, 3080.

16. Jiwon Lee, Bo Hua, Seungyoung Park, Minjeong Ha, **Youngsu Lee**, Zhiyong Fan*, and Hyunhyub

Ko*, "Tailoring surface plasmons of high-density gold nanostar assemblies on metal films for surface-enhanced Raman spectroscopy", *Nanoscale*, **2014**, *6*, 616.

Conference presentations

1. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, and Hyunhyub Ko, "Patterning Technique of Silver Nanowire Electrodes for Flexible and Transparent Photodetector", *The polymer Society of Korea* **2020**, Korea.
2. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, and Hyunhyub Ko, "Black Phosphorus/n-InGaAs Heterojunction for Multi-Functional Programmable Diode", *European Materials Research Society* **2018** (E-MRS 2018 Spring Meeting), France.
3. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, and Hyunhyub Ko, "Gate Tunable Black Phosphorus and p-InGaAs Hetero-Junction Diode for Multi-Functional Devices", *The 16th International Meeting on Information Display* **2016** (IMID 2016), Korea.
4. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, and Hyunhyub Ko, "Multi-Functional Devices Based on Black Phosphorus and p-InGaAs Hetero-Junction Diode", *The Korean Institute of Electrical and Electronic Material Engineers* **2016** (KIEEME 2016 Summer Conference), Korea.
5. Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, and Hyunhyub Ko, "High Resolution Patterning of Silver Nanowires for Flexible and Transparent Photodetector Arrays", *Materials Research Society of Korea* **2016** (MRS-K 2016 Spring Meeting), Korea.
6. Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, and Hyunhyub Ko, "Epitaxial Transfer Printing of High-Performance III–V/Si Hetero-Junction Photodiodes", *Materials Research Society* **2015** (MRS 2015 Spring Meeting), USA.
7. **Youngsu Lee**, Doo-Seung Um, Seongdong Lim, and Hyunhyub Ko, "Gate Tunable and Multi-Functional Black Phosphorus and p-InGaAs Hetero-Structure Device", *The Korean Institute of Chemical Engineers* **2015** (KIChE 2015 Fall Conference), Korea.
8. Doo-Seung Um, **Youngsu Lee**, Seongdong Lim, and Hyunhyub Ko, "III–V/Si Hetero-Junction Photodiode by Epitaxial Layer Transfer", *11th Korea-Japan Symposium on Materials and Interfaces* **2014**, Korea.

Awards

1. Poster award in 2018 E-MRS spring meeting, Symposium – Epitaxial integration of dissimilar materials: challenges and fundamentals, *European Materials Research Society* **2018**.
2. 22nd Humantech paper award, Bronze award in Physical Devices, *Samsung Electronics* **2016**.
3. Outstanding poster paper award, *The 16th International Meeting on Information Display* **2016**.

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