Control of Incoming Drain Currents Drawn by Super-Junction MOSFETs in Voltage Source Bridge-Legs

Zhengyang Feng
Department of Electronic & Electrical Engineering
University of Strathclyde
Glasgow, UK
zhengyang.feng@strath.ac.uk

Neville McNeill
Department of Electronic & Electrical Engineering
University of Strathclyde
Glasgow, UK
neville.mcneill@strath.ac.uk

Barry Williams
Department of Electronic & Electrical Engineering
University of Strathclyde
Glasgow, UK
barry.williams@strath.ac.uk

***Abstract*—To increase the efficiency of renewable energy power conversion systems, traditional silicon IGBTs can be replaced with silicon super-junction MOSFETs. However, the poor performance of the MOSFET's intrinsic diode and the output capacitance present difficulties in voltage source converter bridge-legs. When a MOSFET in this circuit turns on, a charging current has to be sourced into the output capacitance of the complementary freewheeling MOSFET, even if the diode has been deactivated. The peak incoming drain current into the MOSFET turning on can be limited by using a large resistance in series with its gate. However, this increases MOSFET power dissipation. Also, the turn-on propagation delay time is increased. This paper presents a gate driver circuit for profiling the MOSFET's incoming drain current to provide an improved trade-off between incoming peak current, turn-on power dissipation, and delay time.**

Keywords—control, converter, current transformer, gate driver, MOSFET, super-junction.

I. Introduction

High power conversion efficiencies are desirable in many renewable energy applications. The traditional silicon IGBT can be replaced with wide band-gap (WBG) devices including silicon carbide (SiC) MOSFETs, SiC JFETs, and GaN HEMTs. WBG devices [1] offer excellent performance. However, they present challenges. For example, d*v*/d*t*-induced conduction and gate threshold shift can be problems with the SiC MOSFET [2].

Another alternative to the IGBT is the silicon super-junction (SJ) MOSFET. This device has a low on-state resistance $R_{DS(on)}$, is fast-switching and exhibits good short-circuit withstand times [3]. The SJ MOSFET is effective in single-ended converters such as the boost converter when used in conjunction with a SiC Schottky diode [4]. However, the voltage source converter (VSC) bridge-leg is a key element in many renewable power systems, such as with wind turbine generators. In VSCs the high reverse recovery charge Q_{rr} passed by the Si SJ MOSFET's intrinsic diode, and its highly non-linear output capacitance C_{oss} [5] present challenges.

Solutions include the use of auxiliary bridge-legs [6], switching-aid circuits [7], and intelligent commutation schemes such as those in [8] and [9]. SJ MOSFETs can be deployed in a VSC operating in the synchronous conduction mode. However, a variable switching frequency is used, so AC filter design is challenging. The functionality of a VSC can be realized by combining single-ended converters in, for example, the dual-buck arrangement in [10] but factors such as choke utilization can be problematic. As an alternative to the VSC, the SJ MOSFET has been shown to perform effectively in both the current source converter (CSC) [11], and the impedance source converter (ZSC) [12]. However, challenges with the CSC include the need to invert the DC voltage if the power flow is to be reversed. The ZSC requires additional components to form the required impedance network. For these and other reasons, the VSC tends to be prevalent in practical power systems.

II. Background: Dual-Mode Control Technique

A. Operating Principle

Fig. 1(a) shows a bridge-leg with MOSFET intrinsic diode deactivation circuitry incorporated. When a MOSFET would be freewheeling, the reverse current, rather than flowing into its intrinsic diode, will flow into the parallel external diode because of the blocking action of the series diode. The external diodes can be purpose-designed types with good reverse recovery characteristics, such as SiC Schottky types. However, the highly non-linear output capacitance C_{oss} of the MOSFET in the freewheeling position is still problematic.

[13] proposed using a dual-mode control technique in conjunction with the circuitry in Fig. 1(a) to address the remaining problem presented by C_{oss}, shown in Fig. 2(a). In the so-called fast-switching mode, the bridge-leg operates with unipolar PWM modulation according to the direction of the AC load current. Under unipolar PWM modulation, the MOSFET in the freewheeling location is not turned on during a switching cycle. Consequently, its C_{oss} is only partially discharged. This is shown in Fig. 1(b), where C_{oss} discharges down to the reverse breakdown voltage of D_s which is appropriately chosen to be above the voltage of the knee point of the *Q*-*V* curve in Fig. 2(a). In this mode, *TR*1 and *TR*2 do not have to dissipate the full co-energy lying under the curve in Fig. 2(a) in the course of charging the C_{oss} of the complementary device. *TR*1 and *TR*2 are driven with rapid switching for low losses.

At low i_{LOAD} magnitudes, bipolar PWM modulation is enabled to reduce crossover distortion in the AC current. The problem of high peak currents due to supplying high charges into fully-discharged C_{oss} capacitances that occurs with bipolar modulation, is addressed by turning the SJ MOSFETs on slowly (the so-called slow-switching mode) and thereby limiting the d*i*/d*t* in the current conducted by the incoming MOSFET as shown in Fig. 2(b). Fig. 3 shows simulation results for the dual-mode technique over one base-frequency cycle of i_{LOAD}, where the fast-switching and slow-switching modes are selected according to the magnitude of i_{LOAD}. The

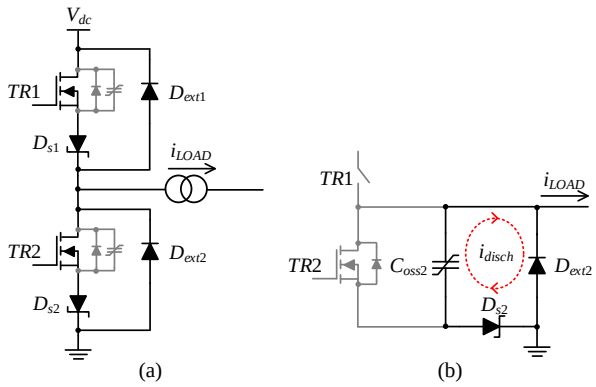

Fig. 1 (a) Voltage source bridge-leg based around SJ MOSFETs equipped with intrinsic diode deactivation circuitry. (b) Route taken by discharge current from output capacitance C_{oss2} when $TR1$ is off and $TR2$ is freewheeling.

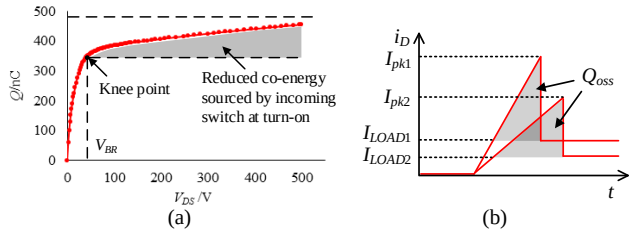

Fig. 2 (a) Q-V curve of IPW60R041P6 SJ MOSFET's C_{oss}. (b) Same Q_{oss} under different I_{LOAD} and different slew rate where load current $I_{LOAD1} > I_{LOAD2}$, peak current $I_{pk1} > I_{pk2}$.

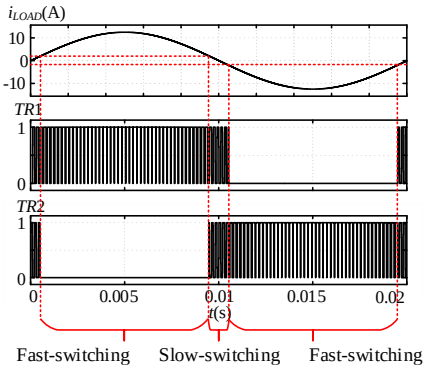

Fig. 3 Simulation results of dual-mode control technique.

dual-mode technique was demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC supply voltage, and switching at 20 kHz in [13]. The full-load efficiency was 98.7%, compared with 97.5% measured with a benchmark circuit using IGBTs. A feature of the technique is that compared to, for example, [6]-[9], little extra hardware is required. Also, the SJ MOSFETs do not have to support over-voltages during the resetting action of switching-aid inductors, as in [7].

With respect to Fig. 1(a), DeWitt *et al.* proposed a technique in [14] where the series diodes are replaced with low breakdown voltage MOSFETs. This reduces the conduction losses of the series elements as the MOSFETs act as synchronous rectifiers, with smaller voltage drops than series diodes. However, as with the basic circuitry in Fig. 1(a), this still does not address the problem of the non-linear MOSFET output capacitances.

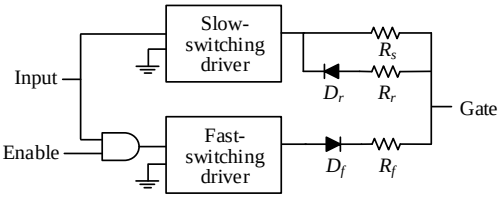

Fig. 4 Dual-mode gate driver circuit from [13].

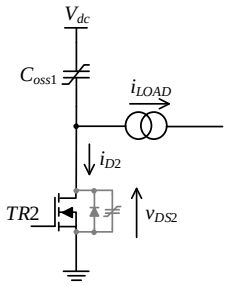

Fig. 5 Equivalent circuit from bridge-leg in Fig. 1(a) when i_{LOAD} is negative and $TR2$ is turning on, and the intrinsic diode in $TR1$ has been deactivated.

B. *Dual-Mode Gate Driver Hardware*

Fig. 4 shows the dual-mode gate driver circuit. When the slow-switching mode is selected, only the slow-switching driver operates and the MOSFET's input capacitance C_{iss} is charged at turn-on via the relatively high-value resistance R_s. When the fast-switching driver is enabled, C_{iss} is charged more rapidly via the parallel combination of R_s, and the much smaller resistance R_f.

C. *Issues with Incoming Current Profile in Slow-Switching Mode*

In Fig. 5, the turn-on action of $TR2$ is considered when the bridge-leg has i_{LOAD} flowing into its mid-point. i_{LOAD} is taken as being low, and hence the converter is operating in the slow-switching mode. If the intrinsic diode of $TR1$ has been deactivated effectively, $TR1$'s equivalent circuit can be approximated solely by its output capacitance C_{oss1}. The reverse recovery charge of D_{ext2} is low in comparison with that drawn by C_{oss1}, so D_{ext2} is neglected here.

In Fig. 5, the peak incoming drain current i_{D2} is limited by using a large gate resistance. A feature of this arrangement is the inherently triangular incoming drain current profile with respect to time, as shown in Fig. 6. When the gate-source voltage v_{GS} reaches its threshold level $V_{GS(th)}$ at Point A, the MOSFET has the full supply voltage V_{dc} across its drain-source terminals. It then begins to conduct whilst in the pinch-off condition, and still supports virtually all of V_{dc}. i_{D2} rises approximately linearly until the bulk of the total charge Q_{oss} has been supplied into C_{oss1} at Point B. During this phase v_{GS} has increased in an approximately linear manner with respect to time as the change in v_{GS} has been over only a small section of an exponential curve. At Point B, C_{oss1} falls abruptly and, in moving to Point C, i_{D2} falls to the steady-state load current level and v_{DS2} falls from the rail voltage to virtually zero.

A disadvantage of the triangular current profile is that the overshoot current I_{os}, as defined in Fig. 6(c), is high. When C_{oss1} falls, a high current has been established in both $TR1$ and $TR2$. Interrupting this current can result in high-frequency oscillations in the voltage at the source of $TR1$. This, in turn, can result in a transient voltage exceeding V_{dc} appearing across $TR1$, and an EMI signature with a raised high-frequency

content. I_{os} can be reduced by switching more slowly to address these problems shown in Fig. 2(b). However, this incurs increased losses in the MOSFET as it spends more time with the rail voltage across it whilst conducting both i_{LOAD} and the C_{oss}-charging current.

Using a large gate resistance to reduce the turn-on speed of a MOSFET has a further disadvantage as the time delay D between the gate signal from the driver IC going high and the MOSFET's gate voltage reaching its threshold value becomes lengthened. Distortion results in the output voltage and current due to this propagation delay between the MOSFET being signalled on and its drain-source voltage falling.

With respect to the waveforms in Fig. 6(c), Q_{oss} is given by

$$Q_{oss} = 1/2\, t_2\, I_{os}. \tag{1}$$

(1) is rearranged to give

$$t_2 = \frac{2\, Q_{oss}}{I_{os}}. \tag{2}$$

The rate of rising of i_{D2} is taken as being the same during the intervals t_1 and t_2, and therefore

$$\frac{I_{LOAD}}{t_1} = \frac{I_{os}}{t_2}. \tag{3}$$

(3) is rearranged to give

$$t_1 = \frac{I_{LOAD}}{I_{os}}\, t_2. \tag{4}$$

Putting the result from (2) into (4) gives

$$t_1 = \frac{2\, I_{LOAD}\, Q_{oss}}{{I_{os}}^2}. \tag{5}$$

The results from (2) and (5) are added to give the total time T_{TOTAL} for i_{D2} to rise from 0 A to $I_{LOAD} + I_{os}$:

$$T_{TOTAL} = \frac{2\, Q_{oss}}{I_{os}} \left(\frac{I_{LOAD}}{I_{os}} + 1 \right). \tag{6}$$

The energy dissipation $E_{on(tri)}$ in $TR2$ with a triangular incoming drain current trajectory is given by

$$E_{on(tri)} = V_{dc} \left(\frac{I_{LOAD} + I_{os}}{2} \right) T_{TOTAL}. \tag{7}$$

Putting the result from (6) into (7), and rearranging yields

$$E_{on(tri)} = V_{dc}\, Q_{oss} \left(1 + \frac{2\, I_{LOAD}}{I_{os}} + \frac{{I_{LOAD}}^2}{{I_{os}}^2} \right). \tag{8}$$

Compared to the triangular profile, a rectangular profile, Fig. 7, would be expected to yield lower turn-on losses for a given overshoot current. With respect to the waveforms in Fig. 7, Q_{oss} is given by

$$Q_{oss} = t_1\, I_{os}. \tag{9}$$

(9) is rearranged to give

$$t_1 = \frac{Q_{oss}}{I_{os}}. \tag{10}$$

The energy dissipation $E_{on(rec)}$ in $TR2$ with a rectangular incoming drain current trajectory is given by

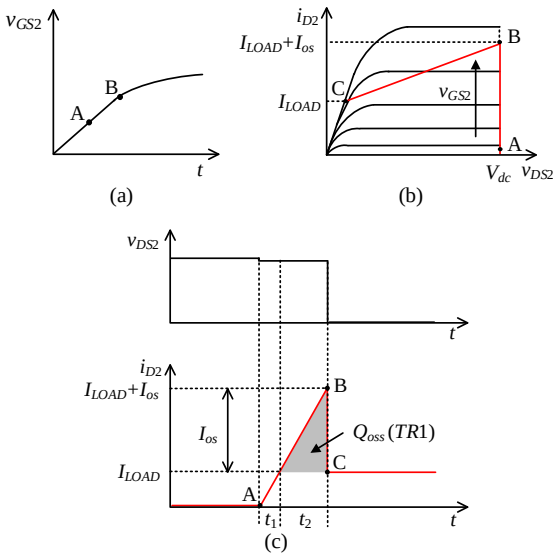

Fig. 6 Idealized behavior of SJ MOSFET in bridge-leg at $TR2$ turn-on, showing its incoming drain current profile. (a) v_{GS2} as a function of time. (b) i_{D2} as a function of v_{DS2}. (c) v_{DS2} as a function of time, i_{D2} as a function of time.

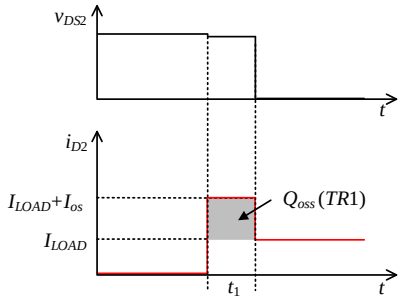

Fig. 7 Idealized rectangular incoming drain current profile.

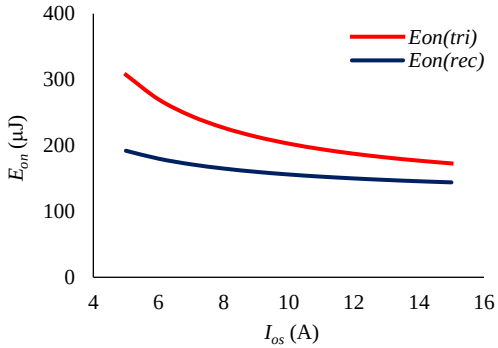

Fig. 8 Expected turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against I_{os}.

$$E_{on(rec)} = V_{dc}\, (\, I_{LOAD} + I_{os}\,)\, t_1. \tag{11}$$

The result from (10) is put into (11) to yield

$$E_{on(rec)} = V_{dc}\, Q_{oss} \left(1 + \frac{I_{LOAD}}{I_{os}} \right). \tag{12}$$

Fig. 8 shows $E_{on(tri)}$ and $E_{on(rec)}$ plotted against overshoot current I_{os} for triangular and rectangular trajectories for some representative conditions. These were V_{dc} = 400 V, I_{LOAD} = 3 A, and Q_{oss} = 300 nC. (8) and (12) were used to calculate the turn-on energies.

III. Proposed Circuitry for Realizing a Rectangular Incoming Drain Current Profile

A technique was presented in [15] for controlling the incoming diode recovery current profile drawn by a MOSFET in a single-ended converter. As shown in Fig. 9, a current transformer (CT) is used to provide a diode recovery current control arrangement. When Q_1 turns on, and the load current is commutated from D_1 to Q_1, a voltage drop across R_2 is developed as a function of the current in the primary conductor of the CT. With an appropriately chosen R_2 and CT turns-ratio, the drain current of Q_1 will be limited to a set value during the diode recovery period.

In this paper, the technique in [15] is extended to a VSC bridge-leg where the incoming drain currents in two SJ MOSFETs need to be controlled. Also, the resetting of the CT is addressed; the technique is applied in conjunction with a dual-mode gate driver arrangement; its efficacy is experimentally compared with that of a traditional arrangement where the incoming current profile is determined by simply setting the gate resistance to a desired value. A feature of the arrangement in [15] is that the CT is used to both detect the recovery current and control it. Other techniques can be used for sensing currents in power devices, for protection against short-circuits or to obtain the current profile for active shaping of currents during switching transients. Methods include the use of a Rogowski coil [16] and detection of the voltage developed across the parasitic emitter inductance of an IGBT [17], [18]. The advantage of the CT here is that its output can be used to directly control the MOSFET's drain current, without the need for integrators or other conditioning circuitry.

Figs. 10 and 11 show the proposed circuitry. In Fig. 10 it is seen that the primary winding of each CT is connected directly in series with each MOSFET. As shown in Fig. 11, the CT in each case acts to limit the gate voltage. This differs from [15] where the primary conductor of the CT limiting the current flow into a MOSFET was connected in series with the freewheeling element sourcing the incoming recovery current. It is noted that the current being directly controlled with the proposed arrangement is therefore not the reverse current through the freewheeling element, as in [15], but is the peak current I_{pk} (I_{LOAD}+I_{os}) in the incoming MOSFET. As shown in Fig. 7, I_{pk} is composed of both i_{LOAD} and the reverse current through the freewheeling element.

Neglecting any magnetizing current drawn by the CT, the secondary current i_2 is related to the primary current i_1 by

$$\frac{i_2}{i_1} = \frac{N_1}{N_2} \tag{13}$$

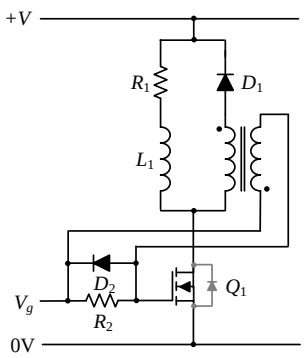

Fig. 9 Circuitry from [15].

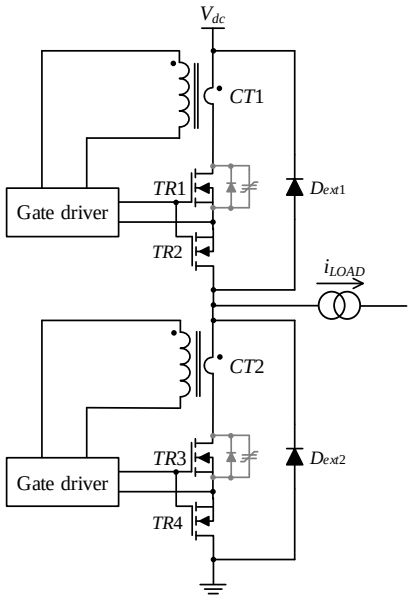

Fig. 10 Bridge-leg equipped with proposed circuitry.

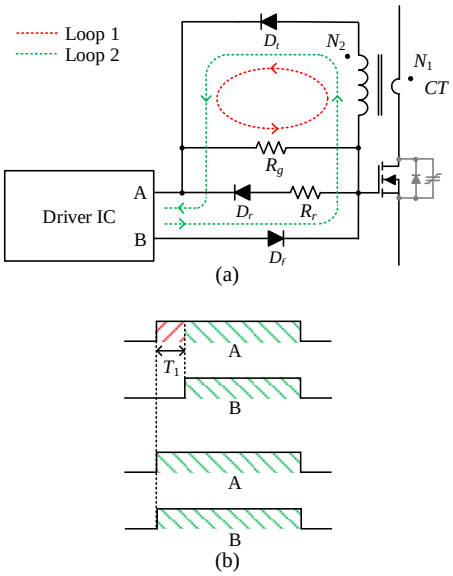

Fig. 11 (a) Local gate driver circuit. (b) Two output signals, A and B, are produced by the driver IC. In the slow-switching mode a delay time T_1 is introduced. In the fast-switching mode A and, B are synchronous.

where N_1 and N_2 are the CT's primary and secondary turns numbers respectively. If $i_1 = I_{pk}$ then

$$i_2 = \frac{N_1}{N_2} I_{pk}. \tag{14}$$

At turn-on in the slow-switching mode, only Output A of the driver IC goes high initially, and i_2 circulates in Loop 1 shown in Fig. 11(a). The voltage v_{Rg} across the resistance R_g during this interval is given by

$$v_{Rg} = R_g i_2. \tag{15}$$

Putting the result from (14) into (15) gives

$$v_{Rg} = R_g \frac{N_1}{N_2} I_{pk}. \tag{16}$$

To maintain the MOSFET in its pinch-off region, the voltage v_{Rg} across R_g is approximated by

$$v_{Rg} = V_{DRI} - V_{GS(th)} \tag{17}$$

where V_{DRI} is the high-state output voltage produced by the driver IC in Fig. 11(a) and $V_{GS(th)}$ is the MOSFET's gate threshold voltage. If this result is put into (16) which is rearranged, then

$$I_{pk} = \frac{N_2 \, (V_{DRI} - V_{GS(th)})}{N_1 \, R_g}. \tag{18}$$

After sufficient time is allowed for the turn-on action to elapse, Output B goes high. This clamps the MOSFET's gate to V_{DRI} via a low impedance route. It also allows i_2 to circulate in the short-circuit loop, Loop 2, for the rest of the MOSFET's on-time. This minimizes the current driven into the CT's magnetizing branch. At turn-on in the fast-switching mode, Outputs A and B rise simultaneously, and the output terminals of the CT are again short-circuited.

When *TR*1 is off, Outputs A and B are low. When *TR*1 is off and also acting as the freewheeling device, the charge Q_{oss} flows through the CT's primary winding when the complementary MOSFET turns on. Again, Outputs A and B present a short-circuit.

IV. Experimental Rig and Results

A. Experimental Circuitry

Key data for the bridge-leg and gate driver circuits are given in Tables I and II. However, in order to evaluate the circuitry, DC tests were carried out using the simplified bridge-leg circuits in Fig. 12.

The CT in Fig. 12(b) was assembled with a TN9/6/3 core in 3F3 material, and with N_2 formed with 50 turns of 0.2 mm diameter copper wire. The primary conductor was passed once through the CT's aperture giving $N_1 = 1$. In [19], a CT is used to measure the drain current of a 10 kV SiC MOSFET for over-current monitoring purposes. The CT's primary current in [19] has a low-frequency component, and the core is consequently gapped to avoid saturation. The primary currents in the CTs in Figs. 10, 11, and 12(b) also have a low-frequency component. However, these currents are in the form of a series of return-to-zero pulses, and the core can be reset between pulses. An un-gapped core can therefore be used without saturation occurring. As seen in Figs. 10, 11, and 12(b) the CT is operated without discrete reset circuitry, and reset occurs by means of the resonant action between the CT's magnetizing inductance and parasitic lumped capacitance during the MOSFET's off-times [20]. R_g was varied experimentally to set I_{pk}, as determined by (18).

The ancillary devices used with *TR*2 were omitted for these tests as they have little influence on the turn-on behavior of *TR*2 in this mode. In each case, *TR*1 and *TR*2 were switched in a complementary manner, as occurs in the slow-switching mode. Consequently, the C_{oss} of *TR*1 is fully discharged when *TR*2 is off. For simplicity, a MBR3060CT Schottky diode was used as the anti-series element in these tests instead of a MOSFET as shown in Fig. 10. The supply voltage V_{dc} was 400 V. The gate driver circuits for *TR*1 and *TR*2 applied an on-state gate-source voltage v_{GS} of 12 V. The off-state v_{GS} was - 3 V, and it was made negative to prevent d*v*/d*t*-induced simultaneous conduction through *TR*1 and *TR*2. The delay time *D* was defined as the interval between v_{DRI} rising and v_{DS2} falling to its 50%-level of 200 V.

TABLE I. Bridge-Leg Components for Circuitry in Fig. 10

$D_{ext1,2}$	SCS220AE
*TR*1, 3	IPW60R041P6
*TR*2, 4	IRFB7546PBF

TABLE II. Driver Circuit Components for Circuitry in Fig. 11

R_r	10 Ω
$D_{r,f}$	1N4148TR
D_t	GB01SLT12-214
Driver IC	IXDN614SI

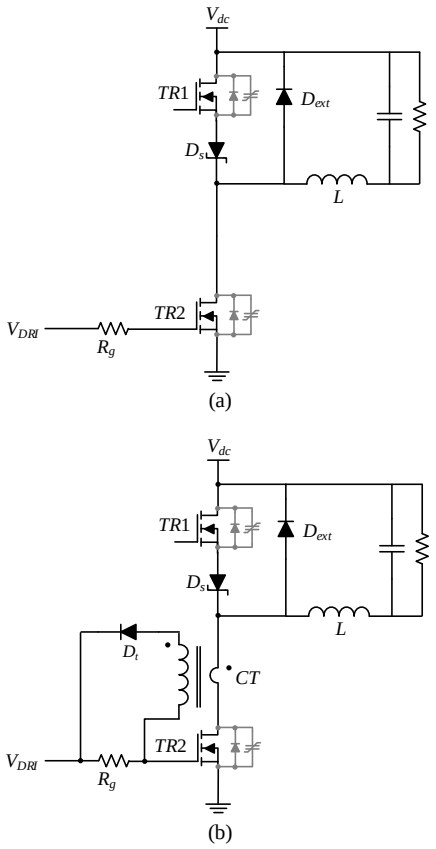

Fig. 12 Experimental circuits for evaluating methods for controlling incoming drain current profile into MOSFET at turn-on. (a) Simple resistance in series with gate for charging MOSFET input capacitance. (b) Negative feedback from current transformer.

B. Tests with Simple Resistor in Series with MOSFET's Gate Terminal

R_g in Fig. 12(a) was set at 160 Ω, 220 Ω, 300 Ω, and 360 Ω. Readings of turn-on energy $E_{on(tri)}$, peak current I_{pk}, and delay time *D* were taken for i_{LOAD} = 1 A, 2 A, 3 A, and 4 A.

Fig. 13 shows exemplifying waveforms with R_g = 300 Ω and i_{LOAD} = 3 A. w_{inst} is the instantaneous power dissipation in *TR*2 and was obtained by multiplying i_{D2} and v_{DS2} using the oscilloscope "MATH" function. Fig. 14 shows the relationship between $E_{on(tri)}$ and I_{os} for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A. Fig. 15 shows the relationship between $E_{on(tri)}$ and I_{pk} for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A. Fig. 16 shows the relationship between $E_{on(tri)}$ and *D* for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A.

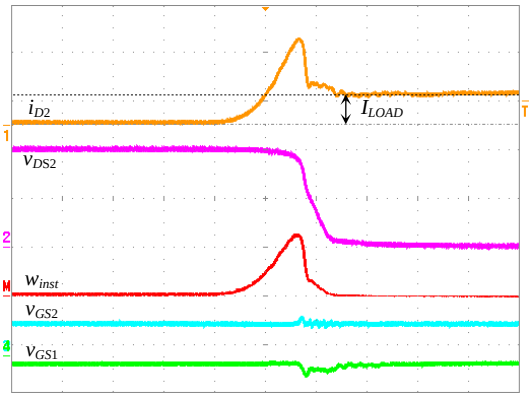

Fig. 13 Exemplifying waveforms from the scheme in Fig. 12(a) with R_g = 300 Ω and I_{LOAD} = 3 A. Scales: i_{D2} = 5 A/div., v_{DS2} = 200 V/div., w_{inst} = 2.5 kW/div., v_{GS2} = v_{GS1} = 20 V/div. Time scale = 200 ns/div.

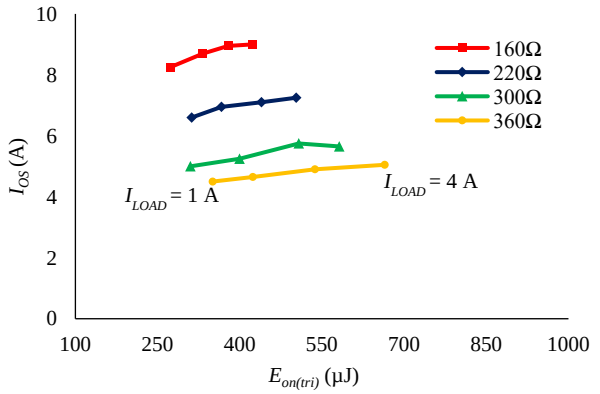

Fig. 14 Relationship between turn-on energy $E_{on(tri)}$ and overshoot current I_{os}.

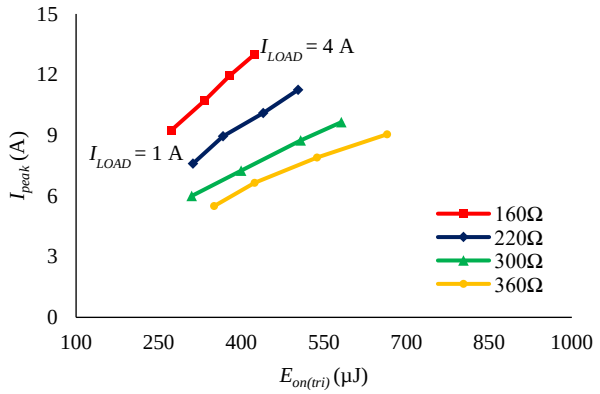

Fig. 15 Relationship between turn-on energy $E_{on(tri)}$ and peak current I_{pk}.

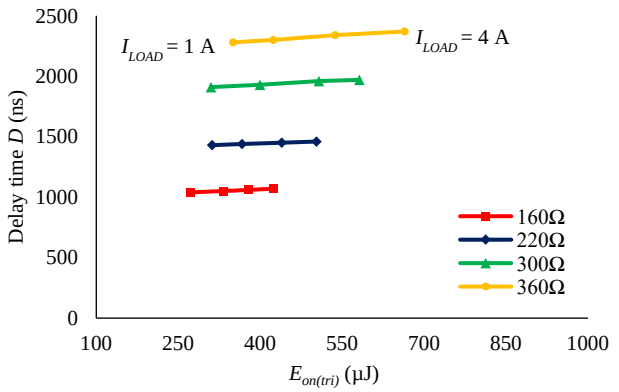

Fig. 16 Relationship between turn-on energy $E_{on(tri)}$ and delay time D.

C. *Tests with CT Arrangement*

R_g in Fig. 12(b) was set at 39 Ω, 47 Ω, 56 Ω, and 68 Ω. Readings of turn-on energy $E_{on(rec)}$, peak current I_{pk}, and delay time D were taken for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A.

Fig. 17 shows exemplifying waveforms with R_g = 56 Ω and I_{LOAD} = 3 A. Fig. 18 shows the relationship between $E_{on(rec)}$ and I_{os} for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A. Fig. 19 shows the relationship between $E_{on(rec)}$ and I_{pk} for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A. Fig. 20 shows the relationship between $E_{on(rec)}$ and D for I_{LOAD} = 1 A, 2 A, 3 A, and 4 A.

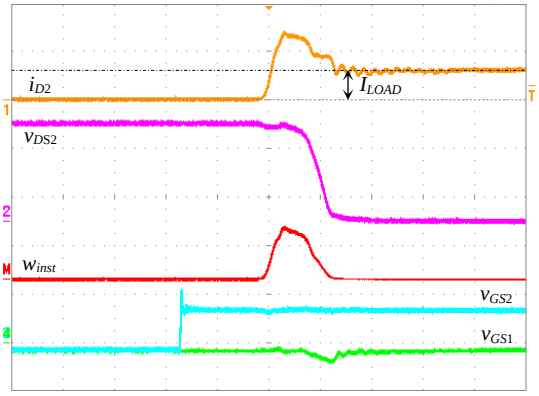

Fig. 17 Exemplifying waveforms from the scheme in Fig. 12(b) with R_g = 56 Ω and I_{LOAD} = 3 A. Scales: i_{D2} = 5 A/div., v_{DS2} = 200 V/div., w_{inst} = 2.5 kW/div., v_{GS2} = v_{GS1} = 20 V/div. Time scale = 200 ns/div.

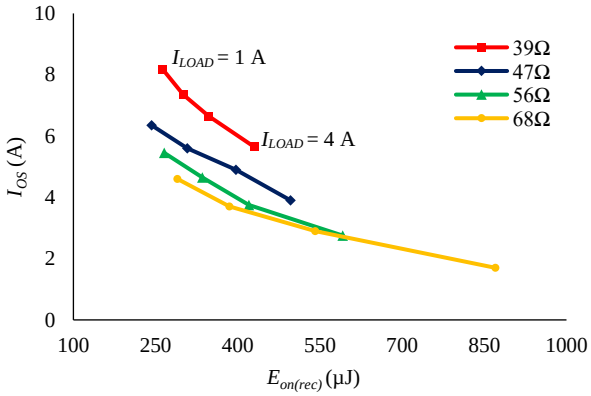

Fig. 18 Relationship between turn-on energy $E_{on(rec)}$ and overshoot current I_{os}.

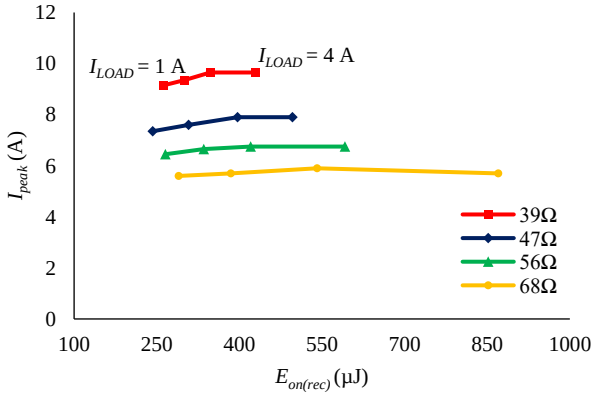

Fig. 19 Relationship between turn-on energy $E_{on(rec)}$ and peak current I_{pk}.

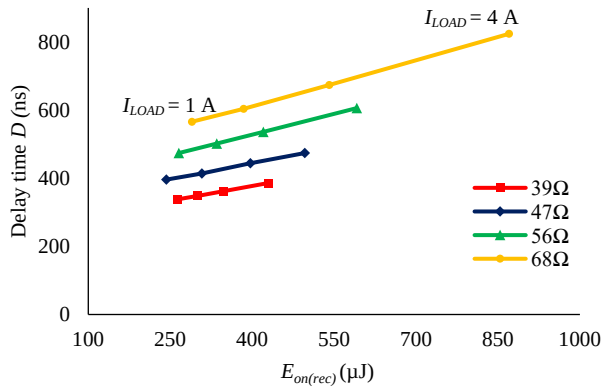

Fig. 20 Relationship between turn-on energy $E_{on(rec)}$ and delay time D.

D. Waveforms from Current Transformer Circuitry

Exemplifying waveforms from the CT circuitry in Fig. 12(b) were taken with R_g = 56 Ω and I_{LOAD} = 3 A. i_2 and v_2 are the CT's secondary current and voltage respectively.

Fig. 21 shows the waveforms when *TR*2 in Fig. 12(b) turns on. The peak magnetizing current drawn by the CT during the transient turn-on period is very small, and i_2 is consequently an accurate replica of the primary current i_{D2} during this period. Fig. 22 shows the waveforms when *TR*2 in Fig. 12(b) turns off. The half-sinusoidal oscillation of v_2 is due to the resonant action between the CT's magnetizing inductance and parasitic lumped capacitance during reset. The half-sinusoidal oscillation elapses over a time t_{rst} which was 816 ns.

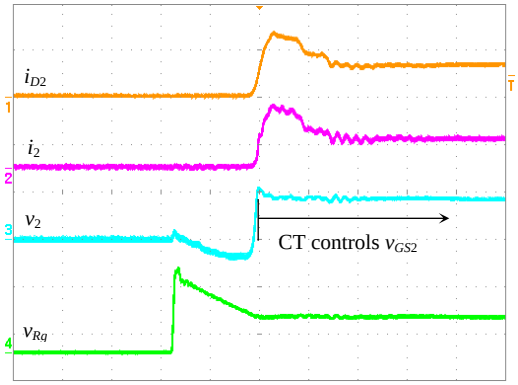

Fig. 21 Exemplifying waveforms from the circuitry in Fig. 12(b) at *TR*2 turn-on with R_g = 56 Ω and I_{LOAD} = 3 A. Scales: i_{D2} = 5 A/div., i_2 = 0.1 A/div., v_2 = 10 V/div., v_{Rg} = 10 V/div. Time scale = 200 ns/div.

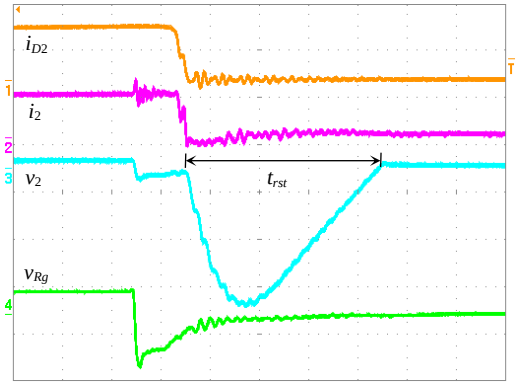

Fig. 22 Exemplifying waveforms from the circuitry in Fig. 12(b) at *TR*2 turn-off with R_g = 56 Ω and I_{LOAD} = 3 A. Scales: i_1 = 5 A/div., i_2 = 0.1 A/div., v_2 = 40 V/div., v_{Rg} = 10 V/div. Time scale = 200 ns/div.

E. Comparison of Results

Fig. 23 shows turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ plotted against overshoot current I_{os} at load current I_{LOAD} = 3 A. Fig. 24 shows $E_{on(tri)}$ and $E_{on(rec)}$ plotted against delay time D, also at I_{LOAD} = 3 A. In Fig. 23, under the same I_{os}, the turn-on energy $E_{on(rec)}$ of the rectangular trajectories is less than that of the triangular trajectories $E_{on(tri)}$. When R_g is made smaller, both $E_{on(tri)}$ and $E_{on(rec)}$ decrease and I_{os} increase consequently. In Fig. 24, the D of the rectangular trajectories only has magnitudes of hundreds of nanoseconds, but the D of the triangular trajectories is greater.

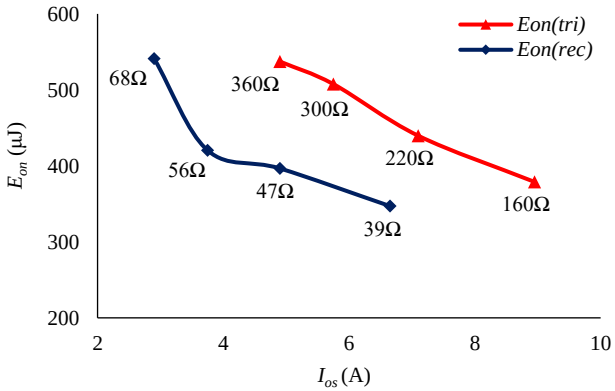

Fig. 23 Turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against overshoot current I_{os} for a load current of 3 A.

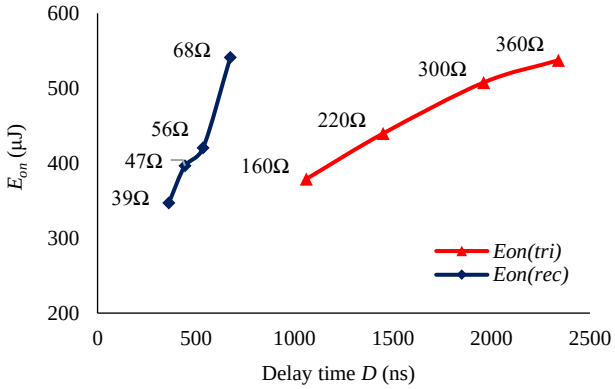

Fig. 24 Turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against delay time D for a load current of 3 A.

V. Discussion

A conventional gate driver and a gate driver with negative feedback applied to the gate signal by means of a CT have been compared. Improved trade-offs between incoming peak current, turn-on power dissipation, and delay time are obtained with the latter.

Both the conventional and CT circuits are simple, without features such as stepped gate voltage waveforms. The proposed circuitry does not use active gate control [18], [21], and standard gate driver ICs can be used. Whilst the CT is an additional component, it uses a low-cost, compact, and un-gapped toroidal core with no safety-isolation requirements.

Whilst the turn-on loss is reduced for a given overshoot current and propagation delay time, it is noted that a loss is incurred by the CT's secondary current flowing through the diodes D_t and D_f in Fig. 11(a) when the MOSFET is conducting. Both losses have to be evaluated in a practical converter design.

VI. Conclusion

A gate driver circuit for super-junction MOSFETs in voltage source bridge-legs has been presented. The circuit controls MOSFET incoming drain current profiles. Compared to conventional driver circuits, improved trade-offs between the incoming peak current, turn-on power dissipation, and delay time have been demonstrated. Further investigation will include collecting experimental results when using a bridge-leg in AC tests as in Figs. 10 and 11, and detailed modelling of the switching action of the proposed scheme. This will allow the turn-on trajectories of the MOSFET's drain current and drain-source voltage to be predicted more accurately.

References

[1] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Silicon carbide power transistors: a new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17-26, Jun. 2012.

[2] S. Jahdi *et al.*, "Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849-863, Feb. 2016.

[3] M. Pfost *et al.*, "Shortcircuit safe operating area of superjunction MOSFETs," in *Proc., 28th Int. Symp. Power Semiconductor Devices and ICs*, Prague, Czech Republic, Jun. 2016.

[4] L. Lorenz, G. Deboy, and I. Zverev, "Matched pair of Coolmos transistor with SiC-Schottky diode - advantages in application," *IEEE Trans. Ind. Appl.*, vol. 40, no. 5, pp. 1265-1272, Sep. 2004.

[5] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 720-734, Mar. 2017.

[6] J. Zhang and J.-S. Lai, "A synchronous rectification featured soft-switching inverter using CoolMOS," in *Proc., IEEE 21st Annu. Appl. Power Electron. Conf. Expo.*, Dallas, TX, USA, pp. 810-815, Mar. 2006.

[7] N. McNeill, P. Anthony, and N. Oswald, "Ultra-high efficiency machine drive inverter using super-junction MOSFETs," in *Proc., IET 7th Power Electron., Machines Drives Conf.*, Manchester, UK, Apr. 2014.

[8] A. Hopkins, N. McNeill, and P. H. Mellor, "Drain current injection circuitry for enabling the deployment of super-junction MOSFETs in a 5kW bidirectional DC-DC converter," in *Proc., IET 8th Power Electron., Machines Drives Conf.*, Glasgow, Scotland, Apr. 2016.

[9] A. Hopkins, N. Simpson, and N. McNeill, "Auxiliary resonant source charge extraction circuitry for enabling the use of super junction MOSFETs in high efficiency DC-DC converters," in *Proc., IEEE 34th Appl. Power Electron. Specialist's Conf. Expo.*, Anaheim, CA, USA, pp. 2159-2166, Mar. 2019.

[10] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159-1167, Mar. 2012.

[11] M. M. Farag, S. M. Gadoue, A. L. Mohamadein, A. M. Massoud, and S. Ahmed, "Elimination of reverse recovery effects associated with Coolmos devices employing current source inverter topology," in *Proc., IET 6th Power Electron., Machines Drives Conf.*, Bristol, UK, Mar. 2012.

[12] J. Kitson and N. McNeill, "A high efficiency voltage-fed quasi Z-source inverter with discontinuous input current using super-junction MOSFETs," in *Proc., IET 8th Power Electron., Machines Drives Conf.*, Glasgow, Scotland, Apr. 2016.

[13] Z. Feng, N. McNeill, and B. W. Williams, "A high-efficiency super-junction MOSFET based inverter-leg configuration using a dual-mode switching technique," in *Proc., IEEE 34th Appl. Power Electron. Specialist's Conf. Expo.*, Anaheim, CA, USA, pp. 2467-2474, Mar. 2019.

[14] D. B. DeWitt, C. D. Brown, and S. M. Robertson, "System and method for reducing body diode conduction," US Patent No. 7508175 (B2), 24 Mar. 2009.

[15] D. Grant, "Diode recovery current suppression circuit," *IET Electron. Letts.*, vol. 38, no. 528, pp. 203-204, 28 Feb. 2002.

[16] S. Mocevic *et al.*, "Comparison and discussion on shortcircuit protections for SiC MOSFET modules: desaturation vs. Rogowski switch-current sensor," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2880-2893, Feb. 2020.

[17] F. Huang and F. Flett, "IGBT fault protection based on di/dt feedback control," in *Proc., IEEE 38th Power Electron. Specialists Conf.*, Orlando, FL, USA, pp. 1478-1484, Jun. 2007.

[18] J. Groeger, A. Schindler, B. Wicht, and K. Norling, "Optimized dv/dt, di/dt sensing for a digitally controlled slope shaping gate driver," in *Proc., IEEE 32nd Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, pp. 3654-3569, Mar. 2017.

[19] D. Rothmund, D. Bortis, and J. W. Kolar, "Highly compact isolated gate driver with ultrafast overcurrent protection for 10 kV SiC MOSFETs," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 4, pp. 278-291, Dec. 2018.

[20] N. McNeill and N. K. Gupta, "Assessment of the error in the average current sensed by the unidirectional current pulse transformer", *IET Circuits Devices Syst.*, vol. 2, no. 2, pp. 265-276, Apr. 2008.

[21] A. Paredes, H. Ghorbani, V. Sala, E. Fernandez, and L. Romeral, "A new active gate driver for improving the switching performance of SiC MOSFET," in *Proc., IEEE 32nd Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, pp. 3557-3563. Mar. 2017.