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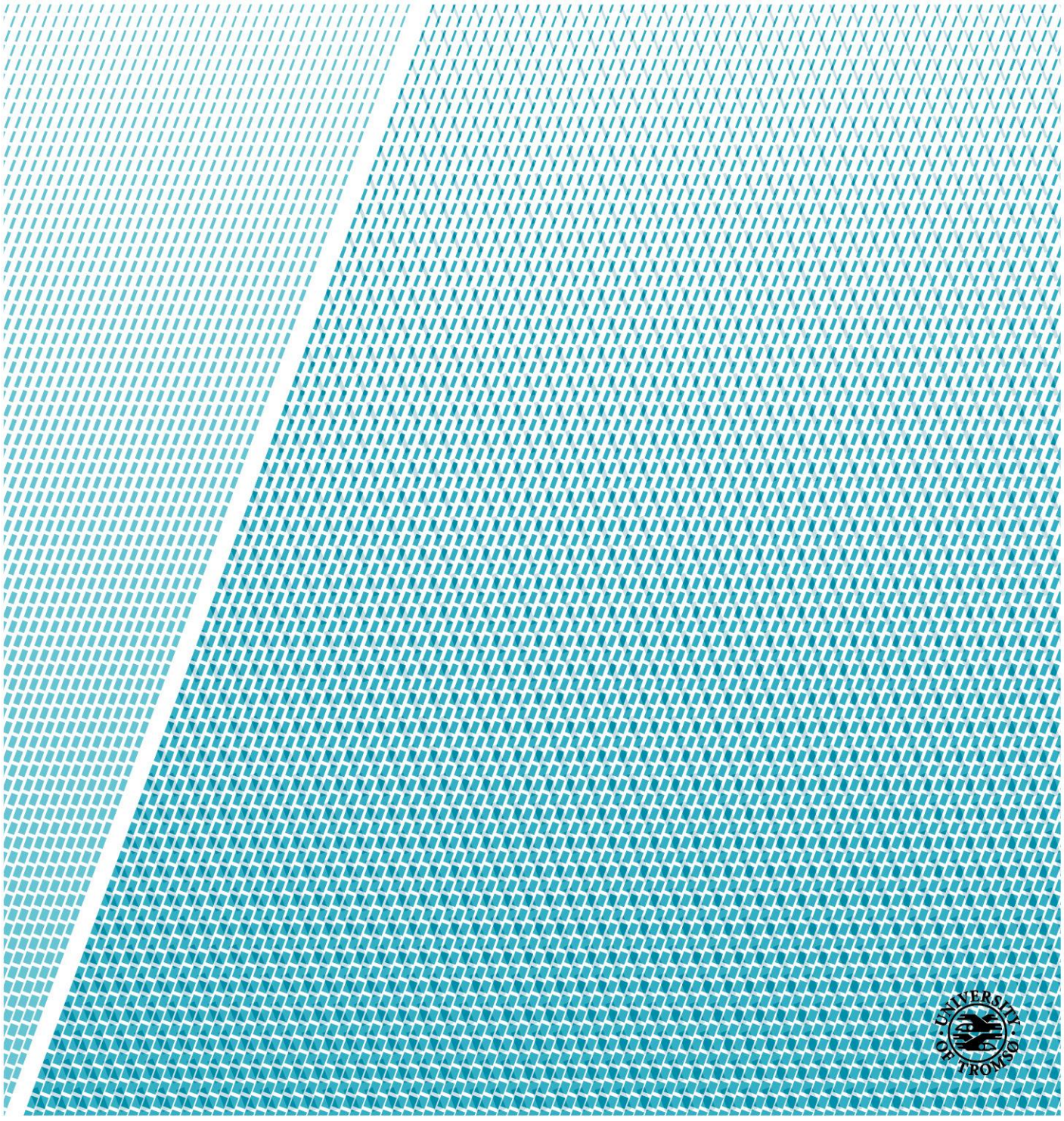
**Ivan Mokrushev**

*Master of Science in Electrical Engineering, June 2018*



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# Evaluation of cascaded MPC performance in voltage source converters

By

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# Abstract

Model predictive control method becomes more popular in research over the last decade. Due to the growing popularity of the model predictive control concept, there are more and more questions about the effectiveness of this method in comparison with other methods.

In this thesis cascaded model predictive control of grid connected voltage source converter with LCL filter has been evaluated. The relevant topics and literature regarding the existing control methods, applying requirements to a converter and different transistor technologies have been studied and reviewed.

Three criteria of performance have been selected to compare the MPC method with conventional voltage oriented control method: total and individual harmonic distortion, power factor and power losses.

The models have been simulated at rated initial values according to EU standards. The results of simulations have been compared.

Existing transistor technologies which can be used in the control models have been investigated. Losses of the converter (without losses in the LCL filter) due to the use of each type of transistors have been calculated for each model.

# Preface

This thesis is submitted in partial fulfillment of the requirement for the Master of Science (MSc) in Electrical Engineering at The Arctic University of Norway (UiT).

I am grateful to my supervisor Associate Professor Bjarte Hoff for advice and support. He was my continuous support during all the five months of this thesis. He answered all my queries and guided me in completing the task.

I am also grateful to all the teaching staff of the Department of Electrical Engineering at UiT for the opportunity to improve my knowledge in electrical engineering.

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# Nomenclature and notation

**Abbreviations**

| | |
|---|---|
| AlGaN | Aluminum gallium nitride |
| BJT | Bipolar junction transistor |
| CCS | Continuous control set |
| FCS | Finite control set |
| FFT | Fast Fourier transform |
| FPGA | Field programmable gate array |
| GaN | Gallium nitride |
| GPC | Generalized predictive control |
| HEMT | High electron mobility transistor |
| IGBT | Insulated-gate bipolar transistor |
| LCL | Inductor-Capacitor-Inductor |
| MPC | Model predictive control |
| MOS | Metal-oxide-semiconductor |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| PLL | Phase Locked Loop |
| PV | Photovoltaics |
| PWM | Pulse-width modulation |
| RMS | Root mean square |
| Si | Silicon |
| SiC | Silicon carbide |
| SVM | Space vector modulation |
| THD | Total harmonic distortion |
| VOC | Voltage oriented control |
| VSC | Voltage source converter |

**Symbols**

| | |
|---|---|
| $\theta, \hat{\theta}$ | Grid voltage angle in phase, estimated grid voltage angle in phase [rad] |
| $\phi$ | Power angle [rad] |
| $a_n, b_n, c_n$ | Constants |
| A,B,C,D | State-space system matrices |
| $C_u, C_v, C_w$ | Capacitance in LCL filter [F] |

| | |
|---|---|
| $E_{SW(on)}, E_{SW(off)}$ | Energy losses [J] |
| $E_{rr}$ | Reverse recovery switching loss [J] |
| F | Disturbance system matrix |
| $f_{SW}$ | Switching frequency [Hz] |
| $HD_n$ | Harmonic distortion |
| $i_\alpha,\ i_\beta$ | Orthogonal stationary frame current quantities [A] |
| $i_a, i_b, i_c$ | Converter side currents [A] |
| $i_d, i_q$ | Rotating frame current quantities [A] |
| $i_{C_u}, i_{C_v}, i_{C_w}$ | Filter capacitor currents [A] |
| $I_C$ | Collector current [A] |
| $I_D$ | Drain current [A] |
| $i_{DC}$ | DC-link current from external sources [A] |
| $I_F$ | Forward current [A] |
| J | Cost function |
| $L_a, L_b, L_c$ | Converter side inductance [H] |
| $L_r, L_s, L_t$ | Grid side conductance [H] |
| M | Modulation index |
| P | Active power [W] |
| P, H, Q | Prediction matrices related to system outputs |
| PF | Power factor |
| Q | Reactive power [VAr] |
| $R_a, R_b, R_c$ | Converter side resistors [Ohm] |
| $R_r, R_s, R_t$ | Grid side resistors [Ohm] |
| $R_u, R_v, R_w$ | Damping resistors [Ohm] |
| S | Apparent power [VA] |
| $t_{ri}, t_{fv}, t_{fi}, t_{rv}$ | Time rise and fall voltage and current [s] |
| $u$ | Input vector |
| $v_\alpha,\ v_\beta$ | Orthogonal stationary frame voltage quantities [V] |
| $v_{cr}$ | Carrier triangle signal |
| $v$ | Disturbance vector |
| $V_{CE}$ | Collector-emitter voltage [V] |
| $V_d, V_q$ | Rotating frame voltage quantities [V] |
| $V_{DC}$ | DC-link voltage [V] |
| $V_{DS}$ | Drain-source voltage [V] |
| $V_F$ | Forward voltage [V] |

| | |
|---|---|
| $v_H$ | Sum of all harmonic voltage [V] |
| $v_n$ | Individual harmonic voltage [V] |
| $w, \widehat{w}$ | Angular grid velocity, estimated grid velocity [rad/s] |
| x | State vector |

# 1. Introduction

*This chapter shortly describes control methods that will be investigated in the project. It also explains which criteria of evaluation will be used to evaluate MPC. Limitations are described in Chapter 1.5.*

## 1.1 Background

Nowadays, renewable energy has become one of the most rapidly developing parts of the industry in the world. 500 000 solar panels were installed each day in the last year worldwide. In China every hour two wind turbines are started. Alternative sources of energy are becoming more and more effective. There are many investigations going on for reducing losses and increasing the efficiency of control methods.

Power electronics is the field in electrical engineering that has a great contribution for reducing losses in the area of renewable energy. Voltage source converter is an important device in controlling and distributing renewable energy into the grids.

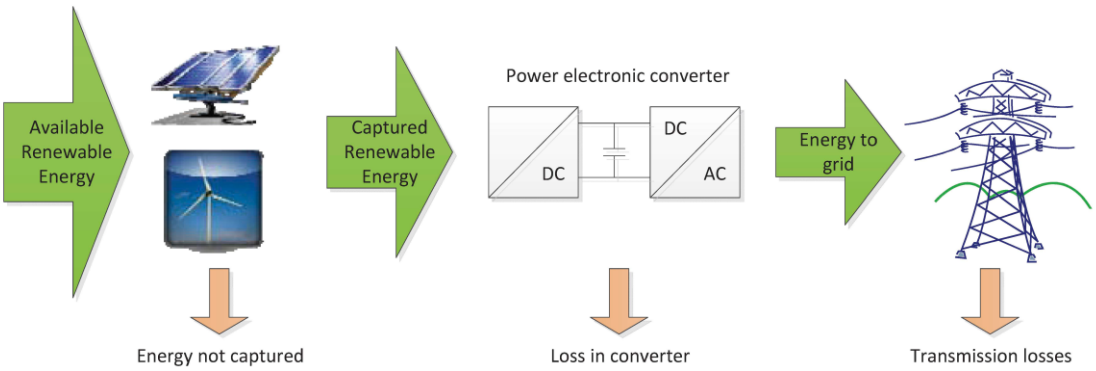


*Figure 1.1 - Supply of renewable energy to the grid [1]*

Many applications use voltage source converter (VSC) to convert DC power to AC power. Figure 1.1 shows an example of a typical renewable power source that captures the energy and transfers it to the grid through VSC. A filter is implemented in the converter to smooth square wave voltage to a sinusoidal current.

There are two types of filter that are using L and LCL-filters nowadays. Since this project is based on [1], LCL filter will be considered and used further. Also, LCL filter has more compact design and better attenuation which increase the efficiency of VSC [1].

Another method to increase efficiency and reduce losses is control algorithm. In the last decades, with the development of computer technologies, VSC is controlled using microcontroller or field programmable gate array (FPGA). There are many common control methods, which are shown in Figure 1.2:

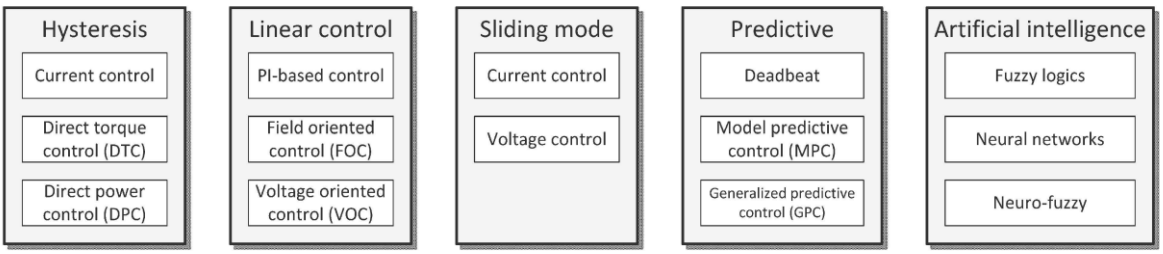


*Figure 1.2 - Common control methods of power converters and drivers [2]*

The most common used control method is voltage oriented control (VOC), but during the last time, according to the fact that the computing speed of modern digital processors has increased many times, model predictive control method becomes more and more popular.

This project is based on [2], and the main purpose is to evaluate cascaded MPC performance. It is reasonable to compare MPC performance with VOC performance under identical conditions.

## 1.2 Model predictive control

Model predictive control uses a mathematical model to predict behaviour in the future. Most of the real systems have uncertainties, nonlinearities, noises, etc. MPC compensates for the mentioned disturbances by updating its projected trajectory every program cycle. This causes the so-called moving horizon, since the length of the horizon is constant, but is shifted one step ahead in time for each optimization.

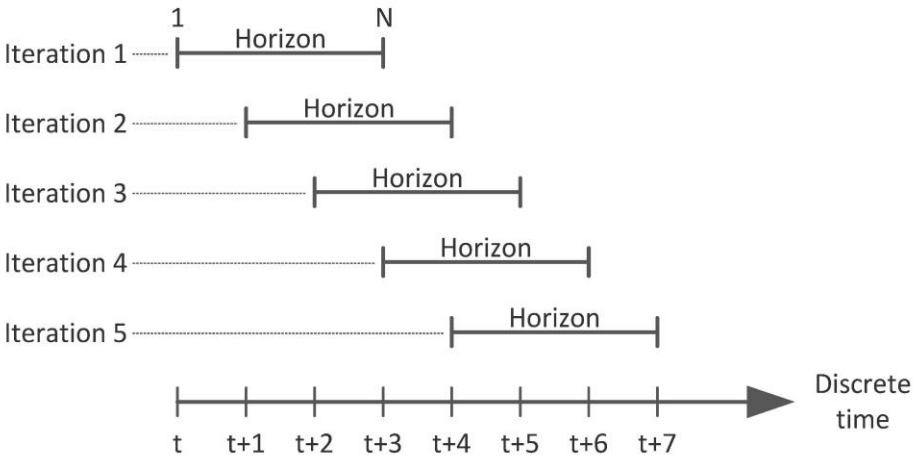


*Figure 1.3 - Moving horizons in model predictive control [2]*

There are two types of MPC: continuous control set MPC (CCS-MPC) and finite control set MPC (FCS-MPC).

### 1.2.1 Finite control set MPC

Finite control set MPC (FCS-MPC) is designed to reduce calculations and processing time. FCS will not necessarily reduce processing time. It depends on how many steps into the future that is predicted. Although, for single step prediction for a converter, there are only seven possible answers. The prediction procedure is limited to a finite number of switching positions in the converter. One of these states should be chosen due to cost minimization function [3].

At each sampling time, the cost function is calculated for all possible input combinations and compared with reference as shown in Figure 1.4. All the predicted values $x(k+1)$ are compared with their references $x_{ref}(k+1)$ in the cost function minimization block. Switching state S that minimizes cost function is selected and applied to the converter.

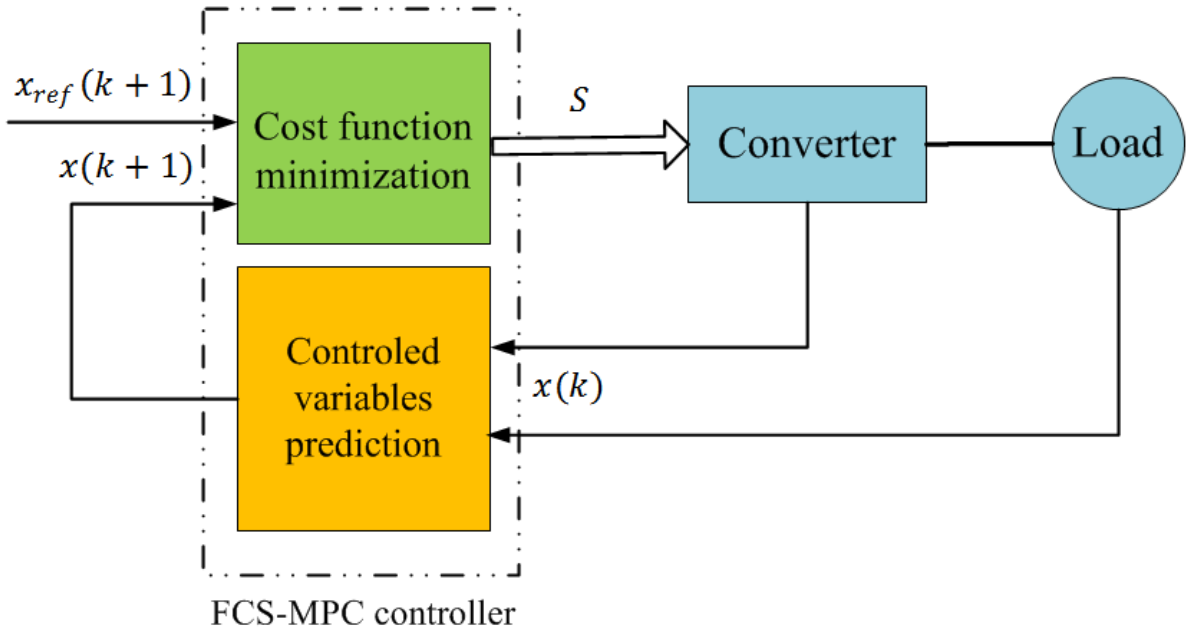


*Figure 1.4 - The control block diagram of FSC-MPC [3]*

One-step optimization in general form:

$$\min_{u \in \{0,1\}} . \ \left|\left|y^* - y_{k+1}\right|\right|_2^2 \tag{1.1}$$

$$s.t. \quad y_{k+1} = G(u),$$

Where G is a model of the system, **u** is a vector of binary variables, **y** is the system outputs and $\mathbf{y}^*$ is the reference value [2].

Two-level three-phase converter consists of six switches with eight possible combinations, and seven of them are unique. This can lead to a huge number of possible combinations $7^n$, where n is a number of prediction horizon. There will be a huge number of combinations, but only if the prediction horizon **n** is increased.

FCS-MPC put large requirements on the control hardware in terms of computational speed. Fast computational speed in FCS-MPC and lack of constraints leads to the fact that the switching frequency can be high. Also, high switching frequency cause high-order harmonics, which can disturb sensitive equipment [4].

### 1.2.2 Continuous control set MPC

In continuous control set MPC (CCS-MPC) the control actions are continuous-time signals that are sent to a modulator. The case with included constraints could be solved as a quadratic program (QP). Since an analytical solution is provided, long horizons may be employed. The most extended method of this type is generalized predictive control (GPC) [5].

The general state of QP is:

$$\begin{aligned} \min_{x} \quad & q(x) = \frac{1}{2}x^T G x + x^T C \\ s.t. \quad & a_i^T = b_i \qquad i \in \mathcal{E} \\ & a_i^T \geq b_i \qquad i \in \mathcal{I} \end{aligned} \tag{1.2}$$

Where $G$ is a symmetrical matrix, $\mathcal{E}$ and $\mathcal{I}$ are finite sets of indices, and c, x and $\{a_i\}, i \in \mathcal{E} \cup \mathcal{I}$ are vectors in $\mathbb{R}^n$ [2].

MPC with continuous control set needs a modulator in order to generate a required voltage (fixed switching frequency). Two cascaded MPC controllers were used in [2] in order to avoid to use a modulator. It will be shown in further chapters.

## 1.3 Voltage oriented control

Several control methods were shown in Figure 1.2. Hysteresis control and linear control with pulse width modulator are most commonly used in literature. Voltage oriented control (VOC) will be considered as one of the linear control methods.

VOC decomposes active and reactive power components and controls them separately. In a pulse width modulator, the reference voltage is compared with carrier triangle signal, and the output of the comparator is used to drive converter switches, as shown in Figure 1.5 [6].

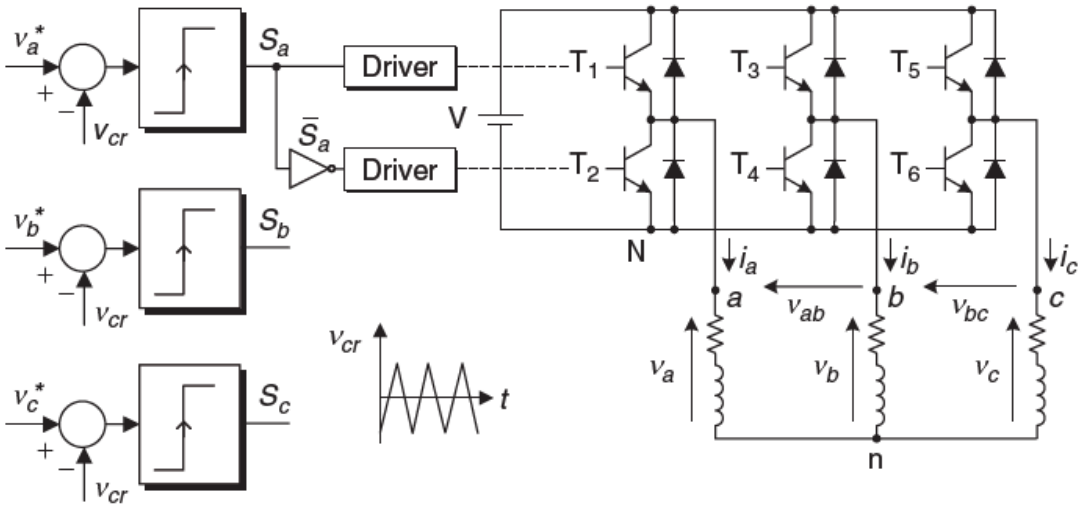


*Figure 1.5 - Pulse width modulator for a three-phase inverter [6]*

Here $\overline{S_i}, S_i$ are the 6 switches of the bridge (i = a,b,c), $v_i^*$ are voltage reference vectors, $v_{cr}$ is carrier triangle signal. The reference voltage of each phase is compared to triangular waveform.

A variation of PWM is space vector modulation (SVM), in which the voltage vectors are calculated from the reference vector. Space vector representation is shown in Figure 1.6.

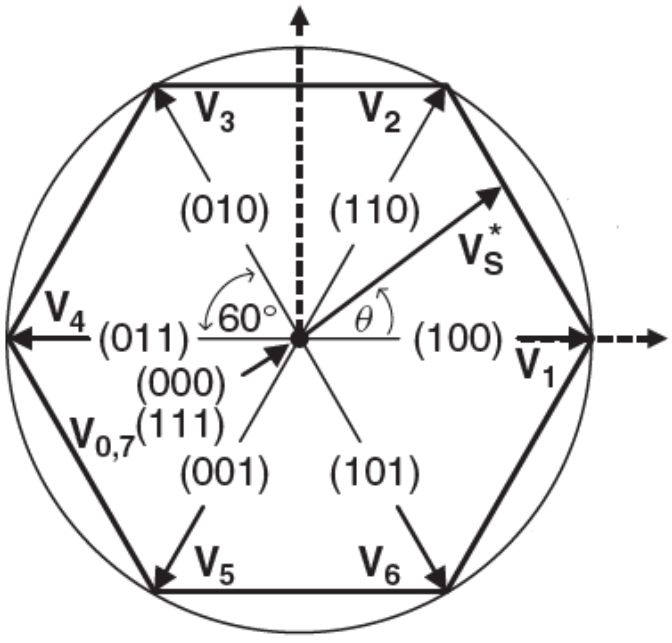


*Figure 1.6 Space vector representation [7]*

A three-phase VSC has eight switching states. 6 are active and 2 are passive. Passive voltage vectors are equal to zero ( $V_0 = 0, V_7 = 0$).

VOC is based on the orientation of the current vector in the same direction as that of the voltage vector by controlling the current vector in the two rotating coordinates dq as shown in Figure 1.7.

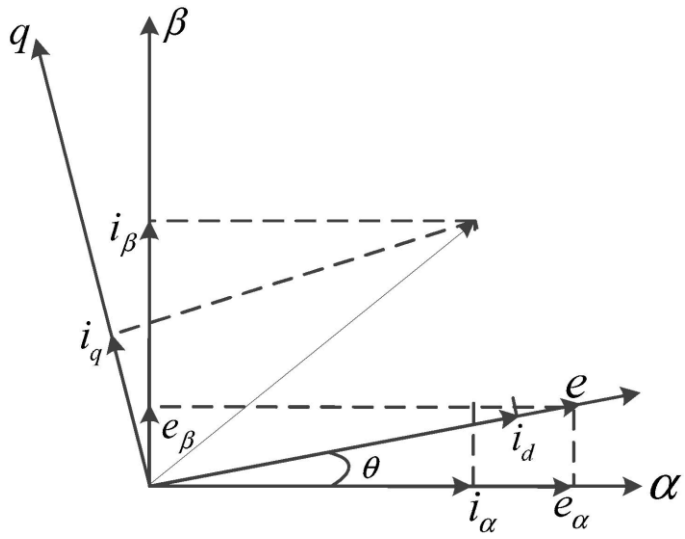


*Figure 1.7 - Vector diagram of the d-axis VOC [8]*

Through Clark and Park transformation $i_a, i_b, i_c$ achieved $i_d, i_q$. This will be described in Chapter 4 in more detail.

## 1.4 Criteria for evaluation

There are several requirements which can be the criteria of converter evaluation. By applying different models of control to the same converter, evaluation of these models can be done.

Requirements depend on application field, country, etc. This project uses criteria that meet the limitations of the project.

Three criteria are used in the project for evaluation of the proposed control concept.

### 1.4.1 Total and individual harmonic distortion

The distorted current and voltage waveforms are operating conditions in a power system. Standards contain numerical quantities – n-th harmonic ratio $i_n/i_1$ and total harmonic distortion (THD). These factors are included in the basis for standardization of power quality. Harmonic distortion can be defined as deviation from an ideal sinusoidal wave of power frequency. Fourier analysis is usually used to find harmonic distortions. THD are most commonly used measures for harmonics and can be found as [9]:

$$THD = \frac{\left[\sum_{h=2}^{hmax} M_h^2\right]^{1/2}}{M_1}. \quad (1.3)$$

The main problems that can cause harmonic distortion:

- Extra losses and heating
- Resonance can cause overvoltage

### 1.4.2 Power factor

Both MPC and VOC algorithms can control the active and reactive power. This requirement should therefore be fulfilled for both algorithms by just providing the correct references. Power factor is important information about the nature of receiving loads. Power factor gives information about the content of electrical load: resistive, inductive, and capacitive. Resistive component of load drives only active power P, while inductive and capacitive – reactive power Q. Reactive capacitive power and reactive inductive power point in opposite directions. Complex power of active and reactive is apparent power S, which can be calculated as:

$$|S|^2 = P^2 + Q^2. \quad (1.4)$$

Power factor is cosines of the angle between apparent and active power. Therefore, power factor shows a correlation between resistive and inductive and capacitive loads.

### 1.4.3 Power losses

Power losses are one of the main requirements for converters. In the project considered only losses in the transistors, excluding losses in the LCL filter. Losses in the transistors are divided into two types:

- Conductive loss;
- Switching loss.

Transistor switching from on-state to off-state and back cause switching losses. These losses depend on the transistors switching frequency, and type of transistor.

Conductive losses are power dissipation during full conduction of transistor. These losses have a direct dependency on duty cycle, conduction current and voltage.

## 1.5 Limitations of the project

The focus of this project is an evaluation of the existing model predictive control. Therefore, it should be achieved by comparing with another model. Since they are few following limitations are used:

- Two-level three-phase converter;

- DC-link voltage 400 V;
- Comparing of existing MPC algorithm with VOC algorithm;
- Using several types of transistors in converters;
- Two evaluation criteria are used at least.

Filters configuration and hardware implementation are not aims of the project.

## 1.6 Outline of the Thesis

The report consists of 8 chapters.

- Chapter 1 describes control methods that will be investigated in the project. It also explains which criteria of evaluation will be used to evaluate MPC.
- Chapter 2 describes how evaluation requirements were selected. It also describes the chosen requirements and their quantities.
- Chapter 3 describes what types of transistor technologies can be applied to the proposed models.
- Chapter 4 describes the detailed and simplified models of a two-level three-phase converter. It also describes the model predictive control and vector oriented control algorithms.
- Chapter 5 represents the simulation results for MPC and VOC algorithms with the different switching frequency of transistors. It also compares the obtained results.
- Chapter 6 represents the calculated power losses of each type of applied transistors. These results are compared with each other and discussed.
- Chapter 7 discusses the results obtained in the previous chapters and gives recommendations for a better solution.
- Chapter 8 gives a short conclusion of the thesis. It also gives suggestions for further work.

# 2. Requirements for power converters

*This chapter describes how evaluation requirements were selected. It also describes the chosen requirements and their quantities.*

The efficiency of a model depends on the requirements that apply to this model. The requirements consist of different parameters and depend on the country where the equipment is being used. All requirements that could apply, consist in standards. Since the project is being done in Norway, "Norwegian electrotechnical standards" will be used. All standards that are being used in Norway are approved by Norsk Elektroteknisk komite which is the member of International Electrotechnical Commission (IEC) and European Committee for Electrotechnical Standardization (CENELEC).

Due to the limitations of the project – standards, that are going to be applied, should comply with conditions: voltage of the system less than 400 V and rated current $\leq 16\ A$.

Some of the requirements will not be considered, assuming a stiff grid. For example: frequency tolerance, DC voltage tolerance, voltage unbalance amplitude, area [10],[11].

These are the main requirements that are useful in evaluating semiconductor converters with conditions which were described above [12], [10].

1. Total and individual harmonic distortion
2. Power factor
3. Power losses

## 2.1 Harmonic distortion

Voltages and currents in the industry are often distorted. Distortion may be caused by the switching action of thyristors, or by any other non-linear load. A distorted wave consists of a fundamental and one or more harmonics. Fundamental harmonic (or first harmonic) has the lowest or base frequency $f$. Second harmonic has frequency $2f$, third harmonic - $3f$, etc. The waveshape depends on their frequency, amplitude and their angular position with respect to the fundamental harmonic [13].

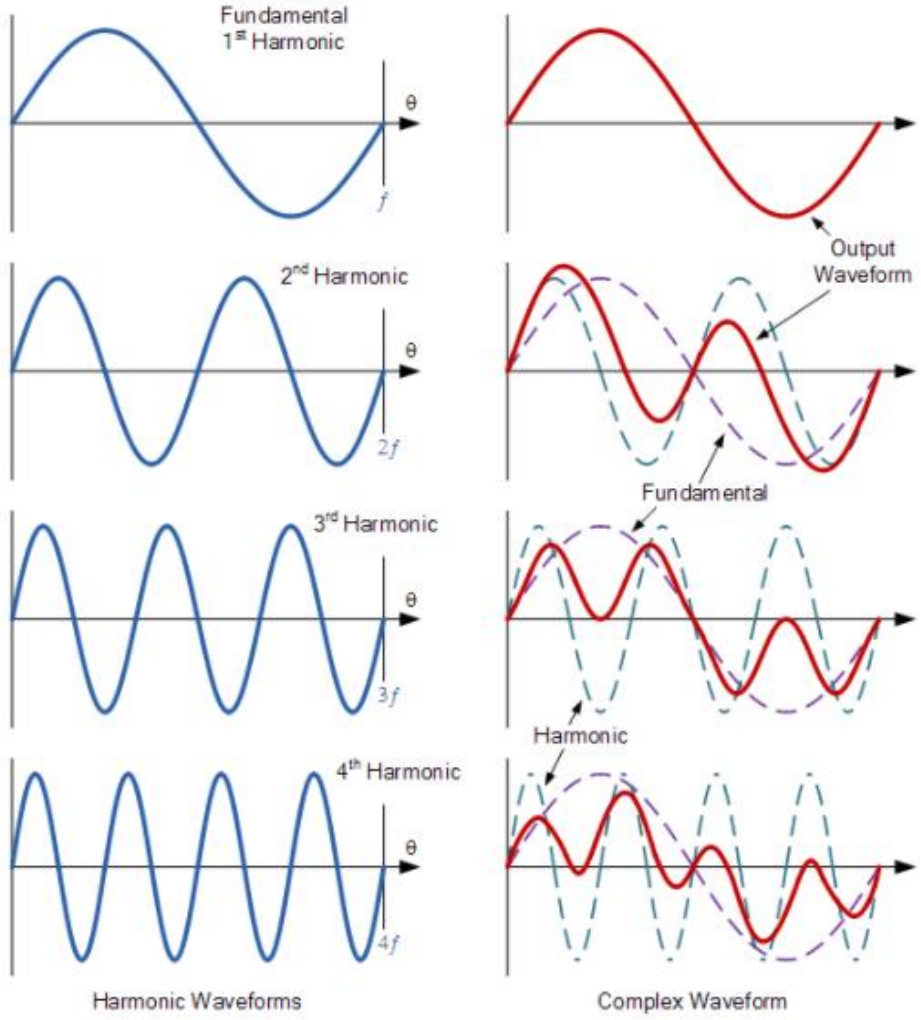


*Figure 2.1 - Complex waveforms due to harmonics [14]*

The harmonic voltage is the sum of all over harmonics,$v_n$, in order n, (n > 1):

$$v_H = \sum_{n=2}^{\infty} v_n. \tag{2.1}$$

The individual harmonic voltages, $v_n$:

$$v_n = a_n \cos\left(\frac{n\pi t}{L}\right) + b_n \sin\left(\frac{n\pi t}{L}\right). \tag{2.2}$$

Where $n$ is the harmonic number, $t$ is timer, $L$ is half the period of the fundamental frequency, $a_n$ , $b_n$ are constants. The harmonics can be rewritten with an amplitude $c_n$ and phase $\varphi_n$:

$$v_n = c_n \sin(\frac{n\pi t}{L} + \varphi_n). \tag{2.3}$$

Where:

$$c_n = \sqrt{a_n^2 + b_n^2}. \tag{2.4}$$

The phase is defined by:

$$\sin \varphi_n = \frac{a_n}{c_n}, \quad \cos \varphi_n = \frac{b_n}{c_n}. \tag{2.5}$$

The harmonic distortion caused by the nth harmonic of the base (fundamental) frequency, $HD_n$, is defined as the ratio of the rms value of the harmonic voltage of order n over time T ( number of periods of the fundamental) divided by the rms value of the fundamental voltage, $v_F$, over the time T [15]:

$$HD_n = \frac{\sqrt{\frac{1}{T}\int_0^T v_n^2 dt}}{\sqrt{\frac{1}{T}\int_0^T v_F^2 dt}}. \tag{2.6}$$

Total harmonic distortion (THD) describe waveform distortion at any point in a system THD is equal to the effective value of all the harmonics divided by the effective value of the fundamental:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} \frac{1}{T}\int_0^T v_n^2 dt}}{\sqrt{\frac{1}{T}\int_0^T v_F^2 dt}} = \sqrt{\sum_{n=2}^{\infty} (HD_n)^2}. \tag{2.7}$$

### 2.1.1 Distortion limits

Three standards are applied to this project:

- NEK IEC 60146-2 Semiconductor converters – Part 2: Self-commutated semiconductor converters including direct d.c. converters [10]
- NEK IEC 60146-1-1 Semiconductor converters – General requirements and line commutated converters – Part 1-1: Specification of basic requirements [11]
- NEK IEC 61727 Photovoltaic PV systems – Characteristic of the utility interface [12]

All of them consist of distortion limit: THD and individual harmonic distortion. The two first are equal with harmonic requirements.

In [11] and [10] are included “immunity levels for stiff AC voltage connections”, where limits depend on immunity class. The strictest class C was chosen. This class is intended for power supply to sensitive electronic units.

Due to these two standards:

*Table 2.1 - Distortion limits based on [7], [8]*

| Voltage waveform | Limits (% of fundamental) |
|---|---|
| THD | Less than 5% |
| Odd individual harmonic distortion | Less than 3% |
| Even individual harmonic distortion | Less than 1% |

Standard [12] has more detailed requirements to distortion:

*Table 2.2 - Distortion limits based on [9]*

| **Odd harmonics** | **Distortion limit** |
|---|---|
| 3rd through 9th | Less than 4% |
| 11th through 15th | Less than 2% |
| 17th through 21st | Less than 1.5% |
| 23rd through 33rd | Less than 0.6% |
| **Even harmonics** | **Distortion limit** |
| 2nd through 8th | Less than 1% |
| 10th through 32nd | Less than 0.5% |
| **THD** | Less than 5% |

There is one difference in the requirements – odd individual harmonic distortion in the converters standards should be less than 3%, but PV systems standards say that few first odd harmonics ( 3rd through 9th ) could be less than 4%.

In this case, more strict limits will be chosen. Table 2.2 should be modified:

*Table 2.3 - United distortion limits*

| **Odd harmonics** | **Distortion limit** |
|---|---|
| **3rd through 9th** | Less than 3% |
| **11th through 15th** | Less than 2% |
| **17th through 21st** | Less than 1.5% |
| **23rd through 33rd** | Less than 0.6% |
| **Even harmonics** | **Distortion limit** |
| **2nd through 8th** | Less than 1% |
| **10th through 32nd** | Less than 0.5% |
| **THD** | Less than 5% |

## 2.2 Power factor

The complex power is defined as

$$S = VI^* = Se^{j\phi}. \tag{2.8}$$

The magnitude of complex power is called apparent power:

$$S = VI. \tag{2.9}$$

Its units are volt-amperes (VA)

The real average power:

$$P = VI\cos\phi. \tag{2.10}$$

The units of power are watts (W). Where $\phi$ is power angle (or angle between voltage V and current I) [16].

In AC circuits, energy flows in and out of energy storage elements (capacitances and inductances). Energy flows into it when the voltage across a capacitance or current flowing through an inductance are increasing. Energy flows out of it when they (voltage or current) are decreasing.

The peak instantaneous power associated with the energy storage elements contained in a general load is called reactive power:

$$Q = VI\sin\phi. \tag{2.11}$$

The units of reactive power are volt-ampere reactive (VAr)

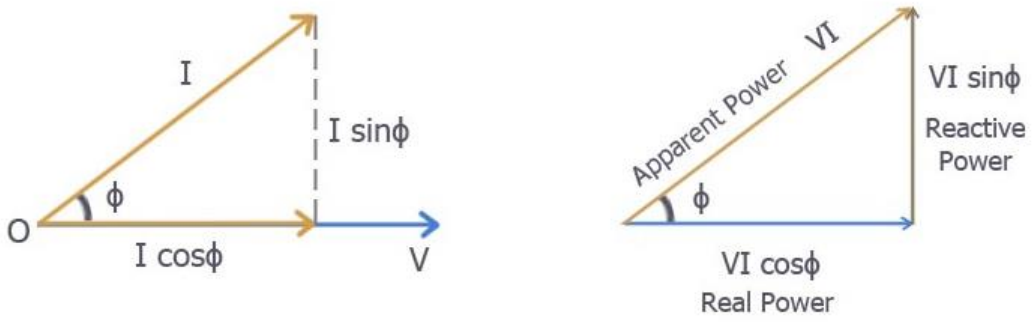


*Figure 2.2 - Power triangular [17]*

The efficiency of AC circuits depends on apparent power since their conductance depends on V and their inductance depends on I. Power P is a physical significance sine since it represents the rate of useful work being performed plus the power losses. In most situations, it is desirable to have the reactive power Q to be zero.

The power factor of a device is the ratio of the active power P to the apparent power S:

$$PF = \frac{P}{S} = \frac{VI\cos\phi}{VI} = \cos\phi. \tag{2.12}$$

The power factor of a circuit or device is simply a way of stating what part of its apparent power is the real, or active, power.

As shown in Figure 2.2., the power factor is the cosine of the angle by which the current lags (or leads) the voltage. If the current lags the voltage, the power factor is said to be inductive or lagging. If the current leads the voltage, the power factor is said to be capacitive or leading ( Figure 2.3) [18].

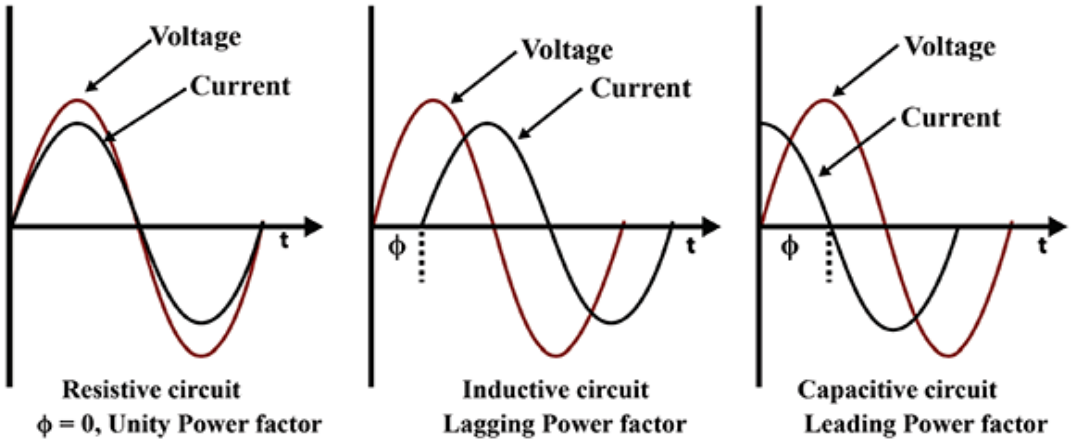


*Figure 2.3 - Power factor (unity, lagging, leading) [18]*

### 2.2.1 Power factor limit

"IEC 61727 Photovoltaic PV systems – Characteristic of the utility interface" [12] specifies that " The PV system shall have a lagging power factor greater than 0.9 when the output is greater than 50% of the rated inverter output power"

From the specification above, it could be calculated, that

$$\cos\phi = 0.9\,, \phi = 25.84^0. \tag{2.13}$$

This means that the angle between voltage U and current I has to be less than $25.84^0$. Current lags behind the voltage, as shown in Figure 2.4

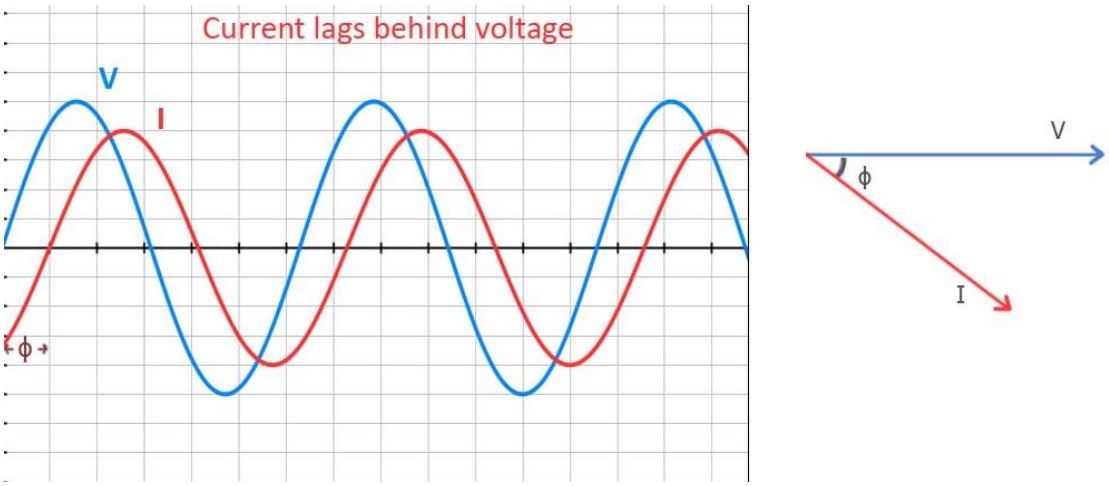


*Figure 2.4 - Lagging power factor [17]*

## 2.3 Power losses

In "IEC 60146-1-1 Semiconductor converters – General requirements and line commutated converters – Part 1-1: Specification of basic requirements" [11] seven types of losses for semiconductor converters are described:

a) Internal losses in the assembly such as losses in semiconductor valve devices, in fuses, potential dividers, current balancing means, capacitor resistor damping circuits and voltage surge diverters;
b) Losses in transformers, transducers, interphase transformers, current limiting and balancing reactors between transformer and thyristors or diode assemblies and the losses of the line side auxiliary transformers and reactors forming part of the equipment and delivered under the same contract;
c) Losses due to main connections between transformer and assembly in cases when transformer and assembly are built together and delivered as a single unit;

d) Power absorbed by auxiliaries such as permanently connected fans or pumps and relays unless otherwise specified;
e) Losses in series smoothing reactors, when supplied by the supplier of the PCE (power conversion equipment)
f) Losses due to circulating currents in double converter connections;
g) Power consumed by the trigger equipment (equipment which provides suitable trigger pulses from a control signal for controllable valve devices in a converter or power switch)

The project considers a model which excluded some auxiliary equipment (transformers, fans, pumps, etc). Also, losses by the trigger equipment will be neglected due to using digital devices which provide insignificant losses.

Therefore, paragraph **a)** could be used as a requirement for converters in the project, internal losses in the converter.

### 2.3.1 Converter losses

A two-level three-phase converter is considered in the project [2].

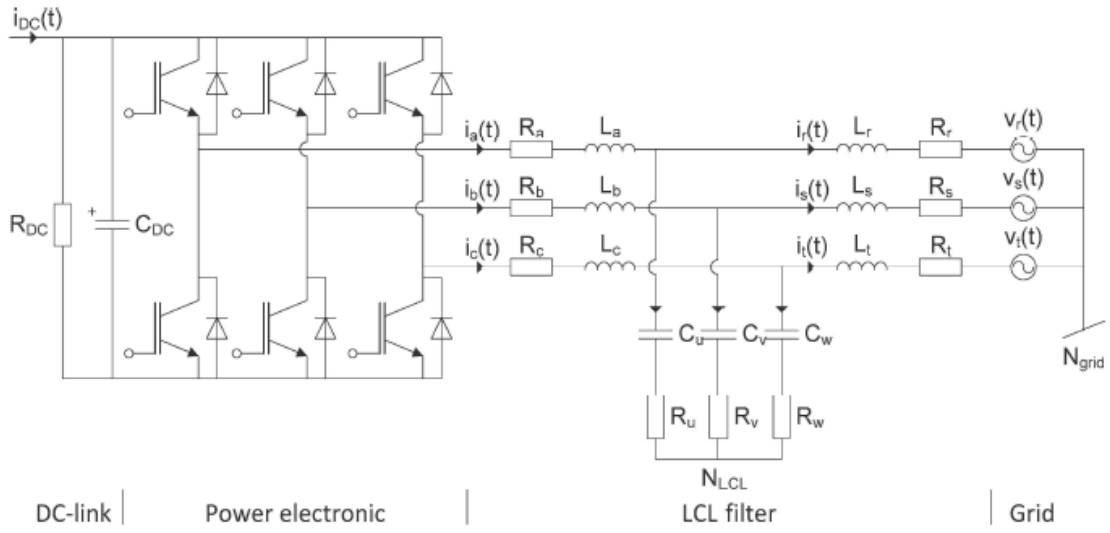


*Figure 2.5 - Power circuit schematic for a stand-alone VSC [2]*

Figure 2.5 shows a two-level three-phase converter and LCL-filter.

First of all, converter consists of 6 IGBT modules that include free-wheel diodes. The IGBT modules and diodes are combined in a power module [19].

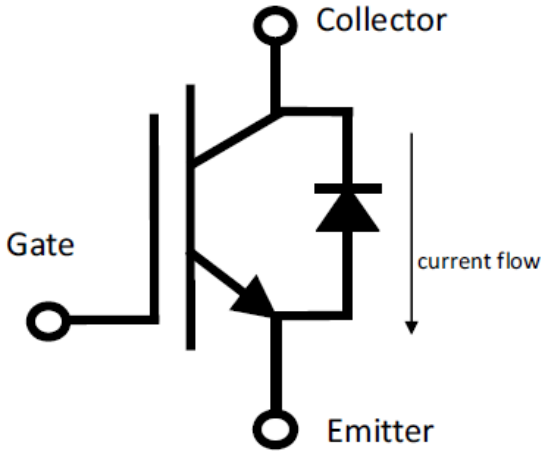


*Figure 2.6 - IGBT with free-wheel diode [19]*

Losses in converter divide into four types, which should be calculated and summarized: IGBT conduction loss, IGBT switching loss (turn-on and turn-off), free wheeling conduction loss, and free wheeling diode recovery loss. See the figure below:

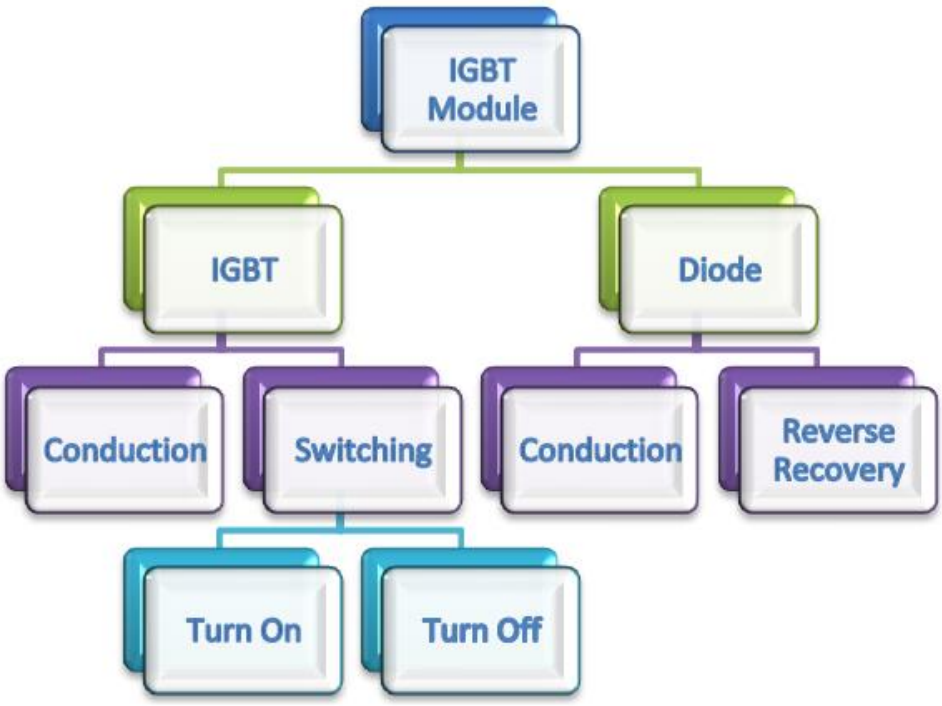


*Figure 2.7 - Losses hierarchy [20]*

The current that flows through diode and voltage drop over collector-emitter produce conduction losses for IGBT and freewheeling diode. Switching losses are the product of energy losses (during state-switching) and switching frequency [20].

#### 2.3.1.1 IGBT conduction losses

Conduction losses in IGBT can be described as [15]: *Conduction losses are the losses that occur while the IGBT or freewheeling diode is on and conducting current, the total power dissipation during conduction is computed by multiplying the on-state voltage and the on-state current.*

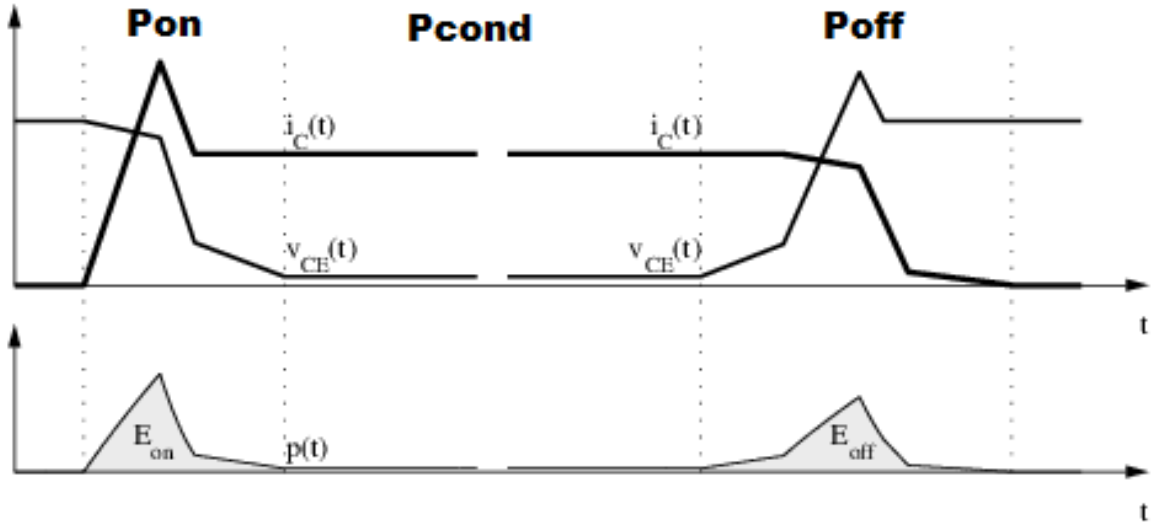


*Figure 2.8 - IGBT switching [20]*

The average power dissipate during steady-state (conduction losses) is derived:

$$P_{IGBT.cond.} = \frac{1}{T}\int_0^T \big(V_{CE}(t) * I_C(t)\big)dt. \tag{2.14}$$

Also, average conduction power losses could be calculated as:

$$P_{IGBT.cond.} = D * V_{CE(sat)} * I_C, \tag{2.15}$$

where:

$V_{CE}$ – collector-emitter voltage. Voltage drop over collector and emitter when conducting a current. Applying voltages to the module exceeding this limit, even of short duration, can lead to device failure. The collector – emitter voltage has a temperature dependency.

$I_C$ - *DC* collector current. DC-current that the IGBT-part of the module can conduct at the given conditions. An exceeding of this limit will lead to over-heating of the device [21].

D – duty-cycle. Duty cycle is a percentage (or ratio) of activity of the system.

$V_{CE(sat)}$- collector-emitter voltage across the IGBT at a specified collector current, gate-emitter voltage, and junction temperature

All current and voltage curves and other information about technical condition of IGBT and diode are shown in the datasheet for this IGBT.

#### 2.3.1.2 IGBT switching losses

In power electronics switching losses typically contribute a significant amount to the total system losses. These types of losses happen when the IGBT switches position from one state to another. During the transition interval both the current through and the voltage across the device are substantially larger than zero which in turn leads to large instantaneous power losses.

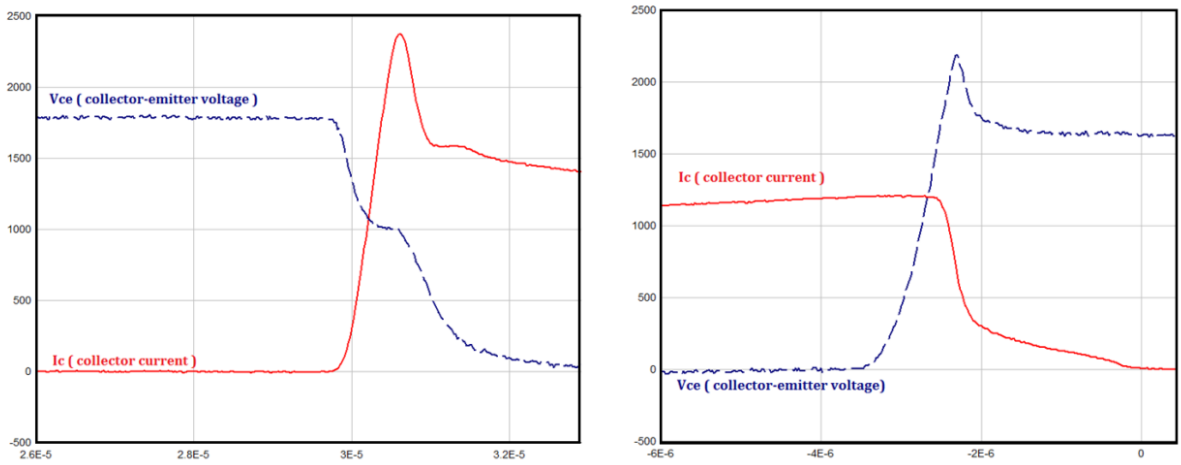


*Figure 2.9 - Voltage and current curves with turn on (left) and turn off (right) state [20]*

As shown in Figure 2.9, the curves show the simplified current and voltage waveforms and the dissipated power during one switching cycle of an IGBT [20].

The switching losses could be calculated as:

$$P_{IGBT.SW.} = \left(E_{SW(on)} + E_{SW(off)}\right) * f_{SW}, \tag{2.16}$$

where:

$f_{SW}$ – switching frequency of IGBT.

$E_{SW(on)}, E_{SW(off)}$ – energy losses (see Figure 2.8), depend on collector current $I_C$ and DC bus voltage. Energy loss curves is shown in the datasheet for IGBT.

Total losses for IGBT are the sum of switching IGBT losses and conduction IGBT losses:

$$P_{IGBT} = P_{IGBT.SW} + P_{IGBT.cond.} \tag{2.17}$$

#### 2.3.1.3 Free wheeling diode conduction losses

A diode is a two-terminal pn–junction device: anode and cathode. It allows current to pass in one direction (conduction state), while blocking current in the opposite direction (the reverse direction).

Since current flows through the diode in time when IGBT is in the turn-off state, diode power conduction losses could be calculated as:

$$P_{cond.diode} = (1 - D) * V_F * I_F, \tag{2.18}$$

where

(1-D) – is the inverse ratio of duty cycle;

$I_F$ – forward current, equals emitter current $I_E$;

$V_F$ – forward voltage, equals emitter-collector voltage, that could be found from curve (in datasheet). This voltage depends on forward current $I_F$.

#### 2.3.1.4 Free wheeling diode recovery losses

When switching from the conduction to the blocking state, a diode or rectifier has stored charge that must be discharged first before the diode blocks reverse voltage. This discharge takes a finite amount of time known as the Reverse Recovery Time, or $t_{rr}$. During this time, diode current may flow in the reverse direction.

When the device turns off it generates losses called recovery losses and the time required to recover is called the reverse recovery time [20].

Free wheeling diode recovery losses:

$$P_{diode,rec.} = E_{rr} * f_{SW}, \tag{2.19}$$

where $E_{rr}$- reverse recovery switching loss, that could be found in datasheet, $f_{SW}$ – switching frequency of IGBT. $E_{rr}$ curve depends on DC voltage and emitter current $I_E$.

The total power losses for diode:

$$P_{diode} = P_{diode,rec.} + P_{cond.diode}. \tag{2.20}$$

The total power losses for the converter (one module):

$$P_{converter} = P_{diode} + P_{IGBT}. \tag{2.21}$$

# 3. Transistors

*This chapter describes what types of transistor technologies can be applied to the proposed models.*

For most of the history of using transistors, a digital transistor was based on metal-oxide-semiconductor (MOS) structure and consists of a polycrystalline silicon gate, a silicon dioxide insulator, and a single crystal silicon channel. But in the last decades new materials and alloys are being used in transistors more and more widely [22].

Several different types of transistors will be described in this chapter, as well as their characteristics and potential of being used in the power converters.

## 3.1 Types of transistors

IGBT (insulated gate bipolar transistor) was considered in Chapter 2 as an example to show losses in transistors. But today two types of transistors are being used in power devices – IGBT and MOSFET (metal-oxide-semiconductor field-effect transistor). It is necessary to show the difference between these two types, their advantages and disadvantages.

### 3.1.1 MOSFET

MOSFET or metal-oxide-semiconductor field-effect transistor is a unipolar device where the current is carried by electrons or holes.

The semiconductor of the channel can be alloyed with impurities to produce electrical conductivity of the P or N type. By applying some potential to the gate, it is possible to change the conductivity type of the channel. If its main charge carriers are displacing by non-main carriers in the channel, then this is the so-called enrichment regime. In this case, the conductivity of the channel increases. By applying the opposite potential to the gate, the channel can be depleted of non-main carriers and reduce its conductivity.

For N-channel MOSFETs, the positive voltage applied to the gate is higher than the threshold voltage of this transistor. Accordingly, for P-channel MOSFETs, the negative voltage applied to the gate is exceeding its threshold.

In most MOSFETs $N^+$ drain and source regions is divided by P-base region as shown in Figure 3.1 [23].

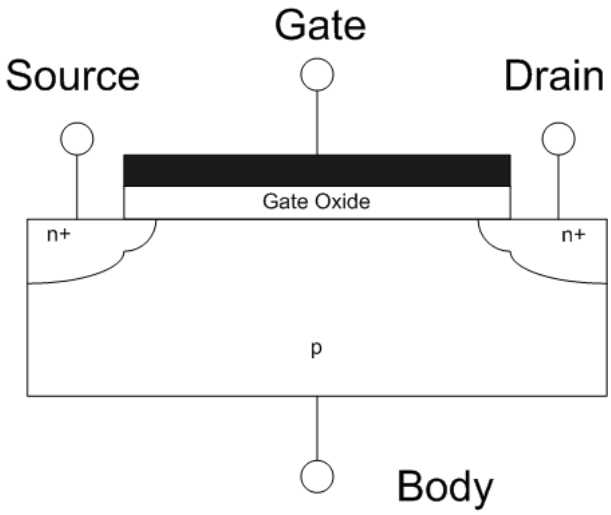


*Figure 3.1 - P-channel MOSFET [23]*

N – channel MOSFET has the difference in structure: $P^+$ drain and source regions and N-base channel.

### 3.1.2 IGBT

IGBT or insulated gate bipolar transistor is a combination of high-input impedance MOS-gate control and low forward voltage drop bipolar current conduction. IGBT is an interesting combination of MOSFET, PIN diode and the bipolar transistor (see Figure 3.2). It combines the attributes of MOSFETs and bipolar transistor with optimal characteristics.

Also, IGBT has no integral diode as MOSFET, it is replaced by external fast recovery diode. Thus, IGBT provides high-impedance MOS gate with large current capability of BJT, and it gives high voltage capability [24].

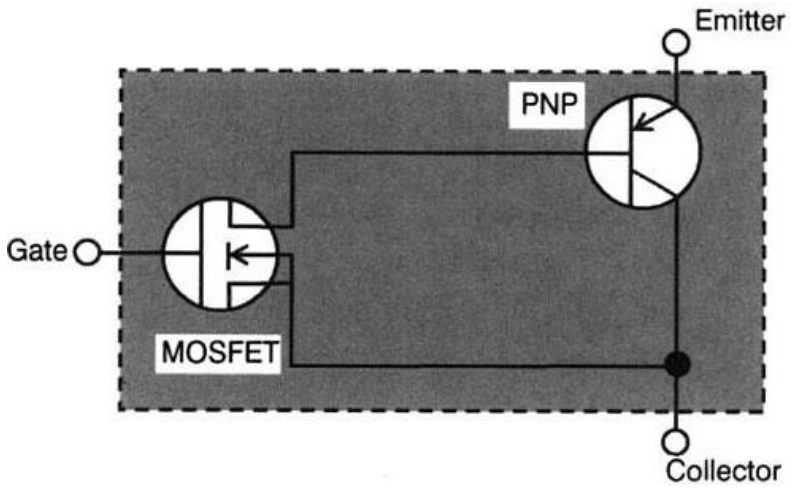


*Figure 3.2 - Simplified equivalent circuit of IGBT [24]*

### 3.1.3 Comparative characteristics

IGBT and MOSFET are the most commonly used power devices. They occupy their own area on the market.

Since the project has a limitation of 400 V, it could be used both - IGBT or MOSFET.

The major difficulty with MOSFETs is reverse recovery characteristic – integral diode produces high losses, and in IGBTs this problem was solved. But IGBT has another disadvantage: IGBT, which includes a field MOSFET transistor that determines the speed of opening, but where the base is not available directly. As a result, the dynamic characteristics of IGBT have limited as well as the switching frequency.

Thus, IGBTs have limited switching frequency up to 30 kHz and high voltage (more than 4000 V). MOSFETs are the fastest transistors today (more than 100 kHz), but they are preferred for low voltage. 250-300 volts were the limit for MOSFETs a few years ago, but today new technologies are imposing new limits, and there are 4000 volts limited MOSFET on the market today, but with low current (0.2 – 3 A with that voltage).

## 3.2 Transistor technology

There are many transistor technologies on the market today. During the last two decades many materials for transistors have been developed and implemented. Some of them are popular and widespread in use, some of them have a very special use.

Gallium-Arsenide, for example, cannot be used in this project. Transistors using this technology have high-electron mobility and a switching frequency of more than 3 GHz. But the technology is at the beginning of its development and has very low drain-source voltage (around 6-8 volts). This HEMT (high-electron mobility transistor) has high gain, high efficiency and high linearity, but according to project voltage limitation (400 V) it is not possible to use these transistors.

Three transistor technologies will be considered in the project silicon (Si), silicon carbide (SiC) and gallium nitride (GaN).

### 3.2.1 Silicon technology

Nowadays, silicon (Si) transistors are most used in power devices. The main advantages are cost and breadth of application.

Pure silicon is produced by the carbothermic reduction of silica. Silica occurs naturally as quartz. Pure silicon can be obtained in an electric arc furnace, the overall reaction is [25]:

$$SiO_2 + 2C \rightarrow Si + 2CO. \quad (3.1)$$

Silicon semiconductors can be performed both by IGBT and MOSFET. The comparative table that is based on experimental results in [26] is shown below. IGBT (STGF6NC60HD) and MOSFET (IRFI840G) with similar parameters ($V_{CES}$ = 600 V, $I_C = 6\ A$ for IGBT and $V_{DS}$ = 500 V, $I_D = 4.6\ A$ for MOSFET) was taken:

*Table 3.1 - Extracted switching parameters at $V_{DS} = 250\ V$ and $I_D = 2.5\ A$*

| | **Turn on timing parameters** | | | | **Turn off timing parameters** | | | |
|---|---|---|---|---|---|---|---|---|
| | $t_{ri}\ (ns)$ | $t_{fv}\ (ns)$ | **Peak di/dt (A/ns)** | **Peak dv/dt (V/ns)** | $t_{fi}\ (ns)$ | $t_{rv}\ (ns)$ | **Peak di/dt (A/ns)** | **Peak dv/dt (V/ns)** |
| **MOSFET** | 5 | 10 | 0.468 | 27.6 | 16 | 14 | 0.193 | 19.68 |
| **IGBT** | 8 | 32 | 0.288 | 2.56 | 158 | 27 | 0.0669 | 8.56 |

Table 3.1 shows that $t_{ri}, t_{fv}, t_{fi}, t_{rv}$ are 2-3 times higher for IGBT in compared to MOSFET. It shows that switching frequency higher for MOSFET 2-3 times. Peak di/dt and shows different parasitic inductance and capacitance and peak dv/dt pushes current back into the gate driver.

Experimental results [26] show that losses in IGBT are much greater than in MOSFET with low current, but the gap is narrowing with the increase of current because of low drain-source on-state resistance

### 3.2.2 Silicon carbide technology

The first research of silicon carbide technology dates from the 1950s, but not until the 2000s the first industrial manufacturing of silicon carbide was made. It was made after new discoveries in the usability of silicon carbide for industrial manufacturing.

With the approaching of physical limits on silicon, the new technologies are interesting for industry. The first choice was silicon carbide - well-known characteristic and relative cheapness.

The crystal structure of silicon carbide can be expressed as stacking compact plans where each plan consists of two layers – a silicon layer and a carbide layer. The link between carbide C and silicon Si is very strong, that is why SiC is a very resistant material: high temperature resistant (breaking at $2830^0 C$),

chemically resistant (it is hard for a foreign atom to penetrate in SiC), mechanically resistant (hardness is three times more than of silicon).

Different variations of stacking sequence lead to different crystalline forms: cubic (C), hexagonal (H), rhomboid (R).

From 170 to 200 polytypes exists, but only a few of them can be synthesized in a stable form. The most common polytypes used for electronics are: 3C-SiC, 4H-SiC, 6H-SiC [27].

The formula to get silicon carbide by the Acheson method (pure silica sand ($SiO_2$) and ground coke (C) are mixed and heated in a furnace):

$$SiO_3 + 3C \rightarrow SiC + 2CO. \tag{3.2}$$

IGBT and MOSFET could be made by silicon carbide. The difference between them is the same as between silicon IGBT and MOSFET, that was shown in chapter 3.2.1.

### 3.2.3 Gallium Nitride technology

The first appearing of power devices, which was based on Gallium Nitride high electron mobility transistor (HEMT), was in 2004.

Figure 3.4 shows that the top layer in GaN semiconductor is AlGaN instead of $SiO_2$ as in silicon or silicon carbide semis. This AlGaN layer creates a strain at the interface (between AlGaN and GaN), and this strain produces a piezoelectric effect that leads to a very high conductivity because of the crystal structure of GaN [28].

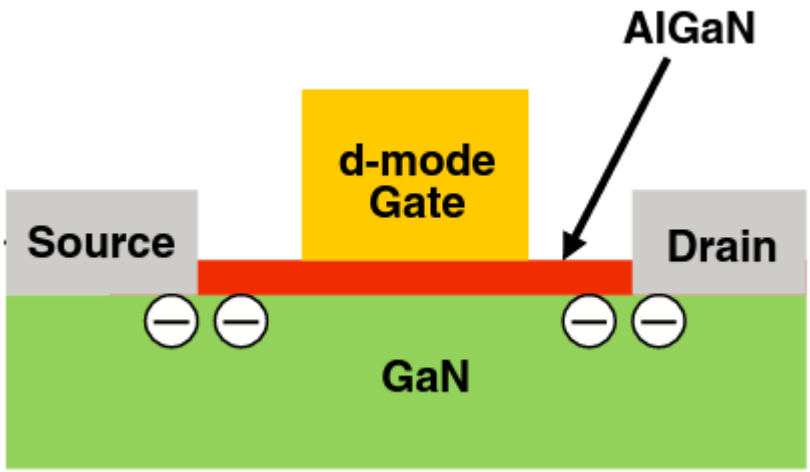


*Figure 3.3 - The basic GaN transistor structure [28]*

### 3.2.4 Comparison of transistor types

From [28] follows Table 3.2

*Table 3.2 - Material properties of Silicon, GaN, and SiC*

| **Parameter** | **Si** | **GaN** | **SiC** |
|---|---|---|---|
| **Band gap (eV)** | 1.12 | 3.39 | 3.26 |
| **Critical field (MV/cm)** | 0.23 | 3.3 | 2.2 |
| **Electron mobility ($cm^2/Vs$)** | 1400 | 1500 | 950 |

Higher bandgap temperature makes higher temperature operation feasible. A higher critical field means that thinner blocking junction could be used to give voltage and therefore provides less losses. Electron mobility shows a drift velocity of carriers.

The table above shows that SiC semiconductors surpass Si semiconductors in all main properties, except electron mobility that depends on the crystalline structure.

From Table 3.2 it follows that GaN has a band gap and a critical field similar to SiC, but the electron mobility is higher and closer to silicon. It shows that the switching frequency of GaN is even more than SiC with lower losses. But all benefits of GaN could be used with very high frequency (400 kHz and higher) [29].

In this project frequencies and voltages with lower values will be used. Conclusion on the best type of transistors applicable in the project can be done only after obtaining the results of the experiments.

# 4. Models of control

*This chapter describes the detailed and simplified models of a two-level three-phase converter. It also describes the model predictive control and vector oriented control algorithms.*

## 4.1 Mathematical model of converter with LCL filter

### 4.1.1 System of equations

The figure below shows two-level three-phase voltage source converter with LCL filter connected to the grid.

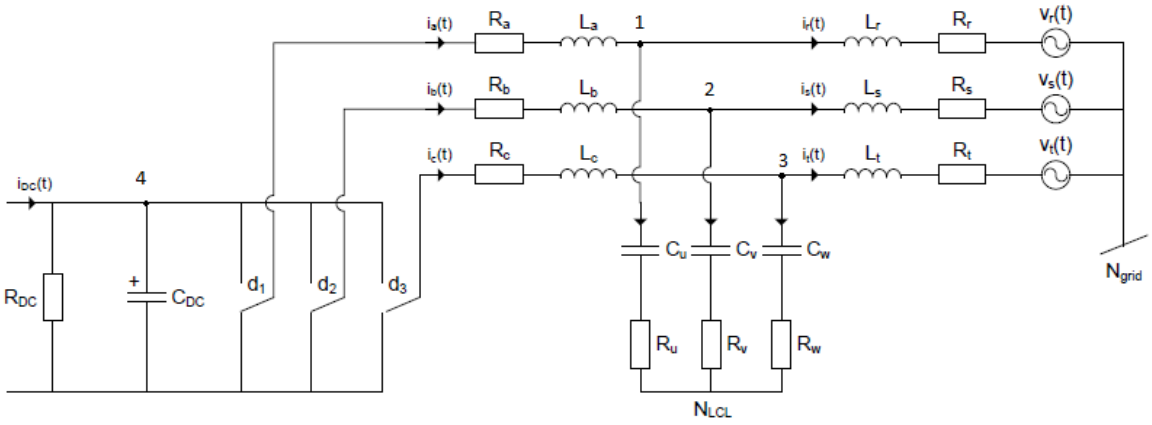


*Figure 4.1 - Converter connected to the grid using LCL filter [30]*

Resistance in cables and inductors on the converter side are $R_a, R_b, R_c$, on the grid side are $R_r, R_s, R_t$. LCL filter consists of inductance on the converter side ($L_a, L_b, L_c$) and grid side ($L_r, L_s, L_t$), conductance ($C_u, C_v, C_w$) and three damping resistors ($R_u, R_v, R_w$). These damping resistors are included in the series with conductance in case passive damping is used.

Voltages $v_r(t), v_s(t), v_t(t)$ are grid phase voltages, $i_r(t), i_s(t), i_t(t)$ are grid side phase currents and $i_a(t), i_b(t), i_c(t)$ are converter side phase currents.

Some simplifications will be assumed in the model, for example the constant DC-link voltage or averaging over a switching period. But DC-link voltage will be included in the mathematical model as a state variable. $N_{grid}$ and $N_{LCL}$ are floating neutral points [31].

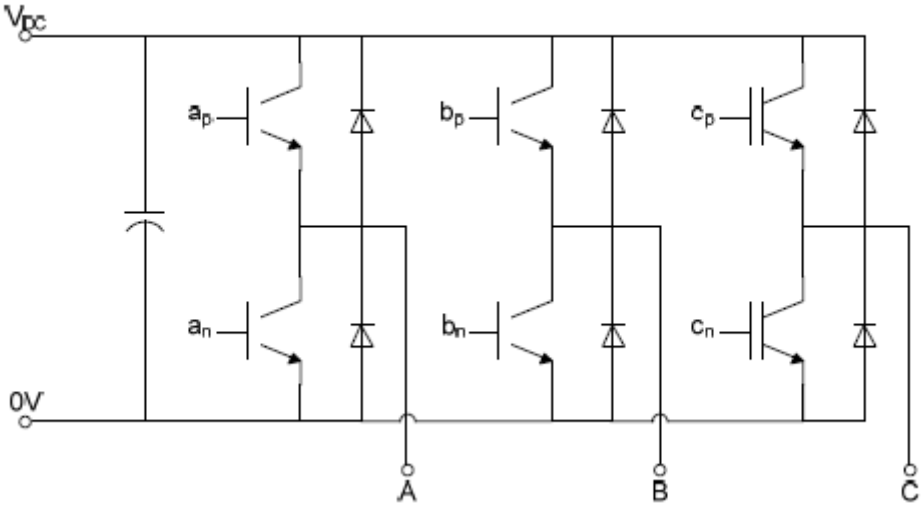


*Figure 4.2 - Configuration of a real converter [31]*

Figure 4.2 shows that each phase has two transistors. In case of $a_p = b_p = c_p = 1$ transistors connected to the positive DC-link, if $a_n = b_n = c_n = 1$ – to the negative.

On the simplified circuit 4.1 transistors with diodes are shown as switches $d_1, d_2, d_3$. Therefore, $d_1 = d_2 = d_3 = 1$ when DC-link is positive, and equal zero when DC-link is negative.

The mathematical model of the electrical circuit can be created using Kirchhoff's voltage and current laws.

According to Kirchhoff's current law for nodes 1,2,3:

$$i_a(t) = i_{C_u}(t) + i_r(t), \tag{4.1}$$

$$i_b(t) = i_{C_v}(t) + i_s(t), \tag{4.2}$$

$$i_c(t) = i_{C_w}(t) + i_t(t). \tag{4.3}$$

Voltages and current that flows through inductors and capacitors can be derived as:

$$i_C = C\frac{dv_C}{dt}, \tag{4.4}$$

$$v_L = L\frac{di_L}{dt}. \tag{4.5}$$

Apply equation (4.5) to equations (4.1-4.3):

$$C_u \frac{dv_{C_u}}{dt} = i_a(t) - i_r(t); \tag{4.6}$$

$$C_v \frac{dv_{C_v}}{dt} = i_b(t) - i_s(t), \tag{4.7}$$

$$C_w \frac{dv_{C_w}}{dt} = i_c(t) - i_t(t). \tag{4.8}$$

The equation for node 4 according to first Kirchhoff's law:

$$i_{DC}(t) = i_{R_{DC}}(t) + i_{C_{DC}}(t) + d_1(t) \cdot i_a(t) + d_2(t) \cdot i_b(t) + d_3(t) \cdot i_c(t). \tag{4.9}$$

Apply equation (4.5) and Ohm law to equation (4.9):

$$C_{DC} \frac{dv_{DC}}{dt} = i_{DC}(t) - \frac{v_{DC}(t)}{R_{DC}} - d_1(t) \cdot i_a(t) - d_2(t) \cdot i_b(t) - d_3(t) \cdot i_c(t). \tag{4.10}$$

DC-link voltage equals $C_{DC}$ charge voltage and depends on converter switches (described by equation (4.10)) [31]

According to Kirchhoff's voltage law, the algebraic sum of voltages of a closed circuit equals zero. The circuit (4.1) can be divided into 4 closed loops: 2 loops – DC-link - $N_{LCL}$( $v_a - v_b, v_b - v_c$ and 2 loops - $N_{LCL}$ - $N_{Grid}$ ($v_a - v_b$ , $v_b - v_c$).

Therefore, there are 4 equations more:

1. DC-link - $N_{LCL}$( $v_a - v_b$):

$$v_{DC} \cdot d_1 - v_{R_a} - v_{L_a} - v_{C_u} - v_{R_u} + v_{R_v} + v_{C_v} + v_{L_b} + v_{R_b} - v_{DC} \cdot d_2 = 0. \tag{4.11}$$

Use equation (4.5) to substitute voltages across inductors and equations (4.1) and (4.2) to derive currents through conductors:

$$L_a \frac{di_a(t)}{dt} - L_b \frac{di_b(t)}{dt} = v_{DC}(t) \cdot d_1(t) - R_a i_a(t) - v_{C_u}(t) - R_u\big(i_a(t) - i_r(t)\big) + \\ + v_{C_v}(t) + R_v\big(i_b(t) - i_s(t)\big) + R_b i_b(t) - v_{DC} d_2(t). \tag{4.12}$$

2. DC-link - $N_{LCL}$( $v_b - v_c$), the same operation as above, but for loop with phases **b** and **c:**

$$L_b \frac{di_b(t)}{dt} - L_c \frac{di_c(t)}{dt} = v_{DC}(t) \cdot d_2(t) - R_b i_b(t) - v_{C_v}(t) - R_v\big(i_b(t) - i_s(t)\big) + v_{C_w}(t) + \\ + R_w\big(i_c(t) - i_t(t)\big) + R_c i_c(t) - v_{DC} d_3(t). \tag{4.13}$$

3. $N_{LCL}$ - $N_{Grid}$ $(v_a - v_b)$:

$$v_{R_u} + v_{C_u} - v_{L_r} - v_{R_r} - v_r + v_{L_s} + v_{R_s} + v_s - v_{R_v} + v_{C_v} = 0. \quad (4.14)$$

By substitution equation (4.5) for inductors and equations (4.1) and (4.2) for currents, it follows that:

$$-L_r \frac{di_r(t)}{dt} + L_s \frac{di_s(t)}{dt} = v_r(t) + R_r i_r(t) - v_{C_u}(t) - R_u\big(i_a(t) - i_r(t)\big) + v_{C_v}(t) + +R_v\big(i_b(t) - i_s(t)\big) - R_s i_s(t) - v_s(t) \quad (4.15)$$

4. $N_{LCL}$ - $N_{Grid}$ $(v_b - v_c)$:

$$-L_s \frac{di_s(t)}{dt} + L_t \frac{di_t(t)}{dt} = v_s(t) + R_s i_s(t) - v_{C_v}(t) - R_v\big(i_b(t) - i_s(t)\big) + v_{C_w}(t) + +R_w\big(i_c(t) - i_t(t)\big) - R_t i_t(t) - v_t(t) \quad (4.16)$$

The equations above describe voltage source converter (VSC) with LCL filter dynamics. The system of equation is based on eight equations ((4.6-4.8), (4.10), (4.12), (4.13), (4.15), and (4.16)) and ten variables (DC-side capacitor voltage$v_{dc}$, three LCL capacitor voltages $v_{C_u}, v_{C_v}, v_{C_w}$ and six currents that flows through inductors $i_a, i_b, i_c, i_r, i_s \; and \; i_t$), but some of them are linear dependent, and the order of system can be reduced.

### 4.1.2 System reduction

Since there are no neutral wires, the algebraic sum of all phase currents equals zero. Applying this statement to the circuit, currents can be expressed as:

$$i_a(t) + i_b(t) = -i_c(t), \quad (4.17)$$

$$i_r(t) + i_s(t) = -i_t(t), \quad (4.18)$$

$$i_{C_u}(t) + i_{C_v}(t) + i_{C_w}(t) = 0. \quad (4.19)$$

Therefore, applying equations (4.17) and (4.18) to (4.10), (4.13) and (4.16), Therefore (4.13) looks like this:

$$L_b \frac{di_b(t)}{dt} + L_c \frac{di_c(t)}{dt} + L_c \frac{di_c(t)}{dt} = v_{DC}(t) \cdot d_2(t) - R_b i_b(t) - v_{C_v}(t) - R_v\big(i_b(t) - i_s(t)\big) + v_{C_w}(t) + R_w\big(-i_a(t) - i_b(t) + i_r(t) + i_s(t)\big) - R_c i_a(t) - R_c i_b(t) - -v_{DC} d_3(t). \quad (4.20)$$

After rearranging the equations (4.12) and (4.20):

$$\frac{di_a(t)}{dt} = -i_a(t)\frac{L_c(R_a+R_u)+L_b(R_a+R_c+R_u+R_w)}{L_{sig_a}} + i_b(t)\frac{L_c(R_b+R_v)-L_b(R_c+R_w)}{L_{sig_a}} + +i_r(t)\frac{L_cR_u+L_b(R_u+R_w)}{L_{sig_a}} + i_s(t)\frac{-L_cR_v+L_bR_w}{L_{sig_a}} + v_{C_v}(t)\frac{L_c}{L_{sig_a}} - v_{C_u}(t)\frac{L_b+L_c}{L_{sig_a}} + v_{C_w}(t)\frac{L_b}{L_{sig_a}} + +v_{DC}(t)\frac{L_c(d_1-d_2)+L_b(d_2-d_3)}{L_{sig_a}}, \quad (4.21)$$

$$\frac{di_b(t)}{dt} = i_a(t)\frac{L_c(R_a+R_u)-L_a(R_c+R_w)}{L_{sig_a}} - i_b(t)\frac{L_c(R_b+R_v)+L_a(R_b+R_c+R_v+R_w)}{L_{sig_a}} + +i_s(t)\frac{L_cR_v+L_a(R_v+R_w)}{L_{sig_a}} + i_r(t)\frac{-L_cR_u+L_aR_w}{L_{sig_a}} + v_{C_u}(t)\frac{L_c}{L_{sig_a}} - v_{C_v}(t)\frac{L_a+L_c}{L_{sig_a}} + v_{C_w}(t)\frac{L_a}{L_{sig_a}} + +v_{DC}(t)\frac{L_c(d_2-d_1)+L_a(d_2-d_3)}{L_{sig_a}}, \quad (4.22)$$

where $L_{sig_a} = L_aL_b + L_aL_c + L_bL_c$.

The same steps can be done with (4.15), (4.16) and (4.18):

$$\frac{di_r(t)}{dt} = i_a(t)\frac{L_s(R_u+R_w)+L_tR_u}{L_{sig_r}} + i_b(t)\frac{L_sR_w-L_tR_v}{L_{sig_r}} + v_t(t)\frac{L_s}{L_{sig_r}} - -i_r(t)\frac{L_s(R_r+R_t+R_u+R_w)+L_t(R_r+R_u)}{L_{sig_r}} + i_s(t)\frac{-L_s(R_t+R_w)+L_t(R_s-R_v)}{L_{sig_r}} - v_{C_v}(t)\frac{L_t}{L_{sig_r}} + v_{C_u}(t)\frac{L_t+L_s}{L_{sig_r}} - -v_{C_w}(t)\frac{L_s}{L_{sig_r}} - v_r(t)\frac{L_t+L_s}{L_{sig_r}} + v_s(t)\frac{L_t}{L_{sig_r}}, \quad (4.23)$$

$$\frac{di_s(t)}{dt} = i_a(t)\frac{L_rR_w-L_tR_u}{L_{sig_r}} + i_b(t)\frac{L_r(R_v+R_w)+L_tR_v}{L_{sig_r}} + v_t(t)\frac{L_r}{L_{sig_r}} + i_r(t)\frac{-L_r(R_t+R_w)+L_t(R_r+R_u)}{L_{sig_r}} - -i_s(t)\frac{L_r(R_s+R_t+R_v+R_w)+L_t(R_s+R_v)}{L_{sig_r}} + v_{C_v}(t)\frac{L_t+L_r}{L_{sig_r}} - v_{C_u}(t)\frac{L_t}{L_{sig_r}} - v_{C_w}(t)\frac{L_r}{L_{sig_r}} + v_r(t)\frac{L_t}{L_{sig_r}} - -v_s(t)\frac{L_t+L_r}{L_{sig_r}}, \quad (4.24)$$

where $L_{sig_r} = L_rL_s + L_rL_t + L_sL_t$ [7].

The system consists of eight state variables. One more variable can be eliminated according to the next action: substitute (4.6-4.8) into (4.19):

$$C_u\frac{dv_{C_u}(t)}{dt} + C_v\frac{dv_{C_v}(t)}{dt} + C_w\frac{dv_{C_w}(t)}{dt} = 0. \quad (4.25)$$

One of the capacitors can be expressed by the two other:

$$\int_0^\tau C_w\frac{dv_{C_w}(t)}{dt}dt = -\int_0^\tau C_u\frac{dv_{C_u}(t)}{dt}dt - \int_0^\tau C_v\frac{dv_{C_v}(t)}{dt}dt \ , \quad (4.26)$$

$$v_{C_w}(\tau) = -\frac{C_uv_{C_u}(\tau)}{C_w} - \frac{C_vv_{C_v}(\tau)}{C_w} + \frac{K}{C_w}. \quad (4.27)$$

The constant K can be derived from initial conditions:

$$K = C_u v_{C_u}(0) + C_v v_{C_v}(0) + C_w v_{C_w}(0). \tag{4.28}$$

In most situations K with initial conditions equals zero or it can be said that the sum of charge in the capacitors equals zero, K=0 [2].

### 4.1.3 State-space model

The system that is shown in Figure 4.1 can be described with equations from the previous chapter, and the state-space model can be constructed.

State-variable representation of a system is a set of first order differential equations on the standard form:

$$\dot{x} = Ax + Bu. \tag{4.29}$$

Where A is an n x n system matrix, B is an n x m input matrix, n is a number of state variables, m – a number of inputs.

From the previous chapter: $i_a(t), i_b(t), i_r(t), i_s(t), v_{C_u}(t), v_{C_v}(t), v_{DC}(t)$ are state variables of the system; $v_r(t), v_s(t), v_t(t), i_{DC}(t), K$ – inputs of the system.

Therefore, the state vector is:

$$x = [i_a(t) \quad i_b(t) \quad i_r(t) \quad i_s(t) \quad v_{C_u}(t) \quad v_{C_v}(t) \quad v_{DC}(t)]^T, \tag{4.30}$$

and the vector input is:

$$u = [v_r(t) \quad v_s(t) \quad v_t(t) \quad i_{DC}(t) \quad K]^T. \tag{4.31}$$

Matrix A depends on converter switching parameters. Each switch this matrix will be calculated. That is why this system is a piecewise linear state-space system. Matrix a depends on a position of the switches $d_1, d_2, d_3$ [2]:

$$
A(d_1,d_2,d_3)=\begin{bmatrix}
-\frac{L_b(R_a+R_c+R_u+R_w)+L_c(R_a+R_u)}{L_{sigA}} & \frac{L_c(R_b+R_v)-L_b(R_c+R_w)}{L_{sigA}} \\
\frac{L_c(R_a+R_u)-L_a(R_c+R_w)}{L_{sigA}} & -\frac{L_a(R_b+R_c+R_v+R_w)+L_c(R_b+R_v)}{L_{sigA}} \\
\frac{L_s(R_u+R_w)+L_tR_u}{L_{sigR}} & \frac{L_sR_w-L_tR_v}{L_{sigR}} \\
\frac{L_rR_w-L_tR_u}{L_{sigR}} & \frac{L_r(R_v+R_w)+L_tR_v}{L_{sigR}} \\
1/C_u & 0 \\
0 & 1/C_v \\
\left(d_3(t)-d_1(t)\right)/C_{DC} & \left(d_3(t)-d_2(t)\right)/C_{DC}
\end{bmatrix}
$$

$$
\begin{bmatrix}
\frac{L_b(R_u+R_w)+L_cR_u}{L_{sigA}} & \frac{L_bR_w-L_cR_v}{L_{sigA}} \\
\frac{L_aR_w-L_cR_u}{L_{sigA}} & \frac{L_a(R_v+R_w)+L_cR_v}{L_{sigA}} \\
-\frac{L_s(R_r+R_t+R_u+R_w)+L_t(R_r+R_u)}{L_{sigR}} & \frac{L_t(R_s-R_v)-L_s(R_t+R_w)}{L_{sigR}} \\
\frac{L_t(R_r+R_u)-L_r(R_t+R_w)}{L_{sigR}} & -\frac{L_r(R_s+R_t+R_v+R_w)+L_t(R_s+R_v)}{L_{sigR}} \\
-1/C_u & 0 \\
0 & -1/C_v \\
0 & 0
\end{bmatrix}
$$

$$
\begin{bmatrix}
-\frac{L_b(C_u+C_w)+L_cC_w}{C_wL_{sigA}} & \frac{L_cC_w-L_bC_v}{C_wL_{sigA}} & \frac{L_b\left(d_1(t)-d_3(t)\right)+L_c\left(d_1(t)-d_2(t)\right)}{L_{sigA}} \\
\frac{L_cC_w-L_aC_u}{C_wL_{sigA}} & -\frac{L_a(C_v+C_w)+L_cC_w}{C_wL_{sigA}} & \frac{L_a\left(d_2(t)-d_3(t)\right)+L_c\left(d_2(t)-d_1(t)\right)}{L_{sigA}} \\
\frac{L_{s(C_u+C_w)}+L_tC_w}{C_wL_{sigR}} & \frac{L_sC_v-L_tC_w}{C_wL_{sigR}} & 0 \\
\frac{L_rC_u-L_tC_w}{C_wL_{sigR}} & \frac{L_r(C_v+C_w)+L_tC_w}{C_wL_{sigR}} & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & -1/(C_{DC}R_{DC})
\end{bmatrix},
$$

(4.32)

The input matrix consists of constant parameters:

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{L_b}{C_w L_{sig_a}} \\ 0 & 0 & 0 & 0 & \frac{L_a}{C_w L_{sig_a}} \\ -\frac{L_s+L_t}{L_{sig_r}} & \frac{L_t}{L_{sig_r}} & \frac{L_s}{L_{sig_r}} & 0 & -\frac{L_s}{C_w L_{sig_r}} \\ \frac{L_t}{L_{sig_r}} & \frac{L_r+L_t}{L_{sig_r}} & \frac{L_r}{L_{sig_r}} & 0 & -\frac{L_r}{C_w L_{sig_r}} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/C_{DC} & 0 \end{bmatrix}. \quad (4.33)$$

### 4.1.4 Simplified state-space models

The model from Chapter 4.1.3 includes unsymmetrical components, but in most common cases the components are symmetrical (i.e., the filter parameters are equal in all three phases) and can be simplified [2]:

$$\mathrm{A(t)} = \begin{bmatrix} -\frac{R_{abc}+R_{uvw}}{L_{abc}} & 0 & \frac{R_{uvw}}{L_{abc}} & 0 & -\frac{1}{L_{abc}} & 0 & \frac{2d_1(t)-d_2(t)-d_3(t)}{3L_{abc}} \\ 0 & -\frac{R_{abc}+R_{uvw}}{L_{abc}} & 0 & \frac{R_{uvw}}{L_{abc}} & 0 & -\frac{1}{L_{abc}} & \frac{-d_1(t)+2d_2(t)-d_3(t)}{3L_{abc}} \\ \frac{R_{uvw}}{L_{rst}} & 0 & -\frac{R_{rst}+R_{uvw}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 & 0 \\ 0 & \frac{R_{uvw}}{L_{rst}} & 0 & -\frac{R_{rst}+R_{uvw}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 \\ \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 & 0 \\ \frac{d_3(t)-d_1(t)}{C_{DC}} & \frac{d_3(t)-d_2(t)}{C_{DC}} & 0 & 0 & 0 & 0 & -\frac{1}{C_{DC}R_{DC}} \end{bmatrix}, \quad (4.34)$$

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{3L_{abc}C_{uvw}} \\ 0 & 0 & 0 & 0 & \frac{1}{3L_{abc}C_{uvw}} \\ -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & \frac{1}{3L_{rst}} & 0 & -\frac{1}{3L_{rst}C_{uvw}} \\ \frac{1}{3L_{rst}} & -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & 0 & -\frac{1}{3L_{rst}C_{uvw}} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_{DC}} & 0 \end{bmatrix}. \quad (4.35)$$

Active damping will be used in this project and damping resistors can be eliminated from the model. The constant K is zero in most cases. Therefore, input vector can be removed either.

The final simplified state-space models after all these simplifications are [2]:

$$A(t) = \begin{bmatrix} -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & -\frac{1}{L_{abc}} & 0 & \frac{2d_1(t)-d_2(t)-d_3(t)}{3L_{abc}} \\ 0 & -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & -\frac{1}{L_{abc}} & \frac{-d_1(t)+2d_2(t)-d_3(t)}{3L_{abc}} \\ 0 & 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 & 0 \\ 0 & \frac{R_{uvw}}{L_{rst}} & 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 \\ \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 & 0 \\ \frac{d_3(t)-d_1(t)}{C_{DC}} & \frac{d_3(t)-d_2(t)}{C_{DC}} & 0 & 0 & 0 & 0 & -\frac{1}{C_{DC}R_{DC}} \end{bmatrix},$$

(4.36)

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & \frac{1}{3L_{rst}} & 0 \\ \frac{1}{3L_{rst}} & -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_{DC}} \end{bmatrix}, \tag{4.37}$$

$$u = [v_r(t) \quad v_s(t) \quad v_t(t) \quad i_{DC}(t)]^T. \tag{4.38}$$

**K** has been removed from the input vector [2].

DC-link voltage can also be removed from the state vector if the voltage is kept constant by an external device or the system is considered over a short period [2].

## 4.2 Model predictive control algorithm

This project is based on the existing model [2]. Finite control is being used to calculate and choose the lowest error/cost. A two-level three-phase converter has eight possible switch variants (but only 7 are unique), and therefore the number of switch combinations is $N^8$ where N is the prediction horizon.

An LCL filter is assumed to be used in the converter and active damping algorithm is the more preferable. Active damping method has less THD than passive method, also passive damping brings more losses due to additional components (damping resistors) [32]. Active damping method requires high computational burden with finite control set because of the fact that a longer prediction horizon is needed to achieve active damping. More time is needed to predict, find and reduce oscillations in the filter. This problem can be solved by using continuous control set [2].

Continuous control set MPC can be used in this project, but it is needed to use a modulator that requires an updated duty cycle each switching period. Using the modulator gives a longer response time. Thus, the best option is to use a cascaded MPC, where the grid current and the converter current are controlled separately.

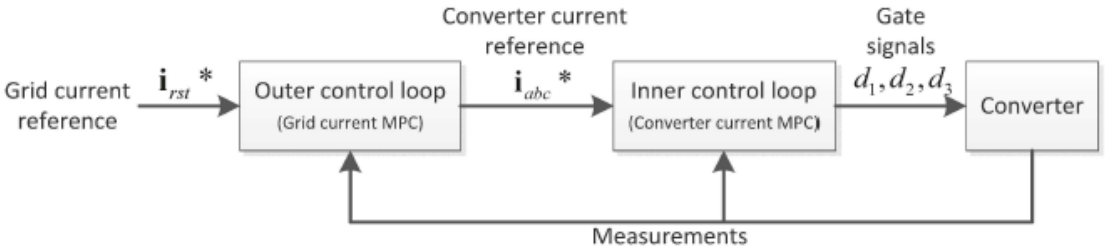


*Figure 4.3 - Cascaded model predictive control [1]*

A step change in voltage on the converter side leads to a chain of changes as follows: this voltage affects the converter current; this current in turn affects the capacitor voltages in the filter, and these voltages in their turn affect the grid side current. This chain leads to a computational delay between these currents – the converter side currents change much faster than the grid side currents.

Figure 4.3 shows that converter current (faster) controller is situated in the inner loop, while grid current (slower) controller is situated in the outer loop.

As approved in [1], converter side MPC can be based on finite control set, while grid side MPC can use a more comprehensive continuous control set.

### 4.2.1 Converter current MPC

The converter controller controls the currents directly and can change it fast. The one-step MPC finite control set calculates eight possible switch combinations and picks the one with the lowest cost.

Some simplifications are used in this project (which were assumed in [2]): no compensation for dead-time and no restriction on switching frequency.

Dead-time is more relevant for a long prediction horizon and it is not relevant for this controller with a one-step prediction.

Since one of the main purposes of this project is to find the efficiency of MPC, it has no sense to restrict switching frequency to what can lead to restriction of converter losses.

The system matrix A in (4.36) is a state-space model for MPC. Since the inner MPC controls only converter side currents, the rows which do not consist of a converter side elements should be eliminated [2]:

$$A_{1,2}(d_1,d_2,d_3)=\begin{bmatrix} -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & -\frac{1}{L_{abc}} & 0 & \frac{2d_1(t)-d_2(t)-d_3(t)}{3L_{abc}} \\ 0 & -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & -\frac{1}{L_{abc}} & \frac{-d_1(t)+2d_2(t)-d_3(t)}{3L_{abc}} \end{bmatrix}. \quad (4.39)$$

The first two rows in matrix B (4.37) are equal to zero, thus matrix B can be removed from the algorithm.

The model converts to the discrete system using zero order hold. The cost function is represented as a minimization:

$$\min_{d_1,d_2,d_3} . \ \left|\left|{i_{abc}}^* - y_{k+1}\right|\right|_2^2$$

$$s.t. \quad x_{k+1} = A(d_1,d_1,d_1)x_k \quad (4.40)$$

$$y_{k+1} = Cx_{k+1},$$

where ${i_{abc}}^*$ are the converter current references, $y_{k+1}$ are predicted converter currents, matrix C shows system measurements:

$$C=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \quad (4.41)$$

### 4.2.2 Grid current MPC

The outer controller produces the converter side current references as shown in Figure 4.3. Thus the inner controller can be described as [2]:

$$\frac{di_{abc}(t)}{dt} = -\frac{1}{T_{inner}} i_{abc}(t) + \frac{1}{T_{inner}} i^*_{abc}(t), \quad (4.42)$$

where $T_{inner}$ is constant response time for converter side currents in the inner controller.

This expression gives the opportunity to remove the switched elements from the grid current controller and describe state-space model with constant matrices only:

$$\dot{x}(t) = Ax(t) + Bu(t) + Fv(t), \quad (4.43)$$

$$y(t) = Cx(t)\,, \quad (4.44)$$

where x(t) is state vector, $u(t)$ is input vector and $v(t)$ – disturbance vector:

$$x(t) = [i_a(t) \quad i_b(t) \quad i_r(t) \quad i_s(t) \quad v_{C_u}(t) \quad v_{C_v}(t) \quad ]^T, \tag{4.45}$$

$$u(t) = [i_a^*(t) \quad i_b^*(t)]^T, \tag{4.46}$$

$$v(t) = [v_r(t) \quad v_s(t) \quad v_t(t)]^T. \tag{4.47}$$

DC-link voltage is not available from the outer controller and not a part of the state vector. But DC-link voltage effects on the outer controller, but indirectly as uncontrolled disturbances $Fv(t)$.

Thus matrices from (4.43) and (4.44) can be expressed and modified from the model (4.36) and (4.37) as [2]:

$$A = \begin{bmatrix} -\frac{1}{T_{inner}} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{T_{inner}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 \\ 0 & 0 & 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} \\ \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{uvw}} & 0 & -\frac{1}{C_{uvw}} & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{1}{T_{inner}} & 0 \\ 0 & \frac{1}{T_{inner}} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$$F = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & \frac{1}{3L_{rst}} \\ \frac{1}{3L_{rst}} & -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, C = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}. \tag{4.48}$$

Computational performance of the outer controller can be increased by the consideration that the inner MPC is ideal. Converter currents can be removed from state vector since the time constant is much lower than the sample time for the outer MPC:

$$x(t) = [i_r(t) \quad i_s(t) \quad v_{C_u}(t) \quad v_{C_v}(t) \quad ]^T. \tag{4.49}$$

Reduced matrices [2]:

$$A = \begin{bmatrix} -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0 \\ 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} \\ -\frac{1}{C_{uvw}} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_{uvw}} & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{C_{uvw}} & 0 \\ 0 & \frac{1}{C_{uvw}} \end{bmatrix},$$

$$F = \begin{bmatrix} -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & \frac{1}{3L_{rst}} \\ \frac{1}{3L_{rst}} & -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}. \quad (4.50)$$

The model converts to the discrete system using zero order hold as with the inner MPC [2].

In order to predict future values in the paper [2] the input vector is modified. Input vector contains difference $\Delta u_k$ instead of input value:

$$\begin{bmatrix} x_{k+1} \\ u_k \end{bmatrix} + \begin{bmatrix} A & B \\ \underbrace{0}_{\hat{A}} & I \end{bmatrix} \begin{bmatrix} x_k \\ \underbrace{u_{k-1}}_{\hat{x}} \end{bmatrix} + \begin{bmatrix} B \\ \underbrace{I}_{\hat{B}} \end{bmatrix} \Delta u_k + \begin{bmatrix} F \\ \underbrace{0}_{\hat{F}} \end{bmatrix} v_k. \quad (4.51)$$

Future values can be calculated by using the expressions below:

$$\underbrace{\begin{bmatrix} x_{k+1} \\ x_{k+2} \\ \vdots \\ x_{k+n} \end{bmatrix}}_{\overrightarrow{x}_k} = \underbrace{\begin{bmatrix} \hat{A} \\ \hat{A}^2 \\ \vdots \\ \hat{A}^n \end{bmatrix}}_{P_x} \hat{x}_k + \underbrace{\begin{bmatrix} \hat{B} & 0 & \cdots \\ \hat{A}\hat{B} & \hat{B} & \cdots \\ \vdots & \vdots & \cdots \\ \hat{A}^{n-1}\hat{B} & \hat{A}^{n-2}\hat{B} & \cdots \end{bmatrix}}_{H_x} \underbrace{\begin{bmatrix} \Delta u_k \\ \Delta u_{k-1} \\ \vdots \\ \Delta u_{k+n-1} \end{bmatrix}}_{\overrightarrow{\Delta u}_{k-1}} +$$

$$\underbrace{\begin{bmatrix} \hat{B} & 0 & \cdots \\ \hat{A}\hat{F} & \hat{F} & \cdots \\ \vdots & \vdots & \cdots \\ \hat{A}^{n-1}\hat{F} & \hat{A}^{n-2}\hat{F} & \cdots \end{bmatrix}}_{Q_x} \underbrace{\begin{bmatrix} v_k \\ v_{k-1} \\ \vdots \\ v_{k+n-1} \end{bmatrix}}_{\overrightarrow{v}_{k-1}} \quad (4.52)$$

Future variables can be expressed by using matrix C as:

$$\underbrace{\begin{bmatrix} y_{k+1} \\ y_{k+2} \\ \vdots \\ y_{k+n} \end{bmatrix}}_{\underset{\rightarrow k}{y}} = \underbrace{\begin{bmatrix} \hat{C}\hat{A} \\ \hat{C}\hat{A}^2 \\ \vdots \\ \hat{C}\hat{A}^n \end{bmatrix}}_{P} \hat{x}_k + \underbrace{\begin{bmatrix} \hat{C}\hat{B} & 0 & \cdots \\ \hat{C}\hat{A}\hat{B} & \hat{C}\hat{B} & \cdots \\ \vdots & \vdots & \cdots \\ \hat{C}\hat{A}^{n-1}\hat{B} & \hat{C}\hat{A}^{n-2}\hat{B} & \cdots \end{bmatrix}}_{H_x} \underbrace{\begin{bmatrix} \Delta u_k \\ \Delta u_{k-1} \\ \vdots \\ \Delta u_{k+n-1} \end{bmatrix}}_{\underset{\rightarrow k-1}{\Delta u}} +$$

$$\underbrace{\begin{bmatrix} \hat{C}\hat{B} & 0 & \cdots \\ \hat{C}\hat{A}\hat{F} & \hat{C}\hat{F} & \cdots \\ \vdots & \vdots & \cdots \\ \hat{C}\hat{A}^{n-1}\hat{F} & \hat{C}\hat{A}^{n-2}\hat{F} & \cdots \end{bmatrix}}_{Q} \underbrace{\begin{bmatrix} v_k \\ v_{k-1} \\ \vdots \\ v_{k+n-1} \end{bmatrix}}_{\underset{\rightarrow k-1}{v}}, \tag{4.53}$$

where $\hat{C}$ is C, but with two additional zero columns to multiply matrices.

Therefore cost function can be written as an error between the reference and predicted grid currents:

$$J = \left\| \underset{\rightarrow k}{i^*_{rst}} - \underset{\rightarrow k}{y} \right\|_2^2 = \left\| \underset{\rightarrow k}{i^*_{rst}} - P\hat{x}_k - H\Delta \underset{\rightarrow k-1}{u} - Q \underset{\rightarrow k-1}{v} \right\|_2^2, \tag{4.54}$$

where future variables were replaced by formula (4.53), moreover as shown in [2], this function can be expressed as:

$$J = \Delta \underset{\rightarrow k-1}{u}^T H^T H \Delta \underset{\rightarrow k-1}{u} + 2\Delta \underset{\rightarrow k-1}{u}^T H^T (P\hat{x}_k + Q \underset{\rightarrow k-1}{v} - \underset{\rightarrow k}{i^*_{rst}}) + \left\| \underset{\rightarrow k}{i^*_{rst}} - P\hat{x}_k - Q \underset{\rightarrow k-1}{v} \right\|_2^2. \tag{4.55}$$

The last term can be eliminated from the optimization because it does not include the input vector. Then, using quadratic programming, minimization problem can be written as:

$$\min_{\Delta \underset{\rightarrow k-1}{u}} \frac{1}{2} \Delta \underset{\rightarrow k-1}{u}^T H^T H \Delta \underset{\rightarrow k-1}{u} + \Delta \underset{\rightarrow k-1}{u}^T H^T (P\hat{x}_k + Q \underset{\rightarrow k-1}{v} - \underset{\rightarrow k}{i^*_{rst}})$$

$$s.t. \quad \Delta u_{lb} \le \Delta \underset{\rightarrow k-1}{u} \le \Delta u_{ub} \tag{4.56}$$

$$x_{lb} \le \underset{\rightarrow k}{x} \le x_{ub}.$$

The first upper and lower bound limits determine step limits for the input vector. The second upper and lower bound limits set the constraints of the state variables and prevent the currents and voltages overlimitations.

The model of VSC control system, which is based on MPC algorithm, is developed in Chapter 4.2. The Simulink implementation of this control system is represented in Appendix A.

## 4.3 Voltage oriented control algorithm

Voltage oriented control (VOC) is the second scheme that controls grid-connected converters. This algorithm is based on transformation between the abc stationary reference frame and dq synchronous frame. Active and reactive power injected into the grid can be controlled separately by VOC.

Figure 4.4 shows VOC structure and its main components. PLL (Phase Locked Loop) estimates and filters the angle of the source and the instantaneous amplitude of the equivalent phase of a three-phase system.

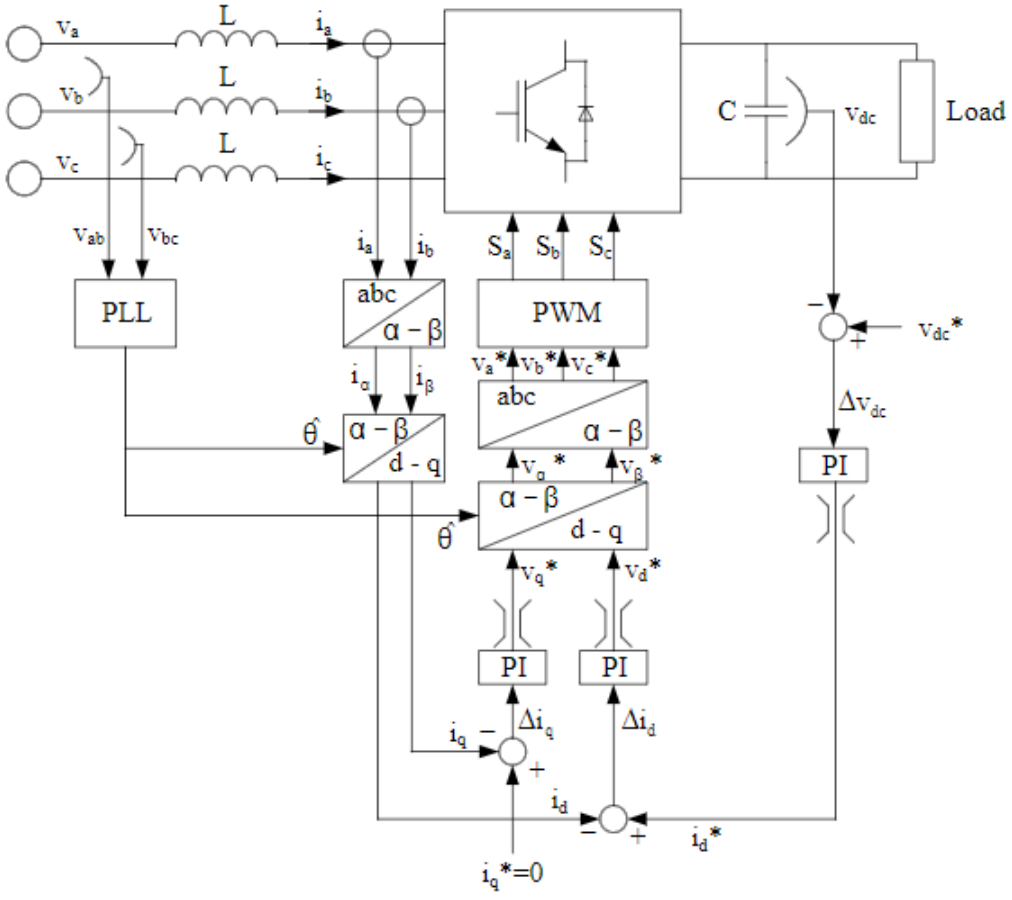


*Figure 4.4 - Voltage oriented control structure [33]*

Voltage reference angle $\theta$ and synchronous references $dq$ can be expressed by Park transformation, stationary references $\alpha\beta$ – by Clarke transformation. The vector diagram with these references and angle between them is shown in Figure 4.5.

A three-phase system should be converted into an equivalent stationary two-phase system. This system in its turn should be converted into a rotating two-phase system.

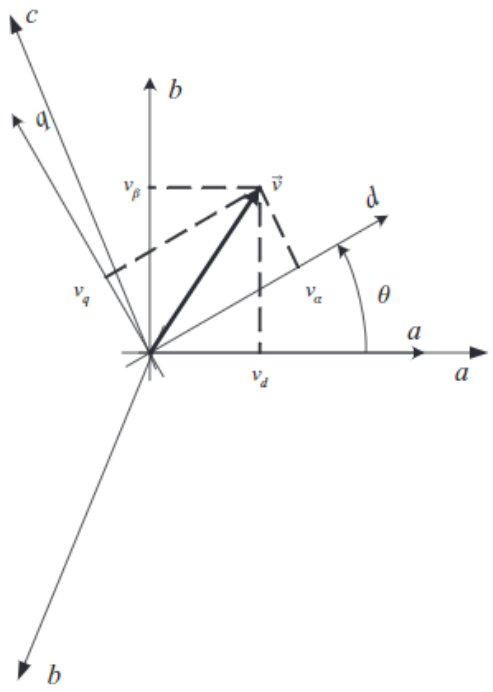


*Figure 4.5 - Stationary αβ frame and rotating dq frame [34]*

## 4.3.1 Control system

### 4.3.1.1 Clarke transformation

Clark transformation converts the three-phase $abc$ frame into a vector with two variables $\alpha\beta$ by adding all three phase vectors.

Three-phase voltages and currents can be defined as:

$$v_a = V\cos(\omega t),$$

$$v_b = V\cos\left(\omega t + \frac{2\pi}{3}\right),$$

$$v_c = V\cos\left(\omega t - \frac{2\pi}{3}\right), \tag{4.57}$$

$$i_a = I\cos(\omega t - \varphi),$$

$$i_b = I\cos\left(\omega t + \frac{2\pi}{3} - \varphi\right),$$

$$i_c = I\cos\left(wt - \frac{2\pi}{3} - \varphi\right),$$

where $w$ – angular frequency, $\varphi$ – the phase angle, V and I – amplitudes of voltage and currents.

Figure 4.5 shows the principle of Clarke transformation. The expression for converting an abc- system into an $\alpha\beta$-system:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}. \tag{4.58}$$

The two-phase to three-phase by inverse Clarke transformation:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}. \tag{4.59}$$

#### 4.3.1.2 Park transformation

The Park transformation is used to convert a stationary frame into a rotating frame, that is defined by direct and quadrature axes that are perpendicular to each other (Figure 4.5). The arbitrary position between a-axis and d-axis is given by angle $\theta$ .The dq-axis frame rotates in space with speed $w$, which is $w = d\theta/dt$ [35]. Park transformation converts AC values into DC values, which can be controlled by a PI controller.

Transformation $\alpha\beta/dq$ can be expressed as:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}. \tag{4.60}$$

The inverse transformation $dq/\alpha\beta$:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} x_d \\ x_q \end{bmatrix}. \tag{4.61}$$

#### 4.3.1.3 Phase locked loop

In a VOC algorithm phase locked loop is used to calculate the voltage reference angle. The voltage reference angle is used in Park and inverse Park transformations, and is also a necessary part of the algorithm.

The block diagram of PLL is shown in Figure 4.6:

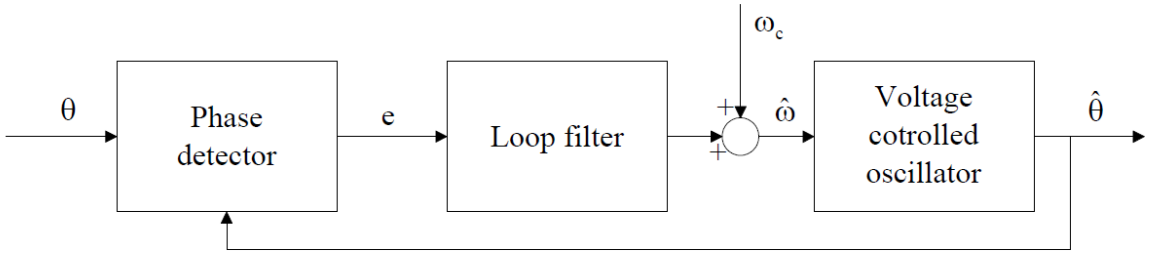


*Figure 4.6 - Block diagram of phase locked loop [33]*

The phase detector compares the estimated reference angle $\hat{\theta}$ with real reference angle $\theta$ and generates the error. The loop filter filtrates disturbances on the error $e$ and can be represented as PI controller:

$$v_{lf} = \left(k_p + \frac{1}{T_i s}\right) e. \tag{4.62}$$

The output of the loop filter goes through adder as well as the angular velocity $w_c$, which depends on the nominal grid frequency ( $w = 2\pi f$). The output of the adder is the estimated angular grid velocity $\hat{w}$.

The estimated reference angle can be calculated as:

$$\hat{\theta}(\mathrm{t}) = \int \hat{w}(\mathrm{t})\mathrm{dt}. \tag{4.63}$$

#### 4.3.1.4 Voltage and current controllers

As it is shown in Figure 4.4, there is a coupling between $d$ and $q$ axes. This coupling can be expressed as [33]:

$$v_{grid,d} = Ri_d + L\frac{di_d}{dt} - wLi_q + v_{conv,d}, \tag{4.64}$$

$$v_{grid,q} = Ri_q + L\frac{di_q}{dt} + wLi_d + v_{conv,q}. \tag{4.65}$$

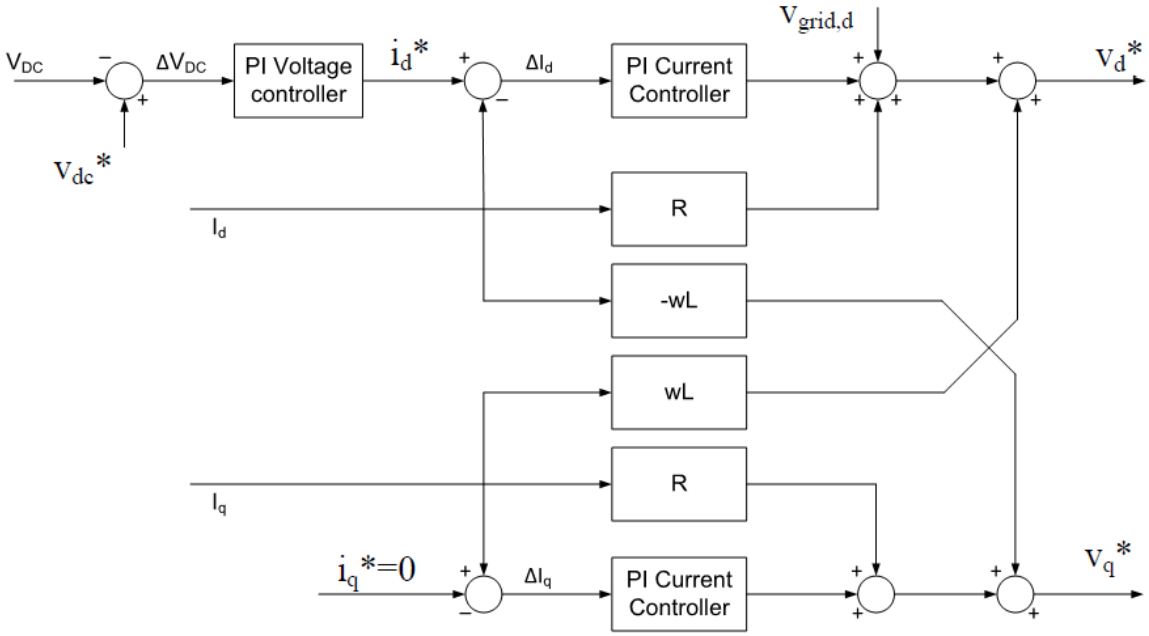


*Figure 4.7 - Decoupled current control [33]*

The decoupling structure is added to the current control loops (Figure 4.7). The current control and decoupling along with its references keep unity power factor and $i_q = 0, v_{grid,q} = 0$. After these assumptions [7]:

$$v_d^* = Ri_d + wLi_q + v_{grid,d} + \Delta v_d, \tag{4.66}$$

$$v_q^* = Ri_q - wLi_d + \Delta v_q. \tag{4.67}$$

### 4.3.2 Space vector modulation

SVM is based on space vector representation (Figure 4.8(a)). A two-level three-phase converter has eight possible switches: six of them are active, two – passive (zero switching states).

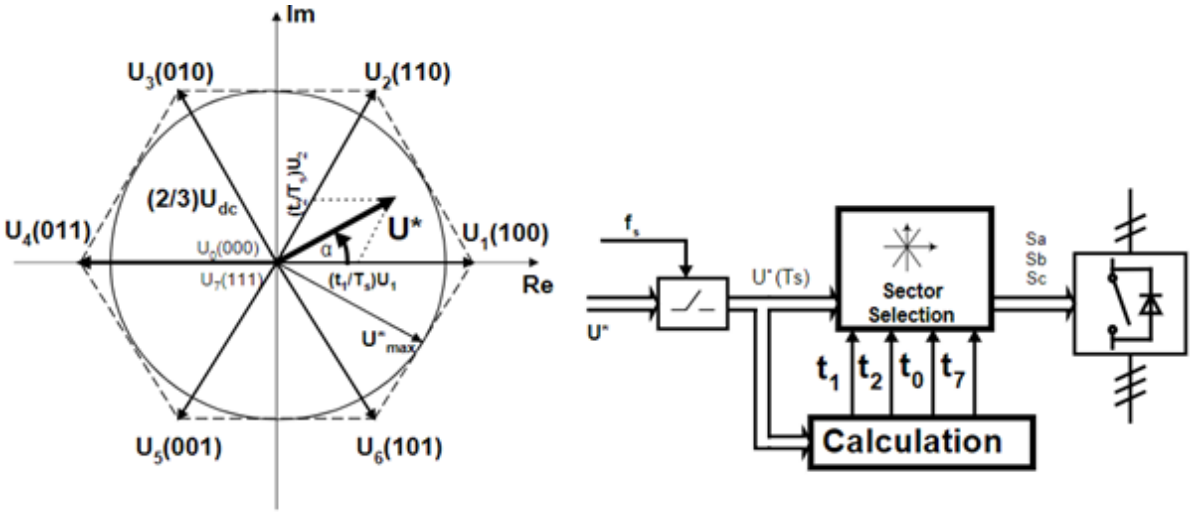


*Figure 4.8 - a) Space vector representation of a three phase converter, b) Block scheme of SVM [8]*

Reference vector $U^*$ can be obtained by combining two neighboring vectors. Figure 4.8 (a) shows that vector $U^*$ is implemented by different sequence $U_1$ and $U_2$. Vectors $U_0$ and $U_7$ reduce modulation index M.

Figure 4.8 (b) points out that reference vector $U^*$ is sampled with fixed frequency $f_s = 1/T_s$. The sampled $U^*(T_s)$ is being used to calculate $t_1, t_2, t_0, t_7$ . Time variable calculations for the first sector sector is being shown in Figure 4.8 (b):

$$t_1 = \frac{2\sqrt{3}}{\pi} M T_s \sin(\frac{\pi}{3} - \alpha), \tag{4.68}$$

$$t_2 = \frac{2\sqrt{3}}{\pi} M T_s \sin \alpha. \tag{4.69}$$

The same trigonometrical equations can be used for all sectors.

The sum of $t_1$ and $t_2$ should be less than $T_s$, and the sum of $t_0$ and $t_7$ is the rest of the sampling time [8]:

$$T_s - t_1 - t_2 = t_0 + t_7. \tag{4.70}$$

The model of VSC control system, which is based on VOC and SPM algorithms, is developed in Chapter 4.3. The Simulink implementation of this control system is represented in Appendix B.

# 5. Simulation results

*This chapter represents the simulation results for MPC and VOC algorithms with the different switching frequency of transistors. It also compares the obtained results.*

## 5.1 Simulation models overview

Simulations are performed using MATLAB/Simulink R2017b. The converter model is described in Chapter 4.1, the MPC and VOC algorithms are derived in Chapter 4.2 and 4.3 respectively.

Two different control model algorithms are being used in this project, and one converter with LCL filter.

The converter is tested with the following parameters:

*Table 5.1 - Converter parameters*

| **Parameter** | **MPC** | **VOC** |
|---|---|---|
| **Converter side resistors $R_a = R_b = R_c$ (mOhm)** | 20 | 20 |
| **Converter side inductors $L_a = L_b = L_c$ (mH)** | 1 | 1 |
| **Grid side resistors $R_r = R_s = R_t$ (mOhm)** | 50 | 50 |
| **Grid side inductors $L_r = L_s = L_t$ (mH)** | 5 | 5 |
| **Damping resistors $R_u = R_v = R_w$ (mOhm)** | 0 | 10 |
| **Filter capacitors $C_u = C_v = C_w$ ($\mu F$)** | 10 | 10 |
| **DC-link load resistor $R_{DC}$ (Ohm)** | 17000 | 17000 |
| **DC-link capacitor $C_{DC}$ ($mF$)** | 2200 | 2200 |
| **Constant K** | 0 | 0 |
| **Initial voltage $V_{DC}$ (V)** | 400 | 400 |

There are few differences between VOC and MPC algorithms. Step changes in VOC algorithm are introduced in the dq current references – $i_d$ and $i_q$, in the MPC algorithm – by the active and reactive power references.

The VOC system has the modulator. Thus, the switching frequency can be set manually. But the MPC algorithm has no modulator, and switching frequency is calculated based on the number of transistor switches during the simulation [2]:

$$f_{SW} = \frac{1}{3}\sum_{i=1}^{3}\left(\frac{1}{T_{sim}}\sum_{k=1}^{N_{sim}}(d_i(k) - d_i(k-1)),\right), \qquad i \in \{1,2,3\}, \qquad (5.1)$$

where $N_{sim}$ and $T_{sim}$ are the total number of simulation steps and the simulation time respectively.

Total harmonic distortion (THD) is defined using the FFT analysis tool in the SimPowerSystem toolbox.

The PLL was removed to eliminate a source of disturbance and focus on the performance for the MPC and VOC algorithms. This gives the same conditions for comparison. In this case the reference angle $\hat{\theta}$ is extracted from the generation of the grid voltage and used without any kind of noise and disturbances. The reference angle is $\hat{\theta} = \theta - \frac{\pi}{2}$. There is implemented $90^0$ phase shift, so that $V_q$ is zero, thus reactive and active power is set by $V_d$ only that it is easier to define.

Step changes in the MPC model are injected by reactive and active power directly, whereas in the VOC model reactive and active power is set by $i_d$ and $i_q$ respectively.

Rated voltage and current are given. Thus, apparent power can be calculated as:

$$S = VI = 230\ V * \sqrt{3} * 16\ A = 6400\ VA. \tag{5.2}$$

Hence, active and reactive power can be obtained

$$P = 0.9|S| \ \rightarrow P = 5800\ W; \quad Q = \sqrt{S^2 - Q^2} = 2705.5\ VAr. \tag{5.3}$$

Currents are expressed from instantaneous active and reactive power in the dq-frame:

$$P = V_d i_d + V_q i_q. \tag{5.4}$$

$$Q = V_q i_d - V_d i_q. \tag{5.5}$$

Reference currents for the VOC model can be found using (5.2) and (5.3). $V_d$ and $V_q$ are obtained from (4.57), (4.58) and (4.60):

$$v_d = \frac{2}{3}\left(v_a * \cos\theta + v_b * \cos(\theta - \frac{2\pi}{3}\right) + v_c * \cos(\theta - \frac{4\pi}{3})), \tag{5.6}$$

$$v_q = \frac{2}{3}(-v_a * \sin\theta - v_b * \sin(\theta - \frac{2\pi}{3}) - v_c * \sin(\theta - \frac{4\pi}{3})). \tag{5.7}$$

Assuming that $\theta = 0$ at $t = 0$, knowing that the grid voltage is 230 V:

$$v_d = \frac{2}{3}\left(230\ V * 1 + \frac{1}{2} * 230\ V * \frac{1}{2} + \frac{1}{2} * 230\ V * \frac{1}{2}\right) = 230\ V, \tag{5.8}$$

$$v_q = \frac{2}{3}\left(230\ V * 0 - \frac{1}{2} * 230\ V * \frac{\sqrt{3}}{2} - \frac{1}{2} * 230\ V * \frac{\sqrt{3}}{2}\right) = 0. \tag{5.9}$$

From (5.4) and (5.5) currents can be expressed as:

$$i_d^{ref} = \frac{P}{v_d} = \frac{5800\,W}{230\,V} = 25.22\,A;\; i_q^{ref} = -\frac{Q}{v_d} = \frac{2705.5\,VAr}{230\,V} = -11.76\,A. \quad (5.10)$$

These values are reference input values for the VOC model.

It is assumed that dead-time is perfectly compensated in both models. In this case no dead-time is included in the simulation.

## 5.2 Case 1 – equal switching frequency

First, the models are compared with equal parameters. The best choice is the comparison of two systems with initial values and same frequency.

There are a few limitations in this project, which are the initial values:

- The voltage of the system ≤ 400 V and rated current ≤ 16 $A$;
- Power factor is greater than 0.9, $cos\phi \geq 0.9$;
- Frequencies are the same in both models in this case.

Since the switching frequency in the MPC algorithm is calculated during the simulation, this calculated frequency from the MPC algorithm is used in the VOC algorithm after that.

### 5.2.1 Simulation and results for the MPC algorithm

Step changes in the MPC model are injected by the reactive and active power that were calculated in (5.3).

Figure 5.1 shows the result of the MPC model simulation. Simulated variables (black lines) and references (yellow lines) are very similar. The switching frequency is 23 kHz. The converter is turned on at 0.05 second.

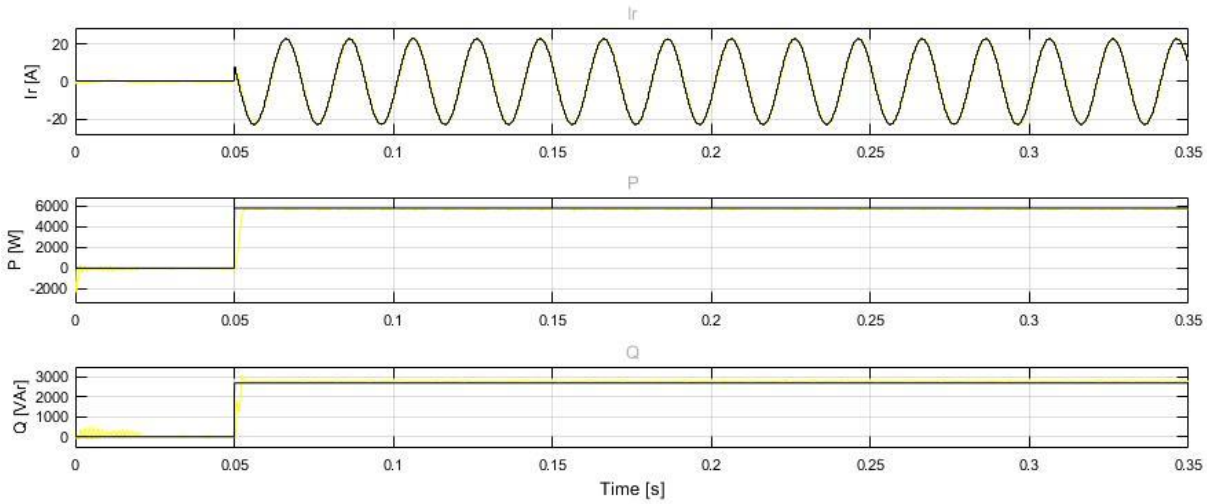


*Figure 5.1 - Simulation of MPC algorithm with rated values (reference values are black lines, simulated values – yellow lines)*

From Figure 5.1 it can be seen that the rated RMS current is 16 A power factor is greater than 0.9. It meets the requirements which are described in Chapter 2.2.1.

As was said above, THD is calculated and draw by Simulink. The result is shown in Figure 5.2:

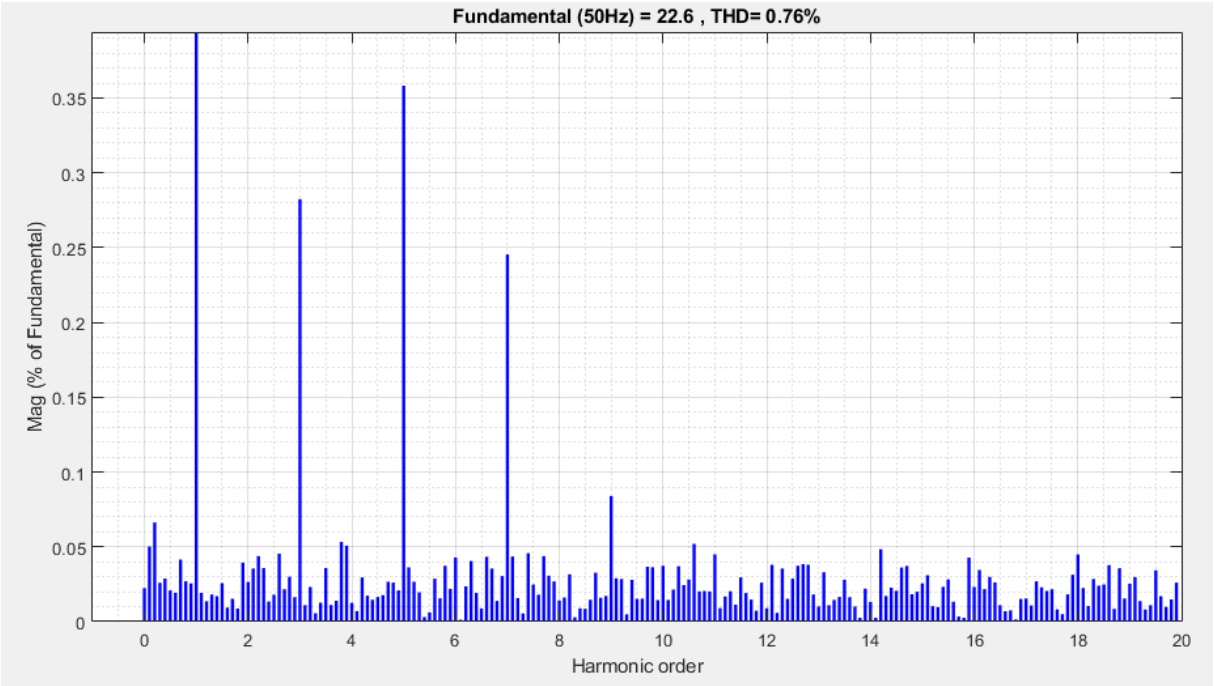


*Figure 5.2 - Grid current spectrum of MPC algorithm at rated initial values*

The figure above shows the total and individual harmonic distortion. The THD is very low in this case, much lower than is required according to the requirements that were described in Chapter 2.1.1. Individual harmonic distortion meets the requirements from Table 2.3.

Power losses requirements are not specified, but it should be as less as possible. Power losses are calculated in Chapter 6.

### 5.2.2 Simulation and results for the VOC algorithm

The frequency is set manually in the VOC algorithm, and it was calculated in the previous chapter (23 kHz).

Figure 5.3 shows the result of VOC model simulation at switching frequency $f_{sw} = 23\ kHz$: grid current $I_r \approx 16\ A$, active power $P = 5803\ W$, reactive power $Q = 2702\ VAr$.

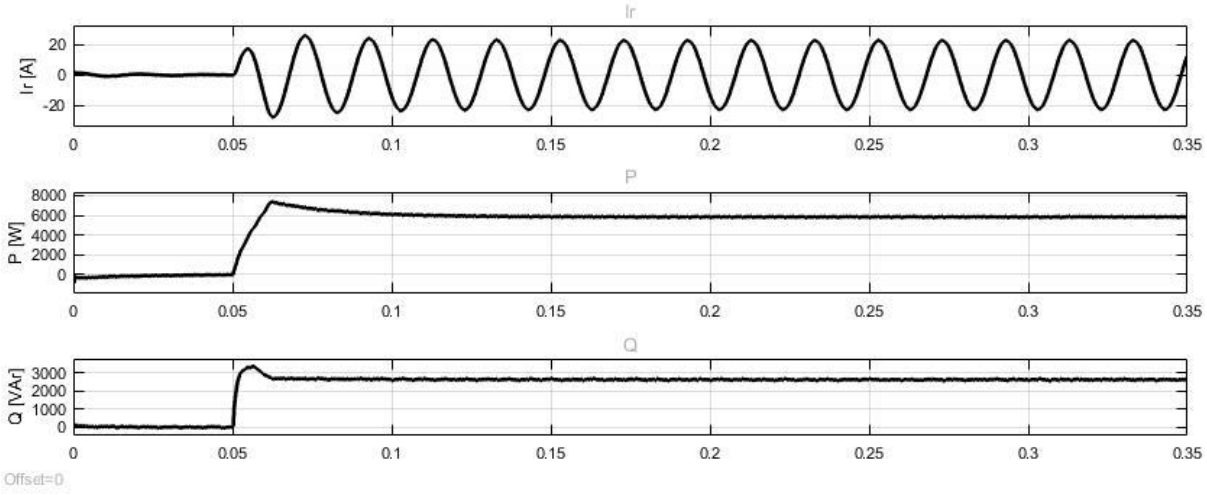


*Figure 5.3 - Simulation of VOC algorithm with rated values at 23 kHz modulator switching frequency*

The figure above shows that power factor and current satisfy requirements.

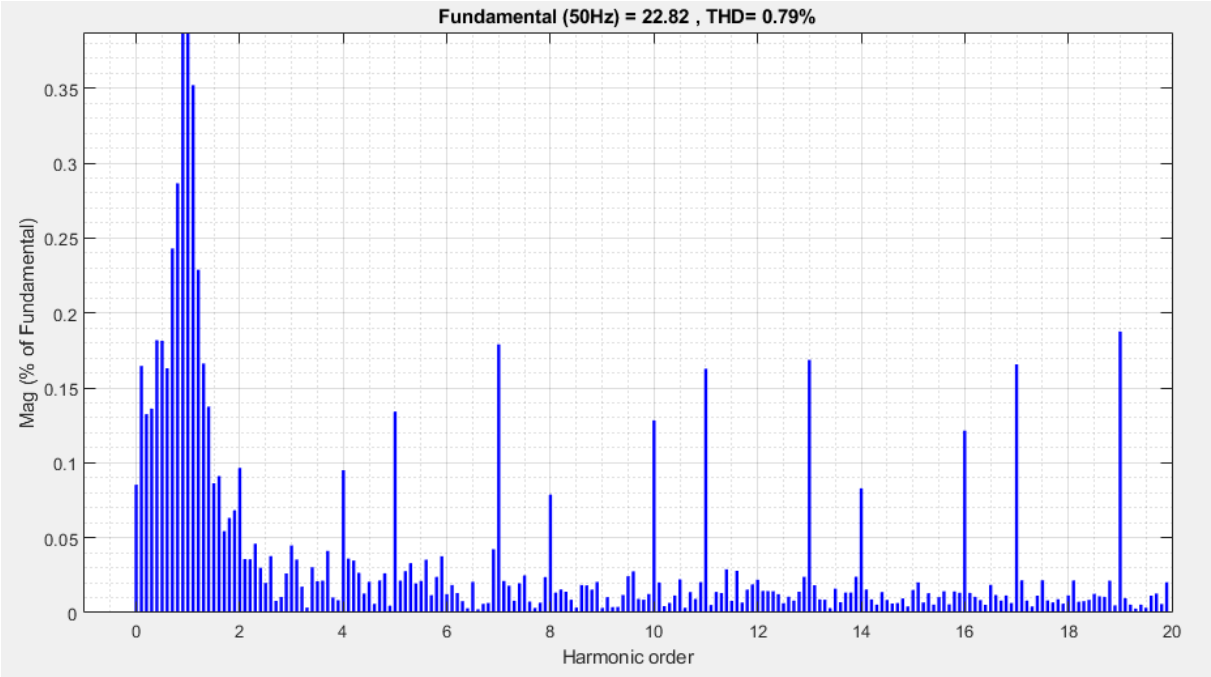


*Figure 5.4 - Grid current spectrum of VOC algorithm with rated values at 23 kHz modulator switching frequency*

The grid current spectrum of the algorithm shows the total and individual harmonic distortion on Figure 5.4. These total and individual harmonic distortions meet the requirements which are set forth in Table 2.3.

Thus, the VOC algorithm can be used at switching frequency 23 kHz because it does meet the requirements according to the specifications being used in the given component values, simulation parameters and controller tuning.

Since the models with high frequency have higher energy losses, it is better to evaluate the VOC model with lower frequency, i.e., 5 kHz.

## 5.3 Case 2 - the VOC algorithm at 5 kHz switching frequency

The new chosen switching frequency has been taken from [7] where the algorithm is very stable at a 5 kHz switching frequency. The lower frequency will also lead to the reduction of the switching losses in transistors.

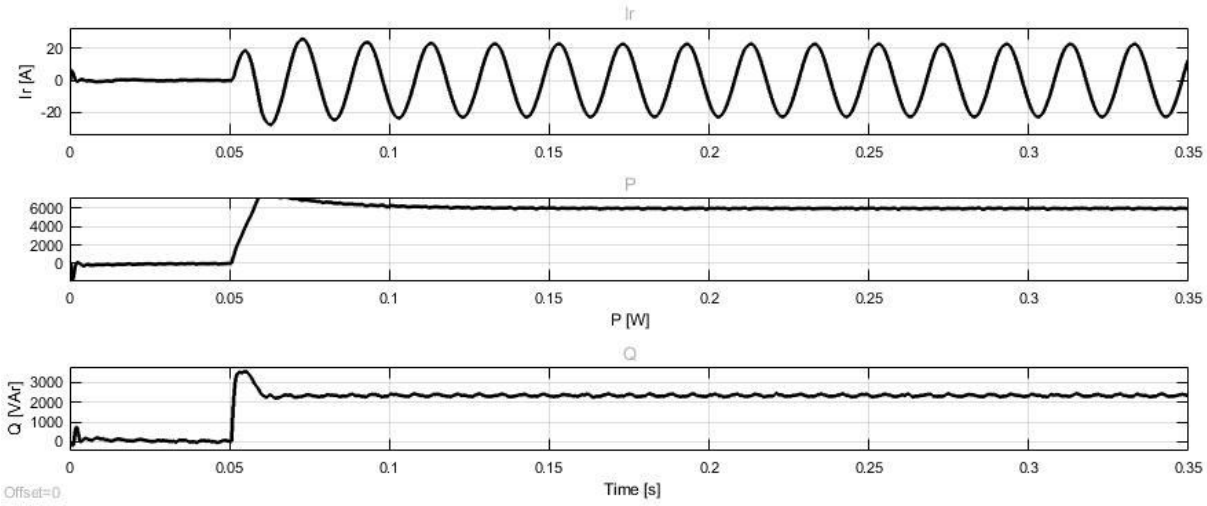


*Figure 5.5 - Simulation of VOC algorithm with rated values at 5 kHz switching frequency*

Figure 5.5 shows the result of VOC model simulation at switching frequency of space vector modulator $f_{sw} = 5\ kHz$: grid current $I_r \approx 16\ A$, active power $P = 5800\ W$, reactive power $Q = 2703\ VAr$. These results satisfy the power factor requirements.

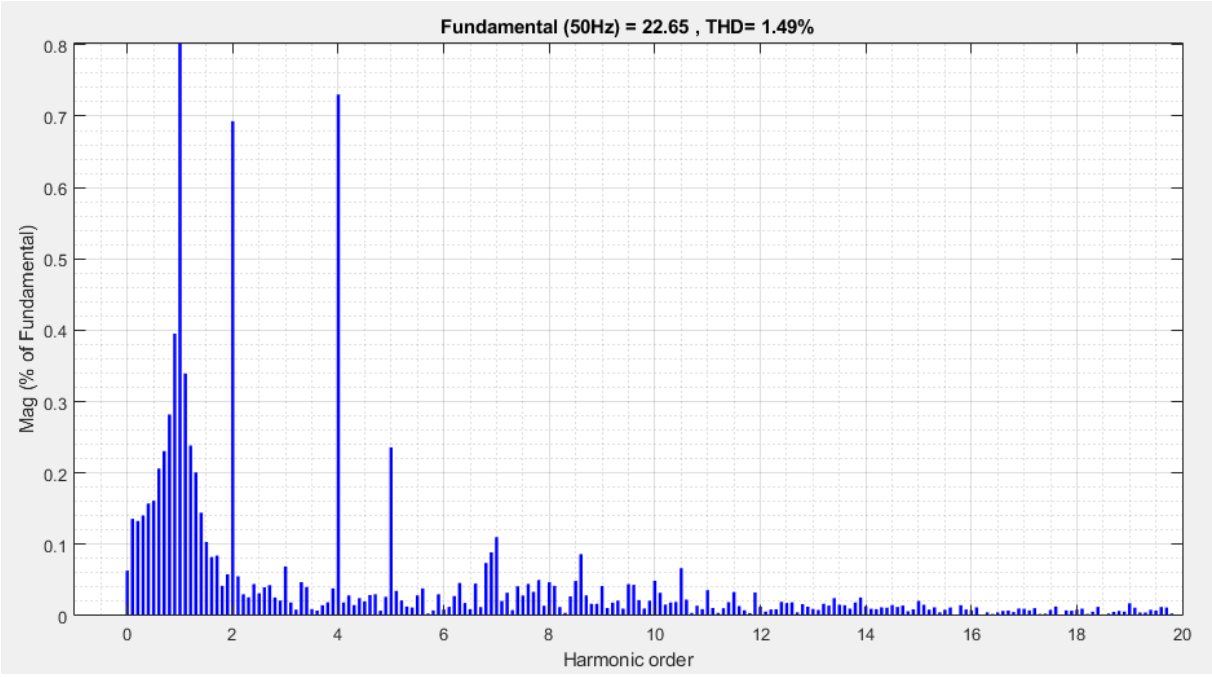


*Figure 5.6 - Grid current spectrum of VOC algorithm with rated values at 5 kHz switching frequency*

The grid current spectrum of the algorithm shows the total and individual harmonic distortion on Figure 5.6. All requirements for Table 2.3 are satisfied. The total harmonic distortion is higher than at 23 kHz switching frequency. This was expected and consistent with the theory – higher frequency makes the signal more smooth.

## 5.4 Comparison of total and individual harmonics of the two algorithms

The results from 5.2.1 and 5.3 can be summarized in one comparative table.

*Table 5.2 - Comparative table of VOC and MPC harmonic distortion*

| Parameter | MPC (23 kHz) | VOC (23 kHz) | VOC (5 kHz) |
|---|---|---|---|
| **THD** | 0.76% | 0.79% | 1.49% |
| **2nd** | 0.04% | 0.1% | 0.7% |
| **3rd** | 0.28% | 0.05% | 0.08% |
| **4th** | 0.05% | 0.1% | 0.74% |
| **5th** | 0.36% | 0.13% | 0.24% |
| **6th** | 0.04% | 0.04% | 0.03% |
| **7th** | 0.24% | 0.18% | 0.11% |
| **8th** | 0.02% | 0.08% | 0.04% |
| **9th** | 0.08% | 0.01% | 0.04% |
| **10th** | 0.04% | 0.13% | 0.05% |
| **11th** | 0.05% | 0.16% | 0.04% |
| **12th** | 0.01% | 0.02% | 0.01% |
| **13th** | 0.03% | 0.17% | 0.01% |
| **14th** | 0.01% | 0.08% | 0.01% |
| **15th** | 0.03% | 0.01% | 0.02% |
| **16th** | 0.02% | 0.12% | 0.01% |
| **17th** | 0.02% | 0.17% | 0.01% |
| **18th** | 0.04% | 0.01% | 0.01% |
| **19th** | 0.03% | 0.19% | 0.02% |
| **20th** | 0.03% | 0.02% | 0.01% |

Chapter 2 describes three types of requirements that are applied to the voltage source converters: power factor, total and individual harmonic distortion and power losses.

The power factor satisfies the requirements and is equal in both algorithms. Total and individual harmonic distortion are also meet requirements. Table 5.2 shows that THD of 5 kHz switching frequency is higher than THD of 23 kHz (in both models). The MPC algorithm shows lower amplitudes than VOC for higher harmonics (10th and above). All total and individual harmonic distortion meet the requirements. Power losses will be discussed in Chapter 6.

# 6. Applying different types of transistors

*This chapter represents the calculated power losses of each type of applied transistors. These results are compared with each other and discussed.*

## 6.1 Transistor selection conditions

Transistors were selected with 20% excess of parameters for safety reasons. The selection parameters are DC-link voltage and peak grid current. Thus, minimum collector-emitter (or drain-source) voltage is 480 V and continuous collector (drain) current – 27 A.

The same transistor of each type is applied to both algorithms. In this case the power losses are complimentary.

According to Figure 4.8, only two legs in the converter will switch at the moment using space vector modulation, therefore the average switching frequency of each transistor in the VOC algorithm is lower than the modulator switching frequency.

Average switching frequency for each leg can be found using (5.1) and a simulation model. Thus, it was obtained that the transistors switching frequency is 3.5 kHz for the VOC model at 5 kHz modulator switching frequency and 16 kHz transistors switching frequency for the VOC model at 23 kHz modulator switching frequency.

Chapter 2 (formulas (2.15) and (2.18)) shows that the power conduction losses are calculated using duty cycle. The duty cycle can be found as [36]:

$$D = \frac{V_o}{V_{DC}}, \tag{6.1}$$

where D – duty cycle, $V_{DC}$ – DC-link voltage, $V_o$- output RMS phase voltage.

Output RMS phase voltage is the same for both algorithms. The grid line voltage is 230 V; RMS phase voltage $V_o = \frac{230\,V}{\sqrt{3}} = 132.8\,V$.

Therefore, duty cycle:

$$D = \frac{132.8\,V}{400\,V} = 0.332. \tag{6.2}$$

## 6.2 Silicon transistors

### 6.2.1 Si IGBT

The first chosen IGBT is **IKFW40N60DH3E** [37]. This IGBT meets all the requirements which were described in Chapter 6.1. The potential applications of the IGBT are general purpose drives and servomotors, and can be used in the converter.

IGBT conduction losses can be calculated using (2.15) and the characteristics of the transistor from the datasheet:

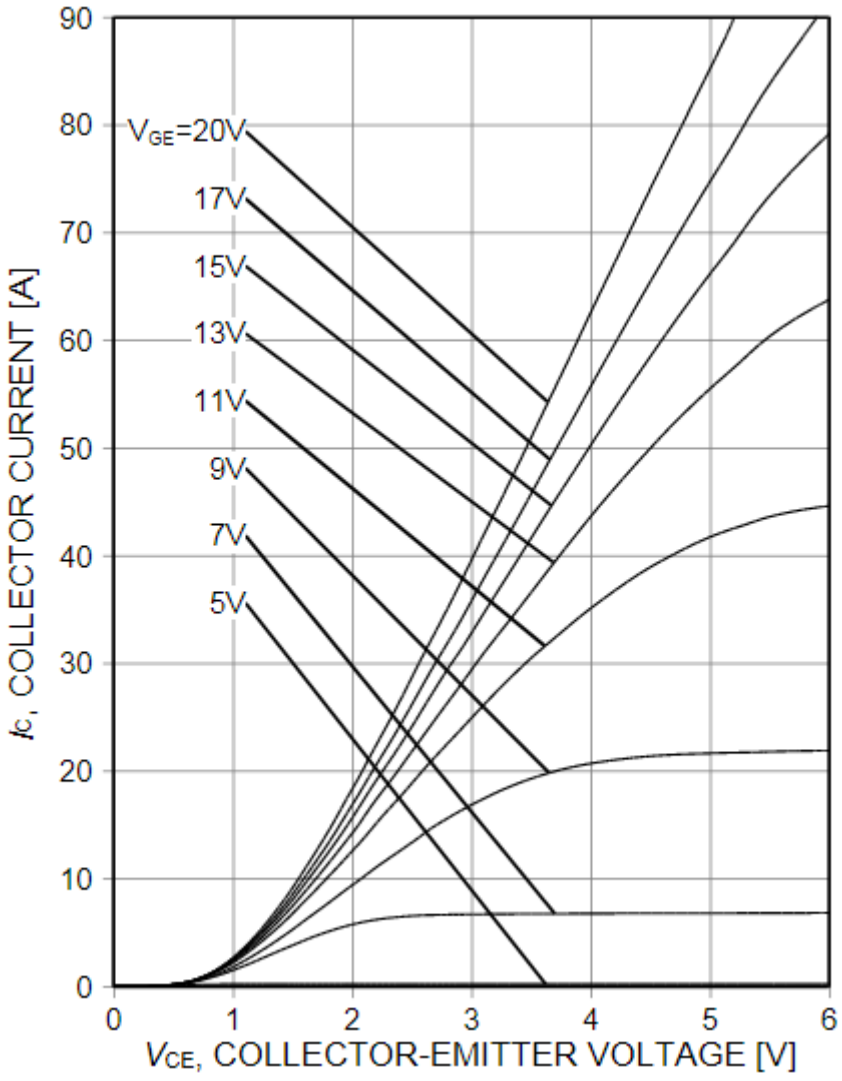


*Figure 6.1 - Typical output characteristics of transistors ($T_j = 175^0$) [37]*

Figure 6.1 shows that under the conditions $T_j = 175^0$ and $V_{GE} = 15$ V, continuous current $I_c = 16\ A$, collector-emitter saturation voltage $V_{CE} = 1.9\ V$.

Thus, IGBT conduction losses can be calculated as:

$$P_{IGBT_{COND}} = D * V_{CE} * I_c = 0.332 * 1.9\,V * 16\,A = 10.09\,W. \quad (6.3)$$

IGBT switching losses can be found using (2.16) and typical switching energy losses of this IGBT:

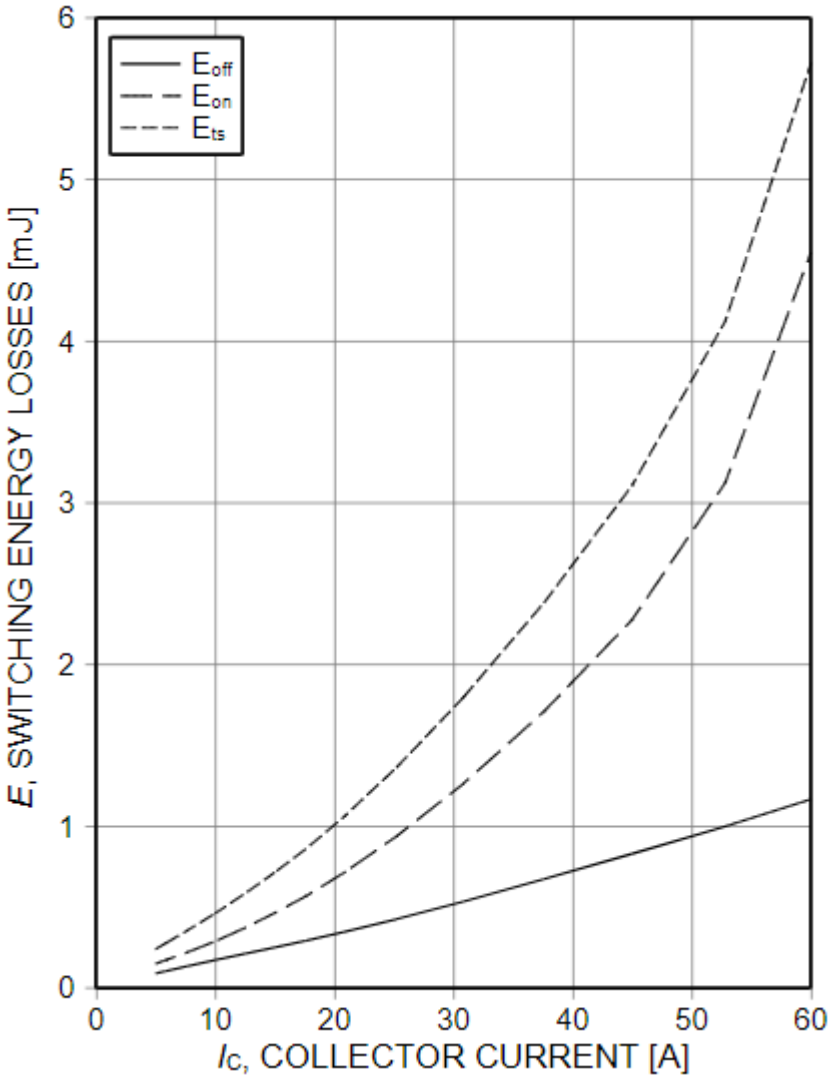


*Figure 6.2 - Typical switching energy losses as a function of collector current [37]*

Figure 6.2 shows that under the conditions $T_j = 175^0$ and $V_{GE} = 15$ V, continuous current $I_c = 16\,A$, switching-on energy losses $E_{SW(on)} = 0.25\,mJ$ and switching-off energy losses $E_{SW(on)} = 0.5\,mJ$.

Therefore, IGBT switching energy losses are at 23 kHz:

$$P_{IGBT_{SW}} = \left(E_{SW_{on}} + E_{SW_{off}}\right) * f_{SW} =$$
$$= (0.25\ + 0.5\ )mJ * 23\,kHz = 17.25\,W, \quad (6.4)$$

for 16 kHz are:

$$P_{IGBT_{SW}} = (0.25 + 0.5)\, mJ * 16\, kHz = 12\, W, \tag{6.5}$$

for 3.5 kHz are:

$$P_{IGBT_{SW}} = (0.25 + 0.5)\, mJ * 3.5\, kHz = 2.625\, W. \tag{6.6}$$

Free-wheeling diode conduction losses are calculated using (2.18) and the figure below from datasheet.

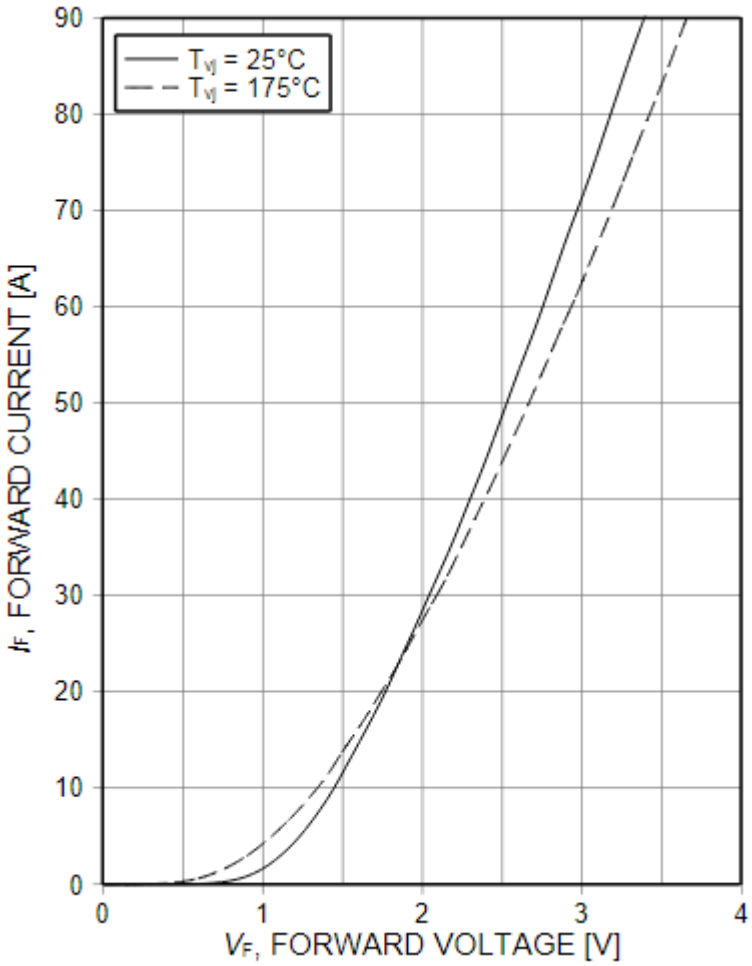


*Figure 6.3 - Typical diode forward current as a function of forward voltage [37]*

Figure 6.3 shows that under the conditions $T_j = 175^0$ and $I_F = 16$ A, forward voltage $V_F = 1.55\, V$. Free wheeling diode conduction losses:

$$P_{COND_{DIODE}} = (1 - D) * I_c * V_F = (1 - 0.332) * 16\, A * 1.55\, V = 16.57\, W. \tag{6.7}$$

Free wheeling diode recovery losses cannot be calculated as described in Chapter 2, because the datasheet has no direct value of reverse recovery switching losses. The formula below can be used instead of it [38]:

$$P_{DIODE_{REC}} = Q_{rr} * V_{DC} * f_{SW}\ , \tag{6.8}$$

where $Q_{rr}$ is reverse recovery charge and can be determined from the figure below.

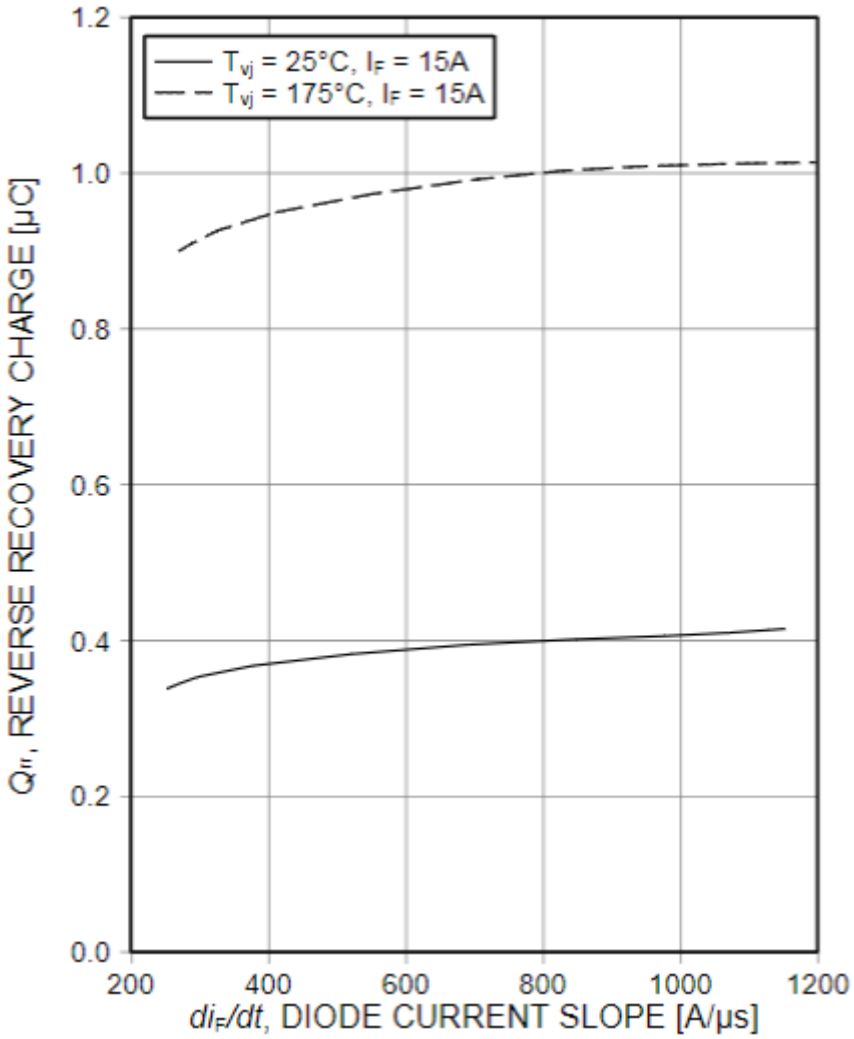


*Figure 6.4 - Typical reverse recovery charge as a function of the diode current slope [37]*

$\frac{di_F}{dt} = 1000\ A$ is defined in datasheet for $I_F = 15\ A$, thus $\frac{di_F}{dt} = 1067\ A$ for $I_F = 16\ A$. In this case, for $T_j = 175^0$, $Q_{rr} = 1.02\ \mu C$.

Therefore, free wheeling diode recovery losses for 23 kHz are:

$$P_{DIODE_{REC}} = 1.02 * 10^{-6}\ C * 400\ V * 23\ kHz = 9.384\ W, \tag{6.9}$$

for 16 kHz are:

$$P_{DIODE_{REC}} = 1.02 * 10^{-6}\ C * 400\ V * 16\ kHz = 6.528\ W, \quad (6.10)$$

for 3.5 kHz are:

$$P_{DIODE_{REC}} = 1.02 * 10^{-6}\ C * 400\ V * 3.5\ kHz = 1.428\ W. \quad (6.11)$$

Thus, total transistor energy losses for 23 kHz according to (2.21) are:

$$P_{transistor} = 10.09\ W + 17.25\ W + 16.57\ W + 9.384\ W = 53.294W, \quad (6.12)$$

for 16 kHz are:

$$P_{transistor} = 10.09\ W + 12\ W + 16.57\ W + 6.528\ W = 45.188\ W, \quad (6.13)$$

for 3.5 kHz are:

$$P_{transistor} = 10.09\ W + 2.625\ W + 16.57\ W + 1.428\ W = 30.713\ W. \quad (6.14)$$

### 6.2.2 Si MOSFET

Silicon MOSFET which meets requirements and was chosen for this project is **SPW52N50C3** [39]. This MOSFET can be applied in high speed power switching and motor drive.

MOSFET losses cannot be calculated as IGBT because of lack of data in the datasheet. Therefore, MOSFET losses are calculated using method and formulas from [40].

MOSFET conduction losses:

$$P_{MOSFET_{cond}} = R_{DS_{on}} * I_D^2 * D, \quad (6.15)$$

where $I_D = 16\ A$- drain current, $R_{DS(on)}$ - drain-source on-state resistance and can be found from the figure below:

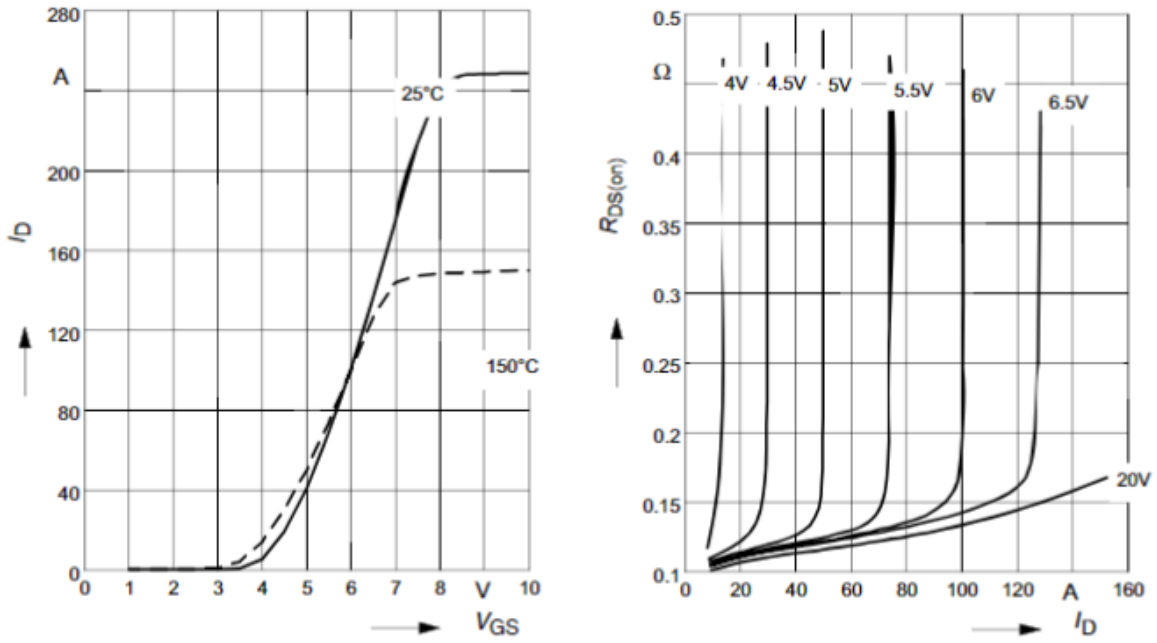


*Figure 6.5 - Typical transfer characteristics ($T_j = 150^0$) [39]*

It is easy to find from Figure 6.5 that $V_{GS} = 4\,V$ $R_{DS(on)} = 0.125\,Ohm$. Thus:

$$P_{MOSFET_{cond}} = 0.125\,Ohm * 16^2 A * 0.332 = 9.89\,W. \quad (6.16)$$

Diode conduction losses:

$$P_{DIODE_{cond}} = V_{SD} * I_F * (1 - D), \quad (6.17)$$

where $I_F = 16\,A$, $V_{SD}$ can be found from the figure below:

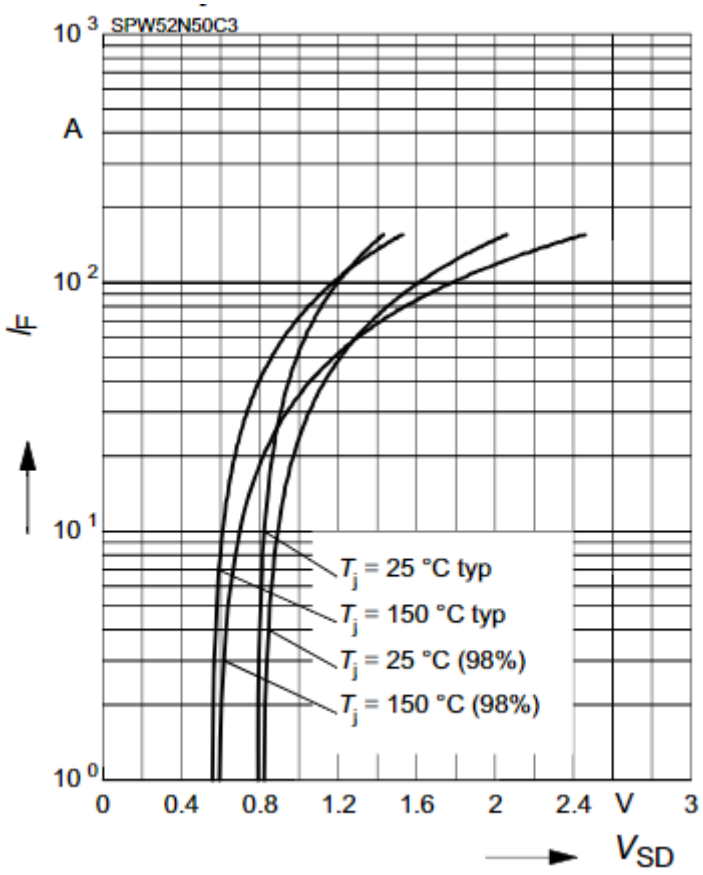


*Figure 6.6 - Forward characteristics of body diode [39]*

Curve $T_j = 150^0$ typ expresses the characteristic $I_F$ as a function of source-drain current. Figure 6.6 shows that $V_{SD} = 0.62\ V$, consequently:

$$P_{DIODE_{cond}} = 0.62\ V * 16\ A * (1 - 0.332) = 6.63\ W. \tag{6.18}$$

MOSFET switching losses are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * V_{DC} * I_{on} * \left(t_{c,on} + t_{c,off}\right) * f_{SW}, \tag{6.19}$$

where

$$t_{c,on} = t_{d,on} + t_r\ , \tag{6.20}$$

$$t_{c,off} = t_{d,off} + t_f\ . \tag{6.21}$$

From datasheet $t_{d,off} = 120\ ns, t_{d,on} = 20\ ns, t_f = 10\ ns, t_r = 30\ ns.$

For 23 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\,V * 16\,A * (50 + 130)ns * 23\,kHz = 13.248\,W, \quad (6.22)$$

for 16 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\,V * 16\,A * (50 + 130)ns * 16\,kHz = 9.216\,W, \quad (6.23)$$

for 3.5 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\,V * 16\,A * (50 + 130)\,ns * 3.5\,kHz = 2.016\,W. \quad (6.24)$$

Diode recovery losses can be calculated with (6.7), data is taken from the datasheet $Q_{rr} = 20\,\mu C, V_{DC} = 400\,V$.

Diode recovery losses for 23 kHz are:

$$P_{DIODE_{rec}} = 20 * \mu C * 400\,V * 23\,kHz = 184\,W, \quad (6.25)$$

for 16 kHz are:

$$P_{DIODE_{rec}} = 20 * \mu C * 400\,V * 16kHz = 128\,W, \quad (6.26)$$

for 3.5 kHz are:

$$P_{DIODE_{rec}} = 20 * \mu C * 400\,V * 3.5\,kHz = 28\,W. \quad (6.27)$$

Thus, the total transistor energy losses for 23 kHz according to (2.21) are:

$$P_{\text{transistor}} = 9.89\,W + 6.63\,W + 13.248\,W + 184\,W = 213.768\,W, \quad (6.28)$$

for 16 kHz are:

$$P_{\text{transistor}} = 9.89\,W + 6.63\,W + 9.216\,W + 128\,W = 153.736\,W, \quad (6.29)$$

for 3.5 kHz are:

$$P_{\text{transistor}} = 9.89\,W + 6.63\,W + 2.016\,W + 28\,W = 46.536\,W. \quad (6.30)$$

Therefore, the total losses in silicon MOSFET are higher than in silicon IGBT. It happens because of a parasitic body diode, which loses 89.2% of the energy at 23 kHz, 87.6% - at 16 kHz and 74.4% - at 3.5 kHz. Also, MOSFET was chosen with high reverse recovery charge value. But the main consequence that can be expressed – is that the VOC algorithm at 3.5 kHz has less losses with both types of silicon transistors.

## 6.3 Silicon carbide transistors

### 6.3.1 SiC IGBT

Since pure SiC IGBT are not available on the market, the Silicon IGBT with SiC Schottky diode which was chosen is **GA35XCP12-247 [41]**. This is IGBT for 5-40 kHz switching, and can be applied in solar inverters, aerospace actuators, etc.
IGBT conduction losses can be calculated using (2.15) and the characteristics of the transistor from the datasheet:

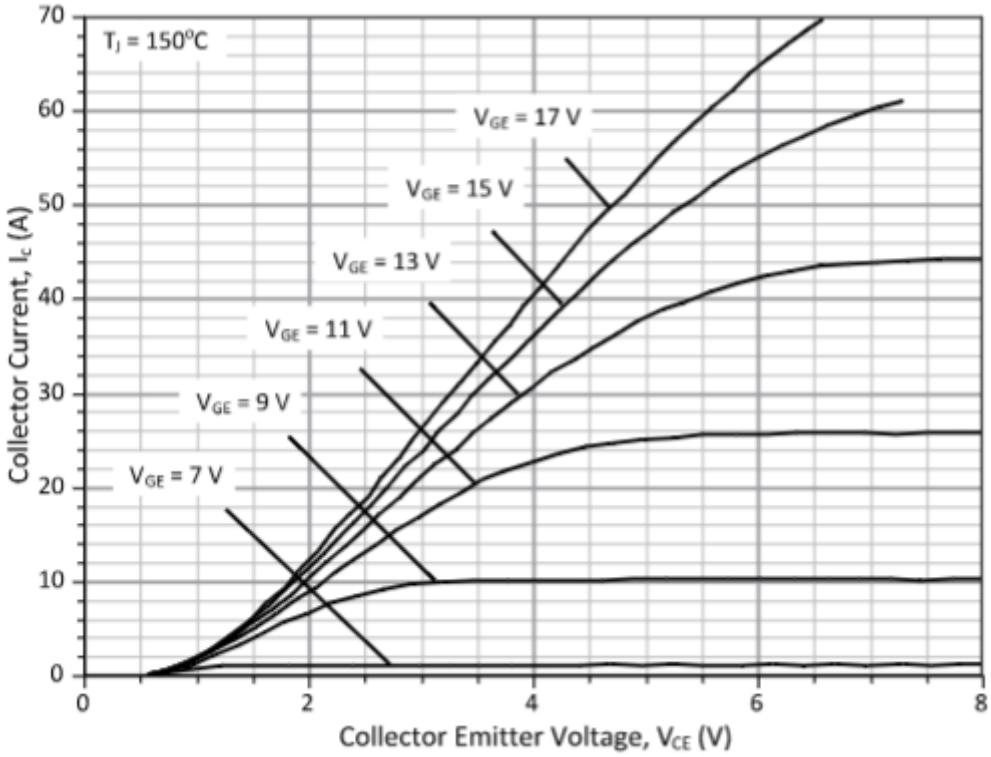


*Figure 6.7 - Typical output characteristics of transistors ($T_j = 150^0$) [41]*

$V_{GE} = 15\ V$ from the datasheet, Figure 6.8 shows that $V_{CE} = 2.2\ V$. It gives IGBT conduction losses:

$$P_{IGBT_{cond}} = 0.332 * 2.2\ V * 16\ A = 11.69\ W. \quad (6.31)$$

Free wheeling conduction losses are calculated with the helping figure below.

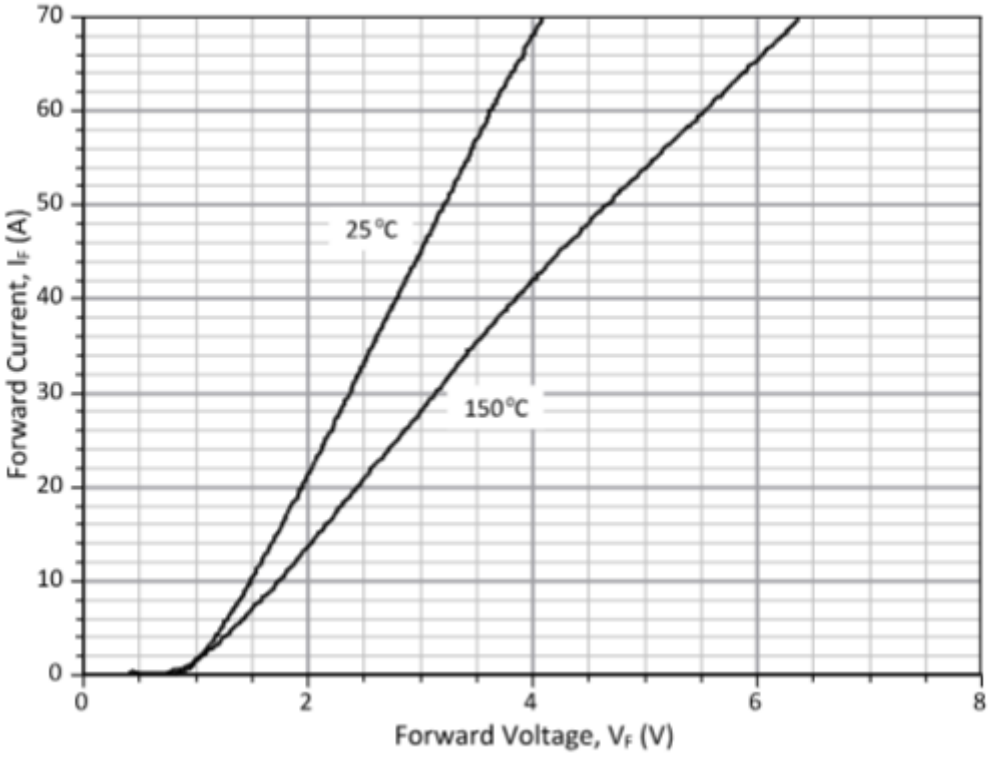


*Figure 6.8 - Free-wheel diode forward characteristic [41]*

Using conditions $T_j = 125^0$ and $I_F = 16\ A$ . According to (2.18):

$$P_{DIODE_{cond}} = (1 - 0.332) * 16\ A * 2.1\ V = 22.45\ \text{W}. \tag{6.32}$$

IGBT switching losses can be calculated with the helping Figure 6.9:

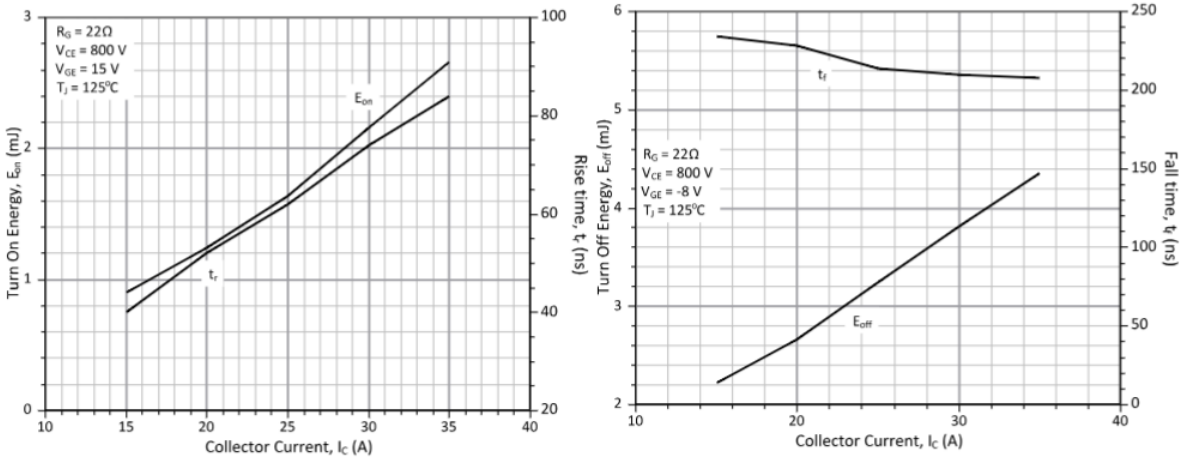


*Figure 6.9 - Inductive switching energy losses [41]*

Figure 6.9 shows that under the conditions $T_j = 125^0$ and $V_{GE} = 15$ V, continuous current $I_c = 16\ A$. Since curves on Figure 6.9 constructed under condition $V_{CE} = 800$ V, for all measured values should

be multiplied on coefficient 400/800=0.5. Switching-on energy losses $E_{SW(on)} = 0.49\,mJ$ and switching-off energy losses $E_{SW(on)} = 1.1\,mJ$.

Therefore, IGBT switching energy losses for 23 kHz are:

$$P_{IGBT_{SW}} = (0.49 + 1.15)\,mJ * 23\,kHz = 37.72\,W, \tag{6.33}$$

for 16 kHz are:

$$P_{IGBT_{SW}} = (0.49 + 1.15)\,mJ * 16\,kHz = 26.24\,W, \tag{6.34}$$

for 3.5 kHz are:

$$P_{IGBT_{SW}} = (0.49 + 1.15)\,mJ * 3.5\,kHz = 5.74\,W. \tag{6.34}$$

Free wheeling diode recovery losses can be calculated using Figure 6.10 [42]:

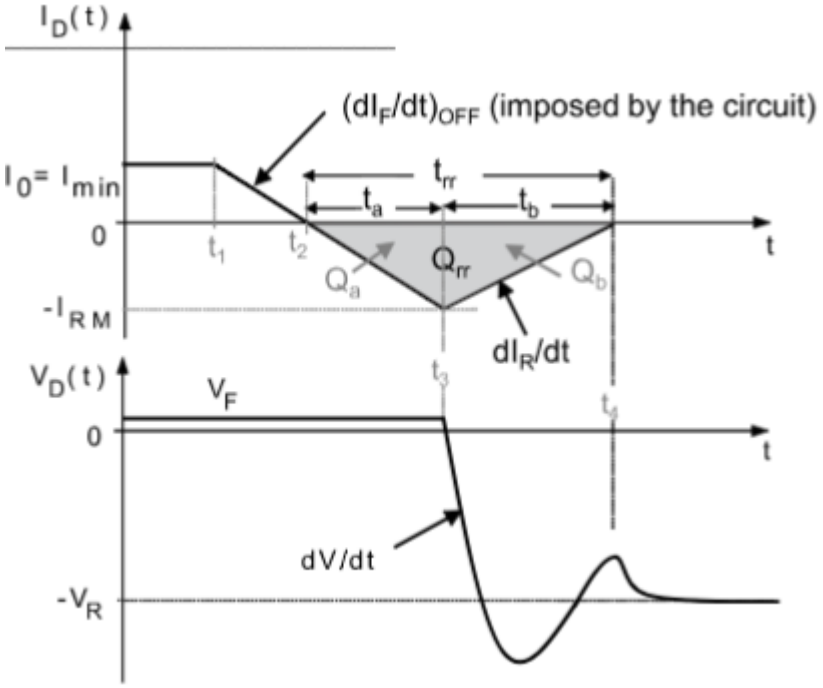


*Figure 6.10 - Current and voltage waveforms of a diode during turn-off phase [41]*

The general turn-off power expression:

$$P_{DIODE_{rec}} = Q_{rr} * V_{out} * f_{SW}. \tag{6.35}$$

Value $Q_{rr}$ can be rewritten as:

$$Q_{rr} = Q_a + Q_b = \frac{dI_F}{dt} t_a + \frac{dI_R}{dt} t_b. \quad (6.36)$$

From datasheet, $I_{rm} = 3.01\ A$, $\frac{dI_R}{dt} = 190\ A/\mu s$ and $t_{rr} = 36\ ns$. All these values are given with $V_R = 650\ V$. In this project we use 400 V. Therefore, values should be rewritten as: $I_{rm} = 1.85\ A$, $\frac{dI_R}{dt} = 117\ A/\mu s$ and $t_{rr} = 36\ ns$. Some values can be calculated:

$$Q_{rr} = \frac{1}{2} * I_{rm} * t_{rr} = 33.3\ nC. \quad (6.37)$$

Free wheeling diode recovery losses for 23 kHz are:

$$P_{DIODE_{rec}} = 33.3\ ns * 400\ V * 23\ kHz = 0.31\ W, \quad (6.38)$$

for 16 kHz are:

$$P_{DIODE_{rec}} = 33.3\ ns * 400\ V * 16\ kHz = 0.213\ W, \quad (6.39)$$

for 3.5 kHz are:

$$P_{DIODE_{rec}} = 33.3\ ns * 400\ V * 3.5\ kHz = 0.05\ W. \quad (6.40)$$

Thus, total transistor energy losses for 23 kHz according to (2.21) are:

$$P_{\text{transistor}} = 11.69\ W + 22.45\ W + 37.72\ W + 0.31\ W = 72.17\ W, \quad (6.41)$$

for 16 kHz are:

$$P_{\text{transistor}} = 11.69\ W + 22.45\ W + 26.24\ W + 0.213\ W = 60.593\ W, \quad (6.42)$$

for 3.5 kHz are:

$$P_{\text{transistor}} = 11.69\ W + 22.45\ W + 5.74\ W + 0.05\ W = 39.93\ W. \quad (6.43)$$

Unfortunately, pure SiC IGBT was not available on the market, and complex transistor was chosen – Si IGBT with SiC freewheeling diode. This is the industrial transistor which is constructed for $V_{CE}$ =1200 V and values of conduction losses are higher in comparison with Si IGBT from the previous chapter with $V_{CE}$ =600 V.

### 6.3.2 SiC MOSFET

The Silicon carbide MOSFET which meets the requirements and was chosen in the project is **SCT3080AL** [43]. Applications of this MOSFET are solar inverters, DC/DC converters, etc.

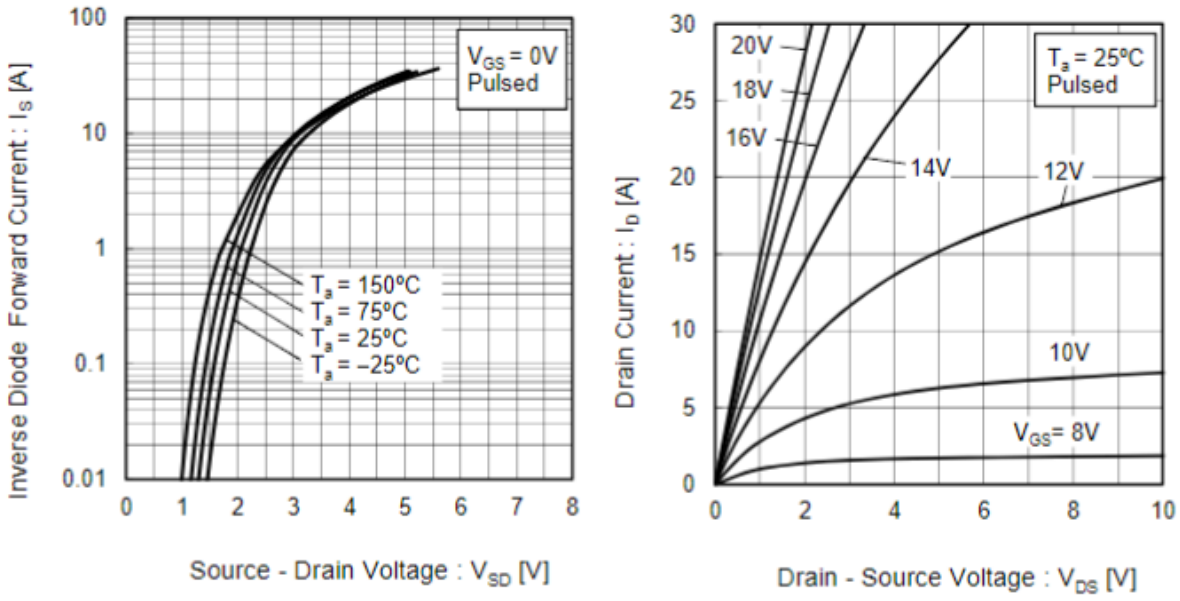


*Figure 6.11 - Output characteristics of transistor [43]*

MOSFET conduction losses can be found using Figure 6.11, where $V_{GS}$ is assumed $18\,V$ and $V_{DS} = 1.1\,V$:

$$P_{MOSFET_{cond}} = 0.332 * 1.1\,V * 16\,A = 5.84\,W. \tag{6.44}$$

Diode conduction losses ($V_{SD} = 3.6\,V$):

$$P_{DIODE_{cond}} = V_{SD} * I_F * (1 - D) = 3.6\,V * 16\,A * 0.668 = 38.48\,W. \tag{6.45}$$

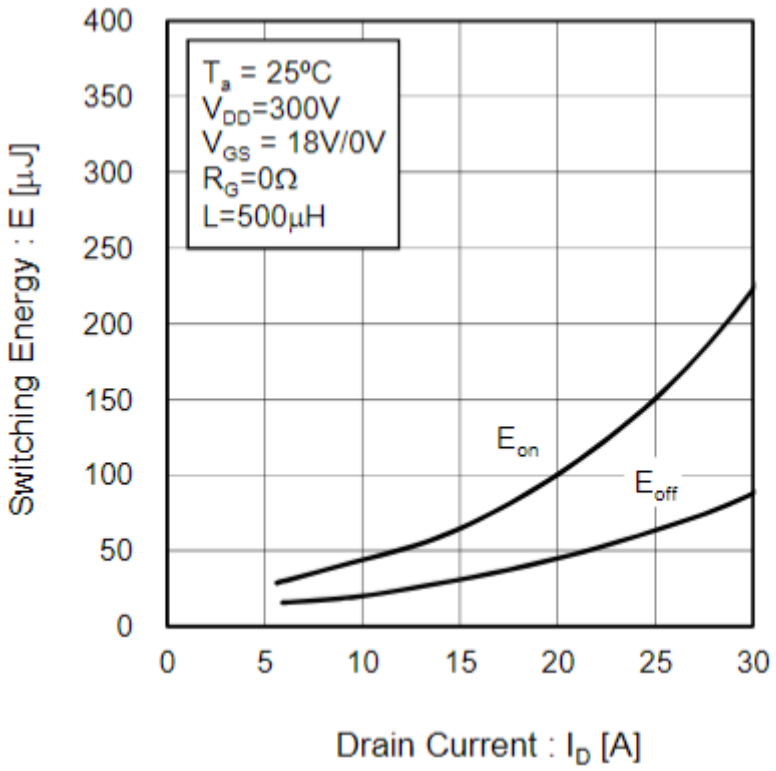


*Figure 6.12 - Typical switching losses [43]*

MOSFET switching energy is showed in Figure 6.12. $V_{DD} = 300\,V, but\, V_{DC} = 400\,V$, thus the coefficient of obtained results is 400/300 = 1.33. $E_{SW(on)} = 60 * 1.33 = 79.8\,\mu J$, $E_{SW(off)} = 30 * 1.33 = 39.9\,\mu J$.

MOSFET switching losses for 23 kHz with the help of (2.16) are:

$$P_{MOSFET_{SW}} = (79.8 + 39.9)\,\mu J * 23\,kHz = 2.75\,W. \tag{6.46}$$

MOSFET switching losses for 16 kHz are:

$$P_{MOSFET_{SW}} = (79.8 + 39.9)\,\mu J * 16\,kHz = 1.92\,W. \tag{6.47}$$

MOSFET switching losses for 3.5 kHz are:

$$P_{MOSFET_{SW}} = (79.8 + 39.9)\,\mu J * 3.5\,kHz = 0.42\,W. \tag{6.48}$$

Diode recovery losses can be calculated with expression (6.35), reverse recovery charge are taken from datasheet $Q_{rr} = 53\,nC$.

Diode recovery losses for 23 kHz are:

$$P_{DIODE_{rec}} = 53\ nC * 400\ V * 23\ kHz = 0.49\ W. \quad (6.49)$$

Diode recovery losses for 16 kHz are:

$$P_{DIODE_{rec}} = 53\ nC * 400\ V * 16\ kHz = 0.34\ W. \quad (6.50)$$

Diode recovery losses for 3.5 kHz are:

$$P_{DIODE_{rec}} = 53\ nC * 400\ V * 3.5\ kHz = 0.07\ W. \quad (6.51)$$

Thus, total transistor energy losses for 23 kHz according to (2.21) are:

$$P_{\text{transistor}} = 5.84\ W + 38.48\ W + 2.75\ W + 0.49\ W = 47.56\ W, \quad (6.52)$$

for 16 kHz are:

$$P_{\text{transistor}} = 5.84\ W + 38.48\ W + 1.92\ W + 0.34\ W = 46.58\ W \quad (6.53)$$

for 3.5 kHz are:

$$P_{\text{transistor}} = 5.84\ W + 38.48\ W + 0.42\ W + 0.07\ W = 44.81\ W \quad (6.54)$$

SiC MOSFET possesses too low switching losses and this fact leads us to the difference between energy losses at 23 kHz and 3.5 kHz - 5.8%

## 6.4 Gallium Nitride MOSFET

**GS66508B** [44] was chosen as the transistor. GaN MOSFET is the newest of the widely available transistors, accordingly it is the fastest ($f_{SW} > 10\ MHz$) and the one with the lowest amount of losses (zero reverse recovery losses).

The transistor is considered with normal temperature $T_j = 25^0$. MOSFET and reverse conduction losses are calculated using (2.15) and (2.18) and the figure below.

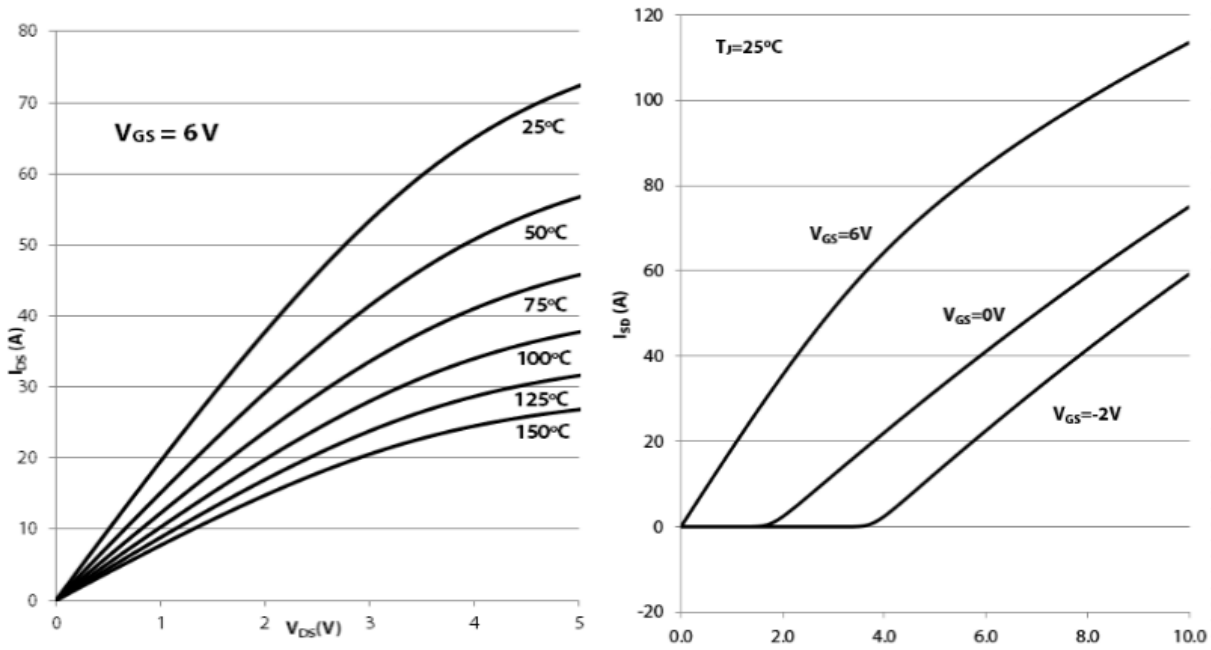


*Figure 6.13 - Electrical performance graphs [44]*

MOSFET conduction losses are:

$$P_{MOSFET_{cond}} = D * I_{DS} * V_{DS} = 0.332 * 16\ A * 0.85\ V = 4.5\ W, \quad (6.55)$$

diode conduction losses are:

$$P_{DIODE_{cond}} = (1 - D) * I_{SD} * V_{SD} = 0.668 * 16\ A * 0.5\ V = 5.3\ W. \quad (6.56)$$

MOSFET switching energy losses are calculated using (6.19) and values from datasheet: fall time $t_f = 5.2\ ns$, turn-off delay $t_{D(off)} = 8\ ns$, rise time $t_r = 3.7\ ns$ and turn-on delay $t_f = 4.1\ ns$.

Therefore, MOSFET switching energy losses for 23 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\ V * 16\ A * (5.2 + 8 + 3.7 + 4.1)\ ns * 23\ kHz = 1.55\ W. \quad (6.57)$$

MOSFET switching energy losses for 16 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\ V * 16\ A * 21\ ns * 16\ kHz = 1.08\ W. \quad (6.58)$$

MOSFET switching energy losses for 3.5 kHz are:

$$P_{MOSFET_{SW}} = \frac{1}{2} * 400\ V * 16\ A * 21\ ns * 3.5\ kHz = 0.24\ W \quad (6.59)$$

As was said above, this transistor has zero reverse recovery losses. Therefore, the total transistor energy losses for 23 kHz are:

$$P_{\text{transistor}} = 4.5\,W + 5.3\,W + 1.55\,W = 11.35\,W. \tag{6.60}$$

Total transistor energy losses for 16 kHz are:

$$P_{\text{transistor}} = 4.5\,W + 5.3\,W + 1.08\,W = 10.88\,W. \tag{6.61}$$

Total transistor energy losses for 3.5 kHz are:

$$P_{\text{transistor}} = 4.5\,W + 5.3\,W + 0.24\,W = 10.04\,W. \tag{6.62}$$

This type of transistor has the lowest level of losses, and almost completely smoothed the difference between the two algorithms.

## 6.5 Comparative analysis

Comparative table with absolute value for three legs of the converter (with 3 transistors) is built up in this chapter.

*Table 6.1 - Comparative table of converter energy losses for three legs*

| Type | MPC (23 kHz) | VOC (23 kHz) | VOC (5 kHz) |
|---|---|---|---|
| **Si IGBT (W)** | 159.9 | 135.6 | 92.1 |
| **Si MOSFET (W)** | 641.3 | 461.2 | 136.6 |
| **Si-SiC IGBT (W)** | 216.5 | 181.8 | 119.8 |
| **SiC MOSFET (W)** | 142.7 | 139.7 | 134.4 |
| **GaN MOSFET (W)** | 34.1 | 32.6 | 30.1 |

Table 6.1 shows that the best possible solution is to use GaN MOSFET in the project. It gives the lowest energy losses.

Efficiency calculating for converter without the filter can be done with a deeper analysis.

Efficiency for MPC (23 kHz) with SiC MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{142.7\,W}{5800\,W}\right) * 100\% = 97.54\%. \tag{6.63}$$

Efficiency for MPC (23 kHz) with GaN MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{34.1\,W}{5800\,W}\right) * 100\% = 99.4\%. \quad (6.64)$$

Efficiency for VOC (23 kHz) with SiC MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{139.7\,W}{5800\,W}\right) * 100\% = 97.59\%. \quad (6.65)$$

Efficiency for VOC (23 kHz) with GaN MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{32.6\,W}{5800\,W}\right) * 100\% = 99.44\%. \quad (6.66)$$

Efficiency for VOC (5 kHz) with SiC MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{134.4\,W}{5800\,W}\right) * 100\% = 97.68\%. \quad (6.67)$$

Efficiency for VOC (5 kHz) with GaN MOSFET is:

$$\eta = \left(1 - \frac{P_{losses}}{P}\right) * 100\% = \left(1 - \frac{30.1\,W}{5800\,W}\right) * 100\% = 99.48\%. \quad (6.68)$$

The Table 6.1 and calculations above show that the models have a small difference between the converter losses for three legs when using SiC and GaN MOSFETs. The difference in losses between MPC (23 kHz) and VOC (23 kHz) be caused by the fact that switching frequency in VOC is higher than the set in the modulator, which was 16 kHz.

The differences of converter losses are less than 1% for SiC and GaN MOSFETs. However, the GaN MOSFETs have the lowest losses in all three models. In the case of GaN MOSFET, MPC (23 kHz) model can be used without large additional energy losses in comparison with VOC (23 kHz and 5 kHz), but with better performance. Converter losses using GaN MOSFETs (without LCL filter losses) with the MPC algorithm at rated initial values is 0.6%; with the VOC (23 kHz) - 0.56%; with the VOC (5 kHz) – 0.52%.

# 7. Discussion

*This chapter discusses the results obtained in the previous chapters and gives recommendations for a better solution.*

The proposed cascaded MPC model has been evaluated. After reviewing the relevant literature, the MPC model was compared with the VOC model in the thesis. Both models were modified for a more equitable comparison. Several requirements for evaluation of the MPC model were chosen: power factor, total and individual harmonic distortion, and power losses. The first two requirements have certain limits, while the limits for power losses are not defined and supposed to be as low as possible.

The necessary simulations have been done. The calculated average switching frequency of cascaded MPC model (23 kHz) was used as switching frequency of the VOC algorithm. Considering the fact that such a high frequency is not normally used in the VOC model, it was decided to use 5 kHz switching frequency for the VOC algorithm as an additional experiment. All experiments were performed at initial values of 400 V DC-link voltage and 16 A grid current. The experiment results for all three experiments were introduced in Chapter 5.

Power factor meets requirements in all the three experiments, provided that the injected active and reactive power are 5800 W and 2705 VAr respectively. Power factor is 0.9 at these power values.

The total and individual harmonic distortion for the experiments were presented in Table 5.2. Distortion for all the three experiments meets the requirements. The cascaded MPC (23 kHz) model has the lowest THD of all the three experiments (0.76%). The VOC model at 23 kHz switching frequency has a THD of 0.79% and VOC model at 5 kHz – has a THD of 1.49%. Higher frequency makes the signal smoother, and this agrees with the theory. Although the THD of the MPC (23 kHz) and VOC (23 kHz) are almost equal, but the magnitudes of some higher frequencies ($10^{th}$ and above) are lower for the MPC algorithm than for the VOC.

Applying different types of transistors to the models was done in Chapter 6. Comparison of results is presented in Table 6.1. The difference between converter losses of two algorithms with the same switching frequency caused by the fact that the modulator switching frequency 16 kHz in VOC is lower than the switching frequency 23 kHz of the control system. The Table 6.1 shows that VOC algorithm at 5 kHz has the lowest losses, but the difference in the losses of the converter using GaN MOSFETs for the MPC (23 kHz) and VOC (5 kHz) is negligible.

The best choice for a cascaded MPC is, therefore, the GaN MOSFET. Converter losses (without losses in the LCL filter) in this case were– 0.6%, using the VOC (5 kHz) algorithm – 0.5%.

The MPC algorithm has the lowest total and individual harmonic distortion of all three cases. But it also has the highest power losses. Taking into consideration the fact that the MPC concept requires high computational powers, it can be concluded that insignificant performance advantage of the MPC concept cannot be a weighty reason to apply the complex computational intensive MPC algorithm in this setup. The VOC algorithm at 5 kHz is seen as the best solution in this setup.

# 8. Conclusion and recommendations for further work

*This chapter gives a short conclusion of the thesis. It also gives suggestions for further work.*

## 8.1 Conclusion

The cascaded model predictive control algorithm has been investigated. The requirements for converter performance were chosen. There were three criteria that were being used for control concept evaluation: power factor, total and individual harmonic distortion, and power losses. A voltage oriented control algorithm was used for comparison with model predictive control. MATLAB Simulink has been used to implement the MPC and VOC concepts and make the simulations. The simulation results, which were obtained, are based on the MPC and VOC algorithms. The VOC concept has been simulated for two cases: at the high and low switching frequency. The results of modelling were obtained and analysed. These simulations have shown that the MPC algorithm produces less total and individual harmonic distortion than the conventional VOC algorithm. Several different transistor technologies were investigated. Converter power losses for each model with different types of transistors were also calculated. A comparison of several transistor technologies has shown that the use of the GaN MOSFET yields almost identical converter losses in all three considered cases. It is concluded that it is not practical to use the complex computational intensive MPC algorithm in this setup, and it can be replaced by the VOC algorithm.

## 8.2 Recommendations for further work

There are two aspects in which further work can be continued:

- The proposed model has been evaluated using computer simulations. Hardware testing of the simulated models is needed. This applies to both algorithms and different transistor technologies.
- The LCL filter power losses in all three models can be determined. Full converter power losses can be found after that.

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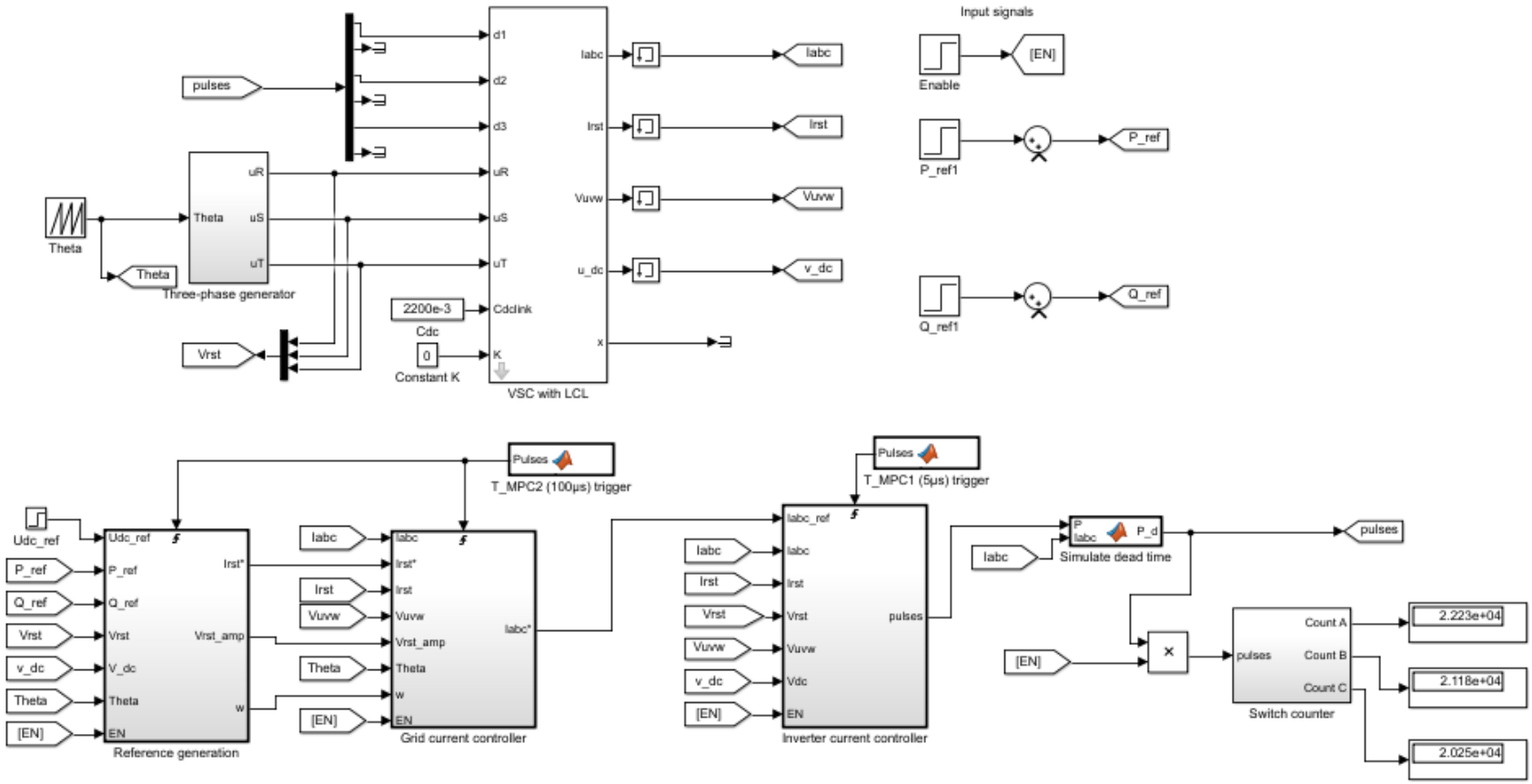
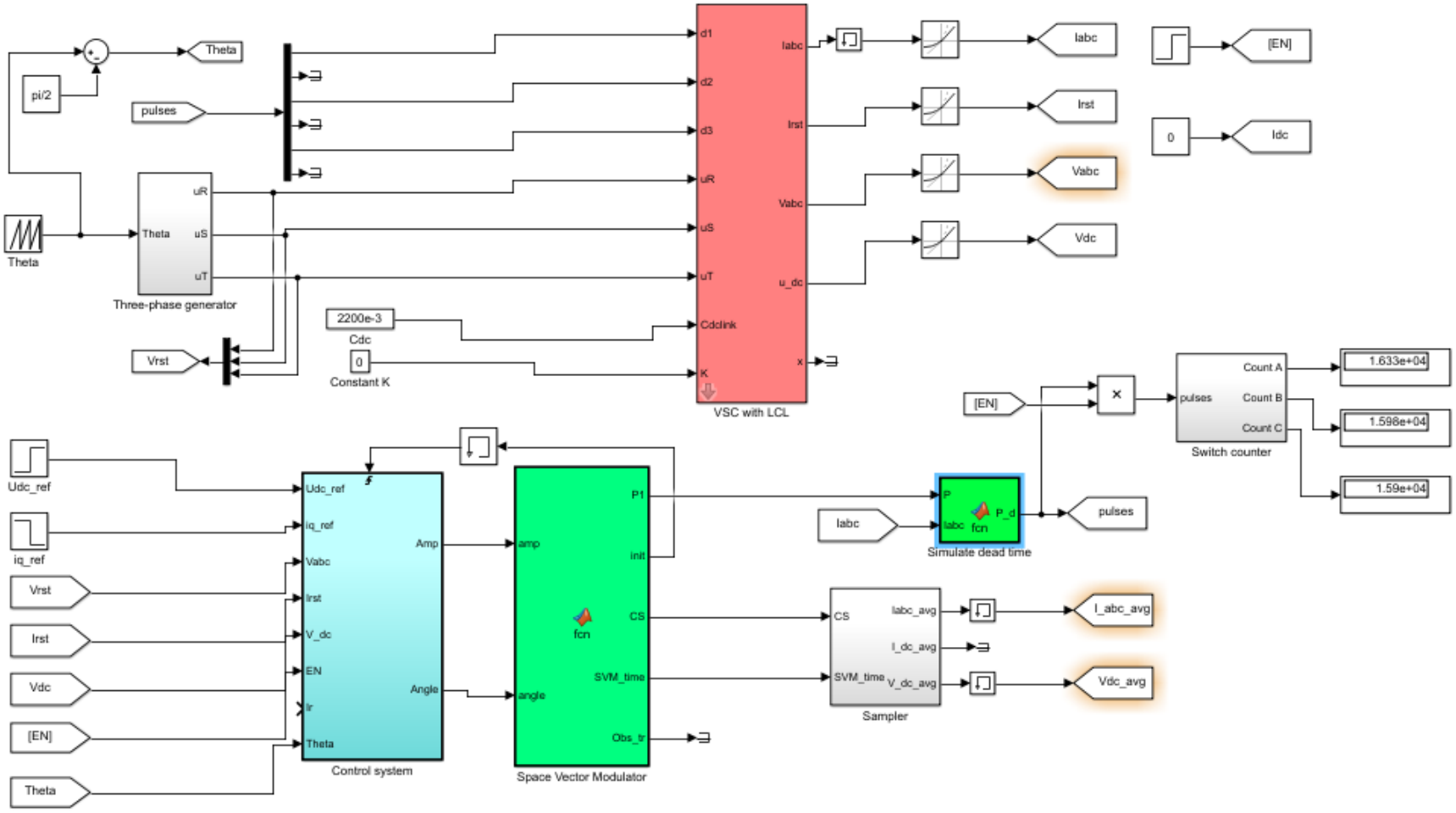
# Appendix A – VSC is controlled by MPC



# Appendix B – VSC is controlled by VOC



# Appendix C – Simulation models

See attached zip-file.