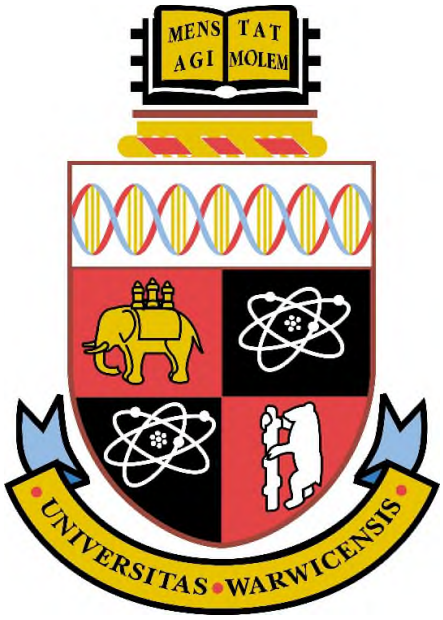
A Fast-acting Protection Scheme for Series Compensators in a Medium-Voltage Network



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DECLARATION

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has been composed by myself and has not been submitted in any previous application for any degree.

Parts of this thesis have been published by the author during the period of study, from March 2017 to January 2020. They are given in full detail in the Publication List section.

Erfan Bashar
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ABSTRACT

In recent 20 years medium voltage networks have been becoming one of the important interfaces between the power plants and loads due to the increasing load demand as well as number of distributed generators connected to the network. This is the reason, managing the power flow, and voltage profile of the network at the lowest possible power losses and also price are of the utmost importance.

The series compensators such as a static synchronous series compensator are of the most cost effective power compensators that also have the high efficiency in controlling the power flow and voltage profile. However, their drawback is their vulnerability against the short circuit. This thesis presents a new protection scheme for an SSSC in an MV network by using a varistor and thyristors to eliminate this weakness.

The DC offset phenomenon is one of the main uncertainties that has been studied in the thesis. This phenomenon could cause a delay in the circuit breakers' performance. In this thesis, the parameters of the machines that have most influence on the time when the fault current will pass the zero point have been analysed. Besides, the impact of the DC offset in the medium voltage network has been studied.

Furthermore, the thermal issues have always been one of the most challenging problems for the power electronics devices. This thesis investigates a new packaging style by using the phase change material to improve the thermal managing of a press-pack thyristor during a short circuit. This packaging style is able to absorb the heat as much as required and also could decrease the thermal resistance.

Publication List

Chapter 3

1. Erfan Bashar, Dan Rogers, Ruizhu Wu, Li Ran, Mike Jennings, Timothy C. Green, and Philip Mawby, “ A New Protection Scheme for an SSSC in an MV Network by Using a Varistor and Thyristors”, in *IEEE Transactions on Power Delivery*, doi: 10.1109/TPWRD.2020.2982512.

2. Erfan Bashar, Robert Wu, Weihua Shao, Li Ran, Han Qin,” An Appraisal of Possible Protection Schemes of Static Series Compensators in Medium Voltage Power Networks”, The 8th International Conference & Workshop, REMOO ENERGY 2018, 29–31 May 2018, VENICE / ITALY.

Chapter 4

1. E. Bashar, Q. Han, R. Wu, L. Ran, O. Alatise and S. Jupe, "Analysis of DC offset in fault current caused by machines in a medium voltage distribution network," in *The Journal of Engineering*, vol. 2019, no. 17, pp. 3494-3499, 6 2019. doi: 10.1049/joe.2018.8221

Chapter 5

2. Erfan Bashar, Ruizhu Wu, Li Ran, Jose Ortiz Gonzalez, Arne Benjamin Renz, Guy Baker, Mike Jennings, Philip Mawby, Tim C. Green, Dan Rogers, " A Method to Contain the Temperature Rise of a Press-Pack Thyristor during a Short Circuit Protection Operation," accepted to publish in IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, 2019

List of Acronyms

B2B VSC	Back To Back Voltage Source Converter
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPC	Neutral Point Clamped
PWM	Pulse Width Modulation
RMS	Root Mean Square
SPWM	Sinusoidal Pulse Width Modulation
SSSC	Static Series Synchronous Compensator
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCPAR	Thyristor-Controlled Phase Angle Regulator
TCR	Thyristor-Controlled Reactor
TCSC	Thyristor-Controlled Series Capacitor
TCSR	Thyristor-Controlled Series Reactor
TSC	Thyristor-Switched Capacitor
TSR	Thyristor-Switched Reactor
TSSC	Thyristor-Switched Series Capacitor
TSSR	Thyristor-Switched Series Reactor
UHVDC	Ultra High Voltage Direct Current
UPFC	Unified Power Flow Controller
VSC	Voltage Source Converter

List of Variables and Symbols

ΔTj	Junction Temperature Variation
A	Area, Cross-Section
C	Specific Heat Capacity
Cdc	Dc Link Capacitor
D	Thickness, Distance
di/dt	Rate Of Change Of Current With Time
Dvth/dT	Rate Of Change Of The Threshold Voltage With Temperature
E_f	Excitation Flux
F	Frequency
I	RMS Current
I_{break}	Break Fault Current, RMS
I_{ac}	AC Current, RMS
I_{dc}	DC Current
I_d	D-Axis Current
I_q	Q-Axis Current
I_m	Maximum Peak Current
I_{make}	Make Fault Current, RMS
L	Inductance
P	Active Power
Q	Reactive Power
R	Resistance, Resistor
Rth	Thermal Resistance
Rth,J-C	Thermal Resistance Junction To Case
X/R	Reactance/Resistance Ratio

X_d''	Direct-Axis Subtransient Reactance
X_d'	Direct-Axis Transient Reactance
X_d	Direct-Axis Synchronous Reactance
Xl	Leakage Reactance
Xσs	Stator Leakage Reactance
X_m	Magnetising Reactance
Xs	Induction Machine Per Phase Stator, Stator Winding Reactance
S	Total Power
s	Rotor Slip
T	Temperature
T_a	The Armature/Stator Time Constant
Tamb	Ambient Temperature
T_d''	The Subtransient Time Constant
T_d'	The Transient Time Constant
Tj	Junction Temperature
Tj-Max	Maximum Junction Temperature
V	Voltage
V1	Primary Busbar Voltage
V2	Load Busbar Voltage
Vabc	Grid Voltage
Vl	Nominal Line Voltage, RMS
Vn	Nominal Voltage, RMS
V_m	Peak Value Of Stator Voltage
Vf	Forward Voltage of a Diode
Vg	Gate Voltage
Λ	Specific Thermal Conductivity

τ	Time Constant
Θ_0	The Initial Rotor Position
Ω	Angular Frequency of The Grid
Δ	Ratio of a Load to The Total Load
h	Overall Efficiency

1 INTRODUCTION

The protection, and reliability of the distribution and transmission networks have always been one of the most critical and challenging issues of the system studies. Finding a cost-effective and reliable technique to protect the network, not only increases the system reliability but also prevents the future expenses that may apply on the system in case of using an improper protection system. Moreover, having a competent protection technique could make possible the utilisation of facilities that are no longer used due to their vulnerability to the faults. This advantage makes the operators enable to have more options in choosing the most cost-effective and optimised utilities in the network that it also can improve the system efficiency and decrease the network cost.

In terms of the protection, the response speed of the protection system has a great impact within the protection process. If the relays and circuit breakers can act faster, which means they can cut off the short circuit current flowing through devices faster, they may be able to prevent the devices' temperature from increasing. Faults like short-circuits are associated with thermal failures due to high temperatures. This high temperature will have a negative impact on the device, especially if the maximum temperature of operation is reached.

In past 20 years, the utilization of medium voltage networks has been gradually increasing. The medium voltage (MV) systems are typically defined as the range of 600-69,000 VAC [1]. These networks are an interface between the transmission lines (which are supplied from the power plant and called the high, extra-high and ultra-high voltages) and the low voltage (which are the final loads or destination). The aim of

medium voltage networks is distributing the power between low voltage systems and also feeding the medium voltages loads such as industrial loads, hospitals or commercial loads. Large industrial complexes and factories that require a substantial amount of power often utilize medium supply voltages. The electrical variational analysis dictates that the voltage is inversely proportional to amperage. This means that when the voltage is increased amperage is decreased to complete the operation. Motors and electrical equipment designed to operate with higher voltages use less electricity and are more economical to operate. Most primary sub-stations do not receive more than 35,000 VAC from utility supply. The primary sub-station can supply stepped down power to secondary sub-station(s) or to a single building [1].

Figure 1.1 demonstrates a schematic medium voltage network. In this schematic two medium voltage feeders are connected to each other through a static synchronous series compensators. The aim of this compensator is improving the power flow and also voltage stability between these two feeders. As it can be seen in the Fig. 1.1, this kind of compensators are located in a series situation in the network. It means they will be highly vulnerable within a fault condition in the network. That is the reason, in spite of their low cost and power losses as well as high efficiency in improving the voltage profile and power flow, they are not utilised in the network.

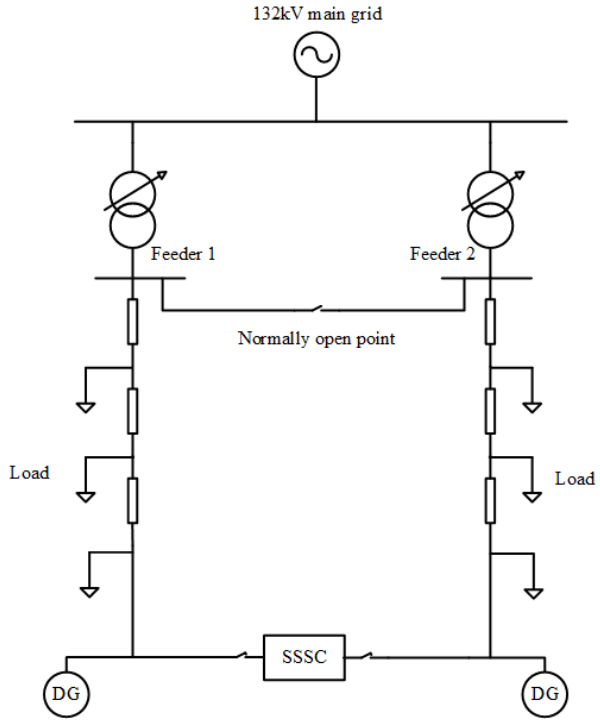

Figure 1.1: A schematic of a medium voltage network

1.1 UTILITIES VULNERABLE TO THE FAULT IN THE NETWORK

The vulnerable utilities, in this thesis, are defined as devices installed in series or having a series compartments in the network such as static synchronous series compensators. These facilities are at a high risk during a short circuit, due to their series part.

Static Synchronous Series Compensators (SSSCs), see Fig. 1.2, are of the important facilities that can improve the voltage profile, power flow, and reliability of the network in a significantly lower cost as well as lower power losses compared to other compensators while their efficiency is almost as high as those. But, their main drawback is their installation location in series with the power system. This position puts them into the risk of getting damaged during a short circuit. This is the reason, these utilities are not being usually used in the network. Therefore, a protection

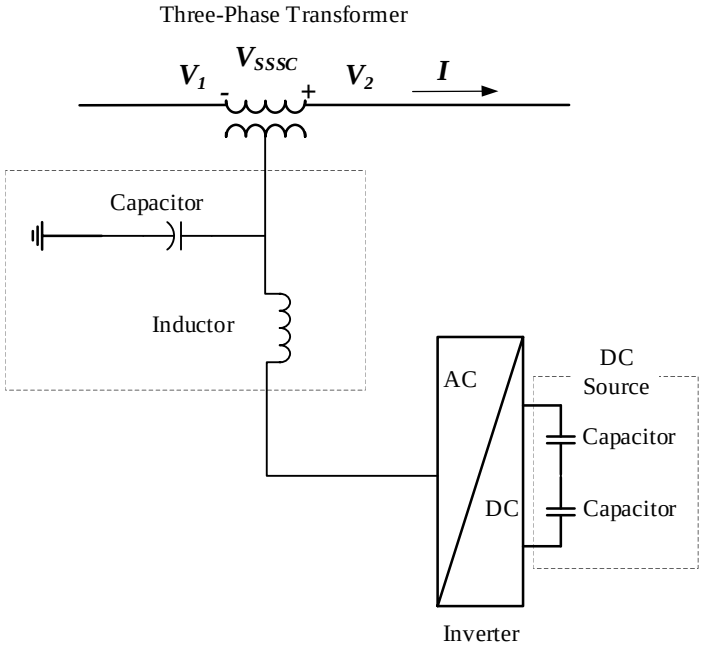

Figure 1.2: A schematic of a static synchronous series compensator

scheme which can eliminate this issue could open a way to make the usage of these practical facilities reasonable.

The following tables show a comparison between different FACTS controllers and prove the SSSC is one of the economic and efficient ones.

Table 1.1: A comparative performance of major FACTS controller [2], [3], [4]

FACTS Controllers	**Load Flow Control**	**Voltage Control**	**Transient Stability**	**Oscillation Damping**
SVC/STATCOM	x	xxx	xxx	xx
TCSC	xx	x	xxx	xx
SSSC	xxx	x	xxx	xx
TCPAR	xxx	xx	x	xx
UPFC	xxx	xxx	xxx	xxx
xxx-strong Influence		xx-average influence		x-small influence

Table 1.2: Cost comparison of various facts device [5]

FACTS Devices	**Cost ($/kVar)**
Shunt Capacitor	8
Conventional Series Capacitor	20
Conventional PAR Transformer	20
SVC	40- controlled part
TCSC	40- controlled part
STATCOM	50
UPFC Series Portions/SSSC	50 (**$/kW**)- series power flow
UPFC Shunt Portions	50- controlled part

Table 1.3: Cost comparison of various facts device [6]

FACTS Devices	Capacity [MVA] (shunt, Series)	Initial Cost (Million USD)
SVC	(150 , 0)	6
TCSC	(0 , 2.4)	0.096
STATCOM	(150 , 0)	7.5
SSSC	(0 , 12.5)	0.625
UPFC	(100 , 18.4)	5.92

Table 1.4: HVDC Cost Estimation [5]

HVDC LINKS	Cost ($/kW/terminal)
Back to Back, 200 MW	108
±250kV, 500MW	145
±350kV, 1000MW	107
±500kV, 3000MW	75

Table 1.5: Initial Cost [7]

HVDC Power Rated	Contracted Cost, Converters (Million USD)
350	75.15
500	138.91
750	165.77

Figure 1.3 shows a location of a three-phase short circuit in the network. In order to show the fault current value passes through a SSSC during a short circuit condition, a simulation has been done. During this simulation, the SSSC works in a normal operation with a closed control system in an MV network. A simulation has been done in MATLAB Simulink in order to show the short circuit quantity in an MV network. As it can be seen in Fig. 1.4, if a short circuit happens in the point shown in Fig. 1.3, the current can rise to 12,000 A that passes through the SSSC. This fault current can severely damage the power electronics facilities used in the inverter.

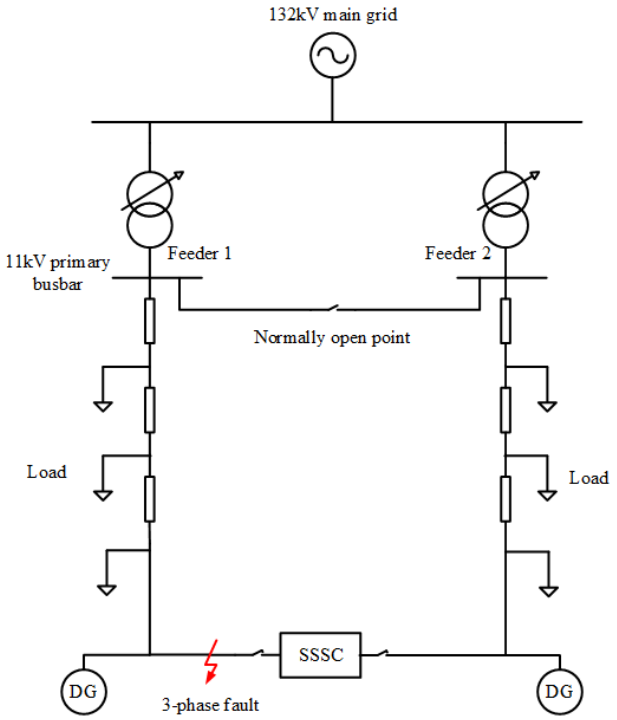

Figure 1.3: A schematic of a medium voltage network

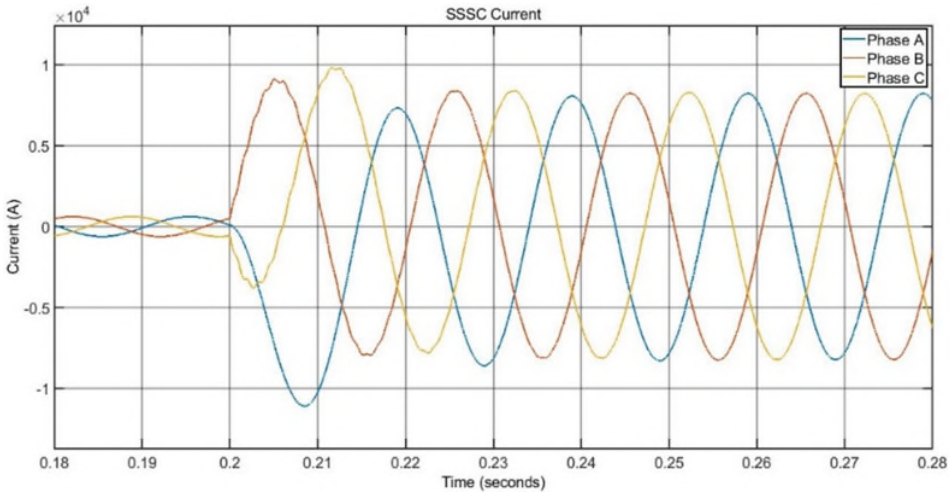

Figure 1.4: The fault current passing through SSSC without protection

1.2 PROTECTION TECHNIQUE BY USING THYRISTORS AND A VARISTOR

As it is known, the power electronics devices are the cutting-edge technology that have been using in many applications because of their unique abilities. In fact, these devices are able to withstand very high current and voltage and also their very fast operation speed makes them more efficient compared to devices containing the mechanical compartments. Also, Power electronics devices can be used to convert and control the flow of electrical power. Their benefits and drawbacks can be categorized as:

- ✓ High efficiency due to the low loss in the power semiconductor devices.
- ✓ High reliability of the power electronic converter system.
- ✓ Long life and less maintenance due to absence of any moving parts.
- ✓ Flexibility in the operation
- ✓ Fast dynamic response compared to the electromechanical converter system.
- ✓ Small size and less weight, thus low installation cost.
- x Generation of harmonics in the supply system as well as in the load circuit.
- x Having low overhead capacity

A protection technique like in Fig. 1.5 can be utilised to improve and expedite the protection process according to the power electronics devices' fast acting and high-current and voltage abilities. In this method,

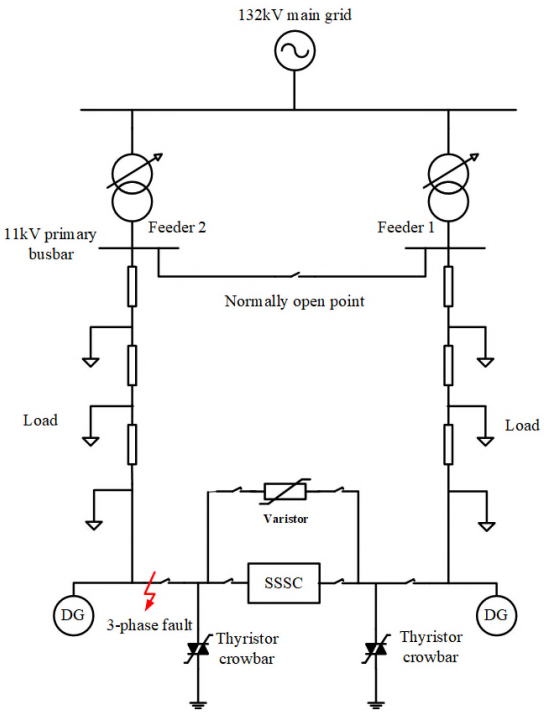

Figure 1.5: A protection method

Thyristor crowbars and a varistor are the main devices to form this technique. In this technique, when a fault happens, first relay recognises the short circuit, then the varistor limits the voltage rise and decreases the current passing through the SSSC by allowing the current to pass through itself. After that, thyristors are triggered on to let the current pass through them rather than the SSSC. At the end, the circuit breakers will open to isolate the SSSC from the MV network.

An MV circuit breaker has shown in Fig. 1.6. MV circuit breakers are conventional methods that are used to protect devices in the MV network. Their cost and dimensions depend on their voltage rate, break fault current and make fault current. Their opening time depends on different parameters such as arcing time and the their current rating [8].

Thyristors, see Fig. 1.7, are still the best choice for high-current and high-power applications over the other semiconductors. Their PNPN

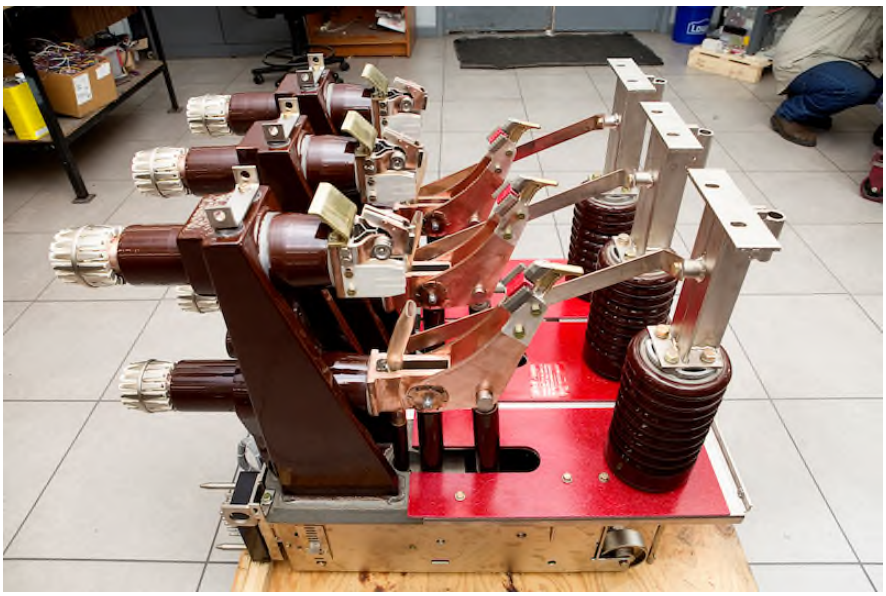

Figure 1.6: An MV circuit breaker [9]

structure which is made of a silicon wafer, is able to withstand several thousand amps in the normal operation that during the surge condition can even be several times more than its normal one. Regarding the voltage it also can tolerate several thousand volts that makes it a very practical and unique device for the high-power applications.

A varistor, see Fig. 1.8, acts like a surge arrester that can control the voltage surge during a fault or overload and its operation time is from some microseconds to a few milliseconds. The varistor acts like an open circuit when the voltage is very low, but by increasing the voltage value it will become like a short circuit and let the current pass through it. They

Figure 1.7: A thyristor crowbar [10]

can withstand very high current and voltage depending on their operation time.

The advantages of the proposed method could be summarised as follows:

- Very fast-response performance compared with Circuit Breakers (A few microseconds for thyristor compared to at least 3 cycle for CBs, more information in Chapter 3).
- Relegating the back-up circuit breaker's rate.
- Decreasing the arc level.
- Decreasing the maintenance cost.
- Cheaper compared to CB with the lower maintenance cost.
- Taking up a smaller room

Figure 1.8: A Varistor [11]

1.3 TEMPERATURE ISSUE AND HEATSINK SYSTEM

It definitely can be claimed that the temperature problem is the most challenging issue in terms of power electronics devices. Therefore, thermal management is a high priority topic in power electronics studies. As it is shown in the Fig. 1.9, a temperature rise during the thyristor operation can cause a failure and a severe damage to the thyristor wafer. That is why, managing the temperature during their operation especially during the surge condition is very important. Because within a short

Figure 1.9: A damaged thyristor during a failure due to the temperature rise [12]

circuit, the temperature rise happens within a very short time (up to 1 second), the heatsink has to be able to absorb the heat very fast.

The conventional heatsinks, see Fig. 1.10, are mostly made of Aluminium material and they are designed to be used within the normal operation condition. It means, during the short circuit condition, they are neither capable nor enough capable of controlling the temperature and protecting the device against the temperature rise. Thus, having a heatsink system that can decrease the delay of heat transmission and also is capable of storing a huge heat within the fault will certainly be very useful.

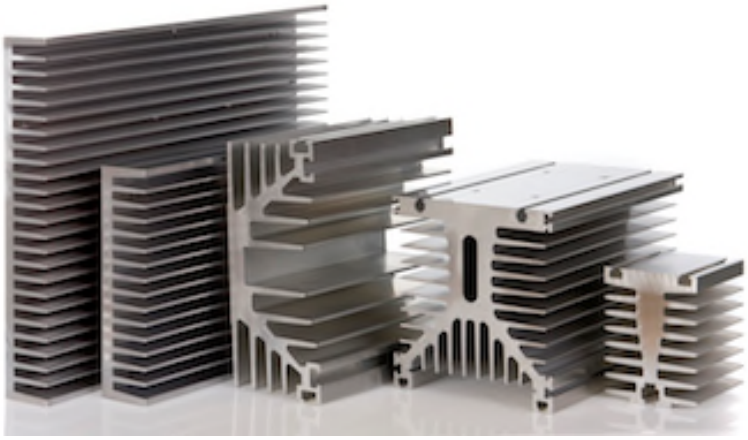

Figure 1.10: The conventional heatsinks [13]

1.4 CONTRIBUTIONS

This section presents contributions and motivation of carrying out this research. The main contributions of this thesis are defined as:

1. Increasing the reliability and protection level of the MV network, by introducing a new protection method for the SSSC. Using this technique will eliminate the SSSC vulnerability against the fault that makes the usage of the SSSC less challenging and risky.

2. Investigating the DC offset effect in the medium voltage networks to study its influence in the MV networks. In fact, this study consider the parameters can change the value of the DC offset. This phenomenon has a great impact during the turning-off process of power electronics devices such as thyristor.

3. Introducing a new heatsink based on the phase change material during the short circuit. The aim of this heatsink is limiting the temperature rise to protect the devices especially during a surge condition.

1.5 THESIS OUTLINE

In this section, each chapter is introduced briefly to give a clear idea about the aims will have been investigated in this thesis.

Chapter 2: A literature review and comparison on different power compensators and also advantages and drawbacks of using the static series compensators have been carried out in this chapter. Then, a review on a thyristor and a Varistor structure has been done to give a clear understanding of their abilities and applications.

Chapter 3: In this chapter, a new fast-acting protection scheme in order to expedite the protection process of a static synchronous series compensator against a short circuit will have been presenting. Furthermore, the surge condition of the thyristor and varistor for using in the fault will be investigated as well. Also, a closed-loop control system for the static synchronous series compensator will be presented.

The results of this chapter have been published in IEEE Transactions on Power Delivery journal, and have been presented at the REMOO ENERGY Conference, 2018, Italy.

Chapter 4: The DC offset phenomena could always be a potential issue for the performance of the protection facilities in the network. Thus, this chapter discusses the effect of the DC offset in the network and also considers how much this phenomenon could influence the protection systems in a medium voltage network.

The results of this chapter have been published in IET journal of Engineering.

Chapter 5: The heatsink facilities are very important in the case of the power electronics system, especially during the short circuit when a huge current passes through the device, this issue is highlighted. This chapter presents a new heatsink style that is capable of absorbing more heat and also decreasing the thermal resistance of a press-pack thyristor from the junction to the case by using the phase change material.

The results of this chapter presented at the ECCE conference (2019 in Baltimore).

Chapter 6: At the end, a conclusion about the achievements obtained within this research is presented, and the aims of doing this research is summarised. Then, the future works that could be carried out in further of the research's objectives are introduced.

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2 POWER COMPENSATORS AND PROTECTION SCHEMES

2.1 INTRODUCTION

Nowadays, due to the increasing number of customers and load demand as well as adding new kinds of loads such as Electrical Vehicles (EV) charging stations to the network, the demand for power has been quickly rising. This means either the current power plants and generators have to produce more power or new generators such as distributed generators (DGs) have to be added to the grid. By adding more DGs and loads to the network, the power management/control, and voltage profile will become very important for the network. Since most of the protection devices which are used in networks (like circuit breakers), are controlled mechanically, thus managing the load changing and damping the transient oscillations, due to the slow and discrete switching response, are very difficult to be coped with.

Given the aforementioned issues, the use of compensators in grids is vital to deal with these difficulties for more security and enhance the power supply quality. In this case, series and shunt compensations are fundamental structures of all compensators or flexible AC transmission systems (FACTS) that are connected to the power system [1]. The main advantages are decreasing the network power losses, fast response, improved controllability and increased power transfer capability. There are different compensation devices/systems: capacitors, capacitors and inductors, and active voltage source (synchronous generator), which can be passive or active. Shunt inductors and capacitors as well as series

capacitors are passive compensators and those including a synchronous generator or using solid-state devices for switching off capacitors and inductors are known as active compensation. Therefore, it can be said that power compensators depending on their structure and compartments can implement power flow regulation, reasonably controlling line's active power and reactive power, improving the transmission capacity of power system; also, improving the system voltage stability, the damping of the system and the power angle stability.

Apart from compensating the power in MV networks, protecting them against faults, overload, overvoltage, and short circuits is very critical. Short circuits can severely damage the utilised facilities in the network, especially those utilities that are located in the path of the short circuit. The series devices are prone to get damaged within a short circuit because they have to tolerate a massive fault current (up to 20 times) passing through them. Conclusively, protecting the series compensators due to their sensitive location against a fault is very critical.

In terms of protecting the series devices, the protection mechanism needs to be very fast to limit or cut off the current before it exceeds the device's maximum withstanding current. In addition, the used facilities have to be able to absorb the energy and also release it after their action. The protection devices also have to be able to tolerate a high current and a great arc value depending on their structure.

This chapter presents a review and comparison of the most recent power compensators. The protections schemes used for series compensators are analysed/evaluated and a new protection mechanism is introduced.

2.2 POWER FLOW AND VOLTAGE CONTROL BY COMPENSATORS

Distributed generation (DG) systems such as Combined Heat and Power (CHP) units, Photovoltaic (PV) systems and wind power generation systems are on the rise due to the increase of the load demand. These facilities can compensate the required power during the peak time and then can be separated from the grid while they are not needed.

However, the increase of distributed generation systems has several side effects which have been intensively studied, including reverse power flows and voltage rises in power distribution networks [1]. Indeed, DGs have a great influence on distribution network stability, reliability and performance, which eventually restricts the DG penetration level. Furthermore, the penetration of DGs has also an impact on the amplitude and characteristics of the fault current depending on the network configuration [1].

The power quality, voltage stability and power flow in distribution networks and transmission lines have been drawn attention in recent years due to the increasing load demand and reactive power consumption. It could be said that the voltage control is one of the most used methods for enhancing the stability, reliability and power quality of the grid, with plenty of research activity in this area, finding the optimal, cost effective, fast response and simple method in order to achieve the mentioned objectives [2].

Different methods have been used for mitigating the voltage distortion and to enhance the power quality and reliability of networks such as

improving the voltage profile, power flow control, voltage control, reactive power control etc. [1]-[3].

As mentioned before, the controlling voltage/VAR solution, e.g. Volt-VAR Control or VVC which refers to the process of managing voltage levels and reactive power (VAR) throughout the power distribution systems, is one of the conventional and most cost effective methods to enhance the voltage profile and power flow in networks. Power compensators due to their abilities in controlling the voltage can be very useful for improving the voltage stability. Unified Power Flow Controller (UPFC), Static Var compensator (SVC), Static Synchronous Compensator (STATCOM), Static synchronous series compensator (SSSC), shunt capacitors bank (fixed or CBs), on-load tap changer (OLTC), as well as the Back to Back Voltage control Converters (B2B-VSC) are of those facilities using this solution to control the voltage in the current networks [2].

A soft open point (SOP) is defined as a device, which creates an interconnection among feeders in place of normally open points (NOPs). The aim of using a SOP is to transmit the active/reactive power or regulate voltage. A voltage source converter, SSSC, STATCOM, or UPFC are of could be used in a SOP [3]-[6].

In comparison with conventional VAR devices such as a SVC, the SOP devices are more accurate, with a quicker response and more controllability. A coordinated VVC method based on SOP has been proposed in [7] that presents how to eliminate the voltage distortion and the operation cost by using VAR devices and VSC-based systems.

The next sections explain in more detail some of the recent technologies of power compensators in the transmission systems including a comparison of the different power compensators.

2.2.1 Combined Series-Shunt/Series Compensation Technologies

A series compensation is an important method to improve the grid voltage for increasing the power transfer capacity and controllability of the power delivery of networks in high transmission lines.

Voltage sags are of the remarkable industrial concerns in power networks. Faults in the network, a large motor starting, and heavy loads are some of the events will cause a voltage sag in a system. Using a series compensator is a conventional way for controlling the voltage to prevent the voltage sag happening in the grid.

There are different types of series compensators that use the different methods to control the voltage and VAR. Thyristor-controlled series capacitor (TCSC) and static synchronous series compensator (SSSC) use the equivalent reactance changing method for controlling the voltage. Phase shift transformer (PST) by controlling the phase angle improves the system stability [8]. However, some of series compensators such as sen transformer (ST) [9], rotary power flow controller (RPFC) [10] employing both magnitude and phase angle for the voltage control are based on mechanical on-load taps [11]-[14] and rotary transformers as well as special driving systems [15]-[17], respectively. Moreover, by using a combination of thyristor-converters and especially a winding-configured transformer one can build a series compensator capable of adjusting both magnitude and phase angle similar to ST and RPFC to control and inject the voltage. However, in spite of them, it does have their limitations such as being slow, capacity restricts. Also, it benefits of power semiconductor

advantages such as faster operation, frequent regulations and wide range of phase angle regulation for voltage injection [18].

2.2.2 UPFC (Unified power flow controller)

The UPFC is one of the most used devices among other FACTS facilities due to its capability of controlling both active and reactive power and improving the stability of system makes it a proper choice for being used in transmission lines [19]. However, UPFC could have an impact on the admittance seen by an impedance relay or distance relay during power swing [20]. That can cause a wrong or a lately trip.

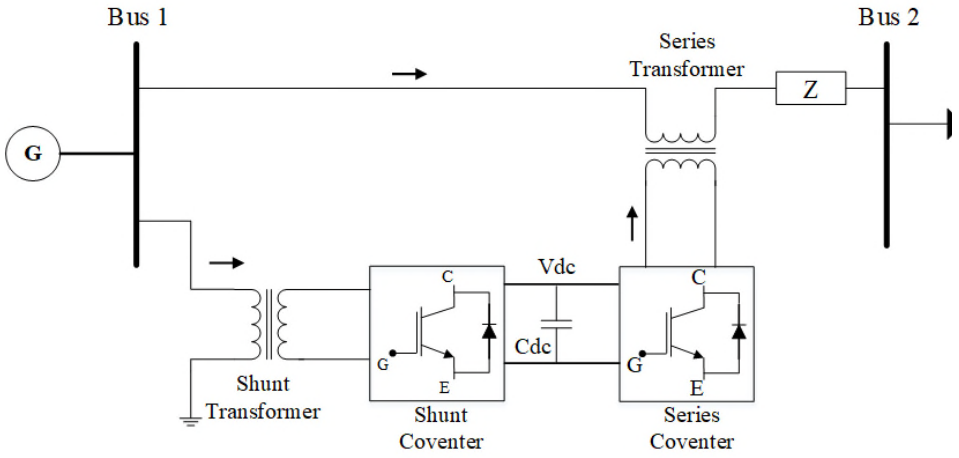

Figure 2.1: Configuration of UPFC: shunt and series converters are on substation and ending sides respectively

The most important aim of using the UPFC (see, Fig. 2.1) is controlling both active and reactive powers of the network. In this regard, the phase angle, Voltage and impedance of system are adjusted and optimised for achieving to this goal. Several control functions such as series or reactive compensations and phase shifting can be employed for this objective, and in this way boosting, e.g. series connection, and exciting transformers are used for injecting the voltage and reactive current, respectively. The AC

to DC voltage source converters are commonly used in a back to back structure with a DC capacitor for making a UPFC [21].

Despite its benefits for optimizing and managing the power in the network the UPFC has a complex structure. Thus, designing a UPFC creates several challenges in its power electronics section and also affects the power system. Besides, the ways of protection and controlling them shall be mainly and critically investigated and considered [22]. In the recent years it has been illustrated that the installation location of a UPFC has a great effect on its overall performance [23].

One of UPFC advantages is its capability in controlling the power flow even during the fault conditions. In fact, the UPFC ability in quelling or relieving the network disturbances by controlling current, voltage and, hereby, power flow could be considered for more studying about its effects on different system situations such as fault conditions, and/or even faster recovery of system to its normal condition after the fault [24].

2.2.3 Static Synchronous Series Compensator (SSSC)

A SSSC (see, Fig 2.2), also known as a series STATCOM, is a controllable voltage source that by employing a voltage-source converter (VSC) controls magnitude and phase of an injected voltage irrespective of the current in series with line. In fact, by inducing both capacitive and inductive voltage is capable of affecting the active and reactive power flow by either increasing or decreasing the reactive voltage/flow on the line. [25]-[28]

A SSSC can be used to improve the stability and damped out the oscillations. The subsynchronous resonance due to the series capacitor

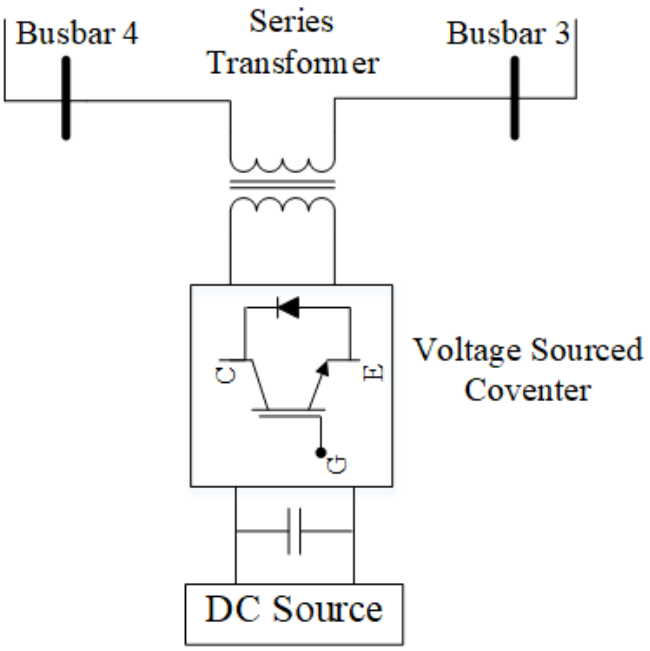

Figure 2.2: A Schematic diagram of the SSSC

could be diminished by using the SSSC. Consequently, the subsynchronous oscillation will be damped out [29], [30]. In addition to the mentioned applications for the SSSC, in the recent years a lot of papers have studied the SSSC in networks in order to ease the simulation and analysing the SSSC performance in the network [31]-[33]. Some examples include presenting an energy function of the SSSC [34] and considering the dynamic respond of the SSSC by using a fuzzy controller [35].

Other applications of the SSSC that have been studied in recent years are: controlling the power flow by using the SSSC in a distribution network [36], control the voltage stability and the power flow in offshore wind plants [37], combining the distribution SSSC (D-SSSC) with fault current limiter (FCL) devices in distribution networks in order to limit the short-circuit as well as control the power flow [38].

2.2.4 Back to Back System

In recent years, the Back to Back (B2B) (see, Fig 2.3) systems have received a great attention due to their ability of improving the full power flow controllability and limitation. Conventional HVDC systems, which employ thyristor converters, are utilised for either a coupled asynchronous network or a power transmission line over long distances. However, they are unable of controlling the reactive power and need a space for filters in order to mitigate the harmonic distortion [39].

B2B-VSCs can be used in synchronous networks in addition to synchronous network interconnections and back-to-back AC system linking [39]. In addition, they are capable of controlling both the reactive and active powers independently, power flow balancing, increasing the transmission capability, operating as two STATCOMS, as well as supporting a weak AC system or even a passive network.

In terms of the VSC-B2B structure, it consists of two converters with a short DC line between them that allows the system to interconnect two AC grids with either the same or a different frequency. The VSC-B2B system employs either a pulse-width modulation (PWM) strategy or a multi-bridge topology for both the rectifier and inverter components due to its symmetric converter configurations [39]-[44]. Studies on VSC-B2B

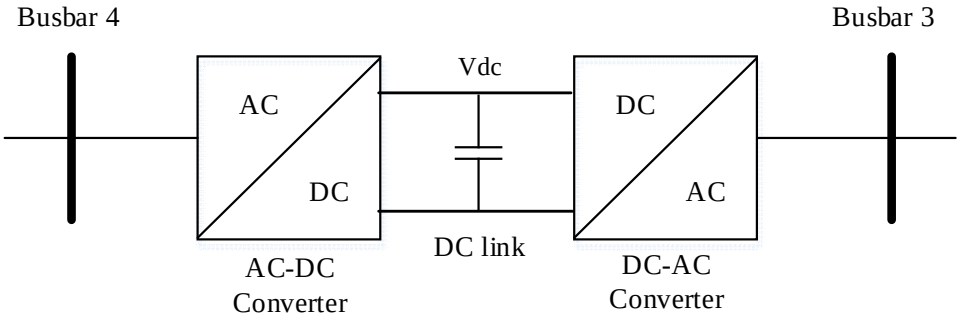

Figure 2.3: A Schematic of the Back to Back Coveter system

include modelling [45]-[47], control [48], protection [49], [50], application [50], [51], reliability and evaluation [52]-[54], power transfer into the modular multilevel converter (MMC) [55] and multiterminal VSC-B2B system [56], [57].

The B2B static synchronous compensator (B2B STATCOM), which is considered as a VSC-B2B system without the long DC transmission [58], in comparison with the conventional VSC-HVDC system has an asymmetrical structure. In fact, the rectifier using the PWM technology controls active and reactive powers and the inverter controls the reactive power by using the multi-pulse technology. Therefore, little space, low cost, less switching loss, and no harmonic frequency in the multi-pulse converter are of B2B STATCOM advantages over the VSC-HVDC [40]-[59]. Some researches on B2B STATCOM features have been conducted such as increasing the transmissibility of a line and the voltage stability [60]-[62], utilising the B2B STATCOM as a transfer switch [63], and for connecting a wind turbine to the grid [64].

Furthermore, other back to back technologies and topologies which in recent years have been studied and proposed for different purposes are medium voltage B2B topologies [65], [66], B2B converters [67], [68] could be used in distribution networks and microgrid systems, respectively.

2.3 COMPARISON BETWEEN A B2B VSC-LINK AND A SSSC

In this section, the SSSC is specifically compared to the B2B VSC-LINK to prove its efficiency in an MV network where B2B VSC-LINK has usually been used. Then, a throughout comparison between different types of power compensators with SSSC has been presented.

2.3.1 A B2B VSC-LINK and a SSSC

For these comparison studies, the network topology shown in Fig 2.4 is selected as the target system. Feeder 1 has 3 load groups evenly distributed along the 5 km cable and Feeder 2 has 3 load groups evenly distributed along the 10 km cable. The resistance and inductance of the cables are 0.06 ohm/km and 0.134 mH/km. A power electronic based device, B2B VSC - link or SSSC, is implemented between busbar 3 and 4 as the connection at the ends of two adjacent networks. The following extreme case is selected to evaluate the compensating performance of both methods: Feeder 2 is heavily loaded, 17 MW with the power factor of 0.98, and Feeder 1 is lightly loaded, 1 MW load with the same power

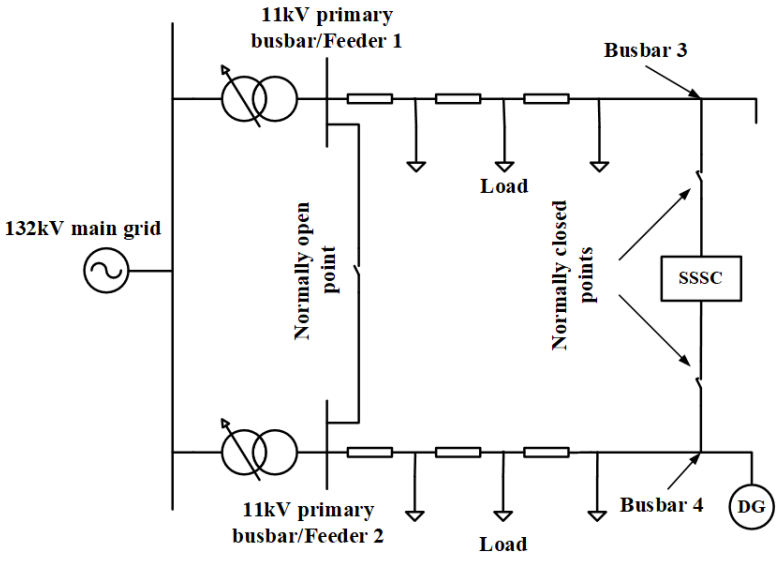

Figure 2.4: A schematic of the case study

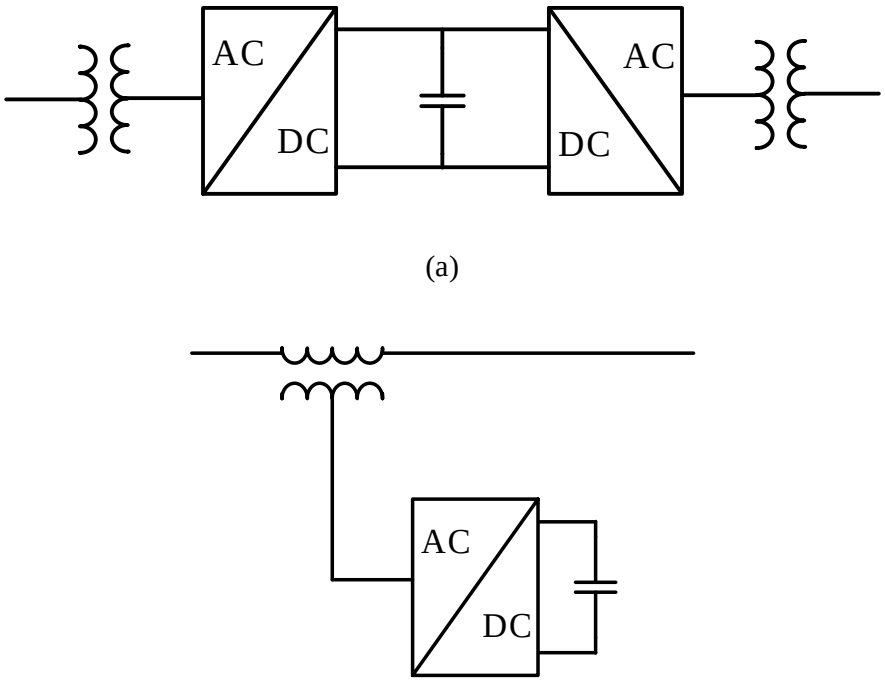

Figure 2.5: a) A schematic of B2B VSC b) A schematic of SSSC

factor. In this case, ideally a load of 8 MW has to be transferred from Feeder 2 to Feeder 1 to balance the system.

For the B2B VSC link (Fig. 2.5(a)), two three-phase 8 MW, 11 kV to 690 V transformers are used for implementing the device. To transfer the active power of 8 MW from one feeder to the other, at the converter side 690 V voltage level, the magnitude of current is about 9500 A. The ABB HiPak IGBT Module 5SNE 0800M170100 which has the rating of V_{ce}=1700 V and I_c=800 A' is selected for building the converters. Considering 100% current margin, the converter will be 2-level and consist of 144 modules.

The situation for an SSSC is different (Fig. 2.5(b)); the SSSC is a partially-rated device which by injecting a voltage orthogonal to the current can manipulate the power flow. The required injecting voltage is

determined by the network, in this study a 690 V converter is more than sufficient to control the power flow. The current flowing through the SSSC is much less than that in a fully-rated device like the B2B VSC - link. A three-phase 600 kVA, 2000 V to 2000 V transformer is used for implementing the device. When transferring the active power of 8 MW, the converter is at the maximum operating point and its output current magnitude is about 600 A. Therefore, with 100% current margin, two IGBT modules for each arm and 12 modules in total are sufficient.

With compensation in the extreme case, the results are shown in Fig. 2.6. Before t=1 s, the two networks are operated separately and the voltage at the end of the heavily-loaded Feeder 2 is below the lower boundary of 0.94 p.u. At t=1 s when the B2B VSC - link or SSSC is enabled, the voltage at the end of Feeder 2 rises meanwhile the voltage at the end of Feeder 1 drops because of the 8 MW active power flows from Feeder 1 to Feeder 2. The voltages are within the limits and the B2B VSC - link gives higher voltage amplitudes because the converters not only transfer the active power but also compensate the reactive power to both feeders.

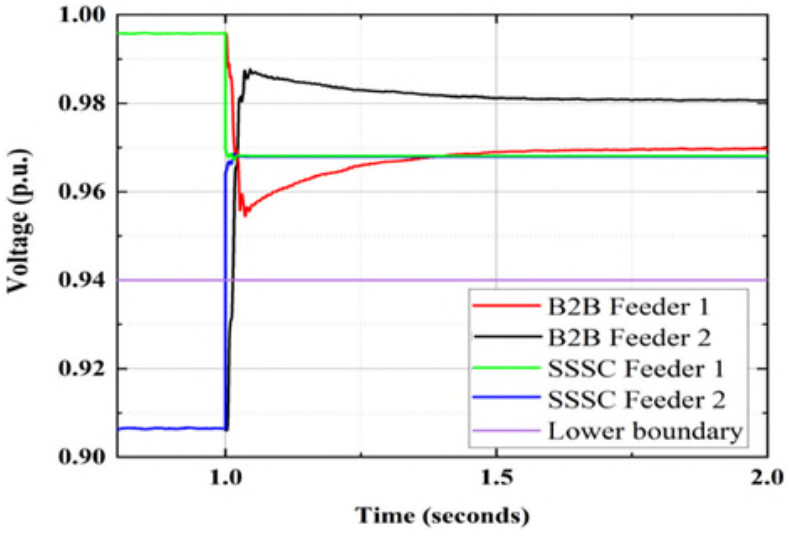

Figure 2.6: Voltage magnitudes at each feeder end before and after compensation by SSSC and B2B VSC - link

In terms of power losses, when an active power of 1 MW to 8 MW is transferred, the power losses of the B2B VSC - link and SSSC are calculated by simulation and shown in Fig. 2.7 and 2.8. The power losses on filters and transformers are assumed to be approximately 1.5% and 1.2%, respectively [71-73]. The device loss consists of the IGBT and diode conduction losses, the IGBT turn on and off losses and the diode reverse recovery loss. In the simulation, the junction temperature is assumed to be at 125 ^{o}C. Thus, the losses are functions of the current. The calculation is shown as below:

$$E_{total} = \int_0^1 \left(v_{ce} \cdot i_c + v_f \cdot i_f \right) + \sum e_{on} + \sum e_{off} + \sum e_{rec} \tag{2.1}$$

where $v_{ce}, v_f, e_{on}, e_{off}$ and e_{rec} are the IGBT on-state voltage, diode forward voltage, IGBT turn on energy loss, turn off energy loss and the diode reverse recovery energy. Currents i_c and i_f are measured in simulation and the functions are obtained by curve fitting the characteristic plots from the product datasheets [90].

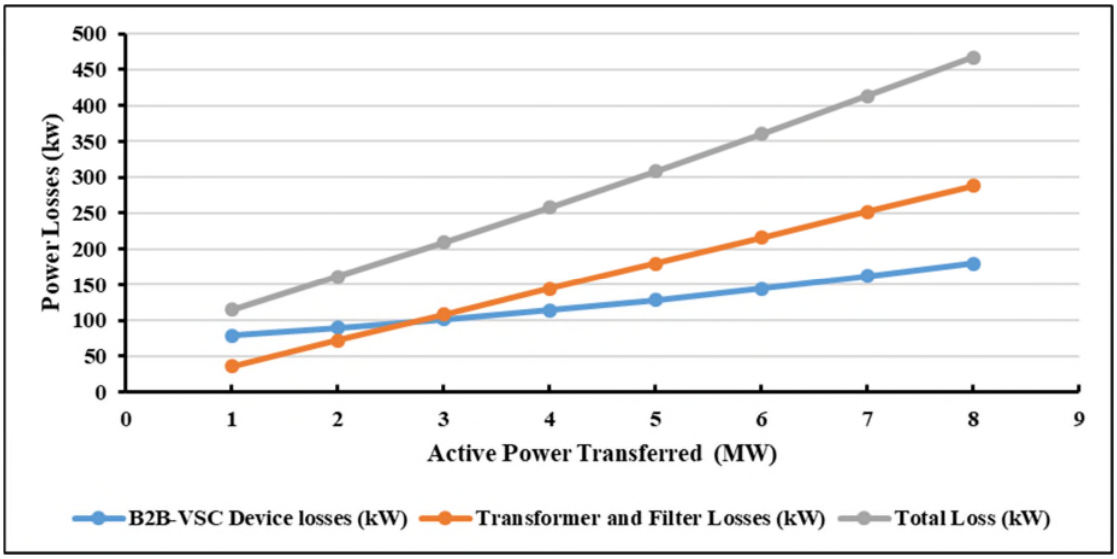

Figure 2.7: Power losses of B2B VSC - link

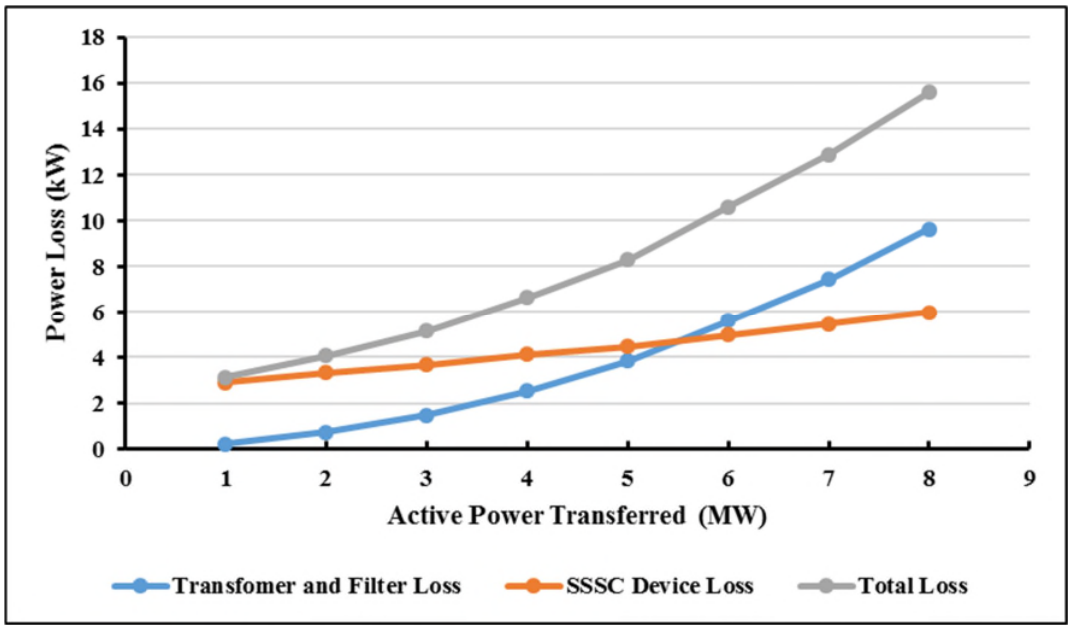

Figure 2.8: Power losses of SSSC

As shown in Figures 2.7 and 2.8, the power loss of SSSC is approximately 30 times lower compared to that of the B2B VSC link in all circumstances because it has significantly lower current rating. Thus, using an SSSC instead of a B2B VSC for power flow control in MV networks is potentially very attractive.

2.3.2 Disadvantages of Series Compensators

Apart from their advantages such as increasing power transfer capability, system stability improvement, voltage regulation improvement, load division between parallel circuits, damping effect [39], they have some drawbacks.

A series compensation by using the series capacitors intends to reduce the series inductive reactance amount of the line in order to enhance the network power flow by increase the power transfer capability, reduction in power angle and improving the maximum loading capability. That will improve the system stability and the voltage regulation as well as the

damping effect. But, series capacitor increases level of fault currents by decreasing the line reactance. Also, the possibility of the sub-synchronous resonance phenomena, ferro-resonance phenomena and maloperation of distance relays will rise. Moreover, due to the installation of protective devises and circuit breaker/ isolator and control circuit for series compensation, the cost of installation will increase as well. [25, 74-77]

2.3.3 Comparison between Different Compensator Systems

In table 2.1, an overall view of primary conventional FACTS devices used in transmission or distribution networks is demonstrated. From tables 2.2 and 2.3, a comparison between various FACTS devices has been conducted that shows their performance, advantages and disadvantages in comparison with each other. FACTS devices are more expensive than conventional compensators, tables 2.4 and 2.5, but their performance and effectiveness is remarkably higher in power/load flow, and voltage control. Regarding the FACTS devices, combined ones such as a UPFC have a strong influence on the network performance such as improving the voltage profile, power flow control, and damping out oscillation but because the series part of these devices such as a SSSC is directly connected to the grid so during the fault current they are very vulnerable. Tables 2.6 to 2.8 show a comparison between HVDC and FACTS devices as it is obvious the HVDC system has more efficiency than different kinds of FACTS, but its cost and losses are significantly higher than FACTS. Thus, using them at most cases is not cost-effective and reasonable.

Table 2.1: Overview of major FACTS-Devices [39]

	Conventional (Switched)	**FACTS-Devices (fast, static)**	
	R, L, C, Transformer	**Thyristorvalve**	**Voltage Source Converter (VSC)**
Shunt-Devices	Switched Shunt-Compensation (L,C)	Static Var Compensator (SVC)	Static Synchronous Compensator (STATCOM)
Series-Devices	(Switched) Series-Compensation (L,C)	Thyristor Controlled / Protected Series Compensator (TCSC / TPSC)	Static Synchronous Series Compensator (SSSC)
Shunt & Series-Devices	Phase Shifting Transformer	Dynamic Power Flow Controller (DPFC)	Unified / Interline Power Flow Controller (UPFC/ IPFC)
Shunt & Series-Devices		HVDC Back to Back (HVDC B2B)	HVDC VSC Back to Back (HVDC VSC B2B)
Shunt-Devices: Q-Compensation, Voltage Control, Stability Improvement, Power Quality Series-Devices: Q-Compensation, Stability Improvement, Power Quality, Short Circuit Limitation Shunt+Series: Power Flow Control			

Table 2.3: Examples of use for FACTS [78]

Subject	Problem	Corrective action	FACTS
Voltage limits	Low Voltage at heavy load	Supply reactive power	SVC, STATCOM
		Reduce line reactance	TCSC
	High voltage at low load	Absorb reactive power	SVC, STATCOM
	High voltage following an outage	Absorb reactive power, prevent overload	SVC, STATCOM
	Low voltage following at outage	Supply reactive power, prevent overload	SVC, STATCOM
Thermal limits	Transmission circuit overload	Increase transmission capacity	TCSC, SSSC, UPFC
Load flow	Power distribution on parallel lines	Adjust line reactance	TCSC, SSSC
		Adjust phase angle	UPFC, SSSC, PAR
	Load flow reversal	Adjust phase angle	UPFC, SSSC, PAR
Short circuit power	High short circuit current	Limitation of short circuit current	TCSC, UPFC
Stability	Limited transmission power	Decrease line impedance	TCSC, UPFC

Table 2.4: Investment cost of asymmetric operation of three 400 kV, 150 km lines, using Conventional devices [79]

Total Power, P=2020MW			
	Q (Mvar)	**Unit cost ($CAN/kVA)**	**Total cost (M$CAN)**
Series compensation	201	35	7.0
Shunt compensation	146	35	5.1
Total cost (M$CAN)			12.1

Table 2.5: Investment cost of asymmetric operation of three 400 kV, 150 km lines, using FACTS devices [79]

Total Power, P=2020MW			
	Q (Mvar)	**Unit cost ($CAN/kVA)**	**Total cost (M$CAN)**
Series compensation	282	100	20.1
Shunt compensation	146	100	14.6
Total cost (M$CAN)			34.7

Table 2.6: FACTS and HVDC: Overview of Functions [27]

Principle	**Devices**	**Impact on System Performance**		
		Load Flow	**Stability**	**Voltage Quality**
Variation of the line impedance Series compensation	FSC (fixed series compensation) TPSC (thyristor protected series compensation) TCSC (thyristor controlled series compensation)	• • ••	••• ••• •••	• • •
Voltage Control Shunt compensation	MSC/R (mechanically switched capacitor/ reactor) SVC (static VAr compensator) STATCOM (static synchronous compensator)	∘ ∘ ∘	• •• ••	•• ••• •••
Load-flow control	HVDC – B2B, LDT HVDC VSC UPFC (unified power flow controller)	••• ••	••• •••	••• •••
Source: ©Copyright 2012 Siemens Energy, Inc. All right reserved. Influence (based on studies and practical experience): ∘, No or low; •, small; ••, medium; ••• strong.				

Table 2.7: Comparison of Power Transmission Using B2B VSC HVDC and FACTS facilities [80]

	B2B VSC HVDC	**FACTS facilities**
Power Control: active	Yes	Yes
Power Control: reactive	Yes	Dependent
Grid interconnections	Any	Synchr.
Losses	Medium+	Low+
Power oscillation damping	Yes	Possible
Power reversal	Fast	Fast
Social implications	Low	Low
Cost	High	Medium

Table 2.8: B2B VSC 2 terminals / STATCOM & SSSC cost comparison [81]

No	Throughout-MW	B2B VSC HVDC 2 terminals Cost (Million $)	FACTS Cost (Million $)
1	200	40-50	5-10
2	500	75-100	10-20
3	1000	120-170	20-30
4	2000	200-300	30-50

Finally, it can be said that series/combined series-shunt FACTS systems, such as a SSSC and a UPFC, are the most suitable choices for being utilised in the networks because of their feature such as cost, losses, efficiency, and also their influence on enhancing the voltage stability and the power flow control are aggregately more reasonable and cost-effective, but their main drawback is their series component that is very vulnerable to the short circuit. Giving the aforementioned vulnerability, it is important to understand how to protect them against faults. The next section presents a review on major topologies of combined series-shunt FACTS and series compensators, and then effective topologies to protect them against a fault has been carried out.

2.4 PROTECTION SCHEMES

In recent years, power semiconductor devices have been applied expansively in circuit breakers to improve or expedite the protection speed up to just hundreds of microseconds. Also, they are practically controlled switches [82]. The object called a solid-state circuit breaker (SSCB), is the CB with pure semiconductor devices. Furthermore, as there is no mechanical compartment, neither contact erosion, electric arc, nor strong mechanical shake exists. However, on the other hand, SSCBs present several disadvantages: (a) the unignorable on-state resistance means significant power loss, which could cause critical heat and lower system efficiency; (b) semiconductors are sensitive to the transient over-voltage and heat-causing over-currents, which makes them a natural weakness of the whole electric system and needs more protection technology; (c) the costs and physical volume of semiconductor devices is no doubt a limitation for further development; (d) bidirectional semiconductor devices are needed for bidirectional applications (e.g., AC or power regeneration fields), thus doubling the number of devices, redoubling the costs and complexity of control, and reducing reliability. In future, by applying next-generation wide bandgap devices e.g., silicon carbide (SiC) or gallium nitride (GaN), the performance of SSCBs may be improved because of lower power loss, higher junction temperature, and better avalanche breakdown capability and so on.

Another main category of CB with semiconductor devices is actually a combination of SSCB and MCB in a proper way to configure a new family, which is named “hybrid circuit breaker” (HCB) .Taking the benefits of both sides, HCBs display lower power losses than SSCBs and higher switching speeds than MCBs [82].

In the following, some of the most recent and utilised SSCBs has been discussed to give a better view of the structure of SSCB. Then, a review on a new protection mechanism has been carried out.

2.4.1 Fast-Breaking Mechanical Devices

Fast mechanical switches (FMSs) are used in a modern mechanical circuit breaker (MCB) which works together with molded-case circuit breakers (MCCB). The FMS could trip and clear faults very fast in hundreds of microseconds (usually within 10 ms), which makes it possible to cut a low-frequency AC current of 50 Hz or 60 Hz before it goes up to the anticipated maximum value [82].

2.4.2 Basic Solid-State/Hybrid Circuit Breakers

As shown in Figure 2.9, a Japanese team introduced a current-limiting circuit breaker (CL-CB) for low-voltage power systems in 1994. The CL-CB consists of high-speed mechanical switch, solid-state switch like a gate turn-off thyristor (GTO), snubber circuit and voltage protection element such as zinc oxide (ZnO) arrester. This is considered a common topology of CL-CB. Eventually, solid-state switches are changing to

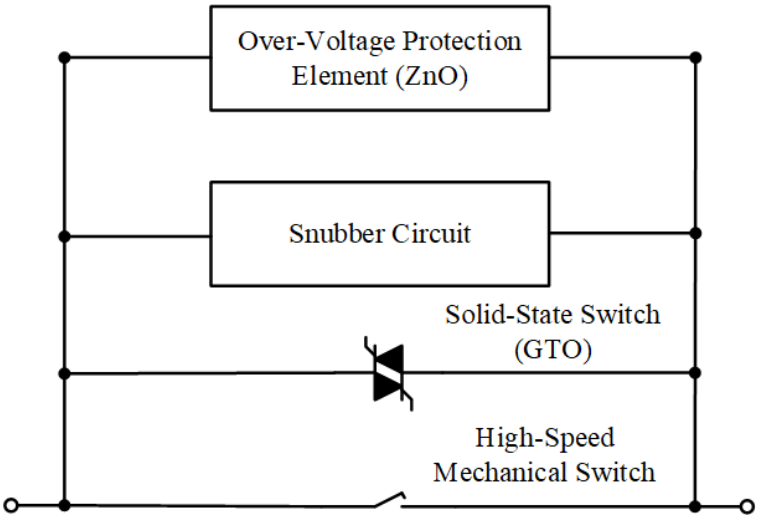

Figure 2.9: An HCB Structure [82]

insulated-gate bipolar transistors (IGBTs) and SiC metal-oxide-semiconductor field-effect transistor (MOSFETs); and mechanical switches are becoming faster and faster [82].

2.4.3 CL-CBs with Ordinary Resistor

A structure of a Hybrid Current Limiting (CL) Circuit Breaker is shown in Figure 2.10. This structure is based on a CL method that has been proposed by the United States Electric Power Research Institute (EPRI) in 1980. By combining fast mechanical switches, diode components, snubber circuits and CL impedances in opposite direction into the old method, this Hybrid CB has been built [82].

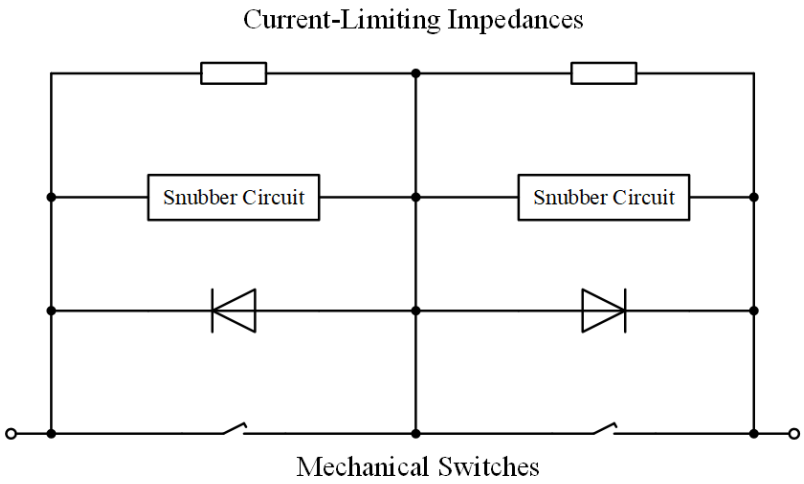

Figure 2.10: Hybrid CL-CB with separated current-limiting path [82]

2.4.4 CL-CBs with Superconductors

High temperature superconductors could be used as CL devices. In 1995, a current limiter was proposed on this basis. With negligible resistance below under a critical temperature, and relatively high resistance above the critical temperature, the current limiting could be achieved automatically and smoothly. Superconductors may be used for power distribution systems which are not sensitive to cost and dimension.

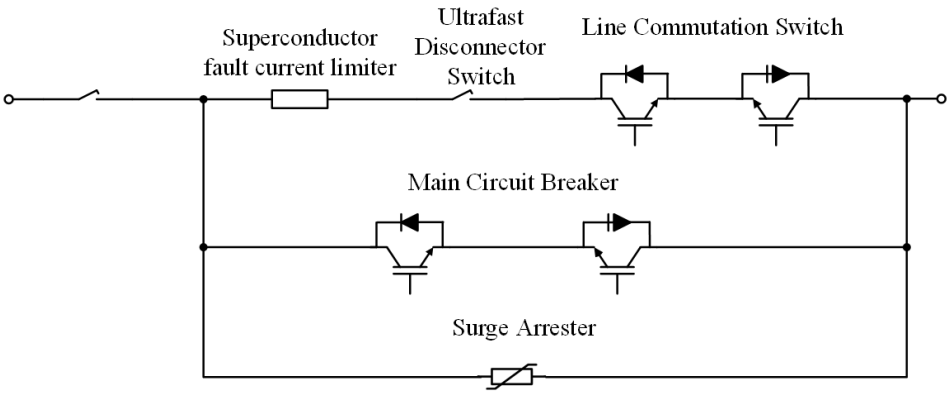

Figure 2.11: A superconducting HCB [82]

2.4.5 CL-CBs with Inductive Components

To limit fault currents, a series-connected inductor is more effective than a paralleled capacitor. If an inductor is added without assistance of semiconductor switches, the impedance of the inductor may cause considerable phase shifts and voltage drops, which results in the bad voltage regulation and higher system losses [82]. A bridge-structured solid-state CL device based on a single inductor working in two different modes is shown in Figure 2.12. In the normal operation, thyristors T1, T2 are off and T3, T4 are on so that the current passes through an inductor from only one direction with negligible effect on an AC power quality, it means the inductor acts in the DC mode. When a fault occurs, T1, T2 are

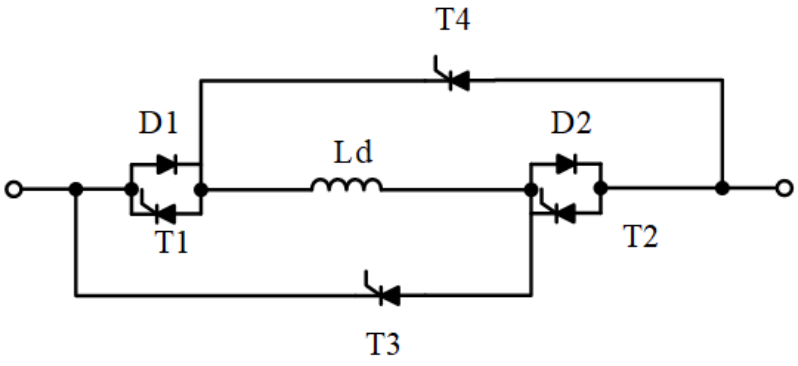

Figure 2.12: A solid-state CL-CB with an AC inductor and a DC inductor [82]

on and T3, T4 are off, the inductor changes from a DC mode to an AC mode to limit the fault current

2.4.6 CL-CB with Semiconductor Power Switches

As shown in Figure 2.13, an SSCB could work as a CL device. This ‘fault-current limiting and interruption device (FCLID)’ has a bi-directional semiconductor switch, like an IGBT or power metal oxide-semiconductor field-effect transistor (MOSFET), resistor-capacitor (RC) snubber circuit, and a voltage varistor. The semiconductor switches could be controlled with pulse-width modulation (PWM) to limit the current. When with a short-circuit condition, the current is limited to a value higher than the nominal current, therefore the power loss will be higher than the nominal input power of the system. This configuration might not work in a CL mode on a long-term basis, and as the power must be absorbed by metal oxide varistor (MOV), then, MOV components with large dimensions are needed. The current could be eliminated by fast switching of the mechanical and semiconductor switches [82].

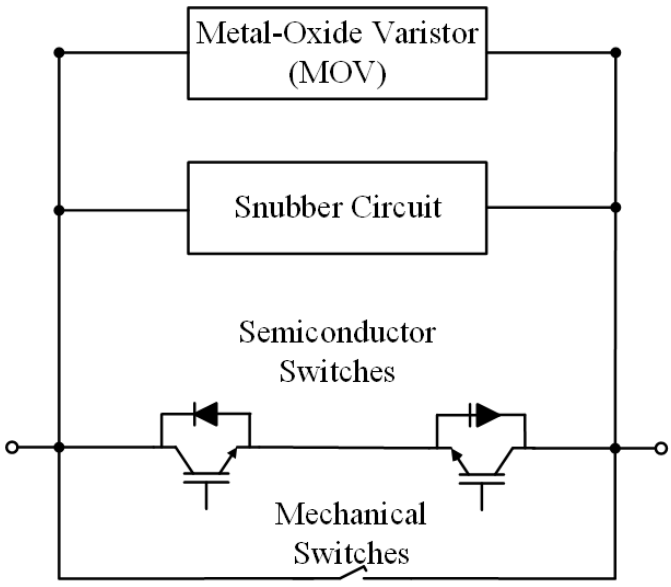

Figure 2.13: A Hybrid CL-CB [82]

2.4.7 MOV- Spark Gap Mechanism

Figure 2.14 shows a MOV-GAP mechanism to protect series capacitors in the network. The operation time of the spark gap and the MOV depending on the rate of devices. It can be from a few microseconds to a few milliseconds. During a fault, first the spark gap and the MOV will act to provide a bypass path for the current until the mechanical circuit breakers will open. Then, the MOV and the spark gap will switch off. However, turning off spark gaps in some cases could be very difficult [83-85].

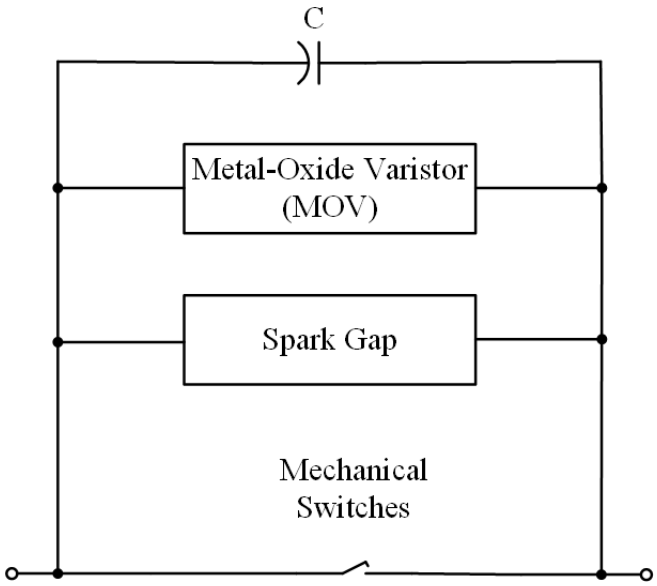

Figure 2.14: A MOV-GAP mechanism

Although, this method does have some disadvantages such as:

1. They require a relatively large voltage to turn on, it can be around 3kV or 4kV [85], [87].
2. Difficult to turn off if current continues to flow after the transient has ended [85].
3. They can be relatively slow to operate (break down electrically and transition through the glow discharge to the arc mode) [87].

4. Their operating time can be up to 2-3 ms in some cases [84]
5. Some spark gaps emit flames and ionized gases during clearing of the AC fault current causing potential fire hazard. Care must be taken never to install spark gaps close to flammable or explosive materials [86].
6. Spark gaps are often unreliable, either failing to strike an arc when needed or failing to turn off afterwards, in the latter case due to material failure or contamination by dust or salt [86].
7. Some spark gaps emit flames and ionized gases during clearing of the AC fault current causing potential fire hazard. Care must be taken never to install spark gaps close to flammable or explosive materials [86].
8. Depending on the relative clamping voltages of the two devices, their separation distance, and the waveform of the impinging surges, the coordination may or may not be effective [86], [87].

2.4.8 Comparing the Protection Mechanisms

Table 2.9 below demonstrates a comparison between different protection topologies.

Table 2.9: Comparison of different protection mechanisms

Categories	Main Components	Advantages	Disadvantages
Fast breaking circuit switches [82],[88]	Fuses	Small size & low cost	Poor maintenance, unclear melting time
	Fast Mechanical Switch	Small size, low power loss	Electric arc with contact erosion, low speed
	Hybrid circuit breakers/Solid-State circuit breakers	Fast, small arcing	Complex structure, relatively high cost
Fault Current Limiter [82], [89]	Switched superconductor devices	Auto-limiting with resistive current	High cost, huge size
	PWM control	Simple structure, resistive current	High power dissipation of MOV
	Gate voltage control	Simple structure, resistive current	High power dissipation of semiconductors
	Controlled bridge with inductor	Controllable current, no additional heat	high current harmonics with thyristor
	Static synchronous series compensators	No additional heat, controllable current, low total harmonic distortion	Complex structure, capacitor charging issues
MOV-Gap Mechanism [83-85]	MOV and spark gap	Small, low cost, relatively fast, no harmonics, no power losses	Coordinating between MOV and Gap, high initial voltage, difficult turning-off process in some cases
Proposed Thyristor Crowbar-Varistor Mechanism [Chapter 3]	**Thyristor and MOV**	**Small, low cost, very fast, simple coordinating, simple structure, no arc issue, no power loss, no harmonics**	**Thyristor Temperature during the Surge condition in terms of the improper choice**

2.5 DC OFFSET

The DC-offset (also called the DC-decay) is simply seen in the waveform of Fig. 2.15. The DC-offset (also called the transient part) which is purely a result of magnetic fields in the supply network not being able to collapse immediately under fault conditions and are thus subject to a gradually easing off effect. The steady-state current added to the DC-offset. Thus, the fault consists of two portions added together. This current is not symmetrical about the time axis until the DC offset component is zero and is thus called an asymmetrical fault current. It is immediately obvious from this curve that the DC-offset can make the peak value during the first half-cycle higher. It could also make the asymmetrical breaking current higher if this DC-offset has a very high value. Take for example the breaking current at 60 ms in Fig. 2.15, here the current still has a component at this time. The duration of this DC-offset is a function that is called the “system time constant”. The slower this current eases-off, the higher the current will be when it is to be interrupted by the circuit-breaker. A measure of how slowly the current eases-off is called the system time-constant. The higher the time-constant the slower the current eases-off. The slower the current eases-off then the higher the portion of transient current that will be present at the point of current breaking of the circuit breaker. The machines that are connected close to the fault will contribute this additional ac-current. So any machine which has low impedance between it and the fault will contribute AC fault current. The larger the machine, the larger the current contribution [91].

The DC offset could not only decay the turning-off of the thyristors in concern but also cause effects to current transformers including saturation, which in the case of feeding protective relays would be detrimental due to malfunctioning [93]. Estimating the related parameters of the DC

component is very important in simulating the network and determining the relay settings. Analysing the characteristics of the DC component is essential in determining the zero-crossing time of the fault current [94]. This needs to understand another side effect of the DC component, which is to make the symmetrical current to be asymmetrical and increase the current peak [95].

DC offset can delay the zero-crossing of the short circuit current. This is a well-known phenomenon in power transmission networks as the large synchronous generators undergo from sub transients to transients and eventually steady states [96]. This is hardly seen in distribution networks which is far from the large centralised power plants. With the introduction of distributed generation, it has now become questionable whether the DC offset in the short circuit current is still negligible

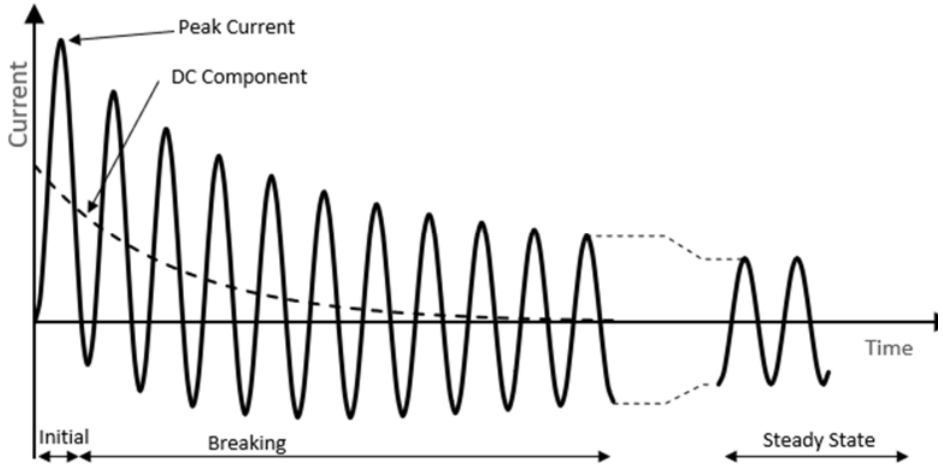

Figure 2.15: A MOV-GAP mechanism [92]

2.6 PHASE CHANGE MATERIAL HEATSINK

Standard heat sinks for the electronics cooling are actually heat exchangers, taking the heat from the electronics, and then transferring it to a fluid, either air or coolant. Phase Change Material (PCM) heat sinks are the only heat sinks that actually act as a temporary sink for heat. They are emerging in the thermal management realm to solve thermal problems in systems where active solutions cannot be used. When there is no place to dissipate the heat generated by electric components, a PCM heat sink is capable of absorbing the generated waste heat [97].

PCMs store thermal energy by changing the phase from solid to liquid. Since the latent heat from melting or freezing is at least 1-2 orders of magnitude higher than the energy stored by the specific heat over a representative 10°C change in temperature. PCM applications in electronics thermal management include [97]:

- Stabilizing temperature during pulsed operation
- Short-term thermal storage, where a suitable heat sink is not available
- Protection from failure during coolant interruptions, when the cooling system is temporarily unavailable

The energy required to transition between solid and liquid phases is known as the latent heat of fusion. Materials with a high latent heat of fusion are able to store a significant amount of heat during a phase transition while maintaining a near constant temperature around the material's melting point. This feature is a great advantageous for electronics cooling applications with transient loading. During transient operation, the thermal energy can be stored in the PCM while the heat is

generated, without the temperature of the source increasing significantly. While the heat source is off, the PCM can refreeze so it is ready to absorb energy during the next heating cycle. This solution works well provided there is enough PCM to store all of the waste heat and the thermal resistance of the PCM heat sink is low enough to handle the required heat flux [97].

The melt temperature and application will dictate the type of PCM that can be used. For most electronics applications, paraffin waxes and non-paraffin organics are a good choice because they are relatively inexpensive and stable through many thermal cycles. For high temperature applications, metals and salts (non-hydrated) can be used [97].

To absorb transient heat, PCMs such as paraffin wax have been appended to commercial modules as part of the heatsink [98]. However, since the PCM is located at a relatively large distance from the semiconductor chip, a large headroom must be considered for the junction temperature in the grid applications targeted. In practice, a much faster PCM response is crucial to contain the chip temperature rise and so it is necessary to integrate the PCM internally in the module [99]. Because phase-change materials are generally poor heat conductors near the phase-change point, this gives rise to a concern regarding possible increase of the internal thermal resistance. The thermal response depends on the amount, geometry and properties of the PCM, and all of these must match the characteristics of the transient energy that has to be absorbed [100].

Grid inverters are increasingly being required to provide grid support duties, some of which will demand short-term overload capability of the power semiconductor modules. [101] has shown that it is possible to

integrate the PCM in a power module to limit the temperature rise and thus allow an overload in these cases.

2.7 CONCLUSION

In this chapter, a comprehensive review on series compensator, shunt compensator and the combined series/shunt compensators as well as B2B-VSC from different aspects such as losses, cost, influence on voltage, power flow, oscillation has been carried out. Then combined/series-based compensators as cost-effective have been investigated in detail. In this way, a review on UPFC, SSSC, and Back to Back devices has also been conducted.

Since the aim of this thesis is proposing a new protection technique to protect the SSSC against the fault, different protection topologies that can be used to protect the static series compensators has been reviewed in order to show their advantages and disadvantages. In fact, the protection scheme is introduced in this thesis will have a greater performance in terms of the protection time to decrease the damage possibility of the SSSC during a short circuit.

Furthermore, a review on PCM materials has been done in order to show the capability of these materials in cooling down the semiconductors. In this thesis, a new heatsink based on the PCM material is introduced to contain the temperature rise of a thyristor during fault as the conventional heatsink is not capable of limiting the thyristor during a short period like a short circuit condition.

Finally, since in this thesis the thyristor and the varistor will be used as fundamental devices in order to construct the protection scheme against a short-circuit, a general look on their structures as well as their characteristics has been carried out in Appendix I.

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3 A FAST-ACTING PROTECTION SCHEME FOR MV SERIES COMPENSATORS

3.1 INTRODUCTION

Low-carbon distributed generation (DG) is being introduced to medium voltage networks, presenting challenges to the control of busbar voltages, branch power flows and operation of relays. To increase the ability of the network to accommodate embedded generation, power electronic compensators could play important roles by adjusting the magnitude and phase angle of the compensating voltage or current. Potential technologies include voltage source converters in different combinations. Figure 3.1 shows a typical medium- voltage (MV) distribution network which is required to accommodate DG. The feeders are usually isolated at the primary busbars, and the further ends are connected only when one of the feeders has lost connection to the supply. In order to accommodate more DG, it is desirable to join the feeders at appropriate positions using controllable devices based on power electronics, such as a static synchronous series compensator (SSSC) as shown in Figure 3.1. Factors such as power quality, power flow, and fault level are often presented as challenges to operating systems with increasing penetration of DG. Some network management techniques to ease this situation are the unified power flow controller (UPFC), static VAR compensator (SVC), soft-open point and transformer on-load tap changers. The UPFC is described as ‘universal’ due to its ability to independently control real and reactive power flow [1]. The series insertion of a voltage, like in an SSSC, is most effective and many studies

have been carried out to find the optimal allocation in terms of costs and dynamic response [2, 3].

With the ever-increasing capacity of DG, fault management will become more challenging, especially the protection of those compensators that use series voltage injection. Mechanical switches are effective, but they are slow. Therefore solid-state circuit breakers (CBs) or other power electronic-based schemes have attracted research attention in recent years involving thyristors, GTOs or IGBTs [3, 4]. However, the high capital cost and large operational power loss have limited their deployment [5, 6]. Furthermore, an increasing number of DGs may cause larger DC offsets during faults which may delay the zero-crossing of the fault current and affect the duties of the power semiconductors [7, 8]. Therefore, estimating the dynamic response is potentially very important when designing a protection scheme [9, 10]. Much of the existing literature focusses on the potential applications of series compensators by considering their cost and efficiency. However, series compensators are inherently vulnerable to short-circuit events, but only a few studies have been conducted regarding the protection of series compensators which

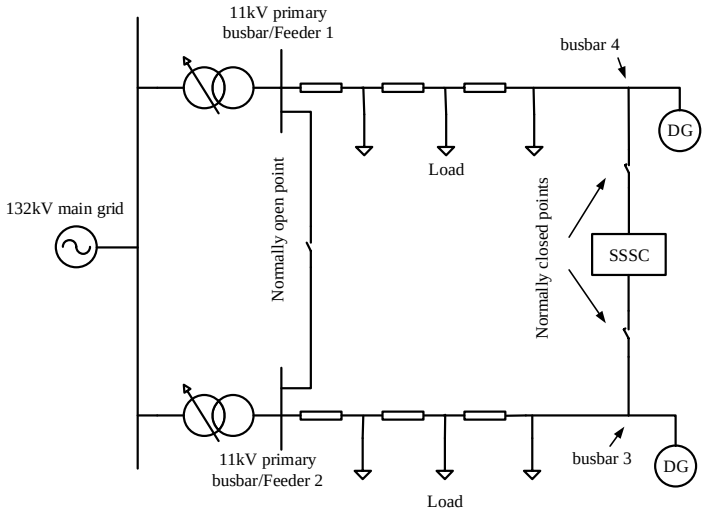

Figure 3.1 : Typical MV network with multiple feeders including SSSC

related either to mitigation of voltage dips [11, 12] or to limit the fault current [13, 14] by using a fault current limiter or different control designs integrated with static series compensators in the network.

3.2 STATIC SYNCHRONOUS SERIES COMPENSATOR

The network topology shown in Figure 3.1 is selected as the target system. Feeder 1 has 3 load groups evenly distributed along the 5 km cable and Feeder 2 has 3 load groups evenly distributed along the 10 km cable. The resistance and inductance of the cables are 0.06 ohm/km and 0.134 mH/km. A SSSC is implemented between busbar 3 and 4 as the connection at the ends of two adjacent networks. The following extreme case is selected to evaluate the compensating performance: Feeder 2 is heavily loaded, 17 MW with the power factor of 0.98, and Feeder 1 is lightly loaded, 1 MW load with the same power factor. As a load of 8 MW has to be transferred from Feeder 2 to Feeder 1 to balance two Feeders.

The SSSC is a partially rated device which by injecting a voltage orthogonal to the current can manipulate the power flow and improve power oscillation damping on power grids, (see Fig. 3.2). The required injection voltage is determined by the network, in this study a 1100 V_{DC} converter is utilised to control the power flow. The ABB HiPak IGBT Module 5SNE 0800M170100 which has the rating of V_{ce}=1700 V and I_c=800 A' is selected for building the converters. A three-phase 600 kVA, 1000 V to 1000 V transformer is used for implementing the device. When transferring the active power of 8 MW, the converter is at the maximum operating point and its output current magnitude is about 730 A. Therefore, under full load conditions, one IGBT module for each arm and 6 modules in total are sufficient. By varying the magnitude Vq of the injected voltage in quadrature with the current, the SSSC acts as a variable reactance compensator, either capacitive or inductive. A low-pass LC filter is utilised to minimise the noise and electromagnetic interference.

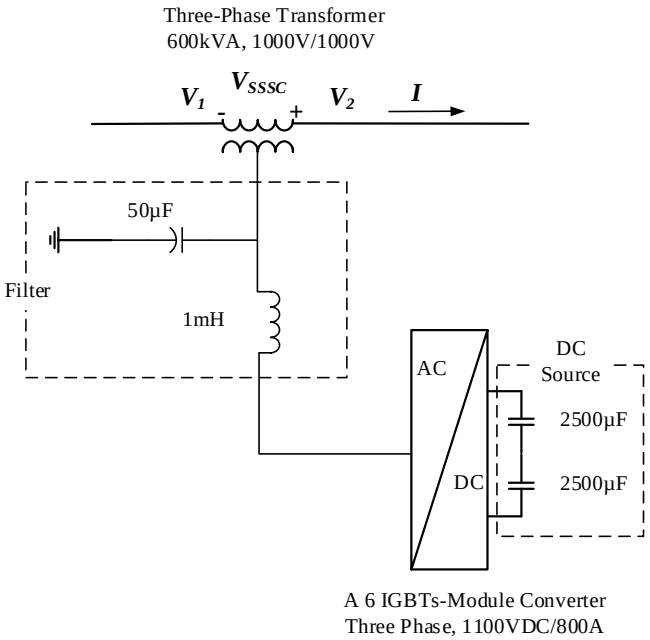

Figure 3.2: A schematic of SSSC

The relevant results for system situations without the SSSC and with using SSSC are presented as follows.

3.2.1 Without the SSSC

In order to show the benefits of using the SSSC, it is assumed that busbars 3 and 4 are connected to each other directly without any interface. In this case, the voltage value of busbars is 0.9656 p.u. (see Fig. 3.3) and the current value is 420 A (see Fig. 3.4). Fig. 3.5 shows the powers are transferred between these busbars which are 7.1 MW and 1.3 MVar. Moreover, Feeder 2 generates 9 MW and 2 MVar (see Fig. 3.6), while Feeder 1 does 8.2 MW and 1.7 MVar (see Fig. 3.7).

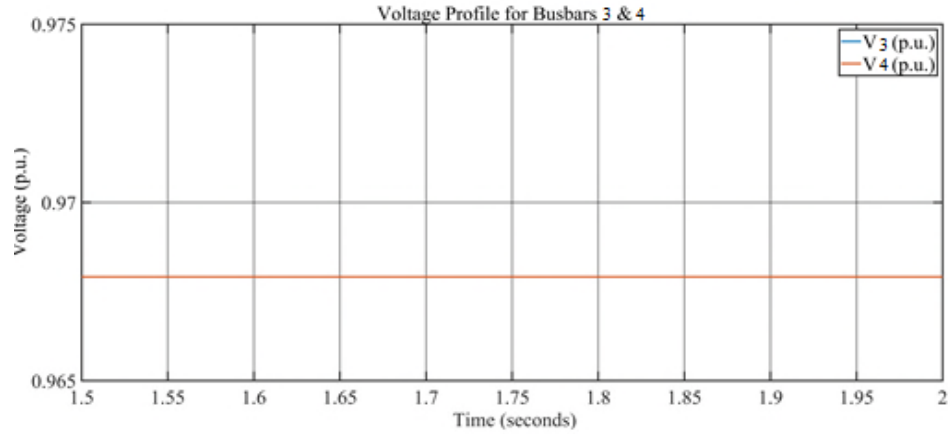

Figure 3.3: The Voltage profile for busbars 3 and 4

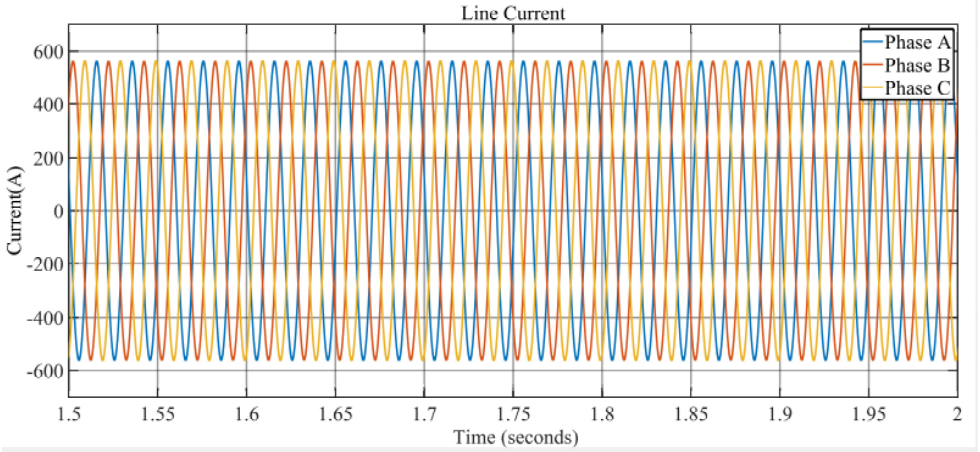

Figure 3.4: The line current

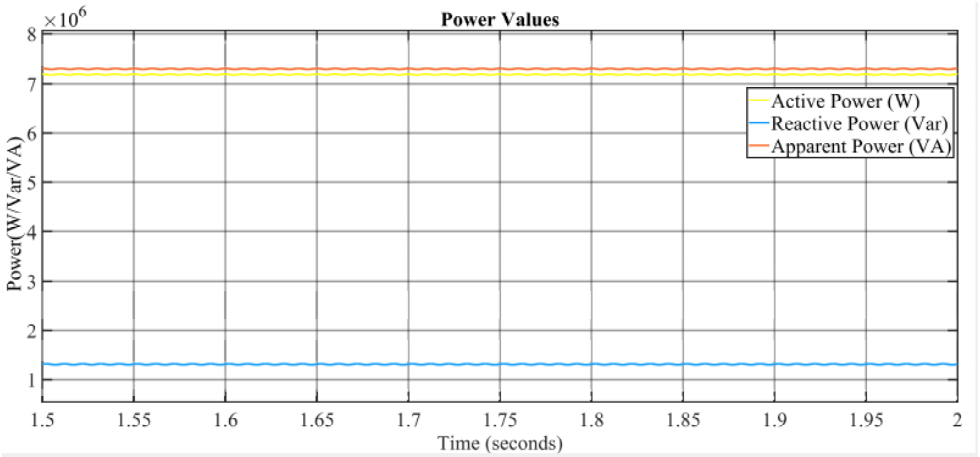

Figure 3.5: The active (Yellow), Reactive (Blue), and Apparent power (Orange)

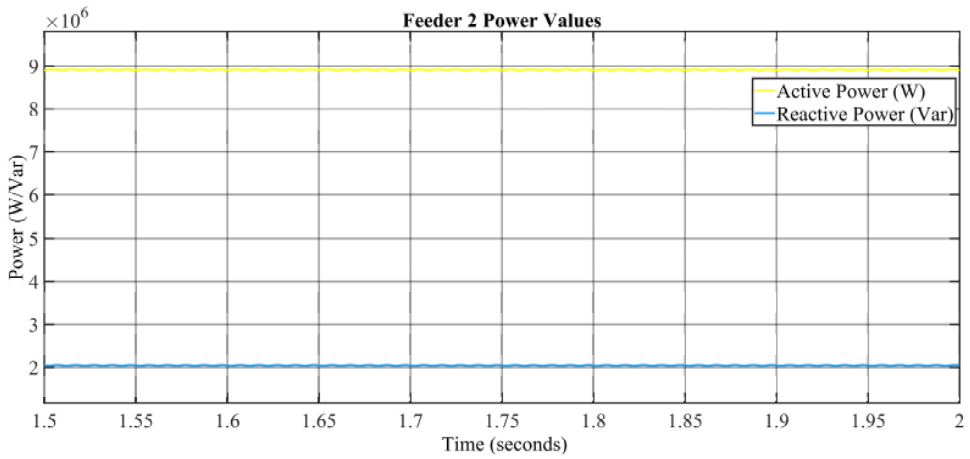

Figure 3.6: The power values for Feeder 2

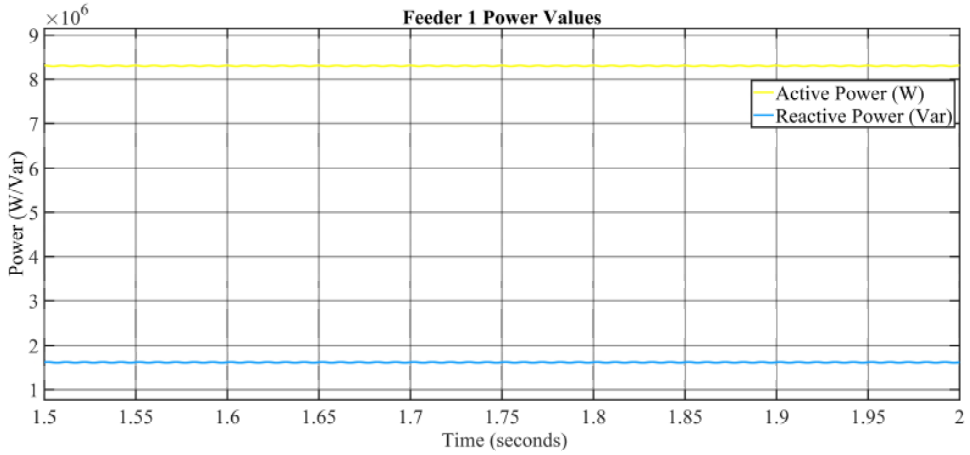

Figure 3.7: The power values for Feeder 1

3.2.2 With using the SSSC

A SSSC is installed between busbars 3 and 4 for a similar network to section A. In this case, the voltage profile for busbars is improved to 0.97 p.u. (Fig. 3.8), and the line current has also increased to 495 A (Fig.3.9). The power transmission and power losses between busbars are amended as the active power is 8.9 MW, while reactive power is decreased to 0.3 MVar which means power losses is reduced (see, Fig. 3.10). Furthermore, the feeder 1's generated active power has rised to 10 MW while that of the feerder 2 has gone down to 7.5 MW (see Fig. 3.11). But, the reactive powers for feeder 1 and 2 are 0.8 Mvar and 2.8 MVar, respectively (see, Fig. 3.12). This means the power transmission in the system has improved.

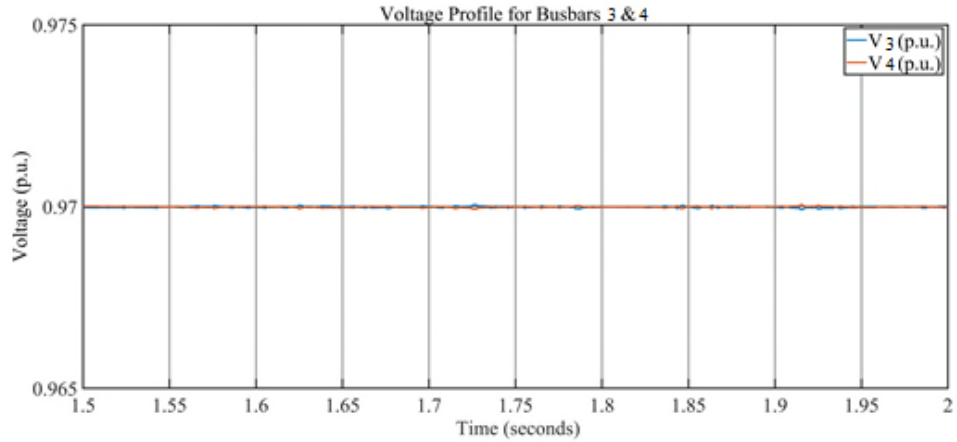

Figure 3.8: The Voltage profile for Busbars 3 and 4

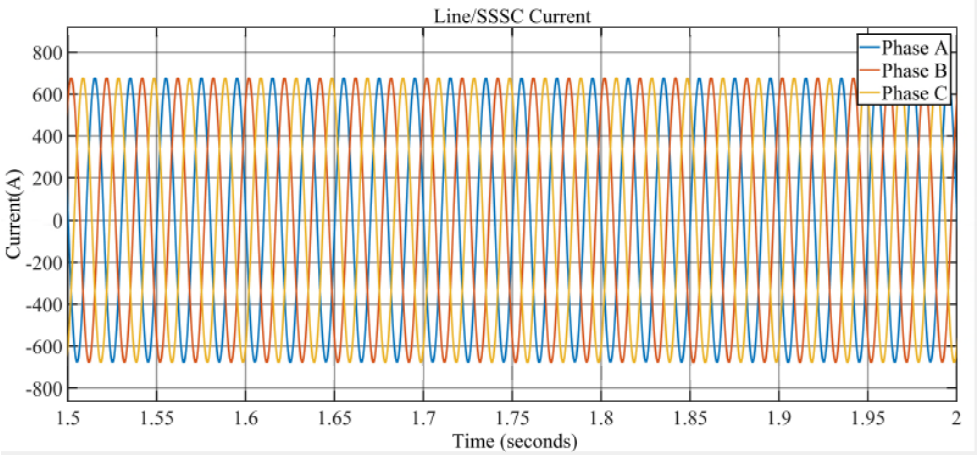

Figure 3.9: The line current

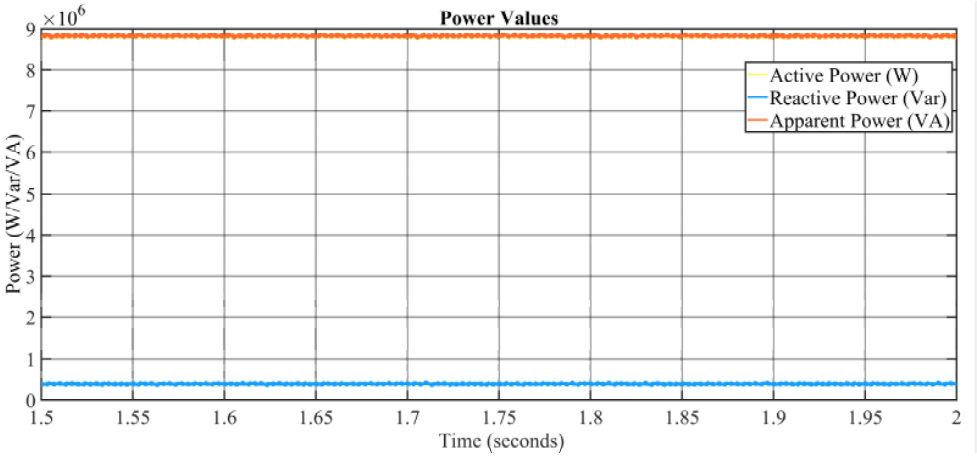

Figure 3.10: The active (Yellow), Reactive (Blue), and Apparent power (Orange)

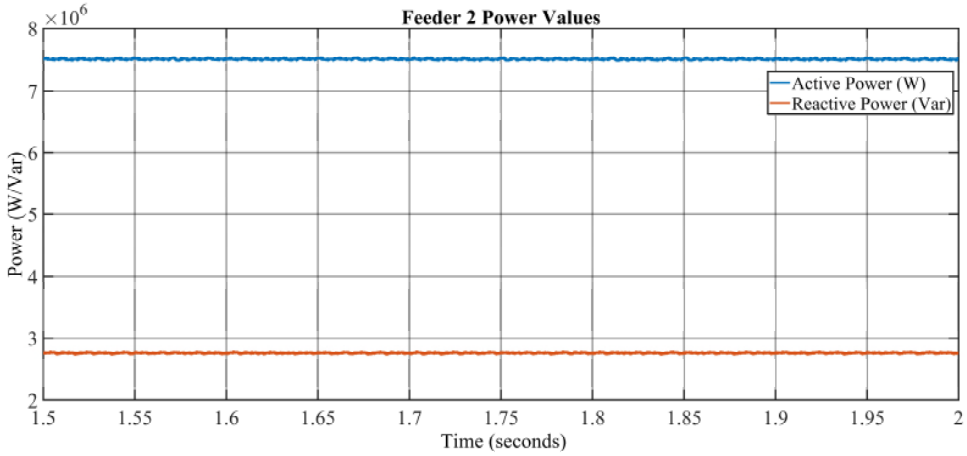

Figure 3.11: The power values for Feeder 2

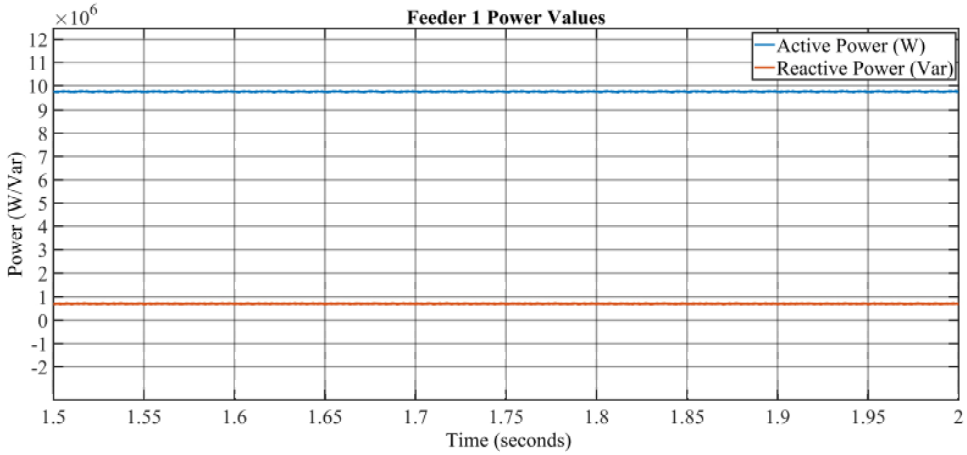

Figure 3.12: The power values for Feeder 1

3.2.3 Closed-Loop Control System

Clarke (αβγ) and Park transformation (dq0) are used in high performance architectures in three phase power system analysis. Current and voltage are represented in terms of space vector which is represented in a stationary reference frame (ABC) or AC quantities. Through the use of the Clarke transformation, the real and imaginary currents can be identified. Then, the Park transformation is used to realize the transformation of those real and imaginary currents from the stationary to the rotating/synchronous reference frame.

There are three modes for this transformation:

- **Variant power - Clarke's original** - The original transformation proposed by Edith Clarke. The γ axis is squashed which makes this output equal to the zero-sequence obtained from the symmetrical component's transformation. This transformation is power variant since the transformation matrix is not unitary.

- **Variant power - uniform** - Adaptation of Clarke's original transformation to keep all axes uniform. Since the γ axis is not squashed, this output is different from the zero sequence of the symmetrical component's transformation. The transformation matrix is not unitary; thus, the power is variant.

- **Invariant power** - Adaptation of Clarke's original transformation to keep all axis uniform while having a unitary transformation matrix. The power computation after this transformation is the same as the computation done before it. Since the γ axis is not squashed, this output is different from the zero sequence of the symmetrical component's transformation.

3.2.4 Clarke Transformation

The Clarke transformation is mathematical transformation employed to simplify the analysis of three-phase circuits. In order to project the three-phases voltages to αβγ reference frame, the invariant power Clarke transformation matrix is utilised as follows:

$$i_{\alpha\beta\gamma}(t) = Ti_{abc}(t) = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{3.1}$$

The projection on γ is zero when the three-phase voltages are balanced.

3.2.5 Dq0 Transformation

The dq0 transformation is a mathematical transformation that rotates the reference frame of three-phase systems in an effort to simplify the analysis of three-phase circuits. In the case of balanced three-phase circuits, application of the dqo transform reduces the three AC quantities to two DC quantities. The park transformation matrix to project the vector to qd0 reference frames is presented as the following equation:

$$i_{qd0}(t) = Ti_{\alpha\beta\gamma}(t) = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \\ i_\gamma(t) \end{bmatrix} \tag{3.2}$$

Therefore, the final dqo transformation matrix for the AC quantities through the Park and Clarke transformation frames where implements a power invariant *a*-phase to *d*-axis alignment will be presented as:

$$i_{qd0}(t) = Ti_{\alpha\beta\gamma}(t) = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{3.3}$$

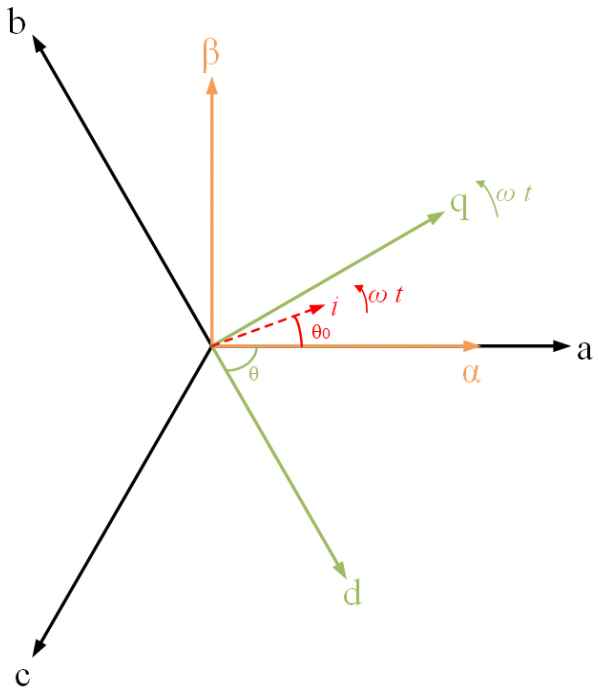

Figure 3.13: Relationship between ABC, qdo and αβ coordinate reference frames

Then, the three-phase active and reactive powers in dq0 reference frame by using the invariant power transformation are obtained as follows:

$$P = \frac{3}{2}(v_d i_d + v_q i_q)$$
$$Q = \frac{3}{2}(v_d i_q - v_q i_d) \tag{3.4}$$

As the rotating reference frame is implemented to the *d*-axis alignment, the *q-axis* component is given as:

$$i_q = i_m^* \sin(\theta_0 - \theta) \tag{3.5}$$

where i_m and θ_0 are amplitude and angle of vector i, θ is the angle of the qd0 reference frame. For synchronizing the qd0 reference frame to the

grid current, the i_q has to be zero which means the d axis will be truly aligned with the vector.

3.2.6 PI Control and Closed-Loop system

In term of a SSSC control design, a proportional integral (PI) control is the most popular variation and mostly used, and by accurately tuning the control gain can achieve the excellent performance. A PI controller is used and can be presented as equation (3.6):

$$G(s) = K_p + \frac{K_I}{s} \tag{3.6}$$

where K_I is integral gain and K_p is proportional gain.

By considering Figure 3.14 as a closed system, the relevant transfer function for the closed-loop can be given as [15]:

$$\frac{\theta_0(s)}{\theta(s)} = \frac{i_m.G_{PLL}(s)}{s + i_m.G_{PLL}(s)} \tag{3.7}$$

Finally, by replacing $G_{PLL}(s)$, the closed-loop transfer function can be rewritten as the equation (3.8):

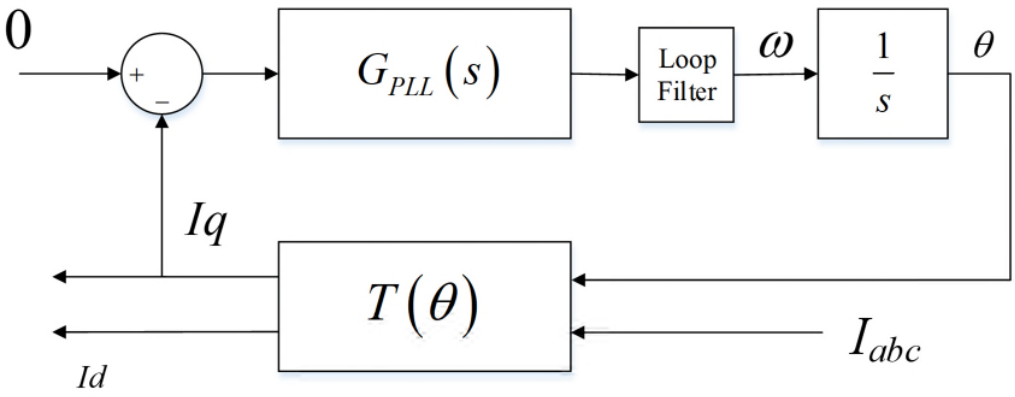

Figure 3.14: A phase-locked loop control system

$$\frac{\theta_0(s)}{\theta(s)} = \frac{i_m.K_{P\_PLL}s + i_m K_{I\_PLL}}{s^2 + i_m.K_{P\_PLL}s + i_m K_{I\_PLL}} \tag{3.8}$$

which can be simplified as:

$$\frac{\theta_0(s)}{\theta(s)} = \frac{2\xi_{PLL}\omega_{PLL}s + \omega_{PLL}^2}{s^2 + 2\xi_{PLL}\omega_{PLL}s + \omega_{PLL}^2} \tag{3.9}$$

where:

$$\omega_{PLL} = \sqrt{i_m.K_{I\_PLL}}, \xi_{PLL} = \frac{K_{P\_PLL}}{2}\sqrt{\frac{i_m}{K_{I\_PLL}}}$$

or (3.10)

$$K_{P\_PLL} = \frac{2\xi_{PLL}\omega_{PLL}}{i_m}, K_{I\_PLL} = \frac{\omega_{PLL}^2}{i_m}$$

and ω_{PLL} and ξ_{PLL} are the natural frequency and damping ratio, respectively.

A closed-loop control system is used to synthesize the appropriate sinusoidal waveform from the DC voltage source. The control system by using the values of the current passing through the SSSC and also the

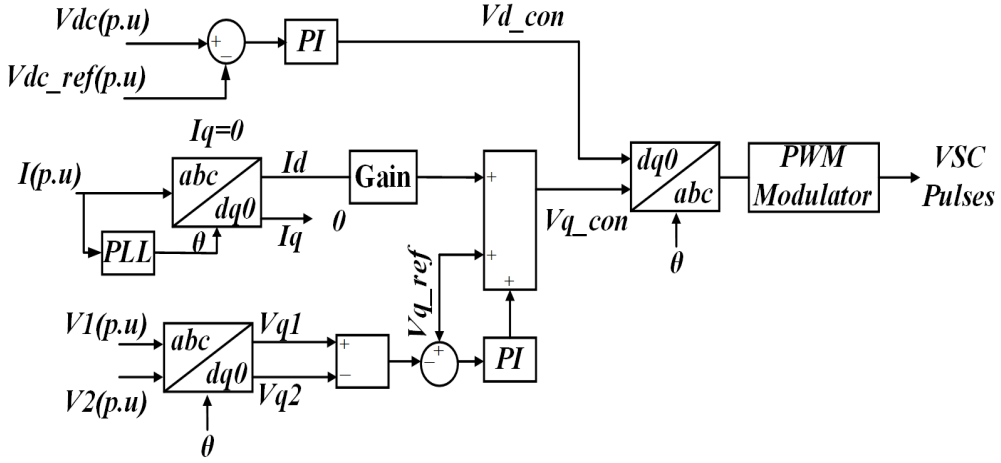

Figure 3.15: Closed-loop controller for voltage-sourced converter (VSC)

voltages of busbars 3 and 4 tries to control the line reactance and reactive power of the line. The V_{q_ref} value depends on the desired power compensation, that here is considered 10%. It means the voltage difference between V_{q1} and V_{q2} has to be remained below the 10% (see Fig. 3.15).

A phase-locked loop (PLL) control system has been used to synchronise the phase of output signals with that of the line current (see Fig. 3.14). Then, the obtained phase is used for all of the dq0 transformation.

As the SSSC injects the voltage to the network either capacitive or inductive one, thus the injected voltage has to stay in quadrature with line current. It means in the ideal system, V_d and I_q must be zero.

$$\begin{aligned} V &= V_d + jV_q, \qquad V_d \approx 0 \\ I &= I_d + jI_q, \qquad I_q \approx 0 \end{aligned} \tag{3.11}$$

The obtained V_{d_con} and V_{q_con} (see, Fig. 3.16) and V_{abc_con} (see, Fig. 3.17) are used to produce sinusoidal references for the 2-level PWM generator which switching frequency is 20 kHz. In this case, the SSSC is working in a normal condition to transfer the power between busbars 3 and 4 in Figure 3.1. The system properties are explained in sections 2.3 and 3.2.2.

The aim of the utilised block diagram is controlling the injected voltage into the network so that that SSSC behaves like an inductor or a capacitor. Since $V_q = X \times I_d$, the "Gain" value in the diagram, that refers to the series converter reactance X, is used to convert the I_d to V_q. The quantity of the injected voltage is controlled by V_{q_ref} that refers to the desired power compensation value. The polarity of the injected voltage is also defined

by V_{q_ref}. In fact, in the steady state V_{q1}-V_{q2}=V_{q_ref}. If it is positive it means the reactive power is injected otherwise is absorbed. Figure 3.16 presents V_q and V_d quantities. As it can be seen in 3.16, the V_q is positive that means the SSSC is capacitive (for example from the feeder 1 view) and injecting the voltage or reactive power to the network to compensate the power in feeder 2. This controller is used for the SSSC during the normal operation (without any fault) and also the fault situation in the continuation of this chapter.

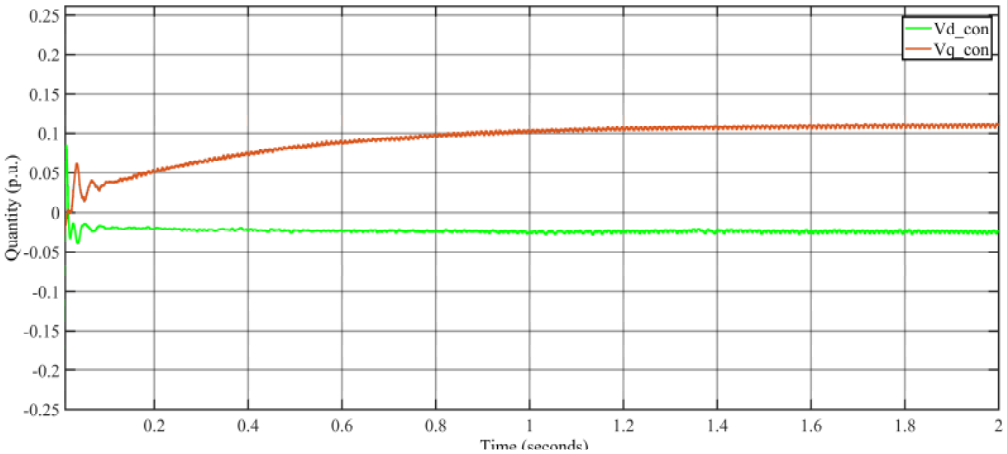

Figure 3.16: V_d and V_q quantities

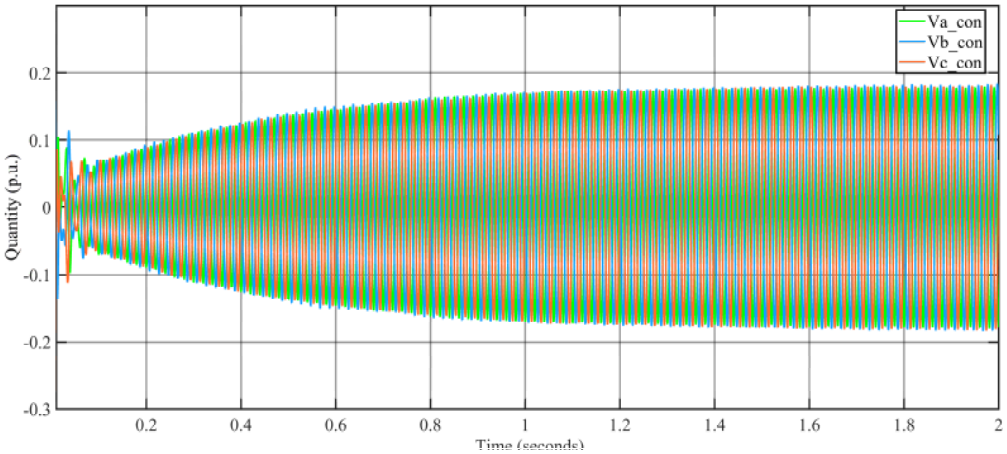

Figure 3.17: PWM reference signals

3.3 THYRISTOR-BASED PROTECTION SCHEME WITH VARISTOR

A major challenge is to protect the series compensator during a network short circuit fault; in this case a large current will flow, and the voltage applied to the series compensator will rise to the full line voltage. When a three-phase-to-ground fault occurs close to an unprotected SSSC as shown in Figure 2.15, the voltage across the SSSC will immediately increase to the full line voltage 11 kV (while the voltage rating of the converter is only 674 V) and the current will also rise rapidly to several thousand amperes (while the current rating of the converter is only 1600 A). Over-voltage and over-current of such magnitudes will simply destroy the converter and conventional mechanical circuit breakers are not able to respond rapidly enough to prevent damage. Using thyristors to provide a faster response could be a potential solution. This section proposes a new thyristor-based protection scheme which includes a varistor, as shown in Figure 3.18, to protect the SSSC in the MV distribution network. Thyristor crowbars have previously been used to mitigate unbalanced voltage dips under utility conditions for SSSCs [11, 12] but they have not been used for protecting the device under short-circuit conditions.

The protection principles are that the thyristor crowbars create another path-to-ground for the fault preventing the fault current from passing through the SSSC. Before the thyristor crowbar is turned on due to the fault detection time delay of the relay, the voltage across the SSSC will be limited by the varistor. The protection process is described in detail in the following sections.

3.3.1 Protection system design

For the proposed topology shown in Fig. 3.18 and 3.19, the protection process is as follows: When a fault happens, the voltage across the SSSC and varistor will increase rapidly until it reaches the clamped voltage of the varistor. At this stage, the varistor will allow a current to pass through it. Therefore, it prevents the voltage across the SSSC rising excessively high by providing an alternative current path for the fault current, which will decrease the current passing through the SSSC. The threshold voltage of the protection relay is set to 50% of the clamped voltage of the varistor. After detecting the fault, a delay of 1 ms is assumed before the thyristor crowbars are gated on and the circuit breakers are triggered to begin opening. Thyristors operate very quickly (~3 μs [16]) compared to mechanical CBs, whose opening time is uncertain and at least 20 ms [17,

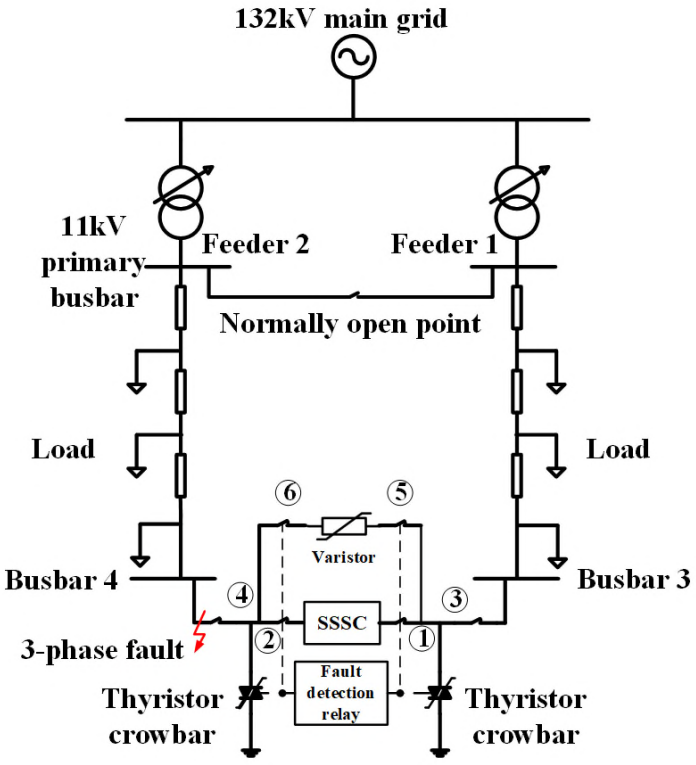

Figure 3.18: Schematic of proposed method by using both thyristor crowbars and Varistor

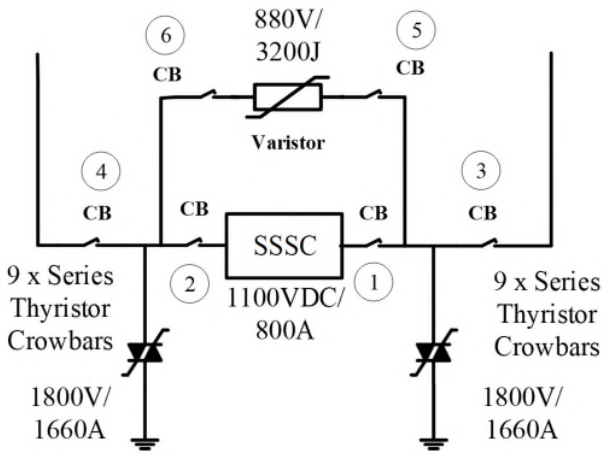

Figure 3.19: Protection circuit schematic

18]. By turning on the thyristors, the varistor comes out of the clamping state and the fault current will pass through them instead of the varistor and SSSC whose current is controlled to discharge the DC link capacitor and the current will eventually be zero; circuit breakers ①, ②, ⑤ and ⑥ are then opened. At this point, the SSSC is completely isolated from the grid and the thyristor crowbars can be gated off. This technique can decrease the effective response time of the SSSC protection from >20 ms

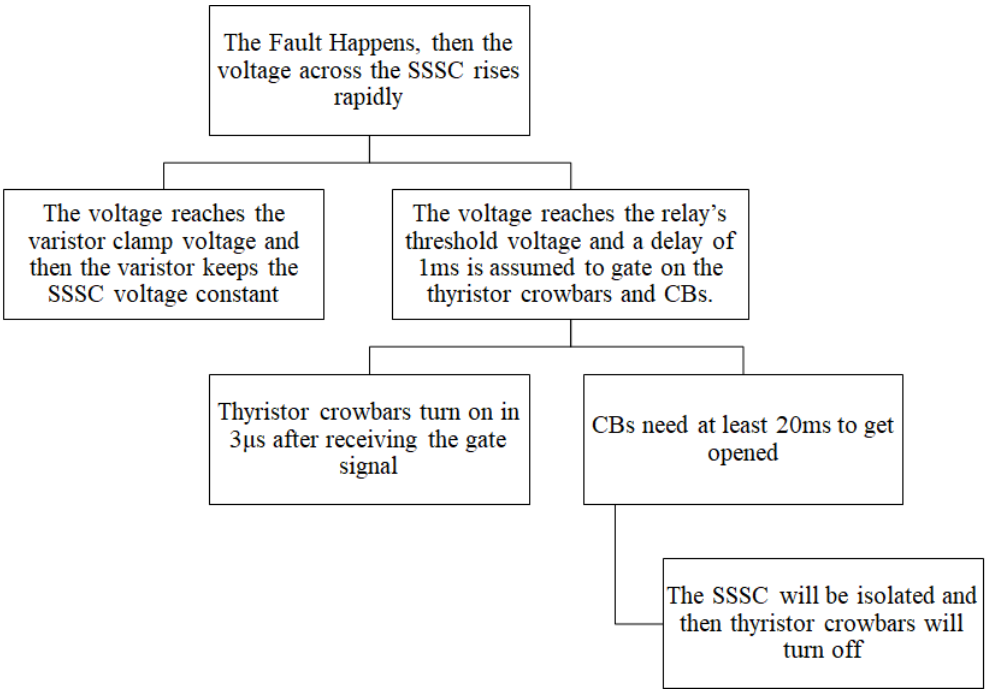

Figure 3.20: A flow chart of protection system procedure

to about 3 μs. Circuit breakers ③ and ④ are backup of ① and ② in case of failure for the thyristors to turn off. All CBs except ③ and ④ are of very low breaking duties (see Fig. 3.20).

3.3.2 Timing Diagram

The procedure of this protection technique from the fault detection to isolating the SSSC can be summarised as the following timing diagram, Fig. 3.21. It shows the proposed technique procedure and also the required timing in sending the gate signal to thyristor crowbars and CBs that has to be at the same time, otherwise any delay could cause severe damage to thyristors and definitely the SSSC.

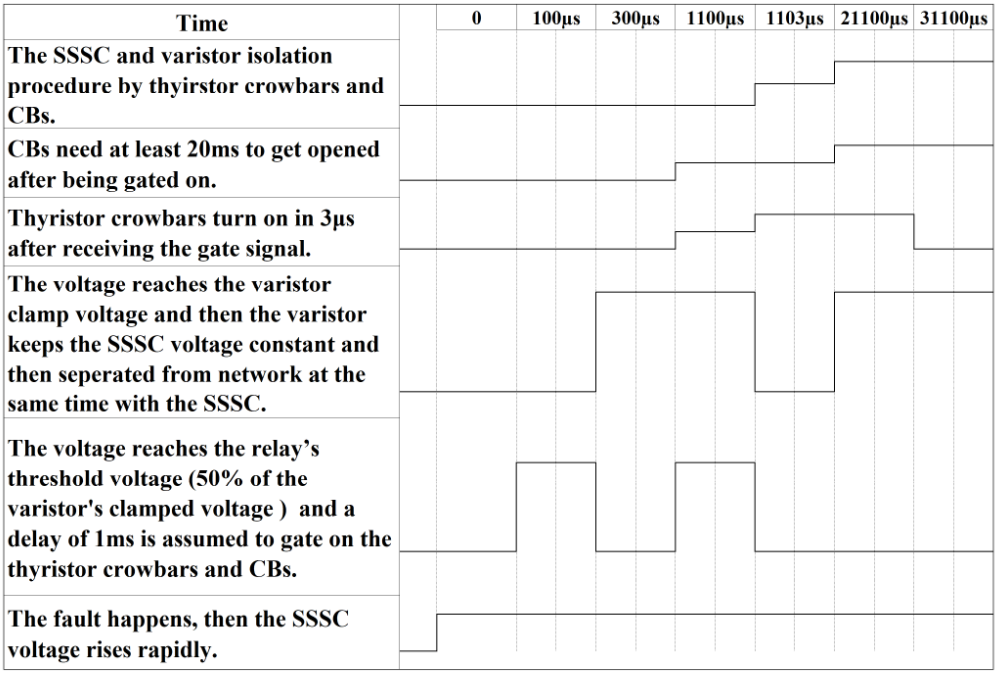

Figure 3.21: A timing diagram of the protection system procedure

3.4 THERMAL MODELS AND DEVICE LIMITS

3.4.1. Thermal Model

All devices must be kept below their maximum temperature ratings. The thermal behaviours of the IGBT chip, PiN Diode, and thyristor chip are modelled using a Foster network [19] as shown in Fig. 3.22.

R_i is the thermal impedance and τ_i is the time constant of each section in the Foster network, which are provided in the device datasheets ($\tau_i = R_i C_i$). The junction temperature can be calculated as follows:

$$T_{vj}(t) = \int_0^t P(t) \times \dot{Z}_{thj}(t-\tau) \times d\tau + T_{case}(t),\ Z_{thj}(t) = \sum_{i=1}^{n} R_i(t) \times (1 - e^{\frac{-t}{\tau_i}}) \qquad (3.12)$$

Which $Z_{thj}(t)$ is total thermal impedance, T_{case} is base plate temperature, T_{vj} is junction temperature and P(t) is power loss.

Here, P(t) is the instantaneous power dissipation of the device. For the IGBT:

$$P_{IGBT}(t) = P_{conduction}(t) + P_{switching}(t) \qquad (3.13)$$

where $P_{conduction}(t)$ refers to transistor power losses when it conducts the current and $P_{switching}(t)$ is the summation of turn-on and turn-off switching losses of the transistor.

For the PiN diode:

$$P_{PiN\ DIODE}(t) = P_{conduction}(t) + P_{reverse\ recovery}(t) \qquad (3.14)$$

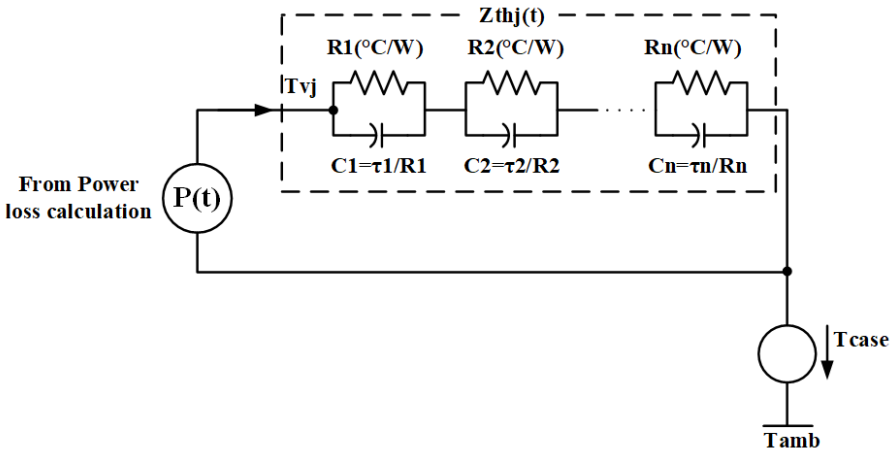

Figure 3.22: A typical Foster thermal model for IGBT, PiN Diode and Thyristor

Table 3.1: Thermal impedance

Model	i	1	2	3	4
IGBT-5SNE 0800M170100-ABB	R_i(K/kW)	15.2	3.6	1.49	0.74
	τ_i(ms)	202	20.3	2.01	0.52
PiN Diode-5SNE 0800M170100-ABB	R_i(K/kW)	25.3	5.78	2.6	2.52
	τ_i(ms)	210	29.6	7.01	1.49
Thyristor- 5STP 18F1800-ABB	R_i(K/kW)	10.350	3.760	2.290	0.670
	τ_i(ms)	0.3723	0.0525	0.0057	0.0023

where $P_{reverse\ recovery}(t)$ refers to the reverse recovery losses of the PiN Diode.

For the thyristor:

$$P_{THYRISTOR}(t)=P_{conduction}(t) \tag{3.15}$$

Varistor devices demonstrate fairly complicated electrical behaviour and their modelling can be approached in several different ways. The most common representation can be defined by an equivalent circuit as shown in Fig. 3.23 [20]. To simplify varistor modelling the following equation is often used [21-23]:

$$I = I_0 \times (V/V_0)^{\alpha} \tag{3.16}$$

For the varistor used in this paper, I_0, V_0 and α are 1000 A, 2450 V and 35. Voltage V is applied across the varistor and so R_X can be presented as the following equation:

$$R_x = \frac{V}{I} = \frac{V}{I_0 \times (V/V_0)^{\alpha}} \tag{3.17}$$

Varistors are typically pulse rated: As long as the peak current and the absorbed energy do not exceed the datasheet values the varistor will function correctly [24, 25], therefore a Foster thermal network model is not used for the varistor. The energy absorbed by the varistor is obtained by:

$$E = \int_0^T V_c(t) I(t) dt \tag{3.18}$$

where V_c is the clamping voltage, and I is the peak current.

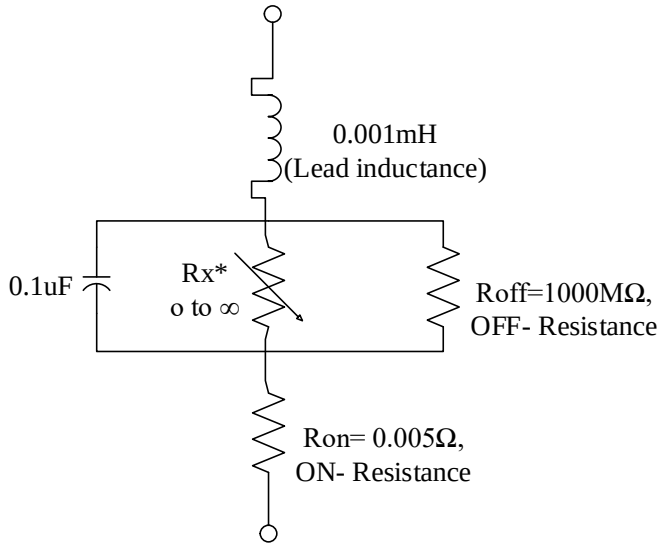

Figure 3.23: An equivalent circuit of a varistor (V881BA60, LittleFuse)

3.4.2 Device Limits

According to the IGBT module datasheet, the maximum withstanding junction temperature is 150°C for both of IGBT chip and PiN diode and the maximum surge current is 6.6 kA for a 10 ms-pulse, where the junction temperature is 125°C.

In terms of the thyristor's surge current, junction temperature, and voltage rating, the utilised one in this simulation can endure 17.5 kA during a 10 ms- and 14.2 kA during a 20 ms-pulse, which means two 10ms-pulses, when Junction temperature is 125°C. Since it is only used within the fault condition, its junction temperature can be assumed between 25°C to 40°C that in this simulation is 40°C. The thyristor's maximum withstanding temperature is 289°C, when T_{vj}=125°C and $V_{R\&D}$=0.6V_{RRM}; where $V_{R\&D}$ and V_{RRM} are the thyristor voltage after the surge current and the reverse blocking voltage, respectively.

Regarding the varistor, a metal-oxide varistor made by Littelfuse (V881BA60) is used. It can absorb 3200J and endure 1 kA and 1.5 kA within a 1ms- and 0.7ms-pulse, respectively. Because the varistor is used for up to 1 ms (the required time delay for the relay to switch on the thyristor), the mentioned data shows its ability during this period.

Table 3.2: Network Properties

		Feeder 2	Feeder 1
Voltage level		11 kV	11 kV
Source fault level		250 MVA	250 MVA
Cable Impedance	**Resistance**	0.06 Ω/km	0.06 Ω/km
	Inductance	0.134 mH/km	0.134 mH/km
Cable length		10 km	5 km
Load		17 MW	1 MW
SSSC-Transformer		1100 V_{DC}/800 A-600 kVA,1 kV/1 kV	
Varistor		880 V/3200 J	
Thyristor		1800 V/1660 A	

3.5 GENERAL SELECTION PROCEDURE FOR THE THYRISTOR AND VARISTOR

Selecting proper thyristor and varistor is important for the effectiveness of the proposed protection scheme. A bad choice could lead to failure of the concept.:

A) Selection of thyristor

The following aspects should be considered:

1. the maximum short circuit current level including the DC offset;
2. the maximum number of surge current pulses that the thyristor has to conduct;
3. the peak voltage that the thyristor has to withstand after the fault clearance.

The making fault level of an 11 kV system is managed below 600 MVA, meaning that the maximum rate of current rise in the thyristor is about 14 A/μs (assuming 50 Hz). This can be easily satisfied and hence the main constraint will be the temperature rise of the device under the current surges. If the number of the current surge pulses to be carried by the thyristor increases, the amplitudes of the pulses have to reduce.

The maximum peak voltage determines the number of series thyristors in the crowbar. Although an 11 kV system is usually neutral unearthed, two strings of thyristors can always withstand the peak line-to-line voltage.

B) Selection of varistor

The procedure of selecting the varistor is as below:

1. determine the clamping voltage of the varistor according to the SSSC maximum peak voltage in normal condition;

2. determine the operating time of the varistor;

3. calculate the surge current through the varistor;

4. calculate the energy to be dissipated in the varistor.

3.6 SIMULATION RESULTS

The parameters of the case study are shown in Table 3.2 and a schematic of the three-phase SSSC is shown as Fig. 3.24. The proposed method is compared with a conventional protection method.

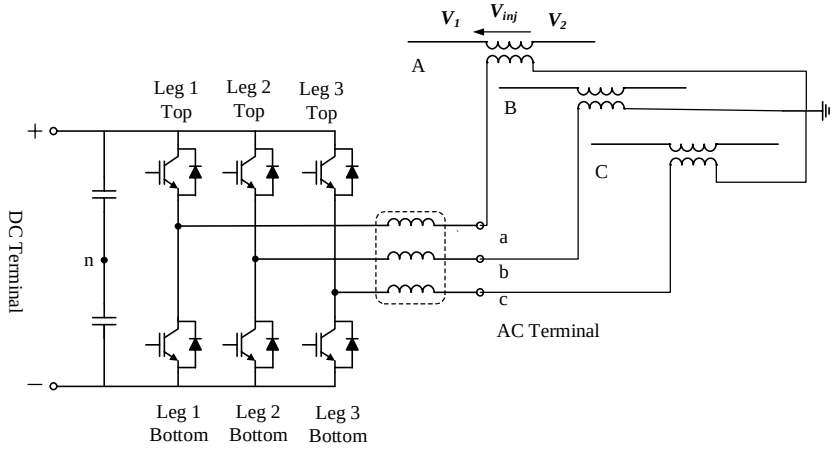

Figure 3.24: A schematic of three phase VSC-SSSC connected to the network through a three-phase coupling transformer

3.6.1 Conventional Protection Method

Figure 3.1 shows the structure of the conventional protection mechanism that only uses CBs. In this case, it is supposed that a fault happens at 1.58s (see, Fig. 3.27) and voltages in phases A, B and C will reach to the threshold voltage of relays at 0.205 ms, 0.230 ms and 2.625 ms after the fault. Then 1ms after that, relays will send the opening command to CBs, and then CBs will cut off the current after 20 ms. For instance, regarding the phase A, the entire cutting off time is 0.205 ms+1 ms+20 ms. Figures 3.25 and 3.26 are related to the current and the voltage of a PI closed-loop voltage SSSC during the fault. The fault level can rise to 7 kA which can severely damage the IGBTs, plus the voltage overshoot is around 18 kV which can saturate the transformer.

Under the saturation, the transformer draws very high magnetizing current and significant Ampere-turns imbalance takes place. The Over-fluxing also causes an increase in transformer losses. The core losses typically increase by 40% for a 10% over-fluxing in the transformer. In the current transformer (CT), it may result in wrong measurements and may even cause malfunctioning of protective relays. Moreover, due to these saturation flux densities, the transformer will overheat and hot spots will form in the transformer. This Flux not flowing in intended paths may link conducting loops in the windings, loads, tank base and structural parts and these circulating currents in these loops can cause a dangerous temperature increase. When working under the high flux density condition, the heat of the inner portion of the winding may be extremely high as a large amount of magnetizing current full of harmonics is flowing in the circuit [26].

Regarding the calculation of IGBT module temperature, the mentioned converter and IGBT modules in section 3.2 have been used for this simulation and the junction temperature is assumed to be at 90^{o}C.

As can be seen in Fig. 3.25, phase B has the highest peak current 7 kA which exceeds the 6.6 kA permissible peak current. Subsequently, phase A current peak reaches to 6 kA which causes the temperature of the IGBT modules to exceed or become very close to the max. T_{vj} 150°C as it is shown in figures 3.28 and 3.31 as the worst cases. Figures 3.28 and 3.31 show the temperature behaviour of IGBTs (blue line) and PiN Diode (orange line), as it can be seen the temperature in these legs has exceeded the 150°C for both IGBT chip, PiN Diode that can severely damage them, especially for cases the CBs need longer opening time to get opened (three cycles or more for some of them). It means the conventional method is not fast enough to protect the SSSC.

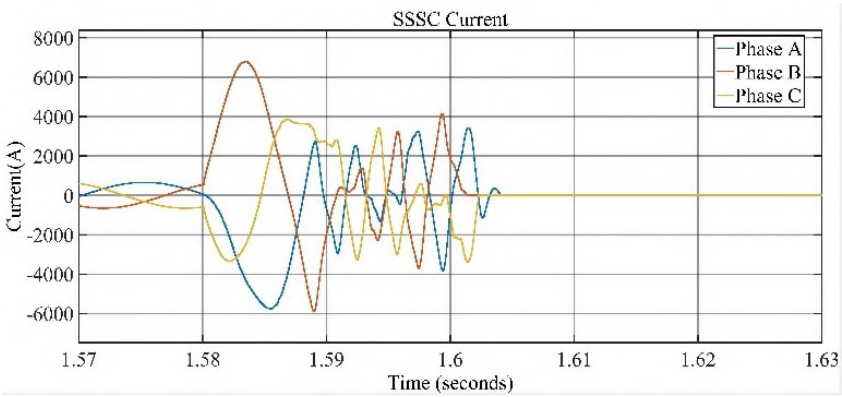

Figure 3.25: The fault current passing through SSSC- Conventional Method

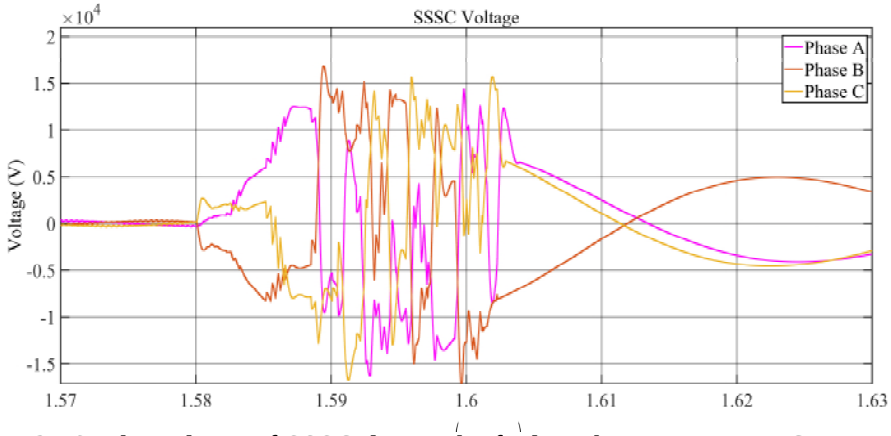

Figure 3.26: The voltage of SSSC during the fault without protection-Conventional Method

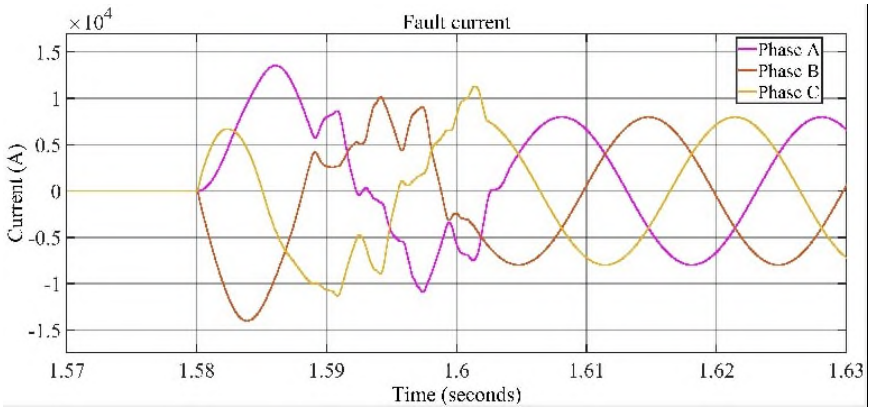

Figure 3.27: The fault current level at fault point

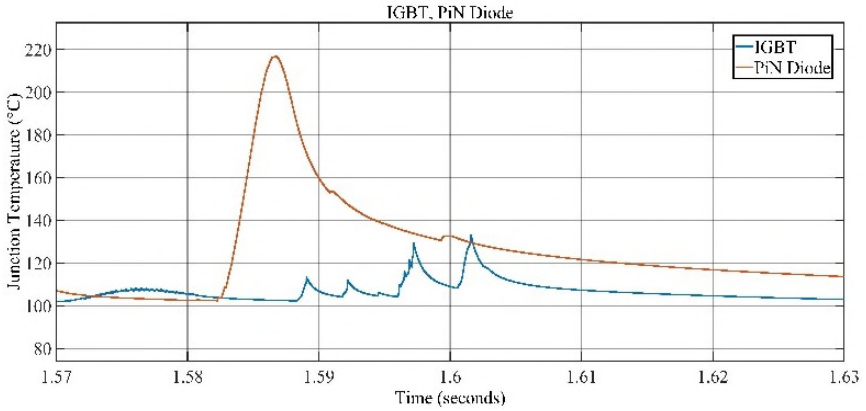

Figure 3.28: Temperature of IGBT in leg 1 top- Conventional Method

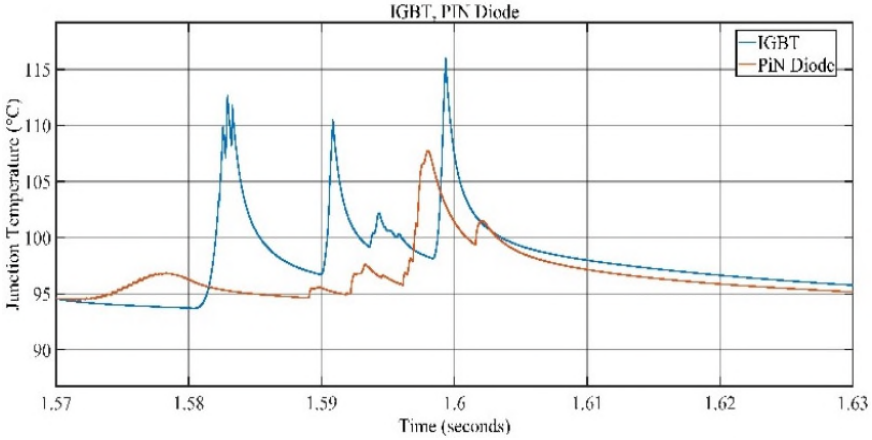

Figure 3.29: Temperature of IGBT in leg 1 bottom- Conventional Method

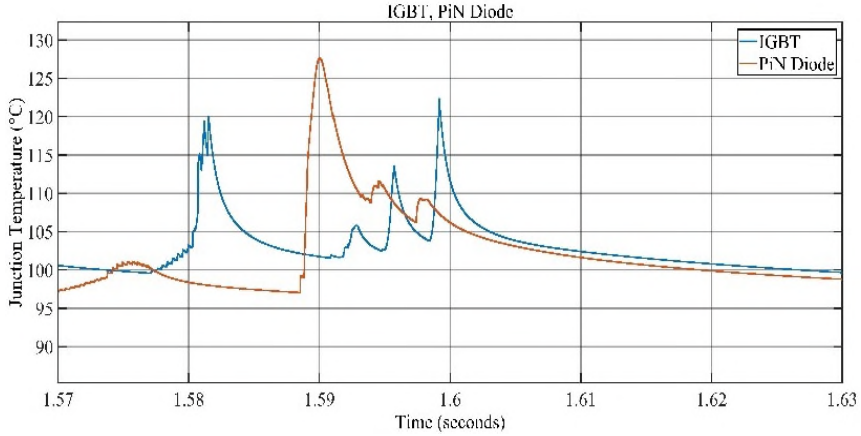

Figure 3.30: Temperature of IGBT in leg 2 top- Conventional Method

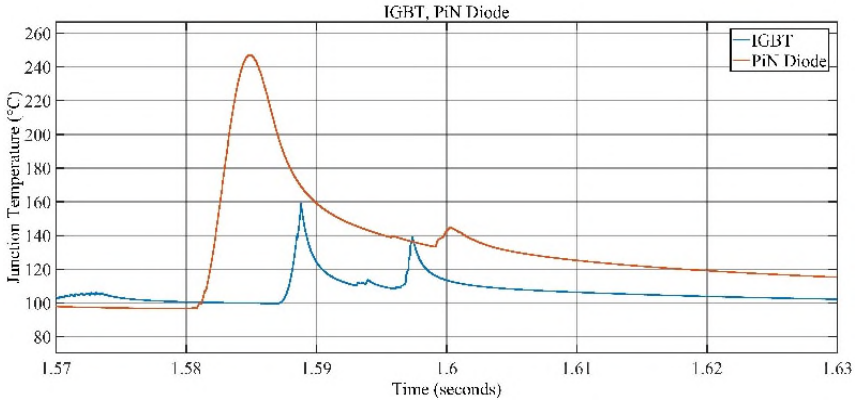

Figure 3.31: Temperature of IGBT in leg 2 bottom- Conventional Method

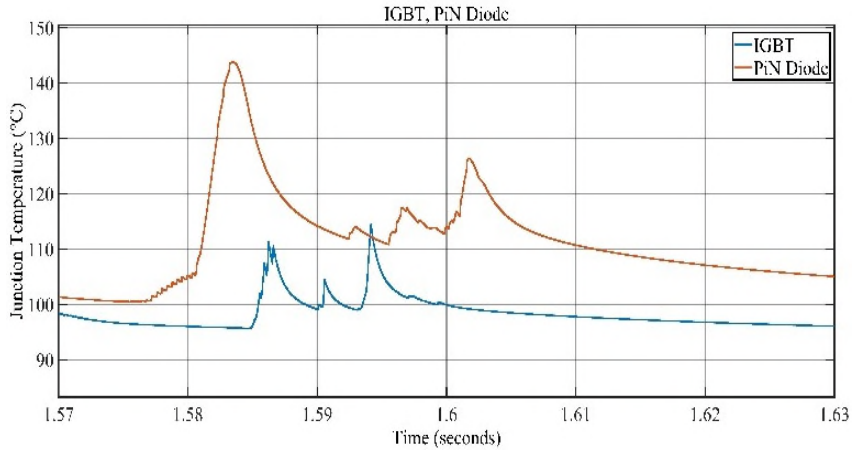

Figure 3.32: Temperature of IGBT in leg 3 top- Conventional Method

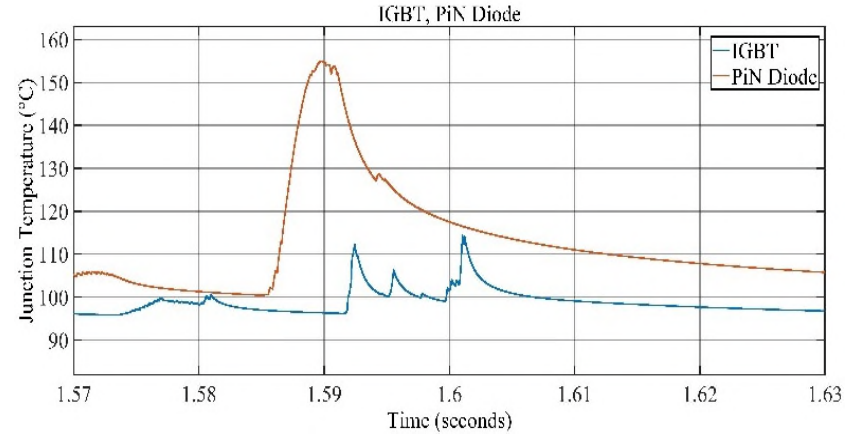

Figure 3.33: Temperature of IGBT in leg 3 bottom- Conventional Method

3.6.2 Proposed Protection Method

In the second case, thyristor crowbars are in a shunt position to the SSSC and a varistor is in parallel with SSSC as shown in Fig. 3.18. The voltage and current ratings of the SSSC semiconductors are 1.7 kV and 1.6 kA respectively.

For simulating this case study, a three-phase-to-ground fault occurs at t=1.58 s and the voltage across the varistor and SSSC increases immediately but is limited at the varistor clamped voltage, 2360 V (Fig. 3.34). Varistors in phases B&C will start to work 0.275 ms after the fault and in phase C 2.275 ms. Therefore, until the thyristor crowbars turn on, the varistor will drive the current through itself so as to control the voltage and current of SSSC. During this period, the voltage of the varistor is

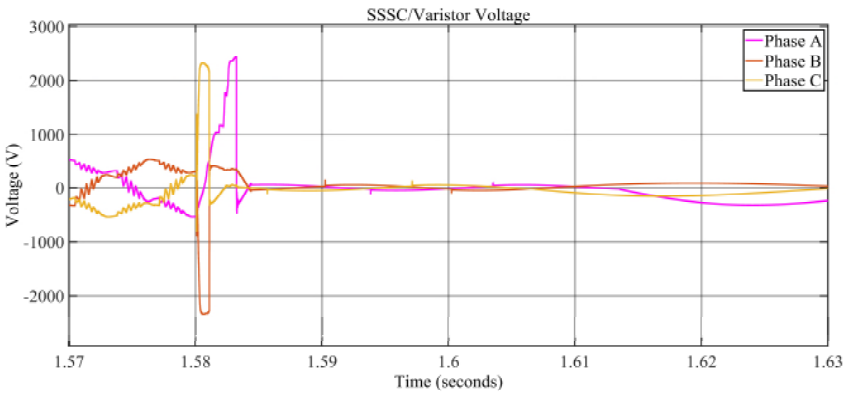

Figure 3.34: Voltage of SSSC/Varistor- Proposed Method

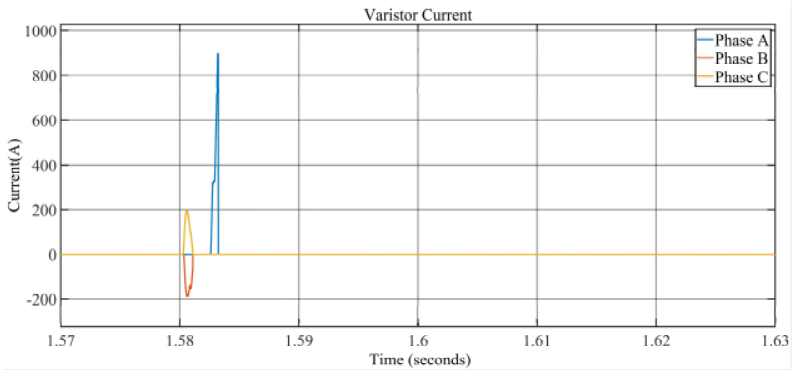

Figure 3.35: Varistor current- Proposed Method

similar to SSSC, Fig. 3.34, and current is shown in Fig. 3.35. Furthermore, the absorbed energy of that is obtained around 700 J (see Fig. 3.36). It can be seen that the energy and also current are completely below the allowable limits so it can be claimed that the varistor temperature is certainly lower than 125°C, its max. tolerable temperature. Voltages in phases A, B and C will reach to the threshold voltage of relays at 0.095 ms, 0.230 ms, and 1.655 ms after the fault. Then after 1ms, the required time for detecting the fault and sending the gate signal, the crowbars are turned on and then most of the fault current passes through them because the thyristor's turn-on impedance is much smaller. For example, the required time to turn the thyristor on in Phase A is 0.095 ms+1 ms. Fig. 3.38 shows the thyristor current value. As it is mentioned, the surge current can be an indicator of the thyristor crowbar capability in tolerating the fault, Fig. 3.37 shows the thyristor crowbar schematic.

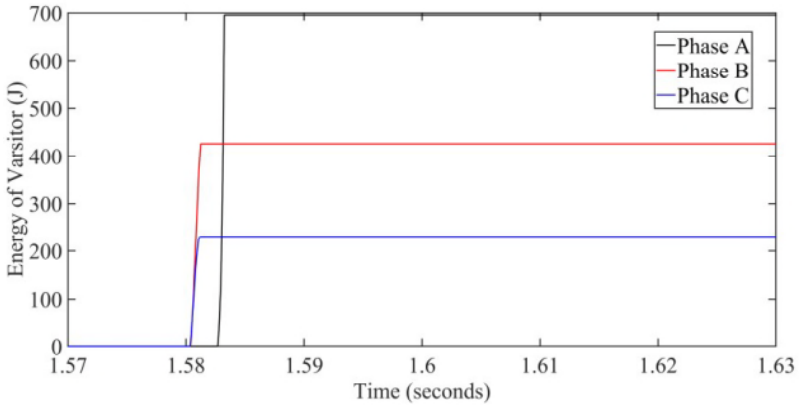

Figure 3.36: Varistor's absorbed energy during fault

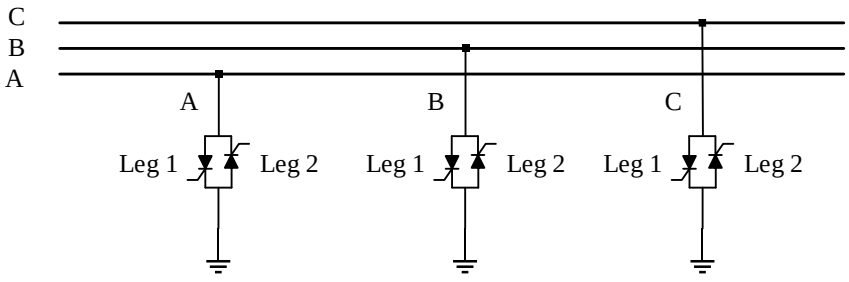

Figure 3.37: Thyristor crowbars schematic of the connection to the network

As it is shown in Fig. 3.38 phase A has the highest surge current which also repeats twice for the thyristor phase A leg 1. Therefore, the absorbed energy for this thyristor has been calculated and obtained around 400 J (see. Figures 3.39 and 3.40).

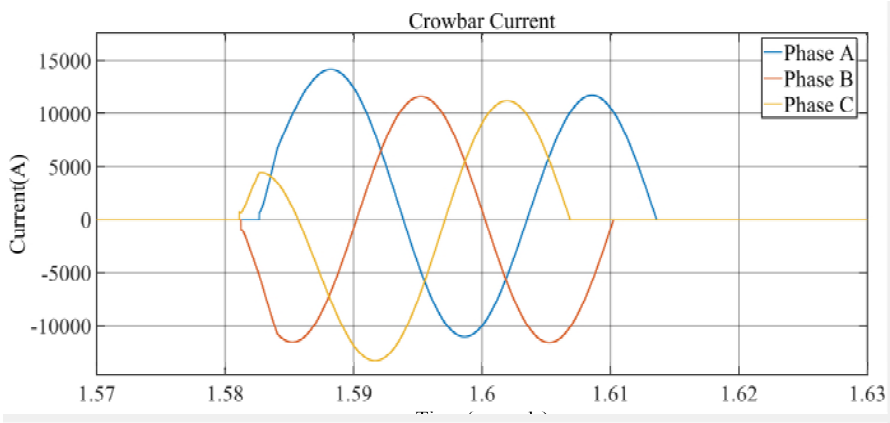

Figure 3.38: Thyristor current during fault- Proposed Method

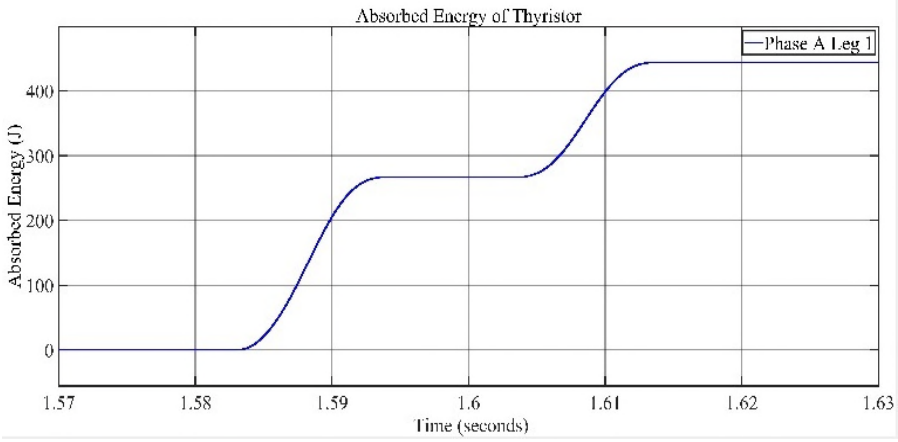

Figure 3.39: Absorbed energy by thyristor in phase A leg 1

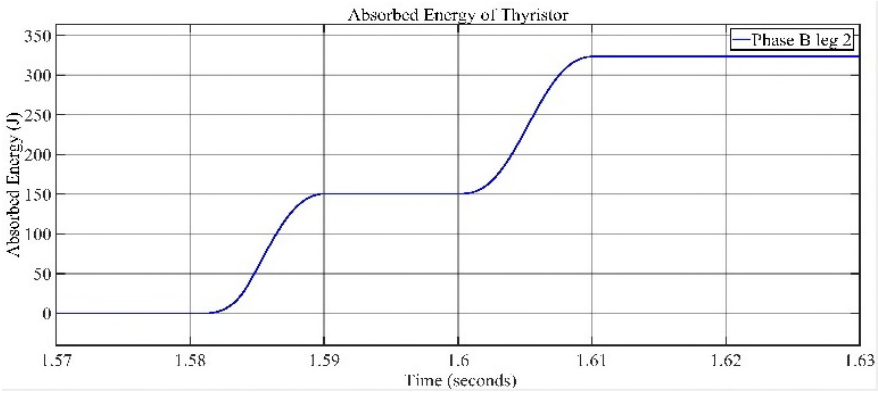

Figure 3.40: Absorbed energy by thyristor in phase B leg 2

Fig. 3.41 to 3.43 show the thyristors' thermal graphs for phases A, B and C legs 1 & 2. That of phase A (Fig. 3.41) is supposed to be the worst-case between other thyristors based on what has been mentioned previously. It can be deduced that no thyristor temperature is exceeding its allowable limit. In parallel with thyristors' operation, after 20 ms of

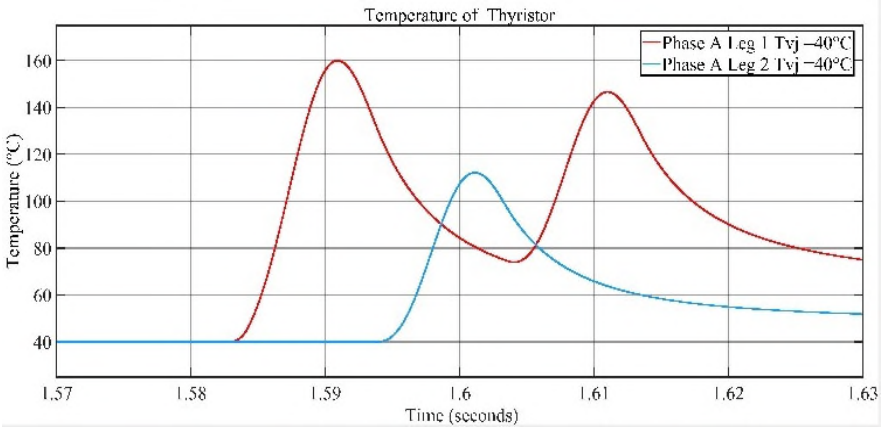

Figure 3.41: Temperature of thyristor crowbar in phase A- Proposed Method

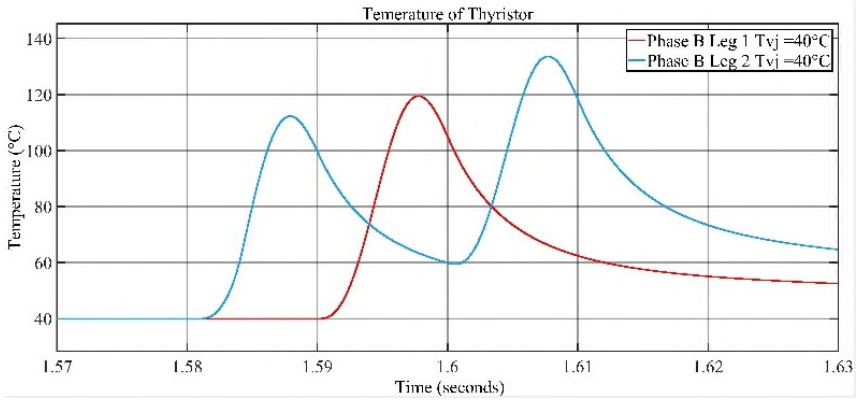

Figure 3.42: Temperature of thyristor crowbar in phase B- Proposed Method

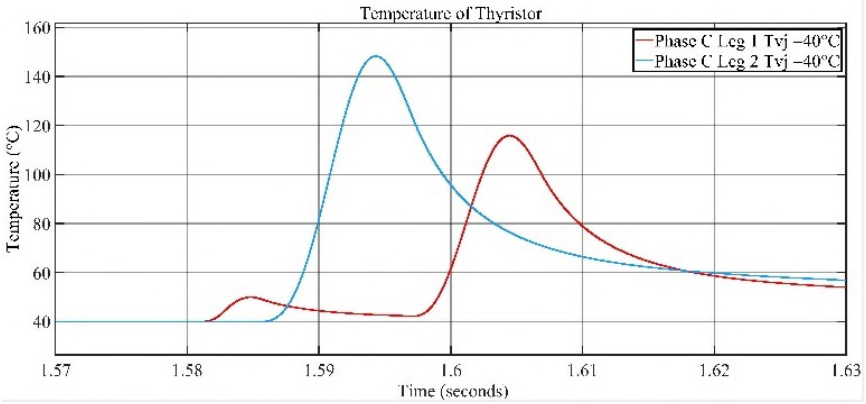

Figure 3.43: Temperature of thyristor crowbar in phase C- Proposed Method

detecting the fault, the circuit breakers 1 and 2 are opened, and then the thyristor crowbars are gated down to be switched off. It is worth mentioning that the thyristor voltage has a great effect on its surge-tolerance ability after the surge. As it is mentioned after the surge current phenomena, the voltage applied across the thyristor must be 0.6 VRRM (0.6 × 1800 V). Therefore, in this case, since the voltage peak value is 9 kV, as shown in Fig 3.44, at least 9 thyristor crowbars for each phase are required. More to the point, the DC offset which is generated during a fault is completely ignorable in medium voltage networks and thus has no influence on the turning-off process of thyristor crowbars [8]. Consequently, as it was expected the short circuit current passing through the SSSC is limited to 3 kA (peak current value), Fig. 3.45, which is less than half of the previous one (6.5 kA peak value) and its duration is also decreased to only 4 ms, however, its rising time is just 1 ms. Besides, the

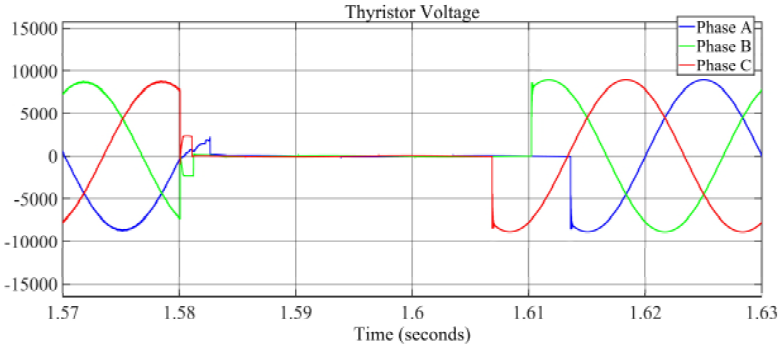

Figure 3.44: Thyristor Voltage- Proposed Method

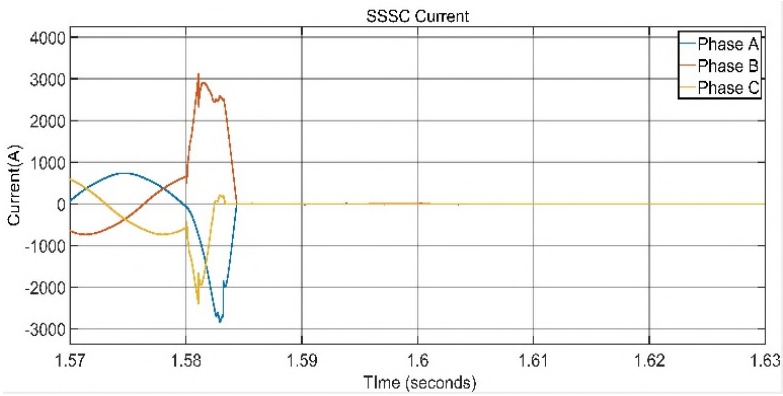

Figure 3.45: SSSC Current- Proposed Method

voltage across the SSSC as mentioned before is controlled by the varistor and its value limited to 2450 V compared to 15 kV in the first case study.

Regarding the IGBT temperature, first of all, the maximum current passing through them is 3 kA which is much smaller than their maximum allowable surge current (6.6 kA). Also the phase B current is the worst case during this fault situation, so the temperature of IGBT module leg 2

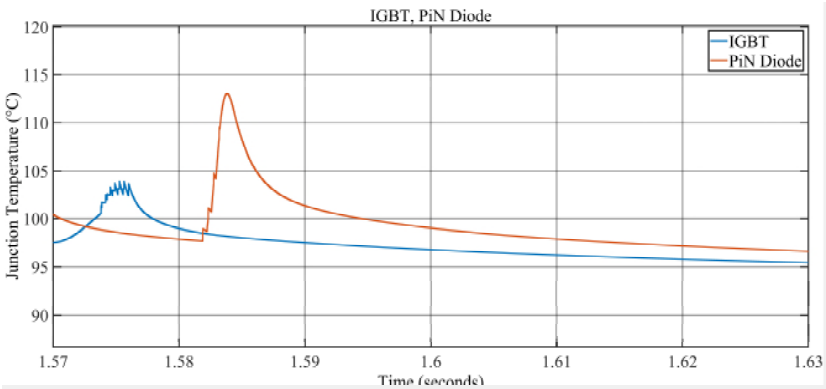

Figure 3.46: Temperature of IGBT in leg 1 top

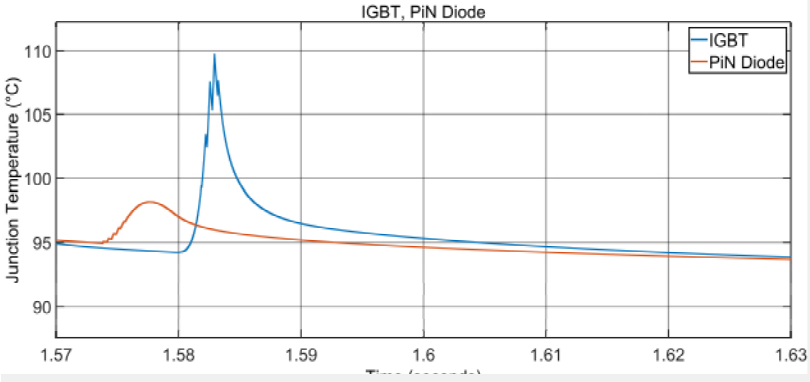

Figure 3.47: Temperature of IGBT in leg 1 bottom

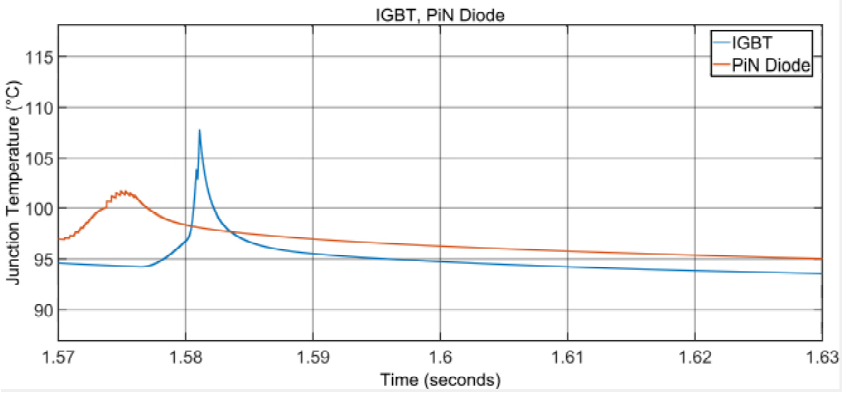

Figure 3.48: Temperature of IGBT in leg 2 top

(lower leg) will be the highest temperature rise (see Fig. 3.49) compared to the other IGBTs (see Figures 3.46 to 3.51) As expected, the PiN Diode temperature is 128°C which is well below 150°C, the max. tolerable temperature for IGBT module for either the IGBT chip or the PiN Diode.

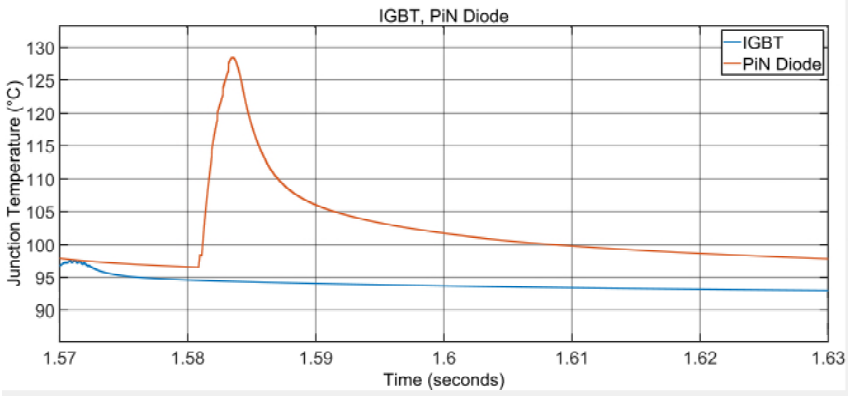

Figure 3.49: Temperature of IGBT in leg 2 bottom- Proposed Method

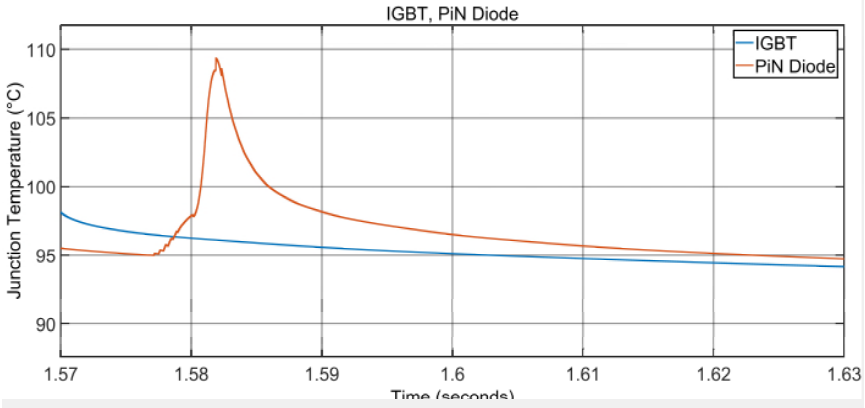

Figure 3.50: Temperature of IGBT in leg 3 top

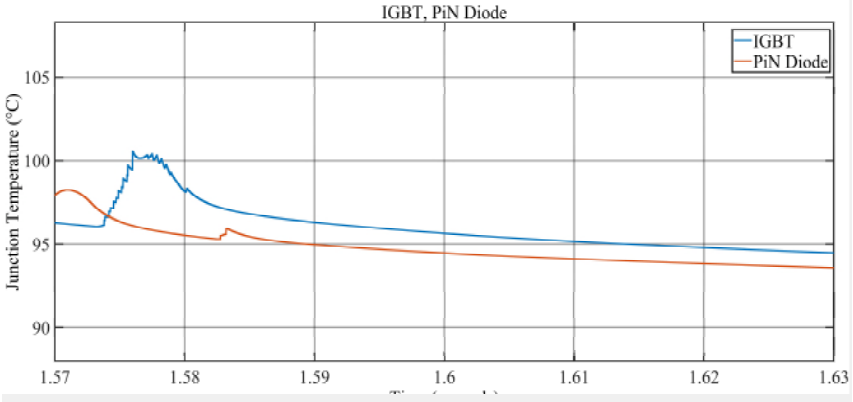

Figure 3.51: Temperature of IGBT in leg 3 bottom

Apart from the IGBT and PiN diode protection, the capacitors utilised in the DC side of the converter could get severely damaged during fault if the protection system will not act very fast, Fig. 3.52 shows the voltage level of capacitors that can reach to 22 p.u. but by using the proposed method it can be limited to 1.5 p.u. when the DC voltage is 1100 VDC.

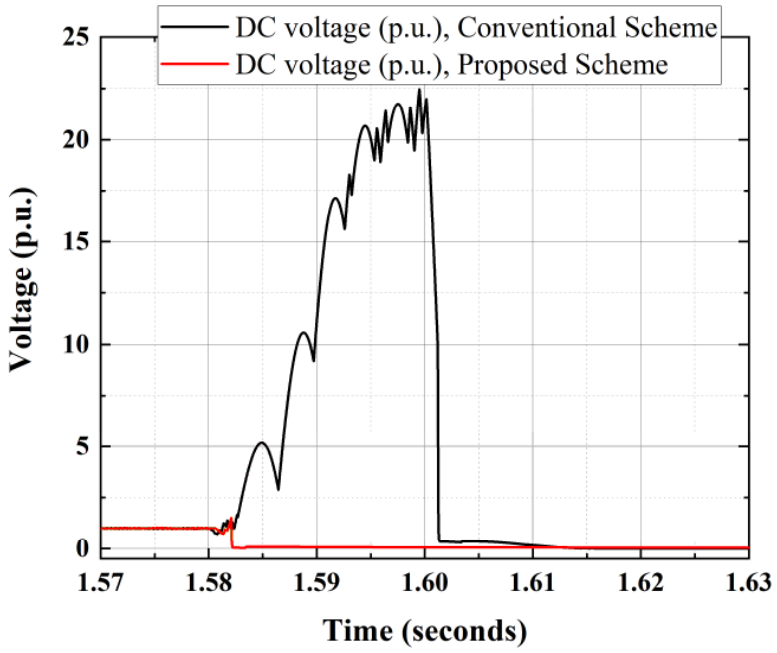

Figure 3.52: Capacitor voltage of the converter- DC side

3.7 EXPERIMENTAL RESULTS

To prove the proposed protection scheme, a scale-down single-phase model has been considered as illustrated in Figures 3.53 and 3.54. However, in this case, instead of using two thyristor crowbars in shunt to the SSSC, one thyristor crowbar in parallel has been used. In fact, the difference between these two methods is the control of the short-circuit level at the fault point, meaning that by bypassing all current to the same side the fault level would now be almost twice. Also, in this case in order to control the fault current passing through the thyristor it has connected to the fault point rather connecting to the ground. A single-phase H-bridge voltage source converter is connected to the line via a series coupling transformer which mimics the SSSC. A 230 V_{AC} 50 Hz single-phase voltage source is implemented to mimic the grid. A resistor bank is connected between transformer and voltage source in order to create a

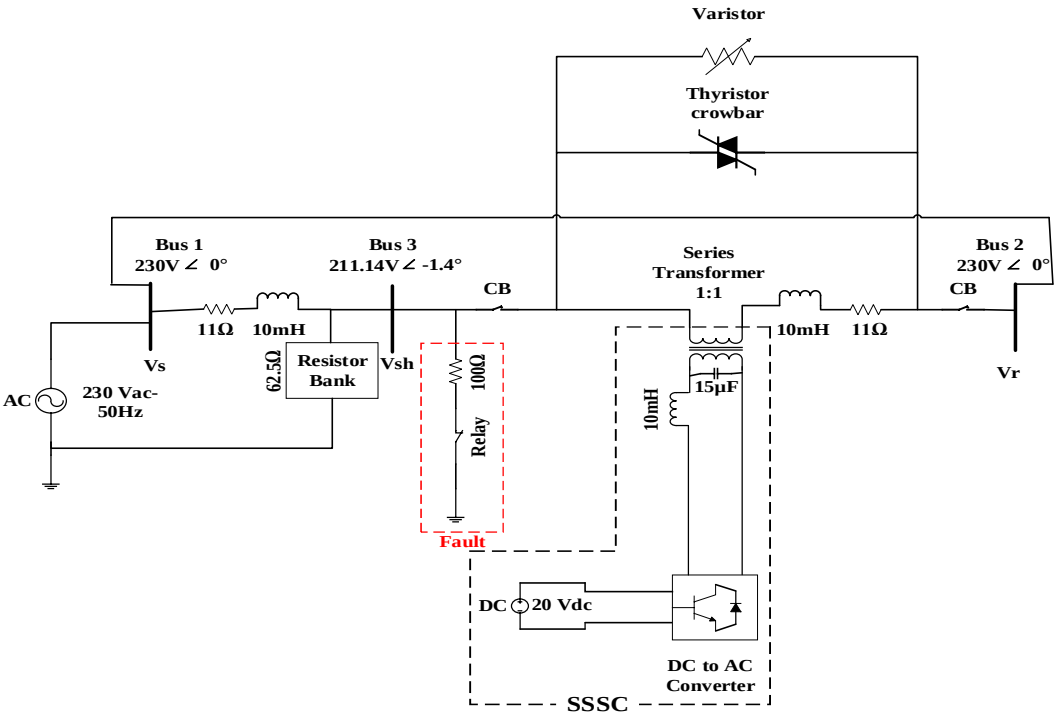

Figure 3.53: Single Phase Protection Scheme

relative phase shift [27, 28] at Bus 3 by drawing a current through the interconnecting impedance. The measured voltages at Buses 1 and 2 are equal to $230\ \mathrm{V}\angle 0^{\circ}$ and in Bus 3 is $204.71\ \mathrm{V}\angle -2.48^{\circ}$ without the SSSC, and $211.14\ \mathrm{V}\angle -1.4^{\circ}$ with the SSSC. It is worth mentioning that an open-loop voltage control system for the SSSC has been considered. That's why there is no control on the voltage phase and amplitude.

3.7.1 Conventional Protection Method

First of all, in the absence of thyristor and varistor, a fault happens in the network in order to check the current, voltage and temperature behaviour of the converter. For monitoring the temperature, a thermocouple is connected to the converter heatsink to record the temperature variation of that. In this case, a fault happens at t=64 ms and then circuit breakers open after 20 ms. The obtained results are as for Figures 3.55-3.57. The utilised IGBT in this test is SEMIKRON SK35GD126ET, and its temperature variations during fault by measuring the heatsink temperature is obtained as Fig. 3.57.

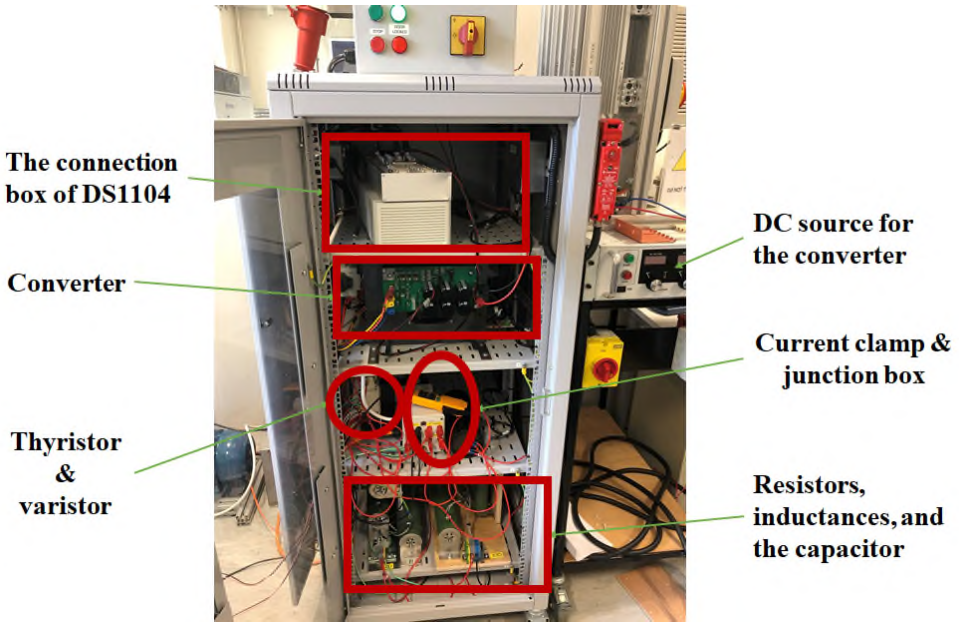

Figure 3.54: Laboratory Prototype

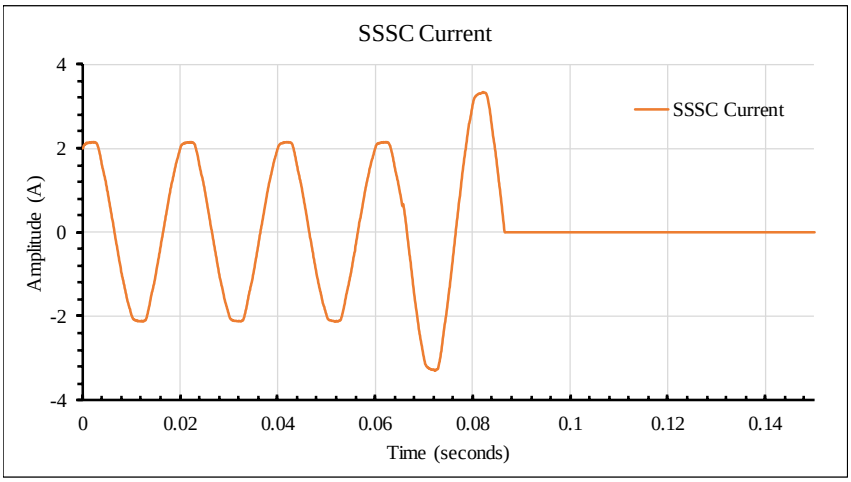

Figure 3.55: SSSC Voltage & Current- Conventional Method

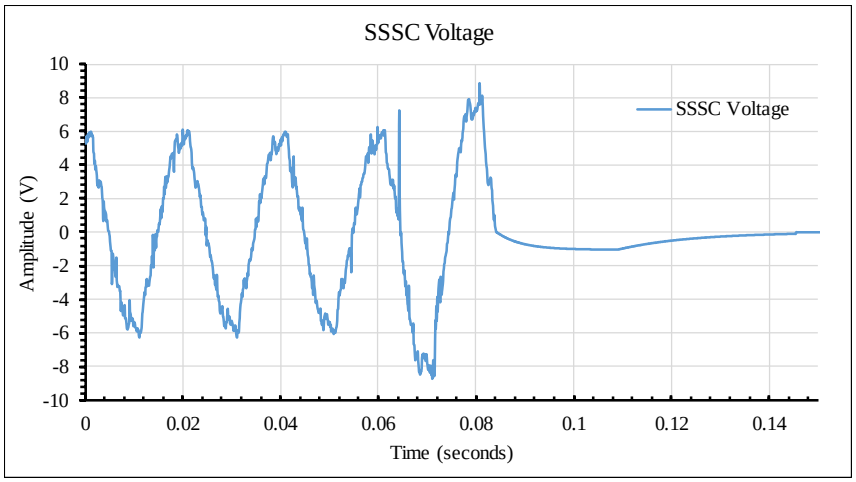

Figure 3.56: SSSC Voltage & Current- Conventional Method

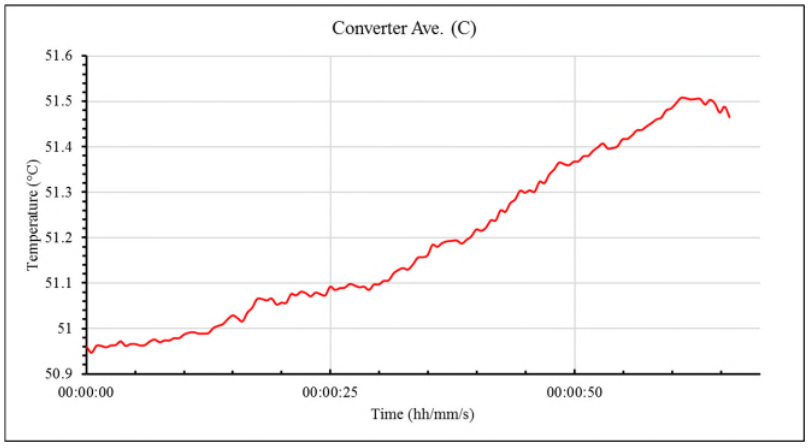

Figure 3.57: Temperature variation of IGBT- Conventional Method

3.7.2 Proposed Protection Technique

In the second case study, the varistor and thyristor crowbar are also being used to prove the efficiency of the proposed technique. The used thyristor crowbar and varistor are SEMIKRON SKKT 273 and TDK metal oxide varistor B72210S0140K101, respectively. In this case, fault happens at t=64 ms, and after 2 ms relay, the thyristors are gated on. During the 2ms delay, the varistor will control the voltage across the SSSC by providing a path for the fault current. After 20 ms the CBs interrupt the current. For measuring the temperature, a thermocouple is connected to the converter heatsink, thyristor crowbar heatsink and varistor body. The results are presented in Figures 3.58 to 3.64.

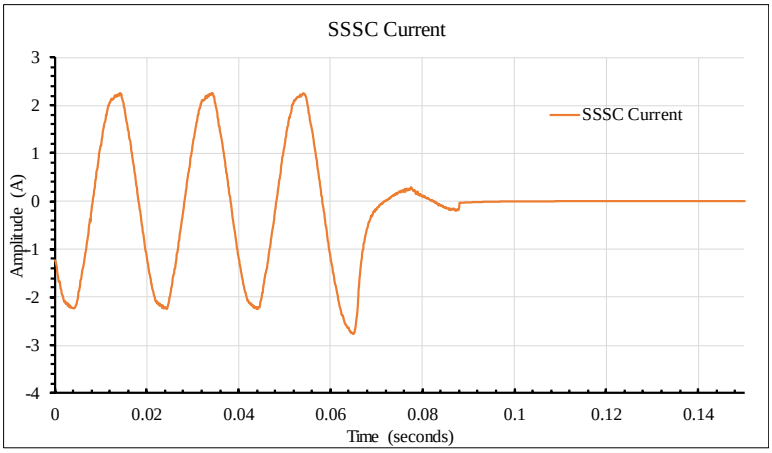

Figure 3.58: SSSC Voltage & Current - Proposed Technique

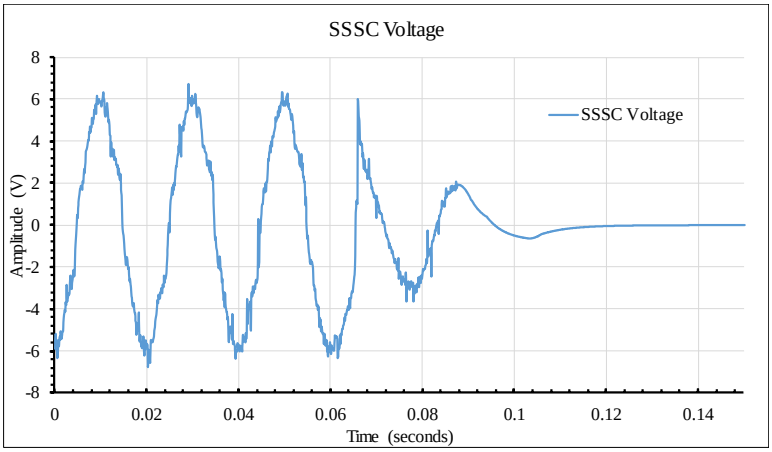

Figure 3.59: SSSC Voltage & Current - Proposed Technique

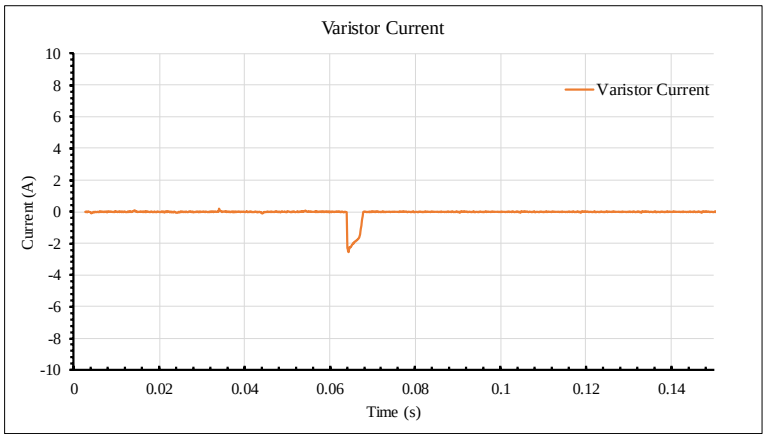

Figure 3.60: Thyristor & Varistor's Current- Proposed Technique

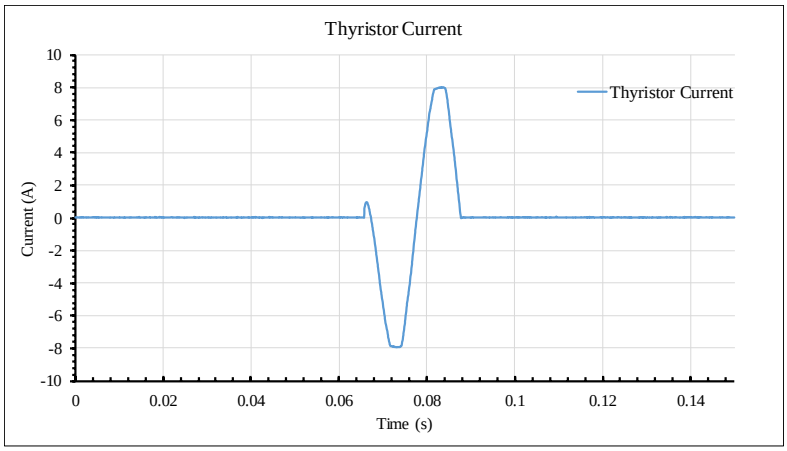

Figure 3.61: Thyristor & Varistor's Current- Proposed Technique

These experimental results indicate the proposed technique can maintain the temperature variations of IGBTs within the safe operating range. However, in Fig. 3.57 the temperature is not changing massively, but in comparison with Fig. 3.62, by cutting off the current passing through the converter, it will control the temperature increase. Moreover, the voltage variations of the SSSC, as shown in Fig. 3.59 is well-controlled by using the proposed technique compared to Fig. 3.56 the conventional one.

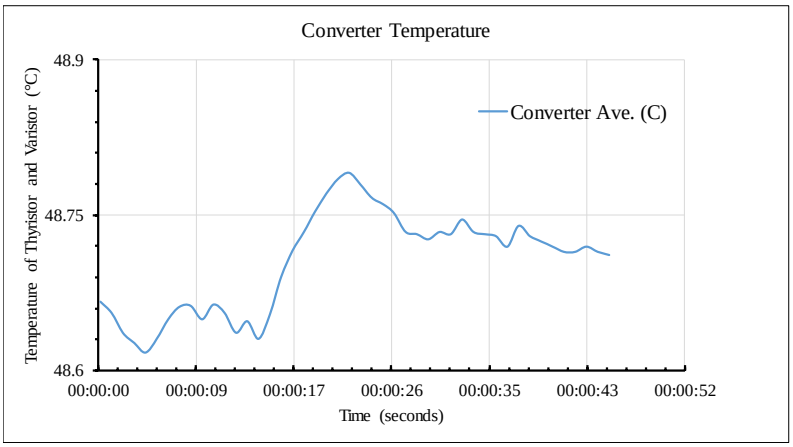

Figure 3.62: Temperature variation of IGBT- Proposed technique

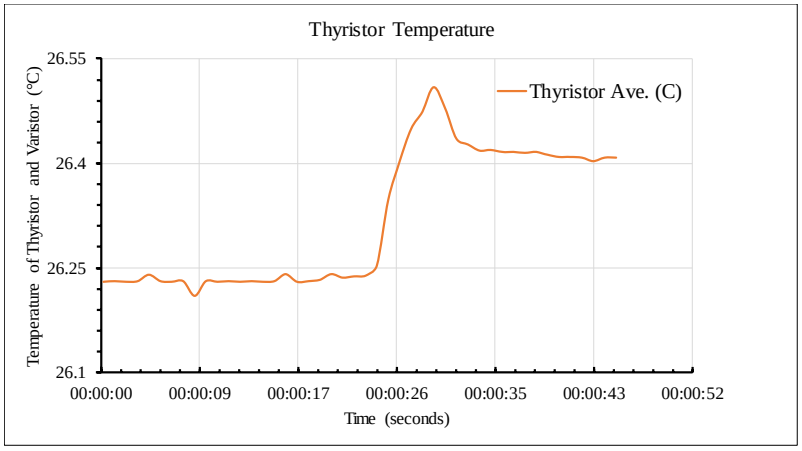

Figure 3.63: Temperature variation of thyristor- Proposed technique

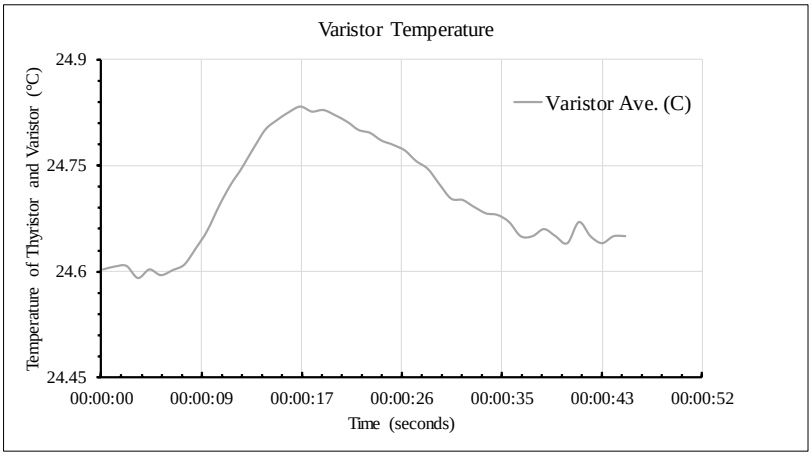

Figure 3.64: Temperature variation of varistor- Proposed technique

3.8 CONCLUSION

In this chapter a novel protection scheme has been introduced to protect the SSSC against the fault. This new technique decreases the needed protection time that can limit the fault current passes through the SSSC and also control temperature rise in the IGBTs. Also, the proposed technique can increase the reliability of the network. The SSSC has a better power flow control compared to the STATCOM and is more cost-effective in comparison with B2B-VSC compensator as well as lower power losses. It means using the SSSC can decrease the capital cost and operating cost of the network compared to the B2B-VSC. Consequently, the proposed method by removing the SSSC vulnerability against the short circuit can allow them to be utilised in the MV network.

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4 INVESTIGATING THE DC OFFSET PHENOMENA IN MEDIUM VOLTAGE NETWORKS

4.1 INTRODUCTION

Nowadays distributed generation systems (DGs) such as CHP units, PV and wind power generators have been on the rise. The increase of distributed generation causes several side effects which have been intensively studied, including reverse power flows and voltage fluctuations in power distribution networks [1]. Indeed, DGs have a great influence on the distribution network's feasible operating region, voltage stability, reliability and efficiency, which eventually puts a restriction on the DG penetration level. In addition to these, the penetration of DGs may severely affect the amplitude and characteristics of the fault current depending on the network configuration, which requires fault level management. The location of the DGs in the network as well as their ratings are very important regarding their effects in this regard [2].

Figure 4.1 shows two radial distribution feeders connected through a power electronic device SSSC (solid state series compensator) which allows controlled power exchange between the two sides, exploiting the benefits of the DGs in a wider system scope without violating the network constraints in the steady state. The SSSC which is designed to insert a fraction of the grid voltage can potentially reduce the capital cost and also power losses during normal operation, but its protection during a grid short circuit fault has been a major challenge as this would put the SSSC under the stress of the full grid voltage [3]. It has been proposed that upon a short circuit fault in the network on either side of the SSSC, both

thyristor pairs are turned on to by-pass the SSSC for protection. The thyristor gates are then prohibited in less than 5 fundamental cycles (100ms) when the SSSC has been isolated from the network, using mechanical switches of very low breaking duties after the SSSC current has been controlled down to zero. Obviously, the turning-off of the thyristors depends on the zero-crossing of the current which will be affected by the DC offset of the currents through them. Understanding the fault current characteristics is important in specifying the surge current capabilities of the thyristors.

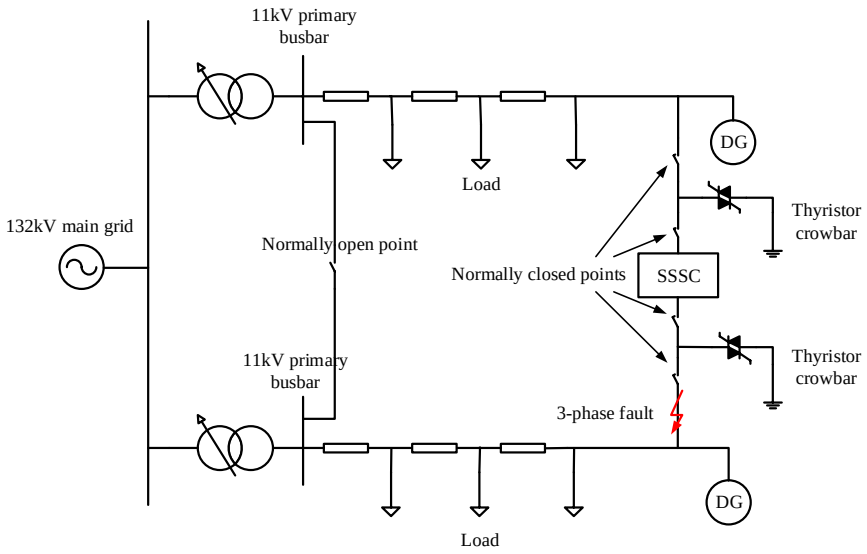


Figure 4.1: System diagram

The thyristors are normally off and hence do not induce operational power losses. It is also known that thyristors can take large surge current which can be 20 times more than the rated average current, provided that the di/dt is within the limit [4]. This current capability is highly dependent on the device temperature rise when the current passes through the thyristor. While the detailed temperature response will be studied later, this chapter reports the work on the DC component in the thyristor current in order to more accurately analyse the device temperature. Adverse DC offset can delay the zero-crossing of the short circuit current. This is a

well-known phenomenon in power transmission networks as the large synchronous generators undergo from sub transients to transients and eventually steady states [5]. This is hardly seen in distribution networks which is far from the large centralised power plants. With the introduction of distributed generation, it has now become questionable whether the DC offset in the short circuit current is still negligible.

In this chapter, the DC offset phenomenon will be investigated for both synchronous and induction machines. In the first part, synchronous machines would be studied, and the results simulated in MATLAB will be shown. And, in the second part, induction machines are analysed. Finally, this chapter will investigate the most influential parameters so that the effects on the zero-crossing could be controlled.

4.2 FUNDAMENTALS & MATHMATICS

4.2.1 Synchronous Machines

The classical 7th-order model of a synchronous machine is used with parameters shown in Table 4.1 [6].

Table 4.1: Synchronous machine parameters

X_d''	Direct-axis subtransient reactance
X_d'	Direct-axis transient reactance
X_d	Direct-axis synchronous reactance
T_d''	The subtransient time constant
T_d'	The transient time constant
T_a	The armature/Stator Time Constant, or DC time Constant

It can be shown that upon the set of a three-phase short circuit fault, the round rotor synchronous machine stator current has two components including the DC and AC which is in the d-axis:

$$I(t)=-I_{AC}(t)+I_{DC}(t)=-i_m(t)\cos(\omega t+\gamma_0)+i_m(0)e^{-t/T_a}\cos\gamma_0 \quad (4.1)$$

where $i_m(t)$ is maximum value of the current and it could be defined that:

$$I_{AC}(t)=i_m(t)\cos(\omega t+\gamma_0), \quad (4.2)$$

$$I_{DC}(t)=i_m(0)e^{-t/T_a}\cos\gamma_0 \quad (4.3)$$

where T_a is the DC time constant, and by assuming that th armature mmf is directed along the d-axis [6]:

$$i_m(t)=E_{fm}\left[\left(\frac{1}{X_d''}-\frac{1}{X_d'}\right)e^{-t/T_d''}+\left(\frac{1}{X_d'}-\frac{1}{X_d}\right)e^{-t/T_d'}+\frac{1}{X_d}\right], \quad (4.4)$$

$$i_m(0) = \frac{E_{fm}}{X_d''} \tag{4.5}$$

where $E_{fm} = \sqrt{2}E_f$ and E_f is the excitation flux which is proportional to the field current. Therefore:

$$I(t) = -E_{fm}\left[\left(\frac{1}{X_d''} - \frac{1}{X_d'}\right)e^{-t/T_d''} + \left(\frac{1}{X_d'} - \frac{1}{X_d}\right)e^{-t/T_d'} + \frac{1}{X_d}\right]\cos(\omega t + \gamma_0) + \frac{E_{fm}}{X_d''}e^{-t/T_a}\cos\gamma_0 \tag{4.6}$$

The envelope format of the current equation can be written as follows and this is illustrated in the Fig. 4.2.

$$I = -I_{AC} + I_{DC} = -E_{fm}\left[\left(\frac{1}{X_d''} - \frac{1}{X_d'}\right)e^{-t/T_d''} + \left(\frac{1}{X_d'} - \frac{1}{X_d}\right)e^{-t/T_d'} + \frac{1}{X_d}\right] + \frac{E_{fm}}{X_d''}e^{-t/T_a} \tag{4.7}$$

Main parameters of synchronous machine during fault has been shown in Table 4.1. Fig. 4.2 demonstrates the status of the fault current of a synchronous generator as well as DC and AC currents after fault separately. Moreover, sub-transient, transient, and DC time constant and their effects on the current have also been shown.

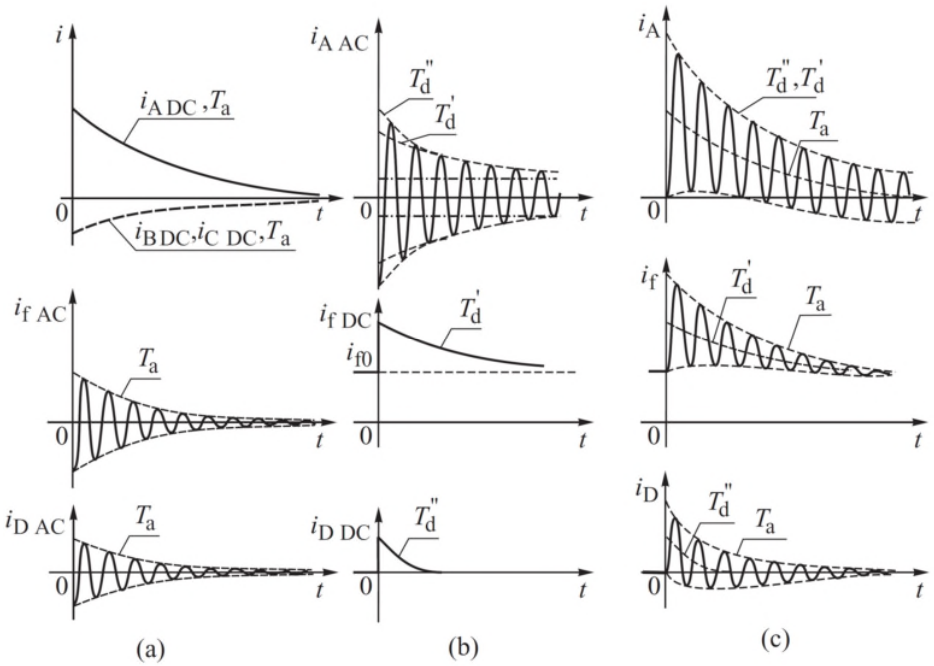


Figure 4.2: Short-circuit currents in the round rotor generator [6]

In Fig. 4.2, (a) DC component of the phase current and the corresponding AC component of the field and damper winding current; (b) AC component of the current in phase and the corresponding DC component of the field and damper winding current; (c) the resulting current in phase, the field and the damper winding as the sum of the currents shown in (a) and (b). [6]

4.2.1.1 Formulating the AC and DC components

To simplify the formulation of the AC and DC components; it is assumed that the synchronous machine during the short circuit is on no load situation. Then, the AC and DC components are formulated as below.

4.2.1.1.1 AC Component

In this case, pre-fault internal emf voltages are equal to the terminal voltage:

$$E'' = E' = E = E_f = Vg \tag{4.8}$$

Where E'', E', E, and V_g are subtransient, transient, steady state, and terminal voltages, respectively.

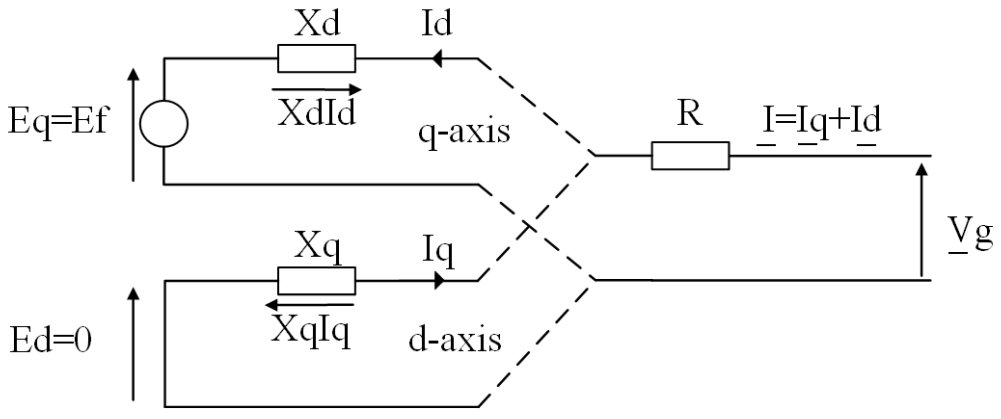


Figure 4.3: The equivalent circuit of d-axis and q-axis of a synchronous machine in the steady state [6]

R is the armature resistance which in the case of the synchronous generator this resistance is very small and can be neglected. Therefore, equivalent circuit of the synchronous generator for sub-transient, transient and steady state could be depicted as follows:

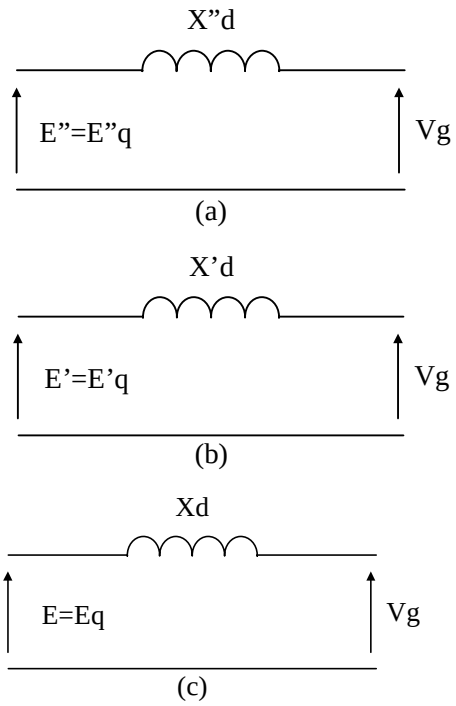


Figure 4.4: Equivalent circuit for a synchronous generator on no load condition in (a) the subtransient state; (b) the transient state; (c) the steady state [6]

Consequently, in line with Fig. 4.4, the envelope format of $i_m(t)$ could be simplified as [6]:

$$i_m(t)=\Delta i'' e^{-t/T_d''}+\Delta i' e^{-t/T_d'}+\Delta i \tag{4.9}$$

$$\Delta i=i_m^{\infty}=E_{fm}/X_d, \quad \Delta i+\Delta i'=i_m'=E_{fm}/X_d', \quad \Delta i+\Delta i'+\Delta i''=i_m''=E_{fm}/X_d'' \tag{4.10}$$

$$i_m(t)=E_{fm}\left[\left(\frac{1}{X_d''}-\frac{1}{X_d'}\right)e^{-t/T_d''}+\left(\frac{1}{X_d'}-\frac{1}{X_d}\right)e^{-t/T_d'}+\frac{1}{X_d}\right] \tag{4.11}$$

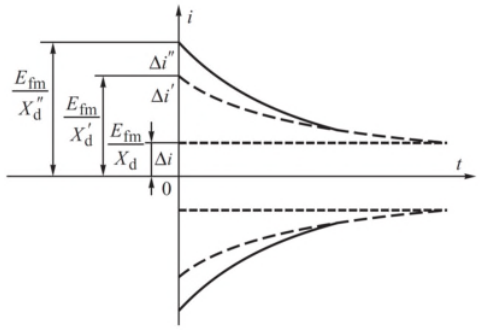


Figure 4.5: Envelopes of the three characteristic AC components of the short-circuit current [6]

4.2.1.1.2 DC Component

The DC component value for generators can be obtained by the below equation [6]:

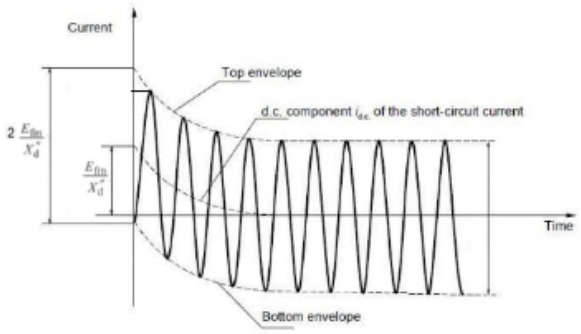
$$\frac{E_{fm}}{2} e^{-t/T_a}[(\frac{1}{X_d^{"}}+\frac{1}{X_q^{"}})\cos\gamma_0+(\frac{1}{X_d^{"}}-\frac{1}{X_q^{"}})\cos(2\omega t+\gamma_0)] \quad (4.12)$$

However, in case of high-rated generators which including the damper windings in both axes, because $X_q^{"}$ is equal to $X_d^{"}$ the equation can be rewritten as [6]:

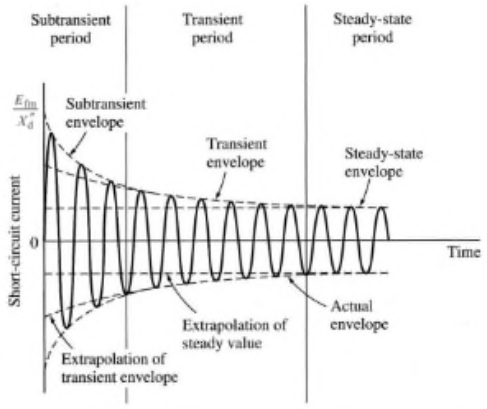
$$\frac{E_{fm}}{X_d^{"}} e^{-t/T_a}\cos\gamma_0 \quad (4.13)$$

Therefore, the short-circuit current for Phase A can be presented as [6]:

$$i_A(t)=-E_{fm}\left[\left(\frac{1}{X_d^{"}}-\frac{1}{X_d^{'}}\right)e^{-t/T_d^{"}}+\left(\frac{1}{X_d^{'}}-\frac{1}{X_d}\right)e^{-t/T_d^{'}}+\frac{1}{X_d}\right]\cos(\omega t+\gamma_0)+\frac{E_{fm}}{X_d^{"}}e^{-t/T_a}\cos\gamma_0 \quad (4.14)$$



(a)



(b)

Figure 4.6: Envelopes of the AC and DC components of the short-circuit current. (a) Phase current and corresponding DC component. (b) Corresponding AC components [7, 8]

4.2.1.2 DC offset Calculations

According to the equation (4.7), if the changes of the AC component in the envelope format is smaller than that of the DC, it means that during the first cycle, the short circuit current will cross the zero-point, as shown in Fig. 4.6; otherwise, it will miss that.

If:

$$\frac{E_{fm}}{X_d''}e^{-t/T_a} > E_{fm}\left[\left(\frac{1}{X_d''}-\frac{1}{X_d'}\right)e^{-t/T_d''}+\left(\frac{1}{X_d'}-\frac{1}{X_d}\right)e^{-t/T_d'}+\frac{1}{X_d}\right] \rightarrow \text{missing the zero point} \qquad (4.15)$$

Else:

$$\frac{E_{fm}}{X_d''} e^{-t/T_a} \leq E_{fm} \left[\left(\frac{1}{X_d''} - \frac{1}{X_d'} \right) e^{-t/T_d''} + \left(\frac{1}{X_d'} - \frac{1}{X_d} \right) e^{-t/T_d'} + \frac{1}{X_d} \right] \rightarrow \text{Crossing the zero point} \quad (4.16)$$

The sub-transient period lasts for up to 5 cycles [9,10,11] as shown in Fig. 4.7. Furthermore, based on the obtained simulation results shown in Fig. 4.7, it is obvious that for synchronous generators greater than 500 kVA the change of short circuit current is very small and perhaps negligible (less than 10%) in the subtransient period. In Fig. 4.8 the value of the transient current ($E_{fm} * \left(\frac{1}{X_d'} - \frac{1}{X_d} \right) e^{-t/T_d'}$) in the period of the subtransient time constant ($t=T_d''$) has been calculated and compared with its maximum initial value (when t=0) for different machines. Moreover, according to Table 4.2, most machines connected to 11 kV networks are 1 MW and greater, hereby, small-rate machines, less than 500 kVA, are actually rare in practice. Thus, it can be supposed that the amount of transient current during the mentioned period for generators greater than 500kVA is fixed and therefore, the enveloped form of the AC component in (4.7) could be simplified as follows:

$$I_{AC} = E_{fm} \left[\left(\frac{1}{X_d''} - \frac{1}{X_d'} \right) e^{-t/T_d''} + \frac{1}{X_d'} \right] \quad (4.17)$$

Table 4.2: CHP electrical capacity in 2011[12]

	Less than 100 KWe	100 KWe but less than 1 MWe	1 MWe but less than 10 MWe	10 MWe and greater	Total
England	**28**	**213**	**695**	**4387**	**5323**
East Midlands	2	13	31	189	234
Eastern	2	20	64	198	285
London	4	29	93		126
North East	2	8	51	849	910
North West	5	34	102	598	739
South East	5	47	837		889
South West	2	20	58	0	80
West Midlands	3	20	81	0	104
Yorkshire/Humberside	4	21	76	1855	1956
Scotland	1	15	61	452	529
Wales	3	14	194		210
Northern Ireland	1	8	40		49
UK Total	33	250	828	5000	6111

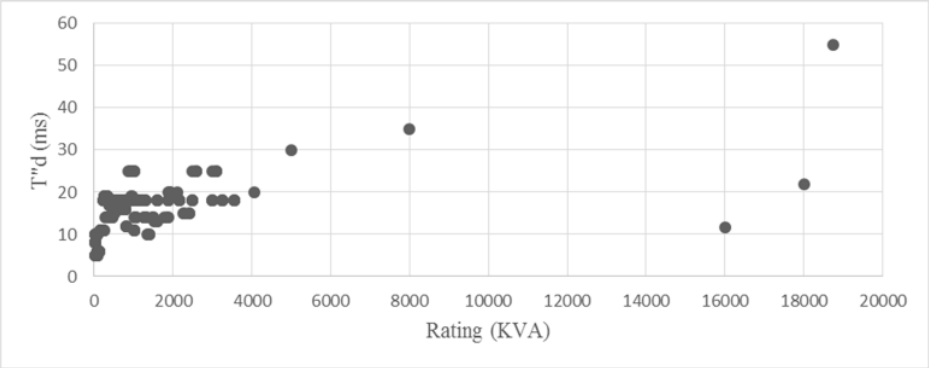


Figure 4.7: Synchronous machine: T"d vs. rating

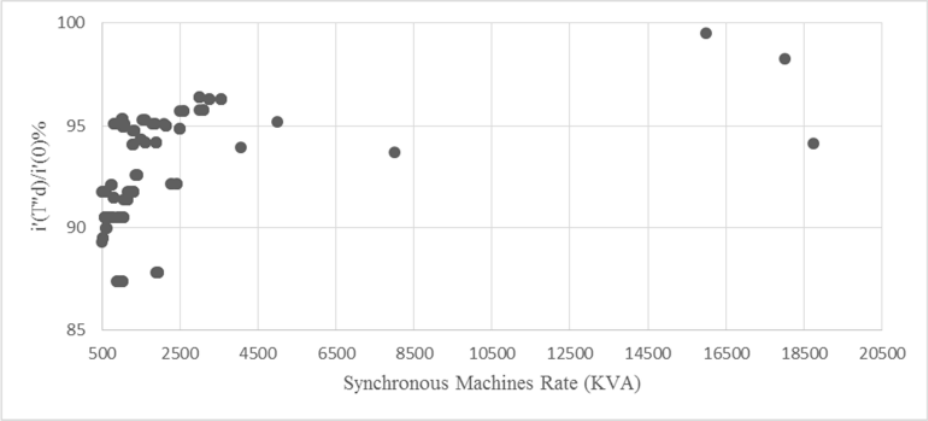


Figure 4.8: Synchronous machine: the ratio of transient current amount in sub-transient time constant period to maximum value of transient current vs. rating

By comparing the enveloped AC and DC components after simplifying as follows:

$$I_{DC}(t) > I_{AC}(t) \rightarrow I_{DC}(t) - \frac{E_{fm}}{X_d'} > I_{AC}(t) - \frac{E_{fm}}{X_d'} = E_{fm}\left[\frac{1}{X_d''}e^{-t/T_a} - \frac{1}{X_d'}\right] > E_{fm}\left[\frac{1}{X_d''}e^{-t/T_d''} - \frac{1}{X_d'}e^{-t/T_d''}\right] \quad (4.18a)$$

$$I_{DC}(t) < I_{AC}(t) \rightarrow I_{DC}(t) - \frac{E_{fm}}{X_d'} < I_{AC}(t) - \frac{E_{fm}}{X_d'} = E_{fm}\left[\frac{1}{X_d''}e^{-t/T_a} - \frac{1}{X_d'}\right] < E_{fm}\left[\frac{1}{X_d''}e^{-t/T_d''} - \frac{1}{X_d'}e^{-t/T_d''}\right] \quad (4.18b)$$

Thus, from equations (4.18a and 4.18b), it is clear that for times (t) bigger than zero $\frac{1}{X_d'} > \frac{1}{X_d'}e^{-t/T_d''}$. Therefore, if $T_a \leq T_d''$ then, $\frac{1}{X_d''}e^{-t/T_a} \leq \frac{1}{X_d''}e^{-t/T_d''}$. Consequently, for $T_a \leq T_d''$, it can be said that the changes of AC current are actually greater than DC current. Even for some values of $T_a > T_d''$ the DC component is still equal or smaller than the AC one. Thus, the current will cross the zero point in the first cycle. As a result, one of conditions for missing the zero point is when the T_a is "enough bigger" than T_d''.

It is obvious that if $T_a > 5T_d''$ the equations (4.15 and 4.16) could be simplified as (4.19):

$$\frac{E_{fm}}{X_d''}e^{-t/T_a} \approx E_{fm}\left[\left(\frac{1}{X_d'} - \frac{1}{X_d}\right)e^{-t/T_d'} + \frac{1}{X_d}\right] \quad (4.19)$$

and, if $T_a > 5T_d'$:

$$\frac{E_{fm}}{X_d''} e^{-t/T_a} \approx E_{fm} \left[\frac{1}{X_d}\right] \tag{4.20}$$

Therefore, by calculating the above equations (4.18), (4.19), or (4.20) the crossing time would be obtained. But, because in the most cases the existing conditions have more correspondence with equation (4.18), thereby, using this equation has been considered in this chapter for obtaining the crossing time of the current.

Then, for calculating the ratio of changes of the AC and DC currents by using equation (4.7), it could be written that:

$$\Delta I_{AC} = I_m - I_{AC}(t) = \frac{E_{fm}}{X_d''} - E_{fm}\left[\left(\frac{1}{X_d''} - \frac{1}{X_d'}\right) e^{-\frac{t}{T_d''}} + \frac{1}{X_d'}\right] = E_{fm}\left[\frac{1}{X_d''} - \frac{1}{X_d'}\right] - E_{fm}\left[\left(\frac{1}{X_d''} - \frac{1}{X_d'}\right) e^{-\frac{t}{T_d''}}\right] \tag{4.21}$$

$$\Delta I_{DC} = I_m - I_{DC}(t) = \frac{E_{fm}}{X_d''} - \frac{E_{fm}}{X_d''} e^{-\frac{t}{T_a}} = \frac{E_{fm}}{X_d''}\left[\left(1 - e^{-\frac{t}{T_a}}\right)\right] \tag{4.22}$$

so,

$$\frac{\Delta I_{DC}(t)}{\Delta I_{AC}(t)} = \frac{X_d'}{X_d' - X_d''} \frac{1 - e^{-\frac{t}{T_a}}}{1 - e^{-\frac{t}{T_d''}}} \tag{4.23}$$

By assuming $\lambda = \frac{X_d'}{X_d''}$, it can be rewritten that:

$$\frac{\Delta I_{DC}(t)}{\Delta I_{AC}(t)} = \frac{\lambda}{\lambda - 1} \frac{1 - e^{-\frac{t}{T_a}}}{1 - e^{-\frac{t}{T_d''}}} \tag{4.24}$$

By considering the outcomes of simulation, Fig. 4.9, it can be shown that if:

$\frac{\Delta I_{DC}}{\Delta I_{AC}} > 1.25$, then current will cross the zero point in the first cycle.

$\frac{\Delta I_{DC}}{\Delta I_{AC}} \leq 1.25$, then current will miss the zero point in the first cycle.

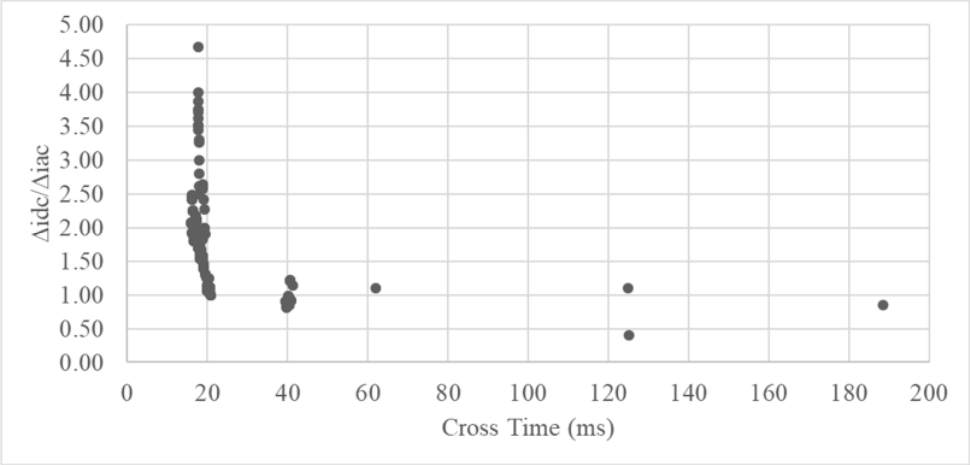


Figure 4.9: Synchronous machine: Δidc/Δiac vs. cross time

It can be further shown that by considering $\frac{X_d^{'}}{X_d^{''}} \geq 2$ and $\frac{T_a}{T_d^{''}} \geq 2$ simultaneously the value of $\frac{\Delta I_{DC}(t)}{\Delta I_{AC}(t)}$ would be smaller than 1.25, thereby the zero point will be missed. In fact, by replacing $\frac{X_d^{'}}{X_d^{''}} = 2$, $\frac{T_a}{T_d^{''}} = 2$ and $t=T_d^{''}$ in (4.24):

$$\frac{\Delta I_{DC}(t)}{\Delta I_{AC}(t)} = \frac{2}{2-1}\frac{1-e^{-\frac{1}{2}}}{1-e^{-1}} \cong 1.25 \qquad (4.25)$$

Moreover, by comparing the parameters of various synchronous machines it becomes clear that the mentioned ratio is acceptable. According to Table 4.3, it can be seen that when both ratios, $\frac{X_d^{'}}{X_d^{''}}$ and $\frac{T_a}{T_d^{''}}$, are bigger than 2 the current will miss the zero point in the first cycle. Moreover, in this situation the ratio of $\frac{\Delta I_{DC}}{\Delta I_{AC}}$ would be smaller than 1.25. Besides, by considering Table 4.4 it could be shown that when only one of ratios is bigger than 2 e.g. either $\frac{T_a}{T_d^{''}}$ is bigger than 2, if the ratio $\frac{T_a}{T_d^{''}} / \frac{X_d^{'}}{X_d^{''}}$ will be bigger than 2, consequently, the ratio of $\frac{\Delta I_{DC}}{\Delta I_{AC}}$ would become less

than 1.25, and hereby the current also will miss the zero point in the first cycle. Therefore, it could be concluded that if:

Status 1: $\frac{X_d^{'}}{X_d^{''}}>2$ and $\frac{T_a}{T_d^{''}}>2 \rightarrow$miss the cross point, (4.26)

Status 2: $\left[\frac{X_d^{'}}{X_d^{''}}\geq 2 \text{ or } \frac{T_a}{T_d^{''}}\geq 2\right]$ and $\frac{T_a}{T_d^{''}}/\frac{X_d^{'}}{X_d^{''}}>2 \rightarrow$miss the cross point (4.27)

Otherwise, the current will cross the zero point in the first cycle.

Table 4.3: Ratio and cross time of synchronous machines for status 1

Ratings (kVA)	A= $\frac{T_a}{T_d^{''}}$	B=$\frac{X_d^{'}}{X_d^{''}}$	A/B	Cross-time(ms)	$\frac{\Delta I_{DC}}{\Delta I_{AC}}$
820	2.75	2.14	1.28	39.585	0.90
1020	3.00	2.22	1.35	39.795	0.82
1050	2.29	2.11	1.08	20.055	1.06
1300	2.43	2.07	1.17	20.37	1.03
1500	2.64	2.00	1.32	20.895	1.00
1600	2.85	2.17	1.31	40.005	0.87
1850	2.86	2.21	1.29	40.425	0.85
2500	2.08	2.18	0.95	20.58	1.11
3000	2.14	2.00	1.07	20.055	1.24
3000	2.50	2.20	1.14	40.32	0.96
3100	2.14	2.00	1.07	20.055	1.24
3100	2.14	2.00	1.07	20.055	1.25
3250	2.50	2.01	1.25	20.685	1.04
3550	2.50	2.14	1.17	40.215	0.98
18000	2	2.305	0.868	124.84	1.1

Fig. 4.10 shows that the ratio $\frac{T_a}{T_d''}$ is greater than 2 for generators bigger than 1 MVA; therefore it means by increasing the rating of the generators their DC component is becoming greater as well and the possibility of missing the zero point in first cycle increases. According to Fig. 4.11, it can be seen that regardless the machine rating, the ratio of $\frac{X_d'}{X_d''}$ for most cases is equal to or greater than 2. By considering the Fig. 4.12, it is obvious that $\frac{T_a}{T_d''}/\frac{X_d'}{X_d''}$ for just a few cases is over than 2 and theses cases most often miss the zero point in the first cycle.

Table 4.4: Ratios and cross time of synchronous machines for status 2

Ratings (kVA)	A= $\frac{T_a}{T_d''}$	B=$\frac{X_d'}{X_d''}$	A/B	Cross-time(ms)	$\frac{\Delta I_{DC}}{\Delta I_{AC}}$
2100	3.5	1.462	2.395	20.37	1.245
2265	4.53	1.346	3.367	40.53	1.217
2290	4.53	1.349	3.361	40.53	1.211
2410	4.533	1.348	3.364	40.53	1.214
2410	4.53	1.349	3.361	40.53	1.21
4050	6	1.271	4.7197	41.37	1.138
8000	3.7433	1.51	2.480	62.055	1.1
5000	3.333	1.48	2.247	20.685	1.248
16000	9.402	1.664	5.649	125.16	0.4
18750	4	1.702	2.35	188.475	0.85

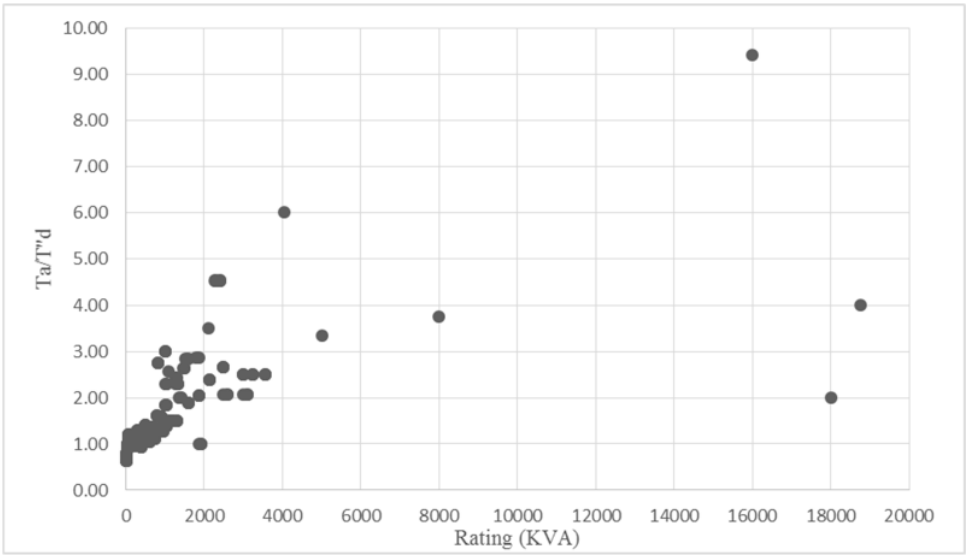


Figure 4.10: Synchronous machine, Ta/T"d vs. machines rating

Regarding the Fig. 4.13, it could be seen that for most synchronous machines with rating smaller than 1 MVA, in the first cycle short circuit current will pass through zero and in none of the conditions missing the zero point is an issue. Although, for machines bigger than 2 MVA, most cases will miss the zero point in the first cycle because one of the mentioned conditions would be valid about them. Therefore, it could be concluded that the larger synchronous machines would give the worst cases for producing the DC offset and then making a delay in turning off the thyristor devices and putting off their turn-off time to after the first cycle.

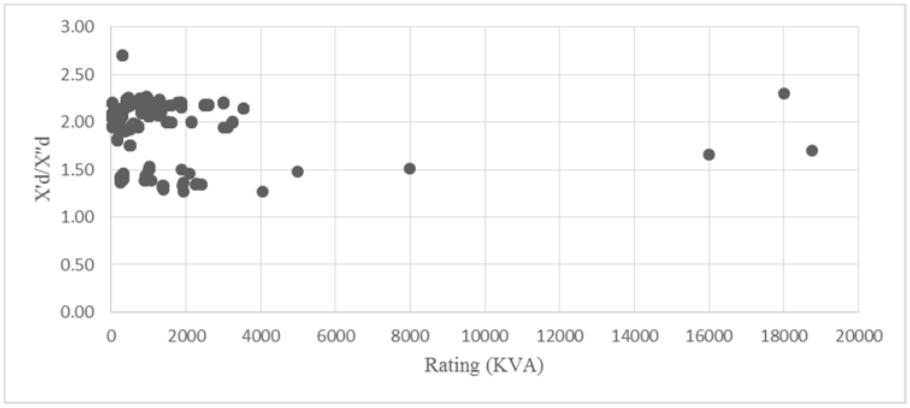


Figure 4.11: Synchronous machine: X'd/X"d vs. rating

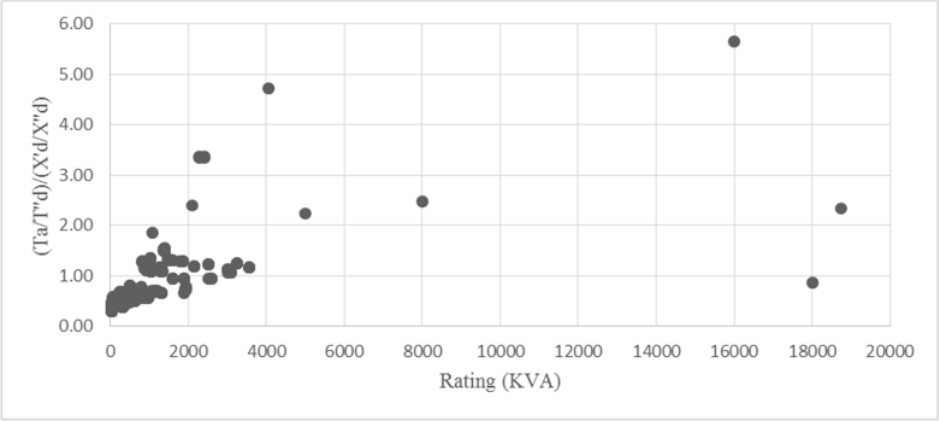


Figure 4.12: Synchronous machine: (Ta/T"d)/(X'd/X"d) vs. rating

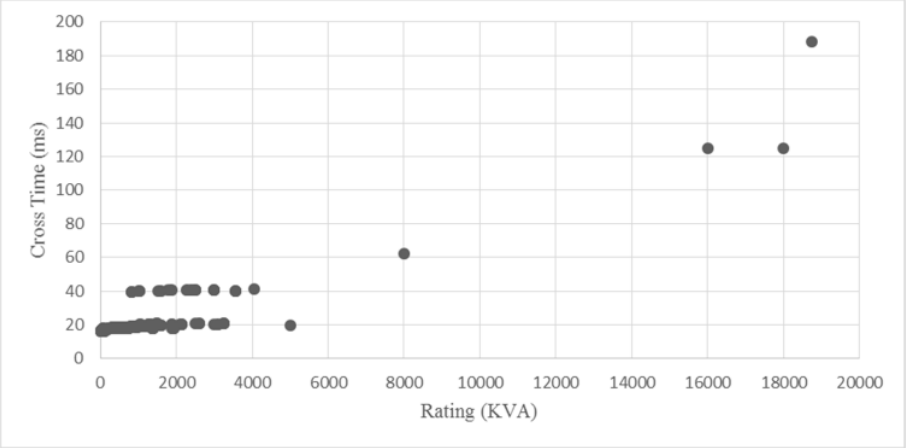


Figure 4.13: Synchronous Machine: Cross time (ms) vs. rating (kVA)

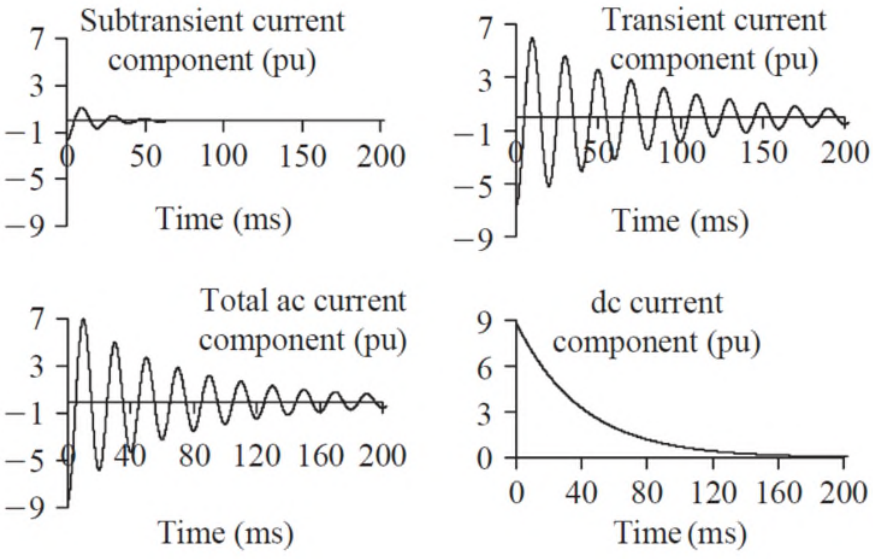


Figure 4.14: Three-phase short-circuit fault at the terminals of a double-cage induction motor from no load: components of phase short-circuit current [13].

4.2.2 Induction Machines

The induction machine conditions and equations during the fault and the production of the DC offset are similar to the synchronous machines. The main difference is in the steady state when the current of the induction machine will be zero while for the synchronous machine the AC current will be constant, Fig. 4.14. But, for investigating the conditions of crossing or missing the zero point during the first cycle, the same scenario, which has been used for synchronous machines, can be used in this case as well.

Table 4.5: Induction machine parameters

V_m	Peak value of stator voltage
$X_{\sigma s}$	Stator Leakage reactance
X_m	Magnetising reactance
S	Rotor Slip
$X_d^{''}$	Direct-axis subtransient reactance
$X_d^{'}$	Direct-axis transient reactance
X_d	Direct-axis synchronous reactance.
$T_d^{''}$	The subtransient time constant
$T_d^{'}$	The transient time constant
T_a	The armature/stator time constant
θ_0	The rotor position when a fault may happen

For a double-cage induction machine, the fault current could be written as follows [13]:

$$i_r(t)=\frac{V_m}{(1-s)}\left[\left(\frac{1}{X'}-\left(\frac{1}{X_{\sigma s}+X_m}\right)\right)e^{-t/T'}+\left(\frac{1}{X''}-\frac{1}{X'}\right)e^{-t/T''}\right]\cos\left[(1-s)W_s t+\theta_0-\frac{\pi}{2}\right]-\frac{V_m}{(1-s)}\frac{1}{X''}e^{-t/T_a}\cos\left(\theta_0-\frac{\pi}{2}\right) \quad (4.28)$$

and for a single cage [16]:

$$i_r(t)=\frac{V_m}{(1-s)}\left[\left(\frac{1}{X'}-\left(\frac{1}{X_{\sigma s}+X_m}\right)\right)e^{-t/T'}\right]\cos\left[(1-s)W_s t+\theta_0-\frac{\pi}{2}\right]-\frac{V_m}{(1-s)}\frac{1}{X'}e^{-t/T_a}\cos\left(\theta_0-\frac{\pi}{2}\right) \quad (4.29)$$

The motor slip ‘s’ is typically less than 1% for large machines and less than 4-5% for smaller machines so that it could be ignored in equations. On the other hand, since using single cage is more conventional than double cage and most of datasheets are based on single cage. For this reason, in this chapter the single-cage machine has been considered. Thus, for a single-cage induction machine, the fault current for the peak current envelop for any time instant, can be given as follows [13]:

$$i_r(t)=V_m\left[\left(\frac{1}{X'}-\left(\frac{1}{X_{\sigma s}+X_m}\right)\right)e^{-t/T'}+\left(\frac{1}{X''}-\frac{1}{X'}\right)e^{-t/T''}+\frac{1}{X''}e^{-t/T_a}\right] \quad (4.30)$$

or

$$i_r(t)=\sqrt{2}\left[(I'-I)e^{-t/T'}+\left(I''-I'\right)e^{-t/T''}\right]+\sqrt{2}I''e^{-t/T_a} \quad (4.31)$$

or

$$i_r(t)=\sqrt{2}I_{ac}(t)+I_{dc}(t) \quad (4.32)$$

where

$$I=\frac{V_{rms}}{X_{\sigma s}+X_m},\ I'=\frac{V_{rms}}{X'},I''=\frac{V_{rms}}{X''} \quad (4.33)$$

and

$$I_{dc}(t)=\sqrt{2}I''e^{-t/T_a}, \quad (4.34)$$

$$I_{ac}(t) = (I' - I)\mathrm{e}^{-t/T'} + \left(I'' - I'\right)\mathrm{e}^{-t/T''} \tag{4.35}$$

$$\mathrm{i_r(t)} = \mathrm{V_m}\left[\left(\frac{1}{X'} - \left(\frac{1}{X_{\sigma s} + X_m}\right)\right)\mathrm{e}^{-t/T'} + \frac{1}{X'}\mathrm{e}^{-t/T_a}\right] \tag{4.36}$$

or

$$\mathrm{i_r(t)} = \sqrt{2}(I' - I)\mathrm{e}^{-t/T'} + \sqrt{2}I''\mathrm{e}^{-t/T_a} \tag{4.37}$$

or

$$\mathrm{i_r(t)} = \sqrt{2}I_{ac}(\mathrm{t}) + I_{dc}(t) \tag{4.38}$$

where

$$I_{dc}(t) = \sqrt{2}I''\mathrm{e}^{-t/T_a}, \tag{4.39}$$

and

$$I_{ac}(t) = (I' - I)\mathrm{e}^{-t/T'} \tag{4.40}$$

Table 4.6: Rating and fault current zero-crossing time for induction machines

Ratings (kVA)	f (Hz)	t	T/t	Cross- time (ms)
3.7285	60	0.00237	7.04275	15.435
5.59275	60	0.00092	18.09828	14.385
7.457	60	0.00068	24.59977	14.175
14.914	60	0.00220	7.58846	15.435
18.6425	60	0.00080	20.63604	14.28
22.371	60	0.00046	36.47989	13.965
55.9275	60	0.0034	4.89863	16.17
74.57	60	0.00204	8.1691	15.54
111.855	60	0.00220	7.58809	15.54
149.14	60	0.00183	9.11835	15.54
372.85	60	0.00360	4.63515	16.17
1677.825	60	0.00584	2.85582	16.59
3504.79	50	0.01374	1.21344	34.44
900	60	0.01635	1.22330	20.58

Because single cage is more common than double cage and most of datasheets are based on single cage, therefore, by considering (4.26) as a base equation it could be said that [16]:

$$i_r(t)=I_{ac}(t)+I_{dc}(t),\quad I_{dc}(t)=\frac{1}{X'}e^{-t/T_a}=I'e^{-t/T_a},\ I_{ac}(t)=\left(\frac{1}{X'}-\left(\frac{1}{X_{\sigma s}+X_m}\right)\right)e^{-t/T'}=(I'-I)\,e^{-t/T'} \quad (4.41)$$

Then, for obtaining the time that the current will cross the zero-point it can be said that:

$$I_{ac}(t)=I_{dc}(t)\rightarrow\left(\frac{1}{X'}-\left(\frac{1}{X_{\sigma s}+X_m}\right)\right)e^{-t/T'}=\frac{1}{X'}e^{-t/T_a} \quad (4.42)$$

By considering (4.42) as a base equation, the time when AC and DC components are equal, can be obtained by:

$$\frac{\mathrm{Ln}\left(\frac{X-X'}{X}\right)}{\frac{1}{T}-\frac{1}{T_a}}=t \tag{4.43}$$

Because the first cycle has priority in this case, by assuming $T=\frac{1}{f}$:

$$\text{If: } \frac{T}{t}\leq 2 \rightarrow \text{miss the zero point in the first cycle}$$

$$\text{Otherwise: } \frac{T}{t}>2 \rightarrow \text{cross the zero point in the first cycle}$$

According Table 4.6 and Figures 4.15 and 4.16 which are based on time domain simulation results, the mentioned ratios are valid about the conditions of induction machines.

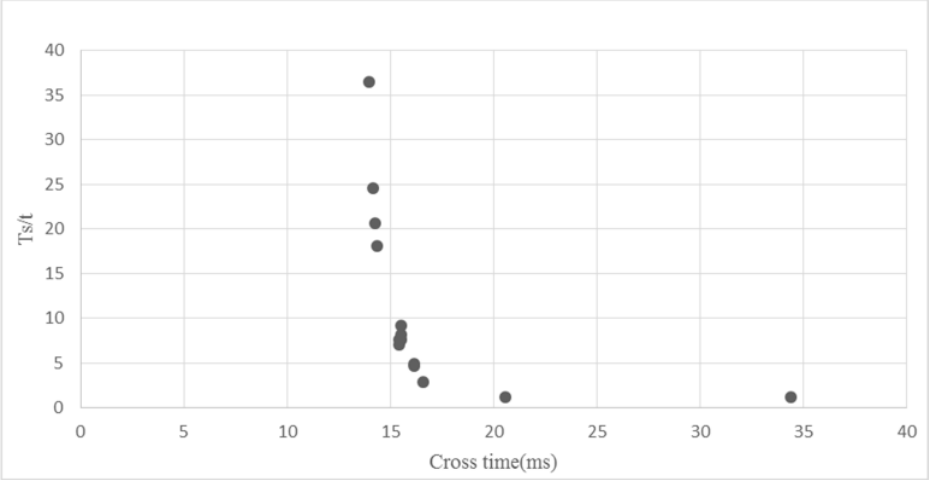


Figure 4.15: Induction machines, Ts/t vs. cross time

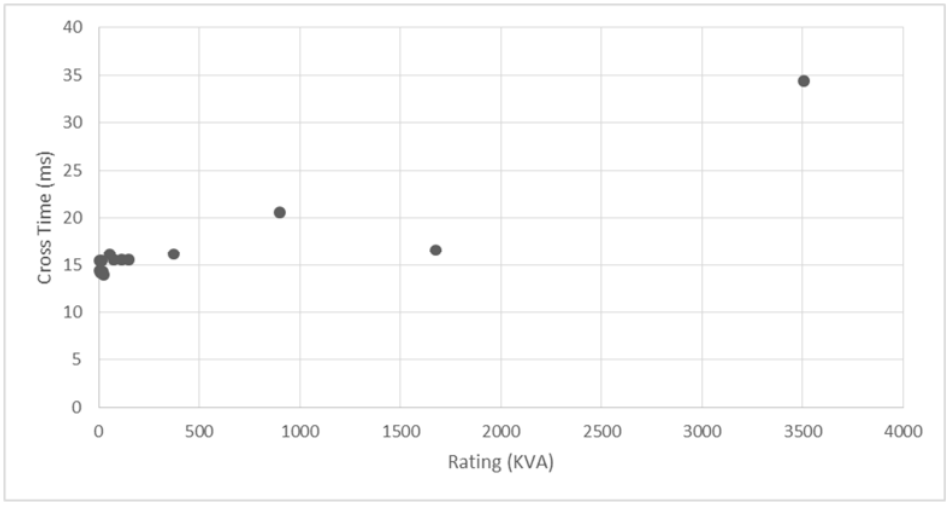


Figure 4.16: Induction machines, cross time vs. rating (kVA)

4.3 EFFECT OF LOCATION AND NUMBER OF MACHINES

The distance of machines to the fault is one of the factors affecting the DC offset. A far distance from the fault location will decrease the DC offset and vice versa. Table 4.7 shows the distance effect in conditions that one 16 MVA generator has placed in different positions with respect to the fault location, from 0 to 20 km distance. It can be seen that by increasing the distance the DC offset impact is reduced because of the effect on the time constants, especially the DC time constant in the stator circuit. For instance, DC time constant will be calculated as [14]:

$$T_a = (X_d^{''} + X_e) / \omega(R_a + R_e) \tag{4.44}$$

Moreover, the effect of the number of generators on the DC offset is shown in Table 4.8 using more smaller generators for proving that they collectively can cause less DC offset in comparison with a single big synchronous generator and compared in two situations 0 and 10 km away from the fault.

Finally, the effects of changing both the distance and number of generators have been shown in Table 4.9.

Table 4.7: Distance effect

16MVA Synchronous Machine	
Distance (km)	Crossing Time (ms)
0	125.16
5	13.9
10	13.0
15	12.6
20	12.4

Table 4.8: Number effect

Distance = 0 km	
Number/MVA	Crossing Time (ms)
4*4	40.01
2*8	58.9
1*16	125.16

Table 4.9: Distance and number effect

Distance=10 km	
Number /MVA	Crossing Time (ms)
4x4	14.3
2x8	12.7
1x16	13.0

4.4 CONCLUSION

This chapter presents a study on the DC offset in the fault current in an MV distribution network with local synchronous and/or induction machines. The aim of this study is analysing the impact and the value of the DC offset in the MV network during a short circuit. Also, by using mathematical calculations the way of obtaining this value is demonstrated. The most effective parameters are determined and then it is depicted how they can have an effect on the DC offset during a fault. This study helps to have a better understating of an MV network during the fault. In fact, the DC offset can cause some troubles for some kinds of protection devices during their turning-off process such as thyristors and circuit breakers. These devices need the current to cross the zero line when they are switching off or becoming open.

Machine equations and time domain simulation are used to identify the conditions when a sustained non-zero current period would occur. For this purpose, different kinds of machines connected to 11 kV grid have been analysed. Besides, the machine specifications have been extracted from various datasheets of manufacturers', companies, books and MATLAB library. It is shown that the larger machines give rise to worse cases in way of generating the DC offset in the network as well as by changing the resistance and inductance of network it is possible to affect the DC offset value and thus crossing time. Most of the used data sheets have been extracted from MarelliGenerators®, AvK-Alternators, and STAMFORD® data sheets as well as from the data utilised in some related books and articles [13,15-20].

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5 A METHOD TO CONTAIN THE TEMPERATURE RISE OF A PRESS-PACK THYRISTOR DURING A SHORT CIRCUIT PROTECTION OPERATION

5.1 INTRODUCTION

As the demand for dynamic loads and distributed generators continue to increase, the reliability and voltage stability of medium voltage power networks have encountered serious control challenges. These include voltage regulation, power quality control and an increase in the short circuit level during normal operation and fault conditions. To address these challenges, power electronic compensators play an important role by adjusting the magnitude and phase angle of the compensating voltage and/or current. There is a number of different compensators which may be used in MV networks to meet the grid requirements such as back-to-back (B2B) voltage source converters (VSCs), shunt converters or static synchronous series compensators (SSSC). SSSC is a cost-effective solution due to the partial voltage rating for the same control capability during normal operation, compared to other compensators such as B2B VSCs. The system power losses can also be reduced as the system requires fewer switching devices. However, the main difficulty is to protect the series compensator during a short circuit in the network during which full voltage will be applied to the SSSC [1]. A new method based on thyristor-crowbars can be used to decrease the time-delay of the protection process [1-2], Fig. 5.1.

When a fault is recognised by the relevant relays, the thyristor-crowbars will be turned on and the fault current passes through them to

isolate the SSSC from the network. This results in a large current which may be chosen as 15~20 times higher than the continuous current rating of the thyristor. Therefore, the thyristor temperature will rise quickly. It is critical to keep the temperature within a safety margin in the system during the grid short circuit fault. In this chapter, a new method which utilises the PCM to control the temperature of the thyristor is proposed to permit a large current through the thyristor and hence reduce the system cost [2-3]. The PCM's large latent heat enables it to quickly store the thermal energy during the melting process and is potentially ideal for the intended application. Depending on the thyristor dimension and the required application, the PCM can be placed outside or inside of the press-pack. If the heat can transfer from silicon to the case during a few milliseconds, putting the PCM outside the press-pack might be enough. In case the heat transfer exceeds a few milliseconds, it could be more practical to put the PCM inside the press-pack for a faster temperature reduction and a decrease of time delay. In this chapter, an outside container has been investigated first.

5.2 PHASE CHANGE MATERIAL

The conventional method for keeping down the temperature of thyristor is using the Heat Sink as a single side or double-side cooling systems. Heat sinks can be mounted on the cathode copper side or anode one or both sides to absorb the thyristor heat during its operation. During the normal operation using the heat sink is reasonable. But if the thyristors are used in critical occasions such as a fault phenomenon, because the temperature of thyristor is rising very quickly to the top tolerable value by thyristor, thus the heat sinks used for the normal operation are no longer suitable to keep down the temperature and they have to be enlarged that this will require a great cost. Another way for cooling thyristors could be using the phase change materials (PCM) instead of heat sinks. They are cheaper and lighter than heat sink facilities, so there is no limitation in required amount of them despite the heat sink which takes up a greater place.

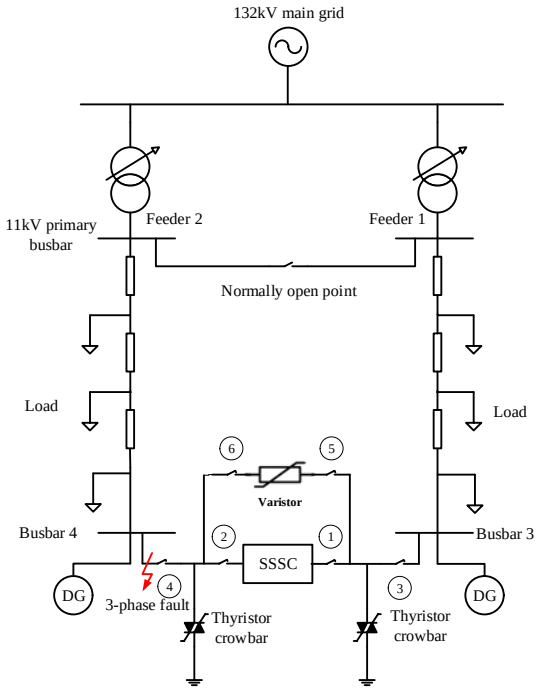


Figure 5.1: Typical MV network with multiple feeders linked by SSSC

PCMs are a good choice for thermal management solutions. Because of their ability in storing and releasing the thermal energy during the process of melting and freezing. When a substance freezes or condenses, it releases large amounts of energy in the form of latent heat of fusion, or energy of crystallisation. Conversely, when this substance is melted or evaporated, an equal amount of energy is absorbed from the surrounding environment while changing from solid to liquid. This feature of PCMs can be used in several ways, such as thermal energy storage which can be very practical in cooling purposes. The way of PCM operation can be shown as the following figure, Fig. 5.2:

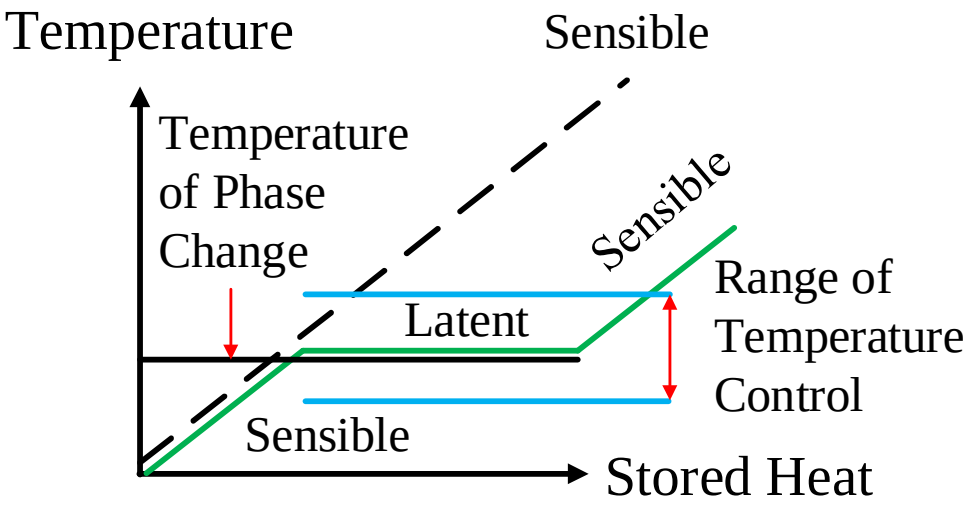


Figure 5.2: The process of the phase changing for a PCM

The PCM heat can be obtained from equation (5.1):

$$Q=m^* C_p^*\Delta T_{solid}+m^*L+m^* C_p^*\Delta T_{liquid} \quad (5.1)$$

where Q is the amount of released or absorbed energy, m is the mass of substance, ΔT_{solid} is the temperature difference in the solid state, ΔT_{liquid} is the temperature difference in the liquid state, L is the latent heat, Cp is the specific heat at constant pressure.

In this research, a new technique for clamping the thyristor temperature has been proposed by using the PCM materials. The purpose of this technique is absorbing the released heat from the thyristor by using PCM to maintain its temperature in the secure rate. The feature of using PCM than heatsink is that the PCM will take up a smaller space and also will be the more cost effective. In this way, the thermal model of thyristor has been used for comparing with obtained results from COMSOL Multiphysics which has been employed for simulating the thyristor temperature during fault and also the PCM effect on controlling the thyristor temperature.

5.3 THERMAL MODEL

The transient thermal behaviour of semiconductor components is described in two dominant thermal network models: partial fraction circuit model (Foster model), see Fig. 5.3, and continued fraction circuit model (Cauer model), see Fig. 5.4. The simple definition of using these models is that the generated heat by a single unit-step heating source flows perpendicularly to the surface of the semiconductor device from the source [4].

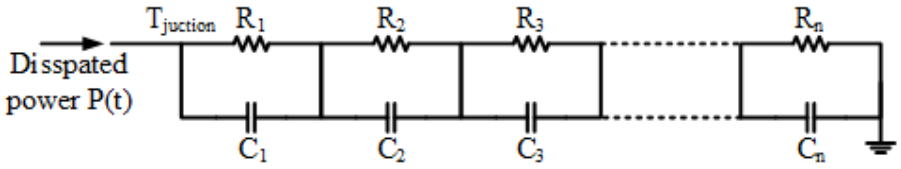


Figure 5.3: Foster thermal equivalent circuit model

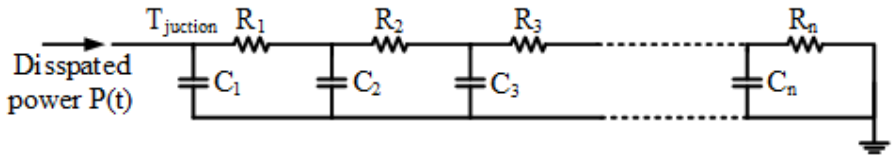


Figure 5.4: Cauer thermal equivalent circuit model

The Foster model's mathematical expressions is:

$$Z(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i}) \tag{5.2}$$

$$\tau = R_i C_i \tag{5.3}$$

where the thermal resistance R_i and thermal time constant τ_i can be obtained from the standard curve fitting algorithm by the measured thermal impedance [5].

The Foster model is only describing the thermal behaviour of the measured system, but not its physical behaviour. Therefore, it is only valid for a single thermal system to describe the thermal behaviour at the input node (the device's junction). That is the reason, it cannot be used to determine the temperature distribution within the device, nor to combine the thermal network with extended thermal system. In the Foster model, the heat enters the left hand side and leaves the right hand side of the thermal system at the same time. In reality, it takes time for heat generated from the device junction to propagate into the cooling system.

The Cauer model can describe the same thermal impedance as the Foster model in case of same constant temperature at the right hand side of the thermal circuit. Unlike the Foster model, the Cauer Model is closely related to the concept of "structure function" [6] that it can correctly describe the internal temperature distribution and the propagation of heat between nodes in a thermal system. For a thermal system including more than one sub-thermal system, the total system can be the series connection among the Cauer circuits of these sub-thermal system. Although the Cauer model has some advantages over the Foster model, it has a complicated mathematical representation in the time domain and also it is difficult to determine the parameters of R_i and C_i for a Cauer model, because the direct calculation of these parameters relates to the material properties of the device. That is why, manufacturer only provides the thermal impedance in Foster Model. But the transformation from Foster model to Cauer model for the same thermal system is available by using the standard circuit transformations [7].

5.3.1 Transforming the Foster Model to the Cauer Model

The transformation from Foster model to Cauer model is executed in the frequency domain. By applying Laplace transformation to equation (5.2), the transfer function of a Foster model is:

$$Z_{thF}(s) = \sum_{i=1}^{n} \frac{R_{thi}}{1 + sR_{thi}C_{thi}} \tag{5.4}$$

The transfer function of a Cauer model in continued fraction expression is written as:

$$Z_{thC}(s) = \cfrac{1}{s_1 C_{th1} + \cfrac{1}{R_{th1} + \cfrac{1}{sC_{th2} \cdots + \cfrac{1}{R_{thn}}}}} \tag{5.5}$$

The recurrence relation of equation (5.4) is used as the form of:

$$\frac{1}{Z_{thCn}(s)} = sC_{thC1} + \frac{1}{R_{thC1} + Z_{thCn-1}(s)} \tag{5.6}$$

The partial fraction representation of the transfer function of the Foster model, shown in equation (5.4), can be formulated into the rational function as:

$$Z_{thFn}(s) = \frac{f_n(s)}{g_n(s)} \tag{5.7}$$

$$\frac{f_n(s)}{g_n(s)} = \frac{f_1 s^{n-1} + f_2 s^{n-2} + \cdots + f_{n-1}s + f_n}{g_1 s^n + g_2 s^{n-1} + \cdots + g_n s + g_{n+1}} \tag{5.8}$$

The polynomial degree of $f_n(s)$ is one degree smaller than that of $g_n(s)$. Since $Z_{thCn}(s)=Z_{thFn}(s)$, by substituting equation (5.7) into equation (5.6), the following equation can be deduced:

$$\frac{g_n(s)}{f_n(s)} = sC_{thC1} + \frac{1}{R_{thC1} + Z_{thCn-1}(s)} \tag{5.9}$$

By substituting equation (5.8) into equation (5.9) and decomposing equation (5.9) using the standard Euclidean algorithm into a polynomial linear *s* and a rational function $rem_n(s)/f_n(s)$ as the remainder, it can be deduced:

$$\frac{g_n(s)}{f_n(s)} = \frac{g_1}{f_1}s + \frac{rem_n(s)}{f_n(s)} \tag{5.10}$$

$$\begin{aligned} rem_n(s) &= g(s) - \frac{g_1}{f_1}s \bullet f_n(s) \\ &= (g_2 - \frac{g_1}{f_1}f_2)s^{n-1} + (g_3 - \frac{g_1}{f_1}f_3)s^{n-2} + \cdots + (g_n - \frac{g_1}{f_1}f_n)s + g_{n+1} \end{aligned} \tag{5.11}$$

The functions $rem_n(s)$ and $f_n(s)$ have the same polynomial degree. By comparing equation (5.10) with equation (5.9), the first Cauer thermal capacitance can be determined by:

$$C_{thC1} = \frac{g_1}{f_1} \tag{5.12}$$

and

$$\frac{1}{R_{thC1} + Z_{thCn-1}(s)} = \frac{1}{\frac{f_n(s)}{rem_n(s)}} \tag{5.13}$$

By substituting equation (5.10) into (5.13) and applying the Euclidean algorithm, the rational function $f_n(s)/rem_n(s)$ can be decomposed into:

$$\frac{f_n(s)}{rem_n(s)} = \frac{f_1^2}{g_1 f_2 - g_2 f_1} + Z_{thCn-1}(s) \tag{5.14}$$

and

$$R_{thC1} = \frac{f_1^2}{g_1 f_2 - g_2 f_1} \tag{5.15}$$

The new $Z_{thCn-1}(s)$ can be defined by $f_{n-1}(s)/g_{n-1}(s)$ by using the same transformation method, and then R_{thC2} and C_{thC2} can be obtained. Until all Cauer R_{th} and C_{th} are calculated, the algorithm continues.

5.4 METHODOLOGY

In order to evaluate the effects that the PCM has on clamping the thyristor temperature, a press-pack thyristor, with the characteristics outlined in Table 5.1, has been selected for a laboratory study. In this case, a customized test configuration has been developed which may be seen in Fig 5.5. To achieve a fast response the traditional aluminium heatsinks have been replaced by the proposed heatsink integrating the PCM. Gallium metal as the PCM is embedded into a copper container as the new heatsink, as may be seen in Fig 5.6. Specialist fins were designed into the structure to increase the thermal conductivity. The thermal properties of Gallium are listed in Table 5.2.

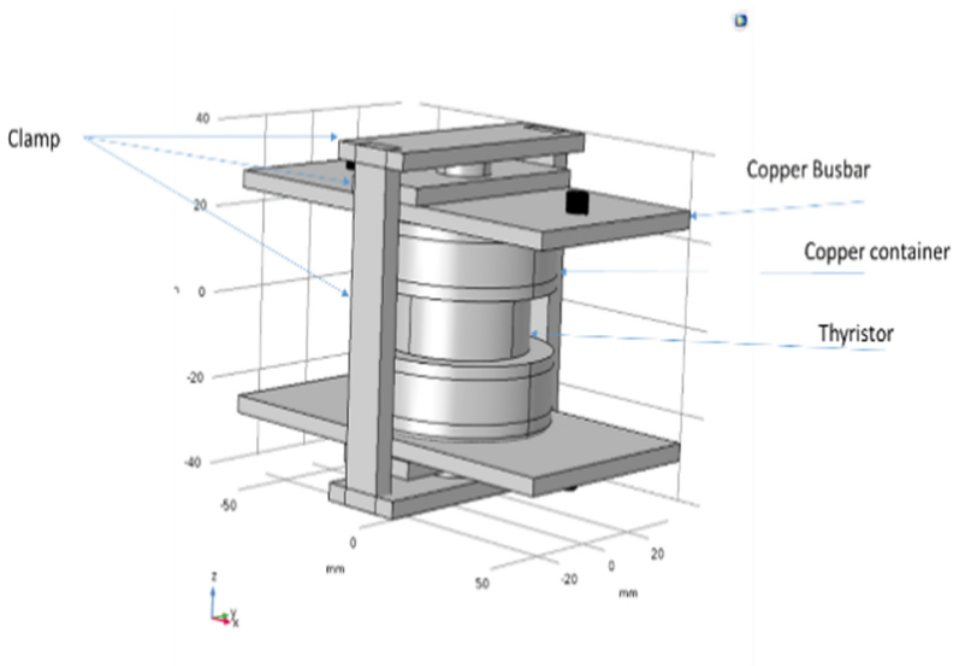


Figure 5.5: Structure diagram of 600A/1600V PCM integrated press-pack thyristor

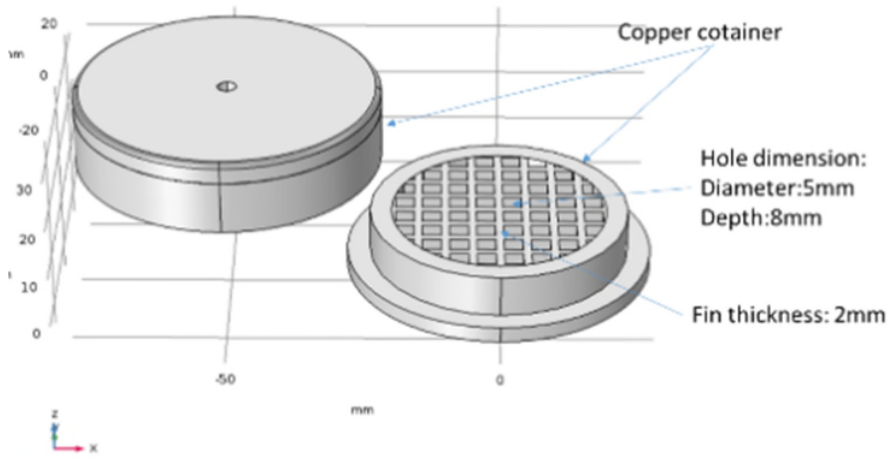


Figure 5.6: Designed container for holding PCM

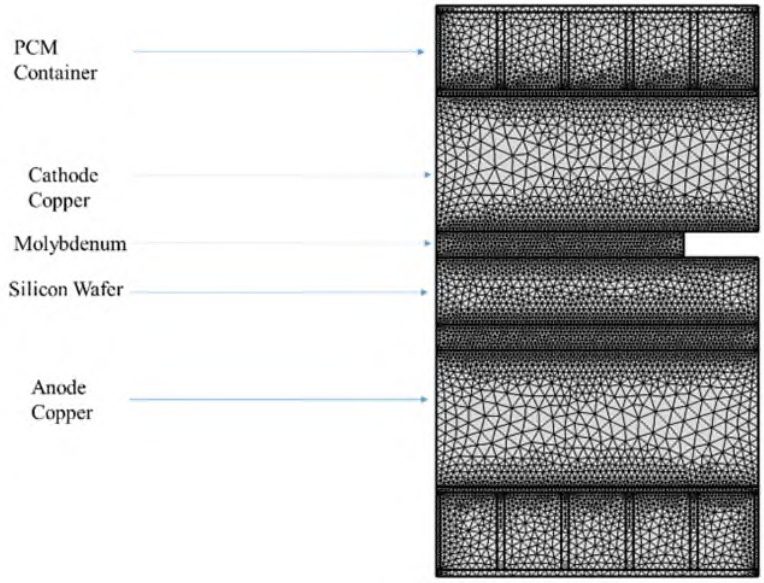


Figure 5.7: FEM model in COMSOL Structure scheme in COMSOL, number of elements: 47400

Table 5.1: Features of used Thyristor

Manufacturer	**Type**	**V_{RRM} (V)**	**I_{TAV} @ T_c (A @ °C)**	**I_{TSM} @ T_j (A @ °C, t_p=10ms)**	**$R_{c\text{-}s}$ (°C/W), θ=180°sin/DC Double side cooling**
Infineon	T390N	1600	381 @ 85	4900 @ 25	0.062/0.055

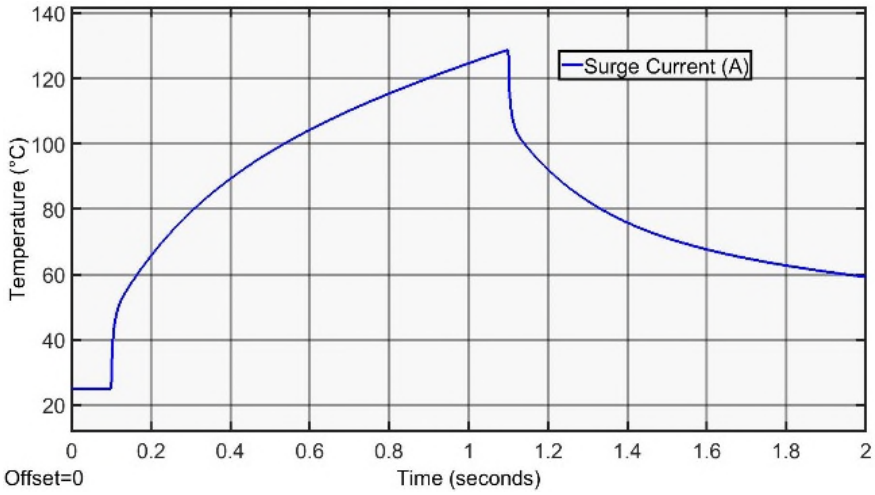
Table 5.2: Gallium metal properties

Density (g/cm3)	**Thermal Conductivity (W/m·K)**	**Specific Heat (J/g·K)**	**Phase Change Temperature (°C)**	**Latent Heat (J/g)**
5.91	40.6	0.37	29.76	80.4

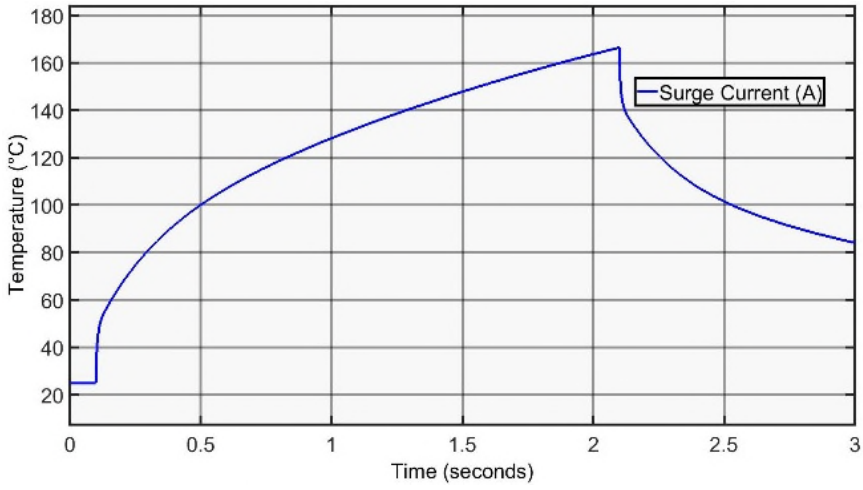
To drive the thyristor's junction temperature to its maximum allowable T_{vjmax} (125°C), 800A DC was passed through the thyristor in two tests: (1) for 1 second (2) for 2 seconds. The temperature of the thyristor during these conditions has been analysed in both the absence and the presence of the proposed the PCM heatsink. These situations are also modelled in COMSOL, Fig 5.7. It is worthwhile to note that in distribution networks, especially low voltage ones, the fault period can last for more than 1 second due to the repetitive faults or relay time setting [8-9]. However, in Medium voltage networks, this time would be too long so the entire protection procedure from the moment when a fault happens until the circuit breakers are opened or fault is removed has to be up to 200ms.

5.5 SIMULATION RESULTS

In this section, both simulation results from MATLAB and finite element modelling (FEM) in COMSOL are shown. First, the junction temperature has been determined by using a Foster network model in MATLAB with 800A DC current passing through the thyristor for 1 second and 2 seconds, Fig 5.8(a) and (b), where the temperature will be 128°C and 166°C, respectively. The aim of using this modelling is to match the introduced Foster model, using the thyristor's datasheet, with



(a) 800A DC/1s



(b) 800A DC/2s

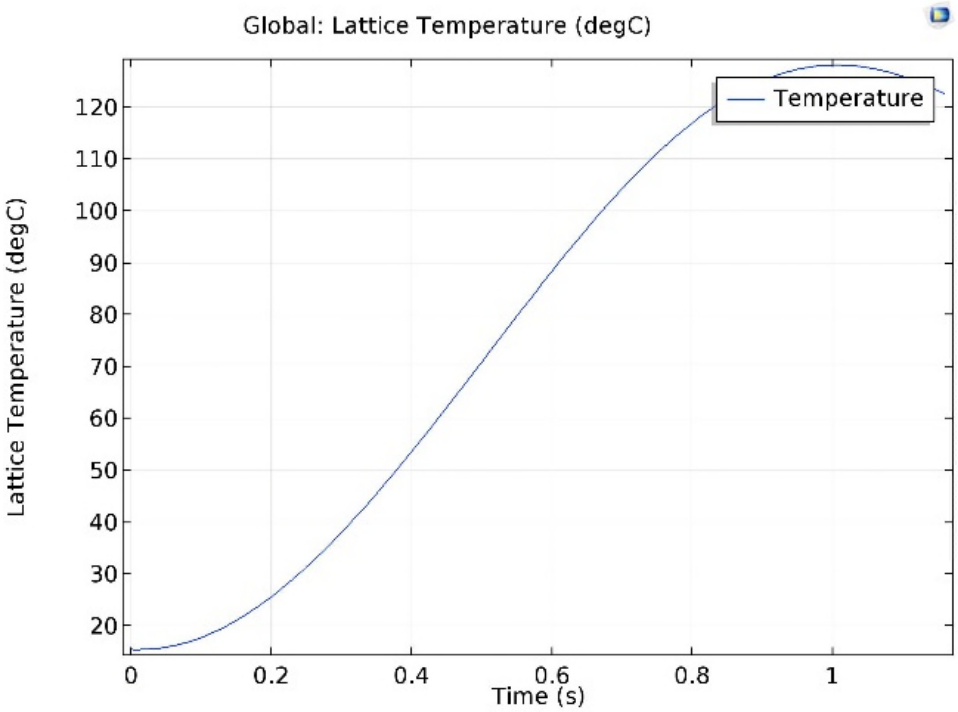
Figure 5.8 (a) and (b): Thyristor temperature by using the foster model in MATLAB

the modelled thyristor in the FEM. Then by using the FE model of the thyristor, the temperature of the same modelled thyristor was obtained (Fig. 5.9 (a) and (b)) which shows a good agreement with the simulated results. Then the thyristor including the proposed heatsink underwent conditions with 800A DC current passing through it for 1 second and 2 seconds as shown in Fig. 5.9 (c)-(f). The purpose of this FE model is to investigate the PCM effectiveness and also the delay time the heat flux takes for transfer from the silicon wafer to the case. The delay is very important in choosing the proper PCM; because it determines the required melting point.

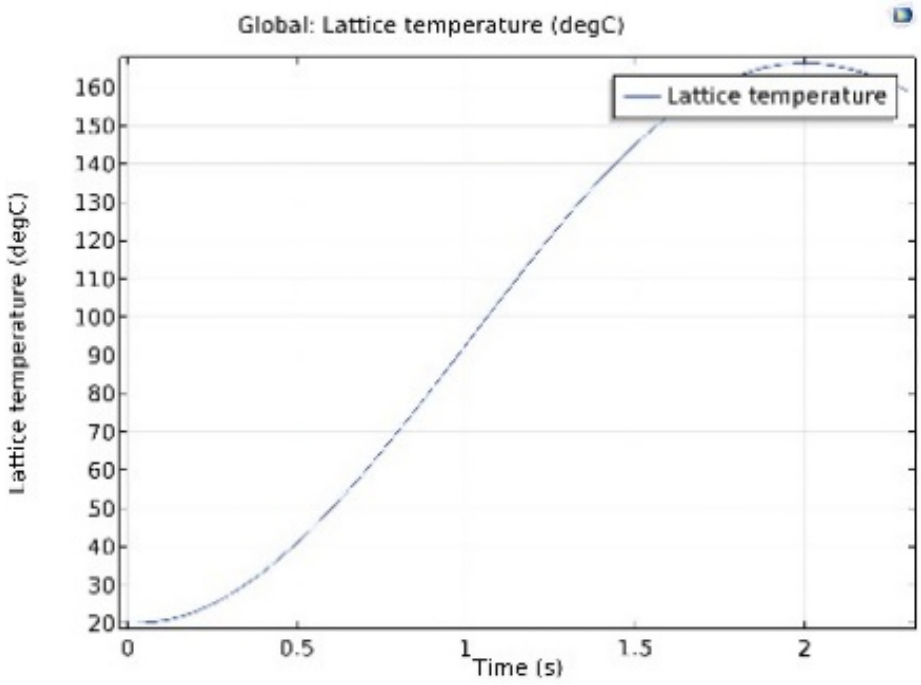
It may be seen in Fig. 5.9 that the PCM can effectively absorb the heat and thus reduces the temperature rise by 21°C. Table 5.3 shows the reduced temperature during this process, the thermal impedance, the used PCM material in this case study as well the absorbed heat by the PCM. The measured temperature in the presented results belongs to the silicon wafer which can be controlled by keeping the case temperature approximately constant by using the PCM. Fig 5.9 (e) and (f) show the temperature distribution within the press-pack thyristor during the peak temperature value and whilst the PCM heatsink has already been used.

Table 5.3: Thyristor thermal results

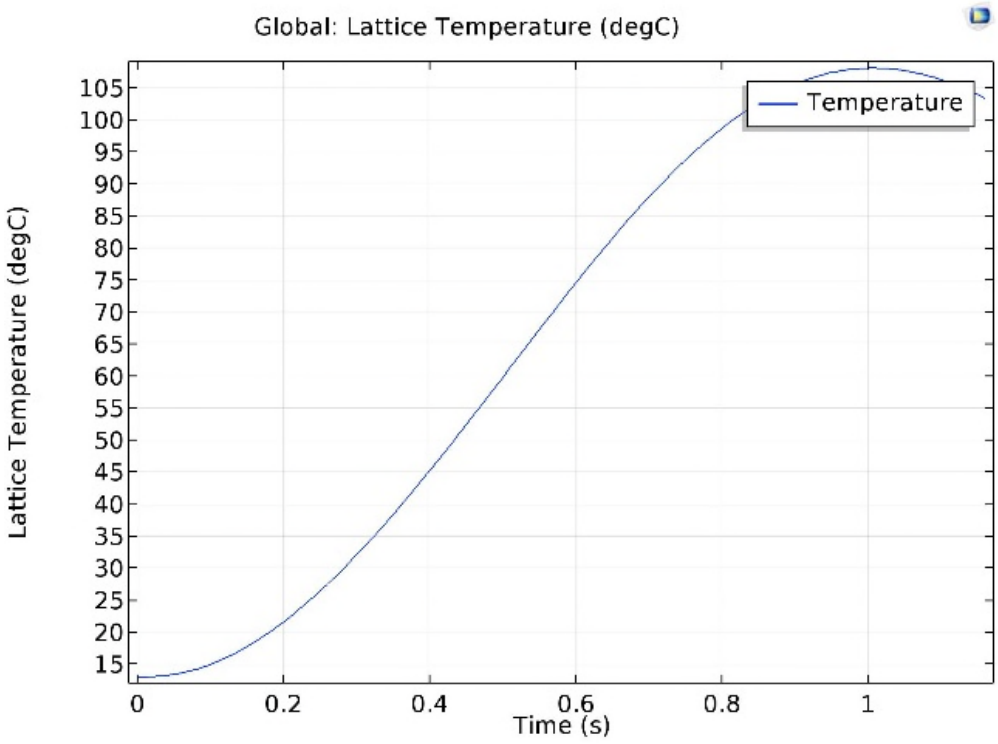
Time of test (second)	**Thermal Impedance/ no heatsink (°C/W)**	**Temperature (°C)**	**Thermal Impedance/PCM heatsink (°C/W)**	**Expected reduced temperature (°C)**	**Temperature after using PCM heatsink (°C)**	**Real reduced temperature (°C)**	**Required PCM for absorbing heat (grams)**	**Maximum Absorbed Heat by PCM (J)**
1	0.08	128	0.062	30	107	21	25-each side	338
2	0.10	166	0.086	30	144	21	25-each side	495



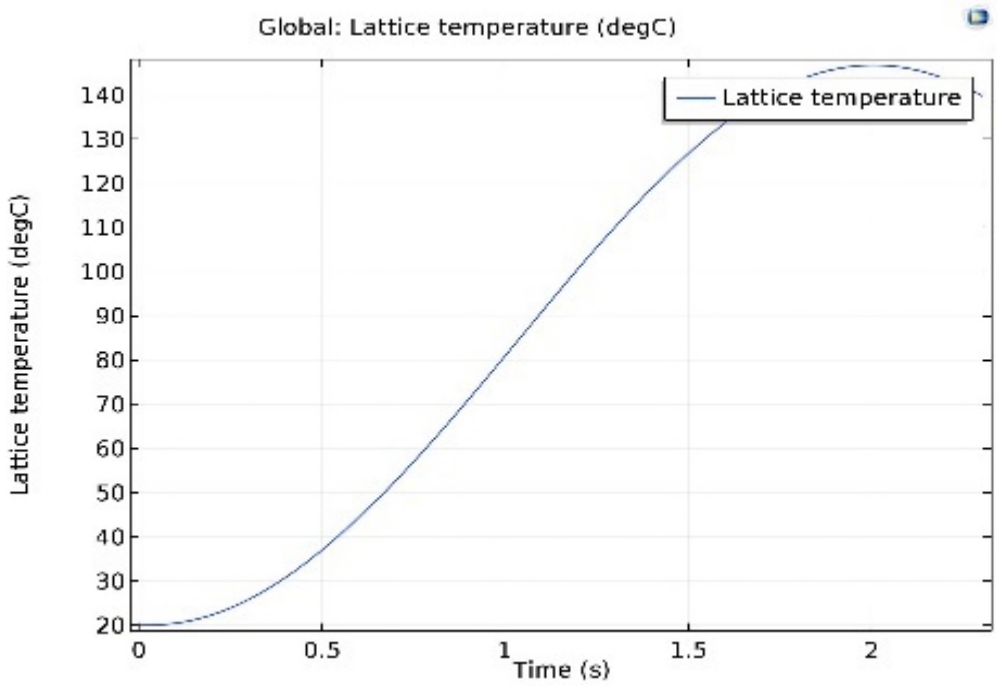
(a) Without heatsink/1s



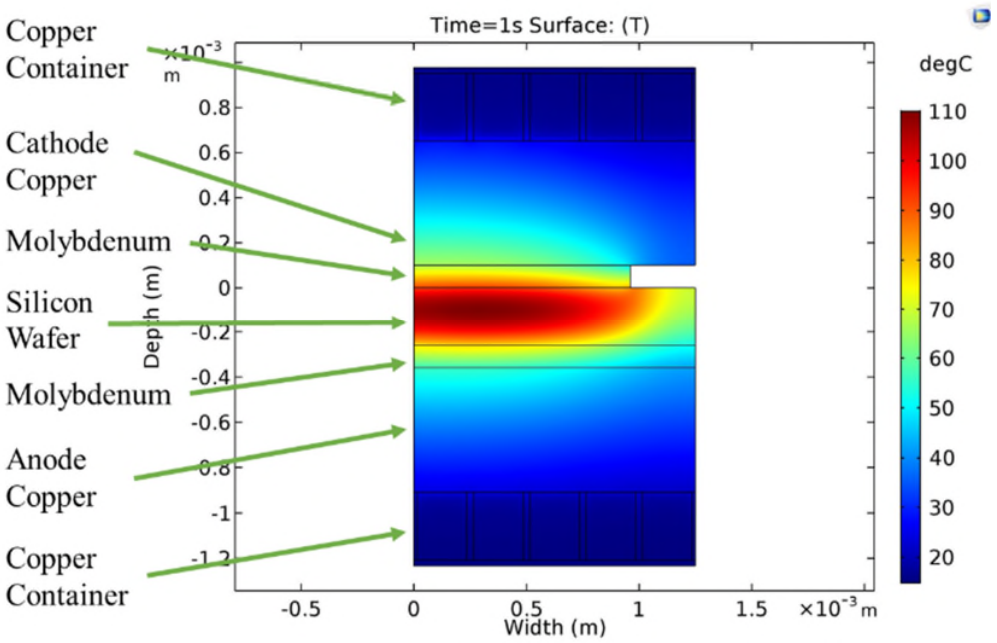
(b) Without heatsink/2s



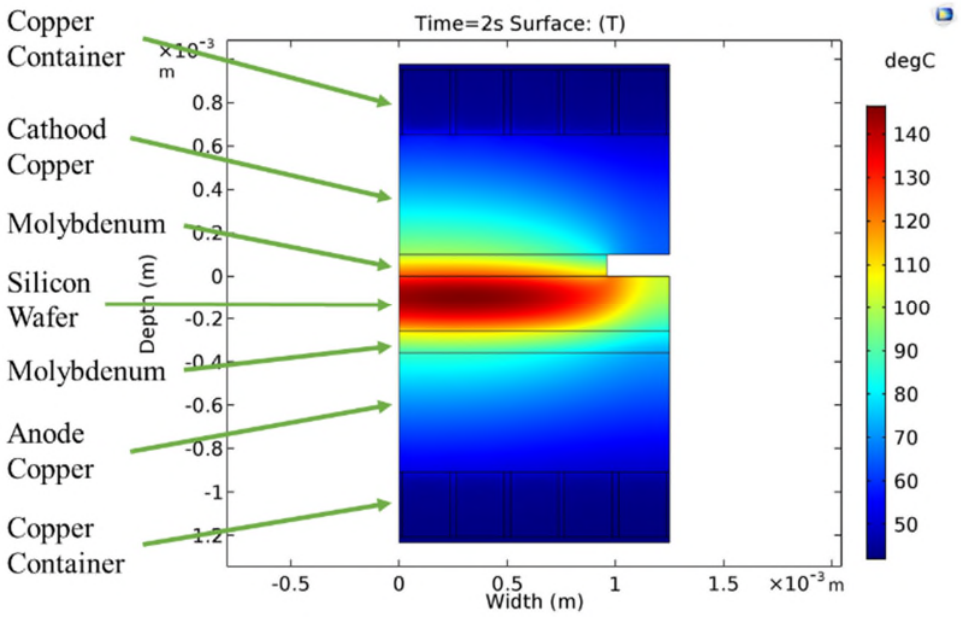
(c) PCM heatsink/1s



(d) PCM heatsink/2s



(e) PCM heatsink/1s



(f) PCM heatsink/2s

Figure 5.9 (a)-(f): Thyristor temperature by using the COMSOL modelling

The utilised power supply in this study is 800A/10V DC current source. First of all, the thermal impedance calculated by using the following equation $T_j = Z_{thjc} \times P(t) + T_{case}(t)$ where T_j, Z_{thj}, P(t) and T_{case} are junction temperature, thermal impedance, thyristor power losses and case temperature, respectively. Then, by using the temperature difference (21°C), which depends on the used volume of the PCM (25 grams on each side in this case) and the obtained thermal impedance, the absorbed heat can be estimated. Furthermore, using this technique will decrease the space required for thyristor heatsink (61mm x 61mm x 20mm-each side) compared to the use of a conventional heatsink (150mm x 129mm x 57mm-each side) based on the datasheet. It means the volume of the conventional Al heatsink is roughly 14 times higher than the proposed one. The volume and type of the PCM depends on the intended heat which has to be absorbed and the intended operating temperature of the thyristor, respectively. The I-V characteristics of the modelled thyristor of Infineon, Table 5.1, has shown in Fig. 5.10.

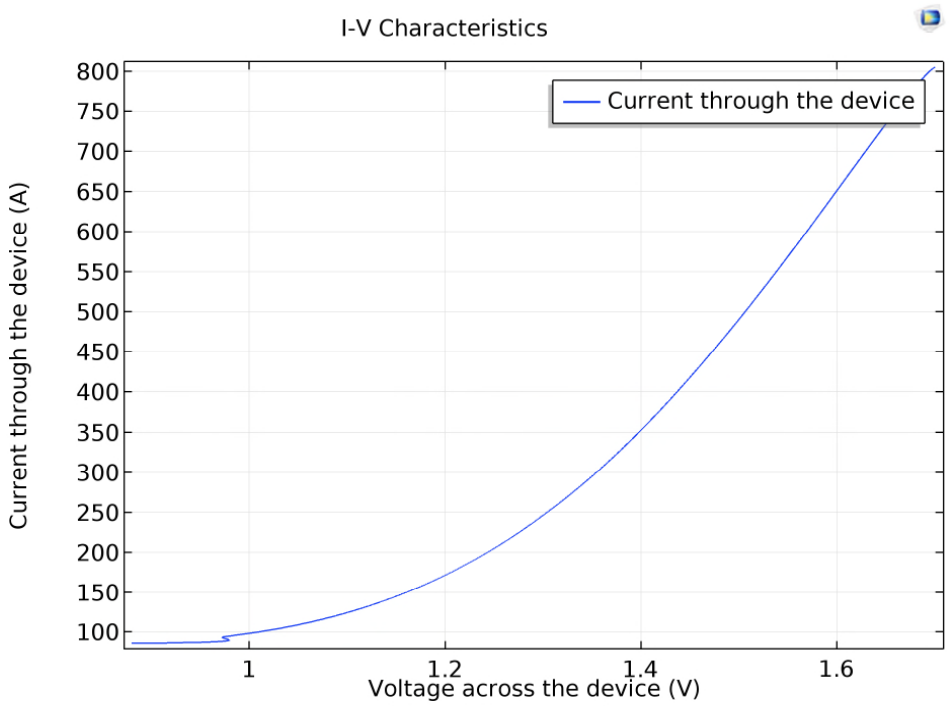
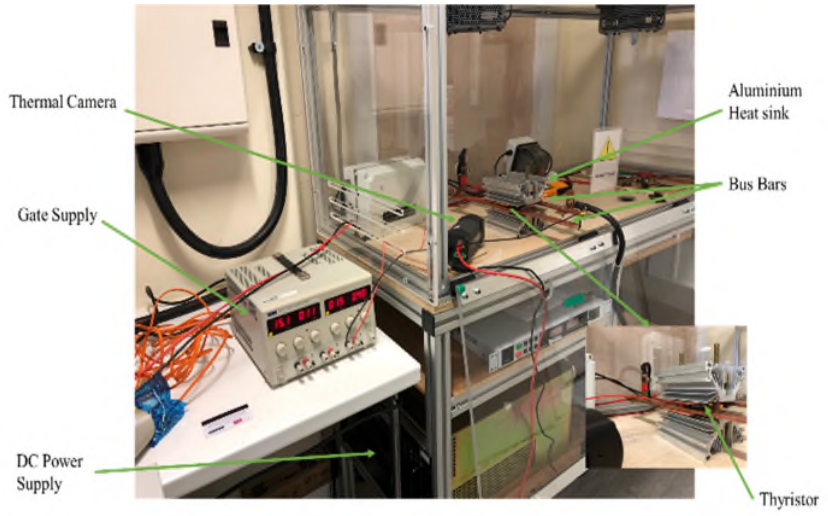


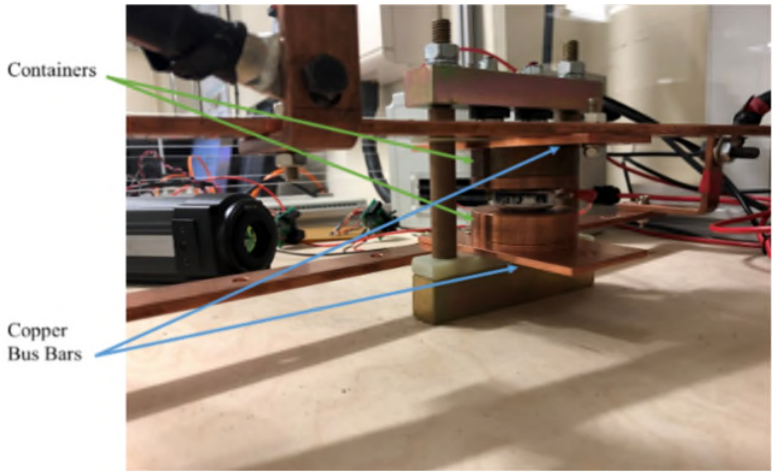
Figure 5.10: I-V characteristics of the thyristor

5.6 EXPERIMENTAL RESULTS

To verify the simulation results and evaluate the impact of using the PCM as a cooling method, two short-circuit test conditions have been used: 800A lasting for 1 second and 800A lasting for 2 seconds. However, in this case, due to the difficulty and complexity of measuring the temperature of silicon wafer, the temperature of the case has been measured for studying the efficiency of the PCM on the delay time and maintaining the temperature. The experiments are performed, using the experimental setup described in Fig 5.11. For both short-circuit



(a) A Scheme of the test including the heatsink



(b) PCM heatsink

Figure 5.11 (a) and (b): A schematic of the experiment by using the heat sink

conditions, the thyristor was tested: (a) without heatsink (only for 1 second, not 2 seconds), (b) with a conventional large aluminium heatsink, (c) small prototype heatsink without the PCM, (d) small prototype heatsink with the PCM. Fig 5.12 shows the temperature difference for the 1-second test. As can be seen from it, using the PCM maintains the “case” temperature around 31°C, which is close to the Gallium metal melting point and hinders the temperature from rising further. Moreover, due to decreasing the thermal impedance, it can be deduced that the delay time will decrease as well.

The results show that using just a copper container without the PCM has a similar value as the Al heatsink due to the higher thermal conductivity of copper. But when the PCM is added, Fig. 5.12, the temperature is significantly decreased. In the second experiment, the same current (800A DC) was applied to the thyristor for 2 seconds whilst all previous measurement parameters were kept the same except the first item

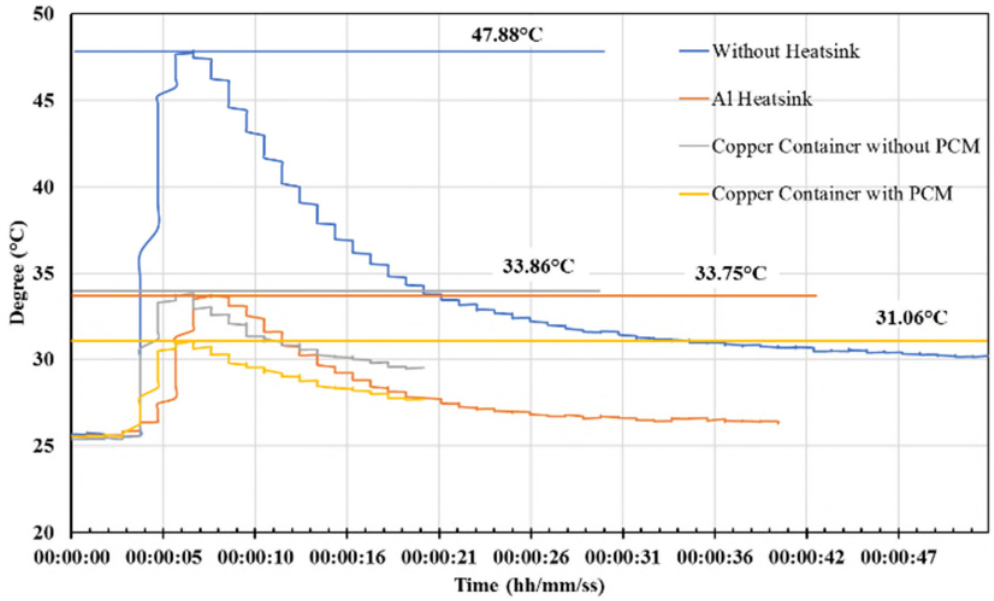
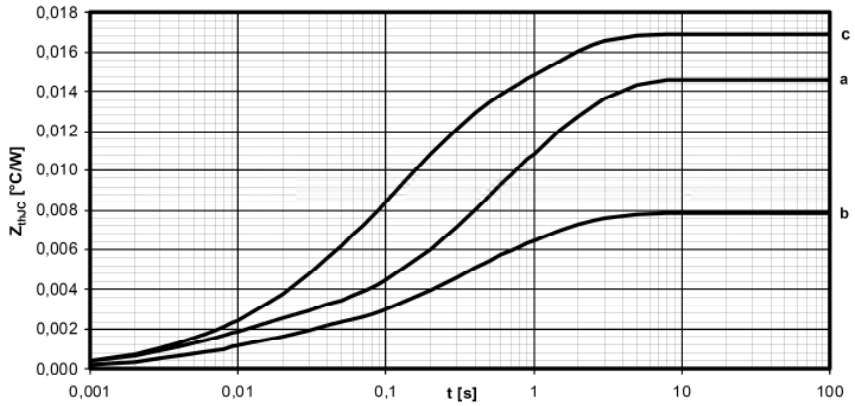
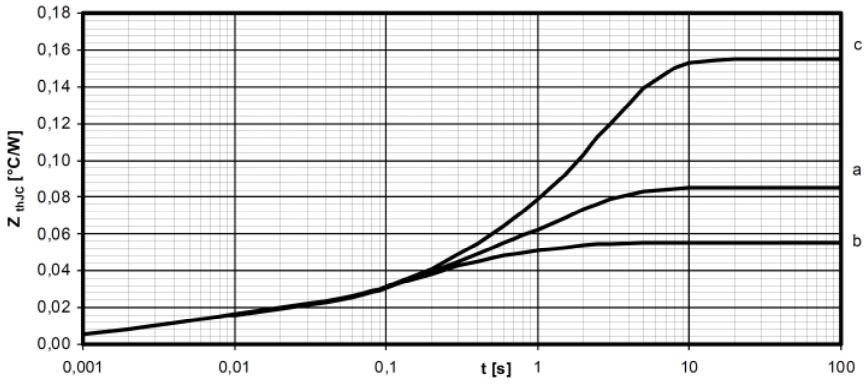


Figure 5.12: The temperature behaviour of thyristor during applying 800A DC current for 1s for (1) without any heatsink (2) the conventional Aluminium heatsink (3) the proposed container without PCM (4) with PCM.

because this test can damage the unprotected thyristor. Fig. 5.14 depicts that the proposed method can absorb more heat compared to the conventional heat sink. It also shows the proposed method can maintain the case temperature at around 33°C, which is very close to the previous test and around the melting point of the PCM as well. It keeps the case temperature on a lower level than the conventional heatsink. It must be considered, even though the Gallium temperature remains roughly 30°C, the used copper container temperature increases gradually. This leads to an increase in case temperature which exceeds the melting temperature of the PCM at one point. Fig. 5.13 [10] shows that the thermal behaviour of thyristors, especially medium voltage thyristors, (Fig. 5.13 (a)) can be transferred to the surface very quickly. This explains why the PCM can



(a)



(b)

Figure 5.13 (a) and (b): different thermal Impedance datasheets [10]

absorb heat in a few milliseconds after the fault. Fig. 5.13 (b) shows the PCM should possibly be placed inside the press-pack to absorb the heat and decrease the delay.

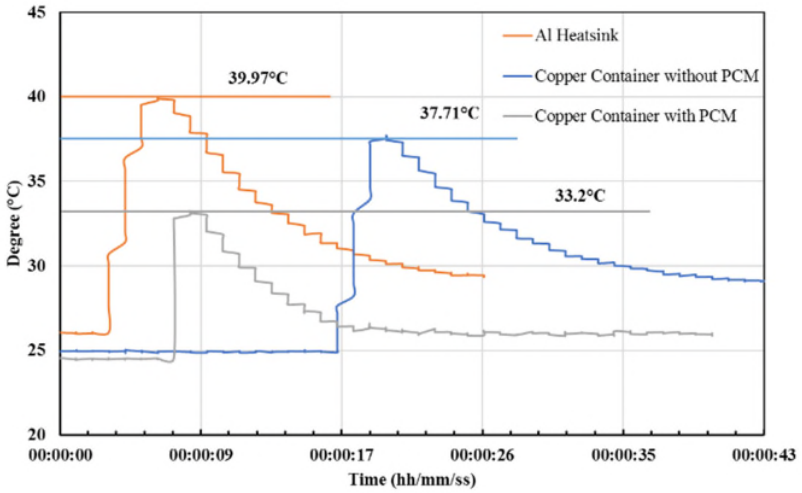


Figure 5.14: The temperature behaviour of thyristor during applying 800A DC current for 2s for (1) the conventional Aluminium heatsink (2) the proposed container without PCM (3) with PCM

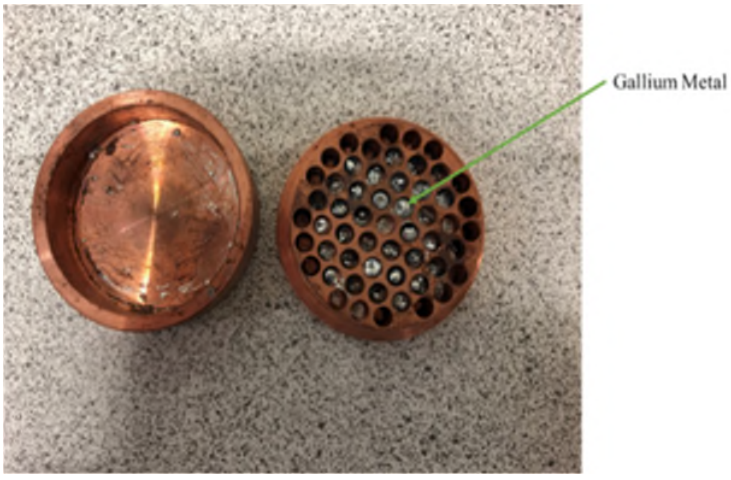


Figure 5.15: copper container with PCM

Fig. 5.16 demonstrates how the “case” temperature is measured by using a thermal camera, while the current is passing through it.

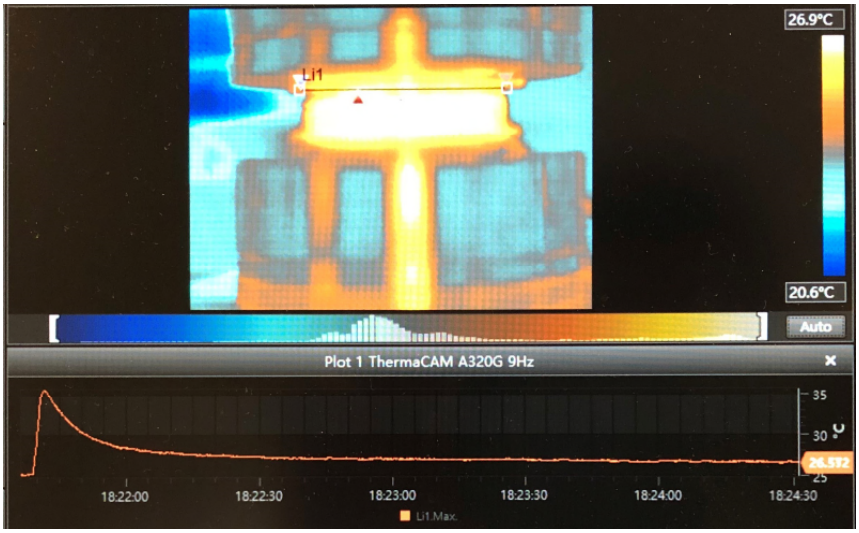


Figure 5.16: measuring the “case” temperature of the press-pack thyristor by using the thermal camera

5.7 SIMULATION RESULTS IN THE MEDIUM VOLTAGE LEVEL

To show the ability of the proposed heat sink, an investigation in medium voltage (11kV) has been conducted. In this case, the condition of thyristor and heat sink in terms of a short-circuit in the network have been analysed as a huge current is driven through it. In MV networks the level of fault current depending on the point of fault, line and fault resistance can reach many tens of kilo amperes. In this case study, the fault current which passes through the thyristor crowbar is roughly 15 kA. It means the performance and ability of the cooling system have a key role during the fault, otherwise, the thyristor crowbar might get thermally destroyed. The ability of the proposed heat sink in the low voltage and current levels has already been discussed and proved through both simulation and experimental results but doing the experiments in the medium voltage level will be very complex and difficult so that this section only presents the simulation results.

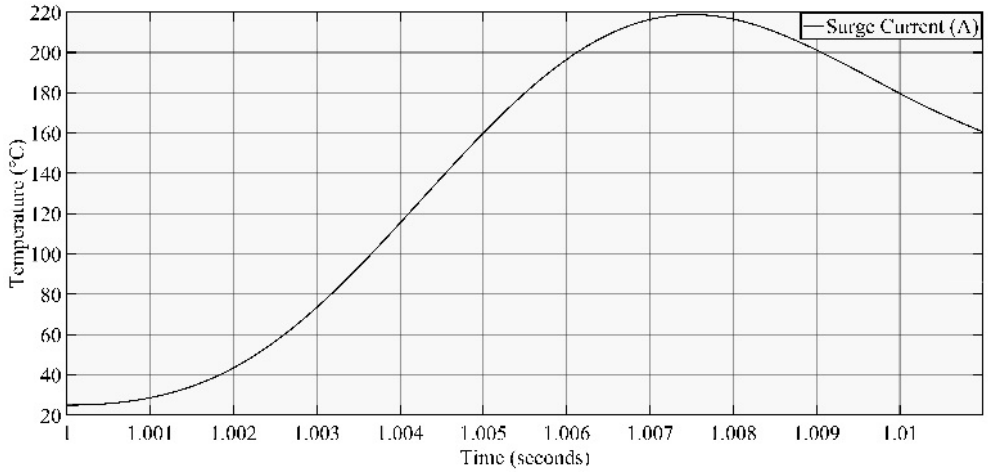


Figure 5.17: Junction temperature for 10ms-15kA pulse, 50Hz half-sine wave in MATLAB

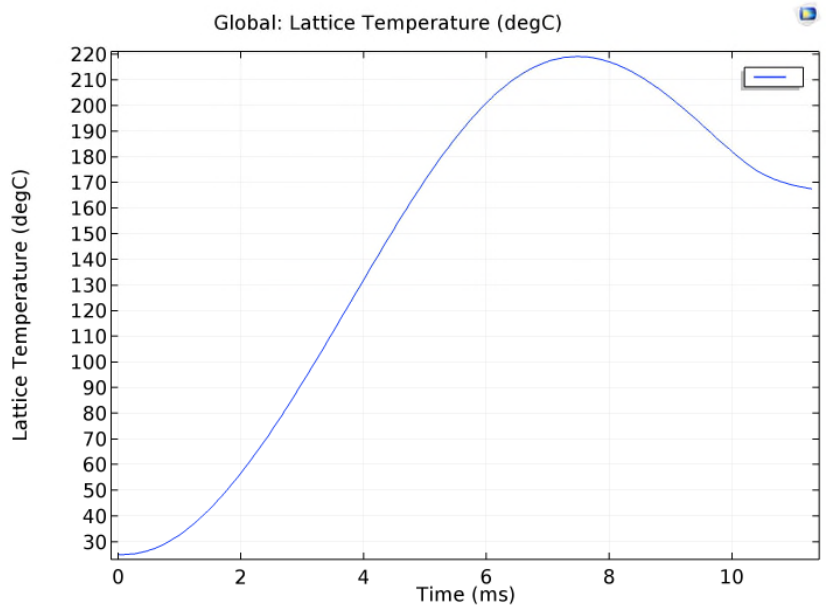


Figure 5.18: Junction temperature for 10ms-15kA pulse, 50Hz half-sine wave in Comsol, without heatsink

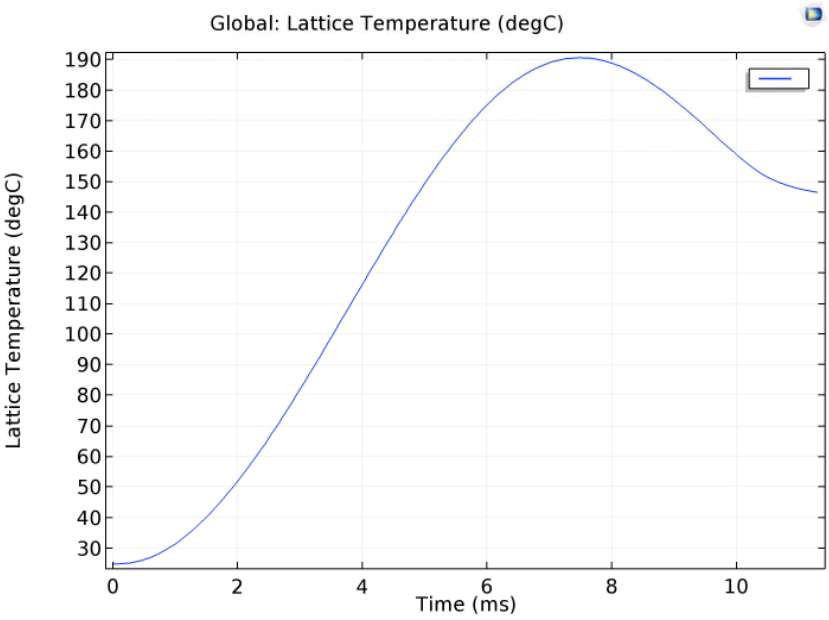


Figure 5.19: Junction temperature for 10ms-15kA pulse, 50Hz half-sine wave in Comsol, with the proposed PCM heatsink

Table 5.4: Features of used Thyristor for medium voltage test [7]

Manufacturer	**Type**	**V_{RRM} (V)**	**I_{TAV} @ T_c (A @ °C)**	**I_{TSM} @ T_j (A @ °C, t_p=10ms)**	**$R_{c\text{-}s}$ (°C/W),DC Double side cooling**
ABB	5STP 10T1600	1600	969 @ 70	15000 @ 25	0.032

Figures 5.17 and 5.18 demonstrate the maximum junction temperature for the thyristor in Table 5.4 in MATLAB and Comsol simulation, respectively. As it clearly depends on the level of voltage, either several thyristors in a series connection or a thyristor with higher V_{RRM} can be used. The temperature of junction temperature goes up by 220°C during a single pulse-half sine surge current which lasts for 10ms. So, figuring out a fast-act heatsink can protect thyristor against the thermal tensions. Fig. 5.19 shows the impact of using a PCM heatsink can theoretically decrease the temperature by 30°C. Table 5.5 presents a summary of the thermal conditions used in this simulation.

Figures 5.20 and 5.21 are about the thermal impedance and I-V characteristics of ABB thyristor which have been utilised for obtaining the thermal impedance of the thyristor with and without the PCM heatsink. As can be seen from Fig. 5.20, the thermal impedance is variable during the surge test to simplify the calculations, an average value which can satisfy the following equation by considering the obtained maximum temperature has been considered:

$$\Delta T = P.R_{thermal\ Impedance}$$

where P can be obtained by using the I-V characteristics when the junction temperature is 25°C.

Table 5.5: Thyristor thermal results-11kV

Time of Pulse (ms)	Thermal Impedance/no heatsink (°C/W)	Temperature before heatsinking (°C)	Thermal Impedance/PCM heatsink (°C/W)	Temperature by heatsink (°C)	Required PCM for absorbing heat (grams)	Maximum Absorbed Heat by PCM (J)
10	0.0025	220	0.0021	190	50-each side	150

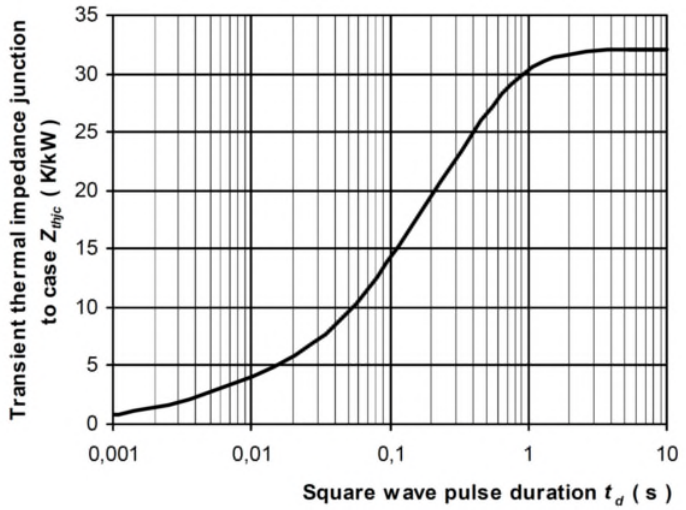


Figure 5.20: Thermal impedance of ABB thyristor for a DC pulse [11]

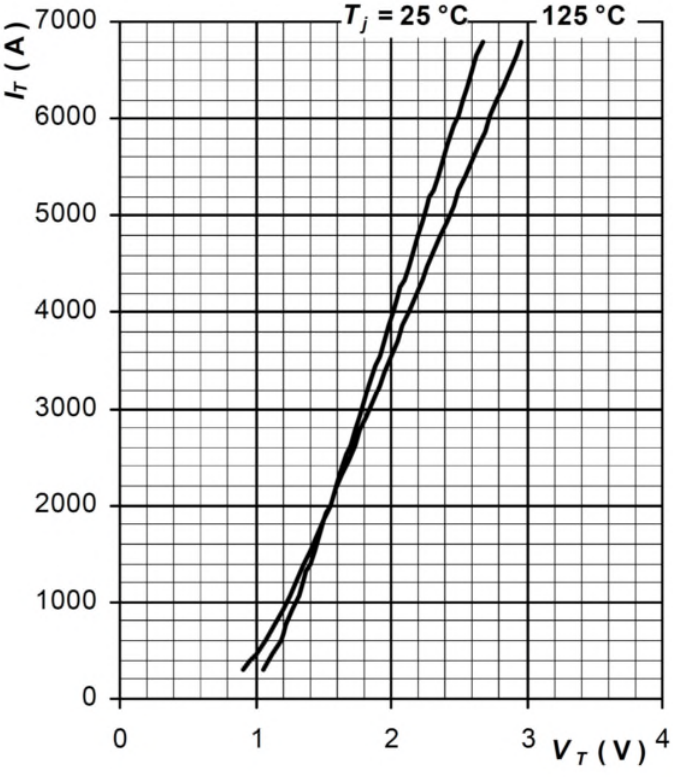


Figure 5.21: I-V characteristics of ABB thyristor [11]

The I-V characteristics of the modelled thyristor of ABB, Table 5.4, has been presented in Fig. 5.22.

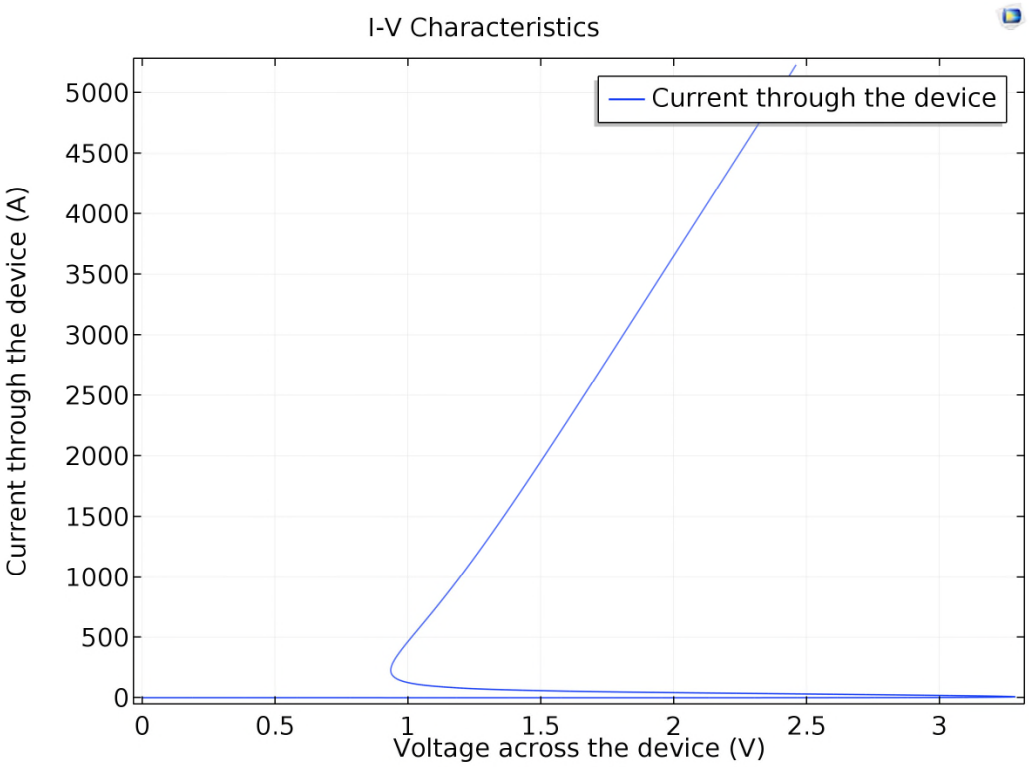


Figure 5.22: I-V characteristics of the thyristor

5.8 CONCLUSION

This study shows that using a cost-effective and practical technique can help to maintain the thyristor temperature within a safety margin during the operation which is necessary for securing the protection process of the SSSC. During a fault, a great current passes through the thyristor that increase its temperature rapidly. In this case, the cooling devices such as heatsinks can limit this temperature rise. PCM materials due their capability to absorb the heat can protect thyristors against a thermal damage or thermal decomposition. The PCM heatsink depends on the used material can be less expensive than conventional heatsinks. They can absorb higher heat as well.

Simulation results using models that are experimentally verified demonstrate that the PCM material can precisely control the thyristor chip temperature due to its ability to absorb the heat as latent heat, as well as its fast response. In fact, the proposed heatsink can maintain the case temperature around the PCM melting point. This not only reduces the temperature but also has a deterministic effect on the cooling of the thyristor and hence presents effective thermal management. Moreover, the size of the proposed PCM heatsink is significantly smaller than the conventional ones. In the future, the aim is to evaluate shorter operation durations (about 100ms) with higher thyristor current examine the heat transferring delay between the silicon wafer and the PCM heatsink.

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6 CONCLUSION

This chapter summaries the main objectives and achievements of the performed research in this thesis as well as provides a guidance for the future research on the topics of protection, reliability and cost in the medium voltage networks and the thermal packaging of the power semiconductor devices.

6.1 CONTRIBUTIONS

- To enable SSSCs' application in MV networks with distributed renewable generation, a new short circuit protection and SSSC isolation technique was developed extending the existing relay protection with a varistor voltage limiter and thyristor switches.

- Benefits of power transfer via SSSC between feeders in the MV network with multiple feeders compared to the feeders' direct connection were justified via a case study simulation with power flow analysis.

- An electric schematic of the SSSC protection and isolation was suggested and verified via timing the short-circuit events and components' response times, and via equivalent single phase experimental testing.

- Thermal modelling and simulation of SSSC transistors with the existing relay protection and with the proposed protection for the same short-circuit case study evidenced 50 °C transistor junction peak temperature reduction while the SSSC short-circuit peak current value reduced about by 50%.

- The influence of the DC offset in the MV networks due to short circuiting synchronous and induction generators on the feasibility of the developed protection technique was assessed via analysis of the corresponding equivalent circuits and introduction of a critical value of the AC and DC short circuit current components ratio determining zero current crossing within the first half period.

- The impact of the DC offset on the developed protection technique was found depending on the generators number and electricity line length and it was shown that the zero crossing happened within the first half period for realistic line values.

- To absorb the heat of the thyristors during the short circuit protection, a new construction of the heatsink was designed exploiting a phase change material leading to the size reduction and heat absorption speed increase compared to the equivalent Aluminium heatsink.

- A thermal modelling and 1 second and 2 seconds simulations of a thyristor under a high current were performed for the case of no heatsink and for the case of the heatsink containing Gallium, using MATLAB and COMSOL, and there was about 20 °C lattice temperature reduction.

- The 1 second and 2 seconds experiments with 800 A current were conducted for a thyristor with a big Aluminium heatsink, with a reduced size Copper heatsink and the Copper heatsink containing Gallium. The designed novel heatsink demonstrated the lowest case temperature increase. In case of 1 second it was about 3 °C lower than for other cases, and in case of 2 seconds it was 5-6 °C lower. The benefits of the new cooling approach were demonstrated in MATLAB and COMSOL simulations for a medium voltage cases.

6.2 FUTURE WORK

The thesis has already discussed a novel protection scheme for a SSSC in an MV network. But, a UPFC has not been studied in this research. The effect of the proposed technique in protecting the UPFC, that has also a series compartment with the network, can be investigated. Moreover, there are some researches that studied a FCL-SSSC, the combinations of this type of an SSSC with the proposed can be studied as well. In fact before isolating the SSSC from the network during a fault, the current can be limited first and if the fault cannot be removed quickly enough from the network, in the next step the SSSC can be isolated.

This thesis has discussed a PCM heatsink that can be used only during a short circuit that is a very specific case. Therefore, it needs to be investigated that how this kind of heatsink can be used for a continuous operation. Since the PCM materials has usually a low thermal conductivity the heatsink structure is used with them has to be investigated in terms of its element like copper, aluminium and its structure so that it can deliver the heat evenly and quickly to the PCM material. Also, locating the heatsink is an important factor. In fact, placing them closer to the semiconductor wafer can decrease the delay time that the heat transfers from the wafer to the PCM heatsink.

At the end, the proposed PCM heatsink can be used for the utilized thyristors in the proposed technique and then its performance can be analysed. As it is said before, the temperature of thyristors while they are used in their surge condition can rise very quickly. This temperature rise can damage them severely. Thus, controlling or limiting this temperature rise is extremely important for thyristor to protect them from thermal damages during a surge condition.

Appendix I

THYRISTOR

Thyristors are one of the oldest solid-state semiconductors that have the highest power-transferring capability (see, Figures 1 and 2). They have a four-layer construction and are a latching switch that can be turned on by the gate terminal. Although, their deficiency in becoming turned off by that gate prevents its usage in the switch-mode applications. There is another type of thyristor that includes a gate turn-off capability which is called GTO, gate turn off thyristors.

In terms of grid, thyristors are of the most important and practical power electronic systems and their various applications in numerous power electronic devices such as converters, or solid-state circuit breaker (SSCB) makes it a key element in power grids. Therefore, in medium-voltage and high-voltage networks due to the voltage level and fault current amount such as the short circuit current, the high temperature thyristor usually is being used because of its withstand capacity. However, power losses and on-state losses shall be considered.

In terms of the lateral dimension, thyristors are among the largest semiconductor devices. In order to make a high-power thyristor, a 10 cm-diameter silicon wafer may be used. The thyristor’s diameter has a great impact on the layout of the gate and cathode as well as the di/dt capability and the range of the switching speeds.

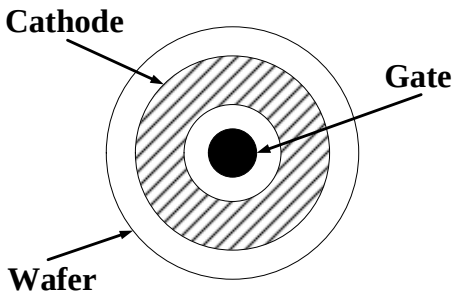

Figure 1: Vertical cross section of a thyristor

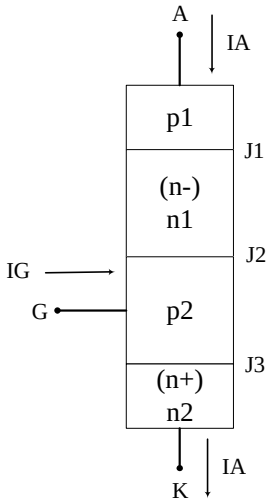

Figure 2: one-dimensional model of a thyristor

I-V CHARACTERISTICS

The I-V characteristics of a thyristor is shown in Fig. 3. For a thyristor the maximum reverse working voltage V_{RWM} can be as high as 7000 V or even much higher. The forward-blocking voltage V_{BO} is quite similar to the reverse voltage. In the on-state mode of the forward direction, a high-power thyristor is able to conduct a current as large as 3000 A or much more with only few volts voltage drops [1].

I_H is the minimum current that can flow through the thyristor and still keep the device in the on-state and V_H is the lowest possible extension of the on-state portion of the I-V characteristic.

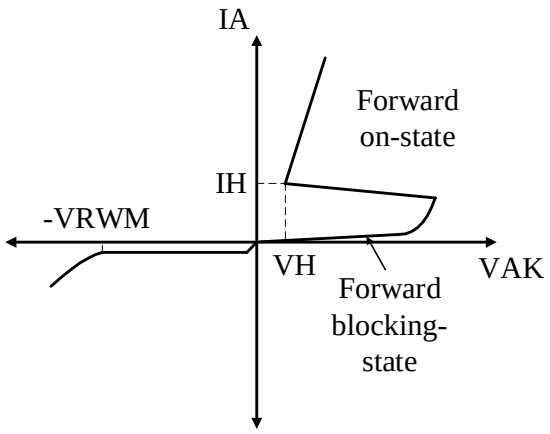

Figure 3: Current-voltage characteristics of a thyristor

VARISTOR

Using Varistor, see Fig. 4, might be another method for protecting the static series compensator devices. Locating it in a parallel position with the static series compensator can avoid flowing current through the static series compensator during a fault by driving the fault current through itself. Totally, due to the very short operation time of varistors which lasts from a few nanoseconds to microseconds, which causes a huge energy delivers through them, they can only be a suitable option for protecting the facilities against a lightening, a overvoltage and even a fault current.

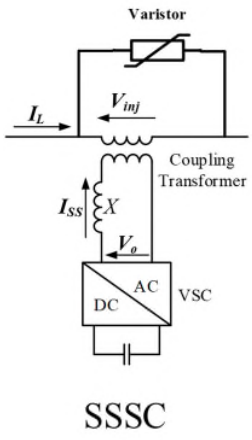

Figure 4: A schematic of a Varistor-based protection device

As a result, the energy absorption capability of varistors has to be big enough to withstand this level of fault energy which is flowing through that [2]-[4]. However, one way to control this high energy is using another circuit in paraller with varistor to divide the current and then the energy is flowing through them as proposed in [2]. Varistors are usually used to protect devices such as transformers against a lightening, due to their fast reaction and high capability against high voltages and currents which enables them to be used in MV systems. Conclusively, using varistor is economic and has less complexity rathar than other techniques, but their absorption energy capability and very quick respond have to be investigated.

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