Comparison of Conventional and Maskless Lithographic Techniques for More than Moore Post-processing of Foundry CMOS Chips

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***Abstract*—This paper details and compares the technology options for post–processing foundry produced CMOS at chip-scale to enable More than Moore functionality. In many cases there are attractions in using chip-based processing through the Multi-Project Wafer route that is frequently employed in research, early-stage development and low-volume production. This paper identifies that spray-based photoresist deposition combined with optical maskless lithography demonstrates sufficient performance combined with low cost and operational convenience to offer an attractive alternative to conventional optical lithography, where spin-coated photoresist is exposed through a patterned photomask.**

***Index Terms*—CMOS, maskless, More than Moore, on-chip, optical lithography, photomask, post-processing, spin-coating, spray-coating.**

I. Introduction

MORE than Moore technology (MtMT) is defined by the addition of extra functionality to standard integrated circuit (IC) processes through the introduction of additional materials, processes and technologies [1]–[5] and has been identified in the International Technology Roadmap for Semiconductors (ITRS) as an increasingly important route to adding value to devices alongside the more traditional scaling option [6]. The definition of MtMT has also been used to encompass 3D stacking/integration [7]–[8], as well as hybridisation of additional devices and related technologies [9]–[10]. A major attraction of MtMT is that it provides researchers with opportunities to innovate without the high investment levels required to continually reduce the smallest achieved critical dimension (CD).

This means that research institutions, start-ups and small scale enterprises have an accessible, cost-effective exploitation route to MtMT through the use of custom IC wafers sourced from silicon foundries, in combination with low cost post-processing techniques that can be performed in smaller R&D facilities. As more MtMT reach maturity, they are being introduced into the leading foundries and offered to customers. Successful examples include Complementary Metal Oxide Semiconductor (CMOS) imagers [11], and polymer based organic light emitting diode (P-OLED) over CMOS microdisplays, which initially involved the hybridisation of CMOS foundry wafers with glass substrates that were patterned with colour filters [12]–[13]. As this latter technology matured, it led to the production of the first commercially available picture-quality colour active-matrix (AM) P-OLED display [14]. Similarly, Liquid Crystal on Silicon (LCoS) microdisplay technology was developed using foundry CMOS post-processed with extra metal layers, planarisation and spacers for liquid crystal integration and packaging [15]–[18]. This process has also become a foundry offering [19].

It should be noted that smaller R&D facilities are typically limited to processing wafers of 200 mm diameter or less. This makes wafer-scale MtMT post-processing of advanced technologies, which use 300 mm wafers, very difficult. However, silicon foundries also offer an attractive and low cost alternative route through the multi-project wafer (MPW) service, where instead of wafers, customers receive chips with their IC design. While this service is typically used during development of an IC design, it also provides the opportunity for low-cost development of MtMT post-processing at chip-level.

In this paper, the focus is on the monolithic post-processing of IC technologies. In particular, it presents and compares the merits of the lithography options available to facilitate the

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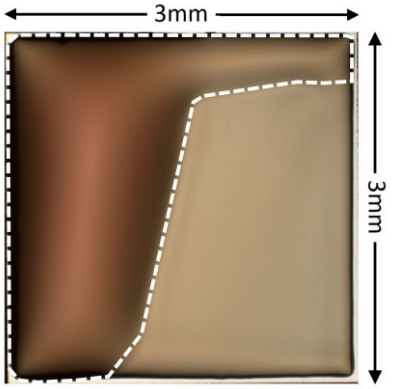

Fig. 1. Optical image of a 3×3 mm silicon chip with spin-coated photoresist showing significant edge bead (dashed line area).

post-processing of individual chips that might typically be received from a MPW service. These processes are required to fabricate the additional patterned layers designed to add extra functionality to the underlying integrated circuitry, e.g. the addition of sensor technologies [20]–[24] or microelectromechanical systems (MEMS) [25]–[28].

II. Post-processing technology options

A. Introduction

As part of the development process the post-processing design of MtMT can be developed in parallel on dummy wafers in readiness for the full integration of the post-processing. Clearly, the most straightforward approach to complete the development is to perform this using fully functional foundry wafers, as fabrication lines are set up and optimised for full wafer processing. However, the cost differential of procuring a full wafer of devices or 20-50 chips from a foundry is of the order of 10-20:1 [29]. Hence, for research and early-stage development purposes, procuring individual chips to first verify the circuit design is functioning correctly is for many a generally accepted approach. In our experience, MPW dicing and subsequent chip packaging has not adversely affected circuit functionality.

Once the chip functionality has been confirmed the remaining chips can then be made available for developing the post-processing integration technology. However, it should be noted that process equipment have been designed primarily to process wafers, which for many process steps, makes chip post-processing problematic.

A major challenge associated with chip-based processing is related to lithography technology. Photoresist deposition processes have historically used spin-coating, which results in an "edge bead" of thicker photoresist around the wafer perimeter. This can be easily removed on wafers, but with millimetre scale chips this is problematic as the edge bead can comprise a large proportion of the coated surface as shown in Fig. 1. In addition, photolithographic exposure systems are primarily designed for wafer-based processing and many do not lend themselves to chip-based exposure. These two factors represent significant challenges to successful chip processing. The following sections introduce the significant benefits of using a combination of optical maskless lithography with spray-coated photoresist to achieve patterning of post-process layers at a chip level.

B. Photoresist deposition – spin and spray-coating

For photoresist deposition spin-coating of wafers is very much the industry standard and robotic processing systems ensure a uniform and highly repeatable photoresist coating. As mentioned above the edge bead with chips is an issue and makes high resolution lithography challenging.

Spray-coating is a less commonly used method used for coating photoresist. It takes longer to deposit photoresist than spin-coating, but for chip-based processing the absence of any significant edge bead is a major advantage. Other elements that may also be of benefit are that spray-coating uses less photoresist and delivers better step coverage [30]–[32]. However, the major advantage associated with chip processing is the effective reduction of the photoresist edge bead.

C. Lithography options – e-beam and optical

E-beam lithography has long been the main choice for single chip post-processing. With the thin layers of photoresist (typically < 1 µm) required for e-beam, and no requirement for close proximity of a mask, the edge bead issue is minimised. An added attraction of e-beam is that, with no mask involved, it is straightforward to modify a design should layout patterns need to be revised. However, e-beam exposure tools are expensive and their exposure speed is relatively slow, particularly if high resolution, full wafer processing is involved. In this paper we have restricted ourselves to comparing the performance of more readily available, cheaper conventional and maskless photolithography options. This is motivated by the more wide-spread availability of maskless photolithography tools with similar attributes to e-beam (but admittedly lower resolution). These tools can be ideal for the majority of MtMT post-processing, which do not require deep sub-micrometre dimensions. In addition, they offer solutions to non-conventional exposure modes, such as grayscale.

III. Comparison of post-processing techniques

Lithographic techniques are required to support most on-chip post-processes, such as thin film deposition, device layer and deep silicon etching. Photoresist thickness requirements vary widely, and while a number of on-chip processes use thin photoresist layers (< 3 µm), where the edge bead problem is not so profound, this is not always the case. In this paper we will restrict the comparison to thicker (> 7 µm) photoresist layers, as they present a greater lithographic challenge.

One common on-chip post-processing requirement with MtMT sensors is the full removal [33] or partial thinning of the foundry passivation layer [34]–[35]. Full removal might be needed in order to electrically contact the CMOS, or deposit a new sensing material that is not available in a standard foundry process. The latter thinning process is also a non-standard foundry step, with the aim being to reduce signal attenuation or increase the sensitivity of the system. Typically, the top insulator is a combination of silicon oxide (SiO_2) and

silicon nitride (Si_3N_4) with a total thickness of ~2 µm. Additionally, some of the processes might include a thick polyimide layer on top of the passivation. The removal of several micrometres of passivation using reactive-ion etching (RIE) requires long process times, thus coating and patterning a thick resist layer is necessary.

The following sections compare coating and photolithographic techniques that could be used prior to selectively etching features on the passivation of a foundry chip in order to expose the underlying metal layer. The test chips used in this evaluation were 3×3 mm and were selected to resemble a typical small-sized sensor system [33].

A. Conventional optical lithography with spin-coating

To render on-chip processing compatible with wafer processing tools, the chips are mounted onto a 100 mm carrier wafer using photoresist which is then soft baked at 90°C for 30 min. A wafer, patterned as shown in Fig. 2, enables accurate manual placement of the product chips close to the desired position. This facilitates an easier photolithographic alignment step between chip and mask prior to exposure. While it might be expected that chips positioned in the centre of a carrier wafer would be more uniformly coated, it has been reported that this is not the case, with more uniform coatings resulting when the chips are located further from the centre [36]. Although photomasks typically have multiple identical patterns, this technique only facilitates the exposure of a single chip, as it is practically impossible to manually mount an array of chips with identical offsets in x, y and θ, e.g. [37] used cavities for embedding die in a carrier wafer that required a 10–15 µm clearance on all sides of the die. This is significantly larger than any photolithographic misalignment errors. It should be noted, that the wafer stage alignment movement of contact/proximity photolithographic tools is typically limited to a few mm. Thus, it is not feasible to expose multiple product chips with an alternative photomask design, using a one at a time sequential exposure approach. This is the case even if the chips are all located in close proximity. Furthermore, spin-coating on a topology consisting of multiple closely spaced chips, can potentially result in coated surfaces with significant photoresist streaking present.

In addition, wafer-mounted dummy chips of the same thickness as the product chip, are used to define the initial sample/photomask contact plane, which is then used to define heights during alignment and close proximity or contact exposures. The dummy chips are typically mounted near the edge of the carrier wafer as shown in Fig. 2, with their positioning not being determined by the position of the product chip.

Test chips were treated with hexamethyldisilazane (HMDS) vapour for 10 min to enhance photoresist adhesion and then spin-coated using a POLOS MCD coater with SPR 220-7.0 positive photoresist (the standard benchmark process). The target thickness of ~9 µm replicates the requirement of a post-processing step for CMOS ion sensitive field effect transistor (ISFET) pH sensors. In this case the foundry passivation is selectively removed with RIE, to expose the top metal layer of an ISFET's extended gate [33]. Wafer-level coating tests at low speed (1400 rpm) achieved the target film thickness. However, on-chip tests at the same speed, produced devices with significant edge bead similar to Fig. 1. It was determined that the optimum spinning method was a two-stage spin at 5000 rpm. Therefore, the chips were coated twice at this speed followed by a soft bake (SB) at 110°C (ramped from room temperature in ~5 min) for 90 seconds, after each coat.

A photomask consisting of a grid of 100×100 µm square holes was chosen to quantify the pattern transfer onto the chip. A coated chip was exposed for 60 seconds using a Karl Suss MA8 mask aligner at 5 µm proximity exposure mode, followed by a post-exposure bake (PEB) at 110°C for 90 seconds, 2 hours after the exposure. The chip was developed for 90 seconds using MF-26A developer and the on-chip patterned features are shown in Fig. 3. It is clear that even

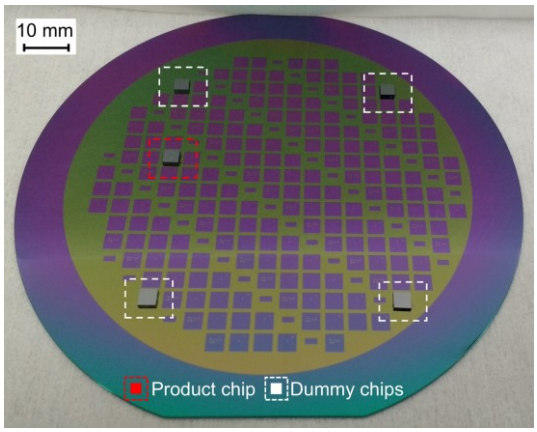

Fig. 2. Photograph of a carrier wafer used for contact exposure of a single product chip. Dummy chips of the same silicon thickness are used to assist with the initial contact between sample and photomask. This is used to define z-axis parameters, during alignment and exposure.

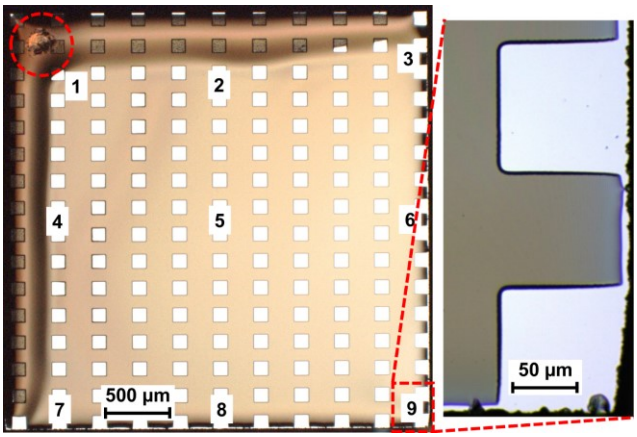

Fig. 3. Optical image of spin-coated chip after photoresist development. Numbers indicate approximate locations where the thickness of the photoresist has been measured using reflectometry. Dashed circle shows a defect caused during photomask contact, while blown up section to the right shows that the photoresist has retracted from the edge.

TABLE I
ON-CHIP SPIN-COATED PHOTORESIST THICKNESS AFTER DEVELOPMENT

	Thickness (µm)				
(1)	10.50	(2)	9.07	(3)	9.12
(4)	9.62	(5)	8.55	(6)	6.07
(7)	9.95	(8)	9.09	(9)	5.08

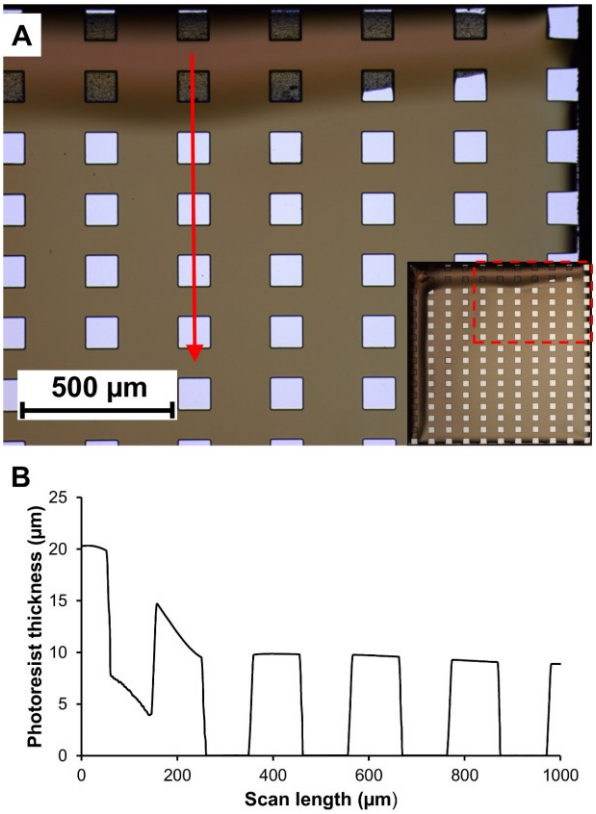

Fig. 4. (A) Optical image of a section of the spin-coated chip, with the arrow indicating the direction of a profilometry scan. (B) Surface profile trace of the above scan, showing the photoresist thickness variation.

with the optimised process the edge bead is significant, though less than that seen in Fig. 1. An option for further reducing edge bead, is to use low viscosity, thin photoresist (~1 µm) and multi-stage spin-coating. For the target thickness of ~9 µm, this would require a ~9-stage spin coating, resulting in significantly increased processing times.

Photoresist thickness measurements were made at nine locations (Fig. 3) using a Nanometrics Nanospec 3000 reflectometer and these results are presented in Table I (average thickness is 8.56 µm, range is 5.42 µm). While the photoresist at the centre of the chip has approximately the target thickness, the top and left edges are significantly thicker and thus it is not possible to extract an accurate measurement by reflectometry. On the contrary, bottom and right-hand edges show significantly reduced resist thickness. In addition, the photoresist has retracted completely within 10-20 µm of those edges, exposing the underlying layer (Fig. 3). To measure the resist thickness at the edge bead, a surface profile measurement was taken using a Bruker Dektak XT. As indicated by the arrow in Fig. 4(A) the scan starts ~150 µm away from the edge of the chip, where the photoresist thickness is ~20 µm, as indicated by the surface profile trace in Fig. 4(B). This is twice the nominal thickness, as shown towards the end of scan at the chip centre. Such significant variation in thickness across the chips is likely to cause photoresist damage when the photomask is in contact with the sample. Such a defect can be seen at the top left corner of the chip in Fig. 3.

The patterned features were inspected optically at higher magnification, with a Leica DM12000 M3. Out of the 176 squares on the chip only 67.6% have been developed correctly. 32.4% were either not fully developed or deformed. In addition, these test patterns only cover 17.7% of the chip's surface area, and therefore those ratios could be worse for denser post-processing designs.

An alternative option to using thick photoresist layers, is to break a process step into multiple photolithographic runs with thinner photoresist layers, with partial processing of the chips after each run. However, in addition to significantly extending the time of this single processing step, this approach is prone to misalignment errors and therefore not feasible when tighter alignment tolerances are required. The results presented so far have demonstrated that conventional lithographic techniques are struggling to meet some of the requirements when processing CMOS chips where almost 100% of the die area requires patterning.

B. Maskless optical lithography with spray-coating

One of the benefits of maskless lithography is the ability to mount multiple product chips on a single carrier wafer and expose them sequentially, as an approach to increase throughput performance on die post-processing. Fig. 5 shows an example where two product chips have been patterned at the same time, although this number could be increased significantly with automated pattern recognition software. Additionally, it should be noted that direct-write exposure is free of photoresist defects caused by contact exposure.

To assess the combination of photoresist spray-coating and maskless lithography two chips were first coated using an EVG101 spray-coater with SPR 220-7.0 photoresist. The resist was diluted with methyl ethyl ketone (MEK) and propylene glycol monomethyl ether acetate (PGMEA), to produce a photoresist solution with 6.5% solid content. Unlike the two-stage method described for spin-coating, the chips are spray-coated using a one-stage process, with a recipe developed for coating ~9 µm thick photoresist. The chips were then exposed using a dose of 400 mJ cm^{-2} on a DMO ML3 maskless lithography system. Surface treatment, SB, PEB and development parameters were kept the same as those described in Section III A.

Fig. 6 shows an optical image of one of the chips, patterned with the same grid of square holes, with approximate locations of reflectometry measurements that are presented in Table II (average thickness is 8.99 µm, range is 0.82 µm). The results show that the thickness variation is less than the spin-coated chips, although as observed in Fig. 6 there is an edge bead in the form of a ring. The mechanism and acting forces leading to the formation of an edge bead with spin-coating are detailed in [38]. For spray-coating the forces associated with fast spinning are not present leaving only the surface tension forces at the edges of the chip. In order to quantify this, a surface profile measurement was made and is presented in Fig. 7. It can be seen that the edge bead is ~1 µm thicker than the average thickness and significantly less than the > 10 µm for the spin-coated chip.

Further optical inspection showed that out of the 176

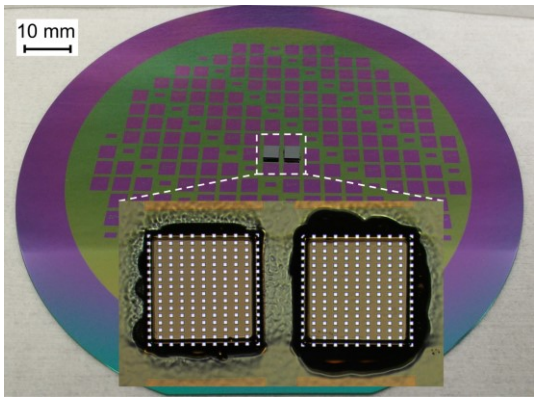

Fig. 5. Photograph of carrier wafer used for maskless exposure with two product chips. Expanded section shows the chips after patterning.

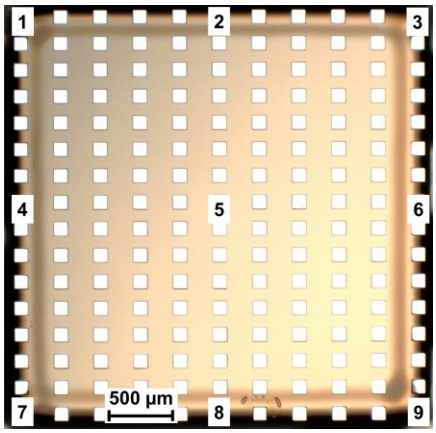

Fig. 6. Optical image of spray-coated chip after photoresist development. Numbers indicate approximate locations where the thickness of the photoresist has been measured using reflectometry.

TABLE II
ON-CHIP SPRAY-COATED PHOTORESIST THICKNESS AFTER DEVELOPMENT

	Thickness (µm)				
(1)	8.77	(2)	8.47	(3)	8.81
(4)	9.15	(5)	8.97	(6)	9.29
(7)	9.03	(8)	9.17	(9)	9.27

structures on the chip 95.5% have been developed correctly. Only 4.5% are not fully developed and, in contrast to spin-coating, there has been partial exposure at the corners of these features. For large critical dimensions, minor over-exposure would result in 100% of the patterns being developed, with small offsets from the design dimensions. This is not the case for the spin-coated chips where the ~20 µm thick edge bead would require significant over-exposure and long development times, which would result in loss of patterns at the centre of the chip where the photoresist thickness is close to the nominal.

While wafer-level spin-coating is a highly repeatable process which ensures uniform photoresist layers, spray-coating requires that a number of parameters are optimised before achieving the same levels of uniformity. For the model used in this work, these include the speed of movement of the nozzle arm and the spraying distance from the wafer. A typical profile will use slower speeds and smaller distances at the edge of a wafer, while higher speed movement and greater distances are used at the centre of a wafer. Other parameters

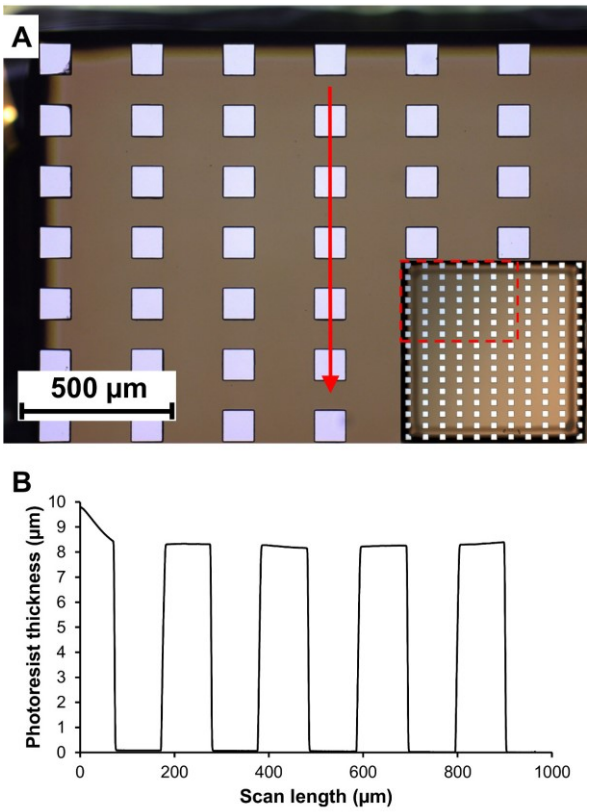

Fig. 7. (A) Optical image of a section of the spray-coated chip, with the arrow indicating the direction of a profilometry scan. (B) Surface profile trace of the above scan, showing the photoresist thickness variation.

include wafer chuck spin speed and temperature, photoresist solution viscosity and flow rate, as well as nozzle sonication power.

The results so far have shown that maskless lithography with spray-coating results in an improvement of the on-chip post-processing with the option to increase throughput by mounting multiple chips. To achieve this the sprayed photoresist must be suitably uniform, so that all product chips mounted on a single carrier wafer, have similar resist thickness. To investigate this, nine chips were mounted on a carrier wafer (Fig. 8), which was then coated using a spraying recipe with a target thickness of ~9 µm. All chips were then measured at nine locations, using reflectometry and the results are presented in Table III. The average photoresist thickness across all chips was 8.72 µm, the range of the averaged chip thicknesses (column 2, Table III) was 0.64 µm, while the highest local thickness range (across a chip) was 0.49 µm. As expected, the variation across the wafer is greater than local on-chip thickness variation. However, it is less than the ~1 µm increase in thickness of the on-chip spray-coated edge bead, which did not cause any problems during exposure and development as identified in Fig 6. The results suggest that it is viable to mount multiple chips onto a wafer with no location restrictions, with perhaps the only exception being near the very edge of a wafer where additional on-wafer measurements have shown greater local variations (highest local thickness range = 1.2 µm), as well as increased offsets (+1 µm) from the averaged measurements.

The test patterns used during this comparison were large,

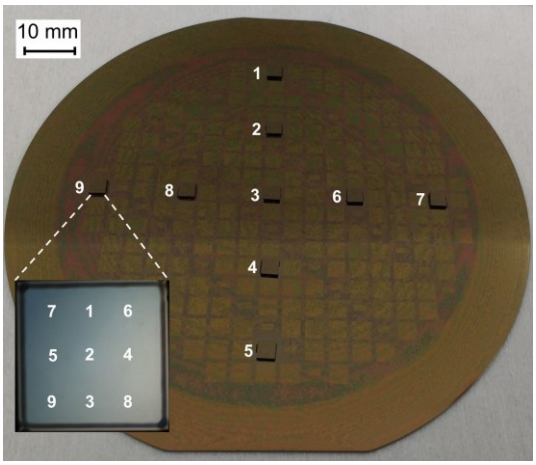

Fig. 8. Photograph of carrier wafer comprising multiple chips to investigate the on-chip spray-coated photoresist thickness across a wafer. The blown-up optical image of one the chips shows the approximate measured positions for each chip.

TABLE III
ON-CHIP SPRAY-COATED PHOTORESIST THICKNESS ACROSS CARRIER WAFER

Chip number	Average thickness (µm)	σ (µm)	Maximum thickness (µm)	Minimum thickness (µm)	Range (µm)
1	8.794	0.172	8.983	8.512	0.471
2	8.797	0.106	8.920	8.569	0.351
3	9.001	0.118	9.204	8.745	0.459
4	8.484	0.165	8.688	8.197	0.491
5	8.473	0.116	8.610	8.258	0.352
6	8.522	0.067	8.609	8.410	0.199
7	8.703	0.107	8.847	8.563	0.284
8	8.601	0.129	8.837	8.418	0.419
9	9.110	0.155	9.307	8.876	0.431

100×100 µm squares, with those dimensions being representative of active areas for electrochemical sensors [39]. However, it might be the case that a number of MtMT applications require patterning of smaller dimensions on thick photoresists. To investigate this a subset of standard optical metrology features with varying CD [40] has been used to pattern features using spray-coating and direct-write exposure. The design also includes nominally 5 µm wide, 1:1 line and space dense features, which are 20× smaller than the square holes.

The photoresist target thickness was kept as before at ~9 µm. Coating, exposure and process parameters remained unaltered, with the exception of a longer photoresist development time (5 min). Imaging of the patterned features was performed using a Tescan Vega3 XMU scanning electron microscope (SEM), in secondary electrons (SE) detection mode. Fig. 9 shows a section of a top view capture of what suggests to be fully developed ~5µm wide line and spaces. However, it can be observed that there is a CD offset between the top and the bottom widths of the photoresist line features. Further process development would be required to optimise the sidewall angle profile of the patterned photoresist features to meet specific process requirements. Clearly optimisation would be necessary to print smaller feature sizes with high aspect ratios between photoresist thickness and linewidth. However, this is unlikely to be common with most small features sizes normally exposed with thin resist layers.

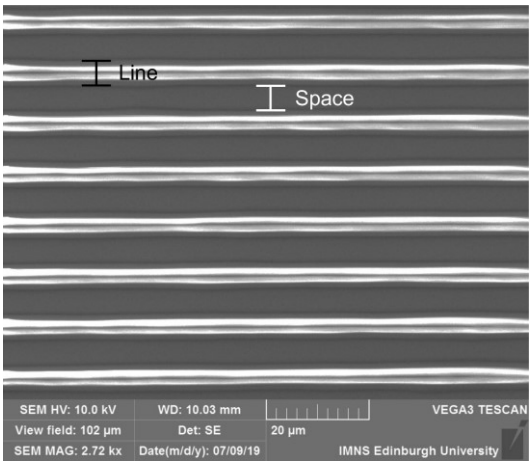

Fig. 9. SEM image of 5µm wide dense 1:1 line and space features patterned on ~9 µm thick spray-coated photoresist.

IV. Effects of Photoresist Etching on CMOS Chips

CMOS foundry chips comprising multiple ISFET layouts with sensing areas up to ~250×250 µm were used to characterise, optically, the way in which patterned photoresist layers are being etched during an RIE process. This is developed to remove the foundry passivation selectively. Coating and lithographic methods (spin/photomask) as described in Section III A were used to pattern the photoresist and expose selected sensors (See Fig. 10 - No etch, "white areas" are exposed - for clarity one of the exposed sensors is highlighted in red). The pattened resist aims to protect the entire chip area and only allow etching of the exposed sensors. A JLS RIE80 was used to etch the photoresist on the chips at 10 minute intervals using an oxygen (O_2) plasma (49 sccm O_2, 100 W, 50 mTorr). Fig. 10 shows that after 10 min of etching the photoresist has been removed at the bottom corner and right edge exposing a number of the bonding pads. The optical fringing effect observed nearby also indicates a significantly reduced layer thickness. After 20 min of etching the photoresist has been removed completely from a large section of the chip, and this became even more apparent after 30 min. This observation matches the earlier findings showing significant non-uniformities on spin-coated samples, ranging from very thick to very thin photoresist layers across a small chip. The result of such extreme variations in photoresist thickness would result in the passivation getting etched in a non-uniform manner, effectively damaging the CMOS chip.

Coating and lithographic methods (spray/maskless) as described in Section III B were also used to pattern the photoresist and expose selected sensors on-chip (see Fig. 11 - No etch). Fig. 11 shows that after 10 min of O_2 plasma, the chip is still protected by the resist, except from the exposed sensors. After 30 min of etching only the very edge of the chip has been exposed. However, this is just a few micrometres of unused silicon area and not part of the product design. It is only after 50 min of etching that the bonding pads have been partially exposed (dashed area Fig. 11), although at this stage the resist has been thinned down significantly and any further etching would expose the chip entirely.

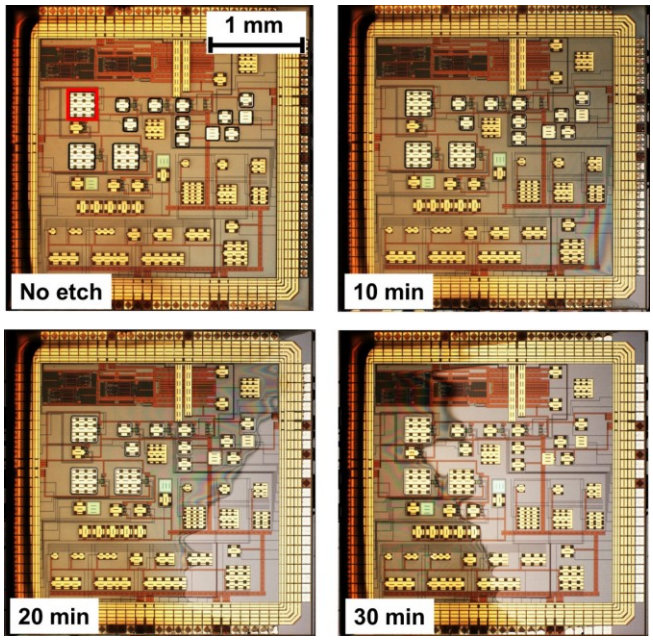

Fig. 10. Optical images of a CMOS ISFET chip, with patterned spin-coated photoresist prior etching and 10, 20 and 30 min after O_2 plasma etching.

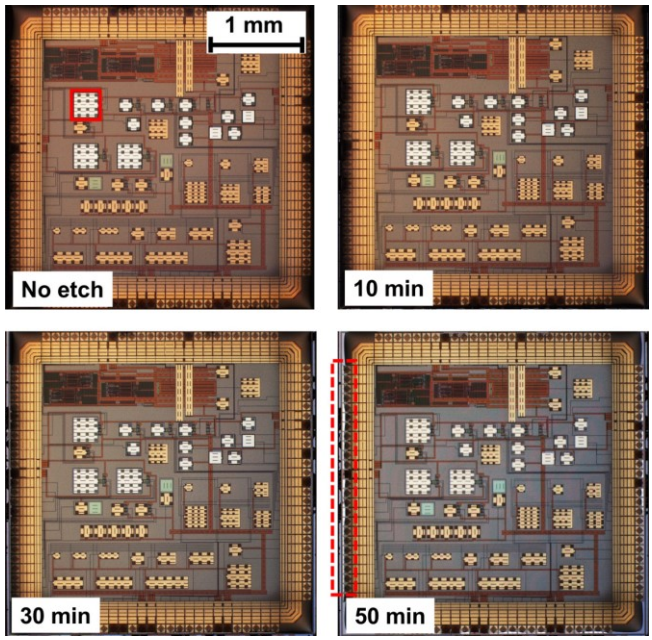

Fig. 11. Optical images of a CMOS ISFET chip, with patterned spray-coated photoresist prior etching and 10, 30 and 50 min after O_2 plasma etching (dashed area shows some of the bonding pads that are partially exposed).

Normally passivation etching on these devices uses a tetrafluoromethane and oxygen (CF_4/O_2) plasma (60 sscm CF_4 / 4 sscm O_2, 150 W, 60 mTorr) which has a lower photoresist etch rate (~90 nm/min) compared to the O_2 plasma process used (~180 nm/min). Therefore, approximately twice the time would be needed before the observed etching effects appear, as shown in Fig. 10 and to a lesser extent at latter stages in Fig. 11. Nevertheless, this would still be a problem for the spin-coated samples, as the etching time for a depassivation process can be up to 1 hour.

A similar investigation could be executed using standard wet etch processes, where Si_3N_4 is first etched with phosphoric acid (H_3PO_4), followed by SiO_2 etching with buffered hydrofluoric acid (BHF). However, for the CMOS chips used for this work, the underlying metallisation layer is aluminium. It would therefore prove very challenging to control the end point of the depassivation process, expose the aluminium without also briefly etching it with the BHF, and therefore damaging it. Nevertheless, for a number of MtMT post-processes, the wet etch approach may be applicable or desirable.

These results clearly illustrate the limitations of conventional lithographic techniques when patterning at chip-level using an RIE process. In contrast, a significantly improved performance has been demonstrated by the spray/maskless tool combination and similar results would be expected, for silicon deep RIE or wet etch post-processing. Finally it should be noted that with spray/maskless lithography, multiple chips can be patterned and etched on a single carrier wafer.

V. Conclusions

MtMTs have become increasingly popular, offering wide-ranging opportunities to innovate alongside Moore scaling and without the requirement for high investment levels. This is achieved by outsourcing the fabrication of the IC technology to foundries with MPW services, and separately developing the MtMT on relatively inexpensive, individual die rather than expensive wafers. This paper has focused on the characterisation of candidate photolithographic options for the monolithic post-processing of such foundry fabricated CMOS chips. In particular it has compared chip-based photoresist spin-coating exposed using conventional mask lithography with, on-chip photoresist spray-coating combined with maskless lithography.

The results have highlighted that on-chip spin-coating suffers from significant photoresist edge bead and thus extreme thickness non-uniformities across die. This results in poor lithographic pattern transfer, compounded with additional defects manifested during photomask contact. An alternative approach that breaks the process into a number of lithographic exposures each coated using thinner photoresist was also considered. However, this method suffers from misalignment errors and extended processing times. It should finally be noted that mask lithography is a low throughput option, as only one chip can be post-processed at a time.

The results from on-chip spray-coated photoresist have demonstrated significantly improved thickness uniformity, and a greatly reduced edge bead. Lithographic pattern transfer using a maskless system correctly resolved the majority of the test features with only a minor fraction being inadequately exposed. For large features on thick resist this could be resolved by a small increase in exposure dose, without significant CD offsets. Furthermore, maskless lithography is a contactless technology, which is therefore free from contact defects, and offers increased throughput on die post-processing. It can also deliver near-micrometre resolution on thick photoresist without any further process development being required.

The two technology options have also been assessed for

their performance when post-processing a CMOS sensor chip. This demonstrated that conventional photoresist coating and lithography was not able to support the etching process, resulting in a damaged post-processed chip. In contrast, spray-coating and maskless lithography have demonstrated that the exposed regions can be fully etched, while all other areas of the chip remain protected under the photoresist.

Monolithic post-processing of MtMT on CMOS foundry chips comes in numerous "flavours" in terms of processing requirements, with techniques and tool sets that are able to support it, ranging from low investment to high-end options. This paper has identified the benefits of a low cost, robust and high throughput prototyping option that combines photoresist spray-coating with maskless optical lithography, and can support most of the standard processing steps required for adding MtMT on single chips.

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