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Research paper

Evaluating the use of graphene electrodes in sub-micrometric, high-frequency n-type organic transistors

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ABSTRACT

In this work we report on fully operational sub-micrometric low voltage OFETs by using graphene as the source-drain electrodes pair and a high-κ ultra-thin dielectric in a local gate architecture. The impact of the graphene electrodes on the miniaturization of the organic devices has been assessed, with particular attention to the influence of the contact resistances as well as the parasitic overlap gate capacitance on the device bandwidth. By the use of a modified Transmission-Line-Method, contact resistances have been analyzed as function of the applied voltages, revealing characteristic functional trends that follow the doping state of graphene electrodes. Through impedance spectroscopy of the electrodes, cut-off frequencies as high as 10^5 Hz have been estimated, highlighting the peculiar role of quantum capacitance of graphene in such architectures.

1. Introduction

The new generation of Organic Field Effect Transistors (OFETs) has to sustain high operational frequencies, high-density integration and low operational voltages in order to meet the requirements needed for their envisaged technological applications, such as radio-frequency identification tags (RFID) [1], flexible circuitry for high-resolution displays [2], stretchable sensor arrays [3] or biocompatible implantable electronics [4,5].

The dynamic response, i.e. the maximum switching speed of organic devices, is largely influenced by the FET architecture as well as by the intrinsic transport properties of the organic semiconductor. Operational bandwidth of field-effect transistors can be characterized in terms of the transition frequency (f_T), which is essentially related to the ultimate switching speed the device can sustain as unity gain buffer. Namely [6]:

$$f_T = \frac{g_m}{2\pi C_G} \propto \frac{\mu}{L^2}, \quad (1)$$

where $g_m = \partial I_{ds}/\partial V_{gs}$ indicates the transconductance (with I_{ds} being the channel current and V_{gs} the gate source voltage), C_G is the equivalent gate capacitance, μ is the field-effect mobility and L individuates the channel length.

The maximization of the operational frequency can be thus pursued aiming at the development of novel organic semiconductors, showing higher intrinsic μ values [7–10] and thus higher g_m for a given L. Nevertheless, state-of-the-art mobility values can hardly exceed the threshold of 10^1 $cm^2V^{-1}s^{-1}$ [11].

As exemplified in Eq. (1), an alternative approach for improving OFET performances is to intervene on the device architecture by downscaling the channel lengths L towards sub-micrometric sizes.

Yet, to obtain reliable transistor operations in organic devices with $L \lesssim 1\mu m$ is still a technological challenge. The reduction of the lateral dimension is in fact typically accompanied by the rising of short-channel effects manifesting as non-linear current-voltage characteristics and high off-state currents [12] which imposes a lower limit to the gate dielectric thickness t_{ox}. A ratio $L/t_{ox} \approx 20$ is traditionally established as rule of thumb in order for the Gradual Channel Approximation to be fulfilled at the nanometric scales [13].

In addition, the downscaling of organic devices is typically

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accompanied by the rising influence of overlap capacitances, adding a non-negligible parasitic term in C_g in Eq. (1) [14], and contact resistances which might greatly degrade g_m. While the former is mainly due to the geometrical characteristics of the OFET architecture, the latter are unavoidable parasitic voltage drops occurring at the organic/electrodes interfaces [15] which are primarily ruled by the contact geometry and the energy band alignment between the electrode and the organic semiconductor [16]. Diminished charge carrier injection/extraction efficiency due to contact effects influences greatly the overall transport properties already at the micrometric scales, thus hindering the maximum achievable switching speed of the device [17].

In the last years, several studies addressed the fabrication and characterization of OFETs with nanometric architectures [18–22], providing deep insights on the possible strategies to overcome such limitations and achieve high frequency operation [23–25]. The general agreement for both short- and long-channel devices is that the control over electrode/organic interfaces, for example trough a tailored chemical functionalization of contact surfaces [26,27], or more generally a proper choice of the organic material according to its intrinsic energy band spectrum [28,29], plays a key role in improving the efficiency of charge carrier extraction/injection phenomena at the electrode interfaces.

In the present work, we propose a viable strategy to control these effects, relying on the electronic peculiarities of graphene as a tunable source-drain electrode material. In this context, the use of graphene has already been demonstrated in micrometric OFETs [30,31], organic light-emitting diodes (OLEDs) [32,33], fully organic [34] or hybrid perovskite solar cells [35], flexible devices [36–39] and in TMD-based FET photodetectors [40].

We recently showed that graphene can be a valuable choice as electrode material also in down-scaled n-type OFET architectures [41]. Taking advantages of its work function tunability [42], short channel effects are indeed mitigated in distributed-gate test-patterns characterized by 300 nm-thick SiO_2 dielectric layer. Here we combine the advantages of graphene electrodes with the use of fabrication standards for modern CMOS technology, such as ultra-thin Hafnium Dioxide (HfO_2) as high-κ dielectric and a local gate layout, addressing in detail the impact of graphene on the miniaturization of n-type OFETs towards sub-micrometric scales and high frequency operations.

2. Materials & methods

For this study, a bottom-contacts/local-gate coplanar architecture has been developed. The device is schematically depicted in Fig. 1(a).

A diapason-shaped local gate electrode (3 nm/35 nm of thermally evaporated Ti/Au bilayer) is firstly patterned on a SiO_2/Si substrate by means of deep-UV lithography. Lower and upper prongs have a width of 2 μm and 5 μm, respectively (Fig. 1(b)). The gate electrode is covered by an 8-nm-thick layer of Hafnium Dioxide (HfO_2) grown by Atomic-Layer-Deposition (ALD). The dielectric buffer ensures a capacitive coupling of $C_{ox} \sim 2.2\mu F/cm^2$, evaluated considering its nominal thickness and a conservative estimation of the dielectric constant, $\kappa = 20$ (typical reported values range from 20 to 25 [43,44]).

The electrical supply lines departing from the center of the device array, where the actual nanopatterned graphene electrodes will be located, and the contact pads are patterned on top of the oxide layer through deep-UV lithography and the deposition of a second Ti/Au metallic bilayer (3 nm/80 nm). Further details on the fabrication of the diapason-like gate electrode, the oxide layer and the supply lines can be found elsewhere [45]. A large area CVD grown monolayer graphene sheet is subsequently transferred on top of the prepatterned substrate following the wet transferring approach described in ref. [46]. Graphene is then electrically contacted by means of an additional over imposed metallic pattern (3 nm/30 nm Cr/Au bilayer). The actual OFET channels are lastly outlined by means of Electron Beam lithography (EBL) and

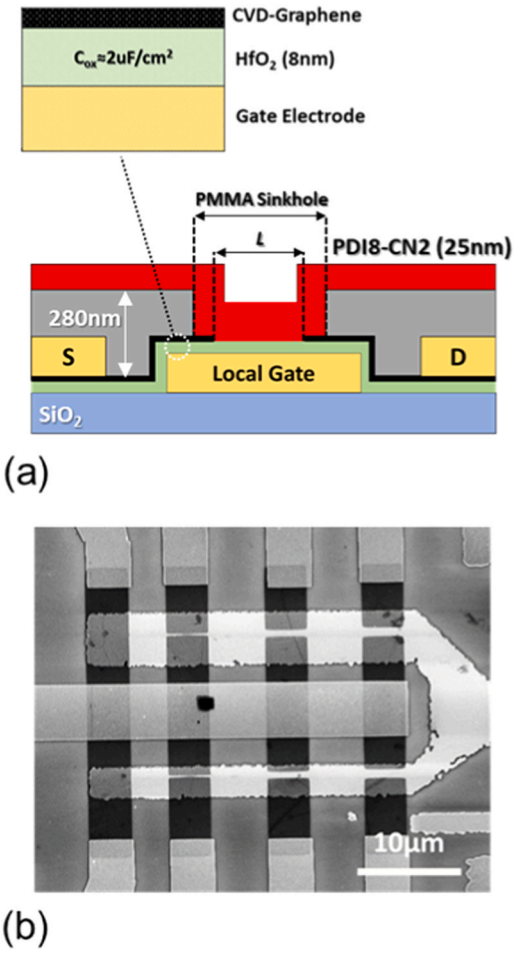

Fig. 1. (a) Schematic depiction of the OFET layout under investigation. Grey areas represent a 280 nm thick PMMA film (b) SEM image of the nanopatterned graphene electrodes in the bottom-contacts/local-bottom-gate configuration. The diapason-shaped gate electrode has two prongs, 2 μm and 5 μm wide. The dielectric layer is an 8 nm thick HfO_2 buffer layer grown by Atomic Layer Deposition.

Reactive Ion Etching (RIE) through exposure of the samples to oxygen plasma (P_{O2}=10 mTorr/20 sccm; *power* = 50 W; *time* = 20 s). Immediately after the oxygen plasma, samples are exposed to a hexamethyldisilazane (HMDS from Aldrich™ Chemistry) saturated atmosphere ($P \approx$ 10mTorr) at 150 °C for 2 h in order to reduce charge trapping phenomena occurring at the organic/dielectric interfaces [47,48].

Three different channel lengths (L = 200 nm, 550 nm, 750 nm) are considered while the channel width W is fixed at 4 μm (Fig. 1(b)). Each final array contains 8 devices sharing a common source gold. Two of the devices consist of an unetched micrometric graphene strip in a Graphene Field Effect Transistor (GFET) configuration, (L = 9 μm and W = 4 μm). The electrical characterization of these GFETs is performed before the organic semiconductor deposition in order to assess the intrinsic graphene characteristics and in particular to determine its doping state. As the organic semiconductor, we employed a perylene- 3,4,9,10-tetracarboxylic acid diimide derivative called PDI8-CN2 (Flexterra ActiveInk ™ N1200), a widely studied and reliable n-type compound [49–53].

A 25 nm thick PDI8-CN2 thin film is deposited by OMBD. The values of deposition rate (R = 0.7 nm min $^{-1}$) and substrate temperature (T_{sub}

= 94 C) were fixed according to our previous works concerning growth optimization on SiO_2 test patterns [54].

Before the organic deposition, the surface is isolated by a 280 nm-thick PMMA layer (All-Resist, AR-P-679.04 950k with 4% solid content in ethyl-lactate, spun at 6000 rpm for 60 s). The effective device areas are defined by micrometric patterned sinkholes. This geometry was chosen in order to minimize the possible presence of fringing currents affecting the substrate areas which do not geometrically intercept the gate track. (Fig. 1(a)), given the tendency of PDI8-CN2 to show negative threshold voltages. The choice of such a material, as additional insulating layer, was primarily driven by its standard use in the previously described EBL processes and by its compatibility with graphene. As further discussed in the following sections, in fact, the presence of the PMMA layer does not influence considerably its doping state.

The DC and AC electrical characterizations of the devices are performed in vacuum and at room temperature in a Janis ST-500 three-armed probe station by means of a Keithley-2612A SourceMeter™ and an Agilent™ 4284 A Precision LCR Meter, respectively. Particular care was taken to protect the OFETs from ambient light during electrical measurements.

3. Results and discussion

Transistor operations can be observed referring to the output curves ($I_{ds} - V_{ds}$) reported in Fig. 2(a)-(c). The effect of the downscaled dielectric buffer layer is evidenced by the fact that current saturation is achieved independently of the channel length for $V_{ds} \geq 3$ V and -2 V$< V_{gs} <+2$ V while minor hysteresis phenomena are present for forward/backward sweeping of the drain-source biases. The scaling behavior of the maximum current values follows the $I \propto 1/L$ trend in agreements with the standard MOSFET model [55].

Typical transfer curves ($I_{ds} - V_{gs}$), acquired in the saturation regime ($V_{ds} = +5V$) are reported in Fig. 2(c) as a function of the channel length. Off-state currents are limited between 1×10^{-9} A and 3×10^{-9} A with on/off ratios reaching values of $\approx 10^2$ for $L = 200$ nm and on-set voltages V_{on} settled at approximately -1 V. Different gate prong widths (Fig. 1(b)) do not influence significantly the current modulation, as it can be seen from the transfer curves referred to a 5 μm wide gate track reported in Fig. S1 of the Supplementary Information section. The field-effect mobility values in the saturation regimes are extracted from the transfer curves by applying standard MOSFET model equations: [55].

$$\mu_{sat} = \left(\frac{\partial\sqrt{I_{ds}}}{\partial V_{gs}}\right)^2 \frac{2L}{WC_{ox}}, \tag{2}$$

where C_{ox} is the oxide capacitance per unit of area, L is the channel length and W is the channel width. Maximum mobility $\mu_{sat} \approx 2 \cdot 10^{-3} cm^2 V^{-1} s^{-1}$ is typically observed. These values are one order of magnitude lower than those recently reported for PDI8-CN2-based devices with graphene electrodes and micrometric channel lengths [56], showing once more that the downscaling of L towards nanometric scales usually leads to a significant drop of the mobility given the non-negligible presence of contact resistances that depresses the charge transport properties of the overall devices.

Such hypothesis is further supported by the clear presence of s-shaped output curves at low drain-source bias ($V_{ds}<2$ V), especially for the shortest channel lengths, that also indicates the dependence of R_C from the applied V_{ds}. An estimation of R_C can be obtained by the application of the widely employed Transmission-Line -Method (TLM) [57–59]. With this approach, R_C is indirectly retrieved as the y-intercept of the width-normalized total resistance (R_{tot}). Namely:

$$R_{tot} \times W(L) = R_{sheet} L + R_C W. \tag{3}$$

In the linear regime, the total device resistance can be in fact assumed as the sum of two distinct contributions: (i) a sheet contribution ($R_{sheet}L$), which scales linearly with the channel length and whose values are dominated by the intrinsic mobility of the organic semiconductor and (ii) an additional term related to the total spurious contribution of contact effects, occurring indistinctly at both the Drain and Source interfaces (R_C). The TLM accuracy, however, is significantly limited by the parameters variability that may characterize different OFETs, especially at low V_{gs} and at very short channel scales.

In our case, given also the limited number of considered L, such limitations can be overcome by the application of a Modified TLM (M-TLM), as proposed by Xu et al. [60] In such approach both terms of Eq. (3) are multiplied by $1/L$, giving more weight to the $R_C W$ contribution of shortest channel data:

$$\frac{R_{tot} \times W(L)}{L} = R_{sheet} + R_C W \frac{1}{L}. \tag{4}$$

The contact resistance is then determined as the slope of the linear fits of the R_{tot} vs L. Results of the applied M-TLM are plotted in Fig. 3. For the sake of completeness, a comparison of reliability between standard TLM and M-TLM is reported in Fig. S3 of the Supplementary Information section. For the data analysis we took into account the specific onset voltage (V_{on}) of the single devices and we considered I_{ds} output curves relative to the equivalent applied gate biases ($V_{gs}' = V_{gs} - V_{on}$). The considered V_{ds} range is limited between 0.3 V and 1 V in order for the analysis to be contained within the pinch-off region. For $V_{ds} < 0.3$ V channel current start to be comparable to the corresponding leakage currents. The M-TLM, as a consequence, loses its reliability to a greater extent.

As a first general observation, the R_C vs V_{gs} dependence follow the form $Rc\left(V_{gs}'\right) \propto V_{gs}'^{-\beta}$, in very good agreement with recently reported R_C estimations performed by Kelvin Probe measurements in a micrometric

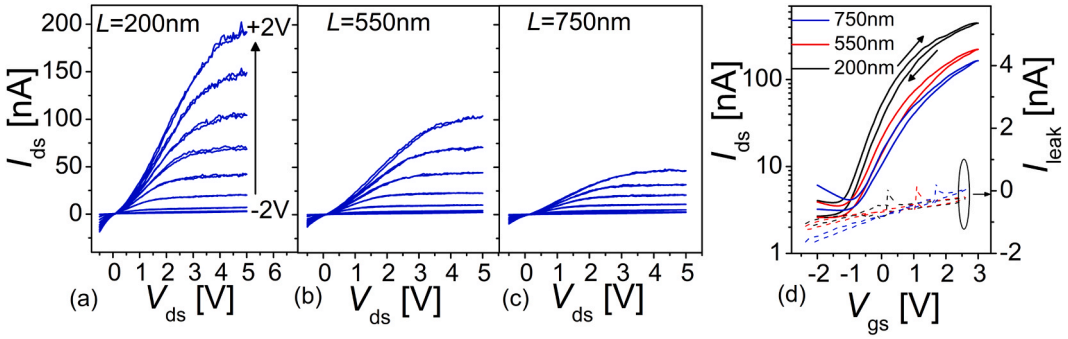

Fig. 2. (a)-(c) Output curves for the bottom-contacts/local-bottom-gate nanometric OFETs with CVD-graphene electrodes and PDI8-CN_2 as organic semiconductor. Plotted data are referred to three considered channel lengths (200 nm$<L<$750 nm). Channel width W is fixed at 4 μm for every L here considered. (d) Transfer characteristics in saturation regime ($V_{ds} = +5$ V) The black arrows indicate the sweeping direction of the gate voltage. (a) Gate-source bias is varied in the range -2 V$< V_{gs} <+2$ V with ΔV_{gs}=0.5 V. (b) The dashed lines correspond to the leakage currents flowing in correspondence of the gate-source interface.

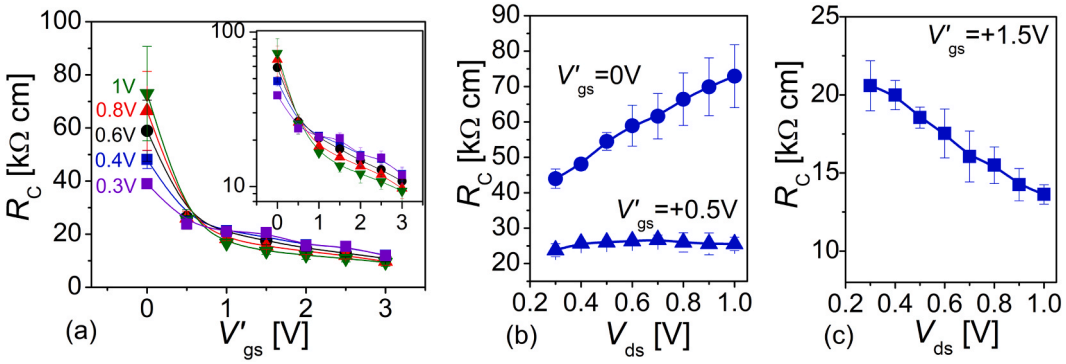

Fig. 3. (a) Width-normalized contact resistances obtained via the M-TLM of Eq. (4) vs V'_{gs}=V_{gs}-V_{on}, with V_{on} being the onset voltage, for V_{ds} values contained within the pinch-off region of the OFETs (0.3–1 V). The inset shows the same dataset in log scale. (b) and (c) R_C behavior vs the applied V_{ds} for fixed V'_{gs} values representative of different graphene electrode doping states: V'_{gs} = 0 V corresponding to p-doped graphene, V'_{gs} = 0.5 V representing the neutrality point and V'_{gs} = 1.5 V for n-doped electrodes. For the sake of clarity, in (a) only a small collection of V_{ds} values considered in (b) and (c) is reported.

graphene-based OFETs architecture with PDI8-CN2 as organic semiconductor [56].

Minimum R_C values in the range of 10–20 kΩ cm are observed for fully accumulated channels (V'_{gs}>1 V). However, *Rc* is strongly influenced by the applied drain-source bias, as it can be seen from the inset of Fig. 3(a). This can be more clearly understood referring to Fig. 3(b) and (c) where R_C data are explicitly plotted as a function of V_{ds} for different fixed V'_{gs} (0 V, +0.5 V and 1.5 V). Close to the onset voltage and in its vicinity(Fig. 3(b)), R_C values increase by increasing V_{ds} while the functional trend is interestingly inverted for V'_{gs}> +0.5 V where R_C decreases from 20 kΩ cm to 14 kΩ cm for V_{ds} approaching + 1 V.

These findings can be directly related to the graphene polarization and its doping state for different V_{gs}. As reported in Fig. S2, bare graphene electrodes are observed to be nearly intrinsic: i.e. no substantial displacement of the neutrality point from 0 V is observed. The doping state is only influenced to a minor extent by the presence of the PMMA layer which displaces V_{np} towards a p-doped condition (+0.5 V). The uphill (downhill) path of R_C vs V_{ds} can be thus directly related to the relative position of the graphene work function W_f: i.e. its p-type (n-type) doping state. Within this picture, contact effects are dominated not only by the gate modulation of the carrier concentration within the organic layer [61] but also by the gate-modulated energy mismatch between the tunable work function of graphene ($W_f(V_{gs} - V_{np})$) and the Lowest-Unoccupied-Molecular-Orbitals band (LUMO) of the organic semiconductor [30]. A simplified depiction of the energy band alignment of the considered heterointerface is reported in Fig. 4. According to those assumptions, for $V_{gs} \lesssim V_{np}$, graphene is characterized by W_f"4.5 eV [42] while the LUMO band of the PDI8-CN2 can be assumed to be settled around the commonly reported value of ≈ 4.3*eV* [62]. This implies that charge injection from the Source electrode is primarily suppressed by the V_{gs}-enhanced barrier (Fig. 4(a)) in addition to the presence of a predominantly charge-depleted channel, given that in such configuration $V_{gs} \approx V_{on}$ and very few electrons are available for the transport to take place. The peculiar linear increase of R_C vs V_{ds} is in total accordance with the already encountered phenomenology of micrometric graphene-based architectures, as we reported in ref [56]. In that case, graphene electrodes were intrinsically p-doped and an increasing trend with R_C values ranging between 25 kΩ cm and 125 kΩ cm were retrieved in linear regime via Kelvin probe microscopy analysis. More generally, this unusual V_{ds} dependence of R_C for the negatively biased gate can be explained by the presence of an extended injection area, thanks to the electric-field permeability of graphene electrodes, that enables current spreading at the Source interface. The situation is in fact similar to what reported by Valletta et al. for top-contacts fully-printed micrometric p-type devices [63]. In our case it could be reasonable to speculate that the same extended injection area, governed by reversed diode current, might occur also in our bottom-gate layout. For higher Drain-Source biases the effective current spreading area is reduced by bringing the injection boundaries progressively closer to the source edge, thus increasing the overall R_C, assuming a fixed contact resistivity. Further investigations are of course needed in order to specifically assess this kind of injection process, with particular attention, for example, to the role of high transversal electric field building up in between the source-drain pair at the nanometric scales (up to 10^6 V/m for L=200 nm). Conversely, for $V_{gs} \gtrsim V_{np}$, charge injection is favored being the graphene W_f approaching the PDI8-CN2 LUMO band (Fig. 4(b)). This implies not only a substantial reduction of the R_C values, given also the

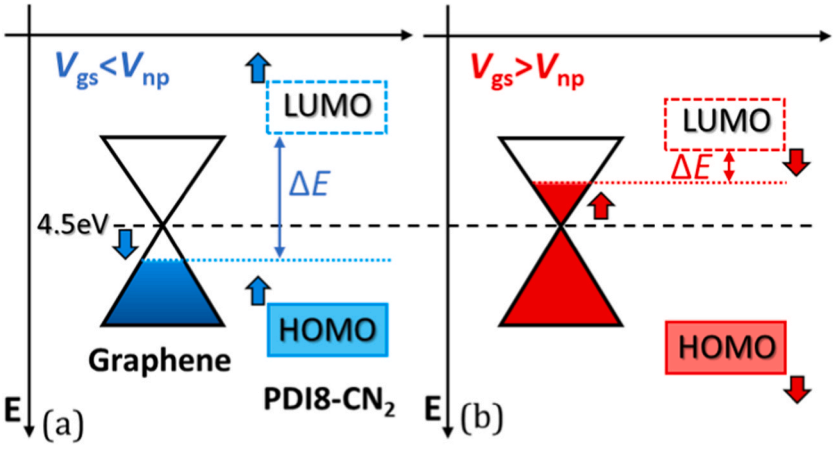

Fig. 4. (a) For gate voltages lower than the neutrality point of graphene (V_{gs}<V_{np}), graphene work function and LUMO level can be considered as moving in opposite directions. (b) For V_{gs}>V_{np} charge accumulation within the organic channel lowers the LUMO band while n-doping of graphene rise concomitantly its W_f, resulting in a reduced energy barrier for charge carriers to be injected. Schematic depiction of the energy band alignment of the graphene/organic heterointerface as function of the applied gate-source bias.

higher I_{ds} values of the fully accumulated organic channel (lower R_{sheet}), but also an R_c vs V_{ds} trends similar to those reported for gold-based architecture with gate-independent contact barriers [51]. Here the V_{ds} modulation is a simple consequence of the electric-field-dependent transport properties of organic materials which are often observed as dominated by Frenkel-Poole transport [64,65]. Lastly, in the intermediate case of $V_{gs} \approx V_{np}$, contact effects appears to be less sensitive to the applied Drain-bias (Fig. 3(b)) as a consequence of the degenerate Density of States of Graphene in the proximity of the neutrality point, where fewer charge carriers are available for the injection into the organic semiconductor from the graphene surface.

As described in the introduction, despite being one of the main factors limiting the transconductance g_m (and thus f_T), contact resistances are not the only spurious contribution that should be addressed concerning the fabrication of sub-micrometric architectures. Aiming to the maximization of the device bandwidth, the role of gate capacitance in Eq. (1) must be carefully investigated. Particularly, C_G has necessarily to take into account the contribution of both the channel capacitance, individuated by the geometrical contribution C_{ox} given by the active channel, and the parasitic overlap capacitance per unit of area (C_{ov}) as depicted in Fig. 5(a). The latter is typically due to the geometrical overlay of the source and drain surfaces and the gate area whenever the two are not in perfect registration. Under these assumptions, f_T can be rewritten as:

$$f_T \approx \frac{g_m}{2\pi[C_{ov}S_{ov} + C_{ox}S_{ch}]}, \tag{5}$$

where $S_{ov} = WL_{ov}$ indicates the overlap area, with L_{ov} being the overlap length, while $S_{ch} = WL$ is the effective channel area.

We have measured surface normalized overlap capacitances C_{ov} through impedance spectroscopy as a function of the frequency ($1kHz \leq f \leq 1MHz$), using a sinusoidal probe signal with $V_{rms} = +0.05$ V and considering the actual overlap length L_{ov} as deduced from SEM images. Several curves have been acquired adding a fixed DC bias to the probing AC signal (-2 V$<V_{bias}<2$ V with steps of 0.2 V) in order to exploit the semi-metallic nature of graphene and its work-function tunability by gate electric fields. Schematics of the experimental set-up is depicted in Fig. S4(a). The system comprising the Au gate track, the dielectric buffer and the semi-metallic counter electrode behaves as an ideal parallel-plates capacitor. The impedance spectroscopy data, reported in Fig. S4(b) and (d), indicate in fact a $|Z| \propto 1/f$ behavior and $\Theta = -\pi/2$ for $f > 1$ kHz and for every V_{gs} considered.

Fixing the frequency, it is also possible to plot the surface-normalized *C-V* trends for the bare graphene electrodes, i.e. before the organic thin film deposition. As reported in Fig. 5(b), in this case data suggest a double dependence both on the frequency of the probing signal *f* and on the applied V_{gs}. The C_{ov} reaches a minimum value in correspondence of the neutrality point of graphene and it shows an overall behavior which retraces exactly the transfer curves of the GFETs (Fig. S2).

While the frequency dependence is likely due to electric dipoles originated by organic contaminations or by the dielectric relaxation of the HfO_2 thin film [66,67], the V_{gs} behavior is a clear signature of the quantum capacitance of graphene [68].

In this configuration, in fact, C_{ov} can be modeled as a capacitance series given by the geometrical contribution of the oxide layer (C_{ox}) and of the graphene surface (C_{gr}), namely:

$$C_{ov}^{-1} = C_{ox}^{-1} + C_{gr}^{-1} \tag{6}$$

A schematic depiction of the equivalent circuit considered is reported in Fig. S4(c). Theoretical considerations on the quantum capacitance contribution of graphene (C_{gr}) are typically inferred from two-dimensional free-electron gas models and in particular from the finite density of states of the channel and the extra energy needed for filling states with higher momentum [68]. Further investigations of such phenomena are currently under consideration. It is worth noting that C_{gr} is usually neglected in the standard configurations with thicker dielectric layers and lower κ values while it must be taken into account when the C_{gr} and C_{ox} values in Eq. (4) are comparable. We note that C_{gr} can be considered as beneficial in our case: since its series contribution, the total C_{ov} is lower than what it should be observed for standard metal electrodes. In the latter case, in fact, the overlap term would be simply $C_{ov} = C_{ox} = \epsilon_0\epsilon_r/d_{ox} \approx 2.2\mu F cm^{-2}$, i.e. an average values that is 20% higher than those reported for our transistors. The impedance spectroscopy of the entire device, i.e. the dynamic response of the heterojunction comprising the graphene electrodes/organic thin film heterojunction, can be retrieved from Fig. 5(c) where the same analysis has been conducted after the thin film growth. Three different regimes can be discerned according to the considered frequency *f* of the probing signal. i) For low *f* it is possible to observe the contributions of the charge carriers of both the organic semiconductor and the graphene electrode. In this case, charge depletion within the active channel is followed by a first increase of the total device capacitance for -1 V$<V_{gs}<0$ V related to the charge accumulation within the organic semiconductor, followed by the contribution from the n-branch of graphene carriers when V_{gs} is further increased.

ii) Charge carriers, whose effective mobility is limited by both the intrinsic properties of the polycrystalline organic solid and the injection-extraction efficiency at the electrodes, struggle to follow the probing signal for *f* approaching values in between 100 kHz and 200 kHz, resulting in a sharp reduction of the organic contribution over the total parallel capacitance ($C_{ov}+C_{ch}$).

iii) Lastly, a bare graphene response, similar to those observed in Fig. 5(b), is reestablished for *f* approaching 1 MHz. In this case the electrodes contributions dominate over the total capacitance of the device.

The same conclusions can be retrieved considering Fig. S5 of the Supplementary Information Section where the C_{ch} and C_{ov} terms are individually discerned for the sake of clarity. In particular, the C_{ch} term has been singled out by subtracting the measured electrode contribution (C_{ov}) at 1 MHz from the total parallel capacitance ($C_{tot}=C_{ov}+C_{ch}$) of Fig. 5(c), indicating the same behavior at $f > 100$ kHz for which the C_{ch} modulation with V_{gs} is almost totally hindered.

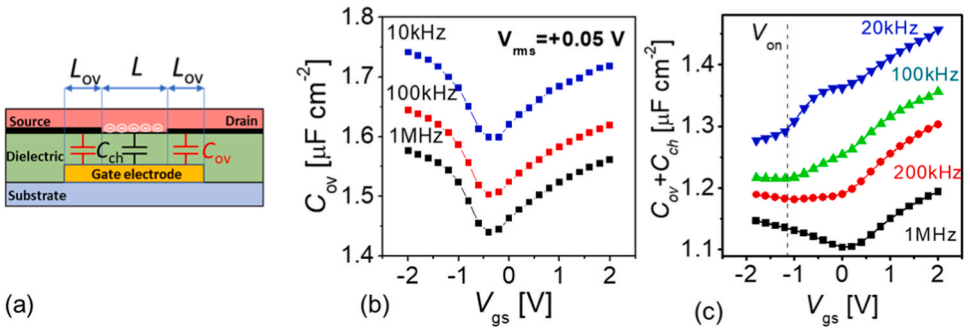

Fig. 5. (a) Schematic depiction of the OFET highlighting the presence of the overlap capacitance contributions in parallel with the actual channel term. (b) Surface-normalized overlap capacitance of the graphene electrodes measured as function of the applied gate bias and for different fixed frequencies. (c) Total capacitance ($C_{ov}+C_{ch}$) of a device with $L = 200$ nm comprising also the organic contribution within the active channel. Data have been acquired as function of the applied V_{gs} and for frequencies falling in a similar range with respect to (b).

This observed trade-off frequency, indirectly suggesting the maximum AC capabilities of our devices, is further confirmed through the direct calculation of the transition frequency f_T via Eq. (5).

Results are reported in Fig. 6(a) considering g_m data for the same transistor array presented previously. For simplicity, data have been obtained taking the overlap capacitance of Fig. 5(b) evaluated at 100 kHz (the effect of the frequency dependence of C_{ov} being negligible).

As a general observation, cut-off frequencies follow the corresponding trend of the transconductances as a function of V_{gs} and showing f_T as high as 10^5 Hz for $L = 200$ nm. Those values are in line with reported values for n-type organic semiconductors and photolithographically patterned gate electrode [69].

Finally, it is worth to note that f_T could be easily improved towards the MHz scale, i.e. the standard benchmark values for modern applicability of our graphene-based OFETs in RFID technology, with straightforward modifications. For instance, reducing the overlap length L_{ov} would increase the cut off frequency by almost a factor of 10, as highlighted in Fig. 6(b), where the maximum of f_T is compared to the ideal case of $C_{ov} = 0$ in Eq. (5). Similarly, an increase of the organic field-effect-mobility would result as well in a corresponding increase of f_T. Effects of Arylene Diimide thin film growth conditions on n-channel OFET performance is in fact a well-known key factor which strictly depends on the relative interaction between the substrate and the organic precursor [49].

4. Conclusions

In conclusion, we presented a viable route to realize short channel n-type OFET. By a novel design of the architecture comprising graphene as the electrode material, we fabricated low-voltage devices with a local gate structures, ultra-thin (8 nm) Hafnium Dioxide as dielectric buffer layer and sub micrometric channel lengths. We addressed the impact of graphene electrodes on the miniaturization of n-type organic devices by evaluating the contact resistances (R_C) by means of a modified TLM method. The behavior of R_C as a function of the drain-source and gate-source bias has been analyzed revealing a distinctive response according to the applied V_{gs}. For gate biases falling in the range of p-doped graphene, R_C is observed to increase for increasing V_{ds}. Conversely, decreasing R_C values were retrieved for n-doped electrodes, highlighting the role of the tunability of graphene work function in our architecture and its impact on the direct control over the energy barrier at the electrode/organic interfaces.

Dynamic capabilities of OFETs have been studied with particular attention to the role of overlap capacitance of graphene electrodes by impedance spectroscopy analysis. The enhanced capacitive coupling of the HfO_2 gate interface highlighted the presence of the quantum capacitance contribution of the graphene electrodes in series with the geometrical contribution of the dielectric buffer layer. The presence of graphene electrodes results in an approximately 20% reduction of the intrinsic overlap capacitance if compared with a theoretical Au/HfO2/Au structure.

Lastly, we indirectly evaluated the operational frequencies of the devices by measuring the overlap capacitance contribution of the graphene electrodes. Maximum values as high as 100 kHz are estimated for $L = 200$ nm and fully accumulated channel. While an operation speed in the kHz range is already suitable for realistic technological applications of OFETs, the projection of the maximum operational frequencies towards the MHz range is in sight through achievable technological optimization.

CrediT authorship contribution statement

Federico Chianese: Conceptualization, Investigation, Formal analysis, Writing - original draft. **Andrea Candini**: Conceptualization, Writing - review & editing, Supervision. **Stefano Lumetti:** Resources, Writing - review & editing. **Camilla Coletti:** Resources, Writing - review & editing. **Neeraj Mishra:** Resources, Writing - review & editing. **Marco Affronte**: Conceptualization, Supervision, Writing - review & editing. **Antonio Cassinese:** Conceptualization, Supervision, Writing - review & editing, Project administration.

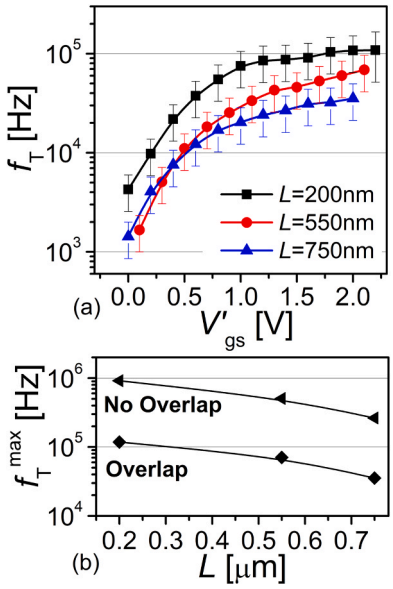

Fig. 6. (a) Transfer frequency calculated by means of Eq. (5) for the three different channel lengths considered in this study. (b) Comparison between the maximum ft as function of L for data obtained in (a) (filled triangles) and theoretical values obtained considering $C_{ov} = 0$ in Eq. (5) (filled diamonds).

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.synthmet.2020.116683.

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