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Inverter Design for SiC-based Electric Drive Systems with Optimal Redundant States Control of Space Vector Modulation

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To my family and friends

Inverter Design for SiC-based Electric Drive Systems with Optimal Redundant States Control of Space Vector Modulation

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Abstract

The need for inverters with ever increasing power density and efficiency has recently become the driving factor for research in various fields. Increasing the operating voltage of the whole drive system and utilizing newly developed SiC power switches can contribute towards this goal. Higher operating voltage allows the design of drives with lower current, which leads to lower copper losses in cables and machine, while SiC switches can drastically increase the inverter efficiency. Offshore renewable power generation, such as tidal power, is a typical application where the increase of operating voltage can be highly beneficial. The ongoing electrification of transportation calls also for high power electric powertrains with high power density, where SiC technology has key advantages.

In the first part of the thesis, suitable control schemes for inverters in synchronous machine drive systems are derived. A properly designed Maximum Power Point Tracking algorithm for kite-based tidal power systems is presented. The speed and torque of this new tidal power generation system varies periodically and the inverter control needs to be able to handle this variable power profile. Experimental verification of the developed control is conducted on a 35 kVA laboratory emulator of the tidal power generation unit.

Electric drives using multilevel inverters are studied afterwards. Multilevel inverters use multiple low-voltage-rated switches and can operate at higher voltage than standard two-level inverters. The Neutral Point Clamped (NPC) converter is a commonly used multilevel inverter topology for medium voltage machine drives. However, the voltage balancing of its dc-side capacitors and the complexity of its control are still issues that have not been effectively solved. A new method for the optimal utilization of the redundant states in Space Vector pulse-width-Modulation (SVM) is proposed in this thesis in order to control its dc-link voltages. Experimental verification on a 4-kV-rated prototype medium-voltage PMSM drive with 5-level NPC converters is conducted in order to validate the effectiveness of the proposed control technique.

Low switching and conduction losses are typical characteristics of SiC switches that can be utilized to build inverters with high power density, due to the increased efficiency and smaller form-factor. Due to the above, SiC power modules have been particularly attractive for the automotive industry. The design approach of 2-level automotive inverters has been studied in this project. Moreover, a new design approach for the cooling system of automotive inverters has been developed in this thesis, which fine-tunes the inverter heatsink utilizing standard legislated test routines for electric vehicles. Multiple conjugate-heat-transfer (CHT) computation results showcase the iterative optimization procedure on a test-case 250 kW (450 A) automotive SiC inverter.

Finally, the experimental testing of high power machine drives in order to verify the control and the hardware design is an important step of the development process. Thus, the performance of the prototype 450 A SiC 2-level inverter has been experimentally validated with a power hardware-in-the-loop (P-HIL) set-up that emulates an automotive drive system. Several challenges have been addressed with respect to the accurate modelling of the motor and the control of the circulating power in the system. A new control technique utilizing the redundant states of the SVM has been developed for this set-up to effectively suppress the zero-sequence circulating current to 3.3% of the line current at rated power.

Index Terms: Common Mode Voltage, Electric Vehicle, Maximum Power Point Tracking (MPPT), Medium Voltage Converters, Multilevel, Space Vector Modulation, Neutral Point Clamped (NPC), Power Hardware-in-the-Loop, Silicon Carbide (SiC), Tidal power, Voltage balancing.

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Γεώργιος Μαδεμλής / Georgios Mademlis
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List of Acronyms

2LC	2-level Converter
ADC	Analog-to-Digital Converter
ANPC	Active Neutral Point Clamped
B2B	Back-to-Back
BEV	Battery Electric Vehicle
CAD	Computer-aided Design
CFD	Computational Fluid Dynamics
CHT	Conjugate Heat Transfer
DBC	Direct Bond Copper
DSP	Digital Signal Processor
DTC	Direct Torque Control
EESM	Electrically Excited Synchronous Machine
EMF	Electromotive Force
EMI	Electromagnetic Interference
ePWM	enhanced Pulse Width Modulator
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
FC	Flying Capacitor
FEM	Finite Element Method
FOC	Field Oriented Control
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
HVDC	High Voltage Direct Current
IC	Integrated Circuit

IGBT	Insulated-Gate Bipolar Transistor
IM	Induction Machine
IPMSM	Interior Permanent Magnet Synchronous Machine
IUT	Inverter-Under-Test
LPF	Low-Pass-Filter
L2L	Line-to-Line
MCU	Microcontroller Unit
MMC	Modular-Multilevel-Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
MTPA	Maximum Torque Per Ampere
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PI	Proportional-plus-Integral
PLL	Phase-Locked Loop
PMSG	Permanent Magnet Synchronous Generator
PMSM	Permanent Magnet Synchronous Machine
pu	Per Unit
PWM	Pulse-Width Modulation
RES	Renewable Energy Sources
rms	root mean square
rpm	revolutions per minute
Si	Silicon
SiC	Silicon Carbide
SG	Synchronous Generator
SMD	Surface-Mount Device
STATCOM	Static synchronous Compensator
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TSR	Tip Speed Ratio
TUSK	Tethered UnderSea Kite
VSC	Voltage Source Converter
WBG	Wide-Bandgap

List of Symbols

Each variable symbol has *italic* font and is defined in the text where it is first mentioned. **Bold** symbols in the thesis describe vectors.

The basic variables of the thesis defined below are sorted alphabetically:

*	reference signal
θ	angle [°]
τ	time constant [s]
ω_r	angular velocity of the electrical machine [rad/s]
ω_{turb}	rotational speed of the turbine [rad/s]
a_c	machine current controller bandwidth [rad/s]
a_ω	generator speed controller bandwidth [rad/s]
a_{cs}	grid current controller bandwidth [rad/s]
a_{PLL}	grid PLL bandwidth [rad/s]
a_{DClink}	grid dc-link controller bandwidth [rad/s]
B_a	active damping term [Ω]
C_P	performance coefficient of the tidal turbine [%]
D	altitude angle of the TUSK plant [deg] (only for Chapter 3)
d_T	duty cycle of the power switch T
f_{sw}	switching frequency [Hz]
i	trajectory position of the kite (only for Chapter 3)
i_0	zero-sequence current [A]
i_{bl}	ac current used for voltage balancing of the 5-level NPC drive [A]
I_{d1} ... I_{d5}	dc currents at the clamping points of a 5-level NPC converter [A]
i_e	motor stator current [A]
i_{gen}	generator stator current [A]
i_s	grid current [A]
J	moment of inertia [kg·m^2]
K_I	integral gain of a PI controller
K_P	proportional gain of a PI controller

L_d	stator inductance in the d-axis [H]
L_f	grid filter inductance [H]
L_q	stator inductance in the q-axis [H]
L_1 ... L_3	inductances of the balancing converter for the NPC drive [H]
$\hat{m}$	modulation index [%]
N	number of levels of the phase voltage of a VSC
p	electrical machine's pole pairs
$\vec{\boldsymbol{P}}(x, y, z)$	parametric equation of the Viviani's Curve in space coordinates
P_{loss_i}	power losses at the trajectory point i owed to the drag of the kite [W]
P_m	turbine mechanical power [W]
P_{grid}	active power at the PCC [W]
Q_{grid}	reactive power at the PCC [W]
r	cylinder radium of the Viviani's Curve [m] (only for Chapter 3)
R	sphere radium of the Viviani's Curve [m] (only for Chapter 3)
R_S	machine stator resistance [Ω]
R_T	turbine radius [m]
t	time [s]
T_e	electromagnetic torque of the machine [Nm]
T_{grid}	electrical torque at the PCC [Nm]
T_m	mechanical torque of the machine [Nm]
t_r	rise time [s]
T_{sw}	switching period of a power converter [s]
t_D ... t_G	dwell times of the switching states in the SVM [s]
v^*	normalized reference voltage of a VSC
v_0	common mode voltage [V]
V_a	effective water speed [m/s]
V_{C1} ... V_{C4}	dc capacitor voltages of a 5-level NPC converter [V]
V_{CC}	supply voltage for electronic circuits [V]
V_{dc}	voltage of each dc-link capacitor bank [V]
$V_{dc\ tot}$	total dc-link voltage of a drive [V]
V_D ... V_G	space vectors of the SVM in (α', β') coordinates
V'_D ... V'_G	three-phase switching vectors of the SVM
v_e	machine terminal voltage [V]
V_{GS}	MOSFET gate-source voltage [V]
v_s	grid voltage at the PCC [V]
V_{tide}	tidal free stream speed [m/s]
V_{tr}	voltage of the triangular carrier in SPWM [V]
$\hat{V}^*_{ph}$	reference of the amplitude of the converter phase voltage [V]

Contents

Chapter 1

Introduction

1.1 Background

Electrical machine drives with high efficiency and power density are currently required in many applications and are under research by both the industry and the academia. Electrification of ground transportation is seen nowadays as one of the most viable solutions for sustainable transports. The electric drive, including a motor and an inverter, is one of the main components of an electric vehicle. An increase of the drive system efficiency is highly beneficial, since this could increase the energy autonomy of battery-powered vehicles. At the same time, automotive drive systems with higher power capabilities than in the past are now requested by customers, while the industry strives to keep the volume, weight and cost of the powertrain as low as possible. Therefore, there is a high demand towards electric drives with high power density.

Exploitation of new renewable energy sources for electric power generation is another application where further improvement of the efficiency and power density of the generator drive has high importance. For example, harvesting electric power from sea tides has seen growing research interest and, thus, the design of the power conversion system is a highly important and challenging task.

The state of the art and the main challenges in designing machine drives for electric vehicles and renewable energy source applications are presented in the following two subsections.

1.1.1 Motor Drives in Battery Electric Vehicles

The propulsion system of a battery electric vehicle (BEV - i.e. vehicle that uses rechargeable batteries as its main energy source) has the following typical structure as cited from [1] and shown in Fig. 1.1. The main motor drive consists of an electric motor and a three-phase inverter. The dc-side of the inverter is supplied by the high-voltage (HV) battery, while a low-voltage (LV) battery is utilized to provide energy to the low-power electronics of the vehicle. The structure of the vehicle charging system and charging ports are described by the IEC 61851-23:2014 and IEC 62196-3:2014 standards [2, 3] and by SAE J1772 [4]. The vehicle has an on-board charger suitable for charging the HV battery through the ac grid, while dc charging is also possible to enable fast charging capabilities.

Modifications of the standard electric powertrain structure have been suggested to reduce the number of components and the cost. For example, the inverter of the main powertrain can be utilized also as an on-board charger [1]. Wireless charging of the HV battery becomes also more and more attractive as this technology evolves [5]. A dc/dc converter between the HV battery and the dc-link of the drive has been used for the cases when the variable voltage of the HV battery does not match the rated voltage of the drive [6]. Hybrid electric vehicles have also similar powertrain structure, with the addition of the internal combustion engine, which can be placed in parallel or in series to the electric powertrain [7].

A closed-loop cooling system is installed in the vehicle that is responsible for extracting the heat out of the motor, the inverter and the on-board charger.

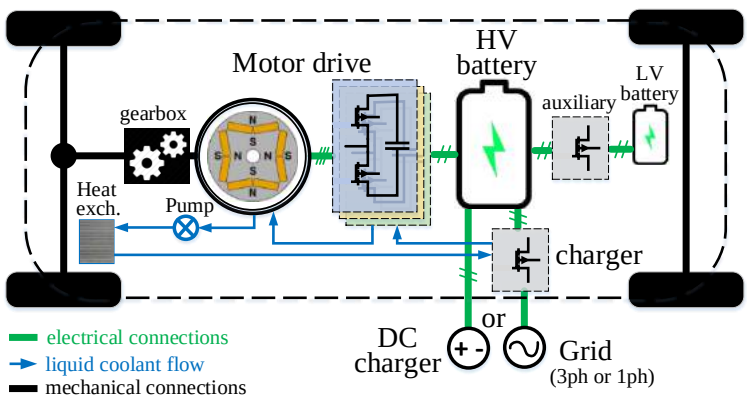


Fig. 1.1: Schematic diagram of the powertrain in a battery electric vehicle and its basic cooling system

Variations of that system exist depending on the type of the coolant [8], which can be oil, water with ethylene glucole or a combination of these two. The main cooling loop studied in this thesis is shown in Fig. 1.1, where the power converters and the electric motor are connected in series with the pump and the heat exchanger. A secondary cooling loop can also cool down the battery pack, as suggested in [9].

Electric Motor Selection

The design of the electric motor is one of the main fields of study related with electromobility. The final selection of the machine type is determined by the specifications of the vehicle and the application where it is going to be used. Electrical machines with permanent magnets are the dominant machine types in electric vehicles and a list of common design solutions have been reported in [10]. The interior permanent magnet synchronous machine (IPMSM) is widely used when high torque density and better efficiency at low and medium speeds are required [11].

Alternative machines without permanent magnets have also been used in electric vehicles [12]. The induction machine (IM) is a common machine type, which has typically lower torque density and lower efficiency than the PMSM, especially at high-torque low-speed operation [13]. The switched reluctance machine (SRM) is also an alternative machine type, which is mostly suitable for high-speed operation [11]. Permanent-magnet-free synchronous machines have recently seen research interest for automotive applications, such as the electrically excited synchronous machine (EESM) [14, 15], which has been studied in comparison with the IPMSM during this PhD project. Many other design aspects of electric motors for traction applications are currently under research, but are not further investigated here. For example, there are studies related with the winding distribution type for IPMSM, such as in [16, 17] where distributed windings are compared with fractional-slot windings. The optimal stator winding types for automotive machines have also been investigated in [18], where hairpin and random windings have been compared.

Therefore, it is not easy to draw a conclusion about the optimal machine design for an electric vehicle, since many aspects need to be taken into consideration. The speed range of the motor can also be selected in correlation with the transmission system design [19, 20], which can be of single-gear or have multiple gears.

Powertrains with multiple motors have been suggested for heavy-duty vehicles, such as dual-motor designs for buses [21] and large trucks [22] and can also be found in passenger vehicles, such as in Tesla BEVs [23]. In-wheel direct-driven

motor drives have also been suggested for passenger BEVs with two-wheel drives [24] or even four-wheel drives [25], where each drive has its individual motor and inverter. Special design requirements exist for the motors of these vehicles.

Inverter Design Considerations

The main inverter of the vehicle that drives the motor is another key component of the powertrain. It is responsible for converting the dc voltage of the battery into ac voltage with the correct frequency and amplitude for the motor. The three-phase voltage source converter (VSC) is the standard inverter type used in the automotive industry [26] and, therefore, it is selected for this study. The main design requirements of the inverter is to have high power density and efficiency, while the cost of the system is kept as low as possible and the vehicle specifications in terms of maximum power, current and voltage are satisfied. Several design aspects can be investigated to optimize the design based on these requirements. The type of semiconductors used for the power switches and their rated voltage, as well as the inverter topology are some of these research aspects.

Based on current industry trends, the majority of the motor drive ratings range between 30 kW and 200 kW [1], while the majority of traction inverters in the future will be in the 100-500 kW range judging from the ongoing research and industry practices [27]. Newly released passenger BEVs with similar price such as Volvo XC40 Recharge [28], Tesla Model 3 [23], Polestar 2 [29] and the expected for 2021 BMW i4 concept car [30] have total power of their powertrain between 300 and 390 kW.

The rated operating voltage of the drive depends on the high-voltage battery, which is currently rated to 400 V in the majority of the cases. However, the need for fast-charging capabilities of the newer BEV models may also be accompanied with a higher-voltage battery at 800 V increasing at the same time the rated voltage of the motor drive [27, 31, 32]. The use of higher dc voltage will also reduce of the current of the drive and, also, the copper losses of the motor.

Because of this trend towards higher voltage in automotive drives, multilevel inverters and specifically 3-level NPC converters have been considered as an alternative to the 2-level converter (2LC). As will be discussed later in this chapter, these inverters have much lower Total Harmonic Distortion (THD) than the 2-level topology for the same switching frequency [33], which will also have an impact on the stator losses of the motor, and are capable of handling even higher voltages than 800 V. However, since the current trend in the automotive industry is to have

maximum 800 V system, the high-voltage capabilities of the multilevel converters cannot be utilized. These inverters suffer also from higher cost and complexity due to their larger number of components [27]. In case higher-voltage voltage automotive drives are considered in the future, multilevel inverters could be an attractive candidate.

Wide-Bandgap Technology in Electromobility

Wide-bandgap (WBG) semiconductors have recently evolved into an attractive solution for power converters of electric vehicles due to the following distinctive advantages compared to silicon (Si) counterparts. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the two most industrialized WBG semiconductors. As evident from the name of these materials, they have a larger bandgap compared to Si. Higher bandgap means that semiconductor dies can withstand larger voltage compared with Si dies of the same thickness. On the other hand, if the voltage rating is kept the same, the semiconductor die can have smaller thickness, higher doping is possible and the resultant on-resistance can be much lower. WBG devices can also have faster switching transients and the switching losses can be extremely low, even at high voltage, that allows the development of faster-switching converters with lower THD. Higher operating temperatures are also possible for WBG semiconductors, even higher than 250°C, and the main limitation is basically the temperature constraints of the packaging.

As a matter of fact, SiC has more than 10 times higher breakdown field compared to Si [34], which leads to 10 times thinner SiC devices of same voltage rating with the Si device. The loss reduction is even larger and when combined with the higher operating temperature, the power density of the final converter can be substantially enhanced.

SiC MOSFETs are competing mainly with Si IGBTs in applications where the commonly found 1200 V switches are used [34]. Therefore, they are a suitable candidate for the main inverter of a BEV with rated dc voltage of 800 V. Automotive inverters with Si IGBTs are still capable of operating with 800 V dc-link, but they have significantly higher switching losses [27].

On the other hand, GaN transistors have even lower switching losses than SiC devices but most products at the moment are rated for voltages up to 600 V, which makes them counterparts of Si MOSFETs. Thus, GaN transistors are more suitable for dc/dc converters and other lower-voltage-rated devices, where high switching frequency is preferable [6, 34].

The main disadvantage of SiC power switches is their higher cost compared to IGBTs, but this cost difference tends to reduce as SiC technology becomes more widely used. The faster switching transients of WBG devices have as an additional side-effect much higher dv/dt on their ac PWM voltage. This can impose an additional stress on the insulation of the stator windings of the electrical machine, in case the machine is driven by a SiC inverter [35]. Similar issue is observed at the dc-link capacitors that need to filter current and voltage ripple with higher transients.

Considerable research work has been conducted on the design of SiC inverters suitable for motor drives, such as in [36]. However, there has not been any comprehensive study about the design process of automotive SiC inverters with high power density, where specific guidelines regarding the design of the whole drive system are given. The design specifications of the vehicle should also be considered and correct sizing of the inverter and its cooling circuit needs to be properly implemented. Lastly, experimental testing of the drive in laboratory conditions is necessary to validate the design.

1.1.2 Kite-based Tidal Power Generation System

Offshore power plants producing energy from the sea tides have attracted significant research interest in the recent years, since this can be a renewable energy source with large potential [37–40] and an alternative to the wind and solar energy sources. Specifically, the United Kingdom and France cover almost 90% of the European tidal resource with 48 GW of power, as reported in [37, 38]. Tidal energy has considerable advantages compared to the other renewable energy sources, such as the fully predictable nature of the tidal movements and its robustness against climatic changes, such as the wind, rain, snow, clouds and fog [41].

Up to now, tidal power has been largely unexploited, although attempts to harvest electric energy from sea tides date back to 1966, when the oldest tidal power plant was installed in France [42]. Most of the traditional tidal power plants required the construction of large dams and static undersea constructions, which had a large investment cost as well as a high environmental impact for the local communities. These are some of the reasons that have hindered until now further development of tidal power projects in large scale.

An emerging hydrokinetic energy technology named "Tethered UnderSea Kite" (TUSK) has been proposed as a new more efficient way to produce electrical energy from the sea tides, using axial-flow water turbines mounted on a kite which can

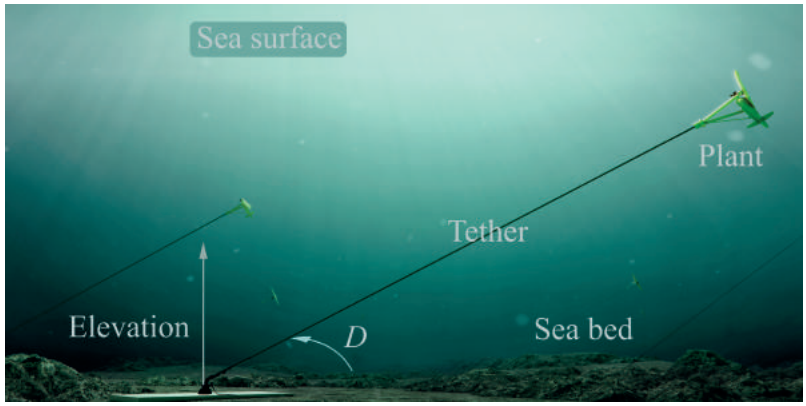


Fig. 1.2: TUSK plant schematic into the sea showing the tether connecting the kite to the sea bed [Property of Minesto AB]

move freely inside the sea following the motions of the sea currents [43]. This type of technology can increase the power production of a specific tidal turbine, when compared to a traditional static tidal turbines of the same size. Therefore, the potential resources of tidal power can be increased by using the TUSK-based systems. Also, the environmental impact of the plant's installation is limited. A recent application of the TUSK system is the Deep Green [44, 45] concept which has been developed by Minesto AB and is under development in various projects, such as the PowerKite project [46]. The undersea kites can be installed either standalone, as shown in Fig. 1.2, or they can build arrays.

The concept of using a moving kite for producing power has initially been proposed for airborne systems that would increase the power density of existing wind power turbines, as cited in [47–53]. As described there, the turbine is mounted on the kite, which is attached to the ground through a tether. While the kite is travelling on the air (in the case of airborne kites) or in the sea (for the undersea kites) following a predefined trajectory, the relative speed of the air or water flowing through the turbine becomes 5 to 8 times higher compared to a traditional static turbine. The kite is moving fast following a trajectory that resembles to the "∞" symbol. Since the power generated from the turbine is proportional to the third-power of the relative wind/water speed, the electric power produced by the generator is highly increased. Thus, the power density of the whole power generation system is also increased.

The increase of the generated power density is a distinctive advantage for TUSK systems compared to fixed marine turbine technologies [43] and this is one of the

characteristics that would make tidal power competitive against other renewable energy sources. Additionally, the increased relative speed of the fluid flowing through the plant's turbine, allows TUSK-based tidal plants to operate at places with medium or low tidal streams, which may not be cost-effective using the traditional fixed tidal turbines that require high-speed tidal streams [44].

Optimal Control of Tidal Power Generator

The TUSK-based plants, however, have some special requirements for the design and control of the power generation subsystem, which are going to be further analyzed in this thesis. Firstly, the speed of the water flowing through the kite's turbine experiences fluctuations, which depend on the trajectory of the TUSK in the sea. These speed fluctuations are periodic and cause variations in the output electrical torque of the plant's generator and of the produced power at the grid side of the system [54]. The speed and power variations can be estimated using analytical calculations, if the trajectory of the kite is known. A proper design of the controllers for the power conversion system should be made in order to ensure stability under this highly dynamic operation. Verifying the effectiveness of the power converters' control in laboratory conditions is necessary and, therefore, a laboratory emulator of the kite's power generation system is needed which will represent the dynamics of the kite's tidal turbine. Laboratory emulators of wind power systems have been presented in [55–59], where the wind turbine has been emulated by a motor and the control of the real wind power generator has been tested. A similar experimental set-up can be used in this thesis to emulate the operation of the TUSK-based tidal generator.

The Maximum Power Point Tracking (MPPT) algorithm of the kite's tidal generator is another topic that has not been extensively investigated. Since the operating conditions are similar to wind power plants, similar MPPT control strategies can be applied for tidal power systems, as the ones investigated in [60–64]. However, due to the highly dynamic operation of the kite and the constantly variating flow speed of the water through its turbine, these methods should be studied and their effectiveness should be experimentally evaluated. The turbine inertia is also a factor that can influence the effectiveness of the MPPT control of the kite's generator. The inertia of the system creates an error between the actual rotational speed of the generator and the reference speed, which is calculated by the MPPT control. Therefore, improvements should be proposed to properly adjust the generator speed control for the specific needs of the examined application.

Medium Voltage Multilevel Machine Drives

An additional constraint of the TUSK systems is the limited available space inside the nacelle of the kite for the generator and the power converters which makes the design of the power conversion system a challenging task. Therefore, power equipment of high power density is a requirement for this application, similarly with the automotive drive described before. Also, the tether of the kite provides both mechanical coupling of the system with the sea bed and electrical connection to the grid. The weight and the diameter of the electrical cables inside the tether should be kept as low as possible in order to reduce the drag that the tether creates, when the kite is moving inside the sea. This makes the efficient transportation of the produced active power from the kite to the grid challenging, since the power of the system is high.

Increasing the operating voltage of the kite's power generation system from commonly used low voltage to the medium-voltage range can increase the efficiency of the power transportation through the subsea cables, since this results to reduced current and ohmic losses. Alternatively, the diameter of the subsea cables and the tether of the kite can be reduced, due to the lower current requirements. Medium voltage is defined by IEEE Std 1623-2004 [65] as the ac rms voltage between 1-35 kV. The 2LC can still be used in medium voltage applications by having high-voltage semiconductors or multiple series-connected low-voltage power switches in each switch position. However, problems with the voltage balancing of these switches during the switching transient are the main disadvantages of this solution [66, 67]. Therefore, the use of multilevel VSCs is a preferable solution for this case.

The main advantage of multilevel converters is the capability to use power semiconductors of low voltage ratings, which have lower cost and good commercial availability [68, 69]. Another important advantage is the reduction of the harmonic distortion at the point of common coupling (PCC) of the kite, which eliminates the need for large passive filters at the grid-side of the system [68] that contribute a lot to the total weight and size of the drive mounted inside the kite. An improvement of the converter's efficiency has also been reported in [70], when using multilevel converters compared to 2LC of the same operating voltage and power. Multilevel converters can also reduce the voltage derivative $\mathrm{d}v/\mathrm{d}t$, which is caused by the switching transients of the converters, as stated in [71]. This decreases significantly the produced EMI that could normally cause lots of operating problems on the low-voltage electronics of the system.

The available multilevel topologies need to be compared with each other in order to select the most suitable converter for the power conversion system of the undersea kite. A comparative study based on literature review for multilevel converters suitable for drive applications is conducted in Section 4.2 of the thesis and the 5-level Neutral Point Clamped (NPC) converter is finally chosen. The 5-level NPC converter can increase the operating voltage of the drive system up to 4 kV (peak), in case power switches with voltage rating of 1.2 kV are used. The 5-level converter has four series-connected capacitor banks at the dc side and a well known problem of this topology is the imbalance of the individual capacitor voltages. This imbalance would create overvoltage in some of the power switches of the converter and low frequency harmonics at the ac side of the system. Special control and/or hardware is required to balance the capacitor voltages, which may increase the complexity and cost of the system. Thus, several methods have been proposed to alleviate this drawback and they can be divided into two types, the software and the hardware based techniques.

The software-based balancing method is based on the modification of the standard space vector modulator of the NPC converter, as suggested in [72–80]. However, most of the solutions proposed in these studies require some limitations in the operation of the drive, such as the difficulty to operate under unity power factor, which is usually the preferred operation mode for the grid-side converter of the drive. Some studies propose also the operation of the 5-level converter in a quasi-2-level [81] and quasi-3-level mode [82] only in order to avoid specific switching combinations that create unbalances of the dc-link voltages. However, this method may increase the harmonics at the ac side of the NPC converters and the need for grid filters, which makes it less suitable for several generator drives, such as the one designed for the TUSK where the available space for the drive is limited.

Another option for balancing the capacitor voltages of the dc-link is by employing dc/dc converters that can actively distribute the voltage across the four series-connected capacitors, as proposed in [83–88]. This technique has several advantages; however, the cost and the losses of the extra power devices for the dc/dc converters are serious drawbacks. From the above it is concluded that further investigation should be conducted to develop a new technique for the capacitor voltage balancing in a drive with 5-level NPC converters without the previously mentioned disadvantages.

Wide-Bandgap Technology in Offshore Power Generation

WBG semiconductors and specifically SiC MOSFETs have been proposed for power converters of future offshore power plants [89], since high-voltage capable SiC power modules could help to increase the voltage rating of the power conversion system. High-voltage SiC devices in 2LC topologies are also studied in [90] for active power filters in offshore applications. However, as stated in [91], currently available SiC power modules do not have large enough power capabilities to fulfil all the requirements of large offshore power plants. Therefore, multilevel converters are still the only solution to build systems with high voltage and high power. Further development of the SiC technology in the future, with the commercialization of high-voltage and high-power modules, might mean that converters for offshore applications could be built using standard 2-level structure.

On the other hand, a power generation system that combines NPC-based machine drive with the use of SiC power switches could benefit from the advantages of both the multilevel converters (lower THD and utilization of low-cost low-voltage-rated switches) and the WBG devices (low inverter losses). A reduction of the inverter losses is highly beneficial for the TUSK-based tidal plant, since this would allow the construction of more compact converters with less cooling requirements. This concept will be investigated in this thesis.

1.2 Aims of the Thesis

The aim of this thesis is to investigate different design approaches for electrical machine drives with SiC power inverters, which are suitable for applications where high power density and efficiency are required.

Firstly, a medium voltage PMSM drive with 5-level NPC converters is designed, which is intended to be used in kite-based tidal power generation systems. One purpose of the thesis is to present suitable control for the converters, considering the highly dynamic operation of the kite due to the periodic variations in the active power and rotor speed. Another target of this work is to develop voltage balancing techniques for the dc-link capacitors of the NPC converters, so that their individual voltage can be effectively controlled.

The second aim of the thesis is to develop a comprehensive design approach for 800 V SiC automotive inverters. High power density in this case is also required, which is achieved through an advanced design of the inverter's mechanical structure, such as the dc bus and the cooling system.

A final goal of the project is to verify the research outcomes through simulations of each system, as well as through experimental tests on laboratory prototypes.

1.3 Contributions

The key scientific contributions of the thesis can be identified as follows:

- MPPT generator control for TUSK power plants:
  A properly designed MPPT controller for the generator of a TUSK tidal power plant has been implemented that can follow effectively the power and speed variations. The developed controller has been tested experimentally on a 35 kVA laboratory set-up where the operation of the turbine is emulated by an induction motor (IM).
- DC-link voltage balancing algorithms for 5-level NPC converter drive:
  New voltage control techniques have been proposed that can balance the capacitor voltages on the dc-link of a generator drive with 5-level NPC converters. An optimized selection of the redundant states on the SVM-plane has been utilized as the basic tool to regulate the capacitor voltages. This is combined with hardware-based balancing using extra dc/dc converters in order to ensure effective voltage control under every operating condition of the drive, without any limitation in the operation of the converters. The developed control requires less components and can reduce the losses compared to conventional techniques that utilize only hardware-based balancing.
- Medium voltage PCB design for NPC inverter with SiC switches:
  A generator drive with two back-to-back (B2B) connected 5-level NPC converters has been developed, which can be used at the power conversion of a TUSK plant. A laboratory prototype of the generator drive with maximum designed dc voltage up to 4 kV has been firstly simulated and then designed and built during this project. The system is tested experimentally with dc-link voltage up to 670 V.

  The power converter PCBs, measurement devices and control platforms of the prototype system have been specially designed for low EMI and ringing on the power switches. Also, SiC MOSFETs and diodes have been used in the NPC converters, which allows further reduction of the losses in the system. Suitable gate driver boards for the SiC MOSFETs have been designed that achieve high voltage insulation and low EMI on the control signals.
- Development of high power 49 kW/liter SiC automotive inverter:

The design procedure of a 450 A SiC automotive inverter has been studied and a new iterative design approach for the liquid cooling components of the inverter has been developed. Transient CFD computations are utilized in combination with simulations of legislative testing procedures for electric vehicles, such as acceleration tests and driving cycle analysis, in order to fine-tune the inverter based on the needs of the specific vehicle. A special design of the dc-link capacitor bank has also been developed in order to further reduce the volume of the system.

- Zero-sequence control strategy for 2LC-based P-HIL systems:
  A machine emulation testing platform for PMSM drives with reduced component count has been proposed. The electrical machine has been emulated by an additional VSC, which is connected to the ac side of the main inverter of the drive and shares the same dc-link. A new control scheme of the common mode voltage of the resultant loop has been developed, so that the zero-sequence current which normally flows in this circuit can be suppressed without the use of hardware filters. Instead, the redundant states of the SVM have been utilized to regulate this current.

  A P-HIL testing platform has been built with the previously mentioned 450 A SiC inverter in order to experimentally verify the functionality of the control.

1.4 Thesis Outline

The thesis is organized into eight chapters:

- Chapter 1 is the introduction of the thesis and describes the motivation, the aim and the main contributions of this study. The background applications of this PhD project, tidal power generation and electrified transportation, are also described.
- Chapter 2 provides an overview of the vector control strategies used in the remaining part of the thesis. The vector control structure for grid-connected inverters and field-oriented-control for synchronous machines are also analyzed.
- In Chapter 3 an overview of the first background application of this project, the TUSK tidal generator, is presented. The tidal power generation system has been modelled with analytical equations, which are described in detail. The control system for both converters of the grid-connected drive is also

designed and experimental results from a low-scaled tidal power emulator are shown.

- Chapter 4 starts with an analysis of the most well-known multilevel converter topologies for drive applications. Modulation strategies for N-level multilevel converters are presented. Capacitor voltage balancing strategies for machine drives with 5-level NPC converters are presented utilizing the Space Vector Modulation.
- Experimental verification of some of these voltage balancing control techniques is presented in Chapter 5, where the design process of a medium voltage prototype multilevel drive is analyzed.
- Machine emulators for testing electric drives are studied in Chapter 6. Space Vector Modulation is utilized to control the common mode voltage of the topology and eliminate the circulating zero-sequence current. Experimental results on a power hardware-in-the-loop set-up emulating a 60 kW PMSM are presented.
- Chapter 7 presents the second background application of this project, the design of high-power inverters with high power density for electric vehicles using SiC power switches. The complete design approach of the inverter is presented, including electrical and thermal modelling by utilizing FEM and CFD simulation tools. The machine drive of a test-case vehicle has also been modelled in order to fine-tune the inverter design to meet the requirements of the specific application.
- Finally, the conclusions of the thesis and suggestions for future work are reported in Chapter 8.

1.5 List of Publications

The peer-reviewed publications originating from this thesis are:

I. **G. Mademlis**, Y. Liu, and N. Saadat, "Combined voltage balancing techniques of the DC link in five-level medium voltage NPC back-to-back converters for offshore renewable generation," in *Proc. 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1-P.10, doi: 10.23919/EPE17ECCEEurope.2017.8099317.

II. **G. Mademlis**, Y. Liu, and J. Zhao, "Comparative Study of the Torque Ripple and Iron Losses of a Permanent Magnet Synchronous Generator

Driven by Multilevel Converters," in *Proc. 23rd International Conference on Electrical Machines (ICEM)*, September 3-6, 2018, pp. 1406-1412, doi: 10.1109/ICELMACH.2018.8506775.

III. **G. Mademlis**, Y. Liu, P. Chen, and E. Singhroy, "Generator Speed Control and Experimental Verification of Tidal Undersea Kite Systems," in *Proc. 23rd International Conference on Electrical Machines (ICEM)*, September 3-6, 2018, pp. 1531-1537, doi: 10.1109/ECCE.2018.8558080.

IV. **G. Mademlis** and Y. Liu, "DC Link Voltage Balancing Technique Utilizing Space Vector Control in SiC-based Five-Level Back-to-Back-Connected NPC Converters," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018, pp. 3032-3037, doi: 10.1109/ECCE.2018.8558080.

V. **G. Mademlis** and Y. Liu, "Feed-forward Control of Active Voltage Balancing Converter in Electric Drive with Five-Level NPC Converters," in *Proc. of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018, pp. 7258-7264, doi: 10.1109/ECCE.2018.8557365.

VI. C. Larsson, A. Rydgård, **G. Mademlis**, Y. Liu, and M. Fredriksson, "Overvoltage Mitigation of Medium Voltage Electric Drives with Long Cables using Multilevel-Converters and Passive Filters," in *Proc. of the 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019, P.1-P.10, doi: 10.23919/EPE.2019.8915441.

VII. **G. Mademlis**, Y. Liu, P. Chen, and E. Singhroy, "Design of Maximum Power Point Tracking for Dynamic Power Response of Tidal Undersea Kite Systems," in *IEEE Trans. Industry Applications*, vol. 56, no. 2, pp. 2048-2060, March-April 2020, doi: 10.1109/TIA.2020.2966189.

VIII. N. Sharma, Y. Liu, **G. Mademlis**, and X. Huang, "Design of a Power Hardware-in-the-Loop Test Bench for a Traction Permanent Magnet Synchronous Machine Drive," in *Proc. 24th International Conference on Electrical Machines (ICEM)*, August 23-26, 2020, pp. 1765-1771, doi: 10.1109/ICEM49940.2020.9270838.

IX. **G. Mademlis**, Y. Liu, J. Tang, L. Boscaglia, and N. Sharma, "Performance Evaluation of Electrically Excited Synchronous Machine compared to PMSM for High-Power Traction Drives," in *Proc. 24th International Conference on Electrical Machines (ICEM)*, August 23-26, 2020, pp. 1793-1799, doi: 10.1109/ICEM49940.2020.9270852.

X. **G. Mademlis**, R. Orbay, Y. Liu, and N. Sharma, "Designing Thermally Uniform Heatsink with Rectangular Pins for High-Power Automotive SiC Inverters," in *Proc. IECON 2020 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1317-1322, doi: 10.1109/IECON43393.2020.9254692.

XI. **G. Mademlis**, Y. Liu, N. Sharma, and X. Huang, "Circulating Current Reduction in Common DC-Link Power-HIL for Drives using SVM with Zero-Sequence Compensation," in *Proc. IECON 2020 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 4673-4678, doi: 10.1109/IECON43393.2020.9254744.

XII. L. Boscaglia, N. Sharma, Y. Liu, and **G. Mademlis**, "Balancing Peak-torque and Drive-cycle Efficiency with Magnet Dimensioning of Permanent Magnet Synchronous Machines," in *Proc. IECON 2020 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 883-888, doi: 10.1109/IECON43393.2020.9255349.

XIII. **G. Mademlis**, R. Orbay, Y. Liu, N. Sharma, R. Arvidsson, and T. Thiringer, "Multidisciplinary Cooling Design Tool for Electric Vehicle SiC Inverters Utilizing Transient 3D-CFD Computations," in *eTransportation journal, Elsevier*, vol. 7, pp. 100092, November 2020, doi:10.1016/j.etran.2020.100092.

XIV. **G. Mademlis**, N. Sharma, Y. Liu, and J. Tang, "Zero-Sequence Current Reduction Technique for Electrical Machine Emulators with DC-Coupling by Regulating the SVM Zero States," under review since Feb. 2021 in *IEEE Trans. Industrial Electronics.*

XV. J. Tang, D. Pehrman, **G. Mademlis** and Y. Liu, "Common Mode Power Control of Three-Phase Inverter for Auxiliary Load without Access to Neutral Point," under review since Feb. 2021 in *IEEE Trans. Power Electronics.*

Chapter 2

Synchronous Machine Drives: Topologies and Control

Electric drives with synchronous machines are studied in this thesis and vector control is used for the three-phase voltage source converters (VSC). The definition and the basic structure of the drive system are presented in this chapter, when it is connected to the grid and when it is connected to a dc source. Vector control theory for the converters in both cases is presented.

2.1 Structure of Electrical Machine Drives

An *electrical machine* is a device that converts mechanical to electrical energy. Depending on the direction of energy flow, the electrical machine can operate as a generator (producing electrical energy) or as a motor (producing mechanical energy). A three-phase ac machine needs an ac voltage source connected to the three terminals of its stator windings. Since this ac voltage source does not always have the correct voltage amplitude and frequency, a *power converter* is required to provide that. The power converter is composed of switching devices and acts as an intermediate step between the machine and the electrical source. It is responsible for processing and controlling the flow of electrical energy by supplying the machine with the correct voltage. Bidirectional power flow is necessary for the converter, since the electrical machine can operate both as a motor and as a generator.

An *electric drive system* comprises of an electrical machine and a power converter, as the schematic layout shown in Fig. 2.1(a). The right side of the power conversion

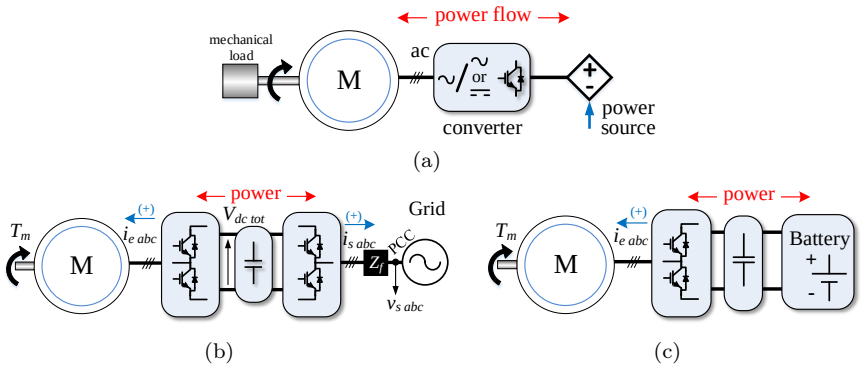


Fig. 2.1: Simple schematic diagram of (a) an electrical machine connected to a power converter, (b) a grid-connected machine drive with two back-to-back connected converters (typical for power generation systems) and (c) machine drive supplied by a dc battery source (typical for electric vehicles)

system is connected to a power source, which can have either dc or ac voltage, depending on the application.

In case the drive system is connected to the grid, the power conversion system is composed of two dc/ac converters, which are connected back-to-back. The first converter at the grid-side rectifies the ac voltage of the grid to an intermediate dc-link and the second converter is responsible for controlling the electrical machine. When only single-direction of power is needed, which flows from the grid towards the machine operating only as a motor, a passive diode rectifier is enough as the grid-side converter. However, when bidirectional power flow is required, such as in power generation systems, an active-front-end inverter is used at the grid-side in order to synchronize it to the grid and control the power exchange [see Fig. 2.1(b)].

In applications where a dc power source is connected directly to the dc-side of the machine converter as in Fig. 2.1(c), only the left-side converter of Fig. 2.1(b) is utilized. A representative example is the drive systems of electric vehicles, where the machine drive is supplied by a battery. The battery model has not been studied in this project and it is considered as an ideal dc voltage source.

The energy flow marked with blue arrow in Figs. 2.1(b)-(c), with direction exiting the converters at their ac-side, is considered positive for the following analysis.

2.2 Field Oriented Control

The Field Oriented Control (FOC) method for synchronous machines consists of two cascaded control loops, with the outer loop being the speed control of the machine and the inner loop the current control. In order to implement the following control strategy, measurements of the machine stator current i_e, rotor angle θ_r and dc-link voltage $V_{dc\ tot}$ are needed.

2.2.1 Speed Controller Design

A schematic of the machine speed controller is shown in Fig. 2.2. It consists of a proportional-integral (PI) control loop and an active damping term $B_{a\omega}$. The gains of the PI loop are chosen based on the Loop Shaping Method [92] in order to have smooth response of the controller, similar to a first-order system. They are defined as

$$K_{P\omega} = a_\omega\ J \tag{2.1}$$

$$K_{I\omega} = a_\omega\ (b + B_{a\omega}) \tag{2.2}$$

where a_ω is the closed-loop bandwidth of the speed controller, J is the inertia and b is the friction constant of the machine drivetrain. The active damping term $B_{a\omega}$ is selected as

$$B_{a\omega} = a_\omega\ J - b \tag{2.3}$$

in order to increase the robustness of the controller against estimation errors of the system parameters.

The output of the speed controller is the reference electromagnetic torque for the machine T_e^* which is limited up to its rated value by a saturation block. Anti-reset windup is also implemented, which is not shown in the block diagram of Fig. 2.2. The speed response of the machine is described by its mechanical model, when

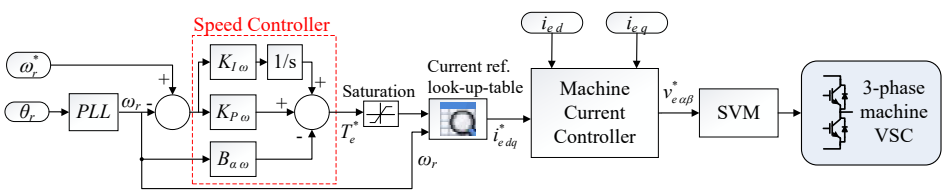


Fig. 2.2: Block diagram of speed control loop

the electromagnetic torque T_e and load torque T_L are applied.

$$J\ \frac{\mathrm{d}\omega_r}{\mathrm{d}t} + b\ \omega_r + T_0 = T_e - T_L \xrightarrow[T_0=0]{T_e^* \approx T_e} T_e^* = J\ \frac{\mathrm{d}\omega_r}{\mathrm{d}t} + b\ \omega_r + T_L \tag{2.4}$$

where T_0 is the static friction constant measured in Nm and can help to increase the fidelity of the machine mechanical model.

The rotational speed of the machine ω_r can be calculated through derivation of the rotor angle $\omega_r = \mathrm{d}\theta_r/\mathrm{d}t$. However, a speed estimator based on the phase-locked-loop (PLL) principle, as described in [93], can offer more stable calculation of the machine speed and is preferred in this study.

2.2.2 Current Reference Generation

The electromagnetic torque T_e produced by a synchronous machine can be calculated as

$$T_e = \frac{3}{2}\ p(\psi_d\ i_{eq} - \psi_q\ i_{ed}) \tag{2.5}$$

where p is the number of pole-pairs. If the inductances of the machine are considered constant, the torque equation becomes

$$T_e = \frac{3}{2}\ P[\psi_{md}\ i_{eq} + (L_d - L_q)\ i_{ed}\ i_{eq}] \tag{2.6}$$

The first term of the above equation depends on the q-current and the magnetizing flux linkage from the rotor ψ_{md} and can be named *synchronous torque*. The second term of (2.6) depends on the difference between the d- and q-axis inductances and is named *reluctance torque*.

Non-salient synchronous machines, such as the surface-mounted PMSM, have equal d- and q-axis inductances $L_d = L_q$ and, therefore, they have only synchronous torque. For salient permanent magnet machines, such as for the IPMSM, the inductances are $L_d < L_q$ and the total machine torque is the sum of reluctance and synchronous torque.

Many methods exist for selecting the optimal combination of dq-axis stator currents in order to create the requested torque of the machine. The current and voltage operating limits of the system need also to be considered, when defining the current reference [94]. In case the synchronous machine has controllable excitation with rotor field current i_f, there is an additional degree of freedom for controlling the machine [14]. Optimal selection of these variables allows the minimization of the machine losses.

A simple way to calculate the required reference current is by setting $i_{ed}^{*} = 0$ A and controlling the machine just with the synchronous torque. This gives the optimal current reference of non-salient machines, since the term T_e/i_e is maximized and the drive operates at MTPA with minimum stator copper losses.

However, a non-zero d-current needs to be applied for salient machines, in order to utilize also the reluctance torque [95, 96]. MTPA operation can then be implemented in salient machines. The current reference generation methods can be classified into three general categories:

1. The current reference is generated using analytical equations for minimizing the machine losses, as in [97]. These equations are based on the machine parameters and the current reference is calculated online, while the drive operates.
2. A search algorithm calculates offline the optimal dq-current combination for a finite number of torque-speed points on the machine operating map utilizing a detailed machine model. FEM computation results of the machine losses, inductances or flux linkages and inverter losses are used. The calculated current is stored in a look-up-table which is loaded on the control board of the inverter. Then, the correct reference is obtained by the MCU with interpolation in this look-up-table, where the inputs are the machine reference torque and speed. The temperature can also be considered as an input parameter of the table, as shown in [98].
3. MTPA point tracking is implemented by injecting an additional high-frequency signal, as presented in [96, 99, 100].

The first two methods have been used for the electrical machine control of this thesis. Analytical current reference generation is applied in the medium voltage PMSM drive of Chapter 5, while look-up-tables of the optimal current reference are used in Chapters 6-7.

2.2.3 Machine Current Controller Design

The terminal voltage of the synchronous machine can be expressed as follows

$$v_{ed} = R_s i_{ed} + L_d \frac{\mathrm{d}i_{ed}}{\mathrm{d}t} - \omega_e \psi_q \Rightarrow v_{ed} = R_s i_{ed} + L_d \frac{\mathrm{d}i_{ed}}{\mathrm{d}t} - \omega_e L_q i_{eq} \tag{2.7}$$

$$v_{eq} = R_s i_{eq} + L_q \frac{\mathrm{d}i_{eq}}{\mathrm{d}t} + \omega_e \psi_d \Rightarrow v_{eq} = R_s i_{eq} + L_q \frac{\mathrm{d}i_{eq}}{\mathrm{d}t} + \omega_e L_d i_{ed} + E_f \tag{2.8}$$

where L_d and L_q are the no-load d- and q-axis stator inductances, R_s the per-phase stator resistance, ω_e the electrical frequency in rad/s and E_f the back-EMF

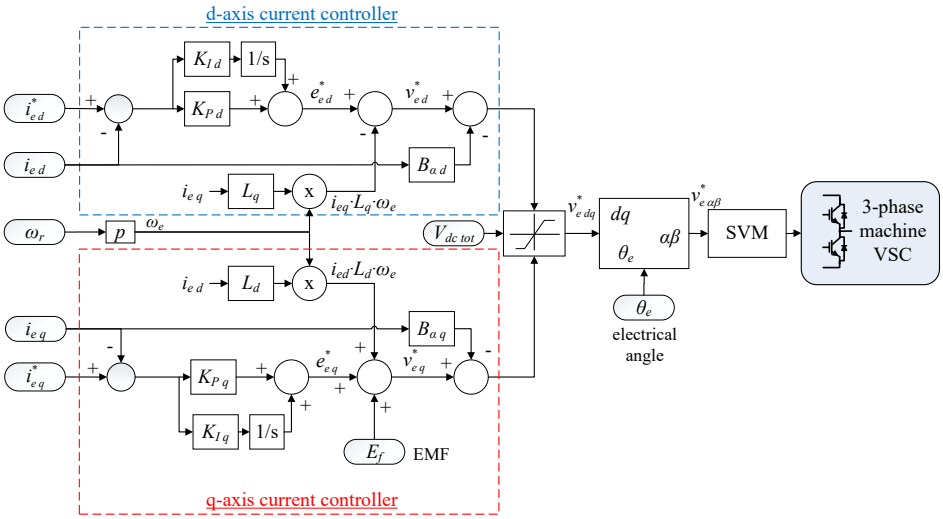


Fig. 2.3: Block diagram of electrical machine current controller in dq-frame

voltage.

The current control is the inner control loop of the machine-side converter and calculates the reference voltage for the machine based on the above equations (2.7)-(2.8). The block diagram of the controller is shown in Fig. 2.3. The current controller split between the d- and q-axis control blocks. Inputs are the current references i^*_{edq} and actual current values i_{edq} in both d- and q-axis. The gains and the active damping term of the d-axis PI controller are selected based on the Loop Shaping Method as follows

$$K_{Pd} = L_d\ a_c \tag{2.9}$$

$$K_{Id} = a_c\ (R_s + B_{ad}) \tag{2.10}$$

$$B_{ad} = L_d\ a_c - R_s \tag{2.11}$$

where a_c the bandwidth of the controller. Similar equations define the parameters of the q-axis PI controller replacing in (2.9)-(2.11) the L_d inductance with L_q. Common practice is to select the bandwidth of the current controller at least an order of magnitude lower than the switching frequency, i.e. $a_c = 2\pi\frac{f_{sw}}{10}$, in order to have a stable system during dynamic and steady-state operation.

A feed-forward of the calculated machine voltage is added to the output of the

PI-regulators e^*_{ed} and e^*_{eq} according to the following formulas

$$v^*_{ed} = e^*_{ed} - L_q \; i_{eq} \; \omega_e \tag{2.12}$$

$$v^*_{eq} = e^*_{eq} + L_d \; i_{ed} \; \omega_e + E_f \tag{2.13}$$

In case the synchronous machine has permanent magnets, the back EMF is calculated by

$$E_{f\ PM} = \psi_{md} \; \omega_e \tag{2.14}$$

where ψ_{md} is the magnet flux linkage. In case we have a synchronous machine with rotor windings

$$E_f = L_{md} \; i_f \; \omega_e \tag{2.15}$$

where L_{md} is the d-axis magnetizing inductance and i_f the rotor field current.

The reference voltage $v^*_{e\ dq}$, which is the output of the current control loop, is limited by a saturation block in order to avoid overmodulation. This limits the voltage amplitude, but does not modify the voltage angle. Anti-reset windup is also implemented, which is not shown in the block diagram of Fig. 2.3.

Space vector modulation is finally used for generating the gate signals of the power switches in the converter.

2.3 Vector Control for Grid-Side Converter

Vector control in the dq-frame is used for the grid-side converter. Two cascaded control loops exist, with the outer loop regulating the voltage of the dc-link capacitor bank and the inner loop regulating the d- and q-axis currents. The converter is synchronized with the grid through a PLL block.

A three-phase passive filter consisting of an inductor L_f with its series resistance R_f is considered to be installed between the ac output of the converter and the PCC.

2.3.1 Real-/Reactive-Power Control Design

The exchange of power with the PCC of the grid can be described as follows

$$P_{grid} = \frac{3}{2}[v_{sd} \; i_{sd} + v_{sq} \; i_{sq}] \tag{2.16}$$

$$Q_{grid} = \frac{3}{2}[-v_{sd} \; i_{sq} + v_{sq} \; i_{sd}] \tag{2.17}$$

where v_{sd} and v_{sq} are the d- and q-axis measured voltages of the grid at the PCC.

The converter is synchronized with the grid voltage through the PLL shown in Fig. 2.4(a), which tracks the grid angle $\theta_{e\ grid}$ and frequency $\omega_{e\ grid}$. The PLL consists of a PI controller that aligns the grid voltage vector with the d-axis. Therefore, if the controller is in steady state, it can be assumed that $v_{sq=0}$. The gains of the PLL controller are selected as described in [93, 101]

$$K_{PPLL} = 2\ a_{PLL} \tag{2.18}$$

$$K_{IPLL} = a_{PLL}^2 \tag{2.19}$$

where a_{PLL} is the bandwidth of the PLL controller.

By considering $v_{sq} = 0$, the previous power equations in (2.16)-(2.17) become

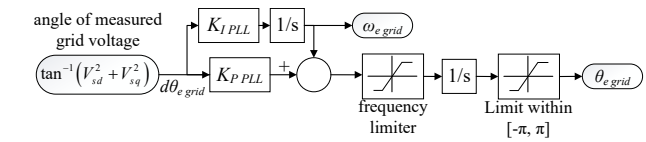
$$P_{grid} = \frac{3}{2} v_{sd}\ i_{sd} \tag{2.20}$$

$$Q_{grid} = -\frac{3}{2} v_{sd}\ i_{sq} \tag{2.21}$$

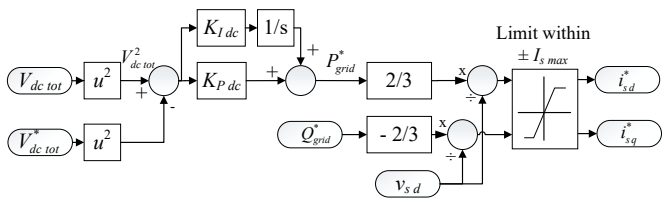
Therefore, it can be seen that the active power injected by the converter to the grid P_{grid} can be controlled by the d-axis current, while the q-axis current regulates the reactive power Q_{grid}.

Since the grid-side converter is used in back-to-back connection with another three-phase converter controlling the electrical machine of the drive, the power balance at the dc-link of the topology can be expressed as follows [102], based on the energy-flow direction labeled in Fig. 2.1(b) with blue arrows,

$$\frac{C_{dc\ tot}}{2} \frac{dV_{dc\ tot}^2}{dt} = -P_{machine} - P_{grid} - P_{loss} \tag{2.22}$$



(a)



(b)

Fig. 2.4: Block diagram of the grid-side VSC (a) PLL and (b) dc-link controller

where $P_{machine}$ the power of the machine-side converter and P_{loss} the power losses of the system. The left part of the above equation corresponds to the rate of change in the energy of the dc-bus capacitors. Since both the $P_{machine}$ and the P_{loss} cannot be directly controlled by the grid converter, it is clear that the dc-link voltage dynamics $V^2_{dc\ tot}$ depend on the P_{grid}, which can be regulated by the i_{sd} as seen in (2.20).

The dc-link controller, shown in Fig. 2.4(b), keeps the dc-link voltage close to its reference value $V^*_{dc\ tot}$. The proportional gain of the controller is selected as

$$K_{P\ dc} = a_{DClink} \cdot C_{dc\ tot} \tag{2.23}$$

where a_{DClink} is the controller bandwidth and is usually selected an order of magnitude lower than the current controller bandwidth, described in the following subsection. In this project, the dc-link PI-controller is selected to have dynamic response with time constant of 0.03 sec/rad and, therefore, the integrator is

$$K_{I\ dc} = \frac{K_{P\ dc}}{0.03} \tag{2.24}$$

Output of the dc-link control loop is the reference current of the grid converter.

2.3.2 Grid-side Current Controller Design

The grid voltage at the PCC can be expressed, transformed in the dq reference frame, as follows

$$v_{sd} = v_{td} - R_f i_{sd} + L_f \omega_{e\ grid} i_{sq} - L_f \frac{\mathrm{d}i_{sd}}{\mathrm{d}t} \tag{2.25}$$

$$v_{sq} = v_{tq} - R_f i_{sq} - L_f \omega_{e\ grid} i_{sd} - L_f \frac{\mathrm{d}i_{sq}}{\mathrm{d}t} \tag{2.26}$$

where L_f and R_f are the inductance and resistance of the three-phase grid filter, respectively, v_{td} and v_{tq} are the d- and q-axis voltages at the ac side of the grid-side converter.

The reference voltage of the converter is calculated by the grid-side current controller and its block diagram is shown in Fig. 2.5. The proportional and integral gains of the PI control loops for both d- and q-axis are K_{Ps} and K_{Is}. The current dynamics for both axes are identical and are described with the following loop-gain transfer function [102]

$$H_s(s) = H_{sPI}(s) \cdot H_f(s) = \frac{K_{Ps}\ s + K_{Is}}{s} \cdot \frac{1}{L_f\ s + R_f} \tag{2.27}$$

where $H_{sPI}(s)$ describes the PI control loop and $H_f(s)$ the dynamics of the grid-filter. The gains are selected based on the Loop Shaping Method, so that the resultant closed-loop current dynamics of the converter have first-order response.

$$K_{Ps\ d} = K_{Ps\ q} = L_f\ a_{cs} \tag{2.28}$$

$$K_{Is\ d} = K_{Is\ q} = a_{cs}\ (R_f + B_{as}) \tag{2.29}$$

$$B_{as} = L_f\ a_{cs} - R_f \tag{2.30}$$

where a_{cs} is the controller bandwidth and B_{as} the current controller active damping. Common practice is to select the current controller bandwidth at least an order of magnitude lower than the switching frequency of the grid converter.

Feed-forward of the measured grid voltage v_s for both axis is used, after being filtered by an LPF. Feed-forward of the voltage drop across the grid filter inductance is also applied, based on the voltage equations of (2.25)-(2.26)

$$\begin{aligned} \boldsymbol{V_{Lf}} &= (L_f\ \omega_{e\ grid})j \cdot \boldsymbol{i_s} \\ &= (-L_f\ \omega_{e\ grid}\ i_{sq}) + (L_f\ \omega_{e\ grid}\ i_{sd})j \end{aligned} \tag{2.31}$$

The reference voltage of the grid converter $v^*_{s\ dq}$ is the output of the current control loop, which is limited by a saturation block. The saturation block limits the voltage amplitude, but does not modify the voltage angle. Anti-reset windup is also implemented, which is not shown in the block diagram of Fig. 2.5.

Finally, the space vector modulation block generates the gate signals for the power switches of the grid converter.

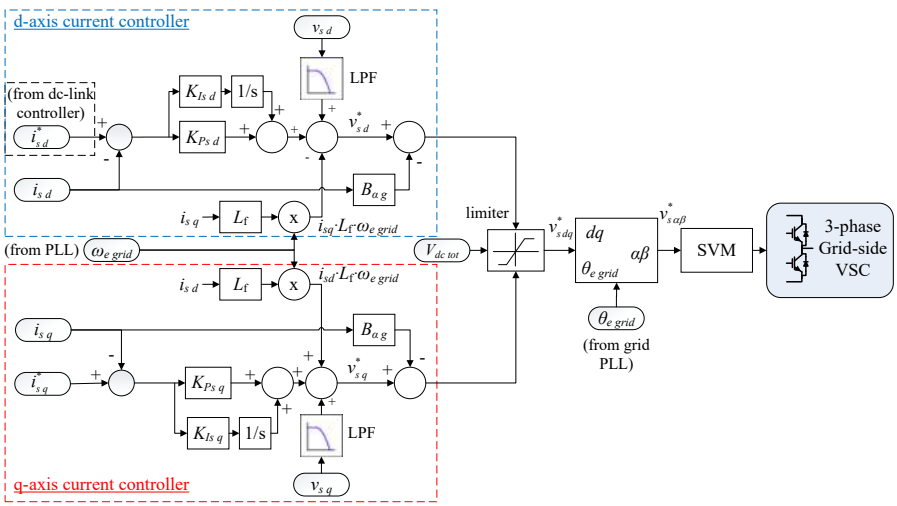


Fig. 2.5: Block diagram of the grid-side VSC current controller

Chapter 3

Modelling and Control of Kite-based Tidal Power Generator Systems

The inverter control of a generator drive for kite-based tidal power systems is analyzed in this chapter. Firstly, the motion of the kite and the power generation profile are modelled. Afterwards, the control scheme of the inverters is described and tested on a low-scaled laboratory emulator of the real kite.

3.1 Introduction to Control Techniques of the Kite

The power conversion system of the kite is mounted inside the nacelle and consists of a generator, two B2B connected VSCs and a passive LCL filter at the point of connection to the grid. A synchronous generator (SG) has been used for the purpose of this study. A block diagram of the kite can be seen in Fig. 3.1(a). The MPPT algorithm of the TUSK is an essential part of the generator control system. The speed of the water flowing though the turbine is constantly changing, because of the kite's crosscurrent motion into the sea. The optimum reference generator speed should be evaluated in order to extract the maximum electric power from the water.

The MPPT algorithms presented in [60, 61] have as input the calculated active power at the terminals of a permanent magnet synchronous generator (PMSG) and calculates the reference speed of the rotor which serves as input of the generator's speed controller. Loss minimization control of the generator through optimal current reference generation (see Subsection 2.2.2) can also be applied

simultaneously. Another type of MPPT algorithm is described in [62–64], which receives as input the measured rotational speed of the generator and generates the optimal reference electrical torque that the current controller of the machine needs to create. The speed of the rotor is controlled indirectly here, since the rotational speed and the mechanical torque of the rotor will settle down to an equilibrium with an optimal torque point, where the turbine operates at the maximum power point. The speed control strategy of the kite's generator is designed in this chapter based on these two MPPT control schemes and their performance is compared experimentally.

The rotational inertia of the tidal power system may affect the accuracy of the applied MPPT control, since the generator speed controller gains are selected based on the inertia of the mechanical drivetrain. This characteristic has a positive influence on the wind turbine drives, where the wind fluctuations are stochastic and cannot be predicted. The large wind turbine inertia has been utilized to smooth out the power fluctuations caused by sudden changes of the wind speed [103, 104] or to filter the highly fluctuating power output of wave generators [105].

The TUSK tidal system experiences also power fluctuations; however, contrarily to the wind and wave power plants these power fluctuations are periodic, highly predictable and dependent mainly on the predefined movement of the kite in the sea. It is possible to smooth out the power fluctuations of a TUSK farm by combining the power output of multiple kites, as shown in the Master thesis of [54]. Therefore, it is not necessary anymore to utilize the turbine shaft inertia in order to limit these power variations of the individual kites and the maximum power should be extracted by the tidal generator at any time instant. The inertia of the TUSK turbine shaft will still affect the transient response of the generator speed controller, which could hinder it from following the optimal MPPT curve. A speed control strategy needs to be applied on the TUSK tidal power generator that has fast dynamic performance, so that the turbine of the kite can follow the MPPT curve with the least possible error. A further analysis of the influence of the shaft inertia is conducted at the experimental results of this chapter.

3.2 Tidal Power Plant System Modeling

The TUSK plant is controlled to undergo periodic movements into the water and the orbit is eight-shaped. Water flows through the turbine blades of the kite and creates a rotational torque that generates electric power at the output of the generator. The generator is attached to back-to-back-connected VSCs which

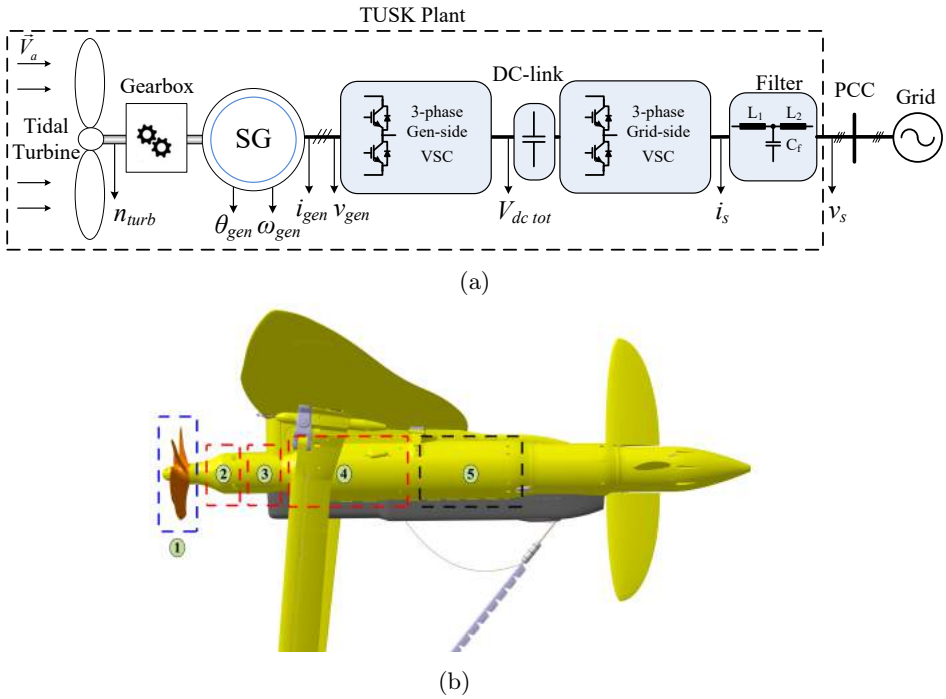


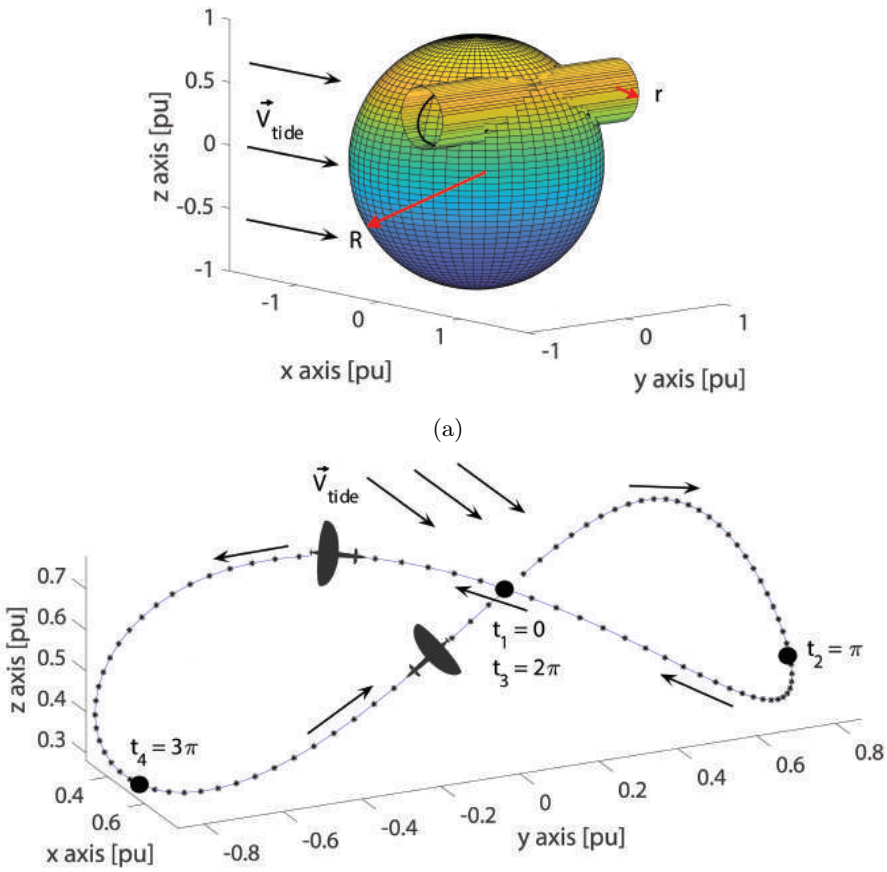
Fig. 3.1: (a) Block diagram of the power conversion subsystem in a TUSK tidal plant; (b) CAD-drawing of an early-concept kite for the DG500 project [106]: 1) tidal turbine, 2) gearbox, 3) generator, 4) power conversion subsystem and grid filters, 5) auxiliary equipment [Property of Minesto AB]

control the generator speed and the synchronization to the grid at the electrical output of the topology. In order to calculate the produced electric power of the topology, a mathematical model of the kite's trajectory is needed.

A detailed analysis of the kite's hydrodynamics can be found in the Master Thesis report [54]. The model presented here is simplified and is utilized only for the modelling of the electrical installation and the control of the power conversion system. The exact geometry of the kite and its hydrodynamic performance have not been modelled and the kite's trajectory is considered to be unaffected by the operation of the electrical generator. Also, the kite is considered to follow its trajectory without error and the control mechanisms for that are not studied here.

3.2.1 Modeling of Kite's Trajectory and Power Generation

The three-dimensional depiction of the kite's trajectory can be mathematically described by the Viviani's Curve, which is defined as the intersection between a cylinder and a sphere, as shown in Fig. 3.2. The Viviani's curve offers the minimum curvature and maximizes power production compared to other trajectories, such as the circle. The parametric equation of the Viviani's Curve in the xyz-coordinate system is given by



(a)

(b)

Fig. 3.2: Three-dimensional drawing of (a) the Viviani's curve used as the trajectory of the kite and (b) the TUSK plant following its trajectory $\vec{P}_r$ with the arrows showing the direction of the kite's movement after applying the rotation matrix in (3.2)

$$\vec{\boldsymbol{P}}\big(x(t), y(t), z(t)\big) = \left\{ \begin{array}{l} x(t) = (R-r) + r \cdot \cos(t) \\ y(t) = 2 \cdot \sqrt{(R-r) \cdot r} \cdot \sin(\frac{t}{2}) \\ z(t) = r \cdot \sin(t) \end{array} \right\} \tag{3.1}$$

where r is the cylinder radius, and R is the sphere radius. The parameter t varies from 0 to 4π and some characteristic values of t on the Viviani's curve can be seen in Fig. 3.2(b). The x-axis of the graph is in-line with the tidal current flow.

The TUSK plant is elevated from the sea floor. Also, the tether of the TUSK and the sea floor have an altitude angle D, as can be observed in Fig. 1.2. Therefore, the position vector $\vec{\boldsymbol{P}}_{\boldsymbol{r}}$ can be rotated by multiplying with the following matrix

$$\vec{\boldsymbol{P}}_{\boldsymbol{r}} = \begin{bmatrix} \cos(D) & 0 & -\sin(D) \\ 0 & 1 & 1 \\ \sin(D) & 0 & \cos(D) \end{bmatrix} \cdot \vec{\boldsymbol{P}} \tag{3.2}$$

The partial derivative vector of the rotated position vector $\vec{\boldsymbol{P}}_{\boldsymbol{r}}$ can be defined as

$$\frac{\partial \vec{\boldsymbol{P}}_{\boldsymbol{r}}}{\partial x \partial y \partial z} = \frac{\partial P_r}{\partial x}\vec{i} + \frac{\partial P_r}{\partial y}\vec{j} + \frac{\partial P_r}{\partial z}\vec{k} \tag{3.3}$$

The kite's trajectory is discretized into a definite number of points m and each trajectory point is named with the variable i. A frame of reference is then defined at each trajectory point, which is a local coordinate system describing the plant's direction with normalized matrix $\boldsymbol{B_i}$ that has dimensions {3 x 3 x m}.

$$\boldsymbol{B_i} = \begin{bmatrix} \vec{\boldsymbol{e_{1i}}} & \vec{\boldsymbol{e_{2i}}} & \vec{\boldsymbol{e_{3i}}} \end{bmatrix} \tag{3.4}$$

where $\vec{\boldsymbol{e_{1i}}}$, $\vec{\boldsymbol{e_{2i}}}$, $\vec{\boldsymbol{e_{2i}}}$ are the normalized direction vectors of the three axes. These three vectors point towards the forward direction, the wing axis and the tether axis, respectively.

The partial derivatives of the position vector in (3.3) and the plant frame of reference (3.4) are used to define the angular velocity matrix $\dot{\boldsymbol{\gamma_i}}$, which describes the rate of change of the kite's pitch, roll and yaw on each point i of the trajectory

$$\dot{\boldsymbol{\gamma_i}} = \begin{bmatrix} \Delta Pitch_i & \Delta Roll_i & \Delta Yaw_i \end{bmatrix} \tag{3.5}$$

A more detailed analysis of the mathematical movement equations can be found in Chapter 5 of [54].

The mechanical power extracted by the tidal turbine can be calculated as follows [104]

$$P_{m_i} = \frac{1}{2}\rho A_T C_p V_{a_i}^3 - P_{loss_i} \tag{3.6}$$

where $\rho = 1025$ kg/m^3 is the salt water density, C_P is the coefficient of performance of the turbine, $A_T = \pi R_T^2$ the swept area, R_T is the turbine radius and V_a the effective linear water speed flowing through the turbine in m/s. The last term P_{loss_i} describes the power losses at each trajectory point i owed to the motion of the kite and can be calculated by

$$P_{loss_i} = \boldsymbol{L_i}^T \cdot \dot{\boldsymbol{\gamma}}_{\boldsymbol{i}} \tag{3.7}$$

where L_i is a torque coefficient matrix dependent on the kite geometry. The following coefficients have been used for the analysis of this study and have been empirically chosen

$$\boldsymbol{L_i} = \begin{bmatrix} 1500 & 2000 & 1000 \end{bmatrix} \tag{3.8}$$

The torque coefficients depend mainly on the design and the physical dimensions of the whole tidal kite system and the empirical choice of these parameters could introduce some error, which is not considered during this study. The tip speed ratio TSR_i of the tidal turbine at each trajectory point i is defined as

$$TSR_i = \frac{\omega_{turb_i} R_T}{V_{a_i}} \tag{3.9}$$

where ω_{turb_i} is the turbine rotational speed in rad/s. By using (3.6) and (3.9), the resultant power is

$$P_{m_i} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^3 - P_{loss_i} \tag{3.10}$$

The active power at the point of connection to the grid can also be expressed as follows

$$P_{grid_i} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^3 - P_{loss_i} - P_{e\,loss_i} \tag{3.11}$$

where $P_{e\,loss_i}$ is the power losses of the electric drive system (mechanical and electrical) between the generator shaft and the connection to the grid. The turbine torque T_{m_i} and the electrical torque at the grid output of the kite T_{grid_i} are defined as

$$T_{m_i} = \frac{P_{m_i}}{\omega_{turb_i}} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} \tag{3.12}$$

$$T_{grid_i} = \frac{P_{grid_i}}{\omega_{turb_i}} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} - \frac{P_{e\,loss_i}}{\omega_{turb_i}} \tag{3.13}$$

The effective water speed V_a depends on the lift and drag of the kite and varies within one trajectory period. The kite's speed is controlled with fixed angle of attack and variable angle of inclination, which provides the optimum performance,

based on the analysis presented in Sections 5.13 and 5.16 of [54]. Therefore, the average value of the water speed V_a can be calculated as follows [47]

$$V_{a_{mean}} = \frac{2}{3}\frac{L}{D_k}V_{tide} \tag{3.14}$$

where L is the kite lift coefficient, D_k is the drag coefficient and V_{tide} is the free stream speed of the tide, which is considered unaffected by the operation of the kite. The V_{tide} varies based of the lunar cycle, as described in Section 2 of [54]. In case the kite's trajectory in the sea is controlled with fixed angle of attack and variable angle of inclination, the optimal lift to drag ratio is equal to $\frac{L}{D_k} = 6.512$, as stated in Fig. 36 of [54], and the water speed speed in (3.14) becomes

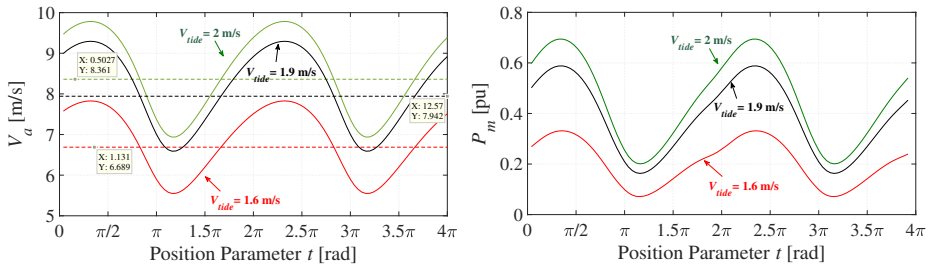
$$V_{a_{mean}} \overset{[54]}{=\!=} \frac{2}{3} \cdot 6.512 \cdot V_{tide} = 4.34 \cdot V_{tide} \tag{3.15}$$

The effective water speed V_a varies periodically around its calculated mean value, since the kite is moving at some time instants with or against the tidal current, as shown in Fig. 3.3(a). These water speed fluctuations create a variation of the extracted mechanical power, as well, since in (3.6) it can be seen that the mechanical power is a function of the water speed. Therefore, the turbine rotational speed ω_{turb} and shaft torque vary also periodically based on (3.11) and (3.13), when the turbine has constant TSR and C_P.

Experimental measurements of the C_P and the TSR for the turbine used in the TUSK plant are not available. Therefore, the curve shown in Fig. 3.4(a) is used for the analysis of this chapter, which is referenced from [107–109] where

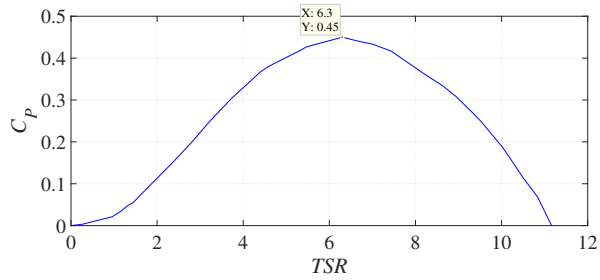
Table 3.1: TUSK Design Parameters

Parameter	Value	Unit
Cylinder radius r	25	m
Sphere radius R	100	m
Turbine radius R_T	0.75	m
Altitude angle D	45	°
Maximum C_{Pmax}	0.45	-
Optimal TSR_{opt}	6.3	-
Power plant base power S_b	500	kVA
Turbine base speed $\omega_{turb\,b}$	84	rad/s
Maximum effective water speed $V_{a\,max}$	10	m/s



(a) (b)

Fig. 3.3: (a) Effective water speed in m/s and (b) turbine power in pu for maximum C_P as a function of the kite's position on the Viviani's curve



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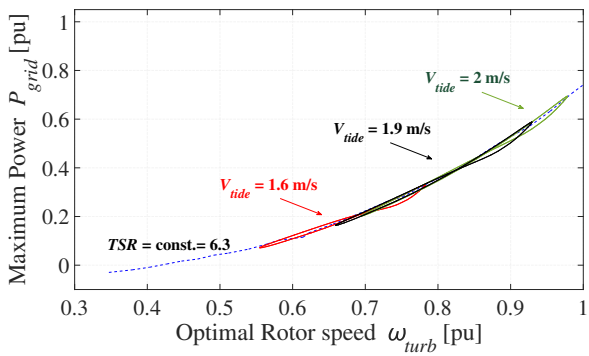


(b)

Fig. 3.4: (a) C_P curve for marine current turbine as referenced from [107–109]; (b) Grid power in pu as a function of the turbine rotational speed for optimal $TSR_{opt} = 6.3$ and maximum $C_{Pmax} = 0.45$

marine current turbines are studied. When optimal $TSR_{opt} = 6.3$ and maximum $C_{Pmax} = 0.45$ are considered, the equations (3.11) and (3.13) are converted into

$$
\begin{aligned}
P_{grid\ max_i} &= k_1 \cdot \omega_{turb_i}^3 - P_{loss_i} - P_{e\,loss_i} \\
T_{grid\ max_i} &= k_2 \cdot \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} - \frac{P_{e\,loss_i}}{\omega_{turb_i}}
\end{aligned}
\tag{3.16}
$$

The TUSK plant's design characteristics of Table 3.1 are used as base model for the power calculations of Fig. 3.3 and Fig. 3.4. A sample plant with 500 kW nominal turbine power has been chosen for the analysis of this section. Fig. 3.3(a) shows the fluctuation of V_a and Fig. 3.3(b) shows P_m during one period of the kite's motion for tidal stream speeds equal to 1.6 m/s, 1.9 m/s and 2 m/s. The dashed lines in Fig. 3.3(a) show the average effective water speed of the tidal stream speed. The average extracted power is higher, when the tidal stream increases; however, the ripple in the extracted power increases, as well. Fig. 3.4(b) shows a graphic depiction of (3.16), the grid power. For a given tidal stream speed V_{tide} the extracted power varies around a middle point, since the kite's speed is changing based on its periodic movement.

The operating region for turbine speed ω_{turb} higher than the nominal value of 1pu has not been considered at this study, due to mechanical constraints of the experimental set-up in Section 3.3. In the real-life kite system the turbine speed would be limited by the pitch controllers, after it exceeds the nominal value.

3.2.2 MPPT with Active Control of Generator Rotor Speed

An MPPT control strategy where the rotational speed of the generator is directly controlled is shown in this subsection. The control system of the generator-side VSC consists of an MPPT block that generates the reference rotor speed ω_{gen}^* in rad/s, an outer speed controller loop and an inner current controller, which finally generates the reference voltage $v_{gen\ \alpha\beta}^*$ of the inverter. The control structure of the SG is based on the FOC strategy for synchronous machines, previously described in Section 2.2. The block diagram of the MPPT control can be seen in Fig. 3.5. The MPPT algorithm presented in [110], which is widely used in wind power plants, has been adopted here in order to develop a suitable control scheme for TUSK power plants.

More specifically, the active power at the grid side of the drive is measured and the optimal rotor speed is calculated though (3.11) for $TSR = TSR_{opt}$ and $C_P = C_{Pmax}$ in order to maximize the power production of the plant. A low-pass filter is applied on the reference rotor speed to filter out high frequency harmonics that come from the grid power measurement.

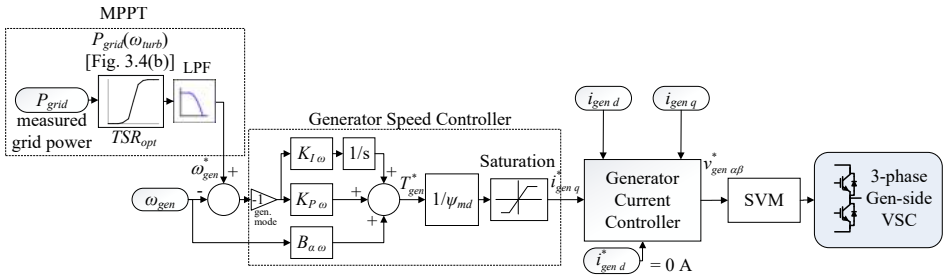


Fig. 3.5: Block diagram of the synchronous generator FOC-based control system with separate speed control loop

The TSR_{opt} and C_{Pmax} in (3.11) depend on the geometry of the turbine and are obtained through experimental results in practical applications. In this study, the tidal turbine optimal TSR_{opt} and maximum C_{Pmax} are equal to the values provided in Table 3.1, which have been referenced from [107–109].

3.2.3 MPPT with Torque Control of the Generator

Another way of operating the turbine on the maximum power point is by generating directly the necessary electrical reference torque without the use of any speed controller loop, as referenced from [111]. There is no active control of the shaft speed, since the speed is only a result of the balancing between the generator electrical torque and the mechanical torque of the turbine. The main advantage of this MPPT algorithm is the simplicity of the generator control, since only the current controller is needed. An analytical comparison of both MPPT methods is described in Subsection 3.4.2.

Input of the MPPT control algorithm is the measured rotor speed and the optimal electrical torque is calculated based on the torque-speed equation in (3.13) for

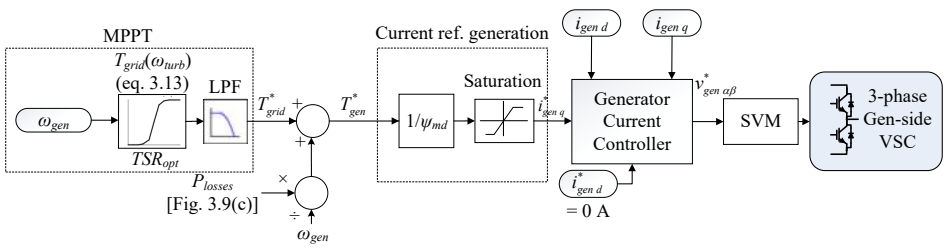


Fig. 3.6: Block diagram of the synchronous generator FOC-based control system with generator torque control

$TSR = TSR_{opt}$ and $C_P = C_{Pmax}$, so that the turbine can operate under MPPT. The torque given by (3.13) is the electrical torque at the grid side of the kite and, therefore, the losses of the system have to be added in order to calculate the reference torque of the generator.

$$T^*_{gen} = T^*_{grid} + \frac{P_{electrical\,loss}}{\omega_{gen}} \tag{3.17}$$

The losses $P_{electrical\,loss}$ include the stator losses of the generator, the B2B converter and the grid filter losses and are shown in Fig. 3.9(c). The reference current I^*_q is calculated by dividing the reference torque with the flux of the generator and the reference current is fed to the generator current controller. The block diagram of the control system for the generator-side converter is shown in Fig. 3.6, when the generator is controlled in torque control mode.

3.3 Design of Tidal Power Laboratory Emulator

A tidal kite emulator was designed in order to test the system model described in Section 3.2 and the control strategy of the SG. Fig. 3.7 shows the structure of the experimental set-up, which consists of an IM and an externally excited synchronous generator. The SG is driven by B2B-connected VSCs, which operate similarly to the generator drive of a real tidal power plant.

The generator-side VSC controls the generator voltage and speed using the field-oriented control scheme [112] (see Section 2.2) and voltage-oriented control is used for the grid-side VSC [102] (see Section 2.3). In order to simplify the machine control, it is set $i^*_{gen\ d} = 0$ A and the generator torque is controlled only by the q-axis current. There is a grid filter L_f at the output of the grid-side VSC and a resistor bank R_{init} for soft-charging the dc-link capacitors at the initial start-up

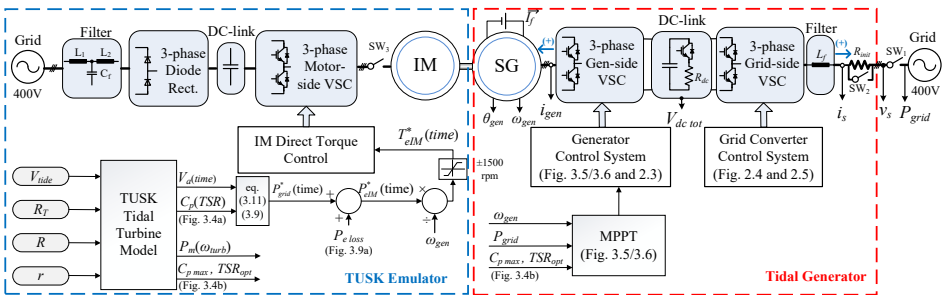
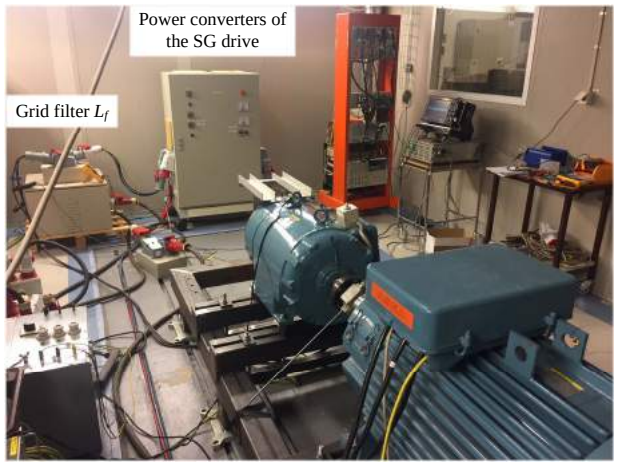
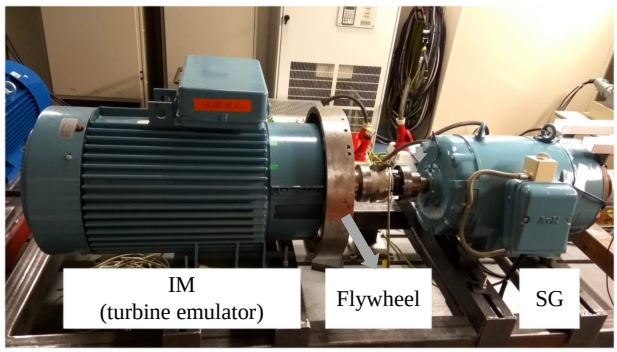


Fig. 3.7: Power circuit and control system diagram of the TUSK tidal plant emulator



(a)



(b)

Fig. 3.8: Laboratory set-up of a 35 kVA converter-driven TUSK tidal plant emulator: (a) overview of the set-up and (b) the electrical machines test bench with the flywheel installed

of the system. The dc-link of the generator drive is protected from overvoltage with a braking chopper R_{dc}.

The IM is supplied by a VSC and a passive diode rectifier and emulates the behavior of the TUSK tidal turbine. The control system of the SG power converters is implemented on the dSPACE 1005 control board. The design parameters of the experimental emulator and the base of the experimental analysis per-unit system are presented in Table 3.2. An overview picture of the laboratory set-up is shown in Fig. 3.8(a).

In order to emulate the turbine shaft inertia of a real TUSK tidal plant, a flywheel

Table 3.2: Tidal Power Emulator Design Parameters

Parameter	Value	Unit
Base rotor speed n_b	1500	rpm
Base power S_b	35	kVA
Base current I_b	71.7	A
SG number of pole pairs P	2	-
Shaft inertia (without the flywheel) J	2.04	kg·m^2
Shaft inertia (with the flywheel) J'	7.78	kg·m^2
SG friction constant b	0.073	Nm/rad·s
SG excitation I_f	22	A
SG Stator resistance R_s	60	mΩ
SG Stator inductance L_d	10.8	mH
SG Stator inductance L_q	6.2	mH
SG d-axis mutual inductance (for rated I_f) L_{md}	10.4	mH
Power converters' switching freq. f_{sw}	5	kHz
Grid filter inductance L_f	2	mH
DC-link capacitance	6.08	mF
Nominal dc-link voltage of the SG drive $V_{dc\ tot}$	670	V
Nominal L2L grid voltage (rms) V_s	400	V

has been installed in the machine set-up as shown in Fig. 3.8(b). The flywheel has the shape of a circular disc and a mass of approximately 90 kg. The additional inertia that the flywheel adds on the shaft of the electrical machines is equal to 5.74 kg $\cdot$ m^2.

The IM of the experimental set-up is controlled in Direct Torque Control (DTC) mode by an ACS600 ABB drive [113]. The rated rotational speed of the IM is 1445 rpm. The electromagnetic torque reference T^*_{eIM} is calculated by the tidal turbine model, which has been previously presented in Section 3.2.

As seen in Fig. 3.7, inputs of the tidal turbine model are the design characteristics of the TUSK trajectory and turbine geometry, while outputs of the model are the optimal power-rotor speed curve (Fig. 3.4), the maximum C_{Pmax}, optimal TSR_{opt} and a time series of the effective water speed V_a. Then, the active power of the TUSK plant is calculated based on (3.11). The losses of the laboratory emulator are compensated by adding them to the reference grid power $P^*_{grid}(time)$. Finally, the reference electromagnetic torque of the IM T^*_{eIM} is calculated by dividing the

active power $P^*_{eIM}(time)$ with the rotor speed.

The losses of the laboratory emulator have been measured with the oscilloscope and are shown in Fig. 3.9 for many different operational points of the SG. Specifically, the measured losses in Fig. 3.9(a)-(b) include the mechanical losses of the IM and SG, the core and copper losses of the SG, the generator and grid VSC losses and the grid filter L_f losses. Fig. 3.9(c)-(d) shows only the converter and grid filter losses of the SG drive.

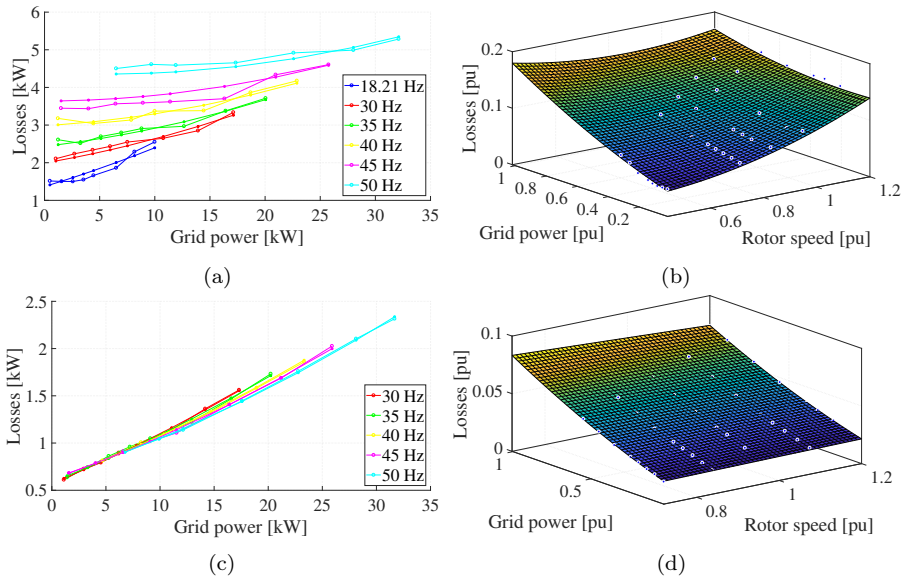


Fig. 3.9: Curve-fitted diagram of the TUSK tidal power emulator losses including the (a)-(b) total SG drive losses and the IM mechanical losses and (c)-(d) the electrical losses of the power converters and grid filter in the SG drive

3.4 Experimental Results of the Laboratory Emulator

The experimental results of this section are divided into two parts. In Subsection 3.4.1 an analysis of the bandwidth of the speed controller is made and its effect on the kite's power generation is shown. Experimental results from the TUSK plant emulator are presented, while in this case the flywheel shown in Fig. 3.8(b) is not installed in the set-up in order to allow faster responses of the speed control.

In Subsection 3.4.2 a comparison of the MPPT algorithms from Subsections 3.2.2

and 3.2.3 is made for different operating conditions of the TUSK. The flywheel is installed in this case on the shaft of the machine system, in order to study also the effect of the inertia on the response of the system and to point out any possible problems that can arise.

3.4.1 Effect of the Speed Controller's Response Time on the kite's Power Generation

The transient response experimental results of the SG speed controller are shown in Fig. 3.10(a)-(b), where a step-change of the speed reference is performed from 0.6 pu (corresponding to 900 rpm) to the nominal speed of 1 pu (which is equal to 1500 rpm). As can be seen in the figure, the rise time t_r is 0.31 s, when the speed controller bandwidth is $a_\omega = 2\pi$ rad/s. The reference q-axis current of the generator I^*_{genq} reaches also its maximum positive value of 71.7 A, while the machine is accelerating. Due to the fast acceleration applied in this test, the SG operates temporarily in motor operation and the current becomes positive. A slower speed controller with bandwidth equal to $a_\omega = 2\pi \cdot 0.1$ rad/s has also been tested in Fig. 3.10(c)-(d), which has a rise time t_r of 3.66 s. The t_r is defined as

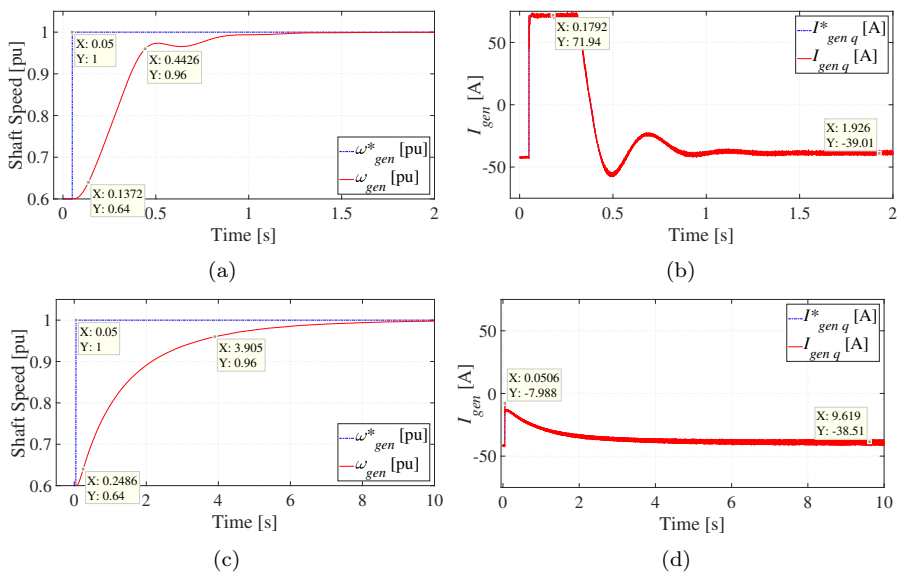


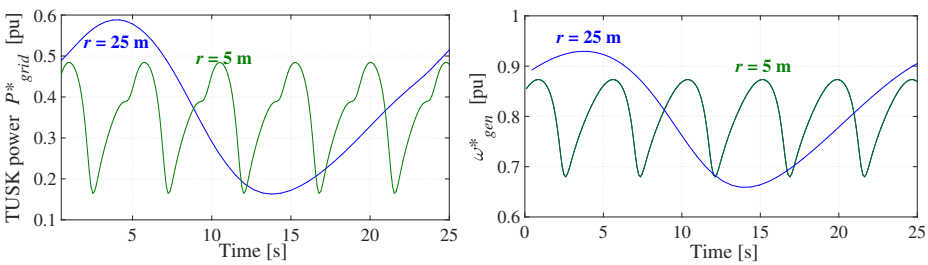
Fig. 3.10: Experimental results of the SG in a step-change of the reference speed from 0.9pu (900rpm) to 1pu (1500rpm) with speed controller bandwidth equal to (a)-(b) $a_\omega = 2\pi$ rad/s and (c)-(d) $a_\omega = 2\pi \cdot 0.1$ rad/s

the response time of the generator between 10% and 90% of the final value of the reference speed.

The TUSK tidal plant model shown in Subsection 3.2.1 is tested experimentally on the laboratory emulator and the power curves of Fig. 3.11 are imported into the dSPACE control platform. The power and speed calculations have been converted into the per-unit system in order to scale down the real 500 kW tidal turbine (Table 3.1) into the 35 kVA electric drive of the emulator (Table 3.2). Aim of this test is to investigate if the generator speed controller can follow effectively the speed reference given by the MPPT block. The MPPT control algorithm with separate speed control loop of the generator (Fig. 3.5) is used in this subsection. As can be seen in Fig. 3.11, a decrease of the Viviani's curve r radius results to faster turbine power variations and faster variations of the generator speed reference, since the system is controlled with TSR_{opt} and C_{Pmax}. More specifically, $r = 25$ m results to a power variation with period 22.9 s, while at $r = 5$ m the period of the power is 4.6 s.

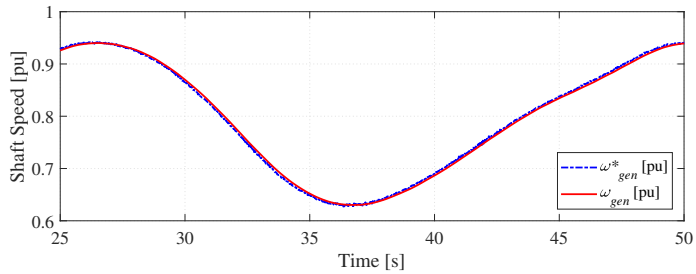
The experimental results of the emulator for Viviani's curve radius equal to $r_1 = 25$ m and $r_2 = 5$ m are shown in Fig. 3.12. The generator actual speed ω_{gen} follows the reference shaft speed given by the MPPT control block with small error, when the bandwidth of the speed controller is equal to $a_w = 2\pi$ rad/s and the radius of the trajectory is $r_1 = 25$ m [Fig. 3.12(a)]. However, when the tidal kite's motion becomes faster at $r_2 = 5$ m, the error between the reference speed and the actual shaft speed becomes larger. This error increases even more when the bandwidth of the speed controller is equal to $a_w = 0.2\pi$ rad/s.

The error between the reference rotor speed and the actual speed causes the

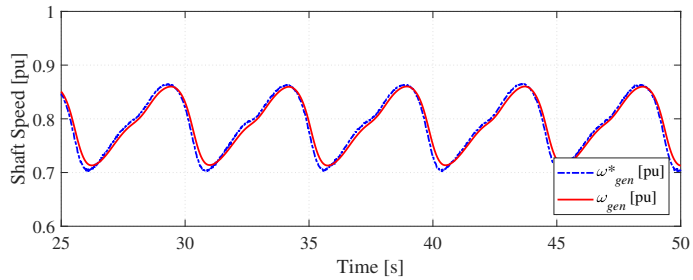


(a) (b)

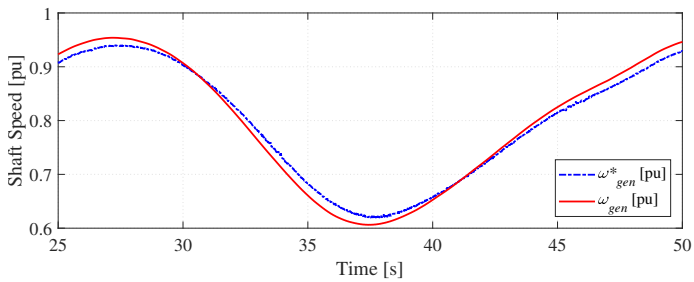
Fig. 3.11: (a) Reference grid power and (b) shaft speed of the tidal power emulator for modelling a TUSK tidal power plant with tidal stream speed $V_{tide} = 1.9$ m/s and Viviani's curve radius $r_1 = 25$ m and $r_2 = 5$ m.



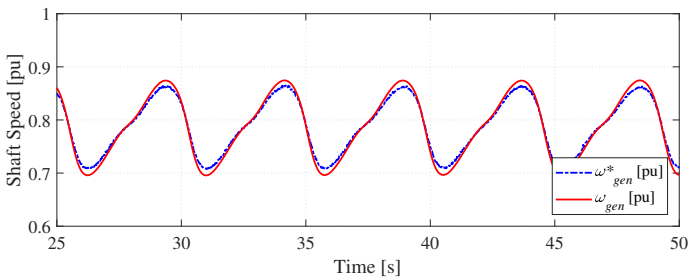
(a) $a_\omega = 2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 2\pi$ rad/s, $r = 5$ m

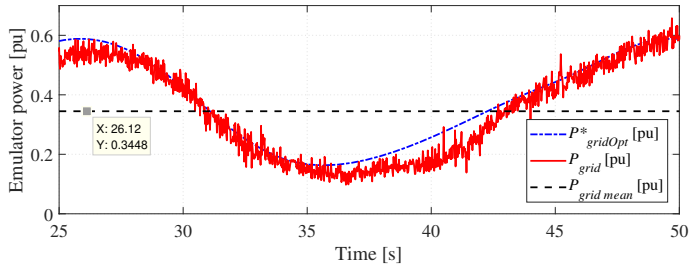


(c) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m

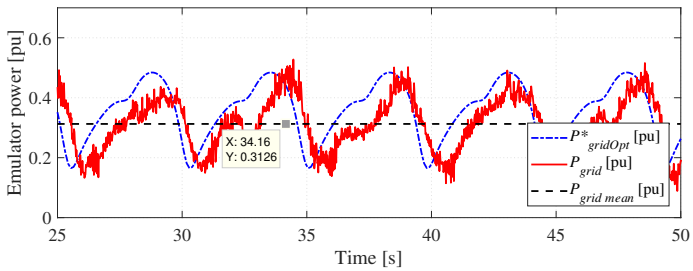


(d) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

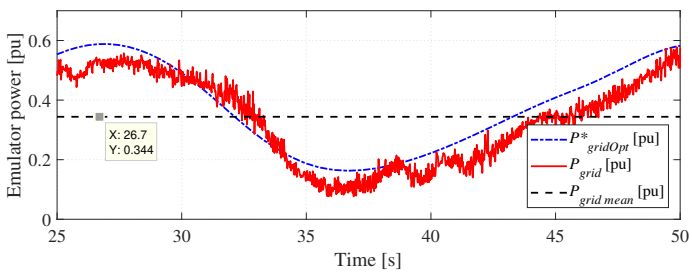
Fig. 3.12: Experimental results of the tidal power emulator reference and actual shaft speed with different profiles of the TUSK trajectory and different generator speed controller bandwidths



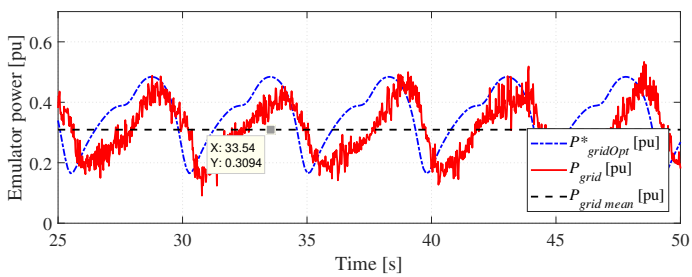
(a) $a_\omega = 2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 2\pi$ rad/s, $r = 5$ m



(c) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(d) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

Fig. 3.13: Experimental results of the tidal power emulator reference and actual grid power with different profiles of the TUSK trajectory and different generator speed controller bandwidths.

emulated power plant to operate with TSR different from the optimal value, which also results to a decrease in the produced power. Fig. 3.13 shows with dashed blue line the active power at the grid side that the emulator would produce, if it could always operate with optimal TSR and maximum C_p. The actual power P_{grid} produced by the emulated plant is also shown with red line and the average actual power is shown with black dashed line. It can be seen that the produced power of Fig. 3.13(a) is the closest to the optimal case, while in all the other cases the actual power is a little lower than the optimal power. There is also a time shift between the $P_{gridOpt}$ and P_{grid}, which is more visible in Fig. 3.13(b) and Fig. 3.13(d). This delay is introduced by the PI controller of the generator speed control loop and by the LPF at the output of the MPPT block (Fig. 3.5).

3.4.2 MPPT Algorithm Comparison Study

The MPPT algorithms described in Subsections 3.2.2 and 3.2.3 are now compared experimentally on the tidal power emulator. The flywheel is installed in this case on the shaft of the machine system and the inertia of the mechanical system increases compared to the previous study and is equal to $J' = 7.78$ kg·m^2. The transient response of the SG speed controller is shown in Fig. 3.14, where a step-change of the speed reference is performed from 0.6 pu (corresponding to 900 rpm) to the nominal speed of 1 pu (which is equal to 1500 rpm). Bandwidths of $a_\omega = 2\pi$ rad/s and of $a_\omega = 2\pi \cdot 0.1$ rad/s are tested, similarly to Subsection 3.4.1.

As can be seen in Fig. 3.14(a), the rise time t_r is 1.07 s, when the speed controller bandwidth is $a_\omega = 2\pi$ rad/s, which is as expected more than three times higher than in the case without the flywheel. The rise time becomes equal to $t_r = 3.46$ s, when the slower speed controller $a_\omega = 2\pi \cdot 0.1$ rad/s is tested [Fig. 3.14(c)].

The TUSK tidal plant model is tested experimentally on the laboratory emulator and the power curves of Fig. 3.11 are imported into the dSPACE control platform. The MPPT control algorithm with speed control loop (Fig. 3.5) is compared with the algorithm with torque control of the generator (Fig. 3.6) in the following figures in order to identify which control structure has the best performance.

The experimental results of the shaft speed for Viviani's curve radius equal to $r_1 = 25$ m and $r_2 = 5$ m are shown in Fig. 3.15. The blue curve shows the reference speed ω^*_{gen} which is generated by the MPPT block, when the generator is controlled with speed controller and bandwidth equal to 0.2π rad/s. The black curve shows the optimal reference speed ω^*_{genOpt}, which is the reference speed that

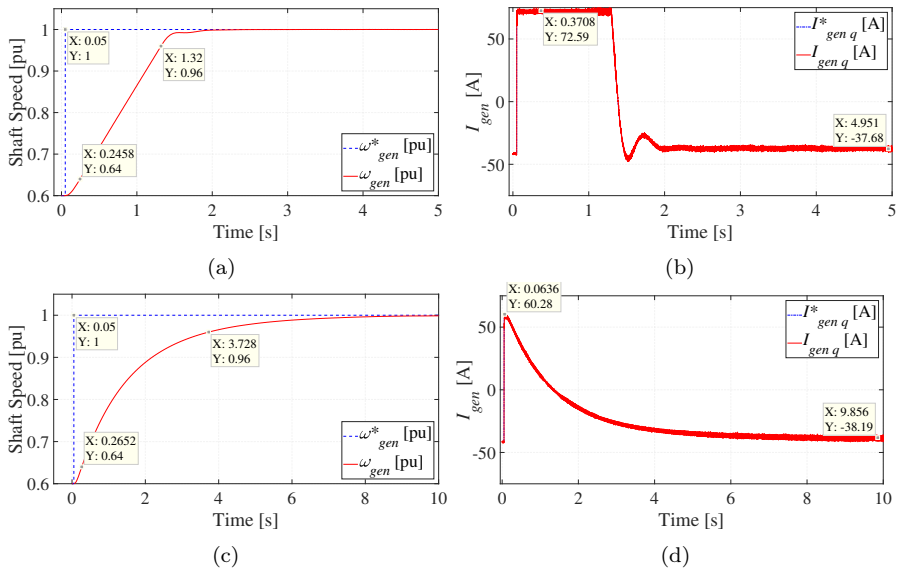
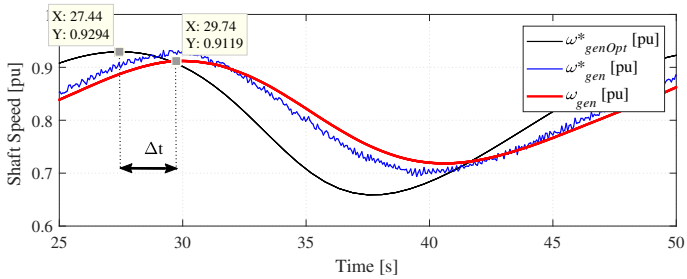


Fig. 3.14: Experimental results of the SG with the flywheel installed on the shaft in a step-change of the reference speed from 0.9 pu (900 rpm) to 1 pu (1500 rpm) with speed controller bandwidth equal to (a)-(b) $a_\omega = 2\pi$ rad/s and (c)-(d) $a_\omega = 2\pi \cdot 0.1$ rad/s

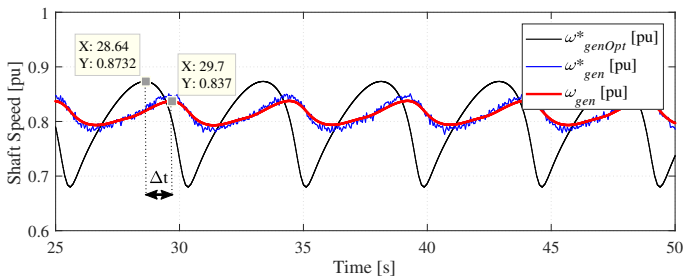
the emulator would have if it operated with constant $C_{Pmax} = 0.45$. Fig. 3.15(a)-(b) show the experimental results of the generator when the speed controller is used, while in Fig. 3.15(c)-(d) the torque control mode is used.

As can be seen in Fig. 3.15, there is a delay Δt between the actual shaft speed ω_{gen} and the ω^*_{genOpt}. The delay is higher in the case of the torque control mode compared to the speed control mode by 0.7 s, when the Viviani's curve radius is equal to $r_1 = 25$ m [Figs. 3.15(a) and 3.15(c)] and higher by 0.07 s when $r_2 = 5$ m [Figs. 3.15(b) and 3.15(d)]. Due to this delay Δt the active power produced by the emulated tidal turbine is expected to be lower in the case of the torque control mode, as will be shown later. Fig. 3.16 shows the C_P curves of the emulator for all the four operating conditions. In all the graphs the C_P curve reaches the peak point of 0.45 when the shaft speed ω_{gen} overlaps with the ω^*_{genOpt}. However, the slower response of the generator operating in torque control mode is also visible here.

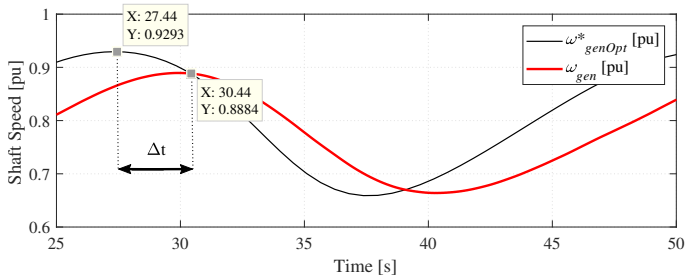
Fig. 3.17 shows the generated active power at the grid side of the emulator. The red solid line shows the actual power of the grid P_{grid}, the dashed blue line is the reference grid power P^*_{grid} and the dashed black line represents the optimal



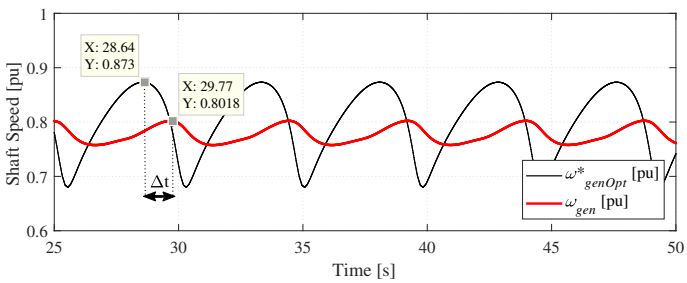
(a) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

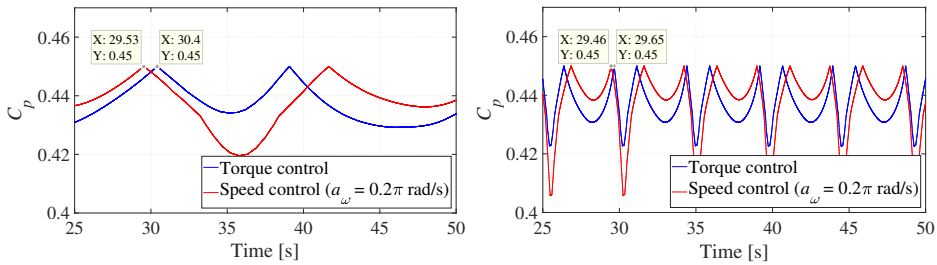


(c) Torque control, $r = 25$ m



(d) Torque control, $r = 5$ m

Fig. 3.15: Experimental results of the tidal power emulator reference and actual shaft speed with different profiles of the TUSK trajectory and different MPPT methods



(a) $r = 25$ m (b) $r = 5$ m

Fig. 3.16: Experimental results of the tidal power emulator power coefficient C_P with different profiles of the TUSK trajectory and different MPPT methods.

reference power $P^*_{gridOpt}$ that the emulator would produce with constant TSR_{opt} and C_{Pmax}. The average power $P_{gridmean}$ is shown with dashed red line and is higher when the MPPT with speed control is used in Figs. 3.17(a)-(b) compared to the results in Figs. 3.17(c)-(d).

Fig. 3.18 shows a closer look of the reference grid powers, where the peak values of the reference active power can be seen. Higher reference power can be seen here as well for the MPPT with speed control.

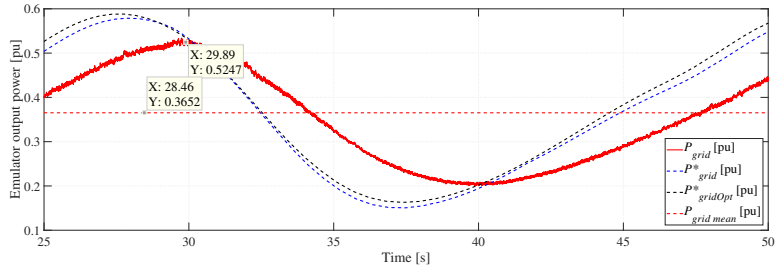
It can be concluded that the generator has a faster dynamic response when the MPPT algorithm with speed control loop is used compared to the MPPT scheme with torque control. The result of this faster response is that the generator can produce higher power at the peak points as well as in average in one cycle of the kite's trajectory. The advantageous performance of the generator speed controller can be explained by considering the time constant of the mechanical model of the generator. The time constant of the generator, when there is no active speed control loop and when torque control mode is used, is equal to

$$\tau_{Tctrl} = \frac{J'}{b} \tag{3.18}$$

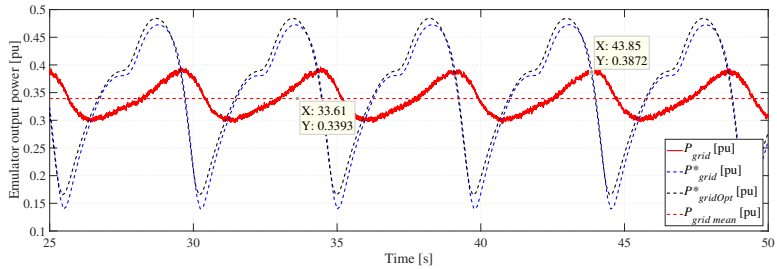
The time constant of the generator, when the speed controller is used, which is described in Subsection 3.2.2, is equal to

$$\tau_{Sctrl} = \frac{K_{P\omega}}{K_{I\omega}} = \frac{J'}{b + B_{a\omega}} \tag{3.19}$$

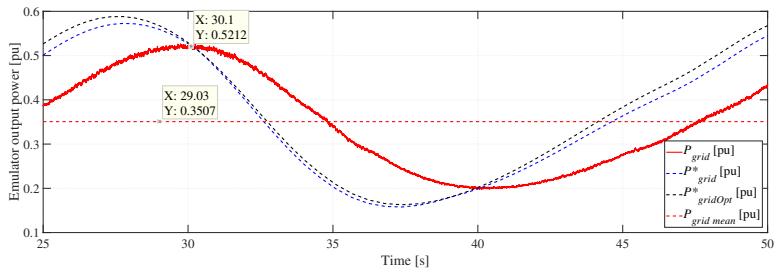
It is clear that $\tau_{Tctrl} > \tau_{Sctrl}$, which explains the previously presented experimental results.



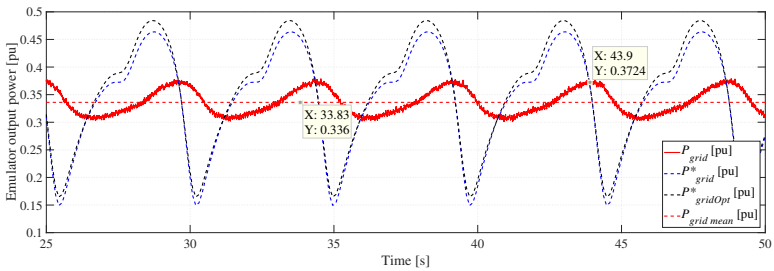
(a) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

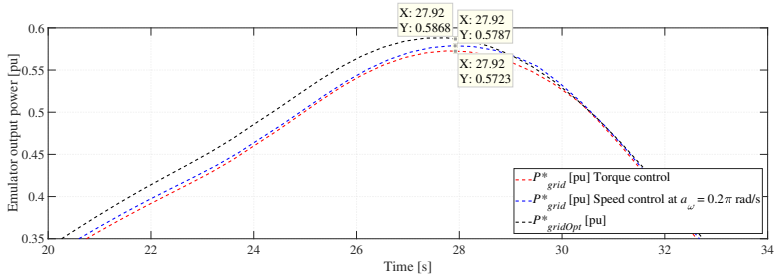


(c) Torque control, $r = 25$ m

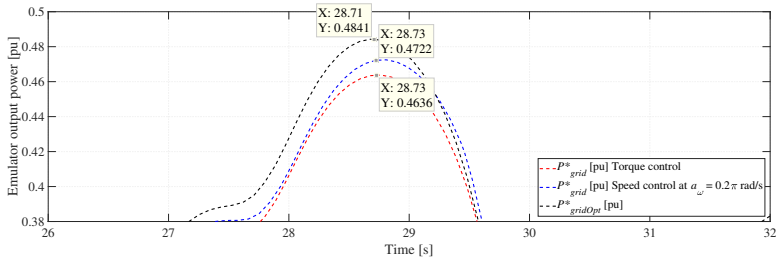


(d) Torque control, $r = 5$ m

Fig. 3.17: Experimental results of the tidal power emulator reference and actual grid power with different profiles of the TUSK trajectory and different MPPT methods



(a) $r = 25$ m



(b) $r = 5$ m

Fig. 3.18: Experimental results of the tidal power emulator reference grid power

3.5 Summary

Chapter 3 presents the model of a TUSK tidal power generator unit describing the kite's trajectory and the produced electric power. It has been shown that the tidal turbine produces fluctuating electrical power due to the motion of the TUSK into the sea. Two different algorithms of MPPT have also been presented, one with closed loop speed control and the second method with torque control of the generator. A laboratory emulator of the TUSK has been constructed for reproducing the performance of the tidal system in laboratory conditions. The accuracy of the shaft speed control has been evaluated with measurements on the emulator for different trajectories of the TUSK and gains of the speed controller.

The experimental results are divided into two parts. The first part in Subsection 3.4.1 analyzes the effect of the speed controller bandwidth on the performance of the MPPT. Specifically, Fig. 3.13 shows that an increase of 10 times of the PI controller gains results to an increase of the average produced power of up to 1%, since the speed controller of the generator converter can follow the reference rotor speed with smaller error. Therefore, a better design of the PI controllers regulating the converters and a fast speed controller can increase the power produced by the TUSK tidal power system.

The second part of the experimental results in Subsection 3.4.2 compares two MPPT control schemes, the MPPT with torque control of the generator which is simpler and easier to design and the control scheme with active speed control. The speed control method has advantageous dynamic response which results to a higher power production of the tidal turbine, although the difference in the performance of both methods is quite small in some cases. Specifically, the average power production of the generator $P_{grid\ mean}$ is approximately 4% higher when using active speed control compared to the MPPT with torque control, as shown in the Figs. 3.17(a) and 3.17(c) where it increases from 0.3507 pu to 0.3652 pu.

The results of this chapter can be utilized to improve the power production of tethered kites. The advantages and disadvantages of each MPPT control scheme need to be considered in order to evaluate if the more efficient, but also more complicated, speed control method should be used or the torque control method is better due to its simplicity. The experimental set-up of the tidal power emulator can also be used for modelling the power generation from other renewable energy sources, such as the wind power. The wind speed variations are stochastic, contrarily to the kite tidal speed variations which have been studied here. Therefore, emulating wind speed variations with the IM of the current experimental set-up could be of high value in order to investigate and optimize the performance of the generator.

Chapter 4

Multilevel Converter Topologies and Modulation Techniques

4.1 Motivation towards Medium Voltage Drives

Increasing the operating voltage of the power generation system has attracted considerable research interest in offshore applications, since it can lead to higher power density. Electrical machine drives with higher voltage have lower current flow in the cables and the power converters, which reduces copper loss and leads to a possible reduction of the cables size. Medium voltage drives are particularly popular in power generation from renewable energy sources (RES), including wind and tidal/wave power systems, where the high power density can lead to a decrease of the system level cost. Large power generation units (e.g. 10 MW or even higher) suffer from high current on the cables and on the semiconductors of the converters [91], whereas by increasing the operating voltage of the system, the conduction losses can be considerably reduced.

Especially in the case of the TUSK, the power cables, which are installed inside the tether of the kite, can hinder its movement inside the sea and create additional drag which is reflected in the power production equation (3.6). Therefore, it is of high importance to decrease the size and weight of the cables as much as possible. Also, the kite is connected to the onshore PCC through long cables which lay on the sea-bed. The power losses and the voltage drop through these cables need to be kept at minimum level in order to connect to the local grid. Increasing the operating voltage of the power generation system will decrease the

copper losses through these undersea cables. Therefore, the efficiency of the power transportation system can be highly increased, if the copper area of the cables is kept constant. Otherwise, the cable size can be reduced making the kite system more compact, if it is decided the efficiency of the cables to remain the same as with a low-voltage system.

4.2 Multilevel Converter Topologies & Capacitor Voltage Balancing

The above issues can be effectively addressed by using medium voltage multilevel converters in the generator drive. The basic concept of these topologies is the interconnection of many low-voltage-rated power switches. A simple series connection of power switches may increase the operating voltage of the converter as that shown in the traditional 2-level converter (2LC) of Fig. 4.1(a). However, this type of converter faces the serious problem of unbalanced voltage sharing among the power switches due to the system parasitic components and the uneven characteristics of the power switches. This problem can be solved by using balancing circuits or special designed gate drivers that ensure synchronous turn on/off of the switches [66, 67]. The losses of the medium voltage 2LC are also higher than in the multilevel topologies described later [67].

Multilevel converters can be defined as the inverters that generate at least three voltage levels at their ac side. Multiple low-voltage-rated power switches are used in these topologies, so that the converter is able to operate with high voltage. This topology also attains reduced total harmonic distortion at the ac side, compared to the 2-level VSC. This is a further advantage in the case of the undersea kites because the passive filters placed inside the kite at the grid-side of the generator drive can be drastically minimized saving space and weight. Another advantage of the multilevel converters is the reduced $\frac{dV}{dt}$ of their generated ac voltage [1] , which is not further studied in this thesis.

Modular converters, such as the Cascaded H-Bridge (CHB) converter or the Modular-Multilevel-Converter (MMC) [114], are commonly used topologies in high-voltage applications. These converters due to their modular structure can have large number of levels handling many tens to hundreds kVs of voltage and,

[1] C. Larsson, A. Rydgård, G. Mademlis, Y. Liu, and M. Fredriksson, "Overvoltage Mitigation of Medium Voltage Electric Drives with Long Cables using Multilevel-Converters and Passive Filters", in *Proc. of the 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019, P.1-P.10.

therefore, they are commonly used in grid applications for improving power flow control and grid voltage stability, such as in parallel connection to the transmission lines as STATCOMs [115] and in HVDC applications [116]. One disadvantage of these topologies is the lack of a common dc-link at their dc-side, since each converter module has its own capacitor. Therefore, they are used less frequently in electric drives where two of these converters need to be connected back-to-back (B2B), because disturbances at the machine-side can affect more easily other control variables at the grid-side of the system and vice versa [117]. Also, the need for many passive components, such as capacitors at each converter module and inductors for each converter leg, can make the converter bulky.

The Neutral-Point-Clamped (NPC) (also known as Diode-Clamped) converter, originally introduced in [118], and the Flying-Capacitor (FC) converter are two of the main multilevel VSC types with a controllable dc-link at their dc-side. Their 3-level [Fig. 4.1(b)] variant has already been used in industrial applications, such as in [119, 120] for the NPC converter. Both the FC and the NPC converters are limited up to 5-levels in practical applications, because their structure becomes too complicated for higher number of levels. The power switches used in these converters are rated to 1/4 of the total dc-link voltage. Therefore, by using power switches of 1.2 kV rated voltage, dc-link voltage of up to 4 kV can be obtained in their 5-level version, depending on the safety voltage margin that we choose to have for the power semiconductors. The schematics of 5-level FC and NPC converters are shown in Fig. 4.1(c)-(d).

The main advantage of the FC converter compared to the NPC is the reduced number of semiconductor components. They have equal number of power switches, but the NPC converter has also got clamping diodes. This makes the structure of the FC much simpler compared to the NPC. However, a large number of capacitors are needed for the FC converter, which becomes even larger in the 5-level version and increases a lot the size of the power conversion system. Proper balancing of these flying capacitor voltages and precharging them during the system initialization is needed making the operation of the converter more complicated [121].

On the other hand, the NPC converter requires the highest number of semiconductors due to the extra clamping diodes that it has, which also do not have equal reverse voltage rating. For this reason, series connection of two diodes are needed in some points, as can be seen in Fig. 4.1(d). However, the NPC converter has the lowest number of capacitors [122], which keeps the volume of the converter small, if a high-power-density design is implemented with low loss semiconductor

devices. Since the size of the power conversion system is of high importance for the TUSK application, the 5-level NPC inverter is chosen as the preferred VSC topology studied in the rest of this chapter.

Another serious issue of the NPC converter is the control of its dc-link capacitors. In general, an N-level NPC converter uses a single dc-bus which is subdivided into $(N-1)$ series connected capacitors, whose voltages should be monitored and properly controlled in order to be balanced in every operating condition.

More specifically, the 3-level NPC converter has two dc-link capacitors which have normally balanced voltages, when a symmetrical three-phase load is connected at

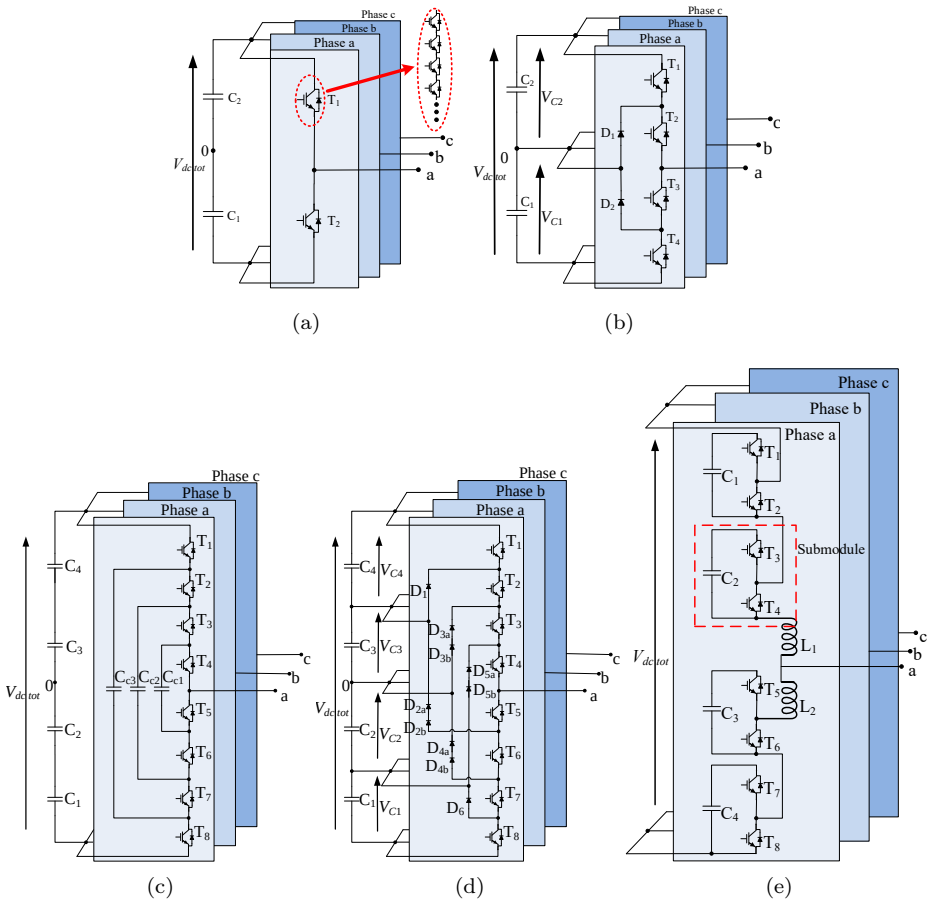


Fig. 4.1: Schematic of (a) 2-level VSC with multiple series connected switches, (b) 3-level NPC, (c) 5-level FC, (d) 5-level NPC and (e) 5-level MMC converters

the ac side. They tend to unbalance only at asymmetrical loads and faults. Many control techniques have been proposed in the technical literature for alleviating successfully the above drawback of the 3-level NPC converter and the majority uses zero-sequence voltage for balancing these voltages [80, 102]. The 5-level NPC converter, shown in Fig. 4.1(d), may be used with higher operating voltage and the harmonic distortion at the ac output is lower compared to that of the 3-level NPC. However, the dc capacitor voltage drift is more apparent here, due to the voltage unbalance in the four capacitors that may be observed even with symmetrical three-phase loads. Therefore, a more advanced control method of the dc-link capacitor voltages needs to be implemented as will be shown in the following sections.

Unequal loss distribution among the switches of the NPC converter is also a serious drawback of the NPC converter. This problem can result to asymmetrical loss distribution and junction temperatures of the semiconductors [121, 123]. The semiconductor losses can be balanced by replacing the clamping diodes with active switches and this modified NPC converter is called active NPC (ANPC) [124]. However, the loss distribution issue has not been covered in this thesis.

This chapter introduces the SVM technique properly adjusted for N-level multilevel converters. Afterwards, simulation results are presented from grid-connected

Table 4.1: Parameters of the simulated 3- and 5-level generator drive

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Total dc-link voltage	4	kV
Maximum ac L2L voltage V_{gen} (rms)	2.8	kV
Number of MOSFETs (each NPC converter)	24	(3-level drive)
	24	(5-level drive)
Number of clamping diodes (each NPC converter)	12	(3-level drive)
	30	(5-level drive)
V_{DSmax} (SCH2080KE MOSFET)	1.2	kV
I_{Dmax} (for the MOSFET at 25°C)	40	A
R_{DSon} (MOSFET)	80	mΩ
Peak Reverse Voltage V_{RRM} (C3D10170H diode)	1.7	kV
Continuous forward current (for the diode at 25°C)	29	A
Total dc-link capacitance	100	μF
Switching frequency f_{sw}	20	kHz

generator drives with 3-level converters and with 5-level NPC converters for the same operating voltage. The generator of the system is a PMSG, which is controlled with field-oriented control, while a back-to-back connected grid converter uses the voltage-oriented control scheme, as described in Chapter 2. The available methods for balancing the dc-link capacitor voltage in the 5-level drives are also presented. A comparison of the performance of the different designs of the generator drives is made in terms of simulated efficiency and voltage-current quality, as well as number of components required for manufacturing the power converters in each case.

The design characteristics of the two converters and a list of the minimum number of components, so that both converter types can operate with the same dc-link voltage, are shown in Table 4.1.

4.3 Multilevel PWM Modulation Strategies

The PWM modulator of a three-phase dc/ac converter is responsible for translating the reference voltage signal, created by the current controller, into the corresponding switching function for each active switch of the converter. The most commonly used modulation strategies for the 2LC are the sinusoidal PWM (SPWM) and the Space Vector modulation (SVM). These two methods can be extended for multilevel converters, as described in the following subsections for 5-level and N-level NPC converters.

4.3.1 Sinusoidal PWM

The SPWM technique is built with a sinusoidal reference signal for each phase of the converter running with fundamental frequency which is being compared to a high-frequency triangular carrier. For the 2LC, when the reference signal is higher than the triangular carrier, the upper switch of the corresponding phase leg is conducting, whereas the lower switch is off. Oppositely, when the reference signal is lower than the triangular carrier, the lower switch is conducting and the upper switch is turned off.

This concept can be extended for an N-level converter by using $(N-1)$ carriers shifted in amplitude instead of a single triangular carrier. This means that for a 5-level converter 4 carriers are needed, as shown in Fig. 4.2. There are many methods of placing the different carriers depending on their phase sequence, as presented in [125, 126]. The case shown in Fig. 4.2, where all the carriers are in

phase is called PH-disposition [125].

The reference phase voltage of the converter is $V^*_{ph}(t) = m(t)\frac{V_{dc\ tot}}{2}$ and $m(t)$ is the three-phase modulation signal. Its peak value is called modulation index $\hat{m}$ and can get values within $\hat{m} \in [0, 1]$. The three-phase modulation signal equations are defined as

$$m_a(t) = \hat{m} \cdot \cos(\omega t) \tag{4.1}$$

$$m_b(t) = \hat{m} \cdot \cos(\omega t - \frac{2\pi}{3}) \tag{4.2}$$

$$m_c(t) = \hat{m} \cdot \cos(\omega t - \frac{4\pi}{3}) \tag{4.3}$$

where ω is the fundamental frequency of the converter. The maximum amplitude of the reference phase voltage of the converter for this specific modulation technique is equal to

$$\hat{V}^*_{phmax} = \frac{V_{dc}\ (N-1)}{2} \tag{4.4}$$

where V_{dc} is the mean dc voltage of the capacitor cells, which is defined as

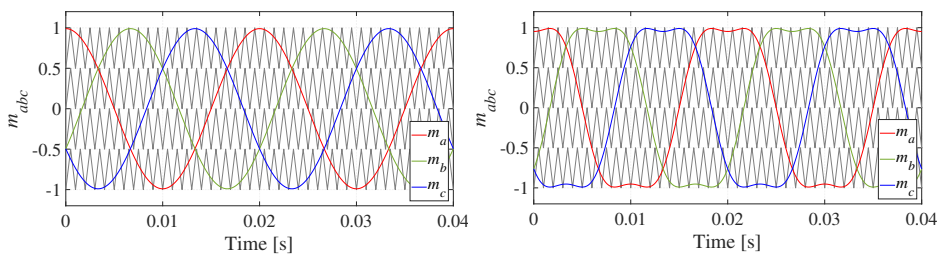
$$V_{dc\ tot} = V_{dc}\ (N-1) \tag{4.5}$$

and $V_{dc\ tot}$ is the total dc-link voltage of the N-level NPC converter.

It is possible to extend the range of the voltage and utilize better the dc-link by injecting third-harmonic components in the voltage reference. Then, the modulation signal for phase A is defined as [102]

$$m'_a(t) = \frac{3}{2}\hat{m} \cdot \cos(\omega t) - \frac{2}{3}\hat{m} \cdot \cos(\omega t)^3 \tag{4.6}$$

The term at the right side of the above equation is the third-harmonic component of the voltage, which is cancelled out in the L2L voltage. However, the maximum



(a) (b)

Fig. 4.2: Modulating signals corresponding to (a) conventional 5-level SPWM and (b) third-harmonic injected 5-level SPWM

amplitude of the voltage is now extended by almost 15% and the modulation index in (4.6) can get values within $\hat{m} \in [0, \frac{2}{\sqrt{3}}]$ without reaching overmodulation. Therefore, the maximum amplitude of the reference phase voltage of the converter becomes

$$\hat{V}^*_{phmax} = \frac{V_{dc}\ (N-1)}{\sqrt{3}} \tag{4.7}$$

The switching sequence for the switches of the 5-level NPC converter shown in Fig. 4.1(d) can be generated based on the algorithm in Table 4.2.

The multicarrier SPWM has the main advantage of being simple and easy to use. However, the main issue with this modulation strategy is the difficulty to obtain the multiple carriers with this specific amplitude shift using a regular MCU. It might be necessary to have an external customized control board which creates the required carriers and generates the suitable switching signal for each power switch of the converter. Also, the Space Vector Modulation (SVM) shown in the next subsection allows more freedom in choosing the switching states, than the SPWM, which can be utilized for control purposes.

Table 4.2: Switching States for phase A of 5-level NPC Converter with SPWM

Condition	State	Pulses*
$m_a > V_{tr1} \wedge m_a > V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	4	[1 1 1 1 0 0 0 0]
$m_a < V_{tr1} \wedge m_a > V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	3	[0 1 1 1 1 0 0 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	2	[0 0 1 1 1 1 0 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a < V_{tr3} \wedge m_a > V_{tr4}$	1	[0 0 0 1 1 1 1 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a < V_{tr3} \wedge m_a < V_{tr4}$	0	[0 0 0 0 1 1 1 1]

* for the power switches [T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8], where 1 = closed, 0 = open

4.3.2 Space Vector Modulation

The SVM allows the direct calculation of the switching state for all the switches of the converter having as input the amplitude and the angle of the ac voltage reference. The SVM diagram for a 5-level converter can be derived from the conventional 2-level space vector plane, as can be seen in Figs. 4.3(a)-(b). The N-level SVM has $6(N-1)^2$ triangles and $[N^3-(N-1)^3]$ voltage vectors [127]. In many points of the space vector plane there are multiple switching states listed the one underneath each other, which are equivalent and create the same L2L voltage. These states are called redundant states and can be utilized for control purposes, such as for balancing the dc-link voltage for the NPC converter.

The switching states can be translated into switching pulses and the conversion is unique for each converter topology. The conversion table for the 5-level NPC converter has been shown in Table 4.2.

The modulation index of the space vector modulation $\hat{m}$ is defined as follows

$$\hat{m} = \frac{\hat{V}_{ph}^{*}\sqrt{3}}{(N-1)V_{dc}} \overset{N=5}{\Longrightarrow} \hat{m} = \frac{\hat{V}_{ph}^{*}\sqrt{3}}{4V_{dc}} \tag{4.8}$$

It can be seen from the above equation that the maximum voltage obtained by the SVM without overmodulation (for $\hat{m} = 1$) is equal to the voltage calculated by (4.7), where SPWM with third-harmonic injection is used. Fig. 4.3(c) shows the vector plane of the SPWM without third-harmonic injection (with green color) and SVM (with red color), as well as the overmodulation region for $\hat{m} > 1$ (marked with yellow color) [128]. However, the overmodulation region of the SVM has not been studied in this thesis.

The space vector plane is divided into six sectors depending on the angle $\theta \in [0, 2\pi]$ of the reference voltage $\hat{V}_{ph}^{*}$, as seen in Figs. 4.3(b)-(c). The sector number is determined by

$$Sector = ceil(\theta \cdot 3/\pi) \tag{4.9}$$

The angle θ is rotated based on the sector number as described in Table 4.3, so that the voltage vector is converted into an equivalent vector of Sector 1.

The normalized value of the voltage $\hat{V}_{ph}^{*}$ can be calculated by

$$v^{*} = \frac{3\hat{V}_{ph}^{*}}{2V_{dc}} \tag{4.10}$$

and then it can be transformed into a 60°-coordinate system ($\alpha'\beta'$), as can be seen

Table 4.3: Sector Selection of SVM

Sector	Angle θ	New θ'	Basic Vector u_a [Phase$_a$ Phase$_b$ Phase$_c$]	Basic Vector u_b [Phase$_a$ Phase$_b$ Phase$_c$]
1	$(0, \pi/3]$	$\theta' = \theta$	[1 0 0]	[1 1 0]
2	$(\pi/3, 2\pi/3]$	$\theta' = -\theta + 2\pi/3$	[1 1 0]	[1 1 0]
3	$(2\pi/3, \pi]$	$\theta' = \theta - 2\pi/3$	[0 1 0]	[0 1 1]
4	$(\pi, 4\pi/3]$	$\theta' = -\theta - 2\pi/3$	[0 0 1]	[0 1 1]
5	$(4\pi/3, 5\pi/3]$	$\theta' = \theta + 2\pi/3$	[0 0 1]	[1 0 1]
6	$(5\pi/3, 2\pi]$	$\theta' = -\theta$	[1 0 0]	[1 0 1]

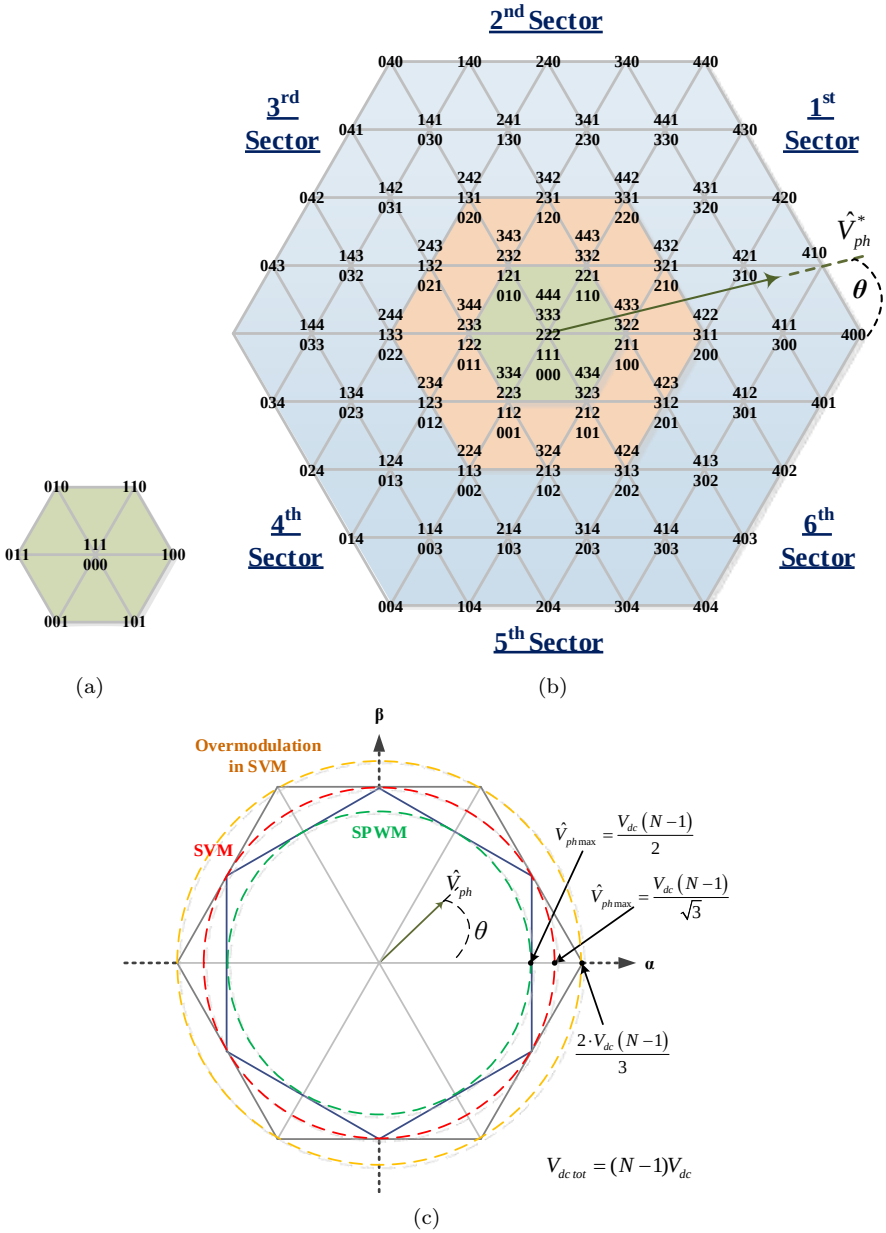


Fig. 4.3: Space vector plane for (a) 2LC and for (b) 5-level VSC; (c) voltage vector plane indicating the maximum voltage reference for SPWM without third-harmonic injection (marked in green) and SVM (marked in red)

in Fig. 4.4 [127]

$$\begin{aligned} v^*_{\alpha'} &= v^* \cos\theta' - v^* \sin\theta'/\sqrt{3} \\ v^*_{\beta'} &= v^* \sin\theta' \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{4.11}$$

The space vector $\begin{bmatrix} v^*_{\alpha'} & v^*_{\beta'} \end{bmatrix}$ is now decomposed into the following vectors

$$\begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} = \begin{bmatrix} \text{floor}(v^*_{\alpha'}) & \text{floor}(v^*_{\beta'}) \\ \text{ceil}(v^*_{\alpha'}) & \text{floor}(v^*_{\beta'}) \\ \text{floor}(v^*_{\alpha'}) & \text{ceil}(v^*_{\beta'}) \\ \text{ceil}(v^*_{\alpha'}) & \text{ceil}(v^*_{\beta'}) \end{bmatrix} \tag{4.12}$$

The vectors of (4.12) are multiplied with the basic vectors $[u_a \; u_b]$ of Table 4.3 in order to convert them back into their original sector

$$\begin{bmatrix} V'_D \\ V'_E \\ V'_F \\ V'_G \end{bmatrix} = \begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \end{bmatrix} \tag{4.13}$$

Each edge of the triangles on the space vector plane seen in Fig. 4.3 corresponds to a switching state of the converter in the format $[Phase_A \; Phase_B \; Phase_C]$. The triangles can be divided into lower triangles and upper triangles depending on their orientation and their switching sequence, as shown in Fig. 4.4 where the lower triangle $\overset{\triangle}{DEF}$ is marked with "L" and the upper triangle $\overset{\triangle}{DEF}$ is marked with "U". During each switching period T_{sw}, the triangle within which the voltage vector is located, as defined by the $\alpha'\beta'$-coordinates in (4.11), becomes active.

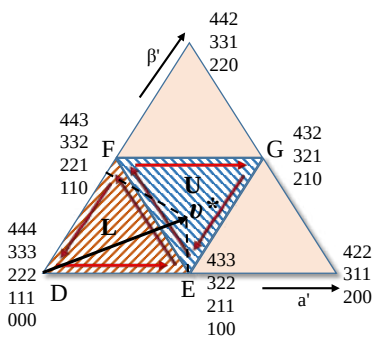
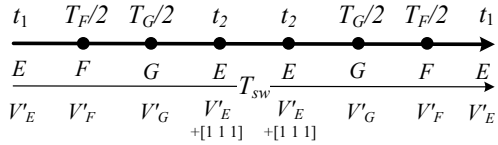


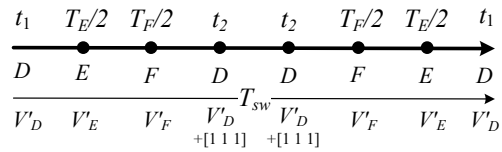
Fig. 4.4: First sector of regions 0 and I indicating the switching states of the lower and upper triangles

Then, its switching states vary in the sequence which is marked with red arrows in Fig. 4.4. More specifically, for the upper triangles the switching sequence will be



(4.14)

and for the lower triangles



(4.15)

SVM - Version 1:

There are now two ways to continue with the generation of the PWM pulses for the switches of the N-level converter. The first way is to calculate the the dwell times of each switching state (which is the percentage during the switching period when the specific state is active). For the upper triangle, the dwell times are given by [127]

$$\begin{aligned} T_E &= \big(ceil(v^*_{\beta'}) - v^*_{\beta'}\big)T_{sw} \\ T_F &= \big(ceil(v^*_{\alpha'}) - v^*_{\alpha'}\big)T_{sw} \\ T_G &= T_{sw} - T_E - T_F \end{aligned} \tag{4.16}$$

and for the lower triangles they are

$$\begin{aligned} T_E &= \big(v^*_{\alpha'} - floor(v^*_{\alpha'})\big)T_{sw} \\ T_F &= \big(v^*_{\beta'} - floor(v^*_{\beta'})\big)T_{sw} \\ T_D &= T_{sw} - T_E - T_F \end{aligned} \tag{4.17}$$

$ceil(x)$ and $floor(x)$ are mathematical operators for rounding towards up and down, respectively. The dwell times t_1 and t_2 in (4.14) and (4.15) are distributed among the redundant states V'_E for the upper and V'_D for the lower triangles

$$\begin{aligned} t_1 + t_2 &= T_E \text{ (for upper triangles)} \\ t_1 + t_2 &= T_D \text{ (for lower triangles)} \end{aligned} \tag{4.18}$$

The standard method is to distribute the dwell times t_1 and t_2 equally as follows

$$\begin{aligned} t_1 = t_2 &= \frac{T_E}{4} \text{ (for upper triangles)} \\ t_1 = t_2 &= \frac{T_D}{4} \text{ (for lower triangles)} \end{aligned} \tag{4.19}$$

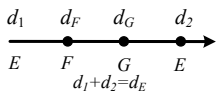
However, different distributions of the redundant states dwell times is proposed in the following sections.

Since now the dwell times for each switching state of the converter is known, the final step is to translate these switching states into pulses for each switch of the converter. Table 4.2 can be used for that in the case of the 5-level NPC converter.

The main disadvantage of this SVM method is that the final PWM pulses of the switches are calculated directly from the modulation algorithm, which is difficult to be implemented on a standard MCU board. Therefore, this version of the SVM algorithm can be used mainly for computer simulations.

SVM - Version 2:
Another version of the N-level SVM is to calculate the duty cycle of the switches instead of the dwell times of each voltage vector. The duty cycles for the switching states of the upper triangles are

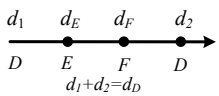
$$\begin{aligned} d_E &= ceil(v^*_{\beta'}) - v^*_{\beta'} \\ d_F &= ceil(v^*_{\alpha'}) - v^*_{\alpha'} \\ d_G &= 1 - d_E - d_F \end{aligned} \tag{4.20}$$



(4.21)

and for the lower triangles

$$\begin{aligned} d_E &= v^*_{\alpha'} - floor(v^*_{\alpha'}) \\ d_F &= v^*_{\beta'} - floor(v^*_{\beta'}) \\ d_D &= 1 - d_E - d_F \end{aligned} \tag{4.22}$$



(4.23)

Similarly to SVM - version 1, the standard distribution of the duty cycles d_1 and d_2 is the following

$$\begin{aligned} d_1 = d_2 &= \frac{d_E}{2} \text{ (for upper triangles)} \\ d_1 = d_2 &= \frac{d_D}{2} \text{ (for lower triangles)} \end{aligned} \tag{4.24}$$

Different distributions of the duty cycles of these redundant states will be proposed in the following sections.

By using (4.12) and (4.20)-(4.23) the following matrices can be generated for the duty cycle of each converter state

$$d_{state} = \begin{bmatrix} d_{PhaseA\ State1} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ d_{PhaseA\ State2} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ d_{PhaseA\ State3} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ \dots & \dots & \dots \\ d_{PhaseA\ State(N-1)} & d_{PhaseB\ State(N-1)} & d_{PhaseC\ State(N-1)} \end{bmatrix} \tag{4.25}$$

and for the duty cycle of each switch for the upper-leg of an N-level NPC converter

$$d_{sw} = \begin{bmatrix} d_{PhaseA\ switch1} & d_{PhaseB\ switch1} & d_{PhaseC\ switch1} \\ d_{PhaseA\ switch2} & d_{PhaseB\ switch2} & d_{PhaseC\ switch2} \\ d_{PhaseA\ switch3} & d_{PhaseB\ switch3} & d_{PhaseC\ switch3} \\ \dots & \dots & \dots \\ d_{PhaseA\ switch(N-1)} & d_{PhaseB\ switch(N-1)} & d_{PhaseC\ switch(N-1)} \end{bmatrix} \tag{4.26}$$

The switches of the lower-leg of each converter phase are complimentary to the upper switches. The detailed code for generating (4.25) and (4.26) is included in Appendix A.

The duty cycle d_{sw} of (4.26) is sent to the ePWM module of the MCU, as shown in Fig. 4.5, which generates the corresponding PWM signal by comparing the duty cycle with a triangular carrier. For a 3-phase N-level NPC converter $3 \cdot (N-1)$ ePWM modules are needed.

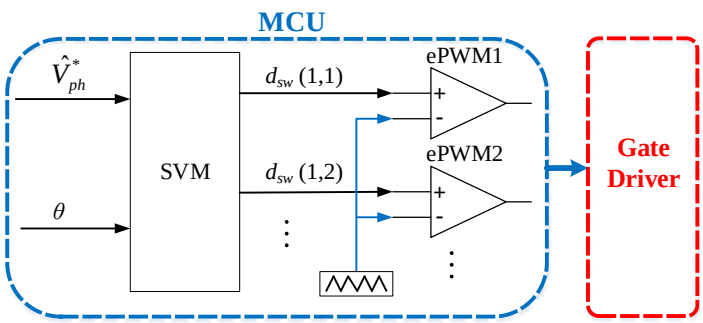


Fig. 4.5: Block diagram of the N-level SVM and the ePWM module of the MCU

4.4 Electric Drive Design using 3-level NPC Converters

An electric drive design with 3-level NPC converters is described in this section and the schematic diagram of the system is shown in Fig. 4.6. The model and the simulation results of the power converters have been implemented on Matlab/Simulink and PLECS.

The power switches of the converters are the SiC MOSFETs SCH2080KE with breakdown voltage $V_{DSmax} = 1.2$ kV and the clamping diodes are the SiC schottky diodes C3D10170H with peak reverse voltage $V_{RRM} = 1.7$ kV. In order to be able to operate the VSC at the required voltage level, two MOSFETs connected in series are used for each power-switch-block and two series-connected clamping diodes for each diode-block of the converter. SiC power switches have been chosen for the simulation analysis of this study, because they have higher voltage capabilities compared to Si switches and also lower losses. The losses of the MOSFETs SCH2080KE and the diodes C3D10170H are modelled according to the information given in their datasheets. The model on PLECS of the switching and conduction losses for the SCH2080KE can be seen in Fig. 4.7.

The following figures present the simulation results of the electric drive. Three operating points of the generator are chosen in order to test the steady-state drive performance at low, medium and high power, as shown in Fig. 4.8(a). These three operating points are at 500 rpm / 1.5 kW, at 2000 rpm / 10.5 kW and at 4000 rpm / 46 kW. The dc-link voltages and the generator current and voltage at the third operating point are shown in Fig. 4.8(c)-(d).

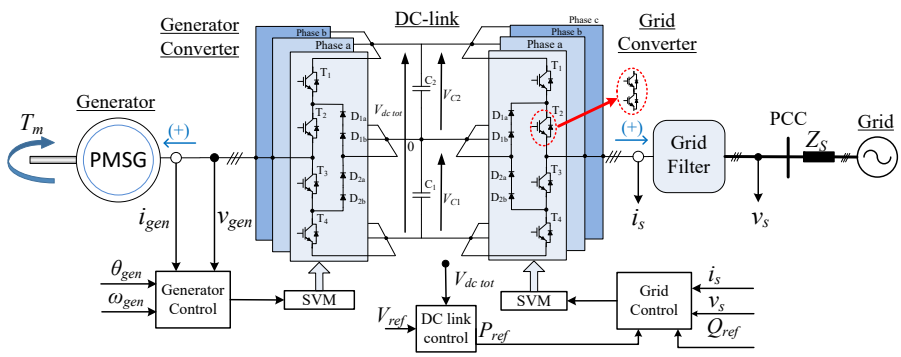


Fig. 4.6: Schematic of 3-level generator drive

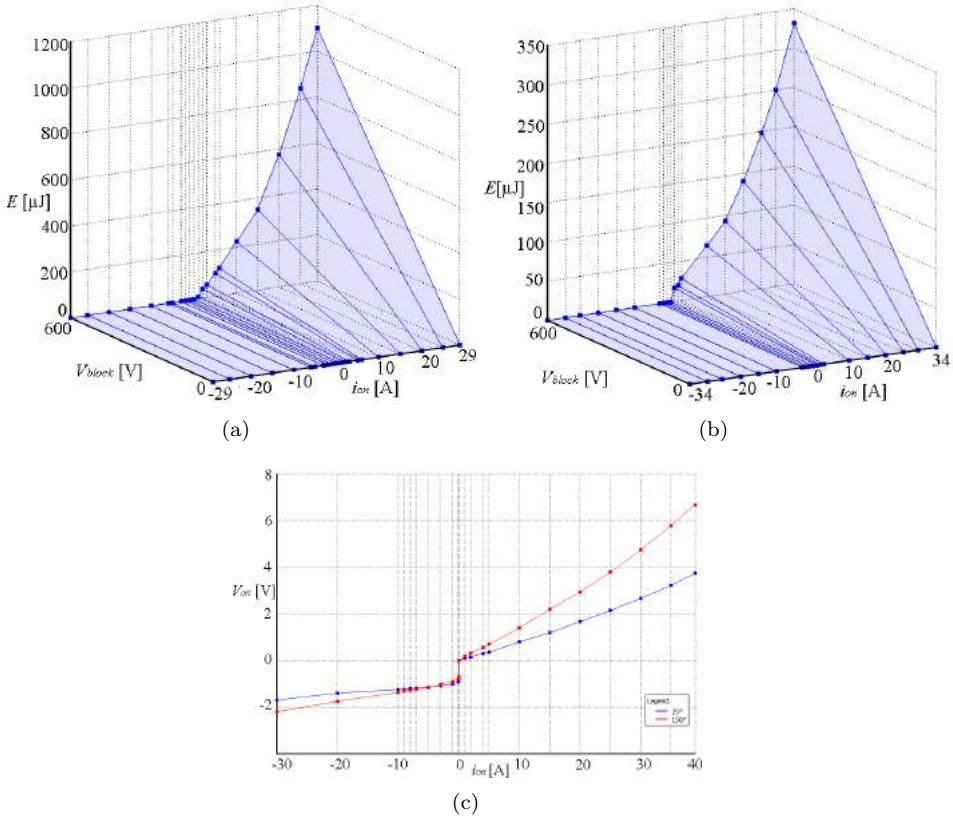


Fig. 4.7: (a) Turn-on losses, (b) turn-off losses and (c) conduction losses of the MOSFET SCH2080KE, as modelled on PLECS

The harmonics of the PMSG terminal voltage and current are analyzed in Fig. 4.9, while the system operates at rated power (operating point 3). The total harmonic distortion of the PMSG current (THD_{IGen}) is equal to 1.8% and the THD of the phase voltage THD_{VphGen} is 54.7%.

The efficiency of the two 3-level VSCs is evaluated on PLECS and the simulation result can be seen in Fig. 4.10. The system efficiency is simulated at these three operating points and the efficiency plot is extracted through curve-fitting.

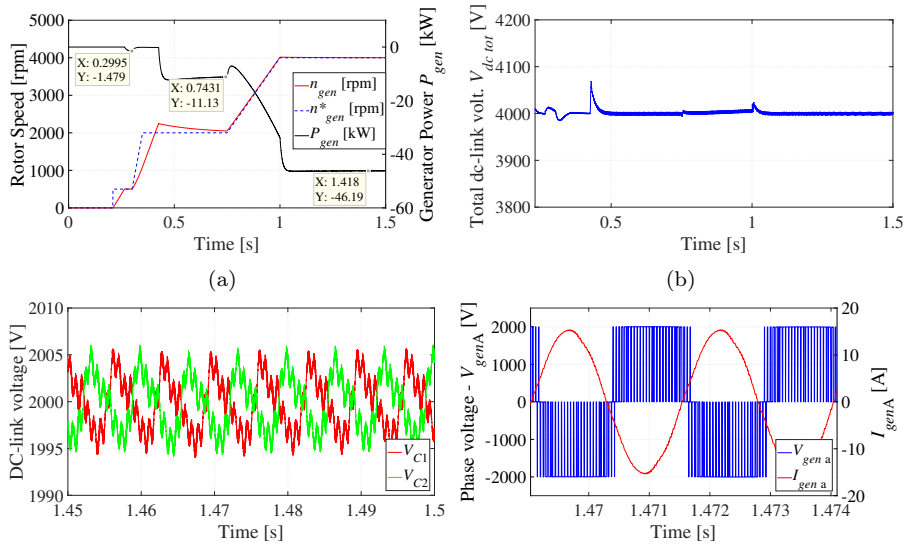


Fig. 4.8: Simulation results of the 3-level generator drive: (a) rotor speed and generator power, (b) total dc-link voltage, (c) dc-link capacitor voltages and (d) phase voltage and current at the generator-side converter

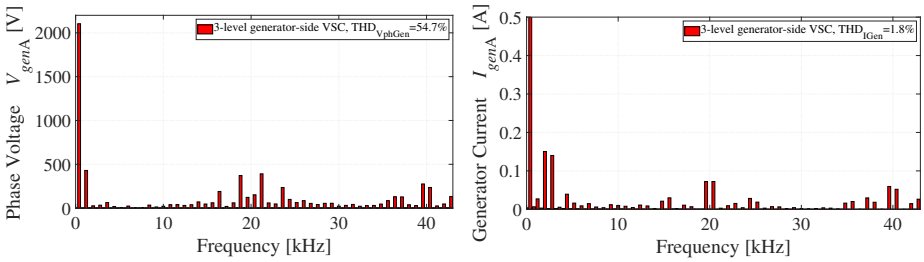
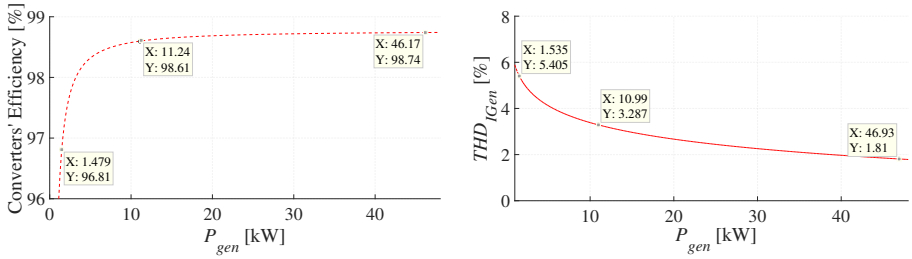


Fig. 4.9: Simulation results of the 3-level generator drive at rated power (4000rpm/46kW): (a) FFT of the PMSG phase voltage and (b) current



(a) (b)

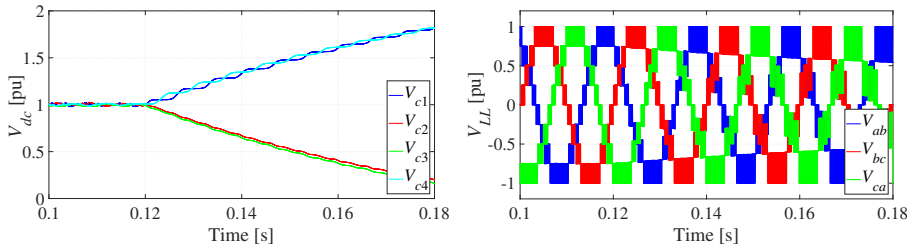
Fig. 4.10: Simulation results of the 3-level (a) power converters' efficiency and (b) THD of the stator current

4.5 Electric Drive Design using 5-level NPC Converters

The electric drive design with 5-level NPC converters is presented in this section. The same power switches and diodes with the ones mentioned in the previous section are used for this drive, namely the 1.2 kV SCH2080KE SiC MOSFETs and the 1.7 kV C3D10170H SiC diodes.

The main challenge in the control of the 5-level NPC converter is the fact that the converter is naturally unbalanced at the dc-side and, therefore, without any special control of its four dc-link capacitors, their voltage will variate a lot from its set-point [Fig. 4.11(a)]. As can be seen on the right side of Fig. 4.11(b), the unbalancing of the dc-link capacitor voltages can create distortions on the ac voltage of the converter and additional harmonics on the ac current. It can also cause the capacitors of the dc-link and the power switches of the converter to exceed their maximum voltage capabilities.

The available methods for balancing the dc-link capacitor voltages in a drive with 5-level NPC converters are divided into two types, the software and the hardware based methods. Many control techniques have been developed based on a modified version of the SVM by utilizing the redundant states of the 5-level space vector plane. The control of the redundant states in the SVM can affect the dc-link capacitor voltages and at the same time, the requested line-to-line voltage at the ac side is created. However, the effectiveness of purely software based control techniques is limited, since they cannot provide voltage balancing when the converter is operating with resistive power factor and high modulation index, as described in [129]. Therefore, some modifications and operational limitations



(a) (b)

Fig. 4.11: 5-Level NPC converter without dc-link balancing control: (a) the four dc-link capacitor voltages and (b) the L2L output voltages

should be applied on the NPC converter. Specifically, a voltage balancing method in a 5-level NPC converter used in active filters has been proposed in [72]. Similar modulation techniques have been proposed in [73, 74]; however, special design of the passive filter is required in [74] and the balanced operation can be accomplished only with capacitive or inductive power factor in [73]. An SVM-based control strategy for HVDC systems with two B2B-connected 5-level NPC converters has been presented in [75], where the capacitor voltages are balanced effectively. However, the modulation index of both NPC converters has to be the same and this is not possible in an electric drive system with a variable speed generator.

Hardware based voltage balancing techniques usually employ multistage dc/dc converters at the dc-link. These dc/dc converters are bidirectional buck-boost converters that control usually the voltage of the four capacitors in pairs. Various control techniques have been developed, such as in [83–85], which can provide effective voltage balancing in every operational condition of the electric drive. However, their main disadvantages are the increased installation cost and size of the system due to the additional hardware, as well as the reduced system efficiency because of the losses on the dc/dc converter. A balancing converter with reduced number of passive components was proposed in [86], but it requires more power switches and the control is more complicated than the previously mentioned topologies.

This sections presents three alternative ways of balancing the dc-link capacitor voltages:

- A purely **software-based balancing control** is presented in Subsection 4.5.1, where a new modified SVM algorithm is used for controlling the four capacitor voltages. This voltage control scheme is based on the quasi-3-level

control proposed for single NPC converters in [82].

- **Hardware-based voltage balancing** is shown in Subsection 4.5.2 where different types of control for the balancing converter are presented.
- A **combination of the hardware and software-based balancing** is analyzed in Subsection 4.5.3, which proposes a balancing converter with reduced number of components, utilizing also the SVM for balancing the voltages under certain operating conditions.

4.5.1 SVM-based DC-Link Voltage Balancing [2]

The multilevel SVM has got redundant states at many points of the space vector plane. These redundant states create the same L2L voltage at the ac side of the converter. However, each state has different effect on the capacitor voltages of the dc-side, which can be utilized to balance their voltages. The 5-level SVM diagram of Fig. 4.3 can be divided into three regions depending on the modulation index $\hat{m}$:

- Region 0 ($0 \leq \hat{m} < 0.25$): The modulation index at this region is low and the 5-level NPC converter generates 2-level L2L voltage at the ac side. There are four different redundant states that can control the voltage level of the four dc-link capacitors.
- Region I ($0.25 \leq \hat{m} < 0.5$): The 5-level NPC converter has 3-level L2L voltage at the ac side. As can be seen in Fig. 4.4, there are four different redundant states to be chosen for controlling the switches.
- Region II ($0.5 \leq \hat{m} \leq 1$): The converter has 4-level voltage between $0.5 \leq \hat{m} < 0.75$ and 5-level voltage for $\hat{m} \geq 0.75$. The redundant states in this region are not enough to ensure balanced condition with every load of the converter [129]. Therefore, the switching sequence of the SVM will be modified, as described later in this section.

The structure of an generator drive with two 5-level NPC converters and a PMSG is illustrated in Fig. 4.12. In this subsection a fully software-based voltage balancing technique is shown and the first step is to split the dc-link capacitors between the two converters, as shown in Fig. 4.12. The NPC converters are connected to each other only at the top and the bottom joint-points (points 5 and 1, respectively)

[2] More details can be found:
G. Mademlis and Y. Liu, "DC Link Voltage Balancing Technique Utilizing Space Vector Control in SiC-based Five-Level Back-to-Back-Connected NPC Converters", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

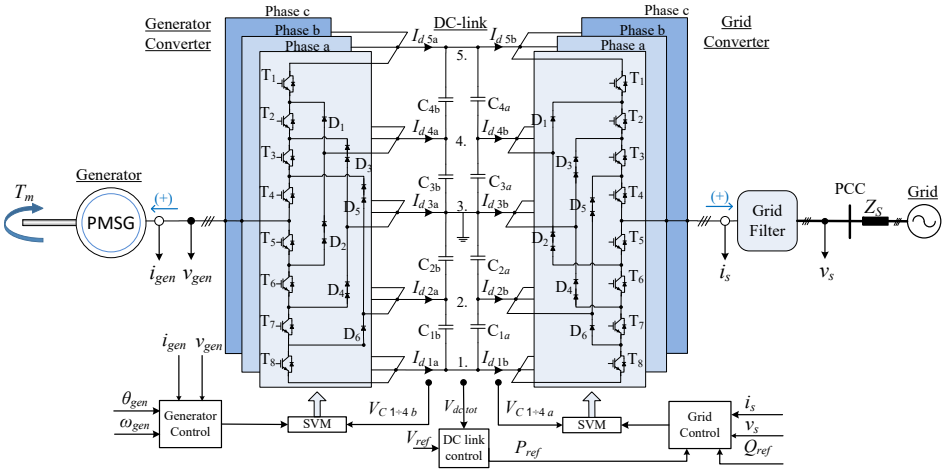


Fig. 4.12: Structure of a generator drive with two 5-level NPC converters connected B2B using modified SVM for voltage balancing of the dc-link

of the dc-link. The parallel connection of the two groups of capacitors (C_a and C_b) will ensure that they will have the same voltage. The middle point of the two converters can be connected to the ground or the neutral point of the system. The two converters operate at different modulation indexes and a common dc-link capacitor bank would have caused interferences that would have affected the balancing of the dc-link voltages. The configuration presented here decouples the generator-side converter of the drive from the grid-side converter allowing individual voltage balancing of the two groups C_a and C_b of the dc capacitors. The total dc-link voltage of the drive $V_{dc\ tot}$ is still controlled by the dc-link controller of the grid converter (Subsection 2.3.1).

The SVM diagram for a 5-level converter can be seen in Fig. 4.13(a) and the modulation strategy described in this section is identical for controlling both NPC converters of the electrical machine drive. The grid-side converter operates at an almost constant modulation index $\hat{m}_{grid} \leq 1$ in region II, whereas, the generator-side converter has variable modulation index $\hat{m}_{gen}$, since the speed and the voltage of the generator are changing. The variable v^* in Fig. 4.13 is the normalized reference voltage of the converter, as calculated by (4.10), and for a 5-level converter it varies from 0 to 4.

Voltage balancing algorithm for regions 0 & I: The switching states and the switching sequence of the SVM on the triangles of the space vector plane are indicated with arrows in Fig. 4.13(b). When the NPC converter operates

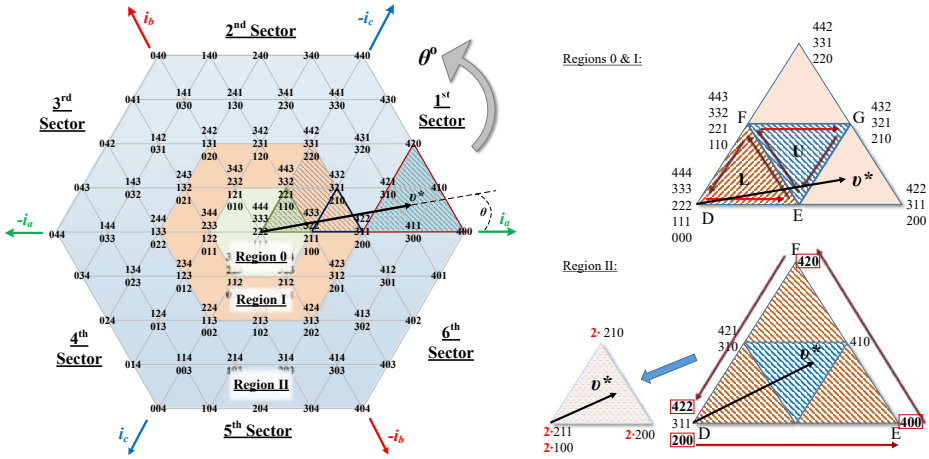


Fig. 4.13: Five-level SVM diagram: (a) space vector plane indicating the regions and sectors; (b) first sector of of the SVM plane indicating the switching sequence

in regions 0 and I, there are four available redundant switching states in each switching cycle that can easily be assigned to each of the four dc-link capacitors in order to charge them or discharge them whenever it is necessary.

An example is shown in Fig. 4.14, where the effect of the redundant states on the state of charge of the dc-link capacitors is demonstrated. The circuit diagram of the NPC converter is shown there, when the redundant states {100}/{211}/{322}/{433} from Sector 1 of the SVM plane are active. The switches which are active in each case are shown with thick black lines, while the inactive switches are marked with grey line. Specifically, when the instantaneous phase A current i_a is positive in Fig. 4.14(a), the state {100} discharges the capacitor C_1. Oppositely, if the current i_a is negative, the capacitor C_1 gets charged. Similarly, in Fig. 4.14(b) the state {211} discharges the capacitor C_2 when $i_a > 0$. In Fig. 4.14(c) the state {322} discharges the capacitor C_3 and in Fig. 4.14(d) the state {433} discharges the capacitor C_4. The L2L voltage at the ac side of the NPC converter is the same in all the four cases.

The three-phase current at the ac side of the NPC converters and the four capacitor voltages are measured and compared with each other in order to choose the correct redundant states from the space vector diagram. The sign of the ac current affects also the charging state of the dc-link capacitors, as has been shown in Fig. 4.14. The current that affects the capacitor voltages at each time instant depends on the

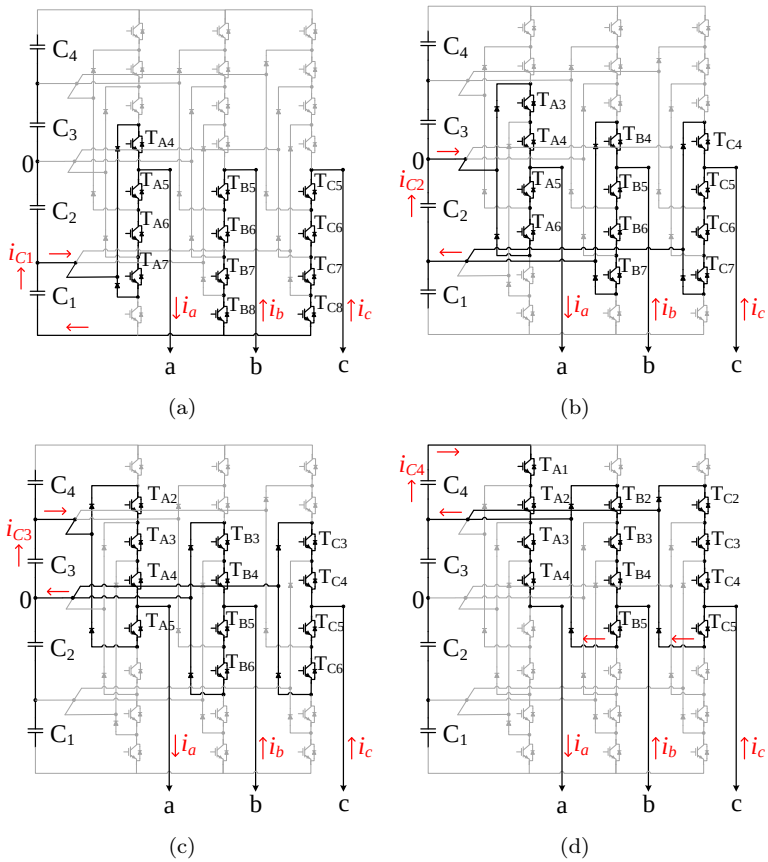


Fig. 4.14: Circuit diagram of the 5-level NPC converter when the switching state (a) {100}, (b) {211}, (c) {322} and (d) {433} is active

Table 4.4: Balancing Current [78]

Voltage angle θ	Balanc. current i_{bl}
(-π/6, π/6]	i_a
(π/6, π/2]	$-i_c$
(π/2, 5π/6]	i_b
(5π/6, 7π/6]	$-i_a$
(7π/6, 3π/2]	i_c
(3π/2, 11π/6]	$-i_b$

Table 4.5: Voltage balancing algorithm for region 0 (lower triangles)

i_{bl}	Condition	Switching sequence	t_1	t_2
>0	$V_{Cmax} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C3}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C4}$	$\{V_D + [3\ 3\ 3]; V_E + [3\ 3\ 3]; V_F + [3\ 3\ 3]; V_D + [4\ 4\ 4]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C3}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C4}$	$\{V_D + [3\ 3\ 3]; V_E + [3\ 3\ 3]; V_F + [3\ 3\ 3]; V_D + [4\ 4\ 4]\}$	$T_D/4$	$T_D/4$

* V_{Cmax}, V_{Cmin} are the maximum and minimum capacitor voltage, respectively

Table 4.6: Voltage balancing algorithm for region I (lower triangles) [72]

i_{bl}	Condition 1	Condition 2	Switching sequence	t_1	t_2
>0	$V_{Cmax1} = V_{C1}$	-	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C2}$	$V_{Cmax2} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
>0	$V_{Cmax1} = V_{C2}$	$V_{Cmax2} = V_{C3}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C3}$	$V_{Cmax2} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/6$	$T_D/3$
>0	$V_{Cmax1} = V_{C3}$	$V_{Cmax2} = V_{C4}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C4}$	-	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C1}$	-	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C2}$	$V_{Cmin2} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C2}$	$V_{Cmin2} = V_{C3}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C3}$	$V_{Cmin2} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C3}$	$V_{Cmin2} = V_{C4}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C4}$	-	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/6$	$T_D/3$

* V_{Cmax1}, V_{Cmax2} are the highest and the second highest capacitor voltage.
* V_{Cmin1}, V_{Cmin2} are the lowest and the second lowest capacitor voltage.

angle θ of the reference voltage v^* and the proper balancing current i_{bl} is chosen according to Table 4.4, as referenced from [78].

It was mentioned in (4.18) that the dwell times t_1 and t_2 are distributed among the redundant states V'_E for the upper and V'_D for the lower triangles. The standard way is to distribute them evenly, in order to minimize the switching losses of the converter and this method from now on will be called as "standard SVM" [127]. However, it is possible by varying these variables to control the capacitor voltages, as shown in Table 4.5 for the lower triangles of region 0 and in Table 4.6 for region

I (which is referenced from [72]). Similar methodology is followed for deriving the switching states for the upper triangles.

Voltage balancing algorithm for region II: The redundant states in the triangles of region II are not enough to keep all the capacitor voltages balanced, as can be seen in Fig. 4.13(b). More specifically, there are only two available redundant states on the D edge of the outer lower triangles in region II, the {300} and {411}, and three redundant states on the D edge of the inner lower triangles, the {200}, {311} and {422}.

One way to overcome this issue is to treat the 5-level NPC converter as if it was a 3-level converter. In this case, the capacitor voltages are controlled in pairs, $V_{C1} + V_{C2}$ and $V_{C3} + V_{C4}$, and the redundant states are enough to balance them effectively. This control strategy has been proposed in [72, 82] for single NPC converters and it is applied here for a drive with two B2B NPC converters. The switching states that generate current at the clamping points 2 and 4 of the NPC converters (Fig. 4.12) are not used in this SVM scheme (such as the states {300}, {311} and {411}) and the currents I_{d2a}, I_{d4a}, I_{d2b} and I_{d4b} are zero. Therefore, there is no voltage drift between the capacitor voltages of each pair. The resultant redundant states marked with a red box in Fig. 4.13(b) are utilized to keep the average current of the middle point 3 equal to zero, in order to balance the two pairs of the capacitor voltages. A more detailed view of the effect of these switching states on the charging state of the dc-link capacitors and the dc-side currents can be seen in Fig. 4.15.

The conversion from 5-level operation into 3-level operation is implemented by converting the large triangle on the bottom side of Fig. 4.13(b) into the equivalent triangle on the left side. Therefore, the reference voltage vector of the SVM in (4.10) is now modified as follows

$$v^{*'} = \frac{v^*}{2} = \frac{3\hat{V}^*_{ph}}{4V_{dc}} \tag{4.27}$$

The modified reference voltage $v^{*'}$ is now used in the rest of the equations (4.11)-(4.13) in order to calculate the space vectors and the dwell times. It can be seen in Fig. 4.13(b) that there are two available redundant states in each triangle, which are selected as shown in Table 4.7.

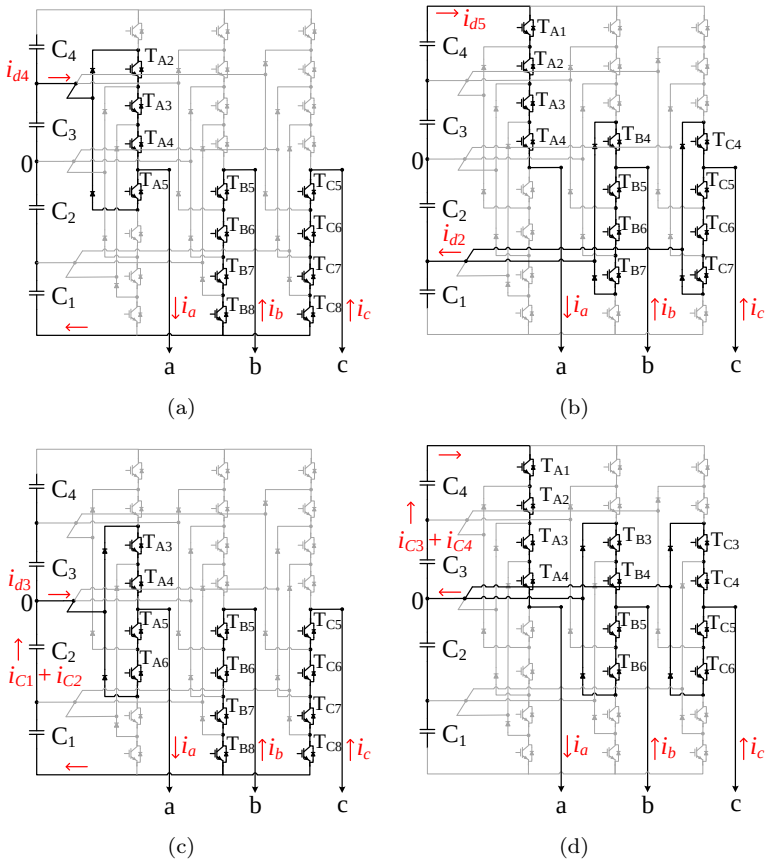
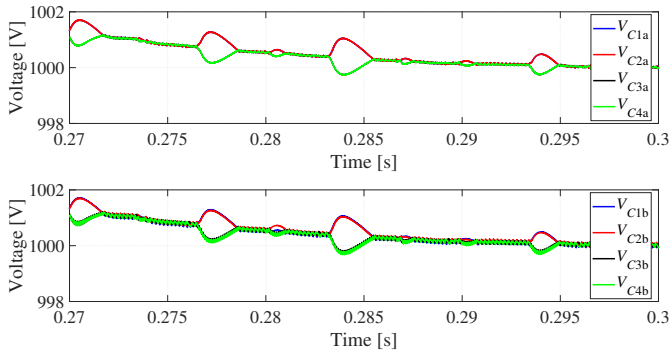


Fig. 4.15: Circuit diagram of the 5-level NPC converter when the following switching states are active: (a) {300}, (b) {411}, (c) {200} (⇒ the C_1 and C_2 are getting discharged) and (d) {422} (⇒ the C_3 and C_4 are getting discharged)

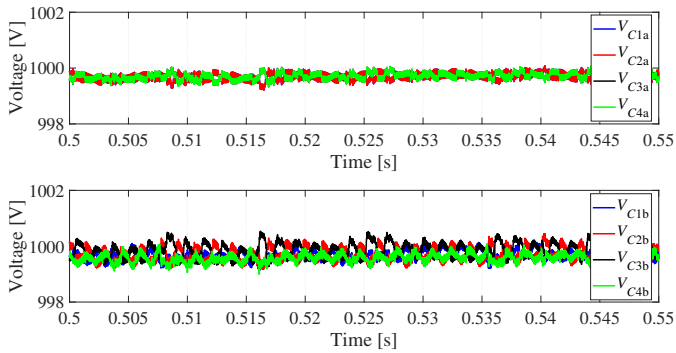
Table 4.7: Voltage balancing algorithm for region II (lower triangles)

i_{bl}	Condition	Switching sequence	t_1	t_2
>0	$V_{C1}+V_{C2}>V_{C3}+V_{C4}$	$2{\cdot}\{V_D;V_E;V_F;V_D+[1\ 1\ 1]\}$	$T_D/3$	$T_D/6$
>0	$V_{C1}+V_{C2}<V_{C3}+V_{C4}$	$2{\cdot}\{V_D;V_E;V_F;V_D+[1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
>0	$V_{C1}+V_{C2}>V_{C3}+V_{C4}$	$2{\cdot}\{V_D;V_E;V_F;V_D+[1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
>0	$V_{C1}+V_{C2}<V_{C3}+V_{C4}$	$2{\cdot}\{V_D;V_E;V_F;V_D+[1\ 1\ 1]\}$	$T_D/3$	$T_D/6$

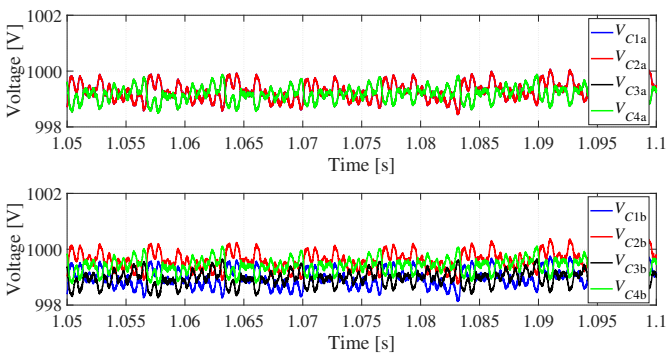
Simulation results: The generator drive of Fig. 4.12 has been simulated on Matlab/Simulink. The parameters of the system are the same with the ones for the 3-level drive reported in Table 4.1. The grid-side converter operates at



(a)



(b)



(c)

Fig. 4.16: Simulation results of the dc-link voltages when the generator-side 5-level NPC converter operates in (a) region 0, (b) region I and (c) region II of the SVM plane

constant modulation index which is at region II of the SVM diagram. However, many operating points of the generator are simulated in order to investigate all the three regions of the SVM for the generator-side converter. The same three operating points shown in Fig. 4.8(a) (500 rpm / 1.5 kW operating at region 0, 2000 rpm / 10.5 kW at region I and 4000 rpm / 46 kW at region II) have been simulated also here.

The reference voltage of each capacitor bank is equal to $4000/4 = 1000$ V. As can be seen in Fig. 4.16, the capacitor voltages remain balanced in all the operating regions of the system (the blue curve of V_{C1a} is overlapped by the red one of V_{C2a} and the black curve of V_{C3a} is overlapped by the green curve of V_{C4a}). The $V_{c1a} \div V_{c4a}$ are the capacitor voltages of the grid-side NPC converter and the $V_{c1b} \div V_{c4b}$ are at the generator-side. The voltages in Fig. 4.16(a) are slightly declining because the converter has not fully reached steady state yet.

The L2L voltage of the generator terminals can be seen in Fig. 4.17, where the 2-level voltage of region 0 is in Fig. 4.17(a) and the 3-level voltage of regions I and II is in Figs. 4.17(b)-(c). It can be seen here that although the generator-side converter operates with high modulation index in region II, the voltage still has 3

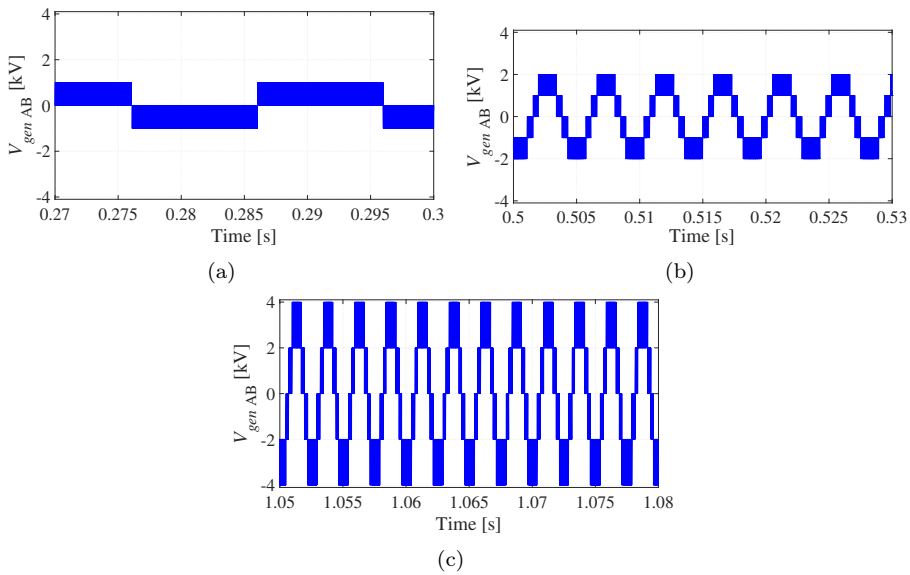


Fig. 4.17: Simulation results of the PMSG L2L voltage when the generator-side 5-level NPC converter operates in (a) region 0, (b) region I and (c) region II of the SVM plane

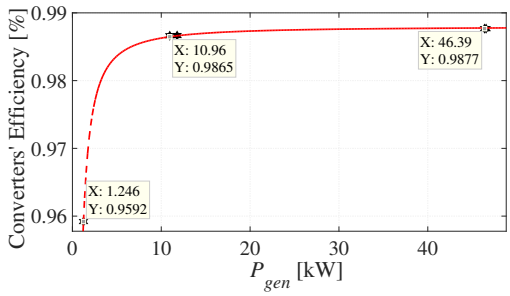


Fig. 4.18: Simulation results of the 5-level power converters' efficiency when SVM-based dc-link voltage balancing is used

levels, due to the voltage balancing algorithm described previously. This is also the main disadvantage of the SVM-based voltage balancing method, because the converters are not possible to generate 5-level voltage, although the voltage stress on each MOSFET is still equal to $V_{dc\ tot}/4$.

4.5.2 Hardware-based DC-Link Voltage Balancing [3]

The dc-link voltage balancing of NPC-based electric drives can be implemented with specially designed dc/dc converters placed in parallel to the dc-link, as described in [84, 88, 130, 131] and shown in Fig. 4.19. The dc/dc converters can be controlled with constant duty cycle in open-loop mode or they can have a closed loop control system. Both ways are described in this subsection.

Open-loop Control of the Balancing Converter

The dc/dc converter balances the capacitor voltages in pairs and, therefore, three stages are needed for a 5-level drive. Each converter stage consists of two power switches with antiparallel diode and an inductor. The maximum instantaneous voltage applied across each switch is equal to

$$v_{T_{bk}} = v_{Ck} + v_{C(k+1)} \tag{4.28}$$

which is two times the rated voltage of the switches of the NPC converter. As can been seen in Fig. 4.19, the dc/dc converter has been modelled here with two series-connected switches in each switch position. Instantaneous currents and

[3] More details can be found:
G. Mademlis and Y. Liu, "Feed-forward Control of Active Voltage Balancing Converter in Electric Drive with Five-Level NPC Converters", in *Proc. of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

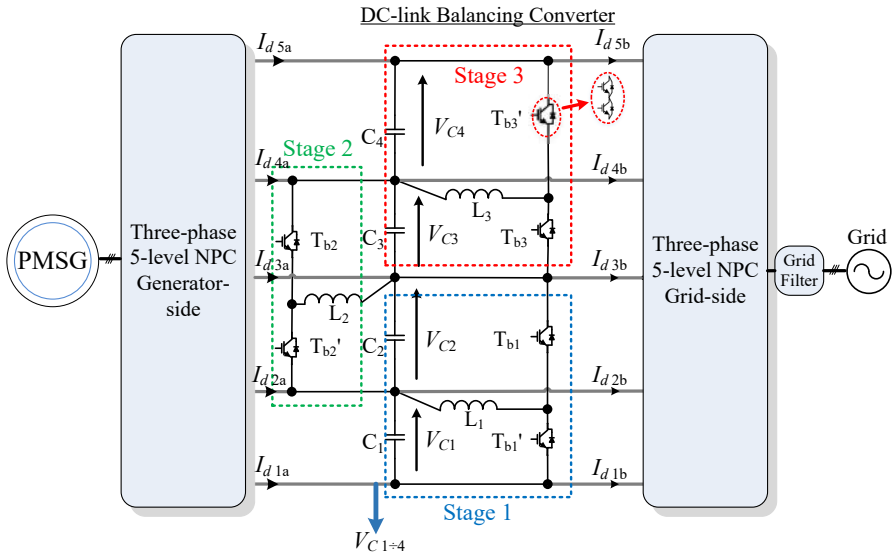


Fig. 4.19: Power circuit of the the dc/dc converter that balances the dc-link of a 5-level drive when only hardware balancing is used

voltages are symbolized here with lowercase letters (i and v respectively), while average quantities are shown with capital letters (I and V).

The two switches T_{bk} and $\mathrm{T}_{bk'}$ are complimentary to each other and the duty cycle of the k-stage power switch is defined as [132]

$$d'_k = 1 - d_k = \frac{v_{C(k+1)}}{v_{Ck} + v_{C(k+1)}} \tag{4.29}$$

When the capacitor voltages of that converter stage are equal

$$v_{Ck} = v_{C(k+1)} \overset{(4.29)}{\Rightarrow} d_k = d'_k = 0.5 \tag{4.30}$$

Therefore, by applying a constant duty cycle equal to 0.5 on all the power switches, the capacitor voltages will have the same voltage.

The operation of the converter can be explained by the graphs in Fig. 4.20. The first stage of the balancing converter is shown as an example and the other two stages operate similarly:

- When $V_{C1} > V_{C2}$ [Fig. 4.20(a)]
  1. the capacitor C_1 charges the inductor and the current flows through the switch T'_{b1} during half of the switching period.

2. During the other half period, the switch T'_{b1} is off and the T_{b1} is on. However, the current does not pass through the switch T_{b1} but through its antiparallel diode and the energy of the inductor is finally transferred to the capacitor C_2.

- When $V_{C1} < V_{C2}$ [Fig. 4.20(b)]

1. the capacitor C_2 charges the inductor and the current flows through the switch T_{b1} during half of the switching period.

2. During the other half period, the switch T_{b1} is off and the T'_{b1} is on. The current now passes through the antiparallel diode of T'_{b1} and the energy of the inductor is transferred to the capacitor C_1.

The average currents of the switches in Fig. 4.20 are defined as

$$\begin{aligned} I_{TB1} &= I_{L1} d_{b1} \\ I_{TB1'} &= I_{L1}(1 - d_{b1}) \end{aligned} \tag{4.31}$$

The following current and voltage equations exist in the circuit of Fig. 4.20

$$i_{TB1'} = i_{C1} + i_{d1a} - i_{d1b} \tag{4.32}$$

$$v_{TB1} = v_{C2} - v_{L1} \tag{4.33}$$

Since the antiparallel diodes of the switches conduct almost half of the time, it is recommended to use power MOSFETs for this converter, due to their ability to have reverse conduction current [133]. MOSFETs allow positive, as well as negative current to flow through their N-channel, when the gate-source voltage is positive. The N-channel of the MOSFET has lower conduction and switching

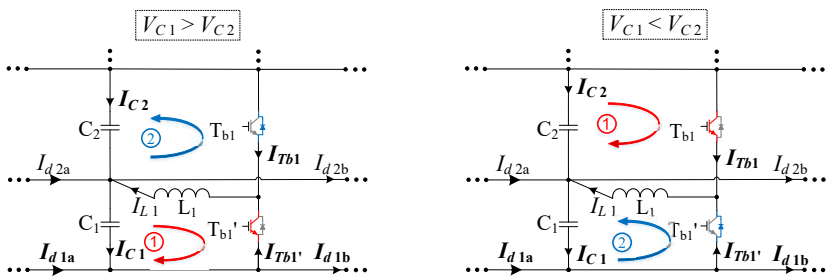


Fig. 4.20: Power circuit of the first stage of the dc-link balancing converter when (a) the capacitor C_2 and (b) when C_1 are being charged

losses compared to the antiparallel diode or the body diode. Therefore, by forcing the current to flow always through the switch even when it is negative, the losses of the balancing converter can be reduced.

It is very important to define a large enough dead-time between the two complimentary switches of each stage of the balancing converter. Otherwise, there is the danger of short-circuiting the dc-link capacitors and creating large current spikes which could destroy the switches.

The open-loop control of the balancing converter offers a simple and effective way of balancing the dc-link capacitor voltages of the 5-level drive. However, since there is no feedback of the actual voltage of the capacitors, there will be steady state error between the four voltages due to the losses and the voltage drop of the system. The most serious drawback of this control method is that there is no active control of the current that flows through the dc inductors and it is actually the resultant of the voltage difference between the capacitors. Therefore, in the case of a step-change of the load of the NPC converters, high current overshoots and oscillations are expected on the inductors, which cannot be suppressed, as seen in Fig. 4.21.

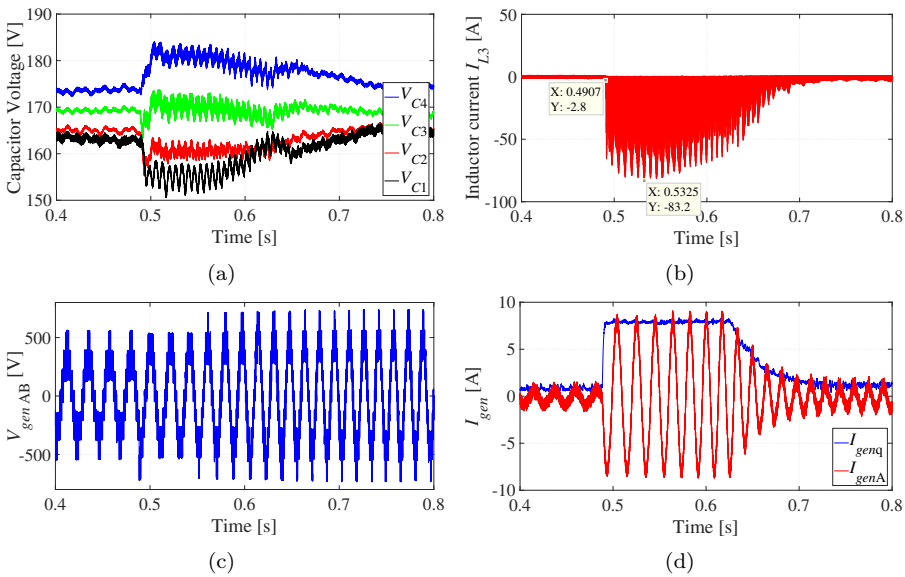


Fig. 4.21: Experimental results of the 5-level generator drive with a step-change of the PMSG speed from 450 rpm to 650 rpm when the dc-link is balanced with open-loop controlled balancing converter and with $V_{dc\ tot} = 670$ V

Experimental results of the generator drive, which will be presented in the next Chapter 5, are shown in Fig. 4.21. Specifically, the total dc-link voltage of the system $V_{dc\ tot}$ is 670 V and a step-change of the generator's reference speed is applied at 0.49 s. The current of the NPC converter I_{gen} increases due to the acceleration of the machine and the sudden current increase creates a larger drift of the capacitor voltages in Fig. 4.21(a). The current of the dc-inductors increases as well trying to eliminate the voltage drift and can reach high values as shown in Fig. 4.21(b) for the I_{L3} which has peak of 83 A. In that particular case, the I_{L3} became so high, because the inductor core got saturated.

Feedforward-based Closed-loop Control of the Balancing Converter

Each stage k of the balancing converter is regulated by separate controllers consisting of two cascaded control loops. The primary control loop is the voltage controller which creates the current reference that balances the two capacitor voltages. The secondary control loop is the current controller, which has as output the duty cycle d_k of the balancing converter. The voltage and current control loops can be made of PI controllers, as described in [84]. A feedforward-based control has been developed for the specific dc/dc converter in [131, 132] which uses only proportional controllers and offers faster dynamic response. It has been adapted in this thesis in order to be applied on the balancing converter of a generator drive with B2B-connected NPC converters.

The control structure of the dc/dc converter is presented in Fig. 4.22. The P_V and P_I are the proportional gains of the voltage and current controllers, respectively. The control of the first stage of the dc/dc converter can be described as follows.

The reference capacitor currents of each stage I_C^* are given by the error between the two capacitor voltages, after being amplified by the proportional gain of the voltage controller P_V. The reference current of the switch is calculated by using (4.6), with feed-forward of the dc-link currents. The reference inductor current is finally calculated with (4.5). The d_{b1} in (4.5) is the duty cycle of the switch T_{b1} during obtained from (4.29) during the previous sample period of the controller.

Input of the current controller is the error between the reference and actual inductor current. The current error is amplified by the gain P_I and becomes the reference average voltage of the inductor V_L^*. Then, the reference voltage of the switch V_{TB}^* is calculated by using (4.7). During steady state operation of the balancing converter, the average voltage of the inductor V_{L1} is equal to 0 and,

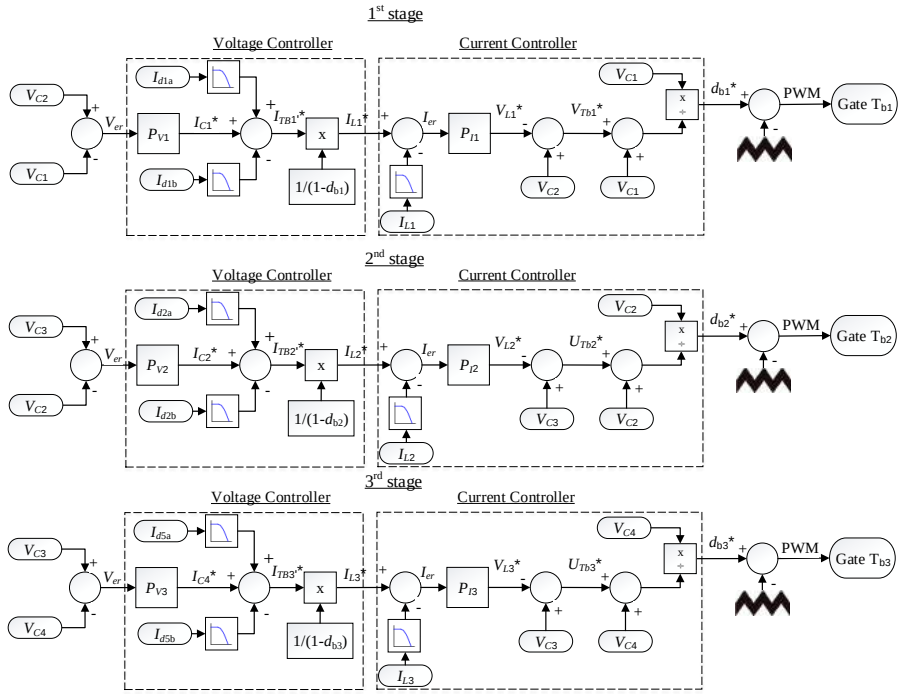


Fig. 4.22: Block diagram of the feed-forward control system of the dc-link balancing converter

therefore, the (4.7) becomes

$$V_{TB1} \approx V_{C2} \tag{4.34}$$

The reference duty cycle of switches in the fist stage of the converter are calculated with (4.29) and (4.34) as

$$d_{b1}^{*} \approx \frac{V_{C1}}{V_{TB1}^{*} + V_{C1}} \tag{4.35}$$

For the implementation of the feed-forward control scheme measurements of the four capacitor voltages, the three inductor currents (I_{L1}, I_{L2} and I_{L3}) and the dc-link currents (I_{d1a} up to I_{d5a} and I_{d1b} up to I_{d5b} shown in Fig. 4.12) are required. The current signals are filtered with LPF in order to suppress high order harmonics. It is possible to reduce the number of measurements by estimating the dc currents of the NPC converters. The dc currents are proportional to the ac output currents and the duty cycle of the NPC converters. A similar study has been conducted in [85] for single phase 5-level NPC converter. The dc-current estimation algorithm for a 5-level 3-phase NPC converter can be described as

follows for the phase a of the grid-side NPC converter

$$\begin{aligned}
I_{d5b_a} &= I_{S_\alpha}[d_{G1_\alpha} + d_{G2_\alpha} + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d4b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + d_{G2_\alpha} + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d3b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d2b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + (1 - d_{G3_\alpha}) + d_{G4_\alpha}] \\
I_{d1b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + (1 - d_{G3_\alpha}) + (1 - d_{G4_\alpha})]
\end{aligned} \tag{4.36}$$

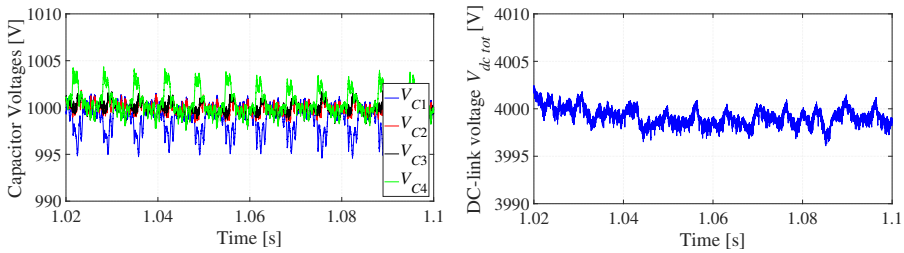
where I_{S_α} is the grid line current of phase α and d_{G1_α} is the duty cycle of the switch T_{G1} at the phase α of the grid-side NPC converter. The current estimation of the other two phases, b and c, can be obtained by similarly utilizing the (4.36). It should be noted that the currents given by (4.36) are the average values and not the instantaneous currents. The final values of the dc currents are calculated by summing the contributions of the three phases

$$\begin{aligned}
I_{d5b} &= I_{d5b_a} + I_{d5b_b} + I_{d5b_c} \\
I_{d4b} &= I_{d4b_a} + I_{d4b_b} + I_{d4b_c} \\
I_{d3b} &= I_{d3b_a} + I_{d3b_b} + I_{d3b_c} \\
I_{d2b} &= I_{d2b_a} + I_{d2b_b} + I_{d2b_c} \\
I_{d1b} &= I_{d1b_a} + I_{d1b_b} + I_{d1b_c}
\end{aligned} \tag{4.37}$$

The dc currents of the machine-side NPC converter I_{d1_a} up to I_{d5_a} are calculated similarly to equations (4.36) and (4.37) by using the machine-side line currents I_{gen} instead of the grid current I_S in (4.36).

The system shown in Fig. 4.19 has been simulated using Matlab/Simulink and the simulation results are shown in the following figures. The variation of the dc-link capacitor voltages is shown in Fig. 4.23(a) and they are balanced with small steady state error. This verifies the effectiveness of the control system described in the previous section. The total dc-link voltage is controlled by the grid-side converter and has mainly remained unaffected by the individual capacitor voltages, as can be seen in Fig. 4.23(b). The estimated and measured currents at the dc side of the grid NPC converter are presented in Fig. 4.24. The estimated currents are calculated by (4.36)-(4.37) and are the average values of the measured currents.

The harmonic analysis of the generator phase voltage and current is shown in Fig. 4.25, when the system has rated power (4000 rpm / 46 kW). The THD of the voltage is 34.7%, while the THD of the current is 0.6%. Both results are improved compared to the harmonic analysis of the 3-level drive in Fig. 4.9 that has shown a phase voltage THD equal to 54.7% and current THD of 1.8% .



(a) (b)

Fig. 4.23: Simulation results of (a) the dc-link capacitor voltages and (b) the total dc-link voltage when feedforward-based voltage balancing is used

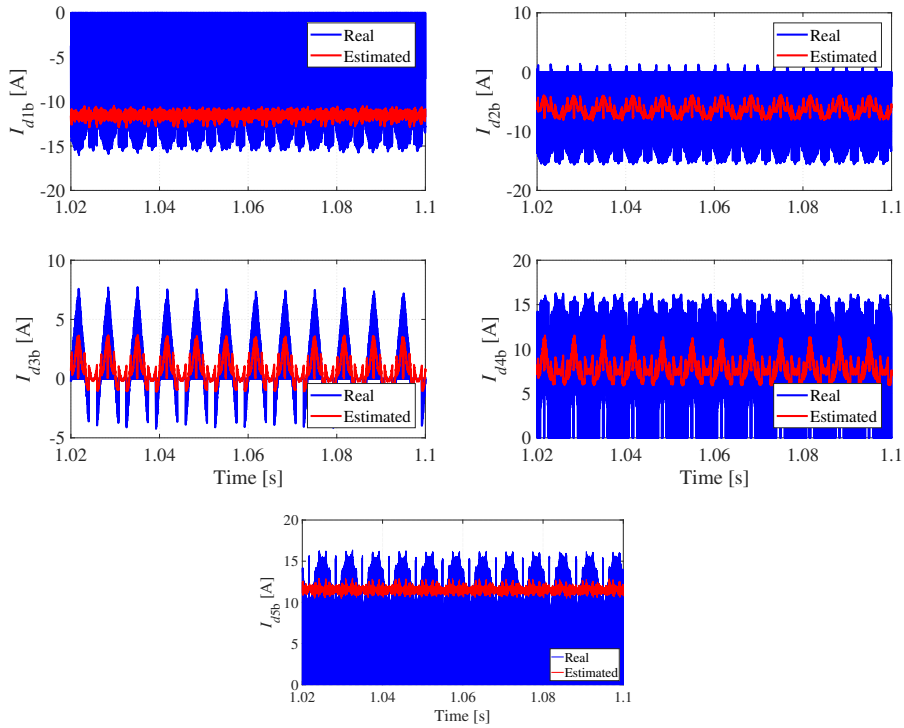
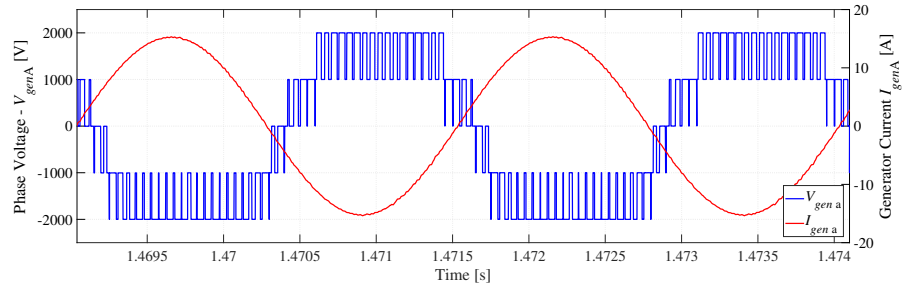
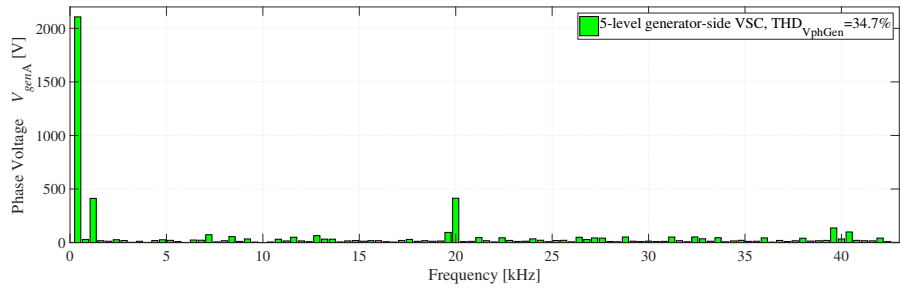


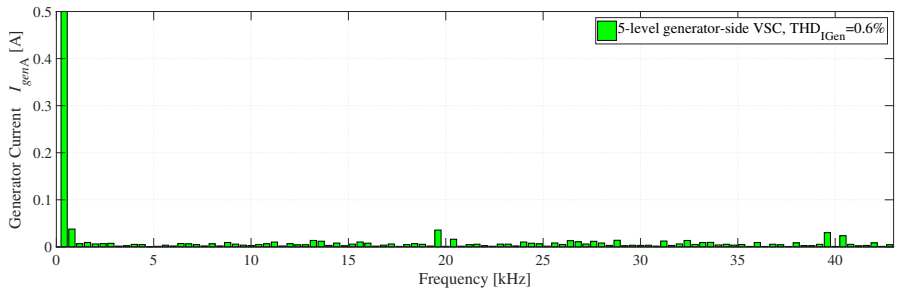
Fig. 4.24: Simulation results of the dc currents of the grid-side NPC converter at rated power of the generator (4000 rpm / 46 kW) when feedforward-based voltage balancing is used



(a)



(b)



(c)

Fig. 4.25: Simulation results of the 5-level generator voltage and current at rated power (4000 rpm / 46 kW) when hardware voltage balancing is used: (a) time-domain analysis and (b)-(c) FFT of the voltage and current

4.5.3 Combined Hardware and SVM-based Voltage Balancing

The SVM-based voltage balancing method works effectively when the 5-level NPC converters operate at regions 0 and I of the SVM plane and their modulation index is lower than 0.5. For higher modulation index, the SVM algorithms needs to be modified, as shown in Subsection 4.5.1, and the ac output voltage of the

NPC converters cannot have 5-level shape, since some specific switching states of the converter are not used. On the other hand, the hardware-based voltage balancing works effectively under every operating condition, but an additional dc/dc converter needs to be installed.

One solution would be to combine the advantages of both balancing techniques, the hardware- and the SVM-based, and build a new balancing converter with reduced number of components which will operate only when the redundant states of the NPC converter are not enough to keep the dc-link capacitors under control. The circuit diagram of the generator drive studied here is shown in Fig. 4.26. Compared to the diagram in Fig. 4.19, the balancing converter which is used here has only two stages, regulating the capacitors C_1-C_2 and C_3-C_4. The voltage balancing strategy depends on the modulation index. The grid side converter is operating at an almost constant modulation index $\hat{m}_{grid} \geq 0.5$, whereas, the generator side converter has variable modulation index $\hat{m}_{gen}$. The control structure of the whole electric drive system (an NPC converter connected to the grid and another converter at the generator side of the power plant) can be summarized in the flowchart of Fig. 4.27.

When the modulation index $\hat{m}_{gen}$ is at Regions 0 and I, the capacitor voltages

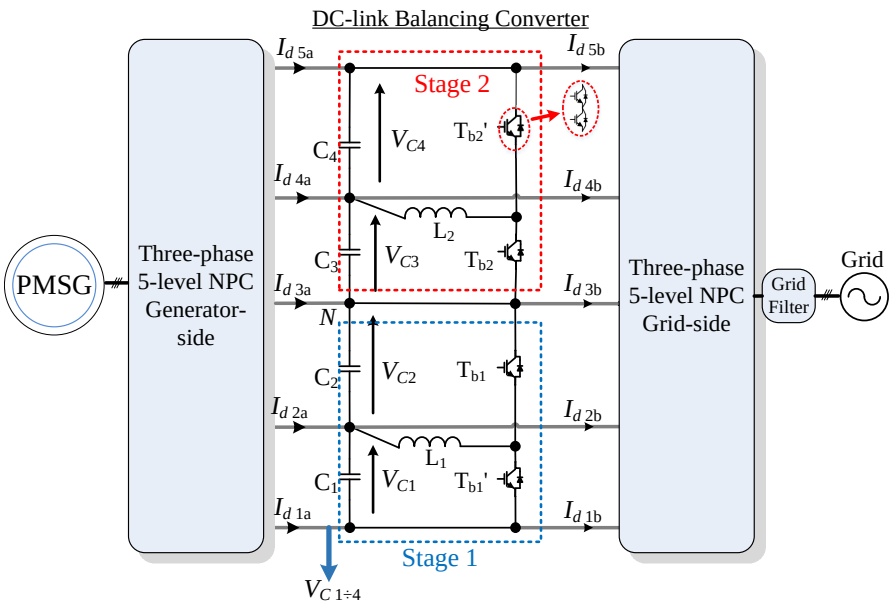


Fig. 4.26: Power circuit of a five-level generator drive with a 2-stage voltage balancing converter at the dc-link

are balanced only from the control system at the generator-side converter and the grid converter is controlled with conventional SVM [127]. The balancing converter does not need to operate during that time.

When the generator-side NPC converter is operating at the Region II of the space vector plane, the redundant states are not enough to control the capacitor voltages and at the same time to keep 5-level voltage. Therefore, the dc/dc converter at the dc-link is activated to keep the V_{C1} equal to V_{C2} and the V_{C3} equal to V_{C4}. The voltage potential at the middle of the dc-link N is controlled by injecting zero-sequence voltage as described in the next paragraph.

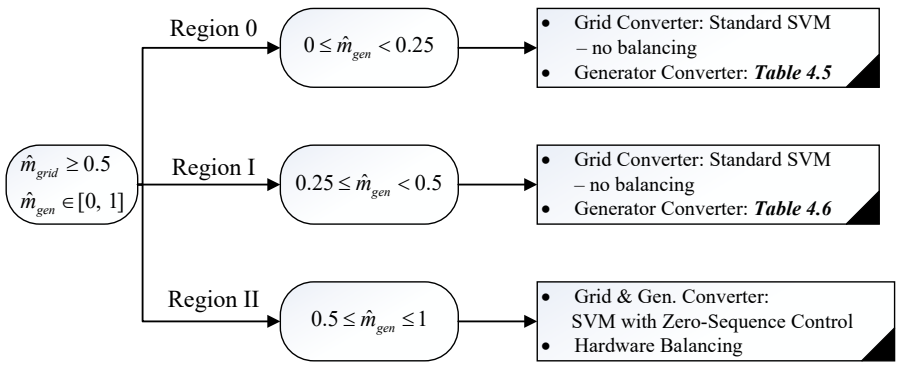


Fig. 4.27: Flowchart of the dc-link voltage balancing algorithm in a 5-level generator drive

Zero-sequence injection control (Region II)

The currents of the middle clamping point I_{d3a} and I_{d3b}, are controlled by the SVM-blocks of both NPC converters using zero-sequence injection. Zero-sequence injection is used in 3-level NPC converters for balancing their capacitor voltages in [102] and can also be applied here using a similar control structure. Fig. 4.28 shows the block diagram of the zero-sequence controller that has been implemented for both space vector modulators of the back-to-back connected NPC converters. Input of the zero-sequence injection controller is the voltage difference between the two upper capacitors C_3 and C_4 and the two lower capacitors C_1 and C_2. This error voltage contains 3rd harmonic components, which are filtered by a notch filter tuned at three times the fundamental frequency. The filtered signal is multiplied with the sign of the active power that goes through the NPC converter. Then, the error voltage goes through a PI controller and the output parameter k is the input of the SVM.

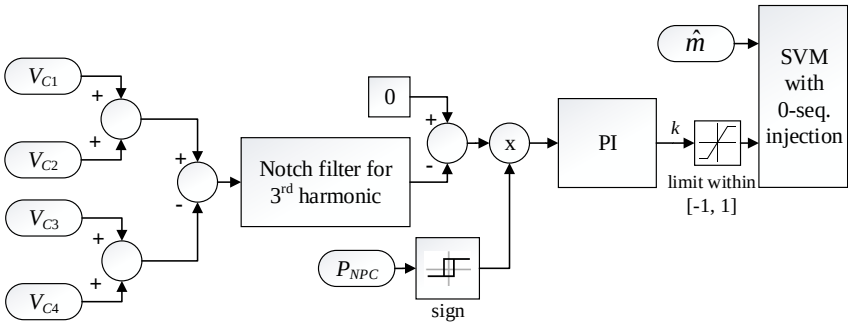
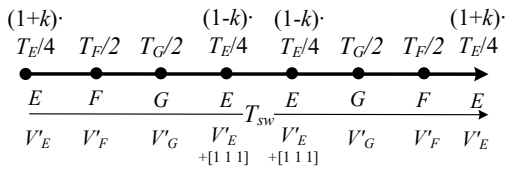


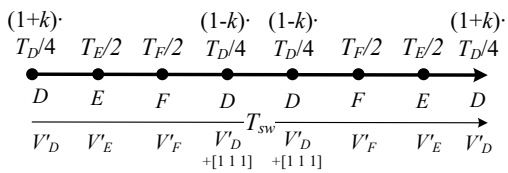
Fig. 4.28: Block diagram of the zero-sequence controller for regulating the potential at the middle point N of the dc-link

The switching sequence of the upper triangles from (4.14)-(4.15) for both NPC converters changes to



(4.38)

and for the lower triangles



(4.39)

The combination of software and hardware control techniques presented here ensures that the additional dc/dc converter is used only when the redundant states of the SVM are not enough for effective dc capacitor voltage balancing. Therefore, the efficiency of the whole system is improved compared to the fully hardware-based balancing of Subsection 4.5.2. Also, the number of components needed for the dc/dc converter has been reduced, because zero-sequence injection is used for controlling the middle point current instead of using a 3rd stage of the balancing converter. Four- and five-level ac voltage is also created when the NPC converters operate at high modulation index, without the limitations imposed in Subsection 4.5.1, where the voltage has maximum three levels.

Simulation results of this voltage balancing technique have been presented in [4] and are not repeated here.

4.6 Summary

This chapter has presented the design process and the simulation analysis of 3-level and 5-level generator drives. Drives with 5-level converters can have operating voltage up to 4 times higher than the systems with 2LCs, without using series-connected power switches. A further advantage of the 5-level converters is the decrease of the voltage and current harmonics at their ac side, compared to converters with less number of levels, as shown by the FFT analysis in Figs. 4.9 and 4.25. Simulation results of a 3-level drive have shown that the generator current and phase voltage THD are 1.8% and 54.7%, respectively. For a drive system with 5-level converters, the THD of the current decreases to 0.6% and the THD of the phase voltage to 34.7%, when the same operating conditions are simulated. The reduction in harmonics that are observed in multilevel drives has also a positive impact on the performance of the electrical machine, as presented in [5] where the torque ripple and core losses of a PMSM were drastically reduced by using multilevel converters.

The voltage drift of the dc-link capacitors is a serious problem in electric drives with 5-level NPC converters that can be solved by various voltage balancing strategies. Three effective voltage balancing methods have been described in Section 4.5 providing also simulation results on a sample 50 kW generator drive for each of these methods. Each technique has its own advantages and disadvantages, as described below.

Firstly, it has been shown that the redundant states on the 5-level space vector plane of the NPC converter's modulator can be utilized to balance the four dc-link voltages. This method is an extension of a similar control technique that is also applied on the 3-level NPC converters, where zero sequence voltage is used to control the two capacitor voltages of that topology. However, contrarily to the 3-level converter, the redundant states are not enough to control all the four capacitor voltages when the 5-level drive operates at the outer regions of the space

[4] G. Mademlis, Y. Liu, and N. Saadat, "Combined voltage balancing techniques of the DC link in five-level medium voltage NPC back-to-back converters for offshore renewable generation", in *Proc. 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1-P.10.

[5] G. Mademlis, Y. Liu, and J. Zhao, "Comparative Study of the Torque Ripple and Iron Losses of a Permanent Magnet Synchronous Generator Driven by Multilevel Converters," in *Proc. IEEE XIII International Conference on Electrical Machines (ICEM)*, 2018, pp. 1406–1412.

vector plane. One way to overcome this problem, is to switch the converter in 3-level mode avoiding the use of some switching states, as shown in Subsection 4.5.1. The capacitor voltages are kept balanced in that case, but the ac voltage of the converter has maximum 3-levels, which results to increased harmonics at the ac side. The main advantage of this balancing technique is that it does not require any additional hardware for the control of the dc-link voltages, since the suitable selection of the redundant states of the converter regulates them.

Another way of balancing the dc-link voltages is the use of dedicated dc/dc converters. This method is the most expensive, since it requires the use of an additional converter and, thus, the cost, losses and complexity of the system are increased. The dc/dc converter can either be controlled open-loop by just switching with constant duty cycle without any feedback of the capacitor voltages or a more complicated feedforward-based closed-loop control system can be used. The open-loop control has the simplest structure, while the closed-loop controller has better dynamic performance and balances the capacitor voltages with smaller steady state error. The SVM of the NPC converters is not utilized in this case for the dc-link control, which makes the redundant states of the NPC converters available to be used in other control strategies, such as in loss and noise reduction of the ac/dc converter [134].

The third method proposed in this thesis is the combination of the two previous voltage balancing techniques. The SVM-based voltage balancing method is clearly advantageous when the converter operates with low modulation index, while it should be avoided when high modulation index is used. The dc/dc balancing converter can be activated in this case, while in all the other cases it can remain idle. Zero-sequence injection can also be used to limit the number of components of the balancing converter, as described in Subsection 4.5.3. This method is the most complicated out of the three previously mentioned, since it includes the control for the additional dc/dc converter as well as the optimal selection of the redundant states of the modified SVM. However, the 5-level drive can operate without any limitation, unlike in the first method. Also, the additional hardware needed is less compared to the second method.

The advantages and disadvantages of the voltage balancing techniques that have been discussed previously are summarized in the following Table 4.8. The comparison of the system complexity in the table refers to the complexity of the control in each voltage balancing scheme. The third method has the most advantages, because it balances successfully the dc-link capacitor voltages, without increasing considerably the cost of the system, while having higher complexity in the control

and the hardware design. However, the optimal choice of the voltage balancing technique depends on the exact needs of the application where the drive is intended to be used.

Table 4.8: Summary of DC-link Voltage Balancing Techniques

Balancing method	Complexity	Cost	AC Harmonics
SVM-based (Subsection 4.5.1)	↗	0	↗ (3-level voltage)
Hardware-based with open-loop control (Subsection 4.5.2)	0	↗↗	0
Hardware-based with closed-loop control (Subsection 4.5.2)	↗	↗↗	0
Combination of SVM and hardware (Subsection 4.5.3)	↗↗	↗	0

Chapter 5

Design and Testing of Medium Voltage PMSM Drive

5.1 System Overview

The prototype power conversion system developed during this study has two identical 5-level NPC converters placed at the generator- and the grid-side of the drive and are responsible for controlling the generator and for the synchronization to the grid, respectively (Fig. 5.1). There is a third converter connected in parallel with the dc-link of the whole structure, which is responsible for balancing the voltages of the dc-link capacitors. The positive flow of energy and the positive d-, q-currents at the output of the converters are marked with blue arrows on the schematic. The connections at the ac side of the converters between the PMSG and the generator-side VSC and between the transformer and the grid-side VSC are implemented using 3.3-4.2 kV litz-wire cables from Nexans with conductor cross section 16 mm^2 (product code 10148758).

The switches of the power converters are controlled by gate drivers, which send suitable signals to the gate of the switches, when they need to turn on and off. The gate drivers receive these control signals from an MCU, as seen in Fig. 5.1. The MCU and the gate drivers are electrically isolated from each other and this isolation is implemented by transferring the PWM signals to the gate drivers through fibre optic cables.

Measurements of the currents and voltages at various points of the power conversion

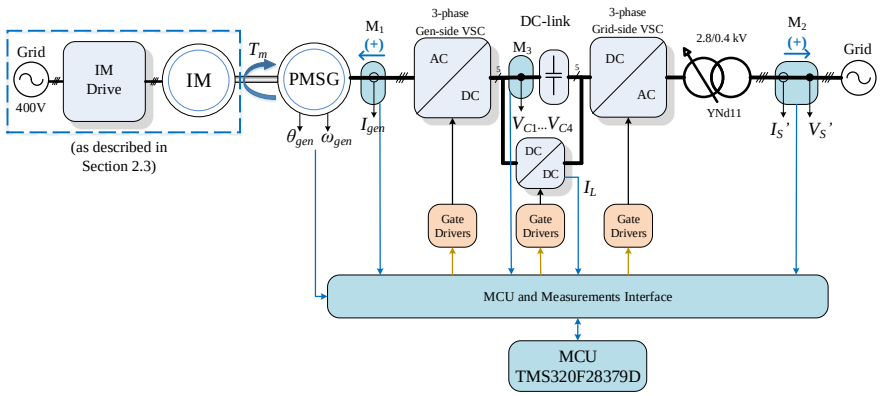


Fig. 5.1: Schematic of the prototype medium voltage power conversion system including the power converters and the control boards

system are needed in order to control the converters. The generator and grid currents and voltages are measured with the measurement blocks M_1 and M_2. The voltage of the capacitors at the dc-link is also measured with another measurement block M_3. The measured signal is sent to the MCU through the "MCU and Measurements Interface". Three MCU boards from Texas Instruments with product code TMS320F28379D are used to control the two NPC converters and the dc-link balancing converter.

The following Section 5.2 describes the design process of the power converters and the measurement devices and Section 5.3 presents experimental results of the multilevel generator drive.

5.2 Prototype PMSG Drive Design

The design parameters of the prototype low-scaled power conversion system is given in Table 5.1. The system described here is a low-power-scaled version, but with higher operating voltage, of the 500 kW TUSK system shown in Table 3.1. The prototype presented in this chapter has been used in the thesis as a proof of concept for the proposed multilevel generator drive and for verifying the developed control strategies described previously in Chapter 4. The dimensions and the power density of the converters have not been optimized in order to allow easier accessibility and measurements with the oscilloscope.

SiC Power switches are used for the converters of the prototype. SiC has advantageous performance in terms of lower switching losses and higher operating

Table 5.1: Parameters of the developed multilevel power conversion system

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Maximum dc-link voltage V_{dctot}	4	kV
DC-link capacitance	295	μF
Inductors of the balancing conv. L_1, L_2, L_3	4	mH
Maximum ac L2L voltage (rms)	2.8	kV
Phase current (rms)	10.31	A
Switching frequency f_{sw}	20	kHz

temperatures compared to the Si power switches [135, 136]. Thus, SiC switches allow the construction of more compact converters due to the higher switching frequency and the resultant decrease of the grid filter size, as well as lower cost for cooling, because of the lower switching losses and higher allowed temperatures. The main disadvantage of these switches is that they have at the moment higher purchase cost compared to the Si IGBTs and MOSFETs. However, their cost is constantly declining, as the SiC technology becomes more mature.

Suitable application regions for each of the available semiconductor devices are shown in Fig. 5.2, namely SiC power switches can substitute IGBTs in applications with power between 1-500 kW and switching frequency higher than 10 kHz. In applications with even higher power the power switches made of Si are expected to remain dominant in the future. The graph of Fig. 5.2 was presented by Infineon

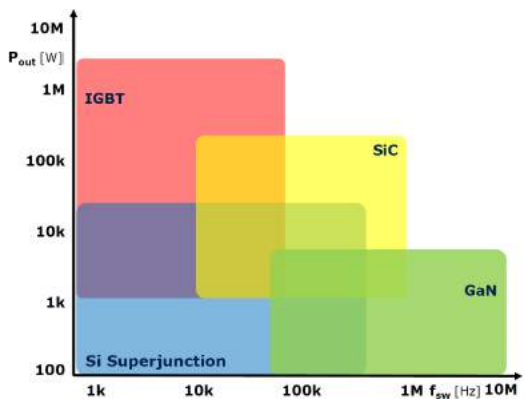


Fig. 5.2: Recommended application ranges for Si, SiC and GaN devices [ISiCPEAW 2016 - presented by Infineon Technologies AG 2016]

(a) (b)

Fig. 5.3: (a) SiC MOSFET SCH2080KE and (b) SiC schottky diode C3D10170H

Technologies AG at the ISiCPEAW workshop in 2016. A proof-of-concept 50 kW inverter of Wolfspeed [137] shows that SiC power switches can reduce the total system cost by 15% compared to Si power switches, if the cost of cooling, filters, etc. is considered. More specifically, although the cost of the power devices is much higher compared to a Si-based system, the cost and size of the grid filter inductors and of the cooling system can be reduced in a SiC converter. This is particularly useful in the case of the undersea kite, since a size reduction of the passive filter at the ac side of the power conversion system is highly beneficial.

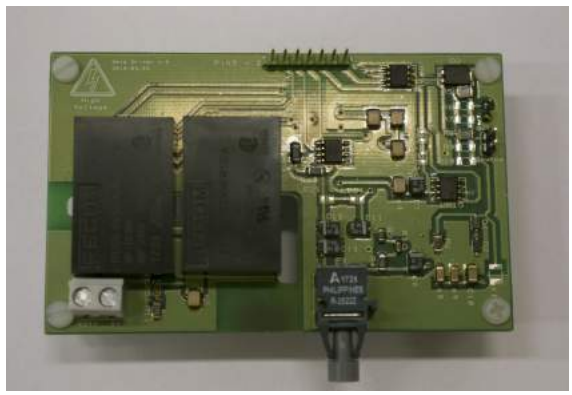
The SiC MOSFETs SCH2080KE of ROHM [Fig. 5.3(a)] are used for the lab prototype of the converters, which have been modelled in the simulation results of Chapter 4. These switches have maximum drain-source voltage 1200 V and maximum continuous drain current 40 A (at 25°C) / 28 A (at 100°C). The clamping diodes of the NPC inverters are the C3D10170H from CREE [Fig. 5.3(b)] with 1700V maximum reverse voltage and 29 A (at 25°C) / 14.4 A (at 135°C) maximum continuous current.

Voltage overshoots caused by parasitic capacitance and inductance between the switching devices are a serious problem, when designing a power converter. Therefore, the power switches should not operate very close to their absolute rated voltage, but a safety limit of approximately 20% or more should be kept. The exact number of the safety margin depends eventually on the design of the power conversion system. The nominal dc-link voltage of the power conversion system is designed to be equal to 4 kV and, therefore, each switch of the converters will have to withstand 1 kV. In this case, a safety margin of 200 V has been chosen between the nominal operating conditions and the maximum voltage of the switches.

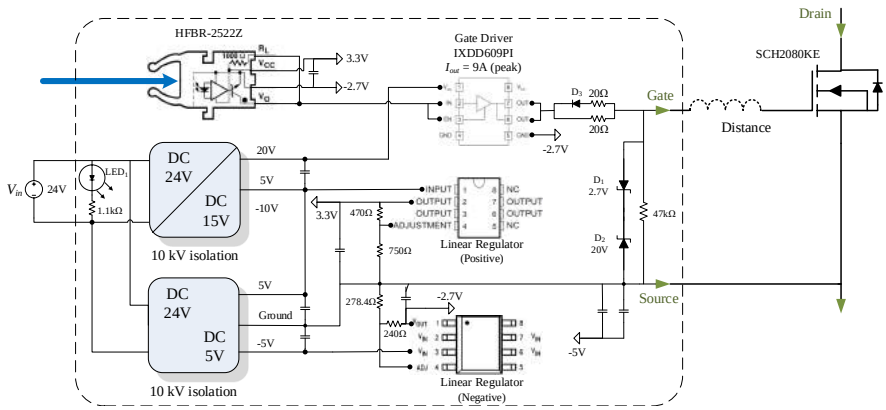
5.2.1 SiC Gate Driver Design

The gate driver is responsible for transferring the control signal from the output of the ePWM peripheral of the MCU to the gate of the MOSFETs. They also provide electrical isolation between the high voltage potential of the switch and the low voltage potential of the microcontroller. The SCH2080KE MOSFET requires a gate-source voltage of 20 V in order for the switch to turn on and -2.7 V for the switch to turn off.

Fig. 5.4(b) shows the circuit diagram of the gate driver PCB. Two separate dc/dc converters are used for each gate driver board which provide ±15 V and ±5 V power supplies. The primary side of these converters receives 24 V input voltage. The secondary side of the dc/dc converters is floating at the voltage potential of



(a)



(b)

Fig. 5.4: (a) Picture and (b) schematic of the gate driver for the SCH2080 SiC MOSFET

the source of the MOSFET, while the primary side is at the voltage potential of the MCU. Therefore, dc/dc converters with reinforced isolation voltage of 10kV need to be used.

Linear regulators modify the output voltage of the dc/dc converters in order to produce -2.7 V and 3.3 V in respect to the ground, which is the source of the MOSFET. The gate resistor is equal to 20 Ω for turning on the switch and 10 Ω for turning off. Lower resistance is used for the turn-off operation in order to increase the speed of the gate driver. This is implemented by using a schottky antiparallel diode D_3 in parallel to the turn-on resistor [138]. Zener diodes D_1 and D_2 and a large resistor of 47 kΩ are used between the gate and source outputs of the gate driver board in order to protect it from overvoltages.

The distance between the outputs of the gate driver IC up to the gate and source of the switch is very critical for the optimal design of both the gate driver and the inverter PCB. Parasitic inductance occurs due to the loop between the gate driver output and the ground return traces as can be seen on the right side of Fig. 5.4(b), which can create voltage ringing in the gate drive waveform [138]. The voltage ringing is defined as unwanted oscillations during a step change of a voltage signal, because the parasitic inductance does not allow the current flowing on that loop of the system to change rapidly its value. Ringing on the power switch can cause unwanted turn-on and turn-off of the switch, which creates additional switching losses and could eventually destroy the switch if these voltage oscillations surpass its maximum voltage ratings. The longer this distance is, the larger the parasitic inductance becomes and more severe oscillations can occur on the power switch. The voltage oscillations due to the ringing usually have high frequency at MHz level, which create EMI noise that can easily interfere with other sensitive devices of the system, such as measurement devices and the MCU.

In order to decrease these oscillations, the following solutions are available to the designer of the PCBs. First, the distance between the gate driver and the power switch has to be minimized. A wider trace for the gate signal can also limit the parasitic inductance. Surface mounted devices (SMD) are also preferable compared to through-hole devices, since they can deal better with EMI and their reduced physical dimensions can limit the parasitic inductance and allow closer placement of the components [139]. In case the problem cannot be solved, capacitors have to be placed close to the gate pin of the switch and on the gate driver PCB in order to filter out the unwanted oscillations. The filter frequency can be optimized by placing multiple capacitors of different capacitance value, which have different resonant frequency.

Fig. 5.5(a) shows the experimental measurements of the gate to source voltage V_{GS} at the terminals of the switch with switching frequency of 5 kHz. The switching frequency of the prototype converters used in the experimental results in later sections is equal to 20 kHz. A closer look of the V_{GS} voltage can be seen in Figs. 5.5(b)-(c), which validate that the voltage created by the gate driver is within the recommended range mentioned in the MOSFET datasheet [140], namely maximum $V_{GSS-surge} \in [-10, 26]$ V.

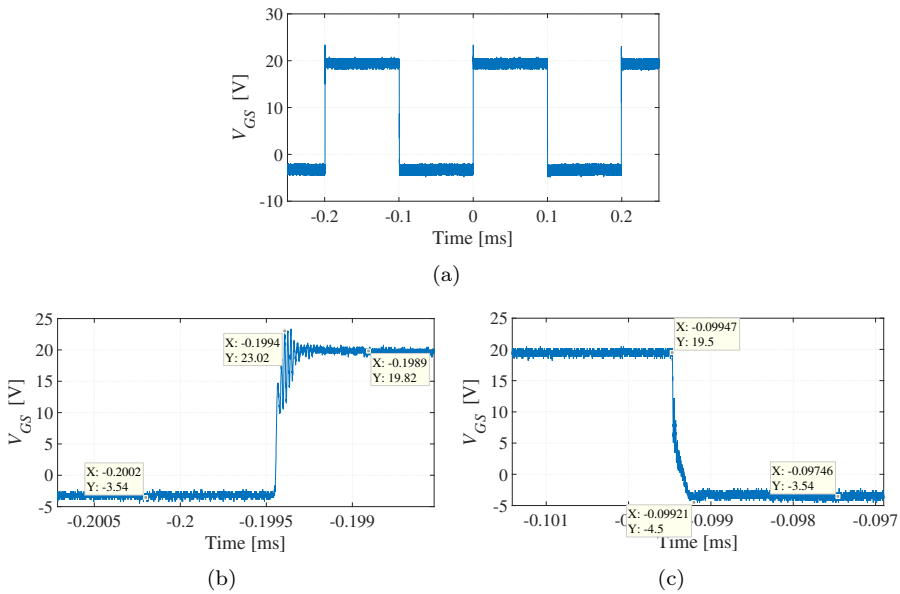


Fig. 5.5: Experimental results of (a) the gate-source voltage of SCH2080KE MOSFET with switching frequency of 5 kHz; zoomed-in gate-source voltage (b) during turn-on and (c) turn-off transient

5.2.2 NPC Converter Board

The developed prototype of the NPC inverter is shown in Fig. 5.7. The inverter has nominal voltage higher than 1.5 kV peak voltage and, therefore, some special rules are followed during the design process. The prototype PCBs have been built based on the design guidelines described in [141].

The first thing that needs to be considered is the proper substrate material for the PCB, especially if double-layer PCBs are used (Fig. 5.6). PCBs with more than two layers are not recommended for high power converters, since they can become fragile due to the large thickness and it is also difficult to dissipate the

heat from the inner copper layers [142]. The substrate of the PCB needs to be able to handle the differential voltage between the top and the bottom copper layer. The substrate (prepreg) used on the developed prototype by the manufacturer of the PCBs is the FR-370HR with dielectric strength of 54 kV/mm [143].

Proper design of the traces on the PCB is very important in order to avoid Corona discharges or a direct arc. Sharp edges and corners on the copper traces should be avoided, because high electric field occurs there, which can initiate Corona. Smooth and round curves should be used wherever possible for the traces and the pads of the PCB [141]. Also, the minimum creepage distances should be kept between the components placed on the PCB and between the traces of the same layer. A rule of thumb of 100 V/mm for the creepage distance between the components has been considered for the design of the prototype.

Due to the high operating voltage of the prototype, longer distances are, therefore, required between the power switches of the converters and the dc-link capacitors of the system. Since the dc-link capacitors operate as a quite stiff voltage source, the parasitic inductance of the PCB traces can cause high frequency voltage oscillations of the switches, which is called ringing. Proper design of the traces in the PCB is very important, as mentioned also in Subsection 5.2.1. The parasitic inductance of the circuit can be reduced in order to limit the ringing by increasing the width of the traces of the PCB as much as possible. Also, the drain and source traces of the power MOSFETs as well as the anode and cathode traces of the schottky diodes should be placed directly over each other, which reduces the parasitic impedance [139]. Resistor-capacitor (RC) snubber circuits are also installed in parallel to each MOSFET and diode of the NPC converter, as can be seen in Fig. 5.7(a). The RC snubber consists of a small capacitor and a small resistor connected in series that suppress the rapid rise in voltage (dV/dt) of the switching device to a value that will not trigger ringing.

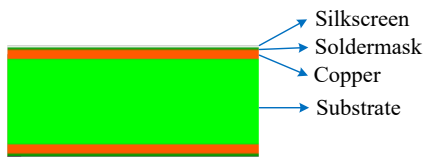
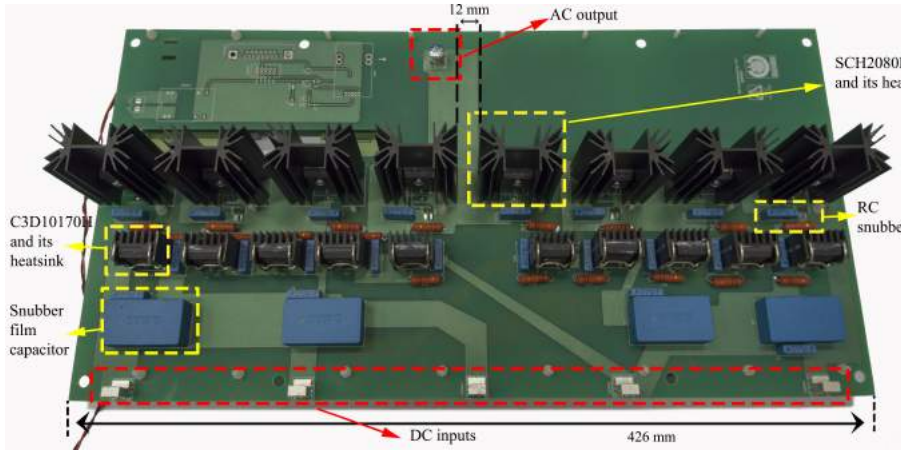


Fig. 5.6: Composition of a two-layer PCB



(a)

(b)

Fig. 5.7: PCB of a single phase 5-level NPC converter with the gate drives connected to the switch terminals: (a) top and (b) bottom view

5.2.3 DC-Link Board

Film capacitors with part number 947D591K132DJRSN are chosen for the prototype power conversion system, which have rated voltage of 1.3 kV and capacitance of 590 μF. Film capacitors are more bulky and expensive compared to electrolytic ones. However, they can handle higher voltage and are, therefore, more commonly used in high voltage drives. Eight capacitors (in two parallel-connected groups of

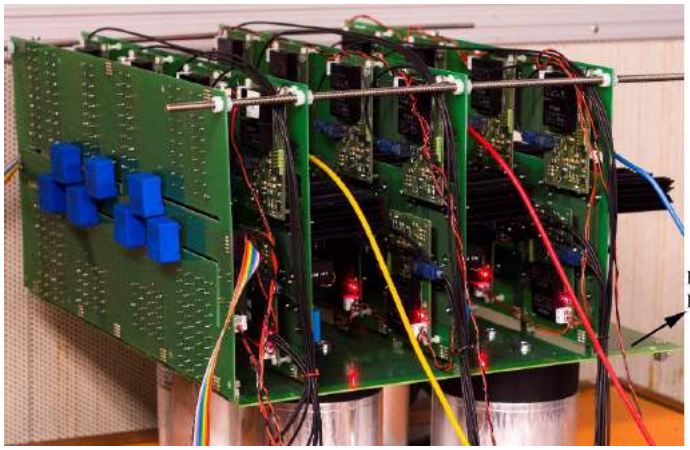


Fig. 5.8: Laboratory prototype of the three-phase 5-level NPC inverter

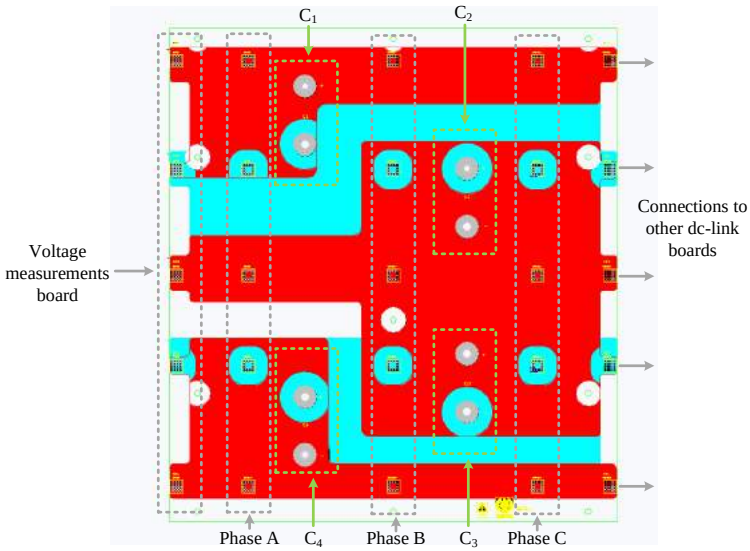


Fig. 5.9: Schematic of the dc-link PCB design, red→top copper layer and blue→bottom copper layer

4 capacitors) are installed in total on the PCBs of the power converters through a special board which is shown in Figs. 5.8-5.9. Therefore, the equivalent capacitance of the dc-link becomes $590 \cdot \frac{2}{4} = 295$ μF. The rated current of each capacitor is 79 A(rms), which is enough for the specific project.

This dc-link PCB serves as the base for connecting the three-phase NPC inverter and the balancing converter to the dc-link of the system. As can be seen in Fig.

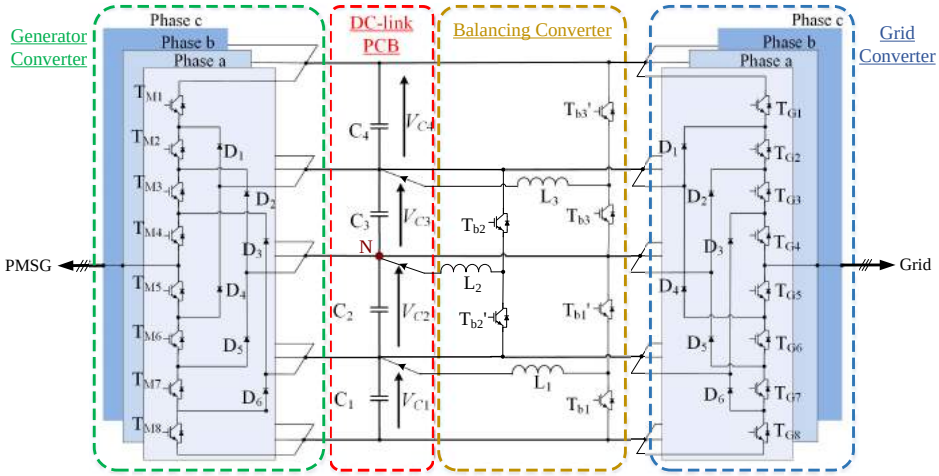


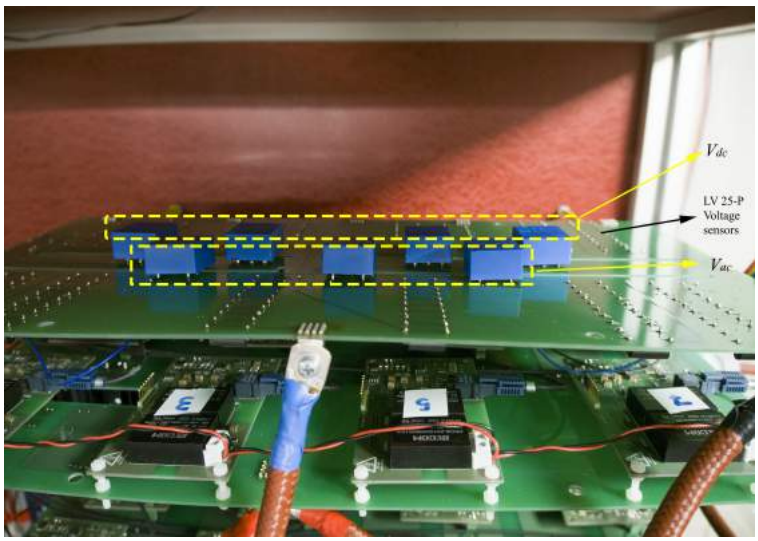
Fig. 5.10: Schematic diagram of the whole prototype power conversion system

5.9, this board has enough connectors for 3 converter boards and 4 capacitors. Therefore, three of these PCB are needed to accommodate the two B2B-connected NPC converters and the balancing dc/dc converter [Fig. 5.18(b)]. Fig. 5.10 shows also the schematic diagram of the whole power conversion system, which is the same with the schematic of the simulated system in Fig. 4.19.

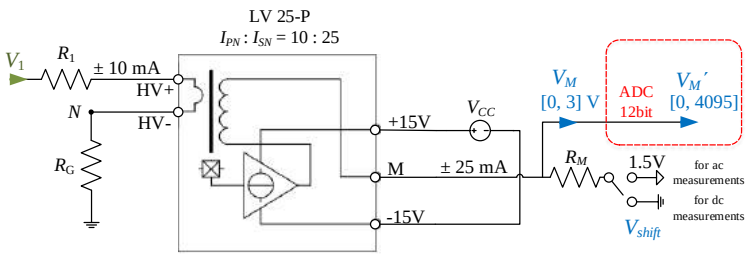
It is important to make sure that the distance between the dc-link terminals of the power converters and the pins of the capacitors is the shortest possible and that the traces on the dc-link PCB are wide in order to keep the parasitic inductance low. The traces connected to the plus and negative poles of each capacitor are also placed over each other, as explained also in Subsection 5.2.2, which can reduce the parasitic inductance even further.

5.2.4 Measurement Devices

Voltage measurements of the four dc-link voltages and of the three phase voltages at the grid output of the converter are needed for the control of the system. The Hall-effect voltage sensors from LEM with product number LV 25-P are used, as can be seen in Fig. 5.11. The voltage to be measured is shown as V_1 in Fig. 5.11(b). The nominal primary current of the sensor is 10mA; therefore, a suitable resistor R_1 is placed between the node V_1 and the input of the sensor HV+. All the required voltages are measured in respect to the neutral point of the dc-link N and, therefore, the negative pole of the sensor HV- is connected to N. The neutral



(a)



(b)

Fig. 5.11: (a) Laboratory prototype and (b) schematic diagram of the dc and ac voltage measurement PCB

point N is grounded though a ground resistor $R_G = 14.1$ kΩ.

The LV 25-P sensor behaves as a current source at its secondary side with nominal secondary current 25 mA. The voltage $V_M \in [0, 3]$ V across the resistor R_M is the input of the ADC channel of the MCU. When the voltage to be measured V_1 is ac and gets both positive and negative values, the signal V_M needs to be shifted up by 1.5 V and the reference of the signal is the 1.5 V, as shown on the right side of Fig. 5.11(b). In case a dc voltage is being measured, the reference of V_M is the ground. The R_M is equal to 60 Ω, when the measured voltage is ac, and is equal to 120 Ω, when measuring dc voltages.

The ADC of the MCU converts the V_M into a 12bit digital signal and the original

voltage V_1 can be calculated as follows

$$V_1 = \left(\frac{3V'_M}{4095} - V_{shift} \right) \cdot gain + V_{offset} \tag{5.1}$$

where the variable *gain* depends on the ratio between the primary and secondary side of the measurement device and on the resistor R_M.

Similar Hall-effect sensors are used for measuring the currents of the system. More specifically, the following current measurements are needed (see Fig. 5.1): three-phase currents of the PMSG I_{gen}, three-phase grid currents I_s and the current of the three dc inductors I_L . The current transducer LA 25-P from LEM is used for the current measurements and similar methodology to the voltage sensors is used for receiving the measured signal in the MCU.

5.2.5 Overcurrent-Overvoltage Protection Strategy

The signals from all the measurement devices end up on the PCB shown in Fig. 5.12 before being sent to the ADC inputs of the MCU. This PCB converts all the measured signals into the correct voltage level which is required for the ADC inputs. Another use of this board is to disconnect the converter in case an overcurrent/overvoltage is measured in the system. The analog circuit shown in Fig. 5.13 compares each measured signal V_M with a maximum and minimum value $V_{ref\ H}$ and $V_{ref\ L}$, respectively. In case V_M exceeds the predefined operating region, an error signal is created, which turns on also a red LED. The global error signal PRT is the output of this board.

This error signal forces all the power switches of the converters to open, in case of a fault. This is achieved through the trip-zone module of the MCU [144] and also though another PCB marked with red color in Fig. 5.13, whose function is to convert the ePWM outputs of the microcontroller into optical signals, which are sent to the gate drivers. The PRT disables the PWM signals of the gate drivers protecting the converters. The error signal is also connected to a relay coupled to a mechanical switch which switches-off the converters. The detailed schematics of the PCBs shown in Fig. 5.13 can be found in Appendix B.

Therefore, there is a three-layer overcurrent/overvoltage protection strategy of the generator drive. The analog circuit that disconnects the control signals of the gate drivers has the shortest reaction time, since the logical gates have delay in the range of a few μs.

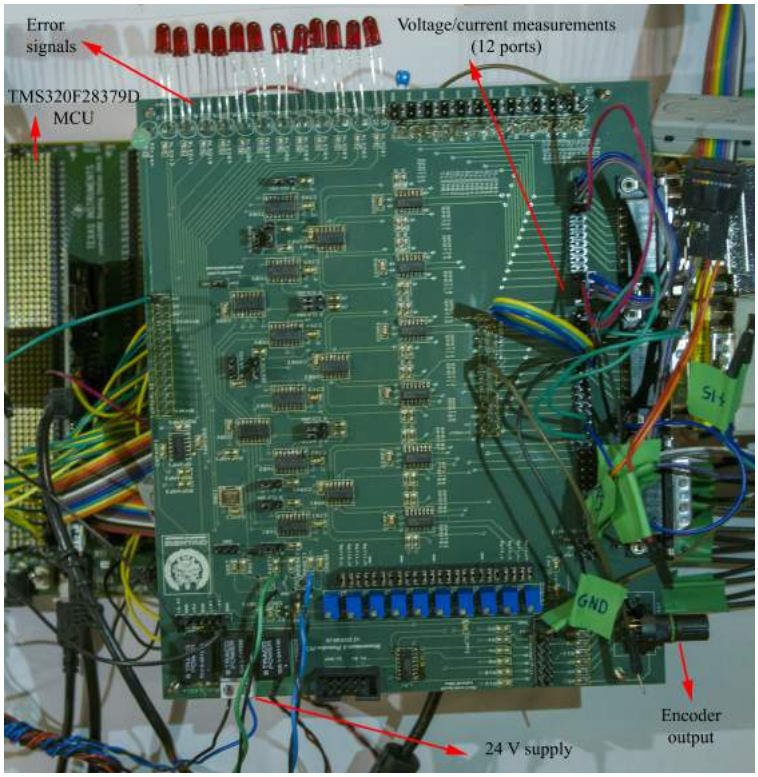


Fig. 5.12: PCB collecting all the measurement signals of the drive before routing them to the MCU

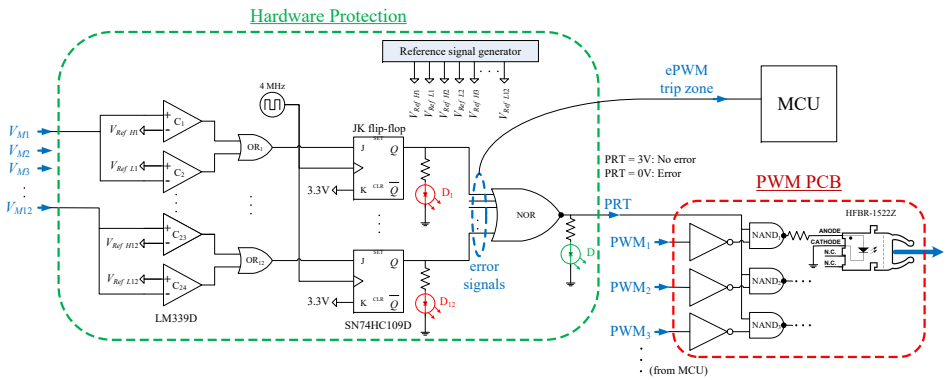


Fig. 5.13: Schematic diagram of the overcurrent/overvoltage protection strategy

5.3 Experimental Results

5.3.1 Medium Voltage PMSG

A medium voltage PMSG has been used within this project and it is tested in this subsection in order to evaluate its performance and measure its parameters. The electrical machine test bench is shown in Fig. 5.14(e), where the PMSG and the driving motor IM are at the right and left side, respectively. Pictures of the generator during its manufacturing phase are shown in Fig. 5.14(a)-(d).

The design of the generator is not part of this thesis.

No-load test of the PMSG

The PMSG is tested first at no-load conditions in order to evaluate the back-EMF and the cogging torque and, afterwards, load-tests are implemented. The

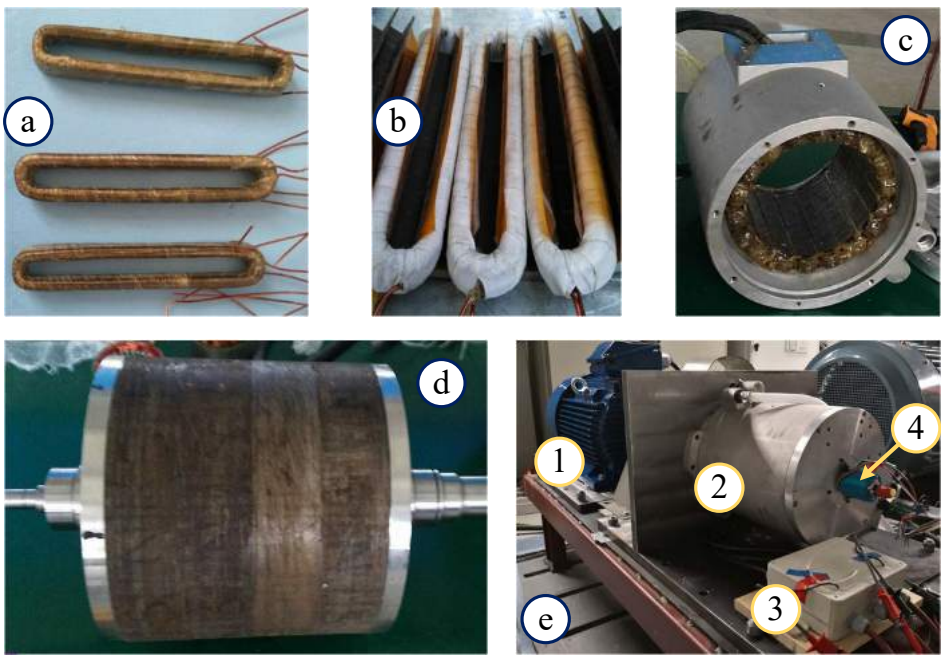


Fig. 5.14: PMSG (a)+(b)Stator windings, (c) stator, (d) rotor and (e) the whole machine test-bench: 1) IM, 2) the medium voltage PMSG mounted on the bench, 3) connection box for the stator cables of the PMSG, 4) terminal for connecting the encoder and temperature sensors of the PMSG

following voltage probes are used for the following experiments of this section: the HVD3106A voltage probe with up to V_{peak}=1500 V measurement range [7] and the CP150 current probe [8].

No-load test of the PMSG is implemented by having the terminals of the generator open-circuited and operating the IM in motor mode. The measured L2L voltage is equal to the no-load back-EMF of the machine, which is shown in Fig. 5.15(a) for rotor speeds equal to 1600 rpm up to 1200 rpm. Fig. 5.15(b) shows one mechanical period of the no-load EMF voltage and the cogging torque for rotor speed 200 rpm.

The torque waveform has 12 positive and negative peaks in one mechanical period of the PSMG, which is the 12th harmonic generated by the slots and poles of the PMSG. There is also 6th harmonic component in the torque waveform generated by the cogging torque of the IM.

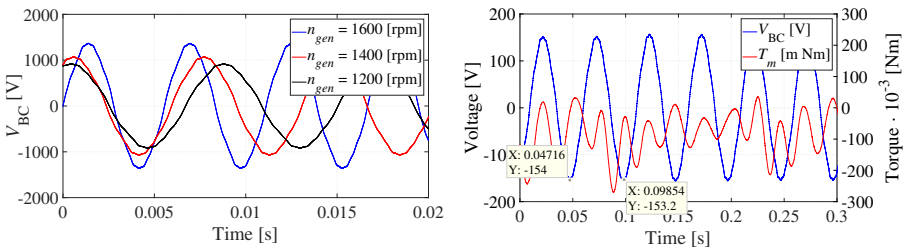


Fig. 5.15: Experimental results of the medium voltage PMSG no-load test: (a) no-load EMF voltage for various rotor speeds and (b) cogging torque for 200 rpm rotational speed

Load test of the PMSG without converter control

The PMSG is tested also with a resistive load R_L, as shown in Fig. 5.16. The load is three resistor banks connected in Y connection and can vary its resistance from 0.4 Ω up to 3 Ω. The PMSG is connected to the resistive load through a step-down transformer and its active and reactive power in each case are determined by the combination of the equivalent resistance and inductance of the load, since it is not controlled by a converter.

Experimental results of this test are presented in Fig. 5.17 for two different operating points. In Figs. 5.17(a)-(b) the load is $R_L = 3$ Ω with $n_{gen} = 2000$ rpm and the apparent power is $S = 6.42$ kVA, while in Figs. 5.17(c)-(d) the load is

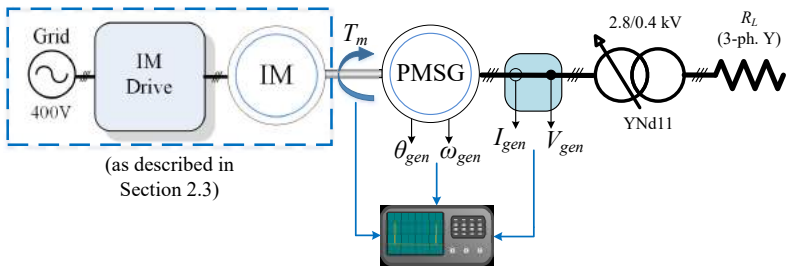
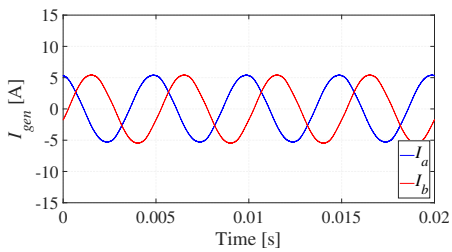


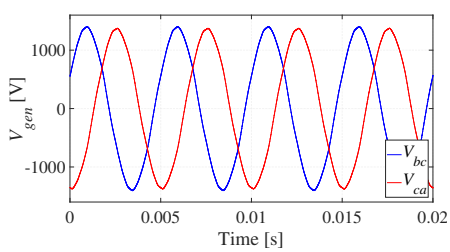
Fig. 5.16: Schematic diagram of the PMSG load test with direct connection of the generator to the resistive-inductive load

$R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm and the apparent power is $S = 12.27$ kVA.

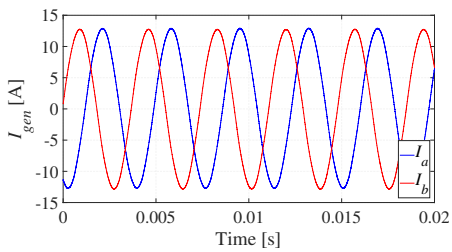
The parameters of the PMSG are shown in Table 5.2, where the inductances in the d- and q-axis have been measured based on the method described in [145, 146]. Specifically, step-change of dc current was applied towards the d- and q-axis of the machine and the inductance was calculated from the response of the current.



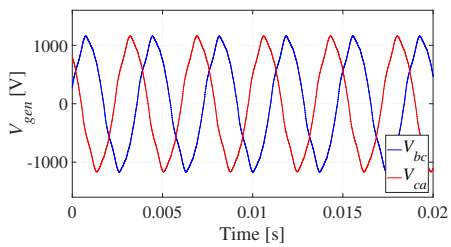
(a) $R_L = 3\ \Omega$, $n_{gen} = 2000$ rpm



(b) $R_L = 3\ \Omega$, $n_{gen} = 2000$ rpm



(c) $R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm



(d) $R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm

Fig. 5.17: Experimental results of the medium voltage PMSG with resistive-inductive load

Table 5.2: Rated values and control parameters of the PMSG and the IM

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Nominal rotor speed	4000	rpm
Number of pole pairs p	6	-
Nominal torque T_N	119	Nm
No-load EMF at rated speed (L2L, peak)	2932	V
Stator inductance L_d	18.9	mH
Stator inductance L_q	25	mH
Stator resistance R_S	1.5	Ω
PMSG inertia J_{PMSG}	0.1274367	kg·m^2
IM inertia J_{IM}	0.2	kg·m^2
Torque sensor inertia J_S	$175.8{\cdot}10^{-6}$	kg·m^2
PMSG current controller bandwidth α_c	1500	rad/s
PMSG speed controller bandwidth α_ω	15	rad/s
PMSG converter switching frequency f_{sw}	20	kHz

5.3.2 Power Conversion System

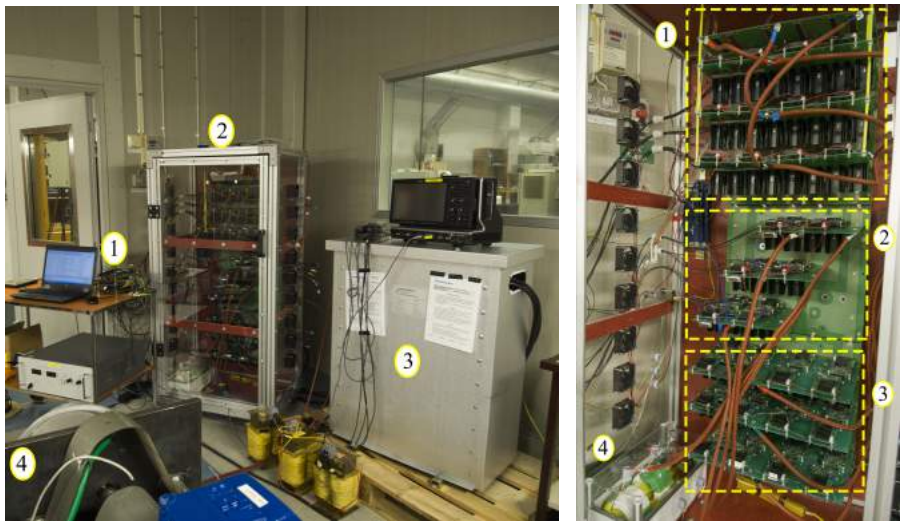
The multilevel generator drive is tested in this subsection and the laboratory set-up is shown in Fig. 5.18(a) with the electrical machine test-bench and the power converter cabinet. Fig. 5.18(b) shows a more detailed view of the power converter cabinet. The converters installed inside the cabinet are marked with dashed boxes and are described in the figure caption.

The dc-link voltage balancing strategy of Subsection 4.5.2 is used here, namely the three-stage balancing converter with open-loop control of its duty cycle. The balancing converter has the same switching frequency with the NPC converters, namely 20 kHz.

Generator-side Converter

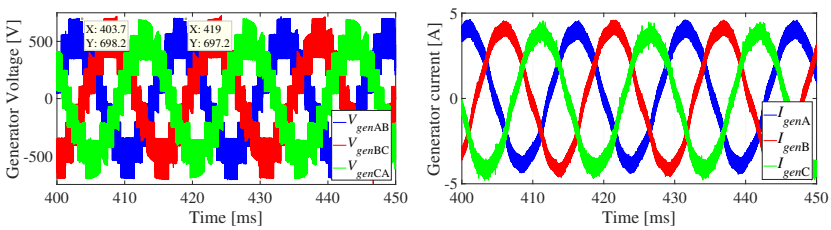
Experimental results of the generator-side NPC converter are shown in Figs. 5.19-5.20. The PMSG operates in generator-mode with 650 rpm and has reference current equal to $I^*_{genq} = -4$ A. The total dc-link voltage is 670 V during this test.

The FFT analysis of the voltages and currents is also shown and specifically the THD of the current is 3.997%, while the THD of the phase voltage is 37.338%. When compared to the simulation results of Fig. 4.25 in Subsection 4.5.2, it can



(a) (b)

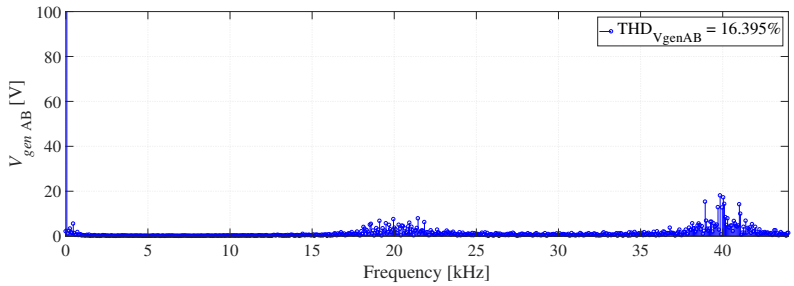
Fig. 5.18: (a) Laboratory set-up of 1) the MCU and measurements board, 2) the power converter cabinet, 3) the 2.8/0.4 kV three-phase transformer 4) the machines test-bench; (b) closer view of the power converter cabinet with 1) the grid side 5-level converter, 2) the dc-link balancing converter, 3) the generator-side 5-level converter and 4) the dc inductors for the balancing converter



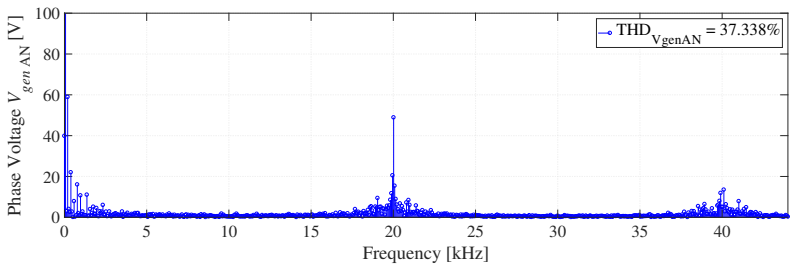
(a) (b)

Fig. 5.19: Experimental results of the generator-side NPC converter when the generator operates at 650 rpm and current $I^*_{genq} = -4$ A: (a) three-phase L2L generator voltage and (b) current

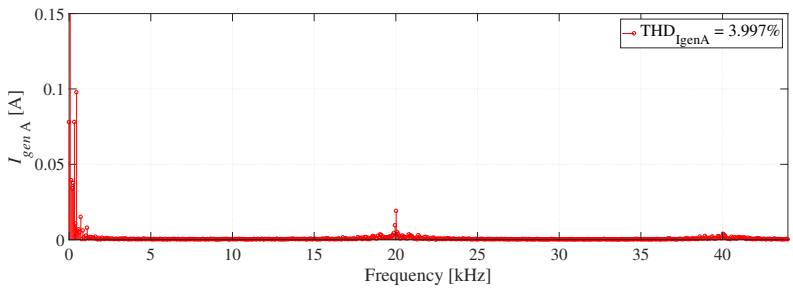
be seen that the phase voltage THD is very close to the simulated value. However, the THD of the current is higher at the experimental results and this is explained due to the lower amplitude of the current there.



(a)



(b)



(c)

Fig. 5.20: Experimental results of the generator-side NPC converter when the generator operates with 650 rpm and current $I^*_{genq} = -4$ A: FFT analysis of the (a) L2L voltage V_{genAB}, (b) phase voltage V_{genAN} and (c) stator current I_{genA}

Grid-side Converter

Experimental results of the grid-side converter are shown in the following figures. The three-phase transformer shown in Fig. 5.1 is not used here, because low voltage tests are implemented. Instead, the grid converter is connected to the 400 V-grid through a series-connected inductor with inductance $L_f = 2$ mH. The grid-side converter control parameters are shown in Table 5.3.

The current controller of the grid current I_s is tested and experimental results

Table 5.3: Parameters of the Grid-side Converter

Parameter	Value	Unit
Tested L2L grid voltage (rms) V_s	400	V
Fundamental frequency f_n	50	Hz
Grid converter switching frequency f_{sw}	20	kHz
Grid filter inductance L_f	2	mH
Tested total dc-link voltage $V_{dc\ tot}$	670	V
Grid current controller bandwidth α_{cs}	8000	rad/s
PLL bandwidth α_{PLL}	10π	rad/s
DC-link controller bandwidth α_{DClink}	400	rad/s

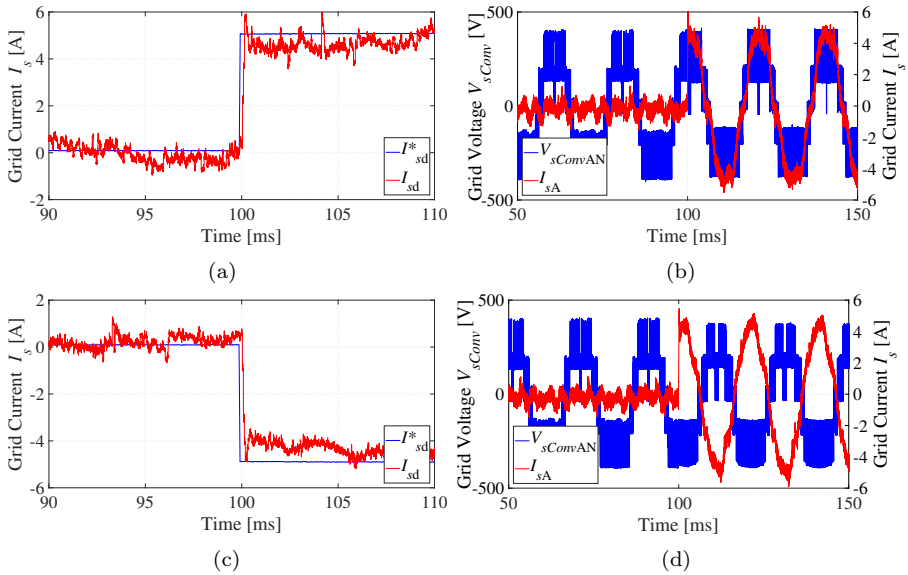


Fig. 5.21: Experimental results of the grid-side NPC converter with a step-change of the I^*_{sd} reference current (a)-(b) from 0 to 5 A and (c)-(d) from 0 to -5 A

of the phase A current I_{sA} and the phase voltage at the output of the converter $V_{sConvAN}$ are shown in Figs. 5.21-5.22. The grid phase voltage is defined as the differential voltage between a phase of the converter and the middle point of the dc-link, marked as N. Specifically, step-change of the I^*_{sd} is applied and the converter is sending active power to the grid in Fig. 5.21(a)-(b), while it receives power from the grid in Fig. 5.21(c)-(d). Similarly, q-axis current I^*_{sq} is applied in Fig. 5.22 and the grid converter is exchanging reactive power with the grid.

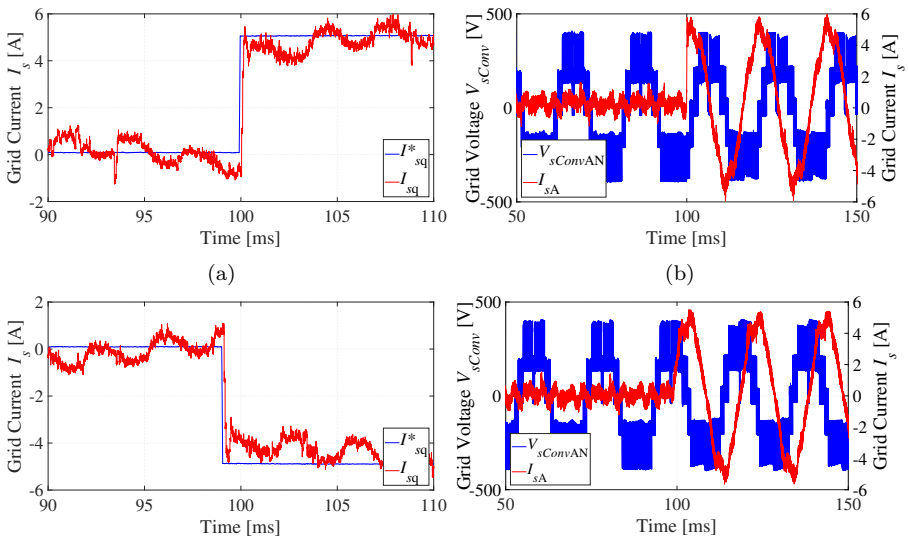


Fig. 5.22: Experimental results of the grid-side NPC converter with a step-change of the I^*_{sq} reference current (a)-(b) from 0 to 5 A and (c)-(d) from 0 to -5 A

The dc-link controller of the grid-side NPC converter is tested in Fig. 5.23 with a step-change of the reference voltage, which changes from 670 V to 600 V at the time instant 85ms. The individual voltages of the four dc-link capacitors in Fig. 5.23(b) follow the change of the total dc voltage. They remain balanced with each other with a small error during this transient. This error can be explained due to the use of open-loop control for the balancing converter, as mentioned previously. Therefore, larger errors between the capacitor voltages are expected compared to the closed-loop control scheme shown in the simulation results of Subsection 4.5.2.

The amplitude of the L2L grid voltage at the output of the converter $V_{sConvAB}$ changes as well, as can be seen in Fig. 5.23(c), since it varies between $+V_{dc\ tot}$ and $-V_{dc\ tot}$. The converter voltage is approximately 40 V higher than the dc-link voltage due to the ringing on the power switches. The grid voltage V_{sAB} is also shown in the same figure, which is in phase with the converter voltage. The d-axis grid current I_{sd} in Fig. 5.23(d) is calculated by the dc-link PI controller. A limiter of 6 A is applied on the reference d-current, which is reflected on the actual current.

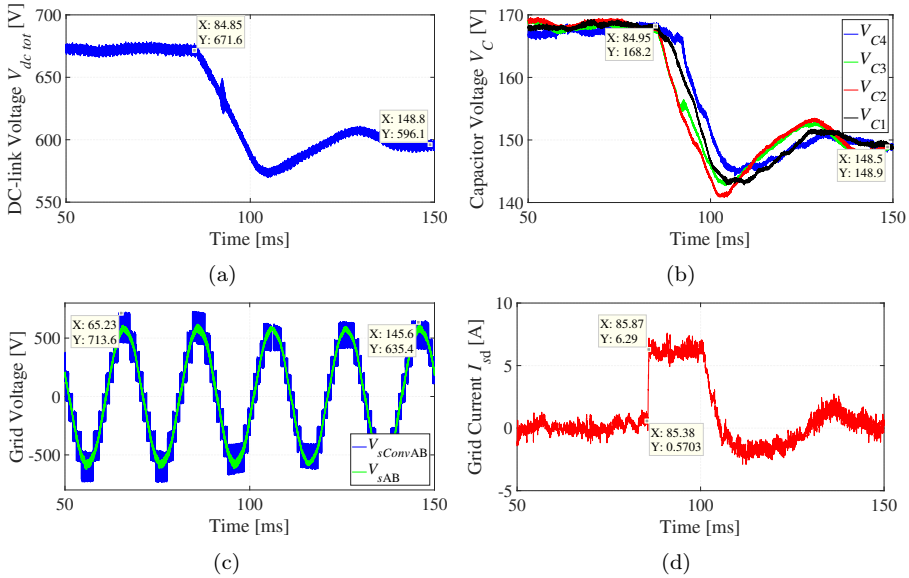


Fig. 5.23: Experimental results of the grid-side NPC converter with a step-change of the dc-link voltage $V_{dc\ tot}$ from 670 V to 600 V: (a) dc-link voltage, (b) dc-link capacitor voltages, (c) grid voltage and (d) d-axis grid current

5.4 Summary

In this chapter, the design process and test results of a novel 5-level NPC-based PMSG drive have been presented. Firstly, the hardware design and component selection of the NPC converters and the balancing circuit are described. Special care has been taken so that the power converters are designed with the potential to operate at medium voltage level, with up to 4 kV at the dc-side. Therefore, large creepage distance has been kept between the power components in order to avoid failures due to the high operating voltage and the control and measurement boards are highly insulated from the power circuit of the converters. The parasitic inductance on the converter boards is also minimized as much as possible and snubber circuits are used in parallel to some of the power switches to further reduce their voltage overshoot during the switching transient. The prototype multilevel drive uses 1.2 kV SiC power switches in order to decrease the converter losses. Suitable gate drive boards have been designed for the specific switches.

Experimental results of both converters of the drive are shown in order to demonstrate the functionality of the system under various operating conditions. DC-link voltage up to 670 V and current of 5 A have been tested in this chapter.

Chapter 6

Power-HIL Testing of High-Power Electrical Machine Drives

6.1 Electrical Machine Emulator

Testing VSCs for electrical machine drives on a machine test-bench, as has been shown previously in Chapter 5, entails difficulties in case the stability of the VSC controller has not been verified yet and when operation close to the voltage, current and speed limit of the system needs to be tested. Safety concerns and cost limitations for developing bulky electrical machine test benches are further common issues. The electrical machine might also not be available at the time when the test has been scheduled.

The electrical machine under-test can be replaced with another VSC that acts as a virtual load emulating the electrical machine operation. An inductive device, such as a three-phase inductor or a transformer, needs also to be placed at the ac coupling between the two VSCs in order to filter the current harmonics. This testing procedure is called Power Hardware-in-the-loop (P-HIL) and its main advantage is that many different machine types of similar rated parameters can be tested using mostly the same hardware, with minor modifications in the control of the two VSCs. Therefore, experimental testing of the inverter-under-test (IUT) can be accelerated, reducing at the same time their development cost.

There are two basic configurations of electrical machine emulators. In the first configuration the IUT and the machine-emulator VSC have separate dc power supplies with power rating equal to the maximum power that needs to be tested,

as shown in [147–149]. The main disadvantage of this concept is the requirement for two high-power supplies, which entails higher cost and complexity. In the second configuration, dc coupling of the emulator VSC and the IUT can be used as in [150–152], so that the energy of the system circulates in this loop and only the power losses of the converters and the passive components need to be supplied by an external dc power supply.

The second type of machine emulators has the simplest system configuration, due to its reduced number of components. However, when a three-phase inductor is used as a filter at the ac coupling of the topology, a conductive path with very low impedance for the zero-sequence is created. Since the dc link of the two converters is directly connected in this specific machine emulator, a circulating zero-sequence current can be created that may reach high values. This circulating current acts as a disturbance for the current controller of the IUT and introduces additional load for the power switches. Its value increases, proportionally with the dc voltage of the topology and the voltage difference between the two inverters. The zero-sequence current contains low- and high-frequency components [152, 153], with the low-frequency ones being mainly dc- and third-harmonic and the high-frequency components being at multiplies of the converters' switching frequency.

Control techniques for suppressing the circulating zero-sequence current are presented in this chapter and verified experimentally on a PMSM emulator.

6.1.1 Machine Modelling Approaches

Emulation accuracy of the studied electrical machine depends to a large extend on the accuracy of the machine model itself, which is implemented either with analytical equations or/and utilizing simulation data in order for the emulator system to perform similarly with the physical machine drive.

Simplifications in the modelling process of the studied electrical machines are often observed in the literature during the development of machine emulators. A synchronous motor has been emulated in [150], where non-salient rotor structure is assumed and magnet saturation has not been considered. Similar assumptions have been made for an induction motor emulator in [154]. This can lead to large deviations, especially at high-load conditions where the machine core is usually saturated. This issue can be solved by utilizing physics-based machine model [148, 155], where the PMSM parameters are determined at any time instant as a function of the instantaneous current and rotor position through look-up-tables with FEM data. Look-up-table based machine models are used also in [147],

where the measured dq-axis voltage of the IUT is the input of the model and the estimated machine current is the output. High-bandwidth current controllers and use of FPGA is necessary to implement this machine emulator.

Another aspect of study is the type of control used for the machine emulator VSC in order to generate the correct PWM voltage that would emulate the physical machine, which are briefly shown in Fig. 6.1. The standard method is to use closed-loop current control for the emulator VSC. The measured three-phase voltage of the IUT $v_{e\ abc}$ is the input of the controller and the reference voltage for the emulator VSC $v_{em\ abc}$ is the output variable. However, this would cause a conflict with the current controller of the IUT, since both inverters have the same current flowing through their ac terminals. This issue can been solved by using PI-regulators with higher bandwidth for the emulator-side current controller that would respond faster than the IUT-side controller [147]. In order to ensure faster dynamics for the emulator converter, significantly higher switching frequency is required, which can be three or more times the switching frequency of the IUT [156]. Increasing the switching frequency so much can be challenging for high-power industrial inverters, which can be alleviated by applying sequential switching [156] or using SiC devices that have lower switching losses [149]. High-bandwidth model predictive controller can also be used for current control of the emulator converter [149]. FPGA is also necessary in these cases to implement the control and model the machine current with high fidelity emulating even the current harmonics of the IUT.

The "inverted" machine model is another control approach for the machine emulator, where the emulator converter is controlled in open-loop mode. To avoid the need for a high-bandwidth current controller, the reference voltage for the emulator converter that represents the voltage response of the machine is calculated

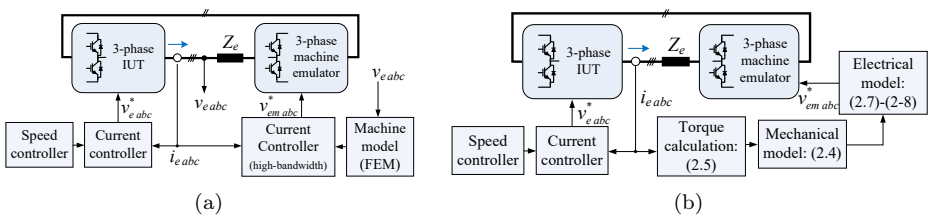


Fig. 6.1: Simplified control diagram of the machine emulator set-up using (a) individual high-bandwidth current control for the emulator VSC or (b) open-loop voltage control using the "inverted" machine model

analytically with the torque and voltage equations of the machine. "Inverted" machine modeling has been used in [150, 154]. The main disadvantage of this method is that only the fundamental current and voltage of the machine can be emulated and not the current harmonics or the torque ripple. Low switching frequency can be used for the emulator converter that allows the use of CPU-based DSP instead of FPGA. Also, there is no need to measure the PWM ac voltage of the inverter in order to implement this control. FEM data can still be utilized in order to consider the variation of the stator inductance due to core saturation.

6.1.2 PMSM Emulation with the Inverted Machine Model

The "inverted" machine model has been studied further in this chapter, since it can model accurately enough the dynamic and steady state response of a PMSM. The detailed diagram of the developed P-HIL system and the structure of the control for both converters is shown in Fig. 6.2. The IUT is controlled with standard FOC, as described previously in Section 2.2. The control structure of the emulator converter consists of three blocks: the machine model calculating the torque and speed of the machine, the voltage reference calculation block and the modulator.

As can be seen in Fig. 6.3, input of the machine model block is the measured three-phase current i_e, which is converted into the dq0-frame. The calculated $i_{e\ dq}$ is utilized to estimate the flux linkages ψ_d and ψ_q of the emulated machine through

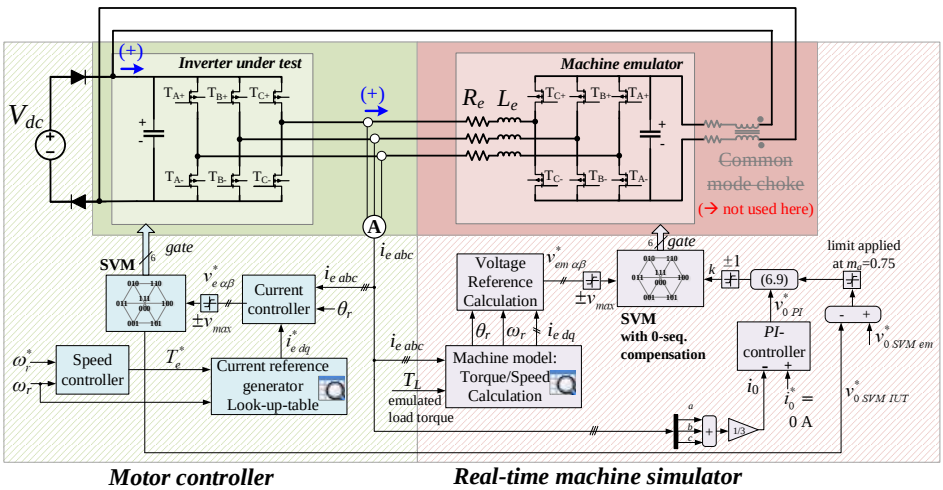


Fig. 6.2: Schematic of a PMSM emulator showing the circuit diagram of the topology and the structure of the control system

look-up-tables that contain FEM-simulated data. Then, by substituting the current and the flux linkage in (2.5), the electromagnetic torque T_e is calculated. Afterwards, by using (2.4), the acceleration $\mathrm{d}\omega_r/\mathrm{d}t$ can be derived which is integrated to get the machine rotor speed ω_r. With further integration of the rotor speed, the rotor angle θ_r can also be calculated.

The voltage reference calculation block receives as input the calculated θ_r, ω_r and the machine current $i_{e\ dq}$. The PMSM voltage equations shown in (2.7)-(2.8) are modified in order to compensate for the voltage drop across the three-phase inductor L_e and its resistance R_e. This voltage drop becomes significant especially when high torque and speed are emulated.

$$v^*_{em\ d} \approx v_{em\ d} = (R_s - R_e)i_{ed} + \frac{\mathrm{d}\psi'_d}{\mathrm{d}t} - \omega_e \psi'_q \tag{6.1}$$

$$v^*_{em\ q} \approx v_{em\ q} = (R_s - R_e)i_{eq} + \frac{\mathrm{d}\psi'_q}{\mathrm{d}t} + \omega_e \psi'_d \tag{6.2}$$

where $\omega_e = p\ \omega_r$ is the electrical frequency and p is the number of pole-pairs of the machine. The stator copper loss of the machine is modelled through the stator resistance R_s. The d- and q-axis flux linkages ψ'_d, ψ'_q are expressed as

$$\psi'_d = \psi_d - L_e i_d, \quad \psi'_q = \psi_q - L_e i_q \tag{6.3}$$

The flux linkages ψ_d and ψ_q are again defined by 2-dimensional look-up-tables for different d- and q-current combinations.

The final reference voltage of the emulator v^*_{em} is sent to the SVM block that generates the corresponding PWM signals.

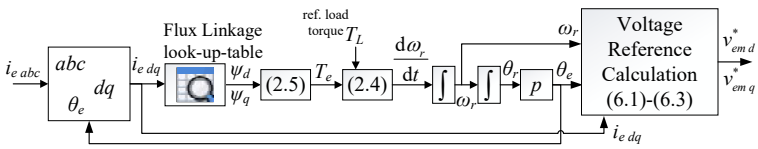


Fig. 6.3: Block diagram of the PMSM model as implemented in the "inverted" machine emulator

6.2 Common Mode Voltage Control

Two-level converters have been used in this study and, therefore, the following common mode voltage control is described for this topology.

SVM is used for both the IUT and the emulator VSC that has 8 available space vectors, of which 6 are active vectors and 2 are zero vectors located at the origin

of the plane. The active vectors contribute mainly to the fundamental frequency of the voltage, while the zero vectors create only zero sequence or else common mode. The 2-level space vector hexagon is divided into 6 triangles and all the three vectors of each triangles become active sequentially during each switching period, as presented in Subsection 4.3.2.

All space vectors of the SVM plane contribute to both the $V_{\alpha\beta}$ voltage components and to the zero-sequence, as listed in Table 6.1. The values of these voltage components originate from the Clarke transformation, when applied on the *abc* phase voltage of each switching state. For example, the switching vector $\underline{V}_1 = [1\ 0\ 0]$ creates the following phase voltages $[V_\mathrm{a}\ V_b\ V_c] = [\frac{1}{2}V_{dc} \quad -\frac{1}{2}V_{dc} \quad -\frac{1}{2}V_{dc}]$, which can be transformed into the $\alpha\beta$-domain as $V_\alpha = \frac{2}{3}V_{dc}$, $V_\beta = 0$ and $V_0 = -\frac{1}{6}V_{dc}$. By multiplying these voltages with their corresponding duty cycles and the dc-link voltage V_{dc}, the average output voltage of the inverter for one switching period can be calculated.

An example is shown in Fig. 6.4(b) for reference voltage $\hat{\mathrm{v}}^* = 0.585$ pu and fundamental frequency 200 Hz. The duty cycle of phase A $d_{ph\mathrm{A}}$ is shown with blue curve, while the duty cycles of the voltage vectors d_E and d_F are shown in red and green, respectively. It can be observed that the duty cycles of both vectors d_E and d_F have a dc and third-harmonic component that creates common mode voltage equal to $-\frac{1}{6}V_{dc}d_\mathrm{E}$ and $\frac{1}{6}V_{dc}d_\mathrm{F}$, respectively. The switching harmonics are not considered with this calculation, since the above voltages are averaged within one switching period.

The common mode voltage component of the long vectors $\underline{\mathrm{V}}_1$ - $\underline{\mathrm{V}}_6$ creates circulating current in the P-HIL test bench, as seen in the equivalent circuit of Fig. 6.5. The two inverters can be represented by the common-mode-voltage sources $V_{e\,0}$

Table 6.1: Switching Vectors of 2-level SVM [153]

Voltage Vector	V_α/V_{dc}	V_β/V_{dc}	V_0/V_{dc}
$\underline{V}_0 = [0\ 0\ 0]$	0	0	-1/2
$\underline{V}_1 = [1\ 0\ 0]$	2/3	0	-1/6
$\underline{V}_2 = [1\ 1\ 0]$	1/3	$1/\sqrt{3}$	1/6
$\underline{V}_3 = [0\ 1\ 0]$	-1/3	$1/\sqrt{3}$	-1/6
$\underline{V}_4 = [0\ 1\ 1]$	-2/3	0	1/6
$\underline{V}_5 = [0\ 0\ 1]$	-1/3	$-1/\sqrt{3}$	-1/6
$\underline{V}_6 = [1\ 0\ 1]$	1/3	$-1/\sqrt{3}$	1/6
$\underline{V}_7 = [1\ 1\ 1]$	0	0	1/2

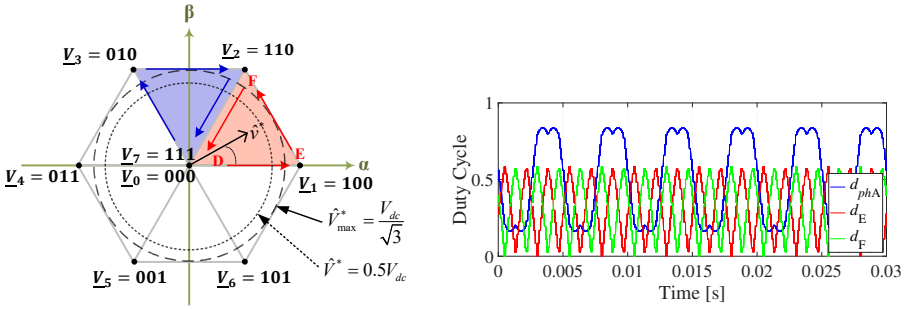


Fig. 6.4: 2-level space vector modulation indicating (a) the eight available switching states, the reference voltage vector $\hat{v}^*$ and with dashed circle the limit between normal operation and overmodulation; (b) the duty cycles of phase A and of the space vectors E and F for $\hat{v}^* = 0.585$ pu

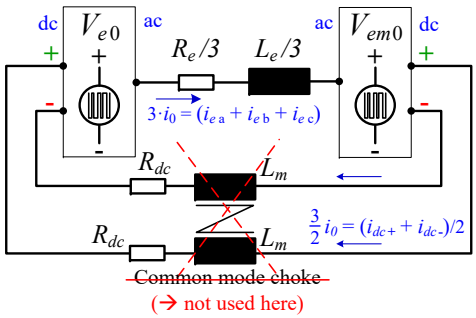


Fig. 6.5: Zero-sequence-equivalent circuit of the machine emulator with three-phase inductor L_e at the ac-side and common dc-link

and $V_{em\,0}$ and the per-phase zero-sequence current is equal to

$$i_0 = (i_{e\,a} + i_{e\,b} + i_{e\,c})\frac{1}{3} \tag{6.4}$$

A common mode choke installed at the dc-link of the topology could filter the common mode voltage and eliminate the circulating current. However, hardware filtering is not preferred in this study. Instead, suitable control techniques are studied in the following subsections that can suppress the circulating current without any additional hardware.

6.2.1 Closed-loop Common Mode Current Control

The zero vectors $\underline{V}_0$ and $\underline{V}_7$ create only common mode voltage with opposite sign, as seen in Table 6.1. In the standard SVM algorithm, the duty cycle d_D from (4.22) is usually distributed equally between these two vectors, as seen in (4.24), in

order to achieve average common mode voltage equal to zero during one switching period. However, a different distribution of the zero vectors duty cycles can be imposed in order to cancel out the the circulating current in the P-HIL test rig.

The circulating current is suppressed in the motor emulator of [152] through a PI-controller that creates a reference common mode voltage $v_{0\ PI}^{*}$. This reference voltage can adjust the distribution of the zero vectors in order to cancel the circulating current. A similar approach has been followed in[157] to limit the zero sequence current in parallel-connected 2-level inverters.

The circulating current dynamics depend on the series inductance of the circuit. Therefore, the proportional and integral gains of this controller are selected as

$$k_{P\ 0seq} = \alpha_{0seq}\ L_e, \quad k_{I\ 0seq} = k_{P\ 0seq}/3 \tag{6.5}$$

where α_{0seq} is the bandwidth of the control loop.

Since the purpose of the P-HIL set-up is to emulate the same operating conditions for the IUT as if it was used with a real machine (i.e. same phase voltages and currents), the standard SVM, as in (4.24), is used for the modulation of that inverter. The common mode voltage is controlled only by the SVM of the emulator-inverter.

6.2.2 Zero-Sequence Voltage Compensation

Although a PI control loop can regulate effectively the dc-component of the zero-sequence, the bandwidth of the controller is not fast enough to eliminate completely the third-harmonic component and, therefore, an improved control structure is needed. More advanced control for the zero-sequence have been proposed for parallel-connected inverters in [158] with a hybrid PWM technique and in [153] presenting an instantaneous common mode voltage elimination technique using SVM.

An improved control system is shown in Fig. 6.6 that manages to eliminate the circulating current in machine emulators with 2-level inverters. The common mode voltage created by the active voltage vectors within each switching cycle is calculated and directly compensated by injecting equally sized voltage through the zero vectors. Specifically, the injected zero-sequence voltage in per-unit can be calculated as

$$v_{0\ SVM}^{*} = -\frac{1}{6}d_E + \frac{1}{6}d_F \tag{6.6}$$

The PI regulator shown in the previous subsection with output $v_{0\ PI}^{*}$ is also used simultaneously in order to regulate the dc-component of the zero-sequence current

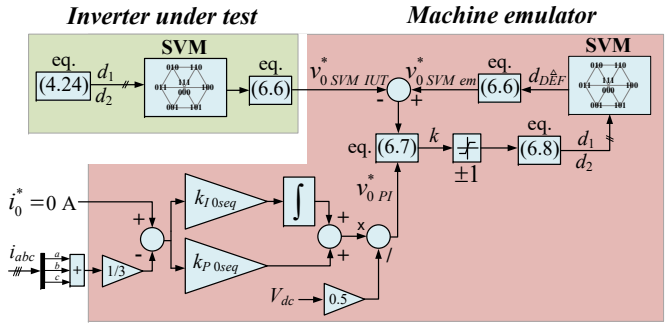


Fig. 6.6: Schematic of the proposed zero-sequence-compensated space vector modulation

and ensure stability in the system. The total injected per-unit voltage for the zero vectors of the emulator converter is

$$k = -v_{0\ PI}^* + (v_{0\ SVM\ em}^* - v_{0\ SVM\ IUT}^*)\frac{2}{d_D} \tag{6.7}$$

A limiter is applied on k with values of [-1,1] and the final duty cycles of the zero vectors d_1 and d_2 are defined as

$$d_1 = (1+k)\frac{d_D}{2}, \quad d_2 = (1-k)\frac{d_D}{2} \tag{6.8}$$

6.2.3 Operation close to the Voltage Limit

The proposed zero-sequence control works effectively when the reference voltage of the emulator converter lays within $\hat{V}_{em}^* \in [0,\ 0.5V_{dc}]$, which is the area inside the dotted circle in Fig. 6.4(a). For $\hat{V}_{em}^* > 0.5V_{dc}$ the variable k exceeds the limits and the duty cycle d_D is not enough to fully compensate the total amount of zero-sequence that flows in the circuit.

This is shown with the simulation results of a PMSM emulator in Fig. 6.7. Voltage reference $\hat{V}_{em}^* = 0.49V_{dc}$ is used in the subplots (a), (c) and (e), whereas higher voltage reference $\hat{V}_{em}^* = 0.53V_{dc}$ is used for the remaining (b), (d) and (f). The variable k approaches the limits of [-1,1] in the first case, while it seems to get saturated in the second case. While in the first case the circulating per-phase current i_0 remains under control, in the second case it becomes larger and almost equal to the system where only a PI-controller regulates the common mode voltage.

In order to avoid such a condition that could cause instability in the common mode voltage control of the inverter, the injected common mode voltage is reduced at the high-voltage region as follows

$$k' = -v_{0\ PI}^* + c(v_{0\ SVM\ em}^* - v_{0\ SVM\ IUT}^*)\frac{2}{d_D} \tag{6.9}$$

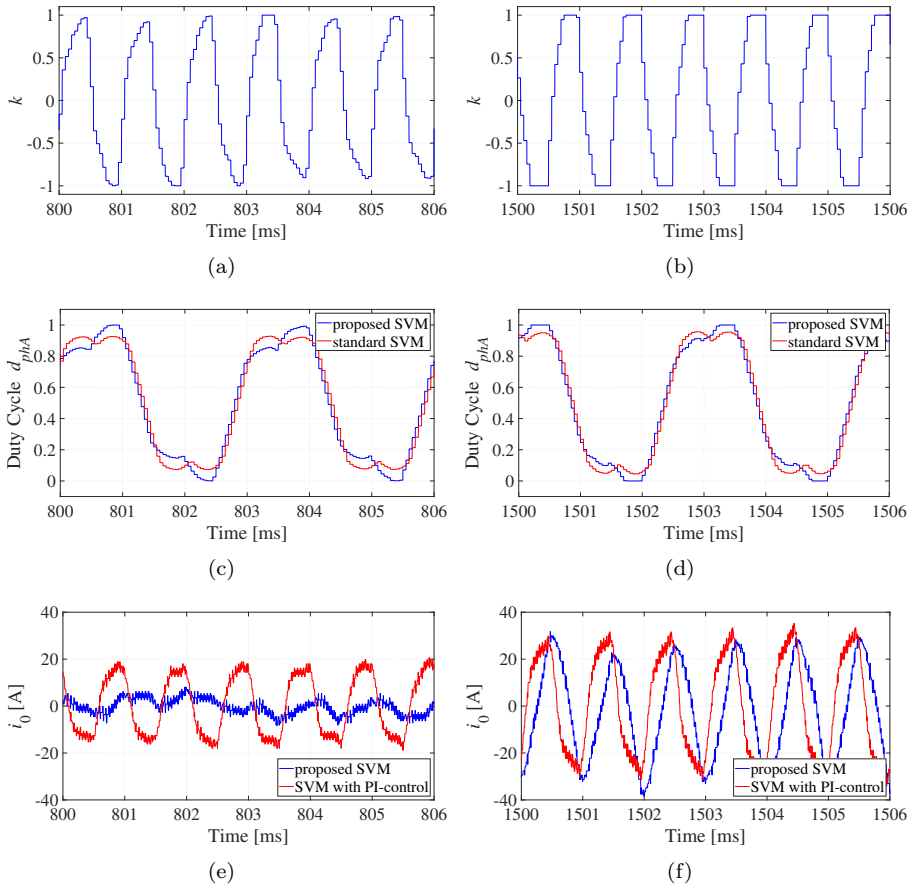


Fig. 6.7: Simulation results of PMSM emulator with zero-sequence voltage compensation when $\hat{V}^*_{em} = 0.49V_{dc}$ in (a),(c),(e) and when $\hat{V}^*_{em} = 0.53V_{dc}$ in (b),(d),(f)

where

$$\begin{aligned} c &= 1\ , \quad \text{for } \hat{V}^*_{em} \in [0,\ 0.5V_{dc}] \\ c &= \frac{1/\sqrt{3} - \hat{V}^*_{em}/V_{dc}}{1/\sqrt{3} - 0.5}\ , \quad \text{for } \hat{V}^*_{em} \in (0.5V_{dc},\ \frac{V_{dc}}{\sqrt{3}}] \end{aligned} \tag{6.10}$$

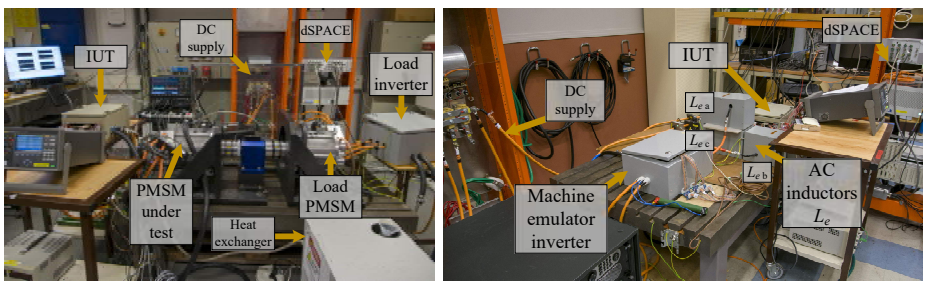
6.3 Comparative Results of PMSM drive and Machine Emulator

A PMSM drive is tested in this section, both in transient and steady-state conditions. The results of a standard machine test-bench are compared with similar results from a machine emulator, which is tuned to emulate that PMSM.

Fig. 6.8 shows the laboratory set-up used for the PMSM test bench and for the emulator of that machine. The same three-phase 2-level inverters are used for both experiments, which are made with SiC power modules of the XM3 family [159]. The IUT has the CAB450M12XM3 modules, while the second inverter [marked as "Load inverter" in Fig. 6.8(a) and "Machine emulator" in Fig. 6.8(b)], has the CAB425M12XM3 modules. More details regarding the design of the SiC inverters can be found in Chapter 7.

The inverters and the electrical machines are water cooled. A closed cooling loop is built in the first set-up of Fig. 6.8(a) with a pump/ heat exchanger dissipating the heat of the system, while running tap water is used for the set-up in Fig. 6.8(b).

The control system of the inverters is implemented on the dSPACE 1005 control board.



(a) (b)

Fig. 6.8: Laboratory set-up of (a) the 60 kW PMSM test bench and (b) emulator of this PMSM drive using the same power converters

6.3.1 Experimental Results of a 60 kW PMSM Drive

The experimental results of the PMSM test bench of Fig. 6.8(a) are presented in this subsection. The corresponding block diagram of the studied topology showing the control of the inverters is shown in Fig. 6.9.

The two machines are identical and both controlled with FOC. Specifically, speed control is applied on the machine-under-test where the input variable is the speed reference ω_r^*. Torque control is used for the load machine with control input being the reference torque T_{e2}^*. Look-up-table-based current reference generation is applied that utilizes offline calculated data from FEM simulations. The optimal stator currents $I_{e\ d}$ and $I_{e\ q}$ are shown in the machine torque-speed operation map of Figs. 6.10(a)-(b), when the stator copper losses are minimized. The resultant stator voltage and machine efficiency are shown in Figs. 6.10(c) and (d), respectively. The mechanical losses of the efficiency subplot are calculated by considering viscous damping equal to $3.8 \cdot 10^{-4}\ \frac{\text{Nm·s}}{\text{rad}}$ and the stray losses are equal to 0.75% of the machine active power.

The parameters of the PMSM test-bench and the control variables of the two inverters are listed in Table 6.2.

The dynamic response of the PMSM drive has been tested with the experimental results in Fig. 6.11, showing that the controllers of the machines are stable and follow their reference. The load machine operates in torque control mode as a generator and the machine-under-test controls the rotational speed of the set-up and operates as a motor. The speed of the system is set to 1000 rpm and, then, at 1.194 sec the load torque increases in a ramp. Specifically, Fig. 6.11(a) shows the reference ω_r^* and actual rotor speed ω_r with blue color, the reference electromagnetic torque for the load machine T_{e2}^* and for the machine-under-test

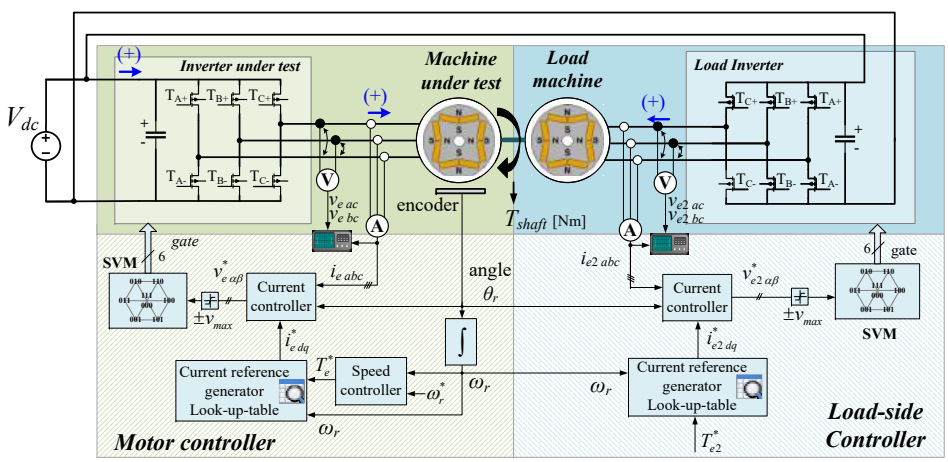


Fig. 6.9: Schematic of a PMSM test bench showing the circuit diagram of the topology and the structure of the control system

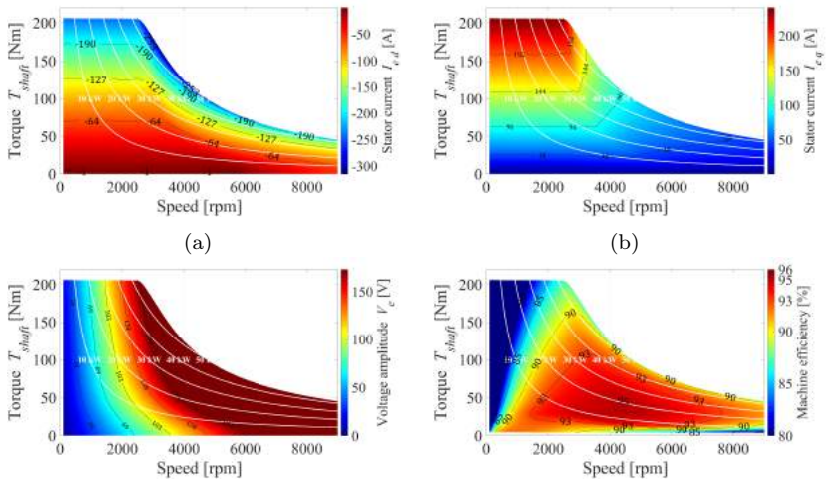
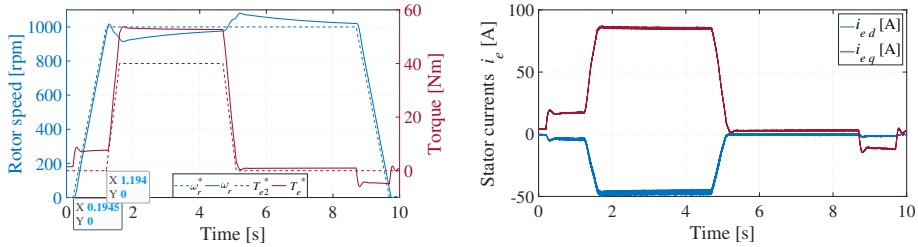


Fig. 6.10: Simulation results of the (a) d-axis current, (b) q-axis current, (c) stator terminal voltage amplitude and (d) efficiency map when stator copper loss is applied on the tested PMSM

Table 6.2: PMSM Rated Parameters & Control

Parameter	Value	Unit
Rated active power	30	kW
Peak active power	60	kW
Measured viscous damping b_{real}	$8.93{\cdot}10^{-4}$	Nm·s/rad
Static friction T_0	0.96	Nm
Shaft inertia J	0.047	kg·m^2
Number of pole pairs p	4	-
Stator resistance R_s	26.4	mΩ
No-load stator inductance L_d	0.44	mH
No-load stator inductance L_q	1.3	mH
Magnet flux linkage ψ_{md}	69.4	mWb
Inverter dc voltage V_{dc}	300	V
Inverter switching freq. f_{sw}	20	kHz
Current control bandwidth a_c	1000	rads/s
Speed control bandwidth a_ω	20	rads/s
Viscous damping (used only in the speed controller gains) b	0.02	Nm·s/rad



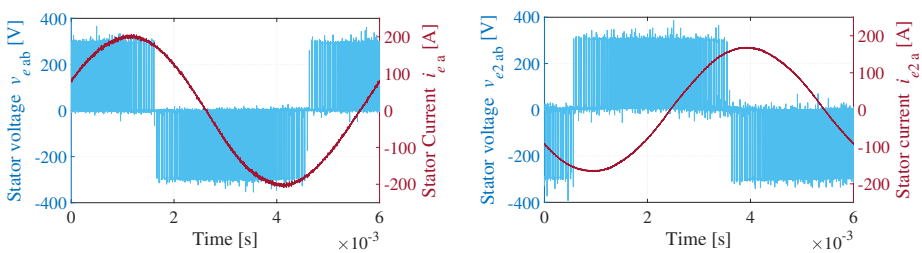
(a) (b)

Fig. 6.11: Ramp test of the PMSM drive with speed set to 1000 rpm and reference load torque $T_{e2}^* = 40$ Nm

T_e^* with red color. The torque T_{e2}^* is set to 40 Nm, while T_e^* is the output of the speed control loop and is equal to 53 Nm, because it supplies also the losses of the machine bench. Fig. 6.11(b) shows the measured stator currents of the machine-under-test $i_{e\,d}$ and $i_{e\,q}$.

Steady-state test results of the PMSM drive are shown in the following Fig. 6.12 and in Table 6.3. The input power of both machines is measured using two high-bandwidth voltage probes and two current probes at terminals of each machine for measuring with the oscilloscope the line-to-line voltages and currents. Sampling frequency of 2.5 MHz is used. Then, FFT is performed on the measured signals and the average power of the machines is calculated using the fundamental current and voltage.

Experimental tests with speed higher than 3000 rpm have not been possible to be conducted with the current laboratory set-up due to mechanical limitations of the machine test-bench.



(a) (b)

Fig. 6.12: Measured stator line voltage $v_{e\ \mathrm{ab}}$ and phase current $i_{e\ \mathrm{a}}$ from the (a) PMSM under test and (b) the load machine with $\omega_r = 2500$ rpm and $T_{e2}^* = 100$ Nm

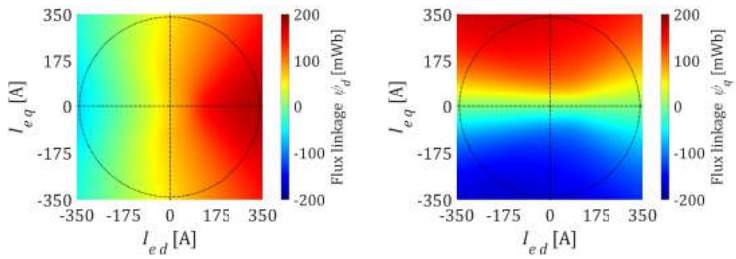
Table 6.3: PMSM Drive Steady-State Experimental Results

Reference load torque	ω_r 1000 rpm	ω_r 2500 rpm	ω_r 1000 rpm	ω_r 2500 rpm	ω_r 1000 rpm	ω_r 2500 rpm	ω_r 1000 rpm	ω_r 2500 rpm	ω_r 1000 rpm	ω_r 2500 rpm
T^*_{e2} [Nm]	T^*_e [Nm] ref. torque PMSM 1		$\hat{I}_{e\ (1)}$ [A] fundamental ph. current ampl.		$\hat{V}_{e\ (1)}$ [V] fundamental volt. ampl.		P_{e1} [kW] input power PMSM 1		P_{e2} [kW] input power PMSM 2	
0	1.01	5.29	3.17	13.68	27.30	66.46	0.1	1.17	0	0.01
20	25.94	27.41	53.46	55.98	28.84	66.48	2.29	5.49	-1.89	-4.90
40	50.80	54.24	93.24	97.57	34.39	76.51	4.75	11.11	-3.80	-10.07
60	76.07	79.30	129.63	133.22	38.86	87.41	7.25	16.67	-5.47	-14.92
80	98.88	103.45	162.41	167.54	43.77	97.43	9.87	22.33	-7.14	-19.71
100	121.24	125.23	195.15	198.97	47.88	108.12	12.53	28.04	-8.76	-24.56

6.3.2 Experimental Results of PMSM Emulator

The PMSM that has been tested in the previous subsection is now emulated on the P-HIL set-up of Fig. 6.8(b). The control diagram of the system can be seen in Fig. 6.2. The flux linkage maps of the machine obtained through FEM simulation of the PMSM, which are shown below in Fig. 6.13 as a function of the stator currents, are utilized in order to calculate the terminal voltage of the emulated machine. The same control parameters are used for the IUT, as with the PMSM drive previously reported in Table 6.2.

A three-phase inductor is installed at the ac-side of the topology with inductance $L_e = 0.55$ mH and resistance $R_e = 53$ mΩ. No common mode hardware filter has been installed in the system, since the circulating zero-sequence current is regulated



(a) (b)

Fig. 6.13: Flux linkage maps of the emulated PMSM

effectively with the common mode voltage control presented in Subsection 6.2.2.

PMSM Model Evaluation:
Accurate estimation of the machine mechanical and electrical parameters is important in order to emulate accurately the currents, voltages, speed and torque of the PMSM. Therefore, the general form of the mechanical dynamics equation (2.4) has been used here with static friction torque $T_0 = 0.96$ Nm, viscous damping $b_{real} = 8.93 \cdot 10^{-4}$ Nm·s/rad and inertia $J = 0.047$ kg·m^2. These parameters have been measured experimentally through dynamic response tests of the PMSM test-bench.

The fidelity of the PMSM emulator is evaluated with the following steady-state experimental results in comparison with the results of the previous subsection, where the real PMSM drive was tested. Due to the presence of common mode voltage and current, all the three phase voltages and line currents need to be measured with the oscilloscope in order to calculate accurately the power at the ac output of the IUT P_{e1}.

$$P_{e1} = \frac{1}{T_1}\int_0^{T_1} p_{e1}(t)\,dt = \frac{1}{T_1}\int_0^{T_1} [v_{eaN}(t)i_{ea}(t) + v_{ebN}(t)i_{eb}(t) + v_{ecN}(t)i_{ec}(t)]\,dt \tag{6.11}$$

where $p_{e1}(t)$ is the instantaneous active power and T_1 the fundamental period.

Time-domain results are shown in Fig. 6.14 for $\omega_r = 2500$ rpm and reference torque $T_e^* = 100.43$ Nm (for the emulator) and $T_e^* = 103.45$ Nm (for the real PMSM). More results are listed in Table 6.4.

It should be noted here that the load torque of the drive (first column of the table) is controlled differently in the PMSM emulator compared to the real PMSM and, therefore, these values do not correspond to the same operating point. In the emulator the T_L is a controllable input of the machine model (see Fig. 6.3) and the reference torque of the IUT T_e^* is the output of the speed control loop and is the sum of the load torque and the mechanical losses, represented by the viscous damping b_{real} and static friction T_0. As for the real PMSM drive, the load torque is regulated indirectly through the reference torque of the load machine T_{e2}^*. Therefore, the reference torque of the PMSM-under-test T_e^* is the sum of the T_{e2}^*, the losses of the load machine, the losses of the two inverters and the core losses of the PMSM-under-test. These losses have not been considered in the model of the machine emulator and a difference can be seen between the values of T_e^* for the same load torque in Table 6.3 and Table 6.4.

The PMSM torque would have been calculated more accurately, if the torque on

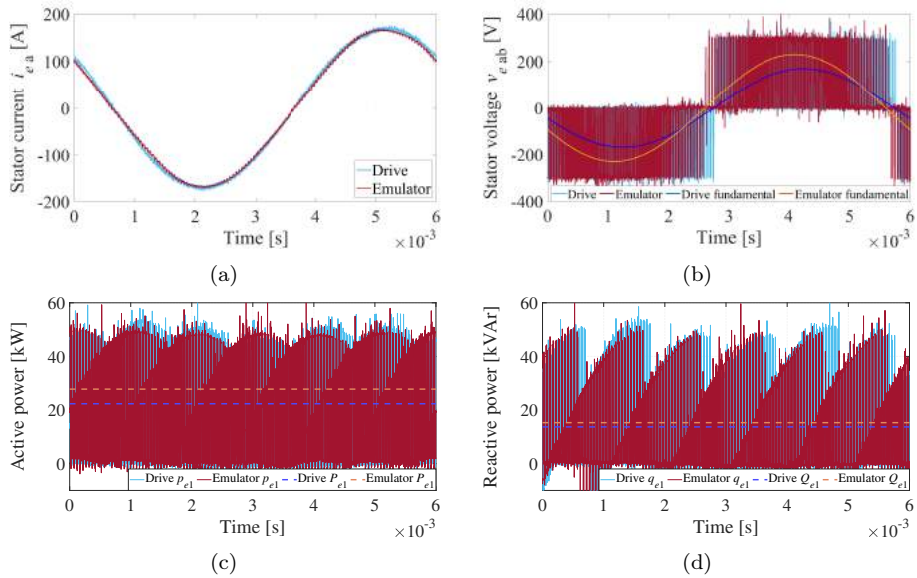


Fig. 6.14: Comparative results of the PMSM drive and emulator with $\omega_r = 2500$ rpm and reference torque $T_e^* = 100.43$ Nm (for the emulator) and $T_e^* = 103.45$ Nm (for the real PMSM drive)

Table 6.4: PMSM Emulator Steady-State Experimental Results

Emulated load torque T_L [Nm]	ω_r 1000 rpm	2500	ω_r 1000 rpm	2500	ω_r 1000 rpm	2500	ω_r 1000 rpm	2500
	T_e^* [Nm] ref. torque		$\hat{I}_{e\,(1)}$ [A] fundamental		$\hat{V}_{e\,(1)}$ [V] fundamental		P_{e1} [kW] input power	
	emulated	PMSM	ph. current ampl.		volt. ampl.		emulated	PMSM
0	0.76	0.80	2.42	2.71	31.49	75.26	0.11	0.30
20	21.65	21.66	45.23	45.36	39.28	89.35	2.29	5.94
40	40.50	40.48	78.57	78.64	46.47	107.52	4.75	11.55
60	60.46	60.43	108.26	108.43	51.03	119.27	7.25	17.03
80	80.43	80.42	137.10	137.44	54.18	127.40	9.87	22.44
100	100.43	100.43	166.22	166.69	56.46	132.17	12.53	27.76

the shaft of the machine T_{shaft} had been measured with a torque sensor. Then, the measured T_{shaft} would be similar with the load torque of the emulator T_L. However, this has not been possible during this project.

When operating points with the same reference torque T_e^* are compared, the current of the IUT in the machine emulator is almost identical with the real PMSM current. However, there is a discrepancy between the emulator and the drive voltage, with the first one being slightly larger. This can be attributed to error in the compensation of the voltage drop across the inductor L_e and also to wrong estimation of the machine flux linkage, since FEM data are utilized which vary from the real PMSM flux linkage. For example for the plotted operating point in Fig. 6.14, the fundamental current amplitude is 166.69 A for the emulator and 167.54 A for the drive (a difference of 0.5%), whereas the fundamental voltage amplitude is 132.17 for the emulator and 97.43 V for the drive. More accurate estimation of the inductance value L_e and measurements of the flux linkage of the PMSM could reduce this error in the voltage.

Common Mode Voltage Control Evaluation:
The proposed common mode voltage control of the machine emulator is validated with experimental results at various operating points of the emulated PMSM. Two versions of the machine emulator are tested. One with just a PI-controller-based zero-sequence regulator (as shown in Subsection 6.2.1), named as "SVM1" in the following results. The second version of the system has the proposed zero-sequence compensated SVM (as shown in Subsection 6.2.2) and is named "SVM2". There is no common mode hardware filter in any of the systems examined.

The PI-regulator of the common mode voltage controller in both cases has bandwidth equal to $a_{0seq} = 10a_c = 10000$ rad/s. The individual gains are selected based on (6.5).

Firstly, the response of the emulator is tested without any common mode voltage control and the results are shown in Figs. 6.15(a)-(b) for $\omega_r = 500$ rpm / $T_e^* = 41$ Nm and in Figs. 6.15(c)-(d) for $\omega_r = 3000$ rpm / $T_e^* = 61$ Nm. The zero-sequence current is proportional with the voltage difference between the IUT and the emulator converter ($V_{e0} - V_{em0}$), since only the equivalent resistance of the resultant loop limits the current. Therefore, the second tested case with the higher emulated speed has also higher i_0, since the power of the system and the inverter voltage in the second case are higher. Based on these results it is clear that controlling the common mode voltage in order to reduce the circulating current is necessary in order to have safe operation of the machine emulator.

The performance of the two systems with "SVM1" and "SVM2" is evaluated with the comparative experimental results of Figs. 6.16-6.18. The response of the system during one fundamental period at three operating points is demonstrated.

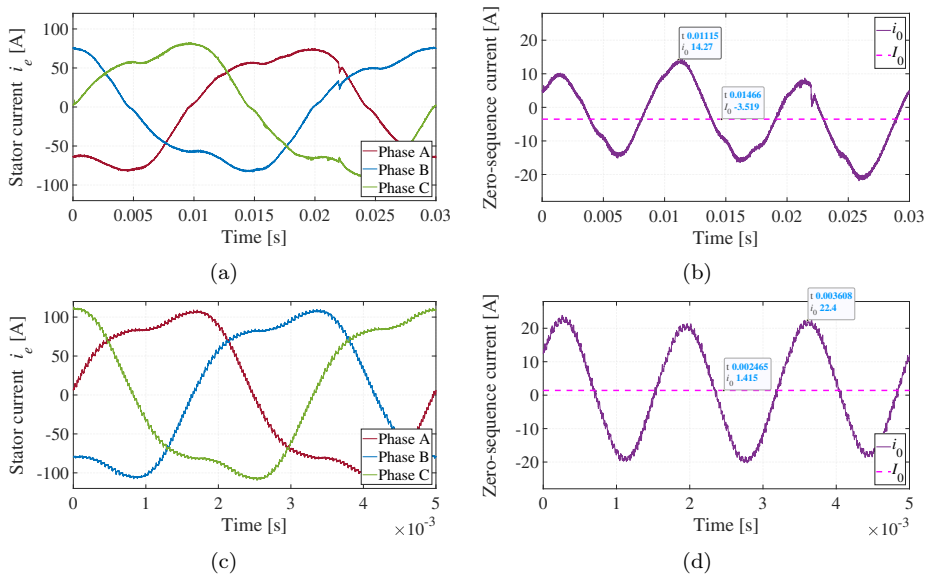


Fig. 6.15: PMSM emulator phase current $i_{e\,\mathrm{a}}$ and zero-sequence current i_0 with no control of the common mode voltage when (a)-(b) $\omega_r = 500$ rpm / $T_e^* = 41$ Nm and (c)-(d) $\omega_r = 3000$ rpm / $T_e^* = 61$ Nm

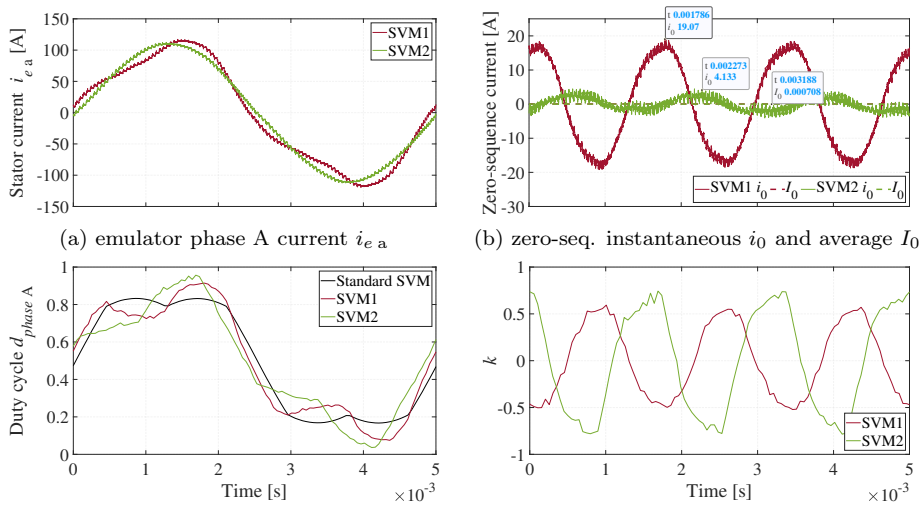
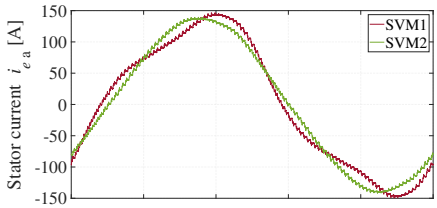
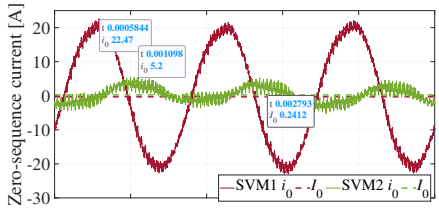


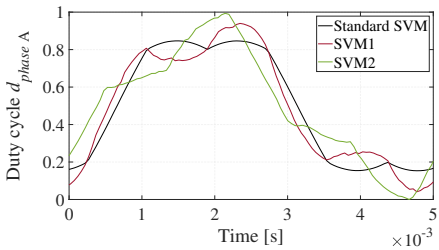
Fig. 6.16: Comparative results of the "SVM1" and "SVM2" when $\omega_r = 3000$ rpm / $T_e^* = 61$ Nm and modulation index of emulator inverter $m_{a\,em} = 0.66$



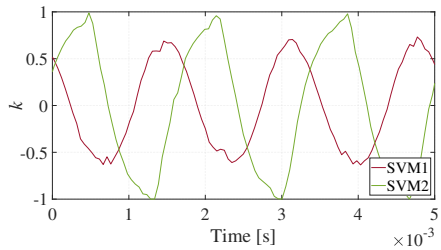
(a) emulator phase A current $i_{e\,a}$



(b) zero-seq. instantaneous i_0 and average I_0

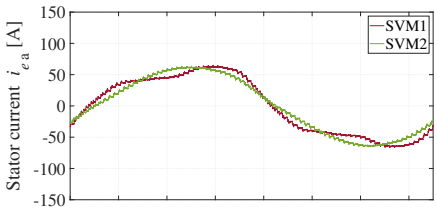


(c) duty cycle of the emulator converter

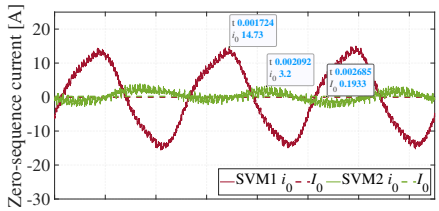


(d) common mode ref. voltage k (in per-unit)

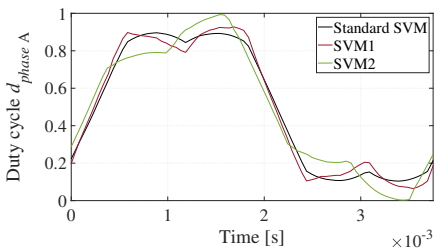
Fig. 6.17: Comparative results of the "SVM1" and "SVM2" when $\omega_r = 3000$ rpm / $T_e^* = 81$ Nm and modulation index of emulator inverter $m_{a\,em} = 0.69$



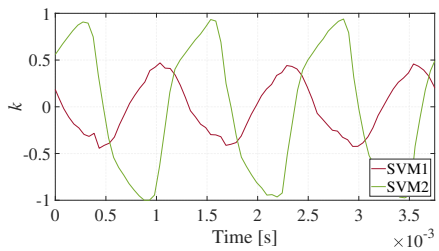
(a) emulator phase A current $i_{e\,a}$



(b) zero-seq. instantaneous i_0 and average I_0



(c) duty cycle of the emulator converter



(d) common mode ref. voltage k (in per-unit)

Fig. 6.18: Comparative results of the "SVM1" and "SVM2" when $\omega_r = 4000$ rpm / $T_e^* = 31$ Nm and modulation index of emulator inverter $m_{a\,em} = 0.79$

At $\omega_r = 3000$ rpm / $T_e^* = 61$ Nm / $m_{a\,em} = 0.66$ (Fig. 6.16) and $\omega_r = 3000$ rpm / $T_e^* = 81$ Nm / $m_{a\,em} = 0.69$ (Fig. 6.17) the emulated machine speed is lower than the base speed. Fig. 6.18 shows the results for $\omega_r = 4000$ rpm / $T_e^* = 50$ Nm /

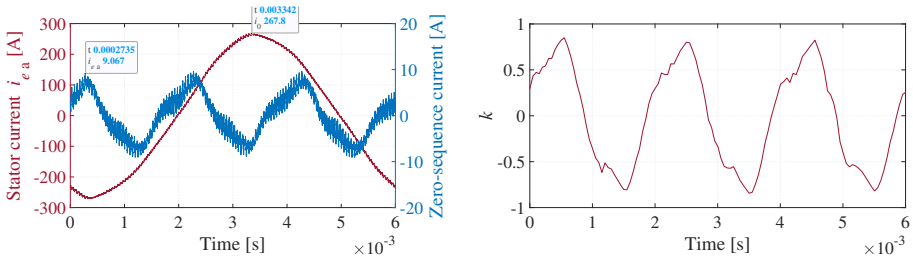
$m_{a\,em} = 0.79$, which belongs to the high-speed operating region of the PMSM. In all three cases the control scheme "SVM2" performs better and keeps the current i_0 much lower than the "SVM1".

Specifically in the first tested case of Fig. 6.16(b), the peak of i_0 equals 3.7% of the phase current amplitude for the "SVM2", while it is equal to 16.7% of the phase current amplitude for the "SVM1", which is a 78% reduction. This results to more sinusoidal current $i_{e\,\mathrm{a}}$ for the "SVM2", which is closer to the stator current of the real PMSM. A large amount of third-harmonic component is present in the current when using the "SVM1" controller. The common mode reference voltage k in Fig. 6.16(d) has similar amplitude for both control schemes. However there seems to be a phase difference between the two variables, which is the reason why the PI-based "SVM1" is not as effective as the "SVM2". The "SVM2" generates the correct amplitude and angle for the common mode voltage, so that the zero-sequence current can be suppressed.

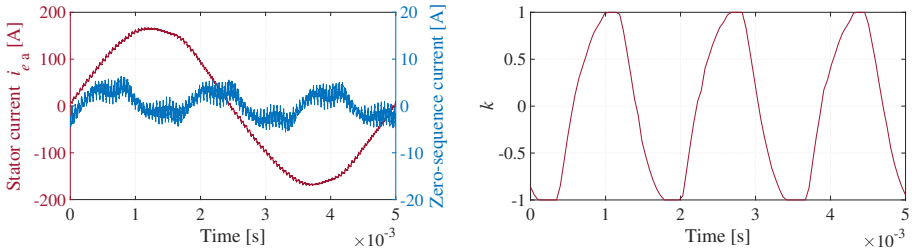
The k generated by "SVM2" starts to have larger amplitude than the one generated by "SVM1" and approaches the limits of $[-1, 1]$ in Figs. 6.17(d) and 6.18(d) as the modulation index of the emulator inverter increases, which complies with the simulation results of Subsection 6.2.3.

Further experimental results are shown in Fig. 6.19 of operating points with even higher modulation index for the emulator converter. As seen in Fig. 6.19(b),(c) the controller reference voltage k gets saturated at ± 1, since the proposed common-mode-voltage-compensation scheme "SVM2" approaches its theoretical limit (based on Subsection 6.2.3). However, the zero-sequence current still remains low, with peak values 9.1 A, 6.3 A and 3.3 A (3.3%, 3.8% and 7% of the ac current amplitude, respectively).

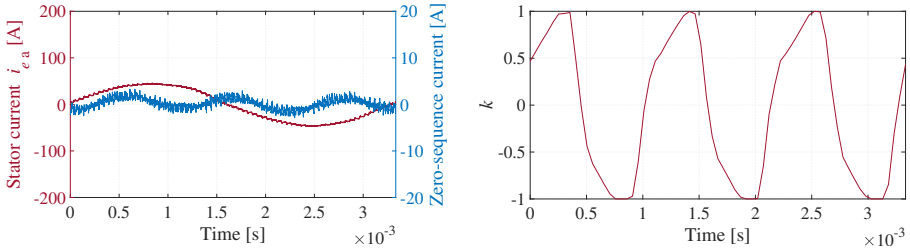
It has not been possible to test operating points on the PMSM operating map with even higher voltage, since the voltage limit of the IUT had already been reached in Fig. 6.19, as seen by the modulation index of the IUT $m_{a\,e}$. However, it is expected that the common mode voltage controller of "SVM2" would be even more saturated and the resultant i_0 would gradually increase, if $m_{a\ em}$ closer to 1 is used.



(a) $\omega_r = 2500$ rpm / $T_e^* = 161$ Nm / $m_{a\,em} = 0.64$ / $m_{a\,e} = 0.84$



(b) $\omega_r = 3000$ rpm / $T_e^* = 101$ Nm / $m_{a\,em} = 0.72$ / $m_{a\,e} = 0.94$



(c) $\omega_r = 4500$ rpm / $T_e^* = 21$ Nm / $m_{a\,em} = 0.84$ / $m_{a\,e} = 0.93$

Fig. 6.19: Results of the PMSM emulator with "SVM2" as the common mode voltage control scheme

6.4 Summary

This chapter has presented the design process and control of a P-HIL set-up with 2-level inverters for emulating the operation of a PMSM. The P-HIL set-up consists of two identical converter, named as inverter-under-test (IUT) and emulator VSC, that share the same dc-link and are connected also at the ac side through a three-phase inductor.

The "inverted" machine modelling approach has been followed, where the machine is modelled with its analytical voltage, speed and torque equations. The machine response is modelled by the resultant voltage which is generated by the emulator

converter. The modelling process of the PMSM has been explained and experimental results on a test-cases PMSM emulator are shown in comparison with a real PMSM drive. The current of the PMSM for each individual torque/speed point is emulated with high accuracy with error as low as 0.5%. However, the terminal voltage of the PMSM is emulated with larger error, which is attributed to inaccuracies of the imported machine parameters and the voltage drop across the inductor that exists in the P-HIL set-up.

A control technique is also presented for suppressing the zero-sequence current that naturally flows in this P-HIL topology. The proposed controller consist of a combination of a PI-regulator and on-the-fly compensation of the common mode voltage in the SVM block of the emulator converter. Experimental results have verified the effectiveness of the proposed control, which is also compared with a simpler common mode voltage controller consisting only of a PI-regulator. The proposed control scheme limits the zero-sequence current amplitude to 3.3% of the main phase current amplitude, when active power of the PMSM equal to 42 kW and its base speed are emulated.

Chapter 7

Electrical and Thermal Design of Automotive SiC Inverter

The design process of a three-phase, 2-level inverter intended to be used in automotive applications is studied in this chapter. The design specifications of motor drives for electric vehicles are firstly analyzed. Then, a prototype SiC inverter is manufactured based on these specifications. This inverter has been used with the experimental set-up of the previous Chapter 6.

7.1 Design Specifications

The electric drive, including the motor and its inverter, is one of the core components of an electric vehicle. Electrification of ground vehicle transportation has been a fast-growing research area and market in the recent years and the electric drive is one of the main research points. Correct dimensioning of the drive and selection of its components is of high importance in order to meet effectively the design requirements of the application.

The design specifications vary depending on the application where the vehicle is being used. The basic classification of vehicles based on their mass is between light- ($\leq$ 3855 kg) and heavy-duty vehicles ($>$ 3855 kg), according to EPA [160]. The same distinctions exist also from other governmental authorities, such as in [161] for the EU. Passenger vehicles, vans and minivans belong to the light-duty vehicles, while trucks, buses and coaches are heavy-duty vehicles. Off-road vehicles is another special classification.

7.1.1 Design Specifications for Light-Duty Vehicles

A detailed analysis of the legislation and the design assessment of drives for light-duty vehicles can be found in [162]. The first step in the design of the drive is the modelling of the vehicle's motion, such as the forces applied on the wheels and the acceleration. The acceleration $a_{vehicle}$ is described as

$$m\ a_{vehicle} = m\ \frac{\mathrm{d}v_{vehicle}}{\mathrm{d}t} = F_{acc} \tag{7.1}$$

where m [kg] is the equivalent mass of the moving object. The acceleration force is calculated as

$$F_{acc} = \frac{T_{motor}}{r}\, gear\, n_{gear} - F_{road\,load} \tag{7.2}$$

where $gear$ and n_{gear} are the gear ratio and efficiency of the transmission system, respectively. The wheel radius is defined as r and the load of the wheels is $F_{road\,load}$. The $F_{road\,load}$ consists of the air drag F_{air}, the rolling resistance F_{roll} and the grading force of the road F_{grade}. These are described as

$$F_{air} = \frac{1}{2}\,\rho_{air}\,C_d\,A\,(v_{vehicle} - v_{wind})^2 \tag{7.3}$$

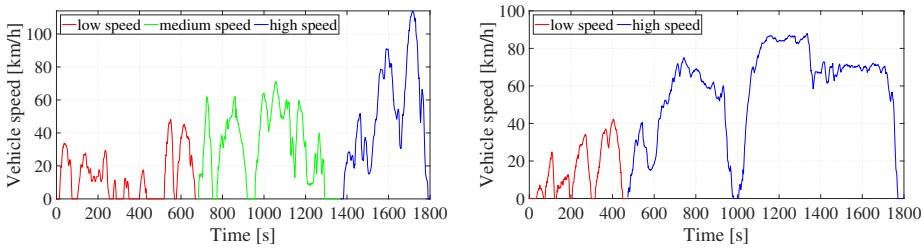
$$F_{roll} = C_r\,m\,g\,cos(\alpha) \tag{7.4}$$

$$F_{grade} = m\,g\,sin(\alpha) \tag{7.5}$$

where $v_{vehicle}$ and v_{wind} [m/s] are the forward speed of the vehicle and the wind, g [m/s^2] is the gravitational acceleration and $\alpha = \tan^{-1}(\frac{\%road\_slope}{100})$ [rad] is the road angle of inclination. C_d is the aerodynamic drag, C_r the rolling resistance and A [m^2] the effective cross sectional vehicle area, which are parameters specific for each vehicle. The parameter A depends on the frontal area of the vehicle and for this study it is set equal to $A = 86\% \cdot height \cdot width$, as referenced from [162].

There are many testing procedures suitable for light-duty vehicles, as described in [163–165]. The vehicle-under-test, modelled with (7.1)-(7.5), can be simulated when these tests are applied. The acceleration test determines the maximum acceleration and the maximum speed that can be maintained by the electric drive of the vehicle for different road slopes. Similarly, deceleration tests would determine the response of the vehicle to the road load force.

Standardized tests with legislative driving cycles is another method of examining the vehicle operation, when it operates with a predefined speed profile. These cycles represent the average driving pattern of the users and traditionally they have been used to calculate the fuel consumption and emissions of non-electric vehicles. In the case of electric vehicles, these cycles can be utilized to simulate the



(a) (b)

Fig. 7.1: China automotive test cycles (a) for passenger vehicles (CLTC_P) and for (a) for large heavy-duty vehicles (CHTC_TT)

load of the electric drive, as well as the aging of these components. There are many cycles suitable for light-duty vehicles, such as the Worldwide Harmonised Light Vehicles Test Cyle (WLTC) [166], which is currently the main drive test procedure in many countries, the New European Driving Cycle (NEDC), the ARTEMIS [167], etc. A new standard has also been developed by the China-Automotive-Test-Cycle program, and has been implemented in China in May 2020. New driving cycles are introduced by this standard for each vehicle category and the one corresponding to the passenger vehicles is named CLTC_P [168]. The speed profile of that cycle is shown in Fig. 7.1(a) and will be further studied in this chapter.

7.1.2 Design Specifications for Heavy-Duty Vehicles

There are some distinctive differences in the requirements of the electric drive design for heavy-duty vehicles, like long-haul trucks, compared to light passenger vehicles. A high peak torque is required in the low-speed operating region in order to startup the vehicle [169]. A wide speed range with high power at the flux weakening region is needed [170], since the drive operates frequently and for a long duration close to its rated power, especially when the truck is driven on a road with large uphill slope or on the highway with a constant speed close to its limit.

The most common operating conditions of a truck are summarized in Table 7.1.Firstly, the start-up conditions of the drive require a high peak torque in order to be able to accelerate the vehicle from standstill while being on a road with slope. The "high power operation" corresponds to driving on an uphill road and the "best efficiency operation" is the high-speed driving condition on a highway, which is the most common for long-haul trucks. The numbers in this table are given as an example for a 40 tonnes vehicle, with peak power 500 kW and maximum speed

Table 7.1: Test-Case Truck Electric Drive Operation Requirements

Parameter	Value	Unit
(1) Start-up Operation with Peak Torque		
Duration	5	min
Road slope	12	%
(2) High Power Operation		
Duration	20	min
Power	400	kW
Road slope	6	%
Vehicle speed	50	km/h

Parameter	Value	Unit
(3) Best Efficiency Operation		
Duration	for a long time	
Power	100	kW
Road slope	0	%
Vehicle speed	80	km/h

100 km/h. This test-case has been studied with more details in [1] .

Typical driving conditions of large trucks can also be modelled with suitable driving cycles, such as the CHTC_TT, shown in Fig. 7.1(b).

7.2 SiC 2-Level Inverter Design Requirements

Two SiC 2-level inverters with identical layout have been designed in this project satisfying the previously mentioned specifications of electric vehicles in terms of power capability. Based on current industry trends in motor drives for BEVs, 800 V rated dc voltage and approximately 200 kW rated active power (250 kW peak) of the prototypes have been selected. The 2019-released SiC power modules of the XM3 half-bridge family [159], manufactured by Wolfspeed, satisfy these requirements and at the same time they offer small form-factor and low parasitic inductance enabling high-speed switching with low voltage ringing.

The CAB450M12XM3 module has been used in one of the prototypes (named as "IUT" in Chapter 6) that is optimized for low-conduction losses with a switching frequency of 10 to 20 kHz, typical values for automotive drives. The second prototype has CAB425M12XM3 modules, which are more optimized towards high switching frequency and is used as the "machine emulator inverter" in Chapter 6.

The dc-link capacitors of the inverter are responsible for filtering out the current ripple caused by the PWM switching pattern, so that the dc-side source can supply

[1] G. Mademlis, Y. Liu, J. Tang, L. Boscaglia, and N. Sharma, "Performance Evaluation of Electrically Excited Synchronous Machine compared to PMSM for High-Power Traction Drives", in *Proc. 24th International Conference on Electrical Machines (ICEM)*, August 23-26, 2020, pp. 1793-1799.

clean current without any harmonics. Correct sizing of the dc-link capacitor bank in terms of current ripple capability, voltage rating and capacitance is important in order to avoid overheating of the capacitors and to filter effectively all the harmonics. Based on the literature [171–173], film capacitors are the optimal choice for automotive applications compared to electrolytic ones due to their lower ESR ratings, leading to much better handling of the fast-switching current ripple and higher inverter efficiency. They also have smaller size and higher efficiency, due to their self-healing capability. Ceramic capacitors can also be a candidate for even lower ESR and better high-frequency capabilities [174, 175], however, with a much higher cost than film capacitors.

The rms ac current of a three-phase inverter, modulated with SVM, having dc-link voltage V_{dc}, line-to-line rms voltage $V_{e\ rms}$ and ac-side power P_e can be calculated as

$$I_{e\,rms} = \frac{P_e}{\sqrt{3}\ n_{inv}\ PF\ V_{e\,rms}} \overset{(4.8)}{=\!=} \frac{P_e}{\sqrt{3}\ n_{inv}\ PF\ \frac{0.98 V_{dc}}{\sqrt{2}}} \tag{7.6}$$

where PF is the power factor, n_{inv} the inverter efficiency and 0.98 is the a maximum allowed modulation index.

The current stress of the dc-link capacitors depends on the power factor and the power rating of the inverter. The worst-case capacitor current $I_{c\,rms}$ for inverters controlling a PMSM can be estimated as follows [176]

$$I_{c\,rms} \approx \frac{1}{\sqrt{2}} I_{e\,rms} \tag{7.7}$$

Considering $P_e = 250$ kW, $n_{inv} = 0.93$, $PF = 0.93$ and $V_{dc} = 800$ V, the capacitor current requirement of the inverter is $I_{c\,rms} = 213$ A.

The required capacitance of the dc-link is determined by the allowed voltage ripple

$$C_{dc\,min} = \frac{T_s \sum_{t=0}^{T_s} \Delta i_{c\,ripple}}{\Delta V_{dc\,max}} \tag{7.8}$$

where $\Delta V_{dc\,max} = 5\% V_{dc}$ is the maximum ripple of the dc voltage. The resultant lowest required capacitance is equal to $C_{dc\,min} = 77$ µF for switching frequency 20 kHz.

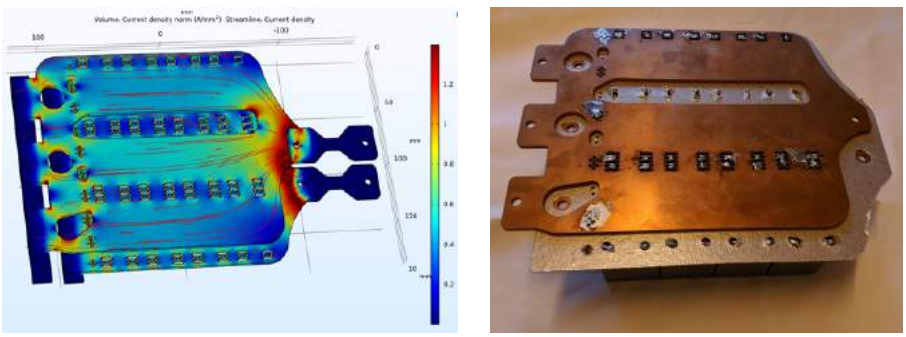
Considering the above calculations and the stock availability at the time when the prototype was built, automotive-graded film capacitors from KEMET with product code C4AQQBW5400A3NJ were selected. These capacitors have ratings 1.1 kV, 40 µF, $I_{c\,rms,10kHz} = 18$ A and $R_{ESR,10kHz} = 4$ mΩ. In order to satisfy

the current requirement of 213 A, 12 pieces of this capacitor connected in parallel are needed.

As can be observed by the rated parameters of the selected product, the equivalent capacitance of the inverter is over-dimensioned, since $12 \cdot 40\mu\text{F} >> C_{dc\,min}$. This shows that the main design limitation when selecting film capacitors for low-voltage and high-current inverters is the capacitor current. As highlighted in [177], the current-carrying capability of film capacitors needs to be further increased by future research, in order to allow the design of SiC inverters with even higher power density. On the other hand, it is easier to satisfy the capacitor current specifications of higher-voltage inverters, such as with the NPC inverter prototype of Subsection 5.2.3.

7.3 DC-Link Capacitor Bank Design

The 12 selected film capacitors need to be connected to the dc terminals of the power modules and in parallel with each other. It is important the capacitors to be connected with the lowest possible parasitic resistance and inductance (ESR and ESL) in order to avoid voltage ringing. A special design of 3 mm-thick copper bars is made, connected to the DC+ and DC- terminals, so that the round pins of the capacitors can be soldered there. FEM simulations of the copper bars are conducted, as seen in Fig. 7.2(a), in order to calculate the resultant current density and to make sure that areas with too high current density are avoided.



(a) current density distribution in A/mm^2 (b)

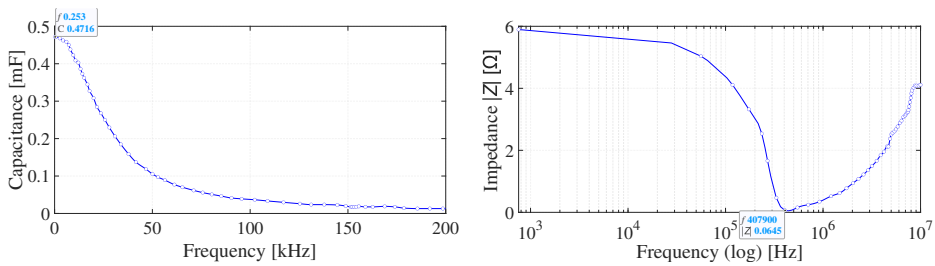
Fig. 7.2: DC-link copper bars (a) FEM simulated with COMSOL when 400 A dc current is applied between the left and the right side of the bars and (b) the capacitor bank after being soldered

High current density is just observed on the right side of the bars, close to the dc-link terminals.

It is also possible to use capacitor banks that are pre-assembled in brick structures, as seen in [178]. However, there has not been any suitable brick capacitor available that could fit the terminals of the specific SiC power modules. A different approach with a combination of aluminium plates and PCB for soldering the capacitors has been presented in [174]. However, such designs are not suitable for the power ratings of this project.

It is important to solder the capacitors with high-enough temperature, so that a proper joint is built between the soldering material and the copper. Cold-soldering should be avoided, since it would cause additional contact resistance increasing the ESR of the capacitors and the joint can also break easily. Many capacitor pins seem not to be properly soldered on the copper busbars of Fig. 7.2(b), which are reheated and fixed at a later stage. Standard soldering material with Sn-Pb alloys melts at around 180-190°C. Solder wire with different materials that have lower melting point, such as indium-based alloys, can also be used.

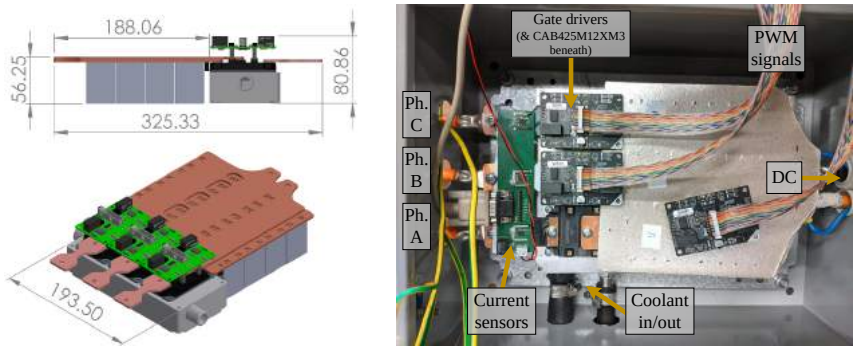
The equivalent parallel capacitance and impedance of the final version of the distributed capacitor bank is measured with an LCR meter and the results are shown in Fig. 7.3 for a wide frequency range. The measured capacitance at dc frequency is 471.6 µF, which is close to the theoretical value of 480 µF. The impedance waveform is typical for film capacitor banks [179]. In low-frequency regions the measured impedance decreases slowly and inversely with frequency up to the resonance point of 408 kHz, where it reaches a minimum impedance value $\mid Z_{min} \mid = R_{ESR} = 6.5$ mΩ. For frequencies higher than the resonant frequency, the capacitor bank has inductive performance.



(a) (b)

Fig. 7.3: Measurements with LCR meter of the equivalent (a) capacitance and (b) impedance versus applied frequency

The final assembled inverter is shown in Fig. 7.4, when mounted inside a metal enclosure for better EMI shielding. A current sensor PCB has also been designed and mounted at the ac side of the inverter, having the Hall-effect sensors ML91208 from Melexis. The main advantage of these sensors is their small footprint; however, they are susceptible to EMI and have lower accuracy than other closed-loop sensors.



(a) dimensions in mm (b)

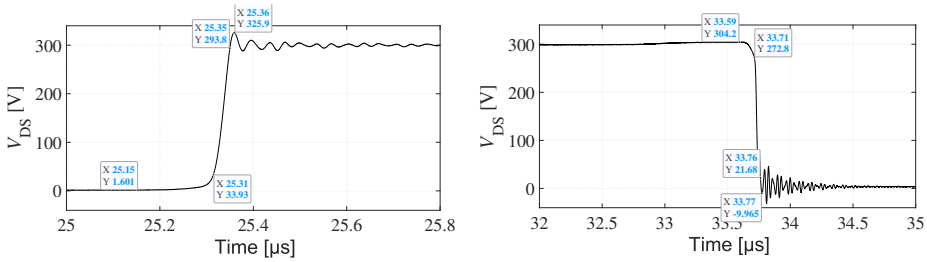
Fig. 7.4: Prototype SiC inverter with XM3 half-bridge power modules: (a) CAD drawing showing its outer dimensions and (b) the final assembled inverter

Considering the above dimensions of the inverter and a peak power of 250 kW, the resultant power density is 250kW/5.107liters = 48.9 kW/liter. The weight of the inverter is estimated to 5.1 kg through calculations on the CAD model, therefore the power-to-weight ratio is 49 kW/kg. These numbers are within the usual power densities reported in [177] for SiC inverters. It should be noted that the MCU board for controlling the switches and the housing of the inverter are not included in these calculations.

The switching transient of the SiC MOSFETs is examined in Fig. 7.5 in order to evaluate the inverter design. The drain-source voltage V_{DS} of the bottom switch of phase B is shown when 300 V dc-link voltage is applied and 148 A current passes through. As seen in the Fig 7.5(a), there is a low voltage overshoot of 25.9 V (8.6% of the applied dc voltage) and $\mathrm{d}v/\mathrm{d}t$ equal to 7.4 kV/µs during the turn-off switching transient. The low voltage overshoot verifies that the designed dc-link has successfully maintained low parasitic inductance between the capacitors and the switches. The $\mathrm{d}v/\mathrm{d}t$ has been calculated with the following formula, as cited from [180]

$$\frac{\mathrm{d}v}{\mathrm{d}t} = \frac{0.8V_{DS\,peak}}{t_r} \tag{7.9}$$

where t_r is defined as the time required for the voltage to rise from 10% to 90% of



(a) (b)

Fig. 7.5: Experimental measurements of the drain-source voltage of phase B bottom switch with 300 V dc voltage and 148 A current during (a) turn-off and (b) turn-on transient

its peak value. The measured rise time equals 35.1 ns for the turn-off transient shown in Fig. 7.5(a). External gate resistance $R_G = 1\ \Omega$ (additionally to the internal gate resistance of the module 2.5 Ω) is used for this inverter.

7.4 Design of Liquid Cooling System for Inverters

Optimizing the heatsink design of a liquid-cooled automotive inverter is an important step that can lead to more compact drivetrains with least possible material expense and longer life cycles. This would allow the development of more efficient packaging of automotive drives [181, 182].

The standard package layout of wire-bonded power modules used nowadays in high-power inverters is composed of multiple layers of materials between the die, which needs to be cooled, and the heatsink, in order to electrically isolate these two points. This structure is called direct bond copper (DBC) and consists of the following layers [183, 184]:

- a copper layer is soldered beneath the the semiconductor die,
- the ceramic substrate is placed beneath, which is made of an electrically insulating and thermally conductive material, such as the AlN,
- a second copper layer follows and
- the baseplate is soldered at the bottom of the whole module, which consists of a thicker piece of copper or aluminium. The heatsink is placed at the bottom side of the baseplate, which is called the case of the module

There are power modules recently released that do not have a baseplate, but

the heatsink is connected directly to the bottom side of the second copper layer, such as the Easy power module family from Infineon [185] and the WolfPACK from Wolfspeed [186]. The main advantages of this structure is the reduced cost of the device due to the absence of the thick baseplate and the better thermal conductivity [187].

In most of the available literature, heatsinks are dimensioned for maximum load, as in [188]. However, the inverter may never reach these limits under normal driving conditions of a passenger BEV. Despite this, steady-state CFD simulations are often utilized in similar thermal modelling studies [181, 189–194], which do not represent the reality, since the load of the drive is constantly varying.

Long real-time thermal simulations of the inverter heatsink are necessary in order to evaluate the temperatures of the designed system under transient load and to evaluate its efficiency and reliability. These simulations are implemented with equivalent and simplified models in [195–198], which cannot represent the thermal behavior of the semiconductor devices and the coolant flow inside the heatsink. Quasi-transient CFD modelling has also been used in [199, 200] in order to reduce the computational load. However, the results are not as realistic as in the fully transient 3D CFD approach.

The sizing of the heatsink involves a multidisciplinary approach in order to capture all the physical properties for thermal conditioning of the electric components. The thermal performance of the inverter can be studied more accurately with 3D Conjugate Heat Transfer (CHT) computations, where both fluid and solid elements in thermal contact are handled. The turbulence of the fluid, which is a strictly 3D mechanism, should also be modelled for accurate results. From the above it is concluded that an effective and practical thermal design technique, specially tuned for the cooling component of automotive SiC high-power inverters, is missing from the technical literature. Time-varying 3D CHT modelling has also not been utilized yet as the design tool for the inverter heatsink.

This section presents a new iterative heatsink design tool based on the transient 3D CHT computation technique, where the cooling plate geometry of the SiC inverter in Fig. 7.4(a) is fine-tuned in order to meet the specific needs of a BEV.

7.4.1 Overview of Cooling Plate Geometries

The main objectives for the heatsink design are

- to have good heat dissipation ability

- the pressure drop of the coolant to be kept as low as possible, since the inverter is usually cooled in the same cooling loop with the motor. A typical limitation for an automotive inverter can be set to 150 mbar, as referenced from [8].
- to have uniform heat dissipation at the contact surface with the power modules, so that the case-surfaces of all the three power modules experience similar thermal conditions and, therefore, the same aging. Inhomogenous cooling of the semiconductor chips would lead to a temperature gradient [191, 201] affecting the lifetime of each switch [202].
- manufacturability with low-cost techniques [192], such as machining and forging, without using special tools or more expensive solutions.

Cooling plates with simple straight channels extruded or machined in the aluminium plate have been traditionally been used in commercial inverter heatsinks [191, 194]. These designs have simple structure and, consequently, low manufacturing cost. However, they cannot be easily optimized for high power density applications where advanced thermal characteristics with low pressure drop of the coolant are required.

Therefore, heatsinks with more sophisticated structure, accommodating multiple fins, have been developed in order to enhance the heat transfer capability between the semiconductors and the coolant. These fin geometries can be found in the design of the baseplate for direct-cooled power modules [203], as well as in cooling plates for power module packages with flat baseplate that require thermal grease for better heat conductivity. There are heatsinks with straight [193] and wavy [204] fin shapes that manage to enhance the heat transfer coefficient between the plate and the coolant, due to increased mixing of the coolant liquid.

Plate designs with pins of different shapes and sizes have also shown to attain good cooling performance with high convective heat transfer coefficient. Pin-fins with round shape are studied in [205] and rectangular pins are shown in [191]. More advanced pin-shapes are proposed by Danfoss [191] and MicroCool [192], which also require a more special, custom manufacturing process. A certain method to optimize the shape of the fins and inner layout of the cooling plate needs to be followed for each study, using a parametric analysis of the key dimensions of the design [201] or iterative optimization algorithms as in [181].

7.4.2 CHT Computation Approach with Steady-State Heat Load [2]

At this step of the design process, multiple heatsink geometries are investigated and simulated with constant heat dissipation. A total power loss of 4 kW has been selected for all the three power modules and coolant flow speeds vary between 2.5 l/min and 10 l/min. A full 3D CFD model is used to simulate the heatsink of the inverter. The simulation toolbox is OpenFOAM [206] and the solver is named *chtMultiRegionSimpleFoam*, which is suitable for steady-state CHT computations.

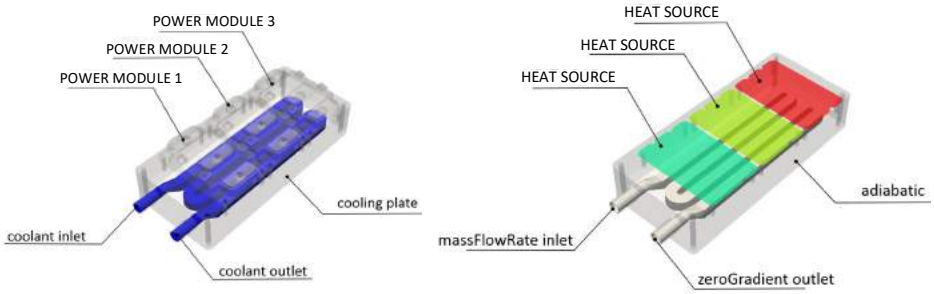
The investigated computational domain comprises individual meshes for the coolant and the heatsink, as shown in Fig. 7.6(a). The following input parameters have been considered:

- The coolant is a mixture of 50% water and 50% ethylene glycol and the solid material is aluminium.
- The coolant inlet temperature is selected equal to 300 K (or 26.85^o) for the results of this subsection.
- The developed inverter is intended to be used together with the liquid-cooled PMSM studied previously in Chapter 6, which has coolant inlet nozzle with inner / outer diameter 14 / 19 mm.
- The outer dimensions of the inverter heatsink are $L \times W \times H = 193.5 \times 85 \times 37$ mm. Further parameters, such as mass and material properties of the heatsink, are provided by the CAD drawing of the heatsink [see Fig. 7.4(a)].

The boundary conditions of the simulation are designed so as to represent the three power modules of the three-phase inverter as surface patches on the sink that have an evenly distributed heat source, with total thermal power of each patch equal to 4/3 kW. The mean temperature of each of these rectangular patches, being averaged at the surface of the heatsink, is shown as T_{sw1} up to T_{sw3} in the following simulation results.

The first design candidates is a standard cooling plate with straight cooling channels as shown in Fig. 7.7. In order to be able to fit 2-loops of the straight rectangular channels in the given cooling plate dimensions, the inlet diameter has been selected to be equal to $d_1 = 9$ mm and the spacing between the channels

[2] More details can be found:
G. Mademlis, R. Orbay, Y. Liu, and N. Sharma, "Designing Thermally Uniform Heatsink with Rectangular Pins for High-Power Automotive SiC Inverters," in *Proc. IECON 2020 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1317-1322.

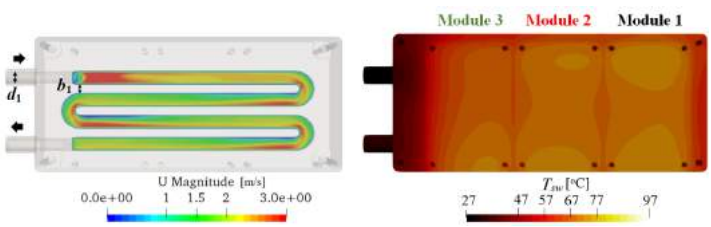


(a) (b)

Fig. 7.6: First investigated heatsink candidate showing (a) the cooling plate (grey) and the cooling circuit (blue) and (b) the boundary conditions for the CHT modelling of the heatsink.

is $b_1 = 5.42$ mm. A straightforward disadvantage of this heatsink design is the different nozzle diameter compared to the motor of the drive. As seen also in Fig. 7.7(b), there is a temperature gradient on the surface of the heatsink, with the power module 1 on the right side experiencing the highest temperature.

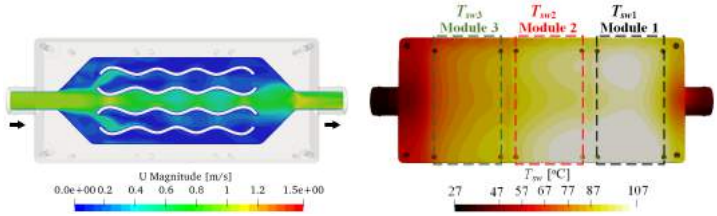
The second heatsink geometry studied is with multiple fins placed along the flow of the coolant similar to the design presented in [207] and it is shown in Figs. 7.8-7.9. The inlet diameter for all the following designs is 19 mm and the coolant enters from the left side of the cooling plate and exits at the right side. The design in Fig. 7.8 has four wave-shaped fins in order to increase the surface area between the coolant and the plate and to introduce turbulence which would further enhance the cooling performance. The main challenge in this design is to split the coolant flow after it enters the plate into the five resultant channels. This is not done



(a) (b)

Fig. 7.7: Initial heatsink design candidate with a 2-loop cooling channel and coolant flow 10 l/min.

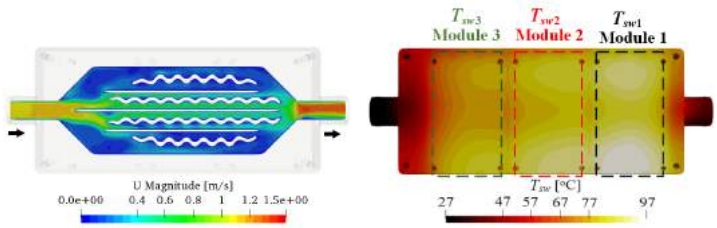
adequately in the first design of Fig. 7.8, since most of the coolant keeps flowing in the middle channel.



(a) (b)

Fig. 7.8: Heatsink design "wave 1", with multiple fins of wavy shape.

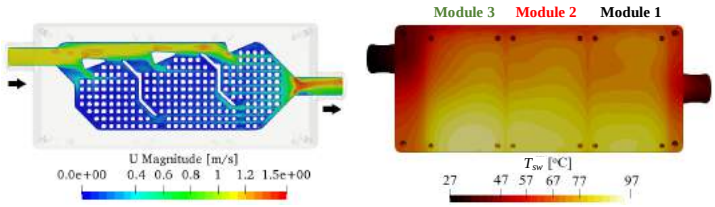
A modified version after some more design iterations is shown in Fig. 7.9, that achieves a more even flow of the coolant through most of the channels. This improvement is also reflected on the sink temperatures T_{sw} shown in Fig. 7.9(b), which are considerably lower compared to the temperatures of Fig. 7.8(b). However, the same temperature gradient with the initial 2-loop design is evident here with the T_{sw1} being the highest among the three.



(a) (b)

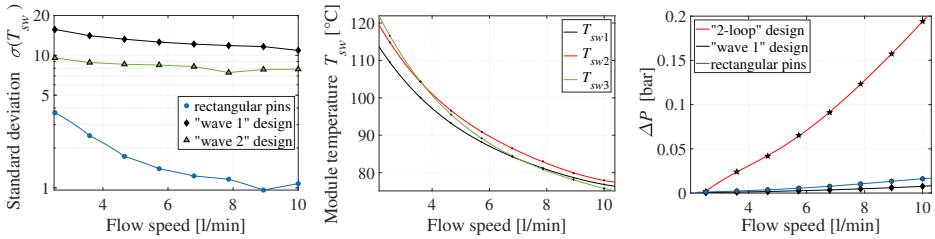
Fig. 7.9: Heatsink design "wave 2", having multiple fins of straight and wavy shape.

Heatsink geometries with pins have also been studied and an example is presented in Fig. 7.10. Rectangular pins are used due to their simpler and cheaper design, since they can be machined [191], and their better thermal performance [208]. The number of pins, their positions and other parameters are optimized through iterative simulations. The presented heatsink design has a more homogenous temperature distribution per MOSFET patch compared to the other candidates, as seen in Fig. 7.11(a), and has quite good thermal performance and pressure drop, as per Figs. 7.11(b)-(c). Therefore, the heatsink with rectangular pins has been selected for further analysis in the next subsection.



(a) (b)

Fig. 7.10: Heatsink designs with multiple rectangular pins and three straight fins dividing the flow into equal sections



(a) (b) for the heatsink with pins (c)

Fig. 7.11: Comparative simulation results of the studied heatsinks: (a) standard deviation in logarithmic-scale showing the discrepancy between the three power module temperatures; (b) average temperature of the power module patches for the heatsink with pins; (c) pressure drop of the coolant (between inlet/outlet)

7.4.3 CHT Computation Process with Transient Heat Dissipation

The results of the final heatsink design with rectangular pins (Fig. 7.10) are shown in this subsection, while the load of the modelled inverter is dynamically changing. The performance of the designed heatsink is evaluated, when typical operating conditions for automotive drives are simulated. Firstly, the acceleration test of a test-case BEV (with parameters displayed in Table 7.2) is performed, when the peak torque of the drive equal to 580 Nm is applied. Then, simulation results of the motor drive with the CLTC_P driving cycle are presented.

The test-case vehicle is simulated first on Matlab/PLECS, where detailed representation of the vehicle dynamics as described by (7.1)-(7.5), the motor and the SiC inverter model are included. As seen in Fig. 7.12, except for the rotor inertia of the PMSM, the inertia due to the mass of the vehicle m is considered, which

converted to the motor side is calculated as

$$J_{car} = \frac{m\, r^2}{gear^2} \tag{7.10}$$

The purpose of the Matlab/PLECS model is the calculation of the inverter losses, which is the heat-load of the studied heatsink. An equivalent thermal network of the inverter is also developed in order to calculate the losses of the power switches at the correct temperature that the inverter experiences. The results from the steady-state CHT computations of the previous subsection can be utilized to build an equivalent thermal model of the inverter's cooling system, which is a combined Cauer and Foster network, cited from [202].

The variable $R_{th\,sa}$ in Fig. 7.12 represents the thermal resistance between the aluminium cooling plate and the coolant fluid. $R_{th\,cs}$ is the thermal resistance between the case and the sink, because of the thermal interface material (TIM). The

Table 7.2: Modelled Passenger Vehicle Parameters

Parameter	Value	Unit
Vehicle mass m	1900	kg
Effective area A [162]	2.2879	m^2
Aerodynamic drag C_d [162]	0.35	-
Rolling resistance C_r [162]	0.012	-
Tire size	245/45R19	
Wheel radius r	0.352	m
Powertrain arrangement	1 motor	
Peak torque $T_{e\,max}$	580	Nm
Gear ratio $gear$	5.7	-
Maximum speed v_{max}	209	km/h
Number of pole pairs p	4	-
Stator resistance R_s	0.026	Ω
Stator inductance L_d	0.90	mH
Stator inductance L_q	2.61	mH
DC-link voltage V_{dc}	800	V
PMSM shaft inertia J	0.018	kg·m^2
Inverter switching freq. f_{sw}	20	kHz
Inverter gate resistance R_G	1	Ω
Case-sink $R_{th\,cs\,sw}$ [209]	0.026	K/W
Heatsink mass m_h	1.36	kg

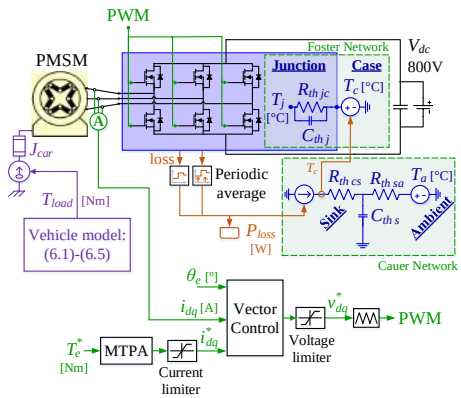


Fig. 7.12: Schematic of the modelled electric drive on Matlab/PLECS

TIM affects the heat spreading in the module and, therefore, $R_{th\,cs}$ is important to be included in the thermal simulation model. $R_{th\,jc}$ is the thermal resistance between the junction of the power switch and the case, because of the different layers of the DBC structure of the module. The $R_{th\,jc}$ has been calculated by a thermal model provided by the switch manufacturer.

$$R_{th\,cs} = \frac{L}{k\,A_{contact}} = \frac{R_{th\,cs\,sw}}{n_{sw}} \overset{[209]}{\underset{n_{sw}=6}{=}} 4.3 \cdot 10^{-3}\ \text{K/W} \tag{7.11}$$

$$R_{th\,sa} = \frac{1}{h_{sa}\,A_c} \tag{7.12}$$

where $A_{contact}$ is the total area of the power modules' baseplate, L the thickness of the TIM. The $R_{th\ cs}$ value is not available for the specific power modules and instead its value is taken from [209] for IGBT power modules of similar dimensions and current rating. $R_{th\,cs\,sw} = 0.026$ K/W is the cited case-sink resistance per individual switch position of the inverter. $A_c = 0.0604$ m^2 is the total surface of the heatsink cooling channel in contact with the coolant and h_{sa} is the heat transfer coefficient of the heatsink with rectangular pins, which is obtained from the CHT results of the previous subsection.

The thermal capacitance of the cooling plate is calculated as

$$C_{th\,s} = c_p\,m_h \overset{c_{p\,\text{Al}}}{\Longrightarrow} C_{th\,s} = 1238\ \text{J/K} \tag{7.13}$$

where $c_{p\,\text{Al}}$ is the specific heat capacity of aluminium equal to 910 J/(K kg).

The conduction losses of the SiC MOSFETs and their body diodes are calculated with the PLECS block periodic average, while periodic impulse average is used for the switching losses. As seen in the schematic of Fig. 7.12, the equivalent thermal model is a closed loop system, due to the feedback of the inverter's temperature in the power loss calculation and, therefore, the losses are accurately estimated at the correct temperature for each simulated operating point.

Acceleration of the BEV with maximum torque:
The acceleration profiles under-test are analysed for inlet coolant temperatures T_{in} equal to 26.85°C (300 K) and 65°C, in order to model driving conditions, when the BEV operates at a cool or a warmer environment, respectively. It has been assumed that the T_{in} remains constant throughout the whole test procedure. Conforming with the usual practice in light duty vehicle cooling systems, 6.8 l/min coolant volume flow is used, similar to [210]. The suitable heat transfer coefficients h_{sa} are obtained from the steady-state CHT results and are equal to $h_{sa\,26.85^o\text{C}} = 2228.41$ W/(m^{2}K) and $h_{sa\,65^o\text{C}} = 2279.21$ W/(m^{2}K).

The motor accelerates at the beginning and constant torque is applied equal to $T_{m\,max} = 580$ Nm. When the current controller reaches its voltage limit and enters the medium- and high-speed operating regions, the applied torque starts to reduce. Then, the motor operates with constant voltage equal to its maximum value, while the current changes. At $t = 5.2$ s the system reaches its maximum power and the inverter experiences also its maximum losses and temperature.

The results from the acceleration test are shown in Fig. 7.13 as obtained from Matlab/PLECS, showing that the modelled BEV can accelerate to 100 km/h in 6 s. The semiconductor losses are shown in Fig. 7.13(c) for both tested coolant temperatures and it can be observed that the increase of the temperature T_{in} leads to higher losses of up to 16.3%.

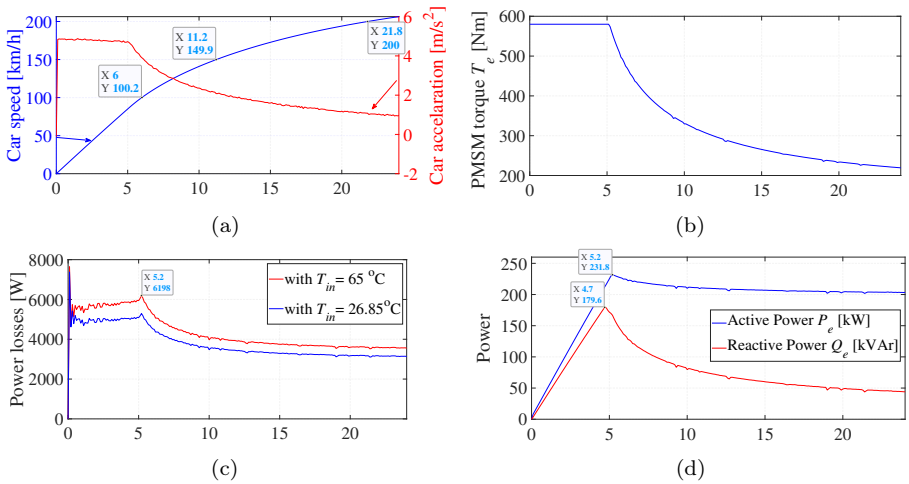


Fig. 7.13: Results of the (a) speed and acceleration of the BEV, (b) applied electromagnetic torque, (c) semiconductor losses of the inverter for different inlet coolant temperatures T_{in} and (d) active / reactive input power of the motor

Then, the inverter is simulated with the 3D CHT model on OpenFOAM and input of the model is the power-loss-curve from Fig 7.13(c). The results from the transient 3D CHT simulations are shown in Fig. 7.14 for the same acceleration profile. The hottest temperature of the heatsink is reached at 10 s. The junction temperatures for each individual power module T'_j are also shown in Fig. 7.14 with dotted curves. The discrepancy between the individual junction temperatures of the three power modules can be observed. For example, as can be seen in Fig. 7.14(a), at 10 s the temperature rise of T'_{j2} (with respect to the T_{in}) is 7.4% and 8.8% higher than the temperature rise of T'_{j1} and T'_{j3}, respectively. In a heatsink

without uniform heat distribution, such as the one in Fig. 7.7, this discrepancy could also be a potential cause of failure for the inverter and faster aging of the hotter semiconductors.

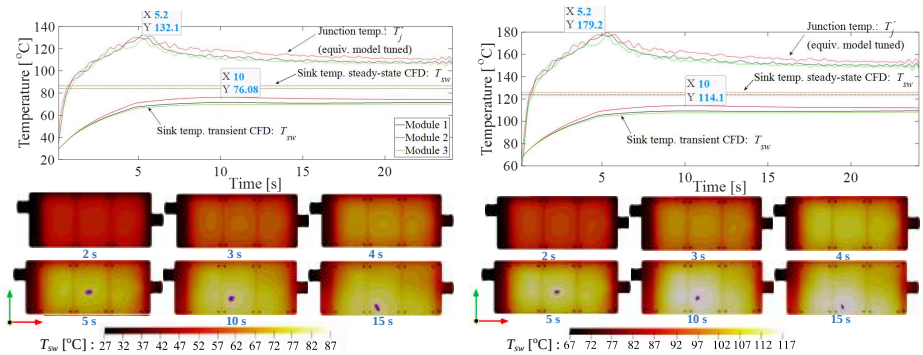


Fig. 7.14: 3D CHT results during acceleration of the BEV with maximum motor torque, when (a) $T_{in} = 26.85$°C and (b) $T_{in} = 65$°C

The heatsink temperatures in Fig. 7.14, which are simulated with the proposed transient method, can be compared with the ones obtained by the steady-state technique (straight dashed-dotted lines), which have been shown previously in Fig. 7.11(b) for 6.8 l/min coolant flow speed. As can be seen, the sink temperature values calculated with the steady-state simulations are higher than the ones obtained with the transient CHT computations, throughout the whole acceleration phase of the vehicle. It should be noted that the steady-state calculations refer to 4 kW semiconductor losses, while the computation results by the proposed transient 3D CHT design technique correspond to dynamic power loss of the SiC inverter up to 6.2 kW [Fig. 7.13(c)]. Designing the heatsink with steady-state CHT simulations to have 6.2 kW of thermal load would lead to an oversized cooling plate, whereas the design with the new transient technique has been accurately tailored to the exact acceleration requirements of the examined electric vehicle. Therefore, it gives the margin for further dynamic overload with additional losses even up to 55%. This means that designing the heatsink with transient CHT simulations allows better exploitation of the inverter at dynamic operation.

Driving Cycle Simulations with Transient CHT:
Simulation results of the tested PMSM drive from the CLTC_P driving cycle are shown in Fig. 7.15. The inlet coolant temperature in both cases is set equal to $T_{in} = 26.85$°C and the coolant volume flow is 6.8 l/min. The semiconductor losses

and temperatures are shown in these figures.

Fig. 7.15(a)-(b) shows the inverter power losses and temperature, when the electric drive is simulated on Matlab/PLECS. Similarly with the acceleration test, these power losses are imported into the 3D CHT model as variable heat-load of the heatsink and the system is simulated again. A closer look of the first 271 s of the CLTC_P cycle is shown in Fig. 7.15(c) showing the average temperature of each power module patch T_{sw} and screenshots of the cooling plate for some characteristic time moments. The junction temperatures T_j' are shown in Fig. 7.15(d).

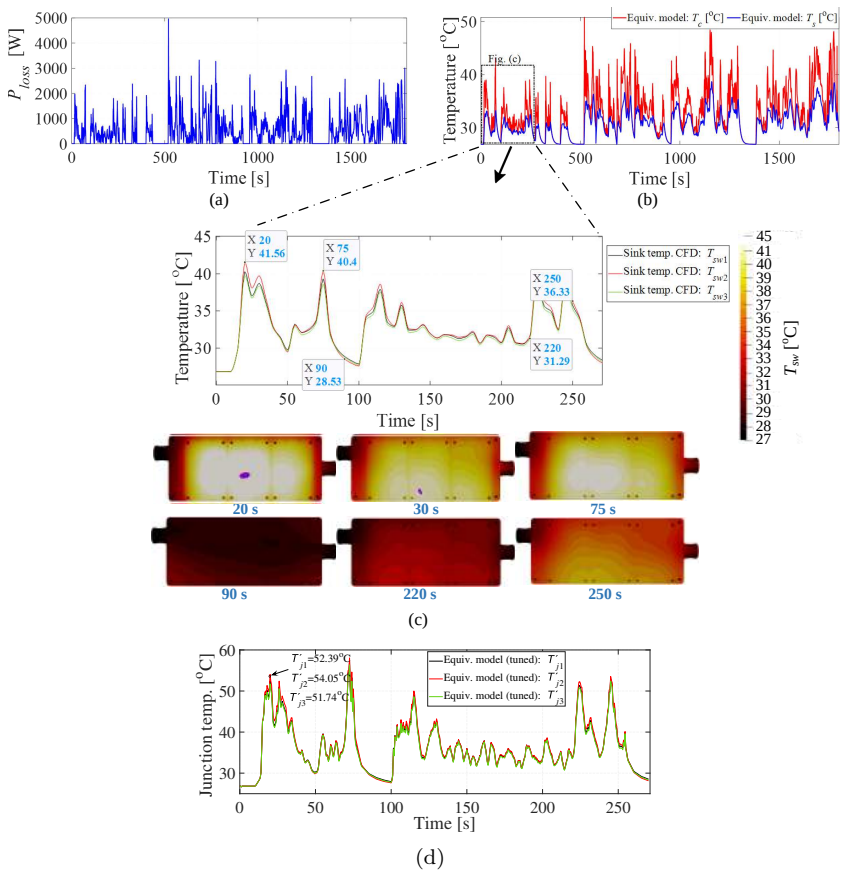


Fig. 7.15: CLTC_P driving cycle: results of the (a) total inverter losses and (b) heatsink temperatures from the thermoelectric system model and (c) individual power module temperatures obtained from the 3D CHT analysis with $T_{in} = 26.85$°C and (d) junction temperatures of the three power modules

The temperature T_{sw2} is the highest most of the time, except for some time instants during the deceleration phase of the cycle such as at 50 s and at 90 s. Then, the T_{sw2} is the lowest temperature among the three. The same results can also be seen for the junction temperatures. The highest temperature discrepancy between the three power modules is seen at 20 s, when the temperature rise of T'_{j2} (with respect to the T_{in}) is 6.5% and 9.3% higher than the temperature rise of T'_{j1} and T'_{j3}, respectively.

Another interesting observation is that the hottest area of the cooling plate (pinpointed with a purple dot) is close to the middle of the device, while the temperature keeps increasing until it reaches its peak value, such as at the time moment 20 s when the hotspot-temperature is 43^oC. Afterwards, when the temperature starts to decrease, the hottest area moves towards the bottom of the plate, such as at 30 s when the purple dot is 20 mm further down. Similar observation can be made for the acceleration speed profile in Fig. 7.14. The consequence of this is that, depending on the operation of the vehicle different areas of the power modules experience the highest temperature affecting also the lifetime of the corresponding semiconductors. Therefore, the transient 3D CHT computations are important in order to study these thermal heterogeneities and to try to tune accordingly the inverter design.

7.4.4 Iterative Cooling Design Process

The following thermal design proceedure for automotive inverters can be formulated as a conclusion from the simulation results of this section. Firstly, the needed thermal dissipation power of the inverter's heatsink is defined with a Matlab/PLECS analysis for constant load of the drive. Drive operation close to its maximum power can serve as a starting point for the iterative design process calculating the losses at the worst-case conditions for the inverter. The initial thermal properties of the cooling plate are decided with a hand-computed Nusselt-number-based approach [211]. The required thermal dissipation power $P_{loss\ init}$ is calculated during this design step, where the first draft of the heatsink design will be based on. The $P_{loss\ init}$ is being updated during later steps of the iterative design process and a more accurate value is later defined, as shown in Fig. 7.16.

Afterwards, a Computer Aided Design (CAD) of the heatsink is prepared for further computations. A full 3D CHT model of the heatsink is then used in the next step using the software OpenFOAM, where the performance of the design is evaluated for various operating conditions of the fluid, such as different flow speeds and cooling media temperatures. In case the designed heatsink fulfills the

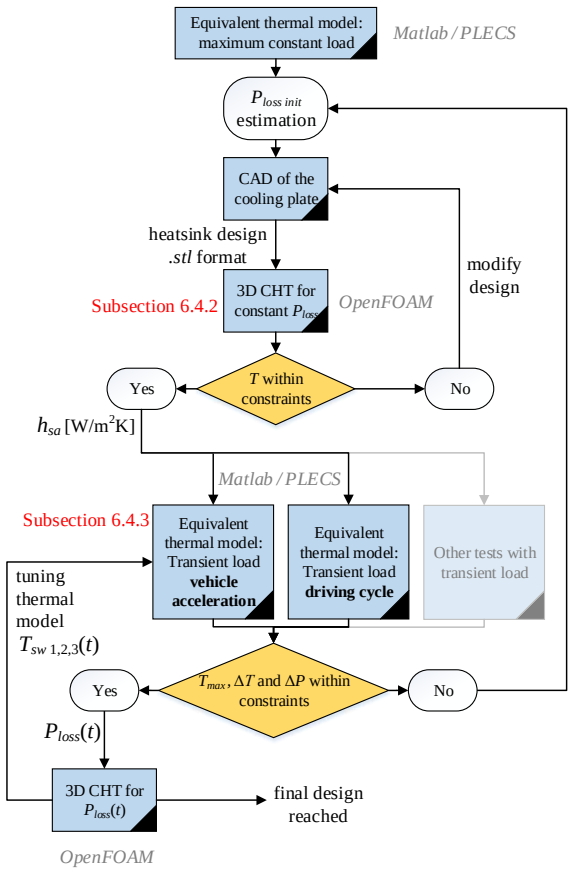


Fig. 7.16: Flowchart of the inverter's heatsink design process adopting an equivalent thermal and electric model and 3D CHT analysis.

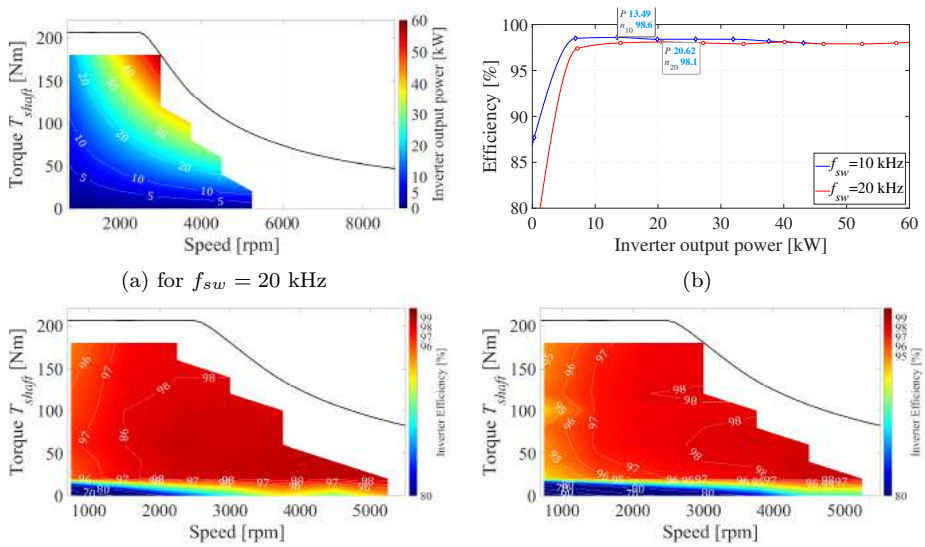
requirements of the specific application (e.g. the temperature of the inverter lays withing the predefined safety limits), the design process moves to the next step which includes testing of the inverter with transient load.

The results of the steady-state 3D analysis are utilized to build a simplified thermal network model of the inverter, where the power losses at various operating points can be calculated. Many driving patterns of the BEV can be tested here with the modelled motor drive, such as an acceleration of the car from standstill up to its maximum speed or legislative driving cycles. If the calculated temperatures of the power modules during these tests lay within the recommended operating conditions defined by the MOSFET manufacturer, the power loss profile is used by the 3D model of the heatsink to run transient CHT computations with the same load

patterns, where the individual temperature of each power module can be obtained. In case the calculated temperatures or the pressure drop of the heatsink's coolant lay outside the design specifications, the design process is repeated, updating accordingly the value of $P_{loss\ init}$ in the first step of the flowchart. The heatsink design is refined by this algorithm with the constant and transient load tests until all the design specifications are fulfilled.

7.5 Inverter Efficiency Measurements

The efficiency of the SiC inverter has been measured experimentally with switching frequency $f_{sw} = 10$ kHz and 20 kHz and the results are shown in this section. The 60 kW PMSM emulator set-up of that has been studied in Chapter 6 is used for the measurements [see the experimental set-up in Fig. 6.8(b)]. The inverter is cooled with cold tap water and an automatized process is used for measuring the voltages and currents of the system at each operating point, so that the inverter is loaded for a short time and and constant temperature can be kept throughout the whole experiment. A dead-time equal to 1 μs has been used between the top and bottom switch of each phase leg of the inverter.



(a) for $f_{sw} = 20$ kHz (b)

(c) for $f_{sw} = 10$ kHz (d) for $f_{sw} = 20$ kHz

Fig. 7.17: Experimental measurements of the inverter (a) output power, (b) efficiency at 3000 rpm, efficiency map (c) for 10 kHz and (d) 20 kHz switching frequency with dc-link voltage 360 V

The operating points on the torque-speed map shown previously in Fig. 6.10 are tested with the PMSM emulator. However, due to the voltage drop across the ac inductors of the topology, the points where the machine operates with maximum stator voltage at the high-speed region cannot be emulated. Also, a slightly larger dc voltage than the one examined in Chapter 6 has been used here, namely 360 V instead of 300 V.

The active power at the ac side of the inverter, which has been tested here, is shown in Fig. 7.17(a). The envelope of the torque-speed map is also shown with black line in the same figure. The inverter efficiency in Figs. 7.17(b)-(d) is calculated as follows

$$\text{Efficiency}\% = 100\ \frac{P_{ac}}{P_{ac} + P_{inv\ loss}} \tag{7.14}$$

where P_{ac} is the inverter active power at its ac side and $P_{inv\ loss}$ is the power loss of the inverter as measured with the oscilloscope.

The inverter efficiency has a peak value of 98.6% for switching frequency 10 kHz and 98.1% for switching frequency 20 kHz, as seen in Fig. 7.17(b). The largest difference between these two graphs can be observed when low power is tested, while similar inverter efficiency for both cases can be observed when the power increases. The measured efficiency complies with previously reported results in the literature for SiC three-phase inverters [212, 213].

7.6 Summary

The design process of an automotive inverter has been presented in this chapter. SiC power switches were used in the inverter in order to reduce its losses and increase its power density. Prototypes of two inverters were manufactured that were used in the PMSM drive which has been tested experimentally in Chapter 6.

The first step involves the formulation of the design requirements for the inverter, as imposed by the expected capabilities of the vehicle where the inverter is intended to be used. The modelling process of the vehicle dynamics is described, which determines the required power of the motor drive.

The next step is the dimensioning of the inverter and the selection of its components, based on the design specifications. The power switches and the dc-link capacitors are the basic components that should be selected.

The last step is the design of the cooling system of the inverter and, specifically, its heatsink. A multidisciplinary design process of the heatsink is proposed here which

consists of multiple simulation stages. The inverter losses are modelled through circuit simulation tools, such as the PLECS toolbox on Matlab. Then, the heatsink is designed through CAD and simulated through CHT computations, firstly with steady-state heat-load and later with transient load considering realistic operating profiles of the vehicle. The main advantages of the transient CHT modelling approach can be summarized as follows:

1. Firstly, the overload capacity of the inverter can be more easily evaluated with the proposed design method, when the maximum acceleration of the investigated vehicle is applied. The results of the simulated test-case system have shown that short-time overloading with an increase of the thermal heat up to 55% still keeps the inverter heatsink temperature beneath the safety limits.
2. The transient CHT model can reveal more accurately the temperature discrepancies among the three SiC power modules during realistic operating conditions, which can reach up to 9.3% for the tested automotive inverter.
3. The location of the hotspots at the surface of the sink can be more accurately calculated with the transient 3D design method. This can allow more fine-tuned design of the heatsink in order to reduce large temperature differences at the surface of the sink.

This procedure has as a result a fine-tuned heatsink design that fulfills at the same time the design specifications of the specific vehicle with the smallest possible component size.

Lastly, experimental measurements of the prototype inverter efficiency are presented for different power and frequency operating points. When the inverter operates with switching frequency 20 kHz and 360 V dc-link voltage, the maximum efficiency is 98.1%.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The design and control of SiC three-phase inverters for machine drives have been investigated in this thesis. Two background applications have been studied, kite-based tidal power generation and battery electric vehicles. Although these applications are very different from each other, they share similar goals and challenges for the design of the power conversion system, namely high power density and efficiency.

Two different approaches have been investigated in order to achieve high power density of the power conversion system. Firstly, the increase of the operating voltage of the machine drive, which is used in offshore tidal power systems, has been motivated by the resultant decrease of the ac current flowing through the undersea cables that connect the kite to the on-shore grid. Since the use of medium voltage drives with 5-level converters can increase the operating voltage of the system more than four times compared to standard low-voltage 2LCs, undersea cables with smaller diameter can be used, reducing in this way the total weight and drag of the kite system. Therefore, a medium voltage multilevel generator drive has been proposed in Chapter 4, which consists of two B2B-connected 5-level NPC converters and a medium voltage PMSG. The 5-level NPC converter has been proven to be a suitable topology for medium voltage grid-connected machine drives, because its main advantages compared to other multilevel topologies are the common dc bus, which is convenient for B2B configurations, and the reduced number of passive components. Conventional vector control can also be used to

control both the machine inverter and the grid inverter.

The harmonics of the ac current and voltage are also highly improved when using drives with 5-level converters instead of 2LCs. This constitutes an additional motivation towards the use of multilevel converters in offshore power plants, since the size of the ac passive filters can be drastically reduced and higher power density of the drive can be attained. Specifically, FFT analysis of the current and voltage has shown that the THD of the generator current is reduced by 66% and the generator phase voltage by 58%, when 5-level instead of 3-level converters are used. Experimental results in Chapter 5 have shown similar results. Similar improvement is observed also on the grid-side voltage and current harmonics.

The main drawback of this converter topology is the balancing of the dc-link capacitor voltages. This problem has been solved in the thesis by proposing four alternative ways of balancing the dc-link voltages, which utilize a modified version of the SVM or dc/dc converters connected in parallel to the dc-link. The advantages and disadvantages of each proposed balancing method have been summarized in Table 4.8 and the conclusions mentioned there are based on simulation results implemented in Matlab/Simulink and PLECS.

The second approach towards high power density involves the use of SiC power switches in the converters. SiC switches have lower losses compared to standard Si IGBTs, which allows to build more compact inverters and to use higher switching frequencies.

The mechanical design of the SiC inverter is an important step of the whole manufacturing process. An optimization procedure of the cooling components using transient CFD computations and the correct sizing of the dc-link capacitor bank have been introduced and applied on a test-case 450 A, 800 V (dc) SiC inverter. The proposed cooling design approach allows an evaluation of the overload capability of the inverter, which can reach up to 55% for the test-case inverter, and a more accurate estimation of the temperature distribution on the inverter heatsink.

A prototype 450 A SiC 2-level inverter has been manufactured and tested experimentally on a 60 kW PMSM test-bench. Afterwards, a P-HIL set-up has been studied, where the 60 kW PMSM has been emulated using an additional converter. P-HIL testing for machine drives is shown to be a useful experimental verification method for inverter design projects, in case multiple machine types need to be evaluated with the same inverter and the machines are not available yet.

However, circulating zero-sequence current is a typical issue of the examined

machine emulator topology, which is usually solved by installing hardware common mode filters. A novel current control scheme has been proposed that can limit the circulating current that flows in the system by controlling the duty cycle distribution among the zero states on the SVM. The effectiveness of the control has been verified experimentally, since the remaining zero-sequence current amplitude has been successfully limited to 3.3% of the ac current amplitude, when the system operates with 42 kW active power at the base speed of the modelled PMSM.

8.2 Future Work

The following research points can be further investigated in future projects in order to extend and further utilize the outcomes of this PhD thesis:

- The use of multilevel-based drives has been investigated only for offshore renewable power generation in this thesis. It would be interesting to investigate the possible advantages of using 3- or even 5-level inverters in automotive drives. Especially, future electrification of heavy-duty or construction vehicles with large power demands would be benefited by an increase of the powertrain voltage and multilevel inverters would be a viable solution to realise these systems.
- The proposed zero-sequence current control for P-HIL systems has been applied only on 2LCs, where two redundant zero states exist. However, it is possible to extend the validity of this control to the multilevel space vector plane, where more zero-state combinations exist. This would be necessary in case multilevel inverters are tested in P-HIL systems.
- Integrated machine-inverter systems, where the power switches of the inverter are mounted directly on the housing of the machine, are considered as a promising solution for future extremely high-power-dense drives. The inverter design approach proposed in this thesis, which uses transient CFD computations to model the cooling system, could be applied in such a project improving the thermal properties of the resultant drive.

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Appendix A

The following C-code is used for generating the matrices of the SVM algorithm in (4.25) and (4.26). Equal distribution of the duty cycles for the redundant states $d_1 = d_2$ (here: duty[0] and duty[3]) is shown in this example, based on 4.24.

The variables from the following C-code are defined as $N\_layer = N - 1$ and the vectors V_D_abc, V_E_abc, V_F_abc and V_G_abc are calculated from (4.13):

```
if ((u_ref_a_SVPWM + u_ref_b_SVPWM) >
            (floor(u_ref_a_SVPWM) + floor(u_ref_b_SVPWM) + 1))
{
    // upper triangle sequence: | E F G E | E G F E |
    duty_E = V_G_ab[1] - u_ref_b_SVPWM;
    duty_F = V_G_ab[0] - u_ref_a_SVPWM;
    duty_G = 1 - duty_E - duty_F;
    duty[0]   = duty_E/2;
    duty[1]   = duty_F;
    duty[2]   = duty_G;
    duty[3]   = duty_E/2;

    //[V_E_abc;V_F_abc;V_G_abc;V_E_abc+[1 1 1]];
    vector[0][0] = V_E_abc[0];
    vector[0][1] = V_E_abc[1];
    vector[0][2] = V_E_abc[2];

    vector[1][0] = V_F_abc[0];
    vector[1][1] = V_F_abc[1];
    vector[1][2] = V_F_abc[2];

    vector[2][0] = V_G_abc[0];
    vector[2][1] = V_G_abc[1];
    vector[2][2] = V_G_abc[2];

    vector[3][0] = V_E_abc[0]+1;
```

```
      vector[3][1] = V_E_abc[1]+1;
      vector[3][2] = V_E_abc[2]+1;

  }
  else
  {
      // lower triangle sequence: | D E F D | D F E D |
      duty_E = u_ref_a_SVPWM - V_D_ab[0];
      duty_F = u_ref_b_SVPWM - V_D_ab[1];
      duty_D = 1 - duty_E - duty_F;
      duty[0]   = duty_D/2;
      duty[1]   = duty_E;
      duty[2]   = duty_F;
      duty[3]   = duty_D/2;

      //[V_D_abc;V_E_abc;V_F_abc;V_D_abc+[1 1 1]];
      vector[0][0] = V_D_abc[0];
      vector[0][1] = V_D_abc[1];
      vector[0][2] = V_D_abc[2];

      vector[1][0] = V_E_abc[0];
      vector[1][1] = V_E_abc[1];
      vector[1][2] = V_E_abc[2];

      vector[2][0] = V_F_abc[0];
      vector[2][1] = V_F_abc[1];
      vector[2][2] = V_F_abc[2];

      vector[3][0] = V_D_abc[0]+1;
      vector[3][1] = V_D_abc[1]+1;
      vector[3][2] = V_D_abc[2]+1;
  }

  // duty cycle of each phase and each state
  //              A                 B                 C
  //      1   duty_phA_state1   duty_phB_state1  duty_phC_state1
  //      2   duty_phA_state2   duty_phB_state2  duty_phC_state2
  //      3   duty_phA_state3   duty_phB_state3  duty_phC_state3
  //     ...
  //N_layer  duty_phA_stateN   duty_phB_stateN  duty_phC_stateN

  for (i = 0; i<=2; i++)            // 3 phases
    {
        for (j = 0; j<=3; j++)      // 4 time intervals
        {
           duty_state[j][i] = 0;
        }
    }
```

```
75
76  for (i = 0; i<=2; i++)          // 3 phases
77  {
78      for (j = 0; j<=3; j++)      // 4 time intervals
79      {
80          for (k = 0; k<N_layer; k++)   // check the state
81          {
82              if (vector[j][i] == k+1)
83              {
84                  duty_state[k][i] = duty_state[k][i] + duty[j];
85                  break;
86            }
87          }
88      }
89  }
90
91  // duty cycle of each switch
92  // sw1 is the top switch of the upper-leg ... sw_N is the bottom
      switch of the upper-leg
93  //              A               B               C
94  // sw1  duty_phA_sw1  duty_phB_sw1  duty_phC_sw1
95  // sw2  duty_phA_sw2  duty_phB_sw2    duty_phC_sw2
96  // sw3  duty_phA_sw3  duty_phB_sw3    duty_phC_sw3
97  // ...
98  // swN  duty_phA_swN  duty_phB_swN    duty_phC_swN
99
100 // sum up the duty cycles for each switch
101
102 for (i=0; i<3; i++)             // 3 phase
103 {
104     for (j=0; j<N_layer; j++)
105     // switch index. "j = 0" corresponds to top switch.
106     {
107       duty_sw[j][i] = 0;
108       for(k=0; k<=j; k++)
109       // sum up the duty cycle from state N_layer until state 1
110       {
111         duty_sw[j][i] += duty_state[N_layer-1-k][i];
112       }
113     }
114 }
```

The matrix *duty_sw* is the final output of the modulator and contains the duty cycle of each switch of the 3-phase 5-level NPC converter.

Appendix B

PCBs of Medium Voltage Drive System with NPC Converters

The PCB layout of the basic boards of the medium voltage generator drive described in Chapter 5 are attached here.

- In Fig. 1 the PCB that receives the current, voltage and encoder measurement signals from the measurement devices of the drive is shown. This PCB has got four copper layers, with the top and bottom layers being available for connecting the components on the board and the middle two layers being occupied with the $V_{CC} = 3$V and the ground potential, respectively. A picture of this board is shown in Fig. 5.12.
- The PCB in Fig. 2 converts the electrical PWM signal from the microcontroller into optical signal through fiber optic transmitters. It is also made of four copper layers and its schematic has been shown in Fig. 5.13.
- The PCB layout of the gate driver described in Subsection 5.2.1 is shown in Fig. 3. This board, like all the power PCBs of the system, is made of two copper layers.

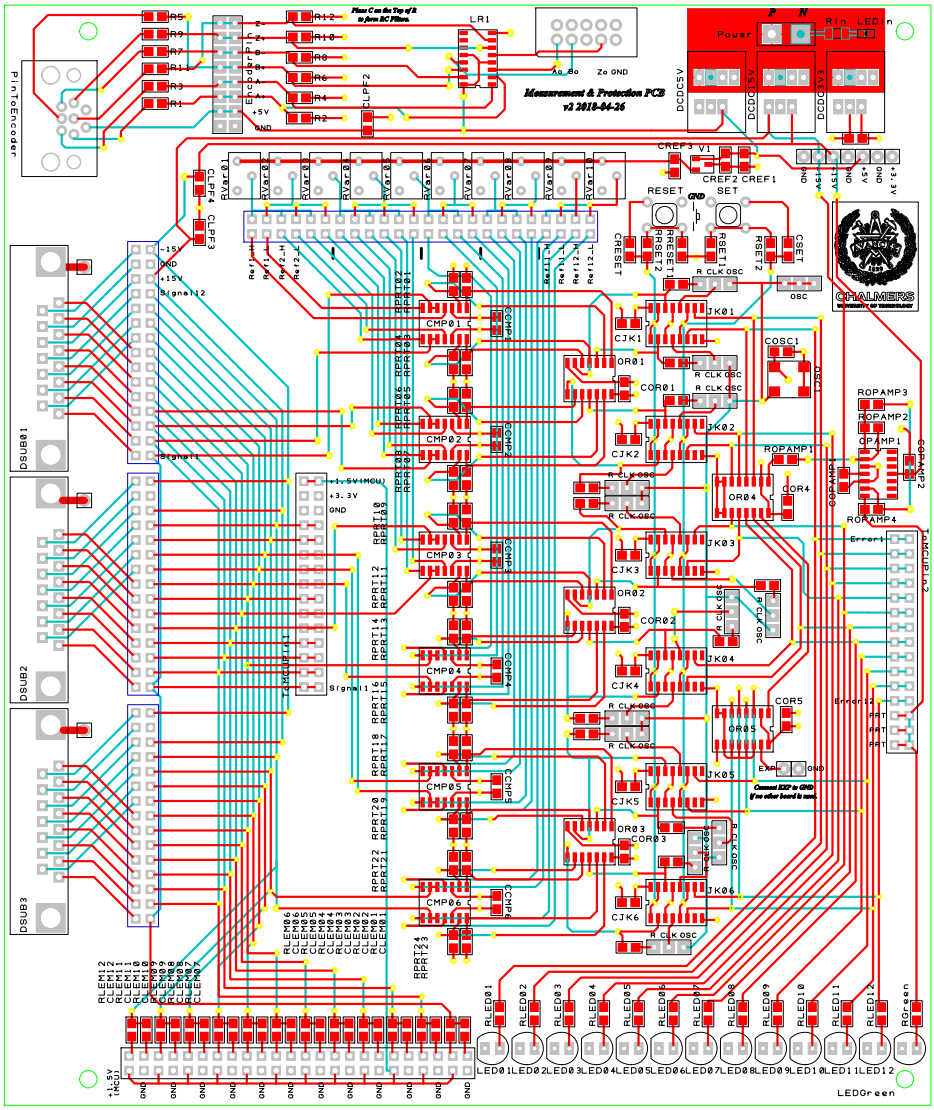


Fig. 1: PCB layout of the measurements and hardware protection board: red and blue lines show the traces of the top and bottom copper layers, respectively

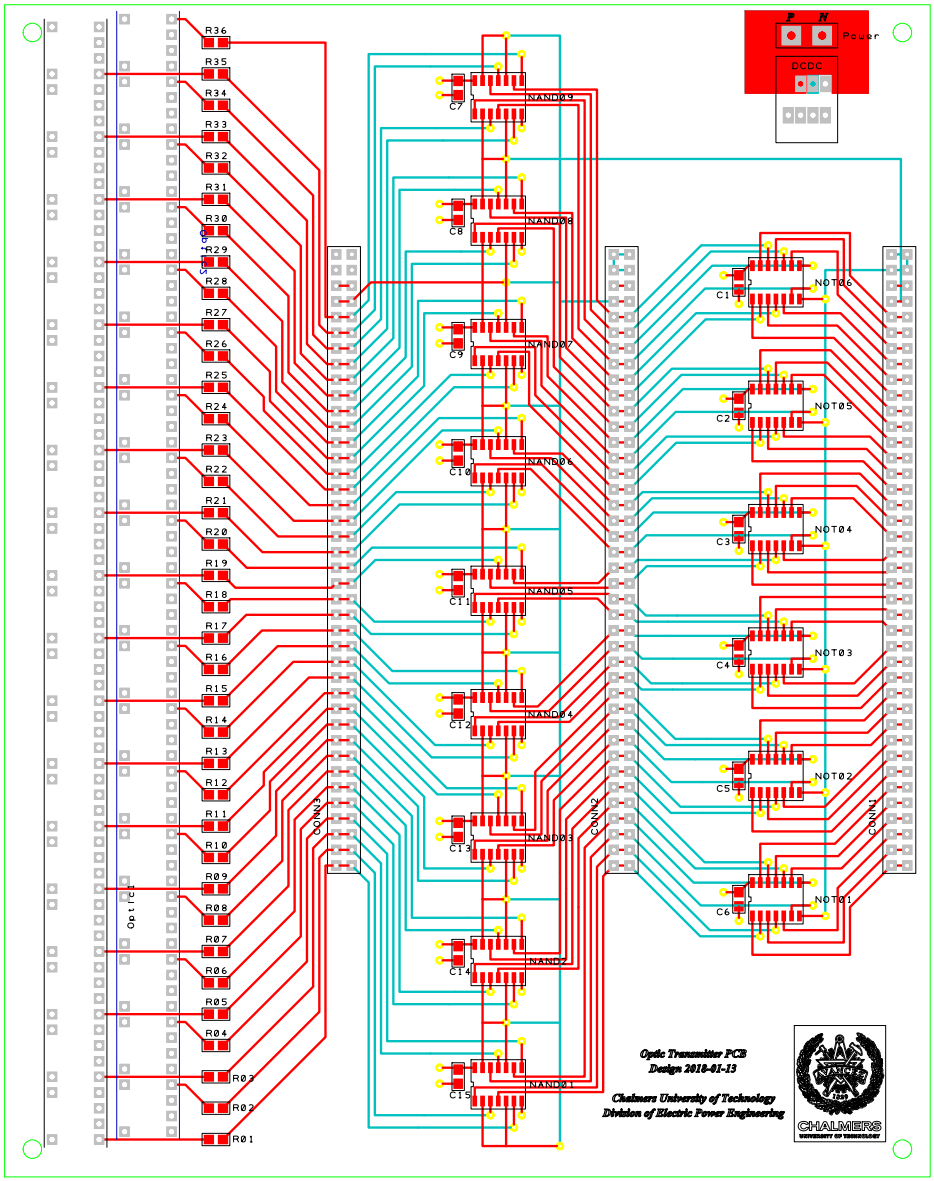
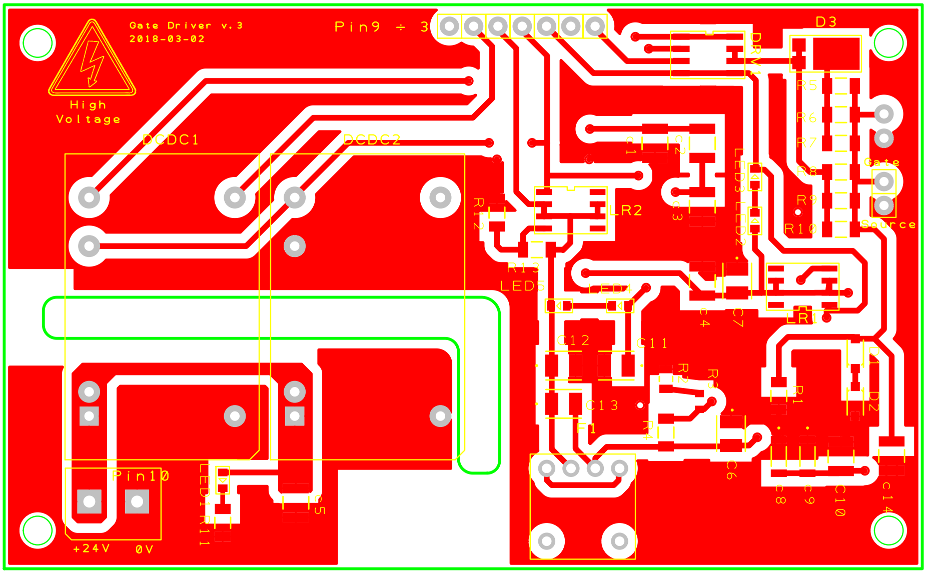
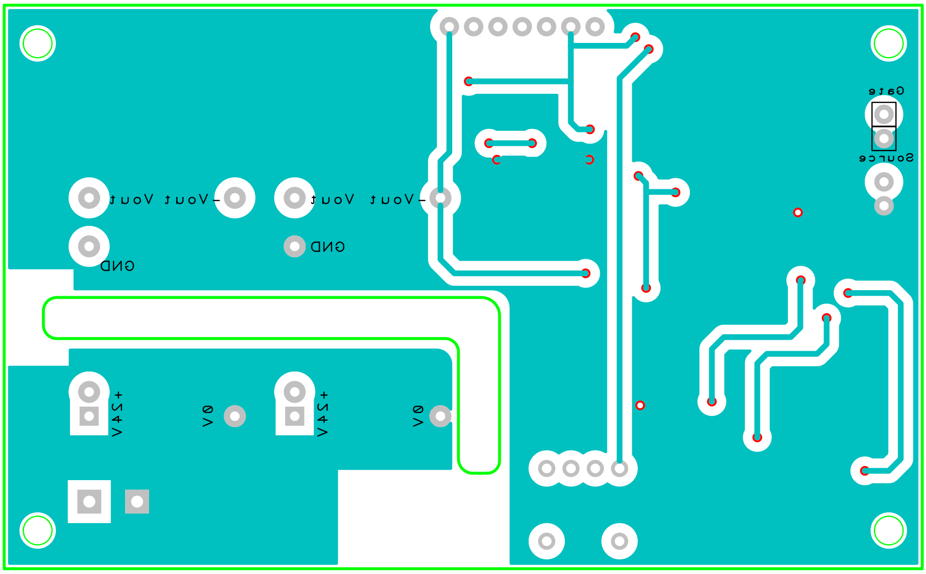


Fig. 2: PCB layout of the PWM board: red and blue lines show the traces of the top and bottom copper layers, respectively



(a)



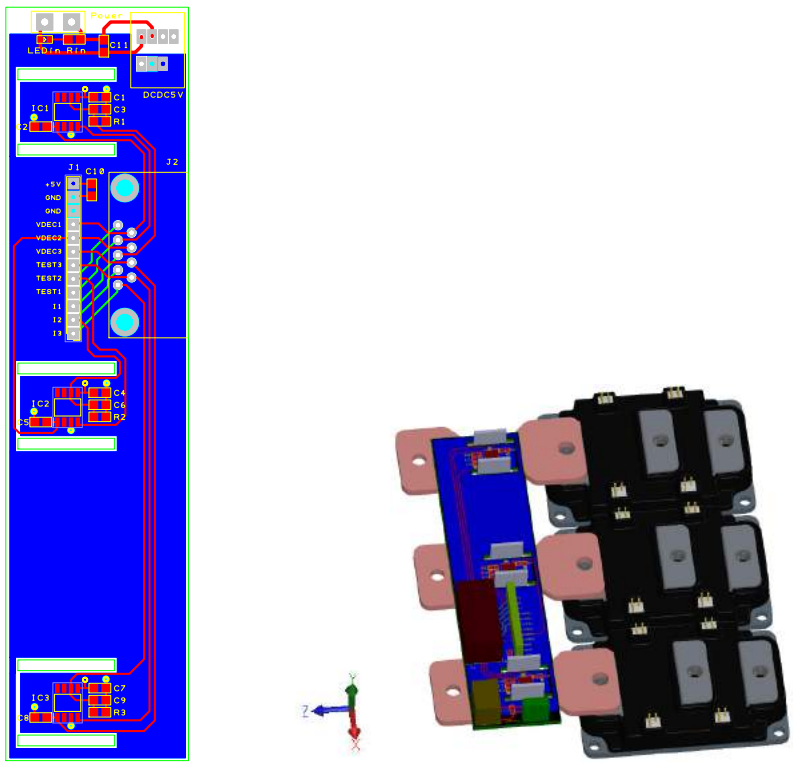
(b)

Fig. 3: PCB layout of the Gate driver for the SCH2080KE SiC MOSFET: (a) top and (b) bottom copper layer

Current Sensor for SiC High-Current Inverter

The IMC-Hall sensors from Melexis have been used for current measurement of the SiC inverter presented in Chapters 6-7. This type of sensors provides a low cost and compact solution for current sensing in power converters. The variant with product code MLX91208-CAV has a large enough measuring range up to 700 A (peak), which is suitable for the specific prototype inverter.

A current measurement PCB has been designed, as seen in Fig. 4(a). The PCB consists of four layers, with the two top layers (red and green) being used for routing the signal traces and the third (dark blue) and fourth (light blue) being reserved for the $V_{CC} = 5$ V and ground potentials, respectively. The CAD drawing of the current measurement PCB is shown in Fig. 4(b), while the final assembled sensor board can be seen on the left side of Fig. 7.4(b).



(a) (b)

Fig. 4: (a) Layout of the current measurement PCB having the MLX91208-CAV sensors and (b) 3-D CAD drawing of the sensor board mounted on the inverter ac terminals