FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Analog Block Evaluation with BIST Instruments

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Resumo

As exigências de qualidade e de capacidade de competição no mercado tornam necessário não só facilitar os testes de circuitos analógicos, mas também de os tornar mais eficientes. Com o aumento da complexidade e nível de integração dos sistemas, o processo de testar circuitos analógicos tornou-se difícil e dispendioso. Esta dissertação foi proposta pela Synopsys Portugal com os seguintes objetivos: realizar um estudo sobre Built-In Self-Test (BIST) analógico e implementar um conjunto de blocos de intrumentos que suportam a implementação de um sistema analógico BIST. Os instrumentos têm de ser capazes de testar parâmetros específicos de um regulador de tensão e de um oscilador. No regulador, os parâmetros para testar são: sobre- e sub- tensão, tempo de estabelecimento, e ondulação de tensão. No oscilador, os parâmetros a medir são: deriva de frequência, tempo de estabelecimento, e distorção de período efetivo.

A disponibilidade destes instrumentos permite realizar operações de autoteste e, assim, reduzir a complexidade e o custo associados à realização do teste em-circuito destes blocos analógicos analógicos. Permite também testar os circuitos periodicamente ao longo da sua vida e, ainda, monitorizar em tempo real alguns parâmetros analógicos.

Um estudo sobre os aspectos fundamentais da arquitectura de um sistema BIST para circuitos analógicos é realizado. Métodos atuais de gerar em chip estímulos de teste e analisar as respostas do circuito, assim como exemplos de métodos de acesso a nós internos de teste são apresentados. Ademais, noções sobre os circuitos a testar e os parâmetros são expostos, juntamente com exemplos encontrados na literatura para testar estes circuitos.

Os instrumentos do sistema BIST proposto são apresentados juntamente com os parâmetros dos blocos em teste. Em seguida, aspetos específicos da funcionalidade e do projeto (numa tecnologia CMOS de 28 nm) de cada instrumento são detalhados e os resultados de simulação, incluíndo verificação Monte Carlo e *corners* dos circuitos são apresentados.

Abstract

The demands for quality and the ability to compete in the market make it necessary not only to facilitate the testing of analog circuits but also to make them more efficient. With the increase of systems complexity and level of integration, the process of testing analog circuits has become difficult and expensive. This dissertation was proposed by Synopsys Portugal with the following objectives: perform a study on analog BIST and implement a set of simple instruments that support the implementation of an analog BIST system. The instruments should be able to test specific parameters of a regulator and an oscillator. As for the regulator, the parameters to be measured are: over- and under- voltage, settling time, and voltage ripple. Concerning the oscillator, the parameters to be measured are: frequency drift, settling time, and duty-cycle distortion.

The availability of these instruments allows for implementing self-test operations and, thus, to reduce the complexity and cost associated with performing analog tests. Additionally, it makes it possible to test the circuits periodically throughout its lifetime and also to monitor some analog parameters in real-time.

A study on the fundamental aspects of the architecture of an analog BIST system is provided. Different methods to generate test stimuli on-chip and analyze the circuit responses are presented. Examples of techniques to access the internal test nodes of the circuits under test are also given. Functional and performance details about the circuits to be tested and the parameters to be measured are provided, along with examples found in the literature on approaches to test them.

The instruments of the proposed BIST system are presented alongside the parameters of the blocks under test. Then, the functionality and design (in a CMOS 28 nm technology) of each instrument are detailed and simulation results carried out to verify their performance are presented.

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"The only true wisdom is in knowing you know nothing."

Socrates

Contents

1 Introduction **1**
- 1.1 Context and Motivation . . . 1
- 1.2 Objectives . . . 3
- 1.3 Structure . . . 3

2 Design for Testability and Built-In Self-Test Concepts **5**
- 2.1 Built-in Self-Test . . . 5
  - 2.1.1 BIST Architecture . . . 6
  - 2.1.2 Test Generation . . . 6
  - 2.1.3 Response Analyser . . . 8
  - 2.1.4 Access to Test Nodes . . . 9
- 2.2 Conclusion . . . 11

3 Review of Literature on Specific Test Approaches **13**
- 3.1 Voltage Regulators . . . 13
  - 3.1.1 Performance Characterization Parameters . . . 15
  - 3.1.2 Testing methods . . . 16
- 3.2 Oscillators . . . 18
  - 3.2.1 Parameters . . . 18
  - 3.2.2 Testing methods . . . 20

4 BIST Instruments **25**
- 4.1 BIST Scheme . . . 25
  - 4.1.1 Specifications . . . 26
- 4.2 Bandgap Voltage Reference . . . 29
  - 4.2.1 Design of the Bandgap Voltage Reference . . . 30
  - 4.2.2 Results . . . 33
- 4.3 Over and Under Voltage Comparators . . . 39
  - 4.3.1 Operational Amplifier . . . 39
  - 4.3.2 Results . . . 42
- 4.4 Peak Detectors . . . 52
  - 4.4.1 Results . . . 53
- 4.5 Voltage Regulator Settling Time Measurement . . . 58
  - 4.5.1 Results . . . 59

5 BIST Blocks - Oscillator **63**
- 5.1 Frequency to Voltage Converter . . . 63
  - 5.1.1 Design of the Frequency to Voltage Converter . . . 65

5.1.2 Frequency Divider 66
5.1.3 Voltage to Current Converter 67
5.1.4 The Switches 69
5.1.5 Results 70
5.2 RC Filter 81
5.2.1 Results 82
5.3 Oscillator Settling Time Measurement 83
5.3.1 Results 84

6 Conclusion and Future Work **87**
6.1 Conclusions and Future Work 87

A Verilog-A Code **89**
A.1 Voltage Regulator Settling Time code 89
A.2 Oscillator Settling Time code 90
A.3 Oscillator Code 92
A.4 Positive Peak Detector Reset Code 93
A.5 Negative Peak Detector Reset Code 95

B Simulations **97**
B.0.1 Simulations Results for the Propagation Delay in PVT 97
B.0.2 Simulations Results for the Propagation Delay in Monte Carlo 99
B.0.3 Simulations Results for the Ranges of Frequencies in PVT 101

C Circuits Netlist **107**
C.1 Bandgap Voltage Reference Netlist 107
C.2 UOV Detection Circuit Netlist 112
C.3 Peak Detectors 117
C.4 FVC Netlist 120
C.5 RC Filter Netlist 125

References **127**

List of Figures

2.1 BIST architecture. . . . 6
2.2 Analog test wrapper . . . 10

3.1 Overvoltage and undervoltage detection circuit. . . . 16
3.2 Block diagram of the ripple detector. . . . 17
3.3 duty-cycle distortion. . . . 19
3.4 Dual mixer time difference method. . . . 20
3.5 BIST structure. . . . 22
3.6 duty-cycle detector. . . . 23

4.1 Block diagram of the BIST instruments. . . . 27
4.2 Bandgap voltage reference. . . . 29
4.3 Bandgap voltage reference output with temperature variation. . . . 32
4.4 Bandgap voltage reference output in PVT. . . . 34
4.5 Bandgap loop gain frequency response for stability analysis. . . . 35
4.6 Bandgap stability analyze in PVT. . . . 35
4.7 Bandgap power supply rejection ratio. . . . 36
4.8 Bandgap power supply rejection ratio in PVT. . . . 37
4.9 Bandgap output in Monte Carlo. . . . 38
4.10 Two-stage operational amplifier. . . . 39
4.11 Bias circuit. . . . 41
4.12 Startup circuit. . . . 41
4.13 Gain and phase of the operational amplifier - 0,65V. . . . 43
4.14 Gain and phase of the operational amplifier - 0,35V. . . . 43
4.15 Gain and phase of the operational amplifier in PVT - 0,65 V. . . . 44
4.16 Gain and phase of the operational amplifier in PVT - 0,35 V. . . . 45
4.17 PSRR of the operational amplifier - 0,65 V. . . . 46
4.18 PSRR of the operational amplifier - 0,35 V. . . . 47
4.19 PSRR of the operational amplifier in PVT. . . . 48
4.20 Operational amplifier offset. . . . 49
4.21 Propagation delay for over-voltage detection. . . . 50
4.22 Propagation delay for under-voltage detection. . . . 50
4.23 Propagation delay for over voltage detection in PVT. . . . 51
4.24 Propagation delay for under voltage detection in PVT. . . . 51
4.25 Positive peak detector. . . . 53
4.26 Negative peak detector. . . . 54
4.27 Peak detector bias circuit. . . . 54
4.28 Propagation delay of the positive peak circuit for a 50 ns peak. . . . 55

4.29 Propagation Delay of the positive peak circuit for a 100 ns peak. 56
4.30 Propagation delay of the negative peak circuit for a 50 ns peak. 57
4.31 Propagation delay of the negative peak circuit for a 100 ns peak. 58
4.32 Voltage regulator passing settling time test. 59
4.33 Voltage Regulator failing settling time test. 60
4.34 Settling time of the voltage regulator code. 61

5.1 Frequency to Voltage Converter. 63
5.2 Circuit that generates the s1 and s2 control signals. 64
5.3 Frequency divider. 67
5.4 Voltage to current converter. 68
5.5 FVC waveforms for a 1 GHz signal. 71
5.6 Input signal directly in the FVC. 71
5.7 FVC waveforms for a 1,2 GHz input signal. 72
5.8 FVC waveforms for a 800 MHz input signal. 72
5.9 FVC output in PVT for 1 GHz input signal. 73
5.10 FVC output in PVT for 1 GHz signal without capacitor variation. 73
5.11 FVC output for a 1 GHz signal in 740 Monte Carlo simulations. 74
5.12 Stability analyze voltage to current converter. 75
5.13 Stability analyze voltage to current converter in PVT. 76
5.14 Voltage to current converter currents in PVT. 76
5.15 Voltage to current converter currents in 740 Monte Carlo simulations. 77
5.16 Output of the FVC with 300 MHz input wave. 78
5.17 Output of the FVC with 600 MHz input wave in the first range. 78
5.18 Output of the FVC with 600 MHz input wave in the second range. 79
5.19 Output of the FVC with 1,2 GHz input wave in the third range. 79
5.20 Output of the FVC with 2,4 GHz input wave in the third range. 80
5.21 Output of the FVC with 2,4 GHz input wave in the fourth range. 80
5.22 Output of the FVC with 4 GHz input wave. 81
5.23 Frequency response of the RC filter. 82
5.24 Transient response of the RC filter 83
5.25 Oscillator passing the settling time test. 84
5.26 Oscillator failing the settling time test. 85
5.27 Settling time of the oscillator code. 86

B.1 Propagation delay for the positive peak detector with 50 ns in PVT. 97
B.2 Propagation delay for the positive Peak detector with 100 ns in PVT. 98
B.3 Propagation delay for the negative peak detector with 50 ns in PVT. 98
B.4 propagation delay for the negative peak detector with 100 ns in PVT. 99
B.5 Propagation delay for the positive peak detector with 50 ns in Monte Carlo. . . . 99
B.6 Propagation delay for the positive peak detector with 100 ns in Monte Carlo. . . 100
B.7 Propagation delay for the negative peak detector with 50 ns in Monte Carlo. . . . 100
B.8 Propagation delay for the negative peak detector with 100 ns in Monte Carlo. . . 100
B.9 Output of the FVC with 300 MHz input wave in PVT. 101
B.10 Output of the FVC with 600 MHz input wave in PVT. 101
B.11 Output of the FVC with 600 MHz input wave in the second range in PVT. 102
B.12 Output of the FVC with 800M MHz input wave in the second range in PVT. . . . 102
B.13 Output of the FVC with 1.2 GHz input wave in the second range in PVT. 103
B.14 Output of the FVC with 1.2 GHz input wave in the third range in PVT. 103

B.15 Output of the FVC with 2.4 GHz input wave in the third range in PVT. 104
B.16 Output of the FVC with 2.4 GHz input wave in the fourth range in PVT. 104
B.17 Output of the FVC with 4 GHz input wave in PVT. 105

List of Tables

2.1 Relationship between type of measurement and test input. 7

3.1 Advantages and disadvantages of the frequency drift measurements methods. . . 21

4.1 Voltage regulator specifications. 26
4.2 Oscillators specifications. 28
4.3 Bandgap voltage reference specifications. 28
4.4 Other specifications. 28
4.5 PVT Specifications of the BIST System. 28
4.6 Resistor values. 32
4.7 Best, worst and typical cases for TC of the bandgap. 34
4.8 Best, worst and typical cases for the PSRR at 1 kHz. 37
4.9 Best, worst and typical cases for the PSRR at 100 kHz. 37
4.10 Best, worst and typical cases for the PSRR at 1 GHz. 37
4.11 Summary of the bandgap results. 38
4.12 Dimensions of the transistors for the two-stage operational amplifier. 40
4.13 Dimensions of the transistors for the bias circuit and start-up. 42
4.14 Best, worst and typical cases for the DC gain for 0,65 V. 44
4.15 Best, worst and typical cases for the DC gain for 0,35 V. 44
4.16 Best, worst and typical cases for the phase margin for 0,65 V. 45
4.17 Best, worst and typical cases the phase margin for 0,35 V. 45
4.18 Best, worst and typical cases for the PSRR for 0,35V at 1 kHz. 47
4.19 Best, worst and typical cases for the PSRR for 0,65V at 1 kHz. 47
4.20 Best, worst and typical cases for the delay for the Over Voltage Detector. 52
4.21 Best, worst and typical cases for the delay for the under voltage detector. 52
4.22 Summary of the comparators results. 52
4.23 Dimensions of the transistors for the peak detectors and bias circuit. 55
4.24 Best, worst and typical cases for the delay for the positive detector for a 50 ns peak. 56
4.25 Best, worst and typical Cases for the delay for the positive detector for a 100 ns peak. 56
4.26 Best, worst and typical cases for the delay for the negative detector for a 50 ns peak. 57
4.27 Best, worst and typical cases for the delay for the negative detector for a 100 ns peak. 58

5.1 Size of the transistors of the FVC 66
5.2 Dimensions of the transistors for the frequency divider. 67
5.3 Best, worst and typical cases for the output of the FVC with 1 GHz input wave. . 74
5.4 Best, worst and typical cases for the output of the FVC with 800 MHz input wave. 75
5.5 Best, worst and typical cases for the output of the FVC with 1,2 GHz input wave. 75

Abbreviations and Symbols

ADC	Analog-Digital converter
AMBs	Analog Boundary Modules
ATAP	Analog Test Access Port
ATE	Automated Test Equipment
BIST	Built-in Self-Test
CAGR	Compound Annual Growth Rate
CMRR	Common-mode Rejection Ratio
CTAT	Complementary to Absolute Temperature
C_{ox}	Gate-Oxide Capacitance per unit
CUT	Circuit Under Test
DC	Direct Current
DAC	Digital-Analog converter
DCD	Duty cycle Distortion
DSP	Digital Signal Processing unit
FFT	Fast Fourier Transform
FVC	Frequency-to-Voltage Converter
IC	Integrated Circuit
k	Boltzmann Constant
L	Length of the Transistor
LDOs	Low Dropout Regulators
LFSR	Linear Feedback Shift Register
MISR	Multi-Input Shift Register
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NAND	Not AND
OUV	Over and Under Voltage
PLL	Phase-Locked Loop
PTAT	(Proportional to Absolute Temperature)
PVT	Process, Supply, Temperature
PSD	Power Spectral Density
q	Electrical Charge of the Electron
RCF	Resistor–Capacitor Filter
RMS	Root Mean Square
ROM	Read-only-memory
SNR	Signal-to-Noise Ratio
TBIC	Test Bus Interface Circuit
TC	Temperature Coefficient
$\mu_{n/p}$	Carrier Mobility
VCO	Voltage-Controlled Oscillator
W	Width of the Transistor

Chapter 1

Introduction

With the development of more complex systems and the use of very deep sub-micron technologies, it became possible to integrate analog and digital circuits in the same substrate. This has promoted the development of increasingly complex mixed-signal integrated systems, both in functional and structural terms.

Nevertheless, this also implies a higher difficulty of testing these integrated microsystems, which are mandatory to ensure that malfunctioning devices are not sent to the market.

1.1 Context and Motivation

The global Analog and Mixed-Signal (AMS) IP market is expected to grow at a CAGR (Compound Annual Growth Rate) of 14.2% [1]. The reasons for the increased presence of analog circuit in an IC (Integrated Circuit) can be summarized as follows: [2][3]:

- Need of an interface between sensors and actuators and digital signal processors;
- Increased use of wireless communications, where the analog circuit is at the front-end of the transceiver;
- The combination of analog and digital circuits into a single chip improves the system's power consumption, the operation speed and decreases system noise;
- Reduction of the system size as well as of production costs.

Mixed-signal IC are common in areas such as telecommunications, multimedia, automotive, avionics, and robotics. With the emergence of various mixed-signal systems, the testing of these heterogeneous circuits has become a major concern, since it is not trivial to test the functionality, quality, and performance of each functional block of a system and then test the overall system.

Truthfully, the bottleneck of testing mixed-signal circuits is in the analog part. Unlike digital circuits, whose test techniques have been extensively developed to be fast and simple with low design overhead, the development of methodologies for testing analog circuits has been stagnated.

The traditional methods are substantially more difficult to implement and time-consuming. There are several reasons for this situation[4][5]:

- The response/performance of an analog circuit is more sensitive to factors like component's values, noise, and thermal effects;
- Fault detection is more difficult due to the continuous nature of time and analog quantities.
- The test equipment used must be more precise than the circuit under test and the input testing stimuli more accurate;
- The variety of signals and parameters found in analog testing is higher than that found in the digital counterpart.
  - The stimuli input and response signal can range from DC (Direct Current) voltage, linear ramps and impulses to sine waves and frequency modulation;
  - There is great variability of parameters to evaluate such as amplitude, phase delay, SNR(Signal-to-noise ratio), jitter and other temporal relations.
- The relation between inputs and outputs in analog circuits is not deterministic, unlike digital circuits, making it difficult to create a reliable fault model. Consequently the results of a testing simulation based on a fault model are not accurate;
- Due to the high integration level of the systems, it is difficult to access the nodes needed to test the circuit;
- The interface used between the device under test and the test equipment has to be taken into consideration during testing, otherwise it can influence the obtained results;

Considering all the reasons mentioned, the cost of analog testing often represents the largest portion of the total cost associated with mixed-signal IC testing. This cost results from the fact that the mixed-signal Automated Test Equipment (ATE) must be capable of meeting the required performance and functionalities demanded by analog testing.

This dissertation focuses on the study and implementation of an analog Built-in Self-Test (BIST) approach based on the design of specific test instruments (hardware blocks) to be used as auxiliary circuits. These instruments are meant to allow the measurement of specific performance characterization parameters, which can be integrated in an IC to support the implementation of a self-test approach [6] and to know, therefore, if the circuit performs as expected. With this technique, it is possible to test each component of the system, which reduces the complexity of the test. Additionally, it reduces production and testing costs since it is not necessary to have high-cost external equipment. Furthermore, it allows for the verification of long-term reliability through periodic tests and provides means for monitoring important analog parameters in real-time[4] [5].

1.2 Objectives

This dissertation was proposed by Synopsys Portugal with the following objectives: perform a study on analog BIST and implement a set of simple instruments that support the implementation of an analog BIST system. The instruments should be able to test specific parameters, specified by Synopsys, of a low-dropout voltage regulator and an oscillator. In the regulator the parameters to be tested are: over- and under- Voltage, settling time and voltage ripple. As for the oscillator the parameters to be tested are: frequency drift, settling time and duty-cycle distortion.

1.3 Structure

This dissertation addresses the development of dedicated instruments that can be included in an integrated mixed-signal device to test specific functional blocks *in-situ*. It is structured in six chapters of which this is the first one and presents the context and motivation of the dissertation, as well as the stated objectives.

In chapter 2, a general overview of analog BIST is given with the presentation of the main definitions and examples of generic architectures of BIST approaches. Relevant aspects of a BIST implementation, such as the on-chip generation of test stimuli, response analysis, and the access to internal test nodes are also presented. Throughout the chapter, advantages and disadvantages of analog BIST are highlighted. The chapter finishes with some considerations on testing analog circuits with a BIST approach.

Chapter 3 details the circuits under test in this work. The definition and relevance of the parameters to be measured are discussed, together with the presentation of examples of circuits published in the literature that have been proposed to test for these parameters.

Chapter 4 describes the various test instruments being proposed here to accomplish the required specific test operations. Besides the description of the design details, preliminary simulation results for the voltage regulator are also presented that characterize his performance.

Chapter 5 describes the instruments designed to test the oscillator. The specific test operations that need to be implemented are the measurement of frequency drift, duty-cycle distortion, and the settling time, i. e., the time the oscillator takes to reach the steady-state operation, at the specified frequency, after turn-on. Design details and preliminary simulation results are provided.

Chapter 6 highlights the main conclusions and identifies further work that should be developed to improve the performance of the designed instruments.

Chapter 2

Design for Testability and Built-In Self-Test Concepts

In this chapter, a general view of analog testing is presented with the presentation of the definition and description of typical analog and mixed-signal built-in and self-test (BIST) schemes. Relevant aspects of a BIST implementation such as the on-chip generation of test stimuli and how the responses of the circuits under test are evaluated in a BIST scheme will be detailed. The access to internal test nodes will also be discussed. The chapter will end with some considerations on BIST implementation.

2.1 Built-in Self-Test

A BIST system is a design for testability approach that provides the ability of self-testing key circuit parameters by adding or reusing hardware that already exists on the IC where it is integrated. Generally, a BIST operation consists in stimulating the circuit under test (CUT) and then capture and evaluate the circuit's response, which is often a simple PASS/FAIL signal. With an appropriate BIST implementation, the cost of testing per chip during production can be reduced significantly. It, also, makes it possible to test individually analog functional blocks, which reduces the test complexity. Contrarily to digital BIST, where methods have been extensively studied and implemented, BIST for analogs circuits is an area that has been developing slowly. BIST techniques can be applied to several analog and mixed-signal (AMS) components or functionalities: ADC/DAC (Analog-Digital Converter/Digital-Analog Converter), filters, amplifiers, comparators, PLL (Phase-Locked Loop), etc. Given their specific functional characteristics and performance characterization parameters, it is not possible to find a single approach or instruments that allows testing all these AMS devices or functions. Furthermore, it would depend also of the specific results meant to be achieved with the test operation.

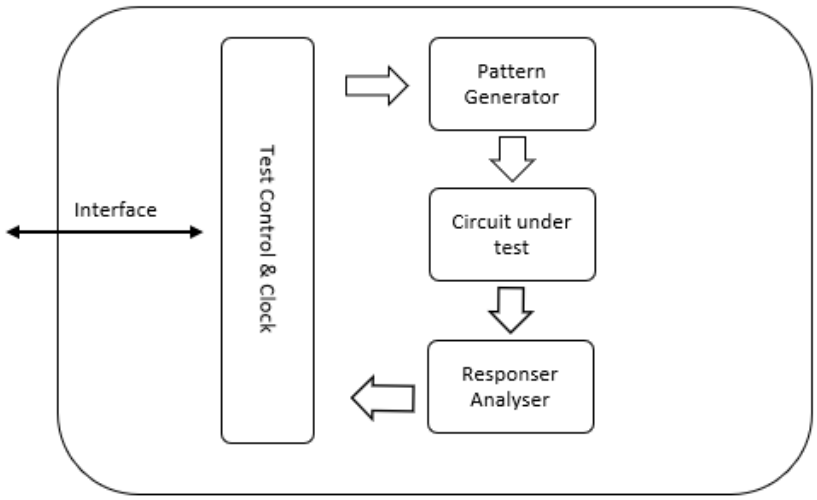

Figure 2.1: BIST architecture.

2.1.1 BIST Architecture

As seen in figure 2.1, an ideal BIST architecture is comprised of several fundamental components, besides the circuit under test: on-chip pattern generator and response/signature analyzer, a test controller, a clock and an interface to communicate with the exterior. The pattern generator provides the test with the appropriate inputs so that the maximum number of faults possible is covered. The response/signature analyzer should compare the response given by CUT with the expected response and give a PASS/FAIL signal which then will be read by the external tester. The test controller manages the actions of the BIST circuitry and provides the test circuit with a clock and an external interface.

Other characteristics of a BIST implementation are: the test circuit should not affect the normal operation of the system where it is integrated in; The circuitry of the BIST should be testable [5] and should always be tested before performing any testing operation to the CUT.

2.1.2 Test Generation

One of the specificities of an AMS BIST scheme is the on-chip generation of an analog input stimuli that complies with the requirements of the CUT functionality. This is one of the main challenges of a BIST implementation since it is not easy to generate an analog stimulus with predictable and controllable characteristics [7] and that allows the detection of all possible faults. Another problem is the area overhead introduced by the extra circuitry that can lead to the reduction of yield [8].

Table 2.1: Relationship between type of measurement and test input.

Type of measurement	Test inputs
DC static	Constant input values
AC dynamic	Sine wave waveforms with variable frequency
Transient response	Pulse signals, ramp or triangular waveforms

2.1.2.1 Advantages

However, if it is successfully implemented, it introduces the following advantages when solving several problems:

- The difficulties associated with the access to internal test nodes to inject the input signal are decreased;
- The degradation the input signal suffers in the path from the test generator to the testing nodes is reduced, since lower noise and losses are introduced;
- Testing time is significantly reduced;
- The costly external instrumentation and wiring are avoided.

2.1.2.2 Examples of Test Stimuli

When testing analog circuits, there is a large set of input signals to be considered since the type of waveform to be generated depends on the test to be performed, namely which parameters the test considers [8]. Table 2.1 shows the relationship between the type of measurement and the test stimuli.

The use of traditional analog generators, such as relaxation or tuned oscillators, is not appropriate for BIST implementation. The reason resides in the fact that the values of analog components are sensitive to variations of the fabrication process, which consequently affects the amplitude and frequency of the signal. They are also hard to manage and do not generate multi-tone signals [9].

Given the disadvantages associated with the analog generators in an on-chip configuration, the test stimuli in BIST are often achieved through digital circuitry. Therefore some of these generators will be presented next.

Direct digital frequency synthesis is presented in [10]. This method generates analog sine-waves from the digital sine-wave saved in a ROM (Read-Only-Memory) that are afterwords converted to their analog counterpart through a DAC and an analog filter. The main disadvantage of this method is the area added by the DAC and the ROM, if these components do not exist already on-chip.

In [7], a staircase-like exponential waveform is used as test stimulus. This stimulus together a 3rd order polynomial fitting algorithm are applied to measure the offset, gain, harmonic distortion of a high-resolution sigma-delta ADC. The circuit behaves as if a linear ramp was used.

In [11] a delta-sigma oscillator and multi-tone delta-sigma oscillators are presented. In [12], a switch-capacitor multi-mode stimuli generator for BIST implementation is presented. This configuration permits the tester to choose the type of waveform (ramp, pulse, sine-wave) it wants to apply and its characteristics (amplitude and frequency). The linear feedback shift register (LFSR) used in digital BIST stimuli can be converted to an analog signal [5].

In [10], a BIST with oscillation based testing is presented where the generator on-chip is not necessary. In this configuration, the CUT is turned into an oscillator and its frequency is evaluated to detect faults. This technique is not simple to implement since it requires the reconfiguration of the circuit.

2.1.3 Response Analyser

Generally, a response/signature analyzer unit captures and evaluates the output of the CUT and compares it with the expected response. The result of this evaluation is then sent to the control unit which then communicates the result to the external tester.

2.1.3.1 Disadvantages

During the design of the response analyzer, the designer should take into consideration several consequences of adding extra circuitry to minimize the impact of the BIST circuitry on the circuits or systems where they are inserted [8] :

- The increased area of silicon can cause the reduction of production yield;
- The introduction of additional hardware, like multiplexers, in the signal path can cause the degradation of the circuit performance;
- Increased power consumption.

The second item in the list can be compensated by the designer by taking into account the additional load of the extra circuitry during the design phase.

2.1.3.2 Examples of Response Analysers

The capturing and evaluation of the output response in BIST circuits can involve several different techniques of signal processing and conditioning.

The utilization of an FFT (Fast Fourier Transform) provides several parameters that can be used to evaluate the goodness of the CUT [13], such as the SNR and the harmonic distortion that helps to analyze the linearity performance of the CUT. However, the implementation of the FFT on-chip implies increased area and resources overhead, if a digital signal processing unit (DSP), capable of meeting the necessary computational power, is not already available. In [14], instead of an FFT, a digital filter is used which uses less computational resources than the FFT.

The correlation of a sine wave can be used to obtain the spectral power of the output signal when only when one frequency is considered. This method uses less computational power than

the FFT if there is only a small number of frequencies to be considered [11]. However, the sine and cosine waves used have to be saved in a ROM or have to be generated.

In [15], a BIST technique is presented where the parameters to be evaluated, such as τ, gain, phase between input and output signals, CMRR (Common-mode rejection ratio), slew rate and other, are translated into a determined voltage value and then compared to minimum and maximum voltage references, determining a range of acceptable values. This is a very efficient BIST method but the area increases significantly, due to the use of analog switches, and there is a degradation of the signal [4].

The BIST implementation presented in [9] allows to obtain four parameters of an ADC — offset, gain, 2nd and 3rd harmonics — after applying a 3rd polynomial fitting algorithm to the ADC output. The four performance parameters are mathematically related to the four coefficients of the polynomial algorithm. This a very simple measuring technique, which can be performed taking advantage of an existing DSP on-chip.

The method presented in [4] uses a Multi-Input Shift Register (MISR) to create a signature based on the output of the ADC, which is then compared to the signature stored in memory. This technique is also used in digital BIST.

When using DSP in a BIST implementation, the need to add data converters like ADC and DAC, should be considered. Besides the area overhead they bring, their resolution can affect testing results so they should be tested first and their impact on the results should be considered during the design phase. Truthfully, to validate the results of any BIST implementation, the test circuitry should be self testable and be up to 10 times more accurate than the circuit under test [5].

2.1.3.3 Advantages

There are several benefits of having the response analyzer integrated on chip:

- It is not necessary to have expensive and complex external instrumentation equipment to test a circuit which consequently leads to the reduction of the test cost;
- There is a decrease in the number of internal test nodes that need to be accessed, which leads to a reduction in the number of access pins in the IC;
- There is a reduction of noise and there is no need to used external acquisition equipment during the measurement of the output results of the CUT, consequently, the number of errors in the measurement results is decreased;
- With these units it is possible to test the circuit during its normal operation.

2.1.4 Access to Test Nodes

The addition of an infrastructure to access internal nodes enhances the controllability and observability of the desired nodes and permits the separation of the digital and analog domain in a mixed-signal circuit, which makes the testing process less complex and less costly. The impact of

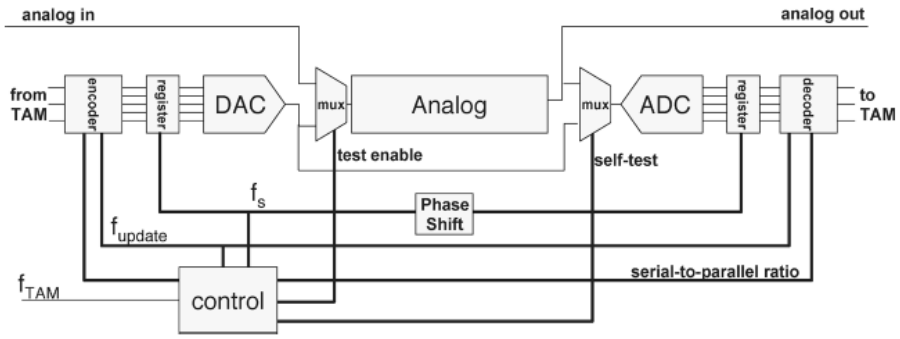

Figure 2.2: Analog test wrapper. Adapted from [17]

the addiction of the infrastructure in terms of area overhead, performance, and other parameters should be considered during the design phase.

In [16], three schemes are proposed to enhance analog testability. They work alongside digital testing techniques such as the IEEE 1149.1 standard and used digital BIST to control the test and require the addition of data converters. This provides a unified framework for mixed-signal testing. The first scheme proposes the introduction of analog multiplexers at the input of each analog macro (i.e CUT) which provides controllability. Another multiplexer which is common to the output of all macros is placed to observe the desired output. The test input signals are transmitted through a demultiplexer. The other scheme is based on analog buses where the connection between the analog macro and the bus is made through a transmission gate, analogous to analog switches. The final scheme is based on a scan-path. The scan-chain is composed of analog switches that allow to bypass the circuits that are not under test.

A test infrastructure for mixed-signal systems that uses analog test wrappers is given in [17]. The test wrapper provides each analog core with test information that includes only digital test patterns, the test configuration, clock frequency, and PASS/FAIL criteria. With this, the analog core is converted to virtual digital cores with the input being a sequential test pattern of digitized analog signals. Consequently, to serve as an interface between the analog core and the digital portion, an on-chip ADC/DAC is added. A block diagram of the analog test wrapper can be seen in 2.2.

Another proposed method is the IEEE 1149.4 standard. The objective of the IEEE 1149.4 standard is *"to define, document, and promote the use of a standard mixed-signal test bus that can be used at the device and assembly levels to improve the controllability and observability of mixed-signal designs and to support mixed-signal built-in test structures in order to reduce both test development time and test cost, and to improve test quality."* [18].

This standard is an extension of the IEEE 1149.1 standard where the focus is the digital domain. In this new method, two extra analog pins were added to form the analog test access port (ATAP). They are the analog test data input and the analog test data output. The connection between the ATAP and the digital test access port (TAP) is managed by the TBIC (Test Bus Interface

Circuit). The access to the analog boundary modules (AMBs), the equivalent to the boundary scan cell in digital, is done by analog buses. The IEEE 1149.4 standard allows the testing of open/short faults in simple interconnections, the testing of discrete analog components and connections between ICs and the testing of the internal analog functions of an IC [18] [4]. This standard allows to access and control integrated BIST blocks, through the instruction RUNBIST, which permits to run and visualize the output response of the BIST. The introduction of an analog boundary scan in some applications is a waste of resources since the number of test nodes is low [19].

In [19], an alternative to the use of analog pins to access the CUT is given. By using data converters the tester can interface with the CUT in the digital domain. Then the test signals can be injected through the 'swopamp' that is a configurable op-amp which has two operation modes: normal mode of operation and to function as a buffer for the test signal. The degradation of the signal is minimal with this solution.

2.2 Conclusion

The utilization of BIST for testing analog and mixed-signal devices is not straightforward. There are several factors to be considered when this approach is used, such as the restrictions imposed by the device under test, the limitations of the BIST itself and the fact that there is not an universal approach to its implementation. On the one hand, some important benefits of BIST can be achieved due to:

- The elimination of external expensive testers;
- Reduction of measurements errors caused by external cabling;
- Reduction of test time/costs;
- Introduction of self-testability, allowing the circuit to be tested throughout its life-cycle;
- Some other benefits mentioned already in this chapter.

Nevertheless, some of these benefits are only achievable if the designer of the BIST considered several key ideas: The cost of the test and the test time must be less than the time and cost of developing and implementing the BIST. The BIST has to be more accurate than the CUT. The area overhead can lead to a reduction of yield, so to minimize this problem there should be a reuse of the hardware present on-chip, something that isn't always possible. Also, the BIST should not interfere with the CUT behavior, otherwise, there can be a degradation of the circuit performance.

In conclusion, when using a BIST approach to test AMS circuits a balance of the benefits and constrains should be made for each situation because in some cases it might not be the best solution.

Chapter 3

Review of Literature on Specific Test Approaches

This chapter describes the specific circuits to be tested, a voltage regulator and an oscillator, and the parameters to be measured in each case. Also, methods that have been proposed for testing these circuits after the measurement of the required parameters are summarised, being aspects that can be retained to be used in this dissertation highlighted.

3.1 Voltage Regulators

The main function of a voltage regulator circuit is to generate an output voltage whose value should remain constant independently of any input voltage and load variation. These circuits are essential in power supply devices since they provide a steady and reliable voltage, protecting the device they supply from damages caused by extreme voltage variations by acting as a buffer. Normally, the circuit of a voltage regulator consists of three parts:

- high gain amplifier;
- feedback circuit;
- stable reference voltage;
- pass element control circuit.

The feedback circuit helps to detect any variations in the output voltage. The pass element is driven by a control signal that depends on the feedback and the reference voltage to compensate for the variations detected. The pass element can be a PN junction Diode or a BJT transistor or a MOSFET. In this report, it will be discussed only the voltage regulators used in IC. There are two types of voltage regulators: linear voltage regulator and switching voltage regulator.

3.1.0.1 Linear Voltage regulator

A linear voltage regulator, also known as low-dropout voltage regulator (LDO), performs as a constant voltage generator, ideally regardless of load current and line voltage source variations. Its operation can be modeled as a voltage source whose output resistance is controlled by the feedback circuit. The resistance of the regulator varies when there is a variation in the load so that the output DC voltage remains constant. When a FET is employed as the series pass element, it can operate in the linear or in the saturation regions. Depending on the load configuration they can be divided into two types:

- **Series voltage regulator**:
  - The load is in series with the variable resistance.
- **Shunt voltage regulator**:
  - The variable resistance connects the power supply to the ground. The current is diverted from the load to the ground.

The linear voltage regulator is very simple to implement and provides a fast response time to load variations. However, they are not very efficient since the regulator imposes a minimum voltage drop (between the input and output) and thus significant heat losses can occur. Another disadvantage is that the output voltage cannot be higher than the input voltage. The low dropout regulators, which are very common in low power devices, work on these conditions.

3.1.0.2 Switching Voltage regulator

A switch voltage regulator switches a device in series to an ON or OFF state. The feedback loop corrects the output voltage by changing the ON time of the switching element. If a FET is used, it works in the saturation region during ON time and in the cut-off region during OFF time. The most common topologies are:

- **Buck (step-down)**
  - The DC output voltage is lower than the input DC voltage.
- **Boost (step-up)**
  - The DC output voltage is higher than the input DC voltage.
- **buck-boost(step-up/step-down)**
  - The DC output voltage is the opposite polarity of the input DC voltage.

Other topologies include the flyback, SEPIC, Cuk and Cuk-Buck, push-pull, forward, full-bridge, and half-bridge topologies.

Unlike the linear regulators, these can generate output DC voltages higher than the input and the polarity of the output can be the opposite of the input DC voltage. They are more efficient than the linear regulators since the active device operates in switch mode and thus dissipate less power.

3.1.1 Performance Characterization Parameters

3.1.1.1 Over- and Under- Voltage

An over-voltage occurs when the device generates a voltage that exceeds the maximum operating voltage established by the manufacturer. An over-voltage, depending on its duration, can be considered transient or permanent. A transient voltage lasts a very short time and can be caused by lightning impulses and switching impulses of the system, insulation failure, arcing ground, and resonance.

An under-voltage occurs when the device generates a voltage below the minimum operating voltage established by the manufacturer. It can be caused by increases of the load or malfunctioning of the power supply.

The voltage limits of the regulator must be respected. Otherwise, it may cause damages or the malfunctioning of other circuits connected to it. So, it is important to test if the output voltage of the CUT is inside the range of acceptable values.

3.1.1.2 Settling Time

Another important parameter of a voltage regulator is the settling time, which corresponds to the time required for the output of a device to achieve and remain within a given error band following some input stimulus or a variation in the load. The settling time is comprised of a propagation delay (delay time), plus the slew time, which corresponds to the time required for the output to arrive at the vicinity of the final value, plus the recovery time and then finally settling in the final value. The slew rate and the recovery time have a big impact on the settling time [20].

The performance of a voltage regular can be measured by its transient behavior when load variations occur in the circuit. Ideally, there should not be seen any variation in the output voltage, but in practice, that is not the case. So, normally, if there is a disturbance in the circuits, like a variation in the load current, a good voltage regular has to react fast (i.e., in the shortest possible time) to stabilize the output voltage. As the load current increases, the higher the degradation of the stability [21]. So testing for the settling time is important to establish if the variations occurred comply with allowed operating conditions.

3.1.1.3 Voltage Ripple

The ripple voltage corresponds to a periodic unwanted small variation in a DC voltage. It can be originated by the output of a rectifier circuit or the periodic switching of the DC voltage. The main function of a voltage regulator is to provide a constant DC voltage. The occurrence of a variable

voltage, even if very small, can cause damage to circuits that are sensitive to voltage variations. So, the measurement of the ripple voltage is important to verify if the CUT is working inside the established ripple voltage limits.

3.1.2 Testing methods

In this section, methods found in the literature to test the CUT in the requested parameters will be presented. Some methods presented here are not specific BIST solutions but could be part of one.

3.1.2.1 Under- and Over- Voltage

In [22], a window comparator is used to detect over- and under- voltage occurrences. Considering there are an inverter and a CMOS transistor at the output of the comparator, the overvoltage output is driven low if the voltage in the inverting input of the comparator is higher than the established overvoltage threshold. The undervoltage output is drive low if the voltage in the on-inverting input is lower than the set undervoltage threshold. The performance of the window comparator method depends on the stability of its reference source.

An overvoltage and undervoltage detection circuit basen on only one transistor is presented in [23]. The detection circuit is composed of a level shifter, a voltage clamper, a voltage regulator, a hysteresis buffer, and a voltage detector. The functional block of the circuit can be seen in 3.1. By comparing the voltage generated by the voltage regulator to the voltage at the output of the buffer, the circuit detects the presence of an over or an under voltage situation. The active area of this implementation is 0,0625 mm^2.

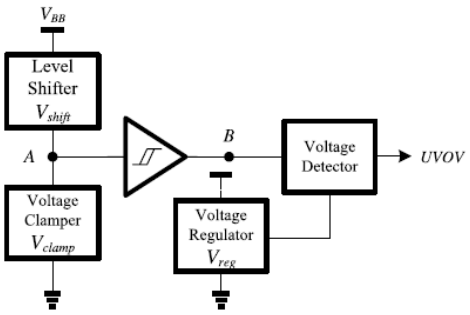

Figure 3.1: Overvoltage and undervoltage detection circuit. Adapted from [23].

3.1.2.2 Settling Time

In [24] [25], an oscilloscope is required to measure the turn-on time (i.e the settling time) of a DC-DC converter (step-down or a step-up). The test software measures the time it takes to reach the desired output voltage after the input voltage was applied to the DC-DC converter. For this test, one SMU (Source-Measure Unit) channel of a DC power analyzer is applied to the input voltage.

One of the channels of the oscilloscope is connected across the input of the DC-DC converter and the other to the output of the converter.

No references to circuits to measure the settling time or BIST solutions were found in the literature.

3.1.2.3 Ripple Voltage

In [25] a method to measure the ripple is presented, through a spectrum analyzer, the ripple is measured in the frequency domain. The testing software being used analyzes, measures, and displays the ripple based on the selected start, stop and bandwidth values. In [26] measuring ripple trough a spectrum analyzer is also used. To use this method as an on-chip solution, it would be necessary to add data-converters and a DSP.

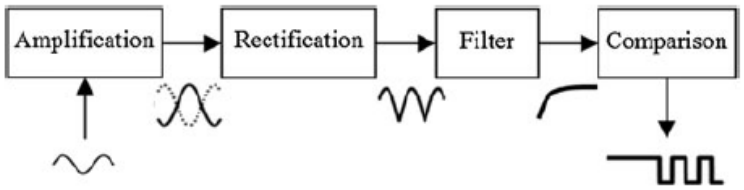

Figure 3.2: Block diagram of the ripple detector. Adapted from [27].

In [27] a BIST implementation based on root mean square (RMS) method for ripple detection in a voltage regulator is presented. The RMS sensor is designed to detect 10 to 50 mV peak-to-peak ripple on the supply voltage of 1,2 V, in a bandwidth of 220 MHz. The architecture of the detector can be seen in 3.2. The principle of this technique is, first, to amplify the input signal, which will then be rectified and filtered. The resulting DC signal of this operation is proportional to the amplitude of the input ripple signal. The digital output of this circuit is a PASS or FAIL signal, depending on the comparison between the output of the filter with an external DC reference input. The detection time of this BIST implementation is lower than 90 ns, depending on the ripple level and the DC reference.

A ripple detection circuit for on-chip testing that also uses the RMS method can be seen in [28]. This detector is capable of sensing a peak to peak ripple voltage in the range of 8 mV to 100 mV in a supply voltage of 1.2 V with an operating frequency of 220 MHz. This circuit behavior is very similar to the circuit presented before. The amplified input signal is injected in a detector circuit that generates a DC output proportional to the input peak amplitude. The DC output is then compared to a DC reference. In case of ripple detection, the output of the ripple detection circuit will be a high-level signal. The DC voltage reference used in the comparator is built-in, unlike the previous detector. The detection time of the ripple in this implementation is 0.5 ns.

3.2 Oscillators

An oscillator circuit generates a continuous, periodic, alternating waveform without any input. In order to generate the desired waveform, the circuit converts the DC power supply to an alternating waveform whose frequency is determined by the circuit components. A basic oscillator configuration is an amplifier whose output is connected to its input through positive or regenerative feedback. When DC power is turned ON, the noise present in the system, travels around the loop, getting amplified until reaching the desired waveform and frequency. Oscillators generate signals that are used in radio and television transmitters, clock signals, quartz clocks, microcontroller systems, etc.

There are two main types of oscillators: the Harmonic or Linear Oscillators that generate sine waves and the Relaxation or Non-Linear Oscillators that generate non-sinusoidal wave-forms like saw-tooth, triangular or square wave-forms. For each type of oscillator the main configurations are:

- **Harmonic or Linear Oscillators**
  - Phase Shift oscillator
  - The Wien-Bridge oscillator
  - Hartley, Colpitts, and Clapp oscillators
  - Crystal oscillator
  - Armstrong oscillator
- **Relaxation or Non-Linear Oscillators**
  - Multivibrator
  - Pearson–Anson oscillator
  - Ring oscillator
  - Delay-line oscillator
  - Royer oscillator.

Another type of oscillator worth mention is the VCO (Voltage-Controlled Oscillator) whose oscillation frequency is controlled by a voltage input. They can be harmonic or a relaxation oscillators. They are, for instance, a fundamental part of a PLL and are used in frequency modulation and phase modulation.

3.2.1 Parameters

In this section, the frequency drift, the duty-cycle distortion, and the settling time parameters are detailed. As in the previous section, some methods presented here are not specific BIST solution but could be part of one.

3.2.1.1 Frequency Drift

Frequency drift corresponds to the variation in an oscillator frequency whose value should be constant. Frequency drift can be caused by the aging of the circuit components, variations in components values due to temperature, humidity, and other environmental factors and poor power supply, namely due to ripple of the voltage provided by the power supply LDO. Drift in the frequency is a long term effect which means that it may not arise until devices are in the field for some years.

The frequency drift can cause problems in communication systems. For example, a device works in a certain frequency band but due to the drift, it starts working in another band which, consequently, causes synchronization issues. Also, the device could have drifted to an illegal band which can cause serious legal problems. Another case is when the oscillator generates a clock with a given frequency, but the drift changes the frequency of the generated clock. The application that uses this clock can start having synchronization issues, data loss, and other serious problems.

Given the reasons mentioned, it is important to measure the frequency drift regularly, during its lifetime, which is something that is possible with a BIST implementation.

3.2.1.2 duty-cycle Distortion

duty-cycle distortion (DCD) is a type of deterministic jitter that occurs when there is a deviation in the expected 50% duty-cycle of a square waveform. This can be caused by asymmetrical rise time and fall time of the waveform [29]. A consequence of DCD is the variation of the average voltage offset. And the appearance of errors in applications where the duty-cycle is an important parameter like, for example, an electronic device that produces sounds or in a communication system where the edges of the clock are fundamental for communication synchronization. Making this a parameter a relevant parameter to test.

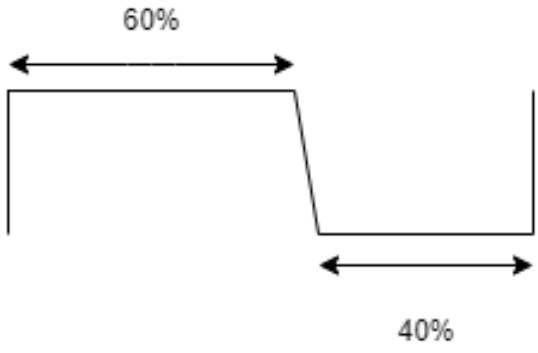

Figure 3.3: duty-cycle distortion.

3.2.1.3 Settling Time

The settling time in oscillators refers to the time it takes to achieve the desired frequency within a given error band. The settling time of an oscillator is a significant parameter of the circuit since it is directly related to how much fast can the oscillator generate the desired signal.

3.2.2 Testing methods

In this section, methods found in the literature to test the CUT in the requested parameters will be presented.

3.2.2.1 Frequency Drift

One of the methods to measure the stability of the frequency is through a time interval counter [30]. This method starts by comparing the signal under test and a reference signal with another whose frequency is much lower. The two resulting signals are then divided by a factor of N. Their time difference is measured by a high-resolution time interval counter.

Through the beat frequency method is possible to measure the frequency variation. The signal of the oscillator under test is mixed with a slightly lower frequency reference oscillator. The resulting signal is then filtered by a low-pass filter and amplified. The frequency of the obtained signal corresponds to the difference between the two initial signals. Its measurement is done by a frequency counter [31].

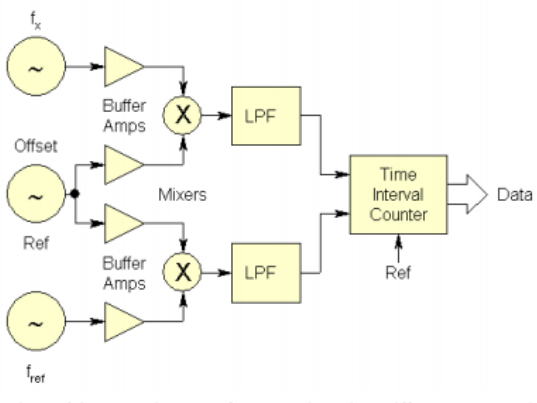

Figure 3.4: Dual mixer time difference method. Adapted from [30].

The dual mixer time difference method [30] is a mix of the beat frequency and the time interval method. In this method, two signals are mixed with a common offset reference. Then their time difference is measured by a time interval counter. A block diagram of the dual mixer time difference is presented in figure 3.4.

Another method to measure frequency variations is in the frequency domain. Through the power spectral density (PSD), it is possible to obtain, as a function of the Fourier frequency, the intensity of the phase or the frequency fluctuations [30].

In a frequency measuring system, the most important feature is its resolution, namely the resolution of its components. A digital frequency, period, or time interval counter resolution is determined mainly by clock rate and, if it exists, the efficiency of its analog interpolator. The averaging time of the measurement generally improves the measurement resolution. Another relevant parameter that affects the measuring system is noise. The stability of the reference source also influences the performance of the system [30]. In table 3.1, a summary of the advantages and disadvantages of each methods is presented [30].

Table 3.1: Advantages and disadvantages of the frequency drift measurements methods.

Method	Advantages	Disadvantages
Time Interval Counter	Simple; Low cost; Covers wide range of carrier frequencies;	Medium Resolution; Drift in the trigger point of the counter; Reference Oscillators;
Beat Frequency	Resolution enhanced by heterodyne factor; Reasonable Cost; Direct frequency measure;	Requires offset reference; Dead Time; No frequency sense; Single carrier frequency;
Dual Mixer	High resolution and low noise; Cancellation of offset reference, noise, and inaccuracy; No need for fixed reference channel;	Relatively complex; Single carrier frequency; Requires reference oscillators;
Spectral power	Simple to implement;	Needs a DSP;

A BIST solution to measure the frequency of a high-frequency super regenerative oscillator is presented in [32]. The working principle of this BIST scheme is to generate a digital output code (*Nf*) based on the counting of the number of oscillations periods in a specific time *Tref*. The frequency (*fosc*) is then measured through the following equation:

$$fosc = \frac{2 \times Nf}{Tref}$$

The *Tref* can be generated by chip resources or by the ATE. The BIST solution can be observed in 3.5. The function of the analog part is to do a division step to down conversion of the frequency, so the frequency of the signal is in the range of operating frequencies of the *"digital standard cells in the targeted process technology"* [32]. The buffer transforms the output voltage of the oscillator into the corresponding signals. The outputs signals of the analog block are two square waves used to drive the asynchronous counter. The frequency of one of the signals is equal to the eighth of the frequency of the oscillator and the other is a quarter of the frequency. The digital portion is composed of an asynchronous counter, a finite state machine (FSM) to control the different phases of the test, and a register bank to store the final count. The power supply is 1,2 V and the silicon area of the circuit is 5582 μm^2, the RMS current consumption is 5,7 mA and the current peak is 7 mA.

This BIST could be used to detected if the variation of the frequency of the oscillator did not

exceed the range of acceptable values by adding a comparison stage. This is also suggested by the authors of the paper.

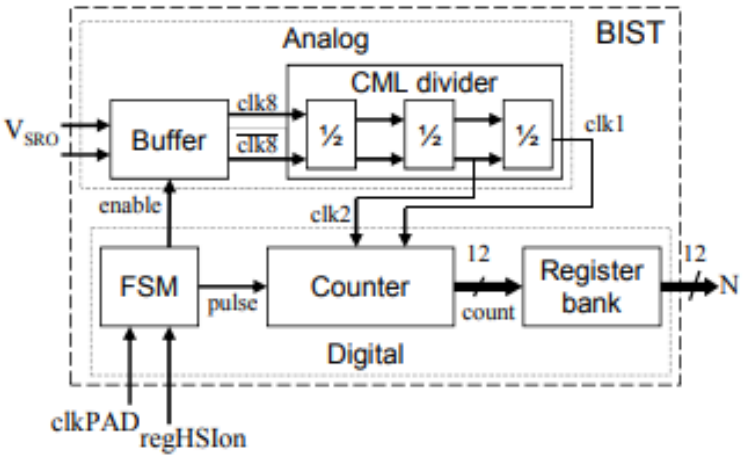

Figure 3.5: BIST structure. Adapted from [32].

A BIST implementation for measuring the output frequency of a VCO is given in [33]. It is composed of a frequency divider and an FVC (Frequency-to-Voltage Converter). The output signal of the VCO is injected in the frequency divider of factor N. In this implementation, given the high frequency of the input signal, the divider factor is 64. Thus, the output frequency of the divider is the VCO frequency divided by N. The FVC then converts the signal to its corresponding DC voltage. Given the linear relation between the output Dc voltage and the period of the input signal of the FVC it is possible to obtain the frequency of the oscillator and its tuning range. To check the functionality of the BIST solution, test nodes were inserted at the output of the VCO and at the input of the FVC. According to the authors, *"the test bandwidth, defined as* $2(fosc_{max} - fosc_{min})/(fosc_{max} + fosc_{min})$*, is limited by the input range of the FVC while the highest testing frequency is determined by the maximum operating speed of the frequency divider."* [33]. The frequency extraction error is less than $\pm 0,4$ %. The BIST area is 0,038 mm^2 and power consumption is 11 mW.

This BIST also could be used to detected if the variation of the frequency of the oscillator did not exceed the range of acceptable values by adding a comparison stage.

3.2.2.2 Duty-Cycle Distortion

A direct way of measuring duty-cycle distortion is through the use of spectrum analyzers, oscilloscopes, and eye diagrams [34] [35].

A method to detect duty-cycle distortion through the use of an integrator is described in [36]. By using an RC integrator, the DC value of the signal is obtained. This DC value is proportional to the value of the duty-cycle of the signal. In order to verify if there is not distortion, the DC value is

compared with the expected value. The settling time of this integrator is ~50 ns, in the worst-case scenario, which determines the cycle duration of the system operation. It is worth mentioning that this detector works alongside a duty-cycle corrector.

In [37], a duty-cycle error detector for a differential clock is presented. This implementation is also based on the fact that the average DC value of the signal is proportional to its duty-cycle. So, it is possible to detect the duty-cycle error through the use of a low pass filter and then convert the error to the respective voltage. In this implementation, the proposed detector is composed of a pair of pass filters and a differential integrator with two capacitors as seen in figure 3.6. The gain of the duty-cycle detector should be high to *"detect the minute duty error"* [37] and have a narrow bandwidth so that the glitch and other noises can be reduced. In order to have a narrow bandwidth feedback loop, a low pass filter is used and the differential integrator gives the detector the gain it needs.

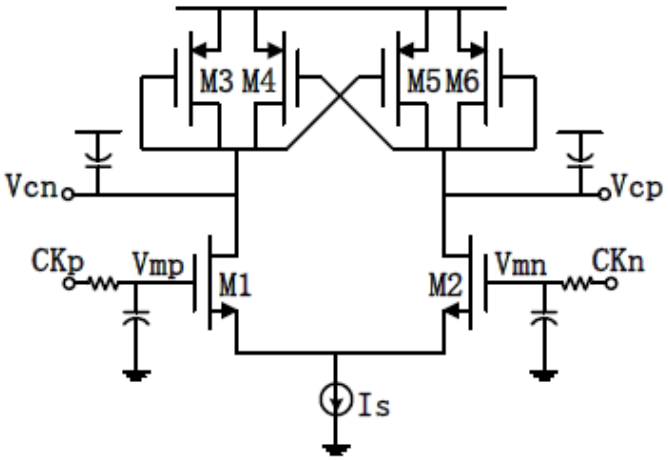

Figure 3.6: duty-cycle detector. Adapted from [37].

A duty-cycle detector in [38] establishes if the duty-cycle of a period signal produced by an incremental encoder is within the acceptable range (45-55%). The detector consists of an oscillator that produces a much higher frequency clock pulse than the signal under test. The counter increments when the signal under test is high and a clock pulse is produced. When the signal under test is low and a clock pulse occurs the counter decrements. In the next rising edge of the signal under test, the counter is put on hold. The evaluation of the counter value is made in the microprocessor.

In [39], the duty-cycle detector is implemented through a time-to-digital converter. In this detector, the widths of the clock high and low phases are converted to digital words through a time-to-digital converter. In terms of performance: *"the detector resolution is inversely proportional to the integrating capacitance C1 and the clock frequency Fclk, while directly proportional to the tail current Ib."* [39]. The duty-cycle value is not given directly but it can be calculated through the

following equation:

$$duty-cycle = \frac{digitalW\_low}{digitalW\_low + digitalW\_high}$$

3.2.2.3 Settling time

No references of methods, in the context of this dissertation, were found in the literature for the testing of this parameter.

Chapter 4

BIST Instruments

This chapter provides an overview of the instruments proposed to implement the BIST strategy and its specifications. The blocks for the testing of the voltage regulator are presented alongside the simulation results.

4.1 BIST Scheme

Figure 4.1 shows the block diagram of the BIST instruments to be designed. The system can be divided into the digital part and analog parts. This work will focus primarily on the analog part. The main analog blocks are the following: The over- and under-voltage block (OUV) is composed of two comparators, which are used to detect if the regulator's output voltage is above or below specified references.

The peak detector block has two peak detector circuits that capture and hold positive and negative voltage peaks of the voltage regulator. Two comparators were added to identify voltages peak over or below a given threshold.

The frequency to voltage converter (FVC) block's main function is to measure the frequency of an oscillator, making it possible to verify if the frequency of the oscillator is inside of an acceptable range of values.

In the RC filter (RCF) block, a low-pass filter is used to detect the duty-cycle distortion of a square-wave oscillator.

Another important block in our system is the voltage reference block. This block should, ideally, provide accurate voltages that are independent of temperature, power supply, and process variations. Since it is meant to be used in the comparison stages and in a voltage to current converter, it is important that the generated voltages are accurate and stable, seeing that their variation can cause the testing circuits to fail to detect errors in the voltage regulator and oscillator or to falsely detected errors in the circuits in test, and to degrade the performance of the test system. The topology chosen in order to satisfy these requirements is the bandgap voltage reference [40].

In order to verify if the settling time of the voltage regulator is below a maximum acceptable time, a counter, implemented in Verilog-A, is used. The settling time of the oscillator is also measured with a counter.

The digital part is composed of a finite state machine that controls the BIST system and serves as an interface with an external controller. This block was not fully implemented. Instead, smaller blocks were developed when it was necessary to send control signals to the analog part.

Another block that should be included in the system to work as an interface between the digital and analog parts is a successive-approximation ADC. The output of the RC filter and the FVC would have been connected to the ADC through a multiplexer. But due to time constraints, this was not implemented.

4.1.1 Specifications

The characteristics of the BIST blocks to be evaluated characterize their performance as test instruments.

Table 4.1 shows the values that determine the performance required for the voltage regulator. Indirectly, these parameters also determine the performance of the blocks under test.

The regulator has a nominal voltage of 1V. Therefore, the comparators used for the under/over voltage will have to detect, respectively, when the voltage of the regulator surpasses 1,2 V or underpasses 0,8 V.

Table 4.1: Voltage regulator specifications.

Nominal Output Voltage	1V
Over Voltage	+20 %
Under Voltage	-20 %
Maximum Peak	+40 %
Minimum Peak	-40 %
Settling Time @20%	1 ms

Given the specifications for the maximum and minimum peak, the comparators of the peak detector circuit, to detect peaks of 1,4 V and 0,6 V. In relation to its settling time, the voltage regulator is considered to be settled when it reaches 80% of its final value and it has to settle in less than 1 ms.

Table 4.2 shows the specifications required for the oscillator. The oscillator under test is a square-wave signal generator with an amplitude of 1 V, a nominal frequency of 1 GHz, and with a duty-cycle of 50%. The maximum frequency drift of the oscillator is 20%, i. e., a range between 800 MHz and 1,2 GHz. The duty-cycle of the wave can not be larger than 60% or narrower than 40%. The maximum settling time of the oscillator is 1μ and the frequency of the oscillator is considered to be settled when it reaches 90% of its final value, namely when the frequency reaches about 900 MHz.

The bandgap voltage reference circuit has a nominal voltage of 1,22 V. In a corners simulation the peak to peak deviation can not be higher than 3%. Since the output voltage of the bandgap is

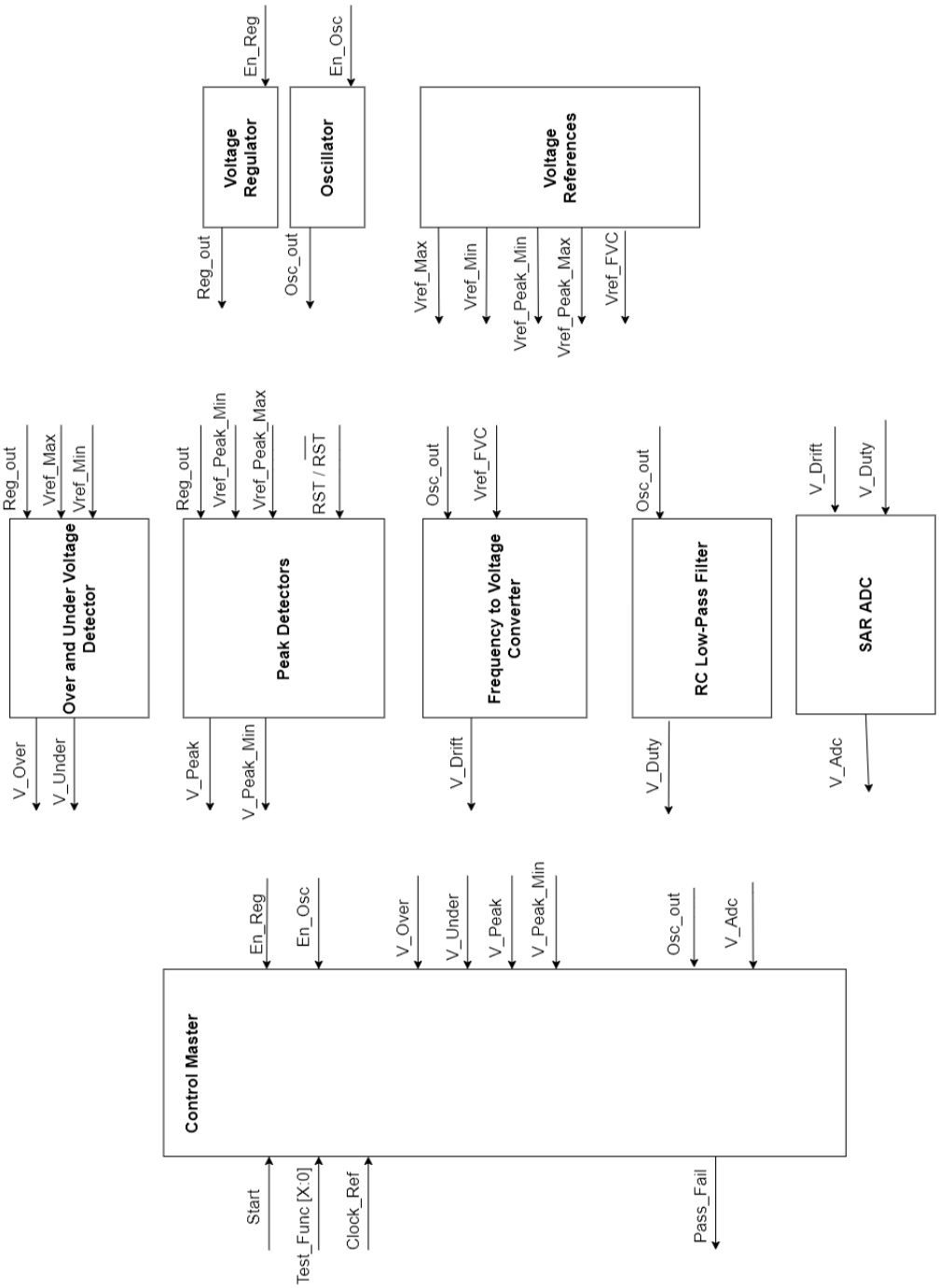

Figure 4.1: Block diagram of the BIST instruments.

Table 4.2: Oscillators specifications.

Nominal Output Voltage	1 V
Waveform	Square
Nominal Frequency	1 GHz
Maximum Frequency	+20 %
Minimum Frequency	-20 %
Nominal Duty Cycle	50 %
Maximum Duty Cycle	+10 %
Minimum Duty Cycle	-10 %
Settling Time @10%	1 μs

Table 4.3: Bandgap voltage reference specifications.

Nominal Output Voltage	1,22 V
Error (PVT)	3 %

lower than some of the voltages in the specifications, we will have to adapt our system. Section 4.2.1.1 describes how the system was adapted.

All circuits will be simulated against the chosen technology of 28 nm corners. The PVT (Process, Supply-Voltage, and Temperature) specifications can be seen in table 4.5.

Table 4.4: Other specifications.

Op-amp Offset	$\pm 2,5\ mV$
Operational Amplifier Gain	$\geq$ 1000 V/V

Other $\geq$ 1000 V/V, and the offset has to be $\pm 2,5$ mV.

Table 4.5: PVT Specifications of the BIST System.

Power-Supply Variation	1,8 $\pm$ 10 %
Temperature Variation	[-40,25,125] °C
Process Variation	Fast_Slow Slow_Fast Fast_Fast Slow_Slow
Resistor and Capacitor Variation	Fast Slow

4.2 Bandgap Voltage Reference

A voltage reference circuit is commonly used in data converters circuits, frequency to voltage converters, power supply circuits, and in other applications where a constant voltage, independent of temperature, power supply voltage, and process variation, is needed. In our system, we need an accurate and constant voltage for the comparators and to generate a constant current for the frequency to voltage converter. A bandgap voltage reference topology was chosen in order to accomplish this goal. The topology can be observed in figure 4.2.

In order to create an output voltage that varies very little with the temperature, a bandgap reference joins a PTAT (Proportional to Absolute Temperature) voltage with a CTAT (complementary to absolute temperature) voltage, see equation 4.8. In other words, a bandgap sums a voltage that increases as the temperature increases (PTAT) with a voltage that decreases with the rising of the temperature (CTAT), thus creating a voltage that, ideally, is independent of temperature variation.

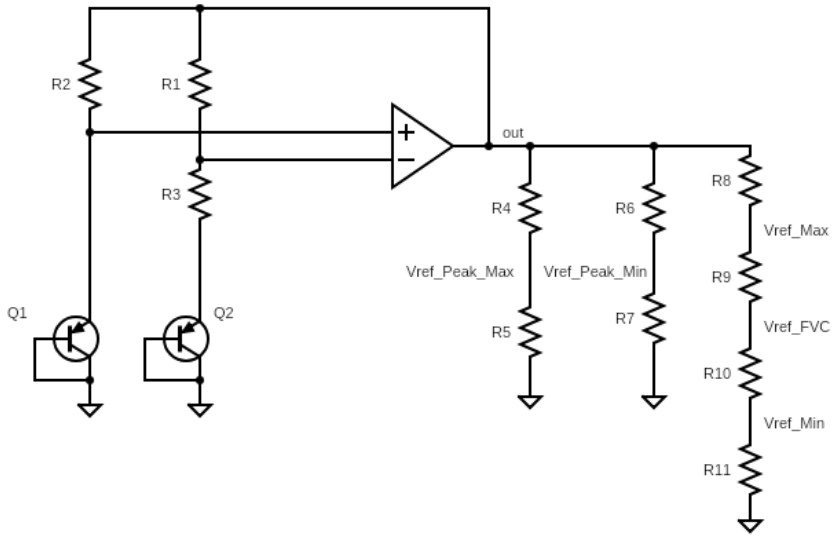

Figure 4.2: Bandgap voltage reference.

In the bandgap circuit, the CTAT voltage is generated by the voltage of a base-emitter junction. This can be demonstrated mathematical. First, we obtain the base-emitter voltage (V_{BE}) from the equation of the current collector:

$$I_C = I_S exp(\frac{V_{BE}}{V_T}) => V_{BE} = V_T ln(I_C/I_S) \tag{4.1}$$

where I_S is the saturation current and $V_T = kT/q$, where k is the Boltzmann constant and q is the electrical charge of the electron. Then, we derived the V_{BE} with respect to the temperature,

equation 4.2, maintaining I_C constant.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} ln(\frac{I_C}{I_S}) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = \tag{4.2}$$

$$= \frac{V_{BE} - (4+m)V_T - E_q/q}{T} \approx -1.54\ mV/K \tag{4.3}$$

The value of $\frac{\partial V_{BE}}{\partial T}$ was obtained through simulation, where the BJT was biased with a current of $\approx 3\ \mu$A.

The PTAT voltage is generated by the voltage difference of the base-emitter junctions biased at a fixed current but with different current densities.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{4.4}$$

$$= V_T ln(\frac{nI_0}{I_{S1}}) - V_T ln(\frac{I_0}{I_{S2}}) \tag{4.5}$$

$$= V_T ln(n) \tag{4.6}$$

Then, if we derived by the temperature we obtain a positive temperature coefficient:

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} ln(n) \tag{4.7}$$

The output voltage bandgap reference is given by equation 4.8. Since the temperature variation of the PTAT voltage and the CTAT voltage are not equal, then the voltage difference of the base-emitter junctions must be amplified by a factor K.

$$V_{REF} = V_{BE} + K\Delta V_{BE} \tag{4.8}$$

Considering n = 16, $\frac{\partial V_{BE}}{\partial T} = -1,54\ mV$ and $k/q = 0,087\ mV$, we can obtain the value of K by deriving the output voltage of the bandgap with respect to temperature.

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{K\partial \Delta V_{BE}}{\partial T} \tag{4.9}$$

$$= -1,54\ mV/K + K\frac{k}{q} ln(n) \tag{4.10}$$

$$K \approx 6,44 \tag{4.11}$$

4.2.1 Design of the Bandgap Voltage Reference

Now, in the chosen topology, we have to find which elements provide the amplification K, so we first start by finding the equation of the output voltage of the bandgap:

$$V_{REF} = V_{EB1} + V_{R2} \tag{4.12}$$

By assuming that our operational amplifier has a large gain and that the voltage at the input terminals are the same, then

$$V_{R3} = V_{EB1} - V_{EB2} = \Delta V_{EB} \tag{4.13}$$

Since the current that flows through R_3 is the same current that flows through R_1, then

$$V_{R1} = \frac{R_1}{R_3} V_{R3} = \frac{R_1}{R_3} \Delta V_{EB} \tag{4.14}$$

Considering the fact that the operational amplifier feedback makes $V_{R1} = V_{R2}$ and equation 4.14, the equation 4.12 turns into:

$$V_{REF} = V_{EB1} + \frac{R_1}{R_3} \Delta V_{EB} \tag{4.15}$$

By comparing equation 4.15 with equation 4.8, we can easily realize that the relationship between the resistances provides the necessary amplification mentioned before

$$K = \frac{R_1}{R_3} \tag{4.16}$$

Then, for our bandagap, where the BJT's were biased at a current of 3 μA, $V_{EB1} = 756\ mV, V_{EB2} = 685\ mV$ and the area of the BJT Q2 is 16 bigger than that of Q1, the values of the resistances are:

$$R1 \approx 156\ k\Omega \quad R2 \approx 156\ k\Omega \quad R3 \approx 24\ k\Omega \tag{4.17}$$

In figure 4.3, we can observe the output voltage of our bandgap configuration when the temperature varies between -40 to 125 °C. The output voltage is $1,2196$ V at 25 °C and presents a variation of $0,178$ %. Ideally, the variation should be zero, however the base-emitter voltage variation is not completely linear with the temperature, creating a slight variation in the output voltage. Also, the offset at the inputs of the operational amplifier creates an error in the output voltage.

4.2.1.1 Extra voltage references

Across the BIST system, we will need different voltage references for the comparators and the voltage to current converter in the frequency to voltage converter. Resistors were used to generate these voltages, as shown in figure 4.2.

Returning to section 4.1.1, where our specifications for the system are presented, it is possible to see that we need voltages that are higher or close to the output voltage of the bandgap. For example, the maximum peak detector comparator would need a voltage of 1,4 V, which is higher than the output of the bandgap. Therefore, we had to adapt the output voltage of the regulator by dividing it by two with two resistors of value 1 kΩ. Another reason to lower this voltages is to reuse the same operational amplifier across all BIST system. The current in each resistor branch is $\approx 10\ \mu$A. The resistor values are shown in table 4.6. It is important to mention that the voltage references were lowered/increased concerning its specification value.

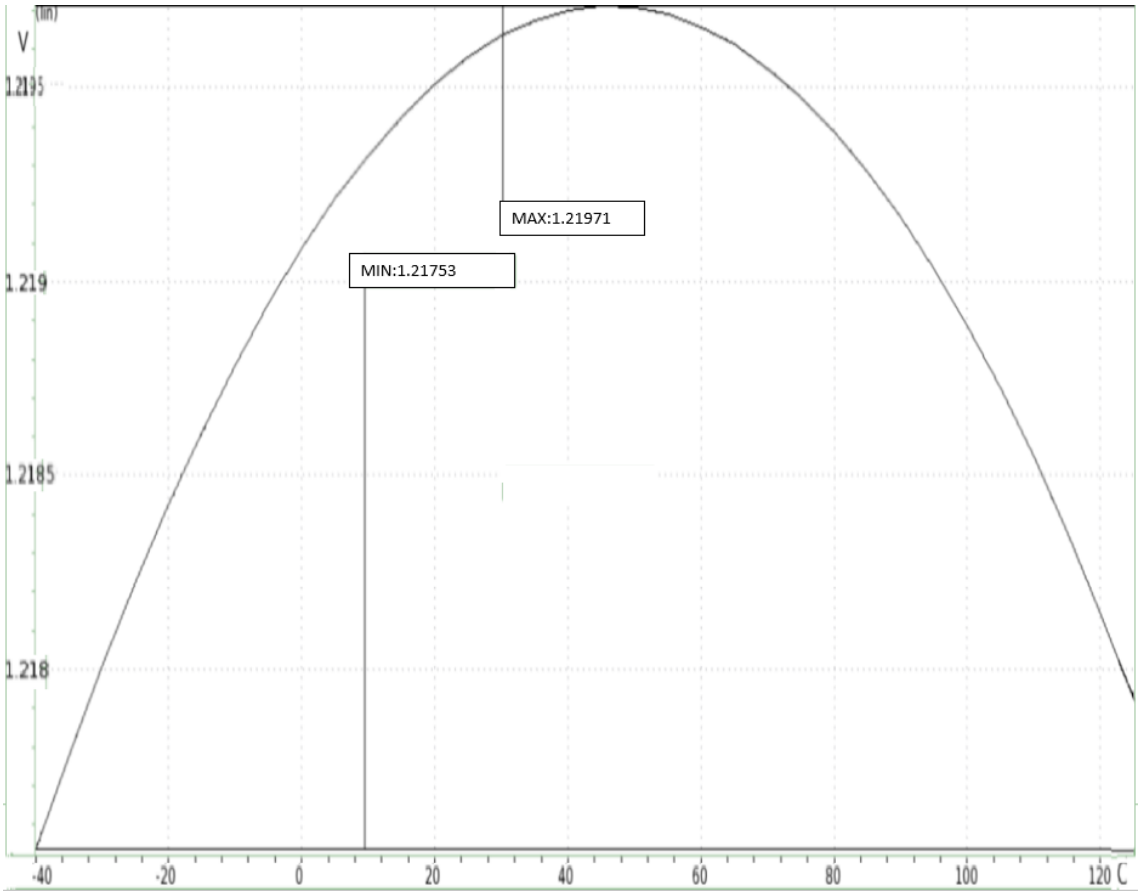

Figure 4.3: Bandgap voltage reference output with temperature variation.

In other words, the voltage reference of the comparator of the over voltage was lowered from 0.6 V (specification value) to 0,575 V and the voltage reference of the under voltage comparator was increased from 0,4 V to 0,425 V. Also, the voltage reference of the maximum peak detector comparator was lowered from 0,7 V to 0,65 V and the voltage reference of minimum peak detector comparator was increased from 0,3 V to 0,35 V. The reason for this is to compensate for the output voltage variation of the bandgap and the operational amplifier offset.

4.2.1.2 The Operational Amplifier Offset in the Bandgap

As stated before, due to the offset (V_{OS}) in the inputs of the operational amplifier, the voltage in these nodes are not equal and thus generates a voltage error in the output of the bandgap. The

Table 4.6: Resistor values.

	R4	R5	R6	R7	R8	R9	R10	R11
Resistor value (Ω)	52 k	60 k	132 k	30 k	64 k	6 k	8.9 k	42 k

following equations demonstrate the impact of the offset at the output

$$V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_2 \tag{4.18}$$

$$V_{REF} = V_{BE1} + (R_2) I_2 \tag{4.19}$$

Then, we have at the output

$$V_{REF} = V_{BE1} + (R_2) \frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3} \tag{4.20}$$

$$V_{REF} = V_{BE1} + (\frac{R_2}{R_3})(V_T ln(n) - VOS) \tag{4.21}$$

The offset of the operational amplifier is amplified in the output by a factor of $(\frac{R_2}{R_3})$ and the offset itself varies with temperature, increasing the temperature coefficient at the output.

In order to minimize this problem, the size of the PMOS differential pair of the operational amplifier and the NMOS current mirror was increased and thus the offset was reduced. Also, the size of the BJT Q_2 was increased (n was increased) in order to reduce the factor $(\frac{R_2}{R_3})$ (see equations 4.9 and 4.10). However, this solution has the disadvantage of increasing the area of BIST system.

4.2.2 Results

In this section, simulation results of the bandgap for several parameters are presented. The behavior of the output with respect to temperature, the stability, and the power-supply rejection ratio of the bandgap will be discussed at typical, best, and worst cases.

4.2.2.1 Temperature

In this section, the behavior of the output of the bandgap concerning temperature will be presented at several corners. To evaluate this behavior, we will use the temperature coefficient (TC) of the output of the bandgap:

$$TC = \frac{\Delta V * 10^6}{\Delta T} \tag{4.22}$$

where the ΔV is the difference between the maximum output voltage of the bandgap and the minimum output voltage when the temperature varies between -40 and 125 °C. The lower the TC, the less the variation of the output voltage will be when the temperature of the system changes. In figure 4.4, we can observe the output voltage of the bandgap in all corners when the temperature changes between -40 °C and 125 °C. In table 4.7, the temperature coefficient for the best, worst and typical cases is presented. The best obtained value is also the typical case.

Considering all PVT conditions, the maximum output voltage is 1,23346 V and the minimum output voltage is 1,20614 V, which gives a peak to peak error of 2,24 %.

Table 4.7: Best, worst and typical cases for TC of the bandgap.

	T.C	Resistor	MOSFET	BJT	Capacitor	Power-Supply
Worst Case	45,9	Fast	Slow_Slow	Slow	-	1,98
Typical/Best Case	13,21	Typical	Typical	Typical	Typical	1,8

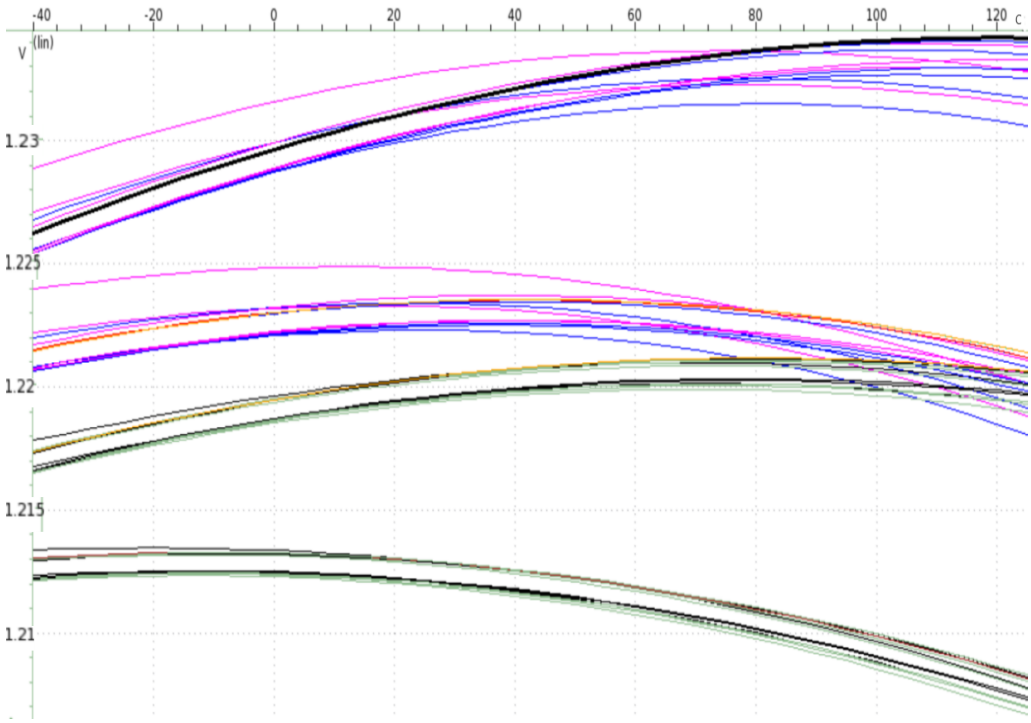

Figure 4.4: Bandgap voltage reference output in PVT.

4.2.2.2 Bandgap Stability Analyzes

In figure 4.5, it is possible to observe the frequency response of the bandgap. The phase margin of the bandgap is 46,9° and the gain margin is 12,3 dB. At DC level the gain is 50,9 dB. In figure 4.6, the PVT analysis of the bandgap stability is shown. The bandgap maintains stability in all corners since the phase margin is always superior to 0 and ranges from 63° to 34 °.

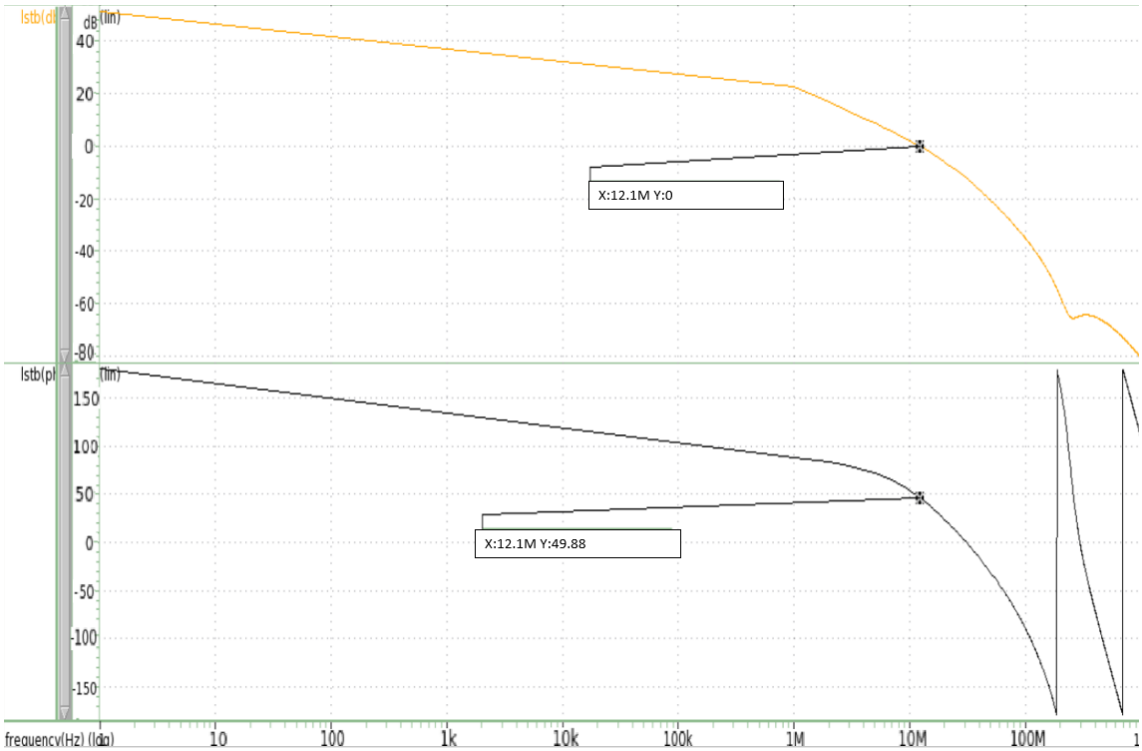

Figure 4.5: Bandgap loop gain frequency response for stability analysis.

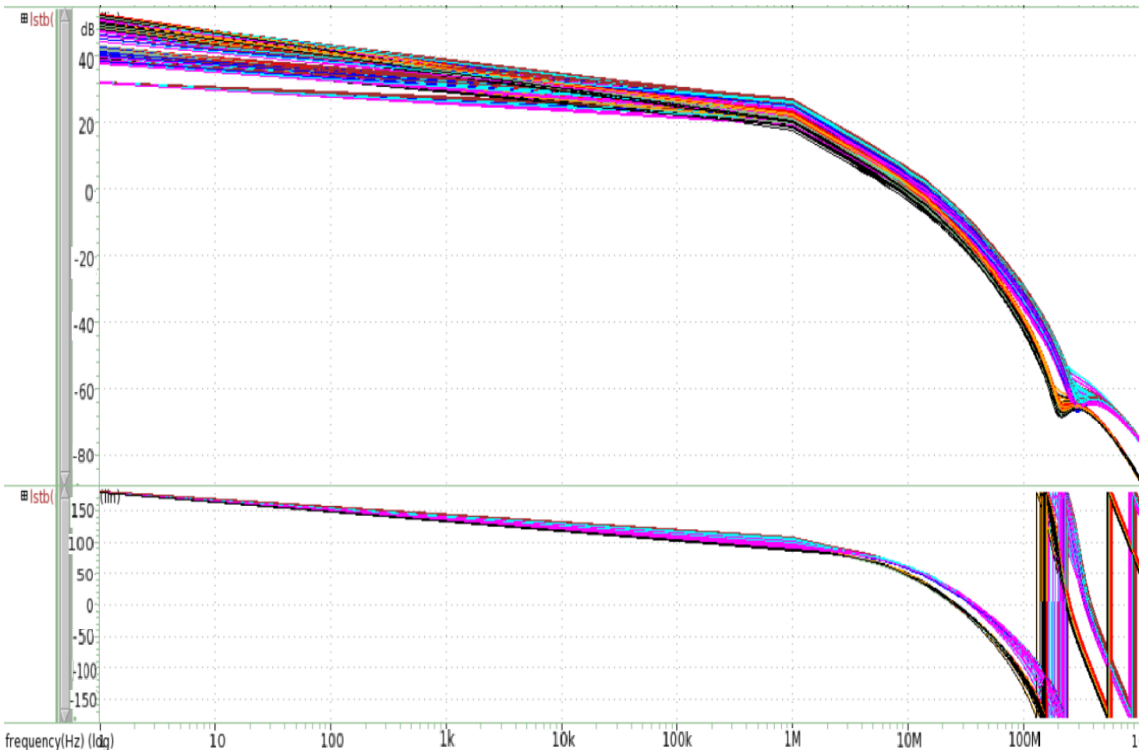

Figure 4.6: Bandgap stability analyze in PVT.

4.2.2.3 Power Supply Rejection Ratio

The power supply, in real-life conditions, is subject to noise and other unwanted signals that cause variation in the power supply voltage. The PSRR measures the capability of a circuit, in this case, the bandgap, of suppressing the presence of these unwanted signals in the output of the circuit.

For the measurement of the PSRR, an AC analysis was performed. The simulation results can be observed in figure 4.7. For a signal with a frequency of 1 kHz in the power supply, the rejection ratio is -61 dB. For a 100 kHz signal the rejection ratio is -52 dB and for 1 GHz, -34 dB. To have a better PSRR, at high frequencies, a capacitor of 1 pF was placed at the output of the bandgap. The lowest rejection ratio, -19.43 dB, is observed at a frequency of 18 MHz for a typical corner.

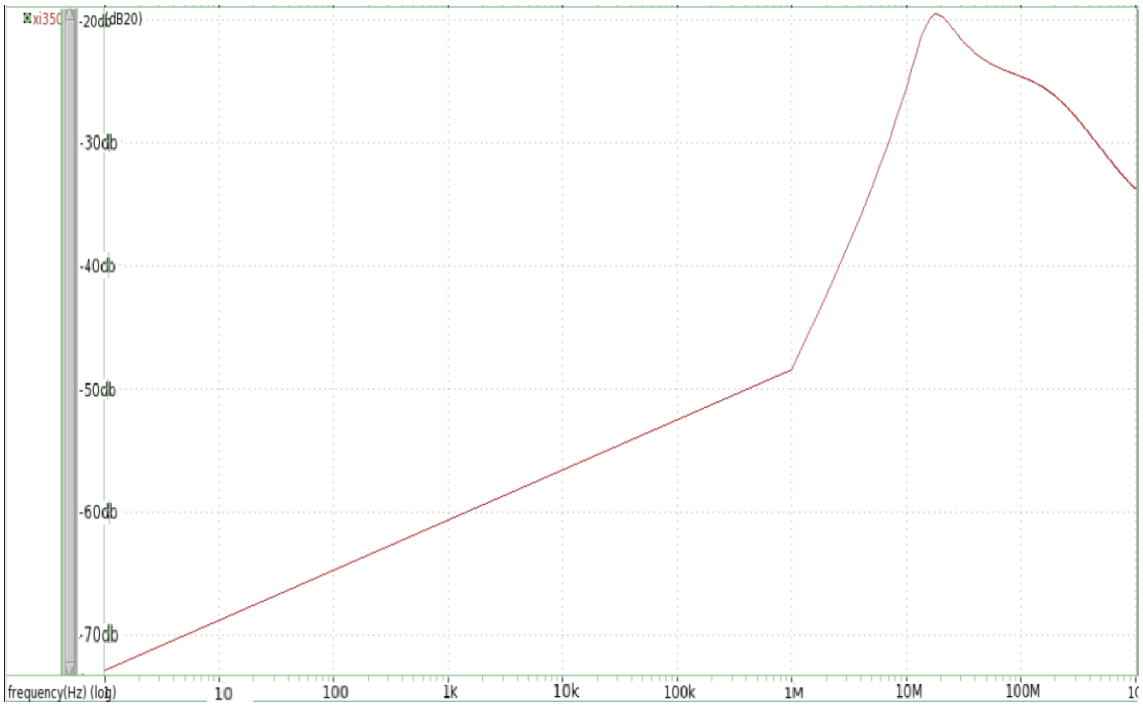

Figure 4.7: Bandgap power supply rejection ratio.

In the following tables, the results for the power supply rejection ratio in PVT are presented for the best, worst and typical cases for the frequency of 1 kHz, 100 kHz, and 1 GHz. In figure 4.8, it is possible to see all results of the PVT. As we can see in the tables, for the frequencies of 1 kHz and 100 kHz, we have the same PVT conditions in the best case for the PSRR. Unlike for what happens at 1 GHz, which has a different PVT condition. The same situation occurs in the worst case.

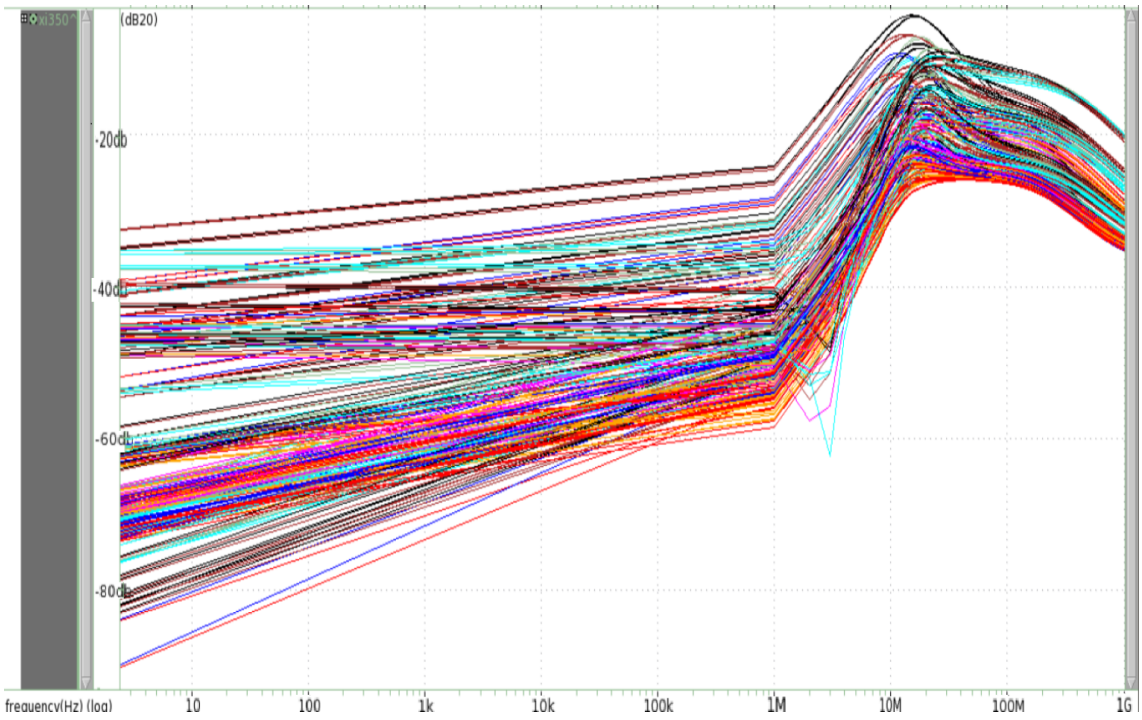

Figure 4.8: Bandgap power supply rejection ratio in PVT.

Table 4.8: Best, worst and typical cases for the PSRR at 1 kHz.

	PSRR(dB)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	-28	Fast	Slow_Slow	Slow	Fast	1.62	-40
Typical Case	-61	Typical	Typical	Typical	Typical	1.8	25
Best Case	-76	Slow	Slow_Slow	Slow	Slow	1.8	-40

Table 4.9: Best, worst and typical cases for the PSRR at 100 kHz.

	PSRR(dB)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	-26	Fast	Slow_Slow	Slow	Fast	1,62	-40
Typical Case	-52	Typical	Typical	Typical	Typical	1,8	25
Best Case	-58	Slow	Slow_Slow	Slow	Slow	1,8	-40

Table 4.10: Best, worst and typical cases for the PSRR at 1 GHz.

	PSRR(dB)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	-19,5	Fast	Slow_Fast	Slow	Fast	1,62	125
Typical Case	-34	Typical	Typical	Typical	Typical	1,8	25
Best Case	-36	Slow	Slow_Slow	Slow	Slow	1,98	-40

4.2.2.4 Summary

In this section, a overview of the results of the bandgap is provided, namely the best, typical and worst case for each parameter of the voltage reference.

Table 4.11: Summary of the bandgap results.

	Typical case	Worst case	Best case
Output voltage (V)	1,2196	1,23346/1,20614	-
TC (ppm/^{o}C)	13,21	45,11	-
PSRR (dB) 1kHz	-61	-28	-73
PSRR (dB) 100kHz	-52	-26	-61

As we can observe in table 4.22, in PVT conditions we have a overall error of 2,24 %. This is lower than the value specified for the system which was 3 %. The bandgap was also subject to 740 Monte Carlo simulations. The results of the output of the bandgap are shown in figure 4.9.

The output of the bandgap has a mean of 1,2196 V and a standard deviation of 6 mV. In Monte Carlo the total error is 3,4 %. Its important to point out that the simulations were performed with the circuit in typical conditions. The variation observed in the output mainly comes from the offset of the operational amplifier which is amplified by the ratio of $\frac{R_2}{R_3} \approx 6,44$.

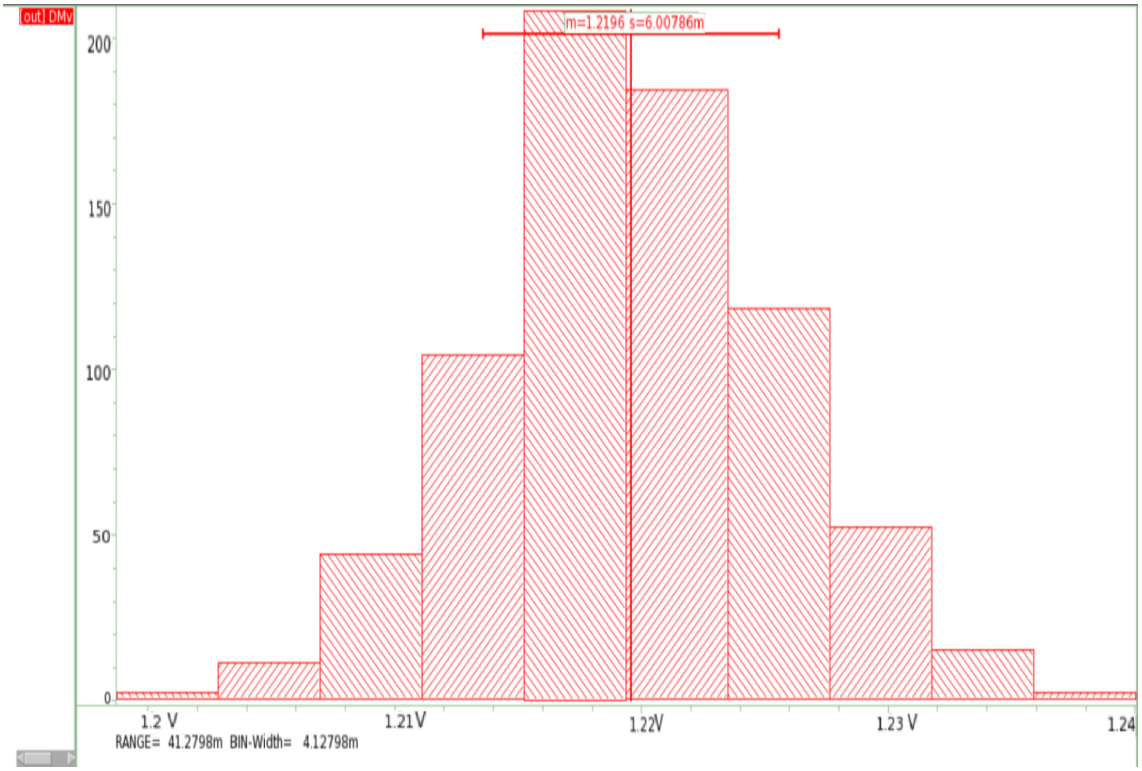

Figure 4.9: Bandgap output in Monte Carlo.

4.3 Over and Under Voltage Comparators

To test the voltage regulator, two comparators were implemented to verify if the output of the regulator is higher than the acceptable value, in this case, 1,2/2 V or is lower than the acceptable value 0,8/2 V.

In the over-voltage comparator, the voltage reference is connected to the inverting input of the comparator and in the under-voltage comparator, the voltage reference is connected to the non-inverting input. The output of the comparator goes high (goes to VDD) in case of an over-voltage or under-voltage detection. Besides the operational amplifier, it was added to the comparators two inverters to provide rail-to-rail output. And at the entrance of the comparators, an RC filter was placed due to the transitory response of the voltage regulator when there is load variation in the system.

4.3.1 Operational Amplifier

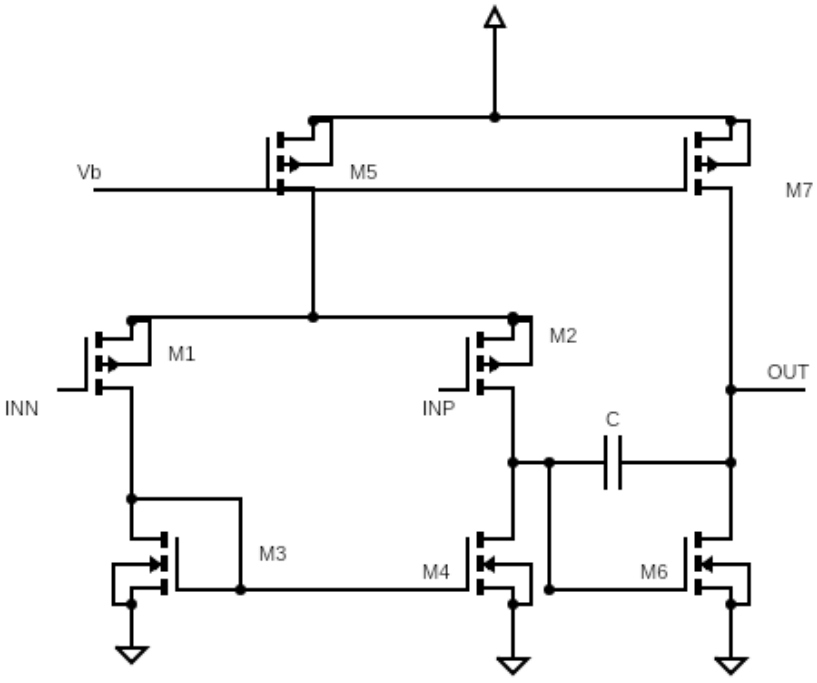

Figure 4.10: Two-stage operational amplifier.

The operational amplifier is a fundamental part of our system. It will be used in the bandgap voltage reference, as a comparator, and in the voltage to current converter in the FVC.

The topology chosen was the two-stage operational amplifier whose schematic can be seen in figure 4.10. The first stage of the amplifier is composed by a PMOS differential input pair, which corresponds to M1 and M2, and an NMOS current-mirror acting as an active load (M3 e M4). The second stage (M6 e M7) corresponds to a common-source with active load (M7). The PMOS

Table 4.12: Dimensions of the transistors for the two-stage operational amplifier.

	W (μm)	L(μm)
M1	75,6	1,08
M2	75,6	1,08
M3	19,6	1,89
M4	19,6	1,89
M5	10,26	1,08
M6	34,6	0,54
M7	34,6	0,54

differential input pair was preferred since they introduce less noise. The capacitor C of the value of 0,49 pF is included to ensure stability when the operational amplifier is placed in a feedback configuration. It was also introduced transmission gate switches in the operational amplifier in order to turn on or off the amplifier when needed.

When choosing the sizes for the transistors, the transistors of the differential pair and of the current mirror were made bigger in order to minimize the operational amplifier offset. And that the relation between the current is $I_7 \approx 7I_5$ and the $I_2 \approx 0,5I_5$ In table 4.12, the sizes for the transistors are presented.

4.3.1.1 The Bias Circuit

The bias circuit of the operational amplifier can be seen in figure 4.11 and the size of transistors and the resistor are in table 4.13. A characteristic of this biasing circuits is that reduces the impact of the variation of supply voltage in the bias current, thus the name of this topology - supply-independent biasing circuit.

When design this circuit its was considered that the current flowing through the two branches were the same, $I_1 = I_2$, which leads to

$$(\frac{W}{L})_{M1} = (\frac{W}{L})_{M2} \tag{4.23}$$

Also, assuming that the NMOS threshold voltage are the same, then $V_{gs3} = V_{gs4} + I_2R_s$. From this, if we consider that the $V_{gs3} = 0.5V_{gs4}$ we can state that

$$(\frac{W}{L})_{M3} = 0,5(\frac{W}{L})_{M4} \tag{4.24}$$

$$R_s = \frac{V_{gs4} - V_{gs3}}{I_2} \tag{4.25}$$

where V_{gs} is the gate-source voltage, W is the width of the transistor and L is the length of the transistor.

A particularity of this circuit is that it has two operating points. When the supply is turned on, and the transistors are all carrying zero current, they may stay turned off, since the circuit can have a zero current in both branches. So, it needs a start-up circuit to reach its correct operating point.

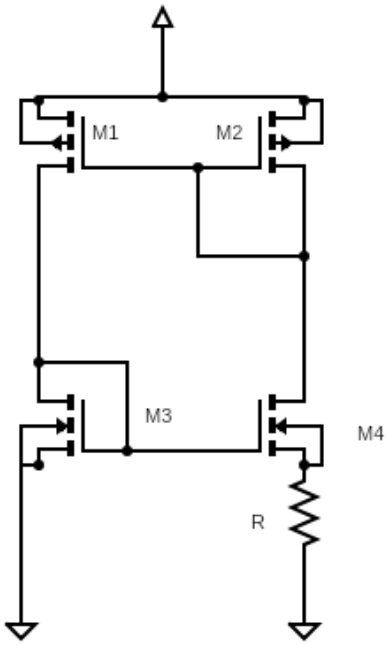

Figure 4.11: Bias circuit.

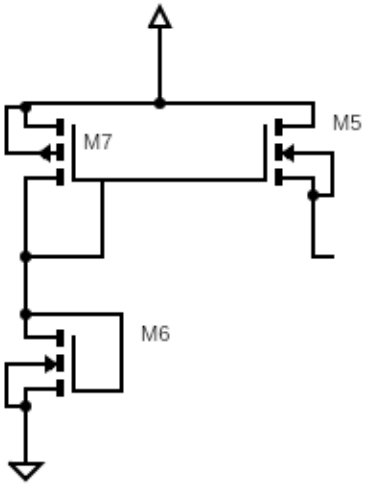

Figure 4.12: Startup circuit.

The start-up circuit is shown in figure 4.12. It has the following behavior, depending on the value of the currents I_1 and I_2:

- $I_1 = I_2 = 0$
  - The gate-source of M4 and the source of M5 is zero, while the voltage at the gate of M5 is set by M6 and M7. Therefore, M5 is injecting current into the branch I_1 and, consequently, the current I_2 is also raising. Moving the circuit from the wrong operating point.
- $I_1 \neq I_2 \neq 0$
  - With the increasing of the currents in the circuit, the gate-source voltage of M4 rises, consequently, the voltage at the source of the transistor M5 goes up and the transistor starts to turn off since the voltage at the gate of M5 is held constant. When the circuit arrives at the desired operating point, where $I_1 = I_2$, the star-up circuit is disconnected from the bias circuit.

4.3.1.2 Inverters and RC filter

To design the inverters, it was first assumed that the PMOS and NMOS have the same length which is 0,15 μm, and that the NMOS is 0,54 μm. After, a DC analysis was performed to find the size of the PMOS. In the analysis, the number of fingers of the PMOS was varied between 1 and 10,

Table 4.13: Dimensions of the transistors for the bias circuit and start-up.

	W (μm)	L(μm)
M1	5,94	1,08
M2	5,94	1,08
M3	1,08	1,08
M4	2,16	1,08
M5	0,27	0,27
M6	1,08	1,08
M7	5,94	1,08

and it was checked in which wave the output and input were equal to half of the supply voltage. The width of the PMOS obtained was 1,62 μm.

The low-pass RC filter has a cutoff frequency of 501 kHz and the value chose for the resistor was 721,5 kΩ and the value for the capacitor was 0,44 pF.

4.3.2 Results

In this section, the simulation results for the operational amplifier, and the comparator (operational amplifier plus the inverters) are shown. To evaluate the performance of the operational amplifier several analyzes were performed in typical conditions and the PVT conditions specified.

4.3.2.1 AC Analyzes

The frequency response of the operational amplifier was evaluated in two situations: when both inputs are 0,65 V or 0,35 V. Since these voltages are the maximum and minimum voltage the comparators of the system will have as a voltage reference. At the output of the operational amplifier, a capacitor of 1 pF was added to act as a load.

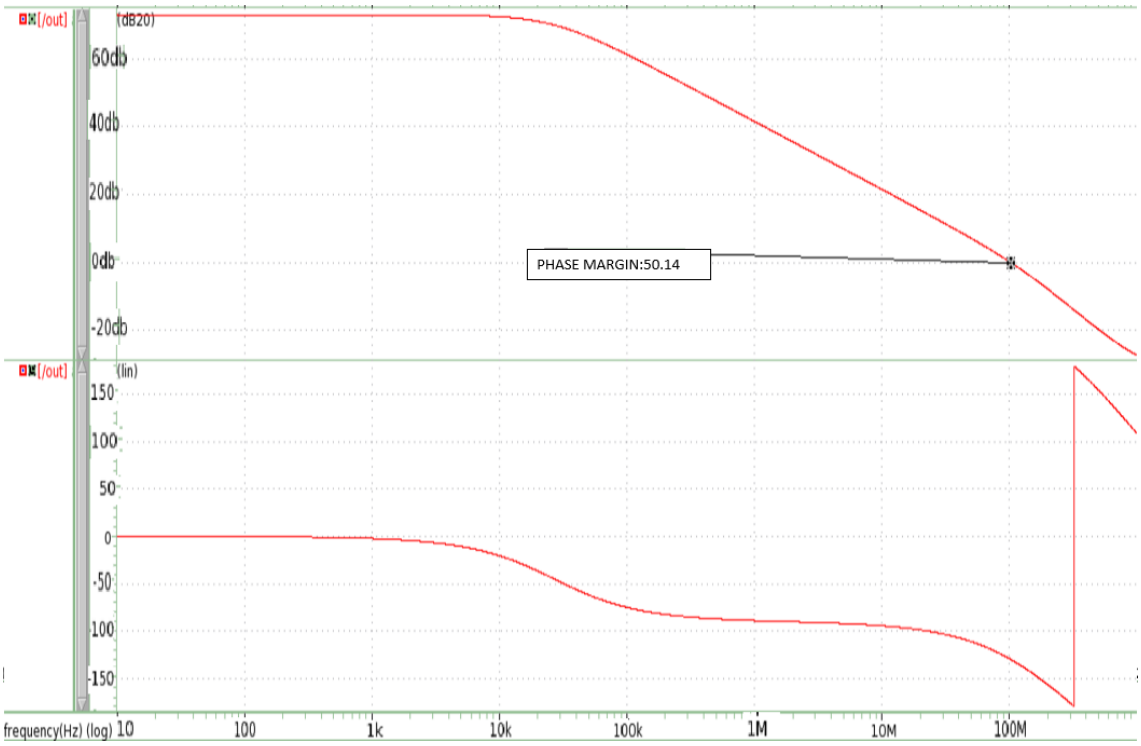

Figure 4.13: Gain and phase of the operational amplifier - 0,65V.

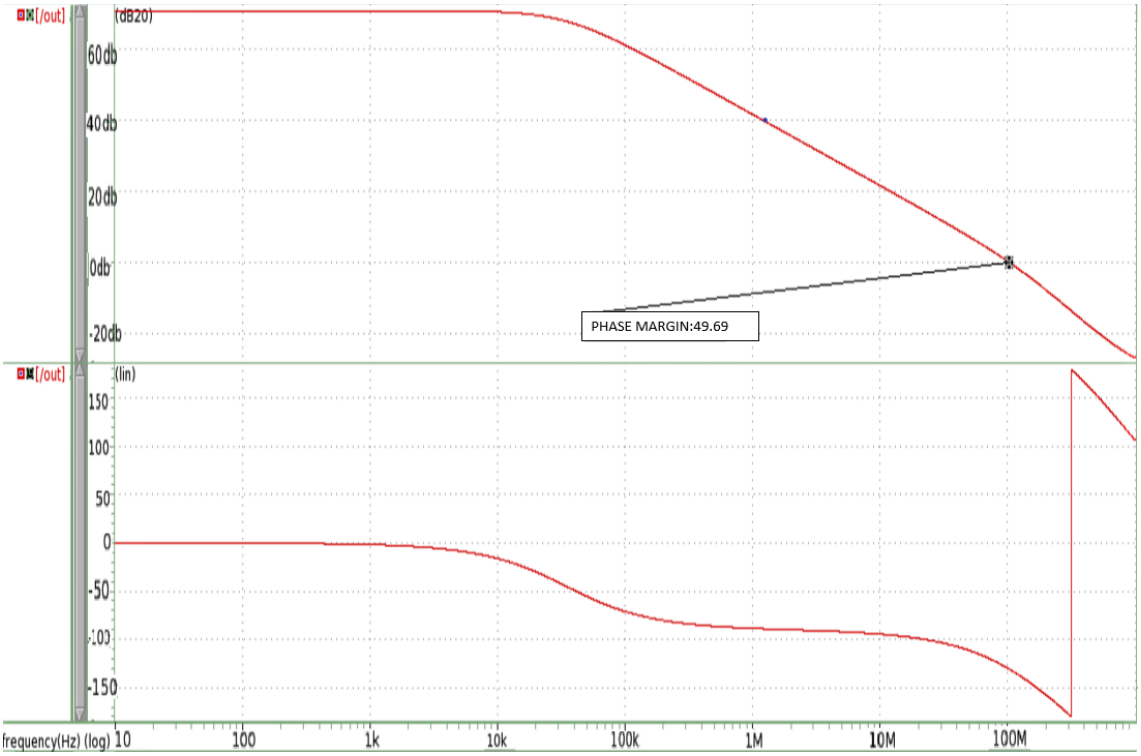

Figure 4.14: Gain and phase of the operational amplifier - 0,35V.

In the typical case, when the both inputs are 0.65 V, we have a DC gain of 73 dB which is higher than the desired 60 dB. However, when simulating in PVT conditions, some of the corners went bellow 60 dB. But, this did not have a visible impact in the functionality of the BIST, so it was consider acceptable. The phase margin value, in a typical case, was 50,9°. In PVT conditions, the phase margin ranges from 43,4° to 56,83 °, maintaining always stability. The results for the best, typical, and worst cases of can be seen in tables 4.14, 4.15, 4.16, and 4.17.

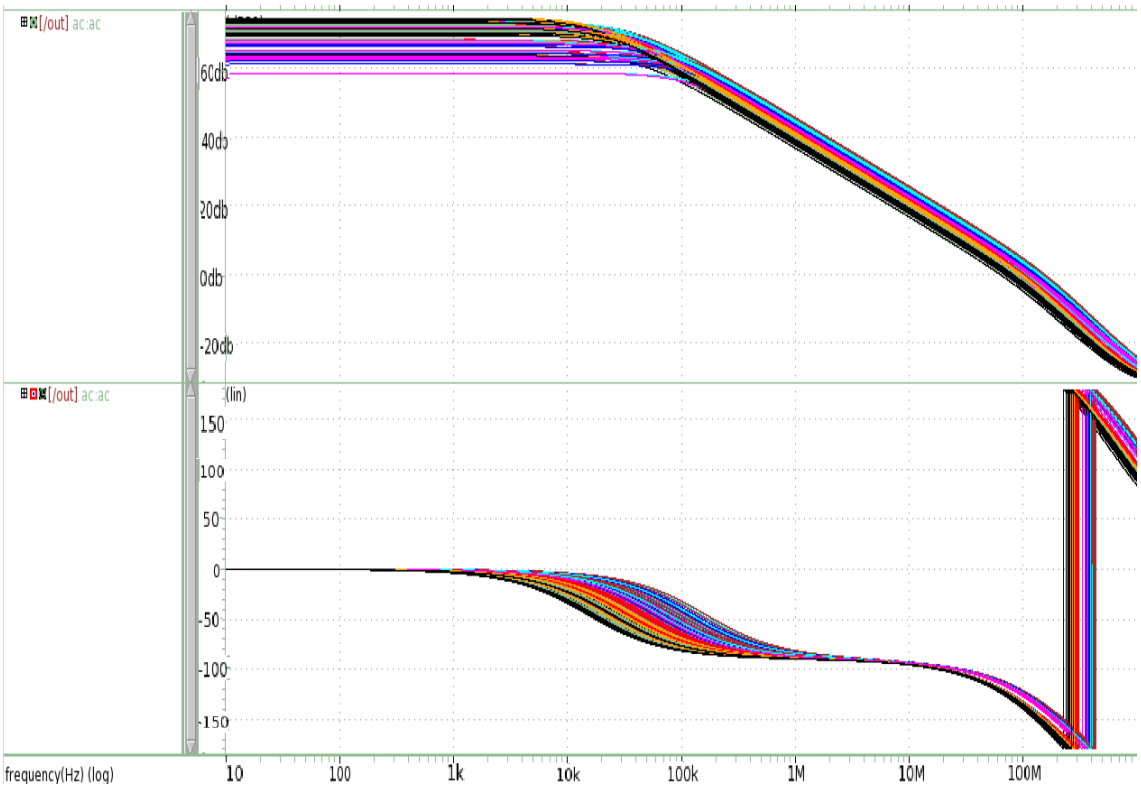

Figure 4.15: Gain and phase of the operational amplifier in PVT - 0,65 V.

Table 4.14: Best, worst and typical cases for the DC gain for 0,65 V.

	Gain (dB)	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	58,5	Fast	Slow_Slow	Slow	1,62	125
Typical Case	73	Typical	Typical	Typical	1,8	25
Best Case	74,2	Slow	Slow_Slow	Slow	1,98	25

Table 4.15: Best, worst and typical cases for the DC gain for 0,35 V.

	Gain (dB)	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	34,9	Fast	Slow_Fast	Slow	1,98	125
Typical Case	71	Typical	Typical	Typical	1,8	25
Best Case	73,8	Slow	Fast_Slow	Slow	1,98	-40

Table 4.16: Best, worst and typical cases for the phase margin for 0,65 V.

	Phase Margin	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	43,4 °	Fast	Slow_Fast	Fast	1,98	125
Typical Case	50,5 °	Typical	Typical	Typical	1,8	25
Best Case	56,83°	Slow	Slow_Slow	Slow	1,62	-40

Table 4.17: Best, worst and typical cases the phase margin for 0,35 V.

	Phase Margin	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	45,4 °	Fast	Fast_Fast	Fast	1,98	25
Typical Case	49,69 °	Typical	Typical	Typical	1,8	25
Best Case	65,1 °	Fast	Slow_Fast	Fast	1,98	125

When both inputs are 0,35 V, the DC gain of the operational amplifier is 71 dB which is higher than the desired 60 dB. But, when simulating in PVT conditions, some of the corners went bellow 40 dB. This was not considered to be a problem since it did not have a visible impact on the functionality of the BIST. The phase margin value, in a typical case, was 49,69 °. In PVT conditions, the phase margin ranges from 45° to 65,1 °, maintaining always stability.

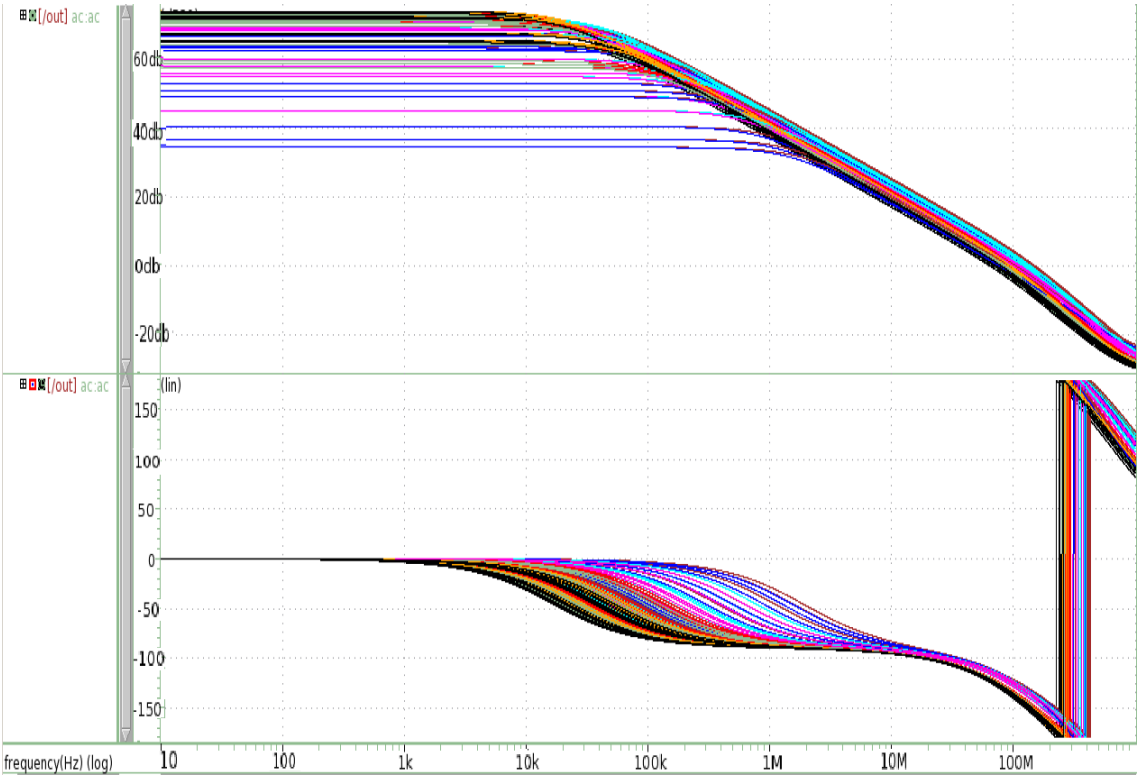

Figure 4.16: Gain and phase of the operational amplifier in PVT - 0,35 V.

4.3.2.2 Power Supply Rejection Ratio

The power-supply rejection ratio of the operational amplifier was, also, simulated for the two different inputs. Table 4.18 and 4.19 displays the results for best, typical, and worst cases of the PSRR of the operational amplifier at the frequency of 1 kHz. It is possible to see that when the input its lower the operational amplifier has a better PSRR.

In figure 4.17 and 4.18, the PSRR of the operational amplifier for the range of frequencies between 10 Hz and 1 GHz is presented. In figure 4.19, the PSRR, in PVT conditions, is also displayed for the same range of frequencies.

The PSRR, in some PVT conditions, for the situation was the inputs are 0,65 V is superior to 0 db, which means that the variation in the power supply is being amplified to the output. This could lead to false detections in the test of the OUV or the peak detectors. So, a future improvement is to increase the PSRR of the operational amplifier.

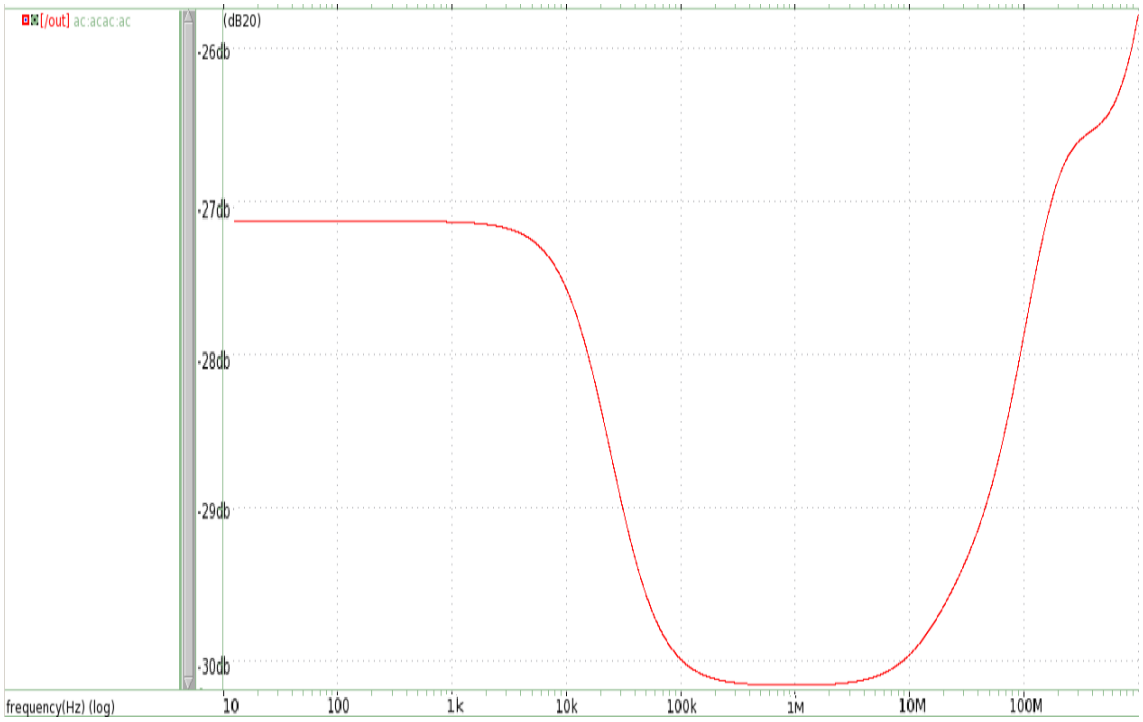

Figure 4.17: PSRR of the operational amplifier - 0,65 V.

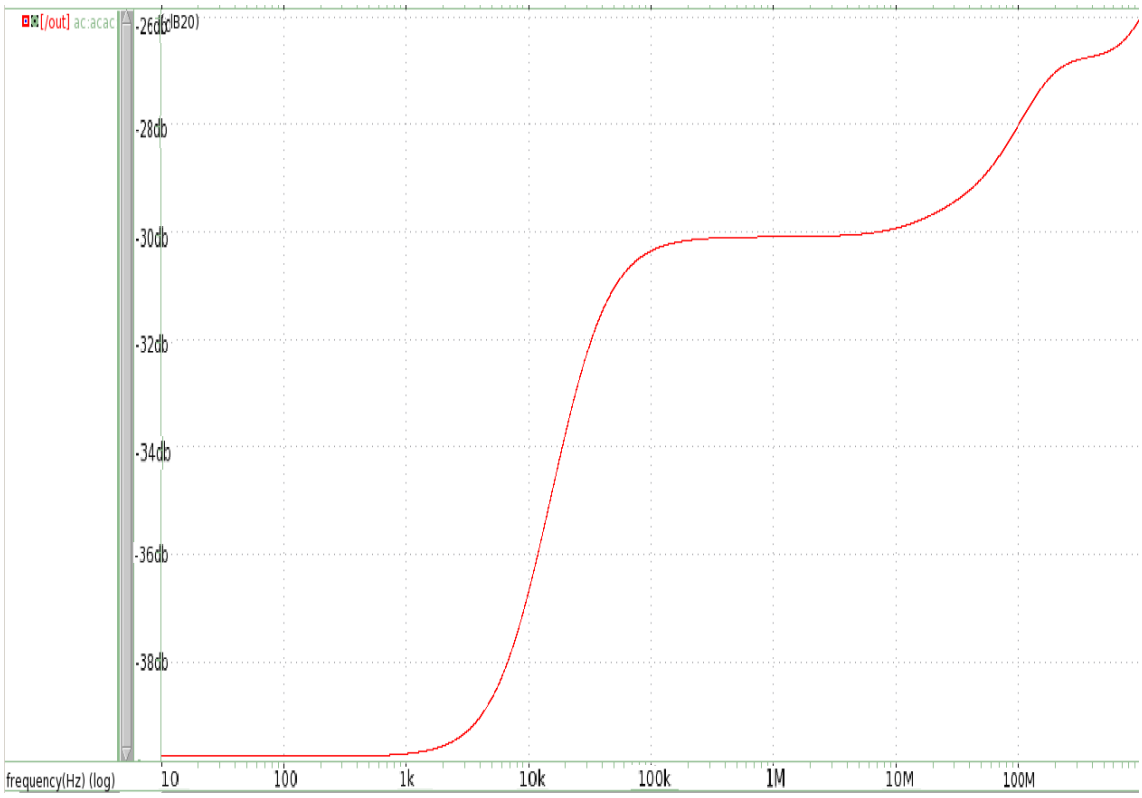

Figure 4.18: PSRR of the operational amplifier - 0,35 V.

Table 4.18: Best, worst and typical cases for the PSRR for 0,35V at 1 kHz.

	PSRR(dB)	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	-4,15	Slow	Slow_Slow	Slow	1,62	-40
Typical Case	-39,7	Typical	Typical	Typical	1,8	25
Best Case	-65,8	Fast	Fast_Fast	-	1,62	125

Table 4.19: Best, worst and typical cases for the PSRR for 0,65V at 1 kHz.

	PSRR(dB)	Resistor	MOSFET	Capacitor	Supply	Temperature
Worst Case	9,5	Slow	Fast_Slow	-	1,62	125
Typical Case	-27	Typical	Typical	Typical	1,8	25
Best Case	-49,1	Fast	Fast_Fast	-	1,98	-40

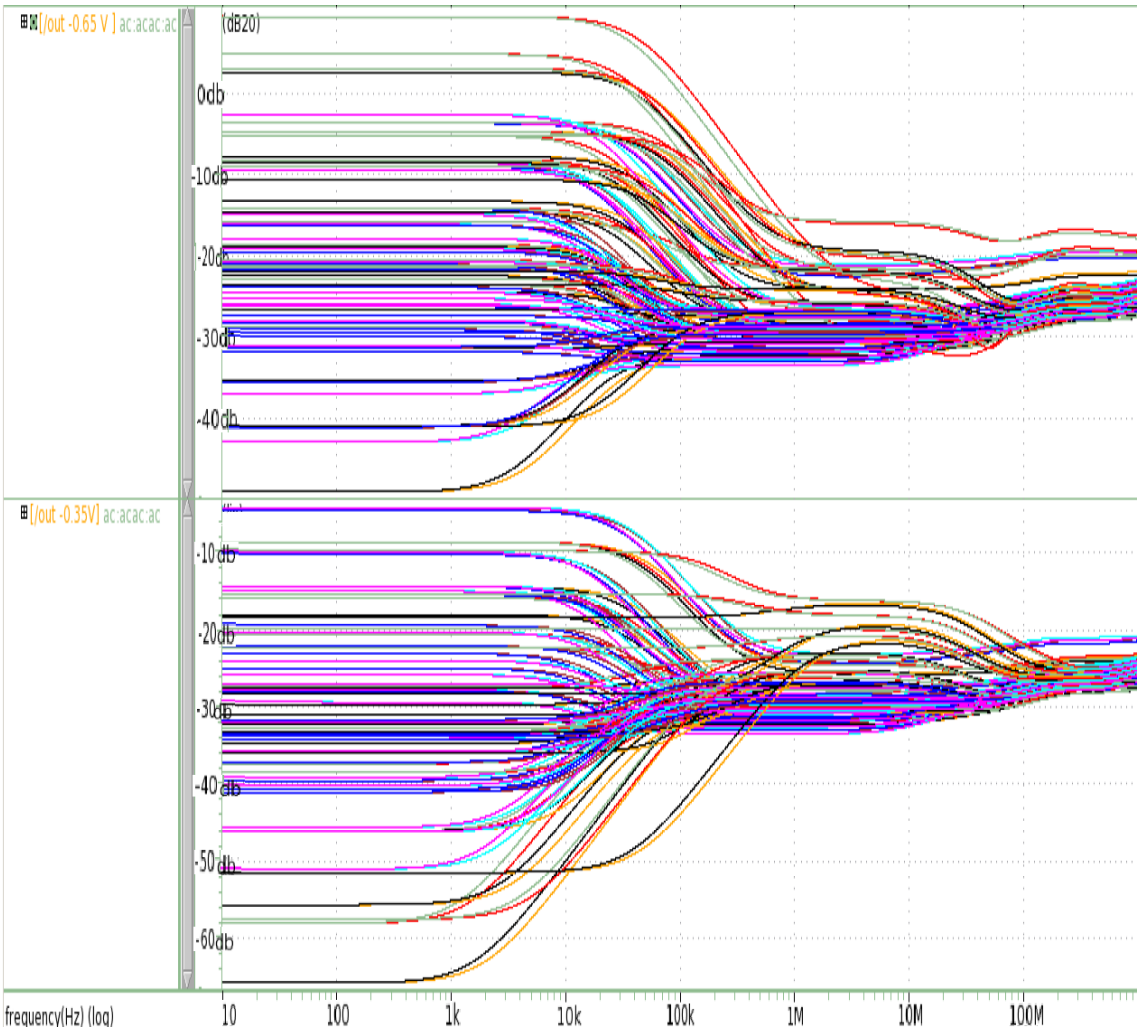

Figure 4.19: PSRR of the operational amplifier in PVT.

4.3.2.3 Offset

The offset of the amplifier is caused by the operational amplifier non-infinite gain and the mismatches between the transistors. To obtained the offset of the two-stage amplifier, it was made 740 Monte Carlo simulations. The results of the simulation can be seen in figure 4.20. The offset of the operational amplifier is $\pm 2,24$ mV which is lower than the specified value of $\pm 2,5$ mV.

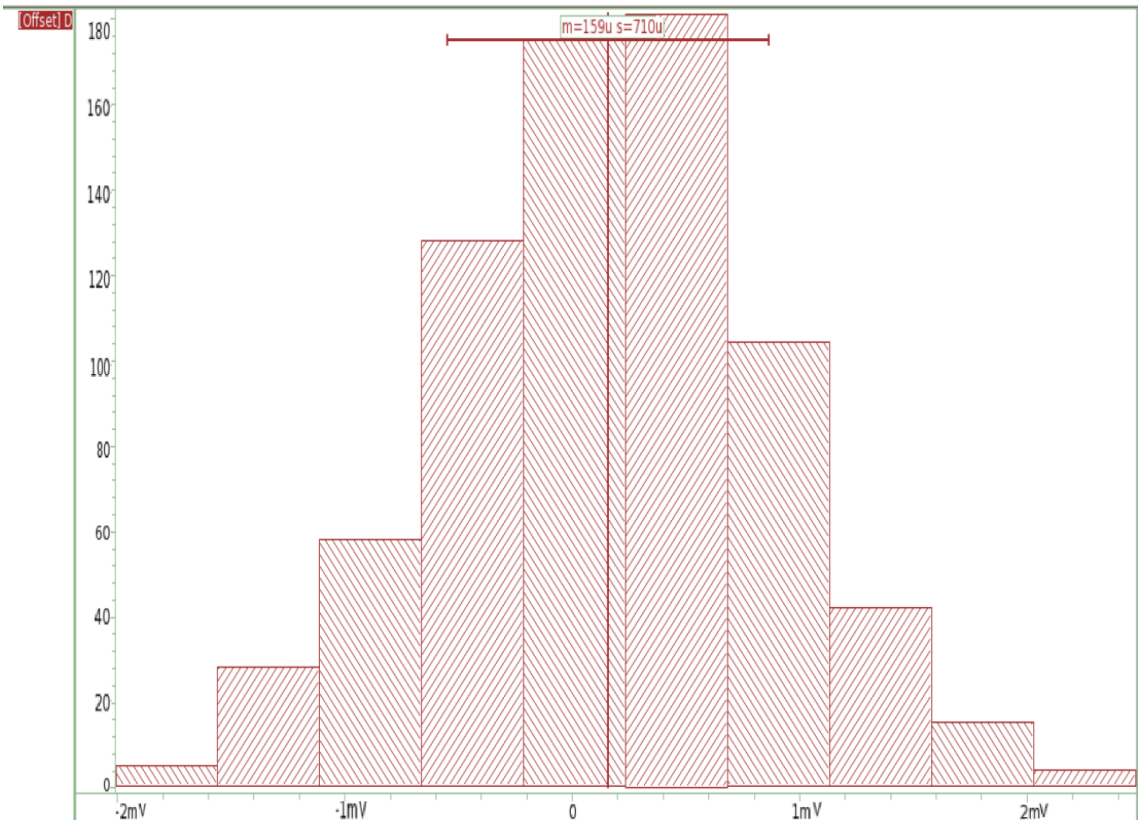

Figure 4.20: Operational amplifier offset.

4.3.2.4 Propagation Delay

Instead of measuring the delay of the operational amplifier, it was considered to be more appropriate to measure the propagation delay of all components - operational amplifier plus inverters and RC filter. Most of the delay will come from the low-pass RC filter and the delay caused by the comparator is negligible, in the situation presented in the results due to the "fast" transition between the nominal voltage of the regulator to 1,2 V or to 0,8 V. If the transition is slower, the delay will decrease.

So, in figure 4.21 it can be seen that the delay for over-voltage detection, in the situation when the output of the voltage regulator is 1,2 V, is $1,6\ \mu$s. When the output of the voltage regulator goes to 0,8 V, the delay obtained was $1,3\ \mu$s, as shown in figure 4.24.

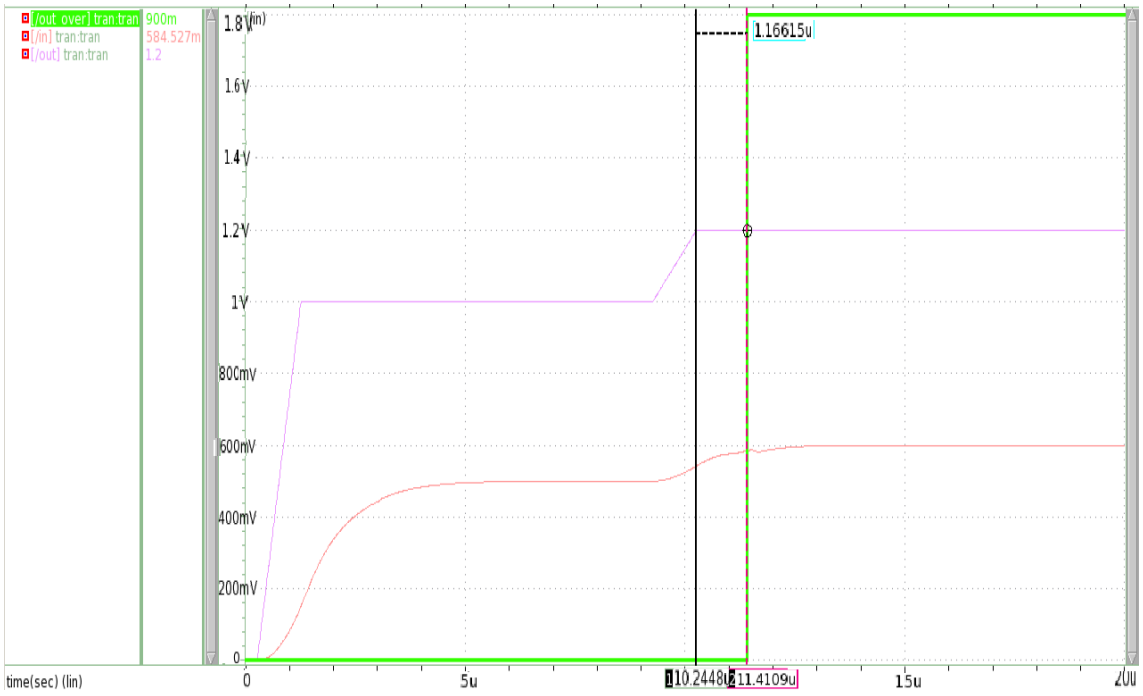

Figure 4.21: Propagation delay for over-voltage detection.

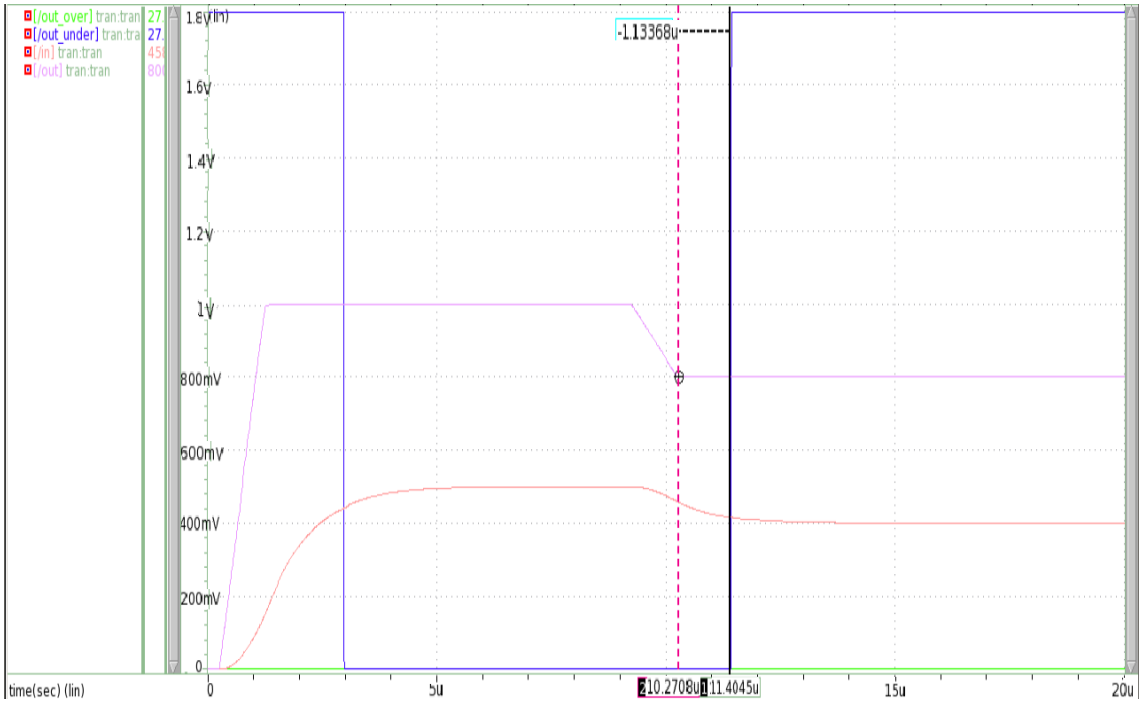

Figure 4.22: Propagation delay for under-voltage detection.

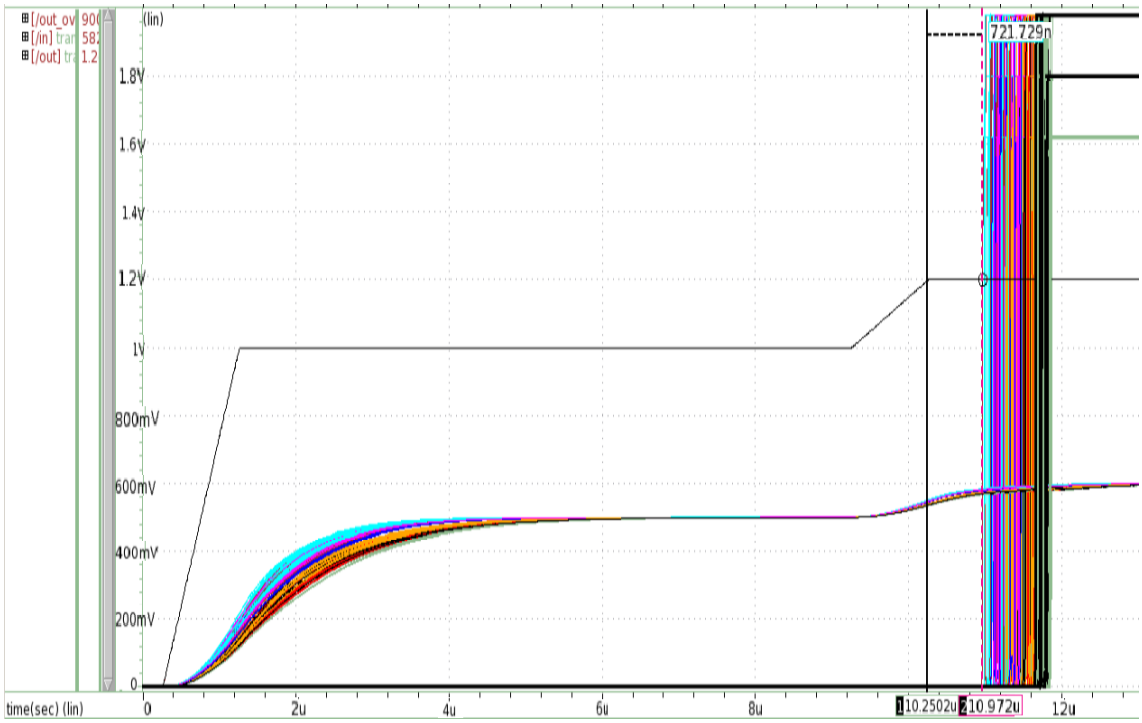

Figure 4.23: Propagation delay for over voltage detection in PVT.

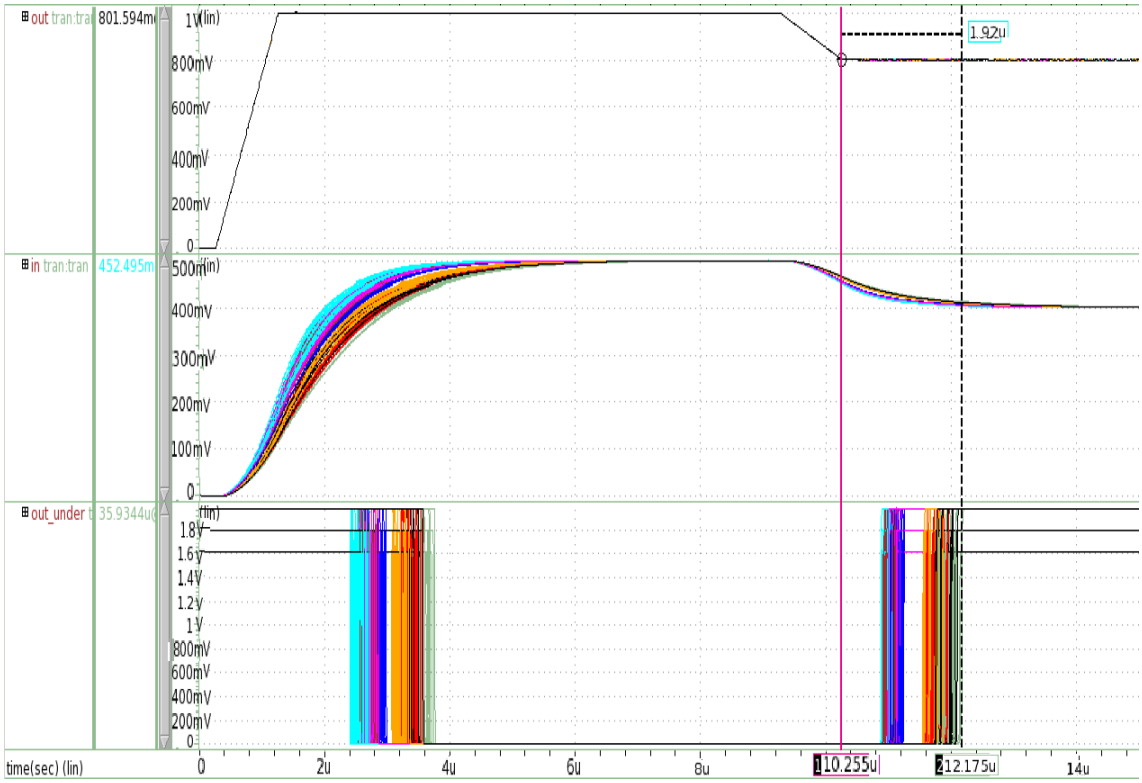

Figure 4.24: Propagation delay for under voltage detection in PVT.

In tables 4.20 and 4.21 its possible to observe the worst, typical and best case of the propagation delay for the over voltage detector and under voltage detector.

Table 4.20: Best, worst and typical cases for the delay for the Over Voltage Detector.

	Delay (μs)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	1,621	Slow	Fast_Fast	Slow	Slow	1,98	25
Typical Case	1,6	Typical	Typical	Typical	Typical	25	1,8
Best Case	0,7217	Fast	Slow_ Fast	Fast	Fast	1,62	125

Table 4.21: Best, worst and typical cases for the delay for the under voltage detector.

	Delay(μs)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	1,92	Slow	Fast_Fast	Fast	Slow	1,98	125
Typical Case	1,3	Typical	Typical	Typical	Typical	25	1,8
Best Case	0,64224	Fast	Slow_Slow	Slow	Fast	1,8	125

4.3.2.5 Summary

In this section, a overview of the results of the comparator is provided, namely the best, typical and worst case for each parameter analysed.

Table 4.22: Summary of the comparators results.

	Typical case	Worst case	Best case
Gain (dB) - 0,65 V	73	58,5	74.2
Phase - 0,65 V	50,5 °	43,4 °	56,83 °
PSRR(dB) 1kHz - 0,65 V	-27	9,5	-49.1
Gain (dB) - 0,35 V	71	34,9	73,8
Phase - 0,35 V	49,69 °	45,4 °	65,1 °
PSRR(dB) 1kHz - 0,35 V	-39,7	-4.15	-65,8
Propagation delay UV (μs)	1,3	1,92	0,64224
Propagation delay OV (μs)	1,6	1,621	0,7217
Offset (mV)	$\pm$2,24	-	-

4.4 Peak Detectors

For the detection of ripple in the voltage regulator, two peak detectors were designed and implemented. The positive peak detector circuit [41] can be observed in figure 4.27 and the negative peak detector 4.26.

In the circuit for the detection of maximum ripple in the voltage regulator, when the voltage at the positive input of the operational amplifier is higher than the voltage in negative input, the output of the operational amplifier goes high, the M1 turns on and the capacitor is charged to half

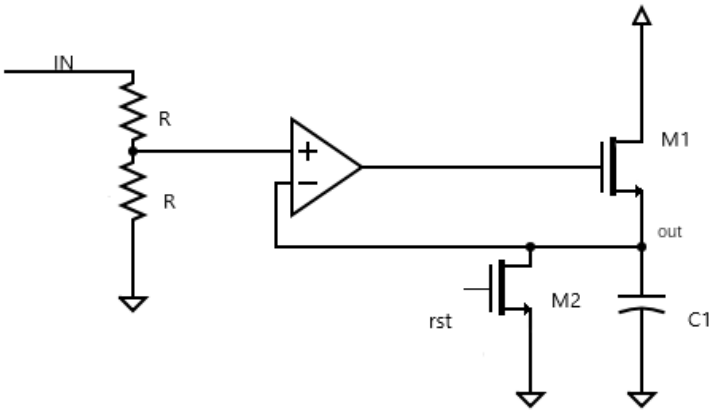

Figure 4.25: Positive peak detector.

of the peak voltage. Then this voltage is compared to the maximum allowed voltage for ripple. A testbench was made in Verilog-A that detects if the output of the comparator goes high and, if yes, then generates a Fail signal and then sends a signal to reset the circuit by turning on the NMOS transistor and discharge the capacitor C1 (1,3 pF). During the reset the operational amplifier is disabled. Otherwise, there will be detection replicas. However, in some PVT conditions, there are still replicas.

The operation of the circuit for the detection of minimum ripple in the regulator is presented in the following. When the voltage at the negative input of the operational amplifier is lower than the voltage in the positive input, the output of the operational amplifier goes high. And the NMOS turns on and the capacitor C2 (2,6 pF) is discharged to half of the peak voltage. After this voltage is compared to the minimum allowed voltage for ripple. A testbench was made in Verilog-A that detects if the output of the comparator goes high and, if yes, then generates a Fail signal and a reset signal to charge the capacitor.

In the minimum peak detector, an M5 transistor working in the subthreshold region provides a small current of 1 nA to charge the capacitor until both of the inputs of the operational amplifier are at the same voltage.

A transistor working in the subthreshold region has $V_{gs} < V_t$, so for M5 to be in this region, it was used the circuit in the figure 4.27. Its has four diode-connected NMOS transistor and a diode-connected PMOS. This way it is possible to have at node v a voltage of 1,46 V with gives M5 a V_{sg} of 0,34 V, which is less than the threshold voltage of the PMOS, 0,5 V.

4.4.1 Results

The peak detectors implemented are capable of detecting peaks of 1,4 V and 0,6 V as specified. The detector is capable of detecting peaks with a width of 50 ns and higher, in all PVT conditions.

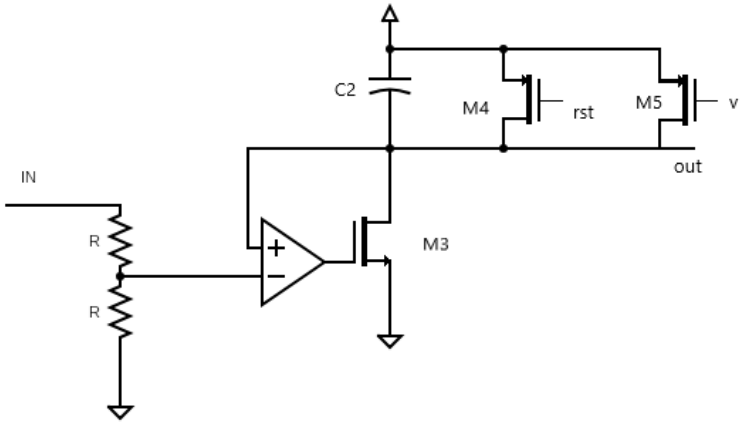

Figure 4.26: Negative peak detector.

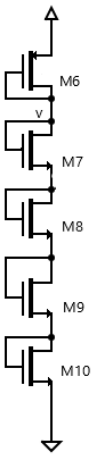

Figure 4.27: Peak detector bias circuit.

The results of these simulations are in appendix B. However, these circuits will not be able to catch peaks in certain situations:

- When the positive peak detector circuit is doing a reset or during sometime after, the negative peak detector may not catch peaks. The opposite may also happen, the positive detector can not catch peaks while the other circuit is in reset.

- Sometimes, in some PVT conditions, the circuits have several resets until the voltage in the capacitor is lower/higher than the voltage reference at the comparator. The digital part has to be able to ignore these situations.

Table 4.23: Dimensions of the transistors for the peak detectors and bias circuit.

	W(μm)	L(μm)
M1	0,54	0,15
M2	0,27	0,27
M3	0,27	0,54
M4	0,27	0,27
M5	0,27	1,08
M6	0,54	0,27
M7	0,27	0,54
M8	0,27	0,54
M9	0,27	0,54
M10	0,27	0,54

4.4.1.1 Propagation Delay

The propagation delay was considered has the time between when the peak reaches its maximum value and the output of the comparator goes high. In typical conditions, for a 50 ns positive peak, the output of the comparator of the detector takes 28,86 ns to go high. In the case of a 100 ns positive peak, the detection time is 40,8 ns.For a 50 ns negative peak, in typical conditions, the detection time is 35,56 ns and for a 100 ns negative peak is 20,39 ns. In the following tables, the results in the PVT conditions are presented.

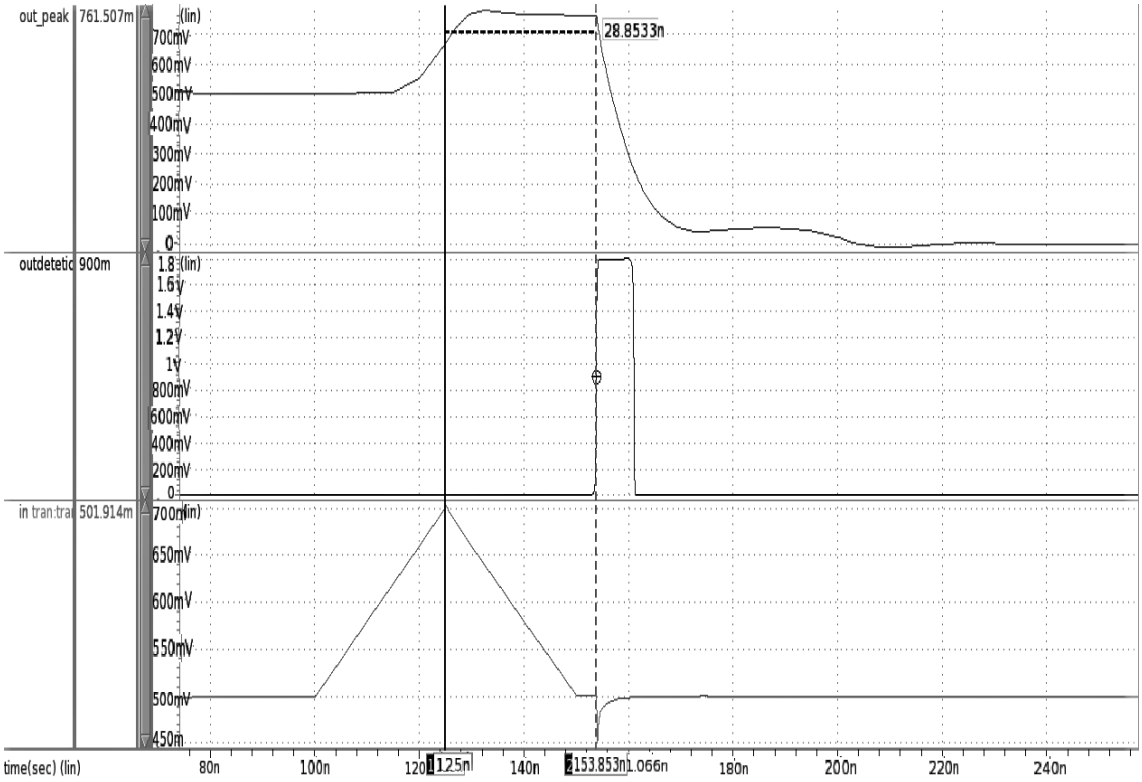

Figure 4.28: Propagation delay of the positive peak circuit for a 50 ns peak.

Table 4.24: Best, worst and typical cases for the delay for the positive detector for a 50 ns peak.

	D (ns)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	100,85	Slow	Slow_Slow	Slow	Slow	1,62	-40
Typical Case	28,86	Typical	Typical	Typical	Typical	1,8	25
Best Case	12,45	Fast	Slow_Fast	Fast	Fast	1,98	125

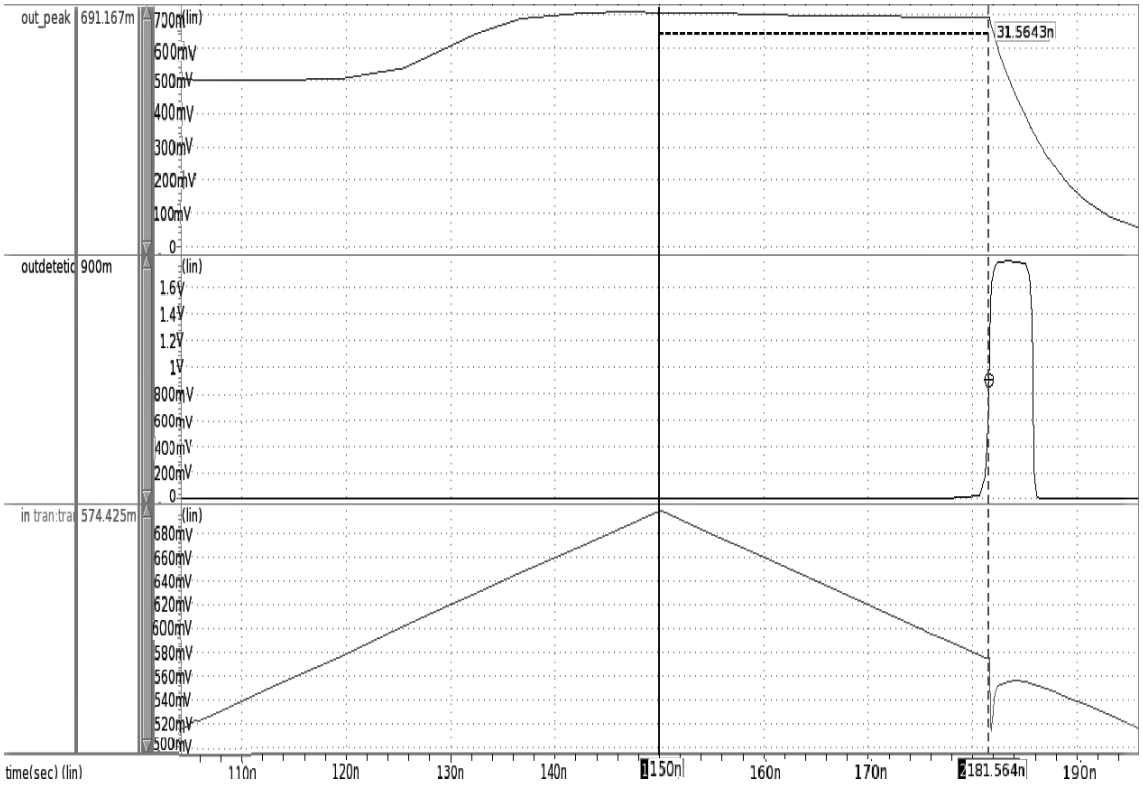

Figure 4.29: Propagation Delay of the positive peak circuit for a 100 ns peak.

Table 4.25: Best, worst and typical Cases for the delay for the positive detector for a 100 ns peak.

	D (ns)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	81,66	Fast	Fast_Slow	Fast	Fast	1,8	25
Typical Case	40,8	Typical	Typical	Typical	Typical	1,8	25
Best Case	15,65	Fast	Slow_Fast	Fast	Slow	1,62	125

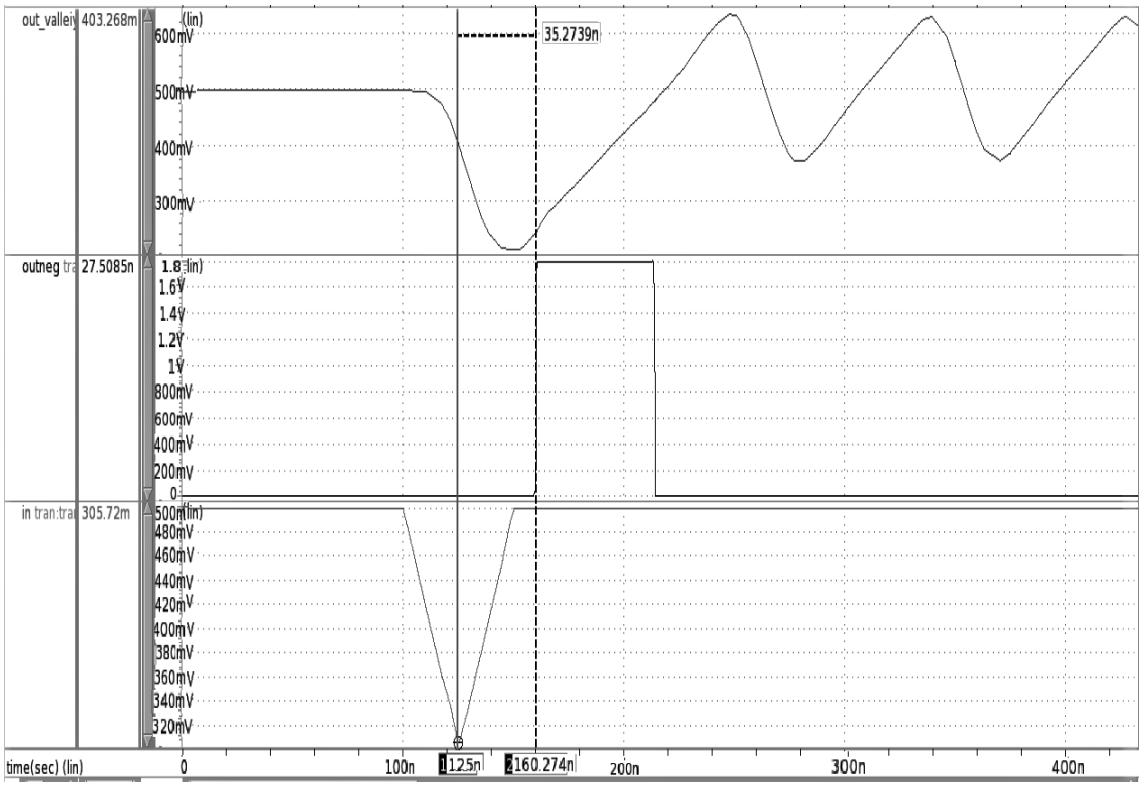

Figure 4.30: Propagation delay of the negative peak circuit for a 50 ns peak.

Table 4.26: Best, worst and typical cases for the delay for the negative detector for a 50 ns peak.

	D (ns)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	103,45	Slow	Slow_Slow	Fast	Slow	1,62	-40
Typical Case	35,56	Typical	Typical	Typical	Typical	1,8	25
Best Case	20,2	Fast	Fast_Fast	Fast	Fast	1,8	25

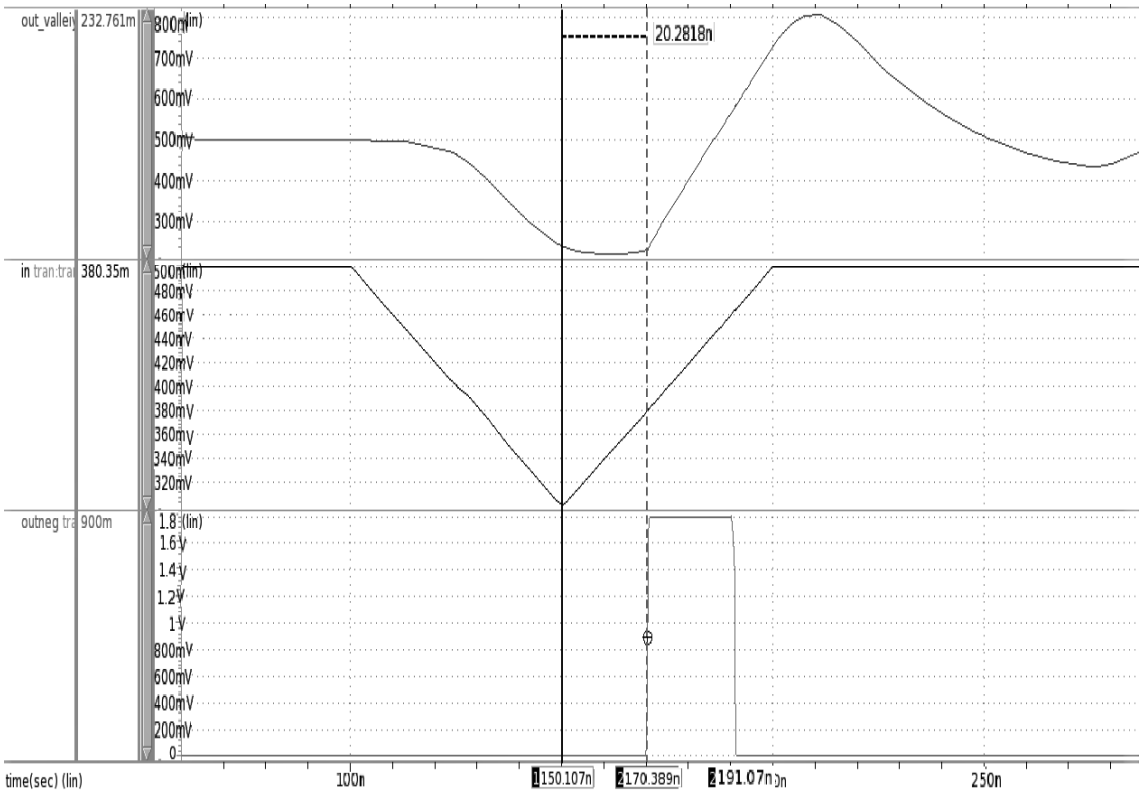

Figure 4.31: Propagation delay of the negative peak circuit for a 100 ns peak.

Table 4.27: Best, worst and typical cases for the delay for the negative detector for a 100 ns peak.

	D (ns)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst Case	42,75	Slow	Slow_Slow	Fast	Slow	1,62	-40
Typical Case	20,39	Typical	Typical	Typical	Typical	1,8	25
Best Case	10,3	Fast	Fast_Slow	Slow	Fast	1,8	125

4.5 Voltage Regulator Settling Time Measurement

For the testing of the settling time of the voltage regulator, the comparator used for the under-voltage detection was reuse to detect when the output voltage of the regulator reaches 80 % of the final output. Additionally, a counter was implemented in Verilog-A, to keep track of the time that passed since the regulator was activated until the output of the comparator goes low.

The clock selected for the system was 20 MHz, which means the maximum number of clock cycles the counter must count since the enable of the regulator, is 20000 plus the number of cycles the dead time of the regulator has. If the counter reaches to superior values, then the regulator has a bigger settling time then the allowed or, in more extreme cases, the regulator never reaches its final value. The number of clock cycles of the delay time was arbitrarily chosen without any criteria. In figure 4.34, the flow of the code can be observed. The code of the counter is in appendix A.

4.5.1 Results

In figure 4.32, it can be verified that the output voltage of the filter, which corresponds to signal in, already had reach 80 % of its final value, and before the maximum time allowed when the signal pass went high. It also can observe the situation, figure 4.33, where 1 ms plus the dead time has pass and the voltage of the regulator has yet to reach 80 % of its value. It is worth mentioning that the delay caused by the comparator or the RC filter is negligible in the test of the settling time. The signal out is the output of the regulator before being divided by two and going through the filter.

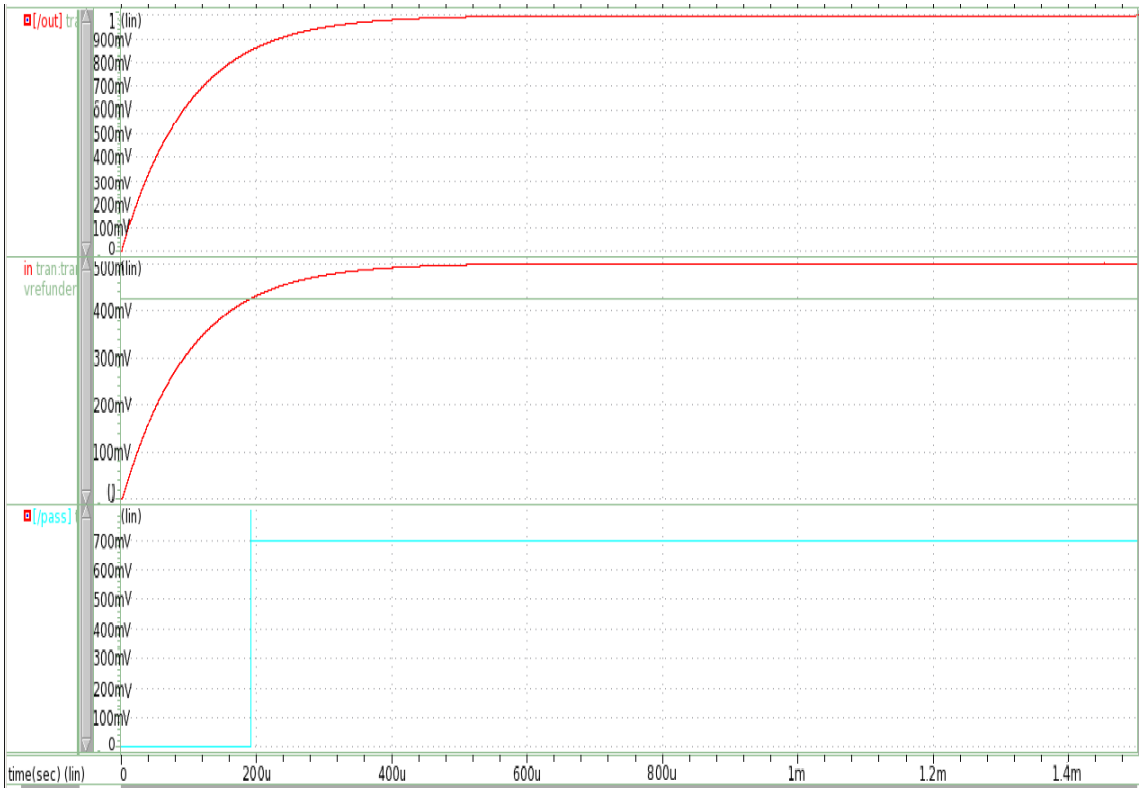

Figure 4.32: Voltage regulator passing settling time test.

Figure 4.33: Voltage Regulator failing settling time test.

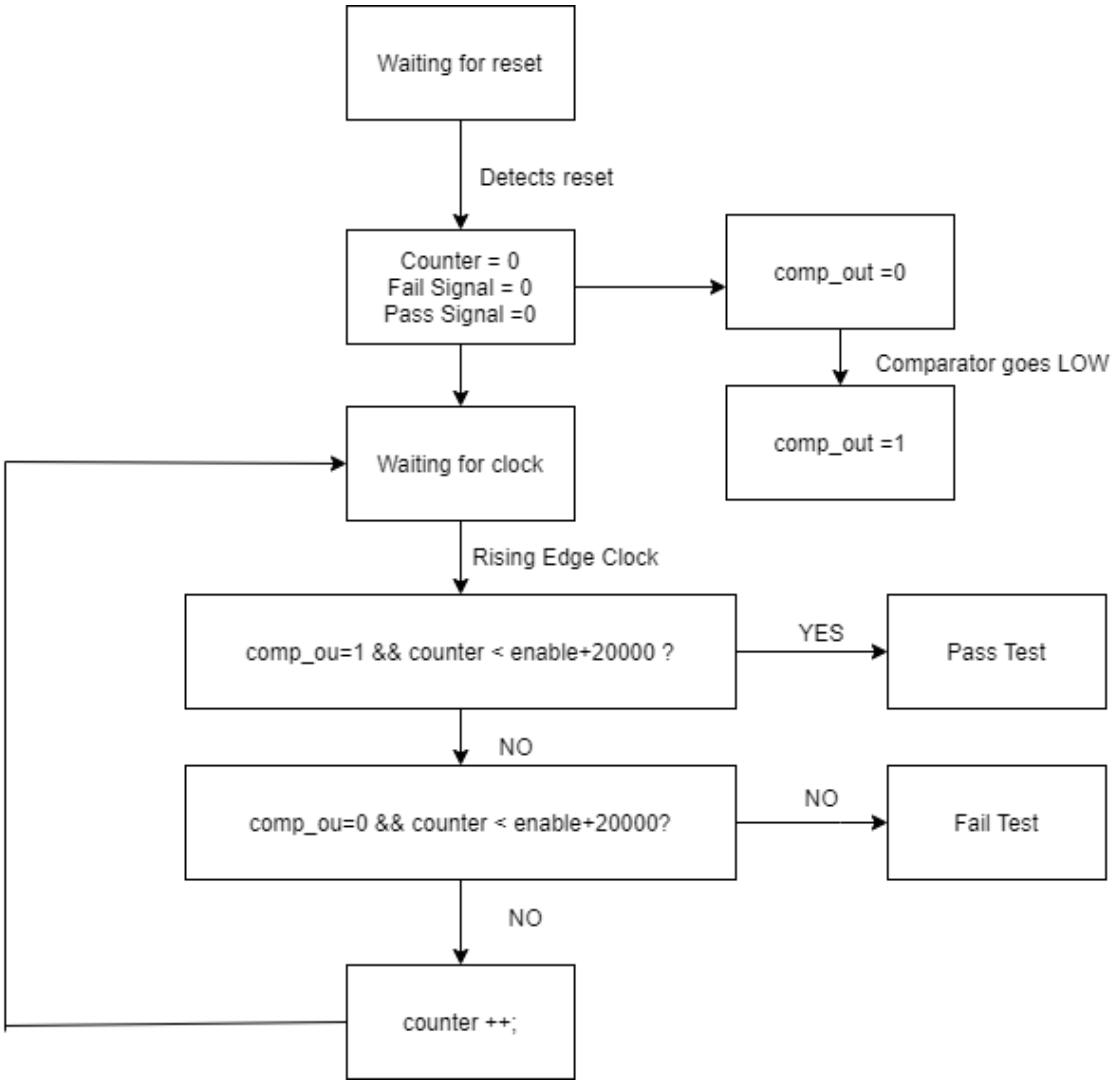

Figure 4.34: Settling time of the voltage regulator code.

Chapter 5

BIST Blocks - Oscillator

The circuits developed to test the oscillator are presented in more detail in this chapter. Simulation results are presented for the frequency drift measurement circuit, for the RC filter that measures the duty-cycle, as well as for the measurement of the settling time of the oscillator.

5.1 Frequency to Voltage Converter

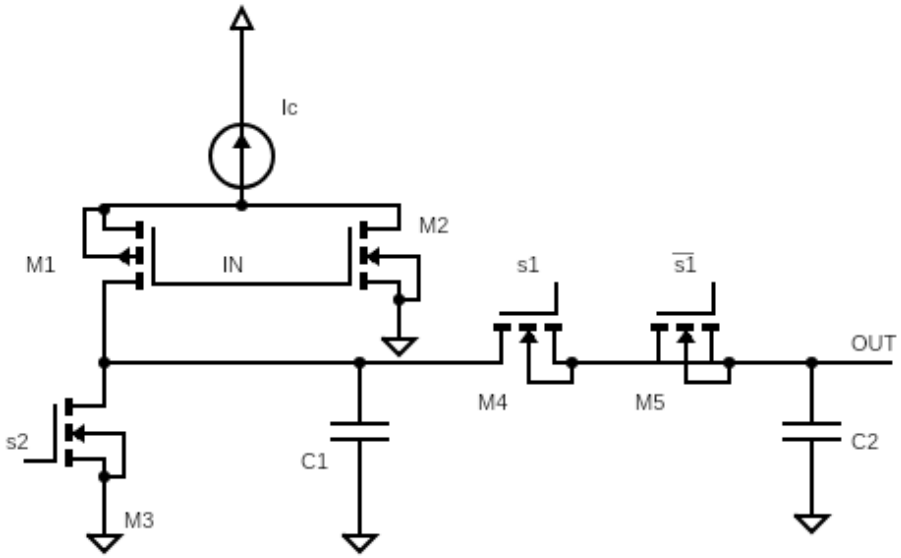

Figure 5.1: Frequency to Voltage Converter.

The BIST method presented in [33] was adopted to measure the frequency drift of the oscillator. This paper proposes the use of a frequency to voltage converter (FVC) and a frequency-divider to measure the frequency of a VCO. These circuits can be seen in figures 5.1 and 5.3, respectively. The FVC is composed of a constant current source I_C, two equal capacitors (C_1 and C_2), and a set of transistors that act as switches. Signals $s1$ and $s2$ are generated by the circuit presented in

figure 5.2. These signals control transistors M3, M4, and M5 and have the same frequency of the FVC input signal, but have a shorter pulse width. In this case, the pulse widths $s1$ and $s2$ are approximately equal to 1 ns.

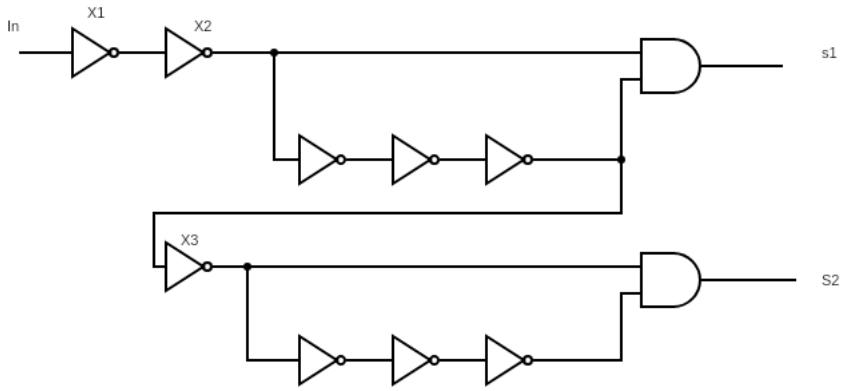

Figure 5.2: Circuit that generates the s1 and s2 control signals.

The FVC operates as follows. When *in* is low transistor M1 is on and M2, M3, and M4 are off, capacitor C_1 is charged during time T1 by I_C. T1 is equal to the half period of the input signal. The function of transistor M2 is to maintain the voltage of the node Ic at a low voltage level when the input signal is high. Thus, when the input waveform switches from high to low, C_1 will begin charging from a very low voltage. Therefore, the voltage error that would appear caused by the transient spikes that appear during the switching of M1, in case M2 is not used, is eliminated.

Transistor M1 is turned off when the input signal turns high and M2 is turned on. The charging of C_1 stops, being the charge accumulated in the capacitor is equal to:

$$V_{C1} = \frac{I_C * T1}{C_1} = Vout \tag{5.1}$$

Then, this charge will be transferred to C_2 through M4, which turns on when s_1 turns high. The charge stored in C_1 is equally redistributed between C_1 and C_2. Then, M3 turns off and the charge stored in C_2 is isolated from the rest of the circuit. The transistor M5 purpose is to act as a dummy switch and minimize the voltage error introduced by the charge injection in M4 when it turns between on and off states. After signal $s1$ goes low signal $s2$ goes high and the capacitor C_1 is discharged.

After the first time, the charge in C_1 is redistributed between the two capacitors, the voltage in$Vout$ is equal to half of the final voltage, then after the second time $Vout$ is increased by a quarter of the final voltage, and so on. After 8 iterations, which correspond to a time interval of 8T, where T is the period of the input signal of the FVC, it can be considered that the output voltage has already reached its final value.

The frequency to voltage converter as several limitations related to the frequency of the input signal. These limitations are imposed by the charging current I_C, the value of the capacitor C_1, and

the maximum and minimum output voltage:

$$F_{min} = \frac{I_C}{2C_1 V_{max}} \tag{5.2}$$

$$F_{max} = \frac{I_C}{2C_1 V_{min}} \tag{5.3}$$

The operating frequency range of the FVC can be fixed by choosing proper current and capacitor values. The maximum and minimum output voltages are limited by the power supply and ground. Another limitation in the maximum operating frequency is imposed by the pulse widths of $s1$ and $s2$:

$$F_{max} <= \frac{1}{2(\Delta T_{s1} + \Delta T_{s2})} \tag{5.4}$$

In our case, since $s1$ and $s2$ pulse widths are 1 ns, the maximum operating frequency of our FVC is 250 MHz.

The output of the FVC would then have to be sampled and converted by the SAR ADC, being the decision whether the oscillator's frequency is inside or not the *apriori* established range of acceptable values, taken in the digital domain.

5.1.1 Design of the Frequency to Voltage Converter

For the design of the FVC the following decisions were made concerning the transistors' aspect ratios. Since the transistors perform as switches their length was chosen to be the minimum value. MOS transistors perform as switches operate in the triode region, exhibiting a behavior similar to that of a voltage controlled resistor:

$$R_{ds} = \frac{1}{\mu_{n/p} C_{ox} \frac{W}{L} (V_{gs} - V_t)} \tag{5.5}$$

where $\mu_{n/p}$ is the carrier mobility of the process technology, C_{ox} is gate-oxide capacitance per unit area, V_{gs} is the gate-source voltage of the NMOS, and V_t is the threshold voltage.

Thus, considering that the time constant of the capacitor charging and discharging operations is equal to a resistance multiplied by the value of the capacitor, we can state that the resistance of transistor M4 when on has to be lower than $\frac{\Delta T_{s1}}{5(C_1+C_2)}$ and the resistance of transistor M3 has to be lower that $\frac{\Delta T_{s2}}{5C_1}$. Taking into account that $s1$ and $s2$ are 1 ns and the value of the capacitors is 0.178 pF, the values of the transistors on resistances have to be:

$$R_{M3} = 1,12\ k\Omega \tag{5.6}$$

$$R_{M4} = 560\ \Omega \tag{5.7}$$

Knowing the transistors' resistances their widths were calculated through a tool that calculates the resistance of the transistor and other parameters for a given V_{gs}, V_{ds}, W and L. Transistor M5 has to have half the width of M4 since its function is to minimize the charge injection caused

Table 5.1: Size of the transistors of the FVC

	W (μm)	L (μm)
M1	0,54	0,15
M2	0,27	0,15
M3	0,54	0,15
M4	0,54	0,15
M5	0,27	0,15

by M4. Transistor M2 has the minimum size and the width of M1 was calculated through the simulation tool. The aspect ratios of the transistors are shown in table 5.1.

Regarding the circuit that generates signals $s1$ and $s2$, as it can be seen in figure 5.2, at the inputs of the AND gates, we have two signals where one is the inverse of the other and its delayed τ_1 or τ_2, this generates at the outputs of the AND gates the controls signals $s1$ and $s2$ which have the same frequency and pulse width of τ_1 and τ_2, respectively. The desired delay is achieved through a cascade of inverters.

The inverters X1 and X2 function is to prevent the overlap of the signals $s1$ and the signal *in* and the inverter X3 is to prevent the overlap between $s1$ and $s2$, and to recover the original signal.

The design of the inverters started by assuming that the PMOS and NMOS have the same length which is 0,27 μm and that the width of NMOS is 0,54 μm. Then a DC analyse was performed to find the width of the PMOS. In the analyze, the number of fingers of the PMOS was varied between 1 and 10, and its was checked in which wave the output and input were equal to half of the supply voltage. The width obtained was 1,62 μm.

The NAND gate was designed to be analogous to the inverter. So, the NMOS transistors in series show double width of the inverter's NMOS transistors, and the PMOS transistors in parallel have the same width as the inverter's PMOS transistor. All transistors length is also 0,27 μm.

5.1.2 Frequency Divider

As stated before, the maximum frequency of the FVC is limited to 250 MHz but the oscillator in test has a nominal frequency of 1 GHz. So, the frequency of the signal has to be lowered before the signal is applied to the FVC. In order to achieve this, a frequency divider was added. The topology chosen to implement this divider is the truly single-phase clock (TSPC) D-FFs [42] that can be seen in figure 5.3. This topology has minimum power consumption, area, and the frequency of the input signal is divided by two.

When designing this circuit the following decisions were taken: the transistors' length is the minimum one and the widths were all the same with the exception of M5 which has to be 2 times wider to maximize the operating speed as suggested in [42]. A reset was included (M8) and an inverter was added at the output "nout" to insure rail to rail voltage swing in the input of the circuit that follows. At the input of the first frequency divider, two inverters were inserted for the signal to have rail to rail voltage swing since the nominal voltage of the oscillator is 1 V which is lower than the power supply. In the first inverter, the PMOS and the NMOS have the same length which

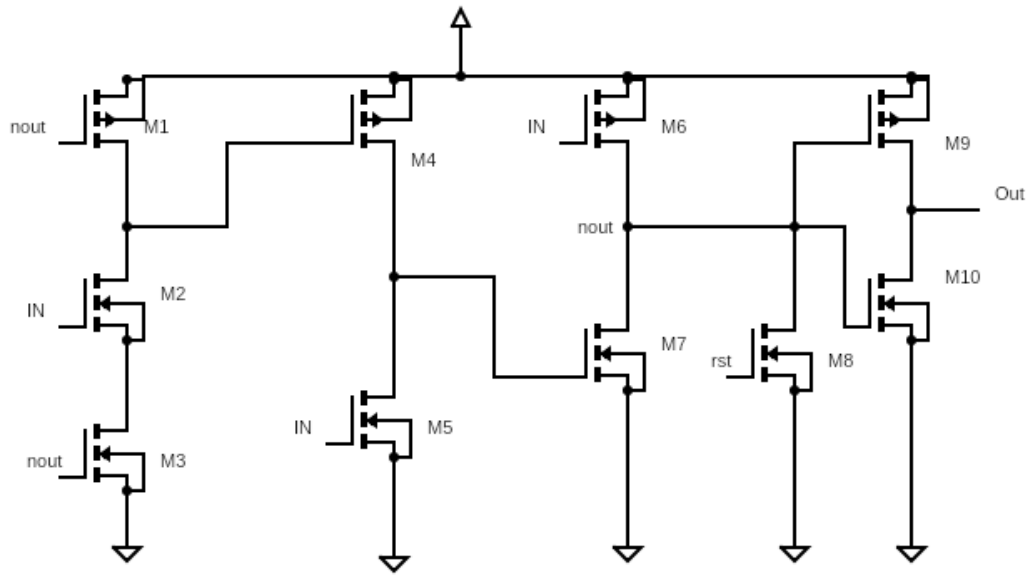

Figure 5.3: Frequency divider.

is 0,15 μm, and that the width of NMOS is 1.08 μm and the width of PMOS is 1.62 μm. The second inverter' transistors have a length of 0,15 μm, and the width of NMOS is 0.54 μm and the width of PMOS is 1.62 μm.

In the this implementation of the FVC 6 frequency dividers were connected in cascade to achieve a frequency 64 times lower than the input frequency.

5.1.3 Voltage to Current Converter

To achieve higher accuracy in the output of the FVC, a constant current that shows very low sensitivity to process, temperature and power-supply variations is needed. So, the voltage to current converter presented in figure 5.4 was chosen. It is composed of an operational amplifier, a NMOS transistor, a PMOS current mirror, and a resistor.

The positive input of the operational amplifier is connected to one of the outputs of the previously mentioned bandgap reference. The negative input is connected to the resistor. The amplifier

Table 5.2: Dimensions of the transistors for the frequency divider.

	W (μm)	L (μm)
M1,4	0,54	0,15
M5	1,08	0,15
M6,7	0,54	0,15
M8	0,27	0,15
M9	1,62	0,15
M10	0,54	0,15

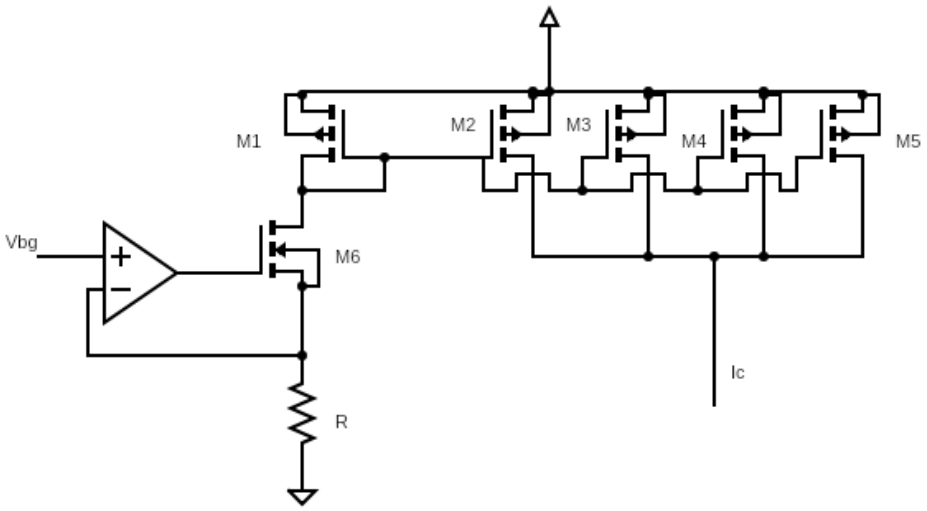

Figure 5.4: Voltage to current converter.

feedback mechanism forces the two inputs to be at the same voltage. Therefore, the voltage across the resistor, taking into account the amplifier offset, will be

$$V_R = V_{Ref} \pm V_{OS} \tag{5.8}$$

Therefore, the current is dependent of the voltage provide by the bandgap plus the offset and the value of the resistor:

$$I_R = \frac{V_{Ref} \pm V_{OS}}{R} \tag{5.9}$$

The variation of the resistor value due to process variations can be 25.7 %, in a typical to fast corner variation, consequently the value of the current has the same variation (assuming constant voltage at the resistor terminals), which is something we do not wish to have. A proposed solution for this problem is to use a trimmed resistor. It is important to mention that in all simulations for this circuit, the process variation of the resistor was not considered and the resistor used in the simulations was a polysilicon resistor at a typical corner.

The variation observed in the current is mostly due to the variation of the bandgap voltage which is 1,2 % in PVT (without process variation of the resistor) and the variation of the resistor value with temperature is 3,79 % for a typical resistor.

To design the voltage to current converter, the considered V_{ref} is 514 mV and the current $\approx 21\ \mu$A which give us a resistor of $\approx 24\ k\Omega$. The current I_C, the capacitor C_1' charging current, will be, approximately, 12 μA. For the transistors' aspect ratios it was considered that they operate in the saturation region and it was established that the overdrive voltage of the NMOS, $V_{gs} - V_t$, would be 0,2 V. Considering that the current is 21 μA, through simulation tool mentioned before,

it was obtained, for M6, that:

$$\frac{W}{L} = 4 \tag{5.10}$$

For the current mirror, the overdrive voltage chosen was also 0,2 V, which gives for M1:

$$\frac{W}{L} \approx 11 \tag{5.11}$$

For the other PMOS transistor, considering that it has to have a current of, approximately, 12 μA:

$$\frac{W}{L} \approx 6,8 \tag{5.12}$$

Originally, it only had a single PMOS transistor on the right side of the mirror, but it was replaced by four transistors where each transistor has 1/4 of the original width. Therefore the copying of the current from one branch to the other branch was improved. So, $\frac{W}{L} \approx \frac{6,8}{4}$.

Thus, the value of the width for M6 is $1,62\ \mu$m, for M1 is $11,88\ \mu$m, and for the other PMOS the width is 5.94 μm. All transistors have the same length of $1,08\ \mu$m. The PMOS current mirrors should have large widths in order to reduced mismatch.

5.1.4 The Switches

Even though, in the specifications the frequency range of the oscillator is from 800 MHz to 1,2 GHz, it was proposed to turn the FVC operational for oscillators with different nominal frequency that can go from 300 MHz to 4 GHz. However, in the current circuit configuration, if a signal with a frequency of 300 MHz is applied to the 6 frequency dividers the output voltage calculated through equation 5.1 would be higher than the power supply voltage. Besides, after going through 6 frequency dividers, a signal with a frequency of 300 MHz would have its frequency divided by 64, originating a signal with a very low frequency, the frequency divider implemented can not operate at such low frequencies.

To overcome this problem, it was decided to insert transmission gate switches at the outputs of the frequency dividers. This way, the appropriate output can be chosen for a given frequency. Four frequency ranges were established:

- 300 MHz to 600 MHz;
- 600 MHz to 1,2 GHz;
- 1,2 GHz to 2,4 GHz;
- 2,4 GHz to 4 GHz.

In the first range the frequencies are divided by 8, in the second divided by 16, in the third by 32 and in the fourth by 64. As mentioned before the transistor displays a similar behaviour to a variable resistor when it is working as a switch.

Therefore, when designing the transmission gate switches the sizes of PMOS and NMOS were chosen so that their resistances were similar and in the order of hundreds Ω, namely 350 Ω.

$$W_{NMOS} = 2,7\ \mu m \quad W_{PMOS} = 8,1\ \mu m \quad L_{MOS} = 0,15\ \mu m \tag{5.13}$$

The switches will be controlled by the digital part of the BIST that knows the range of frequencies we want to use.

5.1.5 Results

This section discusses the results of the several simulations carried out with the FVC.

Taking into account that the current I_C is approximately 11,7 μA and that the capacitor is 0,178 pF and reminding equation 5.1, the voltage at the output of the FVC should be, when the input signal has a frequency of 1 GHz:

$$V_{out} = \frac{11,7u * 8n}{0,178p} \approx 525\ mV \tag{5.14}$$

Note that the period of the input signal in the FVC is 16 ns, since the signal has a frequency of 1 GHz, its period is increased 16 times. However, as we can see in figure 5.5, the voltage at the output of the FVC is ≈ 479 mV, lower than the calculated value. A possible reason for this to occur is that the signal from the frequency divider didn't have a 50% duty-cycle. To verify if this was the problem, the output of the oscillator was directly injected in the FVC, instead of going through the frequency divider.

One can observe in figure 5.6 that the output, in this configuration, is very similar to the voltage obtained when the signal goes through the frequency divider. So, the problem was not the frequency divider. Actually, the problem is in the leakage currents of the capacitors and other leakage associated with the transistors. A solution will be provided bellow.

In figures 5.7 and 5.8, it is possible to observe the FVC output voltage (middle panel) when the oscillator is at its maximum and minimum allowed frequency. The top waveform presents the input signal of the FVC and the bottom one corresponds to the voltage in the capacitor C_1.

As we can observe in figure 5.9 and in table 5.3, the FVC output voltage varies between 419,26 mV and 556,61 mV when the input is an 1 GHz waveform, which corresponds to a variation of 28,14 %. Similar variation was obtained when the input frequency is 800 MHz or 1,2 GHz. The worst cases were equal for every situation, as we can observe in 5.4 and 5.5.

The variation obtained in the output mainly comes from the capacitor whose value may vary, peak to peak, almost 22 % in process variation, from the variation of the current whose value depends on the bandgap variation (1,2 %), and the resistor value which varies with temperature (3,79 %). Without the capacitor process variation, the total variation of the output is 6,9 %, as we can see in figure 5.10. This variation is, approximately, equal to the variation of I_C.

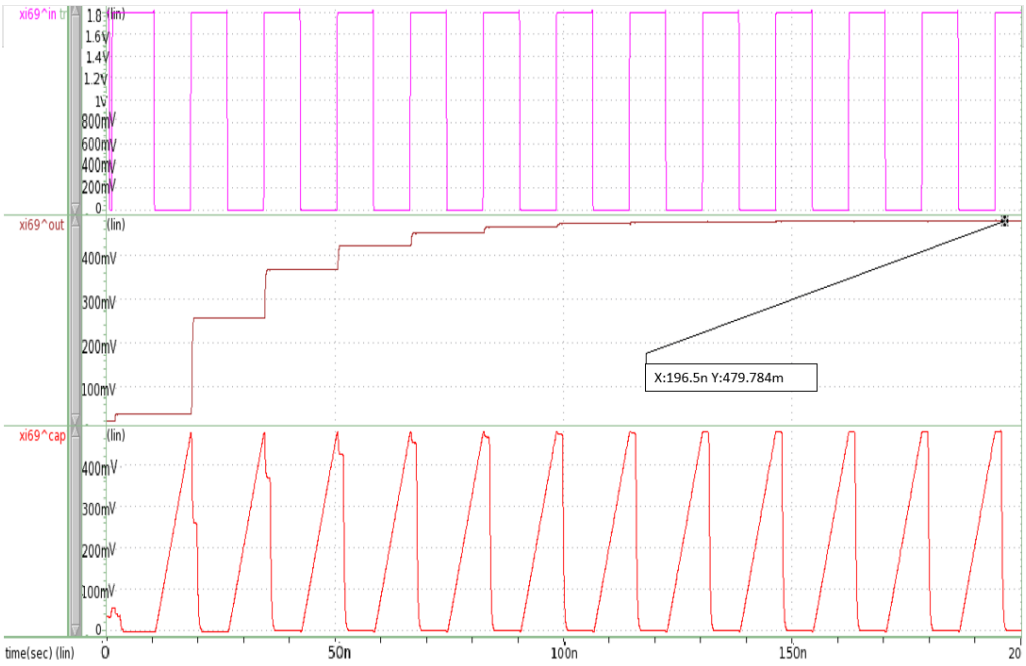

Figure 5.5: FVC waveforms for a 1 GHz signal.

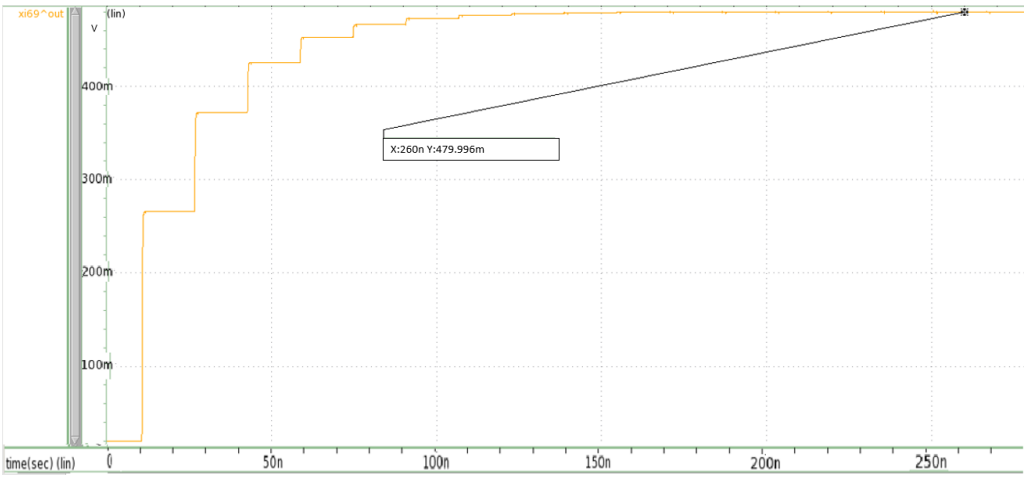

Figure 5.6: Input signal directly in the FVC.

In figure 5.14, it is possible to observe the variation of the current I_C (panel bellow) and the current in the resistor (first panel). The current in the resistor has a variation of approximately 5%. The I_C current has a variation in PVT of approximately 7%.

Taking into account that the variation presented in the output is 28.14 %, it is very difficult to measure accurately the frequency of the oscillator.

If we include Monte Carlo simulation results and the resistor process variation in the bandgap, this variation will increase. Since, in the Monte Carlo simulation for the bandgap, the output voltage has a variation of 3,4 % for typical conditions. If to this we add the offset of the operational

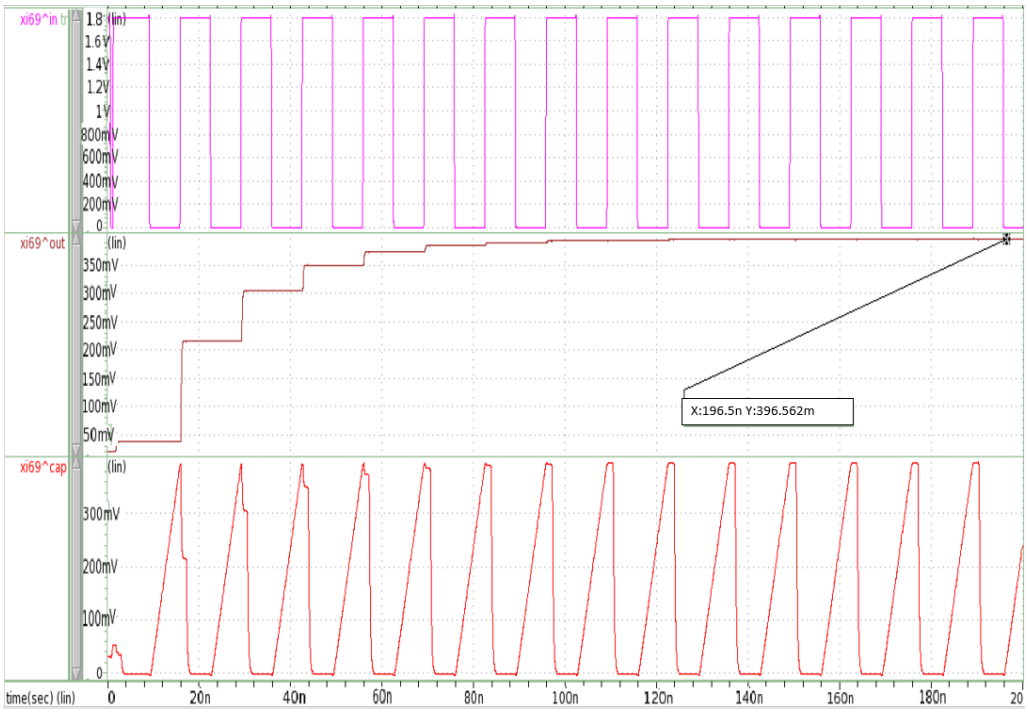

Figure 5.7: FVC waveforms for a 1,2 GHz input signal.

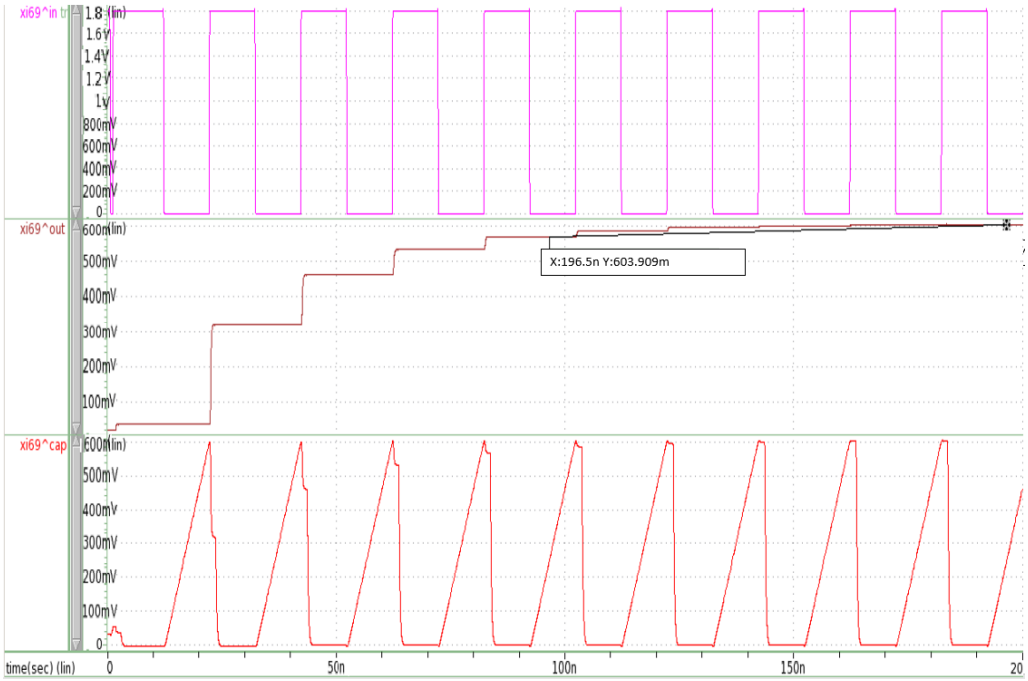

Figure 5.8: FVC waveforms for a 800 MHz input signal.

amplifier and the variation caused by the mismatches in the PMOS current mirror, the variation of I_R will increase, and, consequently the variation of the output of the FVC will increase as well.

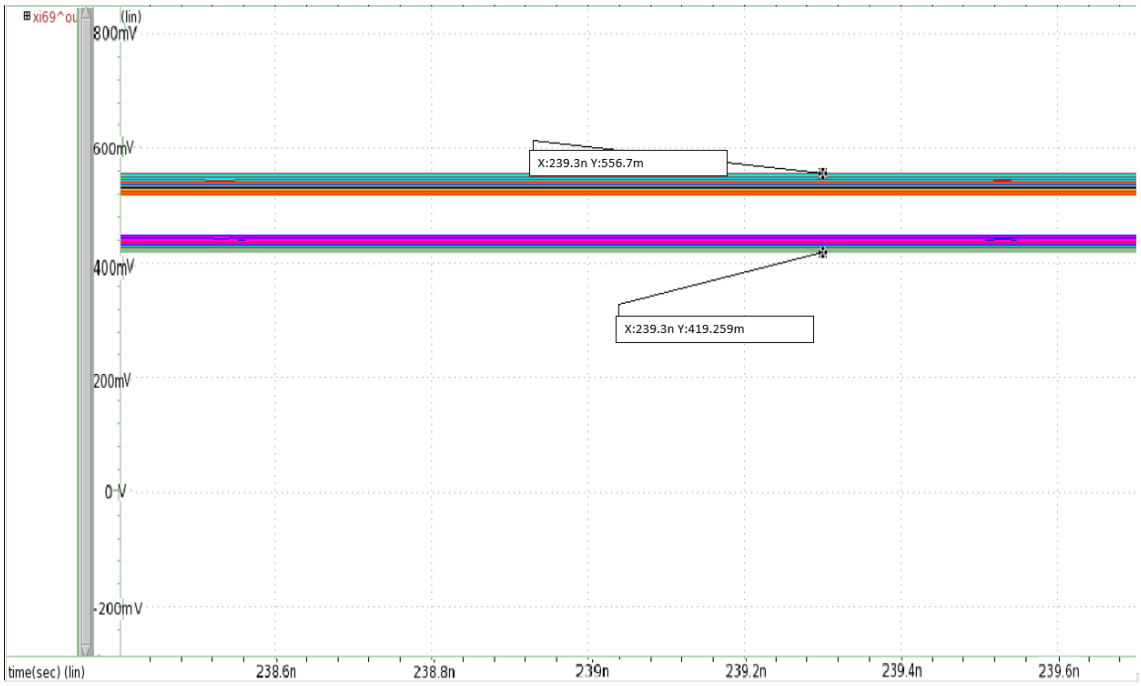

Figure 5.9: FVC output in PVT for 1 GHz input signal.

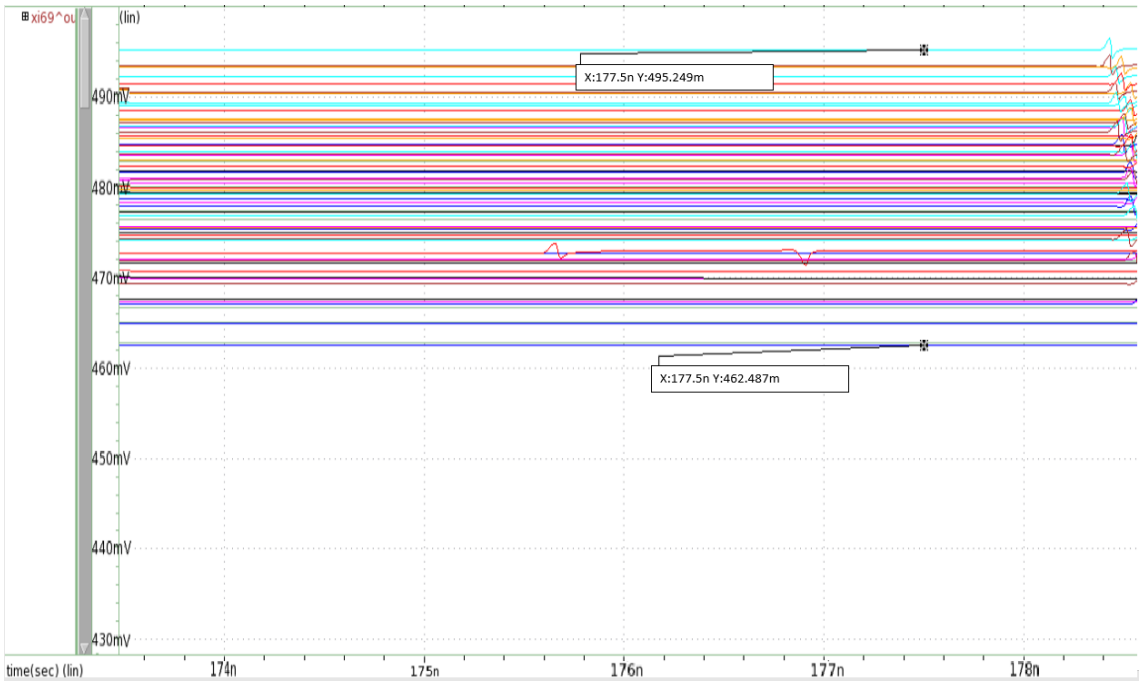

Figure 5.10: FVC output in PVT for 1 GHz signal without capacitor variation.

In Monte Carlo, for typical conditions and 740 iterations, the current I_C has a total variation of approximately 7 %, as does the output. See figure 5.15 and 5.11.

Besides trimming also the capacitor, and because we still have the variation of the current

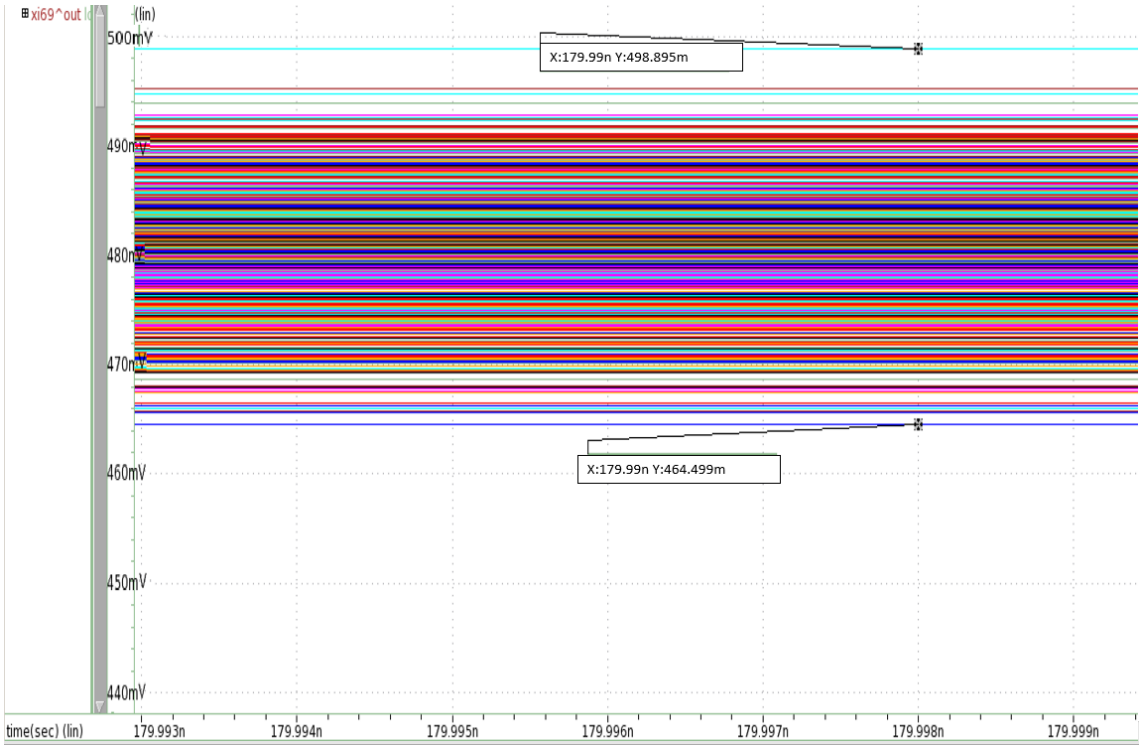

Figure 5.11: FVC output for a 1 GHz signal in 740 Monte Carlo simulations.

and the current losses through the circuit, a proposed solution its to calibrate the FVC with the help of the digital part of the system, before starting the testing of the oscillator frequency. This calibration mechanism was not implemented but it is a suggestion for future work. Nevertheless, an overview of what the mechanism should do is given bellow.

If we introduce in the FVC a signal with a well-known frequency, like for example the system clock, since we know the theoretically expected corresponding voltage (after equation 5.1), when the digital part learns the value given by the FVC, it calculates the relation between the expected value and the one given by the FVC. This will give us a constant that will be applied to all outputs of the FVC. However, this calibration system still does not solve the variation caused by the temperature.

Table 5.3: Best, worst and typical cases for the output of the FVC with 1 GHz input wave.

	Output(mV)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst 1	556,7	Typical	Fast _Fast	Slow	Fast	1,98	-40
Worst 2	429,26	Typical	Fast_Slow	Fast	Slow	1,62	125
Typical/Best	479,78	Typical	Typical	Typical	Typical	1,8	25

Table 5.4: Best, worst and typical cases for the output of the FVC with 800 MHz input wave.

	Output(mV)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst 1	698,32	Typical	Fast _Fast	Slow	Fast	1,98	-40
Worst 2	526,52	Typical	Fast_Slow	Fast	Slow	1,62	125
Typical/Best	603,8	Typical	Typical	Typical	Typical	1,8	25

Table 5.5: Best, worst and typical cases for the output of the FVC with 1,2 GHz input wave.

	Output(mV)	Resistor	MOSFET	BJT	Capacitor	Supply	Temperature
Worst 1	460,42	Typical	Fast _Fast	Slow	Fast	1,98	-40
Worst 2	346,28	Typical	Fast_Slow	Fast	Slow	1,62	125
Typical/Best	396,55	Typical	Typical	Typical	Typical	1,8	25

5.1.5.1 Voltage to Current Converter Stability

In typical conditions the converter has a phase margin of 37.1°. Figure 5.12 shows the Bode diagram of the operational amplifier highlighting a phase-margin of 34,63°.

Considering PVT variations, the voltage to current converter also maintains stability, where the-phase margin value ranges from 39,6° to 31,5°. The PVT simulation results are present in figure 5.14.

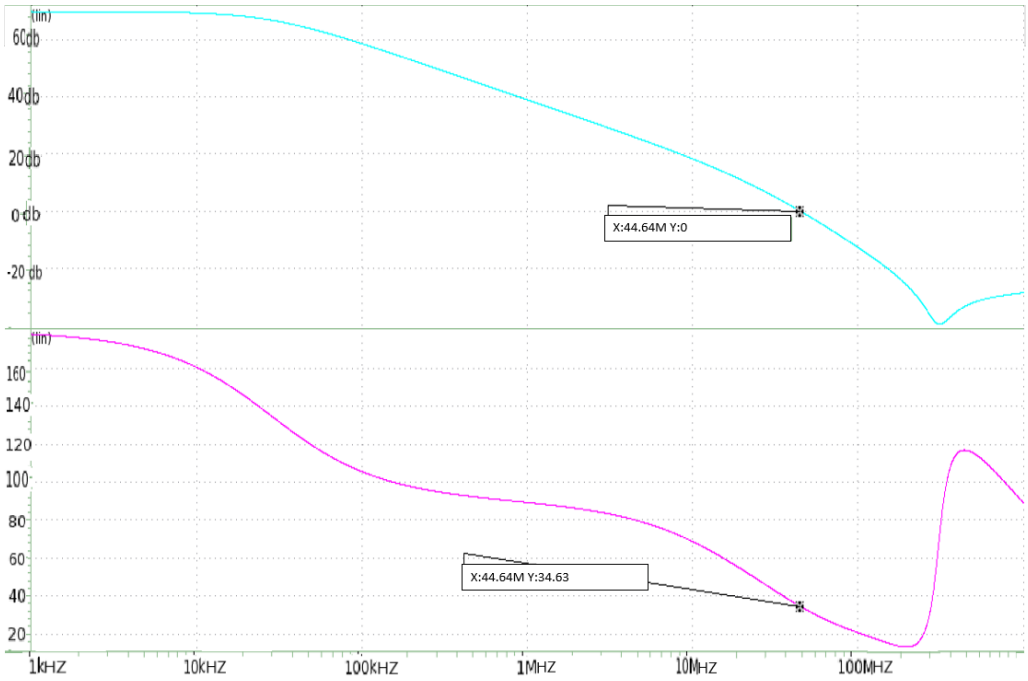

Figure 5.12: Stability analyze voltage to current converter.

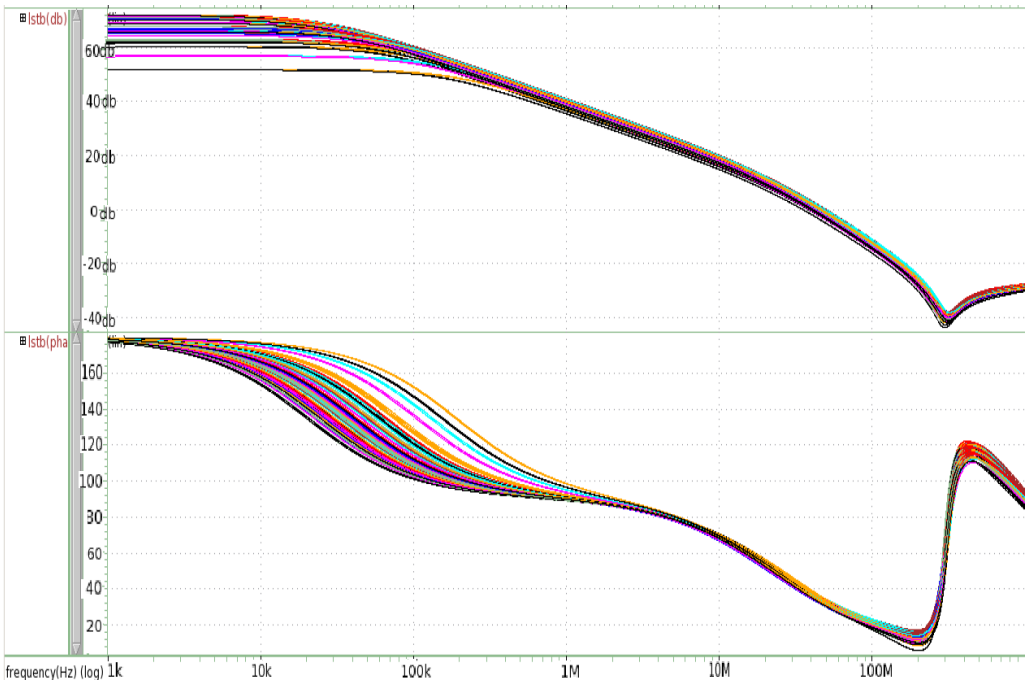

Figure 5.13: Stability analyze voltage to current converter in PVT.

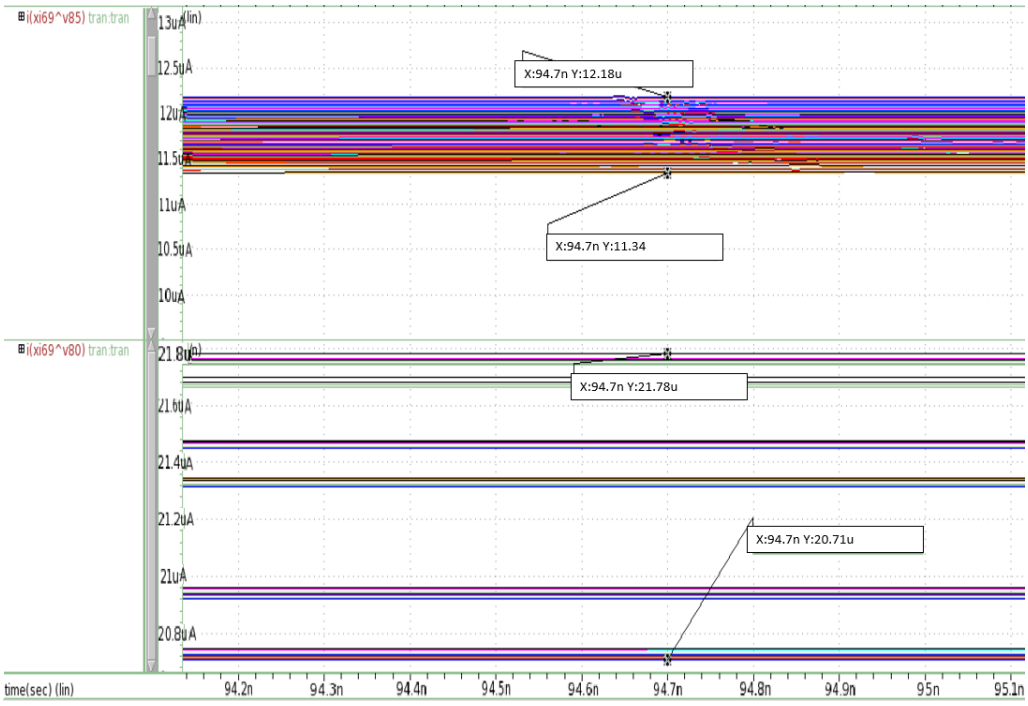

Figure 5.14: Voltage to current converter currents in PVT.

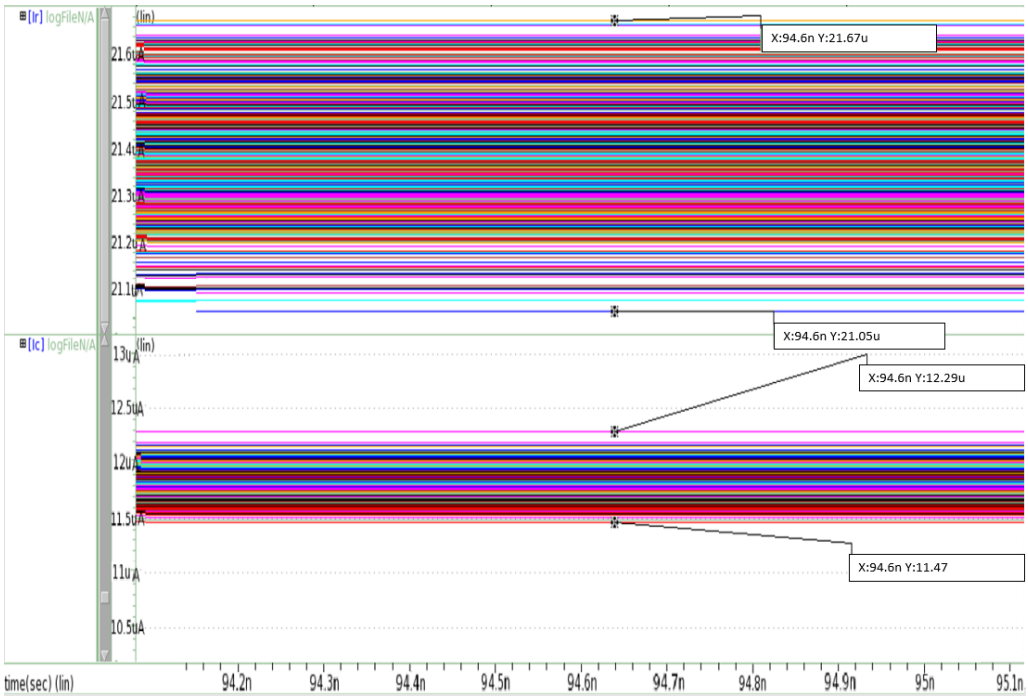

Figure 5.15: Voltage to current converter currents in 740 Monte Carlo simulations.

5.1.5.2 The Frequency Ranges Functionality

In this section the simulation results that proves the functionality of the frequency ranges are presented. Four ranges of frequency measurement were implemented. The following figures display the maximum and minimum output voltage for each range. The PVT simulations are in appendix B.

Thus, figures 5.16 and 5.17 correspond to the first range that goes from 300 MHz to 600 MHz. The corresponding voltage range is from $\approx$ 811,04 mV to $\approx$396,44 mV. For the second range, from 600 MHz to 1,2 GHz, the maximum and minimum voltages are displayed in figures 5.18 and 5.7. The voltages are $\approx$ 811,98 mV and $\approx$ 396,56 mV. The third range that covers frequencies from 1,2 GHz to 2,4 GHz yields a voltage range of $\approx$ 811,8 mV and $\approx$396,9 mV. The last range goes from 2,4 GHz to 4 GHz and has a voltage range of $\approx$ 480,422 mV to $\approx$ 811,9 mV.

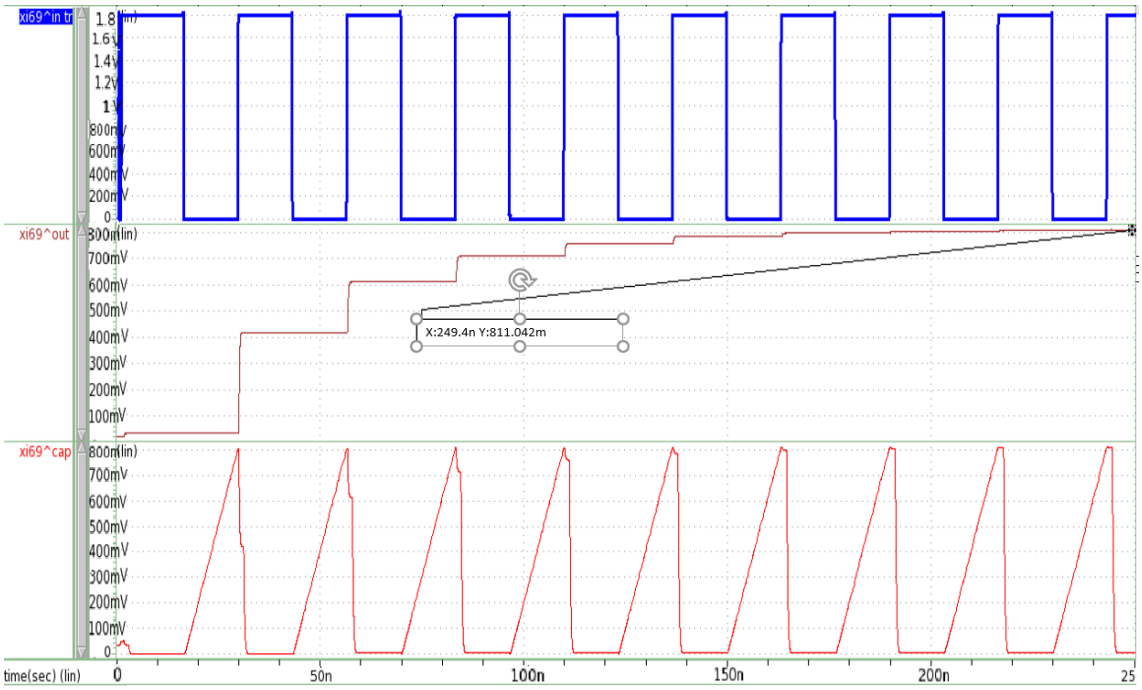

Figure 5.16: Output of the FVC with 300 MHz input wave.

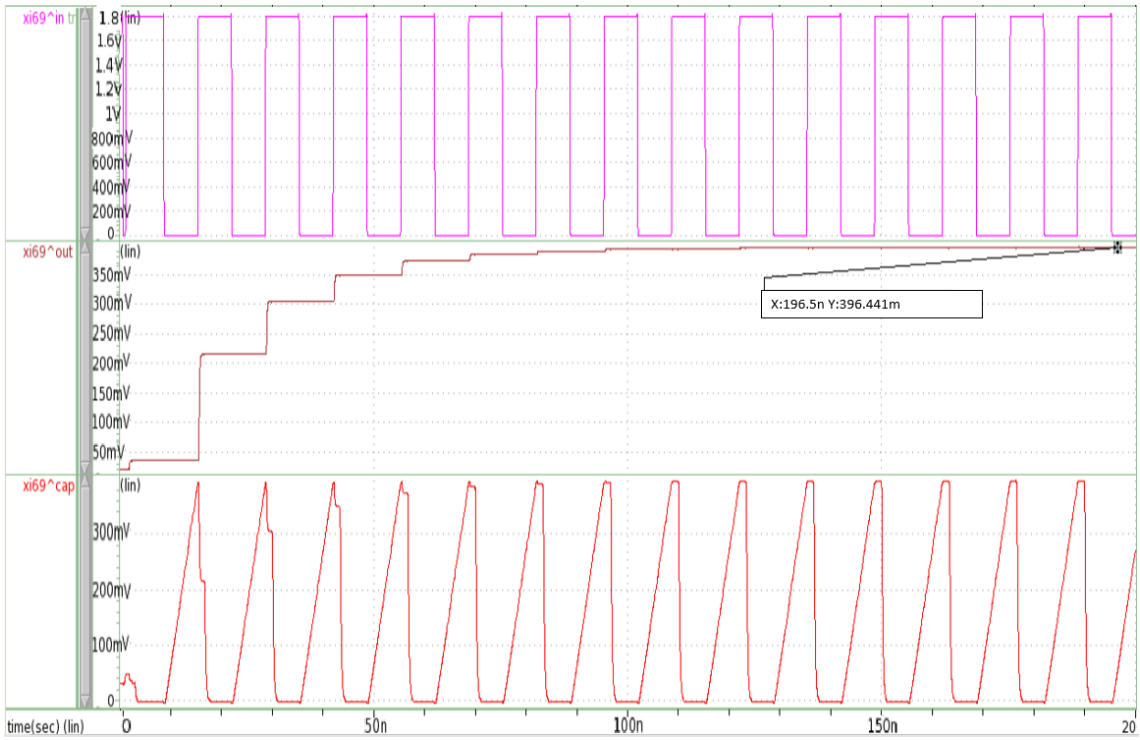

Figure 5.17: Output of the FVC with 600 MHz input wave in the first range.

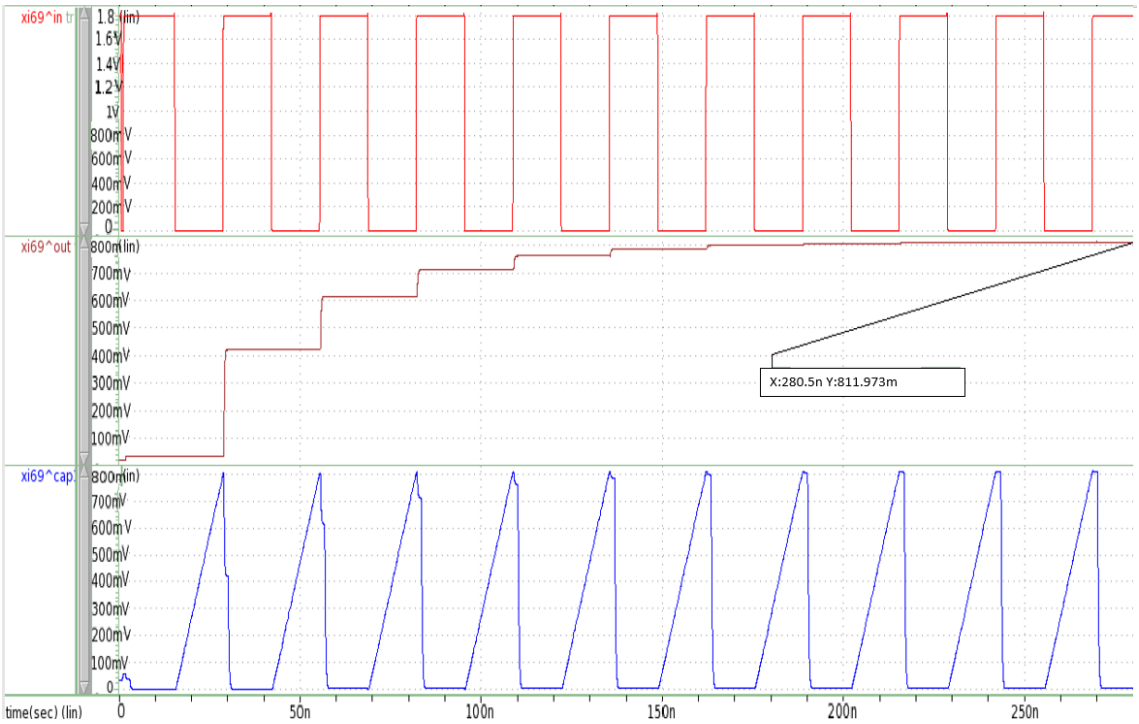

Figure 5.18: Output of the FVC with 600 MHz input wave in the second range.

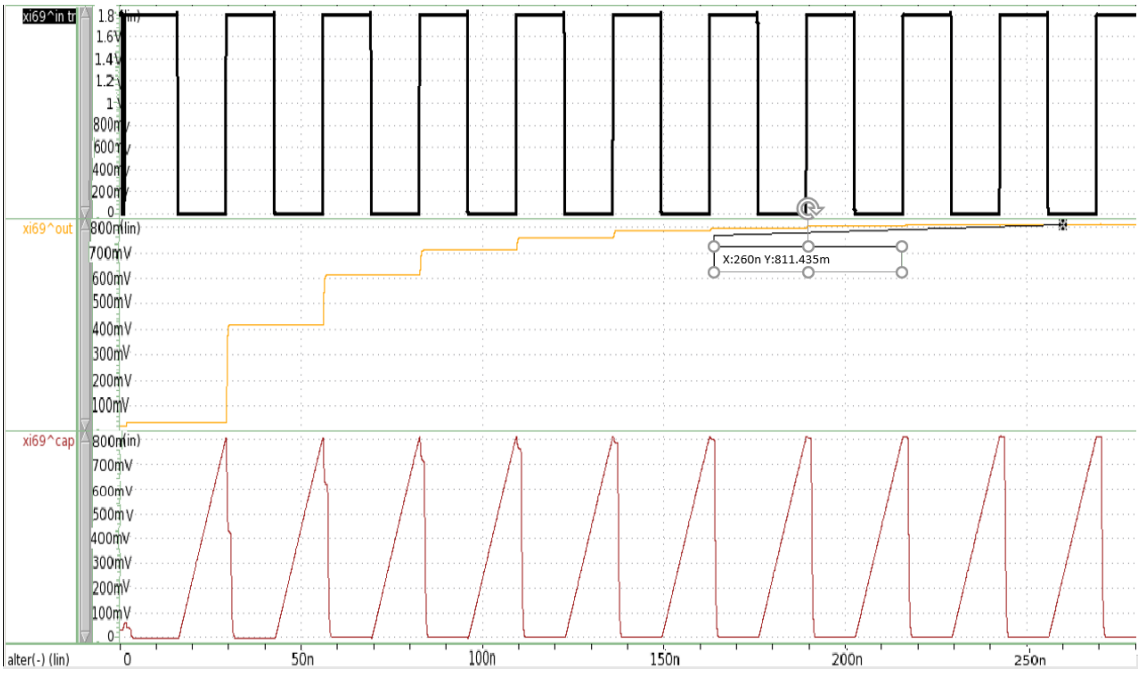

Figure 5.19: Output of the FVC with 1,2 GHz input wave in the third range.

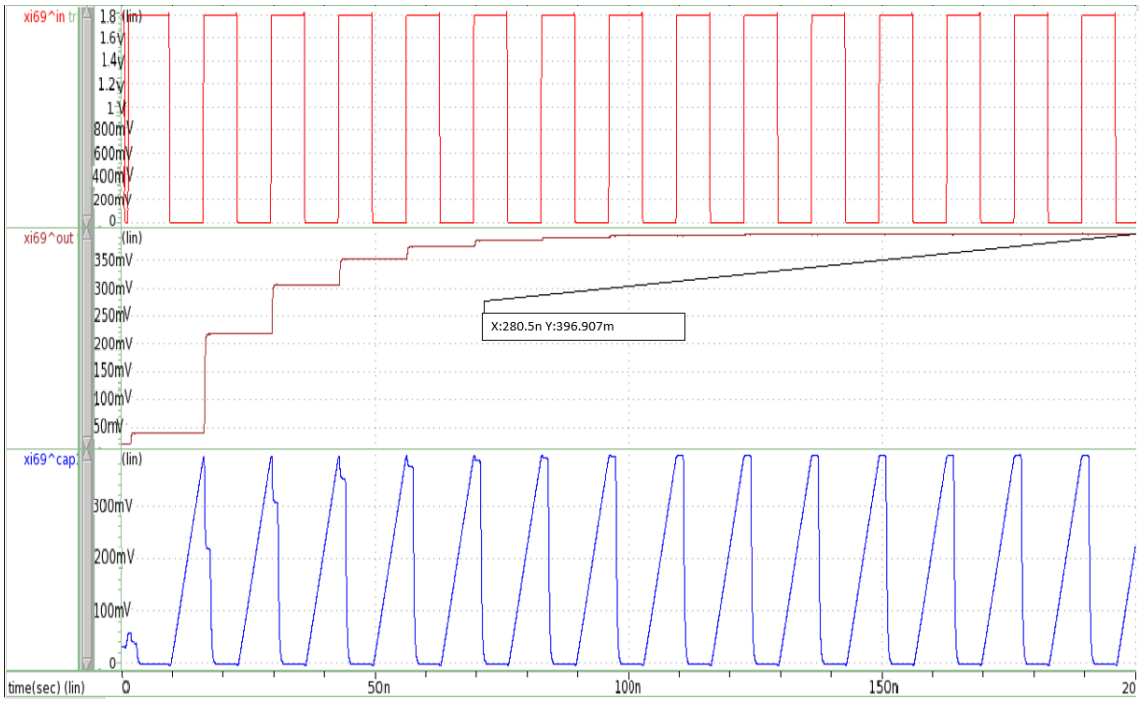

Figure 5.20: Output of the FVC with 2,4 GHz input wave in the third range.

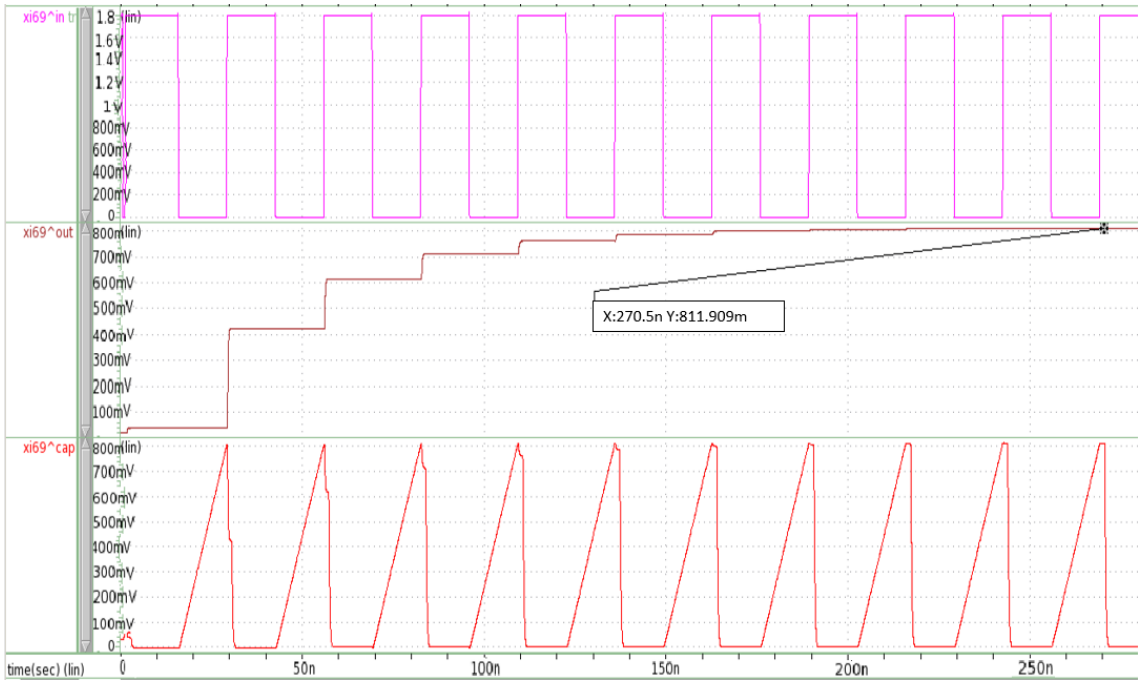

Figure 5.21: Output of the FVC with 2,4 GHz input wave in the fourth range.

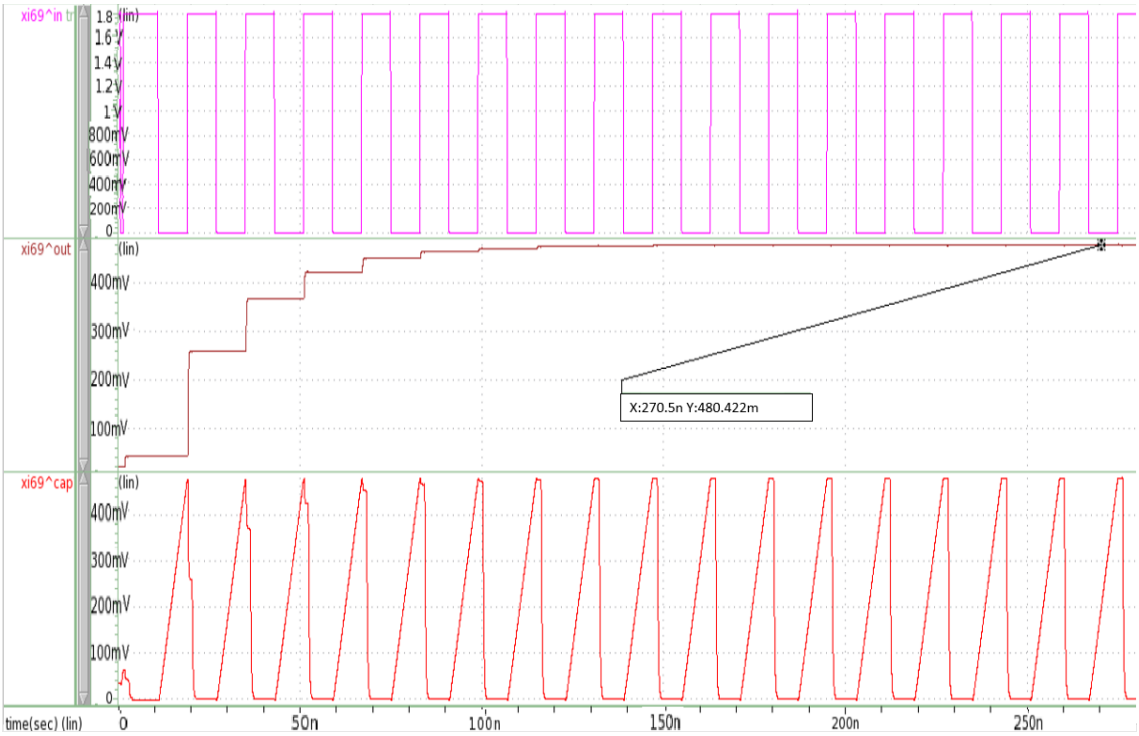

Figure 5.22: Output of the FVC with 4 GHz input wave.

5.2 RC Filter

Another parameter the system has to test is the duty-distortion of an oscillator. Given the relationship between the DC value of a square-wave and its duty-cycle, a simple RC low-pass filter was implemented, as suggested in [36]. Since with this filter we can obtain the DC value of the square-wave oscillator, this value is directly proportional to the duty-cycle of the signal under test.

In our case, since the nominal output value of the oscillator is 1 V and the nominal duty-cycle is 50 %, the voltage at the output of the filter will be 0,5 V. The values of the resistance and capacitor are, respectively, 120,25 kΩ and 0,22 pF, which gives the filter a cutoff frequency of

$$\frac{1}{(2\pi * RC)} = 6\ MHz \tag{5.15}$$

The theoretical value of the rise time is $2,2\tau = 58,2\ ns$.

The output of the RC filter would then be sampled and converted by the SAR ADC and the digital part of the BIST would decide if the duty-cycle of the oscillator is inside of the established values.

5.2.1 Results

This section presents the frequency response simulation of the RC filter, as well as its transient response when the oscillator duty-cycle is 50 %, 60 % and 40 %. The rise time for each situation is also given.

5.2.1.1 Frequency Response

The frequency response of the filter can be seen in figure 5.23. The simulated value for the cutoff frequency is 5,41 MHz, which is lower than the calculated. Due to the parasitic capacitors in the polysilicon type resistors.

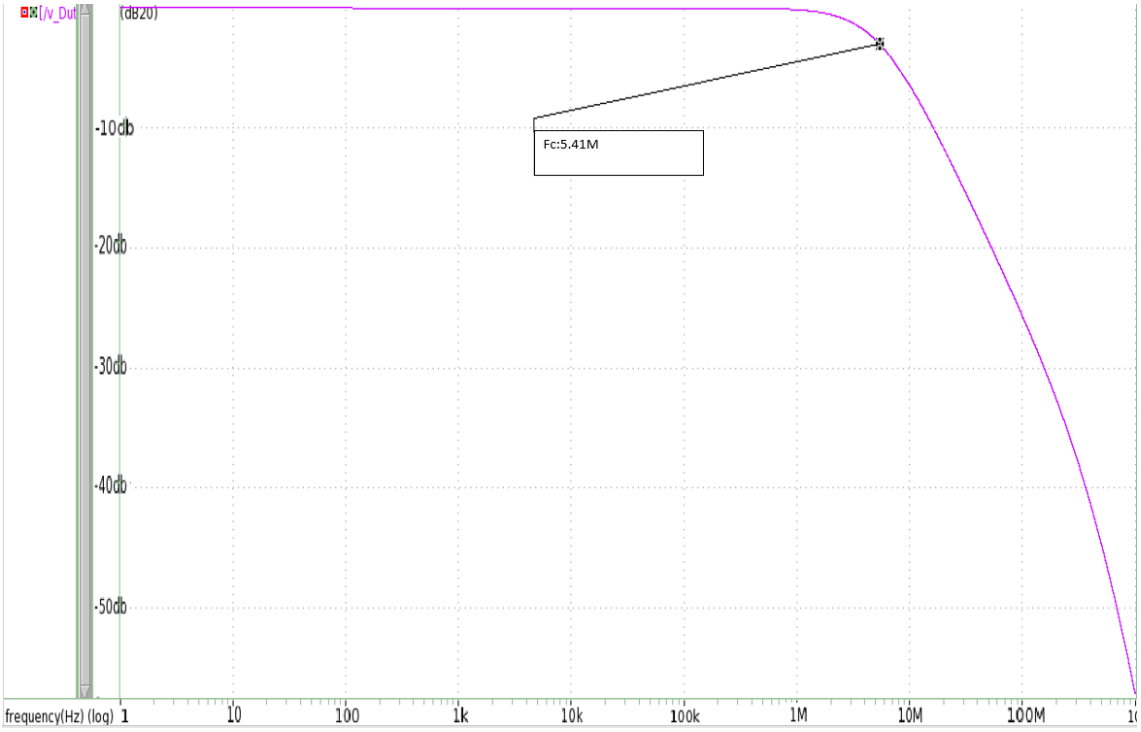

Figure 5.23: Frequency response of the RC filter.

5.2.1.2 Transient Response

Figure 5.24 shows the transient response of the filter when the duty-cycle of the oscillator is 50 %, 60 % and 40 %. As expected the output voltage of the filter is 0,5 V, 0,6 V and 0,4 V when the duty-cycle is 50 %, 60 % and 40 %. The rise time obtained in the simulation is similar to the value calculated.

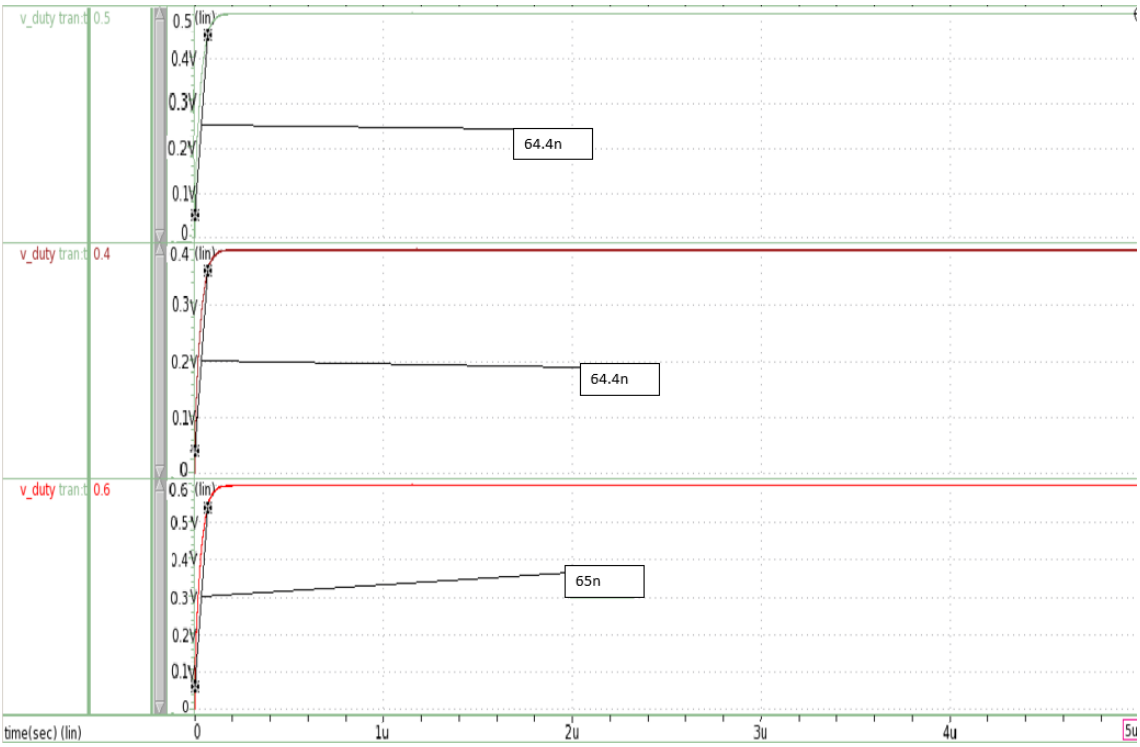

Figure 5.24: Transient response of the RC filter

5.3 Oscillator Settling Time Measurement

For the measurement of the settling time of the oscillator, two counters were implemented. The function of one of the counters is to measure the frequency of the oscillator after counting the rising edges of the signal in a given time interval. Since the nominal frequency of the oscillator is known, we can know *apriori* the number of rising edges of the signal in a time interval, in our case 50 ns. The number of rising edges of a 1 GHz signal is 50, but since we consider that the frequency of the oscillator is already stabilized when it reaches 90 % of its final value, our counter has to count 45 rising edges in 50 ns.

The other counter counts the number of time intervals passed since the oscillator was enabled. The settling time specified for the oscillator was 1 μs which corresponds to 20 time intervals. If the oscillator reaches its final frequency value before the maximum settling time of 1 μs a PASS signal its generated, otherwise a FAIL signal is generated. A flow diagram of the code can be seen in figure 5.27 and the code developed is presented in appendix A.

In order to test this code, a Verilog-A code had to be developed to simulate the initial response of an oscillator, see appendix A. It was considered that an oscillator when starting its frequency has an exponential behavior until reaching its nominal frequency. The code used was based on [43] [44].

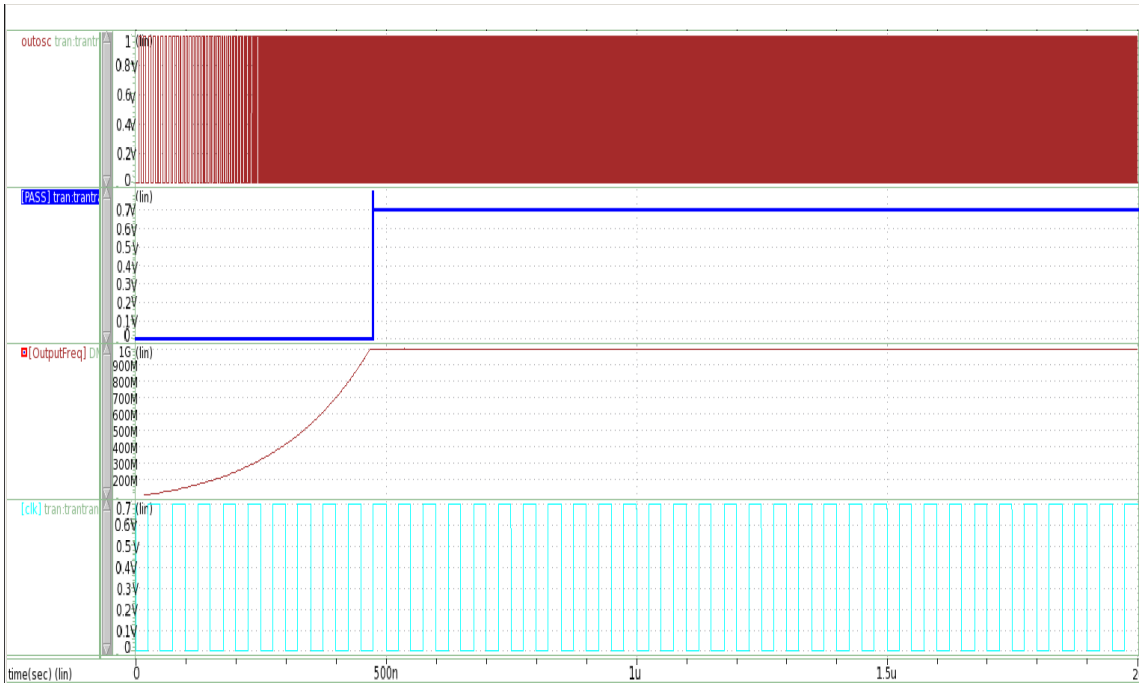

Figure 5.25: Oscillator passing the settling time test.

5.3.1 Results

In figure 5.25 we can observe a situation where the oscillator passes the settling time test, by reaching to its final frequency before the maximum allowed time. In this figure it is possible to observe the oscillator waveform which corresponds to the signal OutOsc. The expected exponential behavior of the frequency of this signal it shown in waveform OutputFreq. The signal clk is the clock signal and PASS is the signal that indicates if the test to the oscillator was successful.

Figure 5.26 displays the situation where the oscillator fails the settling time test, since the oscillator frequency settles to its final value after the maximum allowed time. In this figure it is possible to observe the oscillator waveform which corresponds to the signal outosc. The expected exponential behavior of the frequency of this signal is shown in waveform OutputFreq. The signal clk is the clock signal and FAIL is the signal that indicates that the oscillator failed the settling time test.

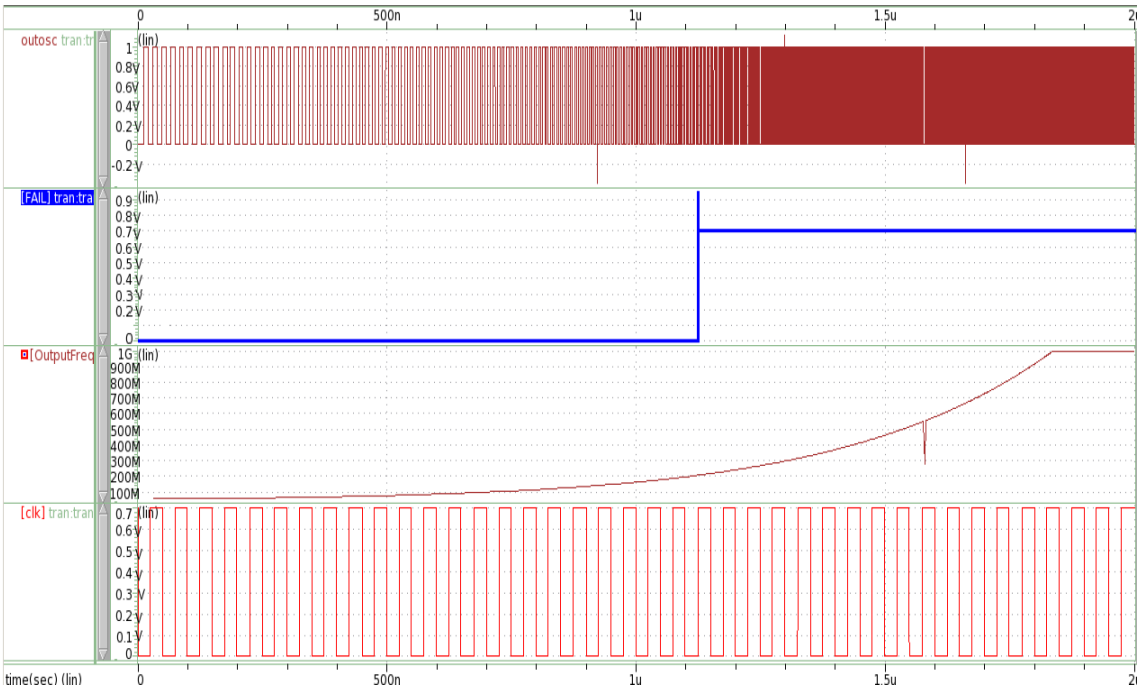

Figure 5.26: Oscillator failing the settling time test.

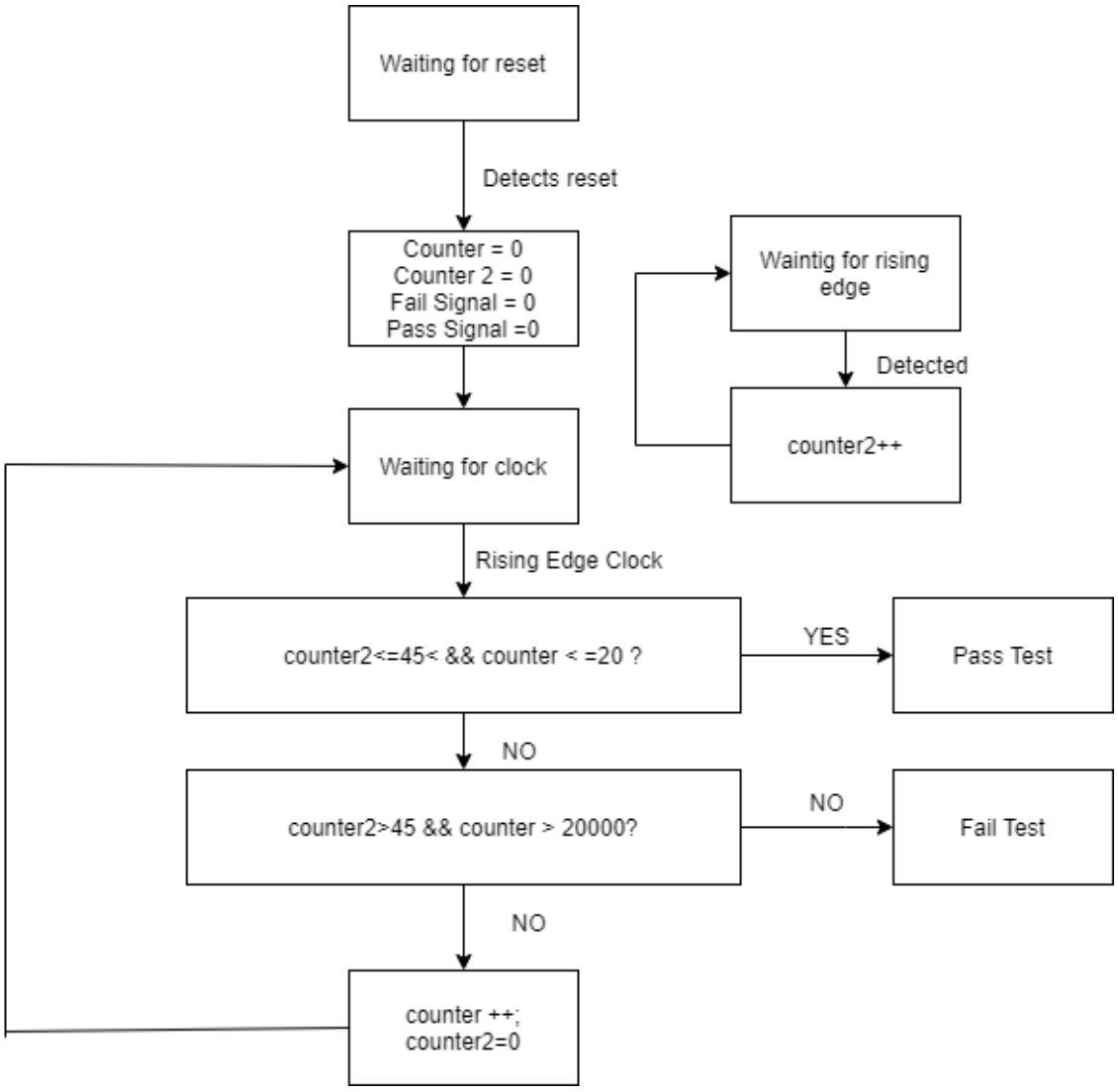

Figure 5.27: Settling time of the oscillator code.

Chapter 6

Conclusion and Future Work

6.1 Conclusions and Future Work

Testing is a critical stage of a circuit or an equipment life cycle. The consequences of sending to the market devices with defects can be life-threatening and cause high monetary losses for companies. Hence the importance of developing high-performance test systems. Even if a circuit fulfills its nominal specifications and is operating according to the design after fabrication, through its lifetime it may suffer a loss of performance and functionality, which is critical in some applications, making it fundamental to the development of test methods that take in consideration all these situations.

The inclusion of specific built-in self-test (BIST) facilities provides the ability of testing operations being carried with less test equipment and allows reducing complexity and cost associated with testing, namely when performing analog circuit tests. It allows testing the circuits periodically when operating in the field, which is important in safety-critical systems, and also allows monitoring some analog parameters in real-time.

The objective of this dissertation was to developed a set of BIST blocks that support the testing of specific parameters of two widely used analog circuits — a voltage regulator and an oscillator. The results obtained and the improvements that can be made can be summarized as follows:

- A bandgap voltage reference was developed to provide the system with voltage references that are stable regardless of the PVT conditions. This bandgap shows, in the initially established PVT conditions, an error lower than 3%. However, when submitting the circuit to 740 Monte Carlo simulations the result revealed a total error of 3,4%, in typical conditions, due to the offset of the operational amplifier. A solution for this problem could be trimming or to implemented dynamic offset techniques like auto-zeroing or chopping. Another parameter that could be improved in the bandgap voltage reference is the PSRR;

- Comparators were developed to detect over- and under-voltage conditions (OUV). Even though the simulations showed that the specified OUV conditions are detected, some of its parameters, like gain and PSRR could be improved. Especially the PSRR in some PVT

conditions, since the variation in the power supply is being amplified in the output, which could lead to false detections;

- Peak detectors were developed to detect maximum peaks of 1,4 V and minimum peaks of 0,6 V with a width of 50 ns and higher, as specified. A possible improvement in these circuits is to reduce the size of the capacitor;
- The test of the settling time of the voltage regulator complies with the specification, possible improvements can be those stated above for the comparator;
- A frequency to voltage converter (FVC) was designed to measure an oscillator's frequency drift. In typical conditions, it shows an output inferior to the expected one due to the leakage currents. Concerning the sensitivity to PVT variations, it shows a deviation of 28,14%, which makes it difficult to measure accurately the frequency drift in the desired range. Future improvement is to calibrate the FVC before starting the test of an oscillator;
- An RC filter is proposed to measure the duty-cycle of a square-wave signal. The achieved performance complies with the initial objectives and no further improvements are needed regarding this circuit;
- Concerning the detection of an oscillator's settling time, all the circuits show to be achieving the desired results. However, a future improvement should be to implement a counter that counts the rising edges of the oscillator to determine the signal frequency, due to being not possible to use digital standard cells that can not operate so high frequencies.

More future work would be finishing the digital part of the system and the interfaces between the digital part and the analog part like the SAR ADC.

All circuits were developed in Verilog-A and the simulations were carried out within the Synopsys simulation tools.

Appendix A

Verilog-A Code

A.1 Voltage Regulator Settling Time code

```
`include "constants.vams"
`include "disciplines.vams"

module settlingtime (clk, fail, in, pass, reset);
        input clk;
        input in;
        input reset;

        output pass;
        output fail;

        parameter vp=0.7;
        //The dead time is igual to enable*clockPeriod
        parameter enable = 20;
        parameter real thrs = 0.9;

        electrical clk, fail, in, pass, reset;

        integer counter,passval,failval,comp_out;


    analog begin

        @(cross(V(reset)-thrs,1)) begin
```

```
        counter =0;
        passval =0;
        failval=0;
        comp_out=0;

    end

    @(cross(V(in)-thrs,-1))
        comp_out =1;

        @(cross(V(clk) - thrs,1)) begin
                if(comp_out==1 && counter <=(20000+enable)) begin
                passval = 1;
        end
        else if(comp_out==0 && counter > (20000+enable)) begin
                failval = 1;
        end
        else
                counter = counter+1;
        end

        V(pass)<+ transition(passval?vp:0);
        V(fail)<+ transition(failval?vp:0);



  end
endmodule
```

A.2 Oscillator Settling Time code

```
module settlingtimeOsc (in,reset,clk,pass,fail);
    input in;
    input clk;
    input reset;

    output fail;
    output pass;
```

```
parameter vp=0.7;
parameter real thresh=0.5;

electrical clk, fail, pass, reset,in;

integer counter,passval,failval,counter2,enable;

analog begin

@(cross(V(reset)-thresh,1) or cross(V(clk)-thresh,1))begin

    if(V(reset))begin
            counter =0;
            passval =0;
            failval = 0;
            counter2 = 0;
            enable=1;
    end
    else begin
            if( counter2 >= 45 && counter <= 20 )begin
            passval = 1;
            enable = 0;
            end
            else if( counter2 < 45 && counter > 20 && enable) begin
            failval = 1;
            enable=0;
            end
            else begin
            counter = counter+1;
            counter2 = 0;
            end
   end
end
    @(cross(V(in)-thresh,1)) begin
    if(enable==1)
        counter2 =counter2+1;
    else
        counter2 = 0;
    end
```

```
        V(pass)<+ transition(passval?vp:0);
        V(fail)<+ transition(failval?vp:0);

    end


endmodule
```

A.3 Oscillator Code

```
`include "constants.vams"
`include "disciplines.vams"

module vco (out, in);

input in;
output out;
voltage in, out;
parameter real vmin=0;
parameter real vmax=vmin+1 from (vmin:inf);
parameter real fmin=1 from (0:inf);
parameter real fmax=2*fmin from (fmin:inf);
parameter real vl=-1;
parameter real vp=1;
parameter real tt=0.01/fmax from (0:inf);
parameter real ttol=1u/fmax from (0:0.1/fmax);
parameter real const = 0.5;
real freq, phase,Vctr,Kvco;
integer n;

analog begin

    Vctr = V(in) - vmin;
    Kvco = (fmax - fmin) / (vmax - vmin);
```

```
    freq =  Vctr*const*Kvco*exp(Vctr)+fmin;


    if (freq > fmax) freq = fmax;
    if (freq < fmin) freq = fmin;


    $bound_step(0.6/freq);


    phase = 2*`M_PI*idtmod(freq, 0.0, 1.0, -0.5);

    @(cross(phase + `M_PI/2, +1, ttol) or
    cross(phase - `M_PI/2, +1, ttol))
        n = (phase >= -`M_PI/2) && (phase < `M_PI/2);


    V(out) <+ transition(n ? vh : vl, 0, tt);
end
endmodule
```

A.4 Positive Peak Detector Reset Code

```
`include "constants.vams"
`include "disciplines.vams"

module ripple_tb (in,fail,pass,reset,clk,nreset);


        input in,clk;
        output pass,reset, nreset,fail;

        parameter vp = 0.7;
        parameter real thrs = 0.9;

        electrical fail, in, pass, reset,clk,nreset;

        integer failval,resetval,counter;
        integer passval =1;
```

```
  analog begin

        @(cross(V(in)-thrs,1)) begin
             failval=1;
        passval=0;
             resetval=1;
             counter = 0;
        end

        @(cross(V(in)-thrs,-1)) begin
            failval=0;
            passval=1;
        end

        @(cross(V(clk)-thrs,1)) begin
        if(counter==25)begin
                  resetval=0;
        end


        end

        V(pass)<+ transition(passval?vp:0,0,50p);
        V(fail)<+ transition(failval?vp:0,0,50p);
        V(reset)<+ transition(resetval?vp:0,0,50p);
        V(nreset)<+ transition(resetval?0:vp,0,50p);

  end


endmodule
```

A.5 Negative Peak Detector Reset Code

```
`include "constants.vams"
`include "disciplines.vams"

module ripple_tb_valley(in,fail,pass,reset,clk);


        input in,clk;

        output fail,pass,reset;

        parameter vp=0.7;
        parameter real thrs = 0.9;

        electrical fail, in, pass, reset;
        integer failval,resetval,counter;
        integer passval =1;



  analog begin

         @(cross(V(in)-thrs,1))begin
         failval=1;
         passval=0;
         resetval=1;
         counter=0;
         end
         @(cross(V(in)-thrs,-1))begin
         failval=0;
         passval=1;
         end
         @(cross(V(clk)-thrs,1))begin
         if(counter==25)begin
         resetval=0;
         end
```

```
    if(resetval)begin
    counter =counter+1;
    end


        end


        V(pass)<+ transition(passval?vp:0,0,50p);
        V(fail)<+ transition(failval?vp:0,0,50p);
        V(reset)<+ transition(resetval?0:vp,0,50p);



  end


endmodule
```

Appendix B

Simulations

B.0.1 Simulations Results for the Propagation Delay in PVT

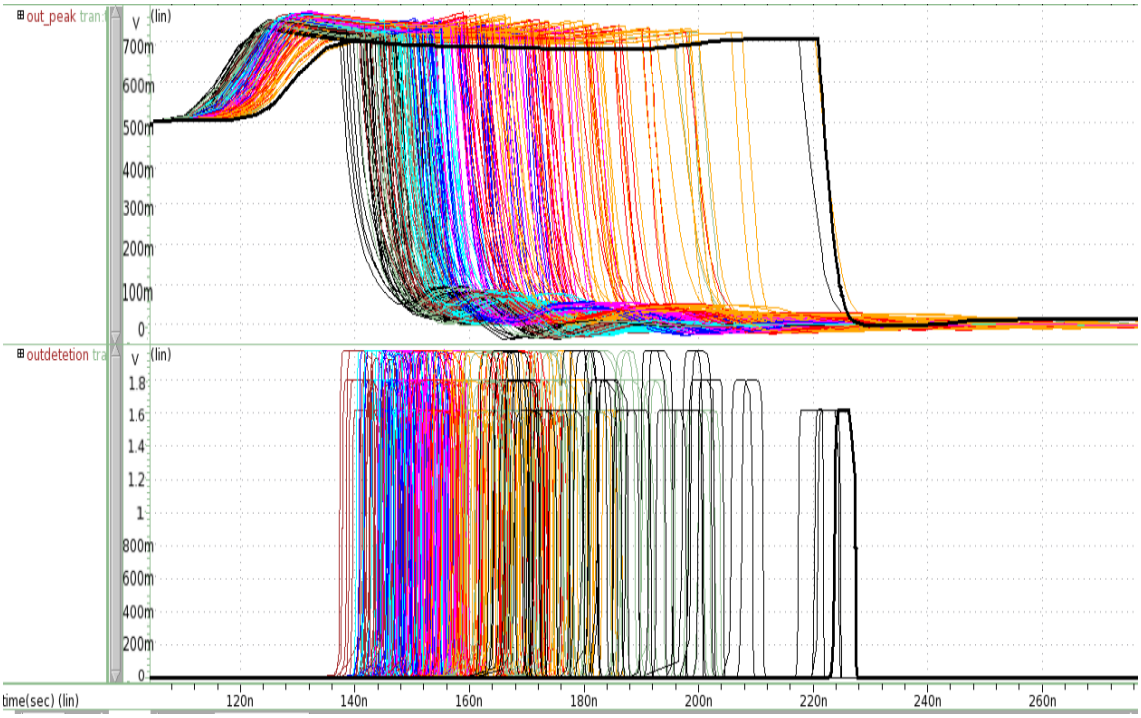

Figure B.1: Propagation delay for the positive peak detector with 50 ns in PVT.

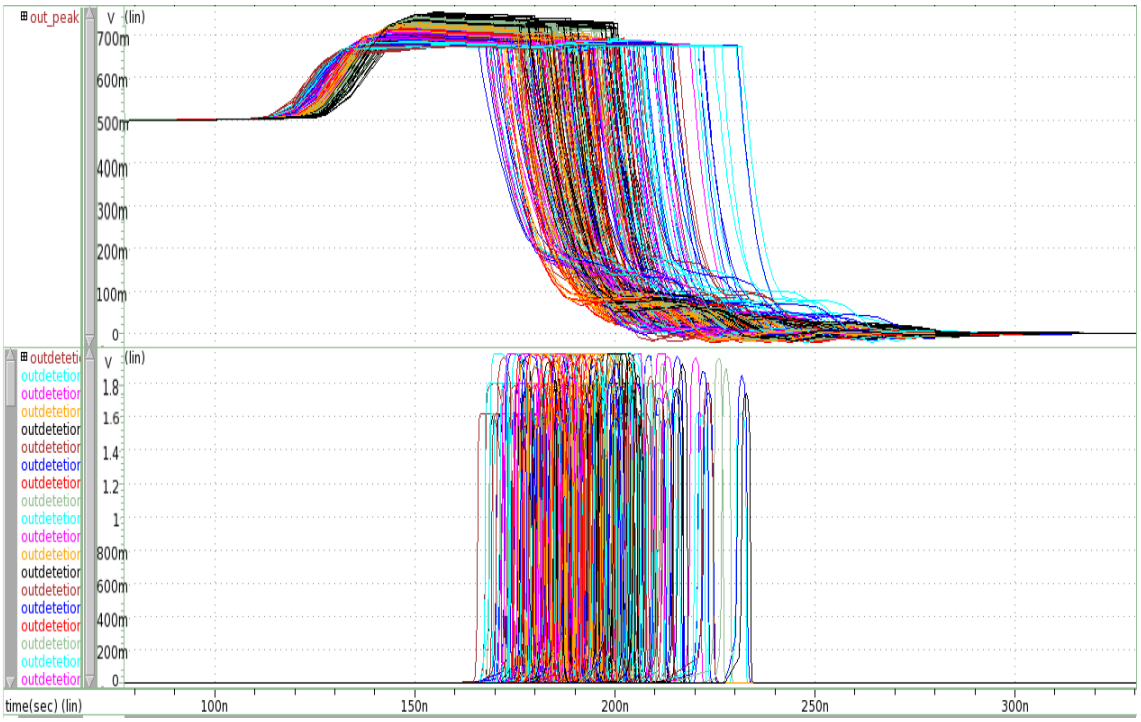

Figure B.2: Propagation delay for the positive Peak detector with 100 ns in PVT.

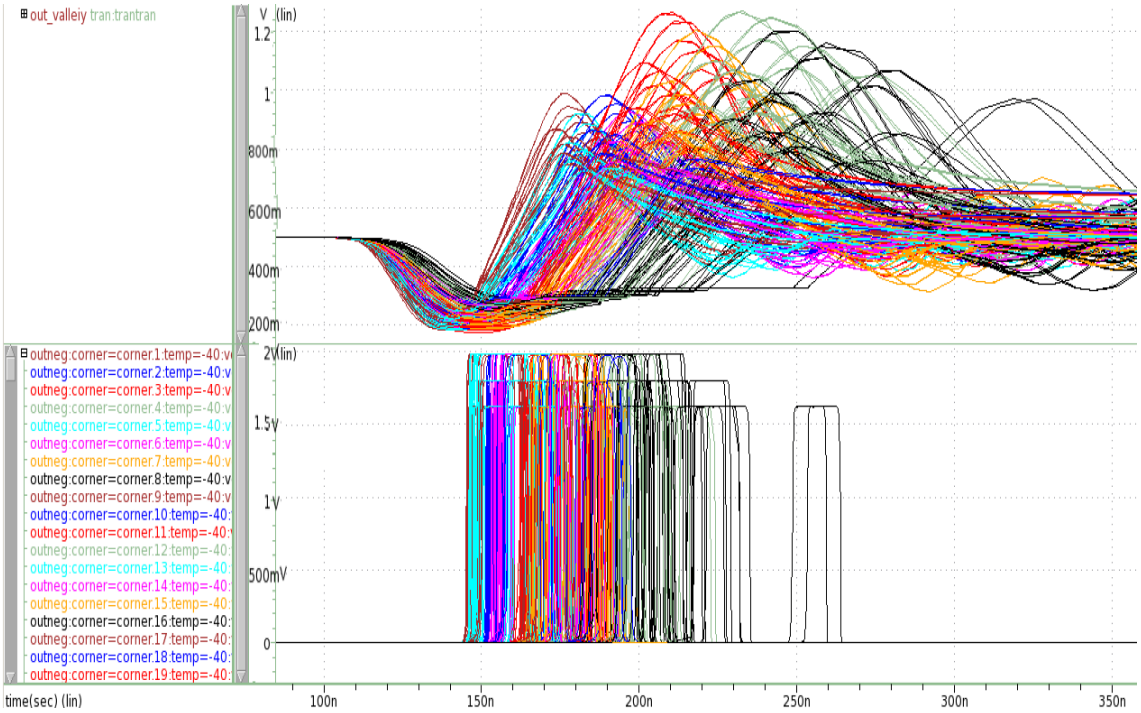

Figure B.3: Propagation delay for the negative peak detector with 50 ns in PVT.

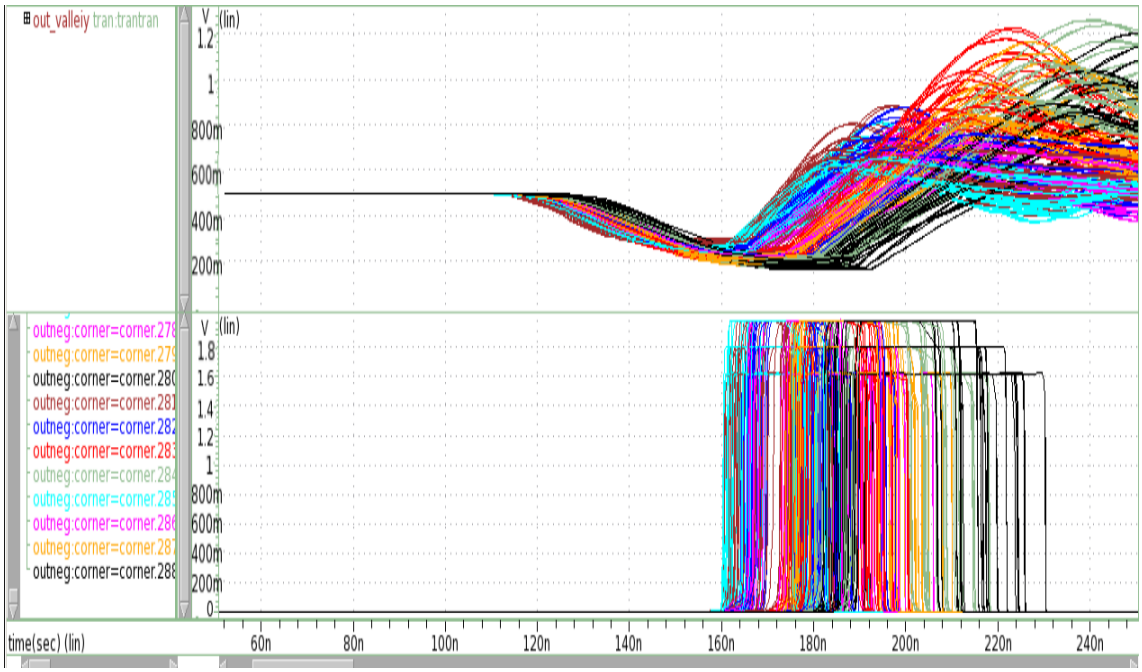

Figure B.4: propagation delay for the negative peak detector with 100 ns in PVT.

B.0.2 Simulations Results for the Propagation Delay in Monte Carlo

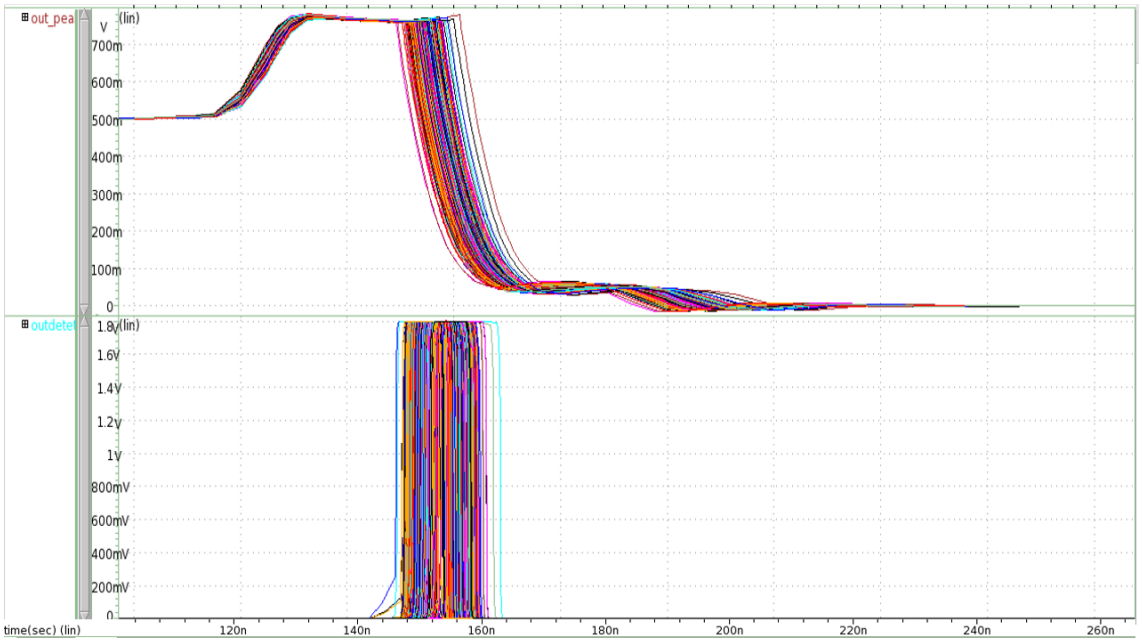

Figure B.5: Propagation delay for the positive peak detector with 50 ns in Monte Carlo.

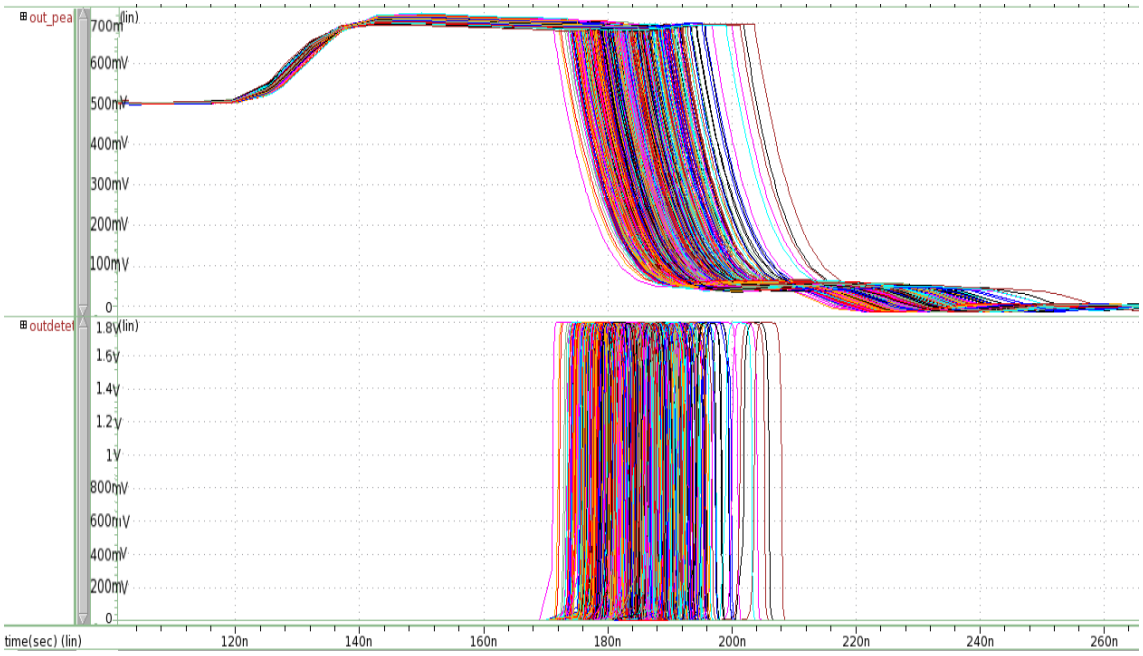

Figure B.6: Propagation delay for the positive peak detector with 100 ns in Monte Carlo.

textwidthtextwidth

Figure B.7: Propagation delay for the negative peak detector with 50 ns in Monte Carlo.

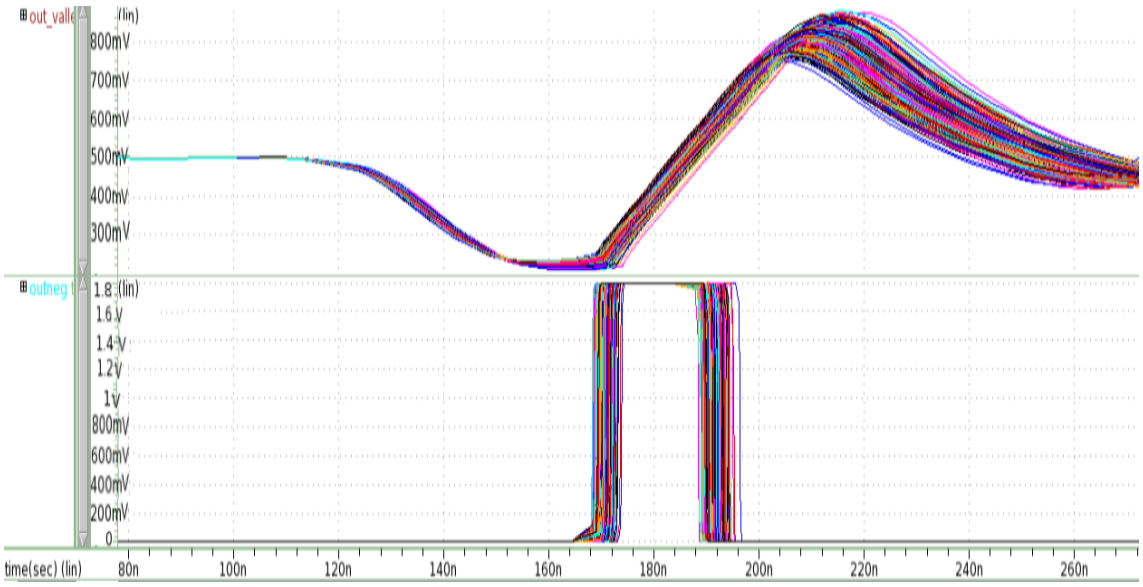

Figure B.8: Propagation delay for the negative peak detector with 100 ns in Monte Carlo.

B.0.3 Simulations Results for the Ranges of Frequencies in PVT

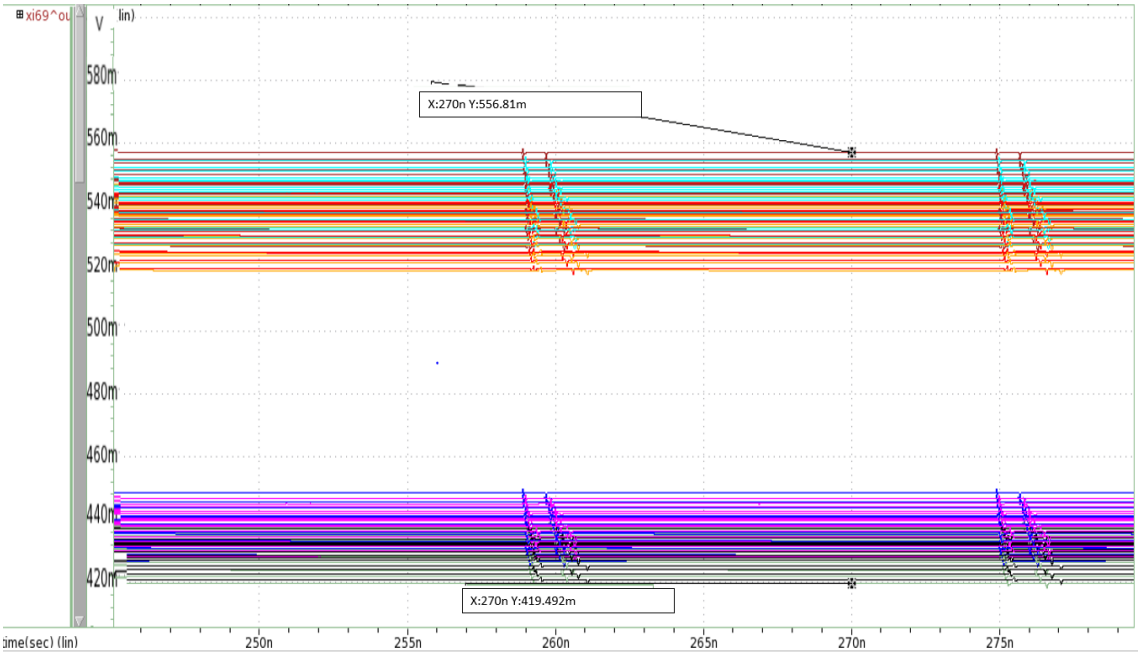

Figure B.9: Output of the FVC with 300 MHz input wave in PVT.

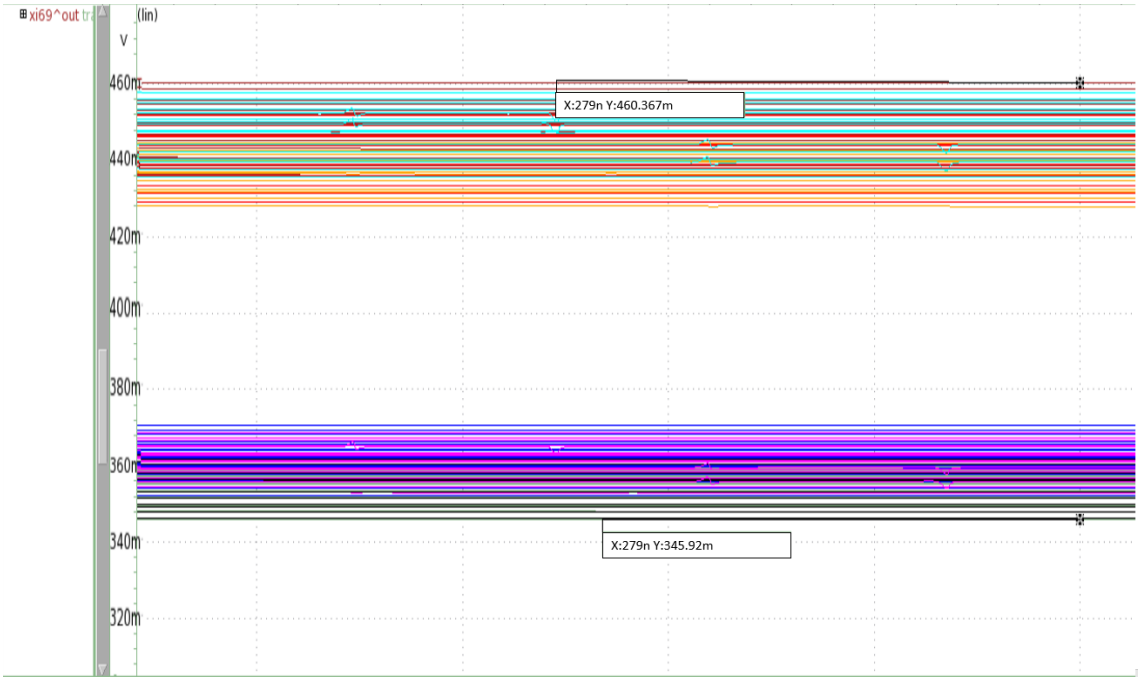

Figure B.10: Output of the FVC with 600 MHz input wave in PVT.

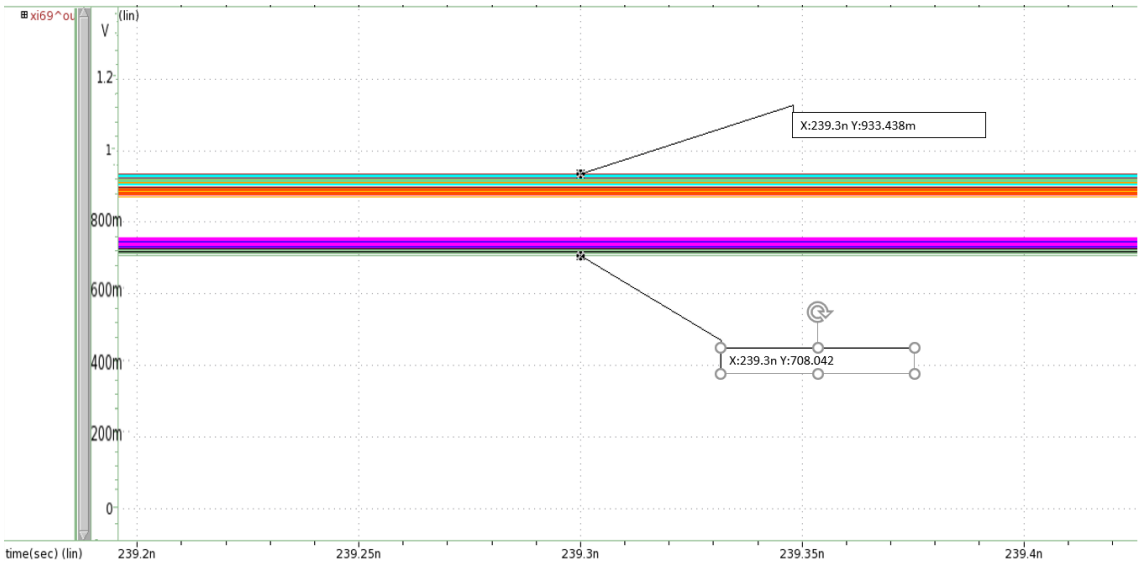

Figure B.11: Output of the FVC with 600 MHz input wave in the second range in PVT.

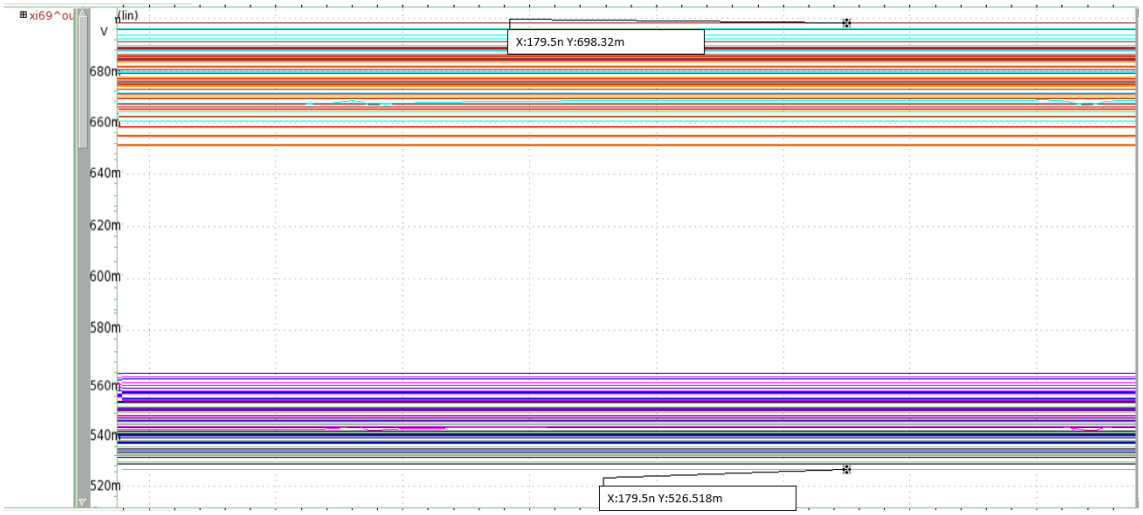

Figure B.12: Output of the FVC with 800M MHz input wave in the second range in PVT.

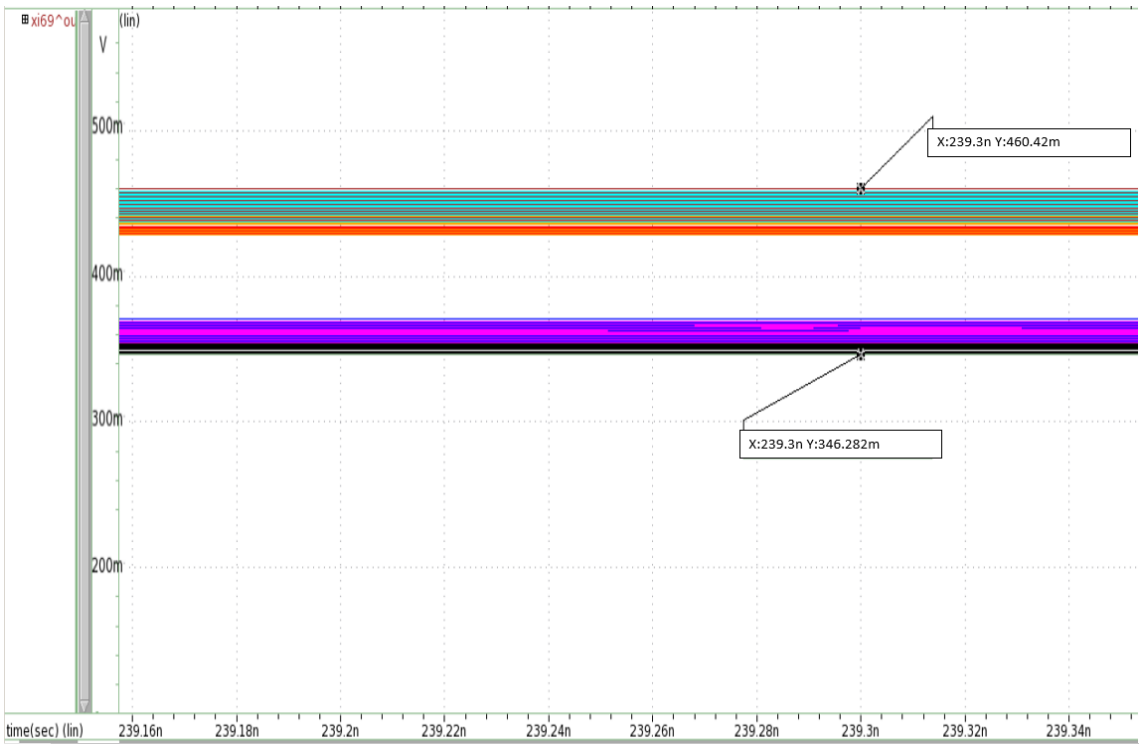

Figure B.13: Output of the FVC with 1.2 GHz input wave in the second range in PVT.

Figure B.14: Output of the FVC with 1.2 GHz input wave in the third range in PVT.

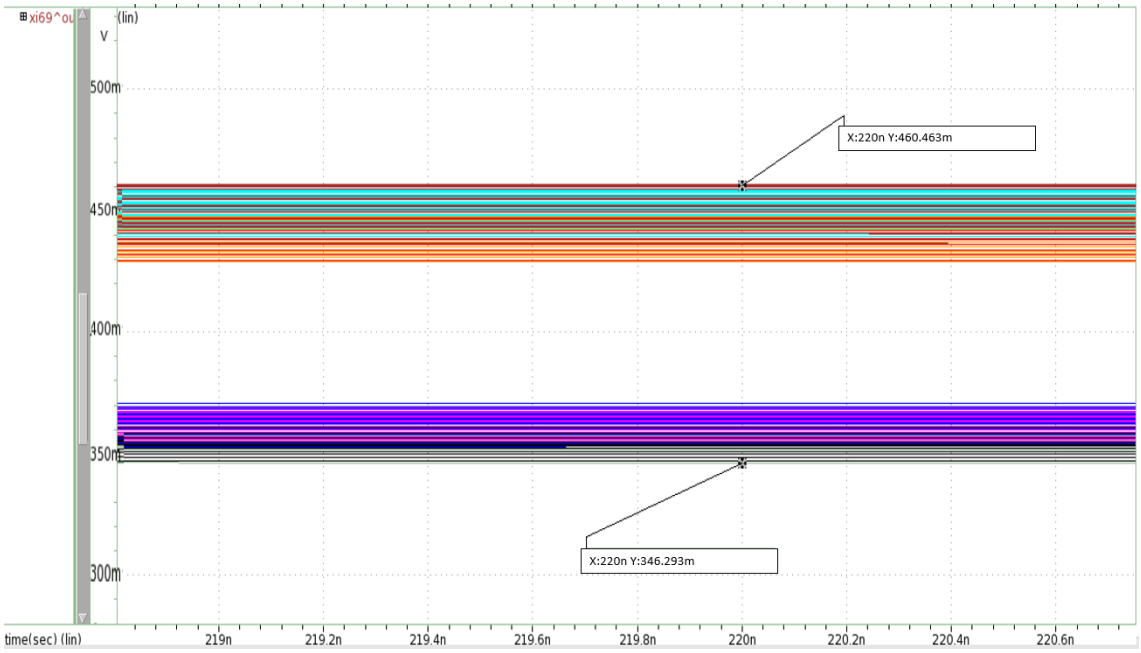

Figure B.15: Output of the FVC with 2.4 GHz input wave in the third range in PVT.

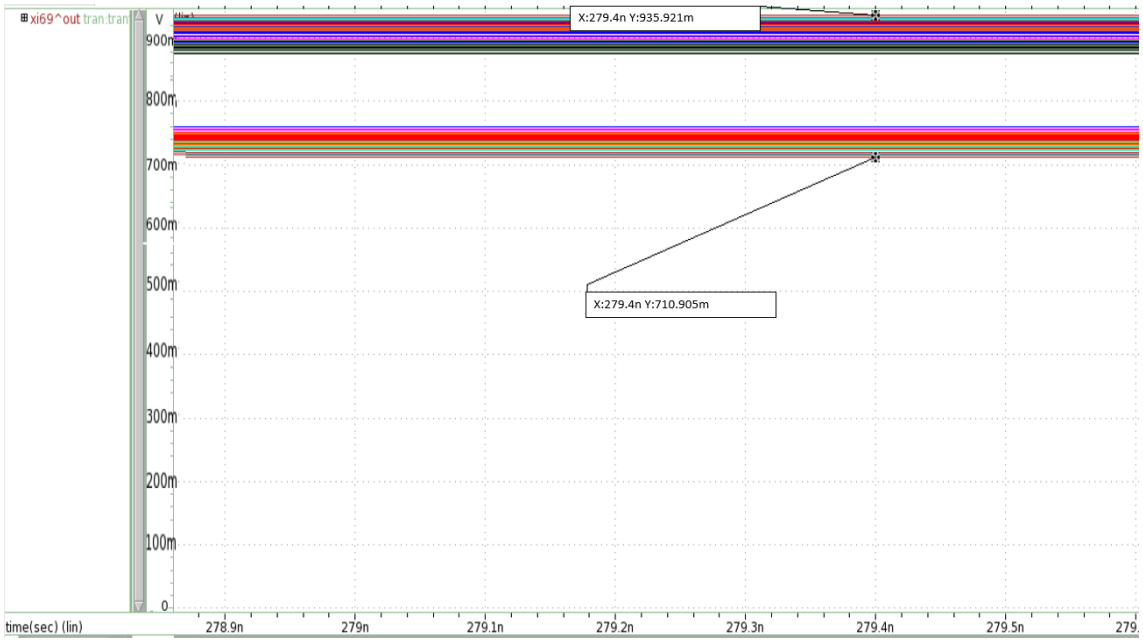

Figure B.16: Output of the FVC with 2.4 GHz input wave in the fourth range in PVT.

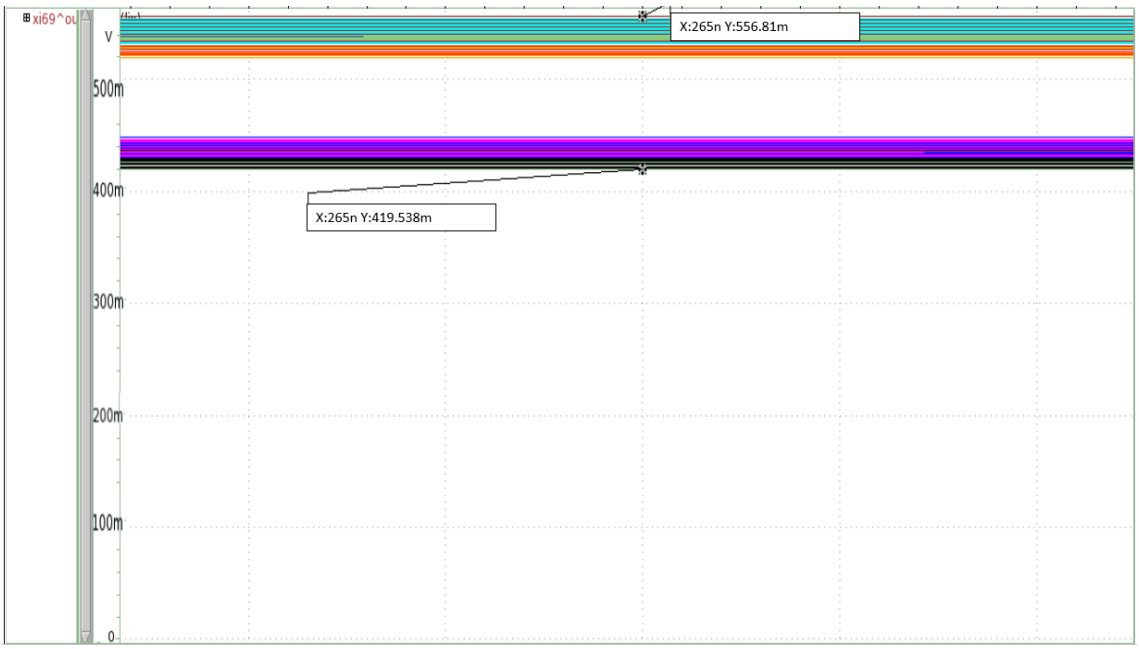

Figure B.17: Output of the FVC with 4 GHz input wave in PVT.

Appendix C

Circuits Netlist

C.1 Bandgap Voltage Reference Netlist

```
.global gnd! vdd!
*********************************************************
* Cell             : bjt
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
*********************************************************
.subckt bjt b c e
xqq0 c b e pnp2_mis m=1
.ends bjt
*********************************************************
* Cell             : buffer_3
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
*********************************************************
.subckt buffer_3 en inn inp nen out
xmn64 vdd! en vp gnd! nch_18_mac w=5.4u l=0.15u multi=1 nf=20
xmn47 s s gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
xmn48 d s e gnd! nch_18_mac w=2.16u l=1.08u multi=1 nf=8
xmn55 vp f s gnd! nch_18_mac w=0.27u l=0.27u multi=1 nf=1
xmn6 out c gnd! gnd! nch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmn37 c b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn38 b b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn54 f f gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
xmp63 vp nen vdd! vdd! pch_18_mac w=16.2u l=0.15u multi=1 nf=60
```

```
xmp62 f f vp vp pch_18_mac w=5.4u l=1.08u multi=1 nf=20
xmp13 c inp a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp10 b inn a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp7 out d vp vp pch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmp46 s d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp5 d d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp6 a d vp vp pch_18_mac w=10.26u l=1.08u multi=1 nf=38
xrr317 e gnd! gnd! rupolym_m wr=1u lr=7u multi=1
xmc69 c out cvpp nfp=2.0 l=0.4997000m w=0.070u cap=0.493971p
.ends buffer_3
********************************************************************************
* Cell             : lstb
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************************
.subckt lstb i o
vi o i dc=0
.ends lstb
********************************************************************************
* Cell             : vbandgap
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************************
.subckt vbandgap out vref_fvc vref_over vref_negpeak vref_pospeak
+vref_under
xi361 gnd! gnd! net794 bjt
xi362<1> gnd! gnd! net767 bjt
xi362<2> gnd! gnd! net767 bjt
xi362<3> gnd! gnd! net767 bjt
xi362<4> gnd! gnd! net767 bjt
xi362<5> gnd! gnd! net767 bjt
xi362<6> gnd! gnd! net767 bjt
xi362<7> gnd! gnd! net767 bjt
xi362<8> gnd! gnd! net767 bjt
xi362<9> gnd! gnd! net767 bjt
xi362<10> gnd! gnd! net767 bjt
xi362<11> gnd! gnd! net767 bjt
xi362<12> gnd! gnd! net767 bjt
```

```
xi362<13> gnd! gnd! net767 bjt
xi362<14> gnd! gnd! net767 bjt
xi362<15> gnd! gnd! net767 bjt
xi362<16> gnd! gnd! net767 bjt
xi368 vdd! net795 net794 gnd! net793 buffer_3
xrr358<1> out resbus3<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<2> resbus3<1> resbus3<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<3> resbus3<2> resbus3<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<4> resbus3<3> resbus3<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<5> resbus3<4> resbus3<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<6> resbus3<5> resbus3<6> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<7> resbus3<6> resbus3<7> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<8> resbus3<7> resbus3<8> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<9> resbus3<8> resbus3<9> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<10> resbus3<9> resbus3<10> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<11> resbus3<10> resbus3<11> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<12> resbus3<11> resbus3<12> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<13> resbus3<12> resbus3<13> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr358<14> resbus3<13> c gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<1> vref_pospeak resbus2<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<2> resbus2<1> resbus2<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<3> resbus2<2> resbus2<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<4> resbus2<3> resbus2<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<5> resbus2<4> resbus2<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<6> resbus2<5> resbus2<6> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<7> resbus2<6> resbus2<7> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<8> resbus2<7> resbus2<8> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<9> resbus2<8> resbus2<9> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<10> resbus2<9> resbus2<10> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr356<11> resbus2<10> gnd! gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<1> out resbus<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<2> resbus<1> resbus<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<3> resbus<2> resbus<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<4> resbus<3> resbus<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<5> resbus<4> resbus<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<6> resbus<5> resbus<6> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<7> resbus<6> resbus<7> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<8> resbus<7> resbus<8> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<9> resbus<8> b gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr359<1> vref_negpeak resbus4<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr359<2> resbus4<1> resbus4<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr359<3> resbus4<2> resbus4<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr359<4> resbus4<3> resbus4<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr359<5> resbus4<4> resbus4<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr359<6> resbus4<5> gnd! gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr357 c vref_negpeak gnd! rupolym_m wr=1u lr=8.4u multi=1
xrr342 net671 net767 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr307 net602 net607 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr303 net590 net602 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr300 net574 net575 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr299 out net574 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr298 net575 net576 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr293 net565 gnd! gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr292 net564 net565 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr291 net562 net564 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr290 vref_under net559 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr289 net560 net561 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr288 vref_fvc vref_under gnd! rupolym_m wr=1u lr=14u multi=1
xrr286 net561 net562 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr309 net607 net812 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr217 net469 net470 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr218 net470 net471 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr219 net467 net468 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr220 net471 net666 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr221 net666 net794 gnd! rupolym_m wr=1u lr=8.9u multi=1
xrr222 net462 net463 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr223 net468 net469 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr224 net481 net457 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr225 net480 net481 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr226 net457 net458 gnd! rupolym_m wr=1u lr=9.38u multi=1
xrr227 net458 net459 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr228 net459 net460 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr229 net461 net462 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr230 net466 net467 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr231 net465 net466 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr232 net464 net465 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr233 net460 net461 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr234 net463 net464 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr235 net474 net475 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr236 net479 net480 gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr237 net478 net479 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr198 net433 net434 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr199 net434 net435 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr249 out net432 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr201 net435 net436 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr202 net436 net437 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr203 net437 net452 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr204 net432 net433 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr206 net442 net443 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr207 net439 net440 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr208 net443 net444 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr209 net444 net445 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr210 net445 net367 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr211 net440 net441 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr212 net448 net439 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr213 net447 net448 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr214 net454 net447 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr215 net452 net453 gnd! rupolym_m wr=1u lr=9.38u multi=1
xrr216 net453 net454 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr337 net657 net663 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr372 net812 vref_over gnd! rupolym_m wr=1u lr=5.9u multi=1
xrr355 b vref_pospeak gnd! rupolym_m wr=1u lr=6u multi=1
xrr143 net366 net362 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr205 net441 net442 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr294 net577 net578 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr283 net559 net560 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr295 net579 net590 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr297 net576 net577 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr341 net663 net671 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr238 net477 net478 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr239 net485 net474 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr240 net476 net477 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr241 net475 net476 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr138 net357 net795 gnd! rupolym_m wr=1u lr=8.9u multi=1
xrr139 net358 net357 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr140 net361 net358 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr62 net795 net657 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr284 vref_over vref_fvc gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr296 net578 net579 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr144 net367 net366 gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr245 out net485 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr141 net363 net361 gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr142 net362 net363 gnd! rupolym_m wr=1u lr=9.4u multi=1
xmc376 gnd! out cvpp nfp=2.0 l=0.4997000m w=0.070u
+ cap=0.493971p
xmc375 gnd! out cvpp nfp=2.0 l=0.4997000m w=0.070u
+ cap=0.493971p
xi2 net793 out lstb
.ends vbandgap
```

C.2 UOV Detection Circuit Netlist

```
.global gnd! vdd!
.hdl 'PATH to VERILOG-A'
********************************************************
* Cell             : inv_f
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************
.subckt inv_f in out
xmp8 out in vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmn9 out in gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
.ends inv_f
********************************************************
* Cell             : buffer_3
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************
.subckt buffer_3 en inn inp nen out
xmn64 vdd! en vp gnd! nch_18_mac w=5.4u l=0.15u multi=1 nf=20
xmn47 s s gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4

xmn55 vp f s gnd! nch_18_mac w=0.27u l=0.27u multi=1 nf=1
xmn6 out c gnd! gnd! nch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmn37 c b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn38 b b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn54 f f gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
```

```
xmp63 vp nen vdd! vdd! pch_18_mac w=16.2u l=0.15u multi=1 nf=60
xmp62 f f vp vp pch_18_mac w=5.4u l=1.08u multi=1 nf=20
xmp13 c inp a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp10 b inn a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp7 out d vp vp pch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmp46 s d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp5 d d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp6 a d vp vp pch_18_mac w=10.26u l=1.08u multi=1 nf=38
xrr317 e gnd! gnd! rupolym_m wr=1u lr=7u multi=1
xmc69 c out cvpp nfp=2.0 l=0.4997000m w=0.070u  cap=0.493971p
.ends buffer_3
********************************************************************
* Cell             : comparator
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
.subckt comparator inp inn out
xi2 net21 out inv_f
xi1 net29 net21 inv_f
xi5 vdd! inn inp gnd! net29 buffer_3
.ends comparator

********************************************************************
* Cell             : regulatortb
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
xi13 vrefunder in out_under comparator
xi31 in vref out_over comparator
v22 vdd! gnd! dc='vdd'
c42 c gnd! c=10p
v21 clc gnd! dc=0 pulse ( 1.8 0 0 0 0 25n 50n )
xi20 clc fail out_under pass reset settlingtime vp=0.7 enable=20
+ thrs=0.350000
v52 reset gnd! dc=1 pwl ( 0 0 200n 1.8 300n 0 )
v82 i gnd! dc=1 pwl ( 'time1' 'v1' 'time2' 'v2' 'time3' 'v3'
+'time4' 'v4' 'time5' 'v5' 'time6' 'v6' td=252.5n )
r41 i c r=95meg
```

```
e43 out gnd! vcvs c out 1 abs=0
xi44 net142 net199 vref net145 net144 vrefunder vbandgap
xmc60 in gnd! cvpp nfp=2.0 l=0.2197000m w=0.070u
+ cap=0.217237p
xmc59 in gnd! cvpp nfp=2.0 l=0.2197000m w=0.070u
+ cap=0.217237p
xrr58<1> md b<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<2> b<1> b<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<3> b<2> b<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<4> b<3> b<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<5> b<4> b<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<6> b<5> b<6> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<7> b<6> b<7> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<8> b<7> b<8> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<9> b<8> b<9> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<10> b<9> b<10> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<11> b<10> b<11> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<12> b<11> b<12> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<13> b<12> b<13> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<14> b<13> b<14> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<15> b<14> b<15> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<16> b<15> b<16> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<17> b<16> b<17> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<18> b<17> b<18> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<19> b<18> b<19> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<20> b<19> b<20> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<21> b<20> b<21> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<22> b<21> b<22> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<23> b<22> b<23> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<24> b<23> b<24> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<25> b<24> b<25> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<26> b<25> b<26> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<27> b<26> b<27> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<28> b<27> b<28> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<29> b<28> b<29> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<30> b<29> b<30> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<31> b<30> b<31> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<32> b<31> b<32> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<33> b<32> b<33> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<34> b<33> b<34> gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr58<35> b<34> b<35> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<36> b<35> b<36> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<37> b<36> b<37> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<38> b<37> b<38> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<39> b<38> b<39> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<40> b<39> b<40> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<41> b<40> b<41> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<42> b<41> b<42> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<43> b<42> b<43> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<44> b<43> b<44> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<45> b<44> b<45> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<46> b<45> b<46> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<47> b<46> b<47> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<48> b<47> b<48> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<49> b<48> b<49> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<50> b<49> b<50> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<51> b<50> b<51> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<52> b<51> b<52> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<53> b<52> b<53> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<54> b<53> b<54> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<55> b<54> b<55> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<56> b<55> b<56> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<57> b<56> b<57> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<58> b<57> b<58> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<59> b<58> b<59> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<60> b<59> b<60> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<61> b<60> b<61> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<62> b<61> b<62> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<63> b<62> b<63> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<64> b<63> b<64> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<65> b<64> b<65> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<66> b<65> b<66> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<67> b<66> b<67> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<68> b<67> b<68> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<69> b<68> b<69> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<70> b<69> b<70> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<71> b<70> b<71> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<72> b<71> b<72> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<73> b<72> b<73> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<74> b<73> b<74> gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr58<75> b<74> b<75> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<76> b<75> b<76> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<77> b<76> b<77> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<78> b<77> b<78> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<79> b<78> b<79> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<80> b<79> b<80> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<81> b<80> b<81> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<82> b<81> b<82> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<83> b<82> b<83> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<84> b<83> b<84> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<85> b<84> b<85> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<86> b<85> b<86> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<87> b<86> b<87> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<88> b<87> b<88> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<89> b<88> b<89> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<90> b<89> b<90> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<91> b<90> b<91> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<92> b<91> b<92> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<93> b<92> b<93> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<94> b<93> b<94> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<95> b<94> b<95> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<96> b<95> b<96> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<97> b<96> b<97> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<98> b<97> b<98> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<99> b<98> b<99> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<100> b<99> b<100> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<101> b<100> b<101> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<102> b<101> b<102> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<103> b<102> b<103> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<104> b<103> b<104> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<105> b<104> b<105> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<106> b<105> b<106> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<107> b<106> b<107> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<108> b<107> b<108> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<109> b<108> b<109> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<110> b<109> b<110> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<111> b<110> b<111> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<112> b<111> b<112> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<113> b<112> b<113> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<114> b<113> b<114> gnd! rupolym_m wr=1u lr=9.4u multi=1
```

```
xrr58<115> b<114> b<115> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<116> b<115> b<116> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<117> b<116> b<117> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<118> b<117> b<118> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<119> b<118> b<119> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr58<120> b<119> in gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr138 out md gnd! rupolym_m wr=2u lr=3u multi=1
xrr136 md gnd! gnd! rupolym_m wr=2u lr=3u multi=1
xi61 out_over failover passover overv_tb vp=0.7 thrs=0.8
xi62 out_under failunder passunder underv_tb vp=0.7 thrs=0.8
```

C.3 Peak Detectors

```
.global gnd! vdd!
.hdl 'PATH TO VERILOG-A'


********************************************************************
* Cell              : buffer_3
* View              : schematic
* View Search List  : veriloga hspice hspiceD schematic symbol
* View Stop List    :
********************************************************************
.subckt buffer_3 en inn inp nen out
xmn64 vdd! en vp gnd! nch_18_mac w=5.4u l=0.15u multi=1 nf=20

xmn47 s s gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4

xmn48 d s e gnd! nch_18_mac w=2.16u l=1.08u multi=1 nf=8
xmn55 vp f s gnd! nch_18_mac w=0.27u l=0.27u multi=1 nf=1
xmn6 out c gnd! gnd! nch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmn37 c b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn38 b b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn54 f f gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
xmp63 vp nen vdd! vdd! pch_18_mac w=16.2u l=0.15u multi=1 nf=60
xmp62 f f vp vp pch_18_mac w=5.4u l=1.08u multi=1 nf=20
xmp13 c inp a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
```

```
xmp10 b inn a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp7 out d vp vp pch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmp46 s d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp5 d d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp6 a d vp vp pch_18_mac w=10.26u l=1.08u multi=1 nf=38
xrr317 e gnd! gnd! rupolym_m wr=1u lr=7u multi=1
xmc69 c out cvpp nfp=2.0 l=0.4997000m w=0.070u cap=0.493971p
.ends buffer_3

********************************************************************
* Cell             : inv_f
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
.subckt inv_f in out
xmp8 out in vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmn9 out in gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
.ends inv_f
********************************************************************
* Cell             : comparator
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
.subckt comparator inp inn out
xi2 net21 out inv_f
xi1 net29 net21 inv_f
xi5 vdd! inn inp gnd! net29 buffer_3
.ends comparator
********************************************************************
* Cell             : ripple
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List
********************************************************************
xmp271 out_valleiy rst_neg vdd! vdd! pch_18_mac w=0.27u l=0.27u
+multi=1 nf=1
xmp242 v v vdd! vdd! pch_18_mac w=0.54u l=0.27u multi=1 nf=2
xmp135 out_valleiy v vdd! vdd! pch_18_mac w=0.27u l=1.08u multi=1 nf=1
```

```
v1 vdd! gnd! dc='vdd'
xi154 net1010 net1012 vref_over vref_negpeak vref_pospeak
+vref_under vbandgap
xi205 out_peak vref_pospeak outdetetion comparator
xi131 vref_negpeak out_valleiy outneg comparator
v82 inp gnd! dc=0.5 pwl ( 'time1' 'v1' 'time2' 'v2' 'time3' 'v3'
+'time4' 'v4' 'time5' 'v5' 'time6' 'v6' 'time7' 'v7' 'time8' 'v8')
xmn254 out_valleiy out_pop_valley gnd! gnd! nch_18_mac w=0.27u
+l=0.54u multi=1 nf=1
xmn90 out_peak rst gnd! gnd! nch_18_mac w=0.27u l=0.27u
+ multi=1 nf=1
xmn291 vdd! out_pop out_peak gnd! nch_18_mac w=0.54u l=0.15u
+multi=1 nf=2
xmn245 v v net924 gnd! nch_18_mac w=0.27u l=0.54u multi=1 nf=1
xmn243 net924 net924 net916 gnd! nch_18_mac w=0.27u l=0.54u
+ multi=1 nf=1
xmn183 net916 net916 net917 gnd! nch_18_mac w=0.27u l=0.54u
+ multi=1 nf=1
xmn54 net917 net917 gnd! gnd! nch_18_mac w=0.27u l=0.54u
+ multi=1 nf=1
xi127 outdetetion failpos passpos rst clk nrst ripple_tb vp='vdd'
+thrs='(vdd/2)'
xrr138 inp in gnd! rupolym_m wr=2u lr=3u multi=1
xrr136 in gnd! gnd! rupolym_m wr=2u lr=3u multi=1
xrr258 inp in9 gnd! rupolym_m wr=2u lr=3u multi=1
xrr259 in9 gnd! gnd! rupolym_m wr=2u lr=3u multi=1
xmc299 out_peak gnd! cvpp nfp=2.0 l=0.6597000m w=0.070u
+cap=0.652105p
xmc301 vdd! out_valleiy cvpp nfp=2.0 l=0.6597000m w=0.070u
+ cap=0.652105p
xmc295 vdd! out_valleiy cvpp nfp=2.0 l=0.6597000m w=0.070u
+cap=0.652105p
xmc141 out_peak gnd! cvpp nfp=2.0 l=0.6597000m w=0.070u
+cap=0.652105p
xmc300 vdd! out_valleiy cvpp nfp=2.0 l=0.6597000m w=0.070u
+cap=0.652105p
xmc280 vdd! out_valleiy cvpp nfp=2.0 l=0.6597000m w=0.070u
+cap=0.652105p
xi167 outneg failneg passneg rst_neg clk ripple_tb_valley vp='vdd'
+ thrs='(vdd/2)'
```

```
v197 clk gnd! dc=0 pulse ( 1.8 0 0 10p 10p 24.99n 50n )
v184 net650 net651 dc=0 pulse ( 0 0 0 )
xi248 nrst out_peak in rst out_pop buffer_3
xi247 vdd! in9 out_valleiy gnd! out_pop_valley buffer_3
```

C.4 FVC Netlist

```
.global gnd! vdd!

********************************************************
* View              : schematic
* View Search List  : veriloga hspice hspiceD schematic symbol
* View Stop List    :
********************************************************
.subckt buffer_3 en inn inp nen out
xmn64 vdd! en vp gnd! nch_18_mac w=5.4u l=0.15u multi=1 nf=20
xmn47 s s gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
xmn48 d s e gnd! nch_18_mac w=2.16u l=1.08u multi=1 nf=8
xmn55 vp f s gnd! nch_18_mac w=0.27u l=0.27u multi=1 nf=1
xmn6 out c gnd! gnd! nch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmn37 c b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn38 b b gnd! gnd! nch_18_mac w=7.56u l=1.89u multi=1 nf=28
xmn54 f f gnd! gnd! nch_18_mac w=1.08u l=1.08u multi=1 nf=4
xmp63 vp nen vdd! vdd! pch_18_mac w=16.2u l=0.15u multi=1 nf=60
xmp13 c inp a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp10 b inn a a pch_18_mac w=75.6u l=1.08u multi=1 nf=280
xmp7 out d vp vp pch_18_mac w=34.02u l=0.54u multi=1 nf=126
xmp46 s d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp5 d d vp vp pch_18_mac w=5.94u l=1.08u multi=1 nf=22
xmp6 a d vp vp pch_18_mac w=10.26u l=1.08u multi=1 nf=38
xrr317 e gnd! gnd! rupolym_m wr=1u lr=7u multi=1
xmc69 c out cvpp nfp=2.0 l=0.4997000m w=0.070u cap=0.493971p
.ends buffer_3


********************************************************
* Cell              : FrequencyDivider
* View              : schematic
```

```
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************
.subckt frequencydivider in out reset
xmm9 out nout vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmm6 nout in vdd! vdd! pch_18_mac w=0.54u l=0.15u multi=1 nf=2
xmm4 net66 net64 vdd! vdd! pch_18_mac w=0.54u l=0.15u multi=1
+nf=2
xmm1 net64 nout vdd! vdd! pch_18_mac w=0.54u l=0.15u multi=1
+nf=2
xmm8 nout reset gnd! gnd! nch_18_mac w=0.27u l=0.15u multi=1
+nf=1
xmm7 nout net66 gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1
+nf=2
xmm5 net66 in gnd! gnd! nch_18_mac w=1.08u l=0.15u multi=1
+nf=4
xmm10 out nout gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1
+nf=2
xmm3 net65 nout gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1
+nf=2
xmm2 net64 in net65 gnd! nch_18_mac w=0.54u l=0.15u multi=1
+nf=2
.ends FrequencyDivider
********************************************************
* Cell             : inv_1
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************
.subckt inv_1 in out
xmp8 out in vdd! vdd! pch_18_mac w=1.62u l=0.27u multi=1 nf=6
xmn9 out in gnd! gnd! nch_18_mac w=0.54u l=0.27u multi=1 nf=2
.ends inv_1
********************************************************
* Cell             : nand_1
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************
.subckt nand_1 a b out
```

```
xmp6 out a vdd! vdd! pch_18_mac w=0.81u l=0.27u multi=1 nf=3
xmp7 out b vdd! vdd! pch_18_mac w=0.81u l=0.27u multi=1 nf=3
xmn5 net18 b gnd! gnd! nch_18_mac w=0.54u l=0.27u multi=1 nf=2
xmn4 out a net18 gnd! nch_18_mac w=0.54u l=0.27u multi=1 nf=2
.ends nand_1
********************************************************************
* Cell              : inv_30
* View              : schematic
* View Search List  : veriloga hspice hspiceD schematic symbol
* View Stop List    :
********************************************************************
.subckt inv_30 in out
xi71 net118 net117 inv_1
xi70 net117 out inv_1
xi69 net119 net118 inv_1
xi68 net120 net119 inv_1
xi67 net114 net113 inv_1
xi66 net113 net120 inv_1
xi65 net115 net114 inv_1
xi63 net111 net110 inv_1
xi64 net116 net115 inv_1
xi61 net110 net116 inv_1
xi32 net71 net70 inv_1
xi33 net70 net104 inv_1
xi37 net76 net75 inv_1
xi41 net80 net79 inv_1
xi34 net75 net74 inv_1
xi38 net77 net76 inv_1
xi58 net107 net106 inv_1
xi59 net105 net111 inv_1
xi60 net106 net105 inv_1
xi57 net103 net102 inv_1
xi55 net104 net103 inv_1
xi56 net102 net107 inv_1
xi40 net79 net78 inv_1
xi42 in net80 inv_1
xi35 net74 net73 inv_1
xi31 net72 net71 inv_1
xi39 net78 net77 inv_1
xi36 net73 net72 inv_1
```

```
.ends inv_30
********************************************************************
* Cell             : clkGn
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
.subckt clkgn in nout1 out1 out2
xi36 net137 net136 inv_1
xi37 net139 net137 inv_1
xi38 net141 net140 inv_1
xi39 net140 net139 inv_1
xi34 net133 out1 inv_1
xi35 net134 out2 inv_1
xi9 b4 net118 inv_1
xi8 net93 b3 inv_1
xi7 net117 net93 inv_1
xi6 net136 net117 inv_1
xi12 out1 nout1 inv_1
xi4 b2 net141 inv_1
xi3 net92 b1 inv_1
xi2 net116 net92 inv_1
xi1 net97 net116 inv_1
xi0 in net97 inv_1
xi11 net117 net118 net134 nand_1
xi10 net116 net141 net133 nand_1
xi32 b3 b4 inv_30
xi33 b1 b2 inv_30
.ends clkGn
********************************************************************
* Cell             : FVC
* View             : schematic
* View Search List : veriloga hspice hspiceD schematic symbol
* View Stop List   :
********************************************************************
.subckt fvc inp ns1 ns2 ns3 ns4 out reset s1 s2 s3 s4 vref_fvc
xmp121 b net658 vdd! vdd! pch_18_mac w=1.62u l=1.08u multi=1 nf=6
xmp120 b net658 vdd! vdd! pch_18_mac w=1.62u l=1.08u multi=1 nf=6
xmp119 b net658 vdd! vdd! pch_18_mac w=1.62u l=1.08u multi=1 nf=6
xmp99 inf i vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
```

```
xmp100 net658 net658 vdd! vdd! pch_18_mac w=11.88u l=1.08u multi=1 nf=44
xmp112 in int vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmp76 i inp vdd! vdd! pch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmp79 b net658 vdd! vdd! pch_18_mac w=1.62u l=1.08u multi=1 nf=6
xmp82 int ns3 freqbus<5> vdd! pch_18_mac w=8.1u l=0.15u multi=1 nf=30
xmp83 int ns2 freqbus<4> vdd! pch_18_mac w=8.1u l=0.15u multi=1 nf=30
xmp84 int ns1 freqbus<3> vdd! pch_18_mac w=8.1u l=0.15u multi=1 nf=30
xmp81 int ns4 ins5 vdd! pch_18_mac w=8.1u l=0.15u multi=1 nf=30 5u multi=1
+nf=4
xmn63 freqbus<5> s3 int gnd! nch_18_mac w=2.7u l=0.15u multi=1 nf=10
xmn62 freqbus<4> s2 int gnd! nch_18_mac w=2.7u l=0.15u multi=1 nf=10 a
xmn99 inf i gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
xmn114 net658 net613 net659 gnd! nch_18_mac w=4.32u l=1.08u multi=1 nf=16
xmn112 in int gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
xmn76 i inp gnd! gnd! nch_18_mac w=1.62u l=0.15u multi=1 nf=6
xmn60 freqbus<3> s1 int gnd! nch_18_mac w=2.7u l=0.15u multi=1 nf=10
xmn70 ins5 s4 int gnd! nch_18_mac w=2.7u l=0.15u multi=1 nf=10
xmm2 ic in gnd! gnd! nch_18_mac w=0.27u l=0.15u multi=1 nf=1
xmm3 cap1 out2 gnd! gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
xmm4 out out1 cap1 gnd! nch_18_mac w=0.54u l=0.15u multi=1 nf=2
xmm5 out nout1 out gnd! nch_18_mac w=0.27u l=0.15u multi=1 nf=1
xrr354<1> vbg resbus<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<2> resbus<1> resbus<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<3> resbus<2> resbus<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr354<4> resbus<3> gnd! gnd! rupolym_m wr=1u lr=9.4u multi=1
v80 net659 vbg dc=0
v111 b ic dc=0
xi108 vdd! vbg vref_fvc gnd! net613 buffer_3
xi31<1> inf freqbus<1> reset frequencydivider
xi31<2> freqbus<1> freqbus<2> reset frequencydivider
xi31<3> freqbus<2> freqbus<3> reset frequencydivider
xi31<4> freqbus<3> freqbus<4> reset frequencydivider
xi31<5> freqbus<4> freqbus<5> reset frequencydivider
xi31<6> freqbus<5> ins5 reset frequencydivider
xi30 in nout1 out1 out2 clkgn
xc2 gnd! out cvpp nfp=2.0 l=0.1797000m w=0.070u
+ cap=0.177704p
xc1 gnd! cap1 cvpp nfp=2.0 l=0.1797000m w=0.070u
+ cap=0.177704p
.ends FVC
```

C.5 RC Filter Netlist

```
.global gnd!
********************************************************************
* Cell                : rcfilter
* View                : schematic
* View Search List    : veriloga hspice hspiceD schematic symbol
* View Stop List      :
********************************************************************
.subckt rcfilter osc_in v_duty
xmc5 v_duty gnd! cvpp nfp=2.0 l=0.2197000m w=0.070u
+  cap=0.217237p
xrr360<1> osc_in resbus5<1> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<2> resbus5<1> resbus5<2> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<3> resbus5<2> resbus5<3> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<4> resbus5<3> resbus5<4> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<5> resbus5<4> resbus5<5> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<6> resbus5<5> resbus5<6> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<7> resbus5<6> resbus5<7> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<8> resbus5<7> resbus5<8> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<9> resbus5<8> resbus5<9> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<10> resbus5<9> resbus5<10> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<11> resbus5<10> resbus5<11> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<12> resbus5<11> resbus5<12> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<13> resbus5<12> resbus5<13> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<14> resbus5<13> resbus5<14> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<15> resbus5<14> resbus5<15> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<16> resbus5<15> resbus5<16> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<17> resbus5<16> resbus5<17> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<18> resbus5<17> resbus5<18> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<19> resbus5<18> resbus5<19> gnd! rupolym_m wr=1u lr=9.4u multi=1
xrr360<20> resbus5<19> v_duty gnd! rupolym_m wr=1u lr=9.4u multi=1
.ends rcfilter
```

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