FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Active Inductor Techniques for BW Extension

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Abstract

Advances in integrated circuit technology have been reducing costs and increasing the functionality of consumer electronics. Today's nano-meter technologies benefit from higher integration allowing for increased complexity but also higher speeds. The demand for higher speeds at lower area and cost pushes the design of integrated systems toward more self-contained circuits without the use of integrated passive components mainly due to the large area required.

There are many circuits that may require the implementation of inductors to improve their performance and thus meet the needs of today's communication systems. These inductors are increasingly being implemented active, due to the effectiveness of the integration of active inductors compared to a passive implementation.

This dissertation aims to take advantage of CMOS technology and its reduced cost to research and design active inductors and its integration in circuits. The final designed active inductor is intended to be integrated into an output driver with the ultimate goal of extending the bandwidth and consequently improve the driver's speed.

A study of different topologies is performed with the respective evaluation of their pros and cons and those configurations that demonstrate a greater potential are implemented. Taking into account the analyses carried out and the respective performance parameters, a circuit architecture is developed resulting in a novel active inductor topology. The proposed solution is evaluated and compared with other approaches, proving to be the most effective solution to fulfill the ultimate goal of extending bandwidth, thus increasing the speed of the driver.

This work is carried out in an enterprise team environment, more specifically at Synopsys - Portugal.

Resumo

O avanço tecnológico na área dos circuitos integrados tem vindo a reduzir custos e a aumentar funcionalidades da eletrónica de consumo. As tecnologias atuais, na ordem dos nanómetros, beneficiam da alta integração, na medida em que, não só suportam maior complexidade, como tambem permitem circuitos mais rápidos. A procura por maior velocidade em sistemas de baixo custo e área reduzida motiva o interesse da adoção de circuitos mais independentes, sem o uso de componentes passivos, principalmente devido à elevada área que é exigida.

Existem diversos circuitos que poderão exigir a implementação de indutores de forma a melhorarem o seu desempenho e, assim, atenderem às necessidades dos sistemas de comunicação atuais. Esses indutores estão a ser, cada vez mais, implementados de forma ativa, uma vez que, revelam ser mais eficientes principalmente em área relativamente às implementações passivas.

A presente dissertação visa ter em consideração a tecnologia CMOS e o seu custo reduzido, de forma a pesquisar e projetar indutores ativos e as respetivas implementações em circuitos integrados. O indutor ativo final tem como finalidade ser integrado num driver de saída, com o objetivo final de extensão de largura de banda e, consequentemente, melhorar a respetiva velocidade do driver.

Um estudo das diferentes topologias é efetuado, juntamente com a respetiva avaliação dos prós e contras, sendo que, as configurações que demonstram maior potencial, são posteriormente implementadas. Tendo em conta as análises realizadas assim como os respetivos parâmetros de desempenho, é desenvolvida uma configuração que resulta numa nova topologia de indutor ativo. A solução proposta é avaliada e comparada com outras abordagens, revelando ser a mais eficaz em cumprir o principal objetivo de aumentar a largura de banda, e consequentemente, melhorar a velocidade do driver.

Este trabalho é realizado em ambiente empresarial, na Synopsys - Portugal.

Acknowledgments

I would like to take this opportunity to express my sincere gratitude to my parents and my brother for all the support during this long journey. My parents always made a great effort to afford my education and from an early age, they taught me the concept of working hard to achieve my goals. For all that, I am very grateful.

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João Pedro Santos

"O que dá o verdadeiro sentido ao encontro é a busca,
e é preciso andar muito para se alcançar o que está perto"

José Saramago

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Abbreviations, Acronyms and Symbols

AI	Active Inductor
BW	Bandwidth
CMOS	Complementary metal-oxide-semiconductor
CML	Current Mode Logic
CTLE	Continuous-Time Linear Equalizer
I/O	Input/Output
IC	Integrated Circuit
LNA	Low-Noise Amplifier
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-type metal-oxide-semiconductor
PMOS	P-type metal-oxide-semiconductor
PVT	Process Voltage Temperature
VLSI	Very-Large-Scale Integration
RF	Radio Frequency

dB	decibel
Hz	Hertz
gds	Drain to source transconductance
gm	Transconductance
V_{th}	Threshold voltage

Chapter 1

Introduction

1.1 Context

The fact that silicon integrated circuit technology is scalable was observed and described in 1965 by Intel founder Gordon Moore [7]. This observation, known as Moore's Law, predicted that the number of devices would double every 18 to 24 months. Through a period of 50 years, the exponential growth of Moore's Law has continued, though with several bumps and turns along the way [8]. The technological evolution that occurred during this time resulted in the integration of large numbers of tiny MOS transistors into a small chip.

Advances in integrated circuit technology (IC) have been reducing costs and increasing functionality. In other words, the cost per transistor and the switching power per transistor has been reduced, while the memory capacity and speed have been improved, following the Dennard's Scaling Law [9], which is a corollary of Moore's law. It states, roughly, that as transistors shrink, they become faster, consume less power, and are cheaper to manufacture.

Nowadays, an increasing number of people are questioning whether the pace of the semiconductor industry is slowing down or not and if it is still in line with what Moore predicted [10, 11]. The truth is that, although the transistors have become smaller, the passive devices used for analog circuits have not scaled at the same pace.

In modern-day communications systems consisting of multiple integrated circuits, high-bandwidth communications between these ICs is one of the most critical concerns regarding the overall system performance. There are many circuits such as low-noise amplifiers (LNA), continuous-time linear equalizers (CTLE), current mode logic (CML) buffers, voltage mode drivers that may require the implementation of inductors to enhance its performance in today's era demand for speed.

While it is possible to shrink the digital circuitry, the same is not true for analog circuits when they require the use of passive devices such as inductors. Since it is economically viable to manufacture an inductor on the chip, the decision to choose the type of inductor to be applied has a significant impact when it comes to the time to integrate it.

1.2 Problem and Motivation

Demand for higher speeds at lower area and cost system pushes toward more self-contained circuits without the use of integrated passive components due to intrinsic constraints. These limitations include a low-quality factor, a low self-resonant frequency, a small and non-tunable inductance, and the need for a large silicon area.

In contrast, inductors synthesized using active devices, known as active inductors, guarantee large and tunable inductances and quality-factors, high self-resonant frequencies, and negligible silicon area consumption compared with that of their spiral counterparts [4].

Therefore, an active inductor solution ensures higher effectiveness compared to a passive implementation, meeting today's needs, pointing to the potential of this dissertation.

1.3 Objectives

This thesis aims to take advantage of CMOS technology and its reduced cost to research and design several active inductor solutions and its integration in circuits. A study of the different topologies/techniques will be performed with the respective evaluation of their pros and cons. Based on these, a circuit architecture will be proposed, developed and integrated within a block circuit with proper validation of the circuit performance parameters.

The designed active inductor topology will be integrated into an output driver with the ultimate goal of extending the bandwidth and consequently improve the driver's speed.

Additionally, the active inductor must guarantee impedance matching, which is required between channels and high-speed circuits to minimize signal reflection at their interfaces. Considering the general form of the voltage reflection coefficient, Γ, which is given by Eq.1.1, for a wave moving from medium 1 to medium 2, in a typical system, the magnitude of the reflection coefficient is a number between zero and one. When the impedance of medium 1, Z_1, is equal to the impedance of medium 2, Z_2, the numerator is zero. Thus, the match is perfect, and there is no reflection. In the case of the reflection coefficient being different from zero, there is a mismatch that results in return loss. To avoid this undesirable situation, the active inductor must have an equivalent impedance accordingly to the impedance of the cable, that in most wired serial protocols is 50 Ω.

$$\Gamma = \frac{Z_2 - Z_1}{Z_1 + Z_2} \tag{1.1}$$

This thesis is based on 28nm technology. Due to confidentiality agreements in place, details on the technology used including device characteristics and biasing voltages are not provided.

1.4 Document Structure

This document presents the following structure:

- Chapter 2 [Background] - Provides a theoretical background regarding several methods for bandwidth extension, implementation of on-chip inductors, a performance analysis of active and passive inductors as well as an introduction to shunt peaking implementations using active inductors. All of these topics are covered in this chapter, in order to familiarize the reader with some of the concepts that are involved in the work carried out.
- Chapter 3 [Shunt peaking implementation] - Presents a detailed analysis to the shunt peaking implementations using active inductors mentioned in the previous chapter. For the topologies which show a greater potential as a possible solutions, this chapter also covers their pratical implementation as well as the comparation between the theoretical analyses and the simulations results.
- Chapter 4 [Simple AI] - Explores the results obtained in chapter 3 to reach a final active inductor design. A novel approach for the simple active inductor topology is presented and it is integrated and simulated. The final of the chapter demonstrates the results of the proposed solution, evaluating and comparing them with other approaches.
- Chapter 5 [Conclusions and Future Work] - Presents the conclusion of this dissertation, discussing the main out-comes obtained, regarding the work developed along with proposals for future improvement of the proposed active inductor topology.

Chapter 2

Background

2.1 Introduction

This chapter covers topics considered relevant to understanding the problems presented in Chapter 1. It is divided into the following sections:

- Methods for bandwidth enhancement - A few methods for bandwidth enhancement are presented with emphasis on the shunt peaking method
- Implementation of on-chip inductors - A brief summary of the implementation of passive and active on-chip inductors is presented
- Performance analysis of active and passive inductors - A detailed comparison between the active and passive inductors is performed based on several performance criteria
- Shunt peaking active inductor implementations - A brief summary of the main active inductor approaches implementing the shunt peaking technique

2.2 Methods for bandwidth enhancement

Nowadays, bandwidth is of critical concern in wired serial communications with protocols reaching the tens of gigabit per second (Gbps), for example USB4 operates at 20Gbps and PCiE5.0 at 32Gbps.

Many methods have been proposed in the past for bandwidth enhancement. This section covers some of the most relevant: capacitive compensation technique, distributed amplification technique, and inductor shunt peaking technique.

2.2.1 Capacitive compensation technique

This bandwidth-enhancing technique is presented in [1] using a simple CR network driven by a source signal source V_s with an internal resistance R_s (Fig. 2.1). The capacitance C and resistance

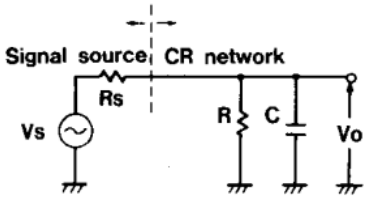


Figure 2.1: Simple CR network, reprinted from [1]

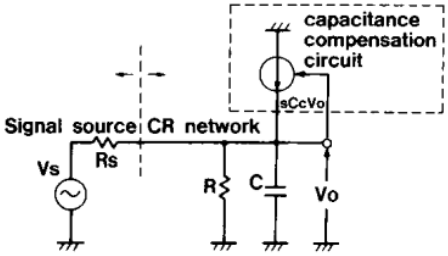


Figure 2.2: CR network with capacitance compensation circuit, reprinted from [1]

R, corresponds to the capacitance and to the input or output impedance, at a certain node in a circuit, respectively. In this case the 3-dB bandwidth f_{3dBo} is expressed by Eq. 2.1.

$$f_{3dBo} = \frac{1}{2\pi C(R//R_s)} \tag{2.1}$$

Eq. 2.1 suggests that the pole resulting from C, R, and R_s limits the bandwidth. It is possible to achieve bandwidth improvement by reducing R or C. A small R, however, could result in gain degradation at lower frequencies. In contrast, a smaller C increases the bandwidth without degrading the low-frequency voltage gain. A new circuit technique to reduce the parasitic junction capacitance is represented in Fig. 2.2 where the part enclosed by the dashed line is a capacitance compensation circuit. It detects the voltage V_0 across the capacitance C and generates a compensation current that charges or discharges the capacitance. This way, both the bandwidth and the gain-bandwidth product are enhanced.

This technique can also compensate for both poles at the input and output nodes. Although [1] suggests a technique for canceling undesired capacitors, frequency limitation of the active compensating network does not allow exact cancellation so the maximum bandwidth obtained is less than 1GHz.

2.2.2 Distributed amplification

This is another approach to improve the bandwidth and focus on minimizing the effect of the large shunt capacitance at critical nodes. The key idea behind this method is to break the large shunt capacitor into several smaller shunt capacitors and separate them with inductors. As a result, the large shunt capacitor is replaced with a distributed LC network or a transmission line.

Fig. 2.3 shows an example of a distributed amplifier architecture based on lumped-element artificial transmission lines, where C_g and C_p are capacitances at the input and output of each active

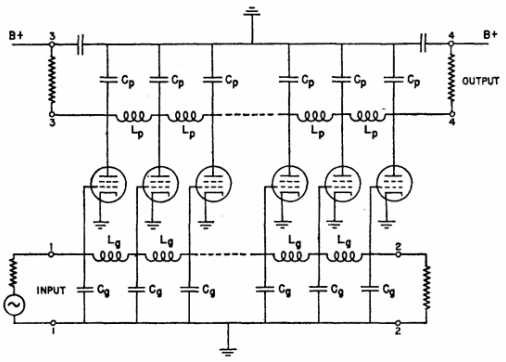


Figure 2.3: The distributed amplifier based on lumped-element artificial transmission lines, reprinted from [2]

device, while L_g and L_p denote the inductance of the input and output line sections, respectively. The bandwidth of the distributed amplifier is limited by the cut-off frequency of the transmission lines. The wave propagating through the lumped-element line experiences significant attenuation beyond the cut-off frequency. In order to achieve high bandwidth, small active devices should be used, but, this lowers the gain of the distributed amplifier. As the ratio L/C determines the characteristic impedance of the lines, inductance L cannot be made arbitrarily small to achieve higher bandwidth. Thus, there is a trade-off between gain and bandwidth of the distributed amplifier [12].

Despite the bandwidth extension, the integration of distributed amplifiers consume large area and high power and are difficult to design owing to delay line losses that necessitate extensive modeling and electromagnetic simulation [13].

2.2.3 Shunt peaking

Considering the simple common source amplifier illustrated in Fig. 2.4 (a), by neglecting the intrinsic parasitics of the transistor, the bandwidth is determined by a single dominant pole, which is determined by the output load resistance R and the load capacitance C. The capacitance $C = C_1 + C_2$, represents all the loading on the output node, including that of a subsequent stage while the effective load resistance at that node is represented by resistance R.

The introduction of an inductance L in series with the load resistance, represented in Fig. 2.4 (b), provides an impedance component that increases with frequency, which compensates the decreasing impedance of the capacitance, leaving a net impedance that remains roughly constant over a wider frequency range than that of an RC network. This technique, called shunt peaking, improves the bandwidth of the amplifier by transforming the frequency response from that of a single pole to one with two poles and a zero (Eq. 2.2).

$$Z(s) = \left(\frac{1}{sC}\right) \;//\; (R+sL) = \frac{R+sL}{1+sRC+s^2LC} \tag{2.2}$$

The frequency response of this shunt peaked amplifier is characterized by the ratio of the L/R and RC time constants. This ratio can be denoted by m so that $L = mR^2C$. The problem, then, is to

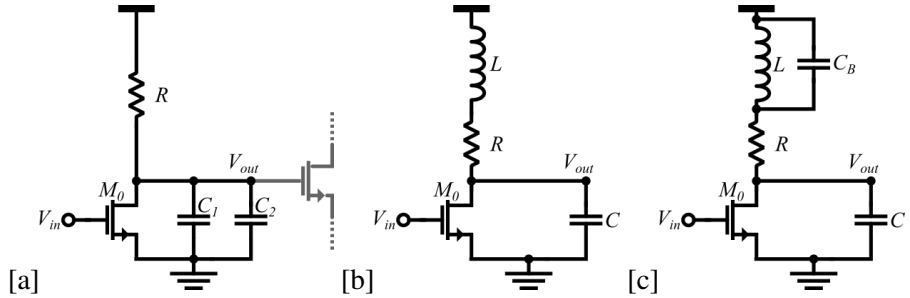


Figure 2.4: (a) Simple common source amplifier (b) Common source amplifier with shunt peaking (c) Common source amplifier with bridged-shunt peaking

choose a value of m that leads to some desired behavior, in this case, maximizing the bandwidth. This maximum occurs at a value of $m = \sqrt{2}$, which extends the bandwidth to a value of about 1.85 times as large as the uncompensated bandwidth [14, 15, 16]. This extension comes with a 1.5dB of peaking. A maximally flat gain is achieved for $m = 1 + \sqrt{2}$ but bandwidth is reduced to 1.72.

2.2.3.1 Bridged-shunt-peaking

Despite the increased impedance of the inductor contribute to the bandwidth improvement, it also leads to peaking in the response. Since there are applications where the presence of peaking is a concern, techniques to eliminate peaking with maximum bandwidth are desired. This can be achieved by adding in shunt with the inductor a capacitor, shown in Fig. 2.4 (c), that should be large enough to negate peaking but small enough to not significantly alter the gain response. Compared to the common source amplifier with shunt peaking (Fig. 2.4 (b)), this new approach achieves approximately the same maximum bandwidth (1.85 times as large as the uncompensated bandwidth), but this time, with a flat gain response.

2.2.3.2 Bridged-shunt-series-peaking

So far, bandwidth has almost doubled while a flat response has been guaranteed, however, it is possible to do better still by employing a two-port network between amplifier and load. An inductor is inserted to separate the total load capacitance into two constituent components. The overall result is a bridged-shunt-series peaking, Fig. 2.5 (a). Without L_2, the transistor charges C (where $C = C_1 + C_2$), but with L_2 only C_1 is charged initially because L_2 delays current flow to the rest of the network. Taking into account some specific values combinations for the components, this approach can potentially achieve bandwidth improvements situated in the range of [3.5 to 4] times larger with no gain-peaking. However, such precise component values are difficult to realize due to distributed parasitic effects and process, voltage, and temperature (PVT) variations making difficult to obtain values near to 4 times more bandwidth [13].

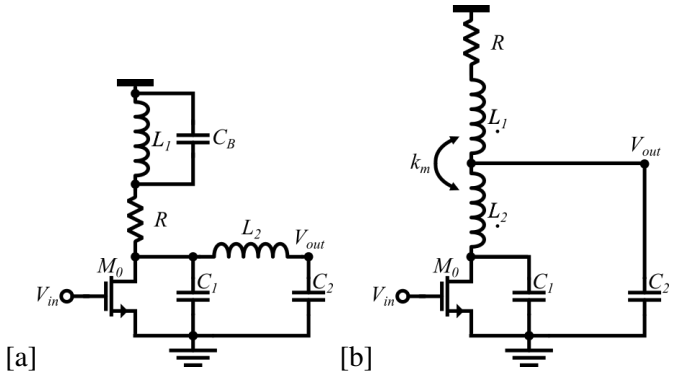


Figure 2.5: (a) Common source amplifier with bridged-shunt-series peaking and drain parasitic capacitance (b) Common source amplifier with asymmetric T-coil peaking and drain capacitance

2.2.3.3 Asymmetric T-Coil peaking

As the load capacitance increases, the capacitive-splitting action of L_2 and the bridging action of C_B become ineffective in achieving a large bandwidth. The magnetic coupling action of a transformer is used as a solution to the mentioned problem. In an asymmetric T-coil-peaked amplifier, Fig. 2.5 (b), the coils are wound to achieve a negative mutual inductance. Similarly to bridged-shunt-series peaking, the secondary inductor L_2 facilitates capacitive splitting so that the initial charging flows only to C_1. Next, the current begins to flow in L_2, which results in a proportional amount of current to flow to C_2. The negative magnetic coupling allows for an initial boost in the current flow to the load capacitance C_2 because the capacitor is effectively connected in series with the negative mutual inductance (-M) element of the T-coil. Improvements in the range of [4 to 5.5] are obtained in [13] using T-Coil peaking although non-peaking is again difficult to implement for the reasons mentioned in 2.2.3.2.

This method is implemented in [16] as well, achieving a bandwidth improvement of 3.23 times, which is considered sub-optimal since finding the layout geometry that yields the best performance is challenging, as the choice of L_1, L_2 and k_m is constrained by layout feasibility and the resulting parasitics. The coupling constant k_m (represented in Fig. 2.5 (b)) is related to the mutual inductance M as $k_m = M/\sqrt{L_1 L_2}$.

A further improvement is possible and it is suggested in [14]. This adjustment consists in adding a small bridging capacitance across the inductors to create a parallel resonance (Fig. 2.6). The increased circulating currents associated with the resonance help to push the bandwidth out even further. Applying these conditions, [14] indicates a theoretical maximum of 2.83 times more bandwidth.

2.3 Implementation of on-chip inductors

What nearly all the approaches to bandwidth improvement have in common is the use of an inductor, which has a significant impact when it comes to the time to integrate it on the chip. The cost increases proportionately with the area so it is desired that the inductor occupies the less area

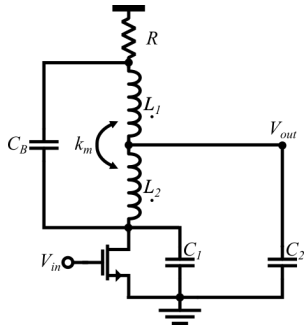


Figure 2.6: Amplifier with T-Coil bandwidth enhancement

possible. But, the integration of the inductor has to take into account more performance factors that are crucial for the proper functioning of the entire system.

Thus, the need arises to study what type of inductors should be implemented in an approach to increase bandwidth, taking into account their characteristics. Traditionally, passive inductors are implemented as off-chip discrete components. The need for off-chip communications using passive components drastically limits the bandwidth, reduces the reliability, and increases the overall system's cost. Since the early 1990s, a significant effort has been made to fabricate inductors on a silicon substrate such that an entire wireless transceiver could be integrated on a single substrate monolithically. In the meantime, the need for a large silicon area to fabricate spiral inductors has also contributed to intensive research on the design of inductors using active devices, aiming to improve the overall performance while minimizing the silicon consumption and subsequently the fabrication cost [4]. In this section, a brief summary of the implementation of passive and active on-chip inductors will be presented.

2.3.1 Passive inductor

Passive inductors are realized on-chip by laying out the metal trace on silicon using one or more interconnects in different ways. The most popular planar inductor topology is the square spiral [17]. Owing to the mutual coupling between every two turns, spirals exhibit a higher inductance than a straight line having the same length [3]. A simple two-dimensional square spiral is fully specified by five quantities (Fig. 2.7): the outer diameter, D_{out}, the inner diameter, D_{in}, the line width, W, the line spacing, S, and the number of turns, N.

2.3.2 Active inductor

A much more compact alternative to running inductors on the chip to improve bandwidth is to use active inductors as they are possible to implement in standard digital CMOS processes, which consist of active networks composed mainly of MOS. transistors.

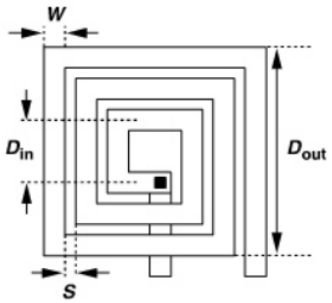


Figure 2.7: Spiral inductor, reprinted from [3]

2.3.2.1 Gyrator-C

The Gyrator-C is an example of an implementation of CMOS active inductors. A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, as illustrated in Fig.2.8 (a), the configuration is called the gyrator-C network. A gyrator-C network is considered as lossless when both the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are constant [4]. The inductance looking into port 2 is given by Eq.A.27.

$$L = \frac{C}{G_{m1}G_{m2}} \tag{2.3}$$

Therefore, Gyrator-C networks can be used to synthesize inductors. These synthesized inductors are called gyrator-C active inductors.

When either the input or the output impedances of the transconductors of gyrator-C networks are finite, the synthesized inductors are no longer lossless, as represented in Fig.2.8 (b) where G_{o1} and G_{o2} denote the total conductances at nodes 1 and 2, respectively.

2.4 Performance analysis of active and passive inductors

Now that there is an idea of how to increase the bandwidth and how to implement the inductors, the focus now is to know what type of inductors to implement taking into account their characteristics. In this section a detailed comparison between the active and passive inductors has been performed regarding several performance criteria such as:

- Quality Factor
- Silicon Area Consumption
- Self-Resonant Frequency
- Power Consumption
- Linearity

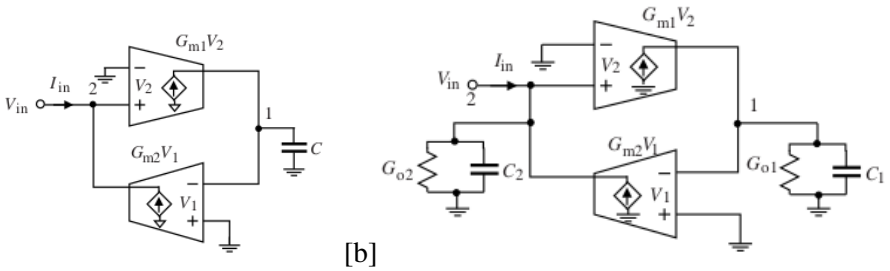


Figure 2.8: (a) Single-ended gyrator-C active inductor (b) Lossy single-ended gyrator-C active inductors (reprinted from [4])

- Noise
- Frequency Range
- Inductance Tunability

The performed comparison establishes important guidelines for choosing which type of inductor to integrate, according to specific applications.

2.4.1 Quality Factor

In RF circuit design, consideration of the total energy stored in the component as well as of the total loss is relevant [18]. As a result, the conventional definition of Q, is the ratio of the stored to the dissipated total energy in the component, so the related quality factor can simply be calculated as Eq.2.4, with z being the impedance of the inductor.

$$Q = \frac{im(z)}{Re(z)} \tag{2.4}$$

Taking into account this ratio, the quality factor of spiral inductor, can be represented by Eq. 2.5 [19], which is the ratio of the energy stored in the inductor to its energy dissipated in one oscillation cycle.

$$Q = 2\pi \frac{energy\ stored}{energy\ dissipated\ in\ one\ oscillation\ cycle} \tag{2.5}$$

The energy dissipated is directly related to the loss mechanisms of inductors, which basically, consists of various resistances within or around the structure that carries current when the inductor does. These loss mechanisms could result from several events [3] such as metal resistance, skin effect and capacitive coupling to substrate:

- **Metal Resistance** - The metal forming an inductor exhibits an intrinsic resistance.
- **Skin Effect and Eddy currents** - At high frequencies, the current through a conductor prefers to flow at the surface - skin effect - causing a nonuniformity in the current. At the same time, the magnetically induced eddy currents will also contribute to non-uniform

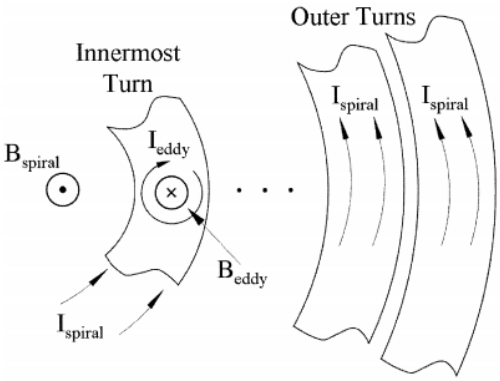


Figure 2.9: Formation of conductor eddy currents, reprinted from [5]

behavior. This way, in passive inductors, the proximity of adjacent turns results in a complex current distribution.

As an example, a circular inductor is shown in Fig.2.9. This inductor carries a current I_{spiral} which flows in the direction as indicated, generating an associated magnetic field B_{spiral}, which has a maximum intensity at the center of the spiral. In the case of a large inductor with a very small core diameter, a significant part of this magnetic field does not pass through the center of the spiral but rather through its inner turns. Following the Faraday and Lenz's laws, an electric field is magnetically induced in these inner turns, that will generate circular eddy currents, I_{eddy}, which flow in the direction opposing the original change in the magnetic field. From the Fig.2.9, it is possible to observe that the eddy current, I_{eddy}, will add to the I_{spiral} on the inner side and subtract from I_{spiral} on the outer side of the conductor. As a result, the current density will be higher on the inner side than on the outer side causing a nonuniform current in the metal turns of the spiral inductor.

The magnitude of these eddy currents is comparable to the spiral current at high frequencies, hence increasing the series resistance of the inductor, reducing this way its quality factor [20].

- **Capacitive Coupling to Substrate** - Once that the substrate resistivity is neither zero nor infinity, there is a flow of current which results in a loss in each cycle of operation, hence, lowering the Q.

Despite some approaches that can potentially raise the Q, that include: thicker metallization [21], stacking of metal layers in a multilevel metal process [22], fabrication using high-resistivity silicon substrates [21] and the selective removal of silicon from beneath the inductor structure by chemical etching [23], the Q enhancement is not very effective considering the increased processing cost and required area.

In contrast, the quality factor of CMOS active inductors is set by the ohmic loss of the inductors, arising mainly from the finite output resistance of the transconductors of the inductors.

Threrefore, the quality factor of CMOS active inductors can be improved by increasing this output resistance. Several techniques are adopted to boost the output resistance, such as cascodes, regulated cascodes, and negative resistor compensation [4].

2.4.2 Silicon Area Consumption

Typically, the implementation of a spiral inductor requires a huge area on the die. Since the cost increases proportionately with the area, the designer always aims to minimize the occupied area. The inductor chip area can be reduced by choosing the optimum physical layout, that is, the strip width, the spacing between adjacent lines, the gap between opposing sets of coupled strips, the outer dimension of the spiral, and the number of turns. Therefore, these chip area reduction techniques are useful for obtaining higher inductances, at the expense of higher parasitic which degrades the overall performance of the inductor [24].

On the other hand, since that only MOS transistors are generally needed in the realization of CMOS active inductors and the inductance of these active inductors is inversely proportional to the transconductances of the transistors, the silicon consumption of CMOS active inductors is considered negligible as compared to that of their spiral counterparts [4, 25].

With the reduction of technological nodes, in CMOS, the scalability factor is related to digital parts while analog components with passive inductors have reduced scalability since they depend on the metal and dielectric characteristics. Despite all the methods to reduce the area occupied by passive elements, they will always fill a significant area.

2.4.3 Self-Resonant Frequency

The self-resonant frequency of an inductor is the frequency at which the parasitic capacitance of the inductor resonates with the ideal inductance of the inductor resulting in an extremely high impedance, so it is highly desirable to have an inductor with a large self-resonant frequency, ensuring that the active inductor has an inductive characteristic over a large frequency range.

The self-resonance of a spiral inductor is the resonance of the *LC* tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low self-resonant frequency of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral [4]. A thicker oxide layer reduces the parasitic capacitance of the structure, which improves the inductor self-resonant frequency [26]. However, despite some efforts to increase the self-resonant frequency, this remains a major drawback of passive components.

Taking the example in [4] to the active inductors, where a lossy single-ended gyrator-c is represented (Fig. 2.8 (b)), being G_{o1} and G_{o2} the total conductances at nodes 1 and 2, respectively. Assuming that the transconductances of the transcoductors are constant the resonant frequency of the RLC networks of the active inductor is given by Eq. 2.6.

$$\omega_0 = \frac{1}{LC_P} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} = \sqrt{\omega_{t1}\omega_{t2}} \tag{2.6}$$

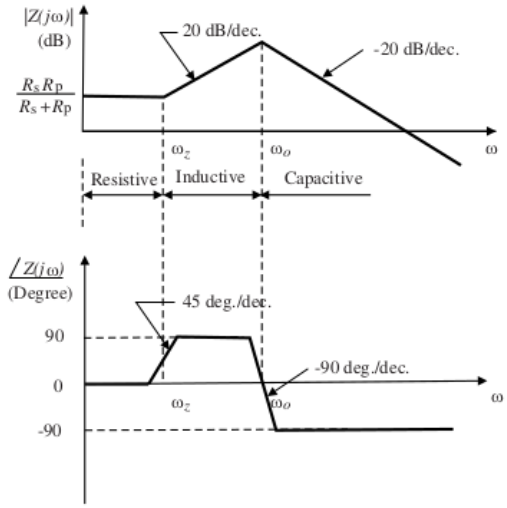


Figure 2.10: Bode plots of the impedance of lossy single-ended gyrator-C active inductor, reprinted from [4]

Where $\omega_{t1,2}$ is the cut-off frequency of the transcoductors (Eq. 2.7).

$$\omega_{t1,2} = \frac{G_{m1,2}}{C_{1,2}} \tag{2.7}$$

ω_0 is the self-resonant frequency of the gyrator-C active inductor. After a careful analysis, it is possible to observe that the pole resonant frequency of the impedance of the RLC equivalent circuit of the lossy inductor is given by Eq. 2.8

$$\omega_p \approx \sqrt{\frac{1}{LC_P}} = \omega_0 \tag{2.8}$$

Also, the impedance of the equivalent RLC circuit has a zero at frequency:

$$\omega_z = \frac{G_{o1}}{C_1} \tag{2.9}$$

The Bode plots of the impedance of the equivalent RLC circuit of the lossy inductor is sketched in Fig. 2.10 and it shows that the frequency range in which the gyrator-C network is inductive is lower-bounded by ω_z and upper-bounded by ω_0. It is possible to conclude, from this example, that the upper bound of the frequency range is set by the self-resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor.

2.4.4 Power Consumption

Unlike passive inductors, active inductors consume power to generate inductive impedance. In active inductor configurations, for instance, Gyrator-C active inductors, the dc power is used mainly for biasing the transconductors. However, power consumption is not a huge concern because the

inductance of the inductors is inversely proportional to the transconductances. This way, gm_1 and gm_2 are designed to be small in order to produce a large inductance. By lowering the dc biasing currents of the transconductors, this goal is achieved. The power consumption of active inductor is often set by replica-biasing and negative resistor networks [4].

2.4.5 Linearity

The linearity of a circuit signifies how well its output power can be represented as a linear function of the input power. Passive components have a wider linear operating range than their electronic equivalents [26]. Linearity is a relevant issue regarding the use of active inductors. When an active circuit is driven with a large signal, the operating points of the devices vary with the signal amplitude. This non-linear large-signal behavior of the devices results in impedance fluctuations and produces higher distortion that leads to the generation of harmonic frequencies [27]. Hence, active inductors do not apply to circuits involving large signal performance, such as power amplifiers.

Following the example in [4], which uses a gyrator-C network that consists of one port of a gyrator connected to a capacitor, as shown in Fig. 2.8 (a), it is possible to conclude that the inductance of the gyrator-C active inductor is represented by the Eq. 2.10, where $G_{m1,m2}$ are the transconductances of transconductors 1 and 2 respectively when in saturation. The inductance of the gyrator-C when in triode is given by Eq. 2.11, where $G_{mt1,mt2}$ are the transconductances of transconductors 1 and 2 respectively.

$$L = \frac{C}{G_{m1}G_{m2}} \tag{2.10}$$

$$L = \frac{C}{G_{mt1}G_{mt2}} \tag{2.11}$$

Fig. 2.11 shows that when the transistors of active inductors enter the triode region, the transconductances of the transistors decrease from G_m (saturation) to G_{mt} (triode) in a nonlinear way. Therefore, when the voltage swing is large enough to change the operating point of the transistors of the transconductors, regarding the Eq. 2.10 and 2.11, the inductance of the gyrator-C active inductors will exhibit a nonlinear characteristic.

2.4.6 Noise

Unlike the passive inductor where the damping resistor is the main noise producer, noise is a major drawback of an active inductor and it is originated from the thermal and flicker noise of MOS transistor channel, while the damping resistor is a fictitious one without any noise contribution [28].

Thermal noise is due to the thermal excitation of charge carriers in a conductor. This noise has a white spectral density, it is proportional to absolute temperature and not dependent on bias conditions (dc bias current) [29].

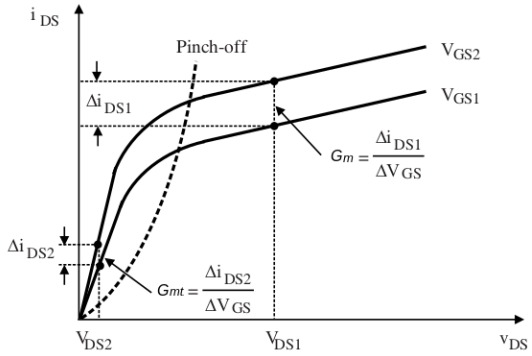


Figure 2.11: Transconductance of MOSFETs in the saturation and triode regions, reprinted from [4]

Although flicker noise is found on all active devices, it occurs only when a dc current is flowing. Typically, flicker noise arises due to traps in the semiconductor, where carriers that would normally constitute dc current flow are held for some time period and then released. Flicker noise is also commonly referred to as $1/f$ noise since it is well modeled as having a $1/f^{\alpha}$ spectral density, where α is between 0.8 and 1.3 [29]. It is apparent that flicker noise is most significant at low frequencies, although, in devices exhibiting high flicker noise levels, this noise source may dominate the device noise at frequencies well into the megahertz range [30].

2.4.7 Inductance Tunability

The inductance of a spiral inductor remains reasonably fixed up to a certain frequency, called self-resonance frequency (low-pass behavior). Beyond this frequency, the inductor has a capacitive behavior. In contrast, the inductance of the active inductor is determined by a specific frequency range (band-pass behavior - represented previously in Fig. 2.10).

There are some techniques to increase the inductance of the spiral inductor such as increasing the number of the turns of the spiral or use a stacked configuration where spirals on multiple metal layers are connected using vias. However, for a given length, width, and spacing, the passive inductor´s inductance is a weak function of the number of turns (Fig. 2.12) [3] and at the expense of a large silicon area. In [31], it is demonstrated that the inductance of stacked spiral inductors increases approximately linearly with the increase in the number of the spiral layers of the inductors (Fig. 2.13) but it increases the spiral-substrate capacitance as well.

In section 2.3.2.1, it was shown that in a gyrator-C network, inductance is proportional to the capacitance and inversely proportional to the transconductances. In this case, transconductance is dependent on current flowing through that transconductor so gate voltage can be manipulated to control the current of that particular branch that will ultimately vary the inductance of the active inductor. Thus, the inductance can be tuned conveniently by varying the dc biasing condition of the transistors. The fine tuning of the inductance of active inductors can also be achieved by

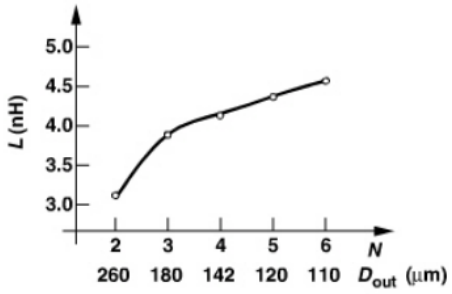


Figure 2.12: Inductance as a function of the number of turns for a given line length, reprinted from [3]

varying the load capacitance of the transconductors of the active inductors using MOS varactors [4].

2.5 Shunt peaking active inductor implementations

The previous Shunt peaking section, 2.2.3, presented several shunt peaking approaches, assuming only the implementation of on-chip inductors, being the simplest one showed in Fig.2.14 (a). As discussed previously, it is desired to adopt an active inductor solution, since it is the most viable option to guarantee a resonant frequency that is aligned with the bandwidth required in today's wired serial communications with protocols reaching the tens of Gbps while using a reduced silicon area.

2.5.1 Simple Active inductor

This way, the replacement of the passive on-chip inductor by an active inductor, results in a simple active inductor, represented in Fig.2.14 (b). However, the main drawback of this basic topology

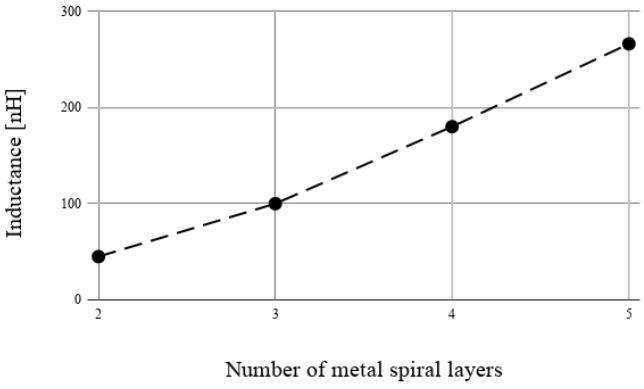


Figure 2.13: Inductance as a function of the number of metal spiral layers

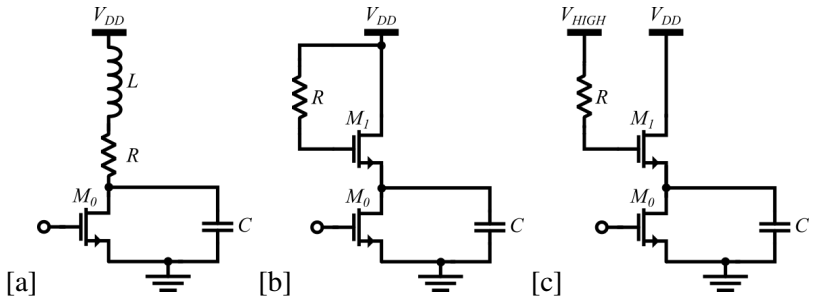


Figure 2.14: Common source amplifier with shunt peaking - (a) Using a spiral inductor (b) Using a simple active inductor (c) Using an active inductor with voltage boosting

is its significant dc voltage drop caused by the NMOS threshold voltage, which is enlarged by the body effect. In [32], it is proposed a solution to this problem, which is biasing the gate of the active inductor one NMOS threshold voltage above V_{DD} reducing the voltage drop across the active inductor to about half its value (Fig. 2.14 (c)). The cost of this method is increased design complexity and area associated with the addition of voltage-boosting circuitry.

2.5.2 Folded Active Inductor

Another solution is presented in [33], initially proposed by [34], and is represented in Fig. 2.15 (a). It adopts a folded topology that allows the gate-source voltage of the NMOS transistor to be biased at much higher than its V_{th} level without additional circuitry, and where M_2 transistor is biased in linear region, operating as a resistor.

This topology is widely used in many high frequency applications, such as limiting amplifiers for optical receivers [33, 34], RF transmitters [35] or even to equalization purposes [36].

Although the folded topology is mostly associated with the use of NMOS, some consider that the PMOS version of folded is the one represented in figure 2.15 (b), for example in [37, 38, 39]. However, this PMOS version is nothing less than the PMOS version of the simple active inductor.

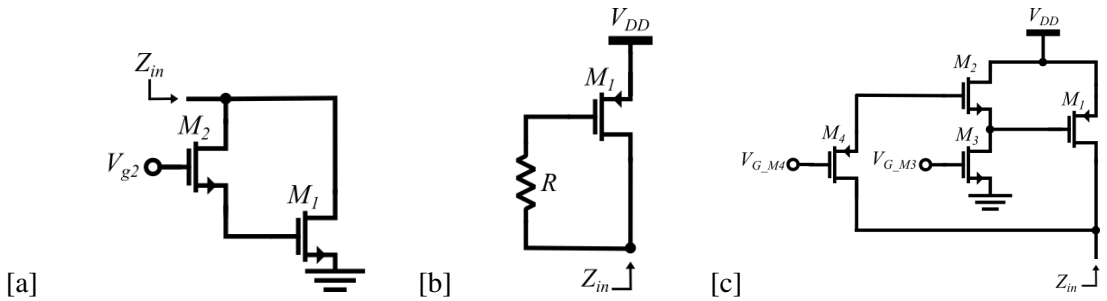


Figure 2.15: (a) Folded active inductor NMOS (b) PMOS version: Simple active inductor and Folded active inductor (c) Lee´s active inductor

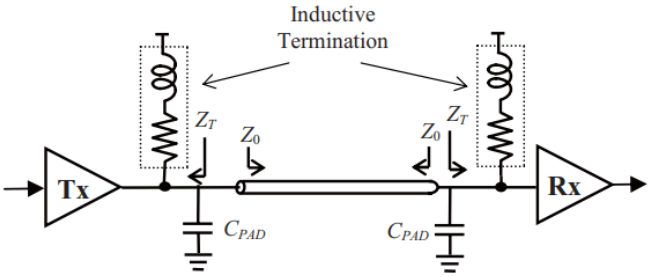


Figure 2.16: Doubly terminated I/O blocks with inductive peaking terminations, reprinted from [6]

2.5.3 Lee's Active Inductor

In [40], an active inductor termination for high speed I/O circuits is presented. This approach, represented in Fig.2.15 (c), has a transistor M_4, operating in linear region to act as a resistor, coupling, this way, the gate of the PMOS M_1 to the output node. To guarantee a lower gate bias voltage for M_1, a level shifter is introduced, which is constituted by a source follower M_2 and a current source M_3. Similarly to the Folded active inductor, this topology does not need the addition of a voltage-boosting circuitry. However, it could have an additional overhead power consumed by the level shifter, which also contributes to increase the overall parasitics in the configuration.

This configuration is also used in [6], as an inductive termination in an output driver in the serial link transmitter shown in Fig.2.16. The active inductor aims to compensate the high frequency loss of the channel.

2.6 Summary

In this chapter, three of the most relevant methods in bandwidth enhancement were covered, namely, capacitive compensation technique, distributed amplification, and shunt peaking. While capacitive compensation suffers from critical frequency limitations, distributed amplification consumes large area and high power. Shunt peaking, in contrast, allows an increase in bandwidth by simply adding a reduced number of inductors.

A detailed comparison between the active and passive inductors was performed based on several performance criteria. Passive inductors suffer from a low quality factor, a low self-resonant frequency, a low and fixed inductance and occupy a large silicon area. On the other hand, active inductors offer a number of attractive characteristics as compared with their passive counterparts. These characteristics include a low silicon consumption, a large and tunable inductance, a large and tunable quality factor. The applications of active inductors, however, are affected by some stiff difficulties arising from the intrinsic characteristics of MOS devices including a limited dynamic range and a high level of noise.

Finally, the concept of shunt peaking was presented considering only active inductors. The basic active inductor has a significant voltage drop, which can be compensated with a voltage-boosting circuitry with the cost of introducing extra design complexity. The folded active inductor avoids both these problems by using just an NMOS transistor with a resistor connected to the gate being widely used in different high speed applications. Lastly, the Lee active inductor is a viable shunt peaking technique that uses a level shifter to increase the ability to regulate the voltage depending on the scenario where it is applied.

Chapter 3

Shunt peaking implementation

As shown in the previous chapter, inductive shunt peaking is a technique that allows the improvement of bandwidth using a reduced number of inductors, which can be implemented passively or actively. Nowadays, since it is economically viable to manufacture an inductor on the chip, the decision to choose the type of inductor to be applied has a significant impact when it comes to the time of integration. The need for a large silicon area to fabricate passive inductors and features such as low-quality factor, low and fixed inductance, and low self-resonant frequency, dramatically increase the interest in using an active inductor solution, aiming to minimize silicon area consumption and, subsequently, the manufacturing cost while improving the overall performance.

During this chapter, the AI (active inductor) configurations presented in the previous chapter will be analyzed. For the topologies which show a greater potential as a possible starting point for the solution of the problem at hand, a practical design will be carried out so that a more complete analysis can be performed with simulation results. Along with the simulation results, a theoretical analysis will be also made. Both of these analyses will serve as a basis for all of the work that will be later done in the thesis.

Taking into account the scenario and the requirements described in chapter 1, a journey begins in search of the most suitable active inductor configuration with the ultimate goal of extending the bandwidth.

3.1 Folded Active Inductor

3.1.1 Small signal analysis

To better understand how the folded configuration works (Fig.3.1 (a)), first, it is considered the small-signal model, which is represented in Fig.3.1 (b), as well as the respective input impedance. In order to simplify the analysis, M_1 is modeled just with C_{gs} and gm, while the M_2 transistor, which is biased in linear region to perform as a resistor, is represented by a R. By the application of a test voltage V_{in} with the current out of the positive terminal being I_{in} it is possible to obtain the Thévenin equivalent impedance Z_{in}, that is given by the ratio of the test voltage to the test current

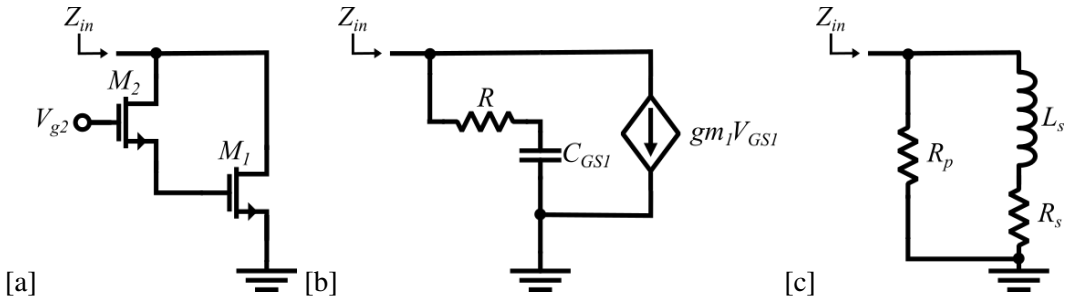


Figure 3.1: Folded active inductor - (a) Schematic (b) Small signal model (c) Small signal equivalent

(Eq. 3.1).

$$Z_{in} = \frac{V_{in}}{I_{in}} \tag{3.1}$$

Considering now the Ohm's and short Kirchhoff's Current Laws, the Eq.3.2 represents the algebric sum of all the currents at the gate of M_1 while I_{in} is given by Eq.3.3.

$$\frac{V_{in} - V_g}{R} - \frac{V_g}{1/(s\,C)} = 0 \tag{3.2}$$

$$I_{in} = gm\,V_g + \frac{V_{in} - V_g}{R} \tag{3.3}$$

Solving these three equations, it is obtained the input impedance, given in Eq.3.4.

$$Z_{in} = \frac{s\,R\,C_{gs} + 1}{s\,C_{gs} + gm} \tag{3.4}$$

From Z_{in}, it can be quickly inferred that it has a zero ($w_z = 1/(R\,C_{gs})$) and a pole ($w_p = gm/C_{gs}$). And similarly the input admittance, Y_{in}, is given by Eq. 3.5.

$$Y_{in} = \frac{1}{R} + \frac{1}{s\frac{R\,C_{gs}}{gm-1/R} + \frac{1}{gm-1/R}} \tag{3.5}$$

The parameters of the *RLC* equivalent circuit are now more easy to reach, once that, the equation of Y_{in} can be represented by an *RL* network in parallel with a resistor R_p (Eq.3.6), that is shown in Fig.3.1 (c).

$$Y_{in} = \frac{1}{R_p} + \frac{1}{s\,L + R_s} \tag{3.6}$$

where

$$R_p = R \qquad L = \frac{R\,C_{gs}}{gm - 1/R} \qquad R_s = \frac{1}{gm - 1/R} \tag{3.7}$$

From these expressions, it is possible to conclude that the value of the inductance can be tuned by the M_2 transistor as the inductance range is strongly dependent on the R value. It is also important to highlight the impact that the gm has on the performance of this topology. If

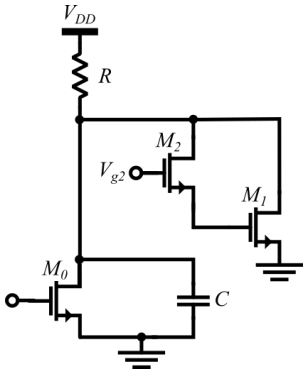


Figure 3.2: Application of the folded active inductor

increasing *gm* corresponds to increasing the pole frequency value, it also decreases the inductance value. Additionally, the value of *gm* is also required to be higher than $1/R$ in order to have $L > 0$.

3.1.2 Shunt vs Series peaking

Simulations carried out, proved what the previous Small signal analysis section demonstrated (3.1.1). A high inductance is achieved during a wide range of frequency, just taking into account the values of specific parameters, especially *gm*, which makes the folded configuration a candidate to be a solution to the exposed problem.

Now, it is necessary to decide where the folded inductor will be inserted. Remembering the conditions mentioned in the chapter 1, the inductor must have a real linear part equivalent of 50 Ω, so the only way will be to apply the inductor in parallel with the resistance, as represented in the Fig. 3.2. This scenario was simulated, and the results were not very encouraging. It seems that the fact of having an inductor in parallel compromises the generated inductance.

In order to evaluate the impact in the equivalent impedance of having a resistor in parallel with an inductor instead of having it in series, a test was performed, considering a resistor and an ideal inductor, as it is suggested in Fig. 3.3.

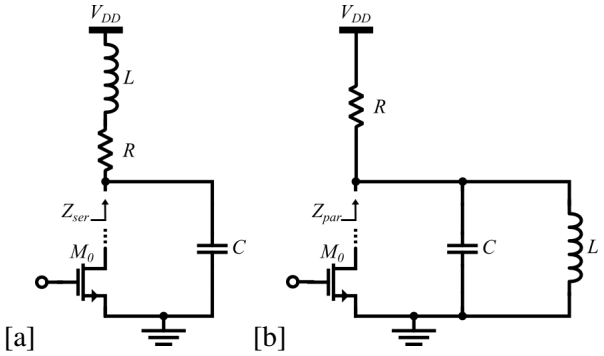
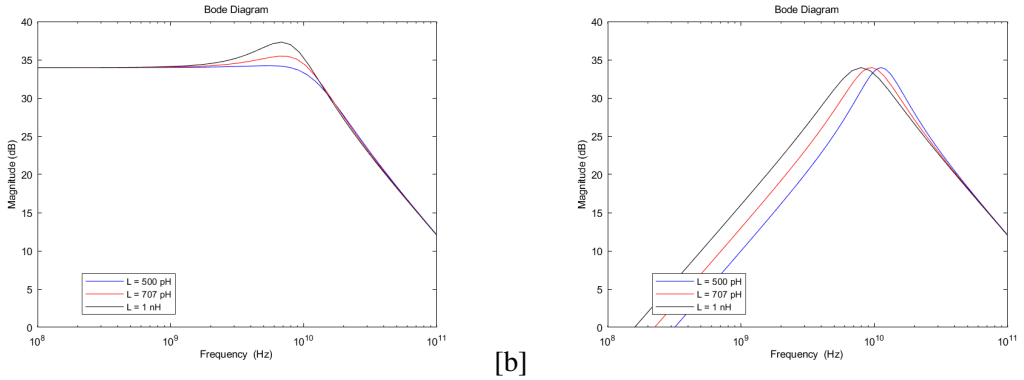


Figure 3.3: Testing scenarios: (a) Resistance in series with the inductor ($(R+sL)\ //\ (1/sC)$) (b) Resistance in parallel with the inductor ($R\ //\ sL\ //\ (1/sC)$)



[a] [b]

Figure 3.4: Simulation results: (a) Resistance in series with the inductor ($(R+sL)\ //\ (1/sC)$) (b) Resistance in parallel with the inductor ($R\ //\ sL\ //\ (1/sC)$)

Fig.3.3 (a) represents the case where the configuration has three branches, each one having just one component, hence constituting, a parallel between a resistor, R, a capacitor, C, and an inductor, L. Elaborating Eq.3.8, the equivalent impedance, Z_{par},is given by Eq.3.9.

$$Z_{par} = R\ //\ s\,L\ //\ \frac{1}{s\,C} \tag{3.8}$$

$$Z_{par} = \frac{s\,L}{s^2\,L\,C + (s\,L/R) + 1} \tag{3.9}$$

On the other hand, Fig.3.3 (b) shows the case where the equivalent impedance, Z_{ser}, corresponds to a parallel of two branches, one with a resistor, R, in series with an inductor, L, and another with just a capacitor, C. This way, Z_{ser} can be obtained through the Eq. 3.10 that results in the final expression of the equivalent impedance in this case is given by Eq. 3.11.

$$Z_{ser} = (R + s\,L)\ //\ \frac{1}{s\,C} \tag{3.10}$$

$$Z_{ser} = \frac{R + s\,L}{s^2\,L\,C + s\,R\,C + 1} \tag{3.11}$$

The main difference between these two approaches is implicit, both in the performed simulation (Fig.3.4) and in the analytical analysis. The approach (b), which has all the components in parallel, has an undesired bandpass behavior due to the presence of a zero at zero frequency. For this reason, it could never be considered a good approach to extend the bandwidth. Despite achieving a high inductance during a wide range of frequency, this folded active inductor configuration does not suit so well when integrated into the described shunt peaking scenario.

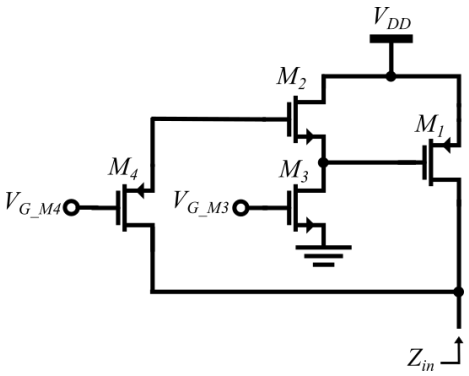


Figure 3.5: Lee´s active inductor

3.2 Lee's Active Inductor

3.2.1 Small signal analysis

The small signal analysis of this subsection follows the analysis carried out in [40] (topology represented in Fig.3.5), which assumes that the level shifter has unitary AC gain. As will be shown later, this assumption is a rough approximation of the actual gain of the level shifter. Transistor M_1 is modelled neglecting C_{gd} (which will be considered later in a more detailed analysis) and considering gm, gds, C_{gs} and C_{ds} inherent parameters of transistor M_1. Resistor R, represents transistor M_4, which is operating in linear region. The small signal of this active inductor is shown in Fig. 3.6.

By deactivating all the independent sources and using a test voltage V_{in} with the current out of the positive terminal being I_{in}, it is possible to obtain the Thévenin equivalent impedance, Z_{in}, that is given by the ratio of the test voltage to the test current (3.12).

$$Z_{in} = \frac{V_{in}}{I_{in}} \tag{3.12}$$

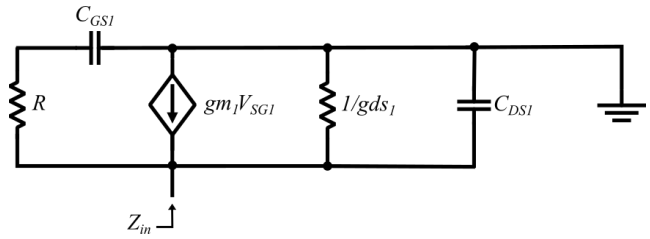


Figure 3.6: Schematic of Lee's active inductor

Considering the Ohm's and short Kirchhoff's Current Laws, Eq.3.13 and Eq.3.14 represents the algebraic sum of all the currents at the gate of M_1 and the expression of I_{in}, respectively.

$$\frac{V_{in}-V_g}{R}+\frac{V_g}{1/(s\,C_{gs})}=0 \tag{3.13}$$

$$I_{in}=\frac{V_{in}-V_g}{R}+gm\,V_g+V_{in}\,gds+\frac{V_{in}}{1/(s\,C_{ds})} \tag{3.14}$$

Deriving these three equations, it is obtained the input impedance, given in Eq.3.15.

$$Z_{in}=\frac{1+s\,R\,C_{gs}}{s^2\,C_{ds}\,C_{gs}\,R+s\,(\,C_{gs}+gds\,C_{gs}\,R+C_{ds})+gm+gds} \tag{3.15}$$

Knowing that the admittance, Y_{in}, is defined as the reciprocal of impedance and neglecting the C_{ds}, to simplify, the expression of Y_{in} can be derived from Eq.3.16.

$$Y_{in}=\frac{1}{Z_{in}}=\frac{s\,(\,C_{gs}+R\,C_{gs}\,gds)+gds+gm}{1+s\,C_{gs}\,R} \tag{3.16}$$

$$Y_{in}=\frac{s\,(\,C_{gs}+R\,C_{gs}\,gds)}{1+s\,C_{gs}\,R}+\frac{gds+gm}{1+s\,C_{gs}\,R} \tag{3.17}$$

$$Y_{in}=\frac{1}{\frac{1+s\,C_{gs}\,R}{s\,(\,C_{gs}+R\,C_{gs}\,gds)}}+\frac{1}{\frac{1+s\,C_{gs}\,R}{gds+gm}} \tag{3.18}$$

$$Y_{in}=\frac{1}{\frac{R}{R\,gds+1}+\frac{1}{s\,(\,C_{gs}+C_{gs}\,R\,gds)}}+\frac{1}{\frac{s\,C_{gs}\,R}{gds+gm}+\frac{1}{gds+gm}} \tag{3.19}$$

The process of solving Eq. 3.16, which is represented by steps through Eq.3.17, 3.18 and 3.19, leads to the parameters of the equivalent *RLC* circuit, Fig.3.7 (a), where:

$$R'_1=\frac{R}{R\,gds+1}\quad C'=C_{gs}\,(\,1+R\,gds)\quad L'=\frac{C_{gs}\,R}{gds+gm}\quad R'_2=\frac{1}{gds+gm} \tag{3.20}$$

At the beginning of this analysis to achieve the equivalent *RLC* model, C_{ds} was neglected to make this procedure simpler. However, now this capacitance can be considered in the respective *RLC* model. Since that C_{ds} is in parallel with the whole signal circuit, as shown in Fig. 3.6, the same will happen when thinking in the *RLC* equivalent shown in Fig.3.7 (a).

In [40], for some reason not mentioned, the branch of the series C' and R'_1 is not considered, resulting in the equivalent *RLC* model represented in Fig.3.7 (b). The expressions of the components involved in this last model are as follows:

$$L=\frac{C_{gs}\,R}{gds+gm}\quad R_s=\frac{1}{gds+gm}\quad C_p=C_{ds} \tag{3.21}$$

As suggested by the L value (Eq.3.21), and similarly to Folded Active Inductor, the inductance value can be tuned by the R value, which represents the M_4 transistor that is operating in the linear

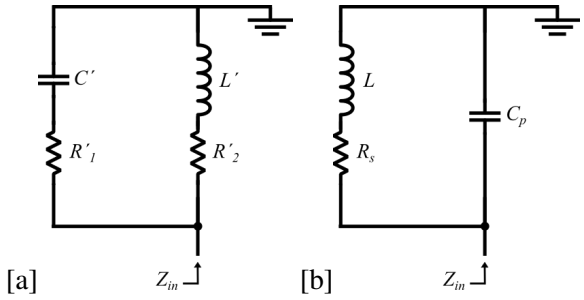


Figure 3.7: Lee´s active inductor RLC (a) initial (b) simplified

region, hence, the inductance can be controlled by changing the voltage at the gate of M_4.

One of the most important performance criteria, and perhaps the main one in this case where the ultimate goal is to expand the bandwidth, is the resonant frequency, which is the maximum frequency at which the inductor operates. Observing the denominator of the input impedance transfer function, Eq.3.15, and considering the characteristic equation of a second-order system, represented in Eq.3.22, the resonant frequency, ω_0 is given by Eq.3.23. At first sight, it is tempting to increase the dimensions of transistor M_1, increasing this way the *gm* and *gds* parameters, contributing to a higher resonant frequency. However, increasing the transistor size leads to higher intrinsic capacitance, which decreases ω_0. This indicates that the sizing of transistor M_1 will have a huge impact on the overall performance of the active inductor. Another relevant observation regarding the resonant frequency is the negative impact that a high R value could have. If this parameter helps to increase the inductance generated by the inductor, at the same time, it decreases ω_0. For this reason, it is another aspect to be taken into account when designing the active inductor.

$$s^2 + 2\,\delta\,\omega_n^2\,s + \omega_n^2 \tag{3.22}$$

$$\omega_0 = \sqrt{\frac{gm + gds}{C_{gs}\,R\,C_{ds}}} \tag{3.23}$$

3.2.2 Active inductor integration

Now that this active inductor configuration was carefully analyzed, it is time to integrate it into the intended scenario. Since that a linear equivalent resistance of 50 Ω is a requirement to meet, a resistor will be needed to guarantee the desired real part equivalent. Following the basic idea of shunt peaking, the simplest solution is to put the resistor in series with the inductor, as shown in Fig.3.8. It is possible, this way, to regulate the equivalent real part of the inductor, by just changing the value of the inserted resistor, R_{AI}.

As explained in the previous chapter, in the section regarding Shunt peaking, the introduction of an inductance in series with the load resistance, provides an equivalent impedance that increases with frequency, which helps off the decreasing impedance of the capacitance. However, in order to achieve the desired behavior, the topology must guarantee an ideal ratio between the inductance,

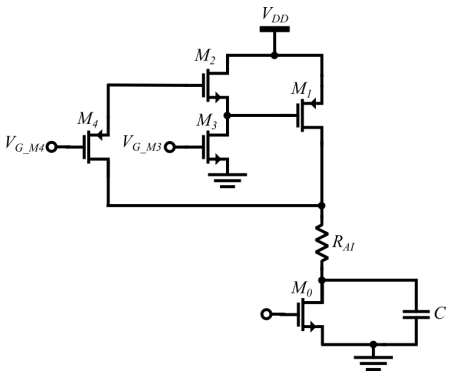


Figure 3.8: Application of Lee´s active inductor

L, the resistance, R, and finally, the capacitance associated with the output node, C. This ratio can be denoted by m so that $L = m\,R^2\,C$. The value of m may vary depending on the application of the shunt peaking method. As the main objective here is to increase the bandwidth, the suggested ratio value is $m = \sqrt{2}$, which extends the bandwidth to a value of about 1.85 times as large as the uncompensated bandwidth [14, 15, 16]. A small test can be performed to prove the value attributed to this ratio. Fig.3.9 shows a simple RC circuit whose equivalent impedance is given by Eq.3.25, and a circuit that is already known and was discussed here, an inductance, L, in series with the resistance, R, to compensate the capacitor, C. The equivalent impedance of the latter is given by Eq.3.26.

$$L = m\,R^2\,C \tag{3.24}$$

$$Z_{RC} = \frac{R}{s\,R\,C+1} \tag{3.25}$$

$$Z_{RCL} = \frac{R+s\,L}{s^2\,L\,C+s\,R\,C+1} \tag{3.26}$$

Fig.3.10 shows the result of plotting the equivalent impedance of each circuit, considering

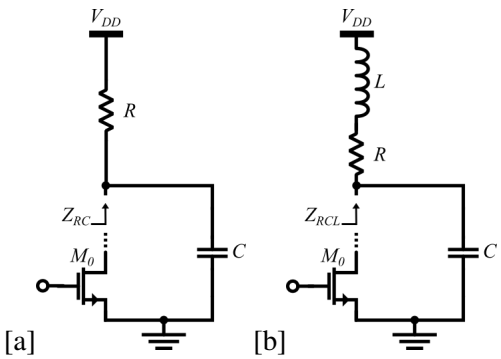


Figure 3.9: Small test to prove the ratio value (a) RC circuit (b) RCL ciruit

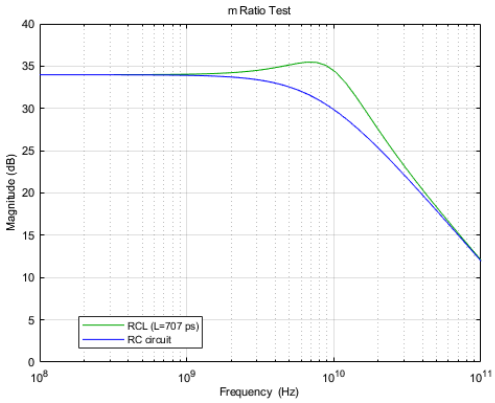


Figure 3.10: Result of the small test to prove the ratio value

a resistor R of 50 Ω and a capacitor C of 400 fF. Following the Eq.3.24 and considering the recommended m ratio, the value of the inductance L is 707 pH. In fact, the introduction of the inductor brought a significant bandwidth improvement, as can be seen in the plot. Measuring the bandwidth of each circuit, it is verified that this improvement is precisely 1.85.

At this moment, there is already an idea of how to implement the inductor as well as the value of the inductance to use that effectively compensates the capacitor. The next step is focused on manage the components to achieve the required inductance, not forgetting the equivalent resistance required, and, most importantly, the main goal of extending the bandwidth.

3.2.3 Imaginary part analysis

The small signal analysis carried out, in section 3.2.1, indicated that M_1 is the transistor that has the most significant impact on the behaviour of the active inductor. This way, the respective sizing of M_1 should be done carefully. The same analysis allowed to conclude how each parameter influences each performance criteria. Now, this imaginary part analysis aims to evaluate the impact of these parameters, thus providing sensitivity to the weight that each parameter has in each performance criteria. As this analysis only takes into account the imaginary part, to simplify the biasing conditions, the resistor R_{AI} that will be used to compensate the real part of the inductor is not considered for now.

3.2.3.1 Signal model

Instead of M_1, it is considered the respective signal equivalent. The same happens with transistor M_4, which is operating in the triode region, and for that reason is converted into a resistor, R. This procedure consists of performing a parametric analysis to each parameter at a time and observing the impact that this variation has on the equivalent inductance generated by the inductor, as well as on the resonant frequency. Fig.3.11 shows the adopted procedure and how is measured the impedance, which can be derived at low frequencies, in a simple way by Eq.3.27, since the capacitive elements can be discarded due to the very large inherent impedance.

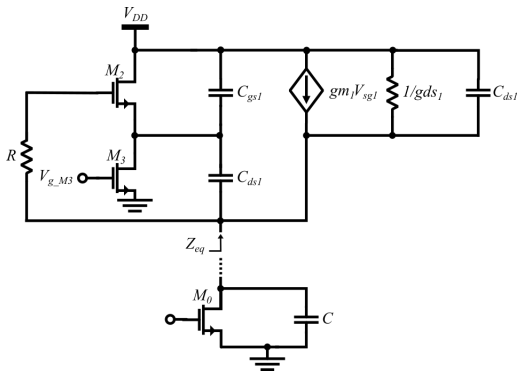


Figure 3.11: Adopted procedure to measure the impedance

$$Z_{eq} = R + j\,\omega\,L \tag{3.27}$$

Following Eq.3.27, the inductance generated by the inductor can be measured considering the ratio of the imaginary part of Z_{eq} to ω, Eq.3.28.

$$L = \frac{imag\,[Z_{eq}]}{\omega} \tag{3.28}$$

The result of these parametric analyses is shown in Fig.3.12. Due to confidential reasons, the parameter values, as well as the values of the sweeps, will not be mentioned. This way, knowing that each line corresponds to a specific value of the parameter under test, the lighter and darker lines represent the lowest and highest value to be tested, respectively. The parametric simulation starts in the lowest value represented by the lighter line, and as the value increases, the respective line gets darker.

Plots (a) and (b), from Fig.3.12, represents the behavior of *gm* and *gds*, respectively. Each parameter was subjected to the same test conditions, which consists of a sweep analysis from a minimum to a maximum value with a given step. Additionally, the value where *gds* is equal to *gm* is in the middle of the tested range. This way, it is analyzed not only the impact that each parameter has but also the effect of the ratio between these two parameters on the inductance and resonant frequency of the active inductor. At first sight, plot (b) indicates that *gds* has a significant impact in inductance value, enough to be considered an alternative to contribute to the inductance tunability. However, it would be an unwise decision, since assigning the responsibility of guaranteeing a specific inductance to a parameter inherent to a transistor would contribute to introduce non-linearity to the inductor. Plot (a) suggests that exists a possibility that in the case of the value of *gm* being higher than that of *gds*, it could bring benefits to ensure a decent resonant frequency. On the other hand, plot (b) tells that a higher *gds* reduces the inductance as well as the resonant frequency.

Plots (c), (d), and (e), from Fig.3.12, show the behavior of intrinsic capacitances of transistor M_1. Again, the parametric simulation for each capacitance was performed in the same way. As

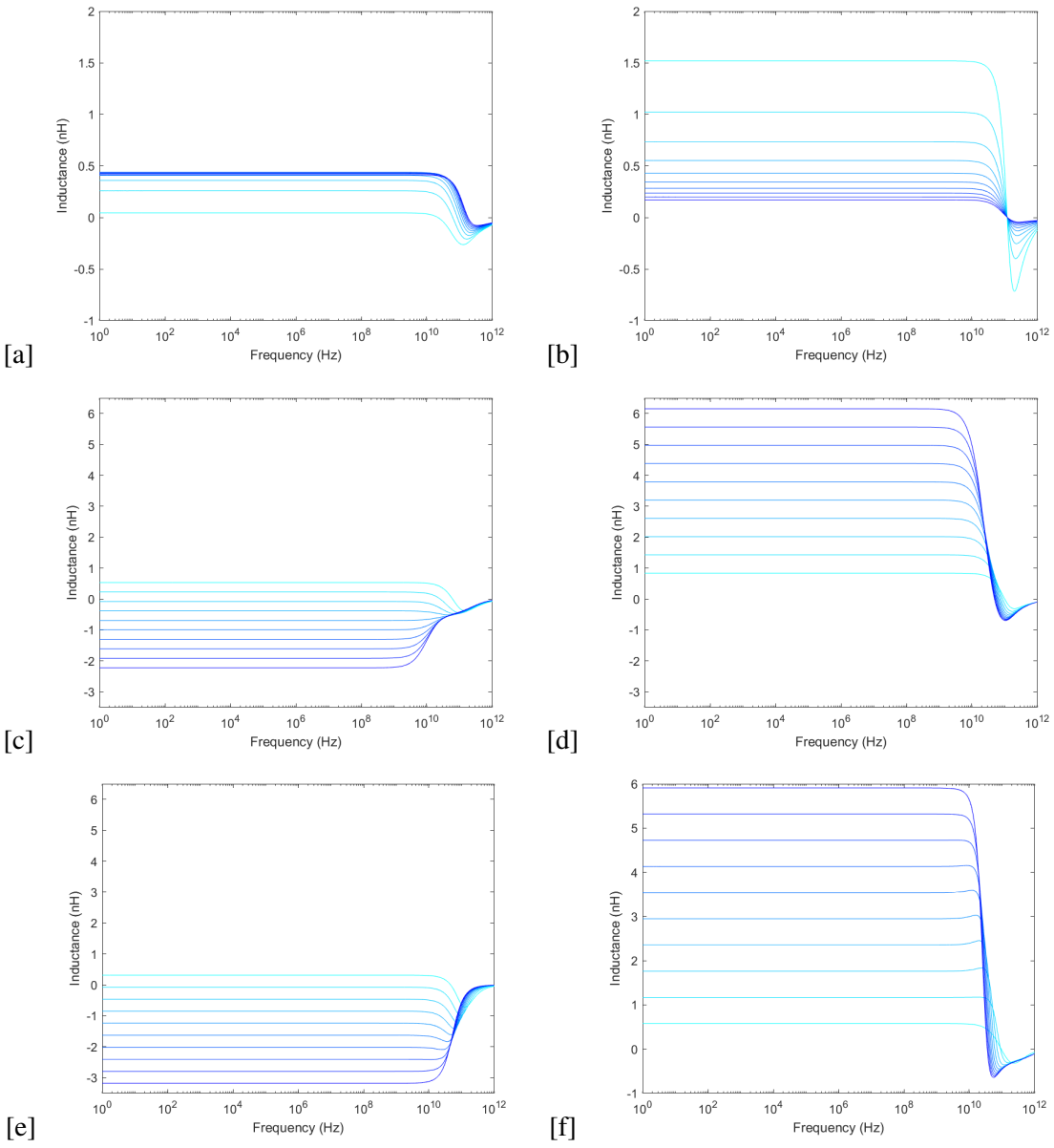


Figure 3.12: Parametric analysis - sweep of each parameter at a time, between a minimum value (lighter line) and a maximum value (darker line): (a) *gm* (b) *gds* (c) C_{gd} (d) C_{gs} (e) C_{ds} (f) *R*

expected, increasing the capacitance decreases the performance of the active inductor, however, by observing the plots, it is possible to conclude that C_{gs} and C_{gd} have more influence on the degradation of the resonant frequency of the active inductor.

Lastly, plot (f) of Fig.3.12 matches the small-signal analyses performed. The value of the inductance is directly proportional to the *R* value (Eq.3.21). Although the increase in the *R* value contributes to a slight decrease in the resonant frequency, it is the most viable solution to adjust the inductance value to a specific desired value.

These parametric analyses revealed that when sizing transistor M_1, it is convenient to guarantee a small *gds* and preferably, a *gm* greater than *gds* at the same time, keep the intrinsic capacitances

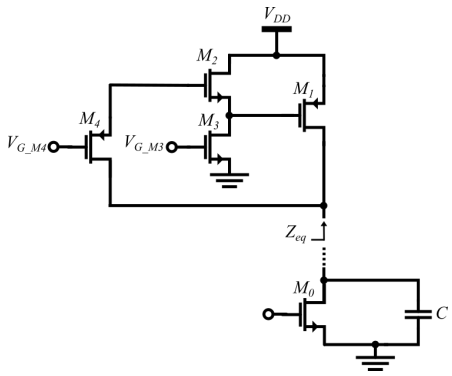


Figure 3.13: Application of Lee´s active inductor

as small as possible. This leads to the main conclusion that transistor M_1 must be of small sizing, to avoid the degradation of the overall performance of the active inductor.

3.2.3.2 Real model

Taking into account these transistor M_1 attributes that are most convenient to the success of the active inductor design, the next step will be focused on finding a suitable real transistor M_1 to integrate into the configuration represented in Fig.3.13.

Since the performed analysis suggests a small transistor, the sizing of M_1 starts by using a minimum transistor size. The level shifter (composed by transistors M_2 and M_3) is designed to guarantee a low voltage at the gate of M_1. Note that these two transistors also contribute to the capacitance seen at the gate of M_1, which adds to the amount of intrinsic capacitance that M_1 already has, contributing this way to the degradation of the resonant frequency. Thus, the level shifter must be designed to fix a specific low voltage at the gate of M_1, while using small transistors. In order to take the less possible voltage headroom, while operating in the saturation region, V_{sd} of transistor M_1 is established at a specific voltage. This source-drain voltage of transistor M_1 will always be set at the same value throughout the work developed in this thesis and will be referred to as V_{sd} of the transistor M_1.

After some adjustments in the sizes of the transistors to obtain a decent resonant frequency, and by regulating the value of R to achieve the desired inductance value (707 pH), the final result of the equivalent L is represented in Fig. 3.14 (a).

The component that remains to be converted from the signal model to the real is precisely the R, which is replaced by a PMOS, as it is suggested in Fig.3.13. Now, the inductance tunability depends on the voltage applied at the gate of M_4, $V_{G_M}4$. Fig.3.15 shows a parametric analysis of $V_{G_M}4$, between a minimum value (lighter line) and a maximum value (darker line). This analysis indicates that even converting the resistor R to a PMOS operating in a linear region, there is still enough margin to regulate the inductance. This substitution has no impact on the resonant frequency, as it can be seen by comparing 3.14 (a) and (b) where the inductance is adjusted by using a resistor R or by using a PMOS as a resistor, respectively.

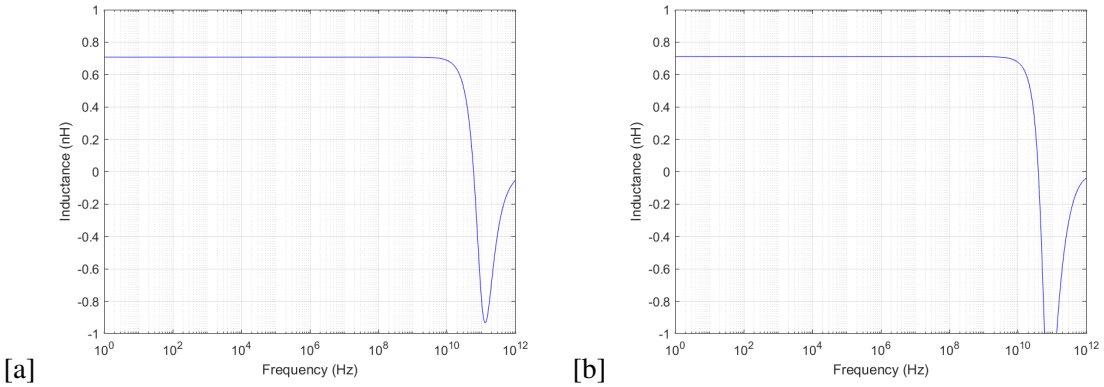


Figure 3.14: Equivalent inductance: (a) After real model adjustments (b) After replacing R by M_4

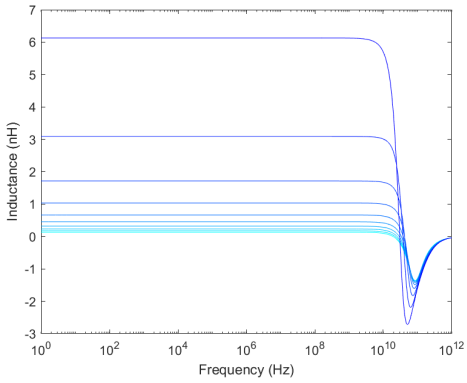


Figure 3.15: Parametric analysis of $V_{G_{M4}}$

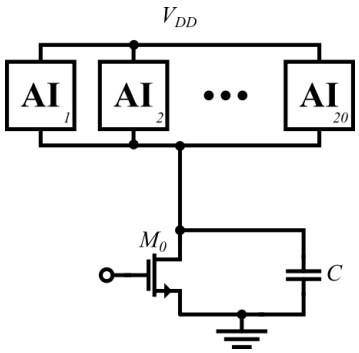


Figure 3.16: Scenario with N branches, each with an active inductor

As it is shown by the previous plot, the imaginary part of the inductor looks fine. However, M_1 is a small transistor, hence the current trough this transistor is in the range of μA, meaning that the inductor only supports currents situated in this range. This way, it fails to accomplish the requirement of supporting currents in the range of mA.

The time has come to make decisions again. If having a small transistor means low current but high resonant frequency, increasing the size of the transistor corresponds to higher current, and low resonant frequency. So, increasing the transistor size seems not to be the right option.

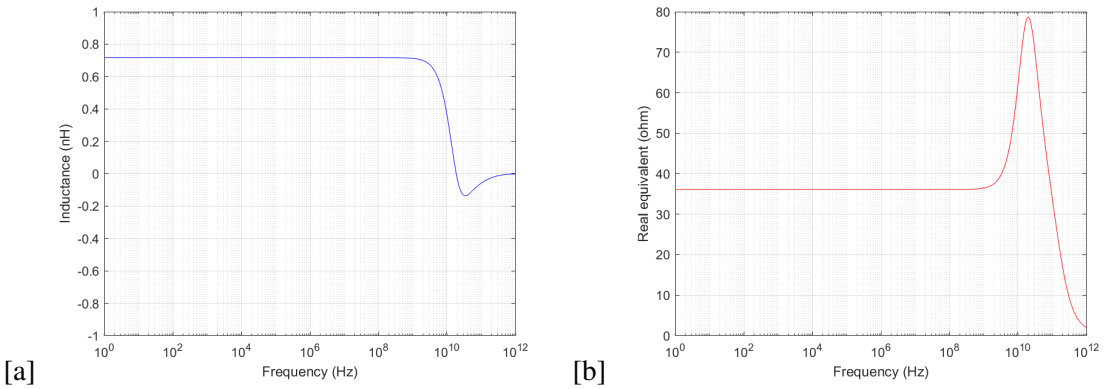
The proposed solution is to use several branches in parallel, as shown in Fig.3.16, each with an active inductor. This way, since the current of the overall active inductor will be the sum of the currents of all branches, using the right number of branches, it is possible to establish the current in the desired range of mA. However, this solution brings a difficulty. Now that the inductor is constituted by a number of branches, N, assuming that L_n is the inductance generated by branch n, the total equivalent inductance, L_{eq}, is given by Eq. 3.29. As a result of being equal, all the branches generate the same inductance, L_{branch} (Eq.3.30). Deriving these two equations leads to Eq.3.31. This equation indicates that in the case of having N branches, the inductance generated by each branch, L_{branch}, needs to be N times greater than the desired equivalent inductance, L_{eq}.

$$L_{eq} = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + ... + \frac{1}{L_n}} \tag{3.29}$$

$$L_{branch} = L_1 = L_2 = L_n \tag{3.30}$$

$$L_{branch} = L_{eq}.N \tag{3.31}$$

The number of branches to use must be chosen wisely, since that a high number of branches require to each branch to generate a high inductance, which can be reached by increasing the R value, as demonstrated previously. However, increasing too much this resistor reduces the resonant frequency. Furthermore, a high number of branches means more parasitics, degrading the resonant frequency as well. For these reasons, the number of branches is a sensitive variable that strongly



[a] [b]

Figure 3.17: After branches approach application: (a) Equivalent inductance (b) Real part equivalent

compromises the performance of the active inductor.

The main goal of the branches approach is to guarantee that the active inductor supports a current situated in the range of mA, while keeps a decent resonant frequency. Increasing the number of branches increases the total current as well. Nevertheless, as soon as the desired total current is achieved, it is still possible to continue the process of increasing the number of branches while decreasing the current allocated in each branch, keeping this way the same total current value. Reduce the current in each branch brings benefits because it allows a proportional transistor size reduction, resulting in an even smaller transistor, which contributes to the resonant frequency enhancement, as shown in the signal model analysis (section 3.2.3.1).

For instance, if each branch is biased at 500 μA, having the transistor M_1 with a width of W and length of L, it is possible to have an active inductor formed by 10 branches with a total current of 5 mA. Duplicating the number of branches to 20, keeping the 5 mA of the total current, the current in each branch is reduced to 250 μA, allowing the reduction of M_1 to $W/2$. This reduction will contribute to the resonant frequency increase. However, this improvement needs to be evaluated based on the resonant frequency decrease caused by the R value adjustment to support the inductance that is required in each branch to design 20 branches active inductor, which, considering a L_{eq} of 707 pH, would be 14.14 nH (following Eq.3.31).

Due to the complexity associated with the trade-off between the number of branches and the active inductor performance, the choice of the exact number of branches to be used in the active inductor is part of a final design stage. After the performed analyses, the number of branches is set to 30, since it is the number that demonstrated at this moment, the better overall result.

At this moment, as it is represented in Fig.3.17 (a), despite the slight reduction in the resonant frequency compared with the previous situation (Fig. 3.14) where it showed the frequency analysis of a single branch, the actual active inductor still has a decent resonant frequency while operating at mA current levels. Now that the imaginary part is behaving as it should, it is time to proceed with the adjustment of the real part.

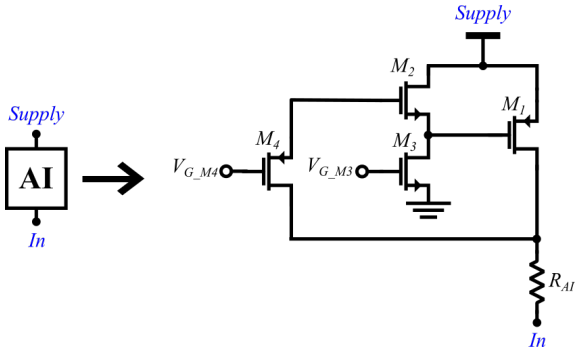


Figure 3.18: Scenario with N branches, each with a Lee's active inductor in series with a resistor

3.2.4 Real part analysis

Fig.3.17 (b) shows the equivalent real part of the active inductor, which is measured by considering only the real part of the equivalent impedance, according to the procedure of Fig.3.13. The equivalent real part represented in the plot is the inherent real part of the Lee's active inductor and is bellow the required resistance of 50 Ω, so it is needed an additional resistor, named R_{AI}, to guarantee that the active inductor meets this requirement.

As it was mentioned at the beginning of the section regarding the active inductor integration, (3.2.2) considering the main idea of shunt peaking, this resistor is inserted in series with the active inductor, as shown in Fig.3.18. Observing this configuration, it makes more sense to put the resistor near to the output node and the active inductor near to V_{DD}. Otherwise, in the case of the active inductor being near to the output node, as it is not directly connected to a fixed voltage, it can exhibit fluctuating behavior at the level of voltages, making it more difficult to ensure that the transistors operate in the intended region. In addition, there may be problems of body effect and it would increase the output node total capacitance due to the parasitics of the active inductor.

The actual design of the active inductor has an equivalent real part of approximately 36 Ω, so it is needed that the introduced resistor compensates the remaining 14 Ω to meet the requirement of 50 Ω. This way, since the active inductor, has 30 branches, each one with one resistor, as suggested in Fig.3.18, there are 30 resistors in parallel. Similarly to the equivalent inductance, the equivalent resistance, R_{eq} generated by the resistors in parallel, R_N, is given by Eq.3.32. Knowing that all the branches are equal, hence all the resistors are equal. Subsequently the resistor introduced in each branch, R_{branch}, is derived by Eq.3.33.

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + ... + \frac{1}{R_N} \tag{3.32}$$

$$R_{branch} = R_{eq} . N \tag{3.33}$$

Considering Eq.3.33, in order to compensate a 14 Ω of equivalent resistance, it is required a 420 Ω resistor to be inserted in each branch. After the resistor implementation and the correspond-

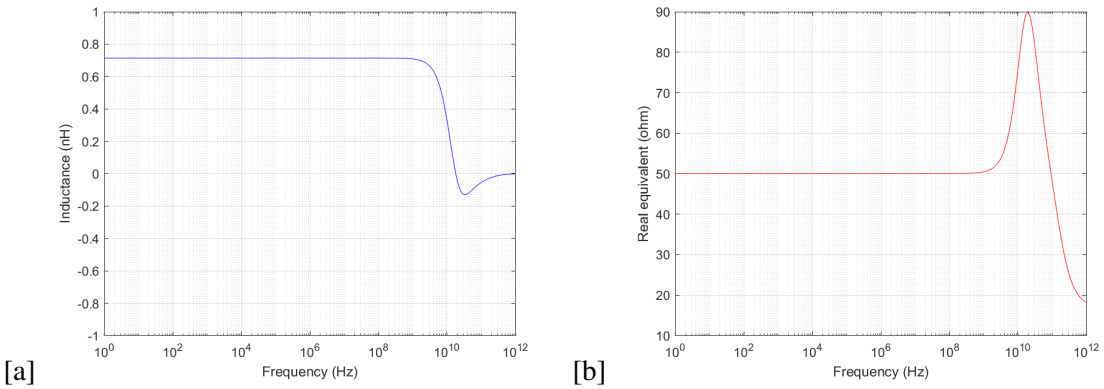


Figure 3.19: After resistor application: (a) Equivalent inductance (b) Real part equivalent

ing adjustments, a final resistor value of 490 Ω is achieved. The difference from the calculated value is due to the small biasing variations caused by the resistor application, thus causing at the same time small variations on the inherent resistance generated by the inductor. Fig.3.19 (a) shows that the resistor implementation had no impact on the equivalent inductance while Fig.3.19 (b) indicates that the equivalent real part is now set to 50 Ω.

At this stage, the active inductor is already meeting the requirements regarding the inductance and the real part. Ensure that the active inductor is doing the work while meeting all the biasing requirements is not a trivial process. However, it will be discussed in the next subsection.

3.2.5 Biasing adjustments

At this moment, the active inductor voltage drop is not enough to put M_0 in the linear region. Keeping the source-drain voltage of M_1, means that the resistor implemented to calibrate the real part must have a sufficient voltage drop to guarantee the output voltage at 0.4 V. With the voltages well defined and considering now the whole configuration, it is time to discuss what is influencing the active inductor biasing.

3.2.5.1 Current

At the beginning, the branches' approach was adopted with the main goal of increasing the total current. However, now that there is a desired operating point to maintain, the total current does not depend exclusively on the number of branches. In fact, it is the V_{sg} of transistor M_1 that has the most impact in setting the total current value. To keep the desired operating point while changing the number of branches, the total current must also be kept.

3.2.5.2 Inserted resistor

The real part analysis carried out in section 3.2.4, allowed to conclude that the value of the inserted resistor, R_{AI}, is linearly related with the number of branches, as demonstrated by Eq.3.33.

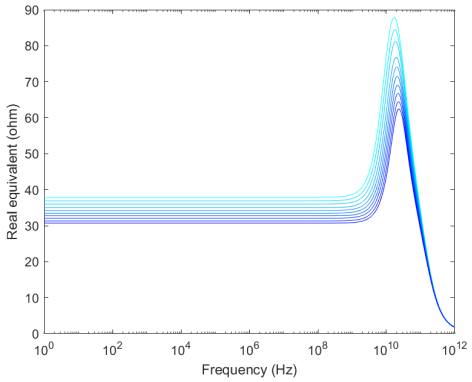


Figure 3.20: M_1 size sweep

However, considering the whole topology of the active inductor, this relationship may not be that perfect.

Although the source-gate voltage of M_1 is the main responsible for the current change, there is another factor that slightly contributes to causing biasing changes. Keeping V_{sg} of transistor M_1 and varying the number of branches, it is expected that the total current does not change. In fact, it suffers a small variation every time the number of branches is changed. This behavior is due to the M_1 sizing influence. In other words, reducing the number of branches means reducing the current in each branch. Thus, transistor M_1 can be designed to be smaller as it now supports lower current. However, as explained previously, the equivalent real part is constituted by the inserted resistor, R_{AI}, and the inherent resistance generated by Lee's active inductor. Reducing the size of transistor M_1 increases the inherent resistance. To calibrate the equivalent real part, R_{AI} must decrease to compensate for the inherent resistance change. As R_{AI} is designed to have a fixed drop voltage, the current will vary according to the variation of the resistor value.

This way, the value of the inserted resistor to calibrate the equivalent real part of the active inductor does not follow perfectly the variation in the number of branches. R_{AI} must suffer small adjustments every time the number of branches is changed due to the impact that the sizing variation of M_1 has on the inherent resistance. To this impact, as shown in Fig.3.20, a small test is carried out. The inherent resistance of the active inductor is measured, while doing a sweep to the size of M_1. The plot reveals that the smaller size of M_1 (lighter line) corresponds to higher resistance, whereas an M_1 transistor of larger size (darker line) corresponds to a lower real part.

If the value of this resistor should be adjusted, why not also adjust its position. Considering the main idea of shunt peaking, R_{AI} was inserted in series with the Lee's active inductor, as shown in Fig.3.18. However, this resistor could be inserted in another place besides the one considered, which is located outside the Lee's active inductor. In fact, it could be introduced in some place somewhere inside the Lee's active inductor, as shown in Fig.3.21. For instance, between the supply and the source of M_1, Fig.3.21 (a), or between the drain of M_1 and the output node, Fig.3.21 (b), or split the resistor between these two places, Fig.3.21 (c). There is still the possibility to join both

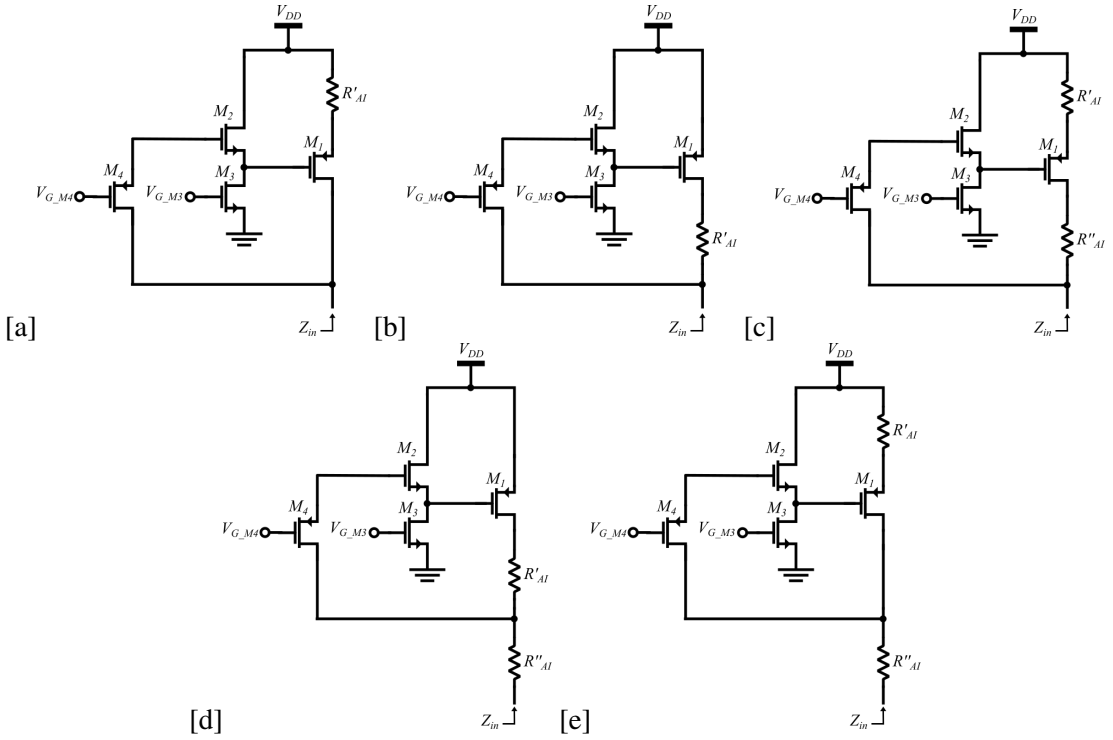


Figure 3.21: Application of the resistor inside the active lee inductor: (a) Between supply and source of M_1 (b) Between drain of M_1 and output node (c) Split the resistor and insert it in both places (d) Split the resistor and insert part of it between drain of M_1 and output node, and other part outside (e) Split the resistor and insert part of it between supply and source of M_1, and other part outside

approaches, and split the resistor and insert part of it inside of the active inductor and the other part outside of it, Fig.3.21 (d) and (e). These are all valid approaches that could even improve the final active inductor performance if they could ensure a correct configuration biasing.

Keeping in mind the initial topology, illustrated in Fig.3.18, as the V_{sd} of M_1 is just enough voltage to keep M_1 operating in saturation region, the gate of M_2 has enough voltage to keep transistors M_2 and M_1 in saturation as well. Following any of the alternative approaches, due to the drop voltage caused by the insertion of a resistor inside the Lee's active inductor, the voltage at the gate of M_2 is less than the previous V_{sd} of M_1, which results to the impossibility of keeping the transistors M_1, M_2 and M_3 in saturation at the same time.

There may be a configuration that consists of putting part of the resistor inside the Lee's active inductor between the supply and the source of M_1 and the other part outside of the Lee's active inductor, which is represented in 3.21 (e). This approach can put all of those transistors in saturation but with the cost of having a very narrow saturation margin. Additionally, it does not improve the final active inductor performance, as it only allows low source-gate voltages of M_1, which is not advantageous for the resonant frequency, as it will be discussed in the next subsection.

Hence, as analyzed, there are no advantages in inserting the resistor in another place or even split the resistor to insert each part in different places. Besides that, it would be required to

fabricate two resistors (perhaps different) for each branch instead of only one.

3.2.5.3 Resonant Frequency

The previous imaginary part analysis, in section 3.2.3, evaluated the impact that each transistor parameter has in the imaginary part. To ensure the best resonant frequency, it was concluded that gm must be higher than gds, and this latter must be kept small. As expected, the intrinsic capacitances should be kept as low as possible. Taking these conclusions into account, and considering now the whole active inductor configuration, the idea is to find the optimal value of biasing that guarantees a high resonant frequency value.

The best solution to keep the intrinsic capacitances value low is to reduce the transistor M_1 size, by increasing the number of branches. Regarding gds and gm, as the V_{sd} of transistor M_1 is fixed, is the V_{sg} that will set these two parameters. The conventional definitions of the transconductance, gm, and drain to source transconductance, gds, are given by Eq.3.34. Considering these formulas, as the V_{sd} is fixed, to ensure that gds is small, the current must not be at the maximum value while there is a range of V_{sg} values that guarantee that gm is greater than gds. This way, there is a specific value of V_{sg} that must not be exceeded. Thus, it is possible to infer that the value of V_{sg} plays a critical role in obtaining the optimal biasing point that ensures the best possible resonant frequency. Since that the source is directly connected to V_{DD}, the source-gate voltage of M_1 is set by the voltage at the gate of the transistor, which is defined by the level shifter. Therefore, transistors M_2 and M_3 (that constitute the level shifter), must be designed to set the required voltage at the gate of M_1. Note that, while sizing these two transistors, it is important to realize that the intrinsic capacitances of the transistors affect the total capacitance at the gate of M_1, degrading this way the resonant frequency. In conclusion, the level shifter must be sized to ensure a specific voltage at the gate of M_1, which guarantees the desired gm and gds values, while using the smallest possible transistors.

$$gm = \frac{\partial I}{\partial V_{gs}} \quad gds = \frac{\partial I}{\partial V_{ds}} \tag{3.34}$$

3.2.5.4 Number of branches

As mentioned previously, due to the complexity associated with the impact of the number of branches on the overall performance of the active inductor as well as the trade-off between power consumption, used devices and improvements obtained, this is a variable that will be defined in a final stage of the design of the inductor.

3.2.5.5 Inductance

Even with the active inductor integrated into the desired scenario, it is possible to conveniently adjust the inductance value just by varying the gate voltage at the gate of transistor M_4, independently of the operating point of the configuration.

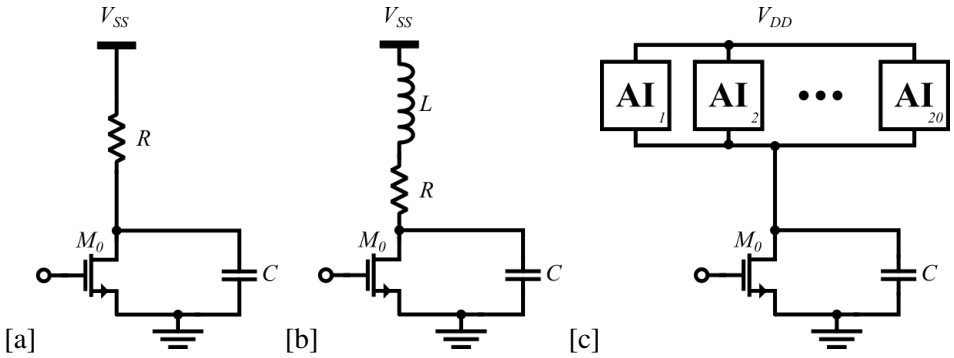


Figure 3.22: Common source test scenarios: (a) Simple (b) With ideal inductor (c) With designed active inductor

3.2.6 Bandwidth enhancement

Taking into account all the conclusions obtained in the process of integrating the active inductor, during the imaginary part analysis (section 3.2.3) and the real part analysis (section 3.2.4), and considering the biasing adjustments (section 3.2.5) that improves the performance of the final active inductor while meets the requirements described in the chapter 1, it is finally achieved an active inductor design that is able to operate successfully in the suggested scenario.

The final active inductor design is operating with a total current of approximately 12 mA. As shown in Fig.3.22 (c), it is constituted of 20 branches, as it gave a good trade-off in terms of the size of M_1 allowing for an acceptable bandwidth. Each branch with the Lee's active inductor topology in series with a resistor, as it is represented in Fig.3.23. The transistors sizes guarantee the desired operation point as well as the optimal value of V_{sg} of transistor M_1, which corresponds to the highest possible resonant frequency. Now that the active inductor is ready to operate, it is time to measure the design performance.

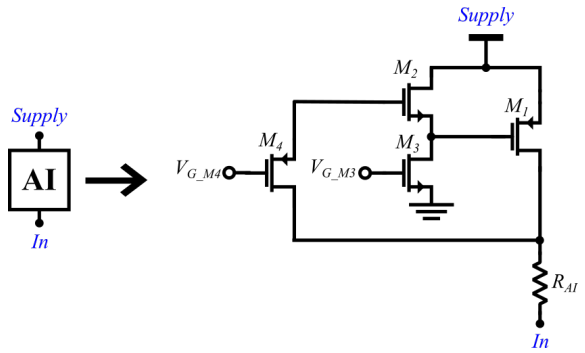


Figure 3.23: Proposed AI topology: Lee's active inductor in series with a resistor

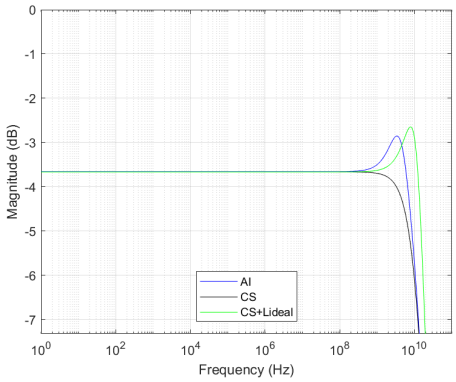


Figure 3.24: AC analysis of the three cases

3.2.6.1 AC Analysis

An AC analysis will be carried out in order to measure the respective bandwidth enhancement caused by the inductor at the desired operating point. Fig.3.22 shows the three test scenarios that will be considered during this AC analysis. The case represented in Fig.3.22 (a) is a simple uncompensated common source with a capacitor associated with the output node and a resistor load of 50 Ω, while Fig.3.22(b), is the case where an ideal inductor is applied to the common source. As discussed previously, in order to effectively compensate the capacitor, this ideal inductor must generate 707 pH. Lastly, Fig.3.22 (c) represents the application of the designed active inductor that, hopefully, will compensate the output node capacitance.

As in case (c), in contrast to Fig.3.22 (a) and (b), there will always be losses caused by the active elements, in order to guarantee a fair comparison, note that both cases (a) and (b) are supplied by a different voltage source, named V_{ss}. The value of this source is calculated by adding the exact output voltage of the case (c), V_{out_C}, adding the drop voltage caused by the multiplication of the total current in (c), I_C by the resistor of 50 Ω, as it is suggested by Eq.3.35. This way, it is ensured that transistor M_0 is working in the same conditions for each case.

$$V_{ss} = V_{out_C} + I_C R \tag{3.35}$$

The results of this first AC analysis are shown in Fig.3.24. The black, green, and blue lines correspond to Fig.3.22 (a), (b), and (c), respectively. The application of the active inductor brings a small bandwidth extension, approximately 1.05x, compared to the uncompensated case. Observing the plot, it is possible to conclude that it has an undesired peaking that be affecting the bandwidth negatively. A peaking excess could be a signal of an inductor that has too much inductance for the context where it is applied.

In order to reduce the undesired peaking, the inductance value can be regulated by adjusting the voltage at the gate of M_4. Fig. 3.25 (a) shows the result of a sweep to the voltage applied to the gate of M_4, with the lower and higher voltage represented by the lighter and darker lines, respectively. This leads to the conclusion that there is a specific gate voltage value that makes the

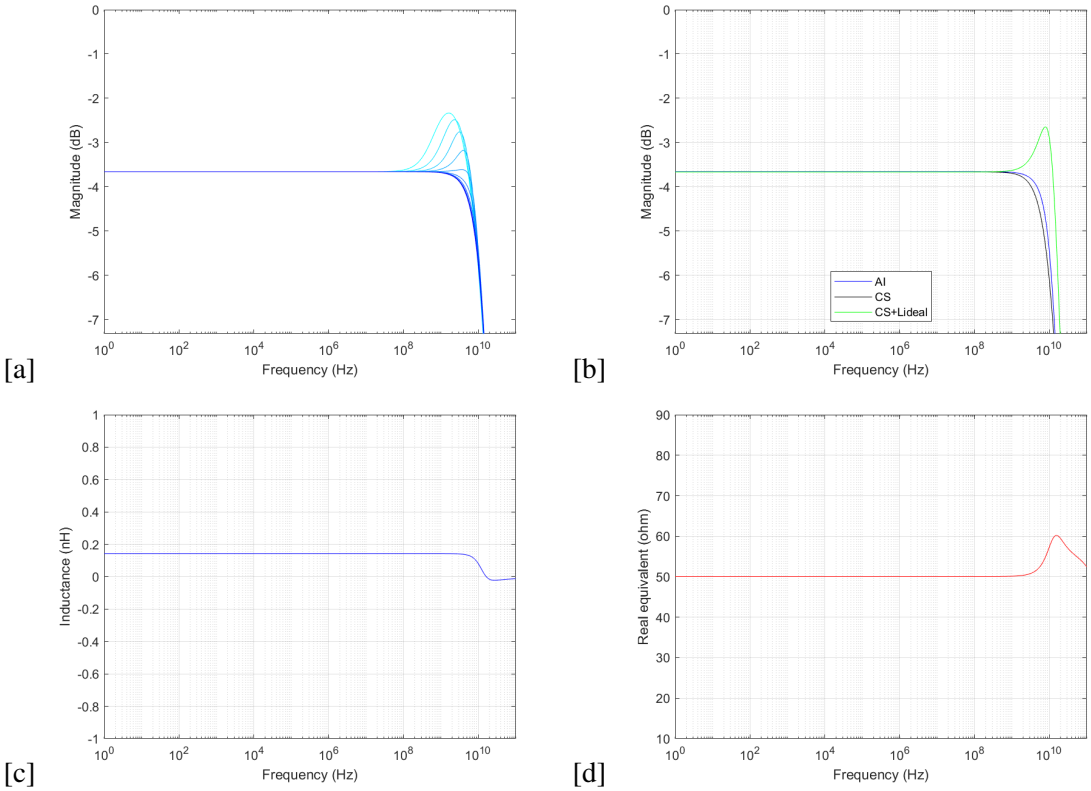


Figure 3.25: (a) Sweep of the voltage at the gate of M_4, lighter and darker lines correspond to the lower and higher applied voltage value, respectively (b) AC analysis of the tree cases after the inductance adjustment of the AI (c) Final equivalent inductance of the AI (d) Final real equivalent of the AI

active inductor to generate a specific inductance value that achieves the highest possible bandwidth value. Fig.3.25 (b), shows the result of this inductance adjustment, leading to a BW improvement of approximately 1.12x compared to the uncompensated case. Fig. 3.25 (c) and (d) shows the final behavior of the active inductor regarding the equivalent inductance and real part, respectively.

While the real part is meeting the requirement of 50 Ω, the equivalent inductance that guarantees higher bandwidth appears to be much less than expected. Since that the expected L of 707pH was calculated by considering the expression $L = mR^2C$, with a ratio m equal to $\sqrt{2}$, it seems that something is affecting the ideal m for which is achieved the maximum bandwidth extension. Recalling the equivalent *RLC* circuit for the lee configuration, represented in Fig. 3.7 (b), it is noticeable that there is a capacitor in parallel with the inductor. This capacitor corresponds to the intrinsic capacitance of transistor M_1 between the drain and the source, C_{ds}. Despite the reduced value of C_{ds}, it may be the reason for this inconsistency between the calculated and obtained equivalent inductance value.

Following the test carried out at the beginning of the active inductor integration, in section 3.2.2 (Fig.3.26 (a) and (b)), which was intended to prove the value of the m ratio to be used, it is considered now a third case, where it is inserted a capacitor of $C * k$ value (being C the

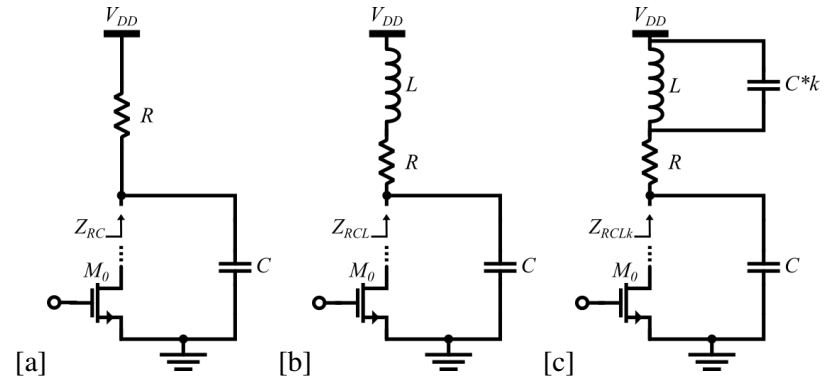


Figure 3.26: Small test to prove the ratio value (a) RC circuit (b) RCL circuit (c) RCL circuit with inserted parallel capacitor

capacitance at the output node) in parallel with the inductor, as Fig.3.26 (c) suggests. Actually, this configuration (c) is known as Bridged-shunt-peaking, as discussed in the Background, in section 2.2.3.1. The equivalent impedance of the case represented in Fig.3.26 (c), Z_{RCLK}, can be obtained through Eq.3.36 that results in the final expression of the equivalent impedance, Eq.3.37.

$$Z_{RCLK} = (R + (sL \,//\, \frac{1}{sC*k})) \;\; // \;\; \frac{1}{sC} \tag{3.36}$$

$$Z_{RCLK} = \frac{s^2\, C\, k\, L\, R + s\, L + R}{s^3\, C^2\, k\, L\, R + s^2\, (\, C\, k\, L + C\, L\,) + s\, C\, R + 1} \tag{3.37}$$

Compared to the second case, the capacitor in parallel with the inductor introduced another pole and zero in the equivalent impedance. To understand the impact that the inserted capacitor has on the impedance, and keeping the ratio $m = \sqrt{2}$, it is performed a sweep to the k value, as represented in Fig.3.27. The result of this simulation leads to the conclusion that the higher the value of k, the greater the peaking. This way, as in the case of Fig.3.26 (b) $K = 0$ and $m = \sqrt{2}$, in case of Fig.3.26 (c), to the same m ratio, a k greater than zero will contribute to an undesired peaking increase causing the degradation of the resonant frequency. As discussed previously, the observed peaking is also directly related to the inductance value. This way, the reduction of the inductance is a solution to compensate for the peaking increase caused by the k value increase.

After this small test, analyzing once again Fig.3.25 (c), the reduced equivalent inductance observed is due to the value of C_{ds} that is in parallel with the inductor, which introduces an inconvenient peaking that degrades the resonant frequency. The undesired peaking is adjusted by reducing the equivalent inductance value of the active inductor. Transistor M_4 is now operating as a resistor of 77 kΩ.

Table 3.1 summarizes the last performed AC analysis. In the end, the designed active inductor accomplishs the main goal for what it was designed, which is to extend the bandwidth. However, since it brings a small improvement with the cost of adding an extra power consumption to the scenario where the AI is implemented, it could not be a viable solution. Nevertheless, before discarding this option, first, it is analyzed in the time domain.

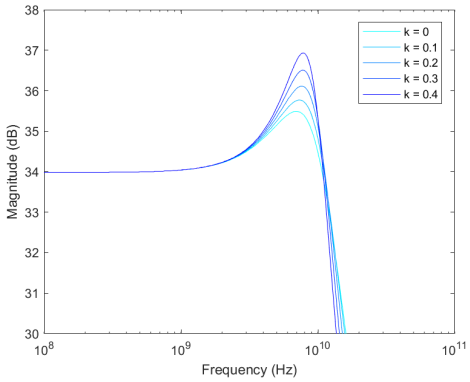


Figure 3.27: Z_{RCLK} behavior with k value sweep between 0 and 0.4 with step of 0.1

3.2.6.2 Transient Analysis

In order to observe the behavior of the active inductor when turned *on* and *off*, transient analysis is carried out, taking into account the same three scenarios that were considered in the previous AC Analysis, shown in Fig.3.28 (c).

When analyzing the plot referring to the rise time, Fig.3.28 (a), which corresponds to when the active inductor is turned *off*, there seems to be no difference between the scenario with the AI and the case of the non-compensated common source. Regarding the fall time plot, Fig.3.28 (b), there is a slight improvement.

Table 3.2 summarizes the performed transient analysis. When turned *on*, the active inductor contributes slightly to reduce the time needed to execute the transition. However, when turned *off*, the AI appears to be ineffective. Thus, it is not a good implementation to a scenario where the transition times are of crucial importance.

3.3 Summary

Throughout this chapter, several active inductor configurations were analysed, such as the folded active inductor and Lee's topology.

The folded active inductor avoids the problem of having a significant voltage drop by using just an NMOS transistor with a resistor connected to the gate, achieving a good inductance value during a wide frequency range. However, it does not suit so well when integrated into the desired

Table 3.1: AC analysis summary (after inductance adjustment)

Fig.	Case	BW (GHz)	BW Extension
(a)	CS	11.46	1.00 x
(b)	CS+Lideal	18.19	1.59 x
(c)	AI	12.86	1.12 x

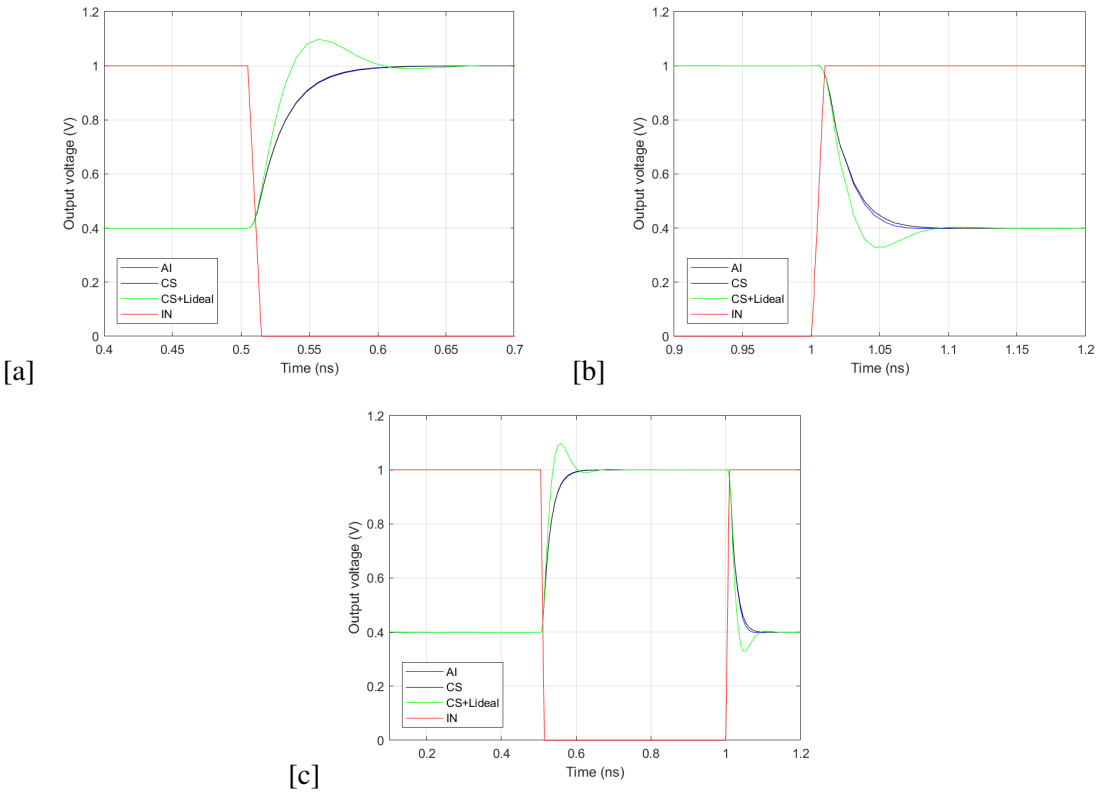


Figure 3.28: Transient analysis: (a) Rise (b) Fall (c) Geral

Table 3.2: Transient analysis summary

Fig.	**Case**	**Rise (ps)**	**Rise Time improvement**	**Fall (ps)**	**Fall Time improvement**
(a)	CS	28.4	1.00 x	22.8	1.00 x
(b)	CS+Lideal	19.6	0.69 x	16.3	0.71 x
(c)	AI	28.8	1.01 x	21.9	0.96 x

shunt peaking scenario, since that it only could be applied considering a $R \,//\, L \,//C$ approach, which is not a good option to extend the bandwidth.

On the other hand, Lee's active inductor is a viable option to implement the shunt peaking technique. However, the integration of this active inductor turned into a lengthy process that involved the analysis of the imaginary part and the real part, followed by the integration in the intended scenario. Finally, AC and Transient analyzes were carried out. During the imaginary part, it was observed the impact of each parameter in each AI performance criteria, with emphasis on inductance and resonant frequency. After the imaginary part is according to the objectives, in order to guarantee a current at the range of mA, a branches solution was considered. Then, it was inserted a resistor to calibrate the real part and ensure that the equivalent real part was meeting the requirement of 50 Ω. At that moment, the active inductor design was already fulfilling some requirements. It was then integrated into the proposed scenario, which required a careful analysis regarding the sizing of the transistors in order to obtain an optimal performance, while the biasing is ensuring that the active inductor is at the required operating point. In the end, an AC analysis was performed, indicating the designed AI was extending the bandwidth in a relation of 1.12 compared to the uncompensated case. Finally, the time domain was observed. When turned *off*, the AI appeared to be ineffective in contrast to when turned *on*, which demonstrated a slight reduction in the fall time.

The series of Lee's topology with a resistor is an interesting active inductor configuration. Despite not being considered a good option to the proposed scenario due to the slow transitions, it could be a starting point to the final solution.

Chapter 4

Simple AI

The previous chapter presented several interesting shunt peaking approaches. One of them, the Lee's active inductor, inspired the design of a novel approach to the use of a simple AI (active inductor), which is presented in this chapter. A careful analysis of Lee's active inductor was carried out, indicating that the series of a resistor with active inductor is a solution to the described scenario, but probably not the most viable. Taking into account this conclusion, it is possible to take Lee's topology as a starting point to reach the final solution.

4.1 Topology Conception

Observing, once again, the AI solution designed in the previous chapter, which is constituted by a Lee's active inductor in series with a resistor, R_{AI}, as shown in Fig.4.1 (a), there may be a way to change the configuration in order to improve the final BW results.

Since that the Lee's active inductor was designed to be applied in environments that require an AI that cause low voltage drop, this topology has a level shifter, consisting of a source follower M_2 and a current source M_3, to guarantee a low voltage at the gate of M_1 and, at the same time, a high voltage at the output node. This way, transistor M_1 is operating in saturation while the Lee's active inductor has a low drop voltage (that corresponds to the drain-source voltage of transistor M_1). Since the target scenario where the AI will be applied will have to reach low output voltages, it can afford to have some voltage drop across the designed active inductor. Therefore, as the voltage at the output node is already low, the need to use a level shifter to reduce the voltage between the output node and the gate of M_1, can be evaluated. If those transistors that make up the level shifter are, in principle, not needed, they are only contributing to the increase in capacitance at the gate of M_1, which degrades the resonant frequency, as discussed in 3.2.3. There is also an extra static power consumption that is needed to make the active inductor work, as the level shifter branch means extra current consumption.

Fig.4.1 (b) shows the resulting configuration after the level shifter removal, which is nothing less than the PMOS version of the Simple Active inductor mentioned in the chapter 2 (2.5.1), in series with a resistor. Despite the clean appearance, this configuration does not work. Assuming

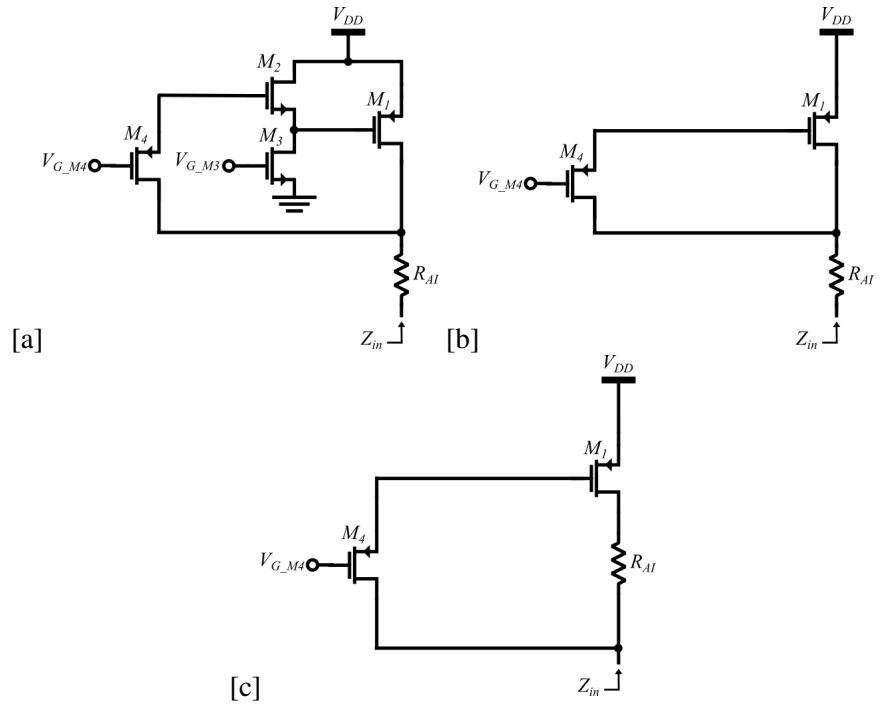


Figure 4.1: (a) AI solution designed in the chapter 3 (b) Level shifter removal that results in the PMOS version of the simple AI in series with a resistor (c) Novel simple active inductor approach

that V_{sd} of M_1 is fixed at a voltage less than to V_{th}, the V_{sg} of M_1 (that is equal to V_{sd}) is not high enough to ensure that the transistor is in saturation. To avoid this problem, V_{sd} of M_1 would be required to be greater than or equal to V_{th} of the PMOS transistor, which would make the active inductor to cause a large voltage drop, leaving a very low voltage range for resistor R_{AI}. It seems now that there is a problem in the AI voltage drop regulation, which was expected since the transistors that were doing that job were removed.

In order to solve this problem, resistor R_{AI} is moved into the feedback, as Fig.4.1 (c) suggests. The output node (that is at 0.4V) is now directly connected to the gate of M_1, which ensures that V_{sg} is always higher than V_{th}. This way, considering that V_{sd} of M_1 is unchanged, the transistor M_1 is operating in the saturation region, while there is enough voltage headroom for resistor R_{AI}. After these changes, it is reached a novel fully operational approach to use the simple active inductor.

4.2 Biasing Adjustments

The complexity associated with the biasing process of the new approach of the simple AI is reduced compared to the AI solution designed in the previous chapter. The main reason for that is the established voltage at the gate of M_1, which is equal to the output voltage (0.4 V), due to the level shifter removal. It is considered the same V_{sd} of M_1 that was used for the previous implementation.

As the voltages are well defined, the role of ensuring a correct biasing is up to two parameters, the value of the inserted resistor and the M_1 size. Keeping in mind that reducing transistor M_1 size, is beneficial to the resonant frequency, these two parameters are designed considering the

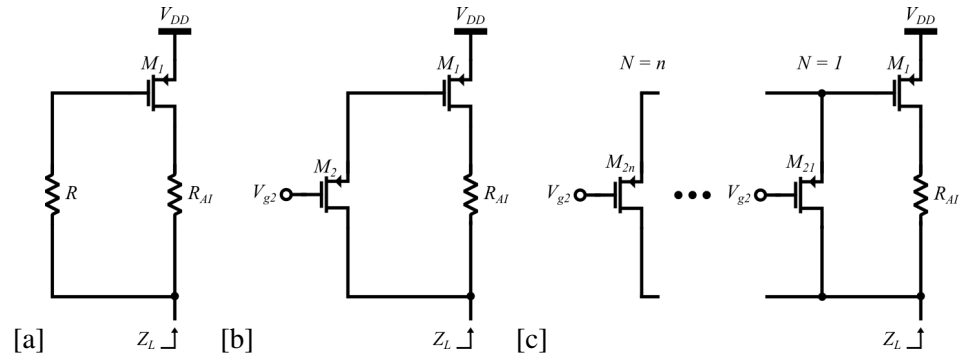


Figure 4.2: Novel approach of the simple AI concept considering: (a) A resistor R (b) PMOS M_2 (c) n transistors PMOS in parallel

minimum possible size of M_1 that guarantees the desired voltages. This way, the size of M_1 is reduced in a proportion of approximately 2/3 compared to the size of M_1 of the solution presented in the chapter 3.

Taking into account the discussed biasing adjustments, similarly to the solution of the previous chapter, the number of branches is kept at 20 branches, as it gave a good trade-off in terms of the size of M_1 allowing for an acceptable bandwidth. As a result, a final design of the simple active inductor is achieved, which ensures the desired operating point while meeting the requirement regarding the equivalent real part, which must be at 50 Ω. The total current is approximately 4.5 mA, in contrast to the approach represented in Fig.4.1 (a), which has approximately 12 mA. Since they are different topologies, in which both present the same real equivalent part as well as the same output voltage, as a result, the current will be different in each solution.

Transistor M_4 is operating in the linear region as before, allowing to regulate the equivalent inductance value of the AI, just by changing the voltage at the gate of M_4. As discussed previously, it is not trivial to find the theoretical components ratio that guarantees maximum bandwidth, since there are factors such as the C_{ds} of transistor M_1 that also have impact on this ratio value. Thus, the optimal inductance value that achieves maximum bandwidth extension will be measured during the next AC analysis. To reduce the complexity of the referred measurement, PMOS M_4 will be replaced by a resistor R, as Fig.4.2 (a) suggests. Then, it will be performed a sweep to the value of the new resistor, which will have a specific value that ensures maximum bandwidth extension, corresponding to the optimal inductance value.

4.3 AC analysis

The result of the first AC simulation is shown in Fig.4.3 (a), which consists of performing a sweep to R value between a minimum (lighter line) and a maximum value (darker line). The bandwidth is measured for each value. In order to achieve an exact R value, this procedure is repeated considering a shorter sweep range in each simulation. This way, the optimal R value is obtained, which is 10.5 kΩ, ensuring a bandwidth of 13.89 GHz. The simple AI is now operating

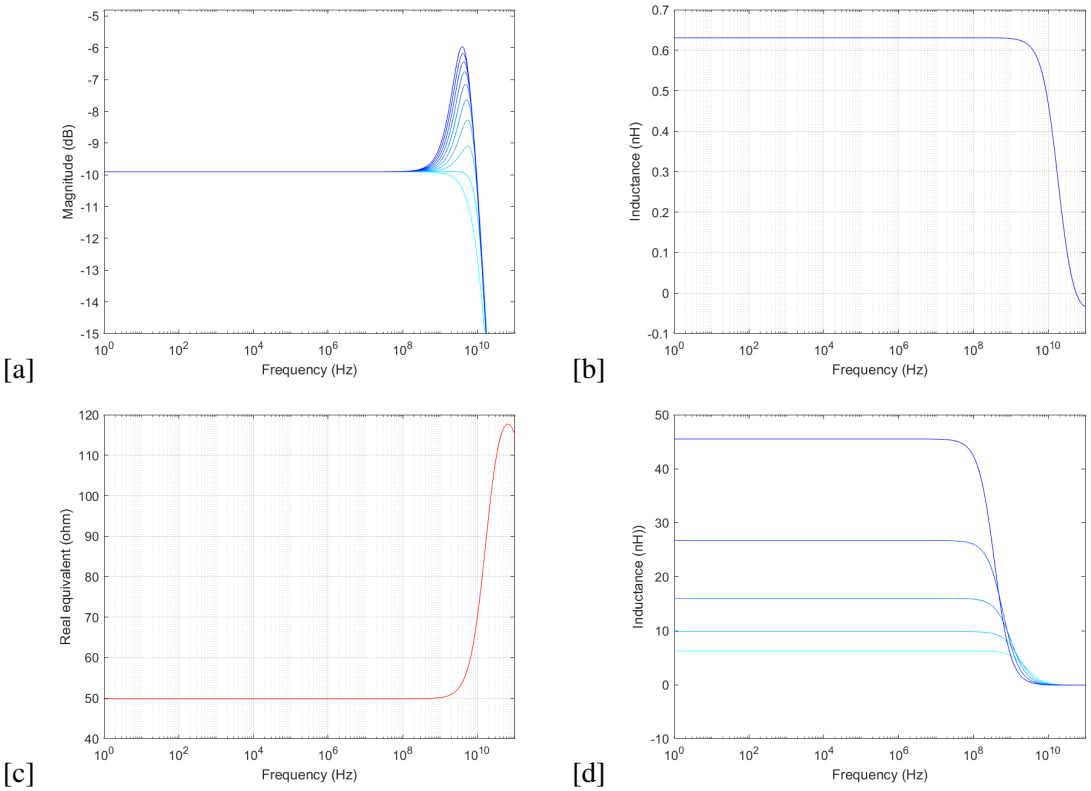


Figure 4.3: (a) R sweep between a minimum and a maximum value, lighter and darker lines, respectively (b) Equivalent inductance of the simple AI with optimal R value (c) Equivalent real part of the simple AI with optimal R value (d) Sweep of the voltage at the gate of PMOS M_4 between a minimum (0V) and a maximum value, lighter and darker lines, respectively

at the maximum performance, having an equivalent inductance of approximately 630 pH and a real part of 50 Ω, represented in Fig.4.3 (b) and (c), respectively.

However, the design process is not finished. Now that it is known the optimal inductance value, resistor R needs to be converted again into transistor M_4, as shown in Fig.4.2 (b). A sweep to the voltage at the gate of PMOS M_4 was performed, and it is represented in Fig.4.3 (d), where the lighter and darker line represents the minimum value and a maximum value, respectively, at the gate of M_4. Observing the plot, it is possible to conclude that even considering the minimum possible voltage at the gate of M_4, the simple AI still has an equivalent inductance of approximately 6 nH, which makes the desired optimal inductance value unreachable.

The solution to obtain a range of reduced inductance values may be to insert transistors PMOS in parallel with M_4, as suggested in Fig.4.2 (c). If using one PMOS, it is possible to achieve a minimum of 6 nH, theoretically, to reach an inductance of 630 pH would be necessary at least 7 PMOS in parallel. It seems that achieving the optimal inductance value comes at a high cost. In fact, using PMOS transistors to obtain a reduced equivalent resistance could not be the smartest approach. As it is known, due to the higher electrons mobility, the NMOS transistor usually has higher gds compared to a PMOS in the same conditions. Therefore, higher gds corresponds to

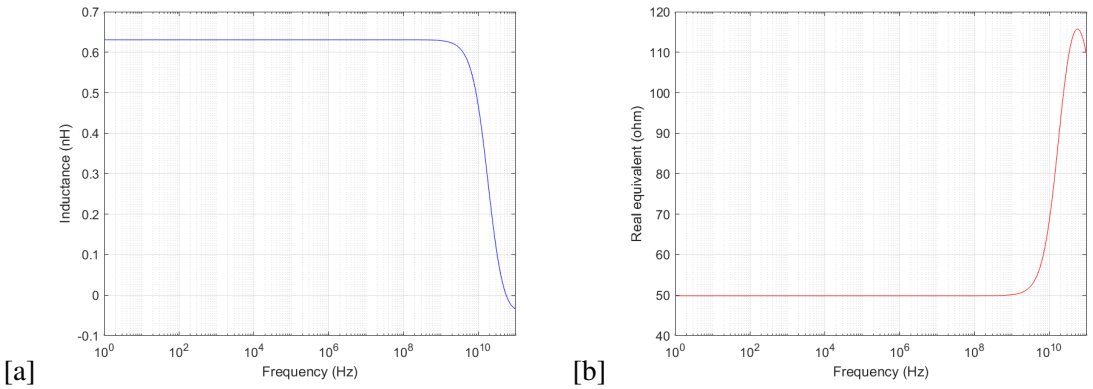


Figure 4.4: (a) Final equivalent inductance of the simple AI (b) Final equivalent real part of the simple AI

lower output resistance. This way, by replacing the resistor R with only one NMOS transistor, as shown in Fig.4.5 (d), it is possible to obtain the desired inductance. Fig.4.4 (a) and (b) shows the final equivalent inductance and real part, respectively, of the simple AI after the discussed modifications and adjustments.

The designed simple AI is now ready to be tested. Similarly to the AC analysis carried out in the previous chapter (3.2.6.1), it is considered the same test scenarios. A case formed by a simple uncompensated common source with a capacitor associated with the output node resistor load of 50 Ω, as shown in Fig.4.5 (a), and another case where the common source is compensated with an ideal inductor, represented in Fig.4.5 (b). Note that the value of the source voltage Vss is different from the simulations carried out in the previous chapter, as well as the M_0 size since the current is now set at 4.5 mA. This way, it is ensured that transistor M_0 is working in the same conditions in each test case.

The results of the performed simulation are shown in Fig.4.6 and summarized in Table.4.1. The black, green, and blue lines correspond to the case represented in Fig.4.5 (a), (b), and (c), respectively. The application of the simple AI brings an impressive bandwidth extension, approximately 1.46x, compared to the uncompensated case.

Before moving on to time-domain simulations, first, a small-signal analysis is performed to understand why this new topology achieves higher bandwidth than the one designed in chapter 3.

Table 4.1: AC analysis summary - Simple AI

Fig.	**Case**	**BW (GHz)**	**BW Extension**
(a)	CS	9.49	1.00 x
(b)	CS+Lideal	16.40	1.73 x
(c)	AI	13.81	1.46 x

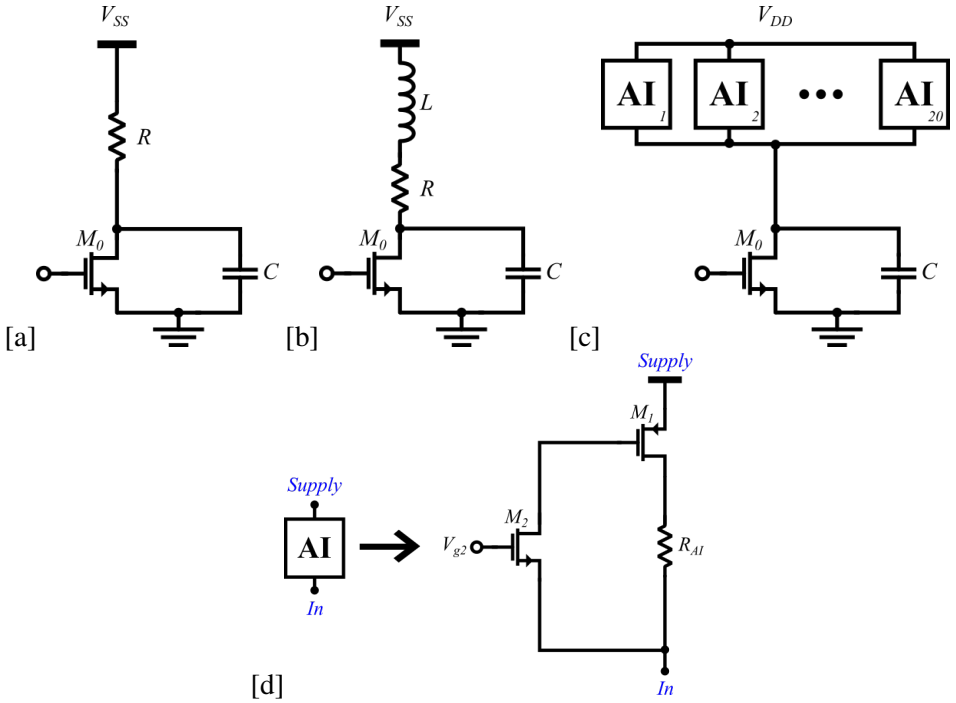


Figure 4.5: Common source test scenarios: (a) Simple (b) With ideal inductor (c) With simple AI (d) Each branch of the simple AI

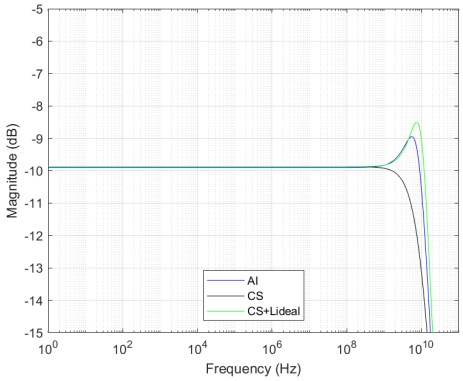


Figure 4.6: AC analysis result - Simple AI

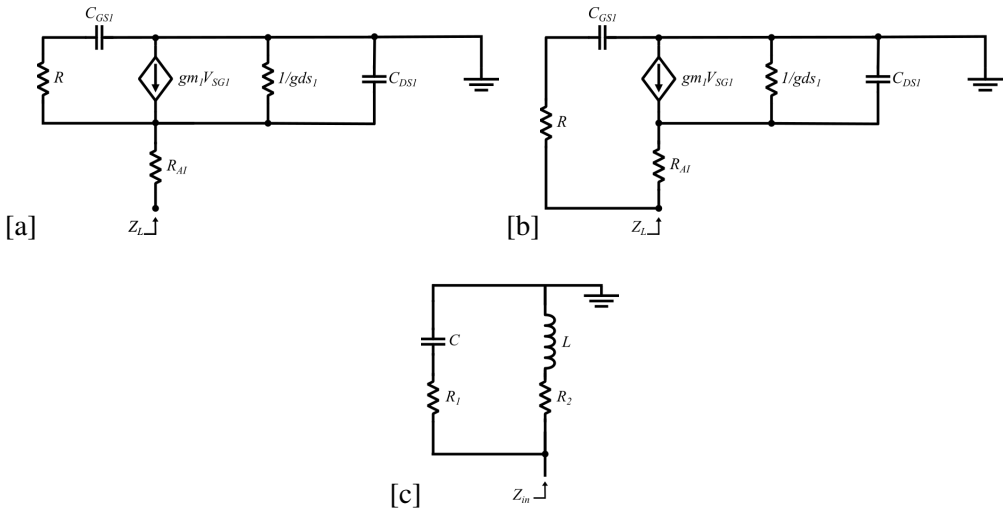


Figure 4.7: Small signal model: (a) AI solution designed in the chapter 3 (b) Simple active inductor approach (c) *RLC* simplified model

4.4 Small Signal Analysis

4.4.1 Transfer function & Resonant frequency

During this analysis, we neglect C_{gd} of transistor M_1. Considering gm, gds, C_{gs} and C_{ds} inherent parameters of transistor M_1 and R representing the transistor M_4, assuming that the level shifter has a unity AC gain, the small signal model of the configuration represented in Fig.4.1 (a) is shown in Fig.4.7 (a). Similarly, the simple AI approach, which is represented in Fig.4.1 (c), has the equivalent small signal model presented in Fig.4.7 (b). It is visible that both small signal models are identical, except in the position of the resistor R_{AI}.

The equivalent impedance of the AI solution designed in the previous chapter and of the simple AI approach is given by Eq.4.1 and Eq.4.2, respectively. The detailed deduction of these equations is presented in section A.1 of appendix A.

$$Z_{in} = \frac{s^2\,(C_{gs}\,R\,R_{AI}\,C_{ds}) + s\,(C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI} + R_{AI}\,C_{ds}) + R_{AI}\,(gm + gds) + 1}{s^2\,(C_{gs}\,R\,C_{ds}) + s\,(\,C_{ds} + C_{gs}\,gds\,R + C_{gs}) + gm + gds} \tag{4.1}$$

$$Z_{in} = \frac{s^2\,(C_{gs}\,R\,R_{AI}\,C_{ds}) + s\,(C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + R_{AI}\,C_{ds}) + R_{AI}\,gds + 1}{s^2\,(C_{gs}\,R\,C_{ds} + C_{gs}\,R_{AI}\,C_{ds}) + s\,(\,C_{ds} + C_{gs}\,gds\,R + C_{gs}\,gds\,R_{AI} + C_{gs}) + gm + gds} \tag{4.2}$$

Analyzing the denominator of both transfer functions, and considering the characteristic equation of a second-order system, represented in Eq.4.3, it is possible to achieve the resonant frequency of the series of the resistor with the Lee's AI, ω_{lee_0} (Eq.4.4), as well as the resonant frequency of the simple AI ω_{simple_0} (Eq.4.5). The latter equation suggests that moving the resistor into the feedback could reduce the resonant frequency compared to the former equation. However,

Table 4.2: Components of *RLC* model

Chapter 3 AI design	**Novel Simple AI**
$L = \frac{C_{gs}\,(\,R\,R_{AI}\,gds+R+R_{AI}\,)}{gds+gm}$	$L = \frac{C_{gs}\,(\,R\,R_{AI}\,gds+R\,)}{gds+gm}$
$C = \frac{C_{gs}\,(\,gds\,R+1\,)}{R_{AI}\,(gds+gm)+1}$	$C = \frac{C_{gs}\,(\,gds\,R+gds\,R_{AI}+1\,)}{R_{AI}\,gds+1}$
$R_1 = \frac{R\,R_{AI}\,gds+R+R_{AI}}{gds\,R+1}$	$R_1 = \frac{R\,R_{AI}\,gds+R}{gds\,R+gds\,R_{AI}+1}$
$R_2 = \frac{R_{AI}\,(gds+gm)+1}{gds+gm}$	$R_2 = \frac{R_{AI}\,gds+1}{gds+gm}$

this statement is valid if both configurations have exactly the same biasing conditions, which is not the case. Thus, all the involved parameters have different values in each configuration.

$$s^2 + 2\,\delta\,\omega_n^2\,s + \omega_n^2 \tag{4.3}$$

$$\omega_{lee_0} = \sqrt{\frac{gm+gds}{C_{gs}\,C_{ds}\,R}} \tag{4.4}$$

$$\omega_{simple_0} = \sqrt{\frac{gm+gds}{C_{gs}\,C_{ds}\,(\,R+R_{AI})}} \tag{4.5}$$

Since the value of R is much higher in the configuration proposed in chapter 3 compared to the simple AI topology, observing Eqs.4.4 and 4.5, it is possible to conclude that the new solution is the approach that presents the highest resonant frequency. This explains the good performance observed in the previous AC analysis.

4.4.2 Equivalent *RLC* model

To better understand the value of R as well as the value of the other components in each topology, it is analysed the respective *RLC* models. Both configurations can be converted to the same *RLC* simplified model, which is represented in Fig.4.7 (c). Table 4.2 shows the expressions of each constituent component of each model. For the detailed deduction of the *RLC* model as well as the involved components, please consult section A.2 of Appendix A.

Due to reasons of confidentiality, the values of the parameters inherent to the transistors cannot be provided, and consequently the values of the components involved in the *RLC* models are not available to the reader. However, even considering the values, the equivalent *RLC* model proved

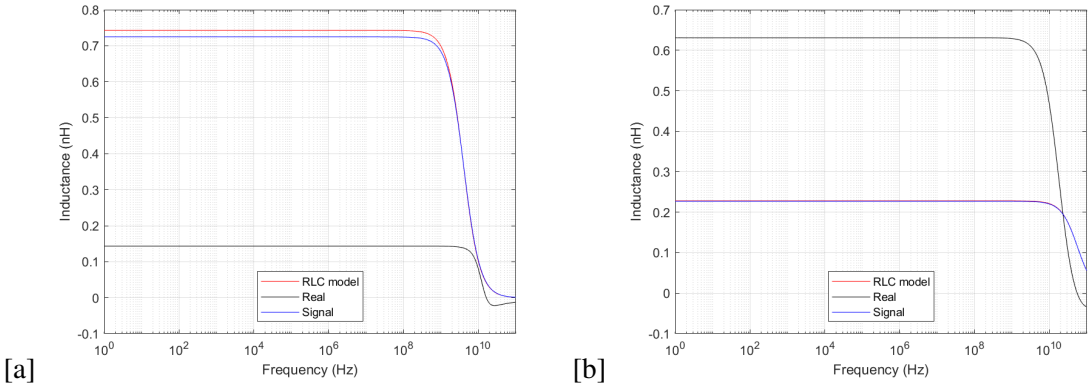


Figure 4.8: Simulation to compare: *RLC* model vs Signal model vs Real model (a) Solution proposed in chapter 3 (b) Simple AI

to be useless to explain the values associated with each configuration. This calls into question the validity of the deduced *RLC* model.

In order to test the accuracy of the *RLC* model, in addition to an analytical review, it is performed a simulation to compare the small signal topologies represented in Fig.4.7 and the equivalent *RLC* model, suggested in Fig.4.7 (c) considering the components values indicated in Table 4.2. The results of this simulation are represented in Fig.4.8. Despite the small differences observed in Fig.4.8 (a), that are due to rounding reasons, it is visible that the *RLC* model is similar to the signal model, which makes the *RLC* model an accurate representation of the small-signal model. Additionally, both models are also compared to the real configuration. Observing the plots, it is possible to conclude that the problem seems not to be in the *RLC* model, but in the signal model, which is not representing the real model so well.

4.4.3 Small Signal Models Analysis

The reason for the observed difference may be associated with intrinsic capacitance that are not being considered, and that have a relevant impact on the behavior of the active inductor. In order to better understand what is missing, an analysis is made of both signal models.

4.4.3.1 Simple AI solution

Since the simple AI provides a slightly simpler analysis compared to the approach presented in the previous chapter, it is analysed first the new solution. To evaluate the contribution of the mentioned intrinsic capacitances it is considered now the small-signal model represented in Fig.4.9 (a). The result of the simulation of this model, that is shown in Fig.4.10 (a), indicates that it is closer to the real configuration. This confirms the significant impact of the intrinsic capacitors in the performance of the active inductor. For this reason, there is still room for improvement since this model only considers part of the intrinsic capacitors associated with the overall topology.

A second small-signal model is presented in Fig.4.9 (b), this time considering the total capacitance associated with each node. Thus, only a small part of intrinsic capacitors are excluded

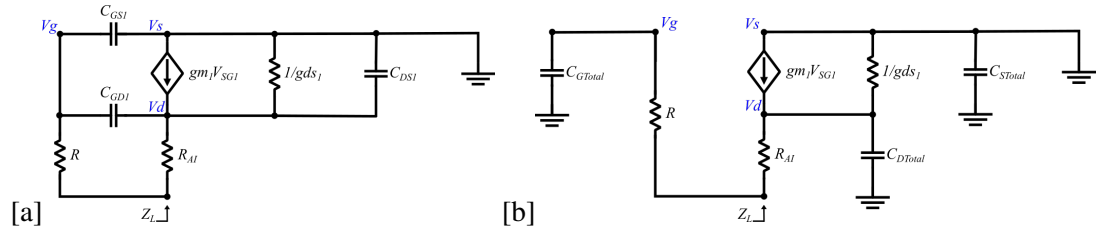


Figure 4.9: Small-signal model for simple AI: (a) Considering C_{gs}, C_{gd} and C_{ds} (b) Considering the total capacitance associated with each node

from this analysis. Another advantage is that it allows us to find out which node has the greatest impact on AI performance. This way, it is considered C_{gtot}, C_{stot} and C_{dtot}, the total capacitance associated with the gate, source and drain of transistor M_1, respectively. A small test is carried out, which consists of performing a simulation excluding one of these capacitors, at a time. As shown in Fig.4.10 (b), the C_{gtot} is the one that has the greatest impact on the behavior of the active inductor, which means that the total capacitance value at the gate of M_1 has to be estimated with special care.

Note that since transistor M_1 behaves as an inverting voltage amplifier, the Miller effect has to be taken into account. As a result, an extra capacior, known as Miller capacitance, C_M, is introduced at the gate of M_1. Analysing Fig.4.11 (b), the gain of M_1 transistor is given by Eq.4.6, hence the Miller capacitance C_M can be obtained by Eq.4.7. The deduction of C_M expression can be found in Appendix A, section A.3.

$$A_{simple} = -gm_1 \left(r_{o1} // R_{AI} \right) \tag{4.6}$$

$$C_M = C_{gtot} \left(1 + A_v \right) \tag{4.7}$$

Taking into account the extra capacitance in the gate of transistor M_1, introduced by the Miller effect, C_M, the simulation of the second small-signal model is shown in Fig.4.10 (a). As can be

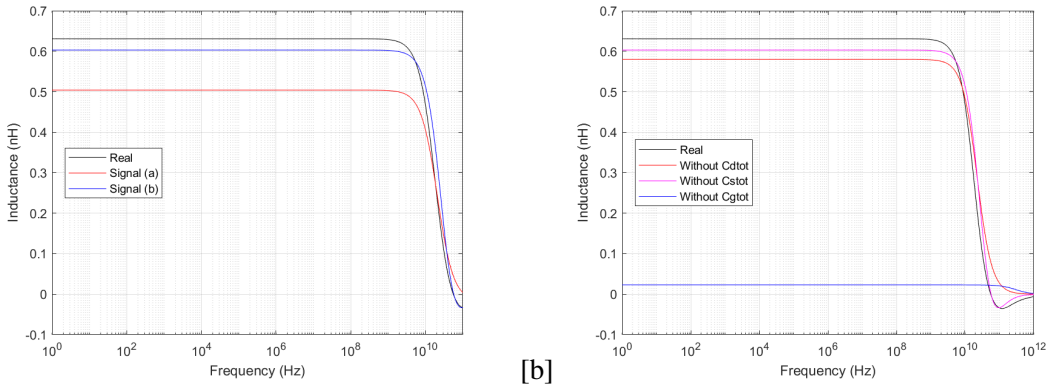


Figure 4.10: (a) Simulation of the small-signal models represented in Fig.4.9 (b) Simulation of the second small-signal model, excluding each node total capacitance, at a time

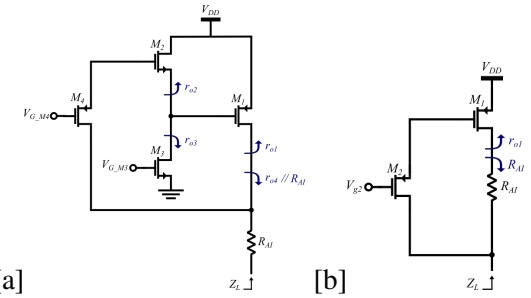


Figure 4.11: (a) Chapter 3 solution (b) Simple AI solution

seen, this second approach is a good approximation of the real configuration.

4.4.3.2 Chapter 3 solution

At the beginning of this section, it was mentioned that the reason for the observed difference between the signal and the real model could be due to an eventual exclusion of some intrinsic capacitance associated with each topology. This fact was proved in the previous simple AI small-signal analysis. However, for the topology presented in chapter 3, there is another reason that contributes to the observed difference. From Fig.4.11 (a), it is possible to conclude that the gain of the level shifter is given by Eq.4.8, which is less than one.

$$A_{Lee_{shifter}} = \frac{gm_2\,(r_{o2}\,//\,r_{o3})}{1+gm_2\,(r_{o2}\,//\,r_{o3})} \tag{4.8}$$

In order to reduce the analysis complexity, the sall signal analysis performed to Lee's active inductor in the previous chapter (3.2.1), was designed assuming that the level shifter has a unity AC gain. Although it works for a brief analysis, this model is not suitable for this context where in-depth analysis is being carried out in order to compare both topologies in detail. The assumption that the level shifter has a unity AC gain is not in accordance with the gain that is calculated by the Eq.4.8 and further confirmed by simulation, contributing this way to the difference observed between the signal model and the real configuration.

Following the idea that originated the second small signal approach to the simple AI, in order to design the small signal model of chapter 3 solution, it is considered the total capacitance associated with each node. Fig.4.12 (a) and (c), shows the resulting circuit and its simulation, respectively. As can be seen, the designed small-signal model is a really good approximation of the real model. This is due to the inclusion of almost all the existing intrinsic capacitors as well as the level shifter AC gain adjustment, which is now set to less than one.

To better understand the impact of assuming the unitary AC gain, it is performed a simulation assuming a unitary AC level shifter gain. Taking into account the gain expression given by Eq.4.8, to guarantee an approximately unitary gain, $gm_2(r_{o2}//r_{o3})$ must be much greater than 1. For this reason, M_3 transistor is replaced by an ideal current source and r_{o2} is considered a very high resistance, as shown in Fig.4.12 (b). Fig.4.12 (c) demonstrates the result of this simulation,

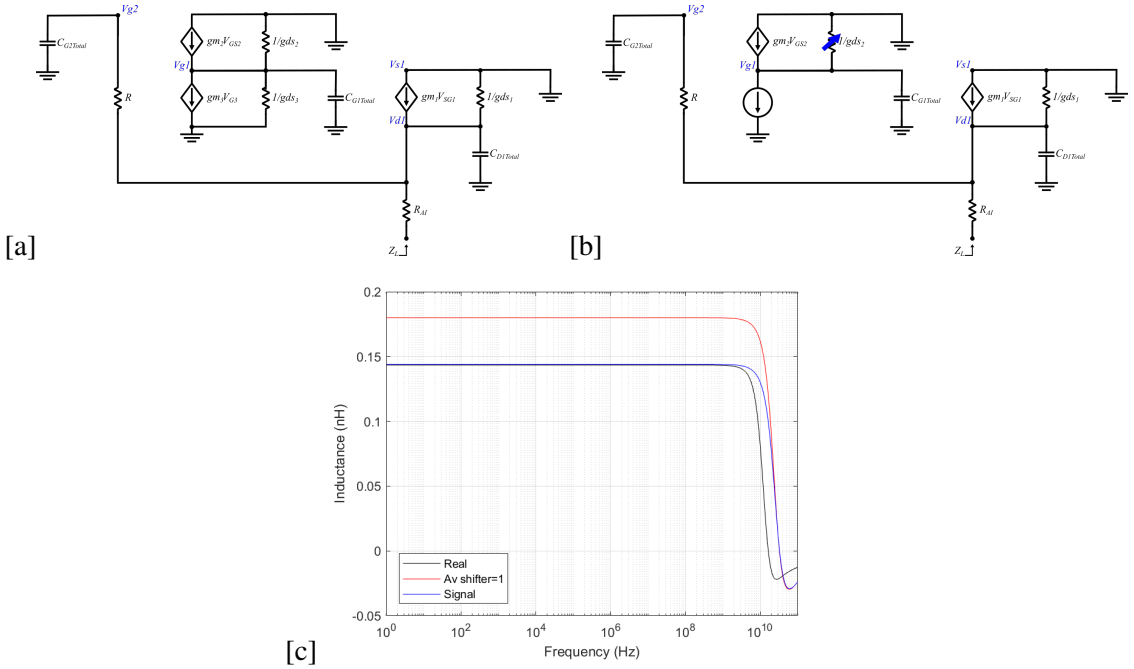


Figure 4.12: (a) Small-signal model to chapter 3 AI solution (b) Small-signal model assuming unitary level shifter AC gain (c) Simulations of the mentioned small-signal models

revealing, as expected, that a unitary AC level shifter gain improves the performance of the Lee's active inductor.

4.5 Transient Analysis

The AC analysis (section 4.3) carried out revealed the significant bandwidth extension resulting from the integration of the novel approach for the use of the simple AI. The reason for this improvement was then analyzed analytically in the previous Small Signal Analysis (section4.4). Considering the success of the configuration in the previous simulations, it is time to observe the behavior of the simple AI in the time domain. As the integration of the novel topology brings higher bandwidth, during the next transient analysis, this configuration is expected to cause an improvement in transition times.

4.5.1 First transient simulation

Fig.4.13 (a), (b) and (c), shows the result of the first transient simulation. The active inductor does not seem to meet the expectations. As it can be seen, the AI takes too long to turn *on* and does not even reach the maximum output voltage when turned *off*. In fact, when the input is zero, the circuit is behaving like a diode, which is the main reason why it is so difficult to turn *off*. Therefore, the voltage at the gate of transistor M_1 (Fig.4.13 (d)) follows the output voltage, what makes difficult to let transistor M_1 reach the triode region quickly.

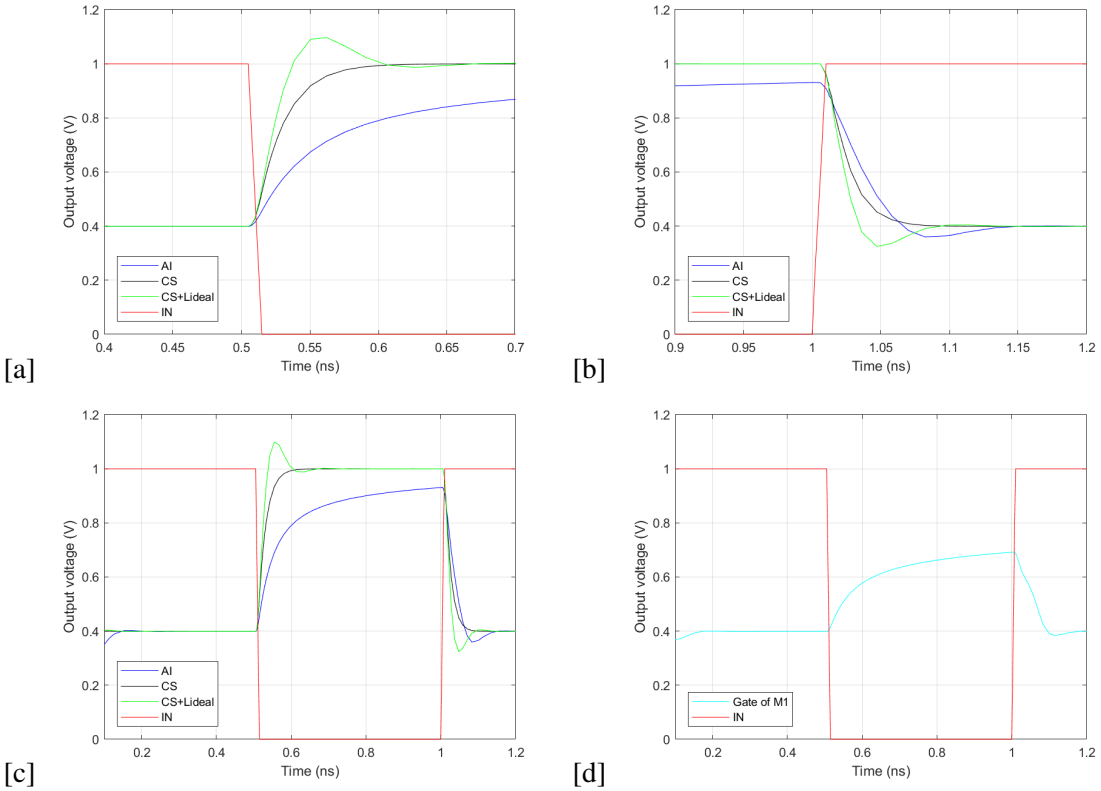


Figure 4.13: Simple AI transient analysis: (a) Rise (b) Fall (c) Geral (d) Gate of M_1

4.5.2 Improvement approaches

The first possible solution to avoid the diode behavior could be to disconnect M_2 when the AI is turning *off*. It is applied a clock signal equal to V_{in}, at the gate of M_2, as suggested in Fig.4.14 (a). As a result, the gate of M_1 could be at an uncertain voltage since it is now a floating node. However, as shown in Fig.4.15 (b), this voltage suffers just a small variation while the proposed solution seems to improve the rise time significantly, Fig.4.15 (a).

Despite this enhancement, the voltage at the gate of M_1 continues to drastically condition the time that transistor M_1 takes to operate in the linear region. This way, the second proposed solution, Fig.4.14 (b), consists in connecting the gate of M_1 to ground, when the AI is turning *off*, using an NMOS transistor regulated by a clock signal inverse to the input signal. Simultaneously, and as suggested by solution 1, the M_2 is disconnected. The result of this approach is represented in Fig.4.15 (c), where it is possible to observe a decent improvement in the rise time compared to the previous solution.

As Fig.4.15 (d) suggests, the voltage gate of M_1 is already ensuring the fastest operating region transition for transistor M_1. However, there is still room for improvement. The third solution, represented in Fig. 4.14 (c), aims to improve mainly the fall time. Instead of using a single NMOS transistor to perform the feedback, it is introduced a PMOS transistor constituting this way a CMOS feedback. This CMOS approach guarantees a more linear equivalent resistance to voltage

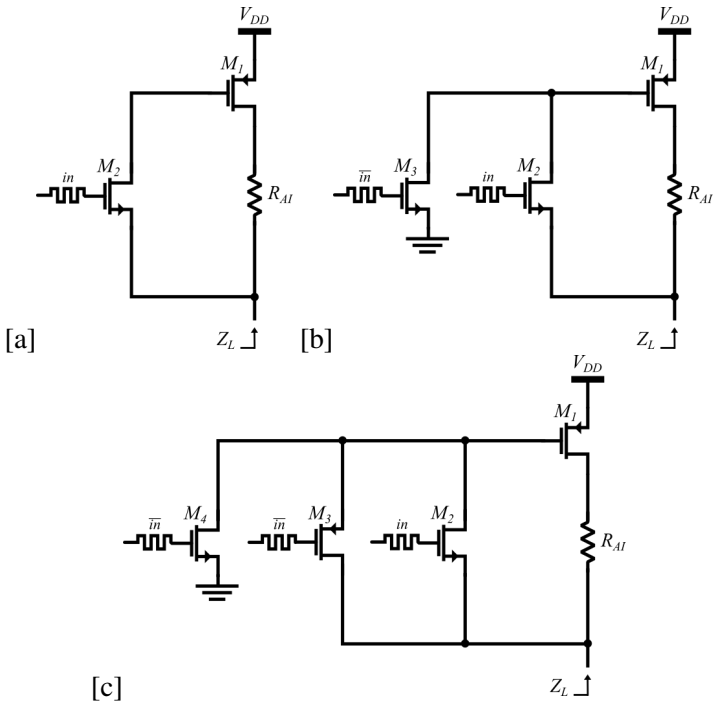


Figure 4.14: Simple AI improvement approaches: (a) First (b) Second (c) Third

variations. For this reason, it improves the transition times of the AI, as can be seen in 4.15 (e).

4.5.3 Output voltage range analysis

Despite all the efforts to improve the active inductor performance in the time domain, the obtained results are far from being considered decent. To better understand the reason for the lengthy transition times a small test is carried out. This test consists of performing an AC analysis to measure the bandwidth of the equivalent AI impedance considering different voltages at the output node, as represented by Fig.4.16 (a). This way, it is observed the behavior of the active inductor for several output voltages, which is roughly, what happens during the transition process. The AI topology of chapter 3 is also tested, and the results are shown in Fig.4.16 (b).

Since the normal operation point sets the voltage at the output node at 0.4V, as expected, both configurations decrease the bandwidth with the increase of the output voltage above 0.4V. However, the simple AI reveals to have a drastic reduction in performance with output voltages above 0.6V. This explains why the topology of the previous chapter did not show such bad transition times compared to this new configuration.

4.5.4 Final transient simulation

As analyzed, having an active inductor operating in a range of 0.6V seems to be an ambitious condition. The results of the previous test suggest that the voltage range cannot exceed 0.2V to ensure that the AI performs well. In fact, an output voltage range of 0.2V is sufficient for the context in which the active inductor will be applied, but also for many other I/O applications.

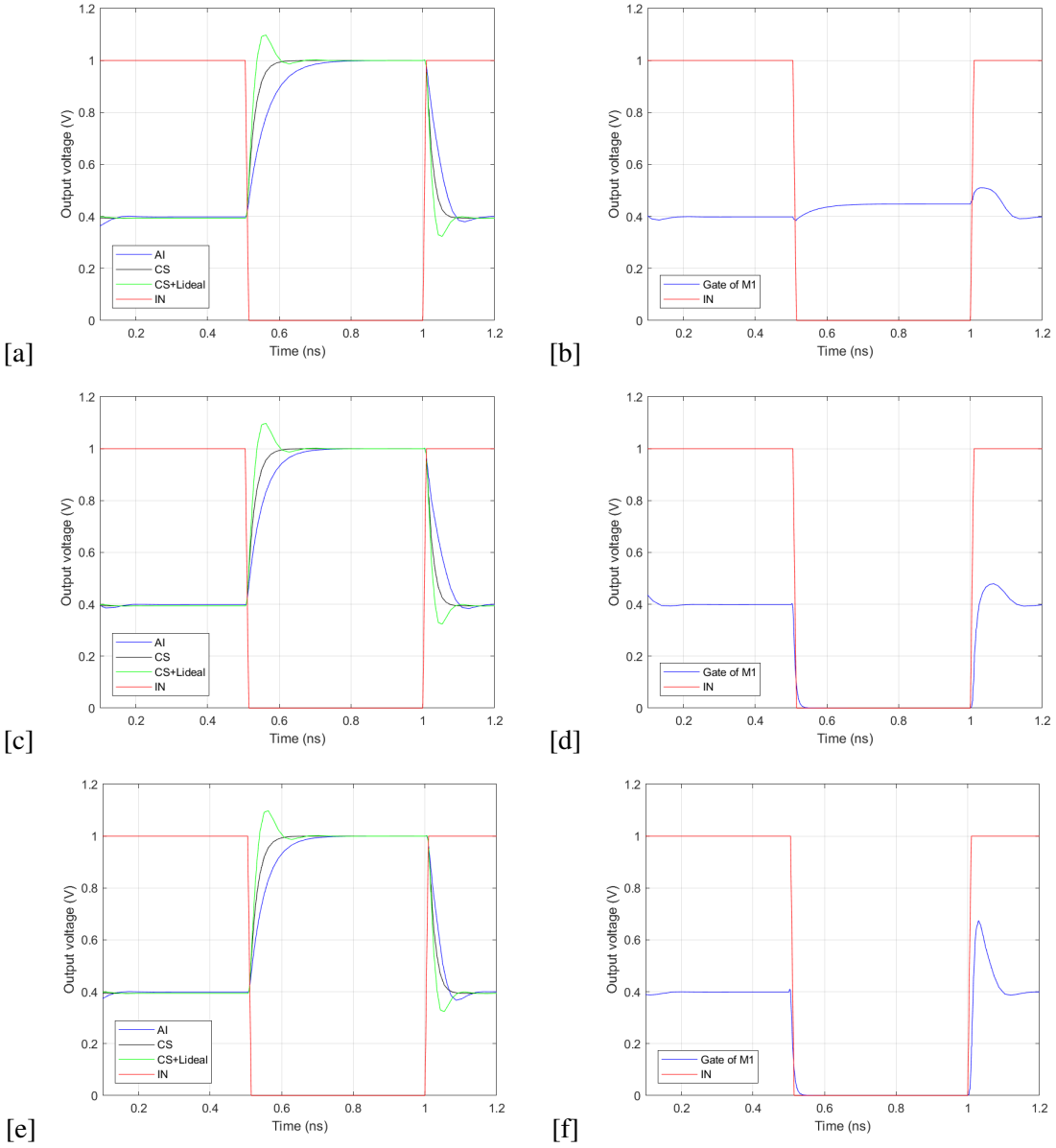


Figure 4.15: Simple AI transient analysis geral and gate of M_1, respectively: (a,b) First approach (c,d) Second approach (e,f) Third approach

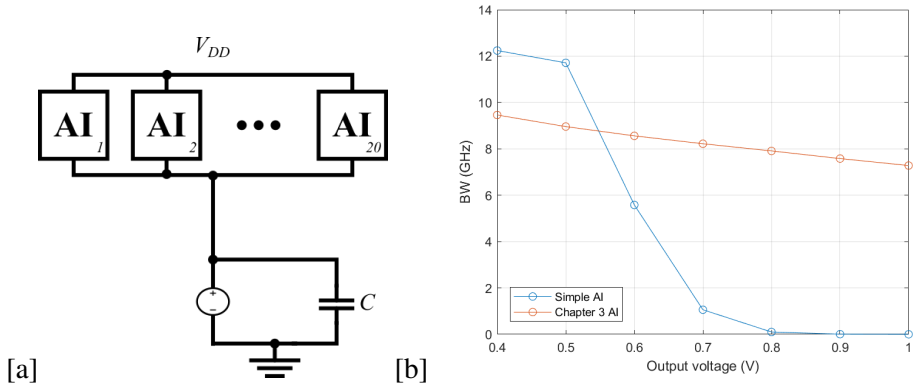


Figure 4.16: (a) AC analysis to measure the bandwidth of the equivalent AI impedance considering different output voltages (b) Result of the simulations carried out

The considered range is therefore set from 0.4V to 0.6V. This way, the driver never shuts down completely having always a minimum current. Hence, the active inductor is always enabled. For this reason, reviewing the previous Improvement approaches (4.5.2), it only makes sense to keep the use of CMOS feedback to guarantee a linear equivalent resistance, resulting in the novel approach to the simple AI topology illustrated in Fig.4.17.

Considering now the new output voltage range, transient analysis is carried out for both configurations. The results are shown in Fig.4.18 and summarized in Tables 4.3 and 4.4, for the topology designed in the previous chapter and for the novel simple AI configuration, respectively. Note that the common-source transistor has different sizes in each case, due to the difference in current used by each inductor approach. Thus, the driver transistor will operate with different transition times in each situation.

As it is possible to observe, with the adjustment of the range, both configurations improved the respective transition times. While the solution proposed in the previous chapter obtained an improvement of 5%, the simple AI achieved an impressive improvement of 15%.

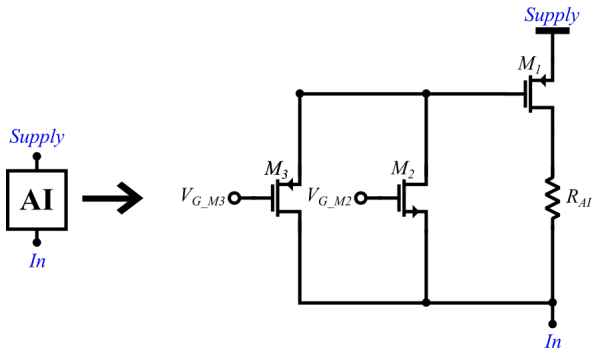


Figure 4.17: Simple AI final topology

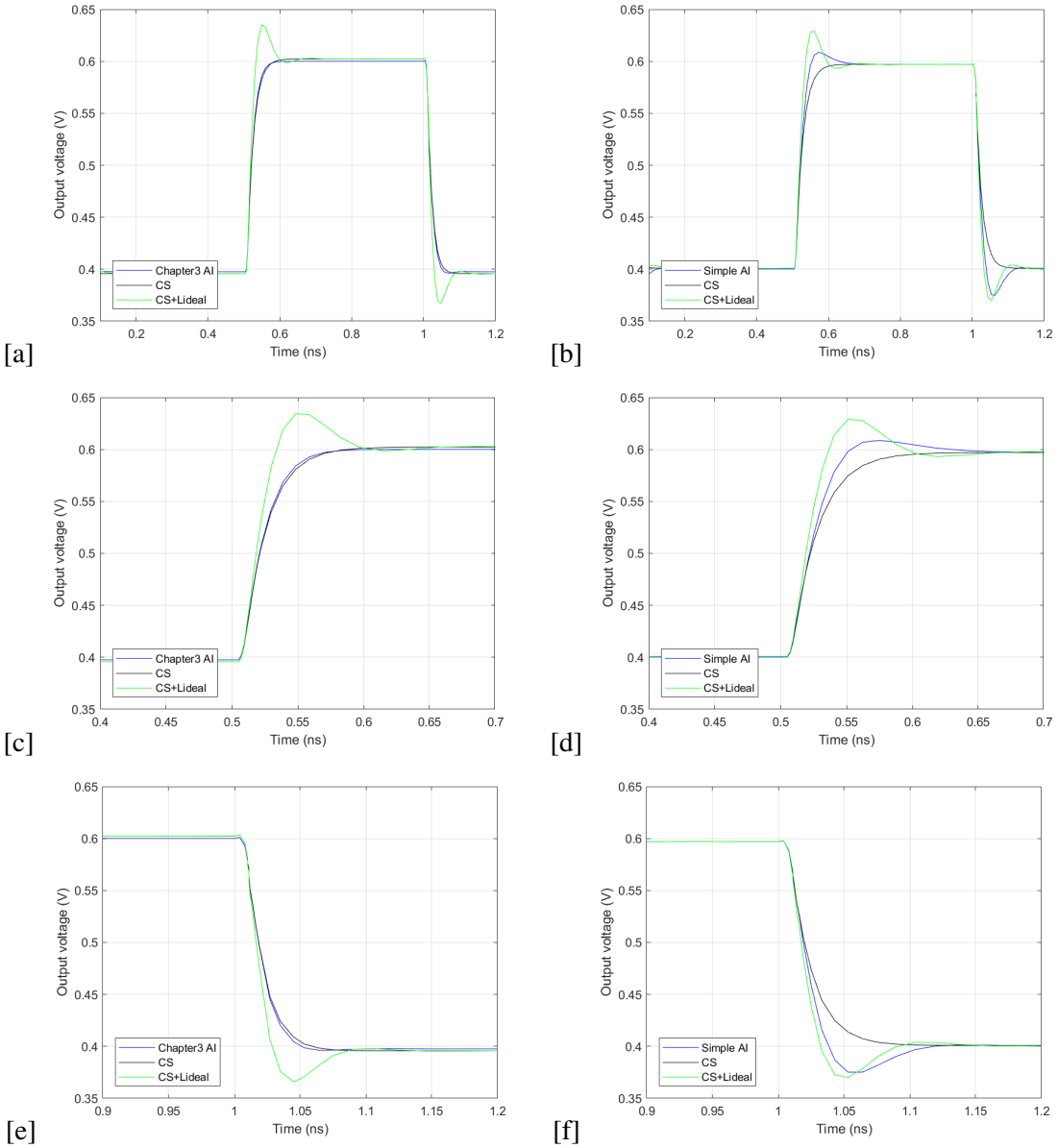


Figure 4.18: Transient analysis with 0.2V output voltage range: (a) Chapter 3 AI (b) Simple AI (c) Chapter 3 AI Rise (d) Simple AI Rise (e) Chapter 3 AI Fall (f) Simple AI Fall

Table 4.3: Transient analysis summary - Output voltage range 200mV - Proposed AI solution in chapter 3: Lee's active inductor in series with a resistor

Fig.	**Case**	**Rise (ps)**	**Rise Time improvement**	**Fall (ps)**	**Fall Time improvement**
(a)	CS	24.8	1.00 x	19.6	1.00 x
(b)	CS+Lideal	17.9	0.72 x	15.0	0.71 x
(c)	Chapter 3 AI	23.1	0.93 x	18.6	0.95 x

Table 4.4: Transient analysis summary - Output voltage range 200mV - Proposed simple AI solution

Fig.	**Case**	**Rise (ps)**	**Rise Time improvement**	**Fall (ps)**	**Fall Time improvement**
(a)	CS	27.4	1.00 x	23.8	1.00 x
(b)	CS+Lideal	19.1	0.7 x	17.6	0.74 x
(c)	Simple AI	23.7	0.86 x	20.3	0.85 x

4.6 Summary

The conclusions of the chapter 3 along with the proposed solution that consisted in the series of the Lee's active inductor with a resistor, served as a starting point to reach a final active inductor approach. Throughout this chapter, this final active inductor solution was developed and compared with the approach presented in the previous chapter.

The removal of the level shifter and the adjustment of the inserted resistor position led to a novel approach to the use of the simple active inductor topology that proved to perform well during AC analysis.

This good performance was then evaluated trough a small signal analysis that revealed the reason for the high resonant frequency demonstrated by the simple active inductor. In addition, this analysis showed the significant impact that the total capacitance at the gate of transistor M_1 has on the overall performance of the active inductor. The same happened to the solution presented in the previous chapter, which is also strongly dependent on the total capacitance at the gate of M_1 as well as at the gate of M_3. It was also studied the impact that the AC gain of the level shifter has on this last configuration, which is not unitary, as assumed at the beginning.

As the integration of the new topology approach demonstrated an impressive bandwidth extension during AC analysis, it was expected that it would bring an improvement in the transition times. However, in the first attempt, this did not happen. A few improvements were suggested, and then the idea came up to use CMOS feedback instead of a single NMOS. Despite all the efforts, the transition times only improved when the output voltage range was reduced.

When integrated, the new approach of the simple active inductor proved to improve significantly the transition times of the driver, thus fulfilling the objective to which the present thesis is proposed.

Chapter 5

Conclusions and Future Work

This chapter presents and overview of all of the work developed during the thesis, along with an analysis of the final state for each of the objectives that were set at the beginning. In addition, some future steps are defined to improve the work resulting from this dissertation.

5.1 Summary of the work developed

The main objective of this work was to design an active inductor topology to be integrated into an output driver with the ultimate goal of extending the bandwidth and consequently improve the driver's speed.

Several phases were carried out to accomplish the mentioned goal. All the work done, as well as all the conclusions drawn, are summarized below.

- The first phase of this work consisted in studying different bandwidth extension approaches. As a result, a method called shunt peaking revealed to ensure a significant bandwidth improvement using a reduced number of inductors, which can be implemented passively or actively. This caused the need to study the differences between these two types of implementations. The need for a large silicon area to fabricate passive inductors and features such as low-quality factor, low and fixed inductance, and low self-resonant frequency, dramatically increase the interest in adopting an active inductor solution aiming to minimize silicon area consumption and subsequently the manufacturing cost while improving the overall performance.

- Secondly, since that an active inductor proved to be the most viable approach, a study of previous shunt peaking active implementations using active inductors was performed. This study led to a few interesting implementations such as a conventional active inductor that presented a significant voltage drop, which could be compensated with a voltage-boosting circuitry at the cost of introducing extra design complexity; a folded active inductor that avoids both these problems by using just an NMOS transistor with a resistor connected to

the gate; Lee's active inductor that uses a level shifter to allow the regulation of the voltage at the gate of the main transitor depending on the scenario where it is applied.

- Then, these active inductor configurations were analyzed in more detail. For the topologies which showed a greater potential as possible starting point for the solution of the problem at hand, a pratical implementation was carried out resulting in a more complete analysis to each approach.

- The integration of the folded active inductor (NMOS version), demonstrated that a R // L // C implementation is not a good option to extend the bandwidth reinforcing the efficiency of adopting the shunt peaking method.

- On the other hand, the integration of the Lee's active inductor turned into a lenghty process that involved the analyses of the imaginary part and the real part, followed by the integration in the intended scenario. For the imaginary part analysis, it was observed the impact of each parameter in the active inductor performance concluding that there is a transistor that has a significant impact on the behaviour of the AI, and for this reason, must be carefully designed. After the reactance being in accordance with the objectives, in order to guarantee a current at the range of mA, an approach based on multiple branches was considered. Then, it was inserted a resistor to calibrate the real part and ensure that the equivalent real part was meeting the requirement of 50 Ω. It was then integrated into the proposed scenario. This process required a careful analysis regarding the sizing of the transistors in order to obtain an optimal performance while keeping the biasing at the required operating point. In the end, an AC analysis was carried out, indicating that Lee's AI in series with a resistor was extending the bandwidth in a relation of 1.12 compared to the uncompensated case. Finally, the time domain was observed and showed that this active inductor approach has not been successful in improving driver transition times.

- The conclusions obtained through the previous implementations served as as starting point to reach a final active inductor solution. The approach of Lee's active inductor in series with a resistor was observed again, and the idea of removing the level shifter came up. Since the target scenario where the AI is applied, has low output voltages, it can afford to have some voltage drop across the designed active inductor. Therefore, there was no need to use a level shifter for voltage regulation. This way those transistors that make up the level shifter were only contributing to extra static power consumption, while increasing intrinsic capacitors. Then, with the adjustment of the position of the inserted resistor, a new novel approach to the use of a simple active inductor topology was obtained.

- The new approach proved to perform well during AC analysis. This good performance was then evaluated through a small-signal analyses, which revealed the significant impact that the total capacitance at the gate of M_1 has on the overall performance of the active inductor. The same happened to the series resistor and Lee's active inductor, which also suffes from the total capacitance of the gate of M_3. In contrast to AC analysis, the analysis in the time

domain was not so successful. A few improvements were tried, and then the idea came up to use CMOS feedback instead of a single NMOS M_2 transistor. Despite all the efforts, the transition times only improved when the output voltage range was reduced to 200 mV.

- When integrated, considering the new output range, both configurations improved the respective transition times. While the series resistor and Lee active inductor obtained an improvement of 5%, the new approach of the simple active inductor achieved an impressive improvement of 15%.

5.2 Concluded Objectives

The main objective was completed. The work done resulted in a novel approach of the use of the simple active inductor, which extends the bandwidth and consequently improves the driver´s speed. An alternative approach was also designed, which consists of the Lee's active inductor in series with a resistor, which despite having a lower performance, slightly improves the transition times.

Both configurations guarantee impedance matching, since they have an equivalent real part accordingly to the impedance of the cable, that in most wired serial protocol is 50 Ω. Thus, the second objective proposed at the beginning, was also achieved.

5.3 Future work

There is still room for improvement on the proposed simple active inductor. As analysed during this work, both configurations show the best performance when the output voltage is at 0.4V, which is the normal operating point. As they move away from that the respective performance degrades. This can be improved in the case of the simple AI, by developing CMOS feedback. A CMOS active resistor approach can be studied and designed in order to keep the same performance for the entire output voltage range.

Another relevant aspect associated with the simple inductor is that, similar to the development of the active CMOS resistor, other options that can also contribute to reduce the total capacitance at the gate of M_1, since a large value has a significant impact on the AI performance.

Appendix A

Expressions Deduction

A.1 Equivalent impedances of the AI solution designed in chapter 3 and of the novel simple AI designed in chapter 4

Fig.A.1 (a) and (b) shows the small-signal models of the solution designed in chapter 3 and chapter 4, respectively. Vg and Vd represents the voltage at the gate and drain of transistor M_1, respectively.

Starting by case (a), it is deactivated all the independent sources followed by the application of a test voltage V_{in} with the current out of the positive terminal being I_{in}, resulting in the Thévenin equivalent impedance, Z_L, that is given by the ratio of the test voltage to the test current (Eq.A.1).

$$Z_L = \frac{V_{in}}{I_{in}} \tag{A.1}$$

Considering the Ohm's and short Kirchhoff's Current Laws, Eq.A.3 and Eq.A.2 represents the algebraic sum of all the currents at the gate and drain of M_1, respectively. I_{in} is given by Eq.A.4.

$$\frac{V_d - V_g}{R} - \frac{V_g}{\frac{1}{s\,Cgs}} = 0 \tag{A.2}$$

$$\frac{V_g - V_d}{R} + \frac{V_{in} - V_d}{R_{AI}} - gm\,V_g - \frac{V_d}{\frac{1}{gds}} - \frac{V_d}{\frac{1}{C_{ds}}} = 0 \tag{A.3}$$

$$I_{in} = \frac{V_{in} - V_d}{R_{AI}} \tag{A.4}$$

Deriving these three equations, it is obtained the input impedance, given in Eq.A.5.

$$Z_{in} = \frac{s^2\,(C_{gs}\,R\,R_{AI}\,C_{ds}) + s\,(C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI} + R_{AI}\,C_{ds}) + R_{AI}\,(gm + gds) + 1}{s^2\,(C_{gs}\,R\,C_{ds}) + s\,(\,C_{ds} + C_{gs}\,gds\,R + C_{gs}) + gm + gds} \tag{A.5}$$

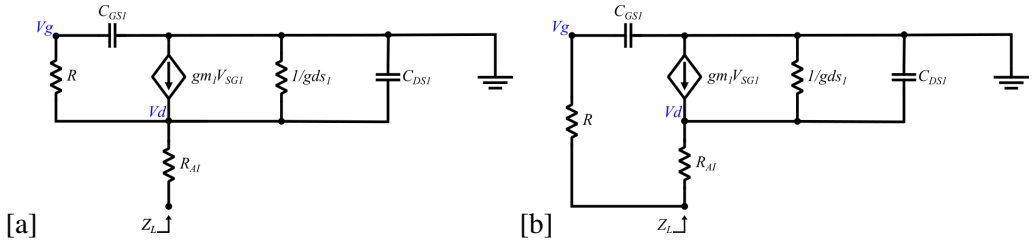


Figure A.1: Small signal model: (a) AI solution designed in the chapter 3 (b) Novel simple active inductor approach

The adopted procedure for case (b) is the same followed in case (a), where Eq.A.7 and Eq.A.6 represents the algebraic sum of all the currents at the gate and drain of M_1, respectively. I_{in} is given by Eq.A.8.

$$\frac{V_{in}-V_g}{R}-\frac{V_g}{\frac{1}{s\,Cgs}}=0 \tag{A.6}$$

$$\frac{V_{in}-V_d}{R_{AI}}-gm\,V_g-\frac{V_d}{\frac{1}{gds}}-\frac{V_d}{\frac{1}{C_{ds}}}=0 \tag{A.7}$$

$$I_{in}=\frac{V_{in}-V_d}{R_{AI}}+\frac{V_{in}-V_g}{R} \tag{A.8}$$

Deriving these three equations, it is obtained the input impedance, given in Eq.A.9.

$$Z_{in}=\frac{s^2\,(C_{gs}\,R\,R_{AI}\,C_{ds})+s\,(C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R+R_{AI}\,C_{ds})+R_{AI}\,gds+1}{s^2\,(C_{gs}\,R\,C_{ds}+C_{gs}\,R_{AI}\,C_{ds})+s\,(\,C_{ds}+C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs})+gm+gds} \tag{A.9}$$

A.2 *RLC* model of the solution designed in chapter 3 and chapter 4

Both configurations can be converted to the same *RLC* simplified model, that is represented in Fig.A.3. In order to reduce the complexity during the *RLC* model deduction, C_{ds} is neglected in both impedance expressions, resulting in Eq.A.10 and A.11 for case (a) and (b), respectively.

$$Z_{in}=\frac{s\,(C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R+C_{gs}\,R_{AI})+R_{AI}\,(gm+gds)+1}{s\,(\,C_{gs}\,gds\,R+C_{gs})+gm+gds} \tag{A.10}$$

$$Z_{in}=\frac{s\,(C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R)+R_{AI}\,gds+1}{s\,(\,C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs})+gm+gds} \tag{A.11}$$

Knowing that the admittance, Y_{in}, is defined as the reciprocal of impedance, the expression of Y_{in} for case (a), Y_{in_a}, can be derived from Eq.A.12, A.13 and A.14.

$$Y_{in_a}=\frac{1}{Z_{in}}=\frac{s\,(\,C_{gs}\,gds\,R+C_{gs})+gm+gds}{s\,(C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R+C_{gs}\,R_{AI})+R_{AI}\,(gm+gds)+1} \tag{A.12}$$

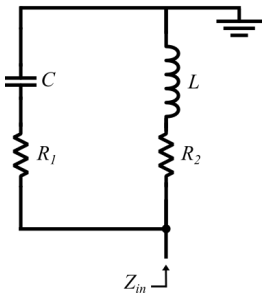


Figure A.2: *RLC* simplified model

$$Y_{in_a} = \frac{1}{\frac{s\,(C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI})}{s\,(C_{gs}\,gds\,R + C_{gs})} + \frac{R_{AI}\,(gm+gds)+1}{s\,(C_{gs}\,gds\,R + C_{gs})}} + \frac{1}{\frac{s\,(C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI})}{gm+gds} + \frac{R_{AI}\,(gm+gds)+1}{gm+gds}} \tag{A.13}$$

$$Y_{in_a} = \frac{1}{\frac{C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI}}{C_{gs}\,gds\,R + C_{gs}} + \frac{1}{s\,(\frac{C_{gs}\,gds\,R + C_{gs}}{R_{AI}\,(gm+gds)+1})}} + \frac{1}{s\,(\frac{C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R + C_{gs}\,R_{AI}}{gm+gds}) + \frac{R_{AI}\,(gm+gds)+1}{gm+gds}} \tag{A.14}$$

Eq.A.14 leads to the *RLC* model since that it can be considered as Eq.A.15.

$$Y_{in_a} = \frac{1}{R_1 + \frac{1}{s\,C}} + \frac{1}{s\,L + R_2} \tag{A.15}$$

where,

$$L = \frac{C_{gs}\,(\,R\,R_{AI}\,gds + R + R_{AI})}{gds + gm} \tag{A.16}$$

$$C = \frac{C_{gs}\,(\,gds\,R + 1)}{R_{AI}\,(gds + gm) + 1} \tag{A.17}$$

$$R_1 = \frac{R\,R_{AI}\,gds + R + R_{AI}}{gds\,R + 1} \tag{A.18}$$

$$R_2 = \frac{R_{AI}\,(gds + gm) + 1}{gds + gm} \tag{A.19}$$

On the other hand, the expression of Y_{in} for case (b), Y_{in_b}, can be derived from Eq.A.20, A.21 and A.22.

$$Y_{in_b} = \frac{1}{Z_{in}} = \frac{s\,(C_{gs}\,gds\,R + C_{gs}\,gds\,R_{AI} + C_{gs}) + gm + gds}{s\,(\,C_{gs}\,R\,R_{AI}\,gds + C_{gs}\,R) + R_{AI}\,gds + 1} \tag{A.20}$$

$$Y_{in_b} = \frac{1}{\frac{s\,(\,C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R)}{s\,(C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs})} + \frac{R_{AI}\,gds+1}{s\,(C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs})}} + \frac{1}{\frac{s\,(\,C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R)}{gm+gds} + \frac{R_{AI}\,gds+1}{gm+gds}} \tag{A.21}$$

$$Y_{in_b} = \frac{1}{\frac{C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R}{C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs}} + \frac{1}{s\,(\frac{C_{gs}\,gds\,R+C_{gs}\,gds\,R_{AI}+C_{gs}}{R_{AI}\,gds+1})}} + \frac{1}{s\,(\frac{C_{gs}\,R\,R_{AI}\,gds+C_{gs}\,R}{gm+gds}) + \frac{R_{AI}\,gds+1}{gm+gds}} \tag{A.22}$$

Eq.A.22 leads to the *RLC* model since that it can be considered as Eq.A.23.

$$Y_{in_b} = \frac{1}{R_1 + \frac{1}{s\,C}} + \frac{1}{s\,L+R_2} \tag{A.23}$$

where,

$$L = \frac{C_{gs}\,(\,R\,R_{AI}\,gds+R)}{gds+gm} \tag{A.24}$$

$$C = \frac{C_{gs}\,(\,gds\,R+gds\,R_{AI}+1)}{R_{AI}\,gds+1} \tag{A.25}$$

$$R_1 = \frac{R\,R_{AI}\,gds+R}{gds\,R+gds\,R_{AI}+1} \tag{A.26}$$

$$R_2 = \frac{R_{AI}\,gds+1}{gds+gm} \tag{A.27}$$

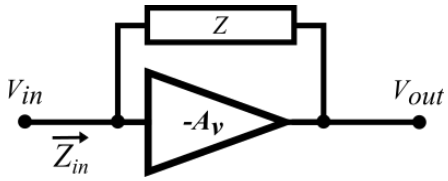


Figure A.3: An ideal voltage inverting amplifier with an impedance connecting output to input

A.3 Miller effect

Considering an ideal inverting voltage amplifier of gain A_v with an impedance Z connected between its input and output nodes, the output voltage is given by Eq.A.28.

$$V_{out} = -A_v V_{in} \tag{A.28}$$

Assuming that at the input, the amplifier draws no current, all of the input current flows through Z, and is given by Eq.A.29

$$I_{in} = \frac{V_{in} - V_{out}}{Z} = \frac{V_{in}(1 + A_v)}{Z} \tag{A.29}$$

Therefore, the input impedance of the circuit is obtained by Eq.A.30.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{Z}{(1 + A_v)} \tag{A.30}$$

Taking into account the context where the miller effect is being considered, the voltage amplifier represents a transistor with gain $-A_v$ while Z represents a capacitor with impedance $Z = 1/(sC)$. This way, the previous equation results in Eq.A.31.

$$Z_{in} = \frac{1}{sC_M} \quad where \quad C_M = C(1 + A_v) \tag{A.31}$$

Thus the Miller capacitance C_M is the capacitor C multiplied by the factor (1+A_v).

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