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Hybrid Model Predictive Control for Modified Modular Multi-level Switch-Mode Power Amplifier

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***Abstract*—This paper proposes a hybrid model predictive control (HMPC) for a modified modular multilevel switch-mode power amplifier (M3-SMPA).The M3-SMPA consists of two parts connected in series including modular multilevel converter (MMC) and full-bridge converter (FBC). Different from available MPC methods that only apply either finite control set MPC (FMPC) or modulated MPC (MMPC), the proposed HMPC method synthesizes the merits of both FMPC and MMPC on different time scales. Firstly, the optimal control option (CO) for MMC is calculated by FMPC with the multiple control objectives including output voltage control, circulating current control, and submodules (SMs) capacitor voltages balance control. Then based on the above optimal CO, the optimal duty cycle for FBC is calculated by MMPC with a single objective of output voltage control. In this case, the FMPC achieves the multi-objective control of MMC while the MMPC eliminates the tracking error of output voltage using FBC with a fixed switching frequency. Furthermore, a circulating current injection method is presented to balance the SMs capacitor voltages and an improved adjacent search (IAS) method is introduced to reduce the evaluated COs for MMC in each control period. The effect of DC-link voltage configuration for FBC on output steady-state performance is also analyzed. Finally, the effectiveness of the proposed HMPC method is verified by experimental results.**

***Index Terms*—hybrid model predictive control (HMPC), modified modular multilevel converter (M3C), switch-mode power amplifier, finite control set model predictive control (FMPC), modulated model predictive control (MMPC), improved adjacent search**

I. Introduction

With the development of the power electronic technology, the concern of power amplifier has increased in industrial and military application. Consisting of a power amplifier and an underwater electroacoustic transducer, the underwater electroacoustic transduction system (UETS) is widely studied and applied for ocean acoustic tomography [1], long-range underwater target positioning [2], and long-range underwater communication [3]. There have been several successes, such as ATOC (Acoustic Thermometry of Ocean Climate) [4] and SURTASS LFA (Surveillance Towed Array Sensor System) [5]. Fig. 1 shows a typical power supply system for subsea observatories and the UETS can be regarded as a subsea load. In order to reduce the power loss over a long-distance power transmission, HVDC system can be adopted in this application, and a typical level of 10 kV can be used with the consideration of cost and insulation breakdown in subsea cable [6]-[7]. The underwater electroacoustic transducer is utilized for converting electrical energy into sound energy, while the switch-mode power amplifier is utilized for converting a small signal into high-level electrical energy. In UETS, the underwater electroacoustic transducer is required to provide sound output with features of high sound source level (SSL) and high sound quality to meet the above application requirement [8]. In this case, the power amplifier should be able to provide electrical energy with features of high power, high fidelity (or high linearity), and high efficiency. Considering that the transducer adopts a closed cavity structure design for reliable underwater operation, the high power transducer is usually designed as a high voltage structure instead of high current structure to avoid overheating during operation [9].

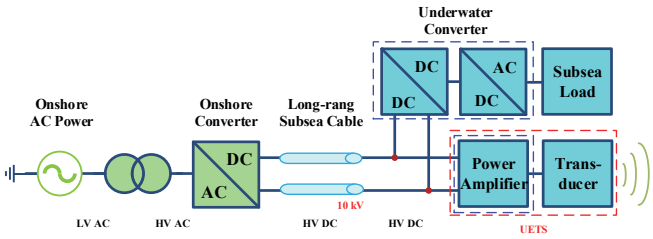

Fig. 1. Power supply system for subsea observatories.

With the characteristic of high fidelity, linear power amplifiers (LPA), such as class-A, class-B, and class-AB, are mainly employed in the past few years. However, the difficulty of LPA is mainly low efficiency, which would create pressure on size and system cost [10]. To improve efficiency, the high bandwidth dc/dc converter, namely envelope amplifiers, is introduced to replace the constant dc supply of LPA [11]-[14]. In this case, the power loss of LPA can be reduced because the dc supply can be adjusted according to the LPA output reference. Although the efficiency is improved, the delivered power is completely provided by the LPA, which makes it difficult to apply its design for high power applications. In order to improve efficiency in high power applications, switch-mode power amplifier (SMPA), in which the switching devices only

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work in the saturation and cutoff regions, has been developed, such as class D and class E. It mainly includes nine-level converter [15]-[16], diode-clamped converter [17], and cascaded H-bridge converter (CHB) [18]. When using these topologies, the bulky passive filters are generally required for eliminating the effect of the switching ripple on the output current. In order to achieve high efficiency and high fidelity simultaneously, the ideas of hybrid configuration are gradually attracting attention. The hybrid power amplifier (HPA) can be constructed by connecting SMPA and LPA in series [19] or parallel [20]. The high efficiency can be ensured by SMPA that delivers the main output power of HPA, while the high fidelity is provided by LPA that supplies a small amount of output power of HPA. To reduce the output filter requirement, a CHB based on phase-shift pulse-width modulation (PWM) is combined with LPA in [21]-[22]. In [23], a comparative study of different HPA topologies is conducted and a choosing guideline for different applications is indicated. Recently, modular multilevel converter (MMC) has gained extensive attention and rapid development due to the characteristic of modularity and scalability [24]-[39]. So In [40], an HPA composed of MMC and LPA is proposed to achieve high fidelity and high efficiency. However, the used LPA in HPA would still reduce the whole system efficiency, especially when the dc voltage of LPA is not small at all. Hence, to take advantages of MMC and HPA, a modified modular multilevel SMPA based on the MMC connected in series with FBC (shorted for M3-SMPA) is studied in this paper. The MMC is operating in main power supply mode to achieve high power while the FBC is operating in auxiliary power supply mode to achieve high fidelity. Since the LPA is replaced by the FBC, the whole system efficiency could be still ensured at high power and high voltage application.

In recent years, thanks to the advances in microprocessor technology, model predictive control (MPC) has become a promising optimal control method for power electronic converters [41]-[43]. MPC presents several advantages such as simple controller design, nonlinear constraints handle, and excellent dynamic performance. In available MPC methods, both finite control set MPC (FMPC) [44]-[46] and modulated MPC (MMPC) [47]-[49] have gained the most popularity in power converter and motor drives. The FMPC was firstly applied to MMC in [50]. The control objectives of MMC including output current tracking, circulating current suppression, and SMs capacitor voltage balance are mapped into the cost function simultaneously. To reduce the computation resulted from enumerating switching states, the control objectives are divided into two parts in [51]. The first part is used to calculate the optimal output level through FMPC while the second part transfers the optimal output level into optimal switching states via sorting algorithm. In [52], the adjacent search (AS) method is developed to further reduce the computation load for CHB. An AS method is also achieved for MMC in similar ways in [53]-[54]. One difficulty of FMPC is the steady-state tracking error because only one switching state is applied to the converter in each control period. In [55], the scholars indicate that the long horizon MPC (LHMPC) can further improve the steady-state performance compared with one horizon MPC. Though the extra computation introduced by LHMPC can be reduced by a sphere decoding algorithm [56], the implementation of LHMPC in FPGA seems to be not easy. The other difficulty of FMPC is the spread spectrum due to the variable switching frequency, which may bring challenges in parameter design of output filters. To eliminate the steady-state error and achieve the spectrum centralization, several MMPC methods have been presented. By analyzing the relationship between the output level and arm current slopes, two different output levels are synthesized to improve the tracking performance in each control period in [57]. In [58], the different output voltages that are considered to be combined are firstly obtained. Then the corresponding duty cycles could be calculated according to the reference output current and reference circulating current. In [59], the reference output voltages are deduced directly by substituting the reference current into a discretized mathematical model and then sent to the modulation block to generate the switching states, which is similar to deadbeat control [60]. Similar modulated ideas for MMC are also reflected in the literature [61]-[62]. In above modulated MPC methods, the steady-state error could be eliminated by synthesizing the different output voltage during on control period and the output spectrum could be more centralized due to the fixed switching frequency. However, when applying the above MMPC methods, the elimination of steady-state error can only be achieved with the limited state variables, i.e., MMPC could be difficult to handle with multiple control objectives compared with FMPC method. In addition, the duty cycle calculation process for multiple controlled variables is more complicated, especially for the second or higher order system.

To overcome these technological challenges with FMPC and MMPC, a hybrid model predictive control (HMPC) is proposed for M3-SMPA in this paper. The HMPC is composed of FMPC and MMPC, and according to the features of M3-SMPA, the optimization process is achieved with two-scale time. Considering the FMPC with the features of multiple objective capability, the optimal CO for MMC is calculated by FMPC to achieve the multi-objective of MMC including output voltage control, circulating current control, and SMs capacitor voltages balance control. Considering the MMPC with the features of steady-state tracking capability, the optimal duty cycle for FBC is calculated by MMPC to improve further the steady-state performance of output voltage with fixed switching frequency. By analyzing the relationship between the reference current and the predicted current, an improved adjacent search (IAS) method is proposed to significantly reduce the number of the evaluated COs for MMC in each control period. To eliminate the power difference among different arms of MMC, a circulating current injection method is also presented. Furthermore, the effect of DC-link voltage selection of FBC on output steady-state performance is analyzed. Finally, the experimental results validate the effectiveness of the proposed control methods.

This paper is organized as follows. In Section II, the system configurations and mathematical model of the M3-SMPA are introduced. Afterward, the operation principle of HMPC is analyzed in Section III. Experiments are carried out to

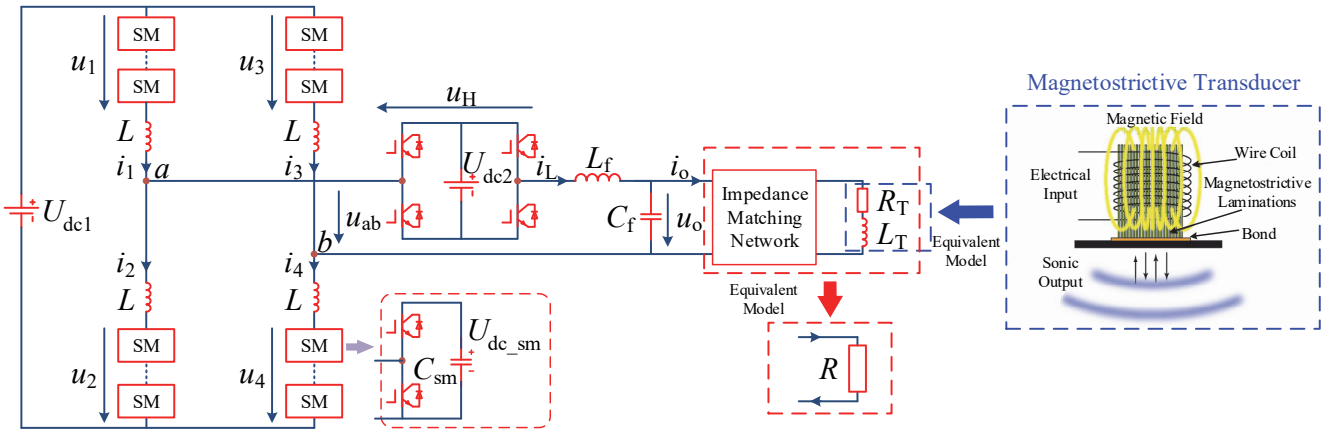

Fig. 2. The main topology of M3-SMPA.

demonstrate the effectiveness of the proposed control methods in Section IV. In Section V, the power loss comparison under different topologies and control methods is performed. Section VI draws the conclusion.

II. System Configuration and Modeling of M3-SMPA

The main topology of the M3-SMPA to be discussed is shown in Fig. 2. It contains three parts incorporating power supply circuit, passive filter branch, and transducer. The powersupply circuit consists of an MMC and an FBC, which are connected in series. The MMC is operating in main power supply mode at the relatively low switching frequency to ensure the high power output of M3-SMPA, while the FBC is operating in auxiliary power supply mode at the relatively high switching frequency to achieve high fidelity output of M3-SMPA. The MMC contains two phases and four arms. Each arm consists of N series SMs and arm inductor L, and each SM consists of the half-bridge converter (HBC) and capacitor C. Considering that the MMC is operating in main power mode with a relatively low switching frequency of SM, the normal high voltage IGBT module (such 1700 V or 3300 V or higher) could be utilized for SM. For example, when we set the typical value of rated SM capacitor voltage as 1000 V or 2000 V, and the MMC system could be designed with the number of SMs N=10 or N=5. The passive filter branch uses a shunt capacitor (C_f) with series inductor (L_f), together with the equivalent ac-side inductor converted from the arm inductor, to form a second-order low-pass LC filter. U_{dc1}, u_j and i_j (j=1, 2, 3, 4) denote DC-link voltage, the arm voltage and the arm current of the MMC, respectively. U_{dc2} and u_H denote the DC-link voltage and the output voltage of the FBC, respectively. i_L, i_o, and u_o denote the inductor current, the output current, and the output voltage, respectively. In general, power factor of the transducer could be ensured by an appropriate impedance matching circuit. For simplicity, the transducer and impedance matching circuit are modeled in a purely resistive load R in this paper.

Firstly, obeying the direction of voltages and currents defined in Fig. 2, the external dynamic characteristic equation of MMC could be deduced as [63]-[64]:

$$\left(L+L_f\right)\frac{di_L}{dt}=\frac{u_2-u_1}{2}-\frac{u_4-u_3}{2}+u_H-u_o \tag{1}$$

Since there are three output states s_H associated with the FBC, u_H could be further expressed as:

$$u_H=s_H U_{dc2} \tag{2}$$

with:

$$s_H=[-1,0,1]$$

According to Kirchhoff's current law, the relation for LC filter is given as:

$$i_L=C_f\frac{du_o}{dt}+i_o \tag{3}$$

Similarly, the internal dynamic characteristic equation of MMC could be deduced as [63]-[64]:

$$L\frac{di_{za}}{dt}=\frac{U_{dc1}}{2}-\frac{u_1+u_2}{2} \tag{4}$$

$$L\frac{di_{zb}}{dt}=\frac{U_{dc1}}{2}-\frac{u_3+u_4}{2} \tag{5}$$

where i_{za} and i_{zb} denote the circulating current of phase-a and phase-b, respectively. Assuming that the SMs capacitor voltages are well-balanced in each arm, the arm voltage u_j could be expressed as:

$$u_j=\sum_{i=1}^{N}s_{ij}u_{ij}\approx N_j u_{jave} \tag{6}$$

where u_{ij} and u_{jave} denote the i^{th} SM capacitor voltage and the average SMs capacitor voltage in j^{th} arm. N_j represents the inserted number of SMs in j^{th} arm and belongs to [0, 1, 2, …, N]. Synthesizing equations (1) to (6), the continuous state equation of M3-SMPA can be described by (7), with the state variable $\boldsymbol{x}=[i_L, u_o, i_{za}, i_{zb}]^T$, input vector $\boldsymbol{u_1}=[u_1, u_2, u_3, u_4, u_H]^T$, and disturbance vector $\boldsymbol{u_2}=[i_o, U_{dc1}]^T$. The order of state equation is only four regardless of the number of the series SMs, which benefits for expanding the number of SMs without increasing the complexity.

$$\dot{\boldsymbol{x}}=\boldsymbol{A}_1\boldsymbol{x}+\boldsymbol{B}_1\boldsymbol{u}_1+\boldsymbol{B}_2\boldsymbol{u}_2 \tag{7}$$

where the matrices $\boldsymbol{A}_1$, $\boldsymbol{B}_1$, and $\boldsymbol{B}_2$ are shown in Appendix I.

III. Hybrid Model Predictive Control for M3-SMPA

A. Mathematical Model Discretization

To apply the proposed HMPC method, the continuous state equation (7) can be discretized by forward Euler method, yields:

$$\boldsymbol{x}(k+1)=\boldsymbol{G}_1\boldsymbol{x}(k)+\boldsymbol{H}_1\boldsymbol{u}_1(k)+\boldsymbol{H}_2\boldsymbol{u}_2(k) \tag{8}$$

with:

$$\boldsymbol{G}_1=e^{\boldsymbol{A}_1 T},\ \boldsymbol{H}_1=\int_0^T e^{\boldsymbol{A}_1\tau}d\tau\boldsymbol{B}_1,\ \boldsymbol{H}_2=\int_0^T e^{\boldsymbol{A}_1\tau}d\tau\boldsymbol{B}_2$$

where k denotes the sampling instant and T denotes the sampling period. The matrices $\boldsymbol{G}_1$, $\boldsymbol{H}_1$, and $\boldsymbol{H}_2$ are time-invariant once the system parameters are determined. Due to the slow dynamic performance of the SMs capacitor voltages, the sum capacitor voltage could be viewed as constant in one sampling period, so $\boldsymbol{u}_1(k)$ could also be calculated via (2) and (6). The vectors $\boldsymbol{x}(k)$ and $\boldsymbol{u}_2(k)$ are measured directly. It is worth to mention that $i_o(k)$ in $\boldsymbol{u}_2(k)$ could be estimated by an appropriate observer [67]. However, it is not the subject of this paper.

B. Control Principle of HMPC

In order to achieve high power and high fidelity, an improved M3-SMPA topology is presented in the paper. The M3-SMPA consists of two parts connected in series including MMC and FBC. The MMC is operating in main power supply mode to achieve high power while the FBC is operating in auxiliary power supply mode to achieve high fidelity. For this characteristic of the improved M3-SMPA, an HMPC method that synthesizes the merits of both FMPC and MMPC on different time scales is proposed to control the M3-SMPA. The proposed HMPC method contains FMPC and MMPC. The FMPC takes responsibility for calculating the optimal CO (N_1^{opt}, N_2^{opt}, N_3^{opt}, N_4^{opt}) of MMC with the multiple control objectives of output voltage tracking, circulating current control, and SMs capacitor voltage balance. Then based on the above optimal CO, the MMPC takes responsibility for calculating the optimal duty cycle d^{opt} of FBC to further eliminate the steady-state error of output voltage with fixed switching frequency. Since the optimization process of HMPC is achieved with two-time scale, as shown in Fig. 3, the control period of FMPC and MMPC can be defined as T_m and T_h, respectively. Both T_m and T_h also satisfy the following relations:

$$T_h=T_m/q,\ q\in N^* \tag{9}$$

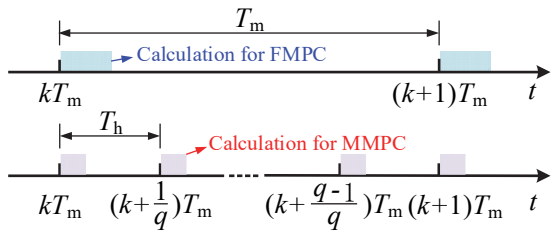

Fig. 3. Timing diagram of HMPC.

C. FMPC for MMC

1) Optimal control options

Firstly, to evaluate the effect of the COs (N_1, N_2, N_3, N_4) on the MMC performance, the controlled variables can be mapped into the following cost function J:

$$J=\left[\boldsymbol{y}^{ref}(k+1)-\boldsymbol{y}(k+1)\right]^T\boldsymbol{W}\left[\boldsymbol{y}^{ref}(k+1)-\boldsymbol{y}(k+1)\right] \tag{10}$$

with

$$\boldsymbol{y}(k+1)=\boldsymbol{C}\boldsymbol{x}(k+1) \tag{11}$$

where $\boldsymbol{C}$=diag([0 1 1 1]) and $\boldsymbol{W}$= diag([w_1 w_2 w_3]) denote the output matrix and weight coefficients matrix, respectively. The design for weighting coefficients could be referred in [66]. $\boldsymbol{y}^{ref}(k+1)$= [$u_o^{ref}(k+1)$ $i_{za}^{ref}(k+1)$ $i_{zb}^{ref}(k+1)$] and $\boldsymbol{y}(k+1)$=[$u_o(k+1)$ $i_{za}(k+1)$ $i_{zb}(k+1)$] denote the reference output value and predicted output value, respectively. In general, the reference output voltage u_o^{ref} is given. Ignoring the loss of MMC, the reference circulating current i_{za}^{ref} and i_{zb}^{ref} can be deduced according to the power balance principle:

$$\begin{cases} I_{za}^{ref}=\dfrac{\left(U_o^{ref}\right)^2}{4RU_{dc1}} \\ I_{zb}^{ref}=\dfrac{\left(U_o^{ref}\right)^2}{4RU_{dc1}} \end{cases} \tag{12}$$

where U_o^{ref} represents the magnitude of the reference output voltage. Then, for each possible COs combination, the predicted value $\boldsymbol{y}(k+1)$ could be calculated by (8) and (11). The corresponding cost function value J could be obtained by (10). The COs that minimizes the J will be selected as the optimal CO. It is worth to mention that when the optimal CO (N_1^{opt}, N_2^{opt}, N_3^{opt}, N_4^{opt}) of MMC is obtained via the proposed HMPC method, the specific switching states of SMs could be determined by a simple *sorting algorithm* [54], which is to achieve the balance among the SMs capacitor voltage inside the arm. There have been several methods for switching states selection in MMC [33], which is mainly to pursue the tradeoff between SM switching frequency and SM capacitor voltage ripple. Then the optimal switching states will be applied to the MMC in the next control period. Noting that the output state s_H for FBC is set to be zero during this optimization process of FMPC and the implementation above will be repeated in the next sampling instant of MMC.

2) SMs capacitor voltage balance control

Although the balance of SMs capacitor voltages in the same arm could be realized by sorting algorithm, the loss of the MMC system and the difference of power deviation among different arms are always inevitable, which will result in the imbalance of SMs capacitor voltages among the different arms. Here, the balance of the SMs capacitor voltages among different arms could be achieved by injecting the circulating current. As the circuit of the MMC is highly symmetrical, the arm voltage can be expressed by DC-link voltage U_{dc1} and ac side voltage u_{ab} as follows:

$$\begin{cases} u_1=u_4=\dfrac{U_{dc1}}{2}-\dfrac{u_{ab}}{2} \\ u_2=u_3=\dfrac{U_{dc1}}{2}+\dfrac{u_{ab}}{2} \end{cases} \tag{13}$$

For the convenience of subsequent description, we define

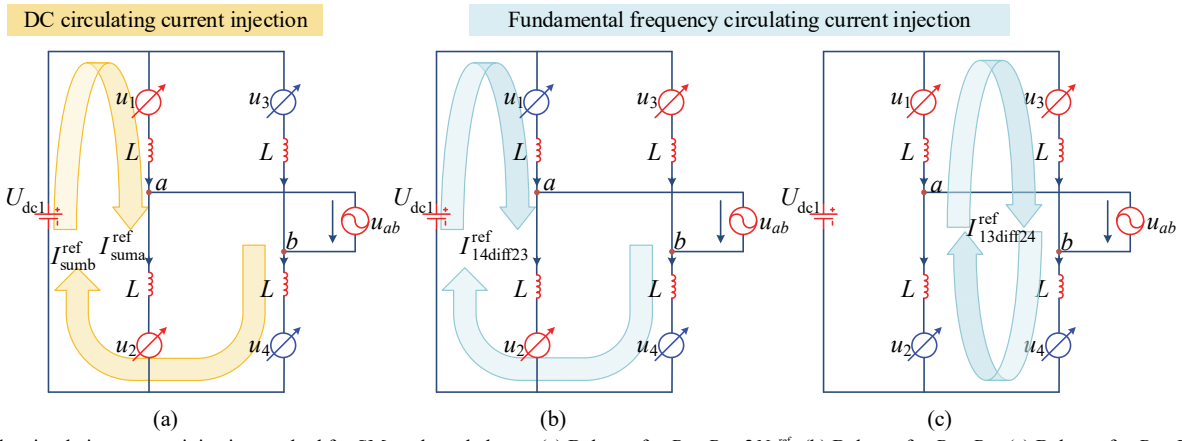

Fig. 4. The circulating current injection method for SMs voltage balance. (a) Balance for P_{12}=P_{34}=$2Nu_c^{ref}$. (b) Balance for P_{14}=P_{23}. (c) Balance for P_{13}=P_{24}.

P_{mn} to denote the power summation of the m^{th} arm and the n^{th} arm (m, n=1, 2, 3, 4, m≠n), P_{mn} could be expressed as:

$$P_{mn}=\sum_{i=1}^{N}u_{mi}^{2}+\sum_{i=1}^{N}u_{ni}^{2} \tag{14}$$

According to (13), the dc components of the four arms voltages are identical, the imbalance between P_{12} (or P_{34}) and reference power can be eliminated by injecting the dc circulating currents, as shown in Fig. 4(a). The reference phase power deviations could be calculated via PI controller as follows:

$$\begin{cases} P_{\text{suma}}^{\text{ref}}=k_{\text{p1}}\left[2N\left(u_{\text{c}}^{\text{ref}}\right)^{2}-P_{12}\right]+k_{i1}\int\left[2N\left(u_{\text{c}}^{\text{ref}}\right)^{2}-P_{12}\right] \\ P_{\text{sumb}}^{\text{ref}}=k_{\text{p1}}\left[2N\left(u_{\text{c}}^{\text{ref}}\right)^{2}-P_{34}\right]+k_{i1}\int\left[2N\left(u_{\text{c}}^{\text{ref}}\right)^{2}-P_{34}\right] \end{cases} \tag{15}$$

So the reference dc circulating currents for phase power balance are deduced as:

$$\begin{cases} I_{\text{suma}}^{\text{ref}}=P_{\text{suma}}^{\text{ref}}/U_{\text{dc1}} \\ I_{\text{sumb}}^{\text{ref}}=P_{\text{sumb}}^{\text{ref}}/U_{\text{dc1}} \end{cases} \tag{16}$$

According to (13), the fundamental frequency components of the 1st and 4th arms show the same magnitude as those of the 2nd and 3rd arms but in opposite phase, so the imbalance between P_{14} and P_{23} can be eliminated by injecting the fundamental frequency circulating currents in the same phase as shown in Fig. 4(b), while the imbalance between P_{13} and P_{24} can be eliminated by injecting the fundamental frequency circulating currents in the reversed phase as shown in Fig. 4(c). The reference power deviations are calculated as:

$$\begin{cases} P_{\text{14diff23}}^{\text{ref}}=k_{\text{p2}}\left(P_{23}-P_{14}\right)+k_{i2}\int\left(P_{23}-P_{14}\right) \\ P_{\text{13diff24}}^{\text{ref}}=k_{\text{p3}}\left(P_{24}-P_{13}\right)+k_{i3}\int\left(P_{24}-P_{13}\right) \end{cases} \tag{17}$$

So the reference magnitudes of the fundamental frequency could be deduced as:

$$\begin{cases} I_{\text{14diff23}}^{\text{ref}}=P_{\text{14diff23}}^{\text{ref}}/U_{\text{ab}} \\ I_{\text{13diff24}}^{\text{ref}}=P_{\text{13diff24}}^{\text{ref}}/U_{\text{ab}} \end{cases} \tag{18}$$

where U_{ab} denotes the magnitude of u_{ab}. According to (12), (16), and (18), the synthesized reference circulating currents are expressed as follows:

$$\begin{cases} i_{\text{za}}^{\text{ref}}=I_{\text{za}}^{\text{ref}}+I_{\text{suma}}^{\text{ref}}-I_{\text{13diff24}}^{\text{ref}}\sin\left(\omega t\right)-I_{\text{14diff23}}^{\text{ref}}\sin\left(\omega t\right) \\ i_{\text{zb}}^{\text{ref}}=I_{\text{zb}}^{\text{ref}}+I_{\text{sumb}}^{\text{ref}}+I_{\text{13diff24}}^{\text{ref}}\sin\left(\omega t\right)-I_{\text{14diff23}}^{\text{ref}}\sin\left(\omega t\right) \end{cases} \tag{19}$$

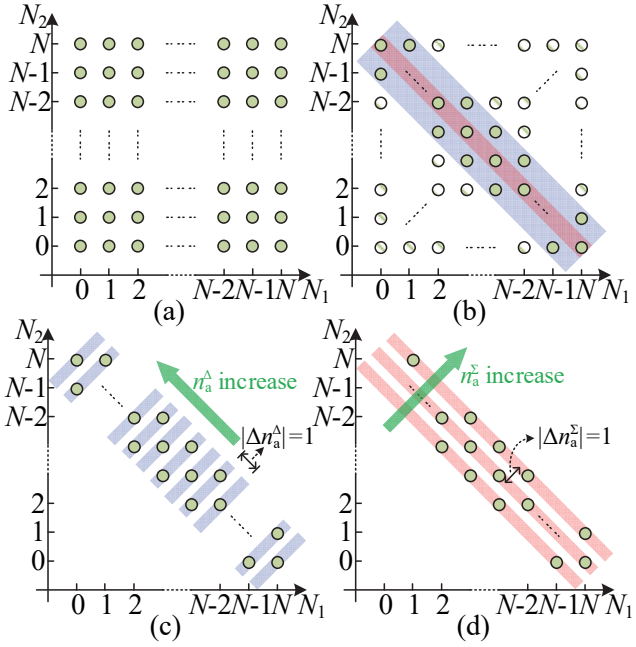

Fig. 5. Diagram of the search space.

where sin(ωt) denotes the phase of u_{ab}. Ignoring the phase shift effect of LC filter, the sin(ωt) can be approximately equal to the phase of reference output voltage $u_{\text{o}}^{\text{ref}}$.

3) Reduced computation complexity

Here, an improved adjacent search method (IAS) is proposed to reduce the number of evaluated COs in each control period. Compared with conventional adjacent search methods [53]-[54], the proposed IAS method can not only ensure the maximum output level of 4N+1, but also keep the number of the evaluated COs at 5 at most in each control period. To explain the proposed IAS method, a preliminary knowledge is given as follows:

Taking phase-a as an example, the maximum number of the evaluated COs is (N+1)^2 without considering the constraints for the total inserted number per phase, as shown in Fig. 5(a). For MMC system, the total inserted number is usually constrained for the harmonic circulating current suppression or to support the DC-link voltage. When the evaluated COs of each phase satisfy the condition that N_1+N_2=N, which refer to the circles located in the red area in Fig. 5(b) and the number of the

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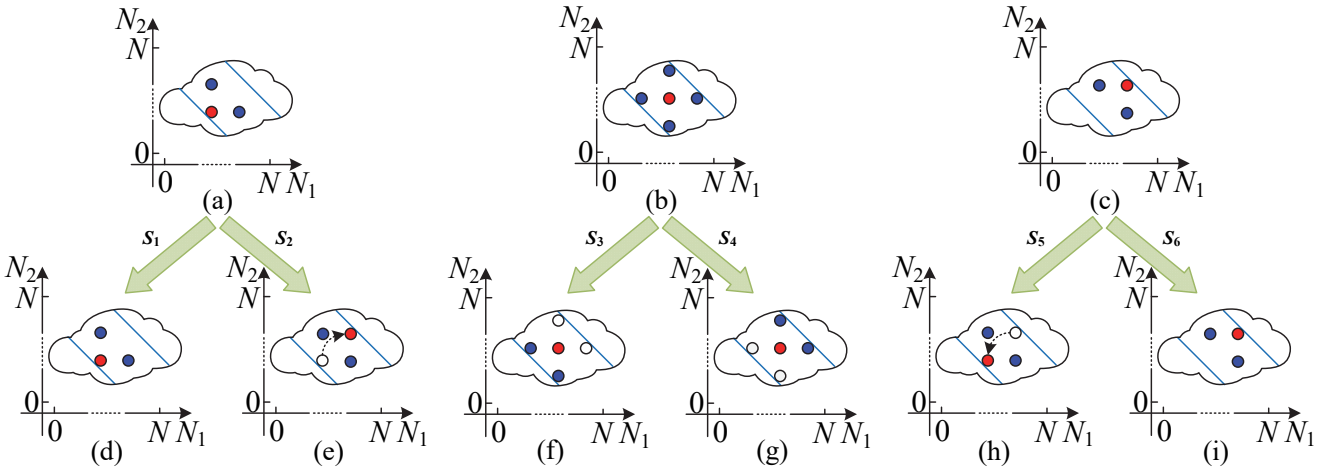

Fig. 6. Search space design for harmonic circulating current control. (a)-(c): Before correction. (d)-(i): After correction.

evaluated COs is N+1, there would be an apparent harmonic component in circulating current because of the inevitable fluctuations in actual SMs capacitor voltages. In general, the harmonic circulating current could be suppressed with the condition that N-$\varepsilon \le N_1+N_2 \le N+\varepsilon$, where ε denotes the limitation for N_1+N_2. The greater the number of SMs, the value of ε should be increased in order to ensure the suppression performance on harmonic circulating current. For the convenience of analysis, we assume that the proposed IAS is applied to MMC with a small number of SMs ($N \le 10$). In this case, the suppression performance could be ensured with ε=1 [54], [67]-[68], and the corresponding evaluated COs refer to the circles located in the blue area in Fig. 5(b) and the number of the evaluated COs is 3N+1. The following analysis is also based on this given search space. Firstly, we define the differential level n_a^{Δ} and common level n_a^{Σ} for the evaluated COs as:

$$\begin{cases} n_a^{\Delta} = N_2 - N_1 \\ n_a^{\Sigma} = N_2 + N_1 \end{cases} \tag{20}$$

As shown in Fig. 5(c), the circles located in the same blue area present the same value for n_a^{Δ}, and according to (1), the predicted inductor current corresponding to those circles could be approximately same. It can be noted that the number of possible values for n_a^{Δ} is 2N+1. n_a^{Δ} shows an increasing tendency in the direction of the green arrow and the increment value is equal to one. Similarly, the circles located in the same red area present the same n_a^{Σ} as shown in Fig. 5(d), and according to (4) and (5), the predicted circulating current corresponding to those circles could be approximately the same. It can be noted that the number of possible values for n_a^{Σ} is three. n_a^{Σ} shows an increasing tendency in the direction of the green arrow and the increment value is also equal to one. Though the search space shown in Fig. 5(c) and Fig. 5(d) is much narrower than that in Fig. 5(a), the number of the evaluated COs is still large, especially when the number of SMs is also large. So, an improved adjacent search (IAS) method is proposed to reduce the number of evaluated COs in each control period and the detailed implementations are as follows:

TABLE I
SEARCH SPACE DESIGN FOR HARMONIC CIRCULATING CURRENT CONTROL

Case	$N_1^{opt}+N_2^{opt}$	D_{za}	The evaluated COs (N_1, N_2) for phase-a
S_1	N-1	≥0	(N_1^{opt}, N_2^{opt}+1), (N_1^{opt}, N_2^{opt}), (N_1^{opt}+1, N_2^{opt})
S_2	N-1	<0	(N_1^{opt}, N_2^{opt}+1), (N_1^{opt}+1, N_2^{opt}+1), (N_1^{opt}+1, N_2^{opt})
S_3	N	≥0	(N_1^{opt}-1, N_2^{opt}), (N_1^{opt}, N_2^{opt}), (N_1^{opt}, N_2^{opt}-1)
S_4	N	<0	(N_1^{opt}, N_2^{opt}+1), (N_1^{opt}, N_2^{opt}), (N_1^{opt}+1, N_2^{opt})
S_5	N+1	≥0	(N_1^{opt}-1, N_2^{opt}), (N_1^{opt}-1, N_2^{opt}-1), (N_1^{opt}, N_2^{opt}-1)
S_6	N+1	<0	(N_1^{opt}-1, N_2^{opt}), (N_1^{opt}, N_2^{opt}), (N_1^{opt}, N_2^{opt}-1)

a) Search space design for harmonic circulating current control

Firstly, we define the adjacent search principle to satisfy:

$$\left|N_1 - N_1^{opt}(k-1)\right| + \left|N_2 - N_2^{opt}(k-1)\right| \le 1 \tag{21}$$

where $N_1^{opt}(k\text{-}1)$ and $N_2^{opt}(k\text{-}1)$ denote the previous optimal CO while N_1 and N_2 denote the evaluated COs in the current instant. Based on the given search space shown in Fig. 5(d), there exist three cases for the summation of $N_1^{opt}(k\text{-}1)$ and $N_2^{opt}(k\text{-}1)$ as N-1, N, and N+1, respectively. They are depicted by the red circles in Fig. 6(a), Fig. 6(b), and Fig. 6(c). Considering the search principle expressed in (21), both red and blue circles together make up the evaluated COs. According to (4) and (6), the discrete equation regarding circulating current could be simplified as follows:

$$i_{za}(k+1) = i_{za}(k) + \frac{T_m u_c^{ref}}{2L}\left(N - n_a^{\Sigma}\right) \tag{22}$$

Then, the increment of circulating current D_{za} is introduced:

$$D_{za} = i_{za}^{ref}(k+1) - i_{za}(k+1) \tag{23}$$

According to (22) and (23), if $D_{za} \ge 0$, n_a^{Σ} should be no more than N to increase the circulating current; If $D_{za}<0$, n_a^{Σ} should be no less than N to decrease the circulating current. Only then can the circulating current track its reference value effectively. So, the evaluated COs depicted in Fig. 6(a), Fig. 6(b), and Fig. 6(c) could be further corrected, as shown in Fig. 6(d) to Fig. 6(i). For example, assuming that the summation of $N_1^{opt}(k\text{-}1)$ and $N_2^{opt}(k\text{-}1)$ is equal to N-1 shown in Fig. 6(a), if $D_{za} \ge 0$, the evaluated COs

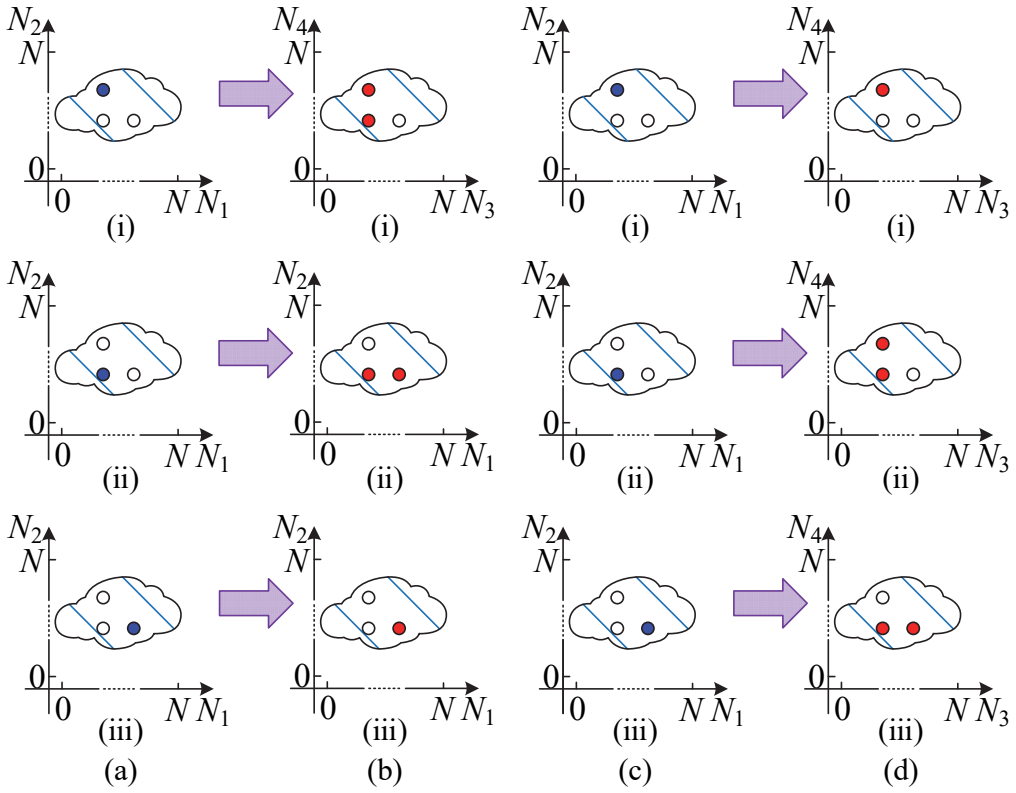

Fig. 7. Search space design for output voltage tracking. (a)-(b): $D_L \geq 0$. (c)-(d): $D_L < 0$.

could be corrected shown in Fig. 6(d) and the expressions of corrected COs are listed in the second row of Table I, while if $D_{za}<0$, the corrected COs are shown in Fig. 6(e) and the expressions of corrected COs are listed in the third row of Table I. Phase-b presents a similar result and not to be covered again. According to the analysis for Fig. 5(c), the corrected search space only affects the predicted circulating current control and the effect on predicted inductor current can be neglected. (Noting that $N^{opt}(k\text{-}1)$ is abbreviated as N^{opt} in Table I).

b) Search space design for output voltage tracking

Firstly, we introduce the two-phase differential level n^{Δ} and the previous optimal differential level $n^{\Delta opt}(k\text{-}1)$ as follows:

$$\begin{cases} n^{\Delta} = n_a^{\Delta} - n_b^{\Delta} = N_2 - N_1 - N_4 + N_3 \\ n^{\Delta opt}(k-1) = N_2^{opt}(k-1) - N_1^{opt}(k-1) \\ \qquad\qquad - N_4^{opt}(k-1) + N_3^{opt}(k-1) \end{cases} \tag{24}$$

Then, the reference inductor current can be obtained by substituting the reference output voltage into following backward difference expression:

$$i_L^{ref}(k+1) = \frac{C_f}{T_m}\left(u_o^{ref}(k+1) - u_o(k)\right) + i_o(k+1) \tag{25}$$

A simple assumption is made that the output current i_o can be approximated as a constant in a short control period yields:

$$i_o(k+1) = i_o(k) \tag{26}$$

Therefore, we could obtain the reference inductor current $i_L^{ref}(k+1)$ according to (25) and (26). According to (1) and (6), the discrete equation regarding inductor current could be simplified as follows:

TABLE II
SEARCH SPACE DESIGN FOR OUTPUT VOLTAGE TRACKING

D_L	The evaluated COs (N_1, N_2, N_3, N_4) for two-phase
≥0	(N_1(1), N_2(1), N_3(1), N_4(1)), (N_1(1), N_2(1), N_3(2), N_4(2)), (N_1(2), N_2(2), N_3(2), N_4(2)), (N_1(2), N_2(2), N_3(3), N_4(3)), (N_1(3), N_2(3), N_3(3), N_4(3))
<0	(N_1(1), N_2(1), N_3(1), N_4(1)), (N_1(2), N_2(2), N_3(1), N_4(1)),(N_1(2), N_2(2), N_3(2), N_4(2)), (N_1(3), N_2(3), N_3(2), N_4(2)), (N_1(3), N_2(3), N_3(3), N_4(3))

$$i_L(k+1) = i_L(k) + \frac{T_m u_c^{ref}}{2(L+L_f)} n^{\Delta} + \frac{u_o(k) T_m}{(L+L_f)} \tag{27}$$

Similar to the definition for the increment of circulating current, the increment of inductor current is introduced:

$$D_L = i_L^{ref}(k+1) - i_L^{opt}(k+1) \tag{28}$$

where $i_L^{opt}(k+1)$ denotes the predicted inductor current based on $n^{\Delta opt}(k\text{-}1)$. According to (27) and (28), if $D_L \geq 0$, n^{Δ} should be no less than $n^{\Delta opt}(k\text{-}1)$ to increase the inductor current; If $D_L<0$, n^{Δ} should be no more than $n^{\Delta opt}(k\text{-}1)$ to decrease the inductor current. It is worth to mention that the absolute value of the difference between n^{Δ} and $n^{\Delta opt}(k\text{-}1)$ is also limited to no more than one, which benefits for a lower dv/dt. Taking the condition of $D_L \geq 0$ as an example, when the evaluated COs of phase-a are located in the blue circle shown in Fig. 7(a)(i), Fig. 7(a)(ii), and Fig. 7(a)(iii), the evaluated COs of phase-b are limited to be located in the red circles shown in Fig. 7(b)(i), Fig. 7(b)(ii), and

TABLE III
COMPARISON OF THE NUMBER OF EVALUATED COS WITH DIFFERENT ADJACENT SEARCH METHODS

Performance	Fast MPC [53]	Preselection MPC [54]	Proposed IAS method
Maximum output level capability	$2N$+1	$4N$+1	$4N$+1
Number of the evaluated COs	7	17	5

Fig. 7(b)(iii) correspondingly. The expression for (N_1, N_2, N_3, N_4) is listed in the second row of Table II and the values of $N_1(l)$, $N_2(l)$, $N_3(l)$, and $N_4(l)$ (l=1,2,3) are provided by Table I. The results of $D_L \geq 0$ can be obtained similarly and not to be covered again.

Give an example to explain the whole process of the proposed IAS method:

1) Firstly, if the summation of $N_1^{opt}(k\text{-}1)$ and $N_2^{opt}(k\text{-}1)$ is equal to N with $D_{za} \geq 0$, according to Table I, the corrected COs (N_1, N_2) should belong to:

$$\left[\left(N_1^{opt}-1, N_2^{opt}\right), \left(N_1^{opt}, N_2^{opt}\right), \left(N_1^{opt}, N_2^{opt}-1\right)\right]$$

2) Then, if the summation of $N_1^{opt}(k\text{-}1)$ and $N_2^{opt}(k\text{-}1)$ is equal to N-1 with $D_{zb} < 0$, according to Table I, the corrected COs (N_3, N_4) should belong to:

$$\left[\left(N_3^{opt}, N_4^{opt}+1\right), \left(N_3^{opt}+1, N_4^{opt}+1\right), \left(N_3^{opt}+1, N_4^{opt}\right)\right]$$

3) Finally, if $D_L \geq 0$, according to Table II, the corrected COs (N_1, N_2, N_3, N_4) should belong to:

$$\left[\begin{array}{c} \left(N_1^{opt}-1, N_2^{opt}, N_3^{opt}, N_4^{opt}+1\right), \\ \left(N_1^{opt}\text{-}1, N_2^{opt}, N_3^{opt}+1, N_4^{opt}+1\right), \left(N_1^{opt}, N_2^{opt}, N_3^{opt}+1, N_4^{opt}+1\right), \\ \left(N_1^{opt}, N_2^{opt}, N_3^{opt}+1, N_4^{opt}\right), \left(N_1^{opt}, N_2^{opt}\text{-}1, N_3^{opt}+1, N_4^{opt}\right) \end{array}\right]$$

To conclude, the proposed IAS method contains two steps. The first step takes advantages of the relations of (23) to design the evaluated COs of each phase shown in Table I. The second step takes advantages of the relations of (28) to synthetically design the evaluated COs for two-phase shown in Table II. Fig.8 shows the flowchart of the proposed IAS method.

Table III shows a comparison of the number of evaluated COs with different adjacent search methods for two-phase MMC system. It is worth to mention that though the existing AS methods in MPC are designed for single or three-phase MMC [53]-[54], it's easy to extend these AS methods to two-phase MMC system and the specific extension process is given in Appendix II. When using the fast MPC method [53], the number of the evaluated COs is 7 but the maximum output level of two-phase is only $2N$+1, this is because the total inserted number of each phase is fixed as N. Both the preselection MPC method [54] and the proposed IAS method allow the total inserted number of each phase to fluctuate with the condition of $N\text{-}1 \leq N_1+N_2 \leq N+1$, so the maximum output level of two-phase can be up to $4N$+1, which benefits for the lower harmonic distortion of the output voltage. However, the number of evaluated COs with preselection MPC is increased to 17. When using the proposed IAS method, the number of the evaluated COs is only 5 at most and less than that of the fast MPC method. Compared

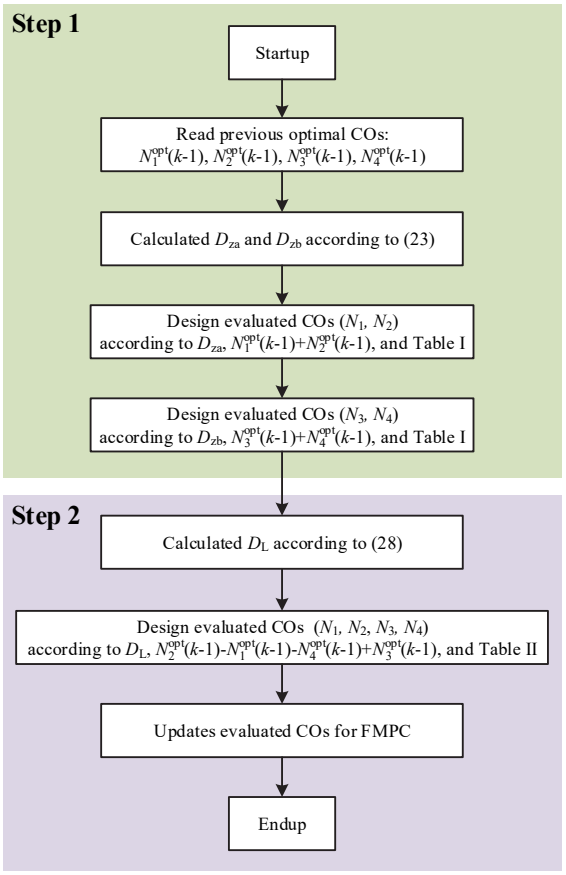

Fig. 8. The flowchart of the proposed IAS method.

to the preselection method in [54], the proposed IAS can further reduce the evaluated COs of two-phase MMC by considering the relations of the predicted current with the reference current. It is worth to mention that the proposed IAS method could be extended to larger ε to ensure the suppression performance of harmonic circulating current when the number of SMs is pretty large.

D.MMPC for FBC

1) Principle of error elimination

To apply the MMPC method for FBC, the reference output voltage is transferred to the reference inductor current via (25) and (26). Therefore, the subsequent content is discussed based on the tracking control of the inductor current.

According to (1), the discretization equation of the inductor current can be obtained based on the control period T_h as expressed in (29) shown at the bottom of the page. Noting that the current optimal CO $N_j^{opt}(k)$ of the MMC has been provided by FMPC method at time instant kT_m and remain unchanged from time instant kT_m to $(k+1)T_m$, the predicted inductor current at time instant $(k+1/q)T_m$ could be deduced via (29) with a given s_H. If s_H remains unchanged from time instant kT_m to $(k+1/q)T_m$, an error e_L will be generated inevitably at time instant $(k+1/q)T_m$:

$$e_L = i_L^{*ref}\left(k+\frac{1}{q}\right) - i_L\left(k+\frac{1}{q}\right) \tag{30}$$

To eliminate this error, the rate of change of inductor current

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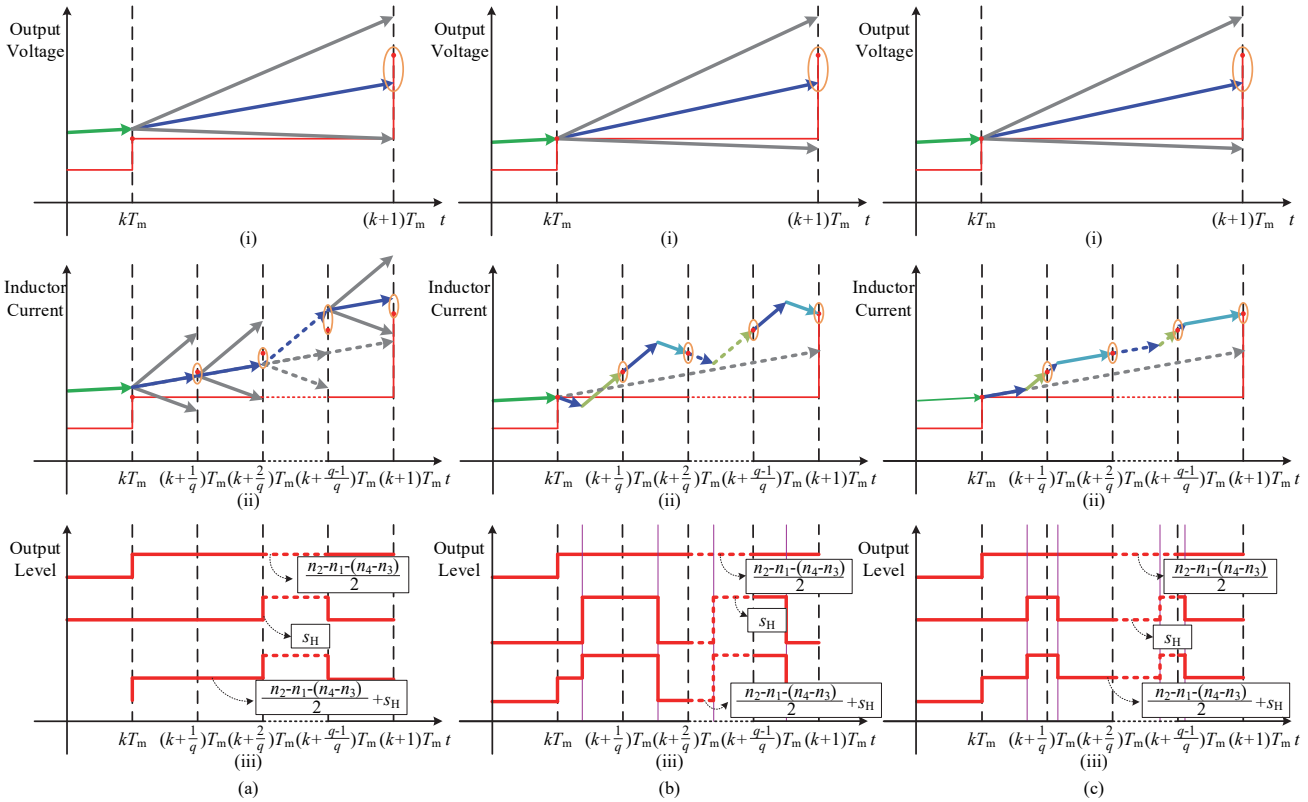

Fig. 9. Operation principle of the different MPC methods. (a) Traditional GFMPC. (b) HMPC-I. (c) HMPC-II. [(i) Output voltage. (ii) Inductor current. (iii) Output multilevel voltage of MMC, FBC, and M3C.]

R_c is introduced as expressed in (31) shown at the bottom of the page. R_c can be seen as a function regarding s_H and there are three kinds of values for s_H with -1, 0, and 1, respectively. When s_H=1, the value of R_c will increase, while s_H=-1, the value of R_c will decrease. When s_H=0, the value of R_c will keep constant, also meaning that the FBC is bypassed and shows no effect on the inductor current. So, to eliminate the e_L, two different s_H could be applied synthetically in each control period T_h. Here, we could define that s_1 represents s_H that applied from time instant kT_m to $(k+d/q)T_m$ and s_2 represents s_H that applied from time instant $(k+d/q)T_m$ to $(k+1/q)T_m$, where d denotes the duty cycle for s_1. The detailed operation principle for error elimination is given as follows:

***Case* 1**: when e_L is greater than zero with s_1=-1, s_2=1 (or s_2=0) could be introduced to make e_L zero;

***Case* 2**: when e_L is less than zero with s_1=1, s_2=-1 (or s_2=0) could be introduced to make e_L zero;

***Case* 3**: when e_L is greater than zero with s_1=0, s_2=1 could be introduced to make e_L zero;

***Case* 4**: when e_L is less than zero with s_1=0, s_2=-1 could be introduced to make e_L zero.

It is worthwhile to mention that when e_L is greater than zero with s_1=1 or less than zero with s_1=-1, no s_H could be used for s_2 to make e_L zero. In this case, keeping the original s_1 from time instant $(k+d/q)T_m$ to $(k+1/q)T_m$ can help reduce e_L. This particular case can always be ignored as long as the DC-link voltage of FBC is appropriately configured, which will be discussed in detail in subsequent analysis.

$$i_L\left(k+\frac{1}{q}\right)=\frac{T_h}{2(L+L_f)}\left[u_2\left(k+\frac{1}{q}\right)-u_1\left(k+\frac{1}{q}\right)-u_4\left(k+\frac{1}{q}\right)+u_3\left(k+\frac{1}{q}\right)+2s_H U_{dc2}-2u_o(k)\right]+i_L(k) \tag{29}$$

with

$$u_j\left(k+\frac{1}{q}\right)=N_j^{opt}(k)\,u_{jave}(k),\ j=1,2,3,4$$

$$R_c(s_H)=\frac{U_{dc2}}{(L+L_f)}s_H+\frac{1}{2(L+L_f)}\left[\underbrace{u_2\left(k+\frac{1}{q}\right)-u_1\left(k+\frac{1}{q}\right)-u_4\left(k+\frac{1}{q}\right)+u_3\left(k+\frac{1}{q}\right)}_{\text{Constant from } kT_m \text{ to } (k+1)T_m}-2u_o(k)\right] \tag{31}$$

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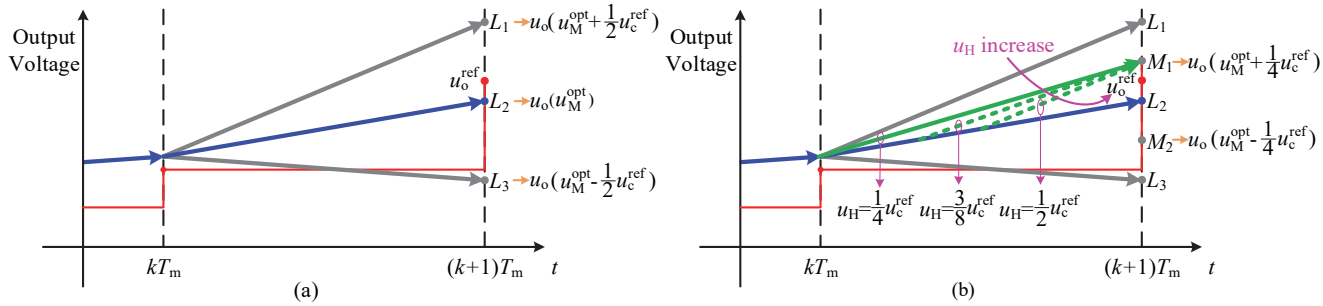

Fig. 10. Effect of DC-link voltage configuration of FBC on the steady performance.

2) Duty cycle calculation

According to (29) and (31), the predicted inductor current at time instant $(k+1/q)T_m$ could be deduced as:

$$i_L\left(k+\frac{1}{q}\right)=i_L(k)+R_c(s_1)dT_h+R_c(s_2)(1-d)T_h \quad (32)$$

By substituting $i_L^{ref}(k+1/q)$ into (32), the optimal duty cycle d^{opt} could be calculated:

$$d^{opt}=\frac{i_L^{ref}\left(k+\frac{1}{q}\right)-i_L(k)-R_c(s_2)}{\left(R_c(s_1)-R_c(s_2)\right)T_h} \quad (33)$$

In order to avoid introducing additional switching operations, s_1 at current time instant could be always consistent with the s_2 at the previous time instant. In such condition, there is only one switching operation happens during the control period T_h. s_2 at the current time could be selected according to ***Cases 1*** to ***Cases 4***. It can be seen that both ***Cases 1*** and ***Cases 2*** have two choices for s_2. So according to whether s_2 can obtain the zero value or not, the HMPC is divided into two categories: HMPC-I and HMPC-II. HMPC-I method eliminates the error by alternately using the different s_H with the values of '-1' and '1', while HMPC-II method eliminates the error by alternately using different s_H with the values of 0 and 1, or 0 and -1. It is obvious that the ripple of inductor current introduced by HMPC-I is larger than that introduced by HMPC-II. Fig. 9 shows the operation principle of the different MPC methods. Fig. 9(a) shows the global FMPC method for M3-SMPA, i.e., not only the optimal CO of the MMC but also the output state of the FBC are determined by the FMPC method. In order to distinguish it from the FMPC part in HMPC, we call it a GFMPC method in the subsequent description.

3) Effect of DC-link voltage configuration on the steady performance

According to (1), (3), and (26), the output voltage based on control period T_m could be predicted as follows

$$u_o(k+1)=a\left(\frac{u_2-u_1-u_4+u_3}{2}+s_H U_{dc2}\right)+b \quad (34)$$

with

$$a=\frac{T_m^2}{C_f(L+L_f)}$$

$$b=u_o(k)\left(1-\frac{T_m^2}{C_f(L+L_f)}\right)+\frac{T_m}{C_f}\left(i_L(k)-i_o(k)\right)$$

With the characteristic of the given search space shown in Fig. 5(c) and Fig. 5(d), the MMC has the ability to output $2N+1$ levels for each phase and $4N+1$ levels for two-phase. In order to analyze conveniently, we assume that the SMs capacitor voltages are equal to u_c^{ref}, so the equivalent output multilevel voltage u_M for MMC will satisfy:

$$u_M=\frac{u_2-u_1-u_4+u_3}{2}\approx\frac{n^{\Delta}}{2}u_c^{ref}\in\underbrace{\left[-N,-N+\frac{1}{2},\cdots,N-\frac{1}{2},N\right]}_{4N+1}u_c^{ref} \quad (35)$$

Firstly, assuming that s_H is zero, the optimal u_M^{opt} could be obtained by FMPC method and the corresponding predicted output voltage is defined as $u_o(u_M^{opt})$ which is symbolized by L_2 shown in Fig. 10(a). Obviously, there exists an inevitable error between $u_o(u_M^{opt})$ and u_o^{ref}. It can also be noted that there exists a positive linear correlation between u_o and u_M due to the positive value for coefficient a. So according to (35), the adjacent predicted output voltages can be defined as $u_o(u_M^{opt}+u_c^{ref}/2)$ and $u_o(u_M^{opt}-u_c^{ref}/2)$ which are symbolized by L_1 and L_3, respectively, as shown in Fig. 10(a). Then, an optimal interval is introduced and the boundary of optimal interval is symbolized by M_1 and M_2 shown in Fig. 10(b). To satisfy the requirement that u_M^{opt} can always be the optimal solution as long as u_o^{ref} is inside the optimal interval, the corresponding predicted value of M_1 and M_2 should satisfy the following relations:

$$\begin{cases} u_o(M_1)=u_o\left(u_M^{opt}+\frac{1}{4}u_c^{ref}\right) \\ u_o(M_2)=u_o\left(u_M^{opt}-\frac{1}{4}u_c^{ref}\right) \end{cases} \quad (36)$$

According to (34), it is obvious that $u_o(u_M^{opt})$ could be close to u_c^{ref} by regulating s_H, i.e., u_H. Considering the critical condition that the absolute error between u_o^{ref} and $u_o(u_M^{opt})$ reaches the maximum value, i.e., u_o^{ref} is located M_1 or M_2 as shown in Fig. 10(b), the maximum absolute error could be eliminated when the following relationship is satisfied:

$$U_{dc2}>\frac{1}{4}u_c^{ref} \quad (37)$$

When U_{dc2} is equal to $u_c^{ref}/4$, the rate of change after synthesizing is indicated by a solid green line. In this case, the maximum absolute error is just eliminated completely. As U_{dc2} increases, the rate of change would increase correspondingly. It is worth to mention that when U_{dc2} is much lower than $u_c^{ref}/4$, the error cannot be eliminated completely. When u_H is much larger than $u_c^{ref}/4$, the error could be eliminated effectively, however, the ripple, especially for inductor current, will also increase

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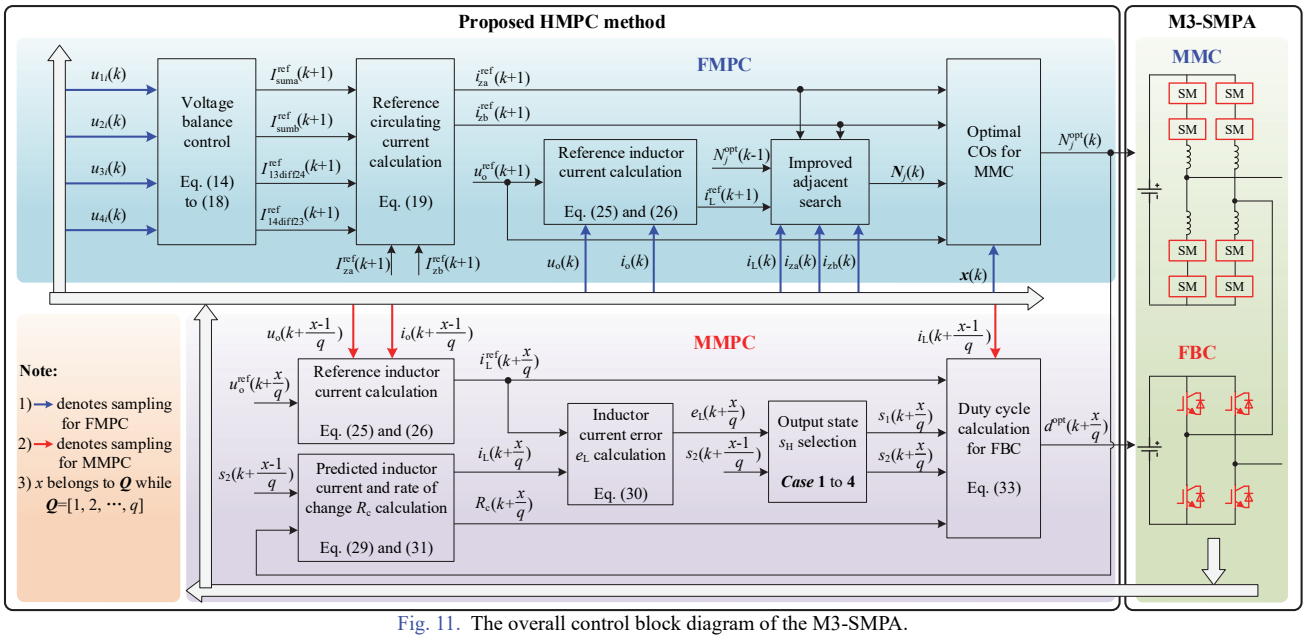

Fig. 11. The overall control block diagram of the M3-SMPA.

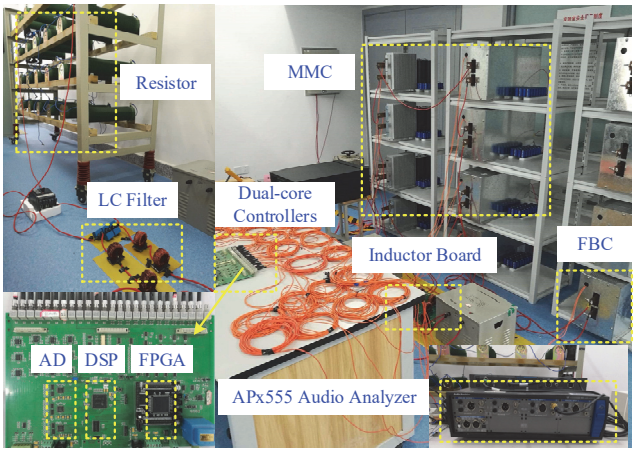

Fig. 12. Experimental setup of the M3-SMPA.

TABLE IV
MAIN PARAMETERS OF M3-SMPA IN DOWNSCALED PROTOTYPE

Parameters	Value
MMC DC-link voltage U_{dc1}	400 V
FBC DC-link voltage U_{dc2}	60 V
Rated SMs voltage u_c^{ref}	200 V
Number of SMs per arm N	2
SM capacitance C_{sm}	5 mF
Arm inductance L	1 mH
Filter inductance L_f	1 mH
Filter capacitance C_f	1.58 μF
Load resistance R	32 Ω
MMC control period T_m	50 μs
FBC control period T_h	12.5 μs
Operation frequency f	50 Hz

unexpectedly.

Synthesizing the above proposed control methods, the overall control block diagram of the M3-SMPA is shown in Fig. 11. It is worth to mention that the optimal CO $N_j^{opt}(k)$ calculated by FMPC would be further transformed into optimal switching states via sorting algorithm. Then the optimal switching states would act on MMC from time instant kT_m to $(k+1)T_m$. The optimal duty cycle $d^{opt}(k+x/q)$ calculated by MMPC would act on FBC from time instant $(k+(x-1)/q)T_m$ to $(k+x/q)T_m$ with $x \in [1, 2, \ldots, q]$. It is obvious that the optimization process of FMPC and MMPC is executed with two-time scale. Note that the control delay is not considered in Fig. 11. The one-step delay compensation method proposed in [66] is utilized in this paper to compensate for the control delay.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed control methods for M3-SMPA, the experiments are designed and constructed in the lab as shown in Fig. 12. The main parameters are listed in Table IV. For LC filters, a film capacitor is chosen as filter capacitor due to its high ac voltage and high reliability at relatively low size, while a sendust magnetic coil inductor is chosen as filter inductor due to its high saturation flux density at relatively low size. An Audio Precision APx555 Audio Analyzer [69] is used to generate the reference signal and measure the distortion performance of output inductor current and output voltage. The reference output signal is provided by the analog generator outputs of APx555, and the output terminals of current probe and voltage probe are connected to the analog analyzer inputs of APx555. High-performance analyzer settings are used in the APx555 so as to minimize any distortion and noise from the measurement equipment itself. Since MPC requires a powerful digital control platform due to the computation burden for prediction and optimization, a dual-core controller with DSP (TMS320F2812) and FPGA (EP2C8Q208) are jointly used to share computations and execute sophisticated control algorithm. The DSP is mainly responsible for the improved adjacent search method and rolling optimization process while the FPGA executes sampling, duty cycle calculation, sorting algorithm and generate pulse signals to control the

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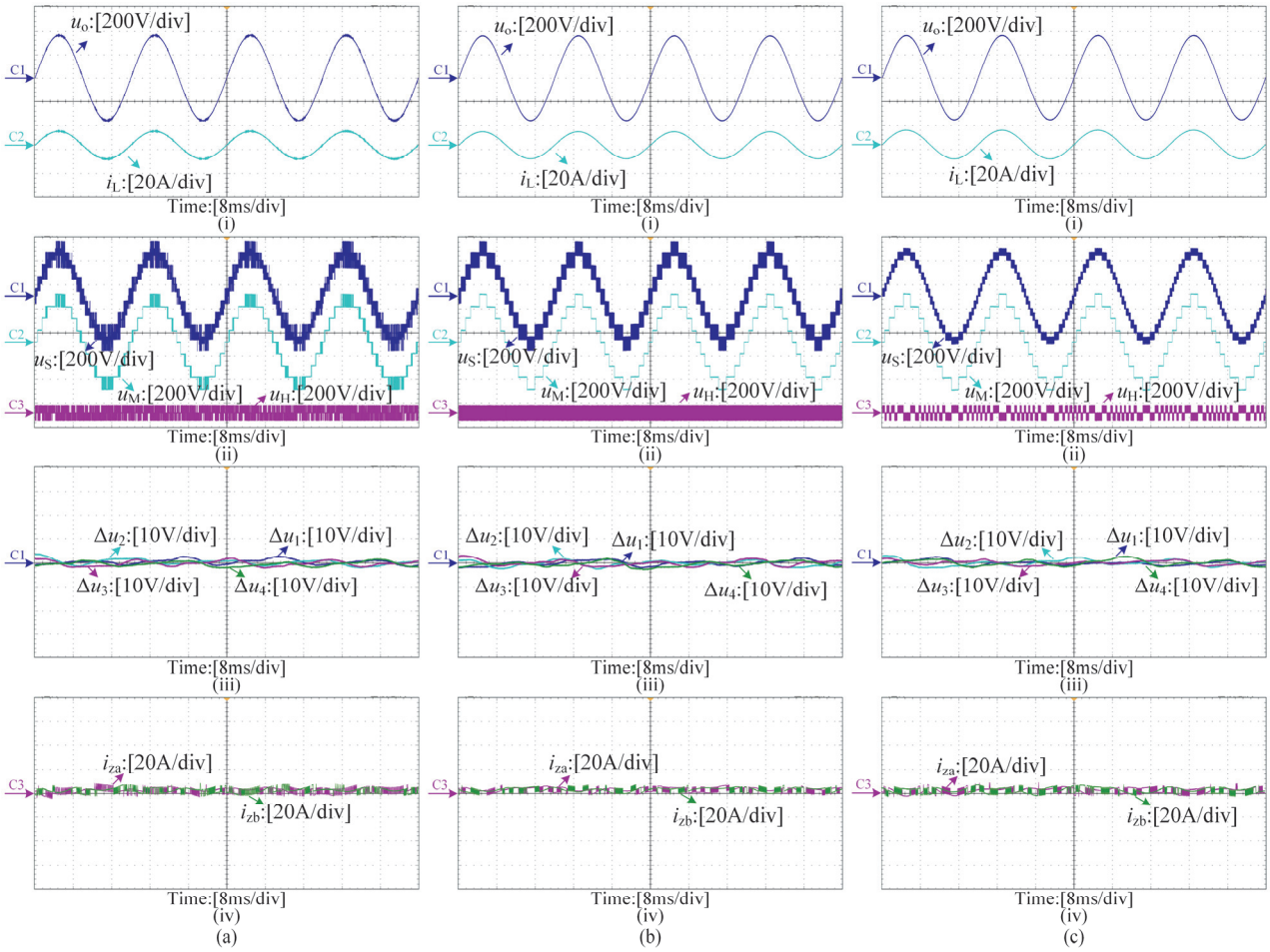

Fig. 13. Steady-state performance with different MPC methods. (a) Traditional GFMPC. (b) HMPC-I. (c) HMPC-II. [(i) Output voltage and inductor current. (ii) Output multilevel voltage of M3C, MMC, and FBC. (iii) SMs capacitor voltages. (iv) Circulating currents.]

TABLE V
STEADY-STATE PERFORMANCE COMPARISON WITH DIFFERENT MPC METHODS

	m=0.9			m=0.5		
Performance	GFMPC	HMPC-I	HMPC-II	GFMPC	HMPC-I	HMPC-II
i_{L_THD}	4.28 %	1.03 %	0.56 %	5.86 %	2.06 %	0.92 %
u_{o_THD}	1.44 %	0.1 %	0.08 %	1.88 %	0.18 %	0.09 %

switching states of SMs.

1) Steady-state performance

The steady-state performance of traditional GFMPC, HMPC-I, and HMPC-II is tested and the corresponding experimental results are presented in Fig. 13 and Table V. The experimental results of GFMPC are shown in Fig. 13(a). The modulation of reference output voltage is set to 0.9. The actual output voltage u_o is following its own reference, as shown in Fig. 13(a)(i). The THD of output voltage and inductor current are 1.44 % and 4.28 %, respectively. Fig. 13(a)(ii) shows the output multilevel waveforms of M3C, MMC, and FBC from top to bottom. Since the total inserted number per phase of MMC is allowed to fluctuate within the range of N-1 to N+1, the maximum output level of MMC reaches nine. Noting that the output voltage of FBC contains $-U_{dc2}$, 0, and U_{dc2}, the synthesized output level of M3C reaches twenty-seven and has an asymmetrical distribution. This asymmetry is caused by the fact that the switching frequency of FBC calculated by the GFMPC method is not fixed. The first SM capacitor voltage of the four arms is shown in Fig. 13(a)(iii). It can be seen that the SM capacitor voltages are perfectly maintained at its reference value 200 V. Fig. 13(a)(iv) shows the circulating currents of MMC. The experimental results of HMPC-I are shown in Fig. 13(b). The output voltage u_o is following its reference perfectly, as shown in Fig. 13(b)(i). The THD of output voltage and inductor current are significantly reduced to 0.1 % and 1.03 %, respectively. Similar to the traditional GFMPC, the output level of MMC also reaches nine. However, different from traditional GFMPC, the output voltage of FBC only contains $-U_{dc2}$ and U_{dc2}. Therefore, the synthesized output level of M3C is eighteen but has a symmetrical distribution. This symmetry is thanks to the fact that the switching frequency of FBC calculated by the HMPC-I is fixed. The output multilevel waveforms are shown in Fig. 13(b)(ii). The SMs capacitor voltages and

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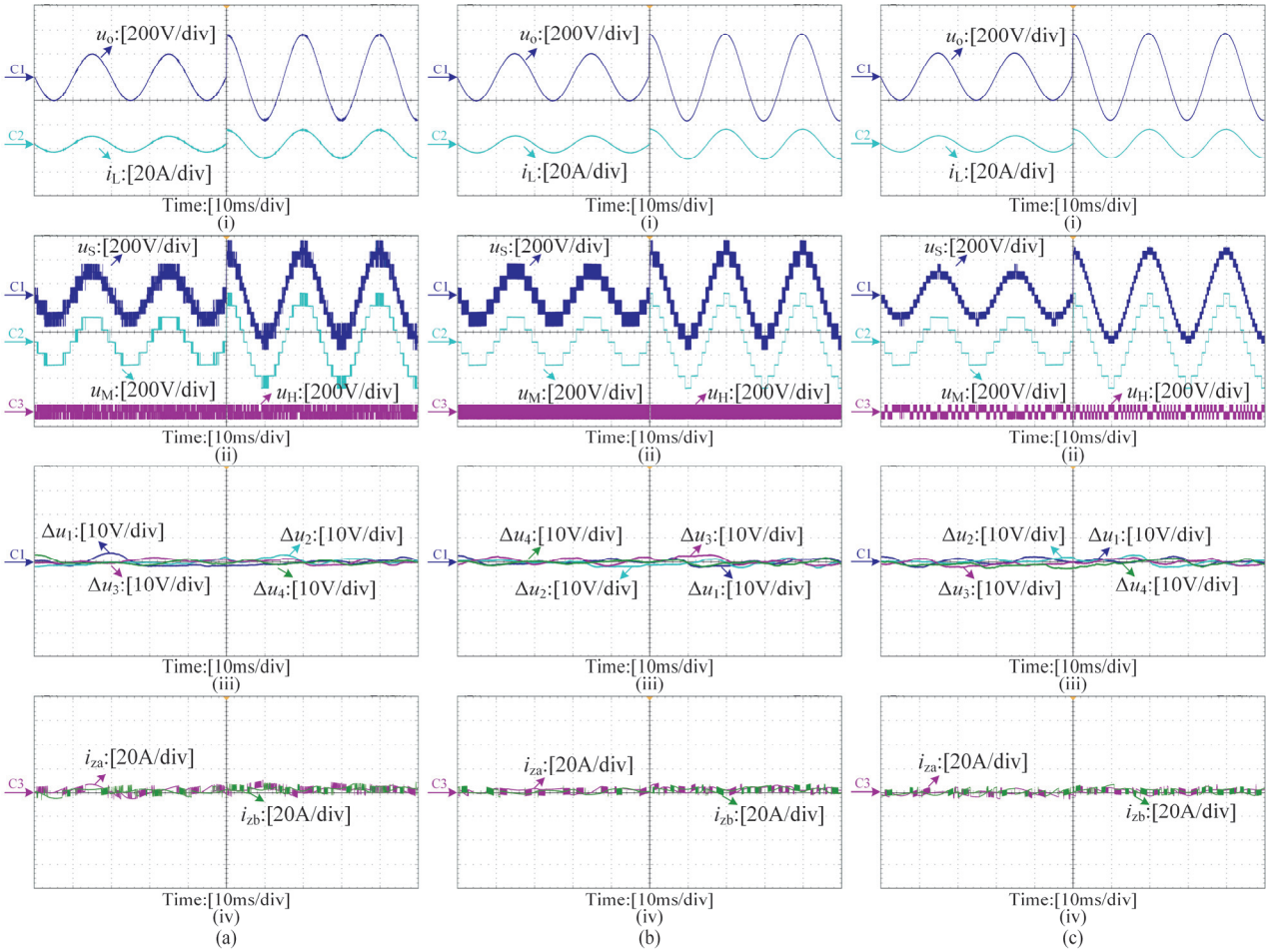

Fig. 14. Dynamic performance with different MPC methods. (a) Traditional GFMPC. (b) HMPC-I. (c) HMPC-II. [(i) Output voltage and inductor current. (ii) Output multilevel voltage of M3C, MMC, and FBC. (iii) SMs capacitor voltages. (iv) Circulating currents.]

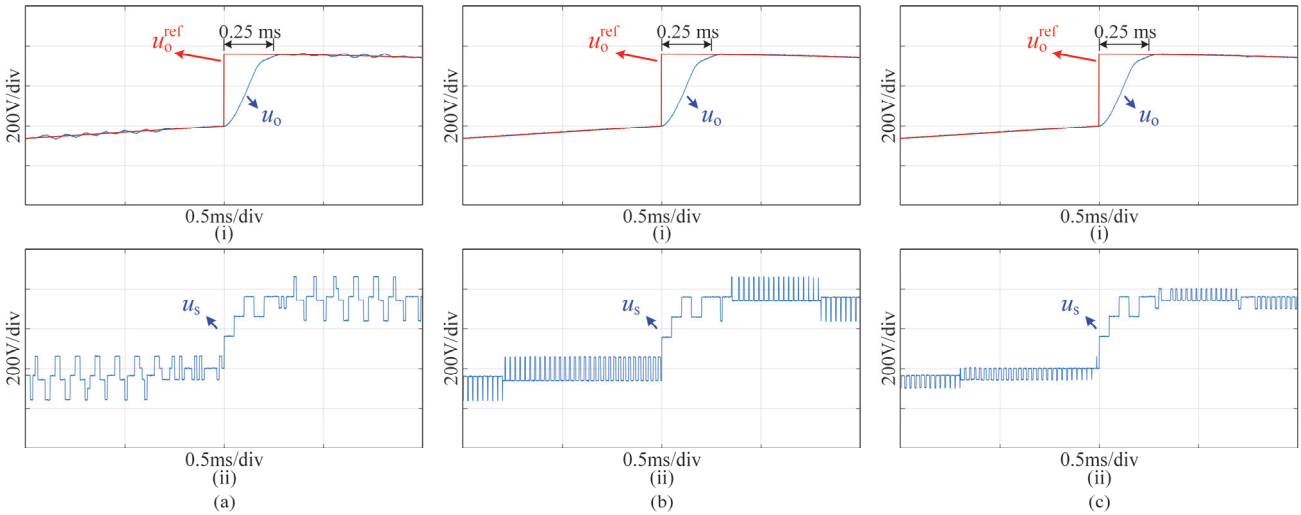

Fig. 15. Zoomed dynamic performance with different MPC methods. (a) Traditional GFMPC. (b) HMPC-I. (c) HMPC-II. [(i) Output voltage. (ii) Output multilevel voltage of M3C.]

circulating currents of HMPC-I show a similar performance as those of GFMPC shown in Fig. 13(b)(iii) and Fig. 13(b)(iv), respectively. The experimental results of HMPC-II are shown in Fig. 13(c). The output voltage u_o is following its reference perfectly, as shown in Fig. 13(c)(i). Compared with HMPC-I, the THD of output voltage and inductor current are further reduced to 0.08 % and 0.56 %, respectively. This is because the current ripple of HMPC-II is smaller than that of HMPC-I by introducing the zero output state of FBC shown in Fig. 9(c)(ii). It can be noted that the synthesized output level of M3C is not

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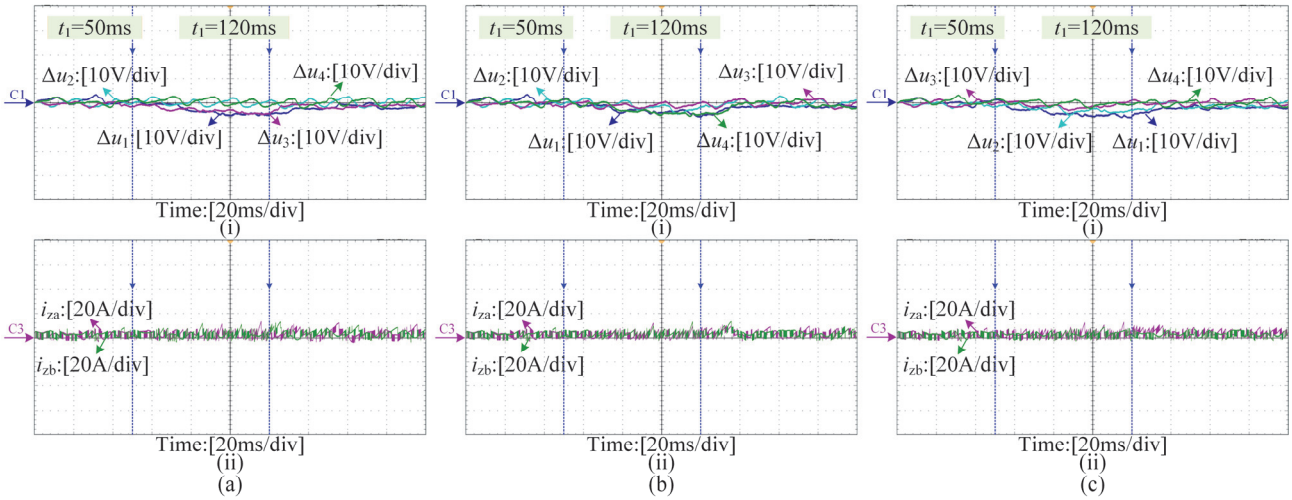

Fig. 16. Effect of balance control with different imbalance operations. (a) Switched resistors on 1st and 3rd arms. (b) Switched resistors on 1st and 4th arms. (c) Switched resistors on 1st and 2nd arms. [(i) SMs capacitor voltages. (ii) Circulating currents.]

only symmetrical but also reaches twenty-seven. This is because the FBC is able to output three voltages of $-U_{dc2}$, 0, and U_{dc2} with fixed switching frequency. The SMs capacitor voltages and circulating currents of HMPC-II show a similar performance as those of GFMPC shown in Fig. 13(c)(iii) and Fig. 13(c)(iv), respectively. The steady-state comparison performance with modulation of 0.5 is also listed in Table V and not covered again here. The experimental results verify the effectiveness of the proposed HMPC methods on improving the steady-state performance of output voltage.

2) Dynamic performance

The dynamic performance of traditional GFMPC, HMPC-I, and HMPC-II is tested and the corresponding experimental results are presented in Fig. 14 and Fig. 15. The experimental results of GFMPC with a step change in the reference output voltage are shown in Fig. 14(a). The modulation of reference output voltage is changed from 0.5 to 0.9. The output voltage shown in Fig. 14(a)(i) quickly steps to its changed reference within about 0.25 ms by observing its zoomed waveforms shown in Fig. 15(a)(i). The output level of MMC and M3C are five and fifteen respectively at m=0.5 while nine and twenty-seven respectively at m=0.9, as shown in Fig. 14(a)(ii). Due to the characteristic of adjacent search method expressed in (21), the output multilevel waveform of M3C is increased stepwise shown in Fig. 15(a)(ii), which can benefit for a reduced dv/dt. The SM scapacitor voltages remain balanced before and after the output voltage step, as shown in Fig. 14(a)(iii). The dc component of circulating current quickly changes from 0.8 A to 2.5 A, as shown in Fig. 14(a)(iv). The experimental results of HMPC-I and HMPC-II with identical step operation are shown in Fig. 14(b) and Fig. 14(c), respectively. The output voltages shown in Fig. 14(b)(i) and Fig. 14(c)(i) also quickly reaches its reference. The settling time is about 0.25 ms by observing their zoomed waveforms shown in Fig. 15(b)(i) and Fig. 15(c)(i). The output level of MMC and M3C under HMPC-I are five and ten respectively at m=0.5 while nine and eighteen respectively at m=0.9, as shown in Fig. 14(b)(ii). The output level of MMC and M3C under HMPC-II are five and fifteen respectively at m=0.5 while nine and twenty-seven respectively at m=0.9, as shown in Fig. 14(c)(ii). During the transient process, the output multilevel waveforms of HMPC-I and HMPC-II show the almost identical trend to that of FMPC, as shown in Fig. 15(b)(ii) and Fig. 15(c)(ii). Under the operation of HMPC-I and HMPC-II, the SMs capacitor voltages are well balanced and dc component of circulating currents can quickly track its changed reference, as shown in Fig. 14(b)(iii), Fig. 14(b)(iv), Fig. 14(c)(iii), and Fig. 14(c)(iv). The experimental results verify that the proposed MMPC methods can effectively ensure the output dynamic performance same as the traditional GFMPC method.

3) SMs capacitor voltage balance

The control performance of SMs capacitor voltage balance method is studied and the corresponding results are shown in Fig. 16. In order to produce a significant imbalance power among the different arms, the DC-link of each SM capacitor is connected in parallel with the switched resistor with a resistance of 300 Ω. For a fair comparison, the HMPC-II method is applied in different imbalance operations with modulation of 0.9. When the switched resistors on the DC-link of 1st and 3rd arms are inserted at t=50 ms, the SMs capacitor voltages of 1st and 3rd arms start to decrease shown in Fig. 16(a)(i). At t=120 ms, the balance control is enabled. The SMs capacitor voltages of 1st and 3rd arms return to its reference of 200 V. It can be noted that the fundamental circulating currents in the reversed phase are injected to achieve this balance, as shown in Fig. 16(a)(ii). Similarly, when the switched resistors on the DC-link of 1st and 4th arms are inserted, the SMs capacitor voltages of 1st and 4th arms start to decrease shown in Fig. 16(b)(i). After injecting the fundamental circulating currents in the same phase shown in Fig. 16(b)(ii), the SMs capacitor voltages of 1st and 4th arms return to its reference. When the switched resistors on the DC-link of 1st and 2nd arms are inserted, the SMs capacitor voltages of 1st and 2nd arms start to decrease shown in Fig. 16(c)(i). After injecting the dc circulating currents shown in Fig. 16(c)(ii), the SMs capacitor voltages of 1st and 2nd arms are also ensured. The experimental results verify the effectiveness of the SMs balance control method.

4) Effect of DC-link voltage U_{dc2} on steady-state performance

The steady-state performance with different DC-link voltage

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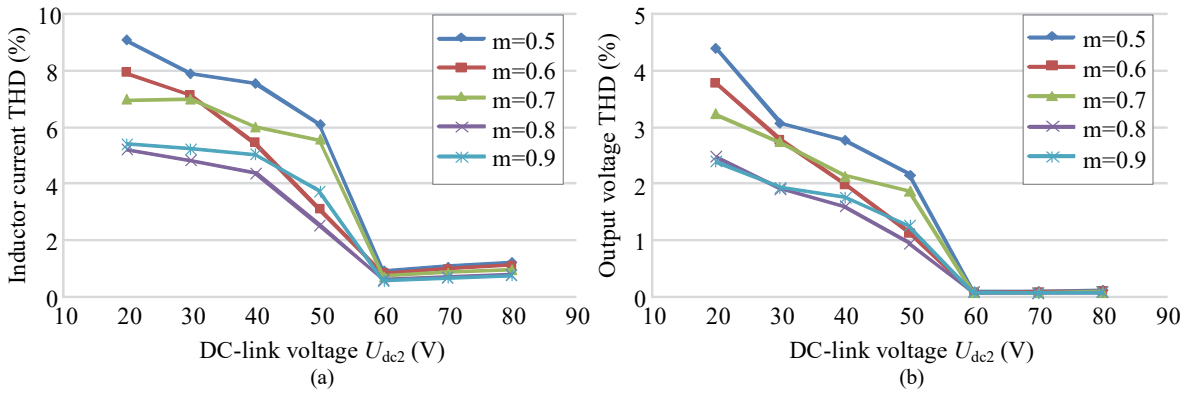

Fig. 17. Effect of DC-link voltage U_{dc2} on steady-state performance. (a) Inductor current THD. (b) Output voltage THD.

TABLE VI
PERFORMANCE COMPARISON WITH DIFFERENT DC-LINK VOLTAGE UNDER M=0.8

	DC-link voltage U_{dc2} (V)						
Performance	20	30	40	50	60	70	80
i_{L_THD}	5.2 %	4.81 %	4.38 %	2.53 %	0.61 %	0.69 %	0.77 %
u_{o_THD}	2.47 %	1.91 %	1.6 %	0.94 %	0.08 %	0.07 %	0.08 %

TABLE VII
COMPARISON OF COMPUTATION TIME (μs) WITH TWO DIFFERENT MPC METHODS

MPC Method	Parallel Data Transmission	Evaluated COs Construction	Rolling Optimization
Proposed MPC	15.87	1.61	9.03
Preselection MPC [54]	15.91	2.69	29.56

of FBC is investigated and the corresponding experimental results are shown in Fig. 17 and Table VI. For a fair comparison, the HMPC-II method is applied in different operations. It can be noted the experimental threshold value is about 60 V and a little larger than the ideal threshold value of 50 V calculated by (37). One of the significant factors is the fluctuation on the SMs voltage, which has a slight effect on (35) and (36). When U_{dc2} is lower than 60 V, both inductor current THD shown in Fig. 17(a) and output voltage THD shown in Fig. 17(b) are significantly reduced with the increase of U_{dc2}. While U_{dc2} is larger than 60 V, the inductor current THD has shown a slight increase and the output voltage THD remains almost unchanged with the increase of U_{dc2}. Taking a modulation of 0.8 as an example, when U_{dc2} is 20 V, the inductor current THD and output voltage THD are 5.2 % and 2.47 %, respectively. When U_{dc2} is 60 V, the inductor current THD and output voltage THD are reduced to 0.61 % and 0.08 % significantly, respectively. However, when U_{dc2} is 80 V, the inductor current THD and output voltage THD are 0.77% and 0.08 %, respectively. This is because when U_{dc2} is lower than 60 V, the tracking error of inductor current and output voltage cannot be eliminated by FBC effectively. In this case, the increase of the DC-link voltage could effectively reduce the tracking error. While U_{dc2} is larger than 60 V, the tracking error could be eliminated. However, the excessive value of U_{dc2} would increase the ripple of the inductor current shown in Fig. 10(b). Since the filter capacitor can absorb the harmonics generated by the ripple of inductor current, the output voltage THD is almost unaffected. It is worth to mention that the critical value of 60 V obtained by the experiments is slightly larger than the theoretical value of 50 V calculated by (37) and this difference is acceptable. The experimental results verify the correctness of theoretical analysis for the effect of DC-link voltage configuration on steady-state performance.

5) Resource consumed in FPGA and DSP

Since implementing HMPC control methods mainly suffers from the resource utilization in FPGA and time consumption in DSP [70], the debugging online is carried out to obtain these information. For Altera FPGA, the logic element (LE) is the smallest unit of logic in the Cyclone II device architecture and each LE contains a four-input LUT, a programmable register, and some other functions. There are 8256 LEs available in Altera EP2C8Q208 controller. The resource consumption on FPGA could be obtained via compiling the whole Verilog HDL files in Quartus II software v11.0. The compilation report shows that the LEs consumed for sampling, duty cycle calculation, and sorting algorithm are 1369. The resource utilization percentage of the used LEs is approximately 17 %. For TI DSP, the numeric execution time is calculated through the DSP Timer Counter Register (TxCNT) in CCStudio software v3.3. For a fair comparison, both proposed MPC method and preselection method [54] are executing with the same limitation for N_1+N_2 that limited as (N-1, N, N+1), and the comparison of computation time with different MPC methods is listed in Table VII. When using the proposed MPC method, the counter points consumed for parallel data transformation between DSP and FPGA, proposed IAS method, and rolling optimization process are 2380, 242, and 1355, respectively, which can be further equivalent to be 15.87 μs, 1.61 μs, and 9.03 μs, respectively. It

TABLE VIII
COMPARISON OF CONTROL PERFORMANCE WITH DIFFERENT TOPOLOGIES AND CONTROL METHODS

Topology and Control Method	Control Period Settings (μs)	u_{o_THD} (%)	Average Switching Frequency (kHz)
MMC with [54] method	50	6.27	1.67
MMC with [54] method	6	0.29	12.93
Proposed M3-SMPA with HMPC	50 (MMC), 12.5 (FBC)	0.27	1.53 (MMC), 19.55 (FBC)

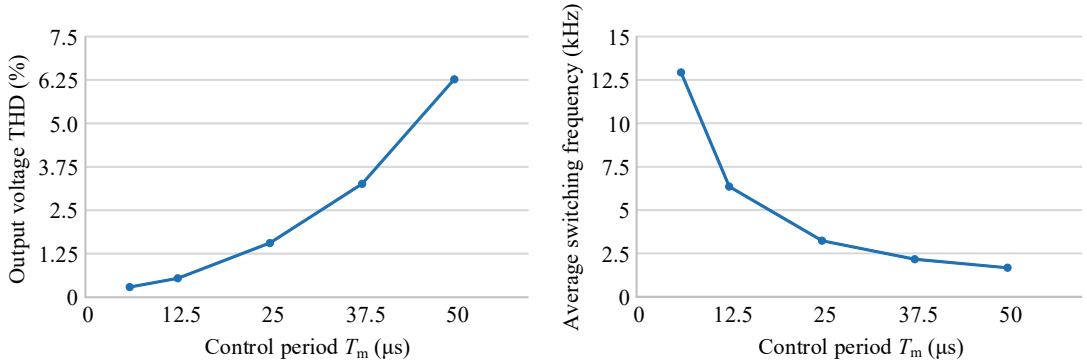

Fig. 18. The control performance of MMC with [54] method with different control periods T_m. (a) Output voltage THD. (b) Average switching frequency.

TABLE IX
COMPARISON OF POWER LOSS WITH DIFFERENT TOPOLOGIES AND CONTROL METHODS

Topology and Control Method	Control Period Settings (μs)	MMC		FBC		P_{total} (W)
		P_{con} (W)	P_{sw} (W)	P_{con} (W)	P_{sw} (W)	
MMC with preselection method [54]	50	32.71	9.02	/	/	41.73
MMC with preselection method [54]	6	30.93	69.89	/	/	100.82
Proposed M3-SMPA with HMPC	50 (MMC), 12.5 (FBC)	33.00	8.24	15.37	9.72	66.33

can be seen that the computation time for constructing evaluated COs with proposed IAS method is pretty small. This is because that if the Eq. (23) and Eq. (28) are calculated, then the evaluated COs could be constructed directly according to Table I and Table II. When using the preselection MPC method, the counter points consumed for parallel data transformation, evaluated COs construction, and rolling optimization process are 2387, 403, and 4434, respectively, which can be further equivalent to be 15.91 μs, 2.69 μs, and 29.56 μs, respectively. It can be seen that the computation time for rolling optimization is increased to 29.56μs, which is due to the increase of the evaluated COs with the preselection method. The experimental results verify the effectiveness of the proposed IAS methods for reducing the computation complexity in MPC.

V. POWER LOSS COMPARISON

To verify the advantages of proposed M3-SMPA topology and HMPC method on system efficiency, the simulation based on prototype parameters is built in PLECS integrated in MATLAB/Simulink to compare the power loss under different topologies and control methods. For a fair comparison, the power loss comparison should be conducted under the same

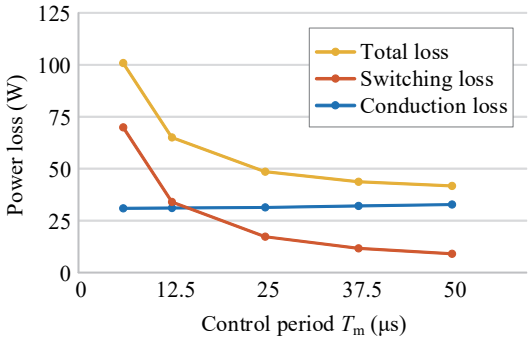

Fig. 19. The power loss of MMC with [54] method with different control periods T_m.

output performance. Firstly, the simulation results with different topologies and different control methods are presented in Table VIII. When using the proposed M3-SMPA topology and HMPC method with the control period T_m=50 μs and T_h=12.5 μs, the THD of output voltage is 0.27 %, and the average switching frequency (ASF) of the MMC and the FBC are 1.53 and 19.55 kHz, respectively. When adopting the MMC topology and the preselection [54] method with the control period T_m=50 μs, the THD of output voltage is 6.27 % and the ASF is

1.67 kHz. To improve the output performance, the control period T_m could be further reduced shown in Fig. 18(a), which also results in a higher ASF shown in Fig. 18(b). When T_m decreases to 6 μs, there is a significant improvement in output performance and the THD of output voltage decreases to 0.29 %, however, the ASF is increased to 12.93 kHz. Then the comparison of power loss with different topologies and different control methods is presented in Table IX and Fig. 19. For MMC topology with preselection method [54], It can be noted that due to the increase of ASF, there is an obvious increase in the switching loss of MMC as the control period decreases. In this case, the total loss of the proposed M3-SMPA topology with HMPC method is much lower than that of the traditional MMC topology with preselection method [54], even if the additional FBC loss is also considered. The simulation results verify the advantages of the proposed M3-SMPA topology and HMPC method on high fidelity and high efficiency.

VI. Conclusions

In this paper, a topology of MMC connected in series with FBC is studied for SMPA and a novel HMPC method is developed for M3-SMPA. The proposed HMPC has the merits of both FMPC and MMPC methods and the optimization process is executed with two-time scale. The multi-objective control of MMC including output voltage tracking, circulating current control, and SMs capacitor voltages balance is achieved by FMPC part of HMPC. While the steady-state error of output voltage is eliminated by MMPC part of HMPC using FBC with the fixed switching frequency. A circulating current injection method is introduced to balance the SMs capacitor voltages and an IAS method is proposed to reduce the number of evaluated COs of FMPC to only 5 at most in each control period. Furthermore, the effect of DC-link voltage configuration of FBC on steady-state performance is analyzed. Finally, the effectiveness of the proposed HMPC method and correctness of theoretical analysis are validated by the M3-SMPA experimental setup.

Appendix I

$$\boldsymbol{A}=\begin{bmatrix} 0 & -\dfrac{1}{L+L_f} & 0 & 0 \\ \dfrac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad \boldsymbol{B}_2=\begin{bmatrix} 0 & 0 \\ -\dfrac{1}{C_f} & 0 \\ 0 & \dfrac{1}{2L} \\ 0 & \dfrac{1}{2L} \end{bmatrix}$$

$$\boldsymbol{B}_1=\begin{bmatrix} -\dfrac{1}{2(L+L_f)} & \dfrac{1}{2(L+L_f)} & \dfrac{1}{2(L+L_f)} & -\dfrac{1}{2(L+L_f)} & -\dfrac{1}{(L+L_f)} \\ 0 & 0 & 0 & 0 & 0 \\ -\dfrac{1}{2L} & -\dfrac{1}{2L} & 0 & 0 & 0 \\ 0 & 0 & -\dfrac{1}{2L} & -\dfrac{1}{2L} & 0 \end{bmatrix}$$

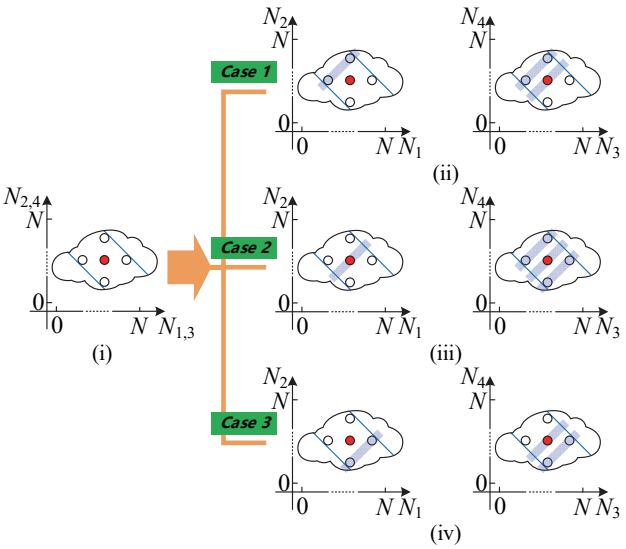

Fig. A. The evaluated COs with AS method in [54]. (i) The evaluated COs for single-phase MMC system. (ii)-(iv) The evaluated COs for two-phase MMC system.

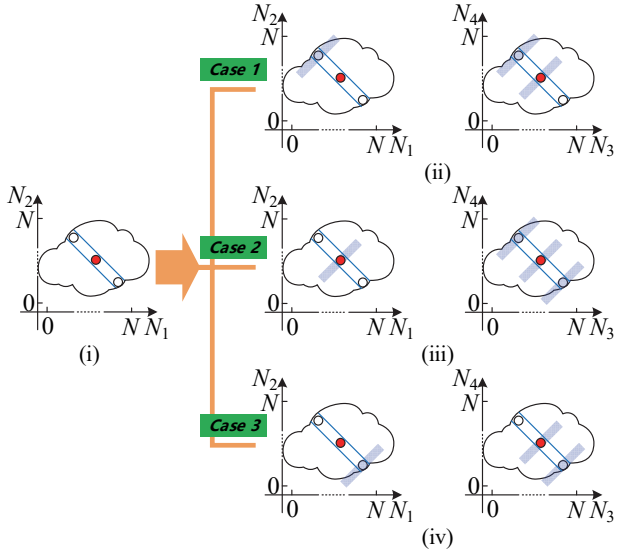

Fig. B. The evaluated COs with AS method in [53]. (i) The evaluated COs for single-phase MMC system. (ii)-(iv) The evaluated COs for two-phase MMC system.

TABLE A
The Number of Evaluated COs in Two-Phase MMC with the Available AS Methods

MPC Method	Case 1	Case 2	Case 3	Summation
AS method in [54]	6	5	6	17
AS method in [53]	2	3	2	7

Appendix II

Though the existing AS methods in MPC, such as [53] and [54], are designed for single or three-phase MMC, it's easy to extend these AS methods to two-phase MMC system. Take AS method proposed in [54] as an example for analysis. With the given limitation of the number of inserted SMs in each phase, the current output level of each phase that generated by evalu-

ated COs should be equal or adjacent to the previous output level. So the maximum number of COs for each phase MMC is 5, as shown in Fig. A(i), where the red circle denotes the previous optimal CO and will be evaluated again with the white circles in the current control period. In this way, the evaluated COs of phase-a and the evaluated COs of phase-b could be obtained separately, and the number of evaluated COs in different phase are also 5. Similarly, the current output level of two-phase MMC that generated by evaluated COs should be equal or adjacent to the previous output level of two-phase. According to the expression of output level of two-phase MMC, i.e., Eq. (24), the maximum number of evaluated COs for two-phase MMC is 17, as shown in Fig. A(ii)-(iv) and Table A, and the maximum output level capability is $4N$+1. For the AS method proposed in [53], the maximum number of COs for each phase MMC is 3, as shown in Fig. B(i), and when extending this AS methed to two-phase MMC system, the maximum number of evaluated COs for two-phase MMC is 7, as shown in Fig. B(ii)-(iv) and Table A, and the maximum output level capability is $2N$+1. It is worth to mention that for a fair comparison, the comparison results of computation complexity listed in Table III, Table VII and Table A are obtained based on the same topology, i.e., two-phase MMC system.

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