Aalborg Universitet

AALBORG UNIVERSITY
DENMARK

FS-MPC Based Thermal Stress Balancing and Reliability Analysis for NPC Converters

Novak, Mateja; Ferreira, Victor; Andresen, Markus; Dragicevic, Tomislav; Blaabjerg, Frede; Liserre, Marco

FS-MPC Based Thermal Stress Balancing and Reliability Analysis for NPC Converters

M. Novak, *Member*, V. Ferreira, *Student Member*, M. Andresen, *Member*,
T. Dragicevic, *Senior Member*, F. Blaabjerg, *Fellow Member*, and M. Liserre, *Fellow Member*

Abstract—**Active thermal control has been introduced to regulate the steady state and reduce the transient thermal-mechanical stress in power electronic modules. Specifically, it can equally distribute the temperature among the devices, thereby better distributing the stress among a set of devices and reducing the failure probability in the most thermally-stressed devices. This is of great importance for multilevel topologies and in particular for the Neutral Point Clamped (NPC) topologies, which have an inherent thermal unbalance among devices of the same phase. In hybrid structures, whereby Si and SiC devices are mixed to achieve a better trade-off between efficiency and cost, this problem is even worse due to technology differences. This paper investigates the advantages introduced by using Finite-Set Model Predictive Control (FS-MPC) algorithms designed for achieving a balanced device junction temperature in hybrid NPC and Active-NPC converters. Moreover, a novel setup composed by a hybrid ANPC based power modules is used to experimentally validate the presented FS-MPC algorithm. A lifetime estimation is performed for the two topologies to highlight the long-term benefits of FS-MPC algorithm in these hybrid topologies for UPS applications.**

Index Terms—**Active Neutral Point Clamped converter (ANPC), Neutral Point Clamped converter (NPC), Finite-set Model Predictive Control (FS-MPC), hybrid power stage, multilevel converter, SiC, lifetime**

I. Introduction

IN 1980s the three level neutral point clamped (NPC) converter was introduced for the medium-voltage large power variable speed drives to improve the conversion efficiency [1]. It was soon noticed that the maximum output power was limited by the unbalanced stress distribution of the power

components [2], [3]. Efforts have been made to solve the problem by sizing the components for the expected stress [4]. However, different converter operating points will produce different temperature distributions. Therefore, for solving this problem not only the hardware needs to be adapted but also the control algorithm needs to take into account different stress distributions of the operating points of the converter.

One of the most popular solutions was the active neutral point clamped (ANPC) topology, first introduced in [2]. The loss distribution is balanced by using the redundant switching states. In [5] online loss calculations are used for the estimation of the junction temperatures, which are used in the control unit. The proposed PWM-based control strategy in [6] has managed to outperform the other PWM algorithms and provide balanced loss distribution. However, it was not experimentally validated. A comparison of three PWM methods with phase shifted carriers is presented in [7]. The methods are very easy to implement, but it is not validated how the methods would performs in terms of the power quality and neutral point (NP) voltage balancing. The methods from [7] were compared to a new balancing method proposed by the authors in [8]. The proposed method is based on space vector PWM and uses loss balancing sequences, which depend on the modulation index. In [9] authors proposed an adaptive double frequency (ADF) PWM that can adapt the duty cycles to optimize the loss distribution. Nevertheless, it is not shown whether the algorithm can also balance the NP voltage or another control loop is required. Another method that combines the ADF PWM and adjustable loss distribution is proposed in [10]. It is most common to use two different zero voltage combinations for positive and negative half line cycle, however in order to balance the losses the use of only one zero voltage combination is proposed in [11]. The results showed higher efficiency but the loss distribution was still unbalanced. The loss distribution can also be improved by carefully defining the commutation sequences and selecting optimum devices for each position as shown in [12].

Algorithms based on FS-MPC have the possibility to include multiple objectives in a single cost function without the necessity of additional control loops [13]–[15]. The fact that control of the output voltage/current, NP balancing and loss distribution can be fulfilled in one single cost function, makes them a very promising alternative to traditional linear algorithms for ANPC applications. In [13] the FS-MPC is divided into two cost functions: in the first current control and NP balancing are evaluated and in the second the loss energy

balancing. The calculation and search time of the algorithm are reduced in [14] where only one cost function is used and the power losses are predicted using a function that contains the most stressed devices. The algorithm presented in [15] is a combination of selective harmonic eliminated (SHE) PWM and MPC. Despite the fact that the method showed decreased junction temperatures and increased output power, the high computational burden prevented an experimental validation. It should be noted that neither of algorithms in [13]–[15] take into account thermal cross coupling among the switches and different technology, corresponding to chip size. Another combination of the linear controller and FS-MPC algorithm was proposed in [16]. Here the current reference is provided by a linear controller, while FS-MPC is used to select one of the four zero voltage level switching combinations. A thermal model is required for calculation of the device losses and junction temperature predictions.

Although the maximum power rating of the ANPC converter was increased in aforementioned publications, the market still demands for even higher power density converters with smaller and lighter filters. To achieve this, one possibility is to increase the converter switching frequency, which on the other hand will introduce higher switching losses. To overcome this problem, one solution is to adopt SiC Power MOSFETs, that consume lower energy during the turn-off process. Conversely, the MOSFETs have higher conduction losses and SiC devices are more expensive, thereby considerably increasing the cost of a multilevel structure. However, strategically replacing just some of the devices with wide band gap (WBG) devices and combining with an efficient use of their low switching losses and Si-IGBT's conduction characteristics, especially for high currents [17]–[19] the miniaturization can be achieved with higher efficiency and relatively lower cost.

A hybrid ANPC (h-ANPC) converter example is shown in Fig. 1 where SiC MOSFETs (T_2, T_3) are used as the inner switches. In [20] the two SiC device topology from Fig. 1 was compared to four SiC device (T_1, T_2, T_3, T_4) h-ANPC topology. One of the conclusions was that higher efficiency and lower cost was obtained for the two SiC device h-ANPC but the thermal balance characteristic was better for the four SiC device h-ANPC. Thus, a development of the control algorithm that could reduce the unbalance would make the two SiC device h-ANPC a superior topology in three aspects.

This work presents a wider investigation of the FS-MPC strategies for pure Si and hybrid NPC converters, presented by the authors in conference papers [21], [22]. Moreover, the FS-MPC algorithm is applied for the first time to an h-NPC structure, and its advantage is demonstrated. As a benchmark, a carrier based modulation methods are used [19], [23]. The presented strategies are validated on a three level h-ANPC converter prototype. In addition, a lifetime-oriented study is carried out, whereby the three solutions are compared to the benchmark ones. The target converter application is a three phase uninterruptible power supply (UPS) with the power rating of 36 kW and 400 V output voltage.

The structure of the paper is the following. In Section II an overview of thermal stress redistribution methods for multilevel converters is presented. The h-ANPC topology
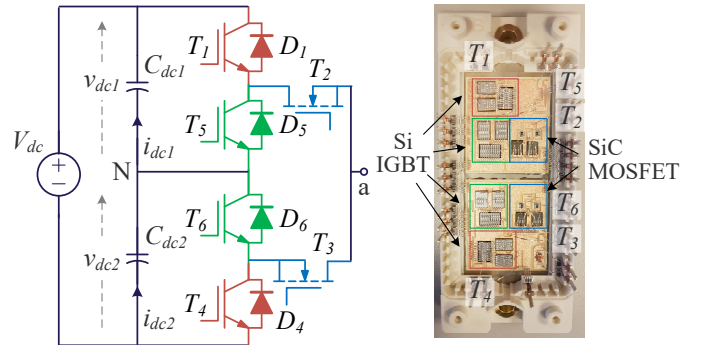

Fig. 1: Single phase hybrid active neutral point clamped (h-ANPC) open module.

is presented in Section III and the control algorithms are explained in Section IV. In Section V the steady state performance of the control algorithm is presented. Evaluation of the loss distribution and the reliability estimation are done in Section VI and Section VII, respectively. Conclusions are given in the last section.

II. THERMAL STRESS REDISTRIBUTION METHODS FOR MULTILEVEL CONVERTERS

In Table I, eight thermal stress distribution methods that can be applied for multilevel converters were selected for a comparison [9], [13], [16], [22], [24]–[29]. The methods are divided into three categories based on the control method: space vector control [24], [25], carrier-based PWM [9], [26]–[28] and model predictive based control [13], [22], [29], [30]. For all the methods the requirements for implementation and limitations are provided. The temperature feedback is used to achieve an even stress distribution in [27], [29]–[31]. This concept is defined as active thermal control concept and it can be implemented for all three control method categories like [28], [29], [31] shown in Table I. The temperature feedback can be obtained either by direct junction temperature measurement, measurements of device's thermosensitive parameters or using device's thermal model to estimate the temperature. The first two solutions are not very practical as they require expensive high-bandwidth temperature measurement equipment or additional circuity [31]. Furthermore, some of the mentioned solutions have a limited application [22], [24], [26].

A common drawback of stress distribution methods is increased harmonic distortion, thus control modifications are necessary to reduce the harmonics [26], [28]. It can also be observed in Table I, that it will be necessary to find a trade-off between the system performance and the effectiveness of the thermal stress distribution. For predictive control methods in [13], [22], [29], [30], this is done by adjusting the weighting factors in the cost function. However, the multi objective cost function with four weighting factors presents a very complex optimization problem. On the other hand, some methods like [15] require a powerful control platform. From the MPC methods, [22] has the simplest implementation and only two weighting factors. The tuning of the weighting factors has to be adjusted to the operating conditions of the converters using one of the advanced weighting factor tuning methods [32].

To solve the above discussed limitations, we will demonstrate that a FS-MPC algorithm can be tailored to evenly redistribute the thermal stress between the devices of the NPC converters. The algorithm does not require a junction temperature estimation, it is using the measurements that are already available in the algorithm. Thus, thermal device characteristics from the data-sheets is not needed in the control algorithm nor a thermal stress detection algorithm during operation like in [16], [27], [29], [30]. This makes the implementation simpler than in [15], [27], [29], [31].

III. HYBRID SiC ANPC CONVERTER

As mentioned in the Introduction, in order to comply with market's need for high power density converters with small and lighter output filters, the switching frequency needs to be increased. To reduce the switching losses WBG devices must be used. Replacing all the devices with WBG devices would be an expensive solution and it may not be necessary if we know, which devices are the ones that suffer under high switching losses. In this case we are looking at applications for unidirectional power flow with a high modulation index like UPS systems, where the inner devices of an ANPC have the highest losses. Thus, the advantages of Si and SiC are combined in the power module by utilizing Si-IGBTs for low conduction losses and SiC MOSFETs for low switching losses using the open modules like shown in Fig. 1.

The module contains two SiC MOSFETs S_2 and S_3, which have two parallel connected chips (V_{DS} = 650 V, $R_{DS(on)}$ = 23 mΩ, I_D = 75 A) and four IGBTs which are also realized as parallel connected chips (V_{CE} = 650 V, I_C = 75 A). For a single phase module, eight different switching combinations can be applied, two combinations that connect the output to the positive DC voltage, two combinations that connect to the negative and four combinations that can realize the zero voltage [6], [33]. However, for ensuring the optimal operation of the power devices, only one positive, one negative and two redundant zero voltage combinations will be used as shown in Table II [19]. The switch state S_1 belongs to device T_1, S_2 belongs to device T_2 etc. It can be noticed that devices $T_1 - T_6$, $T_4 - T_5$ share the gate signals and that $T_2 - T_3$ are complementary pairs. The zero voltage state "0^+" is only used in the positive cycle and zero voltage state "0^-" in the negative cycle. In this way only two switches need to change the state while transitioning from "P" state to "0^+" and "N" to "0^-" respectively. Moreover, only inner switches ($T_2 - T_3$) are changing the states during the half cycle i.e. the MOSFETs are switched with a higher switching frequency to take the advantage of the low switching losses of the devices.

IV. CONTROL ALGORITHM

For the h-ANPC prototype we have chosen to develop a control algorithm based on the FS-MPC because the algorithm offers a simple inclusion of multiple objectives in the control cost function and a fast transient response [34]. The objectives that need to be taken into account in the control design are: voltage reference tracking, NP balancing and device temperature balancing. As pointed out in the previous sections,
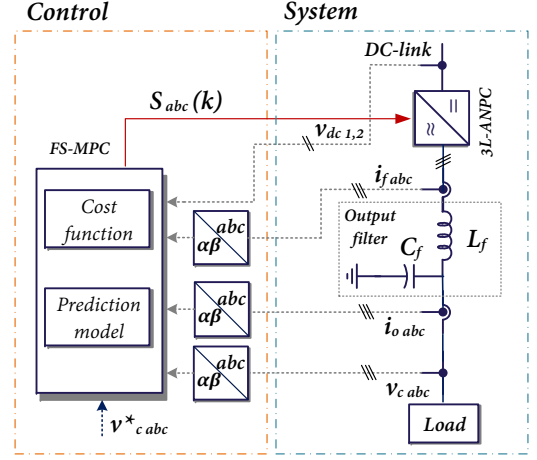

Fig. 2: Simplified system model scheme of 3L-ANPC converter using model predictive control (FS-MPC).

depending on the application (modulation index, power factor) the stress distribution of the ANPC converter will change. In our case, the converter is expected to be working with a high modulation index and unidirectional power flow in a UPS system. The algorithm needs be able to reduce the switching stress of the devices that have the highest switching losses and distribute it to the less thermal stressed devices.

The schematic of the system can be seen in Fig. 2. In each sampling period the FS-MPC controller collects the measurements of the DC-link voltages ($v_{dc1,2}$), converter output current ($i_{f\,abc}$), filter capacitor voltage ($v_{c,\,abc}$) and load current ($i_{o,\,abc}$) to calculate the propagations of the voltages for 27 possible switching states of the three phase converter [22]. The presented control algorithm is using 4 current and 3 voltage sensors. If a current observer is used, like discussed in [35], only 2 current sensors need to be used.

Using Clarke transformation the control variables are transformed from time domain components of the three phase abc system to the stationary $\alpha\beta$ reference frame. The propagations for the next sample period are calculated using the discretized system equations:

$$i_{dc1,2}(t) = C_{dc1,2}\frac{dv_{dc1,2}(t)}{dt} \tag{1}$$

$$i_{f\,\alpha\beta}(t) = C_f\frac{dv_{c\,\alpha\beta}(t)}{dt} + i_{o\,\alpha\beta}(t) \tag{2}$$

$$v_{i\,\alpha\beta}(t) = L_f\frac{di_{f\,\alpha\beta}(t)}{dt} + v_{c\,\alpha\beta}(t) \tag{3}$$

Forward Euler method is used to obtain the discrete system equations. The calculated predictions are used in the cost function, which defines the desired behaviour of the converter.

A. Cost function for ANPC configuration

Three objectives will be used in the cost function: output voltage control, NP balancing and switching control of the inner switches:

$$g = (v^*_{c\,\alpha\beta} - v^P_{c\,\alpha\beta})^2 + \lambda_{dc} \cdot g^2_{dc} + \lambda_p \cdot g^2_p \tag{4}$$

$$g_{dc} = v^P_{dc1} - v^P_{dc2} \tag{5}$$

TABLE I: Comparison of thermal stress redistribution methods for multilevel converters

Control method	Space vector control	Carrier based PWM	Model predictive control
Topology	NPC [24], [25]	NPC [26], ANPC [9], T-type [27], Cascaded H-bridge [28]	2L-VSC [29], [30], NPC [22], ANPC [15], [16]
Operation principle	Reduce the dwelling time of zero voltage vectors and the commutations involving the zero voltage level [24], [25]	Semidipolar modulation [26], adaptive modulation [9], relieving switching sequences for the most stressed device [27], clamping the more damaged H-bridge cells [28]	Multi-parameter optimization in the cost function [15], [16], [29], [30], control of the switching frequency [22]
Implementation requirements	Define the stress reliving sequences for all modulation regions [25], the sequences for LVRT depend on heat sink system and devices. Need to be evaluated case by case [24]	Common-mode voltage (CMV) injection [9], find trade-off between the amount of dipolar injection and current quality [26], define stress relief sequences [27], phase displacement angles calculation [28]	Temperature estimation using device model, losses model [15], [16], [30], thermal model and data from reliability experiments [29], design of weighting factors [15], [16], [22], [29], [30]
Limitations	Not applicable for all operating points of the converter (optimized for LVRT scenarios [24] or moderate modulation index operation [25]), higher current distortion	Applicable only for STATCOM [26], higher output harmonics [26], no NP balancing for CMV injection [9], circuity for measurement of thermosensitive el. parameters [27], harmonic distortion at low frequency [28]	Complexity of weighting factor design [15], [29], reliability data is not always available [29], computational burden [15], [29], not suitable for high switching frequency operations [22]

TABLE II: Switching states of the 3L-ANPC converter.

Switching state	S_1	S_2	S_3	S_4	S_5	S_6
P	1	1	0	0	0	1
0^+	1	0	1	0	0	1
0^-	0	1	0	1	1	0
N	0	0	1	1	1	0

TABLE III: System parameters for analysis.

Description	Parameter	Value
DC-link voltage and capacitance	$V_{dc}, C_{dc1,2}$	700 V, 2.8 mF
Output filter parameters	L_f, C_f	2.4 mH, 15 μF
Nominal load and power	$R_{\text{load}}, P_{\text{nom}}$	2.16 Ω, 36.3 kW
Reference voltage	$V^*_{c\,abc}, f^*$	325 V, 50 Hz
Sampling time	T_s	20 μs

$$g_p = \sum_{x=a,b,c} |S_{2x}(k) - S_{2x}(k-1)| + \quad (6)$$
$$|S_{3x}(k) - S_{3x}(k-1)|,$$

where λ_{dc} and λ_p are the weighting factors, $S_x(k-1)$ represents the previous and $S_x(k)$ the current switching state for all converter phase legs $x \in a, b, c$, $v^*_{c\,\alpha\beta}$ is the reference and $v^P_{c\,\alpha\beta}$ the predicted capacitor voltage, v^P_{dc1} and v^P_{dc1} are predicted DC-link capacitor voltages. When λ_p is set to 1, the priority is given to the voltage vectors that will not switch the inner switches very often. In case the situation was opposite and the losses were higher in the outer switches, the switching states S_{1x} and S_{4x} need to be used in the cost function objective g_P instead of S_{2x} and S_{3x}. All steps of the control algorithm are summarized in the flowchart in Fig. 3.

B. Cost function for NPC configuration

In case if one of the active devices of the ANPC module fails, the converter can still continue its operation in an NPC configuration. The change in the topology will also require a modification of the FS-MPC algorithm. Due to the lack of redundant states that can achieve the zero voltage output (NPC topology has only one), the proposed algorithm can not be efficiently applied to the NPC topology. Therefore, in the cost
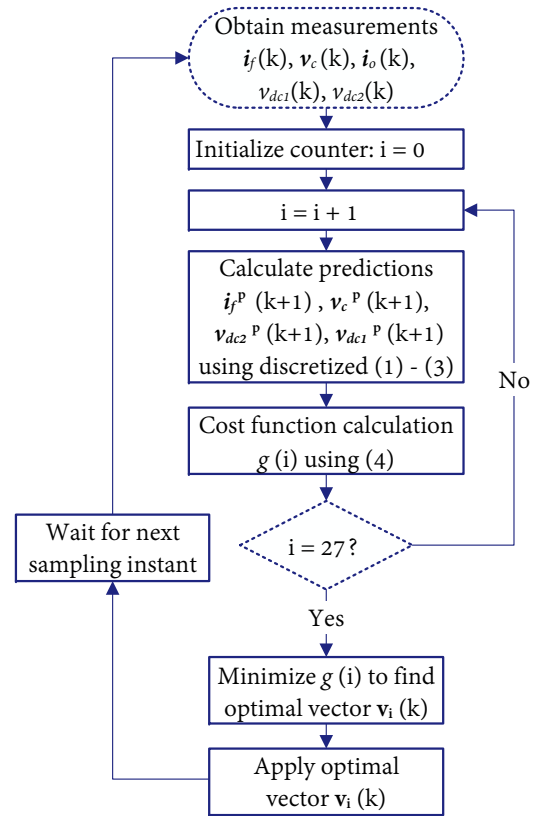

Fig. 3: Flowchart of the used FS-MPC algorithm.

function (4), g_p was replaced with objective (7) for optimized stress distribution in NPC topology, as proposed in [22]:

$$g_t = |I_{fa}(k)| \cdot n_a + |I_{fb}(k)| \cdot n_b + |I_{fc}(k)| \cdot n_c \quad (7)$$
$$n_x = |S_{1x}(k) - S_{1x}(k-1)| + |S_{2x}(k) - S_{2x}(k-1)| \quad (8)$$

where $I_{fx}(k)$ is the measured filter current amplitude for phase $x \in a, b, c$. Compared to the cost function in (4), the switching penalization in (7) is applied for all switches during the interval when the output current amplitude (I_{fx}) is high to reduce the switching losses. The weighting factor for the g_t objective is adjusted to achieve a minimal junction temperature difference between the inner and outer devices. Similar as for

the proposed algorithm, we can notice that (7) does not require thermal measurements. All measurements that are necessary for implementation of the g_t objective are already included.

Presented algorithms could potentially be applied to other modifications of the NPC topology where the unbalanced thermal distribution is limiting the output power of the converter and reducing the converter lifetime. It can not be applied to the topologies without redundant states, as the main principle of the control strategy is to use the redundant states of the converter and reduce the number of switching actions of the most stressed devices. This will lead to a lower junction temperature of these devices.

C. Weighting factor design

The optimum weighting factors can be determined by using the Artificial Neural Networks approach presented in [36]. In the first step simulation model of the ANPC converter system was used to obtain the performance metrics for different combinations of the weighting factors λ_{dc} and λ_p. Similar to [36] the range of the weighting factors was defined as $[0, 1, ..9, 10]$. In total 121 simulations were performed for all possible weighting factor combinations and for each simulation the difference between the DC-link voltages (Δv_{dc}), THD of the load voltage (THD) and the junction temperature difference between the inner and outer device (ΔT_j) were recorded. Afterwards this data was used to train the ANN. Inputs of the ANN are the performance metrics and the outputs are the weighting factors. The trained ANN, can now replace the simulation model and calculate the performance metrics for even higher number of weighting factor combinations in just a few seconds. In the final step, a fitness function (f_{ANN}) was defined using the performance metrics and applied to the data obtained by the ANN.

$$f_{ANN} = THD^2 + \Delta v_{dc}^2 + \Delta T_j^2 \qquad (9)$$

By minimizing this fitness function weighting factors, which provide an optimum trade-off of the performance, will be obtained. This procedure was also repeated for the NPC converter system where the weighting factors λ_{dc} and λ_t were obtained.

V. STEADY STATE OPERATION AND TRANSIENT RESPONSE OF H-ANPC

A. Simulation results

A simulation model of the system presented in Fig. 2 and FS-MPC algorithm explained in the previous section were created in MATLAB Simulink. In Table. IV reference tracking error of filter capacitor voltage and NP balancing error are shown for the proposed cost function and the conventional cost function without the penalization ($\lambda_p = 0$), given the conditions in Table III. Even with the two secondary objectives in the cost function, a good reference tracking performance and NP balancing can be observed for the proposed algorithm. As a consequence of the penalization term, the THD of the load voltage is increased from 0.36% to 0.54% compared to the algorithm with a conventional cost function. One of the requirements for the UPS systems, besides the low voltage
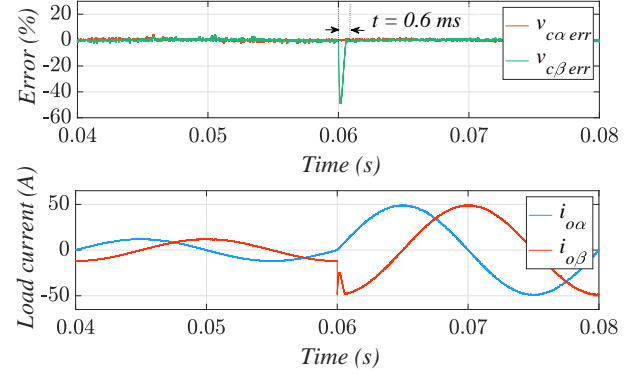

Fig. 4: Transient response of the UPS system to a load change ($P_{\text{load}} = 5.8 \rightarrow 23.9$ kW)

distortion, is also to provide a fast transient response during the load change. In Fig. 4 it can be observed that for the transition from standby load to nominal load using the proposed algorithm, the UPS system requires 0.6 ms to recover the voltage.

B. Experimental results

In Fig. 5 the three phase prototype h-ANPC converter can be seen. The control algorithm is implemented using the MicroLabBox DS1202 PowerPC DualCore 2 GHz processor board and DS1302 I/O board from dSpace. The generated gate signals are then connected to the connector board from which the signals are guided through optic fiber cables to the converter board. To compensate for the computational delay of the FS-MPC algorithm the predictions were calculated one step further ahead and applied at the beginning of the next time sampling interval as proposed in [34]. It was not possible to use the nominal current values in the experiments due to the set-up limitations (PCB design, DC-supply capacity, protection), therefore the testing was done for the $I_o = 30$ A and $V_{dc} = 260$ V. For SiC devices, CRD-001 gate drivers from Cree are embedded to the power board, while the Si devices use the ACPL-330J drivers from Avago. The commutation loops are reduced through layout optimization. Furthermore, film capacitors are added to reduce the dc-link stray inductance.

Experimental waveforms of the load currents and the DC-link voltages can be seen in Fig. 6. It can be noticed that the algorithm can keep a good balance of the DC-link voltages.

VI. LOSS DISTRIBUTION AND DEVICE JUNCTION TEMPERATURE COMPARISON

A. Simulation results

The thermal modelling of the devices was done in PLECS Blockset using the manufacturer datasheets that are comparable to the devices used in module [37], [38]. The losses are calculated in PLECS by using a look-up table. The look-up table is fed with the information about conduction and switching losses from the device datasheets. In Table III the system parameters used for simulations to analyse the device stress under nominal conditions are presented. The weighting factors in the cost function (4) were set to $\lambda_{dc} = 5$ and $\lambda_p = 1$ and in cost function (7) $\lambda_t = 0.06$. The heatsink thermal

TABLE IV: Performance comparison of the proposed FS-MPC algorithm and conventional FS-MPC for hANPC converter.

Weighting factor	$v_{c\,max\,err}$	$v_{c\,mean\,err}$	$v_{dc\,max\,err}$	$v_{dc\,mean\,err}$	THD_{v_c}	$f_{sw\,avg}$	$T_{j1} - T_{j2}$	Efficiency
$\lambda_p = 0$	2.24%	0.45%	0.29%	0.08%	0.36%	5.8 kHz	5 °C	0.983
$\lambda_p = 1$	2.4%	0.5%	0.32%	0.1%	0.54%	5.6 kHz	1.5 °C	0.984
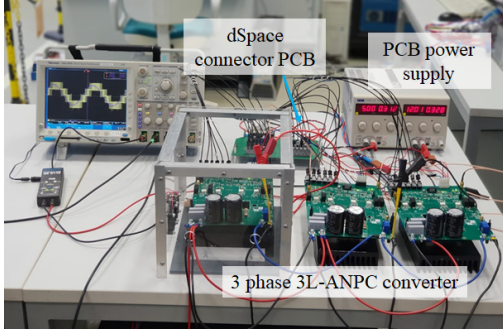
(a) Operation of the hybrid ANPC prototype.
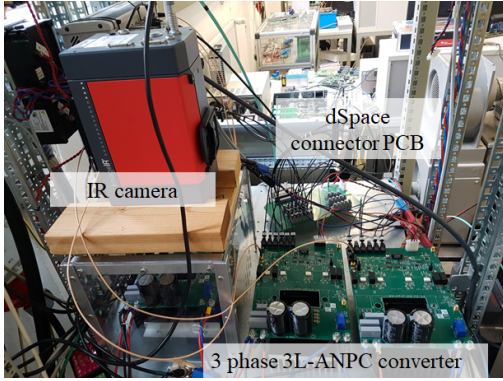
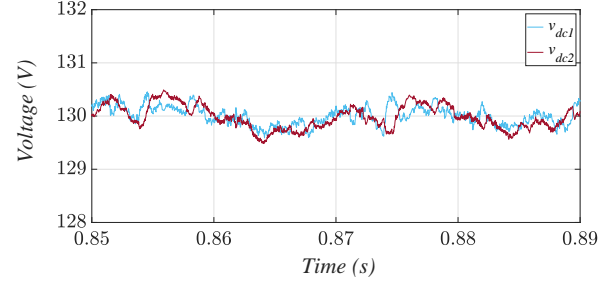(b) Measurement of the device temperatures using the IR camera.

Fig. 5: Three phase 3-level hybrid ANPC experimental set-up.

(a) DC-link voltages $v_{dc\,1,2}$.

(b) Phase load currents $i_{o\,abc}$ (10 A/div).

Fig. 6: Experimental waveforms obtained from the ANPC converter prototype at $P = 4$ kW ($V_{dc} = 260$ V, $I_o = 28$ A, $V_c = 95$ V).

resistance was set to 0.23 K/W. A benchmark model using the algorithm with phase disposition of the carriers presented in [19] was used for comparison. Both the h-NPC and NPC converter will also be included in the analysis. Due to the lack of modulator in the FS-MPC algorithm, the switching frequency of the converter is variable, therefore only the average switching frequency per device can be calculated:
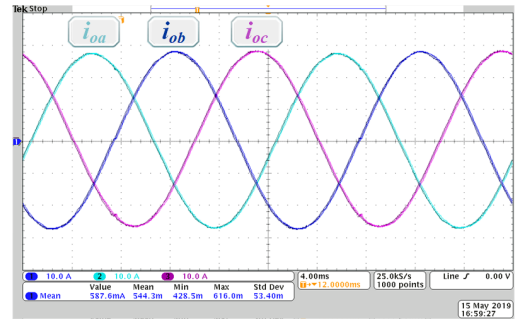
$$f_{\mathrm{sw}_{avg}} = \sum_{i=1}^{m} \frac{f_{\mathrm{sw}_{ai}} + f_{\mathrm{sw}_{bi}} + f_{\mathrm{sw}_{ci}}}{3} \quad (10)$$

where m is the number of switches in the converter. In this paper the switching frequency of the benchmark algorithm was set to the switching frequency at which the total losses of the benchmark control strategy are comparable to the losses produced by the proposed FS-MPC algorithm. In this way the distribution of losses and the junction temperatures of the devices can be kept in focus.

1) ANPC converter: In Fig. 7a the loss distribution in an h-ANPC converter for the proposed FS-MPC algorithm are compared to the benchmark algorithm from [19], which is switching with the switching frequency equivalent to the

average switching frequency of the proposed algorithm (5.6 kHz). The total losses for the nominal output power of 36.5 kW for FS-MPC algorithm are 590 W ($\eta = 0.984$) and for the benchmark algorithm the losses are 610 W ($\eta = 0.983$). Although the efficiency is almost the same, the difference between the two algorithms can be noticed in the device loss distribution. It can be observed that for the benchmark algorithm, the only device producing the switching losses is the inner MOSFET. On contrary, for the proposed algorithm the switching losses for FS-MPC algorithm are spread over all devices. This difference can be explained by the fact that the switching sequence of the benchmark algorithm is fixed and it is always following the pattern from Table II, whereas FS-MPC is evaluating in every sample step where it is possible to avoid switching of the devices without significantly degrading the reference tracking performance and NP balance. In order to maintain the NP balance, a higher utilization of the clamping switches is expected. All of this is also mirrored into the T_{jm} of the devices, which are more balanced for the proposed algorithm like shown in Fig. 7b and Fig. 7c. Lower and balanced device temperatures can increase both the lifetime of the converter, as demonstrated in sequence, and the maximum power output or reduce the size of the heatsink.
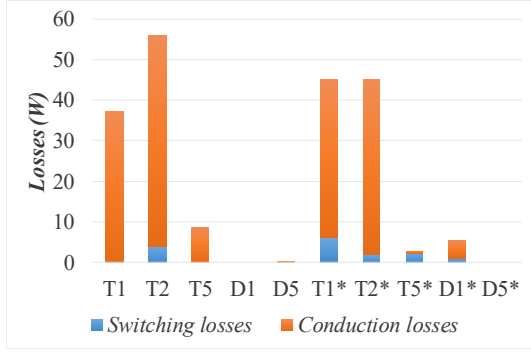
(a) Device losses distribution.
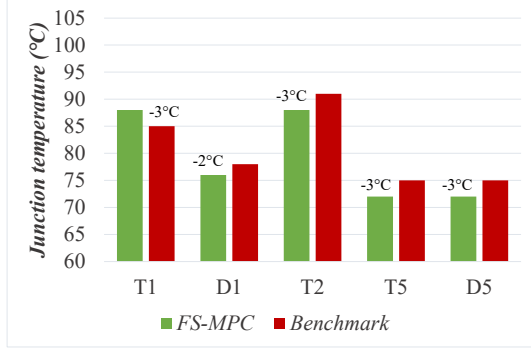
(b) Device mean junction temperatures.
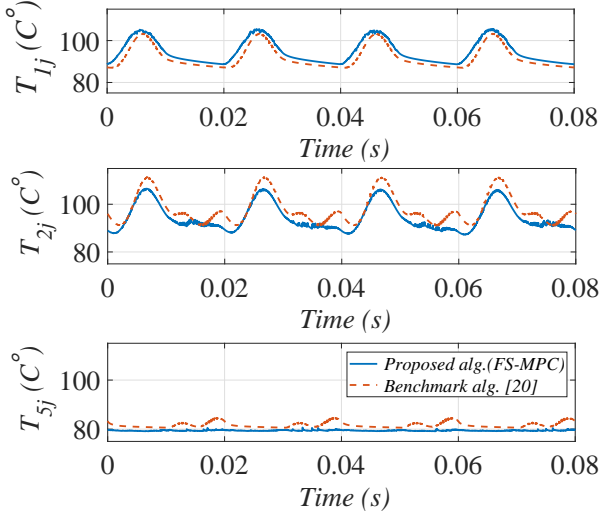
(c) Device junction temperatures cycles.

Fig. 7: Simulation results for one phase module in a h-ANPC configuration for the proposed FS-MPC (*) and the benchmark algorithm used in [19].

It also needs to be mentioned that the benchmark algorithm needs an additional control loop to maintain the NP balance, while in the FS-MPC algorithm this is already included in one control loop. This would have an impact on the transients as the FS-MPC controller will have a faster response than in the benchmark model [34].

2) NPC converter: Using the Simulink model, simulations were performed for the hybrid NPC and full Si NPC converter using the FS-MPC algorithm with the cost function (7). The

simulations were also repeated for the carrier based benchmark algorithm from [23]. The switching frequency of the benchmark was set to 5 kHz, which is equal to calculated average switching frequency of the FS-MPC algorithm applied to NPC converter. The loss distributions are shown in Fig. 8a for h-NPC converter and in Fig. 9a for NPC converter, respectively. For both topologies it can be observed that the losses are lower if FS-MPC algorithm is utilized. Moreover, the switching losses of the inner device are reduced. In Fig. 8b and Fig. 9b the junction temperatures can be observed. Due to the loss reduction, lower junction temperatures of all active power devices are observed. Moreover, by comparing the junction temperatures for the benchmark algorithm in the two topologies, it is noticed that the replacement of the inner device with the SiC MOSFET's helped in achieving a balanced junction temperature for the benchmark algorithm in Fig. 8b. It can also be observed that the device junction temperatures are higher for NPC converter than for h-ANPC converter. Thus, if the same heatsink is used afterwards for NPC converter operation, the heatsink design should be adapted for the worst case scenario.

B. Experimental results

For the measurements of the device temperatures a high resolution Ifratec ImageIR 8300 camera (temperature resolution better than 0.02 K and accuracy of measurement ±1°C) was used [39]. The measurements are first obtained for the h-ANPC converter. Afterwards, the gate signals for the clamping switches were disabled to simulate a scenario where the converter continues its operation as an h-NPC converter.

1) Hybrid ANPC converter: In Fig. 10 a snapshot from the IR camera can be seen for the proposed algorithm and the benchmark algorithm. In order for the device temperatures to reach steady state, the IR snapshot was first performed after 10 minutes of the converter operation. Before the next experiment was conducted the devices were allowed to cool down to the initial temperature of 25°C. The temperatures of the outer device T_4 and inner device T_3 are very good balanced for both control strategies as seen in Table V.

2) Hybrid NPC converter: Obtained junction temperature measurements can be observed in Table V. Due to the difference in the topology (ANPC topology has more redundant states) and the cost function, the switching frequency of the devices is also different. While in case of h-NPC the average switching frequency is 2.6 kHz, the switching frequency for h-ANPC with the proposed cost function is 5.8 kHz. Thus, the focus is not placed on the absolute junction temperatures but more on the device thermal stress balancing. For a comparison the junction temperature measurements on the h-NPC were also taken for a conventional FS-MPC cost function that only has two objectives: voltage tracking and neutral point balancing i.e in equation (4) the weighting factor λ_t is set to 0. The junction temperature measurements showed that inclusion of g_t can reduce the junction temperatures of the devices. In [22] it was shown that for the NPC topology with Si devices, a good balance of the inner and outer switch junction temperatures can be achieved, in the experiment for the hybrid topology the difference was still present but reduced for 1°C.
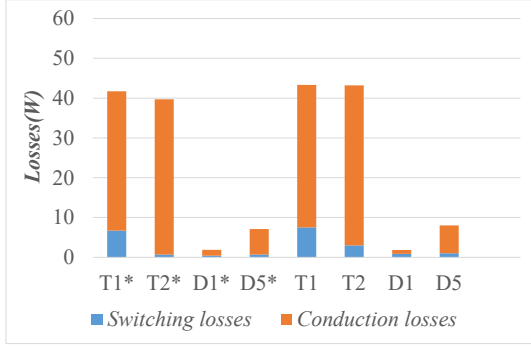
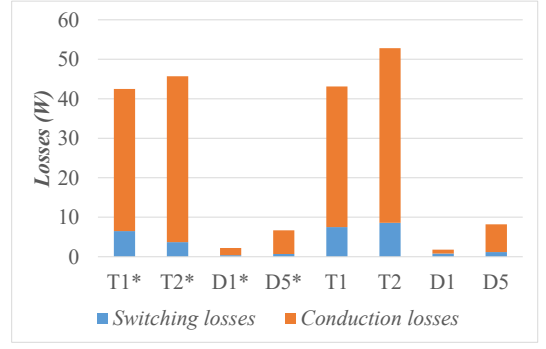(a) Device losses distribution.
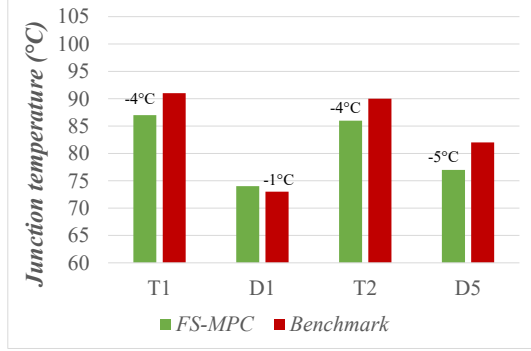
(b) Device mean junction temperatures.
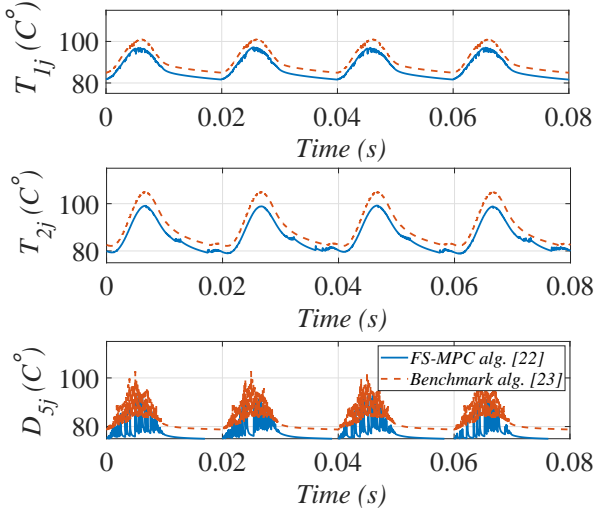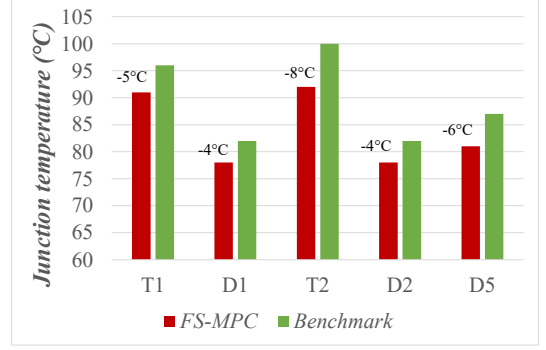

(c) Device junction temperatures cycles.

Fig. 8: Simulation results for one phase module of a h-NPC converter using FS-MPC(*) with the cost function (7) and the benchmark algorithm [23].

(a) Device losses distribution.

(b) Device mean junction temperatures.

(c) Device junction temperatures cycles.

Fig. 9: Simulation results for one phase module of a NPC converter using FS-MPC(*) with the cost function (7) and the benchmark algorithm [23].
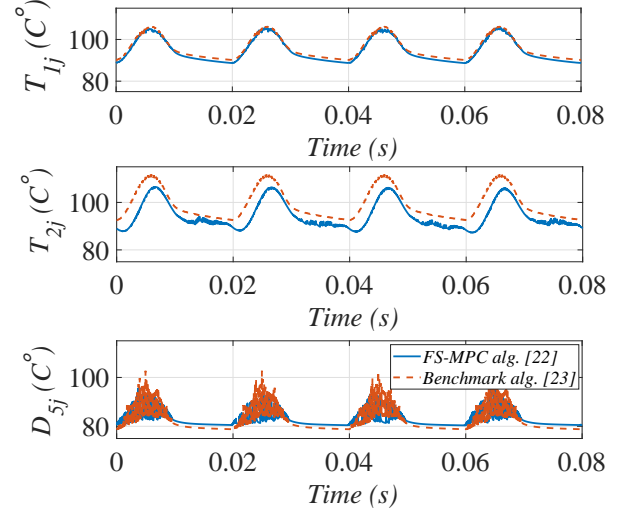
VII. RELIABILITY IMPACT OF THE PROPOSED FS-MPC

The NPC converters and the FS-MPC control algorithms introduced in Section IV will be used to estimate the reliability of the converter in an UPS application. The reliability analysis will be focused on the semiconductor devices to show the impact of the control algorithm on the expected lifetime of the devices. For a comparison, the reliability analysis is also repeated with the carrier based benchmark algorithms.

A. Mission profile and thermal stress analysis

In Fig. 11a repetitive daily load mission profile for the UPS application is presented [40]. It is characterized by long intervals of standby load and short intervals of very high load. In the analysis, a yearly ambient temperature (T_a) profile like shown in Fig. 11b was used.

The thermal resistance of the converter heatsink was designed to keep the device junction temperatures in h-ANPC converter below $130°C$ during the maximum load current of
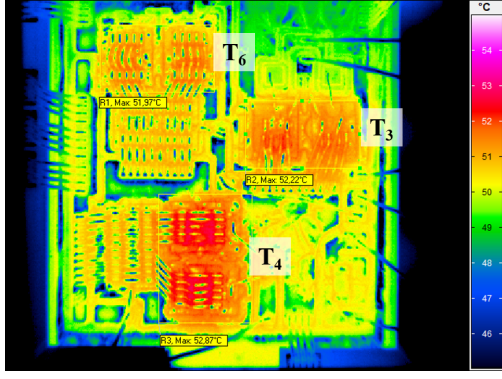
(a) Proposed FS-MPC algorithm (T_6 = 51.97°C, T_3 = 52.22°C, T_4 = 52.87°C).
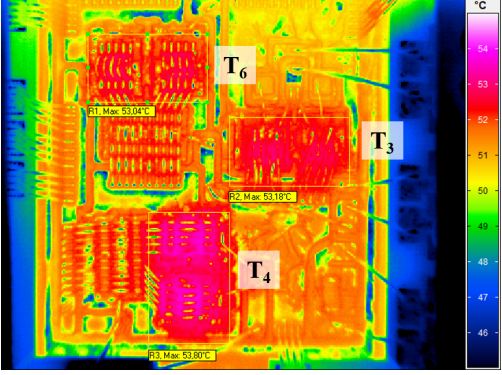
(b) Benchmark algorithm (T_6 = 53.04°C, T_3 = 53.18°C, T_4 = 53.80°C).

Fig. 10: IR snapshot of the one phase ANPC open module during operation at P = 4 kW.

TABLE V: Measured junction temperatures of most stressed devices in h-ANPC and h-NPC converter (P = 4 kW).

Topology	Control	T_4	T_3	T_6	D_6
h-ANPC	Proposed FS-MPC	52.9°C	52.2°C	52.0°C	-
h-ANPC	Benchmark PWM [19]	53.8°C	53.2°C	53.0°C	-
h-NPC	Conventional FS-MPC	57.6°C	54.6°C	-	56.2°C
h-NPC	FS-MPC [22]	50.9°C	48.8°C	-	50.5°C

the converter. Using the electro-thermal model of the converter system, the junction temperature profiles of the semiconductor devices shown in Fig. 12 were obtained. The figure also shows that the temperature difference between the inner and outer device is kept within 1.5°C during the whole mission profile. The obtained temperature profile is used to analyse the accumulated damage of the devices. Two types of temperature cycling that cause the degradation of the devices are analysed: fundamental frequency (FF) cycling and the low frequency (LF) cycling. For the analysis of the low frequency cycles a Rainflow counting algorithm has been applied [41]. After applying the rainflow algorithm, the cycles that were longer than the maximum t_{on} of the lifetime model were removed

from the damage calculation. The information about the cycles (minimum junction temperature ($T_{j\,\min}$), temperature swing (ΔT_j), pulse duration t_{on}) and device parameters (current per bond wire (I_B), bond wire diameter (D), voltage class (V_c)) were afterwards used in an empirical lifetime model (11) to calculate the (LC) consumed device lifetime using the Miner rule (12) [42], [43]:

$$N_f = A \cdot \Delta T_j^{\beta_1} exp\left(\frac{\beta_2}{(T_{j,\min} + 273)}\right) \cdot t_{on}^{\beta_3} \cdot I_B^{\beta_4} \cdot V_C^{\beta_5} \cdot D^{\beta_6}$$
(11)

$$LC = \sum_i \frac{n_i}{N_{fi}}$$
(12)

The empirical lifetime model (11) calculates the lifetime of the bond wires of Si IGBTs [42]. For SiC devices four different failure modes are explained in [43] but at the moment, there are no lifetime models, which would take them all into account. In some references Si device lifetime models were applied to estimate the SiC device lifetime [43], [44]. However, recently published SiC power cycling results indicate that the lifetime for SiC is overestimated by those models [45], [46]. Unfortunately, it is not known how the lifetime ratio is in normal operating conditions, where the ΔT_j are up to 30 K. It is important to stress, that due to this uncertainty, the absolute lifetimes of different topologies can not be compared. Awareness is on the lifetime model limitations and the specific parameter range, which was obtained like high ΔT_j and long t_{on}. Preliminary Si device power cycling results were published for low ΔT_j and short t_{on} in [47], [48] and they showed that the number of cycles to failure are underestimated by using (11), also the cycles with low ΔT_j may cause elastic deformation, which is reversible in the power devices. The authors of [48] stress that further work is still required to obtain a lifetime model for low ΔT_j. Thus, until a new lifetime model is provided that can accurately capture the device wear-out at low ΔT_j, the focus is on the relative improvement of the lifetime that the FS-MPC control can provide, rather than absolute lifetime values.

As explained in [49] the variances of the semiconductor device parameters and the lifetime model need to be included in the reliability analysis. For parameter fitting coefficients (β_1 and β_2), the variance intervals are given in [42]. To simplify the analysis, the yearly dynamic mission profile was converted to an equivalent static one. The parameters of the static profile for the FF and LF cycles with the proposed control algorithm are presented in Table VI for the switches.

B. System reliability

In the next step for the obtained static thermal cycle parameters the variance of 5% with normal distribution was defined as suggested in [49]. This variance is taking into account the uncertainty that originates in the variance of the device manufacturing process. Using a population of 10 000 devices, Monte Carlo simulations were used to obtain the end-of-life cumulative distribution functions (cdf). This workflow is also illustrated in Fig. 13. After obtaining the cdf functions for all
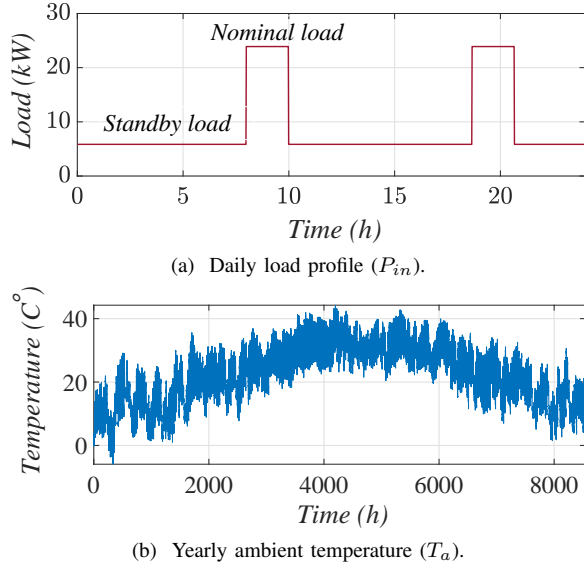
(a) Daily load profile (P_{in}).

(b) Yearly ambient temperature (T_a).

Fig. 11: Mission profiles used in lifetime estimation of the NPC converters for the UPS application.

(a) Mean junction temperatures of the devices.

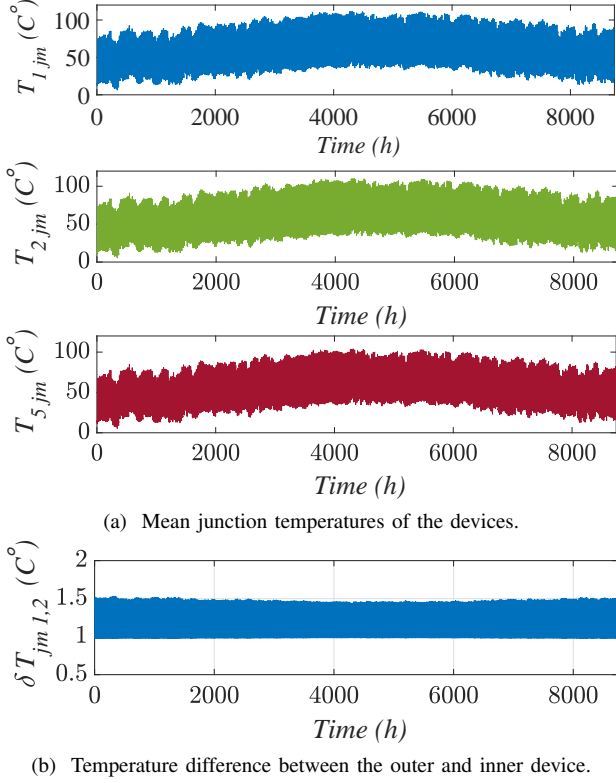(b) Temperature difference between the outer and inner device.

Fig. 12: Junction temperatures of the h-ANPC devices for the proposed algorithm during mission profiles from Fig. 11.

three devices ($F_{T_1}(x), F_{T_2}(x), F_{T_5}(x)$), the converter system unreliability was obtained using the following equation:

$$F_{sys}(x) = 1 - (1 - F_{T_1}(x))^6 (1 - F_{T_2}(x))^6 (1 - F_{T_5}(x))^6 \quad (13)$$

In this equation it is assumed that: 1) the ANPC system has failed if one of the 18 devices fails (i.e. we assume a series connection of all devices in the reliability block diagram), 2) the loading conditions in each phase are equivalent and 3) the
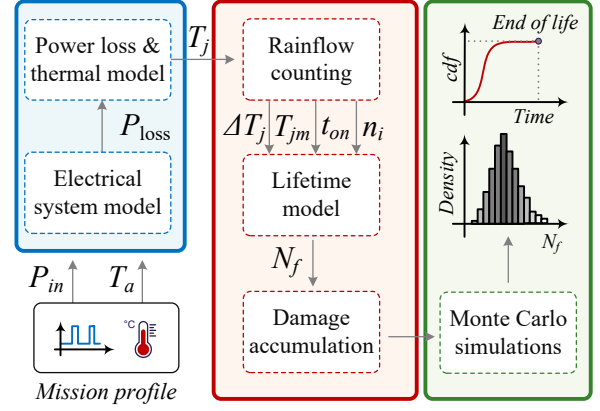

Fig. 13: Mission profile based lifetime estimation of power electronic converters.

thermal stress of the devices in the module is equivalent to the devices in the bottom half. Hence, for a 3 phase system where in each phase there are three pairs of devices with the equivalent thermal stress, the *cdf* functions for all three devices can be raised to the power of 6 in the F_{sys}. Due to unidirectional power flow, the diodes in the ANPC topology are not experiencing a high thermal loading like the active switches. Therefore, in the analysis only the active devices (T_1, T_2, T_5), which significantly contribute to the lifetime consumptions of the ANPC converter are included. One of the commonly used metrics in the lifetime analysis are the B_x lifetimes i.e. the time when $x\%$ of the device population have failed. For the UPS system a high reliability is one of the priorities in the design, thus in this study B_1 and B_{10} are shown to compare the designs.

1) Hybrid ANPC converter: For the h-ANPC converter the unreliability functions for the devices are shown in Fig. 14 for FS-MPC algorithm from Section IV-A and the carrier based algorithm [19]. If the benchmark algorithm is used, the device with a higher failure probability is the inner SiC device. However, if the proposed algorithm is used in this application, the B_1 of the inner SiC devices is much higher than for the conventional algorithm. On a converter level shown in Fig. 15, if all devices are considered the expected B_1 for both control strategies is 13 years, meaning that 1% of the converters will fail in 13 years. This is a rather conservative approach since the B_{10} lifetime (10% failed converters) is commonly used [50]. However, it should be stressed that the h-ANPC with the conventional algorithm will require separate DC-link sources due to the missing NP balancing control.

2) NPC converter: The lifetime analysis were also conducted for the hybrid and Si-NPC converter configuration. Unreliability functions for the h-NPC converter and the Si-NPC in Fig. 15 were obtained for the FS-MPC algorithm from Section IV-B and a carrier based algorithm proposed in [23]. Both converter configurations show a higher B_1 and B_{10} lifetimes for the FS-MPC based algorithm. The B_1 and B_{10} lifetimes for all configurations and control algorithms are summarized in the Table VII. In conclusion, for both NPC configurations the application of the FS-MPC algorithm can provide a good utilization of the devices. To improve

TABLE VI: Equivalent static parameters used in Monte Carlo simulations for the two cycling types (FF: fundamental frequency , LF: low frequency).

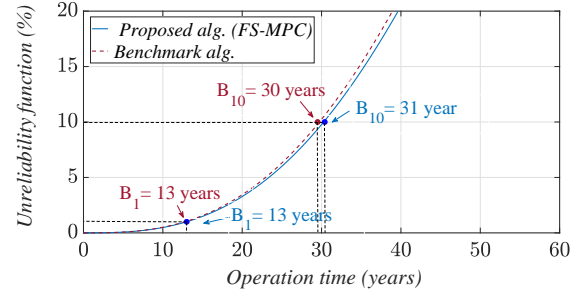| Par.	T_1		T_2		T_5	
	FF	LF	FF	LF	FF	LF
$T_{j\,\min}$	43.1°C	43.1°C	42.4°C	42.4°C	41.8°C	41.8°C
ΔT_j	6.4°C	21.4°C	5.3°C	21.2°C	0.9°C	19.2°C
LC	0.0074	0.0032	0.0033	0.0031	$1\cdot10^{-6}$	0.0019
N_f	$2.2\cdot10^{11}$	$1.9\cdot10^{7}$	$4.8\cdot10^{11}$	$1.9\cdot10^{7}$	$1.6\cdot10^{15}$	$3.1\cdot10^{7}$
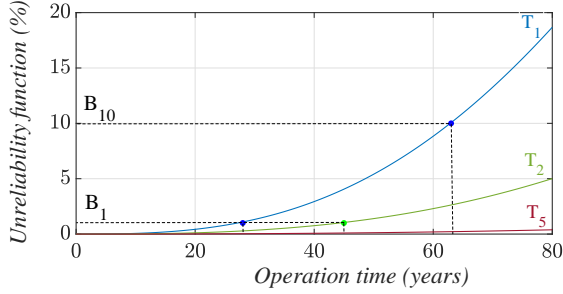
(a) Proposed FS-MPC.
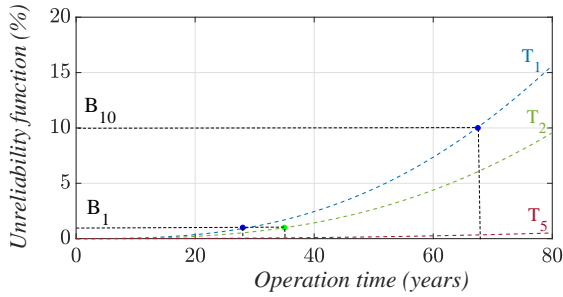
(b) Benchmark algorithm.

Fig. 14: Device unreliability functions of a h-ANPC converter for two control algorithms.

(a) h-ANPC converter.

(b) h-NPC converter.

(c) NPC converter.

Fig. 15: System unreliability functions for different converter configurations and control algorithms for the mission profile in Fig.11.

TABLE VII: System B_{10} and B_1 lifetime estimations for different control algorithms and converter configurations.

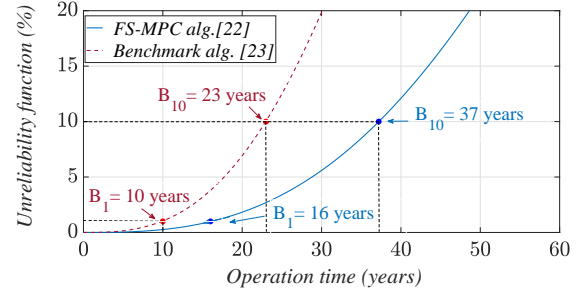| Control algorithm	Configuration	B_{10}	ΔB_{10}	B_1	ΔB_1
Proposed FS-MPC	h-ANPC	31 years	3%	13 years	0 %
Benchmark algorithm	h-ANPC	30 years		13 years	
FS-MPC [22]	h-NPC	37 years	60%	16 years	60%
Carrier based PWM [23]	h-NPC	23 years		10 years	
FS-MPC [22]	NPC	28 years	100%	12 years	100%
Carrier based PWM [23]	NPC	14 years		6 years	

the expected lifetime for the Si-NPC with the carrier based algorithm in this particular UPS application, a redesign of the heatsink or operation at lower switching frequency should be considered. Another alternative that could be considered in the UPS application is the T-type NPC converter solution, which is using SiC diodes and CoolMOS switches like shown in [51].
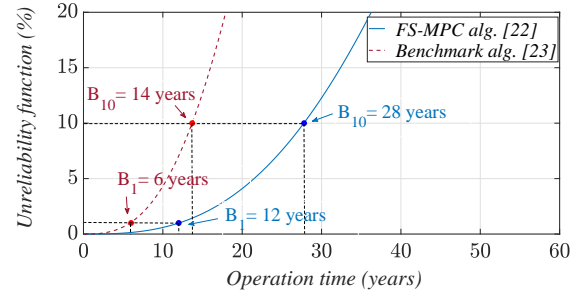
VIII. CONCLUSION

FS-MPC algorithms are presented to balance the temperatures in neutral point clamped converters. This is achieved by penalizing the switching combinations that add more switching stress to the high stressed switches in the cost function. As a consequence, the thermal stress will be more uniformly distributed among the switches. Simulation results for the nominal converter power showed that the proposed algorithm can provide a balanced stress distribution and good reference tracking performance for pure Si and hybrid converters. Furthermore, maximum junction temperature of the power devices was reduced for 3°C compared to the conventional carrier based algorithm. For the h-NPC converter, the junction

temperatures of all active power devices were reduced for 4°C compared to the conventional carrier based algorithm. It was also shown that the proposed algorithm can maintain the DC-link voltages in good balance with voltage deviation below 0.5 V. An improvement compared to the conventional carrier based algorithm is also seen in the clamping device temperature,

which had a lower temperature difference to the outer device than when using the conventional algorithm.

A mission-profile based lifetime estimation for the proposed algorithm on an UPS mission profile showed, that the h-ANPC converter and h-NPC converter can provide a high reliability power supply in the application. Compared to a conventional carrier based algorithm, the use of FS-MPC based thermal stress algorithm can increase the B_1 lifetime of the converter for up to 60% for the h-NPC and up to 100% for the Si-NPC, respectively.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl*, vol. 17, no. 5, pp. 518–523, Sep. 1981.

[2] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active NPC switches," in *Proc. of Annual Power Electron. Specialists Conf.*, vol. 2, pp. 1135–1140 vol.2, 2001.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[4] U. M. Choi and F. Blaabjerg, "Asymmetric power device rating selection for even temperature distribution in NPC inverter," in *Proc. of IEEE Energy Conversion Congress and Expo. (ECCE)*, pp. 4196–4201, Oct. 2017.

[5] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, DOI 10.1109/TIE.2005.847586, no. 3, pp. 855–868, Jun. 2005.

[6] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg, and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," in *Proc. of Southern Power Electron. Conf. (SPEC)*, DOI 10.1109/SPEC.2016.7846157, pp. 1–6, Dec. 2016.

[7] D. Floricau, E. Floricau, and G. Gateau, "Three-level active NPC converter: PWM strategies and loss distribution," in *Proc. of 34th Annual Conf. of IEEE Ind. Electron.*, DOI 10.1109/IECON.2008.4758494, pp. 3333–3338, 2008.

[8] X. Jing, J. He, and N. A. O. Demerdash, "Loss balancing SVPWM for active NPC converters," in *Proc. of APEC*, DOI 10.1109/APEC.2014.6803322, pp. 281–288, 2014.

[9] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, DOI 10.1109/TPEL.2016.2573823, no. 4, pp. 2521–2532, Apr. 2017.

[10] L. Ma, T. Kerekes, P. Rodriguez, X. Jin, R. Teodorescu, and M. Liserre, "A new PWM strategy for grid-connected half-bridge active NPC converters with losses distribution balancing mechanism," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2014.2387152, no. 9, pp. 5331–5340, 2015.

[11] Y. Jiao and F. C. Lee, "New modulation scheme for three-level active neutral-point-clamped converter with loss and stress reduction," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2015.2405505, no. 9, pp. 5468–5479, 2015.

[12] L. Caballero, S. Busquets-Monge, and S. Rates, "A novel commutation sequence for the three-level active neutral-point-clamped inverter to aid in splitting switching and conduction losses among the semiconductor devices," in *Proc. of EPE'16 ECCE Europe*, DOI 10.1109/EPE.2016.7695345, pp. 1–10, 2016.

[13] D. Andler, M. Perez, J. Rodriguez, and S. Bernee, "Predictive control of three-level active NPC converter with evenly energy losses distribution," in *Proc. of Int. Power Electron. Conf.(ECCE ASIA)*, DOI 10.1109/IPEC.2010.5544610, pp. 754–759, Jun. 2010.

[14] D. Andler, J. Weber, S. Bernet, and J. Rodriguez, "Improved model predictive control with loss energy awareness of a 3L-ANPC voltage source converter," in *Proc. of Int. Conf. on Applied Electron.*, pp. 1–6, Sep. 2010.

[15] D. Andler, E. Hauk, R. Alvarez, J. Weber, S. Bernet, and J. Rodriguez, "New junction temperature balancing method for a three level active NPC converter," in *Proc. of European Conf. on Power Electron. and Appl.(EPE)*, pp. 1–9, Aug. 2011.

[16] U. Rauf, M. Schutt, and H. Eckel, "Model predictive control for space vector modulation of a three-level ANPC inverter for efficient loss distribution and neutral point balancing," in *Proc. of EPE '19 ECCE Europe*, DOI 10.23919/EPE.2019.8915514, pp. P.1–P.10, 2019.

[17] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparison and implementation of a 3-level NPC voltage link back-to-back converter with SiC and Si diodes," in *Proc. of Applied Power Electron. Conf. and Expo. (APEC)*, DOI 10.1109/APEC.2010.5433434, pp. 1527–1533, Feb. 2010.

[18] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high efficiency high power density SiC+Si hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems," in *Proc. of Energy Conversion Congress and Expo.(ECCE)*, DOI 10.1109/ECCE.2018.8558199, pp. 806–813, Sep. 2018.

[19] Q. Guan et. al, "An extremely high efficient three-level active neutral-point-clamped converter comprising SiC and Si hybrid power stages," *IEEE Trans. Power Electron.*, vol. 33, DOI 10.1109/TPEL.2017.2784821, no. 10, pp. 8341–8352, Oct. 2018.

[20] L. Zhang, X. Lou, C. Li, F. Wu, Y. Gu, G. Chen, and D. Xu, "Evaluation of different Si/SiC hybrid three-level active NPC inverters for high power density," *IEEE Trans. Power Electron.*, vol. 35, DOI 10.1109/TPEL.2019.2962907, no. 8, pp. 8224–8236, 2020.

[21] M. Novak, V. N. Ferreira, M. Andresen, T. Dragicevic, F. Blaabjerg, and M. Liserre, "FS-MPC algorithm for optimized operation of a hybrid active neutral point clamped converter," in *Proc. of Energy Conversion Congress and Expo. (ECCE)*, pp. 1447–1453, 2019.

[22] M. Novak, T. Dragicevic, and F. Blaabjerg, "Finite set MPC algorithm for achieving thermal redistribution in a neutral-point-clamped converter," in *Proc. of Annual Conf. of the IEEE Ind. Electron. Society*, pp. 5290–5296, Oct. 2018.

[23] J. Pou et. al, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2288–2294, 2007.

[24] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point-clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014.

[25] K. Ma and F. Blaabjerg, "Modulation methods for three-level neutral-point-clamped inverter achieving stress redistribution under moderate modulation index," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 5–10, Jan. 2016.

[26] J. Zhou and P. Cheng, "Modulation methods for 3L-NPC converter power loss management in STATCOM application," *IEEE Trans. Ind. Appl*, vol. 55, DOI 10.1109/TIA.2019.2924407, no. 5, pp. 4965–4973, Sep. 2019.

[27] M. Aly, E. M. Ahmed, and M. Shoyama, "Thermal stresses relief carrier-based PWM strategy for single-phase multilevel inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9376–9388, Dec. 2017.

[28] V. G. Monopoli, A. Marquez, J. I. Leon, Y. Ko, G. Buticchi, and M. Liserre, "Improved harmonic performance of cascaded h-bridge converters with thermal control," *IEEE Trans. Ind. Electron.*, vol. 66, DOI 10.1109/TIE.2018.2868304, no. 7, pp. 4982–4991, Jul. 2019.

[29] J. Falck, G. Buticchi, and M. Liserre, "Thermal stress based model predictive control of electric drives," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1513–1522, Mar. 2018.

[30] L. Wang, J. He, T. Han, and T. Zhao, "Finite control set model predictive control with secondary problem formulation for power loss and thermal stress reductions," *IEEE Trans. Ind. Appl.*, vol. 56, DOI 10.1109/TIA.2020.2991646, no. 4, pp. 4028–4039, 2020.

[31] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, DOI 10.1109/TPEL.2017.2665697, no. 1, pp. 765–776, Jan. 2018.

[32] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7434–7450, 2020.

[33] M. Novak, V. Sunde, N. Cobanov, and Z. Jakopovic, "Semiconductor loss distribution evaluation for three level ANPC converter using different modulation strategies," in *Proc. of Int. Conf. on Electrical Drives and Power Electron.(EDPE)*, DOI 10.1109/EDPE.2017.8123275, pp. 170–177, Oct. 2017.

[34] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*, ser. Wiley - IEEE. Wiley, 2012.

[35] P. Cortes, G. Ortiz, J. I. Yuz, J. Rodriguez, S. Vazquez, and L. G. Franquelo, "Model predictive control of an inverter with output LC filter for ups applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1875–1883, 2009.

[36] T. Dragicevic and M. Novak, "Weighting factor design in model predictive control of power electronic converters: An artificial neural network approach," *IEEE Trans. Ind. Electron.*, vol. 66, DOI 10.1109/TIE.2018.2875660, no. 11, pp. 8870–8880, Nov. 2019.

[37] *SCT3022AL: N-channel SiC power MOSFET (datasheet)*, Rohm, 2018, rev. 1.0.

[38] *IKW75N65EL5: IGBT TRENCHSTOP 5 technology with RAPID 1 fast and soft antiparallel diode (datasheet)*, Infineon, 2014, rev. 2.1.

[39] Ifratec ImageIR 8300 specifications. (2019). [Online]. Available: https://www.infratec.eu/thermography/infrared-camera/imageir-8300/

[40] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of DC/DC converters for a backup power application," *IEEE Trans. Power Electron.*, vol. 33, DOI 10.1109/TPEL.2017.2769161, no. 9, pp. 8030–8039, Sep. 2018.

[41] I. Rychlik, "A new definition of the rainflow cycle counting method," *International Journal of Fatigue*, vol. 9, no. 2, pp. 119 – 121, 1987.

[42] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules - various factors influencing lifetime," in *Proc. of CIPS*, pp. 1–6, 2008.

[43] Z. Ni et al., "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, 2020.

[44] L. Ceccarelli, R. M. Kotecha, A. S. Bahman, F. Iannuzzo, and H. A. Mantooth, "Mission-profile-based lifetime prediction for a sic mosfet power module using a multi-step condition-mapping simulation strategy," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9698–9708, 2019.

[45] F. Hoffmann and N. Kaminski, "Power cycling capability and lifetime estimation of discrete silicon carbide power devices," in *Silicon Carbide and Related Materials 2019*, ser. Materials Science Forum, vol. 1004, pp. 977–984. Trans Tech Publications Ltd, 8 2020.

[46] B. Hu et al., "Failure and reliability analysis of a sic power module based on stress comparison to a si device," *IEEE Trans. Device and Materials Reliability*, vol. 17, no. 4, pp. 727–737, 2017.

[47] G. Zeng, R. Alvarez, C. Kunzel, and J. Lutz, "Power cycling results of high power igbt modules close to 50 hz heating process," in *Proc. of EPE '19 ECCE Europe*, pp. 1–10, 2019.

[48] J. Lutz, C. Schwabe, G. Zeng, and L. Hein, "Validity of power cycling lifetime models for modules and extension to low temperature swings," in *Proc. of EPE '20 ECCE Europe 2020*, pp. 1–9, 2020.

[49] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171–7182, 2016.

[50] J. Berner, "Load-cycling capability of hipak igbt modules," in *ABB Application Note 5SYA 2043-02*, pp. 1–8, 2012.

[51] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level t-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, 2013.