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Multiple Modulation Strategy of Flying Capacitor DC/DC Converter

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Abstract: Flying-capacitor multiplexed modulation technology is suitable for bipolar DC microgrids with higher voltage levels and higher current levels. The module combination and corresponding modulation method can be flexibly selected according to the voltage level and capacity level. This paper proposes a bipolar bidirectional DC/DC converter and its interleaved-complementary modulation strategy that is suitable for bipolar DC microgrids. The converter consists of two flying-capacitor three-level bidirectional DC/DC converters that are interleaved in parallel 90°, and then cascaded with another module to form a symmetrical structure of the upper and lower arms; the complementary modulation of the upper and lower half bridges constitutes an interleaved complementary multilevel bidirectional DC/DC converter. If the bidirectional converter needs to provide a stronger overcurrent capability, more bridge arms can be interleaved in parallel. Once n bridge arms are connected in parallel, the bridge arms should be interleaved 180°/n in parallel. In bipolar DC microgrids, the upper and lower arms should be complementarily modulated, and the input and output are isolated by the inductance. To solve the current difference, caused by the inconsistent parasitic, the voltage-current double closed-loop-control is used, and the dynamic response is faster during bidirectional operation. This paper proposes theoretical analysis and experiments that verify bipolar bidirectional DC/DC converter for high-power energy storage.

Keywords: bidirectional DC/DC converter (BDC); dual mode operation; current sharing; multiplexed modulation

1. Introduction

With the high penetration of intermittent energy, such as solar and wind [1–3], a power electronic interface for distributed energy storage is becoming increasingly attractive. The bidirectional DC/DC converter (BDC) is an important piece of equipment for distributed energy storage in DC microgrids, which helps to promote intermittent energy scale applications. The BDCs are widely used in DC microgrids, due to their simple structure, easy expansion, and transmission power being independent of transformers [4–7].

In particular, it plays a large irreplaceable role in the distributed energy storage of high voltage and high power. For BDCs, current research focuses on buck/boost two-level converters and control strategies for suppressing load disturbances [8,9]; however, switches are subject to low-voltages applications. The voltage and current stresses of the converter are relatively high, so a multilevel

converter is required. A multiplexed multiphase and multilevel BDC is used for a wide range of voltage variations (voltage conversion level less than 10 times); different from multilevel converters required for a high-voltage DC transmission (voltage conversion level more than 10 times), relying on transformer boosting to achieve a higher level of voltage conversion [10–12]. The n-level structure of the multiplexed multilevel BDC reduce voltage stress only 1/n of the high-side voltage; the m-phase of the multiplexed multiphase BDC reduce current stress only 1/m of the low-side current [13]. The multiphase and multilevel BDC adopts the interleaved phase modulation technology to improve the output current ripple frequency, reduce the filter capacitor ripple value in a DC microgrid [14–17].

When a battery is connected to a DC microgrid by a BDC, the BDC needs to have strong input and output impedance matching capability to keep the system stable. In particular, when the BDC operates in buck mode, the input impedance is large; when operating in boost mode, the input impedance is small; when operating in bidirectional mode, the impedance adjustment range is wider, and the response speed is faster, which is beneficial to the system stability [18].

H. L. Do. [19] proposed a soft-switching DC/DC converter with high voltage gain by a boost cell and a coupled inductor cell. Soft-switching characteristic reduces the switching loss of active power switches and increase the converter efficiency. However, the converter can only work in boost mode, and only S_2 and D_4 can achieve ZVS turn-on. The S_1-D_4 current stress is uneven, and S_1 has a higher current stress. In high-voltage and high-power distributed energy storage, it is necessary to consider the equalization and current sharing problems. X. S. Zhang et al. [20] proposed the idea of battery energy storage systems (BESSs) with integrated wind farms to stabilize the grid power. High-power BDCs are required to meet high power requirements.

R. Naderi et al. [21] proposed a dual flying capacitor active-neutral-point-clamped (DFC-ANPC) DC/AC inverter with a five-level modulation method that achieves soft switching and neutral point voltage balancing. More importantly, the five-level modulation method eliminates the transient voltage balancing issue by series-connected switches of S_5 and S_6 and decreases the switching loss. F. Mohammadi [22] discussed the configuration, operation and decoupled control mode of a VSC-HVDC. Compared to the pulse width modulation (PWM) strategies, the vector control method generates fewer voltage harmonics and allows to control the active and reactive power independently. The vector control method is used to control the VSC-HVDC system, which is based on transforming a 3-φ system into a 2-φ system by d-q frame. Droop control is easily affected by the line impedance and the frequency fluctuation of the power grid, which reduces the distribution accuracy of the active and reactive power. In the future, the bidirectional DC/DC converter (BDC) will be connected to a bipolar DC microgrid by droop control.

Reference [23] used a DC bus capacitor to provide a three-level state (buck/boost synchronous PWM modulation). However, the converter operates at high gain, and S1 is subjected to high current stress, which exacerbates the switching losses. In Reference [24], a two-level buck/boost converter is cascaded to form a three-level bidirectional DC/DC converter. However, the modulation method easily causes inconsistent duty ratios of the upper and lower half bridges to be inconsistent, thereby affecting the voltage equalization effect of the DC bus, and requires an additional voltage equalization control loop at boost mode, which increases the complexity of the control structure.

This paper proposes a multiplexed modulation technique of the flying capacitor DC/DC converter to meet the high-voltage and high-power requirements. The BDC has many advantages: (1) the bus capacitor voltage is easily stabilized by the midpoint potential balance control of the rear inverter circuit; (2) the BDC is easy to combine by the PWM sequence to achieve multiple modulations; (3) it is easy to design the control loop and suppress phase-to-phase circulation; and (4) the BDC has a strong fault tolerance ability, and failure of any one of the arms does not affect the operation of other arms. The BDC is suitable for battery energy storage systems in bipolar DC microgrids.

This paper organized as follows. The Flying capacitor type three-level DC/DC basic unit in Section 2. Multiple modulation techniques are presented in Section 3. Controller design in Section 4. Experimental verifications in Section 5. Some conclusions are given in Section 6.

2. Flying Capacitor Type Three-level DC-DC Basic Unit

This paper proposes a bidirectional DC/DC converter (BDC) topology with multiplexed modulation strategy for a high-power system, as shown in Figure 1. The parallel operation improves the current capability of the BDC; the voltage level is increased in series operation; and the high-voltage and large-capacity characteristics are realized in series-parallel operation. The symbols and reference directions are indicated in the figure. The basic unit of the flying-capacitor-type three-level bidirectional DC/DC converter (3L_BDC) easily forms a bipolar BDC of high-voltage and high-current systems.

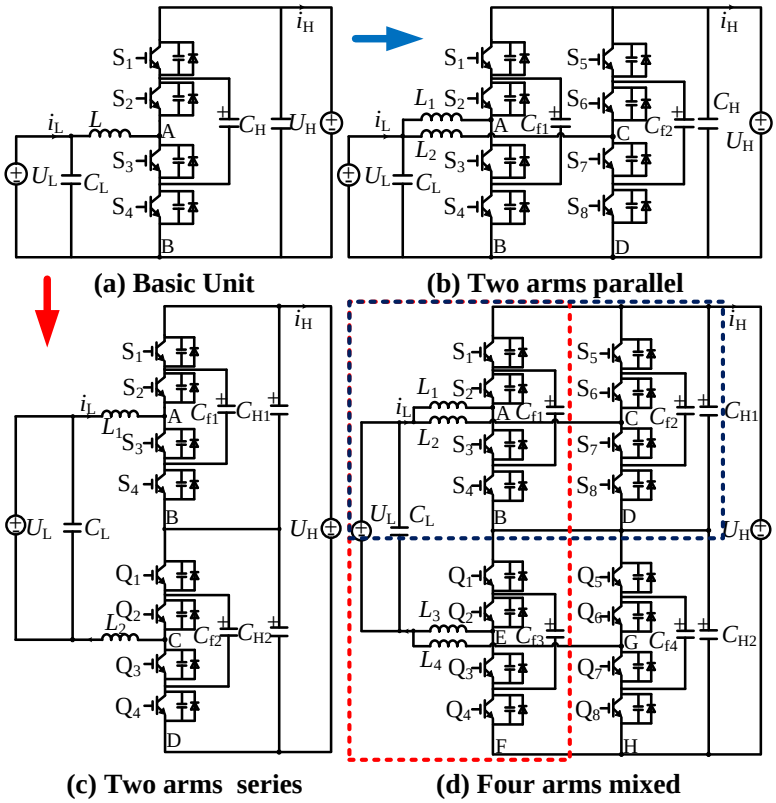


Figure 1. The proposed bidirectional DC/DC converter. (**a**) Flying capacitor type three-level DC-DC basic unit. (**b**) Two basic units parallel. (**c**) Two basic units parallel. (**d**) Four basic units mixed.

In Figure 1a, U_L is the input-side voltage, U_H is the DC bus side voltage, C_L is the battery-side capacitance, and C_H is the DC bus side capacitance. The conduction time of S_3 and S_4 is defined as T_{on} in the switching period T_s, and the duty ratio is $D = T_{on}/T_s$. To facilitate the analysis, define the switch function as follows:

$$M_k = \begin{cases} 00\ (S_1,\ S_2\ \text{ON},\ \ S_3,\ S_4\ \text{OFF}) \\ 01\ (S_2,\ S_4\ \text{ON},\ \ S_1,\ S_3\ \text{OFF}) \\ 10\ (S_1,\ S_3\ \text{ON},\ \ S_2,\ S_4\ \text{OFF}) \\ 11\ (S_3,\ S_4\ \text{ON},\ \ S_1,\ S_2\ \text{OFF}) \end{cases}. \quad (1)$$

The modal analysis is performed on the basic unit of the flying-capacitor-type three-level bidirectional DC/DC converter. The key waveform is shown in Figure 2. When the operating mode at $D > 0.5$, the switching mode of S_3 and S_4 is only 01, 10, 11, and not 00. The voltage at the two points of AB is $0.5U_H$ or 0; at $D < 0.5$, the switching mode of S_3 and S_4 is only 00, 01, 10, and not 11. The voltage of AB is U_H or $0.5U_H$. The inductive current flowing from the low-voltage side to the high-voltage side is defined as the positive direction.

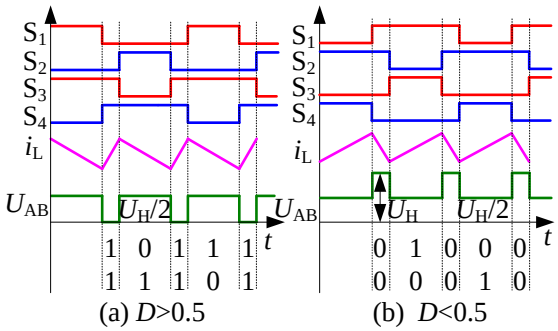


Figure 2. The main waveform of the basic unit. (**a**) Mode $D > 0.5$. (**b**) Mode $D < 0.5$.

2.1. Operational Modal Analysis $D > 0.5$

During the switching cycle, there are three modes of 11, 01, and 10 for each arm.

1. Mode $M_3 = 11$, S_1 and S_2 are turned off, S_3 and S_4 are turned on, S_1 and S_2 voltage stress are $U_H/2$, the voltage of AB two-point is $U_{AB} = 0$, the inductor voltage across L_1 is U_L, and i_L flows to the high-voltage side and linearly increases:

$$\begin{cases} \dot{i}_L = -\frac{r_L}{L} i_L + \frac{1}{L} U_L \\ \dot{U}_H = -\frac{1}{R_H C_H} U_H \\ \dot{U}_f = 0 \end{cases} . \tag{2}$$

2. Mode $M_1 = 01$, S_1 and S_3 turn off, S_2 and S_4 turn on, the S_1 and S_3 voltage stresses are $U_H/2$, the flying capacitor C_{f1} charge according to the differential equation $C_{f1}\, dU_{f1}/dt = I_c$, that is $\Delta U_{f1}=t_2 I_c/C_{f1} = Q_c/C_{f1}$, $U_{AB} = U_{f1} = U_H/2$, the inductor L_1 is U_L - $U_{AB} < 0$, the inductor current i_L decreases linearly, and the average inductor current is $I_L = I_c$.

$$\begin{cases} \dot{i}_L = -\frac{r_L}{L} i_L + \frac{1}{L} U_L - \frac{1}{L} U_f \\ \dot{U}_H = -\frac{1}{R_H C_H} U_H \\ \dot{U}_f = \frac{1}{C_f} i_L \end{cases} . \tag{3}$$

3. Mode $M_3 = 11$, S_1 and S_2 are turned off, S_3 and S_4 are turned on, the S_1 and S_2 voltage stresses are $U_H/2$, the voltage of the two-point of AB is $U_{AB}=0$, the voltage of the inductance L_1 is U_L, and i_L flows to high voltage side and linearly increase, as shown in Equation (2).
4. Mode $M_2 = 10$, S_2 and S_4 are turned off, S_1 and S_3 are turned on, the S_2 and S_4 voltage stresses are $U_H/2$, flying capacitor C_{f1} is discharged, $U_{AB} = U_H - U_{f1} = U_H/2$, the voltage across inductor L_1 is $U_L - U_{AB} < 0$, and i_L flows to the high-pressure side and decreases linearly. The column differential equation can be obtained as:

$$\begin{cases} \dot{i}_L = -\frac{r_L}{L} i_L + \frac{1}{L} U_L + \frac{1}{L} U_f - \frac{1}{L} U_H \\ \dot{U}_H = \frac{1}{C_H} i_L - \frac{1}{R_H C_H} U_H \\ \dot{U}_f = -\frac{1}{C_f} i_L \end{cases} . \tag{4}$$

According to the duty cycle definition, each equation group for the modal action time can be listed during the switching period:

$$\begin{cases} t_1 + t_2 + t_3 = D\mathrm{T_s} \\ t_1 + t_3 + t_4 = D\mathrm{T_s} \\ t_1 + t_2 + t_3 + t_4 = \mathrm{T_s} \end{cases} \Rightarrow \begin{cases} t_2 = (1-D)\mathrm{T_s} \\ t_4 = (1-D)\mathrm{T_s} \\ t_1 + t_3 = (2D-1)\mathrm{T_s} \end{cases} . \tag{5}$$

The inductance satisfies the volt-second balance condition:

$$U_{\mathrm{L}}(2D-1)\mathrm{T_s} + (U_{\mathrm{L}} - U_{\mathrm{H}}/2)(2-2D)\mathrm{T_s} = 0 \Rightarrow \frac{U_{\mathrm{H}}}{U_{\mathrm{L}}} = \frac{1}{1-D}. \quad (6)$$

2.2. Operational Modal Analysis $D < 0.5$

During the switching cycle, each arm has three modes of 00, 10, and 01.

1. Mode $M_0 = 00$, S_3 and S_4 are turned off, S_1 and S_2 are turned on, the voltage of AB is $U_{\mathrm{AB}} = U_{\mathrm{H}}$, S_3 and S_4 voltage stress are $U_{\mathrm{H}}/2$, the voltage of inductance L_1 is $U_{\mathrm{L}} - U_{\mathrm{H}}$, i_{L} flows to the high-voltage side and decreases linearly, and the corresponding differential equation can be expressed as:

$$\begin{cases} \dot{i}_{\mathrm{L}} = -\frac{r_{\mathrm{L}}}{L} i_{\mathrm{L}} + \frac{1}{L}(U_{\mathrm{L}} - U_{\mathrm{H}}) \\ \dot{U}_{\mathrm{H}} = -\frac{1}{R_{\mathrm{H}} C_{\mathrm{H}}} U_{\mathrm{H}} \\ \dot{U}_{\mathrm{f}} = 0 \end{cases}. \quad (7)$$

2. Mode $M_2 = 10$, S_2 and S_4 are turned off, S_1 and S_3 are turned on, S_2 and S_4 voltage stress are $U_{\mathrm{H}}/2$, C_{f1} is discharging, $U_{\mathrm{AB}} = U_{\mathrm{H}} - U_{\mathrm{f1}} = U_{\mathrm{H}}/2$, the voltage across inductor L_1 is $U_{\mathrm{L}} - U_{\mathrm{AB}} > 0$, i_{L} flows to the high-voltage side and increases linearly, and the differential equation can be expressed as Equation (4).
3. Mode $M_0 = 00$, S_3 and S_4 are turned off, S_1 and S_2 are turned on, the voltage of AB is $U_{\mathrm{AB}} = U_{\mathrm{H}}$, S_3 and S_4 voltage stress are $U_{\mathrm{H}}/2$, inductance L_1 voltage is $U_{\mathrm{L}} - U_{\mathrm{H}}$, i_{L} flow to high voltage side and the linearity is reduced, and the differential equation can be expressed as Equation (7).
4. Mode $M_1 = 01$, S_1 and S_3 are turned off, S_2 and S_4 are turned on, S_1 and S_3 voltage stresses are $U_{\mathrm{H}}/2$, flying capacitor C_{f1} is charging, $U_{\mathrm{AB}} = U_{\mathrm{f1}} = U_{\mathrm{H}}/2$, the inductor voltage across L_1 is $U_{\mathrm{L}} - U_{\mathrm{AB}} > 0$, i_{L} flows to the high-voltage side and increases linearly, and the differential equation can be expressed as Equation (3). According to the duty cycle definition, each mode action time can be expressed as:

$$\begin{cases} t_2 = D\mathrm{T_s} \\ t_4 = D\mathrm{T_s} \\ t_1 + t_3 = (1-2D)\mathrm{T_s} \end{cases}. \quad (8)$$

The inductance satisfies the volt-second balance:

$$2D\mathrm{T_s}(U_{\mathrm{L}} - U_{\mathrm{H}}/2) + (1-2D)\mathrm{T_s}(U_{\mathrm{L}} - U_{\mathrm{H}}) = 0 \Rightarrow \frac{U_{\mathrm{H}}}{U_{\mathrm{L}}} = \frac{1}{1-D}. \quad (9)$$

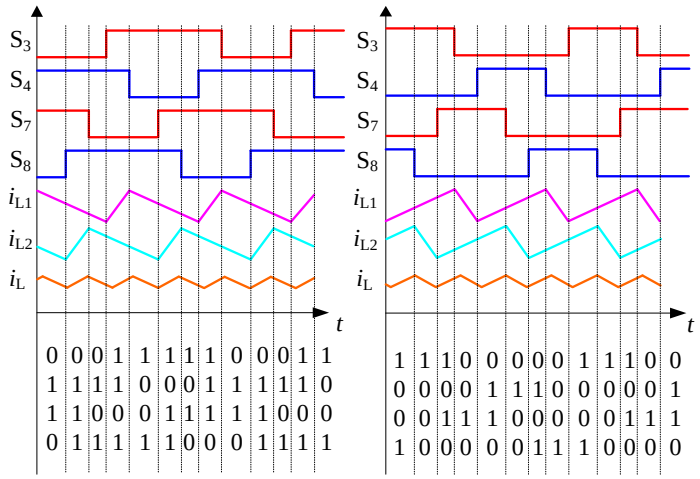
3. Multiple Modulation Technique

3.1. Two Arms Interleaved Parallel Modulation

Two arms are paralleled, as shown in in Figure 1b, to increase the overcurrent capability and reduce the input side ripple. Arm 1 is composed of S_1-S_4, the inductor L_1 and the flying capacitor C_{f1}; and arm 2 is composed of S_5, S_6, S_7, S_8, the inductor L_2 and the flying capacitor C_{f2}. Among them, S_1 and S_4 are turned on complementarily, S_2 and S_3 are turned on complementarily, the modulated waves of S_1 and S_2 are interleaved 180°, and the S_3 and S_4 modulated waves are interleaved 180°, as shown in Figure 3. Arm 2 is modulated in the same manner as arm 1 with a phase lag of 90°.

Two arms are interleaved 90° in parallel; eight modes are used at $0.5 < D < 0.75$, and other eight modes are used at $0.25 < D < 0.5$. The working mode of the space ratio is shown in Table 1. In the forward power flow (Boost mode), the inductor currents i_{L1} and i_{L2} are positive and flow from the low voltage side to the high voltage side. When the negative power flows (Buck mode), the inductor currents of i_{L1} and i_{L2} are negative, and the high voltage side flows to the low voltage side. The driving signal between the two arms is interleaved 90°, and the other side bridge arm switch maintains the

original state when one side bridge arm is operated. After the inductor current is superimposed, the low-voltage side current is $i_L = i_{L1} + i_{L2}$ doubling the pulsation frequency, and the ripple of the i_L is reduced.



(a) 0.5<*D*<0.75 (b) 0.25<*D*<0.5

Figure 3. The main waveform of two parallel arms. (**a**) Mode $0.5 < D < 0.75$, (**b**) Mode $0.25 < D < 0.5$.

Table 1. Two arms interleaved parallel coding.

0~0.25	$D = 0.25$	0.25~0.5	$D = 0.5$	0.5~0.75	$D = 0.75$	0.75~1
0000	0010	1010	1010	0101	1101	1111
0010	0010	0010	1010	1101	1101	1101
0000	0100	0110	0110	1001	1011	1111
0100	0100	0100	0110	1011	1011	1011
0000	0001	0101	0101	1010	1110	1111
0001	0001	0001	0101	1110	1110	1110
0000	1000	1001	1001	0110	0111	1111
1000	1000	1000	1001	0111	0111	0111

Then the inductor current is superimposed, the low-voltage side current is $i_L = i_{L1} + i_{L2}$ doubling the pulsation frequency, and the ripple of the i_L is reduced. According to Equations (2)–(9), the ripple current of three-level bi-directional DC/DC(3L-BDC) in Figure 1b, $\Delta I_{L1\_3L\_LBDC}$, can be calculated as

$$\Delta I_{L1\_3L\_BDC} = \begin{cases} \frac{(U_H - 2U_L)(1-D)}{2L_1 f_s}, & (D > 0.5) \\ \frac{(2U_L - U_H)D}{2L_1 f_s}, & (D \le 0.5) \end{cases}. \quad (10)$$

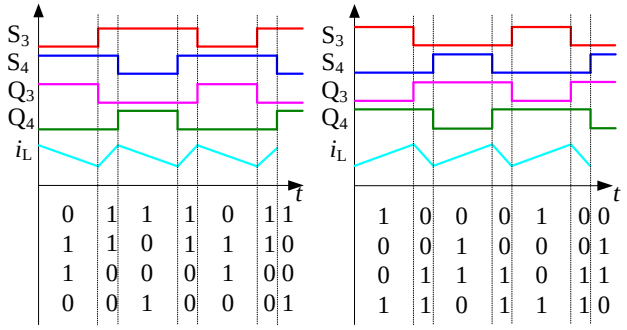
Correspondingly, the ripple current of the inductor of two-level bidirectional DC/DC (2L_ BDC) can be calculated as

$$\Delta I_{L1\_2L\_BDC} = \frac{(U_H - U_L)D}{L_1 f_s}. \quad (11)$$

To reduce currents ripple, n arms can be cascaded, and the drive signals between the arms are interleaved $180°/n$. The more arms that participate in interleaved parallel connection, the more obvious the ripple reduction effect, and the more characteristic points of zero ripple appear at the same time—these zero ripple points show a uniform distribution law. The aforementioned analysis shows that the voltage stress on the switches and the flying capacitors of the 3L_BDC is half of U_H, which is just half of the traditional 2L_BDC. To reduce the voltage stress, it is necessary to employ a series connection.

3.2. Two Arms Complementary Series Modulation

The topology is connected in series with two inductors to reduce the inductor current ripple amplitude; the low voltage side is isolated from the output side by two inductors, which can improve the energy storage unit safety; the series structure can reduce the voltage stress of the switches and increase the voltage level of the DBC, as shown in Figure 1c. The inductor current waveform during complementary modulation is shown in Figure 4. S_4 and Q_1 are the same drive signal, S_3 and Q_2 are the same drive signal, S_2 and Q_3 are the same drive signal, and S_1 and Q_4 are the same drive signal; that is, the switch modulation is based on the topology. The switching period inductance fluctuation frequency is equal to twice of the switching frequency, the inductance fluctuation amplitude is half of that of the single submodule, and the remaining mode complementary series modulation is shown in Table 2.



(a) 0.5<D<0.75 (b) 0.25<D<0.5

Figure 4. The key waveform of two arms series. (**a**) Mode 0.5 < D < 0.75, (**b**) Mode 0.25 < D < 0.5.

Table 2. Two arms complementary series coding.

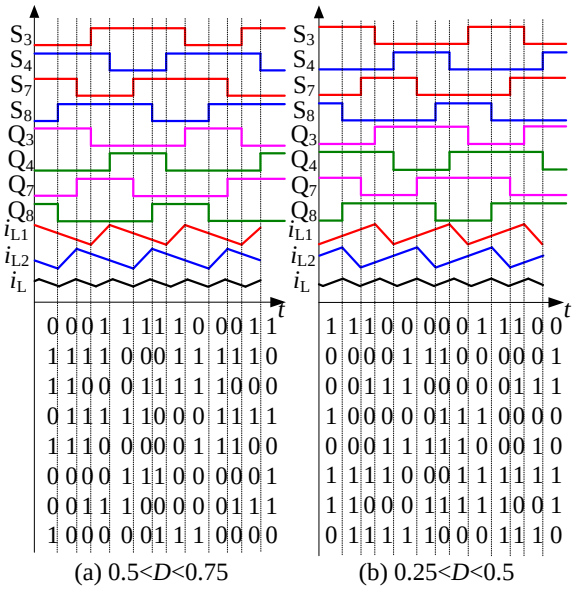
0~0.25	0.25	0.25~0.5	0.5	0.5~0.75	0.75	0.75~1
00/11	00/11	00/11	01/10	11/00	11/00	11/00
01/10	01/10	01/10	10/01	10/01	10/01	10/01
00/11	00/11	00/11	01/10	11/00	11/00	11/00
10/01	10/01	10/01	10/01	01/10	01/10	01/10

The voltage stress on the switches and the flying capacitors is 0.25 U_H in Figure 1c. In order to reduce the voltage and current stress, it is necessary to increase the series and parallel bridge arms simultaneously. The ripple current of L_1 in Figure 1c, $\Delta I_{L1\_3L\_LBDC}$, can be calculated as

$$\Delta I_{L1\_3L\_BDC} = \begin{cases} \frac{(U_H - 2U_L)(1-D)}{2(L_1+L_3)f_s}, & (D > 0.5) \\ \frac{(2U_L - U_H)D}{2(L_1+L_3)f_s}, & (D \le 0.5) \end{cases}. \quad (12)$$

3.3. Four Arms Mixed Modulation

To meet the large-capacity requirements in the bipolar DC bus, the voltage and current stress of the switching tube should be reduced, so a four-arms mixed converter is proposed, that is, the cascaded form of the interleaved parallel flying-capacitor type three-level converter, as shown in Figure 1d. The left and right parallel arms are interleaved 90° parallel modulation, and the upper and lower series arms are complementarily connected in series. For example, when 0.5 < D < 0.75, in mode 0101/1010, it means S_3 is off, S_4 is on, S_7 is off, S_8 is on; while, Q_3 is on, Q_4 is off, Q_7 is on, and Q_8 is off. The modulation rule of the BDC is shown in Figure 5.



(a) 0.5<*D*<0.75 (b) 0.25<*D*<0.5

Figure 5. The key waveform of the four arms mixed. (**a**) Mode 0.5 < *D* < 0.75, (**b**) Mode 0.25 < *D* < 0.5.

By mixed modulation, the average inductor current is only half of the single-arm current, the ripple frequency is doubled, the flying capacitor voltage is 0.25 U_H, and the voltage stress of the switch is only 0.25 U_H compared to the 2L_BDC. The modulation is shown in Table 3. To compare the characteristics of the structure, shown in Figure 1, the voltage and current stress conditions are listed in Table 3, and the four arms mixed modulation is more suitable for bipolar high-power applications. This modulation strategy helps to control and protect the design of the circuit. A topological comparison of the proposed BDC in this paper with others are shown in Table 4.

Table 3. Four arms mixed modulation coding.

0~0.25	*D* = 0.25	0.25~0.5	*D* = 0.5	0.5~0.75	*D* = 0.75	0.75~1
0000/1111	0010/1101	1010/0101	1010/0101	0101/1010	1101/0010	1111/0000
0010/1101	0010/1101	0010/1101	1010/0101	1101/0010	1101/0010	1101/0010
0000/1111	0100/1011	0110/1001	0110/1001	1001/0110	1011/0100	1111/0000
0100/1011	0100/1011	0100/1011	0110/1001	1011/0100	1011/0100	1011/0100
0000/1111	0001/1110	0101/1010	0101/1010	1010/0101	1110/0001	1111/0000
0001/1110	0001/1110	0001/1110	0101/1010	1110/0001	1110/0001	1110/0001
0000/1111	1000/0111	1001/0110	1001/0110	0110/1001	0111/1000	1111/0000
1000/0111	1000/0111	1000/0111	1001/0110	0111/1000	0111/1000	0111/1000

4. Controller design

Define the state variable as $x = [\, i_L, U_H, U_f \,]^T$, the input variable as $u = U_L$, the transfer function as $G_{id}(s)$ from the duty cycle d to the inductor current i_L and the transfer function $G_{ud}(s)$ from the duty cycle d to the output voltage U_H, according to Equations (2)–(9).

$$G_{id}(s) = \frac{\frac{U_L C_H R_H}{1-D} s + \frac{2U_L}{1-D}}{C_H L R_H s^2 + Ls + R_H (1-D)^2 + r_L}, \tag{13}$$

$$G_{ud}(s) = \frac{-\frac{LU_L}{(1-D)^2} s + R_H U_L - \frac{r_L U_L}{(1-D)^2}}{C_H L R_H s^2 + Ls + R_H (1-D)^2 + r_L}, \tag{14}$$

where, R_H is R_{load}, and r_L is the inductance parasitic resistance.

The main circuit *parameters* of the converter are shown in Table 5. Due to the inconsistent impedance of the IGBT parasitic parameters and the inductor winding process, the main loop has a certain degree of impedance difference. The controller's PI regulator is $G_c(s) = k_1 + k_2/s$, where $k_1 = 0.1$, $k_2 = 50$, and the control block diagram is shown in Figure 6.

Table 4. Topological comparison.

(a) Comparison in terms of passive component and out gain, inductor ripple current and switching frequency.

Proposed	Number of Elements	Gain of Voltage	Δi_L	$f_{\Delta i_L}$
SC [23]	$C = 3$ $S = 4$ $L = 1$	$\frac{2U_L}{1-D}$	$\frac{(U_H-2U_L)D}{2Lf_s}$	f_s
Double Buck/Boost [24]	$C = 3$ $S = 4$ $L = 2$	$\frac{U_L}{1-D}$	$\frac{U_H(1-D)D}{Lf_s}$	$2f_s$
Basic FC [5]	$C = 3$ $S = 4$ $L = 1$	$\frac{U_L}{1-D}$	$\begin{cases} \frac{(U_H-2U_L)(1-D)}{2L_1f_s}, & (D > 0.5) \\ \frac{(2U_L-U_H)D}{2L_1f_s}, & (D \le 0.5) \end{cases}$	$2f_s$
Interleaved FC [7]	$C = 4$ $S = 8$ $L = 2$	$\frac{U_L}{1-D}$	$\begin{cases} \frac{(U_H-2U_L)(1-D)}{2L_1f_s}, & (D > 0.5) \\ \frac{(2U_L-U_H)D}{2L_1f_s}, & (D \le 0.5) \end{cases}$	$4f_s$
Complementary FC [21]	$C = 5$ $S = 8$ $L = 2$	$\frac{U_L}{1-D}$	$\begin{cases} \frac{(U_H-2U_L)(1-D)}{2(L_1+L_3)f_s}, & (D > 0.5) \\ \frac{(2U_L-U_H)D}{2(L_1+L_3)f_s}, & (D \le 0.5) \end{cases}$	$2f_s$
This paper	$C = 7$ $S = 16$ $L = 4$	$\frac{U_L}{1-D}$	$\begin{cases} \frac{(U_H-2U_L)(1-D)}{2(L_1+L_3)f_s}, & (D > 0.5) \\ \frac{(2U_L-U_H)D}{2(L_1+L_3)f_s}, & (D \le 0.5) \end{cases}$	$4f_s$

(b) Comparison in terms of out capacitor, flying capacitor voltage, voltage across switch, inductor current and fault tolerant capabilities

Proposed.	Output Capacitor Voltage	Flying capacitor voltage	Switch Voltage	Inductor Current	Fault Tolerance
SC [23]	2 U_L/(1-D)	0.5 U_H	0.5 U_H	I_L	Weak
Double Buck/Boost [24]	U_L/(1-D)	No	0.5 U_H	I_L	Weak
Basic FC [5]	U_L/(1-D)	0.5 U_H	0.5 U_H	I_L	Weak
Interleaved FC [7]	U_L/(1-D)	0.5 U_H	0.5 U_H	0.5 I_L	Average
Complementary FC [21]	U_L/(2-2D)	0.25 U_H	0.25 U_H	I_L	Average
This paper	UL/(2-2D)	0.25 U_H	0.25 U_H	0.5 I_L	Strong

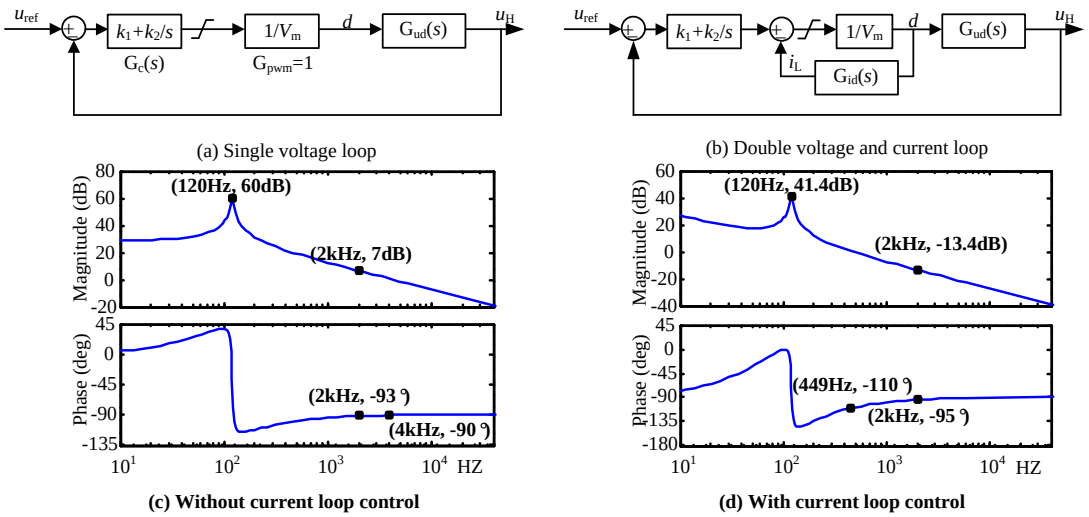


Figure 6. The control strategy. (**a**) & (**c**) are single voltage loop and its Bode without current loop control. (**b**) & (**d**) are double voltage-current loop and its Bode with current loop control.

The Bode diagram of the proposed control strategy by a single voltage loop, as shown in Figure 6c. The low frequency range is 30 dB, the high frequency band traverses 0 dB with a slope of −20 dB/dec, and the corner frequency is 120 Hz. The gain crossover frequency is 4 kHz, the phase margin is 90°,

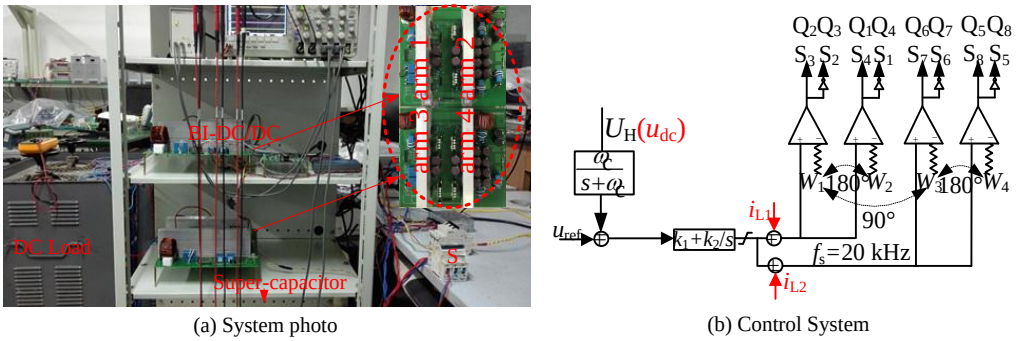
and the system is stable; however, the gain is higher than 0dB at 0.1 times of switching frequency. The current inner loop uses inductor current feedback, as shown in Figure 6d. The PI regulator is $G_c(s) = 0.1 + 50/s$, the crossing frequency of the open-loop transfer function is 449 Hz when crossing the 0 dB line, and the phase margin is 70° at the crossing frequency. It can be judged that the closed loop system is stable. A first-order low-pass filter is added to the loop due to the influence of high frequency noise. The cutoff frequency of the first-order low-pass filter ($\omega_c = 2\pi fc$) is set at 0.1 times the switching frequency, and the gain margin kg (f_c = 2 kHz) is 13.4 dB, which is ideal. The pole introduced by the first-order LPF is far from the real axis, and has little effect on the bode diagram and can be ignored.

Table 5. The Parameters of BDC.

Parameters	Value	Parameters	Value
U_L/V	150~220	C_L/μF	220
U_H/V	400	C_H/μF	110
P_o/kW	1	C_{f1}/μF	110
L_1~L_2/mH	2	C_{f2}/μF	110
r_L/Ω	0.2	f_s/kHz	20

5. Experimental result

The experimental platform is shown in Figure 7. In the platform, the DC power supply E and resistance R are used to simulate the power generation change of the renewable energy source. The rated voltage of the DC power supply E is 450 V, and the DC bus voltage rating is 400 V. Super capacitor rated voltage is 250 V, rated capacity is 10 F, maximum discharge current is 15 A, charging current is 10 A, super capacitor voltage U_L range is 150~220 V; switching frequency f_s is 20 kHz. DC power supply Chroma 62050H-600 (Chroma Systems Solutions, Inc., Foothill Ranch, CA, USA), DC probe YOKOGAWA 701934 (Yokogawa Electric, Inc., Tokyo, Japan), oscilloscope Tek DPO2024B (Tektronix, Inc., Beaverton, OR, USA). The control chip uses DSP (TMS28335) combined with FPGA (EP3C25Q240); DSP is used for signal sampling and control signal generation, and FPGA is used to generate the modulated wave. To test the feasibility of multiple applications, super capacitor U_L = 200V, high side load R_H = 200 Ω, adjustable power supply E = 450 V, resistance R = 10 Ω; during switch S disconnection, super capacitor discharge, converter operates on boost $0.5 < D < 0.75$ mode, the high side capacitor voltage is stable to U_H = 400 V. Super capacitor U_L = 250 V, high-voltage-side load R_H = 200 Ω, adjustable power supply E = 450 V, resistance R = 10 Ω; during switch S closing, super capacitor charging.



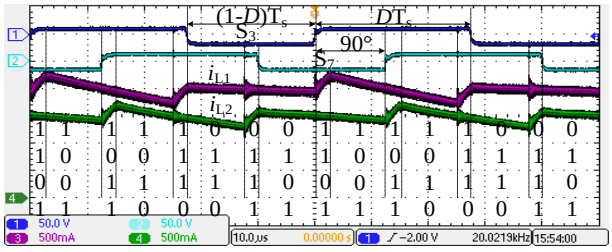
(a) System photo (b) Control System

Figure 7. Experimental setup. (**a**) The experimental system, (**b**) Control system logic.

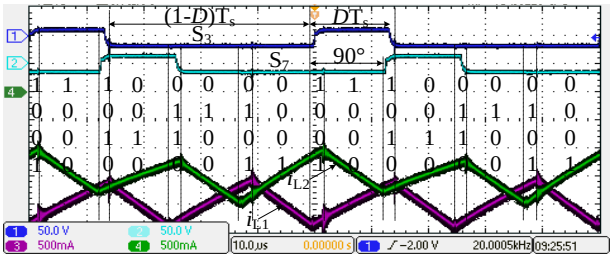
In the project, due to the inconsistent IGBT parasitic parameters and the inconsistent impedance caused by the inductor winding process, the main loop objectively has impedance differences.

The voltage and current double closed-loop PI regulators are used for impedance matching. The two control loops share the voltage outer loop, and the current inner loop uses respective inductor

current feedback. The control loop is shown in Figure 7b. The difference in the modulation signals generated by the control loop adjusts the respective output impedances to achieve current sharing control. The left and right arms are interleaved 90° parallel, the two inductor current ripples cancel each other, and the output voltage is stable, as shown in Figures 8 and 9. The current i_L fluctuating frequency is twice of the switching frequency, and the inductor current fluctuation amplitude is reduced, due to i_L through two inductors evenly. Two arms series, the flying capacitor voltage is 0.25 U_H, as shown in Figure 10. The inductor current ripple is small, and the flying capacitor voltage is equal to 0.25 U_H.

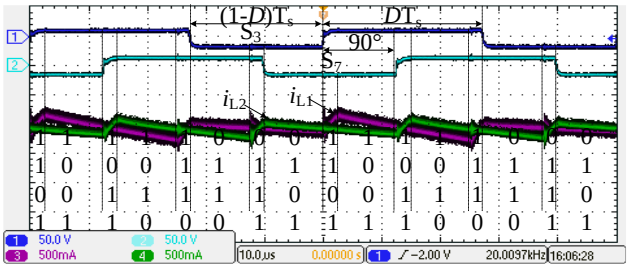


(a) Boost mode without circumferential inhibition

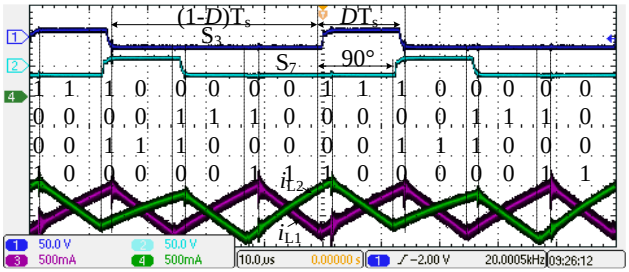


(b) Buck mode without circumferential inhibition

Figure 8. Left and right arms interleaved 90° parallel without circumferential inhibition. (**a**) Boost mode. (**b**) Buck mode.



(a) Boost mode with circumferential inhibition

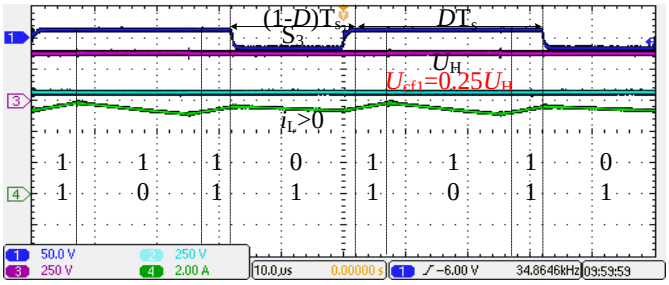


(b) Buck mode with circumferential inhibition

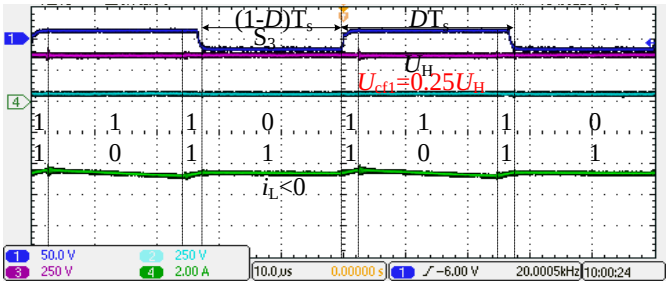
Figure 9. Left and right arms interleaved 90° parallel with circumferential inhibition. (**a**) Boost mode, (**b**) Buck mode.

Switch *S* is turned on at t_{ON}, and the supercapacitor charging power is 800 W in buck mode. Switch S is turned off at t_{OFF}, and the supercapacitor discharging power is 1200 W in boost mode, as shown in Figure 11. The dynamic response time is less than 20 ms from charging to discharging. The dynamic response time is

400 ms from discharging to charging in the four-arms mixed modes. The flying capacitor voltage is always stable, and the DC bus voltage fluctuation is less than 20 V. The input voltage varies between 150–220 V, the output voltage is stable at 400 V, and the change range of D is 0.63–0.45. From the experimental results in Figures 8–11, it can be seen that the input and output side voltage ripple is less than 1%, and the current ripple frequency is relatively small, which is beneficial to the stable operation of the energy storage unit. When Q_7 shorted, i_{L4} ripple is only once per cycle, losing the advantage of three levels. However, the overall performance of the converter remains stable, and the input and output voltage ripples are low, as shown in Figure 12. Therefore, the BDC has a strong fault tolerance ability, and failure of any one of the arms does not affect the operation of other arms.

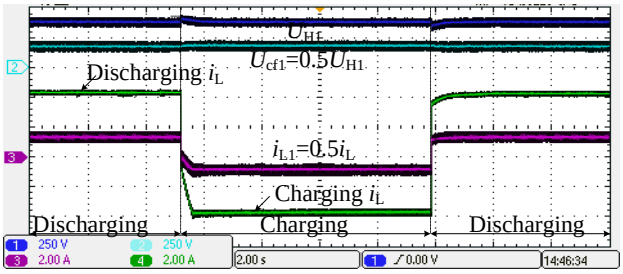


(a) Boost mode

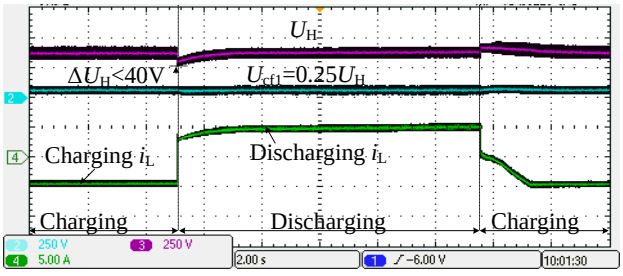


(b) Buck mode

Figure 10. Two arms complementary series. (**a**) Boost mode, (**b**) Buck mode.



(a) Two arms parallel



(b) Two arms series

Figure 11. Transient response for bidirectional operation. (**a**) Two arms interleaved parallel transient response, (**b**) Two arms complementary series transient response.

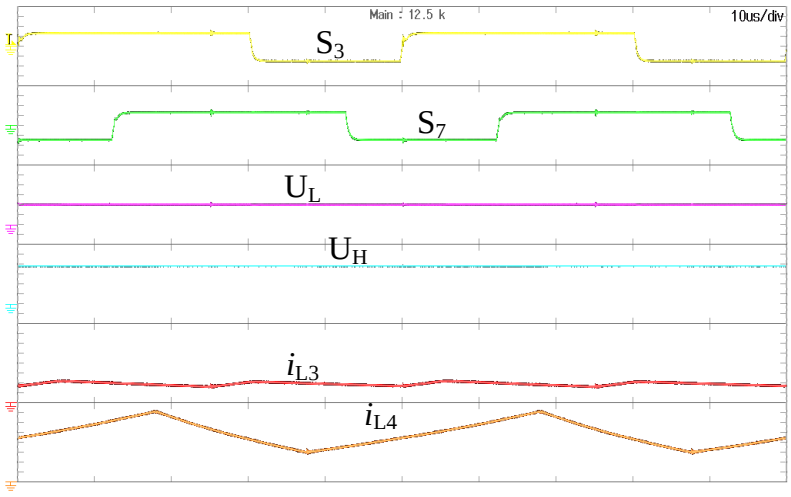


Figure 12. Switch Q7 short circuit experiment.

The efficiency is reduced, due to the inherent loss increase with a light load. Since there is a dead time of 1.5 µs when the converter is actually running, energy can be transferred from the low voltage side to the high voltage side through the IGBT body diode during dead time, as shown in Figure 13. Thus, the boost mode efficiency is higher than the buck mode. The efficiency curve is more than 90% from light load to heavy load, meeting design requirements.

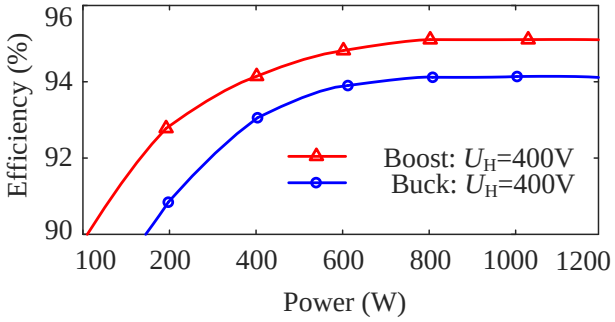


Figure 13. The efficiency curves.

6. Conclusions

This paper proposes a BDC topology with a multiplexed modulation strategy for high-power energy storage in bipolar DC microgrids. The parallel arms divide the input side current, which can effectively overcome the current difference caused by the inconsistent parasitic parameters of the parallel arms. The series arms divide the voltage of the high voltage side, which can effectively reduce the voltage stress of the switch and the flying capacitor. The bidirectional transient response is milliseconds, which ensures the dynamic performance and operating efficiency of the converter. The BDC has a strong fault tolerance ability, and the failure of any one of the arms does not affect the operation of other arms. The proposed BDC topology and its modulation strategy can effectively solve the issue of high-power energy storage in bipolar DC microgrids.

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Conflicts of Interest: The authors declare no potential conflict of interest.

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