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Naidu, Talada Appala; Arya, Sabha Raj; Maurya, Rakesh; Sanjeevikumar, P.

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ORIGINAL RESEARCH PAPER

Variable fractional power-least mean square based control algorithm with optimized PI gains for the operation of dynamic voltage restorer

Talada Appala Naidu[1] | **Sabha Raj Arya**[1] | **Rakesh Maurya**[1] | **P. Sanjeevikumar Fellow IET**[2]

[1] Department of Electrical Engineering, Sardar Vallabhbhai National Institute of Technology, Surat 395007, India

[2] Department of Energy Technology, Aalborg University, Esbjerg 6700, Denmark

Correspondence
Sabha Raj Arya, Department of Electrical Engineering, Sardar Vallabhbhai National Institute of Technology, Dumas Road, Surat, 395007, India.
Email: sabharaj79@gmail.com

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Abstract

The operation of Dynamic Voltage Restorer has been studied for the mitigation of supply voltage disturbances like sag, swell, distortions, and unbalances. A Dynamic Voltage Restorer with three single-phase Voltage Source Converters has been implemented for this purpose. Dynamic Voltage Restorer's compensation capability has been evaluated while introducing the above-said voltage related disturbances in the supply by different means. A control algorithm named Variable Fractional Power-Least Mean Square has been proposed for generating the load reference voltage for Dynamic Voltage Restorer. Variable Fractional Power-Least Mean Square extracts the fundamental active and reactive component out of non-ideal supply voltage and is thus, used in generating reference load voltage. This algorithm is more robust with respect to disturbance due to variable step size and is computationally less expensive. In addition, an optimization-based approach has been proposed to estimate the approximate values of PI control gains. For this reason, a population-based optimization method known as Sine Cosine Optimization has been used. The added feature of the optimization method is the reduction of computational time as compared to conventional PI controller tuning. A model of Dynamic Voltage Restorer using Variable Fractional Power-Least Mean Square control algorithm with Sine Cosine Optimization tuned PI gains has been built in MATLAB Simulink as well as a reduced scale experimental prototype and their results have been presented with discussion.

KEYWORDS

Distortions and imbalances, dynamic voltage restorer (DVR), fundamental components, sine cosine optimization (SCO), variable fractional power-least mean square (VFP-LMS)

1 | INTRODUCTION

Power distribution companies as well as consumers are more concerned about the quality of the power due to heavy use of non-linear and time varying devices [1]. The more often disturbances in the power system are short-term disturbances occurring due to different causes. Automatic reclosing systems are the main reasons for short duration voltage disturbances [2]. The authors in [3, 4] have listed out some flexible ac transmission system devices which have been used for mitigating the voltage and current related disturbances. Series filters are the most used for the compensation of harmonics and other voltage quality issues in the supply system [5]. Series connected device as a Dynamic Voltage Restorer (DVR) has been introduced particularly for voltage related disturbances like sag, swell, distortion etc. [6]. It is used to re-establish the bus voltage at load end with the help of Voltage Source Converter (VSC) [7]. Kangarlu *et al.* [8] have discussed a review on various topologies of DVR, operating range, control algorithm, and its applications. This paper has also illustrated fast voltage compensator

such as Static Series Compensator (SSC) and sag corrector etc. as DVR. A split-capacitor voltage source based VSC has been implemented for the DVR operation using flux-charge model feedback algorithm for limiting the fault ride through elimination [9]. Jimichi *et al.* [10, 11] have discussed the configuration of DVR with series and shunt converters connected back to back and have given the difference in DC capacitor rating in different topologies. A capacitor split battery supported DVR configuration has been built and tested for an unbalance compensation using transformation-based control algorithm in [12]. The authors in [13] have developed a cascaded multilevel inverter-based DVR configuration without using injection transformer at medium voltage level. It is based on self-supported DC bus capacitor where control of DC bus voltage and its balancing is the main challenge. Kim *et al.* [14] have developed a direct PWM cascaded multilevel converter with switching cell structure with coupled inductor, which can avoid the damage due to faults. The authors in [15], have reported the incorporation of DVR in micro-grid application to improve the power transmission capability to the upstream power grid.

Different control algorithms have been proposed since the introduction of DVR in the area of power quality (PQ) [16–20]. Jayaprakash *et al.* [16] have implemented control of battery-based DVR. This control has reduced the rating of voltage source converter. Moreover, it needs the conversion of voltage from abc to d-q axis. The authors in [17] have implemented the control algorithm based on third order sinusoidal signal integral based phase locked loop for DVR to compensate the distortions and supply voltage imbalance. Leon *et al.* in [18] have developed a positive and negative sequence-based control algorithm for DVR under the unbalance condition. The authors in [19] have implemented the instantaneous symmetric component theory-based control algorithm, which uses a Fourier transform to estimate the fundamental component for DVR in compensating unbalances and distortions. A control algorithm has been designed such that the sag or swell in the supply voltage can be compensated using the power measured in the same phase or other two phases [20]. Torres *et al.* in [21] have presented a control algorithm based on stationary reference frame based on two-degree freedom for mitigating balanced as well as unbalanced sag using DVR. The authors in [22] have used a phase-angle control scheme for mitigating the voltage sag, swell, and reactive power compensation utilizing synchronous reference frame-PLL (SRF-PLL) to synchronize the system. Kwong and Johnston [23] have proposed variable learning-based control algorithm where variation of step size depends upon the variation in mean square error. This phenomenon allows tracking of system and with smallest steady state error. In the literature, [24] has reported a variant of variable learning method based on gradient weighted average. Low mis-adjustment error and fast convergence is the main feature of this algorithm. It is useful for system identification in case of low signal to noise ratio. Ahmad *et al.* [25] proposed a variable power with Fractional Least Mean Square (FLMS) to achieve lower steady state error with higher convergence rate. The concept of variable power fraction has been dynamically adapted from the variable step size, which has been implemented in the channel estimation and system identification. It is working in adaptive framework. Due to the discussed characteristics of this algorithm, it is also effective in the area of power quality, specially to control custom power devices. Another integrated part of system control algorithm is PI controller to maintain system parameters at their reference levels. General practice for PI controller tuning is trial–error (manually) method at initial stage, then by conventional methods which are all time taking and relatively complex in computation [26]. Optimization is one of the useful areas for the analysis of the problem, tuning of gains, another constant factor etc. [27]. It needs the modeling of the search problem based on conventional or meta-heuristics concepts. Sine Cosine Optimization (SCO) algorithm, a population-based optimization technique, uses sine and cosine function in developing the technique [28]. The SCO algorithm is split into two phases for exploration and exploitation to simplify the optimization process and produce the fastest solution.

The combination of the Variable Fractional Power-LMS (VFP-LMS) control along with SCO optimized PI gains estimation has been proposed for DVR to mitigate different voltage-based power quality disturbances. The lower steady state error with higher convergence rate is the main feature of this algorithm. It is more robust with respect to disturbance due to variable step size and it adapts the fractional power dynamically. Added advantages of VFP-LMS and SCO algorithm together have been utilized in this manuscript. Since the estimation of fundamental components from the non-ideal input signals can be done by VFP-LMS based control algorithm, this control is implemented for reference voltage generation in DVR control. In addition, the SCO algorithm has been implemented for DC bus PI controller and AC PI controller to maintain them at reference levels. With the gains estimated using SCO algorithm, the VFP-LMS control algorithm has produced the gate pulses by generating the reference load voltage of DVR. The results showing the performance of SCO algorithm and control algorithm have been presented in this paper. At the same time, the compensation capability of DVR has been evaluated by presenting the simulation and experimental results of the above-said issues in the supply voltage.

2 | SYSTEM CONFIGURATION

Three single-phase configurations of DVR that are VSC based has been built as shown in Figure 1. The network topology includes the three-phase non-ideal AC grid. It saves the supply system from different types of voltage-based disturbances. The critical or sensitive load is secured from the supply side disturbances. The DVR configuration also consists of energy storage system i.e. capacitor (C_{DC}), three single-phase VSC, interfacing inductor (L_i), filtering unit (R_f, C_f), and injection transformers (T/F_{inj}) as shown in the Figure 1. The capacitor (C_{DC}) is so designed that, it should be capable of supporting voltage dynamics. The 6-leg VSC is chosen over conventional VSC due to its requirement of low value of capacitor for the same application. VSC works bi-directionally and whenever the system is stable, the VSC is ideal in operation and when the dynamics

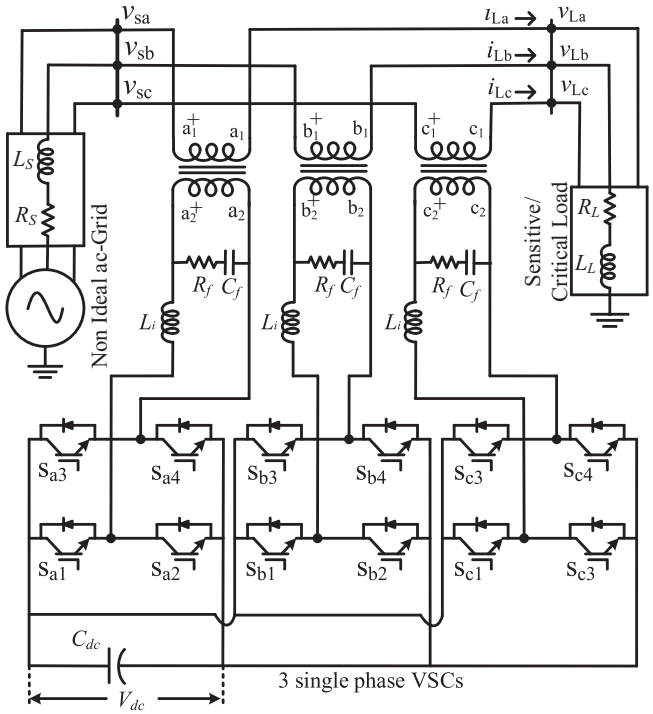


FIGURE 1 Three single-phase VSCs based DVR configuration

occurs in the supply due to various reasons, VSC converts the required amount of DC voltage to AC and works dynamically. The converted AC voltage then is passed through interfacing inductor (L_i) and filter unit (R_f, C_f) for ensuring the filtering of the switching harmonics produced from the VSC. The filtered voltage then is injected into three phase lines through three single injection transformers (T/F_{inj}) as shown in Figure 1. The three-phase supply voltage (v_s) has been measured at the point of common coupling (PCC) where the different types of voltage disturbances can be experienced. The source impedance (R_s, L_s) has been considered for the effect of the line impedance. Three-phase load voltages (v_L) and load currents (i_L) have been measured at the load bus as shown in Figure 1. The three-phase reference load voltage is generated through the proposed control algorithm. Further, these three-phase reference load voltages are used for the generation of gate pulses. A detail of the control algorithm is explained in the next section of this paper.

3 | CONTROL ALGORITHM

The Variable Fractional Power-Least Mean Square (VFP-LMS) has been developed for controlling the DVR system, which has been discussed in Section 2. Figure 2 gives the information of the complete control algorithm in which VFP-LMS has been used for the extraction of fundamental components of input disturbed voltage. The average of three-phase fundamental components have been fed back to their computation block. Figure 2 also consists of three-phase reference load voltage (v^*_L) generation with which the actual load voltages have been compared and the gate pulses have been generated. A block diagram that generates the unit templates, which are useful in the reference, load voltage generation. The clear explanation of the control algorithm has been presented as follows.

3.1 | Mathematical description of VFP-LMS

The mathematical description of fundamental active component estimation, which is useful in generating load reference voltage, has been considered for phase 'a' and analogously for phase 'b' and phase 'c'. The update equation for Fractional-LMS for phase '*a*' is as shown in Equation (1) [24, 25].

$$Z_a(n+1) = Z_a(n) - \lambda \frac{\partial J_a(n)}{\partial Z_a(n)} - \lambda_f \left(\frac{\partial}{\partial Z_a(n)}\right)^u J_a(n) \quad (1)$$

where 'λ', 'λ_f' are the step sizes, 'u' is the fractional power derivative, and Z_a(n) is the weight update. J_a(n) is the cost function which is defined as Equation (2). The error component can be estimated as shown in Equation (3).

The derivative parts of Equation (1), $\frac{\partial J_a(n)}{\partial Z_a(n)}$ and $(\frac{\partial}{\partial Z_a(n)})^u J_a(n)$ are further simplified into Equations (4) and (5).

$$J_a(n) = \frac{1}{2} e_a(n)^2 \quad (2)$$

$$e_a(n) = d_a(n) - y_a(n) \quad (3)$$

$$\frac{\partial J_a(n)}{\partial Z_a(n)} = \frac{\partial J_a(n)}{\partial e_a(n)} \times \frac{\partial e_a(n)}{\partial y_a(n)} \times \frac{\partial y_a(n)}{\partial Z_a(n)} \quad (4)$$

$$\left(\frac{\partial}{\partial Z_a(n)}\right)^u J_a(n) = \frac{\partial J_a(n)}{\partial e_a(n)} \times \frac{\partial e_a(n)}{\partial y_a(n)} \times \left(\frac{\partial}{\partial Z_a(n)}\right)^u y_a(n) \quad (5)$$

$$\frac{\partial J_a(n)}{\partial Z_a(n)} = -e_a(n) \times t_a(n) \quad (6)$$

$$\left(\frac{\partial}{\partial Z_a(n)}\right)^u J_a(n) = -e_a(t) \times t_a(t) \times \frac{Z_a^{1-u}(n)}{\Gamma(2-u)} \quad (7)$$

By the fractional derivative method named after Rieman–Lioville, Equation (4) has been simplified as Equation (6) and similarly Equation (5) as Equation (7) [25]. After substitution of Equations (6) and (7) in Equation (1), Equation (1) can be rewritten as Equation (8) as given below.

$$Z_a(n+1) = Z_a(n) + \lambda \times e_a(n) \times t_a(n) + \lambda_f \times e_a(n) \times t_a(n) \times \frac{Z_a^{1-u}(n)}{\Gamma(2-u)} \quad (8)$$

For obtaining the variable fractional power, Equation (8) can be modified into Equation (9) which gives the active

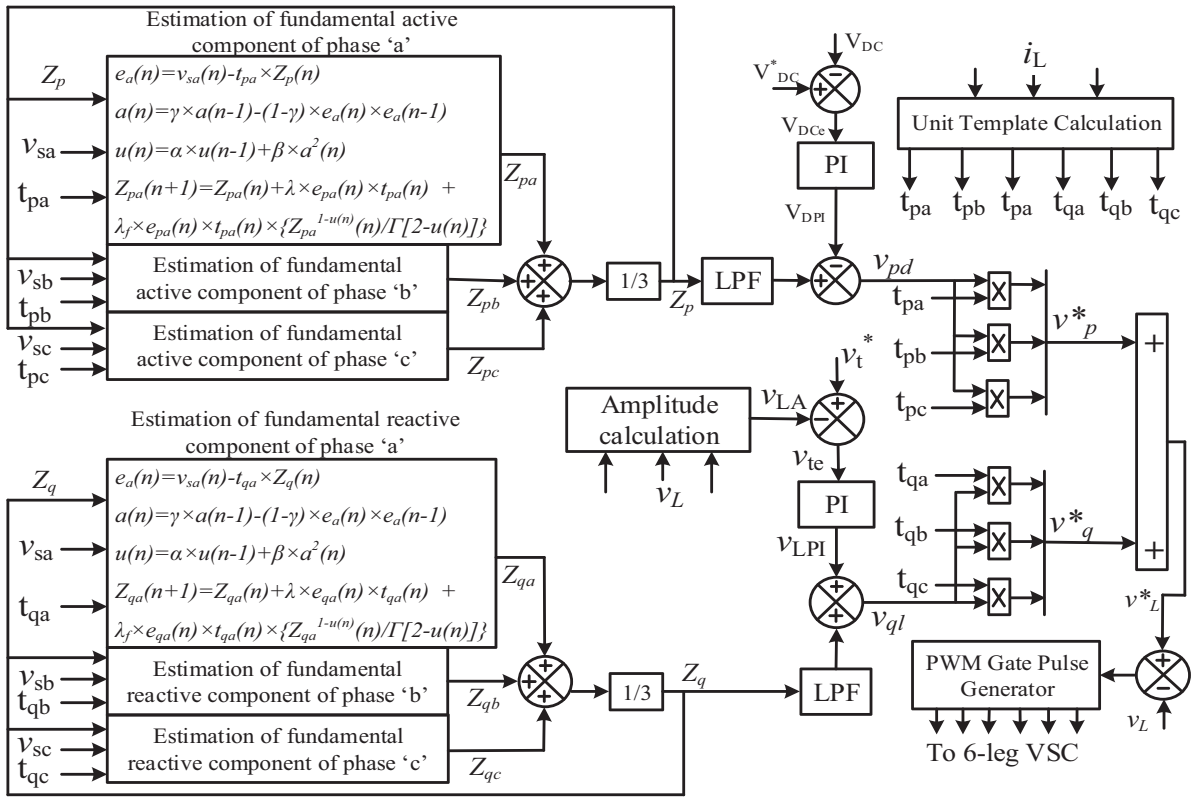


FIGURE 2 VFP-LMS based control algorithm for DVR control

fundamental component of phase 'a'.

$$Z_{pa}(n+1) = Z_{pa}(n) + \lambda \times e_{pa}(n) \times t_{pa}(n) + \lambda_f \times e_{pa}(n) \times t_{pa}(n) \times \frac{Z_{pa}^{1-u_a(n)}(n)}{\Gamma(2-u_a(n))} \quad (9)$$

where the variable fractional power update Equation (10) ensures the variation of fractional power in the weight update Equation (9), where '$a(n)$' is defined in Equation (11) where$0 < \alpha < 1, \beta > 0$ and γ, is a constant $(0 < \gamma < 1)$.

$$u_a(n+1) = \alpha \times u_a(n) + \beta \times a^2(n) \quad (10)$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_a(n) \times e_a(n-1) \quad (11)$$

So, the weight update equation for fundamental active component estimation of phase 'b' and phase 'c' have been described as in Equations (12)–(14) and Equations (15)–(17), respectively, where t_{pa}, t_{pb}, and t_{pc} are in-phase templates computed using Equation (29).

$$Z_{pb}(n+1) = Z_{pb}(n) + \lambda \times e_{pb}(n) \times t_{pb}(n) + \lambda_f \times e_{pb}(n) \times t_{pb}(n) \times \frac{Z_{pb}^{1-u_b(n)}(n)}{\Gamma(2-u_b(n))} \quad (12)$$

$$u_b(n+1) = \alpha \times u_b(n) + \beta \times a^2(n) \quad (13)$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_b(n) \times e_b(n-1) \quad (14)$$

$$Z_{pc}(n+1) = Z_{pc}(n) + \lambda \times e_{pc}(n) \times t_{pc}(n) + \lambda_f \times e_{pc}(n) \times t_{pc}(n) \times \frac{Z_{pc}^{1-u_c(n)}(n)}{\Gamma(2-u_c(n))} \quad (15)$$

$$u_c(n+1) = \alpha \times u_c(n) + \beta \times a^2(n) \quad (16)$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_c(n) \times e_c(n-1) \quad (17)$$

The average fundamental active component 'Z_p' of three phases has been computed using Equation (18).

$$Z_p = \frac{Z_{pa} + Z_{pa} + Z_{pa}}{3} \quad (18)$$

Similarly, the fundamental reactive components of phases 'a', 'b', and 'c' have been computed using Equations (19)–(27), respectively, where t_{qa}, t_{qb}, and t_{qc} are quadrature templates computed using Equation (29).

$$Z_{qa}(n+1) = Z_{qa}(n) + \lambda \times e_{qa}(n) \times t_{qa}(n) + \lambda_f \times e_{qa}(n) \times t_{qa}(n) \times \frac{Z_{qa}^{1-u_a(n)}(n)}{\Gamma(2-u_a(n))} \quad (19)$$

$$u_a(n+1) = \alpha \times u_a(n) + \beta \times a^2(n) \tag{20}$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_a(n) \times e_a(n-1) \tag{21}$$

$$Z_{qb}(n+1) = Z_{qb}(n) + \lambda \times e_{qb}(n) \times t_{qb}(n) + \lambda_f \times e_{qb}(n) \times t_{qb}(n) \times \frac{Z_{qb}^{1-u_b(n)}(n)}{\Gamma(2-u_b(n))} \tag{22}$$

$$u_b(n+1) = \alpha \times u_b(n) + \beta \times a^2(n) \tag{23}$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_b(n) \times e_b(n-1) \tag{24}$$

$$Z_{qc}(n+1) = Z_{qc}(n) + \lambda \times e_{qc}(n) \times t_{qc}(n) + \lambda_f \times e_{qc}(n) \times t_{qc}(n) \times \frac{Z_{qc}^{1-u_c(n)}(n)}{\Gamma(2-u_c(n))} \tag{25}$$

$$u_c(n+1) = \alpha \times u_c(n) + \beta \times a^2(n) \tag{26}$$

$$a(n+1) = \gamma \times a(n) + (1-\gamma) \times e_c(n) \times e_c(n-1) \tag{27}$$

The average fundamental reactive component 'Z_q' of three phases has been computed using Equation (28).

$$Z_q = \frac{Z_{qa} + Z_{qa} + Z_{qa}}{3} \tag{28}$$

$$\left.\begin{aligned} &t_{pa} = \frac{i_{La}}{I_{LA}};\ t_{pb} = \frac{i_{Lb}}{I_{LA}};\ t_{pc} = \frac{i_{Lc}}{I_{LA}} \\ &t_{qa} = 0.577 \times (t_{pc} - t_{pb});\ t_{qb} = 0.289 \times (3t_{pc} + t_{pb} - t_{pc});\ t_{qc} \\ &\quad = 0.289 \times (-3t_{pc} + t_{pb} - t_{pc}) \end{aligned}\right\} \tag{29}$$

$$I_{LA} = \sqrt{0.667 \times (i_{La}^2 + i_{Lb}^2 + i_{Lc}^2)} \tag{30}$$

In-phase and quadrature unit templates have been computed using three-phase load currents (i_L) as shown in Equation (29) where (i_{LA}) is the magnitude of the three-phase currents calculated using Equation (30). The error (V_{DCe}) is obtained between actual DC-bus voltage (V_{DC}) and that of reference (V^*_{DC}). The output (V_{dPI}) of DC-PI controller has been subtracted from the average of three-phase active fundamental component (Z_p) to get (v_{pd}), as shown in Equation (31).

$$v_{pd} = Z_p - V_{DPI} \tag{31}$$

The load terminal voltage (V_{LA}) is calculated using Equation (32) and compared with its reference value, and the error has been processed through the PI controller. The output (V_{LPI}) of terminal voltage PI controller has been added to the average fundamental reactive component (Z_q) to get (v_{ql}), as shown in Equation (33).

$$V_{LA} = \sqrt{0.667 \times (v_{La}^2 + v_{Lb}^2 + v_{Lc}^2)} \tag{32}$$

$$v_{ql} = Z_q + V_{LPI} \tag{33}$$

Three-phase active component of reference voltage (v^*_p) has been obtained by multiplying (v_{pd}) with the unit in-phase templates (t_p), as given in Equation (34). Similarly, three-phase reactive component of reference voltage (v^*_q) has been obtained by multiplying (v_{ql}) with the unit quadrature templates (t_{qa}, t_{qb}, t_{qc}), as given in Equation (35).

$$v^*_{pa} = v_{pd} \times t_{pa};\ v^*_{pb} = v_{pd} \times t_{pb};\ v^*_{pc} = v_{pd} \times t_{pc} \tag{34}$$

$$v^*_{qa} = v_{ql} \times t_{qa};\ v^*_{qb} = v_{ql} \times t_{qb};\ v^*_{qc} = v_{ql} \times t_{qc} \tag{35}$$

The three-phase load reference voltage (v^*_{Labc}) has been generated by adding the active (v^*_{pabc}) and reactive (v^*_{qabc}) component reference voltages, as given in Equation (36).

$$v^*_{La} = v^*_{pa} + v^*_{qa};\ v^*_{La} = v^*_{pa} + v^*_{qa};\ v^*_{La} = v^*_{pa} + v^*_{qa} \tag{36}$$

These generated three load reference voltages (v^*_{Labc}) are compared with the actual three-phase load voltages (v_{Labc}). After comparing, the estimated three-phase errors have been processed through high frequency carrier based triangular waveform and the gate pulses have been generated for the power semiconductor switches used in three single-phase VSCs [6].

3.2 | Description of SCO approach for PI controller tuning

As a contribution of this paper, PI controllers have been tuned using an optimization technique, which tunes the PI controller's gains automatically without any manual effort. A population-based optimization technique named after SCO algorithm has been implemented for the PI gains approximation. The common practice in population-based optimization techniques is to divide the optimization process into two phases called exploration and exploitation. Exploration decides the wide range search space region by combining the random solutions whereas exploitation guarantees the reduction in randomness in solution compared to that of exploration. Equations (37) and (38) have been proposed for exploration and exploitation, respectively, based on sine and cosine functions [28].

$$x_d^{n+1} = x_d^n + r_1 \times \sin(r_2) \times \mathrm{abs}(r_3 \times X_d^n - x_d^n) \tag{37}$$

$$x_d^{n+1} = x_d^n + r_1 \times \cos(r_2) \times \mathrm{abs}(r_3 \times X_d^n - x_d^n) \tag{38}$$

where 'x_d^n' is the current position of the solution and 'X_d^n' is the position of the destination solution. The other parameters which decide the optimization process are listed

as: $r_1 = (1 - \frac{n}{N}) \times 2$; $r_2 = 2 \times pi \times rand()$; $r_3 = 2 \times rand()$ where 'n' is the present iteration number, 'd' is the dimension of the search variable, and 'N' is the maximum number of iterations considered for the optimization process. Equations (37) and (38) have been grouped together for equal sharing of exploration and exploitation using random number '$r_4 = rand()$' which varies in between 0 and 1, which are as given in Equation (39).

$$x_d^{n+1} = \begin{cases} x_d^n + r_1 \times \sin(r_2) \times \text{abs}(r_3 \times X_d^n - x_d^n) \ldots \text{if} \ldots r_4 < 0.5 \\ x_d^n + r_1 \times \cos(r_2) \times \text{abs}(r_3 \times X_d^n - x_d^n) \ldots \text{if} \ldots r_4 \geq 0.5 \end{cases} \tag{39}$$

During the continuous process of optimizing solutions by SCO algorithm, it has been considered that this algorithm is used for the tuning of PI controller gains by adapting an objective function (f_o), as shown in Equation (40).

$$f_o = \int (t \times e^2) dt \tag{40}$$

where, 'e' is an error between the reference level and the actual quantity that is maintained at reference level, 't' is the time. Equation (40) describes that, the Error measure has to be squared, then multiplied with time, and then integrated, which has been referred to as integral time square error (ITSE) in short, which is one of the performance indexes. The actual estimation of PI gains using SCO optimization algorithm is presented in the next section.

3.3 | Estimation of PI controller gains using SCO

As discussed in the previous sub-section, detailed explanation of the process of SCO algorithm for PI controller gains estimation in VPF-LMS control algorithm for DVR has been presented here. After a number of trials of implementation, the required parameters for SCO algorithm have been chosen as follows. The maximum number of iterations (N) is 20, 10 number of search agents, and dimension of search agents (d) is set to be 4 as the number parameters to be estimated are four (i.e. Gains of DC and AC-PI controllers). Figure 3(a)–(c) illustrates the performance obtained during the optimization process for estimation of PI controllers' gains. It includes the convergence curve and the gains of variation curves with respect to iterations.

The convergence curve of SCO algorithm while gains of PI controllers' estimation has been given in Figure 3(a) from which it can be seen that the SCO algorithm has been converged to a minimum value of 101.5875 by the iteration number 8. This shows that at least eight iterations are required to get final values of all four gains by SCO algorithm as shown in Figure 3(b) and (c). Figure 3(b) illustrates the variation of k_p and k_i of DC-PI controller with respect to iterations, in which k_p has been settled to a value of 14.635 by fourth iteration and k_i to the value 0.3199 by eighth iteration. Similarly, Figure 3(c) illustrates the variation of k_p and k_i of AC-PI controller with respect to iterations, in which proportional gain (k_p) has been settled to a value of 31.684 by fourth iteration and integral gain (k_i) to the value 0.004 by eighth iteration. Therefore, the minimum number of iterations that SCO algorithm has taken to estimate the gains of both DC as well as AC-PI controllers is eight.

4 | SIMULATION STUDY

The simulation platform, MATLAB has been utilized for simulating the three single-phase VSC based DVR. The simulation configuration ode-3 has been chosen with the sample time of 20 μs. The gate pulses generated with 5 kHz frequency using VPF-LMS control are processed to the VSC, to work as DVR for the compensation of different disturbances in the supply. The three-phase system is considered as having the voltage related issues in the supply side. Voltage sag, swell, voltage distortions, and imbalances in the voltages have been included in the supply side with a duration of three cycles each. The performance of the VPF-LMS control as well as of the DVR have been studied and presented in this section as follows. The parameters considered for simulation work have been presented in Appendix Table A1.

4.1 | Load reference voltage generation using VPF-LMS based control algorithm

As discussed in the previous section, the load reference voltage generation plays a vital role in the working of DVR; the signals extracted in process of reference voltage generation have been presented here. Figure 4(a) gives the information of all the internal signals of VPF-PLL based control algorithm, which shows the disturbed three-phase supply voltage (v_s) until the three-phase load reference voltage (v^*_{Labc}) generation. Subplot (1) of Figure 4(a) shows the three supply voltages with four different types of voltage related disturbances e.g. voltage sag, swell, voltage distortions, and voltage imbalances having a duration of three cycles each. Subplots (2 and 3) in this figure, are the in-phase (t_p) and quadrature (t_q) templates generated from three-phase load currents (i_L) using Equation (29).The average fundamental active (Z_p) and reactive (Z_q) components of input supply voltage have been presented in subplots (4 and 5) of Figure 4(a). Subplots (6 and 7) of Figure 4(a) show (V_{DPI}) and (V_{LPI}), the outputs of DC-PI controller and terminal voltage PI controller, respectively. Subplots (8 and 9) of Figure 4(a) represent (v_{pd}) and (v_{qi}) which have been computed using Equations (31) and (33), respectively. Fundamental active (v^*_p) and reactive (v^*_q) components of load reference voltage have been shown in subplots (10 and 11) of Figure 4. Finally, the load reference voltage (v^*_L) computed using Equation (36) and the actual sensed load voltage (v_L) have been presented in subplots (12 and 13) of Figure 4(a) for comparison. The generated error between reference and actual load voltage is passed through a high-speed PWM pulse generator as shown in Figure 2 to get gate pulses for three single-phase VSCs.

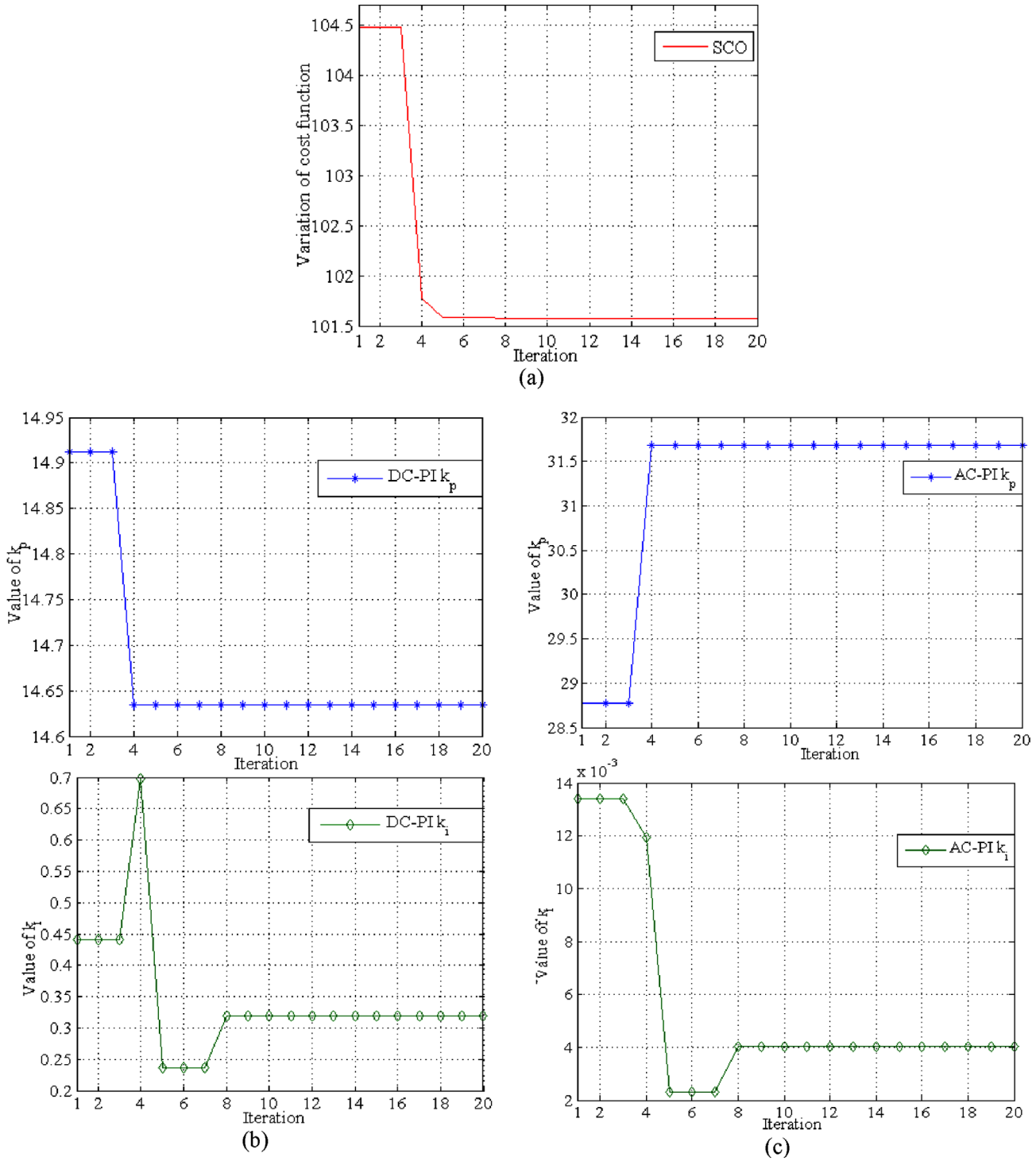


FIGURE 3 (a) Convergence curve of SCO algorithm while tuning PI controllers. (b) Variation in value of PI gains (k_p, k_i) for DC bus. (c)Variation in value of PI gains (k_p, k_i) for AC bus with respect to number of iterations

4.2 | Voltage disturbance compensation capability of DVR using VFP-LMS based algorithm

Figure 4(b) shows the overall performance analysis of DVR in presence of the mentioned issues in supply voltage. The gate pulses generated using VFP-LMS based control algorithm have been produced and given to the VSC, and the DVR performance has been evaluated during different type's disturbances and is presented in Figure 4(a). The subplot (1) of Figure 4(b) depicts the supply voltage (v_s) having voltage sag, swell, distortions, and unbalances in it. Subplots (2–4) of Figure 4(b) show

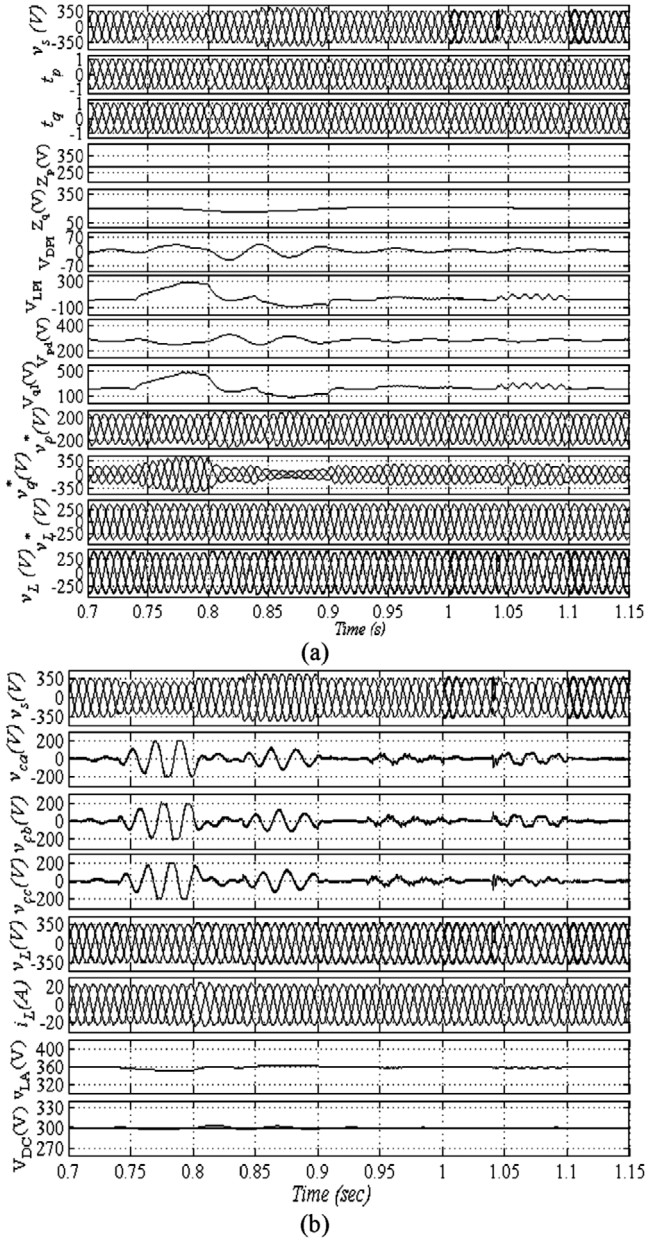


FIGURE 4 (a) Load reference voltage generation using VFP-LMS based control algorithm. (b) Overall performance of DVR with VFP-LMS based control algorithm

three-phase compensated voltages (v_{ca}), (v_{cb}), and (v_{cc}), respectively. From the compensated voltages, it can be understood that during normal time, DVR is not supplying any voltage to the line and it is idle. After compensating these disturbances in voltage, the potential difference at load (v_L) can be seen remaining constant, as shown in subplot (5) of Figure 4(b). As the load considered for protection is linear type, the three-phase load currents (i_L) can be seen without any effect of disturbances on it, as shown in subplot (6) of Figure 4(b). Subplots (7 and 8) of Figure 4(b) represent the load terminal voltage (V_{LA}) and DC-bus voltage (V_{DC}). From load terminal voltage (V_{LA}) and DC-bus voltage (V_{DC}), it can be clearly seen that, both were maintained at their reference level with small variations during the supply dynamics. From Figure 4(b), it has been concluded that, DVR with VFP-LMS based control algorithm is able to compensate the above-discussed voltage disturbances in the supply voltage and maintain the load voltage at desired constant level.

TABLE 1 Time response of DVR with different controls

Sr.No.	Control algorithm	Time taken to compensate (s)
1.	ADALINE *with learning rate* (μ) = *0.45*	*0.03 s (1.5 cycle)*
2.	ADALINE *with learning rate* (μ) = *0.6*	*> 0.04 s (> 2 cycles)*
3.	VFP-LMS *based control algorithm*	*(< 1/2th of cycle)*

4.3 | Comparative analysis

The response time of DVR has been identified during the supply voltage unbalances, which can be seen in Figure 5. This figure represents the response of DVR during unbalance voltage compensation using proposed and adaptive neural network (ADALINE) based control algorithm, respectively. In this figure, both supply voltage "v_{sabc}" and load voltage "v_{Labc}" have been shown for clearly observing the response time of DVR for the disturbance. Figure 5(a) shows the response of the DVR during the voltage unbalance in the supply voltage when ADALINE based control algorithm learning rate (μ) equal to 0.45 is used. In this case, DVR took 0.03 s to compensate the supply voltage unbalances.

Figure 5(b) represents the response of the DVR during the voltage unbalance in the supply voltage when ADALINE based control algorithm with learning rate (μ) equal to 0.6 is used. In this case, DVR took more than 0.04 s to compensate the supply voltage unbalances. Similarly, Figure 5(c) shows the response of the DVR during the voltage unbalance in the supply voltage when the proposed control algorithm (VFP-LMS based control algorithm) is used. It is observed that, DVR took less than half cycle time for mitigation of unbalance in supply voltage.

Table 1 shows the time response of DVR using ADALINE control algorithm with different learning rates and the proposed control algorithm for effective compensation of unbalances in the supply system. From this table, it is concluded that DVR using the proposed (VFP-LMS) control algorithm is able to compensate unbalances in the supply voltage within less than half cycle as compared to ADALINE based control algorithm.

4.4 | Harmonics study of DVR during distortions in supply voltage

The harmonics analysis has been done for supply voltage (v_{sa}), load voltage (v_{La}), and load current (i_{La}) of phase '*a*' during the same time when the distortions have been introduced in the supply voltage. The harmonic analysis has been done during steady state by measuring the Total Harmonic

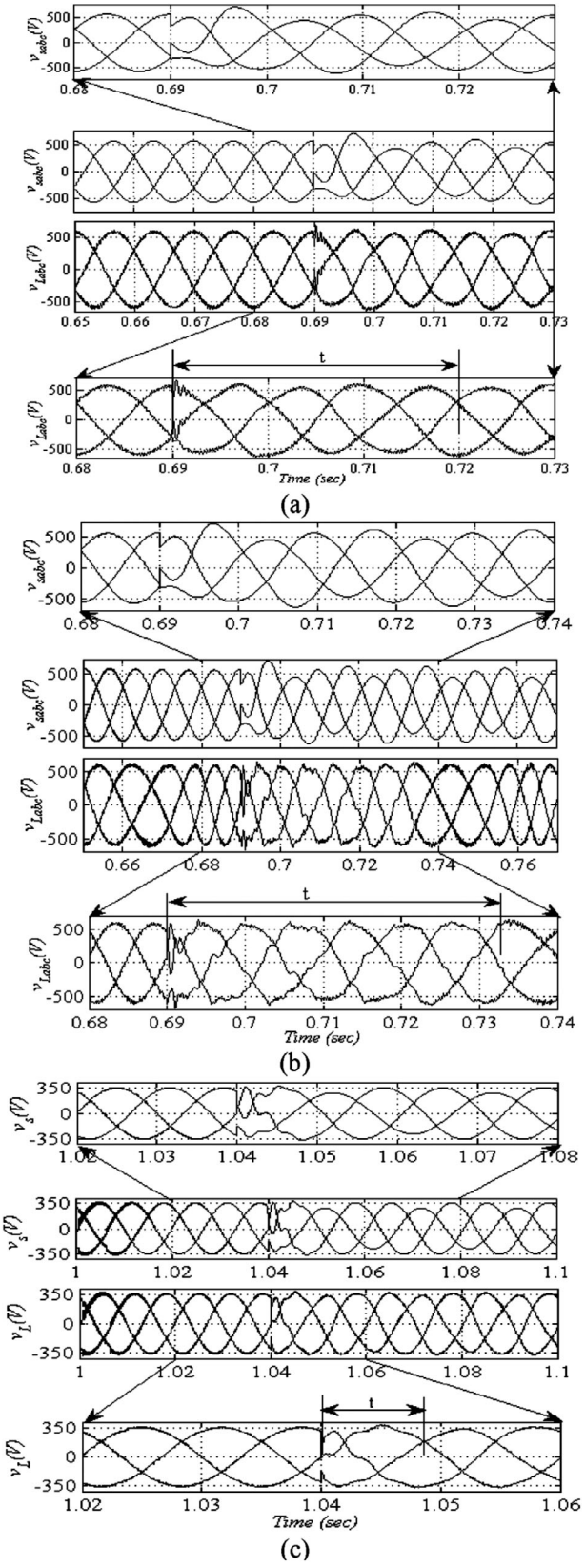


FIGURE 5 Response of DVR in case of unbalanced voltage compensation with (a) basic LMS based control algorithm with constant learning rate (μ) = 0.45, (b) basic LMS based control algorithm with constant learning rate (μ) = 0.6, and (c) VFP-LMS (μ is variable, as well as power fractional) based control algorithm

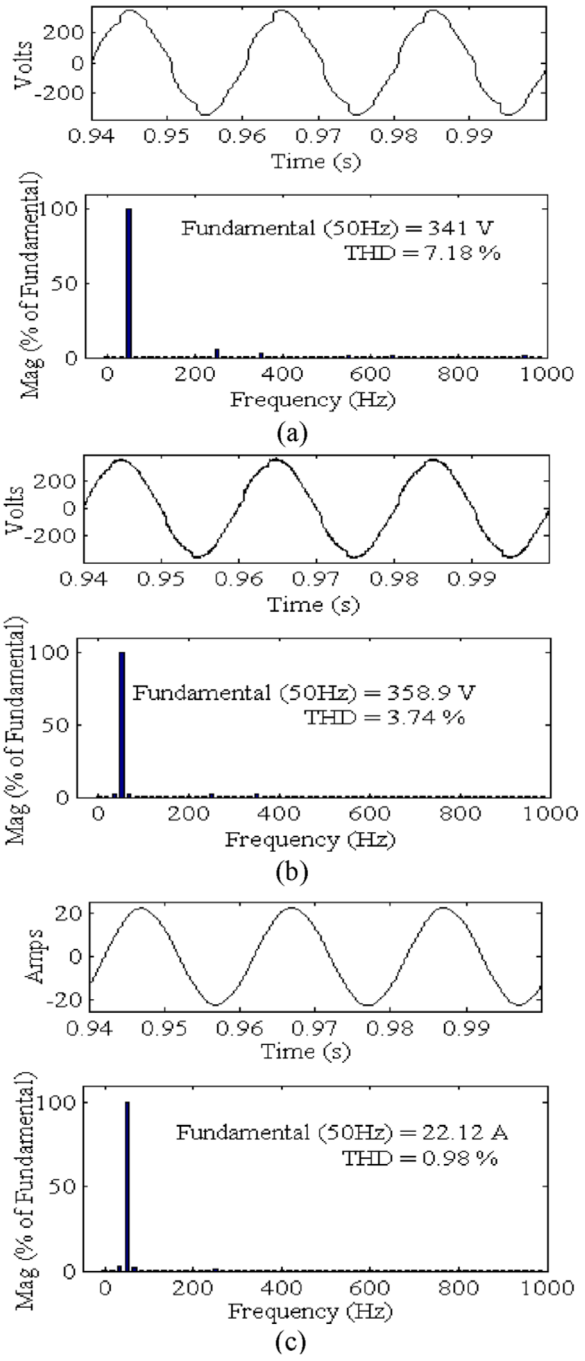


FIGURE 6 Harmonics study of DVR during distortions in supply voltage (a) supply voltage (v_s) of phase 'a' and its THD, (b) load voltage (v_L) of phase 'a' and its THD, and (c) load current (i_L) of phase 'a' and its THD

Distortions (THD) of the waveforms during the distortion. Figure 6(a)–(c) represents the waveforms of supply voltage (v_{sa}), load voltage (v_{La}), and the current flow at phase '*a*' load side (i_{La}), respectively, during distortions and their THD spectrum.

Figure 6(a) shows that the supply voltage (v_{sa}) is having 341 V with 7.18% THD during the distortions in it. After distortions were compensated, the load voltage (v_{La}) can be found to be 358.9 V with 3.74 % THD as shown in Figure 6(b). Figure 6(c) represents the load current (i_{La}) having value of 22.12 A with

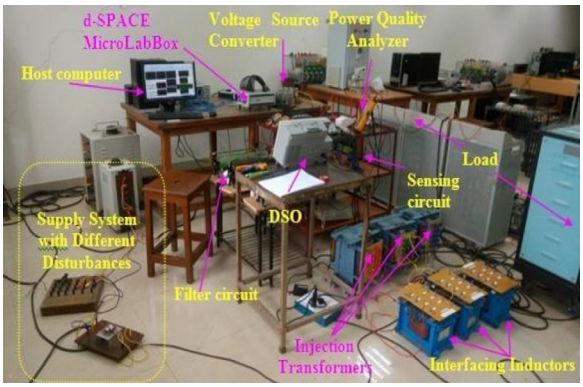


FIGURE 7 Dynamic voltage restorer hardware setup

0.98 % THD as it is linear load. From this figure, it has been concluded that the distortions in load voltage after compensation with VFP-LMS control has come under 5% as per standard limits of IEEE-519-2014.

5 | EXPERIMENTAL STUDY

The proposed control algorithm has also been tested on a scaled down prototype of DVR with d-SPACE made Micro Lab Box processor at the sampling time of 30 μs. The sampling time used for simulation work and experimental work is different due to the limitation of used processors. In experimental work, Micro Lab Box processor NXP (Free scale), QorlQP5020, dual core, 2 GHz is used. Moreover, Intel core i5-3470, 3.2 GHz is used for simulation work in side DELL personal computer. A photograph of the experimental setup is shown in Figure 7. It includes non-ideal AC mains, Micro Lab Box processor, load section, sensing circuits, injection transformer, and voltage source converters. Voltage and current sensors have been made using LEM made LV-25P and LA-55P, respectively.

DVR's dynamic execution in all the cases such as voltage sag, swell, distortions, unbalances in supply voltage has been recorded using a four channel DSO-X-2004A. The performance of DVR in steady state is conducted for unbalance in voltage and distortions in the supply using a Fluke-43B made Power Quality analyzer. This single-phase power quality analyzer is able to capture waveform distortion and transient down to 40 ns and able to catch and save 40 transients up to 20 screens at a time. It is required for fast capturing of power quality disturbances. This instrument includes power quality analyzer, oscilloscope, multi-meter, and recorder within one set. The system parameters used in implementation of DVR as shown in Figure 7 are listed in the Appendix Table A2.

5.1 | Voltage sag and swell compensation with DVR having control algorithm based on VPSLMS

DVR's dynamic execution during voltage sag and swell has been reported in Figure 8. Figure 8(a) shows the sag voltage at supply side supply (v_{sab}), compensated potential difference (v_{ca}), compensated potential difference at load (v_{Lab}), and the phase '*a*' current at the load. Similarly, Figure 8(c) shows the swell voltage at supply side (v_{sab}), compensated potential difference at load (v_{Lab}), and current flow at the load (i_{La}). Figure 8(b) and (d) shows DC-link voltage which remained at 30 V even during the sag and swell in supply voltage, respectively, to support the load voltage.

5.2 | Compensation of distortions and unbalances using DVR with VFP-LMS based control algorithm

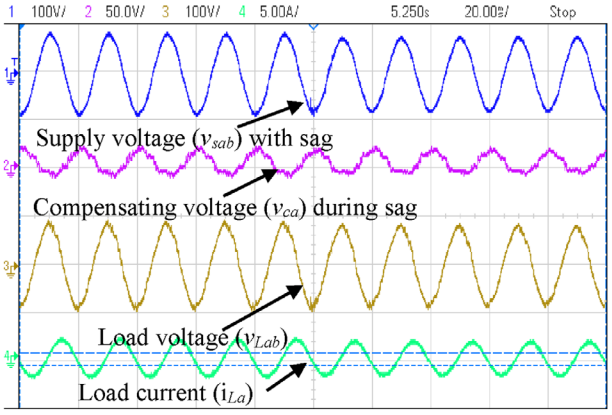
The compensation of distortions and unbalances in supply voltage using DVR can be observed in Figure 9. A level of distortion in the supply system has been injected by connecting a diode rectifier with RC-load at the Point of Common Coupling (PCC) as shown in Figure 7. As a result, distortions are created in the supply voltage up to 7.5 % THD. Figure 9(a) shows the supply voltage (v_{sabc}) which contains the sudden addition of distortions in it and the load current of phase '*a*'. So, after compensation of these distortions, the load voltage can be seen free from distortions in it, as seen in Figure 9(b). The compensation of unbalances in supply voltage using DVR can be seen in Figure 9(c) and (d). Unbalances in the supply voltage have been created by connecting resistive load between two lines at the Point of Common Coupling (PCC). Figure 9(c) shows the supply voltage (v_{sabc}) which contains the sudden change with unbalances in it and the load current. So, after compensation of these unbalances, the load voltage can be seen free from distortions in it, as seen in Figure 9(d). After observing Figures 8 and 9, it is understood that said disturbances in the supply voltage have been compensated using DVR with the proposed control algorithm.

5.3 | Steady state performance of DVR during distortions in supply voltage

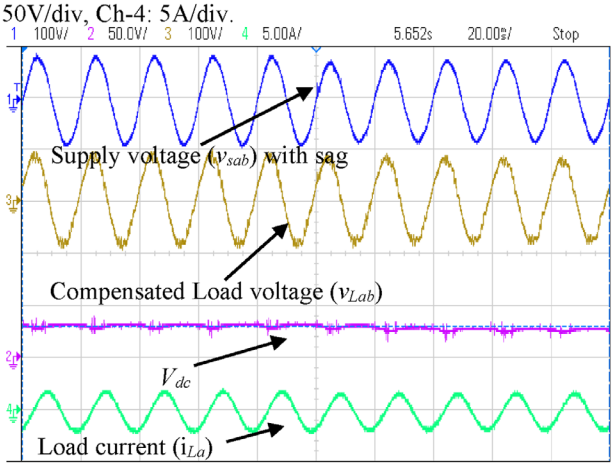
Figure 10 represents the performance of DVR in steady state when the supply voltage is distorted. The supply voltage 'v_{sab}' has voltage magnitude 54.7 V, as shown in Figure 10(a), and their THD is at 7.4 %, as seen in Figure 10(b). However, the load voltage 'v_{Lab}' has voltage magnitude 59.9 V, as shown in Figure 10(c), and its THD at 4.7 %, as seen in Figure 10(d). It is to be noted that steady state results are shown for phase '*a*' only, as other two phases are analogous and found satisfactory. The steady state results shown in these figures ensure that DVR with the proposed control algorithm produced the results with THD under the standard limits. The summarized experimental performance of three single DVR with VFP-LMS based control is given in Table 2 under dynamic and steady state conditions.

6 | CONCLUSION

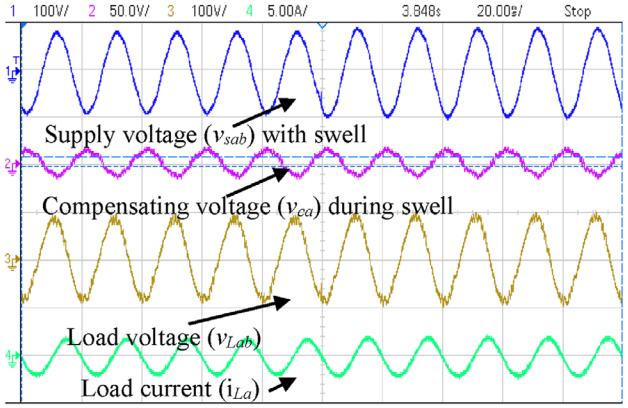
This paper illiustrates the implementation of VFP-LMS control with SCO optimized PI gains for DVR control. The DVR compensation capability has been evaluated during the voltage sag,



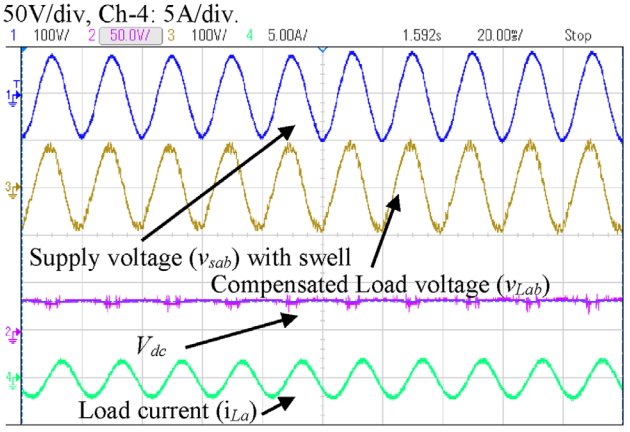
(a) X-axis- 20µ.sec/div, Y-axis Ch-1, 3: 100V/div, Ch-2: 50V/div, Ch-4: 5A/div.



(b) X-axis- 20µ sec/div, Y-axis Ch-1,3: 100V/div, Ch-2: 50V/div, Ch-4: 5A/div.



(c) X-axis- 50µ sec/div, Y-axis Ch-1,3: 100V/div, Ch-2: 50V/div, Ch-4: 5A/div.



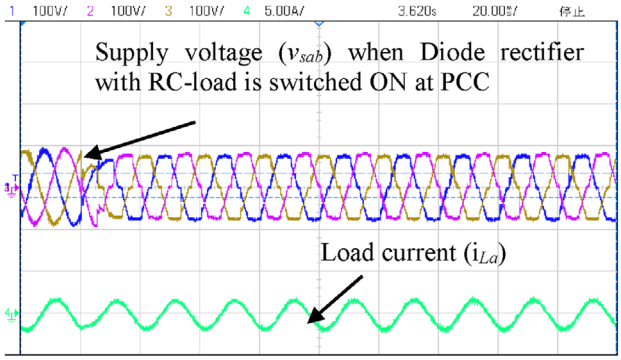
(d) X-axis- 50µ sec/div, Y-axis Ch-1,3: 100V/div, Ch-2: 50V/div, Ch-4: 5A/div.

FIGURE 8 Compensation of voltage sag: (a) Supply voltage (v_{sab}), compensating voltage (v_{ca}), load voltage (v_{Lab}), load current (i_{La}) and (b) supply voltage (v_{sab}), DC-link voltage (V_{dc}), load voltage (v_{Lab}), load current (i_{La}). Voltage swell compensation: (c) Supply voltage (v_{sab}), compensating voltage (v_{ca}),l voltage (v_{Lab}), load current (i_{La}) and (d) supply voltage (v_{sab}), DC-link voltage (V_{dc}), load voltage (v_{Lab}), load current (i_{La})

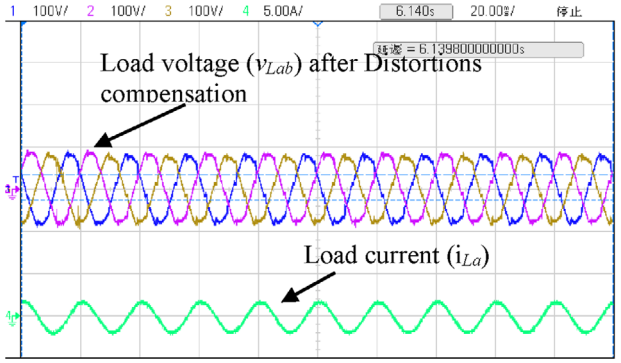
TABLE 2 Test results of DVR with VFP-LMS based control algorithm

Parameter	Dynamic performance				Steady state performance (including % THD)	
	Sag	Swell	Distortions	Unbalance	Distortions	Unbalance
Supply voltage (v_{sab})	54.23 V	66.15 V	55.1 V	54.6 V	55.1 V, 7.4 %	54.6 V, 1.8 %
Supply voltage (v_{sab})	54.10 V	66.54 V	55.4 V	59.6 V	55.4 V, 7.4 %	59.6 V, 1.8 %
Supply voltage (v_{sab})	53.98 V	66.32	54.35 V	54.3 V	54.35 V, 7.5 %	54.3 V, 1.8 %
Load voltage (v_{Lab})	59.8 V	59.9 V	59.6 V	60.3 V	59.6 V, 4.7 %	60.3 V, 4.8 %
Load voltage (v_{Lab})	60.1 V	60.1 V	60.7 V	60.4 V	60.7 V, 4.6 %	60.4 V, 4.8 %
Load voltage (v_{Lab})	60.4 V	60.2 V	60.3 V	59.8 V	60.3 V, 4.8 %	59.8 V, 4.8 %
Load current (i_{La})	1.26 A	1.27 A	1.25 A	1.29 A	1.25 A, 2.7 %	1.29 A, 1.9 %
DC-link (V_{dc})	30 V	30 V	30 V	30 V	30 V	30 V

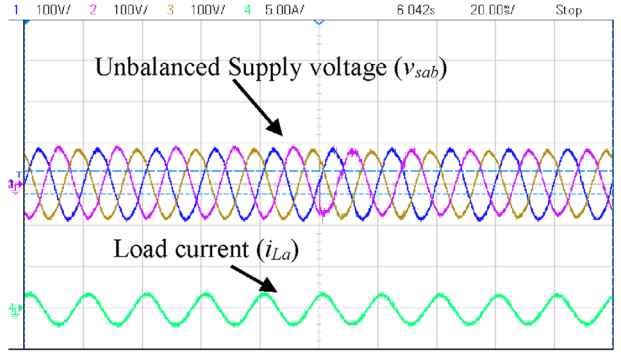
swell, distortions, and imbalances in the supply voltage with the three single-phase VSC based DVR configuration for compensation of mentioned voltage related disturbances. The proposed VFP-LMS control has successfully extracted the fundamental frequency components of non-ideal supplied voltage. Further, extracted fundamental components of AC main are used for generating the load reference voltage. As discussed, implementation of SCO algorithm for PI controllers' gains tuning reduced the computational burden of overall control. The estimated PI controller gains of DC-PI and AC-PI are found to be 14.635,



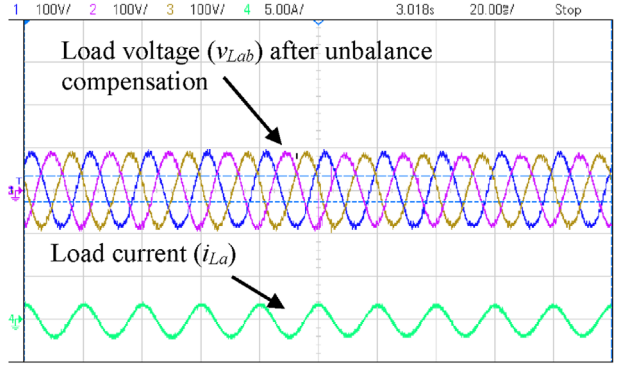
(a) X-axis- 20μ.sec/div, Y-axis Ch-1,2,3: 100V/div, Ch-4: 5A/div.



(b) X-axis- 20 μ.sec/div, Y-axis Ch-1,2,3: 100V/div, Ch-4: 5A/div.



(c) X-axis- 20μ.sec/div, Y-axis Ch-1,2,3: 100V/div, Ch-4: 5A/div.



(d) X-axis- 20μ.sec/div, Y-axis Ch-1,2,3: 100V/div, Ch-4: 5A/div.

FIGURE 9 Voltage distortions compensation: (a) Supply voltage (v_{sabc}) along with load current of phase 'a' (i_{La}) and (b) load voltage (v_{Labc}) after compensation of distortions along with load current (i_{La}). Voltage imbalance compensation: (c) Supply voltage (v_{sabc}) along with load current (i_{La}) and (d) load voltage (v_{Labc}) after in balance compensation along with load current (i_{La})

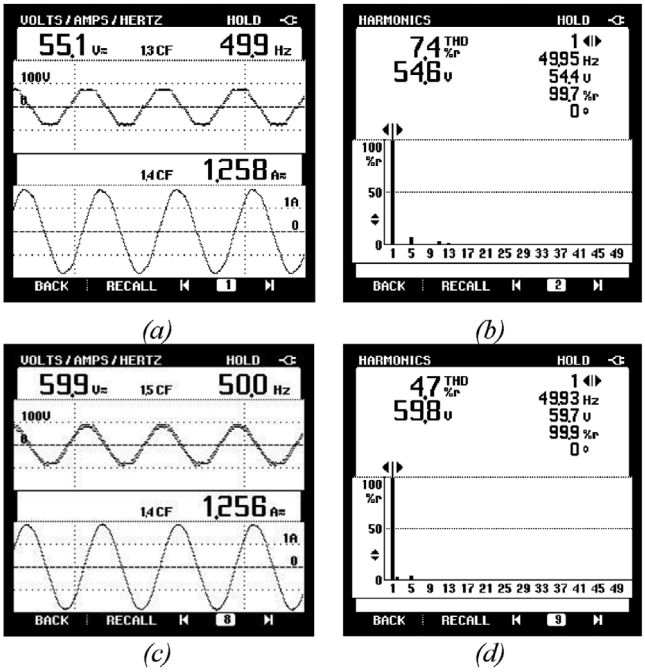


FIGURE 10 Steady state performance during distortions (a) supply voltage (v_{sa}) of phase 'a' (b) THD of (v_{sa}) (c) load voltage (v_{La}) of phase 'a', and (d) THD of (v_{La})

0.3199 and 31.684, 0.004, respectively, at eighth iterations. The dynamic and steady state performance of DVR is evaluated and it is discussed in this paper. The discussed performance has been organized in such a way that the understanding has become simple in the capability of the proposed control algorithm for DVR. The effective time response of DVR has been studied during unbalanced supply, from which it is found that DVR is having the capacity to compensate the unbalances effectively within half of the cycle, as shown in Figure 5. It has been also observed that DVR using VFP-LMS control with optimization-based PI tuning has produced the expected performance in all the cases of voltage disturbances in both simulation and experimental analysis.

List of Symbols

Symbol	Meaning
d	Dimension of variables to be tuned
$J_a()$	Cost function
N	Number of iterations
t	Unit templates
u	Fractional power derivative
Z	Weight update
α, β, γ	Constant parameters
λ, λ_f	Step sizes
Γ	Gamma function

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ORCID

Talada Appala Naidu https://orcid.org/0000-0002-2199-8258

P. Sanjeevikumar https://orcid.org/0000-0003-3212-2750

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APPENDIX

TABLE A1 System data used for simulation work

Sr. No	Parameter	Value
1.	AC grid (non-ideal)	440 V, 50 Hz
2.	Linear inductive Load	10 kVA, 0.8 p.f.
3.	Voltage at DC bus	300 V
4.	Injection transformer ratings	3 kVA, 2:1
5.	Filter (R_F, C_F)	2 Ω, 30 μF
6.	Interfacing inductor (L_i)	1.2 mH
7.	Value of capacitance at DC bus in μF	1200 μF
8.	Switching frequency of three leg voltage source converter	5 kHz
9.	VFP-LMS control algorithm parameters	$\lambda = 0.005$, $\lambda_f = 10e\text{-}6$, $\alpha = 0.9$, $\beta = 0.99$, and $\gamma = 0.5$

TABLE A2 System data used for experimental work

Sr. No	Parameter	Value
1.	AC grid (non-ideal)	60 V, 50 Hz
2.	Load current	1.25 A
3.	Voltage at DC bus	30 V
4.	Injection transformer ratings	4 kVA, 35:35
5.	Filter (R_F, C_F)	12 Ω, 100 μF
6.	Interfacing inductor (L_i)	1 mH
7.	Value of capacitance at DC bus in μF	4700 μF
8.	Sampling time	30 μs