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# Investigations on EMI Mitigation Techniques: Intent to Reduce Grid-Tied PV Inverter Common Mode Current and Voltage

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**Abstract:** Power inverters produce common mode voltage (CMV) and common mode current (CMC) which cause high-frequency electromagnetic interference (EMI) noise, leakage currents in electrical drives application and grid-connected systems, which consequently drops the efficiency of the system considerably. This CMV can be mitigated by designing suitable EMI filters and/or investigating the effects of different modulation strategies. In this paper, the effect of various modulation techniques over CMV and CMC are investigated for two-level and three-level inverters. It is observed that the modified third harmonic injection method reduced the CMV and CMC in the system by 60%. This modified pulse width modulation (PWM) technique is employed along with EMI chokes which results in reduced distortion of the system.

**Keywords:** common mode current; common mode voltage; modulation techniques; electromagnetic interference; mitigation; grid connected inverters

## 1. Introduction

The PV-grid connected power inverter is a necessary part of the PV to electrical energy conversion system [1]. The quality of the voltage depends upon three phenomenons of voltage harmonics, voltage dips or swells and flicker [2]. In the present day, the intense use of electrical loads driven by power electronics (e.g., personal computers) has led to a severe increase of current harmonics drawn from the distribution system. These current harmonics, due to the impedance of the network, induce voltage harmonics into the utility. Voltage dips originate from fault currents in the electrical system or inrush currents of electrical motors and transformers [3]. The common mode circuit is formed in between Photo Voltaiacs (PVs) and the grid, as well as ground due to parasitic capacitance and deficiencies in galvanic isolation between the grid and PVs [1,4]. Electromagnetic interference (EMI) is the main source of unexpected transition at the output port of variable frequency drive (VFD). The fall time and rise time of semiconductor devices (employed in the converter section of VFD) are used to determine voltage transition times. These voltage transition times are around 100ns which is very fast. As a result, high *dv/dt* occurs. In the stray line to ground cables and capacitor, the magnitude of common mode noise current is higher if *dv/dt* is higher [4]. These noise currents affect the control signals and are the main source of EMI.

The instability and disturbances occur at the supply side due to the utilization of a higher number of power devices and components for energy conversion [5]. Mainly, non-linear devices are

responsible for this instability and disturbances. Due to this, harmonics are introduced in the power system. These harmonics causes EMI-related problems, overheating in the equipment, and damage the devices, etc. Inverter common mode voltage (CMV) and its leakage current are the primary concerns of radiated EMI. Noise with high-frequency components is emitted in the form of electromagnetic energy and may interfere with other components and equipment at the common coupling point [6]. To minimize common currents, commonly used methods are [1] improved power inverter structures with common mode current (CMC) suppression capabilities and advanced pulse width modulation (PWM) schemes [7], and (2) the addition of EMI filters [8] and bridge inverter topology based on DC and AC bypass [9]. It is also notable that the circuitry with fast switching semiconductors produces a very high amount *di/dt* and *dv/dt* and which is one of the reasons for the cause of EMI [10]. Decoupling effect-based configurations with constant CMV [11] and transformerless power converter configurations [12] are proposed to suppress CMC. The CM loop impedance can be increased in order to suppress current in CM loop effectively. In [13], the mid-point of DC and AC side voltage nodes are connected to the proposed new CM internal loop scheme in order to suppress CMC. In [14], a novel modulation scheme is presented to control inverter power switches in order to reduce CMC. In [15], a CM internal loop is formed by employing the RC branch in between the negative bus of DC and output terminals. However, detailed analysis of the CMC and its effect on CMC high-frequency components are not presented. In [16], a new scheme based on a dual CM internal loop for a PV grid-connected transformer-less system is proposed to suppress CMC high-frequency components. In [17] characteristics and analysis of the CMV based on the simplified modelling of a cascaded H-bridge power transformer and PWM strategy are presented under the fault grid condition and balanced condition. In [18], in order to reduce CM leakage current, a new hybrid modulation strategy is suggested. The suggested method is efficient and has reactive power provision with low distortion in the current. Filters at the input/output terminal are employed to suppress this unwanted emission or electromagnetic interference (EMI) [19,20]. Generally, filters are employed at the connector of power supply in order to restrict disturbance signals [21,22]. Generally, classical filters are designed by utilizing passive components, i.e., inductor and capacitor values to attenuate high-frequency voltage and current components [23,24]. However, the performance of the filter is dependent on the value of L and C and has limited achievable insertion loss that should be improved to meet the necessary condition. Moreover, passive filters are bulky, costly, and their volume mainly depends on the inductor size which is approximately directly proportional to the required attenuation. Moreover, there is always uncertainty in parasitic components. In order to reduce CMV and current effect, active [25] and passive filters [26] are suggested. However, these filters increase the size, cost of the system, and control of the equipment. As a result, it is good to advance control strategies in order to reduce the CMV's effect. In order to eliminate or reduce CMV, numerous control schemes are proposed based on the modulation strategy, such as the Sine PWM for three-level neutral point clamped (NPC) inverter [27], PWM based on non-nearest vectors, Space Vector PWM for high-level inverters [28,29], etc. In [30], a detailed comparison of SPWM and SVPWM techniques are presented for the three-phase inverter. Nevertheless, similar PWM schemes presented in [31,32] are restricted to 3–5 levels inverters. Synchronous reference frame and feedforward reference frame-based dynamic voltage restorer comparative study are presented in [33]. In [34], a new SVPWM scheme is presented with advanced features, such as the proposed scheme, which is suitable for inverters with any number of levels, zero CMVs can be achieved at any modulation index, the simple realization of CMV vectors, fast control scheme, etc. In [35], a new methodology called the spread spectrum (SS) technique is presented in order to reduce EMI of power converters over a wide range of frequency. However, this SS technique is competent to reduce EMI levels around 5–10 dB [36]. Based on the output voltage waveform and its alignment, another technique is suggested in [37,38]. However, this methodology has a specific application. In [39], a new technique based on software is presented to reduce EMI. The methodology is suitable for single- and three-phase power inverters. In [40], analysis on the CM EMI and methodology to mitigate EMI in power inverters is discussed by using a delay compensation

technique. In order to mitigate EMI, numerous passive filter methods are proposed based on the phases of the noise signal. In [41], a common mode-coupled inductor is designed in order to mitigate common mode noise. Nevertheless, differential mode noise is not able to be reduced by using this technique. Hence, later, a new method based on an integrated choke is presented in order to reduce differential, as well as common mode, noise at the same time [42].

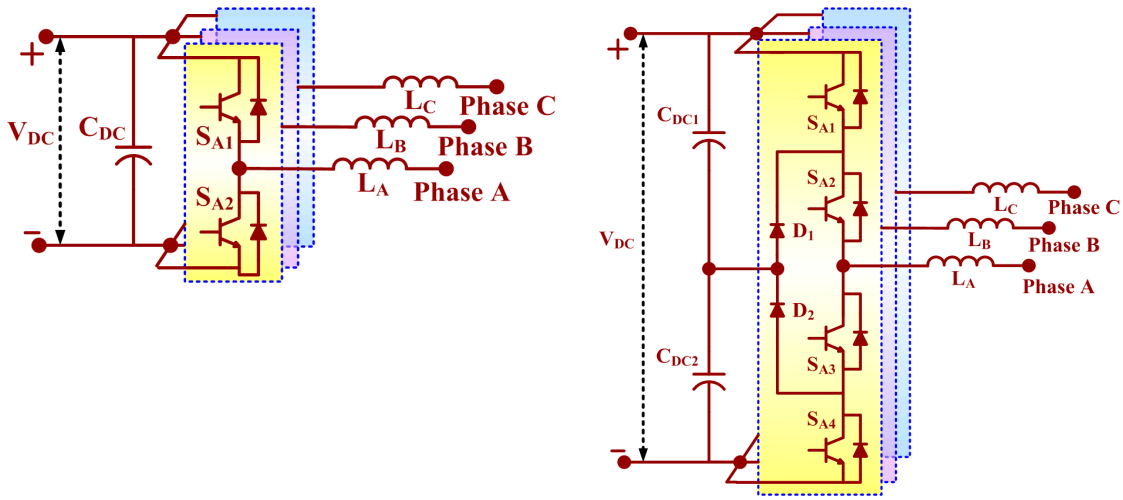
In [43], a new method based on the parasitic component's determination is presented in order to predict EMI noise. In [44,45], computer-based three-dimensional modelling is presented for the noise current prediction by determining the value of parasitic components. A novel EMI filter is discussed with sufficient attenuation with a limited LC value in order to CM EMI [46]. Nevertheless, filters are additional components and increase the volume and cost of the system. Moreover, the implementation of the effective filter is important and the effort for the mitigation of EMI without knowing the system may degrade the performance and require additional cost. To reduce CM voltage, a new impedance balancing method is presented instead of impedance mismatching [47]. The three-phase phase-lock-loop for a distorted utility is discussed in [48]. In [49], controllable devices are used and active filters are presented to suppress CMC generated by the CMV method, called the active noise cancellation scheme, in order to mitigate the noise signal [50]. In [51], a new wavelet transform-based technique to mitigate EMI noise in power converter is presented with a frequency band of 3–30 MHz.

In this paper, EMI mitigation techniques are investigated with the aim to reduce CMV and CMC in a PV-grid tied power inverter. The effect of modulation techniques over CMV and CMC are investigated for two-level and three-level inverters to observe the mitigation of EMI. The modified third harmonic injection method reduced the CMV and CMC by 60% in the system. In order to reduce distortion and to improve the overall efficiency of the system, the modified PWM technique is employed along with EMI chokes.

The article is organized in the seven sections, discussing explicitly the important aspects for investigations and design of EMI filters for the mitigation of CMC and CMV in grid-tied inverter system. In Section 2, the modulation techniques for high power two-level and three-level inverters, are discussed in brief. Section 3 explains the concept of CMV of the inverters and design of filters or EMI chokes. Section 3 also deals with the comparative study of space vector-based and sine-based pulse width modulation (SVPWM and SPWM) techniques. A modified PWM strategy is discussed in Section 4. The results obtained through simulation and experimental works are presented in Section 5. Finally, the conclusion is given in Section 6.

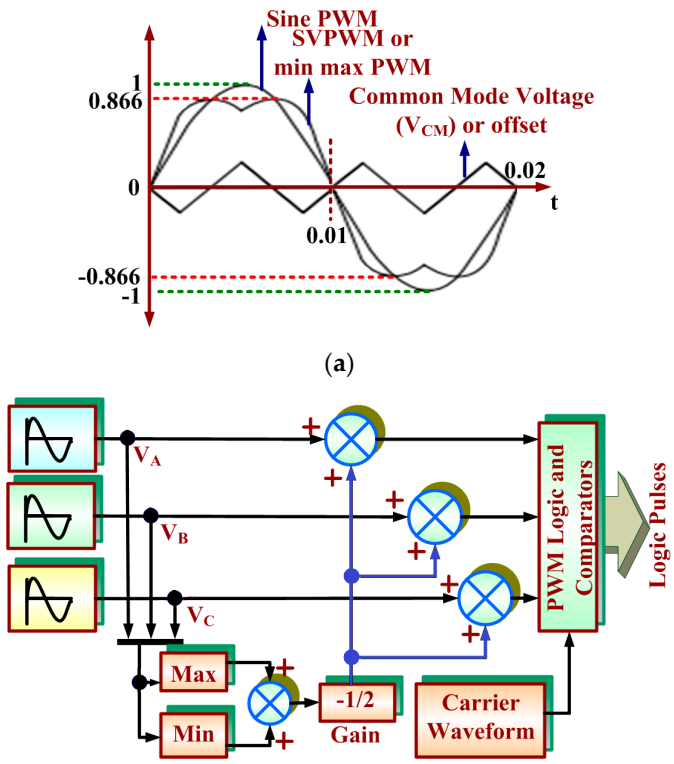
## 2. Modulation Techniques for High-Power Inverters

Space vector-based and sine wave-based PWM techniques are the common techniques used to generate pulses for the switches of the inverter [29,30]. In the SPWM technique, high-frequency triangular carrier waves (typically several kHz) are compared with the modulating signal (50 Hz or 60 Hz) to generate pulses for a three-phase inverter. In the SVPWM technique, instead of modulating signals, a rotating vector reference is used to generate pulses of the inverter [29,30]. The prime objective of this control and pulse generation scheme is to generate a sinusoidal AC output whose magnitude is limited. The PWM switching scheme not only helps to achieve reduced Total Harmonic Distortion (THD), better harmonic spectrum, and maximum utilization of DC bus but also provides a solution to reduce EMI, switching loss. Figure 1 depicts the power circuitry of three-phase two-level inverter and neutral point clamped (NPC) three-level inverters [21] and its PWM strategies shown in Figures 2–5.




(**a**) (**b**)

**Figure 1.** Power circuitries of (**a**) three-phase two-level inverter, and (**b**) neutral point clamped (NPC) three-level inverter.




(**a**)

(**b**)

**Figure 2.** Reference generation through Min–Max modulation strategy (**a**) associate waveform, and (**b**) mathematical model.

The Min–Max modulation strategy is supposed to be equivalent to the space vector modulation strategy. Thus, using this approach, the modulation index can be extended up to 1.15. Figure 2a,b explains the associated waveforms and mathematical model of the reference waveform generation technique through Min–Max modulation strategy, respectively [48]:

$$offset\ in\ (\mathrm{V}) = -\left[\frac{\max(V_A, V_B, V_C) + \min(V_A, V_B, V_C)}{2}\right] \tag{1}$$

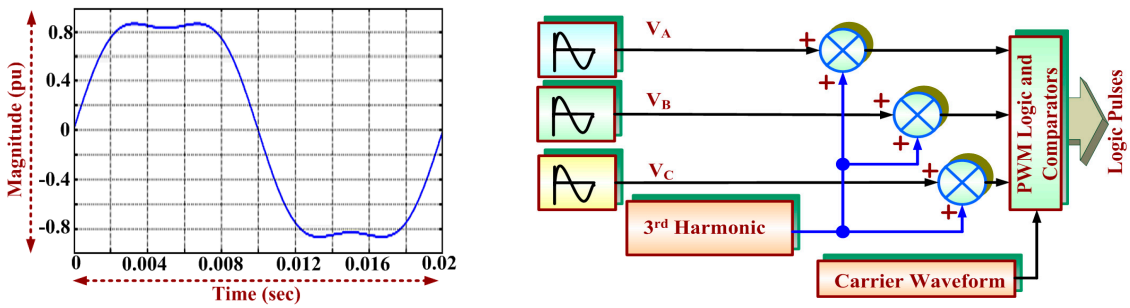
where:

$$\begin{cases} V_A = V_m \cos(\omega t) \\ V_B = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_C = V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \tag{2}$$

$$V_{ref} = V_A + V_B + V_C + offset \tag{3}$$

The reference modulating signals are mathematically defined as follows:

$$\begin{cases} V_{Am} = V_m \cos(\omega t) + offset \\ V_{Bm} = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) + offset \\ V_{Cm} = V_m \cos\left(\omega t + \frac{2\pi}{3}\right) + offset \end{cases} \tag{4}$$




(**a**) (**b**)

**Figure 3.** Modulating signal of third harmonic injection control technique (**a**) modulating signal, and (**b**) mathematical model.

In the third harmonic injection method [52,53], the third harmonic is injected in a modulation scheme to improve the gain of the pulse width modulator in the inverter. Figure 3a,b shows the third harmonic injection modulating signal control reference waveform and mathematical model, respectively.

The reference modulating signals are mathematically defined as follows:

$$\begin{cases} V_{Am} = V_m \cos(\omega t) + V_{m3} \cos(3\omega t) \\ V_{Bm} = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) + V_{m3} \cos(3\omega t) \\ V_{Cm} = V_m \cos\left(\omega t + \frac{2\pi}{3}\right) + V_{m3} \cos(3\omega t) \end{cases} \tag{5}$$

In this technique, approximately 17% of third harmonics components are added in the reference waveform of classical SPWM [29,30,34]. The reference waveform of the method third harmonics injection can be also expressed as follows:

$$f(\omega t) = (1.15 M_a \times \sin(\omega t) + 0.19 M_a \times \sin(\omega t)),\ 0 \le \omega t \le 2\pi \tag{6}$$

where $M_a$ is the modulation index ratio.

## 3. Common Mode Voltage

The inverter common mode voltage is calculated by averaging the output voltage ($V_A$, $V_B$, and $V_C$) of each leg as follows [38]:

$$V_{CM} = \frac{V_A + V_B + V_C}{3} \tag{7}$$

For the three-phase two-level inverter, the achievable phase output voltage levels could be $-V_{DC}/2$ or $+V_{DC}/2$ where $V_{DC}$ is input voltage. If the voltage at the DC link is zero then only the common mode voltage is zero. For the three-level inverter, the achievable phase output voltage levels could be

positive, negative, and neutral point voltage. Tables 1 and 2 tabulated the output vectors and possible common mode voltages for two-level and three-level inverters, respectively.

**Table 1.** Output vectors and common-mode voltages for two-level inverter.

| Output Vector ($V_A$, $V_B$, $V_C$) | CMV ($V_{CM}$) |
|---|---|
| (+ + +) | $(1/2) \times V_{DC}$ |
| (+ + −), (+ − +), (− + +) | $(1/6) \times V_{DC}$ |
| (+ − −), (− + −), (− − +) | $-(1/6) \times V_{DC}$ |
| (− − −) | $-(1/2) \times V_{DC}$ |
| (+ + +) | $(1/2) \times V_{DC}$ |
| (+ + −), (+ − +), (− + +) | $(1/6) \times V_{DC}$ |

**Table 2.** Output vectors and common-mode voltages for three-level NPC inverter.

| Output Vector ($V_A$, $V_B$, $V_C$) | CMV ($V_{CM}$) |
|---|---|
| (+ + +) | $(1/2) \times V_{DC}$ |
| (+ + 0), (+ 0 +),(0 + +) | $(1/3) \times V_{DC}$ |
| (+ + −), (+ − +), (− + +), (+ 0 0), (0 + 0), (0 0 +) | $(1/6) \times V_{DC}$ |
| (+ - 0), (+ 0 −), (− + 0), (0 + −), (− + 0), (0 − +), (0 0 0) | *0* |
| (+ − −), (− + −), (− − +), (− 0 0), (0 − 0), (0 0 −) | $-(1/6) \times V_{DC}$ |
| (− − 0), (− 0 −), (0 − −) | $-(1/3) \times V_{DC}$ |
| (− − −) | $-(1/2) \times V_{DC}$ |

### *3.1. Filtering of Common Mode Voltage*

The appropriate designed filter circuitry is needed to reduce the common mode voltage. The complete three-phase to grid (AC–DC–AC) system with the connection of a passive filter is shown in Figure 4. The DC link with voltage $V_D$ is created between the AC–DC and DC–AC converter and passive filters are added at the input and output side. The filter consists of damping resistance, Y-connected capacitor and common mode chokes. In the given system, a damping resistor $R_{CM2}$ is connected between grid and neutral point capacitor. Additionally, two chokes, $L_{CM1}$ and $L_{CM2}$, and three Y-connected capacitors, $C_{CM2}$, are connected for filter purposes [12–14]. $R_{CM1}$ and $C_{CM1}$ are connected between the grid and negative terminal of the DC link. The range of the resonant frequency for the common mode circuitry is about 1.5 kHz [7] and is calculated as follows:

$$f_o = 1/\left(2\pi\sqrt{L_{CM} \times C_{CM}}\right) \tag{8}$$

where $L_{CM}$ and $C_{CM}$ are the equivalent inductance and capacitance values. The practical limitation of the real-time application needs to be considered while designing the capacitors. The capacitor size should be small for the designed frequency in order to reduce the bulkiness of the hardware unit.

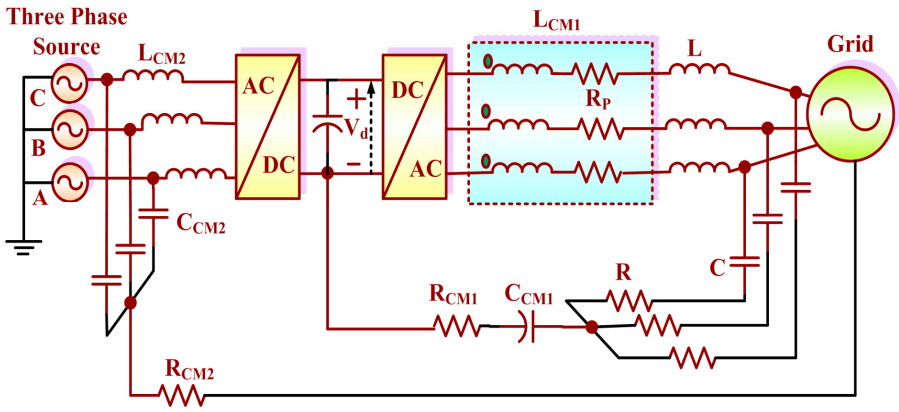



**Figure 4.** Complete three-phase to grid (AC–DC–AC) system with the connection of a passive filter.

### *3.2. Comparison of SPWM and Space Vector PWM Techniques for a Two-Level Inverter at a Higher Switching Frequency*

The simple open-loop analysis is carried out for a two-level inverter for current and voltage distortions both with and without a filter. For the analysis, the modulation index is maintained at 0.8 and taken over a range of frequencies between 1 kHz and 150 kHz and the obtained results are tabulated in Table 3. After comparing SPWM and SVPWM results, it is known that SVPWM provides superior results for two-level inverter system. For reduction in CMV, the SVPWM technique provides the best results; however, due to tedious calculations, the requirement of high-end processors and complex hardware implementation, space vector modulation can be replaced with the carrier-based modulation strategy which will give the same results as that of the space vector modulation technique. If the reduction in the CMC can be achieved by using such a modulation strategy, the size of the common mode choke can be reduced.

**Table 3.** THD comparison of SPWM and SVPWMM techniques.

| Switching Technique | Switching Frequency | Without Filter (THD%) | | With Filter (THD%) | |
|---|---|---|---|---|---|
| | | Line Current (A) | Line Voltage (V) | Line Current (A) | Line Voltage (V) |
| SPWM | 1 kHz | 64.81 | 138.2 | 2.53 | 6.88 |
| | 10 kHz | 24.9 | 88.46 | 1.04 | 4.16 |
| | 50 kHz | 24.27 | 67.92 | 1.03 | 4.12 |
| | 100 kHz | 24.27 | 67.92 | 1.03 | 4.12 |
| | 120 kHz | 31.39 | 106.82 | 3.86 | 5.63 |
| | 150 kHz | 43.95 | 301.92 | 7.42 | 7.89 |
| SVPWM | 1 kHz | 4.82 | 52.84 | 0.14 | 0.66 |
| | 10 kHz | 3.15 | 43.89 | 0.11 | 0.42 |
| | 50 kHz | 3.15 | 43.89 | 0.11 | 0.43 |
| | 100 kHz | 8.74 | 31.84 | 0.36 | 1.47 |
| | 150 kHz | 5.75 | 56.33 | 0.45 | 1.03 |

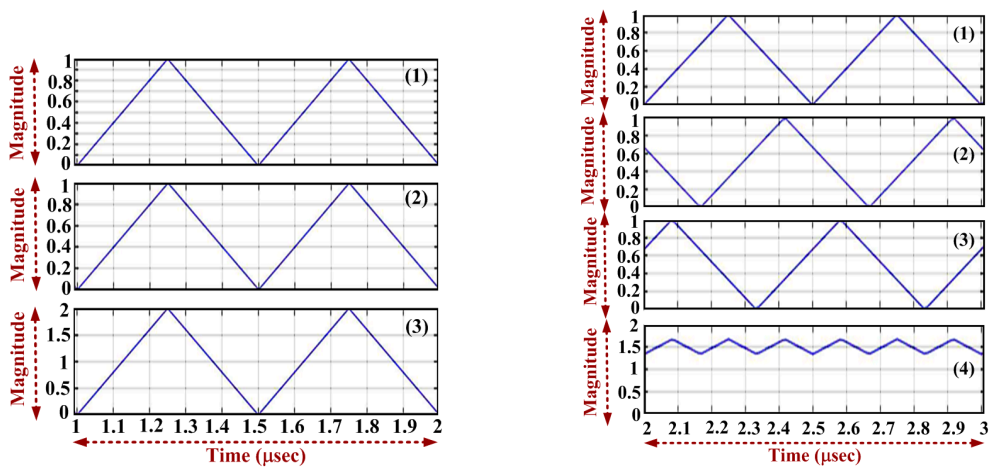
## 4. Modified PWM Schemes

Among discussed PWM schemes, SVPWM provides quality results [30]. Nevertheless, due to some inherent disadvantages, the space vector modulation strategy is ruled out from the agenda. Thus. the next challenge was to obtain similar results, which were given by the space vector modulation, in carrier-based modulation as well. The modified carrier phase shift scheme is developed based on the concept of phase disposition PWM scheme. It is given that the input voltage is balanced and the possible two conditions are:

- One input phase voltage is negative and two input phase voltage is positive.
- One input phase voltage is positive and two input phase voltage is positive.

$$V_A + V_B + V_C = 1 \tag{9}$$

It is considered that $0 < V_A$, $0 > V_B$, and $0 > V_C$ and CMV are caused with the peak value to reach a higher voltage level than $1/6 \times V_{DC}$. The carrier signals and output voltage reference relation for the switching 0–1–1 is as follows:




(**a**) (**b**)

**Figure 5.** Waveform associated with PWM strategies (**a**) PDPWM method, max amplitude of the addition of the carrier waves is 2, (**b**) modified PWM method, max. amplitude of the addition of the carrier waves is around 1.5.

As phase disposition PWM (PDPWM) is used, at any point of time:

$$for\ the\ state\ '0-1-1' \begin{cases} V_{CarrierA} - V_{CarrierB} = 1 \\ 3 \times V_{CarrierA} - 2 > 0 \end{cases} \tag{10}$$

Hence, to avoid this state,$3 \times V_{CarrierA} - 2 < 0$, this condition is to be satisfied. This is done by using three carrier waves, which are 120° apart from each other. Figure 5 shows the waveform associated with PWM strategies. Figure 5a depicts the associated waveform of the PDPWM method where the max amplitude of the addition of the carrier waves is 2 (see amplitude in (3) in Figure 5a). Figure 5b depicts the associated waveform of the modified PWM method where the max amplitude of the addition of the carrier waves is around 1.5 (see amplitude in (4) in Figure 5b).

## 5. Simulation and Experimental Results

The simulation results are presented for the complete AC–DC–AC system. The circuit-level model was developed using the Simulink platform. The closed-loop analysis of both two-level and three-level inverters is carried out. The specifications of the system parameters are given in Appendix A.

### *5.1. Closed-Loop Analysis of the Two-Level Inverter*

The model of the system is done in various stages. Figure 6 shows the complete closed-loop AC–DC–AC system Simulink model with the two-level inverter. The first section includes the diode rectifier model to obtain a constant DC voltage. Then the DC link capacitor was designed so as to provide a constant DC input voltage to the three-phase two-level inverter circuit which is modelled using Insulated Gate Bipolar Transistor (IGBTs) and SVPWM techniques were implemented for firing the inverter circuit.

The analysis of CMV and CMC for the given system is done without filter implementation and the achieved results are depicted in Figure 7a–d. The Fast Fourier Transform(FFT) analysis of the CMV and CMC waveform (150 kHz component) are done without filter, and it is observed that THD of the CMV

and CMC is 38.01% and 3152.31%, respectively. The analysis of the common mode voltage and current for the given system are done with a filter implementation and the achieved results are depicted in Figure 7e–h. The FFT analysis of the CMV and CMC waveform (150 kHz component) are done with a filter and it is observed that the THD of the CMV and CMC is 73.39% and 2213.58%, respectively.

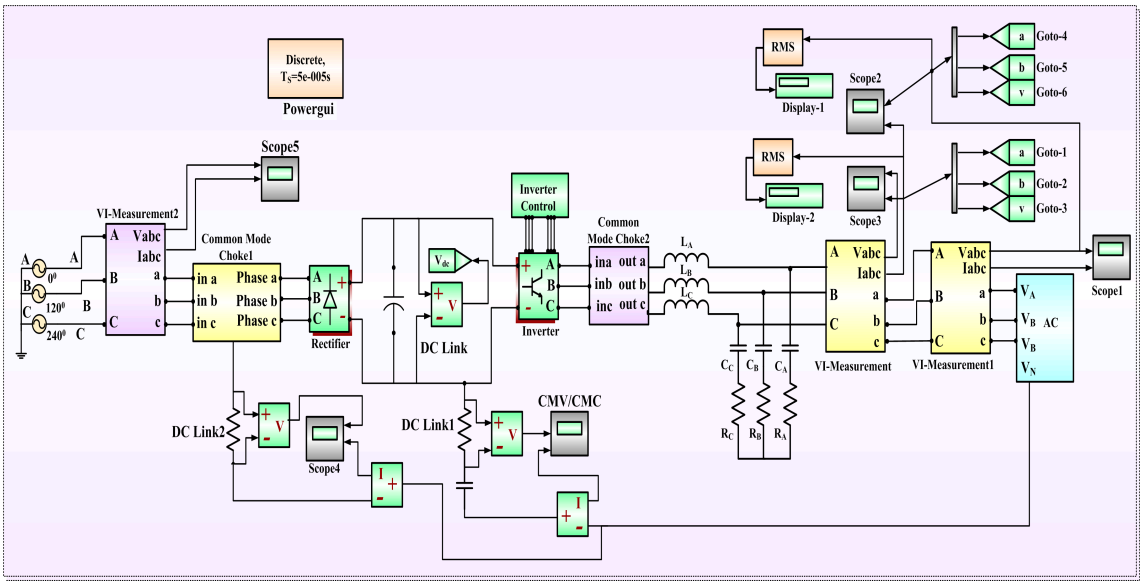



**Figure 6.** Complete closed-loop AC–DC–AC system Simulink model with the two-level inverter.

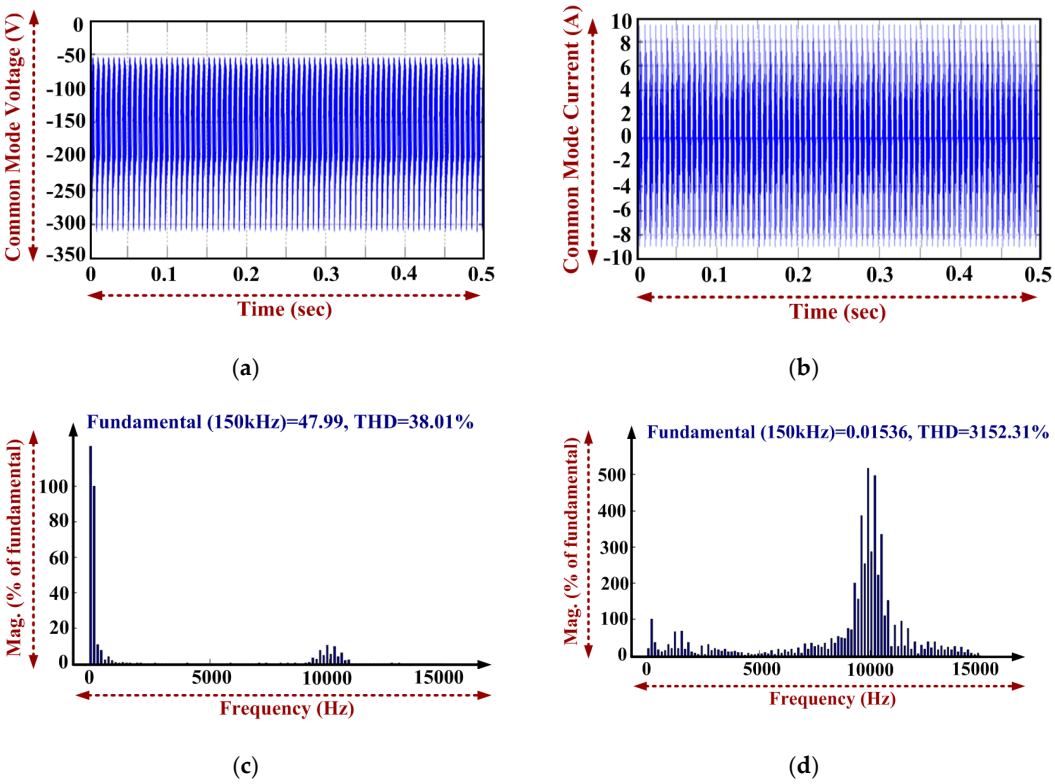



**Figure 7.** *Cont.*

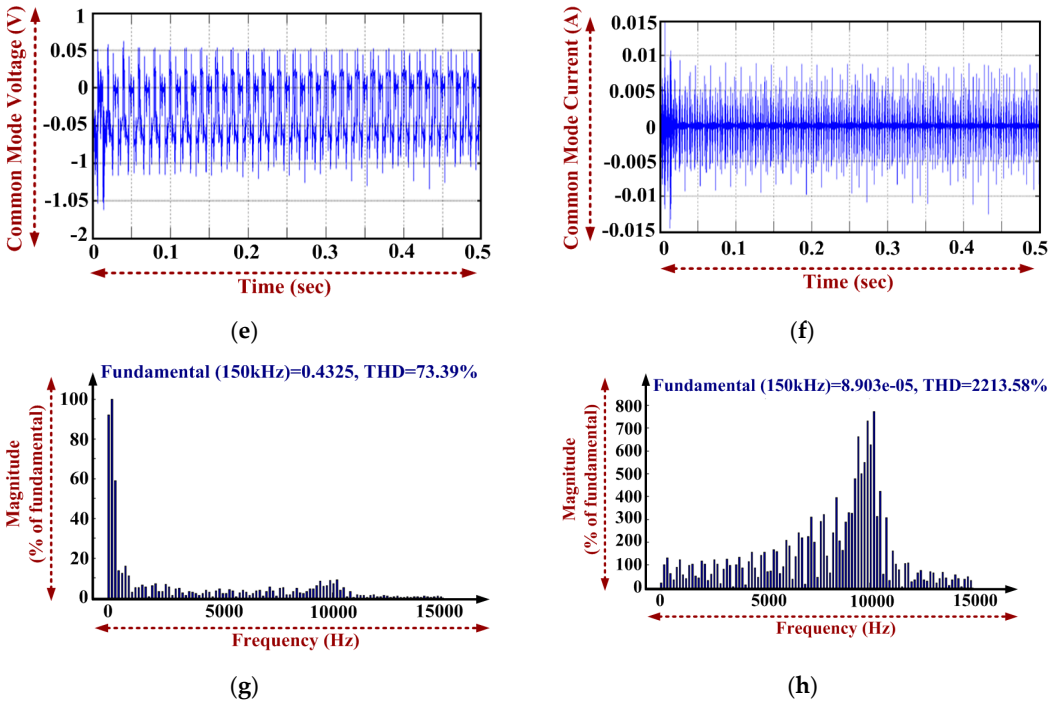



**Figure 7.** Simulation results: (**a**) CMV without filter; (**b**) CMC without filter; (**c**) without filter, common mode voltage FFT analysis; (**d**) without filter, common mode current FFT analysis; (**e**) CMV with filter; (**f**) CMC with filter; (**g**) with filter, common mode voltage FFT analysis; (**h**) with filter, common mode current FFT analysis.

From the investigation, the objective of reducing the CMC and CMV of the two-level inverter is achieved. From the analysis made, it can be concluded that when the two-level inverter is operating at a frequency above 10 kHz, the EMI increases drastically. Additionally, the CMV and CMC of the system cannot be reduced effectively by changing the reference, instead the size of the EMI filters have to be larger. Therefore, we need to consider the three-level inverter analysis.

### *5.2. Closed-Loop Analysis of the Three-Level Inverter*

Based on the earlier explanation, the Simulink model of the three-level NPC system is designed in MATLAB. Figure 8 shows the Simulink model of the designed three-level NPC system.

#### 5.2.1. Existing PWM Method

Using Min–Max and the third harmonic injection method, the common mode current and voltage are investigated for the three-level NPC inverter. Figure 9a–d depicts the waveforms of CMC using existing Min–Max method, CMV using existing Min–Max method, CMC using the existing third harmonic injection methods, and CMV using the existing third harmonic injection method, respectively.

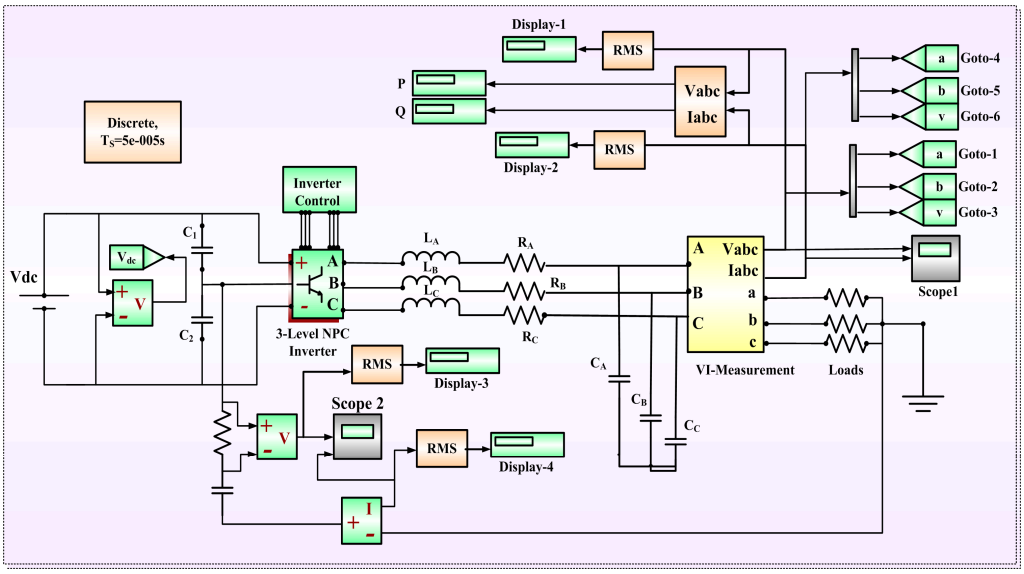



**Figure 8.** Matlab/Simulation model of the three-phase three-level NPC inverter.

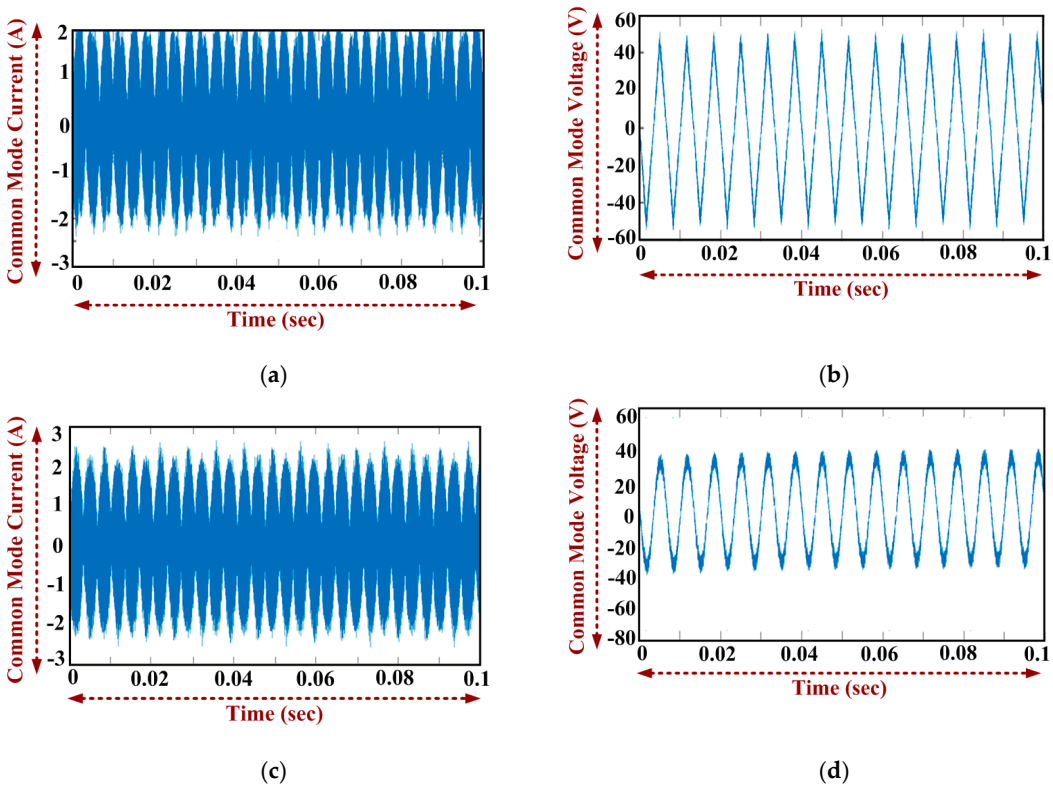



**Figure 9.** Simulation results: (**a**) CMC using existing Min–Max method; (**b**) CMV using existing Min–Max method; (**c**) CMC using the existing third-harmonic injection method; (**d**) CMV using the existing third-harmonic injection method.

The fast Fourier transform (FFT) is conducted for Min–Max and third harmonic injection PWM techniques and it is observed that common mode voltage THD is 14.74% for Min–Max strategy and 11.60% for the third harmonic injection method. In the existing PWM method, the magnitude of the common mode current (rms value) is 1.191 A using the Min–Max and 1.199 A in the case of the third harmonic injection method. This can be reduced further by using Modified PWM Technique.

### 5.2.2. Modified PWM Method

The simulation results for the modified Min–Max method and third harmonic injection methods as applied in the three-level NPC inverter. Figure 10a–d obtained waveform of CMC using modified Min–Max method, waveform CMV using modified Min–Max method, waveform of CMC using modified third harmonic injection methods, and waveform of CMV using modified third harmonic injection methods, respectively. Figure 10e,f show the FFT analysis of CMV and CMC with filter, respectively. It is observed that the THD of the CMV and CMC are 12.95% and 5.91%, respectively. Before modifying the PWM scheme, the common mode voltage and current of the inverter are experimentally investigated and shown in Figure 11a. Without modification, the RMS values of the common mode current and common mode voltage are 1.95 A and 4.73 V, respectively.

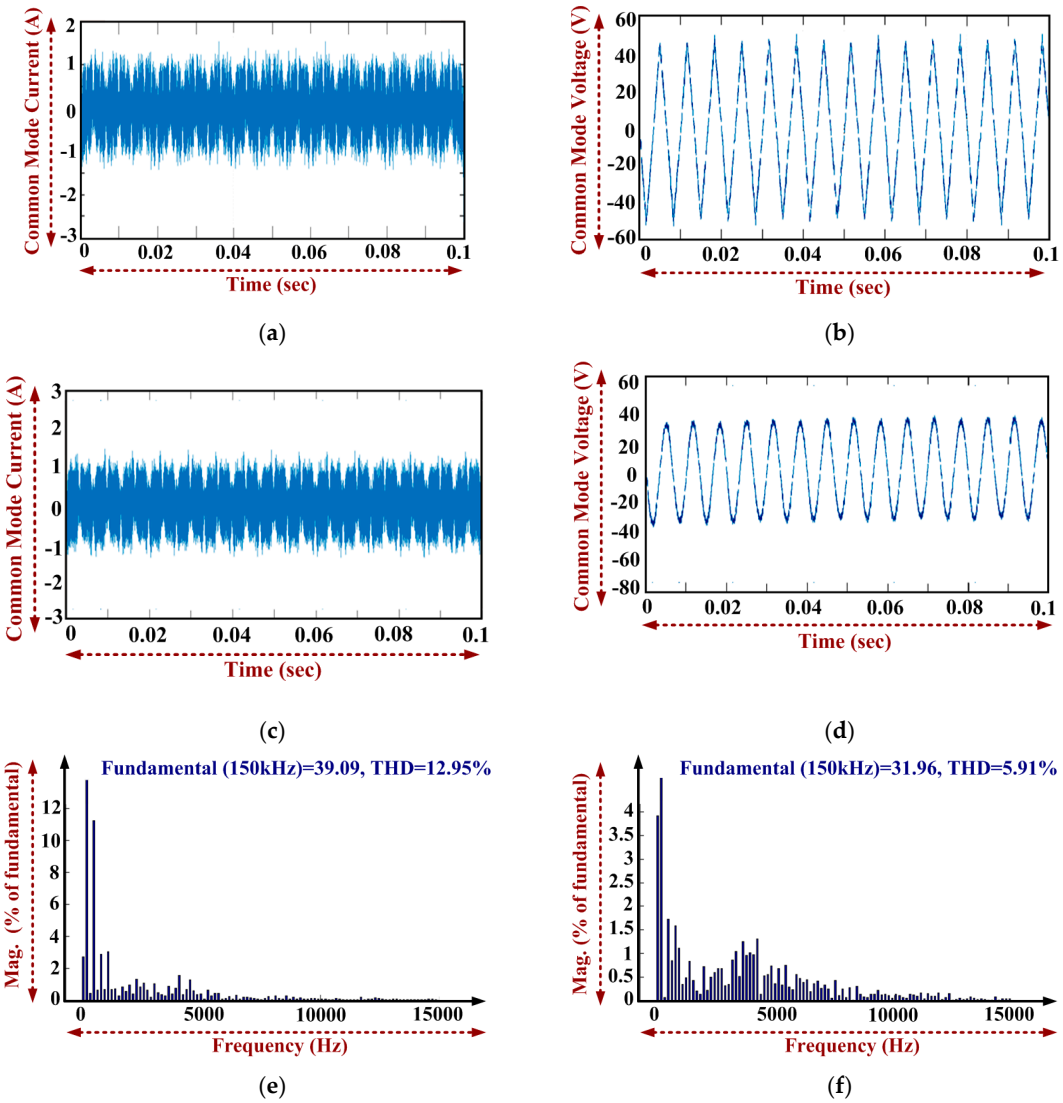
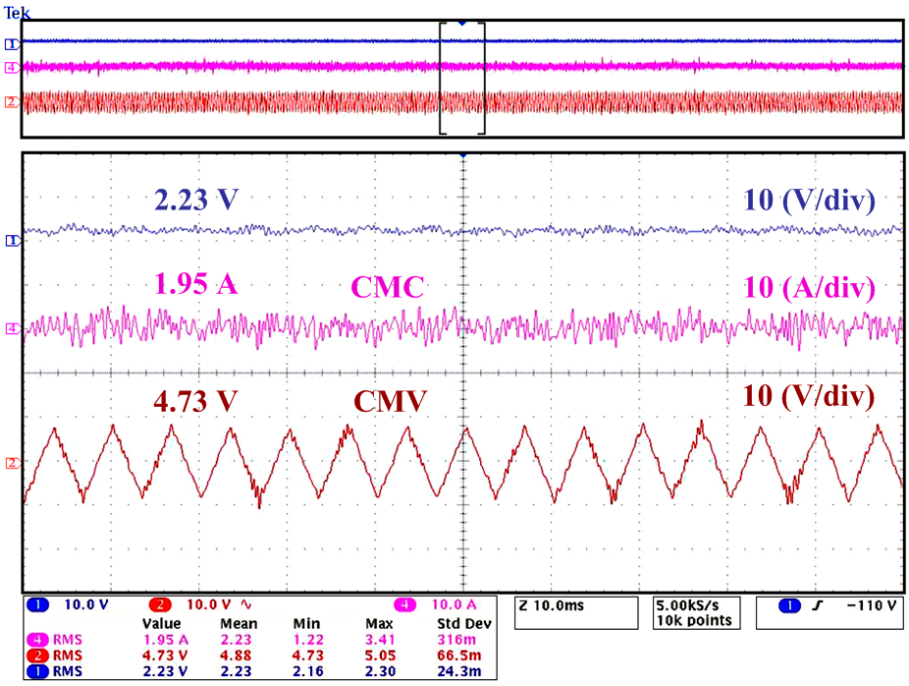
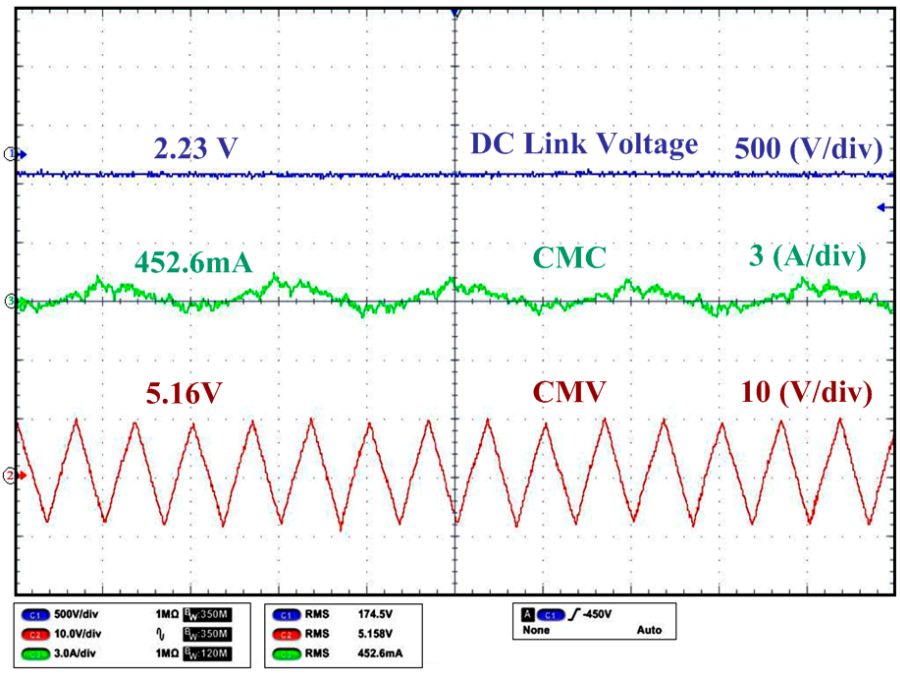



**Figure 10.** Simulation results: (**a**) CMC using the modified Min–Max method; (**b**) CMV using the modified Min–Max method; (**c**) CMC using the modified third-harmonic injection method; (**d**) CMV using the modified third-harmonic injection method; (**e**) with filter, common mode voltage FFT analysis; (**f**) with filter, common mode current FFT analysis.




(**a**)




(**b**)

**Figure 11.** Experimental results: common mode current and common mode voltage, (**a**) before modifying the PWM strategy, and (**b**) after modifying the PWM strategy.

After modifying the PWM scheme, the common mode voltage and current of the inverter are experimentally investigated and shown in Figure 11b. After modification, the RMS values of the common mode current and common mode voltage are 452.6 mA and 5.16 V, respectively. In Table 4, the observed results are tabulated and it is clear that, after modifying the PWM method, the common mode current is reduced significantly with a small increment in the common mode voltage.

**Table 4.** Experimental results.

| Experimental Test | CMV (V) | CMC (A) |
|---|---|---|
| Before applying modified PWM | 4.73 V | 1.95 A |
| After applying Modified PWM | 5.16 V | 452.6 mA |

In Table 5, a comparison of PWM strategies for reduction in CMC, CMV, and voltage THD of the three-level inverter is tabulated based on the obtained results. The simulated results show that when the modified PWM method is implemented there is a considerable reduction in CMC. The voltage THD of the system is also observed to be reduced considerably. This satisfies the objective of optimizing the PWM technique to reduce the CMV and current in grid-tied inverters. From the above comparison, it is clear that the modified third harmonic injection approach shows a significant amount of reduction in the CMV and CMC. EMI mitigation techniques are investigated with the aim to reduce the CM voltage and current in PV grid-tied power inverters. The common mode undesirable effects for grid-tied inverter systems has been discussed and compared for different PWM schemes. Two small passive filters are connected between the rectifier input and grid neutral point, and in between the grid and output port of the inverter and tested for a three-phase two-level inverter using a passive cancellation method.

**Table 5.** Comparison of PWM strategies for reduction in the CMC, CMV, and voltage THD of the three-level inverter.

| Modulation Technique | CMV (V) | CMC (A) | Voltage THD (%) |
|---|---|---|---|
| Existing PWM Strategy | | | |
| Min–Max | 34.7 | 1.863 | 14.27 |
| Third Harmonic Injection | 34.7 | 1.863 | 11.5 |
| Modified PWM Strategy | | | |
| Modified Min–Max | 43.31 | 0.74 | 12.95 |
| Modified Third Harmonic Injection | 34.84 | 0.74 | 5.77 |

## 6. Conclusions

In order to reduce distortion in the system, the modified PWM technique is employed along with EMI chokes. Various PWM strategies are analyzed to reduce the CMV and CMC, and a modified PWM approach is presented for a three-phase three-level inverter. The modified third harmonic injection method reduced the CMC by 60% in the system with a tradeoff to CMV. Simulation and experimental results are provided which show good agreement with each other and validate that the control strategies with different PWM techniques are valuable, optimize the output parameters, and are effective in preventing common mode undesirable effects along with and without filters. Hence, it is economic to use modified techniques so that the filter size can be reduced and the final product will be lightweight with a reduced cost compared with conventional strategies and existing PWM techniques.

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## Nomenclature

| | |
|---|---|
| CM | Common mode |
| CMC | Common mode current |
| CMV | Common mode voltage |
| DC | Direct current |
| AC | Alternating current |
| EMI | Electromagnetic interference |
| PWM | Pulse width modulation |
| PV | Photovoltaic |
| VFD | Variable frequency drive |
| *dv/dt* | Change in voltage |
| *di/dt* | Change in current |
| LC | Product of inductance and capacitance |
| SPWM | Sinewave pulse width modulation |
| NPC | Neutral point clamped |
| SVPWM | Space vector pulse width modulation |
| PDPWM | Phase disposition PWM |
| SS | Spread spectrum |
| $V_A$, $V_B$, $V_C$ | AC voltage of each leg |
| $V_{Ref}$ | Voltage of reference modulating signal |
| $V_{Am}$, $V_{Bm}$, $V_{Cm}$ | Voltage of reference modulating signal for each leg |
| $V_m$ | Peak value of output voltage |
| $V_{m3}$ | Peak value of third harmonic of output voltage |
| $f(wt)$ | Function of reference waveform of the method third harmonics injection |
| $V_{dc}$ | DC input voltage |
| $R_{CM1}$, $R_{CM2}$ | Damping resistor |
| $L_{CM1}$, $L_{CM2}$ | Chokes |
| $C_{CM1}$, $C_{CM2}$ | Capacitor |
| $L_{CM}$, $C_{CM}$ | Common mode equivalent inductance and capacitor |
| $f_o$ | Common mode resonant frequency |

## Appendix A

**Table A1.** Specifications of the system parameters.

| Name of the Component | Rating |
|---|---|
| DC link voltage | 560 V |
| DC link capacitor | 2200 μF |
| Filter inductance | 450 mH |
| Filter capacitance | 11.6 μF |
| Rated phase voltage | 230 V |
| Frequency | 50 Hz |
| **Grid Parameters** | |
| Grid voltage and frequency | 230 V, 50 Hz |
| Carrier frequency | 20 kHz |

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